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Single Event Upsets in Gallium Arsenide Dynamic Logic

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Abstract

The advantages and disadvantages of using gallium arsenide (GaAs) dynamic logic in computers and digital systems are briefly discussed, especially with respect to space applications. A short introduction to the topology and operation of GaAs Two-Phase Dynamic FET Logic (TDFL) circuits is presented. Experiments for testing the SEU sensitivity of GaAs TDFL, using a laser to create charge collection events, are described. Results are used to estimate the heavy-ion, soft error rate for TDFL in a spacecraft in geosynchronous orbit, and the dependence of the SEU sensitivity on clock frequency, clock voltage, and clock phase. Analysis of the data includes a comparison between the SEU sensitivities of TDFL and the more common static form of GaAs logic, Directly Coupled FET Logic (DCFL). This is the first reported SEU testing of GaAs dynamic logic.

I. INTRODUCTION

Gallium Arsenide (GaAs) digital logic is now the technology of choice for high-performance, terrestrial-based computers and digital systems [1]. GaAs logic and memory devices offer the shortest logic delays and the fastest memory access times of any logic family in any fabrication technology. When compared to silicon emitter-coupled logic [2], GaAs offers higher speed, lower power, higher logic function density, and often reduced cost. Although CMOS logic is denser and consumes less power than GaAs logic, if current CMOS clock rates are extrapolated into the 500 MHz to 1.5 GHz region where GaAs logic is capable of operating, the calculated power consumption of CMOS exceeds that of existing GaAs logic. Furthermore, research has shown that GaAs digital ICs suffer only minimal permanent damage from exposure to high total doses of radiation [3, 4]. These characteristics would tend to make GaAs logic ideal for use in high-performance, space-based computers and digital systems. However, the most common GaAs logic circuits are prone to single event upsets (SEUs) in high radiation environments [4, 5]. They also consume a fairly large amount of static power, which causes total power consumption to be high even at low clock rates.

Recent advances in GaAs logic circuit development have produced several different low-power/high-speed logic families, including Two-Phase Dynamic FET Logic (TDFL) [6], GaAs Dynamic Logic [7], GaAs Domino Logic [8], and GaAs Capacitively Coupled Domino Logic (CCDL) [9]. All of these logic families provide high switching speeds and reduced power consumption, relative to static GaAs logic families such as Directly Coupled FET Logic (DCFL), Buffered FET logic (BFL), and Source Coupled FET logic (SCFL) [7]. All of these newer types of GaAs logic utilize dynamic operating principles in some form or another. That is, they require a clock signal in order to evaluate and propagate logic values, and at some point in time, the logic value is stored as a charge on a capacitance. The advantage of dynamic logic is a savings in power, and sometimes a decrease in gate complexity as well, which can result in increased logic function density. However, until now, none of the various different forms of GaAs dynamic logic have been tested to determine their susceptibility to single event upsets (SEUs). Conventional wisdom has been that the dynamic circuits are more susceptible to SEUs than GaAs static logic.

II. GaAs TWO-PHASE DYNAMIC FET LOGIC

This paper describes SEU testing on a TDFL test IC. The circuit topology and operation of TDFL is significantly different from the more common forms of GaAs logic such as DCFL. This section presents a brief introduction to TDFL. For more information, the reader is referred to [6] and [10].

For comparison purposes, Figure 1 is a schematic diagram of a typical DCFL inverter. The input to the logic gate is connected to an EFET, and a DFET serves as an active load. When the input to the gate is less than V_T of the EFET, the EFET is cut off and the DFET load pulls the output node high. When the input to the gate is significantly greater than V_T of the EFET, source-drain current flows through the EFET, and the output voltage drops to a value near ground potential. The process used to fabricate the test IC for the described research produces EFETs

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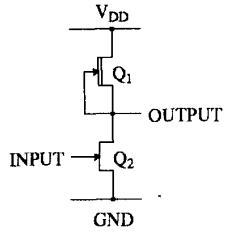

Figure 1: Typical DCFL inverter schematic diagram.

with a V_T of approximately 0.23 V and DFETs with a V_T of approximately -0.87 V.

Figure 2 is a schematic diagram of a typical TDFL inverter. The clock signals ϕ_1 and ϕ_2 are 180° out of phase and are non-overlapping, as shown in Figure 3. Referring to Figure 2, when ϕ_1 goes high, Q_2 turns on and precharges the output node to a logic 1. Simultaneously, Q_1 turns on and the gate of Q_4 is allowed to charge or discharge, depending on whether the input to the gate is a logic 1 or 0, respectively. When ϕ_1 turns off, the output node is isolated. The output value stays constant because of the charge stored on the output node capacitor. To reduce the implementation layout area, the output node capacitor is implemented with a reverse biased diode. The gate of Q_4 is also isolated when ϕ_1 goes low. The voltage on the gate of Q_4 stays nearly constant because of the gate capacitance.

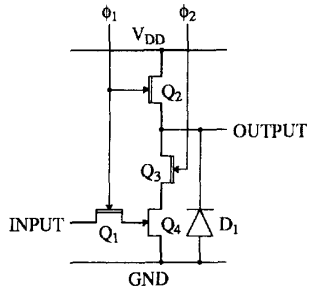

Figure 2: Typical TDFL inverter schematic diagram.

When ϕ_2 goes high, Q_3 turns on, and the logic gate goes into the evaluation phase. If the gate of Q_4 is low, Q_4 will be cut off, a small amount of charge will flow from the output node, through Q_3 to the drain of Q_4, and the voltage on the output node will only drop a small amount. The output logic value will remain a logic 1, assuming appropriate sizing of the output node capacitor. However, if the gate of Q_4 is high, Q_4 will be on, and current will flow through Q_3 and Q_4 to ground, discharging the output node to near ground potential. The output value of the gate is only valid during the evaluation phase when ϕ_2 is high. Cascaded stages of TDFL must have their ϕ_1 and ϕ_2 clock signals reversed so that cascaded stages of logic always evaluate 180° out of phase, as shown in Figure 4.

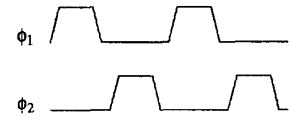

Figure 3: ϕ_1 and ϕ_2 non-overlapping clocks.

III. SEU TESTING AND EQUIPMENT

It can be seen from Figure 2 that if any single transistor or the diode capacitor experiences a charge collection event, then the output logic value of the gate can be affected. Electrons are attracted toward regions of positive potential such as the drain of a transistor, and holes are attracted toward regions of negative potential such as the source of a transistor. For example, if Q_2 in Figure 2 experiences a charge collection event when ϕ_1 is low, and if the output value is a logic 0, then negative charge will collect at the drain of Q_2 and flow to V_{DD}, and positive charge will collect at the source of Q_2 and flow to the output node. If the charge is great enough, the output logic value of the gate will change from 0 to 1. Therefore, in order to determine the soft error rate for an entire gate, it is necessary to determine the SEU sensitivity of each active device in the gate.

To measure the SEU sensitivity of each active device in the logic gate, the circuit of Figure 4 was used. The circuit consists of four TDFL inverter stages cascaded together. Not shown in Figure 4 is a 50 Ω output driver connected to the last stage of the inverter chain. The test circuit was fabricated at Vitesse Semiconductor using their HGaAsII E/D MESFET process. The test IC was packaged in a high-performance, 28-pin, leaded ceramic flat pack. The lid was left unsealed to provide for easy removal of the lid and access to the chip with laser light. Figure 5 is a photograph of the test IC with the lid removed. The IC is shown mounted in the test fixture, ready for SEU testing with the laser.

To obtain an indication of the SEU sensitivity of the various different active devices in the circuit, a single test IC was operated with $V_{DD} = +2.0$ V and $GND = 0.0$ V. The input was held low (0.0 V). The ϕ_1 and ϕ_2 clock signals were generated with a Colby Instruments PG-1000A pulse generator. Clock voltages of -1.0 V for logic 0 and $+0.25$ V for logic 1 were used, except where indicated otherwise. These values are typical for GaAs TDFL. The clock frequency was 67.67 MHz except where otherwise noted. This was very near the minimum speed of operation of 50 MHz for the circuit under test. 67.67 MHz was chosen because it provided an adequate operating margin above the minimum operating frequency, and because the signal generator was able to provide stable and noise-free clock signals at this frequency. The circuit could not be tested at the maximum frequency of operation of approximately 1.5 GHz because the maximum frequency of the signal generator is only 1029 MHz. The output of the test circuit

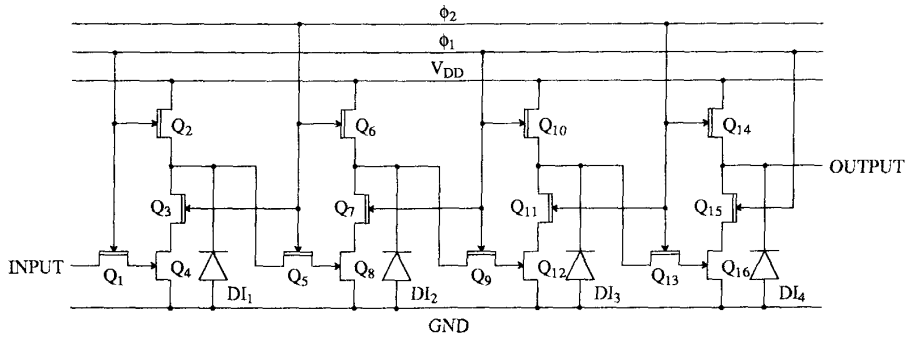

Figure 4: TDFL circuit for measuring SEU sensitivity.

was monitored with a Tektronix 11801A digitizing sampling oscilloscope, which has a bandwidth of 18 GHz. The minimum SEU energy thresholds given in later sections of this paper refer to the minimum laser energy required to produce a positive-going pulse on the oscilloscope at the output of the test circuit.

Charge-collection events were induced with the output of a modelocked, cavity-dumped, dye laser centered at 620 nm (2.0 eV). The use of pulsed lasers in charge collection experiments for testing the SEU characteristics of devices and circuits is well documented [11, 12, 13, 14], as are the limitations of the method [15, 16, 17]. The pulse repetition rate of the laser used in the experiments described here was 12.198 KHz, with a pulse duration of 1 ps. Spot size was approximately 1 μm in diameter.

From the laser energies measured during the experiments, the amount of charge created in the semiconductor from the laser pulse can be calculated. Irradiation with 620 nm light corresponds to an absorption coefficient $\alpha = 5 \times 10^4/\text{cm}$, and the 1/e absorption depth is approximately 0.2 μm below the surface. It is assumed that each photon absorbed by the GaAs creates a single electron-hole pair, and any remnant photon energy is converted to phonons (heat). It is assumed that approximately 67% of the incident light is absorbed in the GaAs. The rest is reflected at the SiO_2 and SiO_2/GaAs boundaries.

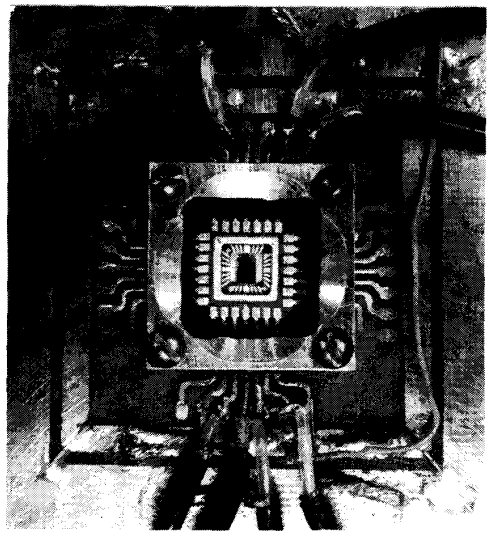

Figure 5: GaAs TDFL test IC, with lid removed, and test fixture.

Figure 6 is a plot of the layout of one of the inverters in the circuit shown in Figure 4. Figure 7 is a legend for the stipple patterns used in Figure 6. Layout dimensions can be determined by comparison with the gate length of the MESFETs shown, which is 1.2 μm. Gate width is 4 μm for all MESFETs except Q_1 which has a 2 μm gate width. The diode size is 2.4 μm x 2.8 μm. The device sizes and layout shown are typical for GaAs TDFL ICs. Marked on the plot in Figure 6 are the target locations for the laser. The locations are labeled A through J. Locations A1 through J1 refer to the first inverter stage, and locations A2 through J2 refer to the second inverter stage. Table 1 describes the locations of the different laser target points.

IV. RESULTS AND DISCUSSION

Extensive work has previously documented the charge collection properties of the GaAs MESFET [15], and data has been presented on the sensitivity of GaAs SRAMs [5]. However, with dynamic logic, several more variables exist than when working with static logic or individual transistors. The experiments described here can be divided into two categories, synchronized and unsynchronized, referring to whether or not the clock of the dynamic logic circuit was synchronized with the laser pulses. Unsynchronized experiments include tests to determine the effect on SEU sensitivity of the location of the SEU on the substrate, the input logic value, the clock frequency, the clock low voltage, and the clock high voltage. Synchronized experiments include tests to determine the SEU sensitivity as a function of the phase relationship between the clock and the laser pulse for different SEU locations and for different input logic values.

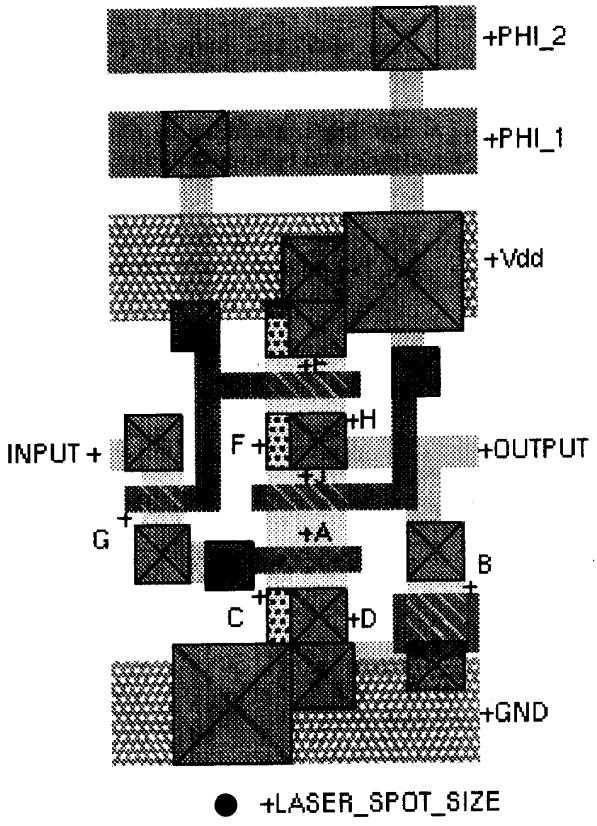

Figure 6: Plot of layout of TDFL inverter showing laser target locations.

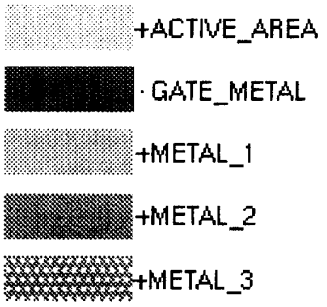

Figure 7: Legend for stipple patterns for Figure 6.

Table 1: Laser Target Locations.

Designator	Laser Target Location
A1	drain of Q_4 and source of Q_3
A2	drain of Q_8 and source of Q_7
B1	on substrate, to upper right of DI_1
B2	on substrate, to upper right of DI_2
C1	on substrate, to left of source of Q_4
C2	on substrate, to left of source of Q_8
D1	on substrate, to right of source of Q_4
D2	on substrate, to right of source of Q_8
E1	on drain of Q_2
E2	on drain of Q_6
F1	on substrate, to left of source of Q_2 and drain of Q_3
F2	on substrate, to left of source of Q_6 and drain of Q_7
G1	on substrate, to left of drain of Q_1
G2	on substrate, to left of drain of Q_5
H1	on substrate, to right of source of Q_2 and drain of Q_3
H2	on substrate, to right of source of Q_6 and drain of Q_7
J1	on drain of Q_3
J2	on drain of Q_7

A. Unsynchronized Experiments

Table 2 lists the minimum laser energy required to induce SEUs at the test circuit output for the different target locations on the single chip that was tested. Two inverter stages were tested to determine if an inverter with a logic 0 input would have a different SEU sensitivity than an inverter with a logic 1 input. It can be seen from Table 2 that some areas of the circuit are more sensitive to SEUs with a logic 0 input, some are more sensitive with a logic 1 input, and for some areas of the circuit the value of the input signal makes little difference. Because the laser was free running, it can be assumed that the most sensitive portion of the clock period was measured at each location. The data provides a worst-case approximation of the soft error rate because the error-rate calculations assume each node is vulnerable 100% of the time. Upset locations ranged in sensitivity from 30 fJ to 1.75 pJ.

Table 2 indicates the sensitive surface area, estimated from layout parameters, for each of the active devices in the test circuit. This information, together with the deposited charge data, can be used to estimate the heavy-ion soft error rate for a TDFL IC in a spacecraft in a geosynchronous orbit. The method used is described in detail in [18]. The charge collection depth is assumed to be 2.2 μm [4]. Table 2 lists the soft error rate that can be attributed to each of the devices in the circuit. The soft error rate for an entire inverter operating at 67.67 MHz can be obtained by summing the soft error rates for each area in the circuit. The result is 4.939×10^{-4} soft errors per day for an inverter with a logic 0 on the input and a logic 1 on the output, and 5.289×10^{-4} soft errors per day for an inverter with a logic 1 on the input and a logic 0 on the output.

It is not unreasonable to compare the soft error rate of a dynamic inverter with the soft error rate of a static memory cell because a dynamic inverter is, essentially, a single-bit storage element. For DCFL static memory cells fabricated with the Vitesse E/D HGaAsII process, the same process used to fabricate the TDFL test circuits, and using the same approximate device sizes and physical geometries as the TDFL test circuits, soft error rates of 1.2×10^{-3} to 2.1×10^{-3} errors per bit-day have been measured [5]. The soft error rates for the TDFL inverters are similar to the soft error rate for the DCFL static memory cells fabricated with the same process, although the soft error rate for the DCFL static memory cells was measured using protons and

heavy ions instead of a laser. Agreement within an order of magnitude should be expected if the estimate of sensitive surface area is reasonable.

Table 2: Minimum SEU Energy Thresholds Observed, Collected Charge, Sensitive Areas, and Soft Error Rates vs. Laser Target Location. Clock Frequency is 67.67 MHz.

Location	Energy (pJ)	Charge (pC)	Sensitive Area (μm^2)	Soft Error Rate (Errors/Day)
A1	0.038	0.013	24.64	2.557×10^{-4}
B1	0.058	0.019	21.12	9.289×10^{-5}
C1	0.090	0.030	8.96	1.614×10^{-5}
D1	0.055	0.018	11.20	5.364×10^{-5}
E1	0.113	0.038	15.68	1.798×10^{-5}
F1	0.100	0.033	6.72	9.767×10^{-6}
G1	0.163	0.054	15.84	8.743×10^{-6}
H1	0.150	0.050	8.96	5.811×10^{-6}
J1	0.063	0.021	8.96	3.326×10^{-5}
A2	1.500	0.501	24.64	1.594×10^{-7}
B2	0.030	0.010	21.12	3.424×10^{-4}
C2	0.045	0.015	8.96	6.457×10^{-5}
D2	0.055	0.018	11.20	5.364×10^{-5}
E2	0.300	0.100	15.68	2.537×10^{-6}
F2	0.120	0.040	6.72	6.776×10^{-6}
G2	0.063	0.021	15.84	5.880×10^{-5}
H2	1.750	0.584	8.96	4.257×10^{-8}
J2	Could not induce a SEU	—	8.96	—

The operating characteristics of dynamic logic are sometimes dependent on the frequency of the clock. Therefore, an experiment was conducted with the same test chip to determine if the SEU sensitivity is a function of the clock frequency. For this series of tests, the laser was focussed at location A1, the drain of Q_4 and the source of Q_3 in the first inverter stage. This location was selected because, as can be seen from Table 2, it is a fairly sensitive area. The clock frequency was varied between 49.9 MHz and 1029 MHz. Clock voltages of -1.0 V for logic 0 and $+0.375$ V for logic 1 were used. Table 3 lists the minimum laser energy required to induce a SEU at the output of the test circuit for the various different clock frequencies. Figure 8 plots the laser energy as a function of the clock frequency. There does not appear to be a systematic dependence of the SEU threshold on clock frequency. It should be noted that the interconnect stubs between the clock line terminators and the chip under test cause some reflections, and therefore standing waves, on the clock lines. When the clock frequency changes, the locations of the standing waves along the clock lines also change. Therefore, the actual clock voltage present at the chip changes as the clock frequency changes. This is why the clock high voltage was increased from 0.25 V to 0.375 V for this experiment. It was desired to keep the on-chip clock high voltage at 0.25 V or greater. It will be seen later that the SEU sensitivity of GaAs TDFL circuits is a function of the clock voltage. This may explain the scatter seen in Figure 8. Based on previous experience [13], it was expected that the SEU sensitivity of the drain of Q_4 and source of Q_3 would be frequency dependent. A gradual increase in the upset rate with increasing frequency was expected. For a complete understanding of how TDFL is effected by charge collection events, all nodes need to be investigated and the clock reflection problem analyzed.

Table 3: Minimum SEU Energy Thresholds Observed at Different Frequencies. Laser Target Location is A1 (drain of Q_4 and source of Q_3).

Frequency (MHz)	Energy (pJ)	Frequency (MHz)	Energy (pJ)
49.9	0.020	506.7	0.035
125.0	0.035	701.2	0.045
241.0	0.028	865.0	0.020
250.0	0.058	1000.0	0.033
375.0	0.015	1029.0	0.050

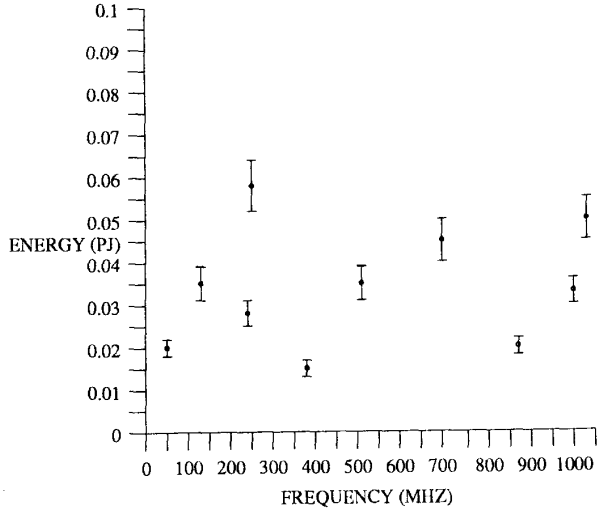

Figure 8: Minimum SEU energy thresholds observed vs. clock frequency. Laser target location is A1 (drain of Q_4 and source of Q_3).

The operating characteristics of dynamic logic can also be dependent on clock voltage. This is especially true when the logic is implemented with MESFETs because the gate of a MESFET is not insulated from the channel, and current can flow from the gate to the source if V_{GS} exceeds $V_{GS(ON)}$. $V_{GS(ON)}$ is between 0.55 V and 0.7 V for the MESFETs in the test IC. For the clock voltage experiments, the clock frequency was held constant at 67.67 MHz. The laser was again focussed at location A1, the drain of Q_4 and the source of Q_3 in the first inverter stage. For the first part of the clock-voltage experiment, the clock high voltage was held constant at 0.0 V, and the clock low

voltage was varied between −1.75 V and −1.0 V. This relatively low value for the clock high voltage was chosen to ensure that MESFET gates would not conduct and interfere with the clock low voltage experiment. The results of this series of tests are given in Table 4 and Figure 9. The clock low voltage was not expected to have a significant effect on the SEU sensitivity, unless pass transistors Q_1 or Q_5 could not be turned off. This did not appear to be a problem, as indicated by the data in Table 4 and Figure 9.

Table 4: Minimum SEU Energy Thresholds Observed at Different Clock Low Voltages. Laser Target Location is A1 (drain of Q_4 and source of Q_3). Clock Frequency is 67.67 MHz.

Voltage	Energy (pJ)	Voltage	Energy (pJ)
−1.75	0.018	−1.25	0.023
−1.50	0.015	−1.00	0.025

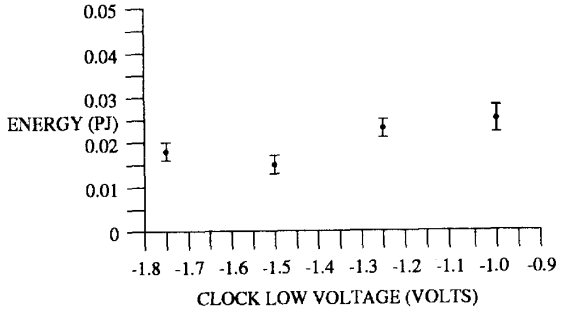

Figure 9: Minimum SEU energy thresholds observed vs. clock low voltage. Laser target location is A1 (drain of Q_4 and source of Q_3). Clock frequency is 66.67 MHz.

For the second part of the clock voltage experiment, the clock low voltage was held constant at −1.0 V, and the clock high voltage was varied between −0.5 V and +0.25 V. The results of this series of tests are given in Table 5 and Figure 10. It is clear from Figure 10 that there is a definite relationship between the SEU sensitivity of TDFL and the clock high voltage. The SEU threshold goes down as the clock high voltage goes up. The reason for this can be determined by referring to the schematic diagram of the test circuit in Figure 4. For this experiment, the laser was again focussed at location A1, the drain of Q_4 and the source of Q_3 in the first inverter stage. The SEU is caused by positive charge collecting on the gate of Q_4, which turns Q_4 on. The gate of Q_4 is normally at a potential of 0 volts and Q_4 is normally off. The SEU threshold is higher when the clock high voltage is lower because only the charge collected at the gate of Q_4 is available to turn Q_4 on. When the clock high voltage is higher (more positive), the collected charge sums with the charge leaking onto the gate of Q_4 from the gate of Q_1. The results of this experiment indicate that the SEU tolerance of GaAs TDFL can be optimized by judiciously selecting the clock voltage levels.

B. Synchronized Experiments

It was hypothesized that the SEU sensitivity of TDFL would be influenced by the phase relationship between the clock signals and the charge collection event. To test this hypothesis, the arrival of the laser pulse was synchronized with the ϕ_1 and ϕ_2 clock signals. The repetition rate and phase of the laser pulses was held constant at 12.198 KHz, and the clock signal of 49.99 MHz was derived from the mode-locker oscillator. Clock voltages were −1.0 V for logic 0 and +0.25 V for logic 1. By utilizing calibrated delays of 0.00 ns, 4.80 ns, 9.40 ns, 14.20 ns, and 19.05 ns in the clock cables, charge collection events were synchronized with the test circuit at five different phases of the clock waveform, as is illustrated in Figure 11.

Table 5: Minimum SEU Energy Thresholds Observed at Different Clock High Voltages. Laser Target Location is A1 (drain of Q_4 and source of Q_3). Clock Frequency is 67.67 MHz.

Voltage	Energy (pJ)	Voltage	Energy (pJ)
−0.50	0.040	0.00	0.030
−0.38	0.038	+0.13	0.026
−0.25	0.044	+0.25	0.019

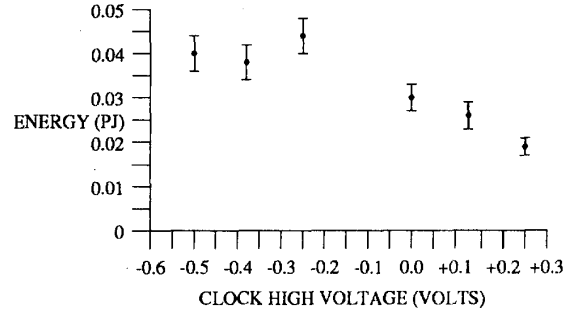

Figure 10: Minimum SEU energy thresholds observed vs. clock high voltage. Laser target location is A1 (drain of Q_4 and source of Q_3). Clock frequency is 67.67 MHz.

The effects of synchronizing the laser pulse to either the precharge or the evaluation half of the clock cycle were measured at two different locations in each of two consecutive inverters. In the first inverter, the locations were E1, the drain of Q_2, and J1, the drain of Q_3. In the second inverter, the locations were E2, the drain of Q_6, and J2, the drain of Q_7. These locations were selected based on the assumption that they would have the most affect on the operation of the clock. Note that the first inverter has an input of logic 0 (0.0 V) and an output of logic 1 (+0.6 V), and the second inverter has an input of logic 1 (+0.6 V) and an output of logic 0 (0.0 V).

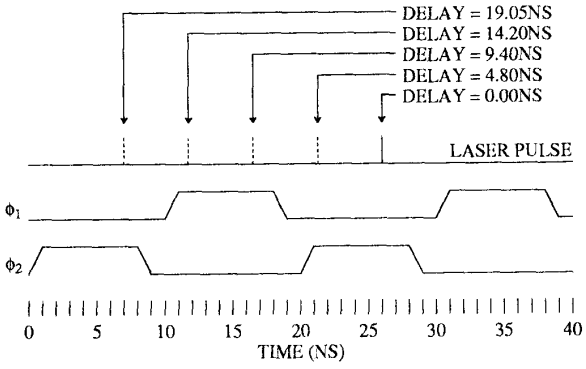

Figure 11: Laser pulse timing with respect to clock phase.

It is clear from examining Table 5 and Figure 12 that the phase of the clock has a significant effect on the SEU sensitivity of TDFL. Referring to Figures 4, 6, and 12, a charge collection event at location E1 or J1 causes negative charge to collect on the source of Q_2 or the drain of Q_3, respectively, because this node of the circuit is initially positively charged and thus attracts the negatively charged electrons. When ϕ_1 is high, Q_2 is on, and some of the collected charge flows through Q_2 to V_{DD}. Therefore, more charge must be collected to cause an upset when Q_2 is on than when Q_2 is off, which is consistent with the data in Table 6 and Figure 12. With clock delays of 0.00 ns, 4.80 ns, and 19.05 ns, the laser pulse occurs when ϕ_1 is low, and the SEU thresholds for locations E1 and J1 are lower than for the case when ϕ_1 is high, which corresponds to clock delays of 9.40 ns and 14.20 ns. A charge collection event at location E2 or J2 causes positive charge to collect on the source of Q_6 or the drain of Q_7, respectively, because this node of the circuit is initially negatively charged (relatively) and thus attracts the positively charged holes. When ϕ_1 is high, Q_7 and Q_8 are on, and some of the collected charge conducts through Q_7 and Q_8 to ground. More charge must be collected to cause an upset when Q_7 and Q_8 are on than when they are off. Therefore, the SEU threshold is higher if the event occurs when ϕ_1 is high, which is consistent with the data in Table 6 and Figure 12. With clock delays of 0.00 ns, 4.80 ns, and 19.05 ns, the laser pulse occurs when ϕ_1 is low, and the SEU thresholds for locations E2 and J2 are significantly lower than for the case when ϕ_1 is high, which corresponds to clock delays of 9.40 ns and 14.20 ns. It is interesting to note that the first inverter is more sensitive to SEUs that the second inverter. In retrospect, it would have been interesting to switch the input signal to the first inverter from a logic 0 to a logic 1. If this were done, then one would expect the circuit to be more sensitive to SEUs when ϕ_1 is high. This is the first reported SEU testing of GaAs dynamic logic with the clock signal of the circuit under test synchronized to the energy source used to induce SEUs.

Table 6: Minimum SEU Energy Thresholds Observed at Four Different Target Locations at Five Different Clock Phases. Clock Frequency is 49.99 MHz.

Inverter Input = 0 Output = 1			Inverter Input = 1 Output = 0		
Location	Delay (nS)	Energy (pJ)	Location	Delay (nS)	Energy (pJ)
E1	0.00	0.150	E2	0.00	1.50
E1	4.80	0.175	E2	4.80	1.75
E1	9.40	5.00	E2	9.40	11.0
E1	14.20	7.50	E2	14.20	29.0
E1	19.05	0.150	E2	19.05	2.15
J1	0.00	0.045	J2	0.00	1.25
J1	4.80	0.058	J2	4.80	1.75
J1	9.40	3.50	J2	9.40	7.50
J1	14.20	3.00	J2	1420	11.0
J1	19.05	0.048	J2	19.05	2.00

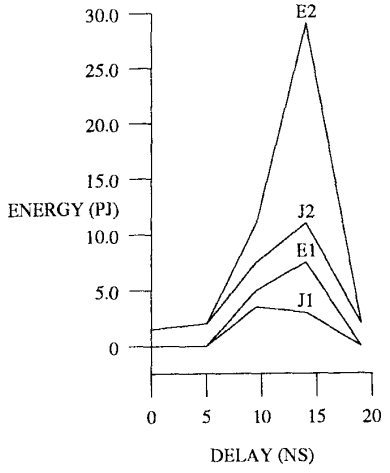

Figure 12: Minimum SEU energy thresholds observed for four different target locations at five different clock phases. Clock frequency is 49.99 MHz.

V. CONCLUSIONS

Although SEU testing with a laser is not a substitute for actual heavy ion testing, the ability to synchronize the laser pulse to the test circuit provides important information to understanding the nature of single event upsets in high speed combinational logic. The results presented in this paper show that examining the SEU sensitivity of high speed digital switching circuits requires analysis in regards to timing and phase considerations and clock levels when examining non-insulated gate FETs. With heavy ion testing, ion displacement damage and the inability to control the timing and phase of charge collection events makes it extremely difficult to conduct such studies.

The topology and operation of GaAs Two-Phase Dynamic FET Logic (TDFL) circuits have been presented.

The advantages and disadvantages of using GaAs dynamic logic in computers and digital systems, especially with respect to space applications, have been discussed. The use of GaAs dynamic logic can significantly increase the performance of a digital system, without the high power consumption that is normally associated with high-speed logic. The results of SEU testing of the GaAs TDFL test IC, using a laser to create charge collection events, have been presented. The SEU sensitivity of TDFL is significantly effected by the clock high voltage and by the phase relationship between the clock and the charge collection event. The SEU sensitivity of GaAs dynamic logic can be optimized by judiciously choosing the clock voltages. The experiments described indicate that DCFL, the more common form of GaAs static logic, and TDFL have similar SEU thresholds. The relatively high SEU sensitivity of both GaAs static and dynamic logic, compared to complementary SOI technology, indicates that further research is necessary in the areas of device physics, fabrication, and circuits.

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