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SEU Design Considerations for MESFETs on LT GaAs

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Abstract

Computer simulation results are reported on transistor design and single-event charge collection modeling of metal-semiconductor field effect transistors (MESFETs) fabricated in the Vitesse H-GaAsIII® process on Low Temperature grown (LT) GaAs epitaxial layers. Tradeoffs in Single Event Upset (SEU) immunity and transistor design are discussed. Effects due to active loads and diffusion barriers are examined.

I. INTRODUCTION

A. *Background*

GaAs MESFET digital logic has shown some of the highest sensitivities to single event effects (SEE). To understand these high sensitivities, GaAs MESFETs have been studied using 2-D charge transport codes to understand charge collection mechanisms [1].

Measurements have been performed on discrete devices for comparison to simulations [2]. Results suggest several charge collection mechanisms (bipolar, back-channel modulation) are responsible for measurements of enhanced charge collection. These earlier efforts led to proposing buffer layers to improve the recombination of carriers below the GaAs FET during charge collection events. Low-temperature grown GaAs (LT GaAs), with its three order-of-magnitude shorter carrier lifetime than normally-grown GaAs was suggested as a candidate to harden GaAs ICs [3]. Charge collection simulations using LT GaAs as a buffer suggest a significant reduction in charge collection can be attained. Recently, others have investigated the effects of buffer thickness on charge collection [4]. The feasibility of LT GaAs buffers to reduce SEU has been demonstrated in other GaAs FET processes [5],[6] but not in a MESFET technology.

Implementing LT GaAs buffers in implanted bulk GaAs MESFET processes is challenging because of the manufacturing issues. However, if VLSI circuits can be fabricated in a GaAs MESFET process on LT GaAs, it would be possible to produce 500 MHz (or higher), rad-hard, Application Specific ICs (ASICs) by just substituting bulk wafers with epitaxial wafers utilizing LT GaAs buffers.

The Naval Postgraduate School, Naval Research Laboratory and Vitesse Semiconductor are collaborating to design Molecular Beam Epitaxial (MBE) wafers incorporating LT GaAs buffers to produce SEU-immune digital GaAs ICs. The particular challenge is to utilize the same implants and process steps in the standard Vitesse H-GaAsIII® process without degrading performance. The implant activations and background impurities are considerably different between the two wafer types. However, this approach allows previous Commercial-Off-The-Shelf (COTS) designs to be used without the need for design rule changes or modification of existing mask sets.

To achieve this goal, several tasks were performed: a) characterization and modeling the standard Vitesse Enhancement mode FETs (E-FETs) and Depletion mode FETs (D-FETs), b) design and modeling of MBE-based implanted FETs equivalent to the standard process, c) examination of the influence of the LT GaAs buffer structure on transistor properties, and d) examination the charge collection properties of both the standard and MBE structures.

II. VITESSE HGaAs III MESFET PROCESS

The Vitesse process includes E-FET and D-FET MESFETs arranged in direct coupled FET logic (DCFL) circuits. Implants form the channel and ohmic regions. The E-FET utilizes a shallow n-implant to provide a normally off device, whereas the D-FET channel is formed from a deeper n-channel implant and is normally on. Schottky gate metal defines the length of the transistor. Additionally a deep buried p-implant over the complete bulk wafer prior to processing is provided as a channel stop to the bottom of the D-FETs and E-FETs.

LT GaAs is realized with molecular beam epitaxy (MBE). To implement LT GaAs buffer layers in the Vitesse process, a high-quality crystalline GaAs epitaxy must be implemented above the buffer to accommodate channel implants. This higher background requires special consideration when designing transistors which utilize low energy and low fluence implants (E-FETs). MBE-based material is normally 2 or 3 orders of magnitude higher in unintentional background impurities than bulk GaAs. The structure of the reengineered E-FET is shown in Figure 1.

Material and device characterization was performed to help model the standard E-FET and D-FET. Hall, capacitance vs. voltage, current vs. voltage, and gate measurements were performed on specifically designed process monitors. Doping profiles, mobility values, and barrier height information were

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incorporated into the ATLAS® code to develop models that correlate with current and voltage measurements.

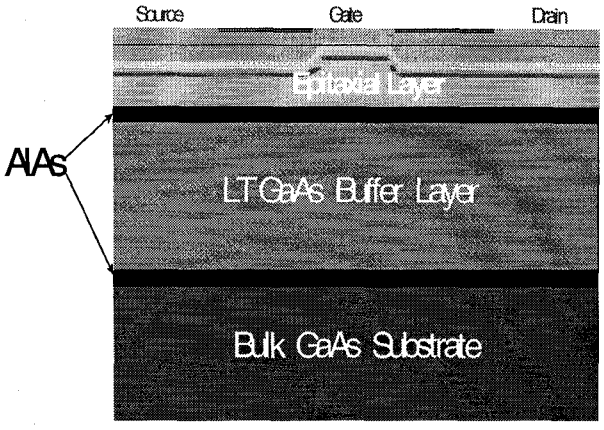

Figure 1: Structure of the Vitesse MESFET implemented in a MBE epitaxial GaAs wafer with a low-temperature grown GaAs buffer layer.

Fabrication had been performed on standard bulk wafers, and a combination of MBE wafers with and without LT GaAs buffers. Additionally, some MBE LT GaAs wafers included diffusion barriers. Table 1 summarizes the various wafer types characterized for devices and material, where several wafers of each type were grown, except wafer type 4. All wafers were studied for implant activation by comparing threshold voltages and resistivity. The MBE epitaxial wafers were supplied by commercial vendors, Picogiga and Quantum Epitaxial Designs.

Table 1
Wafer structures fabricated.

Wafer type	Material	LT GaAs	diffusion barriers	Vendor
1	bulk			na
2	MBE	-	-	QED
3	MBE	-	-	Picogiga
4	MBE	2000A	100A AlAs	Picogiga
5	MBE	2500A	-	QED

Characterization of the MBE wafers (2 and 3) showed increased threshold voltages for both the E-FET and D-FET. Implant activation was reduced in the MBE material. Devices fabricated in wafer types 2 and 3 provided very similar shifts in thresholds for both transistors. Wafer 4 showed less shift in E-FET threshold voltages (250mV to 450mV), while both 4 and 5 showed large changes in D-FET threshold voltages (-800mV to -400mV). Clearly, the epitaxy and the vicinity of the LT GaAs buffer affected the FET thresholds. The E-FET implant utilized lower fluences and was more susceptible to background defects or impurities. However, the larger D-FET implant was susceptible to the nearby LT GaAs buffer. All devices were affected by reduced activation.

III. LT GaAs Buffer

The primary purpose for low-temperature growth is to increase the As concentration in the GaAs crystal. Excess As is introduced interstitially due to high overpressure in the low temperature growth. Annealing of this as-grown (as grown without annealing) material allows As to precipitate, occupy antisites, or to induce Ga vacancies. The presence of the As precipitate is an indication that defects exist. The As antisite and Ga vacancy defects are responsible for the large capture cross sections and short carrier lifetimes. Arsenic is confined with diffusion barriers to keep the excess As concentration high and to prevent the mobile As from entering the FET's channel region [7].

This work characterized devices without diffusion barriers (wafer type 5) and showed considerable gate leakage in the MESFET. This is attributed to an increase in defects in the GaAs epitaxy, possibly from the diffusion of As from the buffer region. To contain As within the buffer region, AlAs diffusion barriers were fabricated on wafer 4. The Transmission Electron Microscopy (TEM) image of wafer type 4, shown in Figure 2, clearly shows arsenic precipitates in the LT GaAs buffer layer confined within the AlAs diffusion barriers.

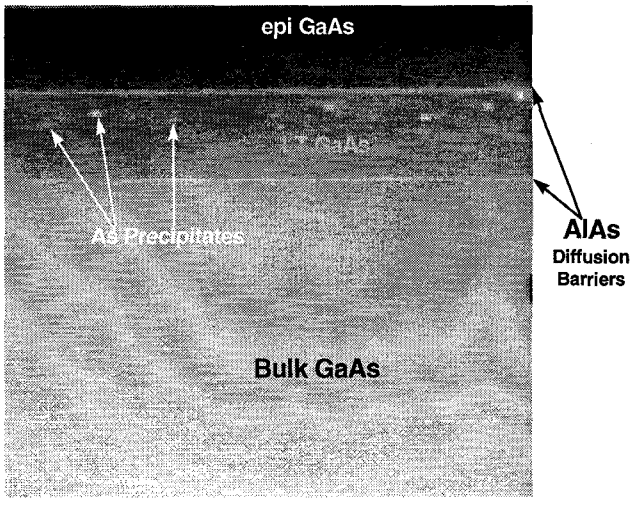

Figure 2: A TEM image of a GaAs epitaxial wafer utilizing an LT GaAs buffer. The region between the two thin diffusion barrier lines is the LT GaAs buffer. Notice the precipitates in the LT GaAs buffer.

The role of the defect lifetime is critical to SEU hardening. However, the LT GaAs buffer does not appear neutral to the transistor. LT GaAs normally appears slightly p-type and is capable of introducing threshold shifts. Initially, Shockley-Read-Hall recombination was investigated to model Fermi level changes and capture/emission rates. However, the recombination mechanism in LT GaAs relies on trap-to-trap recombination [8]. Currently, the software cannot

accommodate recombination between two trap centers. Therefore, we chose to use band-to-band recombination with a carrier lifetime of 1 ps and introduced a background p-doping for the current study.

IV. Charge Collection Simulations

Charge collection in the MESFET was analyzed for several cases:

a) discrete device without an active load,

b) E-FET with resistor load,

c) E-FET with D-FET load, and

d) E-FET with LT GaAs buffer and D-FET load.

To best understand the upset mechanisms in conventional DCFL logic, it was decided to compare charge collection photocurrent between cases where the drain was tied to a supply voltage and where a load equivalent to the actual circuit condition exists. Earlier work had modeled and measured charge collection on discrete devices but not with active loads [1],[2]. The influence between circuit components and internal photocurrents had not been previously determined in the standard MESFET process. The discrete device in this simulation was modeled with the drain biased at 2.0 volts, whereas the DCFL inverter is biased at 2.0 volts on the D-FET load which is connected as shown in Figure 3. Notice that the inverter input is biased off while driving a diode load to simulate the leakage of an inverter load connected to the output.

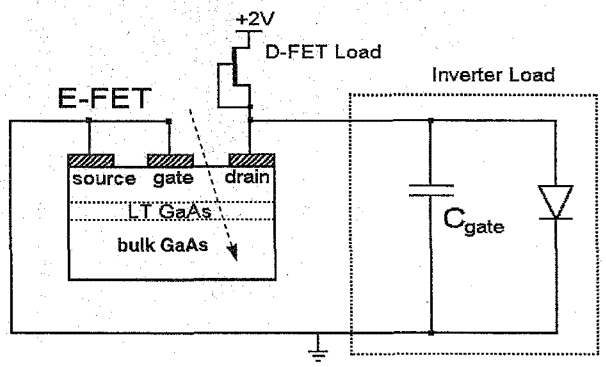

Figure 3: Schematic of the DCFL inverter modeled using Silvaco's MIXEDMODE® and ATLAS®. The E-FET and D-FET make up the inverter circuit.

The GaAs DCFL inverter was modeled with the E-FET in ATLAS® and the D-FET, diode and parasitic capacitance in MIXEDMODE®. MIXEDMODE® is a SPICE simulator that exchanges boundary conditions with the ATLAS® device simulator.

Integrated charge of the active load case is more than 50% below the discrete case. In the active load, the drop in E-FET drain potential is due to a current increase in the D-FET load. Figure 4 shows the interaction between each of the circuit components. The upset mechanism is initiated by the photocurrent in the perturbed E-FET. Normally, the D-FET current and the subsequent gate diode are in equilibrium. Once the E-FET supplies electrons to the drain, the active D-FET load can not increase current and thus the gate capacitance is discharged and the succeeding gate diode turns off. Once the photocurrent dissipates, the D-FET load current begins to exceed the photocurrent magnitude, the capacitor charges via the D-FET load current, and the circuit recovers. The recovery time is related to the magnitude of the photocurrent, active load impedance, off state of the gate diode, and gate capacitance. The existence of a long photocurrent tail is irrelevant if it is below the magnitude of the active load current. In Figure 4, the beginning of the recovery occurs at 32 ps.

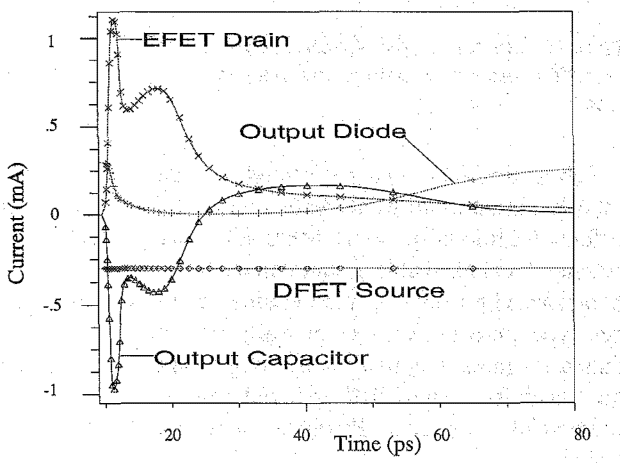

Figure 4: Currents of the E-FET drain, gate diode, capacitor and active load.

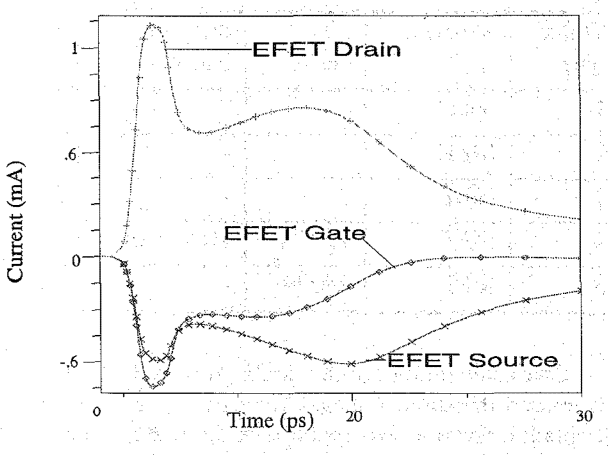

Figure 5: Terminal currents of the E-FET. Figure 6 is taken at the first peak while Figure 7 is from the second peak.

Several mechanisms are occurring, as can be observed in the drain-current trace in Figure 4. Two peaks can clearly be observed. Figure 5 is the terminal currents of the conventional device. The initial peak in Figure 5 shows the gate current (holes) exceeding source current due to a photoconductive

effect at the surface. Because the ionization track has passed through the n+ drain ohmic implant, electron current is at a maximum due to drift. Previous modeling which utilized only uniform-doped regions and different gate-ohmic spacing [1,4] did not show photoconductive effects at the surface of the drain ohmic implant. Figure 6 is a 2-dimensional plot representing the log scale of electron current minus hole current for the first peak in Figure 4. Electrons are removed from the track region and the drain contact due to the high drain potential held by the subsequent gate capacitance.

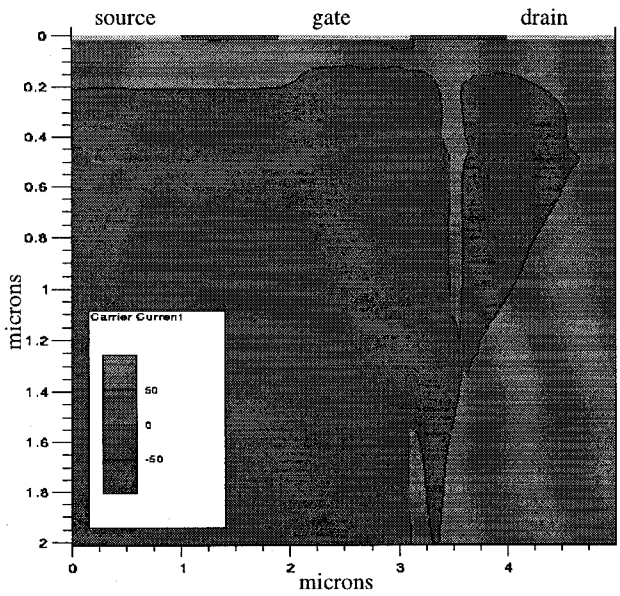

Figure 6: Cross-section of the conventional E-FET current densities. Positive values in the plot are regions of high electron current density, negative values are regions of high hole current density. Notice electron current dominates along the surface of the transistor due to photoconductivity.

Hole current has been observed to come from two sources, the initial particle ionization and the p region beneath the gate. The hole current supplied by this "p-reservoir" below the source implant sets up conditions for a temporary parasitic bipolar action [9]. By the second peak, as shown in Figure 7, the hole current supplied from the "reservoir" toward the gate contact acts as a base current to a parasitic NPN. However, the positive potential of the hole "reservoir" competes to backgate the FET channel to provide source electrons to the drain by modulating the bottom of the FET channel. At the source side of the channel region back channel modulation can be observed while at the same time, hole current below the gate and channel supplies the bipolar mechanism.

Based on the 2-D analysis, the bipolar and backgating mechanism may be much more dominant in a 3-D simulation. In this 2-D simulation, the plane of ionization shields the electrons on the source side. In a 3-D case, shielding by the ionization track would only occur only at one location along the FET's gate width. The effect of the "p-reservoir" would be more dominant when compared to the initial prompt drift component in a 3-D simulation.

From these simulations, we observe charge collection from: 1) prompt charge due to ionization in the ohmic implant, 2) photoconductive collection between drain and gate, 3) hole collection at the gate from the ionization, 4) gate hole collection due to holes below the source, 5) electrons modulated below the channel, and 6) a source-to-drain bipolar current controlled from holes in (3 and 4). The objective of the LT GaAs buffer is to limit as many of these contributions as possible.

Ionization track density was examined for three cases. The ionized "plane" in these 2-D simulations were 15 fC, 30 fC and 150 fC, deposited over a 0.25 μm thick plane, 2.0 μm depth, and 10 μm width. These charges would correspond to LETs of 0.13, 0.26 and 1.32 MeV/mg/cm^2. Figure 8 illustrates the drain photocurrents. To incur upset in a dynamic circuit, the voltage must drop below the succeeding logic gate threshold voltage (250 mV for DCFL) of the following inverter.

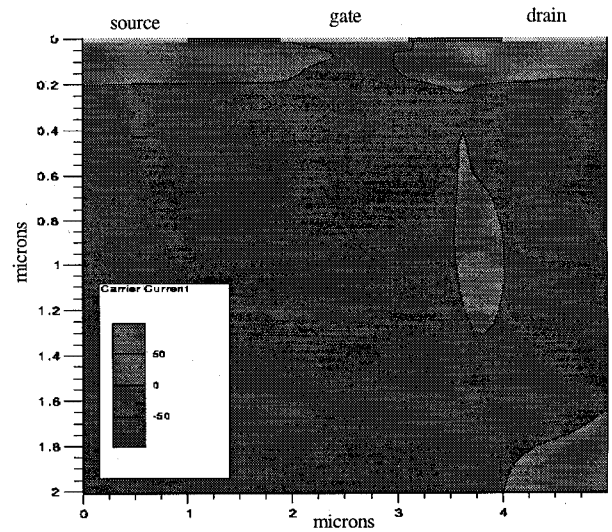

Figure 7: Cross section of electron and hole current occurring at the second peak of drain current in Figure 4. Notice hole current dominants the region under the gate, supporting a bipolar effect.

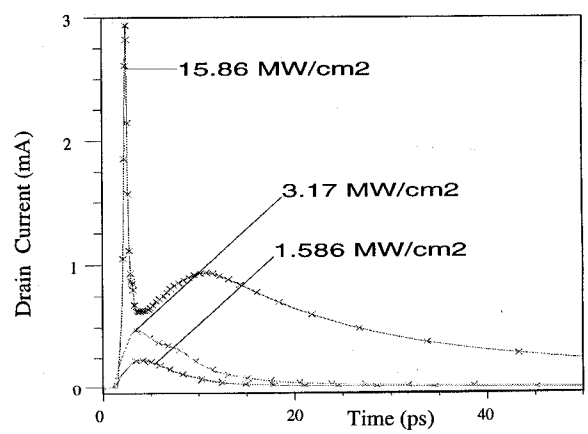

Figure 8: Drain photocurrents for three different ion track intensities.

The different time constants in the trailing rise of the voltage transient is due to the output-node change in small signal impedance between the following load gate and the active D-FET load. Four of the simulations performed illustrate the voltage upset: 1.0 MW/cm^2 (9.5 fC / 0.08 MeV/mg/cm^2), 2.0 MW/cm^2 (18.9 fC / 0.16 MeV/mg/cm^2), 3 MW/cm^2 (28.4 fC / 0.25 MeV/mg/cm^2), 5 MW/cm^2 (47.3 fC / 0.42 MeV/mg/cm^2). A full swing transient was observed in all but the 0.08 MeV/mg/cm^2 case, as shown in Figure 9.

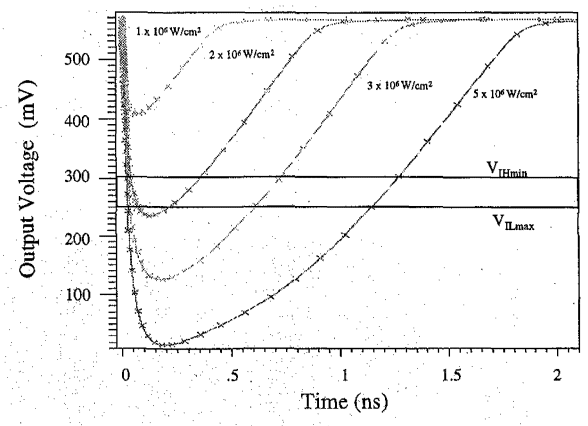

Figure 9: Voltage transients for three intensities of ionization. The largest swing is from the 5.0 MW/cm^2 case which is equivalent to an LET of 0.42 MeV/mg/cm^2. VIHmin and VILmax correspond to the input high and low noise margin.

V. LT GaAs Epitaxial Structure

The wafer design must meet two criteria: a) show equivalent performance to the standard bulk process, and b) show reduced sensitivity to SEU. Figure 1 shows the general structure of the epitaxial wafer.

The initial design parameters were the E-FET and D-FET threshold voltages. The profile of the p-layer had to be determined to accommodate both the E-FET and D-FET n-channel implants because we chose to utilize a p-dopant in the MBE growth. Using the MBE growth to dope the p-layer improved control of the p-impurity level. Otherwise, additional research would be needed to investigate activation issues of p-implants in the epitaxy and LT GaAs buffer.

Lower activation of channel implants had to be considered in the design. Figure 10 shows a doping and material structure profile for the MESFETs in this work. The critical parameter to control the thresholds of both devices are the p-layer doping, location, and thickness. The LT GaAs buffer was placed just below the p-layer.

The diffusion barriers, mentioned earlier, are critical to create the short carrier lifetimes and to insure minimal degradation in transistor operation. Additionally, it was observed that the diffusion barrier can hinder the movement of electrons and holes to the LT GaAs buffer. Actually, there is a compromise between how much prompt charge can be eliminated in the first peak of the photocurrent verses how much charge can flow through the diffusion barriers into the LT GaAs buffer. As shown in Figure 11, comparisons of the drain currents between a LT GaAs structure with diffusion barriers show larger amplitudes (and integrals) than without diffusion barriers. The AlAs diffusion barrier does reduce the prompt response by hindering any charge below the diffusion barriers from escaping to the drain terminals. However, excess charge near the FET channel is limited from entering the LT GaAs. Holes diffuse toward the buffer but are retained and not recombined. Channel modulation is observed from this large hole density at the diffusion barrier. Figure 12 shows hole confinement at the diffusion barriers. This effect has been observed previously when superlattices are utilized [11]. Figure 13 examines the effect of diffusion barrier thickness. Minimal change is observed in the photocurrent response between a 100A or 500A barrier.

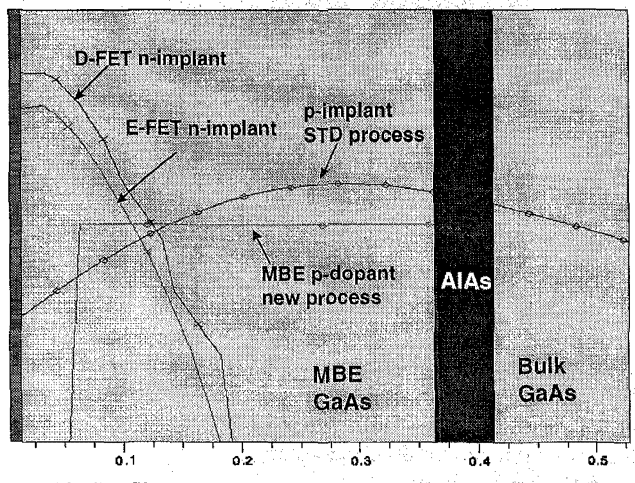

Figure 10: Profiles comparing standard structure and MBE LT GaAs structure.

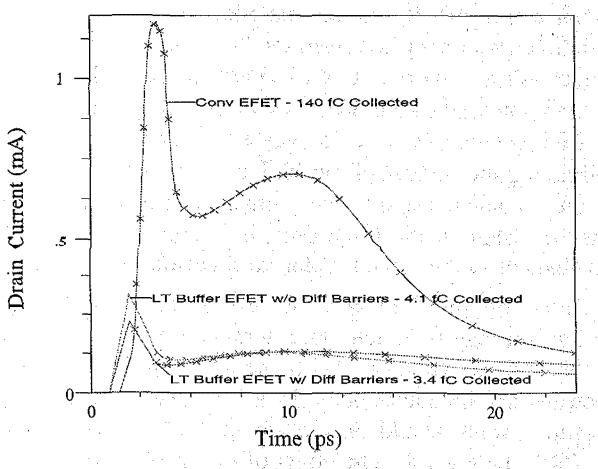

Figure 11: Drain current comparisons between conventional FET, an LT GaAs buffer without diffusion barriers, and a LT GaAs buffer with 500A AlAs diffusion barriers.

The material utilized for diffusion barriers should be lattice-matched to the LT GaAs buffer. AlGaAs, AlAs and GaAs has been utilized in literature by various researchers [12]. Related work on implementing LT GaAs buffers in HIGFETs has shown equivalent device performance with AlGaAs and AlAs [6]. The use of thicker layers is used to provide a stabilized layer for subsequent high-crystalline epitaxial layers. A critical parameter in the growth of MBE is the stress induced by interfaces. As-grown LT-GaAs (not annealed) has a lattice constant 1% larger than GaAs. After annealing, the interstitial As is reduced, thus returning the lattice constant to the normal GaAs spacing. Techniques to relieve stress are needed to insure high quality epitaxy above the buffer structure.

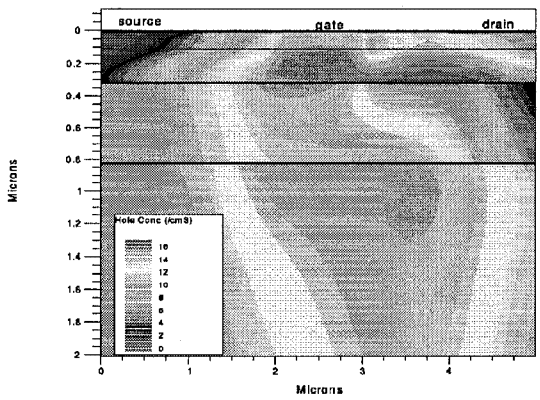

Figure 12: Hole concentration showing confinement above and below the diffusion barriers.

VI. Discussion

The basic charge collection mechanisms on discrete devices and integrated transistors are similar. However, the charge enhancement mechanisms are reduced in the integrated cases. In a discrete device biased at a constant drain voltage, a strong field always exists to assist electrons. In a strong ionization event, the drain node is shorted to ground very quickly, thus eliminating the strong field that is required for bipolar action or channel conduction. Only after the circuit begins to recover, and depending on the response of the circuit components (active load, gate diode leakage, nodal capacitance, Schottky gate capacitance), the charge collection mechanism begin to slow down the response as the drain voltage increases. It was shown in Figure 4 that the back-channel modulation component is not critical if the active load current exceeds it.

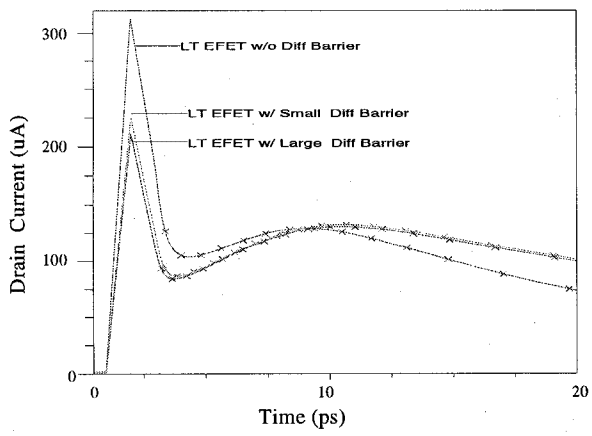

Figure 13: Compares the drain photocurrent for varying diffusion barrier thicknesses and no diffusion barrier. Observe the initial pulses and the changeover at 10 ps from the diffusion barrier case showing larger tails in the response.

It is clear that the parasitic bipolar effect occurs earlier in the charge collection event and does have a strong role in discharging the succeeding gate capacitance, see Figure 4. The source of this mechanism is due to two components, holes funneling from the ionization track and holes from the undepleted p-layer to the reversed-bias Schottky gate. The dominant characteristic of this response is the hole lifetime and hole current. To sustain an NPN bipolar (source implant - emitter, high hole density - base, drain implant - collector) parasitic effect, a hole current must exist to forward bias the source implant junction. In these simulations, the E-FET gate electrode has been kept grounded to mimic the logic low state and to simplify the simulation. However, the holes collected on the E-FET gate capacitance will reduce the reverse bias on the gate and lower the hole current at the gate. The bipolar action may be a shorter-lived mechanism in this case, or the bipolar mechanism may move lower in the transistor.

One purpose of the LT GaAs buffer layer is to assist the gate junction to remove holes. This not only limits charge collection but reduces backgating effects in GaAs FETs, which are also dominated by holes (and hole traps) in the substrate [12]. The efficiency of the LT GaAs buffer to absorb excess holes is regulated by the potential of the diffusion barriers and the capability of providing a high recombination current inside the buffer.

These simulations have also shown that the LT GaAs buffer does an efficient job of reducing the prompt (drift) component of the initial event, which can be a considerable proportion of the photocurrent, see Figure 10. For large ionization events, while an electron-hole plasma exists in the LT GaAs buffer, the transit of electrons from the substrate must be constrained by reducing both electron and hole lifetimes or increasing barrier thickness. Essentially, the diffusion length must be less than the transit time across the buffer.

Conflicts to reducing lifetimes in LT GaAs and increasing buffer thickness occur in manufacturing. In this particular process, high temperature anneals of much higher temperatures than the intentional LT GaAs precipitate anneal are utilized to reduce implant damage. Reflectivity measurements on wafer type 4 and 5 have shown lifetimes on the order of 10 ps [13], an order of magnitude above the 1 ps lifetime commonly observed [14]. We expect this may be a combination of the implant damage anneal compromising the LT GaAs carrier lifetimes and a drawback in the reflectivity measurement observing the substrate lifetime.

Considerations to minimize parasitic bipolar effects in the design of the epitaxy structure conflict with the design of the MESFETs requiring a p-region to define the bottom of both the D-FET and E-FET. Even though the LT GaAs region appears slightly p-type, this could not be relied upon to control threshold voltages. Increasing p-doping in the buried layer increases the undepleted holes below the FET, thus adding to the "hole reservoir" as discussed earlier. The acceptor level of the p-region was kept as low as possible to minimize bipolar action but high enough to insure both the D-FET and E-FET thresholds were within design requirements.

The location of the LT GaAs buffer was chosen primarily on the ability to provide sufficient high quality epitaxy for the implanted process. Carrier profile measurements in this work and other work [6],[15] have shown degradation in the vicinity of LT GaAs buffers due to several effects. The current design and fabrication iteration is being done to obtain correct thresholds for the D-FET and E-FET.

The integrals of charge collected between initial ionization and where the photocurrent magnitude drops below the active load (or drain node resupply) current for the conventional and LT GaAs buffer examples show an order of magnitude reduction. If the current fabrication provides functional SRAM and test structures, we would expect the soft error rates to show a three order of magnitude reduction taken from simple estimates of GaAs soft error rates in geosynchronous orbit.

VII. Conclusions

LT GaAs buffers have shown considerable advantages in reducing soft error rates in GaAs ICs [5,6]. The properties of the buffer to act as an efficient structure to sink excess carriers by recombination has been shown in this work. The mechanisms to limit prompt charge (assisted with diffusion barriers) is very similar to silicon on insulator (SOI) technologies. Additionally, LT GaAs should have advantages over SOI in reducing charge collection due to its high density of recombination centers. We have shown that excess charge above and below the buffer is sinked by recombination currents internal to the buffer. However, the buffer recombination rate can be compromised by diffusion barriers intended to confine arsenic to the buffer during MBE growth.

Manufacturing issues (growth temperatures, annealing techniques, structure design) are currently being investigated. The challenges in the Vitesse technology are greater due to the replacement of the bulk wafer by a MBE wafer and higher processing temperatures.

Finally, successful implementation of LT GaAs buffers will provide a very cost effective technique to harden GaAs implanted MESFET circuits against soft errors. Once the LT GaAs structure is optimized for both fabrication and charge collection, previous and future mask designs can utilize this hardening technique.

Acknowledgments

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