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Single Event Upsets in Gallium Arsenide Pseudo-Complementary MESFET Logic

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Abstract

An introduction to gallium arsenide (GaAs) Pseudo-Complementary MESFET Logic (PCML) circuits is presented. PCML was developed to reduce the sensitivity of high-speed GaAs logic to radiation-induced single event upsets (SEUs). Experiments for testing the single-event upset (SEU) sensitivity of GaAs PCML integrated circuits (ICs) are described. The results of the experiments are analyzed. This new type of high-speed, low-power, GaAs logic provides decreased sensitivity to SEUs compared to more traditional circuit designs such as Directly-Coupled FET Logic (DCFL). PCML is fully compatible with existing GaAs E/D MESFET fabrication processes, such as those commonly used to make DCFL.

I. INTRODUCTION

Gallium arsenide (GaAs) Pseudo-Complementary MESFET Logic (PCML) [1] is a new type of high-speed, low-power logic for space applications or other radiation-prone environments. In developing this new logic family, the main goal was to reduce the sensitivity of GaAs logic to single event upsets (SEUs) without requiring changes to the fabrication process. Changes to the fabrication process were deemed undesirable because of the high costs involved with developing a new fabrication process, and with maintaining two separate fabrication processes for commercial parts and radiation-tolerant parts. Instead, the main goal has been accomplished by experimenting with new logic circuit topologies, and PCML is the result. GaAs PCML has reduced sensitivity to single event upsets (SEUs) when compared to more traditional forms of GaAs logic such as Directly Coupled FET Logic (DCFL) [2] and Two-Phase Dynamic FET Logic (TDFL) [3].

Other goals of this research included keeping the power consumption of the new type of logic as low as possible, maintaining the high speed characteristics of DCFL and TDFL, and keeping the required logic gate layout area small. Only a few PCML ICs currently exist because PCML is a new type of GaAs logic. Therefore, the speed and power consumption of PCML has not been fully characterized. Simulations and preliminary measurements indicate that PCML is as fast as DCFL and TDFL, and consumes less power than DCFL but more than TDFL. Minimizing layout area is especially important because the sensitive cross section of a logic gate increases as transistor area increases. The number of active devices and the layout area for PCML is approximately the same as for dual-rail DCFL for circuits that perform the same logic functions. The number of devices required to implement a TDFL dual-rail gate is much greater than for PCML. For dual-rail TDFL, all transistors are relatively small, but the required layout area is still greater than for PCML and DCFL. Also, distribution of ϕ_1 and ϕ_2 clock signals in TDFL layouts utilizes extra space. However, with DCFL and TDFL, if complementary outputs are not required they do not have to be generated (see Figure 1), and layout area can be saved. With PCML, complementary outputs are always required. A single output TDFL gate will have about the same area as a PCML gate. A single output DCFL gate requires less area than a PCML gate. It should be noted that if complementary outputs are not needed in a DCFL or TDFL circuit, and if they are eliminated to save layout area, then the ability to detect SEUs at logic gate, module, and subsystem outputs using the principles of dual-rail logic is lost.

Previous research has indicated that in a spacecraft in a geosynchronous orbit, SEU rates in the range of 1.2×10^{-3} to 2.1×10^{-3} errors per bit-day can be expected for GaAs DCFL [4], and 4.9×10^{-4} to 5.3×10^{-4} errors per bit-day can be expected for GaAs TDFL [5]. These are moderately high SEU rates relative to the requirements of most space systems, which sometimes require SEU rates as low as 10^{-10} errors per bit-day. The relatively high SEU sensitivity of GaAs MESFETs is the result of efficient charge enhancement mechanisms [6], such as back channel modulation. These mechanisms cause the collected charge to exceed that deposited by an ion when the ion passes through the semiconductor material. A detailed, quantified explanation of this mechanism, complete with cross-sectional views of the MESFET, can be found in reference 7. The collected charge changes the voltage on the node of the circuit connected to the affected transistor. If enough charge is collected, the change in voltage becomes large enough to cross the threshold of the logic gate or flip flop. There are

different methods for reducing the sensitivity of GaAs logic to SEUs. For example, at the device level, one can reduce the amount of charge that is collected. However, this usually requires changes to the fabrication process, which are usually very expensive. Another method, which can be accomplished at the circuit level, is to develop a circuit that does not easily change logic states when a single transistor experiences charge collection, such as dual-path logic. This is the method that was pursued in this research. The advantage of the circuit topology used in PCML is that the dual-rail approach also eliminates static power consumption, which is a problem for DCFL even if dual-rail DCFL is used. It also eliminates the need for ϕ_1 and ϕ_2 clock signals, which is a problem for TDFL even if the dual-rail approach is used with TDFL.

A schematic diagram of a PCML 2-input OR/NOR gate is shown in Figure 1A. Gates sizes in Figures 1, 4, and 5 are in microns, length×width, and area in square microns is given for diodes. Referring to the schematic in Figure 1A, it should be noted that when the logic gate is at rest (not changing states), the outputs of the OR half of the gate and the NOR half of the gate are pulled directly to either GND or V_{DD} by enhancement-mode MESFETs. Furthermore, whichever direction an output is pulled, the transistor that is on is operating in the ohmic (linear) region, with V_{GS} being well above the threshold voltage (V_T) and V_{DS} being significantly less than V_{GS}. This allows the on transistors to sink or source a large current to rapidly dissipate any charge that collects on the OR or NOR output nodes because of a SEU. This minimizes the duration of the resulting voltage transient on the output node of the circuit. Furthermore, in PCML circuits, the off transistors are turned completely off, with V_{GS} being significantly below the threshold voltage. Therefore, when a SEU occurs, the on transistors only need to sink or source the current caused by the charge collection, and not the sum of a static operating current and the current caused by charge collection. From the perspective of circuit topology, PCML is analogous to GaAs HIGFET and Si CMOS static complementary logic, and collected charge is dissipated in a similar manner in all of these circuit types. However, PCML does not require any P-type FETs, thus allowing fabrication on standard GaAs E/D MESFET processing lines.

An additional advantage that results from the off transistors being biased well below threshold in PCML circuits is that charge collection in GaAs MESFETs is highly dependent on device bias conditions [6]. For gate biases well below threshold, charge enhancement mechanisms are greatly reduced, resulting in significantly less collected charge [7] [8]. This minimizes the amplitude of the resulting voltage transient on the output node of the circuit. Another benefit of PCML is that a SEU will only affect either the uncomplemented or the complemented output, but not both. Therefore, SEUs can be easily detected at the output of a critical logic block by taking the exclusive-OR of the two outputs, which should always be a logic 1.

For comparison purposes, the schematic diagram of a GaAs dual-rail DCFL 2-input OR/NOR gate is presented in Figure 1B [2]. Note that when one of the outputs is high, it is pulled up by a depletion-mode MESFET ($V_T = -0.8\,V$) with a V_{GS} of zero volts. It should be remembered that V_{GS} for a GaAs MESFET can rise as high as 0.6 V without any significant flow of gate current. A depletion-mode MESFET with a V_{GS} of zero volts has a much higher on channel resistance than it would if V_{GS} were actively driven to a higher value, as is the case for on transistors in PCML. Therefore, if a SEU occurs and charge is collected on an output node while the node is high, the pull-up MESFET will not be able to sink or source as much current, and will not be able to rapidly deplete the collected charge. Thus, the duration of the resulting voltage transient will be greater. Furthermore, when an output of a DCFL OR/NOR gate is low, the pull-up transistor fights the pull-down transistor and the output voltage is determined by whichever transistor has a lower channel on resistance. If charge collects on the output node while it is low, the pull-down transistor will be required to conduct this static operating current plus the current resulting from charge collection. Therefore, the amplitude of the resulting voltage transient will be greater. If the amount of collected charge is large enough, the voltage transient will cross the logic threshold of the gate input connected to the output node being affected.

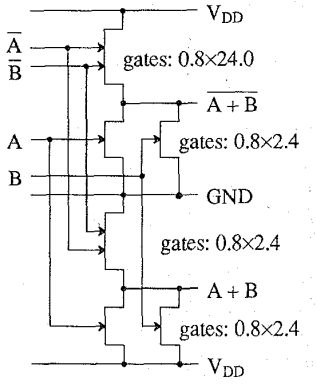

Figure 1A: PCML 2-input OR/NOR gate.

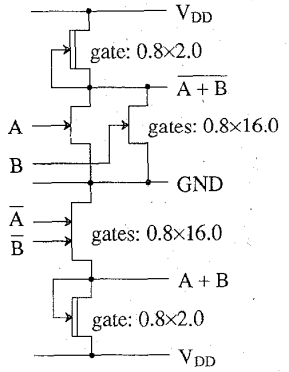

Figure 1B: DCFL dual-rail 2-input OR/NOR gate.

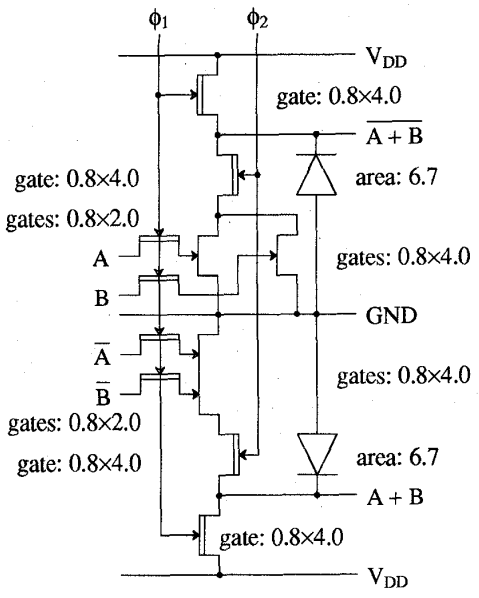

Figure 1C: TDFL dual-rail 2-input OR/NOR gate.

Figure 1C shows a schematic diagram of a GaAs dual-rail TDFL OR/NOR gate [3]. TDFL gates do not experience the pull-up/pull-down fight that DCFL gates experience, and all transistors operate with a high value of V_{GS} when they are turned on. Furthermore, when transistors in TDFL gates are turned off, they are operated with V_{GS} significantly below the threshold voltage. Also, there is no static current flow in TDFL circuits. Current only flows when the clock signal changes state. However, because they operate dynamically, TDFL circuits must temporarily store a logic value on an isolated node, usually an input or output node. This is accomplished by storing charge on a capacitor, which is usually implemented using a reverse biased diode as shown in Figure 1C. If the isolated node collects charge because of a SEU, the voltage on the node will change. If the change in voltage is large enough, it will cross the logic threshold of the gate input connected to the output node being affected.

II. SEU TESTING, EQUIPMENT, AND PROCEDURE

It can be seen from Figure 1A that if any transistor in a GaAs PCML logic gate experiences a charge collection event, then the output logic value of one of the gate outputs can be affected. Therefore, for the laser experiments described here, it was necessary to determine the SEU sensitivity of each transistor in a gate in order to determine the soft error rate for the entire gate. To measure the SEU sensitivity of each transistor in PCML gates, a custom PCML test and evaluation IC was designed that contained several experimental PCML circuits. In addition to serving as a vehicle for SEU testing, the experimental IC also provides evaluation data for comparison of PCML against DCFL and TDFL for power, speed, and logic density. The IC design was fabricated at Vitesse Semiconductor Corporation using their standard, HGaAs-III, E/D MESFET fabrication process. With this process, nominal transistor threshold voltages are approximately +0.25 V for enhancement-mode FETs and −0.8 V for depletion-mode FETs. The IC was packaged in a 52-pin leaded ceramic flat pack. The package lid was left unsealed to allow easy removal of the lid and access to the surface of the IC with laser light.

Figure 2 shows the top of the PCML test and evaluation IC, mounted on the test fixture, ready for SEU testing with the laser. Laser light shines through a hole in the test fixture, through the open package lid, and onto the chip. Figure 3 shows the bottom of the IC and test fixture. The use of coaxial cable interconnect, terminated with 50 Ω chip-type microwave resistors, reduces reflections and cross talk and allows the IC to function properly at high frequencies during testing. The use of dedicated power, ground, and termination power rings, and chip-type microwave capacitors for bypassing, keeps high-frequency noise off the power, ground, and termination power supply leads. An aluminum clamp padded with felt holds the package leads to the test fixture.

Initially, proper operation of the GaAs PCML test and evaluation circuits was confirmed in a friendly (non-radiation) environment. It should be noted that all circuits were designed to be power-supply compatible with low-voltage CMOS ICs. Thus, the IC was intended to be operated with a V_{DD} supply voltage of +3.3 V. However, for monitoring outputs and detecting SEUs, it was desired to use the internal 50 Ω terminations of the oscilloscope inputs to reduce reflections on the output cables. Therefore, during testing, the V_{DD} supply to the IC under test was

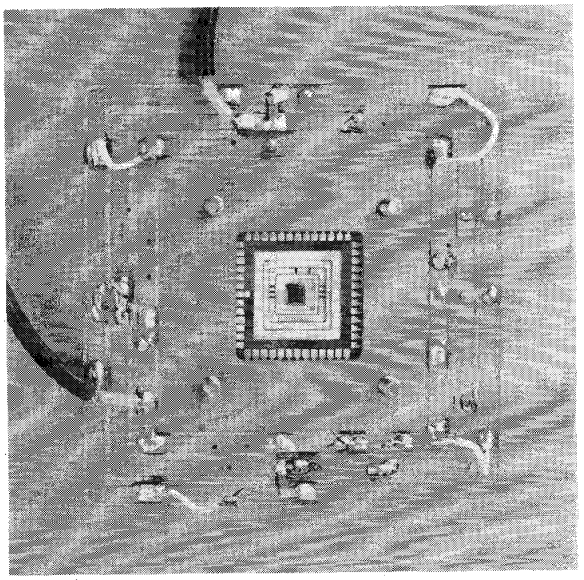

Figure 2: Top of PCML test and evaluation IC and test fixture.

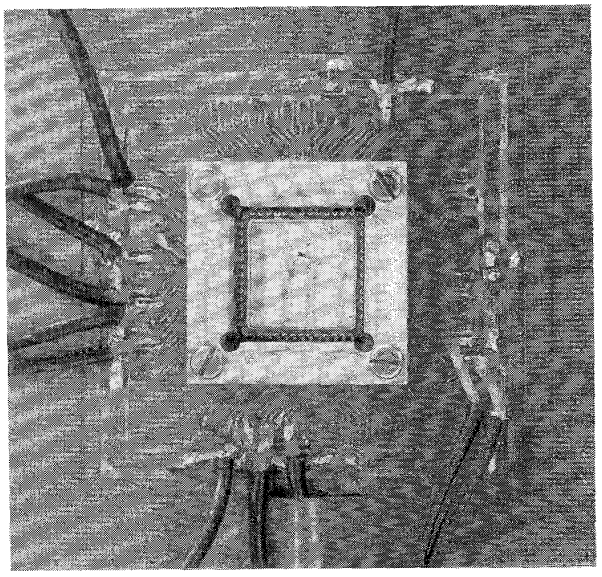

Figure 3: Bottom of PCML test and evaluation IC and test fixture.

operated at +1.65 V, relative to true ground. The GND supply to the test IC was operated at −1.65 V, relative to true ground, thus providing the IC with a total supply voltage of 3.3 V. With these power supply voltages, on-chip logic levels are approximately −1.6 V for a logic 0 and −1.1 V for a logic 1. Off-chip logic levels are approximately −1.0 V for a logic 0 and +0.4 V for a logic 1. The difference in on-chip and off-chip logic levels is due to the output driver and input receiver circuits that provide a high input impedance and a low output impedance. The on-chip loading of all logic gates tested is typical for these types of gates when used in larger circuits and systems.

Charge-collection events were induced with the output of a modelocked, cavity-dumped, dye laser centered at 615 nm (2.0e V). The use of pulsed lasers in charge collection experiments for testing the SEU characteristics of devices and circuits is well documented [6] [8] [9] [10] [11] [12]. The pulse repetition rate of the laser used in the experiments described here was 12.198 KHz, with a pulse duration of 1 ps. Spot size was approximately 1 μm in diameter.

Laser energy was measured at the minimum intensity necessary to cause a complete change of logic states in the circuit under test. From the laser energies measured during the experiments, the amount of charge created in the semiconductor from the laser pulse can be calculated. Measurements are accurate to approximately ±20%. Irradiation with 615 nm light corresponds to an absorption coefficient $\alpha = 5 \times 10^4$/cm, and the 1/e absorption depth is approximately 0.2 μm below the surface. It is assumed that each photon absorbed by the GaAs creates a single electron-hole pair, and any remnant photon energy is converted to phonons (heat). It is assumed that approximately 67% of the incident light is absorbed in the GaAs. The rest is reflected at the SiO_2 and SiO_2/GaAs boundaries.

A total of four circuits were tested, including two inverter/buffer circuits, an OR/NOR gate, and a ring oscillator composed of inverter/buffers. A schematic diagram of the inverter/buffer circuit is shown in Figure 4. A schematic diagram of the OR/NOR gate is shown in Figure 5. The mask layout of the inverter/buffer is shown in Figure 6. The mask layout of the OR/NOR gate is shown in Figure 7. A legend for the stipple patterns used in Figures 6 and 7 is shown in Figure 8. Laser target locations are indicated in both Figures 6 and 7, and verbal descriptions of laser target locations are given in Tables 1 and 2. For reference, approximate laser target locations are also indicated in Figures 4 and 5.

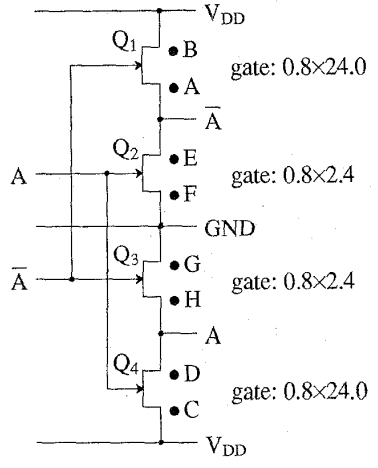

Figure 4: Schematic diagram of PCML inverter/buffer circuit.

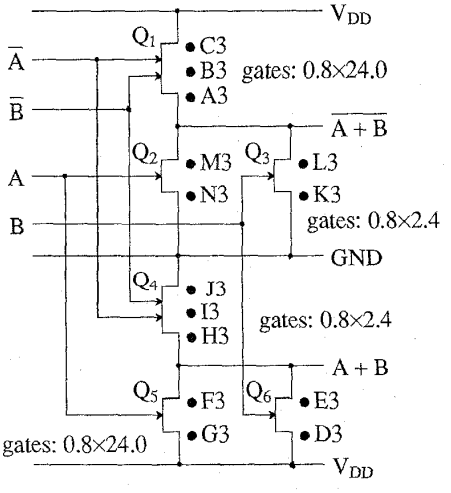

Figure 5: Schematic diagram of PCML OR/NOR gate.

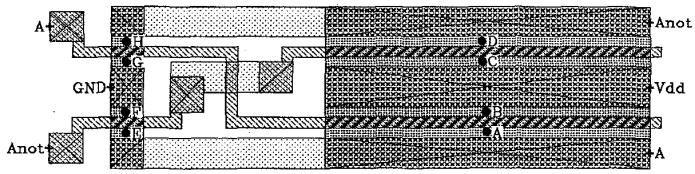

Figure 6: Mask layout of PCML inverter/buffer.

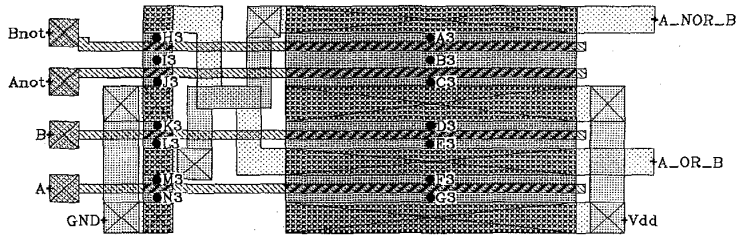

Figure 7: Mask layout of PCML OR/NOR gate.

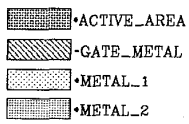

Figure 8: Legend for stipple patterns used in Figures 6 and 7.

III. EXPERIMENTAL RESULTS AND ANALYSIS

The first PCML circuit tested was an inverter/buffer circuit. The test was conducted with the input held at a constant value of logic 1 (output = 0). The output was monitored with an oscilloscope to detect a 0-1-0 SEU. A permanent change in the output logic value of the inverter/buffer was not observed, or expected, because inverter/buffers are purely combinatorial logic circuits. The second circuit tested was another inverter/buffer circuit, but with the input held at a constant value of logic 0 (output = 1). The output was monitored with an oscilloscope to detect a 1-0-1 SEU. The third circuit tested was an inverter/buffer that was part of a ring oscillator and that was constantly switching back and forth between low and high. The output was monitored with an oscilloscope to detect distortions in the output waveform. Tables 3, 4, and 5 list the minimum amount of deposited charge required to induce SEUs at all laser target locations for the three inverter/buffer circuits that were tested. All deposited-charge data in Tables 3, 4, 5, and 6 was obtained using the experimental procedure previously described. For the 35-stage ring oscillator, the period of oscillation was measured at approximately 20 ns, which equates to a propagation delay of approximately 286 ps per stage. The use of this logic in a system would allow system clock rates of well over 2 GHz. It should be noted that the laser was not synchronized to the ring oscillator. Therefore, it can be assumed that the most sensitive portion of the period was measured at each laser target location.

The fourth PCML circuit tested for SEU sensitivity was a 2-input OR/NOR gate. For this experiment, the A and B inputs of the OR/NOR gate were held low. The output was monitored with an oscilloscope to detect a 0-1-0 SEU. As with the inverter/buffers, a permanent change in the output logic value of the OR/NOR gate was not observed, or expected, because OR/NOR gates are purely combinatorial logic circuits. Table 6 lists the minimum amount of deposited charge required to induce SEUs at all laser target locations in the OR/NOR gate.

Referring to the data in Tables 3 and 4, it is clear that the value of the input logic signal has a pronounced affect on the SEU sensitivity of a PCML inverter. Similar results have been observed for other types of GaAs logic [5]. If the data in Tables 3 and 4 is compared against the layout of the inverter/buffer shown in Figure 6, it can be seen that the change in SEU sensitivity between a gate with a logic 0 input and a gate with a logic 1 input is because the affected transistor has changed states from the ohmic (linear) region to the cut off region. When a transistor is cut off, a nearby charge collection event will cause a rapid buildup of charge, and therefore voltage, on the isolated circuit node because there is no leakage path. This rapid buildup of charge causes a rapid change in the voltage on the affected node. However, when a transistor is operating in the ohmic region, as soon as charge starts to collect, current flows through the on transistor and the charge dissipates from the affected node. Therefore, the total voltage change on the affected node, and also the rate of change, is significantly less than when the transistor is cut off. It can be seen from Tables 3 and 4 that there is some variation in the sensitivity of transistors that might at first be expected to have the same sensitivity. We

attribute some of this variation to the difference in operating biases of the different transistors in the circuit. Not all transistors that are cut off have the same V_{GS} and not all transistors that are operating in the ohmic region have the same V_{GS}. As previously mentioned, the sensitivity of a MESFET is dependent upon the bias voltage. Furthermore, larger transistors have more capacitance, and thus require more charge to cause the same change in voltage as a smaller transistor. Also, even though the inverter layout in Figure 6 is geometrically symmetric, it is not electrically symmetric. The input node that transitions to metal one to bridge over the gate metal of the other input will have less parasitic capacitance.

Referring to the data in Table 6, it can also be seen that for an OR/NOR gate, the SEU sensitivity of a transistor is affected by whether it is cut off (nonconducting) or operating in the ohmic region (conducting). The results indicate that laser target locations A, B, and C are less sensitive than locations D, E, F, and G, even though SEUs at all of these target locations induce charge in pull-up transistors. The difference is that SEUs at locations A, B, and C affect a pull-up transistor that is operating in the ohmic region, and at locations D, E, F, and G SEUs affect pull-up transistors that are cut off. Laser target locations H, I, and J are less sensitive than locations K, L, M, and N, even though SEUs at all of these target locations induce charge in pull-down transistors. However, SEUs at locations H, I, and J affect a pull-down transistor that is operating in the ohmic region, and SEUs at locations K, L, M, and N affect pull-down transistors that are cut off.

It is also interesting to note that the SEU sensitivity of PCML goes up as the frequency of operation goes up. This can be seen by comparing the data in Tables 3, 4, and 5 for the various different laser target locations. In all cases, inverter/buffers with a static logic 0 or a static logic 1 input are less sensitive to SEUs than an inverter/buffer that is constantly switching back and forth between two logic values, as is the case for inverters in a ring oscillator. The effect of frequency on SEU sensitivity has been noticed with other forms of GaAs logic [5] [10]. When designing an IC or a logic system for a high radiation environment, a worst-case analysis of the soft error rate should be done assuming the highest clock rate at which the IC or system will operate. Future work may focus on the design of logic circuits that have a SEU sensitivity that is not dependent on operating frequency.

Another interesting observation is that pull-up FETs, or FETs with the drain connected to V_{DD}, are more sensitive to SEUs than are pull-down FETs, or FETs with the source connected to ground, when both FETs are turned on. The same is true when both FETs are turned off. For example, compare laser target locations C and D in Table 3 (on pull-up FET) with locations G and H in Table 4 (on pull-down FET). Or, compare locations C and D in Table 4 (off pull-up FET) with locations G and H in Table 3 (off pull-down FET). The reason for this is that even though both transistors are turned off or both are turned on, they do not have the same bias points. And, as previously explained, the bias point has a pronounced effect on the charge enhancement mechanisms of the MESFET.

Table 1: Laser Target Locations for Inverter/Buffer Circuit

Laser Target	Target Location
A	in channel on source side of gate of Q_1
B	in channel on drain side of gate of Q_1
C	in channel on drain side of gate of Q_4
D	in channel on source side of gate of Q_4
E	in channel on drain side of gate of Q_2
F	in channel on source side of gate of Q_2
G	in channel on source side of gate of Q_3
H	in channel on drain side of gate of Q_3

Table 2: Laser Target Locations for OR/NOR Gate

Laser Target	Target Location
A3	in channel on source side of gate of Q_1
B3	in channel between dual gates of Q_1
C3	in channel on drain side of gate of Q_1
D3	in channel on drain side of gate of Q_6
E3	in channel on source side of gate of Q_6
F3	in channel on source side of gate of Q_5
G3	in channel on drain side of gate of Q_5
H3	in channel on drain side of gate of Q_4
I3	in channel between dual gates of Q_4
J3	in channel on source side of gate of Q_4
K3	in channel on source side of gate of Q_3
L3	in channel on drain side of gate of Q_3
M3	in channel on drain side of gate of Q_2
N3	in channel on source side of gate of Q_2

Table 3: SEU Sensitivities of Inverter/Buffer Circuit with Static Logic 1 Input

Laser Target Location	Deposited Charge (pC)	Sensitive Area (μm^2)	Soft Error Rate (Errors/Day)
A	0.53	51.2	2.9×10^{-7}
B	0.07	51.2	1.9×10^{-5}
C	10.18	51.2	8.0×10^{-10}
D	7.34	51.2	1.5×10^{-9}
E	166.9	8.0	4.7×10^{-13}
F	0.18	8.0	3.8×10^{-7}
G	36.72	8.0	9.6×10^{-12}
H	11.52	8.0	9.8×10^{-11}

Table 4: SEU Sensitivities of Inverter/Buffer Circuit with Static Logic 0 Input

Laser Target Location	Deposited Charge (pC)	Sensitive Area (μm^2)	Soft Error Rate (Errors/Day)
A	10.68	51.2	7.3×10^{-10}
B	7.00	51.2	1.7×10^{-9}
C	2.17	51.2	1.8×10^{-8}
D	2.34	51.2	1.5×10^{-8}
E	40.06	8.0	1.3×10^{-10}
F	36.72	8.0	9.6×10^{-12}
G	46.73	8.0	5.9×10^{-12}
H	40.06	8.0	8.1×10^{-12}

Table 5: SEU Sensitivities of Inverter/Buffer Circuit in a Ring Oscillator

Laser Target Location	Deposited Charge (pC)	Sensitive Area (μm^2)	Soft Error Rate (Errors/Day)
A	0.47	51.2	3.8×10^{-7}
B	0.06	51.2	2.5×10^{-5}
C	0.23	51.2	1.5×10^{-6}
D	0.13	51.2	4.6×10^{-6}
E	0.02	8.0	4.5×10^{-5}
F	0.03	8.0	1.8×10^{-5}
G	0.05	8.0	4.6×10^{-6}
H	0.02	8.0	4.5×10^{-5}

Table 6: SEU Sensitivities of Laser Target Locations for a 2-Input OR/NOR Gate.

Laser Target Location	Deposited Charge (pC)	Sensitive Area (μm^2)	Soft Error Rate (Errors/Day)
A3	13.35	51.2	4.7×10^{-10}
B3	9.35	61.44	1.1×10^{-9}
C3	6.68	51.2	1.9×10^{-9}
D3	0.13	51.2	4.6×10^{-6}
E3	0.13	51.2	4.6×10^{-6}
F3	0.40	51.2	5.2×10^{-7}
G3	0.27	51.2	1.2×10^{-6}
H3	26.70	8.0	1.8×10^{-11}
I3	33.38	9.6	1.4×10^{-11}
J3	25.04	8.0	2.1×10^{-11}
K3	13.35	8.0	7.3×10^{-11}
L3	16.69	8.0	4.7×10^{-11}
M3	16.69	8.0	4.7×10^{-11}
N3	23.37	8.0	2.4×10^{-11}

When comparing an off pull-up FET to an off pull-down FET, the pull-up FET will have a lower V_{GS}. The same is true for two FETs that are on. When V_{GS} is lower, the depletion capacitance of the FET is smaller. Therefore, less collected charge is required to cause a given voltage change, compared to a FET with a higher value of V_{GS}.

The deposited-charge data in Tables 3, 4, 5, and 6 can be combined with worst-case estimates of the sensitive area of each affected device to obtain an estimation of the soft error rate of each device in the circuit. For these calculations, it is assumed that the logic gate is a part of a digital system in a satellite in a geosynchronous orbit [13] [14]. The worst-case estimates of sensitive area, and the related soft error rate associated with each area, are listed in Tables 3, 4, 5, and 6. Sensitive areas were determined by aiming the laser at different locations on and nearby transistor channels. The perimeter of the sensitive area was thus determined. For most of the transistors tested, the sensitive area includes the active channel region and a border around the active region of approximately 1 μm. For each transistor, the actual location where the deposited charge was measured, shown in Figures 6 and 7, was the most sensitive spot on the transistor. For the data in Tables 3, 4, 5, and 6, the entire sensitive area is assumed to be as sensitive as the most sensitive spot. Therefore, the sensitive area estimates in the tables are worst-case estimates.

The error-rate estimates for all devices in a gate can then be summed to obtain an estimation of the soft error rate for the entire logic gate. The estimates for an inverter/buffer, in errors per day, are 1.9×10^{-05} for an inverter/buffer with a steady-state logic 1 on the input and 3.5×10^{-08} for an inverter/buffer with a steady-state logic 0 on the input. For an inverter/buffer operating at a frequency of 1.5 GHz, the estimated soft error rate is 1.4×10^{-04}. For a 2-input OR/NOR gate with steady-state 0s on the inputs, the estimated soft error rate is 1.1×10^{-05}. These figures do not include the reduction in the soft error rate that results from the ability to detect SEUs with the dual-path, complementary outputs of PCML gates. Utilization of this built-in error detection capability requires the addition of an exclusive-OR gate at each output of each logic module or subsystem component.

In comparison to other types of GaAs logic circuits PCML fairs quite well, even when operating at high speed where PCML is the most sensitive. Laser SEU testing of TDFL circuits fabricated using the same process, and operating at a clock frequency of 67.67 MHz, has yielded a soft error rate of approximately 4.9×10^{-4} to 5.3×10^{-4} errors per day [5]. This error rate would increase if the clock frequency were increased. For DCFL static memory circuits fabricated using the same process, soft error rates, in errors per bit-day, of 1.2×10^{-3} to 2.1×10^{-3} have been measured [4]. As with the SEU rates for PCML, the SEU rates for DCFL and TDFL do not include the reduction in the soft error rate that results from the ability to detect SEUs with dual-path complementary outputs. Although the error rate for DCFL is significantly greater than the error rate reported here for PCML, it is difficult to draw any quantitative conclusions between the data for DCFL and the data presented here because the measurements for the DCFL memory circuits were conducted with an ion beam rather than a laser. The estimate of the SEU rate for TDFL is directly comparable to the results of this work because both experiments were done using the same experimental apparatus.

IV. CONCLUSIONS

The design and operation of GaAs PCML circuits have been reviewed. Experiments for testing the SEU sensitivity of GaAs PCML have been described. The results of the experiments have been presented and analyzed. These results indicate that GaAs PCML is approximately one order of magnitude less sensitive to SEUs induced by ionizing radiation than more common forms of GaAs logic such as DCFL and TDFL, when the dual logic paths of the PCML is not being used to detect errors. The SEU rate of PCML would be further reduced in a system that utilized the dual logic paths to detect and correct transient errors. As with other forms of GaAs logic, the SEU sensitivity of a PCML gate varies according to the input logic value(s) and the frequency of operation. The improved tolerance of PCML to SEUs, combined with its low power

consumption, high speed, and ease of detecting transient errors, makes this dual-path logic family a desirable alternative to other forms of high-speed logic for the space systems designer.

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