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# Design improvements in digital seismograph for recording long duration seismic events and aftershocks

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The paper highlights a new design approach to overcome technical limitations of digital seismographs by incorporating optimum hardware and efficient software modules etc. The paper illustrates how the new design approach has enhanced the limited 64 kbytes addressing capability of 8-bit microprocessor based seismograph to 16 Mbytes capacity. Instrument based on this design philosophy can now record many long duration seismic events and the series of subsequent aftershocks, which need storage of several mega bytes. The technique has enabled uninterrupted data acquisition and processing even when the data of earlier recorded events is being transferred from main storage to PC hard disk. The design concept has been validated successfully by operating the instrument based on this technique for long time in the field.

**Keywords**: Aftershocks, Digital seismographs, Long duration seismic events

## Introduction

Seismic instruments for earthquake monitoring and risk reduction purpose are gaining rapid importance because of their multiple uses in civil and defense applications[1]. These instruments based on advanced technology and digital communication interfaces can now be configured as earthquake alert systems[2,3], which are now in use in few advanced countries to put off critical parts of nuclear power stations, to defer temporarily the take off and landing of air flights, to switch off the fast running trains, and to close the gas supply system etc. before the ground shaking due to major earthquake takes place at these vulnerable sites[4-6].

Seismograph is used to measure, record and analyze seismic signals emanated either from natural source like earthquakes or from an artificial source like underground nuclear explosion, induced seismicity, and quarry blasts etc[7]. In order to fulfill the technical need of recording seismic signals in digital form to enable on the spot analysis in the field, digital cassette seismograph (DCS) was realized as first digital version of analog seismograph[8].

### Technical Limitations of Digital Seismographs

Seismic instruments, which are operated round the clock on rechargeable batteries at the inaccessible terrain in remote areas, require having minimum possible power consumption. But the cassette recording (CR) unit, incorporated in early digital version of seismograph being electromechanical device, is not suitable due to its more power consumption, continuous wear and tear, frequent mechanical break down, and unreliable event triggering[9]. Besides this, CR duration of a cassette is approx 15 min only when the data is recorded at a rate of 4800 bits per sec. It is too small a recording capacity for a seismograph, which is operated in the field generally for weeks together. In order to record higher frequency components, when data sampling rate is kept high, there are following problems. i) Sluggish recording response of CR mechanism; and ii) Error in synchronization of recorded data and the data produced during playback because of two independent deck units being used for this purpose. The CR does not provide on the spot analysis, it is time consuming, and human error prone. Moreover, to analyze the data of an event, one has to go serially through the entire data recorded before the desired event resulting into slow data retrieval and generation of lot of unwanted data in print form[10,11].

The event recording, which includes pre event, event and post event data, is generally done for 10-20 min and even for more time if the event is of long duration. Major earthquakes are also followed by a series of aftershocks occurring in quick succession for weeks together after the main event. To fulfill this

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essential requirement, the seismic recorder must have at least 6-8 h data storage[12,13]. To overcome these technical problems, CR has been replaced by solid state memory based storage in the upgraded version designed around 8 bit microprocessor, which has several techno-commercial merits but can address 64 kbytes memory only. The incorporation of 16-bit microprocessor improved overall performance of the recorder but it could not enhance its addressing capability beyond 1 Mbyte capacity, which can store data only for 30 min duration only. When active sites are put under seismic investigation, there may be several long duration events followed by many aftershocks occurring within one or two week's period after the main event[14].

#### Design Consideration and Improvements

The recording media within the instrument should be of fairly large capacity good enough to store the data of at least 6-8 h duration so that it can record when left unattended in the field, all the true events and aftershocks occurring within one or two weeks after the occurrence of main events. The data transfer from the instrument main storage to hard disk of a laptop PC is required either for making storage available for recording further fresh events/aftershocks or for getting event data for immediate analysis on the spot by PC. Therefore, some mechanism must be incorporated in the design to ensure uninterrupted acquisition and processing of incoming data. In order to use instrument storage economically, only true events may be recorded. For this, incoming signal produced by seismic sensors must always be checked through some fast algorithm to ascertain if the event is true or false. Therefore, the design approach must ensure that the instrument has the capability to distinguish between the true event and false event[15,16].

In order to overcome above problems of the existing 8 bit/16 bit microprocessor based digital seismographs, an improved version based on a new technique has been designed and developed in CSIO. By using this new design approach, 16 Mbyte solid-state memory storage has been provided as an integral part of the recorder realized around 8 bit Intel 80C85 CMOS microprocessor, which is capable of addressing the 64 Kbytes memory only.

## Design Philosophy

#### Hardware Design and Operation

Under this design approach, the instrument has been designed around two processing cards each based on Intel 80C85 micro-processor having independent bus structure with communication through standard input/output devices[17,18]. One of these cards has been designated as Digital Signal Processing (DSP) card while the other one as Data Transfer and Processing (DTP) card (Fig. 1).

The DSP card executes signal acquisition, digitization, processing and computation of algorithm meant to distinguish between true and false event. The DSP card has been provided with one block of 32 Kbytes of RAM, which has been used in the form of ring memory to store the digital data obtained straight after signal acquisition and its digitization. The other block of 2 kbytes RAM has been used as cache memory while an EPROM of 2 kbytes has been provided to store program instructions required to execute all the tasks assigned to this card. Other than these chips, DSP card has few 82C55 Programmable Peripheral Interface (PPI) devices, a 16 bit high-resolution A/D converter for signal digitization, and related microchips for signal processing, and interfacing etc. When the event is true, the DSP card sends the event data byte by byte at the output port of an assigned PPI (82C55) from where the data is picked up in hand shake mode by the DTP card to store in the instrument main storage.

Similarly, DTP card has its own Intel 80C85 microprocessor and interacts independently on one hand with DSP card and on other hand with laptop computer. The whole exercise has been done in synchronized manner using some hardware interrupts at both the cards. DTP card picks up the data made available by DSP card at its output port and stores it into one of the 2 Mbyte capacity eight modules, which all together constitutes instrument main storage of 16 Mbytes capacity. The process of storing and writing of true event data into instrument main storage is controlled by DTP card, which gets filled to 80% of its total capacity, starts retrieving the data from the instrument main storage and send it in serial byte form to the assigned output port. DTP card has been provided with optimum number of PPIs (82C55) to execute the tasks related to data communication between ring memory of DSP card, instrument main storage (memory modules), and hard disk. DTP card also has necessary microchips required to realize the control circuit for addressing scheme of 16 Mbytes memory designated as 'Instrument main storage'.

The main storage has been configured into eight memory modules each of 2 Mbytes capacity. The

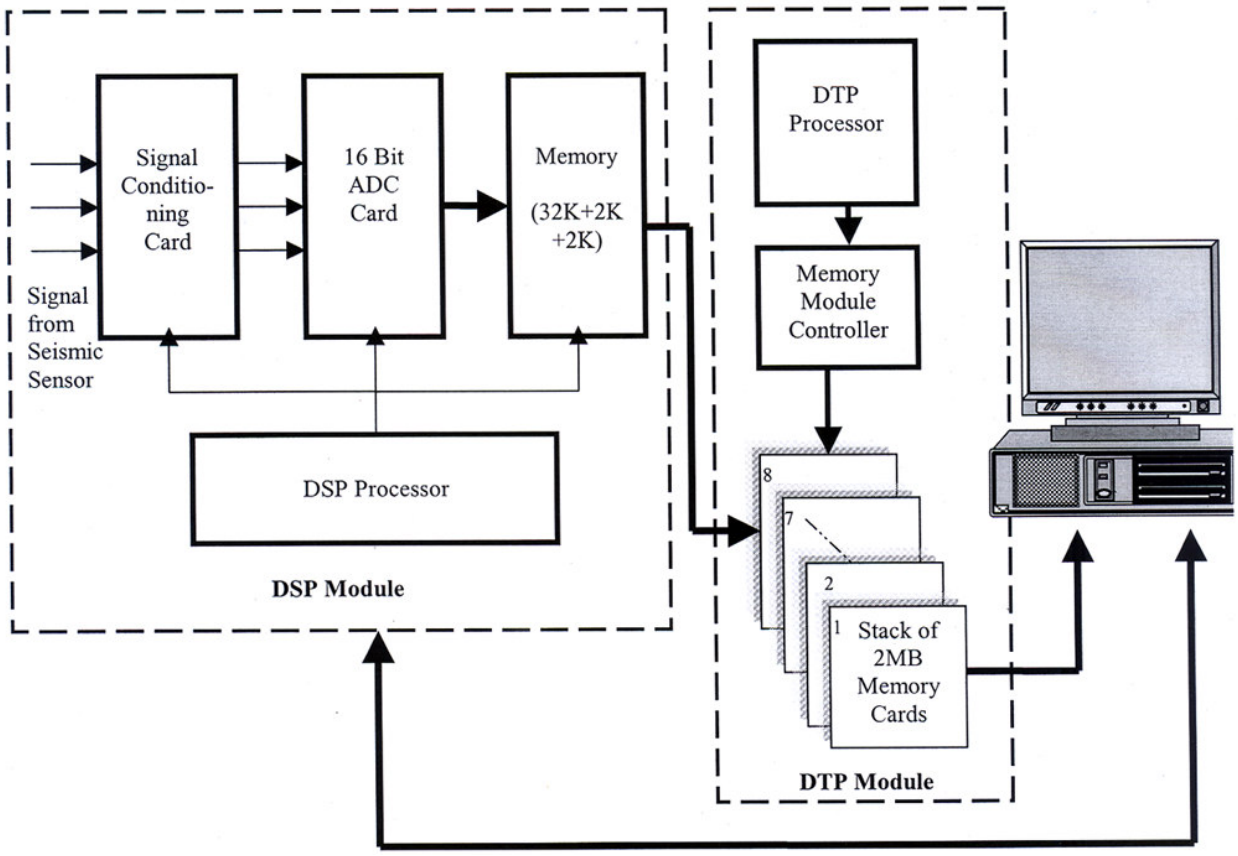


Fig. 1— Block diagram of complete system

DTP card interacts with: i) DSP card for lifting data from the ring memory; ii) Main storage for storing the data retrieved from the ring memory, and iii) laptop for transferring the event data from the main storage to hard disk for offline analysis and interpretation. When the instrument is in operation, the DSP card performs most of the tasks and DTP card remains almost idle. When true event is detected and established by the DSP card, then DTP card becomes operational in parallel with DSP card. DTP card starts collecting independently the data bytes made available by the DSP card from the ring memory at the output port of the assigned 82C55 chip. DTP card picks up the data byte and stores it into the main storage before the arrival of next byte. The data byte transfer from ring memory into memory module (main storage) is done in handshake mode under the control of DTP card.

**Design of Ring Memory**

Pre-event data of some duration is required to understand the changing geophysical/geological conditions immediately before the occurrence of earthquake. Pre- event storage under the control of DSP card is used as ring/circular memory and retains at any moment of time the incoming data, which is equal to one, received in total pre event period. Pre-event time is programmable. In order to realize this design requirement, fresh incoming data sample is written over the current oldest data sample of ring memory and oldest sample is rejected. The address counter is incremented by one for storing the next incoming sample and the same process continues after every 3.3 millisecond till the true event is detected (Fig. 2).

Size of the circular buffer=Number of bytes of ADC*sample rate*Pre-event time
i.e.
Pre-event = 20 sec
Sample rate = 100
16 bit ADC So 3 bytes/sample
Pre-event storage = 20x100x2 bytes = 4000 bytes = 4KB

**Technique for Data Transfer from Ring Memory to Main Storage**

When DSP card declares occurrence of true event by executing STA and LTA algorithm, then the oldest

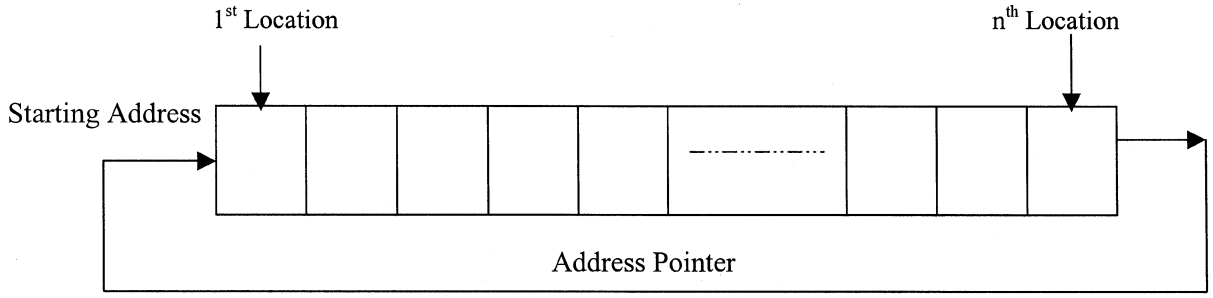


Fig. 2— Ring memory

data sample of the ring memory is first read out and instead of rejecting it as done when event is not true[19], the DSP card sends it at the output port of the assigned PPI device (82C55) under its control. From here, it is picked up by DTP card. After reading out the oldest sample, the new incoming data sample is stored now at this very location. Thereafter, the address counter is incremented to repeat the same process for the next data sample. DTP card, which is waiting for the arrival of data byte from the ring memory (handshake data transfer mode), immediately picks up this data byte and stores it into one of the module of main storage. The process is repeated till the total event data along with the pre-event and post event data is stored into main memory storage.

**Technique for Enhancing Addressing Capability**

The main memory has been configured to provide 16 Mbytes storage by using eight modules of 2 Mbytes capacity each. The 8-bit microprocessor, around which the instrument has been realized, cannot address more than 64 KB locations. Therefore, a methodology has been devised to enhance addressing capability of 80C85 microprocessor from its inherent 64 Kbytes addressing capability to 16 Mbytes through a mix of hardware and software technique. Using the worked out addressing scheme, at any time, only one of the eight modules is selected and only one memory chip is enabled either to read or write one of the 128 Kbytes locations. To select a particular location in 16 M byte location, first of all, the particular module is selected, and then in this module, the very memory chip of 128 Kbyte capacity is selected, and thereafter, the particular location is addressed where one can either write into or read out the data.

Whenever the basic block of 64 Kbytes of the main memory is filled, a pulse is generated through software at the output port of the assigned PPI mounted on DTP card (Fig. 3). This pulse increments a 12 bit binary counter (CD 4040). The output Q2, Q3, Q4, and Q5 of binary counter are connected to a 4-to-16 line decoder (CD4514) to generate 16 output signals. These signals are used to enable 16 memory chips of 128 Kbyte capacity one after the other. The second chip enable line of all the 16 chips are connected together to make one block of 2 MB (128 Kx 16=2048 Kbytes) storage.

To enable the addressing of a module, the output Q6, Q7, and Q8 are connected to another 3 to 8 decoder (74C138) to generate eight output signals (R1-R8). The second chip selects of all the 16 memory chips are shorted together to provide one common point. This common point of each module is connected to one of the 8 output lines produced by 3 to 8 decoder to select/enable one of the 2 M byte modules of 16 M bytes storage. The address of the desired location in selected memory chip is provided by the lines A0 to A15 coming from the 80C85 microprocessor of DTP in association with the line A16 that comes directly from the Q1 output of 12 stage binary counter.

**No Loss Data Assurance**

The data pertaining to a number of true events is stored in digital form into the instrument main storage till the 80 percent of the total space for storage is filled, after which, no more data can be stored in it without making the storage space available in it. For this purpose, the data stored into the main storage is down loaded into the hard disk of a laptop computer. During data transfer, the acquisition and processing of incoming signal is not halted. When 80 percent occupancy of the main storage is detected by the processor of DTP card, then DTP card automatically starts sending out the data in byte serial form from the main storage to its assigned output port. This output port is continuously scanned by the laptop PC to check the availability of data byte at this port and it is picked up immediately and is stored in its hard disk. While the data transfer from main storage to hard disk

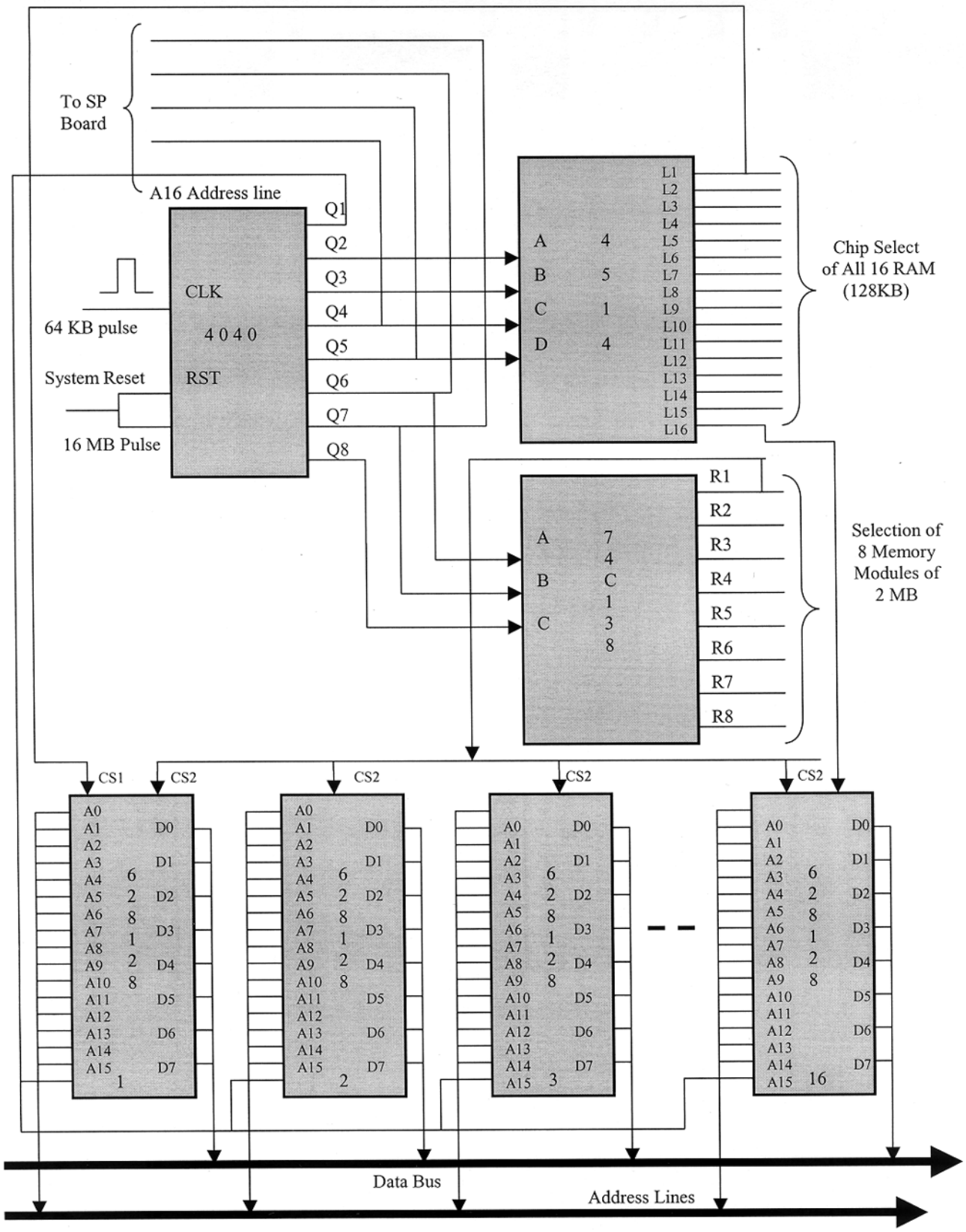


Fig. 3— Expandable memory module up to 16 MB

of PC is being executed by the DTP card, the DSP card keeps on executing its all functions uninterruptedly and independently because of independent microprocessors incorporated in both of these cards. Interrupt structure has been used to schedule the different tasks for data acquisition, processing, storing and its transfer at different levels from ring memory to main memory, and from main memory to laptop hard disk.

## Conclusions

The new digital seismograph has been developed and fabricated as engineered model. The instrument has been tested in the lab and in the field for long duration. The performance of the instrument was found as per design specifications and user's satisfaction. To handle the large dynamic range of seismic signal, it is suggested that a high-resolution digitizer may be incorporated. Due to the technical limitations of microprocessor-based instruments, PC architecture based instruments are to be developed with GPS (Global Positioning System) synchronization.

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