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Capacitor Voltage Balancing Algorithm with Redundant Level Modulation for a Five Level Converter with Reduced Device Count

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***Abstract*— A new five-level multilevel converter topology with a reduced device count has been brought up for medium-voltage inverter applications. However, as an inherent issue of this simplified topology, the voltage balancing of flying capacitors is challenging. Conventional approach utilizing redundant switching states cannot achieve the balancing under a unity power factor and high modulation indexes. This paper proposes a novel voltage balancing algorithm to solve this issue, which is based on Redundant Level Modulation (RLM). The proposed algorithm is verified by simulation and experiment. This novel voltage balancing scheme overcomes the limitations of the conventional approach and enables this topology to operate at high power factors and high modulation indexes.**

Keywords—multilevel converter, flying capacitor, voltage balancing, 5 level, redundant level modulation

I. INTRODUCTION

Compared to the two-level converter, multilevel converters have a number of attractive merits, such as higher voltage handling capability and lower switching loss and harmonic distortion. Therefore, they are widely used in various industrial applications. The most typical multilevel topologies include the neutral-point-clamped (NPC) converter [1], the flying capacitor (FC) converter [2] and the cascaded H-bridge (CHB) converter [3]. In the past decades, researchers have actively developed various multilevel converter topologies for medium-voltage applications, such as the five-level active NPC (5L-ANPC) converter [4], five-level hybrid-clamped (5L-HC) converter [5] and five-level nested neutral-point-piloted (5L-NNPP) converter [6]. Recently, a novel derivation of five-level topologies is brought in [7], which is based on three flying capacitors and offers a reduced device count, i.e. 8 devices per phase. However, as an inherent issue of this simplified topology, the voltage balancing of flying capacitors is challenging. Conventional approaches, e.g. utilizing redundant switching states cannot achieve the balancing under high power factors and high modulation indexes.

To address the voltage balancing challenge in this topology, this paper presents a novel voltage balancing algorithm based on Redundant Level Modulation (RLM). The concept of RLM is utilizing an extra output voltage level in one switching cycle to gain extra controllability over capacitor voltages, which only alter the high-frequency behaviour of the converter and does not change the fundamental-frequency output voltage. RLM has been successfully implemented in 3-level and 4-level NPC topologies to improve the voltage balancing performance, as presented in [8], [9]. The following aspects will be elaborated in this paper: (1) the new five-level converter topology and the challenges in balancing its flying capacitors (2) proposed voltage balancing algorithm (3) validation of the proposed scheme in simulation and experiment.

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II. AN EMERGING FIVE LEVEL CONVERTER TOPOLOGY

A. Principles of the novel five-level converter topology

Fig. 1 is the five-level converter proposed in [7]. As shown in Fig. 1, each phase leg of this topology has eight switches (S_1~S_8) and three flying capacitors (C_1~C_3). The required blocking voltages of the switches S_7 and S_8 will be the twice of other switches. In principle, the three flying capacitor voltages must be maintained at a quarter of the DC-link voltage U_{dc}.

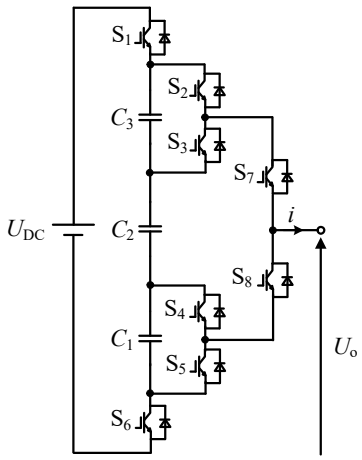


Fig. 1. A 5-level flying-capacitor converter topology with reduced device count proposed in [7].

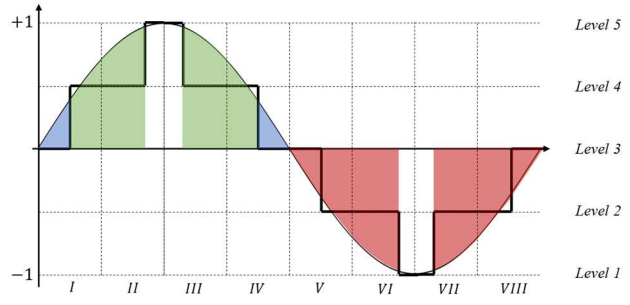
The converter outputs five voltage levels with the switching states shown in Table I, where U_{C1}, U_{C2}, and U_{C3} are the flying capacitor voltages; "↑" denotes the flying capacitor being charged; "↓" denotes the flying capacitor being discharged; "-" shows there is no effect on the flying capacitor; i is the load current, for which the positive direction is defined as flowing out of the converter.

TABLE I SWITCHING STATES AND EFFECTS ON FLYING CAPACITORS

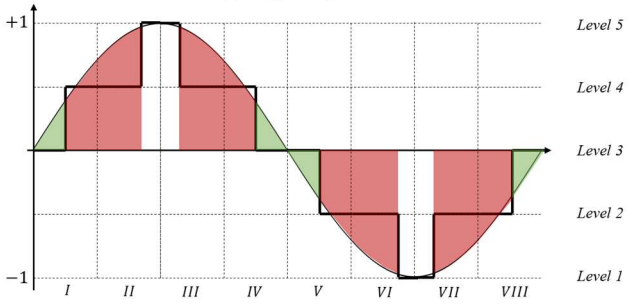
Level	U_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	U_{C3}		U_{C2}		U_{C1}		State
										i>0	i<0	i>0	i<0	i>0	i<0	
5	U_{dc}	1	1	0	0	0	0	1	0	-	-	-	-	-	-	L5
4	$3U_{dc}/4$	1	0	1	0	0	0	1	0	↑	↓	-	-	-	-	L4-2
		0	1	0	0	0	1	1	0	↓	↑	↓	↑	↓	↑	L4-1
3	$U_{dc}/2$	1	0	0	1	0	0	0	1	↑	↓	↑	↓	-	-	L3-2
		0	0	1	0	0	1	1	0	-	-	↓	↑	↓	↑	L3-1
2	$U_{dc}/4$	1	0	0	0	1	0	0	1	↑	↓	↑	↓	↑	↓	L2-2
		0	0	0	1	0	1	0	1	-	-	-	-	↓	↑	L2-1
1	0	0	0	0	0	1	1	0	1	-	-	-	-	-	-	L1

B. *Limitations of the ordinary flying capacitor balancing scheme based on redundant switching states*

For normal functioning of the converter, all flying capacitor voltages need to be balanced at $U_{dc}/4$. As the common approach, selecting the appropriate redundant switching states can achieve directional voltage balancing, as demonstrated in [7]. As shown in Table I, *Level 5* and *Level 1* have only one switching state respectively. *Level 4, 3* and *2* have two redundant switching states respectively. For example, when the converter outputs *Level 4*, the redundant switching states L4-2 and L4-1 have opposite effects on the flying capacitor C_3. Depending on the deviation of capacitor voltages and load current direction, the voltage of C_3 can be balanced by selecting 4-2 or 4-1. However, the controllability of this method is limited, and the voltage of C_2 is difficult to balance at high modulation index (e.g. M = 1) and high power factor (e.g. $cos\ \varphi > 0.7$).



(a) Upper capacitor C_3



(b) Middle capacitor C_2

Fig. 2. Energy change of capacitors C_3 and C_2 with ordinary modulation ($cos\ \varphi$ = 1).

To demonstrate this issue, Fig. 2 shows the energy change of capacitors C_3 and C_2 under unity power factor in one fundamental cycle. The condition of C_1 is symmetric to C_3 and therefore it is not shown. Considering the output voltage and load current, the operation region of the converter is illustrated in eight regions (I ~ VIII) in Fig. 2, in which each region represents one switching cycle. For example, in the region I in Fig. 2 (a), the converter outputs two voltage levels with ordinary modulation, *Level 4* and *Level 3*. In this case, *Level 3* either charges the upper flying capacitor C_3 or has no effect on C_3 depending on the selection of switching states (L3-2 or L3-1). Therefore, in region I, selecting the redundant switching states in *Level 3* only has a unidirectional control of U_{c3}, i.e. charge or no change.

In Fig. 2 (a), regarding the outer capacitors C_3 and C_1, the following observations can be made: (1) the voltages of C_3 and C_1 are bidirectionally controllable in half of a fundamental cycle where the load current is high (see the green areas) (2) the energy charge/discharge of C_3 and C_1 can be balanced over a fundamental cycle if the blue + green area is controlled to be equal to the red area by selecting redundant switching states.

In Fig. 2(b), the following observations can be made regarding the middle capacitor C_2: (1) the voltage C_2 is bidirectionally controllable only when the load current is low (see the green areas) (2) the energy charge/discharge of C_2 cannot be balanced over a fundamental cycle by selecting redundant switching states, because there are only discharging states (see the red areas) at a high load current.

In short, the balancing of C_2 is the main problem in this case. With ordinary modulation and selection of redundant switching states, the middle capacitor will constantly discharge and not be able to maintain the voltage of $U_{DC}/4$, especially at unity power factor. This theoretical analysis explains why [7] only shows the capacitors balanced at a low power factor of $cos\ \varphi \leq 0.7$ while proposing this topology.

III. PROPOSED VOLTAGE BALANCING CONTROL

A. *Redundant level modulation*

To solve the voltage balancing problem in this topology, a novel approach is proposed in this paper, which utilizes the Redundant Level Modulation (RLM). RLM has been successfully implemented in three-level and four-level converters for voltage balancing [8], [9]. The concept of RLM is illustrated in Fig. 3, in which an additional voltage level (the redundant level) is introduced in each switching window to gain extra controllability. The redundant voltage level only serves the purpose of voltage balancing and does not affect the synthesized

low-frequency output voltage. As shown in Fig. 3, in region II, the existence of the redundant *Level 3* introduces a period of time where the bidirectional control of C_2 is gained (green area), which does not exist in Fig. 2(b).

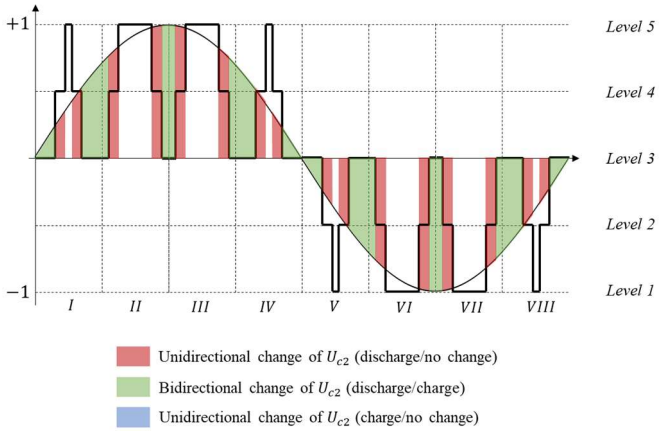


Fig. 3. Illustration of Redundant Level Modulation to balance the middle flying capacitor C_2 ($cos\ \varphi = 1$).

Fig. 4 shows the implementation of RLM with level shifted carriers, which is a popular modulation scheme in multilevel converters due to its simplicity. Similar to [9], the RLM operation is realized by split the modulating waves and inject an offset signal U_{off} >0 in two adjacent modulating waves to generate the additional voltage level. As can be seen in Fig. 4, the converter outputs one additional voltage level in U'_o while the total volt-time of the switching window is the same as U_o.

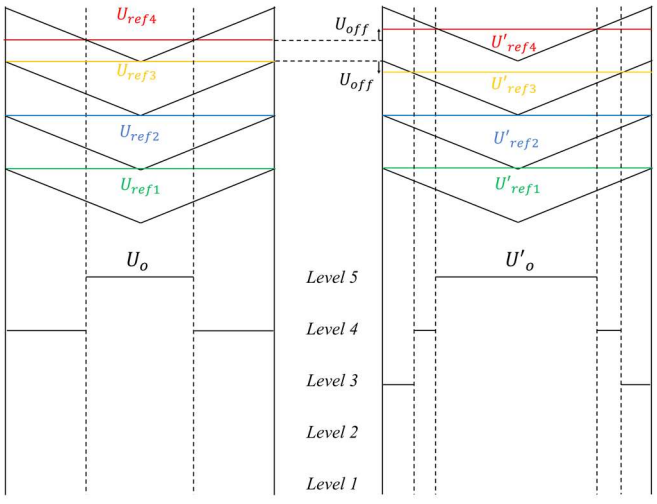


Fig. 4. Illustration of RLM implemented in level shifted carriers (U_{ref}>0).

The drawback of RLM is the additional switching transitions, which lead to increased switching losses and increased high-frequency harmonics. But, multilevel converters generally operate at a lower switching frequency and reduced dv/dt that would moderate the increased switching loss.

When the RLM is activated, the algorithm needs to calculate the offset voltage U_{off} in Fig. 4 to apply the suitable compensation, which is determined by the measured capacitor voltage deviations. The deviation of the capacitor voltages ΔU_{c1}, ΔU_{c2}, ΔU_{c3} are defined as

$$\Delta U_{C3} = U_{C3-\mathrm{ref}} - U_{C3}$$

$$\Delta U_{C2} = U_{C2-\mathrm{ref}} - U_{C2} \quad (1)$$

$$\Delta U_{C1} = U_{C1-\mathrm{ref}} - U_{C1}$$

Where U_{c3}, U_{c2}, U_{c1} are the measured capacitor voltages; $U_{c3\text{-ref}}$, $U_{c2\text{-ref}}$, $U_{c1\text{-ref}}$ are the reference voltages, which are normally defined at $U_{dc}/4$.

Considering all the possible switching states, the change of the capacitor voltages within one switching cycle can be expressed as

$$\Delta u_{C3} = \frac{I \cdot (D_{4-2} - D_{4-1} + D_{3-2} + D_{2-2})}{C \cdot f_{sw}} \quad (2)$$

$$\Delta u_{C2} = \frac{I \cdot (-D_{4-1} + D_{3-2} - D_{3-1} + D_{2-2})}{C \cdot f_{sw}} \quad (3)$$

$$\Delta u_{C1} = \frac{I \cdot (-D_{4-1} - D_{3-1} + D_{2-2} - D_{2-1})}{C \cdot f_{sw}} \quad (4)$$

Where C is the capacitance of C_1, C_2 and C_3; f_{sw} is the carrier frequency; I is the instantaneous load current; D is the duty ratio of one switching state, e.g. $D_{4\text{-}2}$ is for state L4-2 in Table I.

As an example, when (U_{ref}>0), the levels L5, L4-1, L3-2 are used to synthesis the reference voltage. Therefore, the modified duty ratios of these three voltage levels must satisfy the following equation

$$D'_5 + \frac{1}{2} D'_{4-1} = U_{ref} \quad (5)$$

Additionally, the duty ratios must add up to one cycle as

$$D'_5 + D'_{4-1} + D'_{3-2} = 1 \quad (6)$$

To pull the middle capacitor deviation to zero, the three selected duty ratios (D_5, $D_{4\text{-}1}$, $D_{3\text{-}2}$) can be solved from equations (3)(4)(5), which yields the reference duty ratio of the middle level $D'_{4\text{-}1}$ in this case as

$$D'_{4-1} = \frac{2 \cdot (-\Delta U_{C2} \cdot C \cdot f_{sw} + I - I \cdot U_{ref})}{3 \cdot I} \quad (7)$$

It should be noted that the calculated $D'_{4\text{-}1}$ can be unfeasible because it intends to pull back the imbalance ΔU_{c2} within one

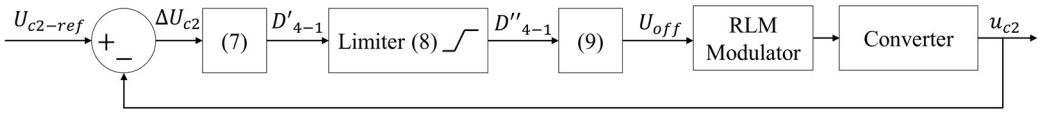


Fig. 5. Closed-loop control of middle capacitor voltage with RLM implemented (U_{ref}>0).

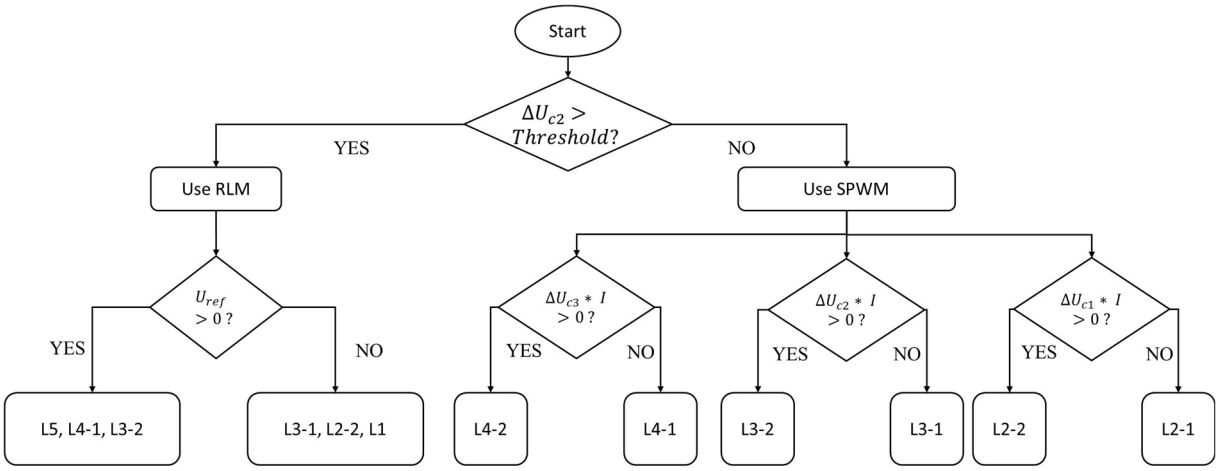


Fig. 6. Voltage balancing algorithm utilizing both redundant switching states and redundant voltage level.

switching cycle. By observing Fig. 4, it can be seen that the duty ratio of the middle level can only be reduced from Fig. 4(a) to Fig. 4(b), which should not be increased, while maintaining the same volt-time product. Therefore, the final achievable duty ratio $D''_{4\text{-}1}$ must be less than the original $D_{4\text{-}1}$. Additionally, $D''_{4\text{-}1}$ must be greater than zero to maintain the multilevel operation. If $D'_{4\text{-}1}$ equals zero, it leads to the skip of *Level 4* where the output voltage jumps from *Level 5* straight to *Level 3*. In practice, the minimum value of $D''_{4\text{-}1}$ can be constrained to leave a "dwell time T_{dwell}" to avoid skipping a level. These two constrains are expressed as

$$T_{dwell} \cdot f_{sw} \le D''_{4-1} \le D_{4-1} \tag{8}$$

Based on the geometry relationships in Fig. 4, the offset voltage for RLM in this case is derived with reference to the original middle level duty ratio

$$U_{off} = (D_{4-1} - D''_{4-1})/4 \tag{9}$$

Through the above process, a closed control loop is formed as shown in Fig. 5 that regulates the middle capacitor voltage dynamically when $U_{ref} \ge 0$. When $U_{ref} < 0$, levels L3-1, L2-2, L1 are used and the offset voltage U_{off} is calculated based on the middle level L2-2 in this case. The injections of U_{off} in these two cases are expressed in (10) and (11).

$$\begin{cases} U'_{ref4} = U_{ref4} + U_{off} \\ U'_{ref3} = U_{ref3} - U_{off} \\ U'_{ref2} = U_{ref2} \\ U'_{ref1} = U_{ref1} \end{cases} (U_{ref} \ge 0) \tag{10}$$

$$\begin{cases} U'_{ref4} = U_{ref4} \\ U'_{ref} = U_{ref3} \\ U'_{ref} = U_{ref2} + U_{off} \\ U'_{ref1} = U_{ref1} - U_{off} \end{cases} (U_{x-ref} < 0) \tag{11}$$

This RLM based control can gain extra controllability on top of selecting redundant switching states, which breaks the limitations elaborated in II.B. Qualitatively, the RLM attempts to supress the usage of *Level* 4 and *Level 2*, where the middle capacitor cannot be charged as shown in Fig. 3. By introducing more duration of *Level 3*, the controllable region for middle capacitor is extended, hence the extra controllability. By design, the RLM operation alters the high-frequency behaviour and does not change the volt-time product of one switching cycle. Hence, the fundamental-frequency output of the converter is not affected by RLM and should witness no associated distortions.

It should be highlighted that the presented RLM can only focus on controlling the middle capacitor C_2. If controlling the outer capacitor voltages is also included as the objective, the duty ratios (e.g. $D'_{4\text{-}1}$ in (7)) becomes unsolvable, because the three control objectives, instead of one, along with (5) and (6) will over-constrain the duty ratios.

B. Hybrid voltage balancing scheme

Based on above analysis, a hybrid control algorithm is developed to employ both redundant switching states and redundant voltage levels to achieve the voltage balancing of all three capacitors as shown in Fig. 6. As demonstrated in Section II.B, the balancing of the middle capacitor C_2 is the main challenge in this topology. Therefore, the control of U_{c2} is prioritized in this balancing scheme by introducing a threshold judgement step.

When the deviation of middle capacitor voltage ΔU_{c2} exceeds the threshold, the algorithm applies RLM to balance U_{c2}. When the demand of controlling ΔU_{c2} is moderate, the normal SPWM with selecting suitable redundant switching states is implemented to balance the capacitors. The redundant switching states are selected based on the charge/discharge demand of the capacitors and the polarity of the load current as summarized in Table I. As can be observed in Fig. 2, utilizing *Level 4* is the key of controlling C_3, and *Level 3* is the key of controlling C_2. Therefore, when RLM is not activated, the selection between L4-2 and L4-1 is determined by upper capacitor C_3, and the selection between L3-2 and L3-1 is determined by the middle capacitor C_2. Similarly, the status of C_1 determines the selection between L2-2 and L2-1.

The above introduced approach based on selecting redundant switching states is the conventional scheme, which alone can be effective when the power factor is not high (e.g. $\cos \varphi \leq 0.7$ as shown in [7]). The performance of both the conventional approach and the proposed hybrid scheme will be investigated in the next section.

IV. Validation of the Proposed Voltage Balancing Algorithm

A. Simulation

An Matlab/Simulink model is built to validate the proposed control scheme. The model is based on one phase leg configuration, because this topology is a single-phase topology with three flying capacitors experiencing the power flow only within that phase leg. As a comparison, the DC-link capacitors in Neutral Point Clamped (NPC) topologies [1] are multi-phase capacitors that buffer the sum of power flow in all phases.

TABLE II System Parameters of Simulation

Power Rating	40 kVA
DC-link Voltage U_{DC}	4 kV
Carrier Frequency f_{sw}	5 kHz
Fundamental Frequency f_0	50 Hz
Load Current	40 A peak
Flying Capacitors	2 mF
Power Factor $\cos \varphi$	0 ~ 1
Modulation Index	0 ~ 1

The simulation results are shown in Fig. 7 at full modulation index and unity power factor. When the ordinary modulation is implemented, the middle flying capacitor cannot be well controlled, and its voltage goes down due to discharging. This issue is explained in Section II.B as the limitation of selecting redundant switching states to balance the capacitors in this topology. When the proposed RLM scheme is enabled, the middle capacitor voltage is pulled back to the reference value, and all three flying capacitor voltages are successfully balanced when it enters the steady state. As can be seen from Fig. 7, the output voltage starts to jump between three voltage levels when RLM is enabled. This performance proves the proposed voltage balancing scheme to be effective. The scheme enables this topology to operate at a high modulation index and a high power factor without the capacitor voltages drifting away.

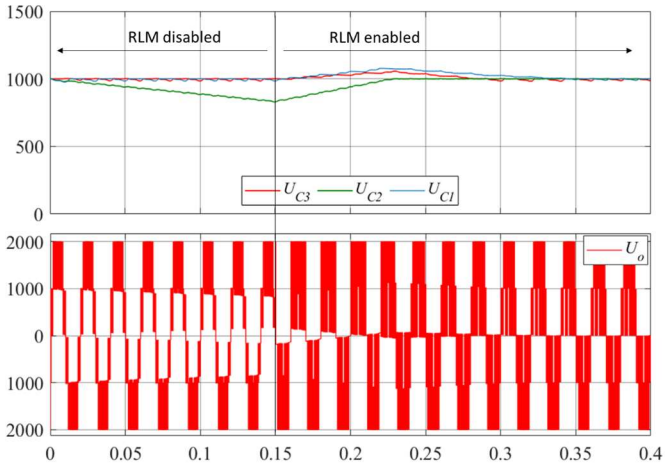
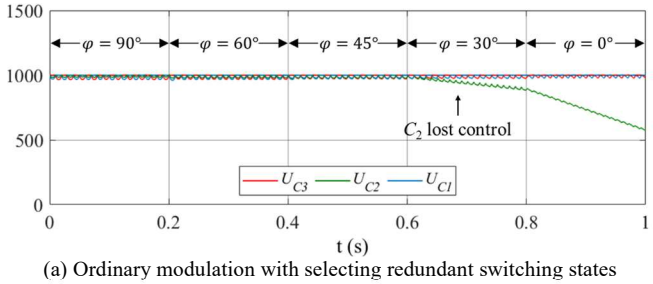
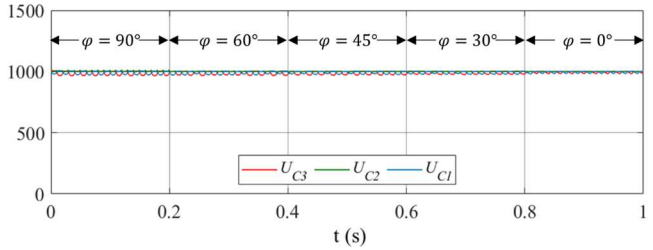


Fig. 7. Capacitor voltage and converter output voltage U_o without/with the proposed RLM ($M = 1$, $\cos \varphi = 1$).

To further demonstrate the limitation of conventional voltage balancing scheme, the capacitor voltages against the load power factor angle φ is captured in simulation and plotted in Fig. 8. As shown in Fig. 8(a), at lower power factor, selecting redundant switching states is effective in voltage balancing. When the power factor angle decreases to less than 30°, the ordinary scheme loses the controllability of C_2 and it starts to discharge. On contrary, the proposed RLM can effectively balance capacitor voltages even at unity power factor as shown in Fig. 8(b). It should be highlighted that the outer capacitors C_3 and C_1 still see low-frequency voltage ripples in this case, although the energy charge and discharge are balanced over one fundamental cycle. The reason is demonstrated in Fig. 2(a) that the outer capacitor voltage is not controllable in half of the fundamental cycle. In the illustration, the C_3 discharges when the load current is negative, but the energy can be pulled back in the positive cycle by selecting the suitable redundant switching states. This can be considered a limitation of the proposed voltage balancing scheme, that the outer capacitors need larger capacitance to supress the low-frequency ripples.



(a) Ordinary modulation with selecting redundant switching states



(b) Proposed voltage balancing scheme based on RLM

Fig. 8. Capacitor voltages in simulation ($M = 0.9$).

Fig. 9 illustrates a zoomed-in view of the converter output voltage U_o, which shows that the converter outputs three voltage levels, instead of two, in the marked intervals within the fundamental cycles. This operation is intended by the proposed RLM for voltage balancing purpose.

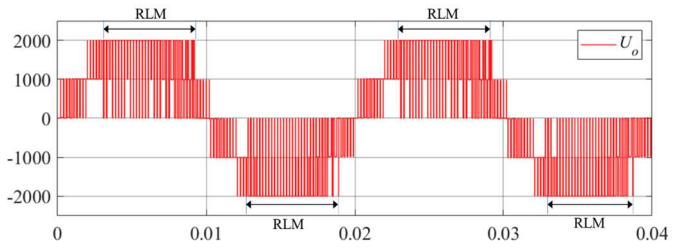


Fig. 9. Zoomed-in converter output voltage U_o (M = 0.9, $cos\ \varphi$ = 1).

B. Experiment

A single-phase downscaled prototype based on this topology is designed and built. The specifications of the test rig are listed in Table III. The prototype is connected to a DC-link supply and a RL load to verify the proposed voltage balancing algorithm. The load is connected between the output node in Fig. 1 and the DC-link neutral point. The algorithm is programmed in a Digital Signal Processor (DSP) TMS320F28335. The ΔU_{c2} threshold in Fig. 6 is set as 0.5 V.

TABLE III TEST RIG SPECIFICATIONS AND COMPONENTS

DC-link voltage U_{DC}	120 V
Carrier frequency f_{sw}	5 kHz
Fundamental frequency f_0	50 Hz
Flying capacitors	B43508A9180M (EPCOS, 1000μF/400V)
Current sensor	LA55-P (LEM)
Voltage sensor	LV25-P (LEM)
R	11 Ω
L	5 mH

Fig. 10 shows a picture of the built converter prototype with three flying capacitors.

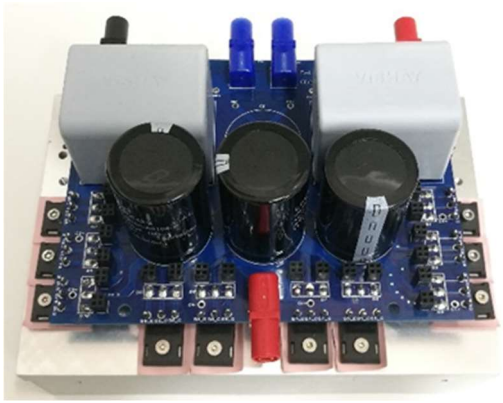


Fig. 10. Built single-phase five-level converter prototype.

Operating the converter at M = 1 and $cos\ \varphi$ = 0.99, Fig. 11 shows the converter output voltage U_o and the load current I_{load}. It is visible that the output voltage has five voltage levels as a result of balanced flying capacitors, and it shows the RLM operation similar to Fig. 9. The load current is sinusoidal with no visible low-frequency distortion. Note the measured converter output voltage is referenced to the dc-link neutral point voltage due to the single-phase configuration, where the other end of the load is connected back to the dc-link neutral point created by two dc-link capacitors in series. Since the dc-link neutral point voltage sees a low-frequency oscillation as a result of the fundamental-frequency load current (power), it is noticeable that the top and bottom of the output voltage is not flat, which do not exist in a three-phase configuration.

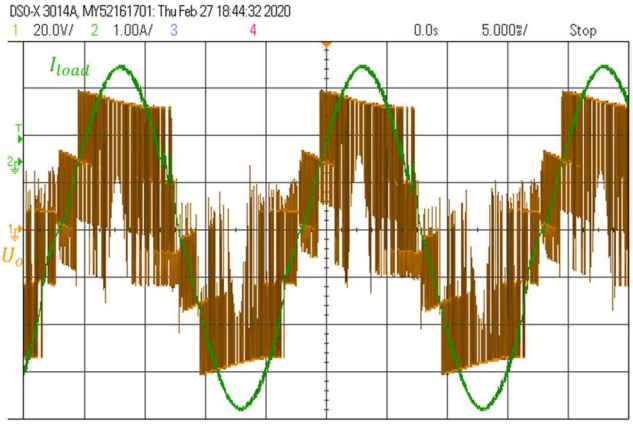


Fig. 11. Measured converter output voltage and load current (M = 1).

Fig. 12 shows the dynamic performance of the closed-loop control. The reference voltages of the capacitor are step-changed to arbitrary values from U_{DC}/4 for 200 ms and set back to 30 V afterwards. It can be seen that the capacitor voltages well follow the control command, which proves the proposed closed-loop control is effective. It should be highlighted that this effective dynamic performance is also achieved at full modulation index and high power factor.

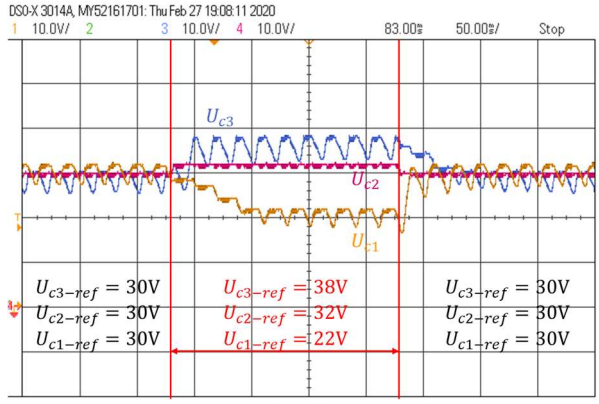


Fig. 12. Dynamic performance of closed-loop control (M = 1).

V. CONCLUSION

This work has proposed a novel voltage balancing algorithm for a emerging five-level converter topology with three flying capacitors and 8 devices per phase. The challenge of achieving voltage balancing of this topology at high power factor has been demonstrated through analyzing the charge/discharge states of the capacitors. The main difficulty is to keep the middle capacitor from discharging so that the converter can normally

output five voltage levels. Conventional approach that selects the redundant switching states cannot maintain the controllability when the power factor is high, which limits the practicability of this topology. This limitation is confirmed by the theoretical analysis and simulation.

To address the voltage balancing issue, this work proposes a novel algorithm that employs Redundant Level Modulation to gain extra controllability of the flying capacitor voltages. The proposed control scheme overcomes the limitation of conventional approach based on selecting the redundant switching states. Simulations and experiments have confirmed the effectiveness of the proposed algorithm. This algorithm enables the novel topology to operate at unity power factor and high modulation index without the capacitor voltages drifting away. The presented Redundant Level Modulation can also be implemented on other multilevel converter topologies.

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