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Characterizing Threshold Voltage Shifts and Recovery in Schottky Gate and Ohmic Gate GaN HEMTs

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***Abstract*—Threshold voltage shift in normally-OFF GaN High Electron Mobility Transistors (HEMTs) is an important reliability concern in GaN devices. Differences in device architecture between Schottky gate and Ohmic gate normally-OFF GaN HEMTs means that there are important differences in the physical mechanism behind threshold voltage shift due to gate stress. In this paper, a non-intrusive technique for the characterization of threshold voltage shift is applied to both technologies. The technique relies on using a sensing current to measure the third quadrant voltage before and after gate-voltage stress. The results show that in Schottky Gate GaN HEMTs, a positive threshold voltage shift occurs at low gate stress voltages due to electron trapping in the GaN/AlGaN interface while at higher gate stress voltages, the threshold voltage shift becomes negative due to hole trapping and accumulation. The stress time has a fundamental role on the measured threshold voltage shift at medium gate voltage levels and pulsed gate stresses are able to capture this phenomenon. For the Ohmic Gate GaN HEMTs, only a negative threshold voltage shift is observed for all stress currents with no apparent shift as the junction temperature is increased.**

***Keywords*—GaN HEMT, Threshold Voltage Instability**

I. INTRODUCTION

GaN power devices have become commercially available for power conversion in the sub-650V market. GaN devices are well recognized for their ultra-fast switching rates and good conduction losses [1, 2]. The good performance of GaN High Electron Mobility Transistors (HEMTs) is due to the two-dimensional electron gas (2DEG) formed at the AlGaN/GaN interface. This 2DEG contains high mobility electrons shielded from various scattering mechanisms typically present in typical inverted MOS channels. The commercially available devices in the 650 V application range are lateral devices with two main gate structures for achieving normally-OFF operation: (i) p-GaN gate on AlGaN with an ohmic contact [3] and (ii) p-GaN gate on AlGaN with a Schottky contact [4]. The two GaN HEMT device structures and gate stacks are shown in Fig. 1.

Commercially available GaN HEMTs have been the subject of different studies including electrothermal characterization [5-7]and reliability studies (summarized in [8]), with a JEDEC committee (JC-70) focused on the development of standards for GaN power devices [9, 10]. The reliability studies include power cycling [11-13], dynamic ON-state resistance [14-16] and threshold voltage (V_{TH}) instability [17-23], which is the focus of the investigations presented in this paper.

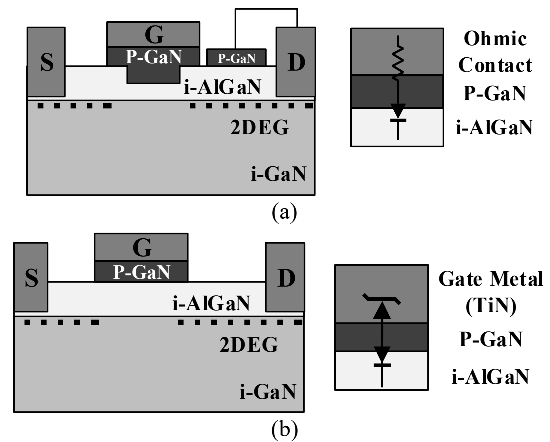

Fig. 1 Device and gate stack structures, adapted from [2-4]
(a) Ohmic Gate GaN HEMT (b) Schottky Gate GaN HEMT

The previous studies [17-23] highlight the complexity of the gate stack structure and different threshold voltage shifts depending on the magnitude of the gate stress voltage. For example, in Schottky gate GaN devices, positive V_{TH} drift at low gate voltage V_{GS} bias has been reported due to electron trapping in acceptor like states at the AlGaN/GaN interface [21, 24]. For Schottky gate GaN HEMTs, electron trapping at the interface yields a net negative charge in the p-GaN layer thereby resulting in a positive V_{TH} shift since more voltage is required to create the 2DEG. The magnitude of the V_{TH} shift depends on the magnitude of trapped electrons. However, as the V_{GS} stress is increased, the V_{TH} shift changes from positive to negative due to hole trapping and accumulation at the GaN/AlGaN interface [21]. At higher V_{GS} bias, the PiN diode in the gate stack becomes forward biased with hole injection from the p-GaN gate into the AlGaN layer and electron injection in the reverse direction.

This paper introduces a novel technique for characterizing V_{TH} shift in GaN HEMTs using the third quadrant characteristics. Section II presents the experimental setup and the third quadrant operation in GaN HEMTs, section III introduces the technique while section IV presents the threshold voltage instability study results for both gate technologies as function of the stress level, duration and temperature. Section V presents the use of the novel methodology for the evaluation of pulsed gate stresses and negative gate stresses and section VI concludes the paper.

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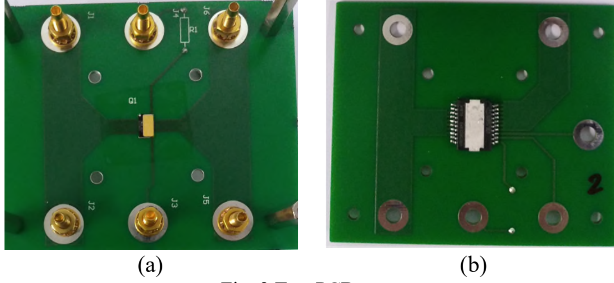
II. Third Quadrant Characteristics in GaN HEMTs

A. Experimental Prototypes

Two commercially available normally-OFF GaN HEMTs have been studied in this paper a 600V/31A Ohmic Gate GaN HEMT from Infineon with datasheet reference IGOT60R070D1 and a 650V/30A GaN HEMT from GaN Systems, with datasheet reference GS66508T. The gate of this device has been identified as a Schottky Gate in [22], although there is no gate structure description available from the manufacturer, as stated in [1, 5]. Fig. 2 shows the PCB prototypes that have been designed for testing both GaN HEMTs.



(a) (b)

Fig. 2 Test PCBs
(a) Schottky Gate GaN HEMT (b) Ohmic Gate GaN HEMT

The selected devices have a thermal pad on the top, which allows the use of a heatsink/heater for controlling the temperature of the device during the tests. The heater and its connection to the Ohmic Gate GaN HEMT is shown in Fig. 3. The terminals of the PCBs are accessible using 4 mm banana connectors, allowing an easy connection with the characterization equipment.

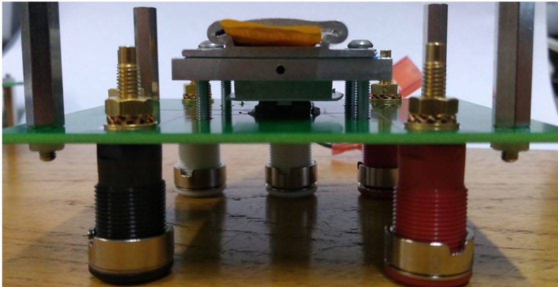


Fig. 3: Detail of the DC heater connection

B. Third Quadrant Characterization

GaN HEMTs, like silicon and SiC MOSFETs, are capable of reverse conduction, however, unlike MOSFETs, they do not have an inherent body diode.

The mechanism of reverse conduction is called self-commutating reverse conduction [1]. The device can be considered symmetric [1] and when a gate-source voltage V_{GS} greater than the gate-source its threshold voltage $V_{GS\text{-}TH}$ is applied, there is current conduction. Similarly, when a gate-drain voltage V_{GD} higher than the gate-drain threshold voltage $V_{GD\text{-}TH}$ is applied to the device, there is also current conduction. If the device is reverse biased V_{GD} is given by (1) [1].

$$V_{GD}=V_{GS}-V_{DS} \tag{1}$$

If this value is higher than the threshold voltage, the device turns ON and the resulting third quadrant voltage V_{SD} can be calculated using (2).

$$V_{SD}=V_{GD\text{-}TH}-V_{GS}+I\cdot R_{SD} \tag{2}$$

The value of $V_{GD\text{-}TH}$ can be considered equal to $V_{GS\text{-}TH}$ [1] and at low currents the voltage drop across the source-drain resistance is negligible, hence (2) can be rewritten as (3).

$$V_{SD}=V_{GS\text{-}TH}-V_{GS} \tag{3}$$

Using (3), if V_{GS}=0 the measured V_{SD} can be considered equal to V_{TH} ($V_{SD}\approx V_{TH}$) [1]. This has been verified for both GaN HEMTs and the results are shown in Table I. The threshold voltage was measured forcing a current of 10 mA through the device with $V_{GS}=V_{DS}$ [25] using a source-measurement unit model 2602B from Keithley.

TABLE I: Measured V_{SD} and V_{TH} at Ambient Temperature

	V_{TH} (V)	V_{SD} (V)
Ohmic Gate HEMT	1.478	1.483
Schottky Gate HEMT	1.597	1.576

Additionally, if a negative gate voltage is used for turning OFF the device, the value of V_{SD} increases. This is shown in Fig. 4 for the Ohmic Gate GaN HEMT.

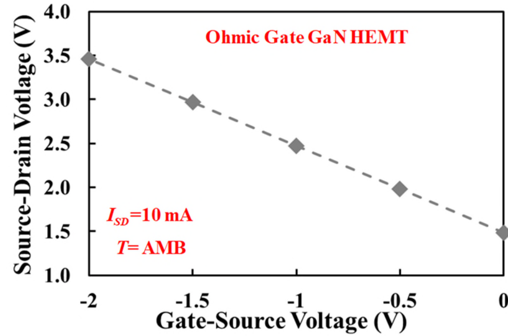


Fig. 4: Impact of negative gate-source voltage on the source-drain voltage during reverse conduction of current

III. Threshold Voltage Instability Characterization Methodology

In [26-28], it was shown how the third quadrant characteristics of SiC MOSFETs can be used as an indicator of V_{TH} for tracking the peak shift and recovery of V_{TH} after gate stress. In the case of SiC MOSFET, the methodology is based in the relationship between V_{TH} and V_{SD} at low currents when V_{GS}=0. It was show that a calibration relationship is required for the application of this method.

In the case of GaN HEMTs, that relationship already exists, as demonstrated in section II. Hence, this methodology can be applied to GaN HEMTs for evaluating threshold voltage instability resulting from gate stress. The circuit is shown in Fig. 5 and it is similar to the circuit used for measuring the junction temperature using V_{SD} [29].

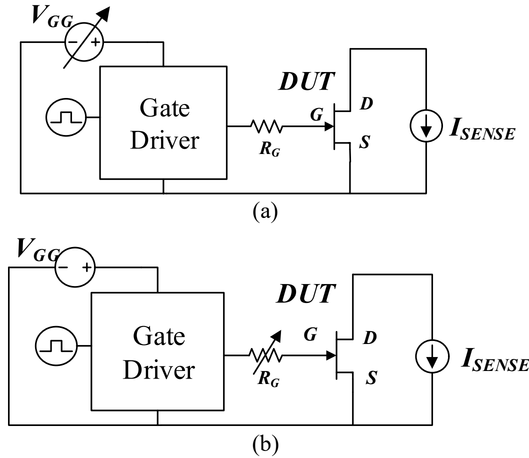


Fig. 5 Electrical schematic for gate stress and characterization using third quadrant characteristics (a) Gate voltage stress (b) Gate current stress

It consists of a current source that forces a small reverse sensing current I_{SENSE} through the GaN HEMT, which is the Device Under Test (DUT), and a gate driver that is used for stressing the gate of the device. As the gate structures are different, in the case of the Schottky gate GaN HEMT, the gate stress voltage is adjusted by varying the gate driver supply voltage V_{GG} and keeping the gate resistance R_G at a fixed value (voltage stress), whereas in the case of the Ohmic Gate GaN HEMT the gate driver supply voltage was fixed and the gate current (current stress) was adjusted by means of varying the gate resistance. Both circuits are shown in Fig. 5.

The operation of the circuit and the methodology is shown in Fig. 6 for the Schottky Gate GaN HEMT and a gate stress of 3 V during 10 s at ambient temperature. The value of the sensing current I_{SENSE} is 10 mA. In the pre-stress stage, the V_{GS}=0 and $V_{SD} \approx V_{TH}$. The current flows through the device by means of self-commutated reverse conduction. During the stress phase (5 s to 15 s), a positive gate voltage is applied to the device and the channel conduction is enabled. The resistance of the device is low, resulting in a low voltage drop. When the stress is removed, V_{GS}=0 and the current flows through the device by means of self-commutating reverse conduction again, hence the

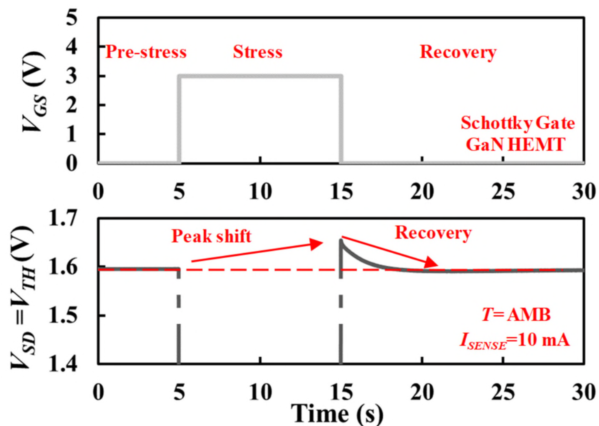


Fig. 6 Operation of the method for a Schottky Gate GaN HEMT. Stress Voltage: 3 V, Stress Time: 10 s, Ambient temperature

measured $V_{SD} \approx V_{TH}$. During this phase there is an increase of V_{SD}, indicating a positive shift of V_{TH} followed by a recovery transient after the stress removal, where V_{TH} returns to its pre-stress value. Since V_{SD} is approximately equal to V_{TH} when V_{GS}=0, the measured V_{SD} can be used for characterizing the peak shift and recovery of V_{TH} after stress removal according to charge trapping and de-trapping.

IV. Single Pulse Gate Stresses

This section presents the application of the proposed methodology for the Schottky Gate GaN HEMT and the Ohmic Gate GaN HEMT at different gate stress levels, evaluating the impact of the stress duration and temperature.

A. Schottky Gate GaN HEMT

For evaluating the Schottky Gate GaN HEMT, the circuit in Fig. 5(a) was used. The sensing current I_{SENSE} was 10 mA and the stress voltages selected were 3 V, 5.5 V and 7.5 V. These stresses were applied for 1s, 10 s and 100 s and the role of temperature was investigated by performing the tests at ambient temperature (22 °C) and high temperature (150°C). Between each stress-characterization sequence there was a recovery time of 40 minutes for allowing the V_{TH}(V_{SD}) to return to its pre-stress value.

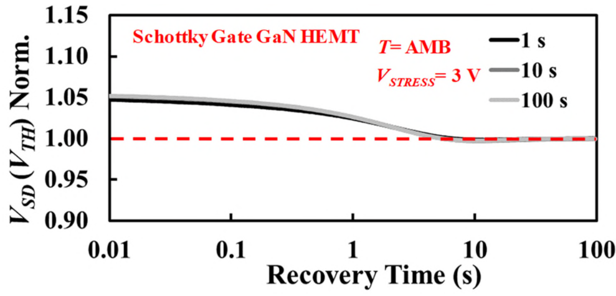
The results at ambient temperature are presented in Fig. 7 and they show that the stress voltage plays a key role on the measured V_{SD}(V_{TH}) shift. The measurements were done using an oscilloscope model TDS5054B from Tektronix. For easy comparison, the values are normalized respect to the measured pre-stress V_{TH} (V_{SD}) and plotted using a logarithmic time scale, where t=0 is defined for the peak V_{TH} shift.

Considering the 3 V gate stress in Fig. 7(a), the Schottky Gate GaN HEMT exhibits a positive threshold voltage shift, which is in agreement with [18]. This positive V_{TH} shift is caused by trapping of electrons in the AlGaN/GaN interface [18]. For the stress durations evaluated (1s to 100 s) there is no significant impact of the stress time on the threshold voltage shift, which is around +5%. The recovery to the pre-stress value is in the range of 5-10 s.

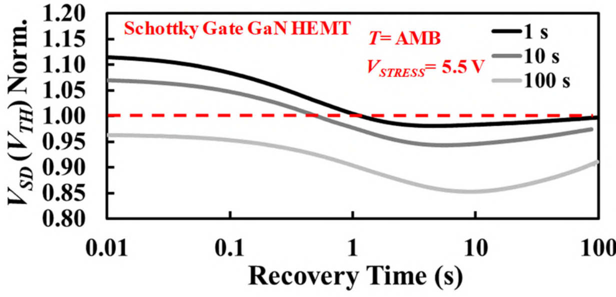
Fig. 7(b) shows the results for V_{STRESS}=5.5 V, where it can be observed that the stress duration has a key role. For a stress duration of 1 s, the Schottky Gate GaN HEMT exhibits a positive peak shift (+11.8%), which recovers to the pre-stress value with a small negative dip (-1.9%).

Increasing the duration of the stress to 10 s, causes a reduction of the peak positive shift to +7.3% as well as a greater negative dip (-5.7%). The recovery after the negative dip is slow, as the results in Fig. 7(b) show. The impact of the stress time becomes more apparent for the 100 s stress measurements. In this case the peak shift is now negative (-3.6%), followed by a fast dip, with a further reduction to -14.7%, and a slow recovery transient to the pre-stress value. In [18] the authors reported similar characteristics for medium gate voltage stresses, identifying three different mechanisms responsible of the different V_{TH} shifts: electron trapping at the AlGaN/GaN interface, hole trapping in the AlGaN barrier and hole depletion.

Fig. 7(c) presents the results for the 7.5 V stress, where it can be seen that the stress duration (in the range of 1 s to 100 s) has



(a)



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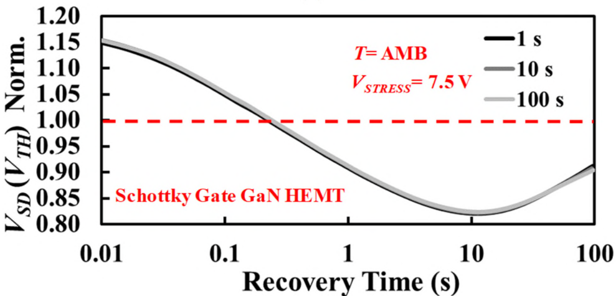
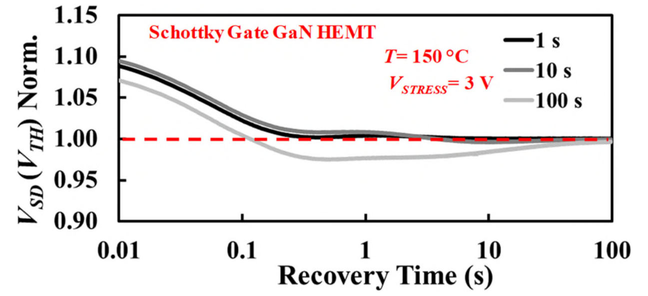
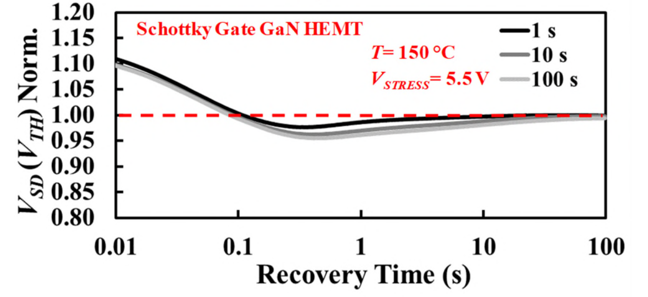


(c)

Fig. 7 Schottky Gate GaN HEMT. Threshold voltage recovery after gate stress. Ambient Temperature
(a) V_{STRESS}= 3 V, (b) V_{STRESS}= 5.5 V, (c) V_{STRESS}= 7.5 V



(a)



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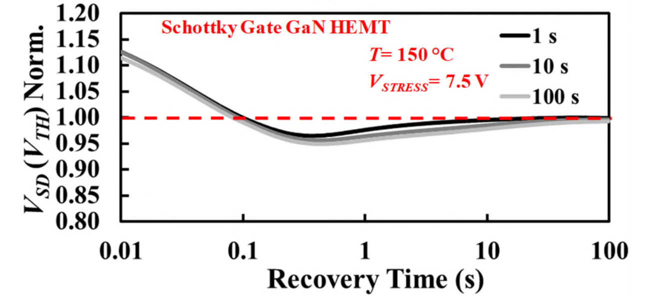


(c)

Fig. 8 Schottky Gate GaN HEMT. Threshold voltage recovery after gate stress. 150 °C
(a) V_{STRESS}= 3 V, (b) V_{STRESS}= 5.5 V, (c) V_{STRESS}= 7.5 V

no impact on the peak shift and recovery transients. For this stress voltage, an initial positive peak shift (+17%) is followed by a negative dip (-18%) and a long recovery transient, which required around 40 minutes for V_{TH} to return to its pre-stress value.

The same gate stresses were performed at 150 °C for evaluating the role of temperature on the V_{TH} shift and recovery. The results are shown in Fig. 8, for stress voltages of 3 V, 5.5 V and 7.5 V, where the values have been normalized respect to the pre-stress value at 150 °C. Evaluating the recovery transients, the most obvious conclusion is that the recovery is highly accelerated by temperature, as it is clearly observed for the 5.5 V and 7.5 V gate stresses, and the negative dip following the initial positive peak shift has reduced to less than -5%. The long recovery transient is also accelerated at 150 °C, with a recovery to the pre-stress value in the range of seconds.

For the gate stress voltages of 5.5 V and 7.5 V, increasing the duration of the stress has no significant impact on the initial positive peak shift, which is higher for the 7.5 V stress (+18%) than the 5.5 V stress (+13%). The negative dip is directly proportional to the stress time and the long recovery transient is slower as the stress time is increased. This is attributed to more slow traps being charged and released.

The results for the gate stress of 3 V at 150 °C show a similar trend to the 5.5 V stress at ambient temperature. The initial positive peak shift reduces from +10.5% for 1 s stress to +8.8% for 100 s stress and a negative dip of -2.5 % is also observed for the stress duration of 100 s.

It is also important to compare the shift at ambient temperature and 150 °C. This has been done for the stress voltage of 5.5 V, which can be considered the nominal gate voltage for this device. At ambient temperature a negative peak shift of -3.6% is observed for a stress duration of 100 s, whereas the same stress at 150 °C causes a positive peak shift of +12.8%. In [18] similar results are reported, which highlight the complexity of GaN HEMTs regarding gate stress and threshold voltage shift characterization. These results may be especially relevant for power cycling of GaN devices, where the devices are subjected to long duration gate voltage biasing.

B. *Ohmic Gate GaN HEMT*

Unlike the Schottky Gate GaN HEMT where the test was done at different voltage levels, in this device the stresses were performed at different current levels using the circuit in Fig. 5(b). This circuit is based in a voltage source gate driver and the current is adjusted by keeping the gate driver supply voltage V_{GG} constant while changing the gate resistance to adjust the stress current I_{STRESS}.

The stress currents selected for evaluating threshold voltage instability on the Ohmic Gate GaN HEMT are 5.2 mA and 73 mA. The continuous gate current rating of this device is 20 mA; hence, one stress is accelerated and other is within the driving range. The selected stress currents result in gate voltages of around 3.2 V and 4 V. The stress and recovery results at ambient temperature are show in Fig. 9.

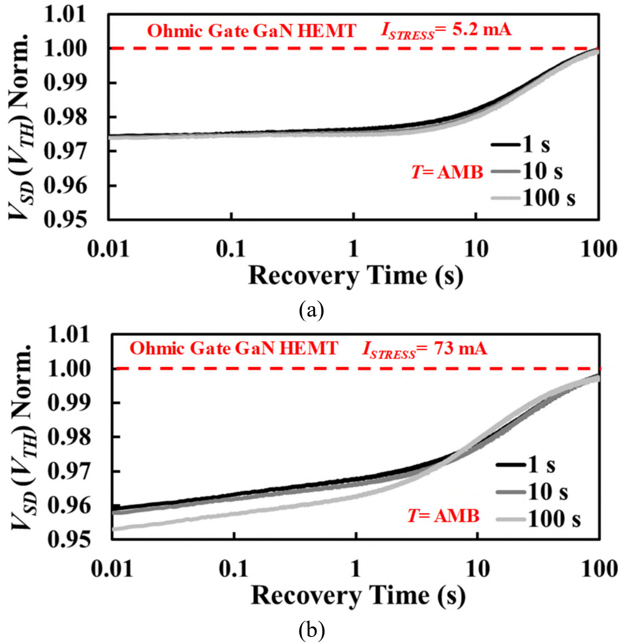


Fig. 9 Ohmic Gate GaN HEMT. Threshold voltage recovery after gate stress. Ambient Temperature
(a) I_{STRESS}= 5.2 mA, (b) I_{STRESS}= 73 mA

The first and most obvious analysis is that in the case of the Ohmic Gate GaN HEMT the resulting V_{TH} shift after stress is negative and the peak shift increases with increasing stress, with a peak shift of -2.5% for the low current stress and -4% for the high current stress. Minor negative shifts for this gate contact technology at this stress levels were also reported in [30].

Increasing the stress time causes a slight increase of the negative peak shift for both stress gate currents, more apparent for the stress current of 73 mA. The recovery is in the range of seconds for both stress levels.

The impact of temperature on the recovery has also been evaluated for the Ohmic Gate GaN HEMT, using the high current gate stress. The complete stress sequence at 150°C for a duration of 1 s is shown in Fig. 10. The results are normalized respect to the pre-stress value at 150 °C.

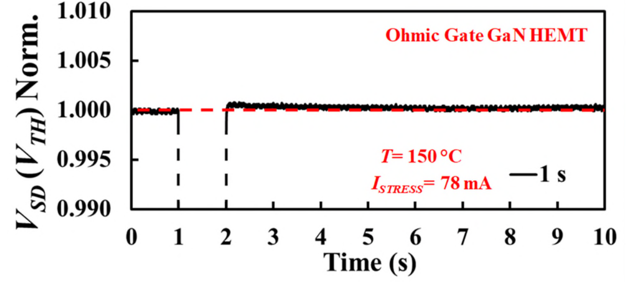


Fig.10 Ohmic Gate GaN HEMT. Complete stress and recovery sequence at 150 °C. I_{STRESS}= 78 mA

Evaluating the results in Fig. 10, where the pre-stress, stress and recovery sequences are shown, it is clearly observed how the shift after stress removal is almost negligible, with a very marginal positive shift of V_{TH}. The recovery transients for stress times from 1s to 100 s are shown in Fig. 11, with no apparent impact of the stress time on V_{TH}.

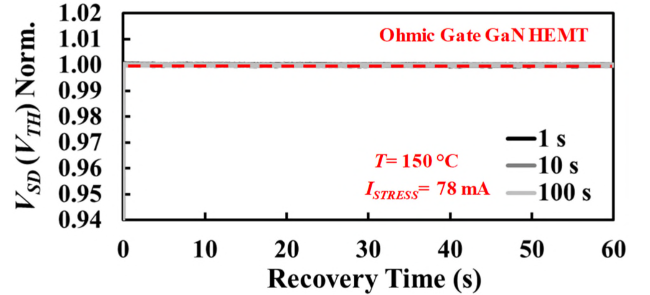


Fig. 11 Ohmic Gate GaN HEMT. Threshold voltage recovery after gate stress. 150 °C I_{STRESS}= 78 mA

The circuit used for the stresses at 150 °C uses the same gate driver voltage and gate resistance than at ambient. As a result of the temperature sensitivity of the forward biased diode in the gate structure [31], shown in Fig. 1(b), the gate voltage reduces to 3.7 V. This causes the increase of the stress current to 78 mA. Additionally, the high power dissipation can also affect the temperature during the tests, highlighting the complexity of gate stress for characterization in ohmic gate GaN HEMTs.

Compared with the Schottky Gate GaN HEMT, it can be concluded that the Ohmic Gate GaN HEMT has a better threshold voltage instability performance.

V. Third Quadrant Characterization Technique Investigations

A. *Repetitive Pulse Gate Stresses*

One of the main benefits of this methods is that it can easily applied for the evaluation of pulsed stresses. By switching V_{GS} at a defined magnitude, duty ratio and frequency, the net effect of the continuous charging and discharging of the traps in the GaN gate can be studied over a defined pulse sequence.

This can reveal transient mechanisms hindered in the long stress sequences. In the case of SiC [28], it was able to reveal the phenomenon of dip-and-rebound of the threshold voltage at highly accelerated stress levels. This can be highly relevant for evaluating the results obtained for the Schottky Gate GaN

HEMT in section IV, focusing on the medium and high gate voltage stresses.

The pulse sequence selected for these investigations consists of 2 s at the defined stress voltage V_{STRESS} and 2 s at 0 V for 40 cycles. The selected stress voltages are 5.5 V and 7.5 V. Fig. 12 shows the repetitive pulse measurements with a V_{GS} stress of 5.5 V. Here, it is clearly seen how the shift of V_{TH} is affected by the stress duration, with a clear positive shift in the initial stages, moving to a negative shift at the final stages of the stress. The change from positive peak shift to negative peak shift is clearly observed in Fig. 13(a), where the normalized peak shift after stress removal is plotted as function of the number of stress pulses. Moreover, the recovery of V_{TH} during the 2 s window reduces as the number of pulses increases, as shown in Fig. 13(b). It starts with a reduction of -13 % for the first pulse and gradually reduces to -8.2 %.

The same device was subjected to the repetitive gate stress at V_{STRESS}= 7.5 V and the results are shown in Fig. 14. In this figure, opposed to the stress at 5.5 V, the peak shift and recovery are not affected by the repetitive stress pulses. The measured peak shift and recovery as function of the number of stress pulses are shown in Fig. 15(a) and Fig. 15(b) respectively.

The pulsed stress results can be highly relevant for power cycling of GaN devices. In SiC power MOSFETs, the role of threshold voltage shifts in power cycling was evaluated in [32] and the impact of the threshold voltage shift on the electrical parameters was studied in [33, 34]. Further investigations on GaN HEMTs are required.

B. Negative Gate Stress

Studies regarding negative gate stresses in GaN HEMTs have also been performed and the results are presented in this section for the Schottky Gate GaN HEMT. In this gate structure, when the gate is biased with a positive gate voltage the gate leakage current increases considerably if the voltage is close the breakdown voltage of the reverse biased Schottky diode structure in the gate stack, as shown in Fig. 1(b). This has been identified as a reliability concern [2], as just a few volts over the rated voltage can damage the gate structure. On the other side, the gate of a Schottky Gate GaN HEMT can biased with large

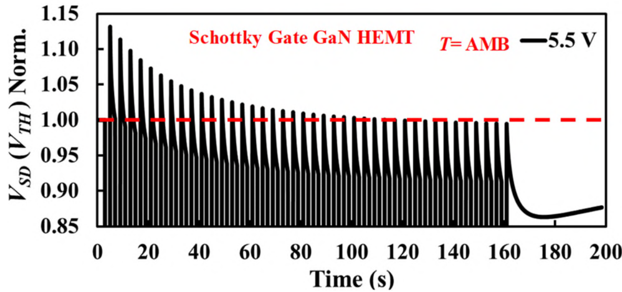
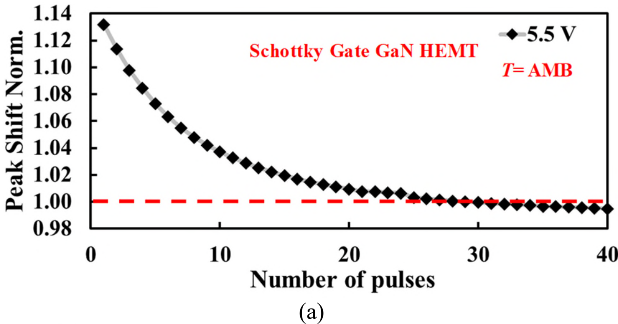
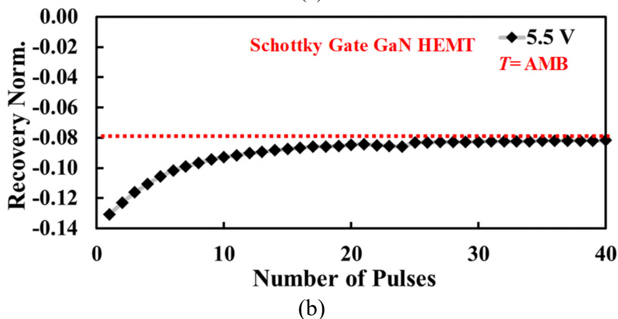


Fig. 12 Schottky Gate GaN HEMT. Pulsed gate stress results. Ambient temperature. 40 pulses (2 s V_{GS}=5.5 V, 2 s V_{GS}=0)



(a)



(b)

Fig. 13 Schottky Gate GaN HEMT. 5.5 V Pulsed gate stress
(a) Normalized V_{TH} peak shift as a function of number of pulses
(b) Normalized V_{TH} recovery during recovery phase

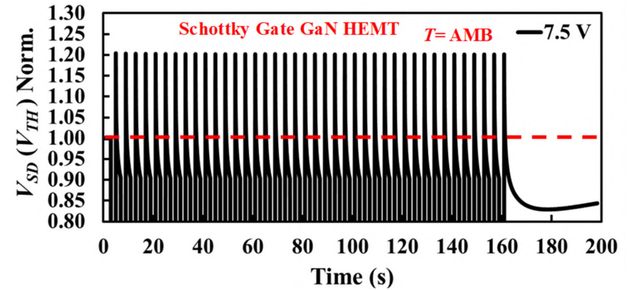
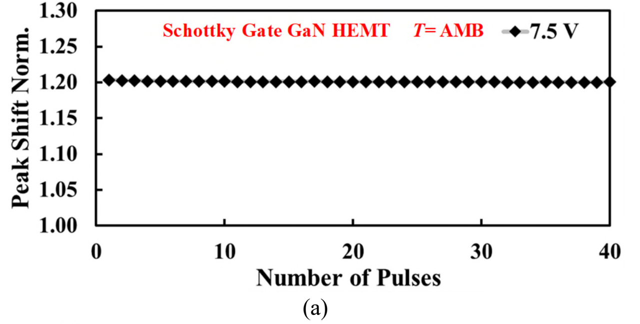
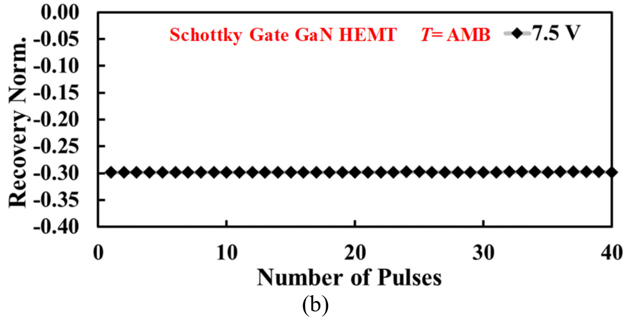


Fig. 14 Schottky Gate GaN HEMT. Pulsed gate stress results. Ambient temperature. 40 pulses (2 s V_{GS}=7.5 V, 2 s V_{GS}=0)



(a)



(b)

Fig. 15 Schottky Gate GaN HEMT. 7.5 V Pulsed gate stress
(a) Normalized V_{TH} peak shift as a function of number of pulses
(b) Normalized V_{TH} recovery during recovery phase

negative gate voltages without noticeable increase on the gate leakage current. This is shown for the evaluated Schottky Gate GaN HEMT in Fig. 16. Increasing the gate voltage bias to +8 V causes a gate leakage current around 200 µA, whereas a negative gate bias of -20 V has no noticeable impact on the gate leakage current.

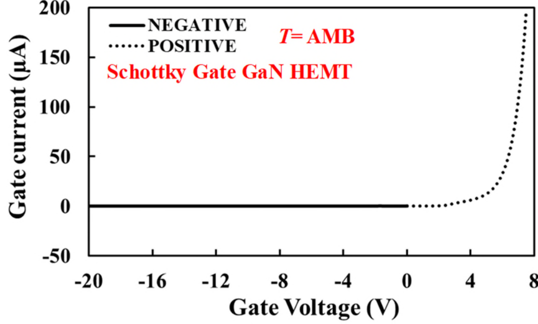


Fig. 16 Gate current as function of gate voltage for the Schottky Gate GaN HEMT. Positive and negative gate voltage sweep

Considering the gate stress at negative gate voltages using the proposed methodology, the main implication is that during reverse conduction of current, the third quadrant voltage V_{SD} increases by a magnitude equal to the applied gate bias, as analyzed previously in section II. According to (3) applying a negative gate voltage stress V_{STRESS} results in a measured V_{SD} equal to $V_{STRESS} + V_{TH}$. This is what is shown in Fig. 17, for the application of a gate stress pulse of –5 V and 10 s duration to the Schottky Gate GaN HEMT.

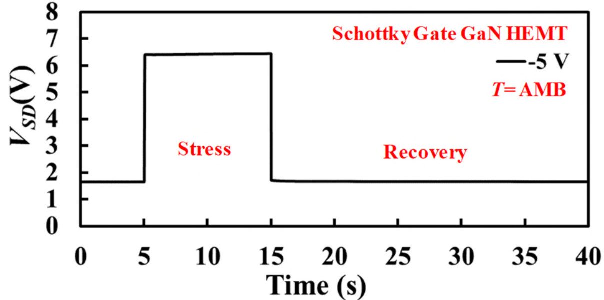


Fig. 17 Schottky Gate GaN HEMT. V_{SD} during a negative gate stress sequence. (V_{STRESS}= -5 V, Stress time: 10 s, I_{SENSE}= 10 mA

In Fig. 17, before the stress pulse, V_{GS}=0 and V_{SD} is equal to V_{TH}. During the stress pulse (t=5 s to t= 15 s), the gate voltage is -5 V and the measured V_{SD} is approximately 6.5 V When the stress is removed, V_{SD} returns to the pre-stress value (V_{SD}=V_{TH}) with no apparent shift after stress removal. It is also important to consider the self-heating of the device during reverse conduction. In this case, the sensing current is 10 mA, and the dissipated power will be approximately 65 mW which will cause a minor self-heating.

The normalized V_{SD}(V_{TH}) for the stress pulse of 10 s duration and V_{STRESS} = -5 V is shown in Fig. 18. This figure shows that the negative gate stress has a minor impact on the V_{TH} shift after stress removal, with only a positive shift of around +4% for the -5 V stress. This stress recovers to the pre-stress value in the range of seconds, with an initial fast recovery. It is also worth to

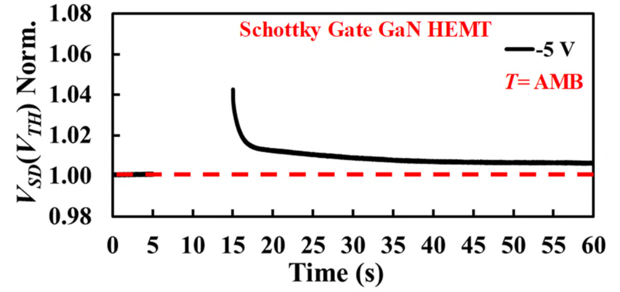


Fig. 18 Schottky Gate GaN HEMT. Normalized V_{TH} before and after a negative gate stress pulse of 10 s (Stress voltage -5 V)

mention that the shift can be affected by the self-heating of the device during the stress. A positive V_{TH} shift under negative gate bias was also reported in [19, 35].

VI. Conclusions

In this paper a methodology for characterizing threshold voltage shifts after gate stress in GaN HEMTs is presented. The methodology is based on the third quadrant characteristics of GaN HEMTs and the direct relationship between V_{SD} and V_{TH} during reverse conduction of a small current. The methodology has been applied to commercially available GaN HEMTs, one with an ohmic gate contact and other with a Schottky gate contact.

In the case of the Schottky Gate GaN HEMT, the stress voltage plays a fundamental role on the measured V_{TH} shift. A positive shift is detected at low gate voltage stresses, whereas as the gate stress level is increased the shift becomes negative. At medium stress voltages the duration of the stress causes the shift to change from positive to negative. In the case of the Ohmic Gate GaN HEMT the stress was performed using different gate current levels and only a minor negative threshold voltage shift was detected. For both gate contact technologies, the recovery after stress removal is accelerated at higher temperatures, with no apparent shift in the case of the Ohmic Gate HEMT.

The method can be used for negative gate stresses and pulsed gate stresses as the initial characterization results in this paper demonstrate and it can be fundamental for understanding the stress and recovery transients in GaN HEMTs.

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