Trade-offs Between Gate Oxide Protection and Performance in SiC MOSFETs

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Abstract—**The reliability of gate oxides in SiC MOSFETs has come under increased scrutiny due to reduced performance under time dependent dielectric breakdown and increased threshold voltage instability. This paper investigates how 10% gate voltage (V_{GS}) derating in SiC MOSFETs can be implemented with minimal impact on loss performance. Using experimental measurements and electrothermal simulations of power converters, the trade-off between reduced V_{GS} and conversion loss is investigated. It is shown that 10% V_{GS} de-rating increases the ON-state resistance by 10% and the turn-ON switching energy by 7% average while the turn-OFF switching energy is unaffected. The low temperature sensitivity of the ON-state losses in SiC MOSFETs can be exploited since the rise in junction temperature due to V_{GS} derating is marginal, unlike Si devices where ON-state resistance rises significantly with temperature. The load current and switching frequency influences the effectiveness of V_{GS} derating. It is also shown that reducing the gate drive output impedance can compensate for V_{GS} derating at high switching frequencies, with reduced total loss penalization. This may be important for protecting the gate oxide and enhancing its reliability.**

Keywords—SiC MOSFET, Gate Oxide, Electrothermal Modeling, Reliability

I. INTRODUCTION

The reliability of the gate oxide of SiC MOSFETs have been the subject of different studies in the recent years [1-4]. The main challenge of SiC MOSFETs is the existence of carbon [5, 6], resulting in an increased trap density in the oxide and at the interface. This makes the SiC/SiO₂ interface of SiC MOSFETs more complex than the Si/SiO₂ interface in Si MOSFETs and IGBTs.

Studies show that the performance in Time Dependent Dielectric Breakdown (TDDB) tests of SiC MOSFETs is lower than for Si IGBTs and heavily dependent on the manufacturer [7]. Another issue is the threshold voltage instability under gate bias stress also called Bias Temperature Instability (BTI) [3]. This results in parameter drifts [8, 9] that may have serious reliability implications in the case of parallel devices with uneven threshold voltage (V_{TH}) shift [10]. Studies in [3] indicate that some vendors have a high dispersion of V_{TH} shift after gate bias stress, even using the rated gate voltage values. Some challenges have been addressed and the reliability of the new generation devices is improved compared to the previous generations of SiC MOSFETs [7, 11], however they still lag behind MOS gated silicon devices.

A key parameter for the reliability of SiC MOSFETs is the selected gate driver voltage. On one hand, a high gate voltage is recommended to reduce the ON-state resistance and improve the performance of the device during conduction. On the other hand, a high gate voltage results in higher stresses on the gate oxide, which may result in a reduced lifetime. Reducing the gate voltage may result in an increased lifetime of the gate oxide, with a penalization in the performance of the device. Given the superior properties of SiC power devices [12], evaluating and benchmarking the performance of SiC MOSFETs using reduced gate driver voltages may still result in a superior performance in the application. This paper presents a study of the implications of reducing the gate driver voltage in SiC MOSFETs. A fully electrothermal model, based on the extensive experimental characterization of the SiC MOSFET under study is used to benchmark impact of a reduction of 10% of the gate driver voltage on the performance of a grid-connected converter in different scenarios, including the impact of the switching frequency and the load current.

II. SiC MOSFET CHARACTERIZATION

The device evaluated in this study is a 900 V SiC planar MOSFET from Cree/Wolfspeed with datasheet reference C3M0065090D and a current rating of 23 A at a case temperature of 100 °C. The recommended gate driver voltage for this device is 15 V.

A. ON-state resistance

In the voltage range of 900 to 1200 V, the channel resistance R_{CH} plays a fundamental role in the total ON-state resistance R_{DS-ON} of SiC MOSFETs, which can be approximated by (1). The other main components are the channel resistance (R_{CH}), resistance of the drift blocking layer R_{DRIFT} and the resistance of the JFET region R_{JFET} [13].

$$R_{DS-ON} \approx R_{CH} + R_{DRIFT} + R_{JFET} \quad (1)$$

The channel resistance is gate voltage dependent and a high gate source voltage V_{GS} is required for minimizing its value, as shown in (2) [3, 13], where L_{ch} is the length of the channel, W is the width of the channel, μ is the mobility, C_{OX} is the gate oxide capacitance density, V_{GS} is the applied gate source voltage and V_{TH} is the threshold voltage

$$R_{CH} = \frac{L_{ch}}{W\mu C_{OX}(V_{GS}-V_{TH})} \quad (2)$$

The impact of the gate voltage is not only in the nominal R_{DS-ON}. It also affects its temperature sensitivity. Fig. 1 shows the normalized ON-state resistance of different 1200 V SiC and Si MOSFETs, of a similar current rating of around 20 A at case temperature of 25 °C. It can be observed that for a gate voltage of 17 V, the temperature sensitivity of SiC MOSFETs is lower, especially in the case of the 1st generation SiC MOSFET. This is caused by the different temperature coefficients of the resistances in (1), negative for R_{CH} and positive for R_{DRIFT} and R_{JFET} [14].
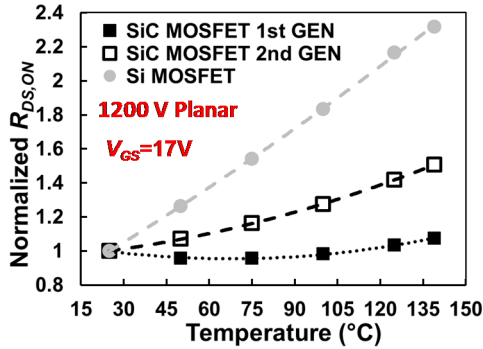

Fig. 1 Normalized ON-state resistance as function of temperature for different Si and SiC MOSFETs [8]

Evaluating an earlier generation SiC MOSFET with a similar current rating than the selected 3rd generation SiC MOSFET, the role of the gate driver voltage on R_{DS-ON} is particularly important. Fig. 2(a) shows that the 1st generation devices required a gate voltage in the range of 16-20 V to operate in well-defined Positive Temperature Coefficient (PTC) region. The selected 3rd generation SiC MOSFET operates in a positive temperature coefficient at gate voltages of 10-15 V, as the measurements in Fig. 2(b) indicate. However, the temperature sensitivity of the
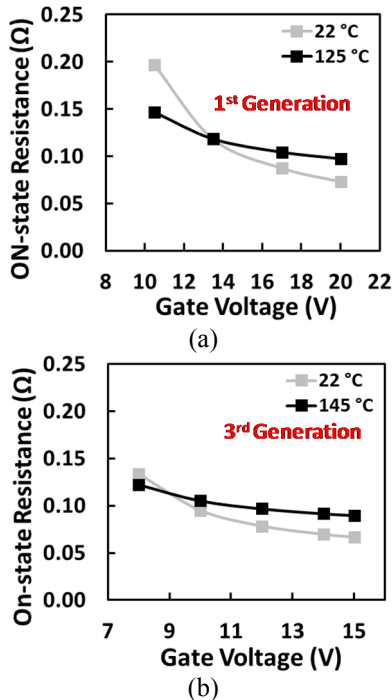

(a)

(b)

Fig. 2 Impact of gate driver voltage and temperature on the ON-state resistance: (a) First generation 1200 V/80 mΩ SiC MOSFET (b) Third generation 900 V/65 mΩ SiC MOSFET

ON-state resistance reduces as V_{GS} is reduced. This is critical for paralleling devices without the risk of thermal runaway [10, 14].

B. Switching transients

Reducing the gate voltage will also affect the switching transients, which can be characterized using a conventional double pulse test setup [15, 16], as shown in Fig. 3.
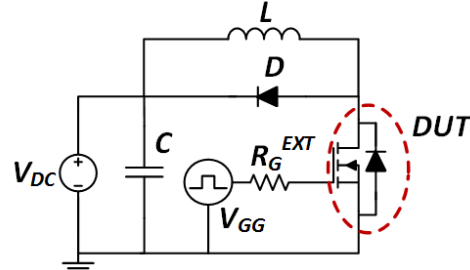

Fig. 3 Double pulse test circuit [15]

The Device Under Test (DUT) is the SiC MOSFET C3M0065090D and the switching transients were characterized for a set of load currents (10 A and 20 A) at different case temperatures. The case temperatures were adjusted using a small DC heater attached to the case of the device, allowing enough time to reach thermal equilibrium, hence the chip temperature can be assumed equal to the case temperature. The clamping diode D in Fig. 3 is a 650 V SiC Schottky with datasheet reference C3D10065A.

The measured turn-ON and turn-OFF transients for a load current of 10 A, temperature T of 25 °C and DC link voltage V_{DC} of 400 V are shown in Fig. 4.
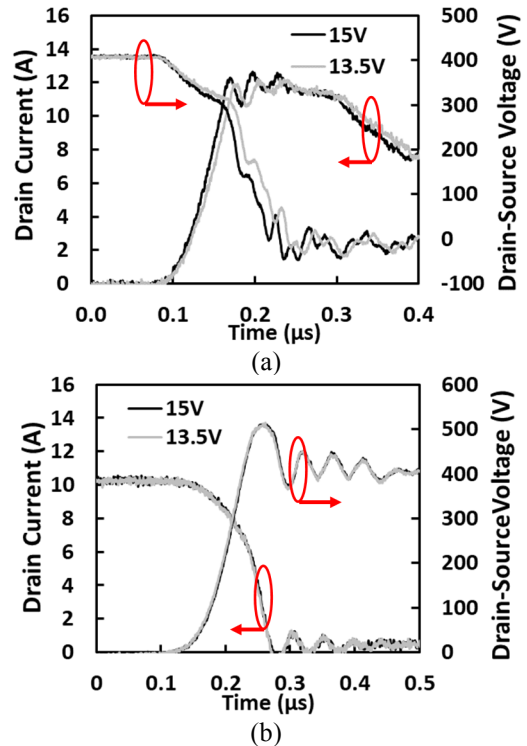

(a)

(b)

Fig. 4 Impact of gate driver voltage on the switching transients. V_{DC}=400 V, I_{LOAD}= 10 A, R_G^{EXT}=100 Ω, T=25 °C (a) Turn-ON (b) Turn-OFF

The measurements in Fig. 4 were performed using gate driver voltages V_{GG} of 13.5 V and 15 V and an external gate resistance R_G^{EXT} of 100 Ω. The gate driver is unipolar, meaning that the turn-OFF voltage is 0 V. From the switching transients it is clearly observed that the turn-ON transient is affected by the reduction of the gate driver voltage whereas there are no noticeable changes in the turn-OFF switching rates.

Equations (3) to (6) are useful to understand the switching transients [13]. V_{GG} is the gate driver voltage, V_{GP} is the gate voltage plateau, R_G is the total gate resistance (sum of the internal gate resistance of the device and the external gate resistance R_G^{EXT}), C_{GS} and C_{GD} are the gate-source and gate drain parasitic capacitances, V_{TH} is the threshold voltage and g_m is the transconductance of the device.

$$\frac{dV_{DS-ON}}{dt} = -\frac{V_{GG}-V_{GP}}{R_G C_{GD}} \tag{3}$$

$$I_{D-ON} = g_m \left[V_{GG} \left(1 - e^{-\frac{t}{R_G(C_{GS}+C_{GD})}} \right) - V_{TH} \right] \tag{4}$$

$$\frac{dV_{DS-OFF}}{dt} = \frac{V_{GP}}{R_G C_{GD}} \tag{5}$$

$$I_{D-OFF} = g_m \left[V_{GP} \left(e^{-\frac{t}{R_G(C_{GS}+C_{GD})}} \right) - V_{TH} \right] \tag{6}$$

Equations (3) and (4) correspond to turn-ON while equations (5) and (6) correspond to turn-OFF. As can be seen in equations (3) and (4), V_{GG} is directly proportional to the turn-ON voltage and current switching rates (dV_{DS}/dt and dI_{DS}/dt). At turn-OFF, as the gate drive voltage is 0 V, V_{GP} is the critical factor since V_{GG} does not appear in equations (5) and (6). From the results shown in Fig. 4 and the analytical equations, it is clearly

observed that the penalization because of the reduction of the gate driver voltage will be in the turn-ON switching energy, as the turn-OFF switching energy will be gate driver voltage independent.

The turn-ON measurements for a load current of 20 A at a temperature of 75 °C are shown in Fig. 5, including the turn-ON energy, turn-ON dI/dt and turn-ON delay time. Fig. 6 shows the corresponding measurements for turn-OFF. From these results it is clearly observed that the penalization of reducing the gate driver voltage a 10% will be on the turn-ON energy, especially when using large gate resistances. The turn-ON and turn-OFF delay times were calculated according to [17, 18]. The delay times are important when high switching frequencies are required, as they define the required dead time [18]. From the results in Fig. 5(c) and Fig. 6(c) it can be observed that reducing the gate voltage increases the turn-ON delay and reduces the turn-OFF delay. In this case, the total delay can be considered V_{GG} invariant, hence the impact of reducing V_{GG} on the dead time can be neglected.

III. MODEL DEVELOPMENT

With all the previous considerations, it is important to evaluate how the reduction of the gate driver voltage will affect the performance of a converter. Electrothermal modelling is be important for understanding the implications of V_{GG} reduction on the converter's performance. The application selected for evaluating the performance of the device is a grid-connected 3-phase voltage source converter, which has been implemented in MATLAB/Simulink using the structure shown in Fig. 7. The converter is connected to the grid using an inductive filter and the operating conditions are DC link voltage V_{DC} 400 V and
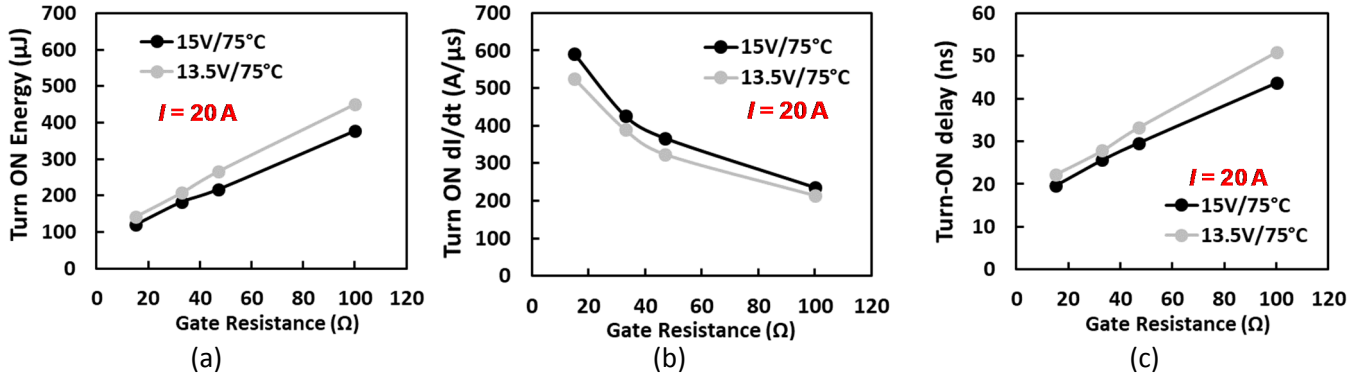

Fig. 5 Impact of gate voltage reduction on turn-ON metrics ($I = 20$ A). (a) Energy (b) Drain Current Switching Rate, (c) Delay Time
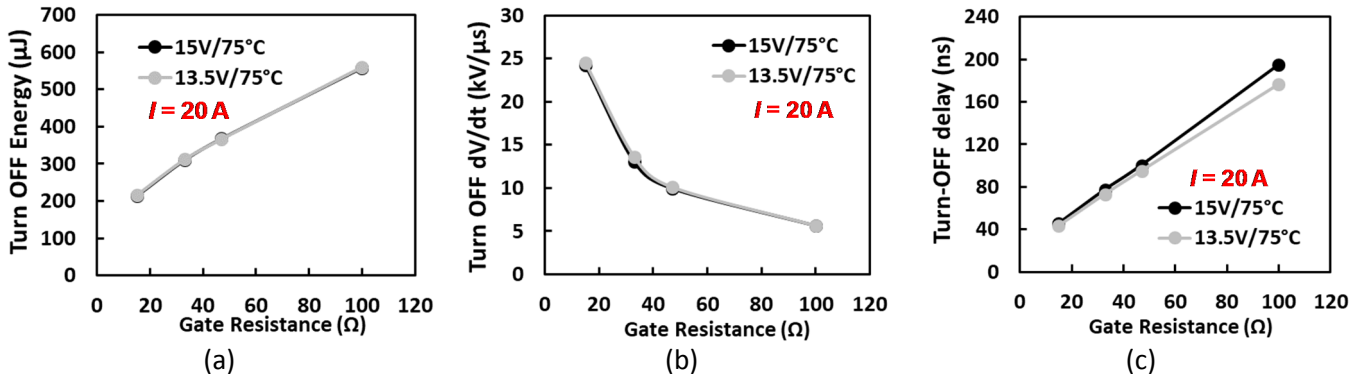

Fig. 6 Impact of gate voltage reduction on turn-OFF metrics ($I = 20$ A). (a) Energy (b) Drain-Source Voltage Switching Rate, (c) Delay Time

mains frequency 50 Hz. The parameters of the filter are $R_{FILTER} = 0.15\ \Omega$ and $L_{FILTER} = 0.01$ H.
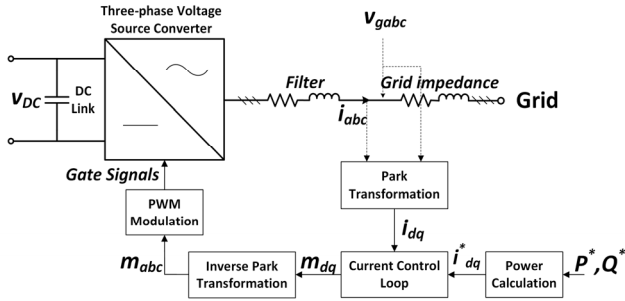

Fig. 7 Grid-connected 3-phase voltage source converter model implemented in MATLAB/Simulink, including control and PWM modulation

The measured 3-phase output voltages v_{gabc} and currents i_{abc} of the converter are transformed to the i_{dq} values using the Park transformation. The required active power P^* and reactive power Q^* are converted to the respective i_{dq}^* current values. A current control loop is used to adjust the required m_{dq}, which is then converted to the abc frame using the inverse Park transformation. The PWM gate signals of the converter are modulated using the obtained m_{abc}. The 3-phase output currents, considering a peak current of 20 A, are shown in Fig. 8.
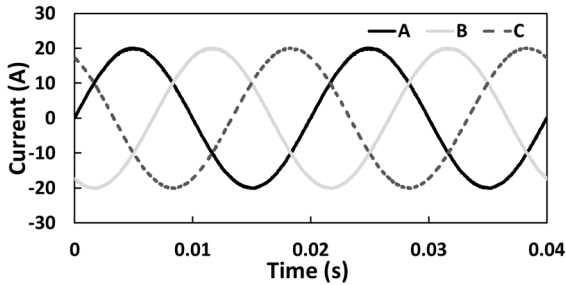

Fig. 8 3-phase output current generated using the MATLAB/Simulink model

This paper uses a fully electrothermal model where the measured switching energies at different gate driver voltages, load currents and temperatures are uploaded in a Look-Up-Table (LUT). The ON-state resistance as function of the gate voltage is circuit independent and its temperature sensitivity can be extracted from the device datasheet and uploaded into another LUT. The methodology for calculating the conduction and switching losses (including load current and temperature dependencies) is shown in Fig. 9. This methodology was used in [19] for evaluating the use of different power semiconductor devices in an electric vehicle powertrain inverter. Fig. 9(a) shows how the conduction losses and the temperature dependency are determined. First, a logic operation is executed to verify if the MOSFET is operating in the first quadrant. If the current i is positive, the conduction losses are calculated as the product of the current and ON-state voltage of the MOSFET. The ON-state voltage is calculated using a 2D-LUT, which includes the ON-state resistance as function of temperature. Fig. 9(b) shows the methodology for calculating the turn-ON switching losses. As shown in the conceptual representation in Fig.10, the current across the device is pulsed as a result of the

gate signal applied, with a turn-ON energy corresponding to the positive edge of the gate signal. The algorithm in Fig. 9(b) uses the gate signal to detect the turn-ON edge and the corresponding turn-ON current (i_{SAMP}). A 2D-LUT is used to determine the turn-ON energy as function of the temperature T_J and i_{SAMP}. The total switching losses are dependent of the frequency, which is the inverse of the period T.
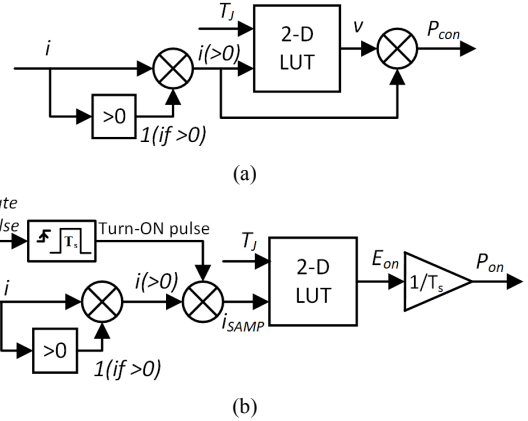

(a)

(b)

Fig. 9 Calculation of (a) ON-state losses and (b) turn-ON switching losses [19]
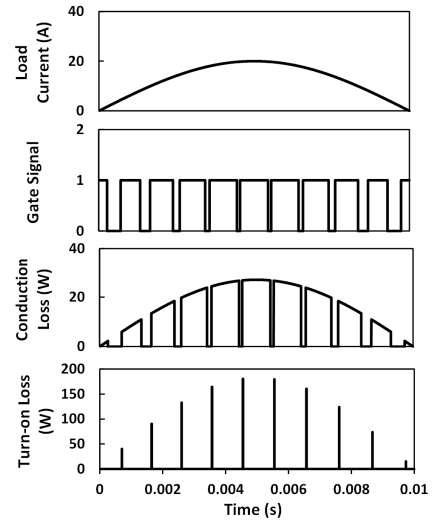
Fig. 10 Conduction loss and turn-ON loss in a positive load current cycle. Conceptual plot

A similar algorithm is used for calculating the turn-OFF losses but using the negative edge of the gate signal. The model uses a SiC Schottky Barrier Diode (SBD) as anti-parallel device and it is important to remark is that the temperature of the SBD does not affect the switching losses of the SiC MOSFET [20] as its reverse recovery is temperature independent [21].

IV. IMPACT OF GATE DRIVER VOLTAGE REDUCTION ON THE CONVERTER OPERATION

Different parameters will influence the impact of V_{GG} reduction on the efficiency of the converter, including the load current I_{LOAD} and the switching frequency f_{SW}. Increased losses from V_{GG} reduction will cause increased junction temperature (T_J) and larger junction temperature swings (ΔT_J) during

operation, which can cause a reduction of the lifetime of the converter due to higher thermomechanical stresses [22, 23]. However, accelerated stress tests show that reducing the gate voltage extends the lifetime of the gate oxide [24-26], hence the importance of evaluating the trade-offs of using a lower V_{GG}. This has been studied using the grid-connected converter (mains frequency of 50 Hz) in Fig. 7, evaluating a reduction of the gate driver voltage of 10%, from 15 V to 13.5 V in different operation scenarios.

A. Impact of load current

First, the impact of the load current was investigated. For this investigation, the switching frequency f_{SW} was 10 kHz, the gate resistance was 33 Ω for both gate driver voltages and the case temperature T_{CASE} was fixed at 60 °C. The load is purely resistive and the Simulink control adjusted the load current to the desired values, namely a peak current of 10 A (load power of 2.4 kW) and peak current of 20 A (load power of 4.8 kW). The fully electrothermal model determined the resulting power losses in the converter and junction temperature excursions.

The junction temperature excursion for a load current of 10 A is shown in Fig. 11(a), whereas the results for a load current of 20 A are shown in Fig. 11(b). Fig. 11(a) shows that for a load current of 10 A, there is no significant impact of V_{GG} reduction on ΔT_J (less than 0.2°C increase). However, as shown in Fig. 11(b), if the load current is increased to 20 A, the impact of V_{GG} reduction becomes more apparent, causing a peak junction temperature T_{J-PEAK} increase of 1.3°C and the junction temperature excursion ΔT_J increases 1°C. This is caused by the higher conduction losses and turn-ON switching losses, causing the total losses to increase an 8%. As the current is increased, the relative contribution of the conduction losses is higher, hence the increased junction temperatures. The losses and temperature excursions are summarized in Table I.
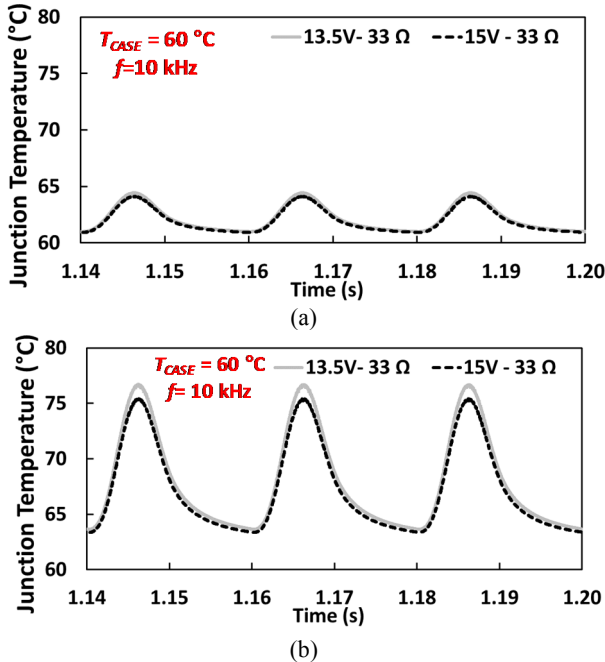
TABLE I: IMPACT OF GATE DRIVER VOLTAGE REDUCTION ON LOSSES AND TEMPERATURE. METRICS FOR DIFFERENT LOAD CURRENTS (F_{SW}=10 KHZ, T_{CASE}=60 °C, R_G^{EXT}=33 Ω)

	I_L= 10 A		I_L= 20 A	
	V_{GG}= 15 V	V_{GG}=13.5V	V_{GG}=15 V	V_{GG}=13.5 V
Conduction Losses (W)	8.69	9.52	35.55	38.76
Switching Losses (W)	3.34	3.45	8.59	9.00
ΔT_J (°C)	3.2	3.4	12.1	13.1
T_{J-PEAK} (°C)	64.1	64.4	75.4	76.7

B. Impact of switching frequency

One of the main benefits of SiC is the ability to operate at higher switching frequencies, enabling the reduction of the passive components and filtering requirements [12]. Hence, it is important to evaluate the impact of V_{GG} reduction on the converter operation at higher switching frequencies. This has been evaluated for load current of 20 A and a case temperature of 60 °C, at switching frequencies ranging from 10 kHz to 80 kHz. The results for a switching frequency of 10 kHz are already shown in Fig. 11(b) and the junction temperature excursions for switching frequencies of 20 kHz and 60 kHz are shown in Fig. 12. The losses and temperature excursions are summarized in Table II.

The switching frequency has an impact on the balance between conduction and switching losses as shown in Table I (for the load current of 20 A) and Table II. For a switching frequency of 10 kHz, the switching losses represent

Fig. 11 Impact of reducing V_{GG} on the junction temperature excursions.
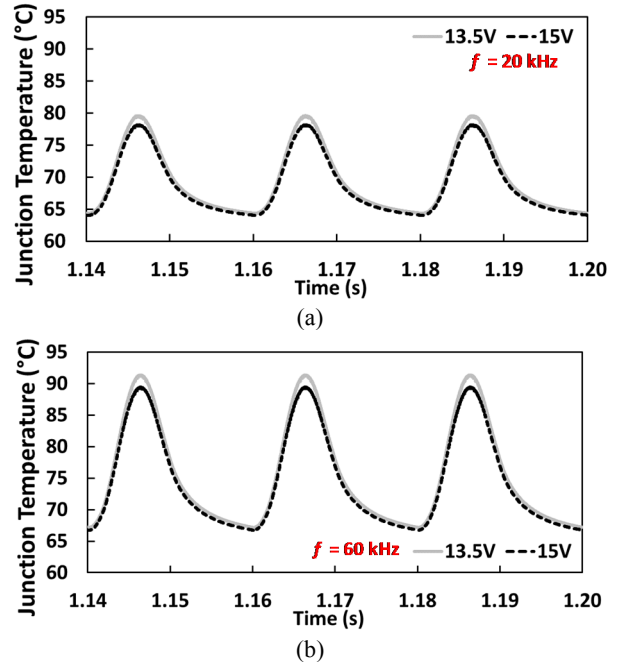f_{SW}=10 kHz, T_{CASE}=60 °C, R_G^{EXT}=33 Ω
(a) I_{LOAD}=10 A (b) I_{LOAD}=20 A

Fig. 12 Impact of reducing V_{GG} on the junction temperature excursions.
I_{LOAD}=20 A, T_{CASE}=60 °C, R_G^{EXT}=33 Ω
(a) f_{SW}=20 kHz (b) f_{SW}=60 kHz

approximately a 20% of the total losses, however for a switching frequency of 60 kHz they account for approximately a 59 %.

	f_{SW}=20 kHz		f_{SW}=60 kHz	
	V_{GG}= 15 V	V_{GG}=13.5V	V_{GG}=15 V	V_{GG}=13.5 V
Conduction Losses (W)	35.84	39.05	36.55	39.73
Switching Losses (W)	17.15	17.97	51.49	53.87
ΔT_J (°C)	14.1	15.2	22.7	24.2
T_{J-PEAK} (°C)	78.2	79.6	89.4	91.4

Higher switching losses will cause a higher junction temperature. In SiC MOSFETs the total switching energy is temperature invariant or reduces slightly with temperature [27], hence an increased junction temperature does not translate into higher switching energy. For example, increasing the switching frequency 6 times results in the switching losses increasing approximately by the same factor (5.985 times), despite the T_{J-PEAK} increase of 14.7 °C for a gate voltage of 13.5 V and R_G^{EXT} = 33 Ω.

Increasing the switching frequency from 10 kHz to 60 kHz has a minor impact on the conduction losses, caused by the higher junction temperature. The increase of 14.7 °C results in an increase of 2-3% of the conduction losses. Again, as shown in Fig. 1, the low temperature sensitivity of SiC MOSFETs is key for this. The results are summarized in Fig. 13, where the
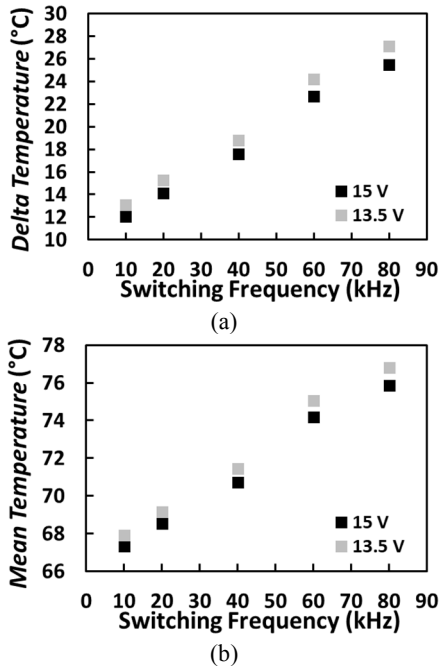

(a)

(b)

Fig. 13 Impact of switching frequency on
(a) Junction temperature excursion (b) Mean junction temperature
(I_{LOAD} = 20 A, T_{CASE}=60 °C, R_G^{EXT}=33 Ω)

mean junction temperature and junction temperature excursion are plotted as function of the switching frequency.

C. Switching loss mitigation techniques

As the analysis in section 2 shows, the turn-OFF losses are not affected by V_{GG} hence an option for compensating the impact of V_{GG} reduction can be increasing switching speeds. Minimizing the switching losses can be particularly important if the switching frequency is increased, as the results in Fig. 13 indicate. The most common technique of increasing switching speeds is reducing the external gate resistance (R_G^{EXT}). How reduced R_G^{EXT} ca be used to compensate for reduced V_{GG} has been evaluated for a load current of 20 A and switching frequencies of 20 kHz and 60 kHz. In the simulations, a converter with MOSFETs driven with V_{GG}=15 V and R_G^{EXT}=33 Ω is compared to one with MOSFETs driven with V_{GG}=13.5 V and R_G^{EXT}=15 Ω. The junction temperature excursion is shown in Fig. 14 and the performance metrics are shown in Table III.

(a)

(b)
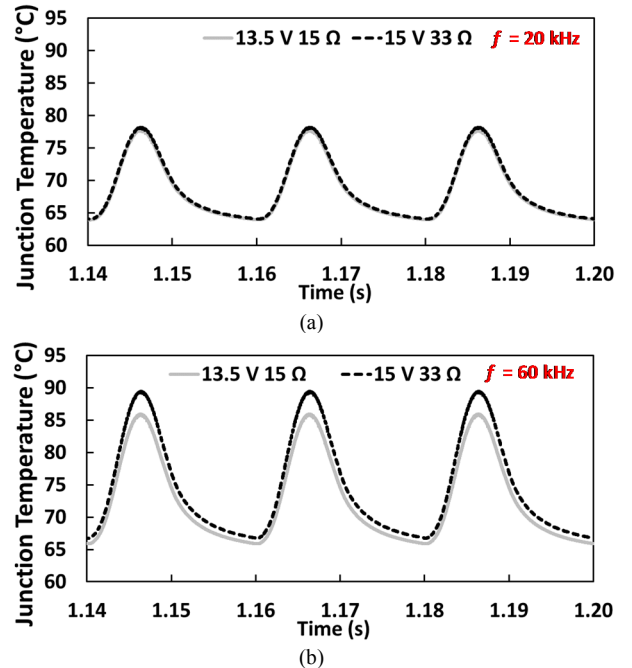
Fig. 14 Impact of switching loss improvement at reduced gate driver voltages (I_{LOAD}=20 A, T_{CASE}=60 °C) (a) f_{SW}=20 kHz (b) f_{SW}=60 kHz

	f_{SW}=20 kHz		f_{SW}=60 kHz	
	V_{GG}= 15 V R_G^{EXT}=33 Ω	V_{GG}=13.5V R_G^{EXT}=15 Ω	V_{GG}=15 V R_G^{EXT}=33 Ω	V_{GG}=13.5V R_G^{EXT}=15 Ω
Conduction Losses (W)	35.84	38.94	36.55	39.35
Switching Losses (W)	17.15	12.46	51.49	37.45
ΔT_J (°C)	14.1	13.9	22.7	20.1
T_{J-PEAK} (°C)	78.2	77.8	89.4	85.9

The results in Fig. 14 and Table III clearly indicate the effectiveness of reducing the R_G^{EXT} as a switching loss mitigation technique. At f_{SW} = 20 kHz, the increased conduction losses (from lower V_{GG}) are balanced with the reduced switching losses (from lower R_G^{EXT}) and the impact on the junction temperature is compensated, with T_{J-PEAK} decreasing -0.4 °C and ΔT_J -0.2 °C. This is particularly effective at higher switching frequencies, as the results for f_{SW}=60 kHz show in Fig. 14(b). The switching losses are dominant and reducing R_G^{EXT} improves both turn-ON and turn-OFF switching energies, resulting reduction of the total losses of -12.7%, and lower junction temperatures, with T_{J-PEAK} and ΔT_J reducing -3.5 °C and -2.6 °C respectively.

The effectiveness of reducing the R_G^{EXT} for mitigation of the total losses is summarized in Fig. 15, where it is clear that the benefits of R_G^{EXT} reduction are greater at higher switching frequencies. The reduction of the temperature of operation is reflected in a slight reduction of the conduction losses and the switching losses clearly improve if a smaller R_G^{EXT} is used.
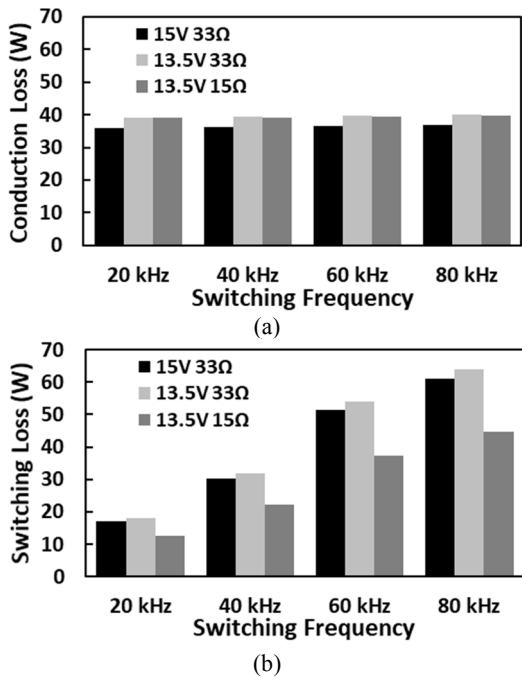

Fig. 15 Impact of reducing the gate driver voltage and gate resistance on the converter losses at different switching frequencies
(I_{LOAD}=20 A, T_{CASE}=60 °C) (a) Conduction loss (b) Switching loss

Other option could be a switching aid capacitor, as defined in [28], for boosting the turn-ON voltage transient. It is also important to mention that if different R_G^{EXT} are considered for turning ON and OFF the MOSFET, special attention to parasitic turn-ON [29] is required when selecting the resistor values.

D. Gate oxide lifetime and reliability considerations

The main objective of reducing the gate driver voltage is protecting the gate oxide and improving its lifetime. The lifetime of the gate oxide in SiC MOSFETs is usually obtained using accelerated stress tests and extrapolating the results obtained for higher gate voltages to the predicted lifetime at the nominal gate voltage. Using nominal gate voltages for extracting the lifetime would provide a more accurate prediction but time required will

make these studies unfeasible [30]. Furthermore, the number of parts tested is also dependent on the acceleration factor and for obtaining the required failure metrics at stress values close to the nominal gate voltage required very large sample numbers [30]. Examples of lifetime calculations for SiC MOSFETs are available in [24, 26, 31]. In [31], accelerated gate stresses were performed at different temperatures and the data indicated that reducing the gate voltage from 20.588 V to 19.127 V improved the predicted lifetime of the gate oxide from 10 to 20 years for a temperature of operation of 150 °C. The studies in [24] used a previous generation of the device evaluated in this paper and from the lifetime projections, reducing the gate driver voltage 10% (from 20 V to 18 V) increases the lifetime approximately 3.6 times. In [26] the lifetime projections for the device evaluated in this paper are presented. The lifetime of the gate oxide of the C3M0065090 MOSFET, extracted from the data in [26], increases 2.3 times, when the gate driver voltage is reduced from 15 V to 13.5 V.

It may not only be a question of lifetime improvement. The role BTI-induced threshold voltage in the converter operation should also be considered, as it has been done with power cycling [32] and SiC MOSFET electrical parameters [8, 9]. A lower shift is expected if the device is driven with a lower V_{GG} [33] and this can be highly relevant for the long-term converter operation. Preliminary studies using simulation models have been presented in [34]. Recent investigations in [35] indicate the importance of defining the gate driver voltage window (maximum negative gate voltage for turning-OFF the device and maximum positive gate voltage for turning-ON). The role of the switching frequency is mentioned, indicating the existence a switching induced threshold voltage shift [35]. Protecting the gate oxide is paramount in SiC MOSFETs, but the increased temperature of operation and temperature excursions can also play a key role on the lifetime of the packaging. The simulations in this investigation show a marginal temperature increase and its impact on the lifetime of the packaging will be difficult to quantify. Finite element simulations [36] can be paramount for understanding the impact of these small junction temperature changes on the packaging stresses.

V. CONCLUSIONS

Protecting the gate oxide is paramount of extending the lifetime and reliability of SiC MOSFETs. De-rating the gate driver voltage for protecting the gate oxide and improving the lifetime of SiC MOSFETs can be a suitable option, as a reduced gate voltage improves the lifetime of the gate oxide. This paper uses experimental measurements of conduction and switching losses in SiC MOSFETs driven with the recommended V_{GS} and 90% V_{GS} and a full-electrothermal model of a grid-connected inverter to study the impact of V_{GS} de-rating on performance with the objective of protecting the gate oxide. Experimental measurements show that reducing the gate driver voltage increases the conduction losses and turn-ON switch losses, whereas the turn-OFF switching losses are not affected by this reduction. The average increase of the conduction losses is 10% and the average increase of the turn-ON energy is 7% and the electrothermal simulations indicate that the operating conditions (load current and the switching frequency) have a significant impact on what the loss penalization is.

The loss penalization increases with the load current and switching frequency, causing a higher junction temperatures during operation. As the switching frequency is increased, the penalization of V_{GS} de-rating on conduction losses remains constant while the loss penalization in the switching losses can be compensated by reducing the gate resistance. The reduced temperature sensitivity of the ON-state resistance and switching energies in SiC MOSFETs plays a critical role in the effectiveness of reducing the gate driver voltage for protecting the gate oxide without incurring in a bigger loss penalization.

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