UIS performance and ruggedness of stand-alone and cascode SiC JFETs

S. N. Agbo[a], J. Ortiz Gonzalez[a], R. Wu[a], S. Jahdi[b] and O Alatise[a]

[a] *School of Engineering, University of Warwick, Coventry, United Kingdom*
[b] *Faculty of Engineering, University of Bristol, Bristol, United Kingdom*

Abstract
In this paper the ruggedness of stand-alone and cascode SiC JFETs is evaluated under single and repetitive unclamped inductive switching (UIS). The impact of the JFET gate resistance, avalanche current and temperature are evaluated. The results show that the avalanche characteristics are strongly affected by the peak avalanche current and the JFET gate resistance. Due to the absence of an insulating gate, there is significant JFET gate current during avalanche. This gate leakage current plays a fundamental role on the reduced performance under repetitive UIS of SiC cascode JFETs compared with stand-alone SiC JFETs.

1. Introduction

The superior properties of wide bandgap power semiconductors (namely SiC and GaN) have improved the energy conversion efficiency and power density in power electronics. However, there are some reliability issues still to be addressed. In the case of SiC MOSFETs, reduced gate oxide reliability and higher threshold voltage instability are major concerns [1, 2], despite improvements in the latest generations. The SiC JFET was already commercially available in 2006 [3], nevertheless being a normally-ON device, it was not attractive from the application point of view. The emergence of the SiC MOSFET [3], a voltage driven normally-OFF device, meant the SiC JFET reduced in relevancy. However, due to the gate oxide issues in SiC MOSFETs, there is a recent interest in SiC Cascode JFETs.

The SiC Cascode JFET configuration consists of a High Voltage (HV) SiC JFET and Low Voltage (LV) Si MOSFET, where the LV Si MOSFET ensures that the cascode operates as a normally-OFF device. SiC Cascode JFETs are a promising alternative to SiC MOSFETs [4-7], as they combine the switching performance of a SiC JFET with the gate oxide reliability of a silicon MOSFET [1, 8, 9]. The SiC cascode has potential to be used in different applications, like electric vehicles [10], however, in order to accelerate its adoption, further reliability and robustness studies are required.

This is important given the preliminary results in [11], which indicate an unusual performance under Unclamped Inductive Switching (UIS). These unusual results appeared at high temperatures and include reduced drain-source voltage V_{DS} during avalanche, increased avalanche duration and reduced drain-source voltage switching rate (dV_{DS}/dt) during the avalanche transient. These characteristics appeared to make the device more avalanche rugged as the temperature is increased, which is not typical of power MOSFETs under avalanche.

The aim of this paper is to investigate the above described unusual performance by comparing the single and repetitive avalanche performance of SiC cascode JFETs with stand-alone SiC JFETs.

The structure of the paper is defined as follows: Section 2 presents the experimental setup and introduces the UIS peculiarities of SiC Cascode JFETs. Section 3 investigates the UIS performance of the stand-alone SiC JFET, evaluating the impact of the JFET gate resistance and the peak avalanche current at both ambient and high temperature. Section 4 investigates the UIS performance of SiC cascode JFETs and compares the obtained results with the UIS performance of the stand-alone SiC JFET. Section 5 evaluates the repetitive UIS capability of both devices, Section 6 presents Finite Element Analysis (FEA) simulations of a stand-alone JFET to explain the experimental results and Section 7 concludes the paper.

2. Experimental configuration and SiC cascode JFET peculiarities under UIS

UIS is a suitable methodology for evaluating the ruggedness of power devices, as described in [12]. The test circuit is shown in Fig. 1 and it consists of a DC power supply with a voltage V_{DC} of 50 V and an inductor L of 1 mH.

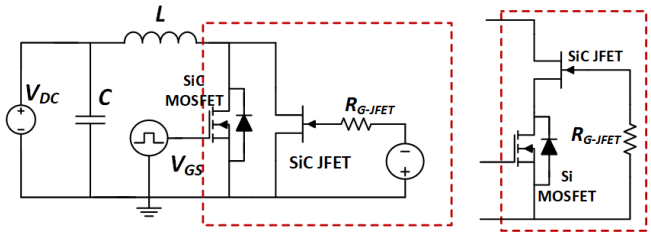


Fig. 1. UIS schematic circuit for SiC JFET and SiC cascode JFET

The stand-alone SiC JFET is a normally-ON device which required a gate driver circuit with a fixed gate-source voltage V_{GS} of -16 V to ensure that the device is OFF. An auxiliary SiC MOSFET with a breakdown voltage rating higher than the SiC JFET under test was used for charging the inductor. In the case of the cascode SiC JFET, the Device Under Test (DUT) was used for charging the inductor. When the device used for charging the inductor is ON, the current ramps at a rate V_{DC}/L and the peak current $I_{AV\text{-}PEAK}$ is defined by adjusting the duration of the gate pulse. When the device is turned-OFF, the current flows through the DUT as an avalanche current. The voltage across the device increases to its breakdown voltage V_{BR}, causing a high instantaneous power dissipation in the device.

The resulting current and voltage transient characteristics

during UIS for a SiC cascode are shown in Fig. 2 where the breakdown voltage of the device is clearly observed. The evaluated device is a 650 V/ 31 A SiC Cascode JFET from UnitedSiC.

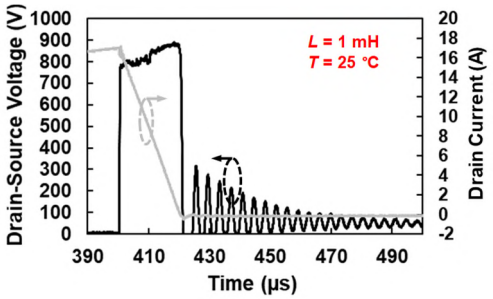


Fig. 2. UIS test – SiC Cascode, - Ambient temperature

Initial investigations [11] indicated a peculiar performance of SiC cascode JFETs, especially at high temperature, resulting in a reduced turn-OFF dV_{DS}/dt and a dip in drain-source voltage during avalanche, as shown in Fig. 3, for a case temperature of 105 °C. The case temperature T of the device was adjusted using a small DC heater attached to the device, allowing enough time to reach thermal equilibrium.

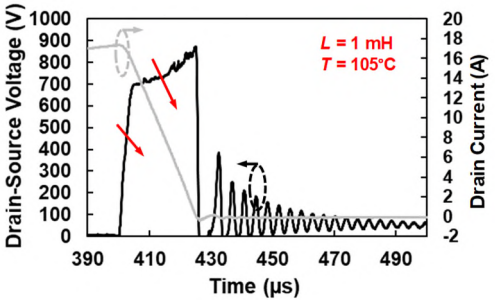


Fig. 3. UIS test – SiC Cascode, - Temperature 105°C

The authors attribute this to the gate current flowing through the internal gate resistance ($R_{G\text{-}JFET}$) of the SiC Cascode JFET as well as the positive temperature coefficient and increase of $R_{G\text{-}JFET}$. The combination of these factors results in the partial turn-ON of the SiC JFET during avalanche [4]. Hence, it is important to compare and benchmark the performance under UIS of both stand-alone and cascode SiC JFETs.

3. UIS performance of stand-alone SiC JFETs

3.1. Impact of JFET gate resistance on the UIS performance

In the commercially available SiC cascode JFET, the JFET gate terminal is not accessible, hence the role of the JFET gate resistance $R_{G\text{-}JFET}$ has been evaluated using a 650 V/ 32 A SiC JFET from UnitedSiC. Using the test circuit in Fig. 1, the gate voltage of the JFET was adjusted to -16 V and $R_{G\text{-}JFET}$ was varied from 6 to 220 Ω. The measured drain-source voltage V_{DS} and JFET gate current are shown in Fig. 4(a) and Fig. 4(b) respectively, for $I_{AV\text{-}PEAK}$ of 12.3 A at a case temperature of 25 °C. The same measurements were repeated with a case temperature of 150 °C and the results are shown in Fig. 5. Evaluating the results in Fig. 4 and 5, it is clearly observed that increasing $R_{G\text{-}JFET}$ has an impact on V_{DS} during avalanche. Increasing $R_{G\text{-}JFET}$ causes a reduction of dV_{DS}/dt during turn-OFF, a reduction in V_{DS} during avalanche and a longer avalanche duration. Analyzing the gate current, for a case temperature of 25 °C, increasing $R_{G\,JFET}$ reduces the value of the gate current, from a peak value close to 1 A for $R_{G\text{-}JFET}$=6 Ω to 80 mA peak for $R_{G\text{-}JFET}$=220 Ω.

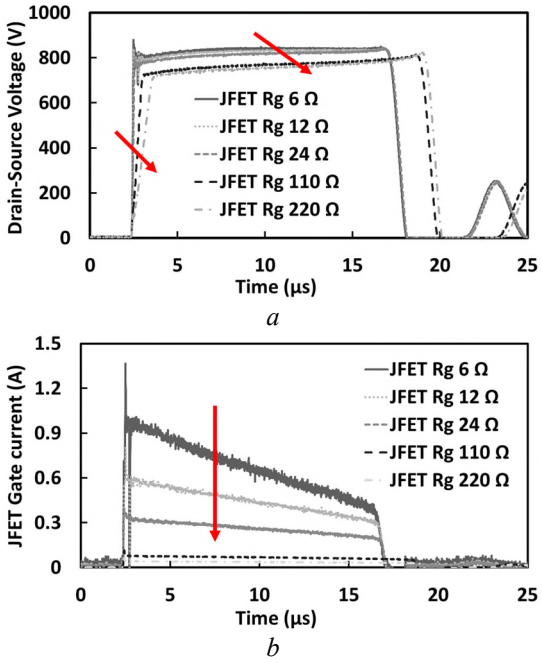


Fig. 4. Impact of $R_{G\text{-}JFET}$ during UIS (I_D=12.3 A, T=25 °C). (a) Drain-source voltage (b) JFET Gate current

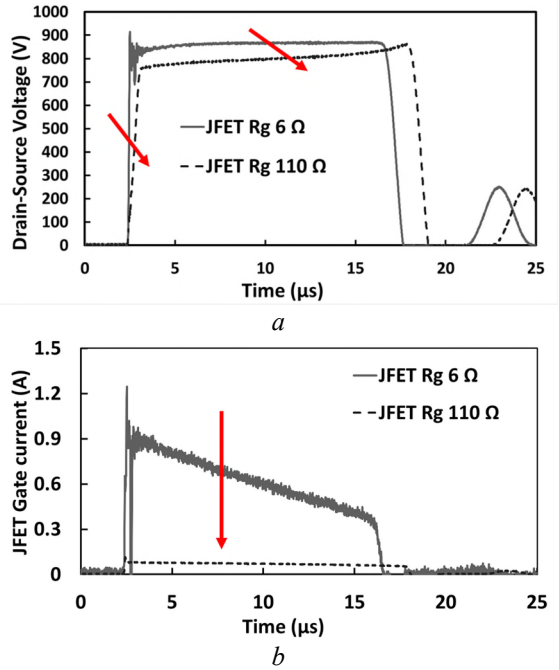


Fig. 5. Impact of $R_{G\text{-}JFET}$ during UIS (I_D=12.3 A, T=150 °C). (a) Drain-source voltage (b) JFET Gate current

Analyzing the gate current transients at 150 °C in Fig. 5(b), a similar trend is observed with temperature having a negligible impact on the gate current. Fig. 6 shows the peak JFET gate current during UIS for a combination of $R_{G\text{-}JFET}$ (6, 24 and 110 Ω) and different case temperatures (25 °C, 75 °C, 125 °C and 150 °C). The drain current for test was fixed at 10 A and the results show that temperature has no significant impact on the JFET gate current during UIS.

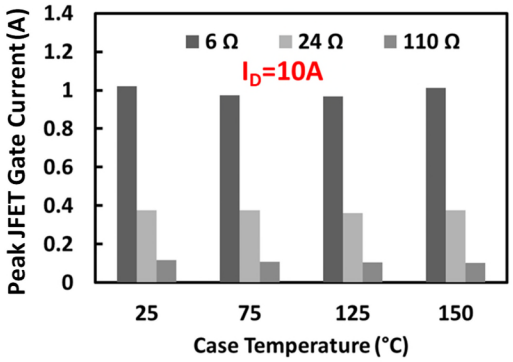


Fig. 6. Peak JFET gate current for different $R_{G\text{-}JFET}$ values at case tempearutures of 25 °C, 75 °C, 125 °C, and 150 °C

3.2. Impact of avalanche current on the UIS performance

Another important factor in the performance of the device under UIS is the peak avalanche current, as it is the parameter that will define the maximum avalanche capability of the device for a fixed inductor value. This has been evaluated for the stand-alone SiC JFET, for $R_{G\text{-}JFET}$=6 Ω and $R_{G\text{-}JFET}$= 220 Ω at both 25 °C and 150 °C case temperatures. The results are shown in Fig. 7 and Fig. 8.

At both 25 °C and 150 °C, when $R_{G\text{-}JFET}$ is 220 Ω, Fig. 7(a) and Fig. 8(a) show that as the current increases there is a V_{DS} reduction resulting from the voltage drop across $R_{G\text{-}JFET}$, which causes the operation of the JFET to go from avalanche mode to linear mode. This is not observed in Fig. 7(b) and Fig.8(b), for $R_{G\text{-}JFET}$=6 Ω, as the voltage drop across $R_{G\text{-}JFET}$ is not enough partially turn-ON the device.

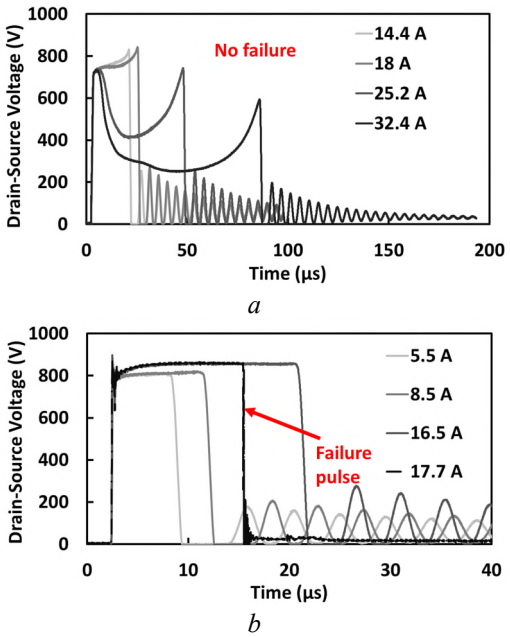


Fig. 7. Drain-Source Voltage during UIS (T=25 °C). (a) $R_{G\,JFET}$= 220 Ω (b) $R_{G\,JFET}$= 6 Ω

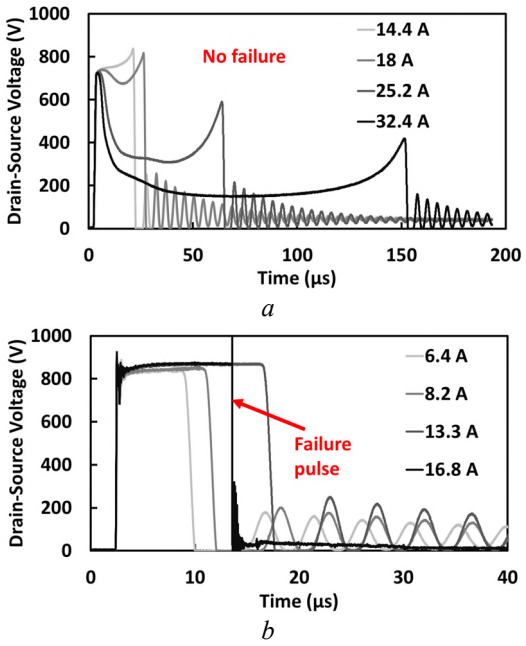


Fig. 8. Drain-Source Voltage during UIS (T=150 °C). (a) $R_{G\,JFET}$= 220 Ω (b) $R_{G\,JFET}$= 6 Ω

Analyzing the avalanche energies, in the test with $R_{G\text{-}JFET}$= 6 Ω, the energies dissipated before failure are 122 mJ (25 °C, 16.5 A) and 71 mJ (150 °C, 13.3 A). However, for $R_{G\text{-}JFET}$= 220 Ω, the device can withstand UIS pulses of 32.4 A and dissipate 555 mJ of energy without failure (at 25 °C). This energy is not actual avalanche energy since the device is not in avalanche, as it partially turns-ON as result of the gate voltage drop. This results in a reduced V_{DS} which means that UIS energy and junction temperature of the device can increase without failure.

Using the transient thermal impedance of the device provided in the datasheets, the junction temperature can be estimated using the UIS pulse power. Fig. 9 shows the calculated peak junction temperature from the tests performed in Fig. 7, for the $R_{G\text{-}JFET}$ values of 6 Ω and 220 Ω.

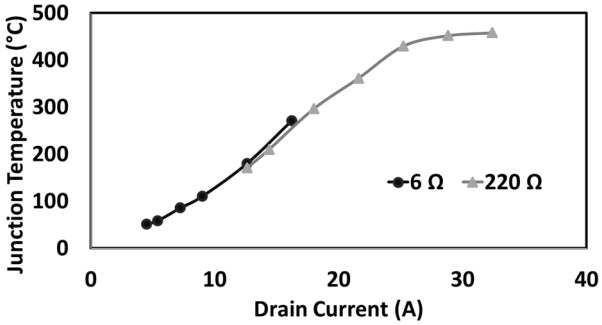


Fig. 9. Maximum junction temperature with increasing drain current for $R_{G\text{-}JFET}$ =6 Ω and $R_{G\text{-}JFET}$ =220 Ω (T=25 °C)

Evaluating results in Fig. 9, where uniform temperature distribution within the chip is assumed, the calculated junction temperature indicates that the DUT fails with a junction temperature of approximately 300 °C when $R_{G\text{-}JFET}$= 6 Ω, whereas the peak junction temperature increases above 450 °C without failure when $R_{G\text{-}JFET}$= 220 Ω. This indicates that temperature is not the only factor influencing the device failure.

4. UIS performance of SiC cascode JFETs

Given the analysis of the UIS performance of the stand-alone SiC JFET in the previous section, it is important to evaluate the UIS performance of the SiC cascode JFET. The tests were performed at 25 °C and 150 °C case temperatures, increasing the avalanche current gradually until the device failure. The results are shown in Fig. 10.

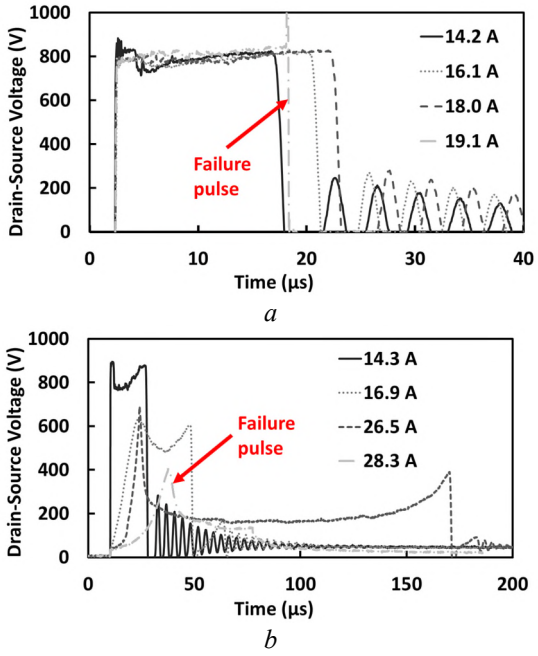


Fig. 10. UIS Drain-source Voltage for a cascode JFET at (a) 25 °C (b) 150 °C

The results at 25°C in Fig. 10(a) show the conventional UIS voltage waveform during avalanche, similar to the results of the stand-alone JFET with $R_{G\text{-}JFET}$ = 6 Ω, as shown in Fig 7(b) and Fig. 8(b). The SiC Cascode JFET withstands a maximum of 18 A and 132 mJ, which is similar to the measured avalanche energy capability of the stand-alone SiC JFET determined in the previous section.

However, the results at 150 °C in Fig. 10(b) show characteristics that require further analysis. At 150 °C, the device initially shows a slower dV_{DS}/dt at turn-OFF, more apparent as the avalanche current is increased. The results also show a characteristic V_{DS} reduction, with this V_{DS} reduction and the avalanche duration increasing as the avalanche current is increased (thereby indicating operation in linear mode).

The performance of the SiC cascode at 150 °C is similar to the performance of the stand-alone JFET with $R_{G\text{-}JFET}$ = 220 Ω, with a noticeable difference observed: a catastrophically failure at a very high current (28.3 A) for the Sic Cascode JFET. This indicates that UIS of the SiC Cascode JFET at high temperatures accelerates failure due to the positive temperature coefficient of $R_{G\text{-}JFET}$ aggravating the linear mode operation. i.e. the device becomes more susceptible to linear mode operation as the case temperature is increased during UIS. The SiC cascode JFET withstands UIS pulses of 26.5A and 411 mJ energy before failure, however it would not be accurate to define this as avalanche energy capability since it is not undergoing UIS as a conventional device would.

It is important to note that although the stand-alone SiC JFET (with high gate resistance) and SiC cascode JFET (at high temperatures) show similar UIS transients, the stand-alone SiC JFET does not fail. The authors attribute this to the different power rating of the gate resistance used, indicating that the failure is originated due to the robustness of the gate path.

5. Repetitive UIS in SiC JFETs

From the previous section, it is clear that $R_{G\text{-}JFET}$ is important for single shot UIS performance. Previous studies have investigated the optimization of $R_{G\text{-}JEFT}$ for improved losses [13, 14] whereas in this paper, its impact on robustness under repetitive UIS is considered. Repetitive UIS tests were performed on both the stand-alone JFET and SiC Cascode JFET using the circuit in Fig. 11. In this setup, two auxiliary transistors (Q1 and Q2) are used. Q1 (with a higher current and voltage rating than the DUT) is used to isolate the DUT from the DC supply during avalanche of the DUT, whereas Q2 (with a higher current and voltage rating than the DUT) is used for charging the inductor as DUT is always OFF. The diode *D* is used for clamping the inductor during avalanche. The two auxiliary transistors control the charging and discharging of the inductor *L* as well as failure detection.

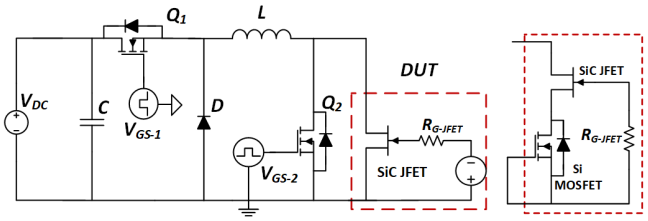


Fig. 11. Repetitive UIS schematic circuit

For the repetitive UIS tests, an inductor of 1 mH and a DC voltage of 50 V were used. To control the junction temperature rise from self-heating during repetitive UIS, the pulse period was set to 100 ms. Furthermore, an aluminium block was also used as a heatsink for the DUT to monitor the temperature. In the stand-alone JFET, the gate was biased at -16 V with a gate resistance of 6 Ω whereas in the case of the cascode, the gate of the LV MOSFET was shorted to the source. Both devices have similar current ratings: 31 A for the SiC cascode JFET and 32 A for the stand-alone SiC JFET. The tests were performed at ambient temperature, using a cumulative approach: starting from 5 A, the avalanche current was increased in steps of 2.5 A every 20000 pulses. The results of the repetitive avalanche tests are shown in Fig. 12(a) for the stand-alone SiC JFET and Fig. 12(b)

for the SiC Cascode JFET.

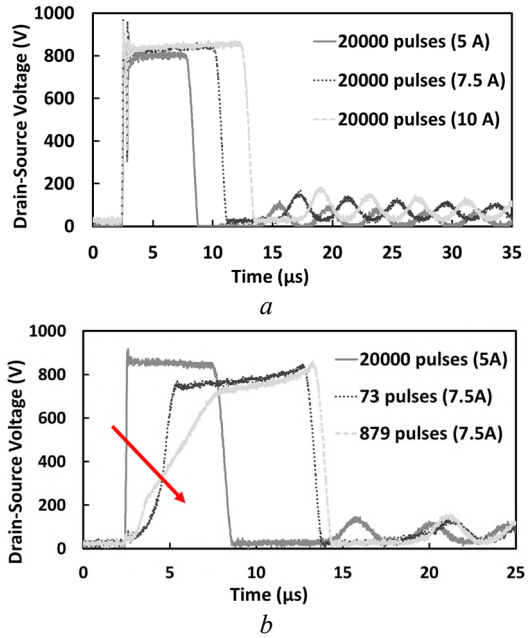


Fig. 12. Repetitive UIS tests (a) Stand-alone JFET ($R_{G\text{-}JFET}$=6 Ω) (b) Cascode JFET

The results show that both devices can withstand 20000 UIS pulses at 5 A, with the cascode JFET not showing any significant degradation. However, when the current is increased to 7.5 A, while the stand-alone SiC JFET can withstand 20000 UIS pulses, the SiC Cascode JFET shows degradation of the gate path after 73 pulses at 7.5 A, becoming more apparent as the number of pulses is increased to 879 pulses.

This suggests the progressive degradation of the $R_{G\text{-}JFET}$ from repetitive UIS pulses. The positive temperature coefficient of $R_{G\text{-}JFET}$ means more apparent reduced dV_{DS}/dt as well as V_{DS} reduction during avalanche, with these characteristics becoming more easily observable as the device progressively gets closer to failure. In summary, Fig. 12 shows that the stand-alone SiC JFET can withstand up to 20000 UIS pulses at 10 A, while the SiC cascode JFET starts showing progressive degradation at 7.5 A.

6. Simulation results

In this section, a stand-alone SiC JFET model is developed in SILVACO and UIS simulations are performed to further investigate the experimental results. The model for the JFET used for the simulations has a drift layer N doping (N_{drift}) and channel region P doping (N_{ch}) of 2.33 x 10^{16} cm^{-3}, and two highly doped N^+ regions of 1 x 10^{19} cm^{-3}. The channel width and length of the model are 1 µm and 1.5 µm respectively.

The drift layer thickness W_{DRIFT} is set to 6.15 µm. Using W_{DRIFT} and a critical electric field E_C of 2.6 MV/cm [15], the theoretical breakdown voltage V_{BR} is 800 V, in the range of the experimental results. Simulations were done with the same circuit schematic illustrated in Fig.1 using the SILVACO mixed mode circuit simulator. The physical models specified included mobility (FLDMOB, CVT, ANALYTIC), recombination (SRH, AUGER), carrier statistics (BGN), and impact ionisation (IMPACT SELB). The model was fully electrothermal by using LAT.TEMP.

Fig. 13 presents the drain-source voltage transients during UIS for $R_{G\text{-}JFET}$= 6 Ω, and $R_{G\text{-}JFET}$ = 220 Ω, acquired from the mixed mode simulation. The case temperature was constant at 25 °C and the peak drain current was set at 10 A. This figure shows the impact of varying the JFET gate resistance on the UIS voltage, reproducing the trend observed in the experimental results in Fig. 4 and Fig. 5.

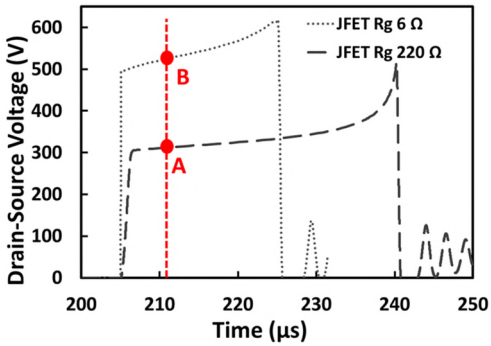


Fig. 13. Simulated UIS Drain-Source voltage of JFET structure

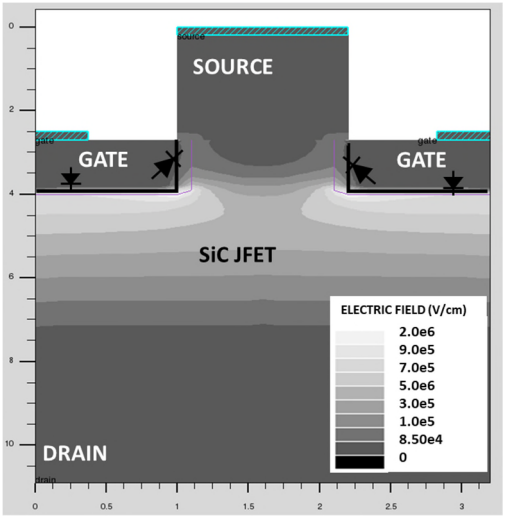
When $R_{G\text{-}JFET}$ = 6 Ω, the JFET goes into avalanche and a high V_{DS}, around 600 V, is observed. However, when $R_{G\text{-}JFET}$= 220 Ω, the simulated V_{DS} transient shows a slower dV_{DS}/dt at turn-OFF together with the reduction of V_{DS} to approximately 300 V, thereby indicating linear mode operation.

The 2D profiles of the simulated electric field and current density are shown in Fig.14 and Fig. 15 respectively. In Fig. 14(a), which represents the case labelled A in Fig. 13 ($R_{G\text{-}JFET}$=220 Ω), the JFET drift layer is not fully depleted (linear mode operation) and the corresponding current density profile in Fig. 15(a) shows negligible current through the gate, as already observed in the experimental results in Fig. 4(b) and Fig.5(b).

In contrast, for case B in Fig.13 ($R_{G\text{-}JFET}$ =6 Ω), Fig. 14(b) shows the full depletion in the JFET drift layer and Fig. 15(b) clearly shows current going through the gate-drain junction. In this case, the voltage across the $R_{G\text{-}JFET}$ is not high enough to cause linear mode operation (partial depletion in drift region).

7. Conclusions

This paper investigated the unusual performance of SiC Cascode JFETs during UIS at high temperatures by comparing the single and repetitive avalanche performance of SiC cascode JFETs with stand-alone SiC JFETs. Both commercially available SiC Cascode JFETs and stand-alone SiC JFETs were evaluated and the results show that the positive temperature coefficient of the JFET gate resistance in the SiC Cascode JFET is critical since it caused linear mode operation during UIS. This was also a limiting factor during repetitive avalanche testing of the SiC Cascode JFET. The failures observed were reproduced using 2D FEA simulations showing the underlying physical mechanisms behind unusual characteristics of SiC Cascode JFETs under UIS.



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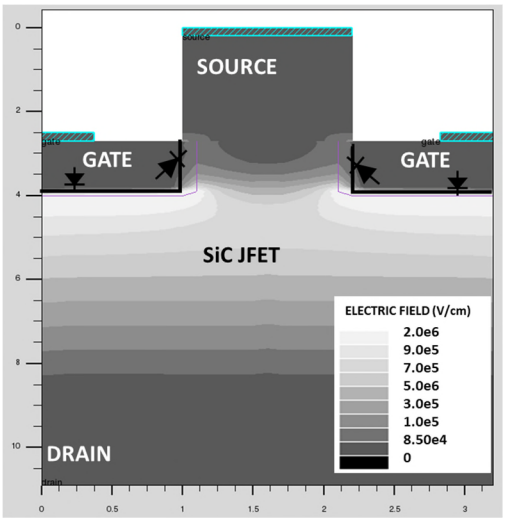
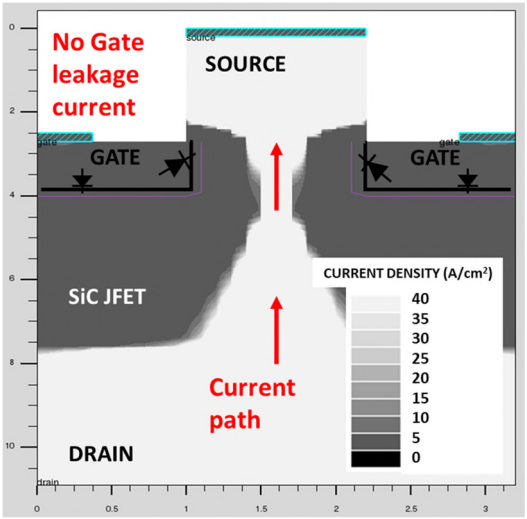


b

Fig. 14. 2D plots of electric field at marked points in Fig. 13
(a) $R_{G\text{-}JFET}$ = 220 Ω (b) $R_{G\text{-}JFET}$ = 6 Ω



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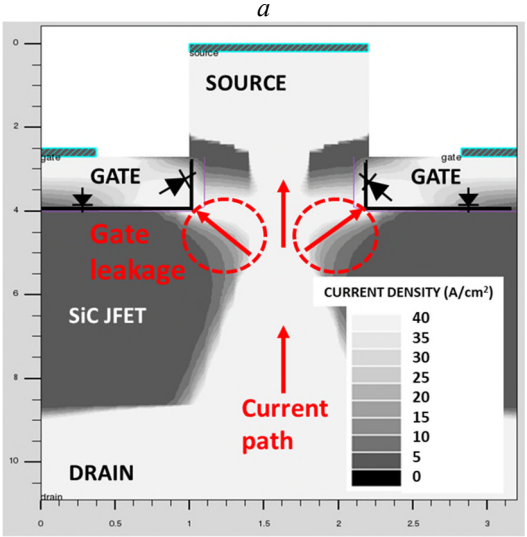

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Fig. 15. 2D plots of current density at marked points in Fig. 13
(a) $R_{G\text{-}JFET}$ = 220 Ω (b) $R_{G\text{-}JFET}$ = 6 Ω

Acknowledgements

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