A 10 nV/rt Hz noise level 32-channel neural impedance sensing ASIC for local activation imaging on nerve section

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***Abstract*— A 10 nV/rt Hz noise level 32-channel neural impedance sensing ASIC is presented for the application of local activation imaging in nerve section. It is increasingly known that the monitoring and control of nerve signals can improve physical and mental health. Major nerves, such as the vagus nerve and the sciatic nerve, consist of a bundle of fascicles. Therefore, to accurately control a particular application without any side effects, we need to know exactly which fascicle was activated. The only way to find locally activated fascicle is to use electrical impedance tomography (EIT). The ASIC to be introduced is designed for neural EIT applications. A neural impedance sensing ASIC was implemented using CMOS 180-nm process technology. The integrated input referred noise was calculated to be 0.46 µVrms (noise floor 10.3 nVrms/rt Hz) in the measured noise spectrum. At an input of 80 mV, the squared correlation coefficient for linear regression was 0.99998. The amplification gain uniformity of 32 channels was in the range of + 0.23% and – 0.29%. Using the resistor phantom, the simplest model of nerve, it was verified that a single readout channel could detect a signal-to- noise ratio of 75.6 dB or more. Through the reservoir phantom, real-time EIT images were reconstructed at a rate of 8.3 frames per second. The developed ASIC has been applied to in vivo experiments with rat sciatic nerves, and signal processing is currently underway to obtain activated nerve cross-sectional images. The developed ASIC was also applied to in-vivo experiments with rat sciatic nerves, and signal processing is currently underway to obtain locally activated nerve cross-sectional images.**

***Clinical Relevance*— This introduces a tool for non-invasive viewing of locally activated fascicles in a nerve cross section.**

I. Introduction

Electroceuticals is an implantable device that monitors and stimulates nerves to improve physical and mental health [1]. Body organs communicate using electrical signals through nerves with brain. Monitoring nerve communication can tell you about the state of organs, and manipulating nerve communication gives you control over organ function. Moving proximally from distal point, the nerves merge and become a bundle. For example, the sciatic nerve includes the tibial and peroneal fascicles. When non-invasively monitoring the sciatic nerve, the mixed signal from the two fascicles is monitored. Monitoring using biopotential signals cannot identify locally activated points. The only way to identify locally active points is to use nerve EIT [2].

Fig. 1 illustrates the principle of neural impedance change detection. As the action potential moves along the fascicle, the ion channels of the fascicle open and the cross-sectional impedance is lowered. Injecting the carrier current through the electrodes (*E1* and *E2*), the voltage coupled to the internal impedance change is induced on the electrodes (*E3* and *E4*). It is necessary to limit to low carrier current magnitudes to avoid unwanted nerve stimulation.

To be able to indicate a local activation point, the required multiple electrode arrays and connection configuration are shown in Fig. 2. The electrodes on the outer two rings are commonly connected to all negative inputs. Each electrode of the inner two rings is connected to the respective positive input of the read amplifier. Multiple measurements are required for multiple current injection pairs. Current injection pair can be a combination of different electrodes. Thus, each output of the current source must be selectively connectable to any electrode. In Reference 2, the authors showed locally activated neural EIT images using current source instrument and recording instrument. In this paper, instruments used in the previous work are integrated on one chip to make implantable in the body and the performances of the chip are

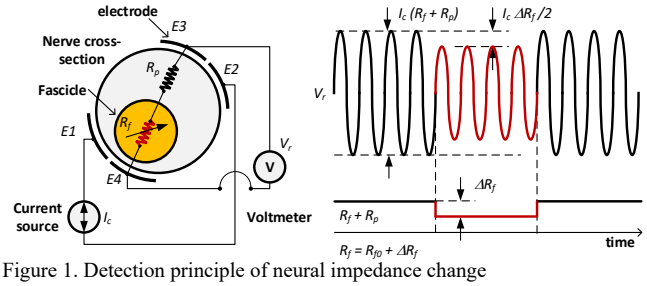

Figure 1. Detection principle of neural impedance change

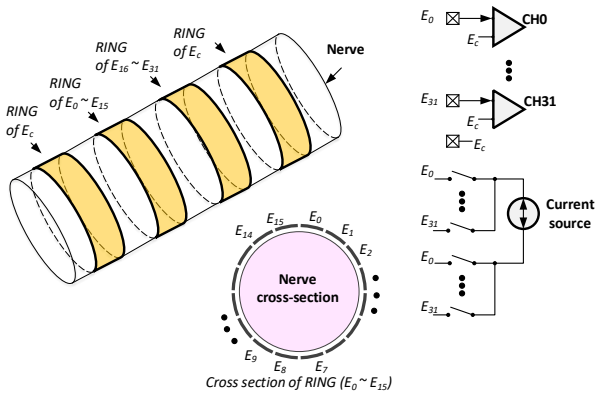

Figure 2. Detection configuration for nerve EIT application

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evaluated.

II. Circuit Architecture and Design

A top architecture of the multi-channel neural impedance detection ASIC is shown in Fig. 3. The ASIC consists of main blocks such as current source (CS), switch group for controlling the connection from the current source to electrodes (CS2EL_MUX), 32 readout channels (CH0 ~ CH31), 16 analog-to-digital converters (ADC0 ~ ADC15), bias block to support analog blocks (BIAS), and digital blocks (DIG_GR).

The current source consists of a seed current generator (ISEED_GEN), a shape generator (SHAPE_GEN), and a current path changer (CPC). A seed current generated from

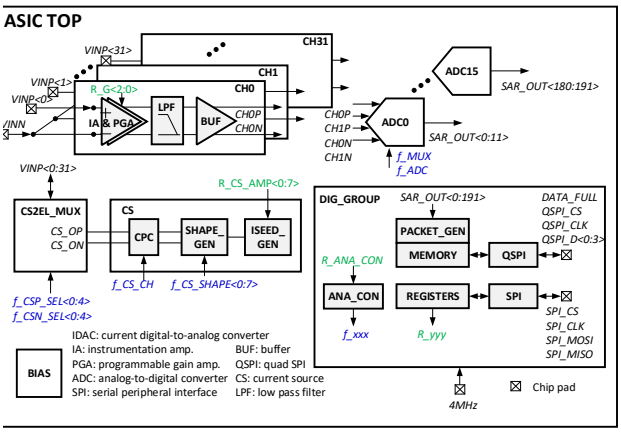


Figure 3. Top architecture of multi-channel neural impedance detection ASIC

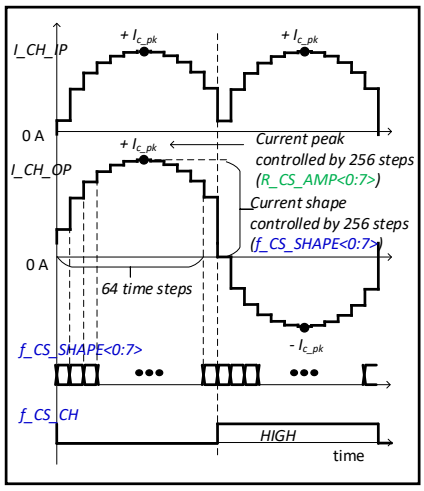
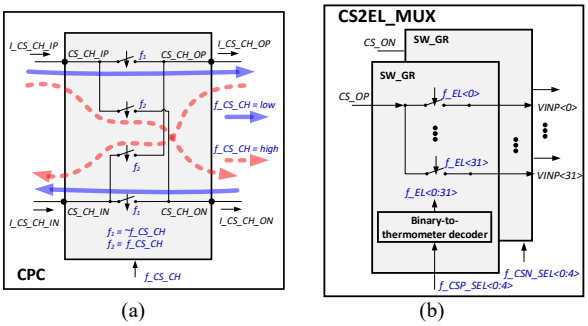


Figure 4. Bipolar pseudo-sine current generation



(a) (b)

Figure 5. Circuit details of (a) current path changer and (b)

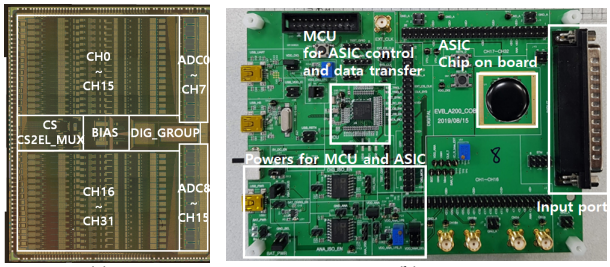
ISEED_GEN can be adjusted in 256 steps by controlling the register (R_CS_AMP<0:7>). The shape generator can produce any shape signal with 64 timely different 256 amplitude steps by controlling *f_CS_SHAPE<0:7>*. The LSB current in the shape generator corresponds to the seed current from the seed current generator. Fig. 4 shows how the current source produces a full pseudo-sine wave current. The shape generator produces the first half phase of the pseudo-sine current (*I_CH_IP*) repeatedly, and then the current path changer completes the entire phase of the pseudo-sine current (*I_CH_OP*). Fig. 5(a) shows the details of the current path changer, in which the polarity of the connection between the input and output ports changes according to the current path changer control signal (*f_CS_CH*). The each two current ports (*CS_OP* and *CS_ON*) from the current source can be connected to one of the 32 electrode inputs (*VINP<0>* ~ *VINP<31>*) as shown in Fig. 5(b).

The readout channel consists of an instrumentation amplifier (IA), a programmable gain amplifier (PGA), a low pass filter (PGA), and a buffer (BUF). The IA has a capacitively-coupled IA (CCIA) architecture with a fixed gain [3]. To improve the common input impedance, the common mode signal of an operational amplifier (OP-AMP) is amplified and fed back to the inputs. To improve the differential input impedance, the output of the IA is positively fed back to the inputs. The OP-AMP has a folded-cascade architecture for a wide input range [4]. The feedback pseudo-resistor in the CCIA is implemented using diode connected PMOS and has a two-step value for fast settling situation. A fast settle control signal generator monitors whether the common signal from the OP-AMP exceeds a predetermined boundary. When the common signal crosses the boundary, a fast settle control signal is enabled, the feedback resistance of the CCIA becomes smaller, and the CCIA settles faster. Once the common signal comes within the boundary, the fast settle control signal is disabled and the feedback resistance of the CCIA returns to its normal value. The PGA also has a CCIA architecture and has eight levels of variable gain. The LPF is added to eliminate an aliasing noise before ADC sampling.

The analog outputs of two readout channels are multiplexed to one ADC using the ADC input MUX control signal (*f_MUX*). The ADC has a 12-bit asynchronous successive approximation (SAR) type and oversamples 8 times to achieve 15-bit resolution using the ADC conversion control signal (*f_ADC*) [5].

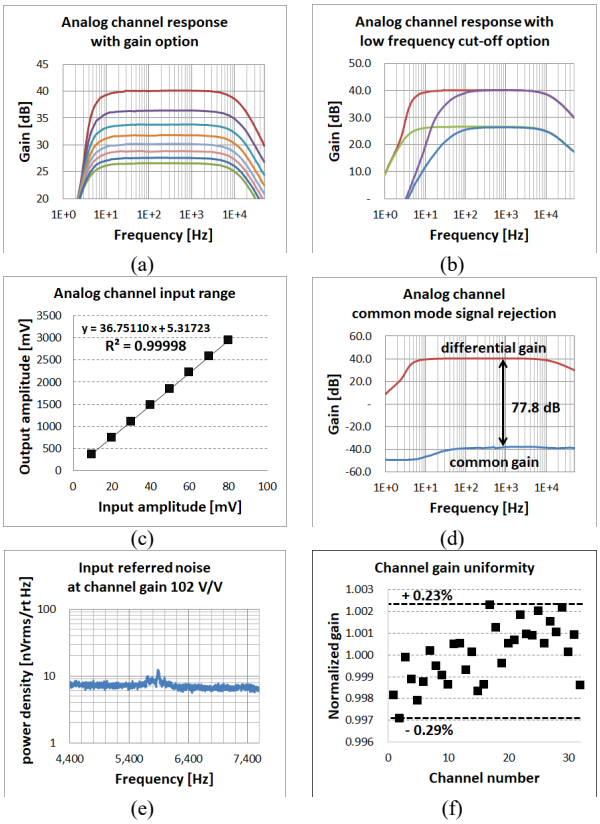
The digital blocks (DIG_GROUP) consist of SPI, REGISTERS, ANA_CON, PACKET_GEN, MEMORY, and QSPI. The register sets can be changed through the serial peripheral interface (SPI). The REGISTERS manages all static sets inside the ASIC (e.g. read channel gain, current amplitude, current shape, etc.). At ANA_CON, control and clock signals are generated based on the system clock of 4 MHz. For EIT application, the current injection pair can shift automatically by changing the CS-to-electrode MUX control signals (*f_CSP_SEL<0:4>* and *f_CSN_SEL<0:4>*). The CS-to-electrode MUX control signals can be also programmable by register set. In PACKET_GEN, eight oversampled 12-bit ADC data are averaged and converted to 15-bit data. A data packet is formed of a 15 bit data and a 1 bit

header representing the data packet. In addition, an information packet is generated for every 32 data packets. In MEMORY, 32 data packets and one information packet are buffered consecutively. When the preset buffering limit is reached, a pulse event occurs on the memory full alarm signal (*DATA_FULL*). An external MCU then reads packets from MEMORY using quad serial peripheral interface (QSPI).



(a) (b)

Figure 6. Photography of (a) ASIC (8 mm × 10 mm) and (b) evaluation board



(a) (b) (c) (d) (e) (f)

Figure 7. Measured ASIC performance

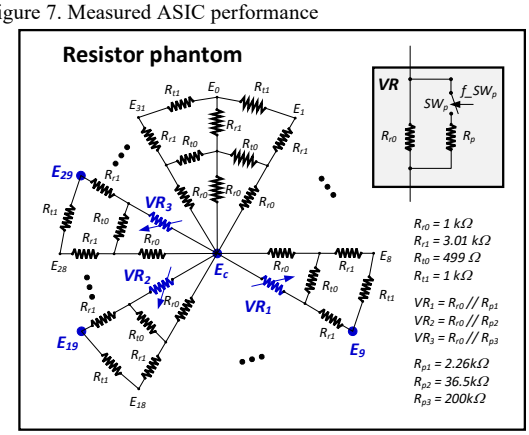


Figure 8. Structure and values of resistor phantom

QSPI transfers 16 Mb data per second (16 bits × 33 packets × 30 kHz).

III. Fabrication and Measurement Results

The designed circuit is implemented using 180-nm CMOS process technology, as shown in Fig. 6(a). The size of the ASIC is 8 mm × 10 mm. The main blocks in Fig. 3 are marked on the chip photograph. To evaluate performance, the ASIC is wirebonded to the PCB and molded with black compound epoxy as shown in Fig. 6(b). A MCU receives a set of registers from PC using UART and passes it using SPI to the ASIC. The MCU reads data from the ASIC using QSPI and transfers data to PC using USB.

A. Circuit Characteristics

Fig. 8(a) shows the measured frequency response curves of the ASIC. The amplification gain of the readout channel can be programmable from 21.4 V/V to 102.1 V/V in 8 steps. The upper – 3 dB cut-off frequency is 15.1 kHz, and the lower – 3 dB cut-off frequency can be selected between 5.4 Hz and 50 Hz as shown in Fig. 8(b). The relationship of the readout channel output amplitude to the input amplitude is displayed in Fig. 8 (c). The input dynamic range reaches 80 mV with a squared correlation coefficient of 0.99998. The common mode rejection ratio is calculated as 77.8 dB with a common mode input signal of 1 Vpp as shown in Figure 8 (d). The input referred integrated noise level of readout channel integrated from 5 kHz to 7 kHz at the maximum gain was calculated to be 0.46 μVrms based on the measured noise power spectrum as shown in Fig. 7(e). Since the effective frequency bandwidth of neural signals is 1 kHz, the noise bandwidth is defined as 5 kHz to 7 kHz when the signal is modulated with a carrier frequency of 6 kHz. The amplification gains of 32 readout channels are normalized and plotted in Fig. 7(f). The gain difference among readout channels ranges from + 0.23% to – 0.29%.

B. Resistor Phantom Test

To evaluate basic impedance sensing performance, a resistor phantom is used that simply models the nerve cross-section as resistors. The impedance depends on the type and dimensions of the nerve, but the equivalent resistance can be assumed to be approximately 1 kΩ for a simple test [6]. The resistor network structure and resistor's values are plotted in Fig 8. A variable resistor is implemented with a parallel resistor (R_p) and a connection switch (SW_p). The change in VR_1 (, VR_2, and VR_3) is designed so that the resistance change between E_c and E_9 (, E_{19}, and E_{29}) is 1% (, 0.071%, and 0.017%). The common node (E_c) is connected to the negative input (*VINN*) and the surface nodes from E_0 to E_{31} are connected from *VINP <0>* to *VINP <31>*, respectively. In the resistor phantom, the resistance of the variable resistor (VR_3) toggled between two resistance values at 0.5 second intervals. The signal difference due to resistance change overcomes noise and can be distinguished, therefore, the signal-to-noise ratio is greater than 75.6 dB.

C. Reservoir Phantom Test and Image Reconstruction

A reservoir phantom for setting up image reconstruction using EIT technology was used as a test object. Image reconstruction procedures are as shown in Fig. 9. Reservoir phantom is divided into small elements that describe

geometrical and electrical properties to create a finite element method (FEM) model. Measuring reservoir phantom without an inserted object produces reference data. With the FEM model and reference data, the forward solver generates Jacobian matrix used for image reconstruction. Jacobian matrix contains information about the relationship between conductivity and voltage. After that, data coming in from the reservoir phantom in real time is processed for filtering and envelope detection. Inverse solver generates conductance data using Jacobian matrix and preprocessed data. Finally, the conductance map is visualized based on the conductance information. A detailed reference can be found in [6].

The reservoir phantom with an inner diameter of 20 cm is a tubular tank containing 10 liters of brine as shown in Fig. 10(a). The stainless steel electrodes are placed inside the tank in a circular manner at the same distance. Data collected during eight current injection pairs creates one reconstructed image. After collecting data from current injection pair at electrodes 0 and 7, data collection is repeated by moving the current injection pair to electrodes 1 and 8. The carrier frequency and amplitude of the injected current are 6 kHz and 30 uA, respectively. A plastic tube with an outer diameter of 5 cm and a thickness of 3 mm is inserted and stirred in a circular manner. Conductance images are reconstructed at a rate of 8.3 frames/second and two snapshots are captured in Fig. 10 (b).

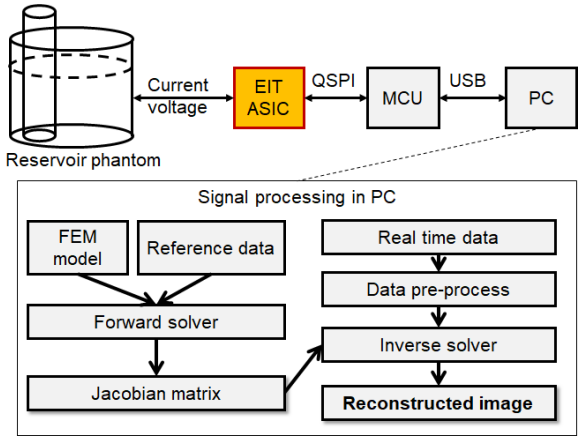
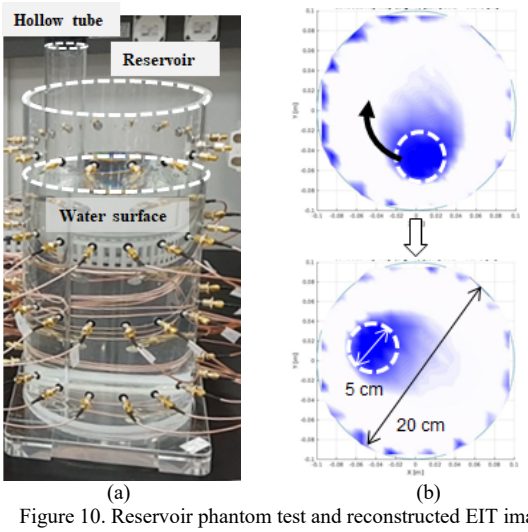


Figure 9. EIT image reconstruction signal process flow



(a) (b)

Figure 10. Reservoir phantom test and reconstructed EIT image

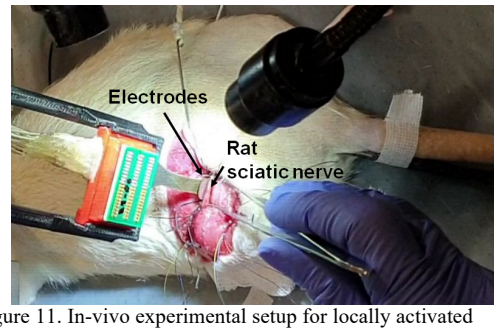


Figure 11. In-vivo experimental setup for locally activated imaging of rat sciatic nerve

D. In-vivo Test and Image Reconstruction

The neural impedance sensing ASIC has also been applied to in-vivo experiment in a rat sciatic nerve. Nerve stimulation at a distal position initiates an artificial action potential that moves proximally along the nerve. The measured data is truncated to a fixed length from the point of occurrence of the stimulus artifact. Averaged truncation data to improve the signal-to-noise ratio is used for image reconstruction. Fig. 11 shows in-vivo experimental setup for obtaining rat sciatic nerve data.

IV. Summary

A neural impedance sensing ASIC was designed and implemented using CMOS 180-nm process technology. The integrated input referred noise was calculated as 0.46 µVrms (noise floor 10.3 nVrms/rt Hz). At an input of 80 mV, the squared correlation coefficient for linear regression was 0.99998. The amplification gain uniformity of 32 channels was in the range of + 0.23% and – 0.29%. Using the resistor phantom, the simplest model of nerve, it was verified that a single readout channel could detect a signal-to- noise ratio of 75.6 dB or more. Through the reservoir phantom, automatic current injection pair shifting was performed and real-time EIT images were reconstructed at a rate of 8.3 frames per second. The developed ASIC was also applied to in-vivo experiments with rat sciatic nerves, and signal processing is currently underway to obtain locally activated nerve cross-sectional images.

References

[1] K. Famm, B. Litt, K.J. Tracey, E.S. Boyden, M. Slaoui, "A jump-start for electroceuticals," *Nature*, vol. 496, pp. 159–161, April 2013.

[2] K. Astrovich, M. Donega, C. Blochet, J. Avery, S. Hannan, D. Chew, and D. Holer, "Imaging fast neural traffic at fascicular level with electrical impedance tomography: proof of principle in rat sciatic nerve," *IOP J. Neural Eng.*, vol. 15, pp. 1–12, August 2018.

[3] J. Kim and H. Ko, "Self-biased ultralow power current-reused neural amplifier with on-chip analog spike detections," *IEEE Access*, vol. 7, pp. 109792– 109803, August 2019.

[4] E. Bharucha, H. Sepehrian, and B. Gosselin, "A survey of neural front end amplifiers and their requirements toward practical neural interfaces," *MDPI J. Low Power Electron. Appl.*, vol. 4, pp. 268– 290, November 2014.

[5] M. Seo, D. Jin, Y. Kim, J. Kim, D. Chang, W. Lim, J. Chung, C. Park, E. An, S. Ryu, "A Single-Supply Buffer-Embedding SAR ADC with Skip-Reset Having Inherent Chopping Capability," in *Proc. IEEE Asian Solid-State Circuits Conference*, Macao, China, 2019, pp. 189–192.

[6] https://github.com/EIT-team.