Novel approaches in voltage-follower design

by

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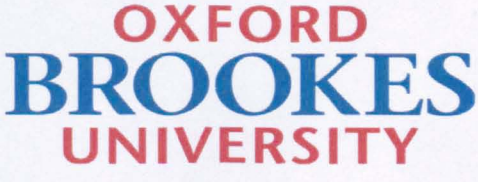

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Nikolaos Georgios Charalampidis
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To my parents

Georgios and Anna Charalampidis

Abstract

The aim of this research programme was to design and develop novel voltage-followers/buffers, suitable for radio frequency (RF) applications. The emphases throughout has been on improving key characteristics, in particular distortion, operating bandwidth, input and output impedances, offset-voltage and power supply demands of the design. The majority of the results of this work have been reported by the author in the technical literature **[1] to [6]**.

Initially this research focuses on the investigation of the underlying operating principles of the voltage-follower to provide an in-depth understanding of its operation. This study concentrates on establishing reasons for the poor distortion, low input and high output impedances and increased offset-voltage and confirmed that these designs have inherently poor performance in these parameters. The analysis is carried out using both theoretical modelling and computer simulation, using the well-established software package ORCAD PSpice. Despite the availability of high performance computer simulation tools, it becomes apparent that 'hand' calculations in the design process, generally based on DC and small-signal transistor parameters, are essential. Therefore a detailed analysis of the transistor-models used throughout this research is carried out with PSpice data.

Using the analytical results of the conventional voltage-follower as a benchmark, various novel circuit techniques investigated. Several new circuits are proposed with respect to improving the previously mentioned key characteristics. The first technique comprises local feedback and single-valued current biasing and

consists of emitter-followers exclusively throughout the signal path, keeping the distortion of the input signal to low levels **[1]**, **[2]**. The second technique is based on local feedback with double-valued current biasing, increasing somewhat the power dissipation but reducing, notably, the distortion of the configuration **[3]**, **[4]**, **[5]**, **[6]**. The final technique employs the emitter-followers throughout the signal path in combination with global feedback and double-valued current biasing, which presents significantly better results, on certain parameters, than conventional and existing configurations. It is anticipated that this work will be published in the near future.

Publications by the author

[1] Charalampidis N., Hayatleh K., Hart B.L., Lidgey F.J., 'A voltage 'Super follower'', IEEE Proceedings of IEE ASP2004, Oxford, UK, 2004, pp.11-1 to 11-5.

[2] Charalampidis N., Hayatleh K., Hart B.L., Lidgey F.J., 'A High Frequency Low Distortion Voltage-Follower', IEEE Proceedings of International Conference on Communications, Circuits and Systems, ICCCAS 2006, Gui Lin, China, June 2006, Vol. IV, pp.2291-2295.

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[6] Charalampidis N., Hayatleh K., Hart B.L., Lidgey F.J., 'A high-frequency voltage-follower designs based on local feedback techniques', IEEE Proceedings of IEE ASP2006, Oxford, UK, 2006, pp. poster2-1 to poster2-6.

List of principal symbols

Av, A	Op-amp open-loop voltage gain
A_{CL}	Magnitude of closed-loop d.c. voltage gain
BJT	Bipolar Junction Transistor
BW	Bandwidth
β	Transistor DC current gain
γ	Transistor emitter injection efficiency
CB	Common-base
CC	Common-collector
CM	Current-mirror
C_{μ}	Base-collector capacitance
C_{π}	Base-emitter capacitance
EF	Emitter-follower
f_{T}	Transistor unity-gain frequency
$f_{\text{-3dB}}$	Closed-loop -3dB frequency
g_m	Transconductance
I_S	Forward saturation current
IMD	Intermodulation distortion
λ	Current-mirror transfer coefficient
r_{π}	Transistor base-emitter incremental resistance
r_{ce}	Transistor collector emitter incremental resistance
r_e	Transistor emitter incremental resistance
r_i	Input resistance
r_O	Output resistance
ε	A.C.-gain error
THD	Total harmonic distortion
VT	Thermal voltage (KT/q)
V_A	Early Voltage
V_{OS}	Input-referred offset-voltage
V_{BE}	Transistor base-emitter voltage
VF	Voltage-follower
$XFCB$	Extra fast complementary bipolar

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Chapter 4. The conventional emitter –follower / a critical review

Appendix 4.

CHAPTER 1

Introduction to the thesis

1.1 The voltage-follower

The subject of this thesis is voltage-follower (VF) design. VFs are one of the most commonly encountered building blocks, found in almost all analogue systems. An ideal voltage-follower is a unity-gain voltage amplifier with infinite bandwidth, infinite input impedance and zero output impedance, which implies infinite current gain, as well as offset voltage and zero input bias current **[1-1]**. Functionally, it is an analogue buffer able to transfer an input voltage from a signal source to a lower impedance load, without taking any current from the input source. In reality the bandwidth will be limited and as, also, will be the desired input and output impedance levels. The focus of this research is on the design and development of novel voltage-follower architectures with the goal of achieving high-frequency bandwidth and low distortion performance.

1.2 Historical perspective of the voltage-follower

The voltage-follower is a configuration that has been in use for over 100 years. The original voltage-follower in vacuum or valve technology is the cathode-follower, the second most common electron-tube circuit in use after the common-cathode amplifier. This circuit dates back to the early days of the thermionic valve or electron tube, to the beginning of the last century **[1-2 to 1-5]**, after which developments of the bipolar transistor in the early 1950s led to the replacement of the electron tube mainly, due to the lower cost, size and improved reliability.

The impact of the cathode-follower amplifier with negative feedback was significant because it reduces distortion level. The principal application of the circuit was to isolate amplifying stages from each other due to the very high input impedance and very low output impedance inherent features of the cathode-follower. It was widely used in the radio-transmitters **[1-6]** at 1920s, TV sets at 1930s **[1-5]**, and several biomedical applications at 1950s **[1-7]**, **[1-8]**.

Later, at early 1950s, the bipolar transistor was born, using semiconductor material **[1-9]**, replacing gradually the majority of electron-tube based configurations with transistor-based circuits. The need for buffering between amplifier stages was greater in bipolar circuit design than electron-tube design due to the lower input impedance of the common-emitter stage. Voltage-followers, the bipolar equivalent of the cathode-follower, were useful as input and output stages and they were integrated into the chip. In order to optimize performance, companies like National Semiconductors created dedicated integrated circuits specially designed as voltage-followers, such as the LM102, in 1967 **[1-10]**.

Nowadays, several voltage-follower configurations exist in an integrated circuit form and others have been presented recently, claming they exhibit superior performance to existent configurations **[1-11 to 1-30]**. Nevertheless, in almost every case there is a trade-off between operating bandwidth, signal distortion, slew rate and power dissipation. The inter-dependence of these parameters is complex and optimisation of any voltage-follower design to maximise performance is a major challenge.

1.3 Negative feedback / local and global

Although a thorough review of negative feedback is inappropriate here, a brief reference is necessary to provide a basis for the design and development of the voltage-follower. The work presented here is divided into two main circuit categories; the local feedback and the global feedback.

Negative feedback has been used for many years mainly for amplifier linearization, **[1-31 to 1-33]**. It is a process whereby a linear proportion of the output signal is subtracted from the input. That results in an effectively constant gain, independent of the signal level, thereby improving the overall distortion of the circuit. Additionally, using negative feedback the designer has the flexibility to increase the input impedance and decrease the output impedance of the circuit, desirable characteristics of voltage-follower designs. Furthermore, using a negative feedback, the operating bandwidth of a circuit can be increased, at the expense of the overall gain. Finally, the gain of an active device can be precisely controlled becoming less sensitive to the variations of active device parameters and the tolerances of circuit components, as well as such factors as the ambient operating temperature.

On the other hand, there are two significant drawbacks when using negative feedback. Firstly, limitation in the maximum gain that can be achieved, which is unavoidable since it is directly related to the benefits achieved. Secondly, the tendency of the circuit to oscillate if, under certain conditions, the feedback changes from negative to positive **[1-34]**, **[1-35]**.

Negative feedback is divided by the author into two main categories, local feedback and global feedback. The first is concerned with linearising an individual stage, improving the distortion and reliability of the circuit **[1-36]**. It provides gain stabilisation and is preferred in configurations with small number of cascaded stages. Nevertheless, under specific operating conditions, each feedback loop modifies the signal and generates distortion which is additive when multiple stages used.

However, global feedback is considered to give much better results than several small local feedback loops, but only if the amplifier has a high open-loop gain. Global feedback contributes to the removal of significant amount of distortion from all stages at once, overcoming the effect of additive distortion from each cascaded stage **[1-37]**, **[1-38]**. The main drawback of this type of feedback is the requirement for a dominant-pole capacitor, to prevent sustained circuit oscillations. Consequently, the bandwidth of the circuit will reduce as well as the open-loop gain at higher frequencies.

1.4 Thesis outline

The thesis is divided into eight main chapters, and to make the reading of it more straightforward, only the results of longer mathematical derivations are included in the relevant text, with the full working given in the appendix linked directly to the end of each chapter. In addition, chapter references are laid out at the end of each chapter as well as in a complete alphabetical order at the end of the thesis.

Following this introductory chapter, Chapter 2 concentrates on the fundamentals of the voltage-follower and its ideal and practical properties. A review of voltage-follower classifications is presented, together with the specifications to be met in this thesis. The chapter finishes with several popular application examples of the voltage-follower.

A detailed analysis of the transistor-models used throughout this research, is presented in Chapter 3. The process of developing a new circuit is supported by theoretical analysis. Unfortunately analytical device model parameters are not easily obtained directly from PSpice parameters. A key part of this chapter is extraction of these model parameters from PSpice device characteristics, at the particular operating conditions required for each design. It will be shown that a thorough analysis of these parameters is necessary for accurate design, based on 'hand-calculations' and that without them, in a number of cases, the simulation results do not match the theoretical analysis. In the same chapter, a review of biasing techniques is included together with an introduction to current-biasing circuitry that has been chosen for use because of its superior performance compared with other similar configurations.

Chapter 4 is a critical review of the conventional emitter-follower, including analysis of both DC and small-signal conditions. Comparatively, the treatment of the emitter-follower given in textbooks is not as extensive as that undertaken by the author, consequently the analysis presented in this chapter is quite thorough and thought to be original in some respects. Also, Chapter 4 sets the benchmarks for this research. All the proposed configurations are investigated, analysed and compared with the conventional circuit, in order to give the reader clear insight into the

performance of each proposed design, and its relative superiority over the conventional circuit.

In Chapter 5, a novel voltage-follower, using local feedback and single-valued current biasing is presented. The circuit idea is based on the on the original 'LH0002' type buffers developed in the 1970s by National Semiconductors **[1-39]**, more recently referred to as the 'Diamond' circuit **[1-40]** which is very commonly used as the input or output stage of a current feedback op-amp (CFOA) **[1-41]**, **[1-42]** and a current conveyer **[1-43]**. After the analysis and the simulation of the 'Diamond' circuit, according to the benchmarks set in the previous chapter, progressive modifications are presented, up to the proposed circuit, which is again analysed and simulated in a similar manner.

Chapter 6 presents two more novel voltage-follower designs, again with local feedback, but this time with double-valued current biasing. The analysis and simulation of both designs, similar to the previous circuit, showed that even better results, as far as the input and output impedance as well as distortion, can be achieved, compromising slightly the power dissipation of the circuit. Their performance parameters have been tabulated and compared at the final chapter with all the rest circuits, for the convenience of the reader.

A further novel voltage-follower design is developed in Chapter 7. This time, the circuit uses global feedback to achieve low signal distortion and even lower output impedance than the previous designs described. As described in the previous section, under certain conditions, the negative feedback can cause oscillations to a circuit

when it becomes positive. A good example of that is the circuit presented in this chapter. Consequently, in addition to the analysis of the new circuit, a compensation technique is presented which provides stable operation for the circuit. Finally, this chapter presents a comparative assessment of the most important parameters of the VFs investigated in this work. The assessment shows that the best voltage-follower is subject to trade-offs.

The last chapter, Chapter 8, is entitled Conclusions and future work. This contains an overview and reflection on the main body of work on the voltage-follower designs investigated. Finally, comments on implementing some of the designs in BiCMOS technology are included, and future development possibilities are described.

Some of the work reported in this thesis has been published and it is a recommendation/regulation of Oxford Brookes University that these papers are included in the thesis as they appeared in the publication. They can be found at the end of this thesis, after the list of references.

1.5 The original contribution of this work

The outcome of this work is four new designs which exhibit better performance parameters than similar in the market or recently presented circuits **[1-11 to 1-30]**. All four circuits, in addition to the overall good performance, present a strong point, and the decision for the most suitable design is subject to the application.

The first novel voltage-follower presented (Type A) is a circuit with very low offset voltage (64uV), wide bandwidth (2.7GHz), low power dissipation (34.6mW) and low signal distortion. The second and third novel circuits (Type B, VFB/1 and VFB/2) have been designed to provide fast operation, low distortion and wide voltage swing in addition to the good overall performance. In particular, the VFB/1 follower presents a very high slew-rate (4810V/us), low distortion (-70dB at 250MHz) and increased, compared to the Type A, voltage swing (±2V on a ±3.3V supply), while the VFB/2 combines the good performance of the VFB/1 with even higher voltage swing (±4.5V on a ±5V supply), low output impedance (2.4Ω) and small, in size, core (six devices). Finally, the fourth novel design (Type C) combines high input (15.1MΩ) and low output (0.036Ω) impedance, high Gain flatness (170MHz to within 0.1dB), low offset voltage (228uV) and good output swing.

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CHAPTER 2

The ideal and real voltage-follower

2.1 Introduction

This chapter considers some of the basic features of voltage-followers (VFs). Initially, a definition of the ideal VF together with its symbolic and system representation is given combined with graphic illustrations of its practical properties. In addition, practical terminal parameters required by a VF are listed followed by the performance parameters required to be met in this work. Finally, the classification system of VF designs adopted in this work is presented, followed by some typical VF applications.

2.2 The ideal and non-ideal voltage-follower and its properties

An ideal VF **[2-1 to 2-3]** may be defined as a module that senses, at its input, the instantaneous value of a signal voltage, without loading it in any way, and produces at its output a replica (i.e. exact copy) of that signal irrespective of the output loading or environmental conditions. Consequently, it should provide unity gain for any type of input signals, it should have an infinite input impedance and zero output impedance under any operating conditions as well as infinite slew rate. Nevertheless, it is not possible to produce an ideal voltage-follower. Figures 2.1 and 2.2, respectively show the symbolic and system representation of the ideal voltage-follower. Figure 2.3 shows graphically some of the properties of a non-ideal VF.

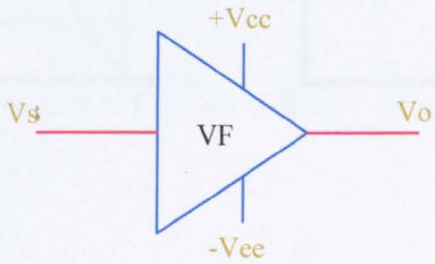


Fig. 2.1 Symbolic representation

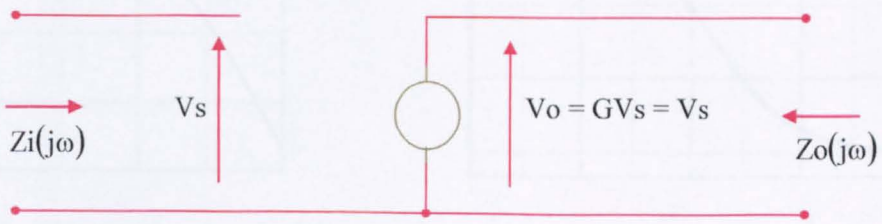
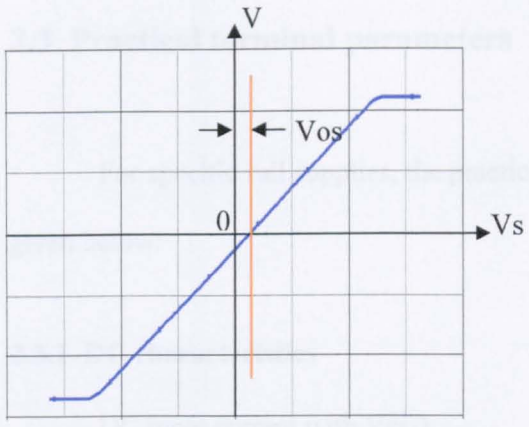
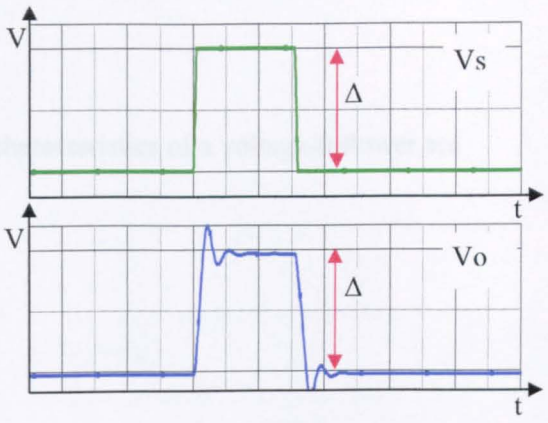


Fig. 2.2 System representation

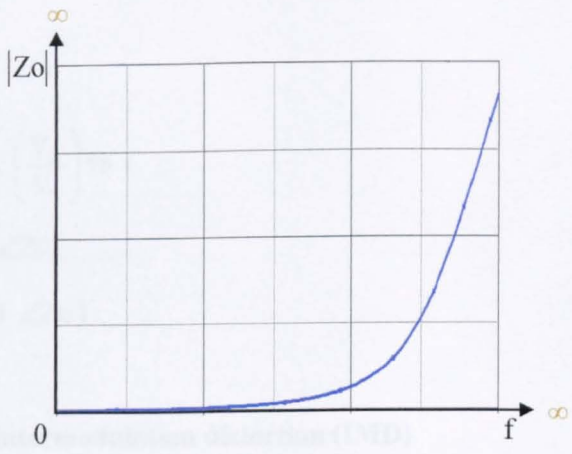


a) DC transfer characteristic

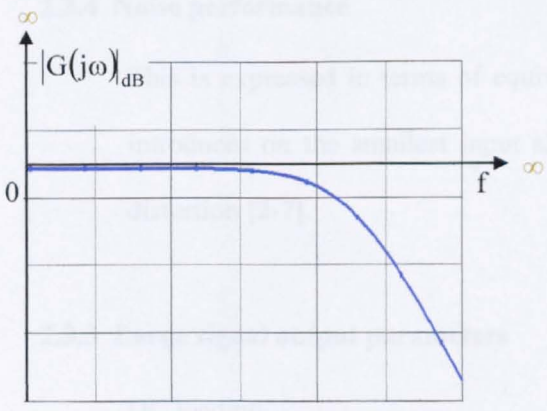


b) Large signal step response

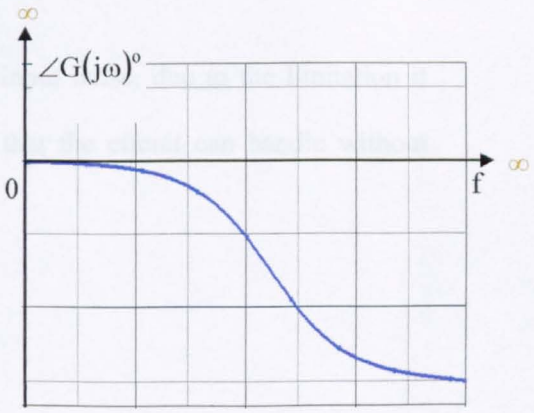
c) Input impedance



d) Output impedance



e) Gain magnitude in dB



f) Phase

Fig. 2.3 Graphical illustration of some non-ideal VF properties

2.3 Practical terminal parameters

For specific rail supplies, the practical characteristics of a voltage-follower are given below:

2.3.1 DC characteristics

DC input current with Vs=0

Quiescent power dissipation P_D with Vs=0

2.3.2 Loading characteristics

Small-signal voltage gain characteristic, $\left(\frac{V_O}{V_S}\right)$ vs f

Incremental input impedance ($|Zi|$ and $\angle Zi$)

Incremental output impedance ($|Zo|$ and $\angle Zo$)

2.3.3 Total harmonic distortion (THD) and intermodulation distortion (IMD)

2.3.4 Noise performance

This is expressed in terms of equivalent input noise, due to the limitation it introduces on the smallest input signals that the circuit can handle without distortion **[2-7]**.

2.3.5 Large signal output parameters

DC loading

Large signal voltage step response

2.4 Specifications to be met in this thesis

Important parameters (specifications) adopted in this work is given in Table 2.1

Parameters	Values
$\|V_{cc}\|$, $\|V_{ee}\|$	$\leq 5V$
P_D	$\leq 35mW$
$\|Zi\|$	$> 5M\Omega$
$\|Zo\|$	$< 10\Omega$
$V_{S(min)}$	$2V_{P-P}$
$\|G\|$	$(1-\varepsilon)$, where $\varepsilon < 0.1$ up to 250MHz
THD	$\leq -80dB$ at 5MHz
THD	$\leq -60dB$ at 250MHz
IMD	$\leq -55dB$
Temperature range	-20°C up to 100°C

Table 2.1 Specifications to be met in this work

2.5 A classification of voltage-follower designs

2.5.1 Type A, using local feedback and single-valued current bias

A single stage feedback rather than a complete multistage configuration is used. In addition, only one value of current bias is used. Two elementary examples of this, discussed in detail later, are shown in Figure 2.4.

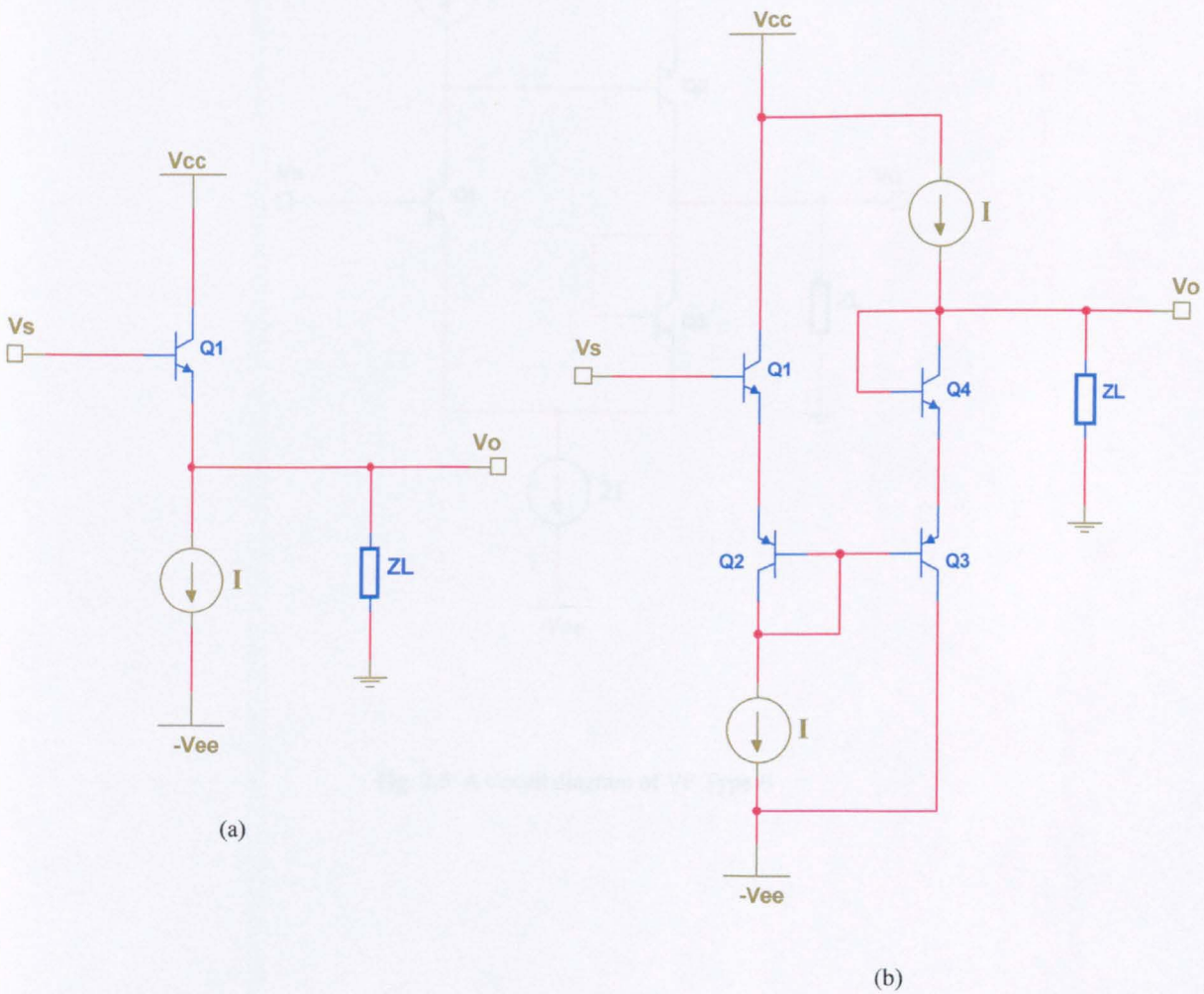


Fig. 2.4 Elementary examples of voltage-followers Type A:

(a) conventional emitter-follower, and

(b) two-stage emitter-follower

2.5.2 Type B, using local feedback and double-valued current bias

An example of Type B is shown in Figure 2.5.

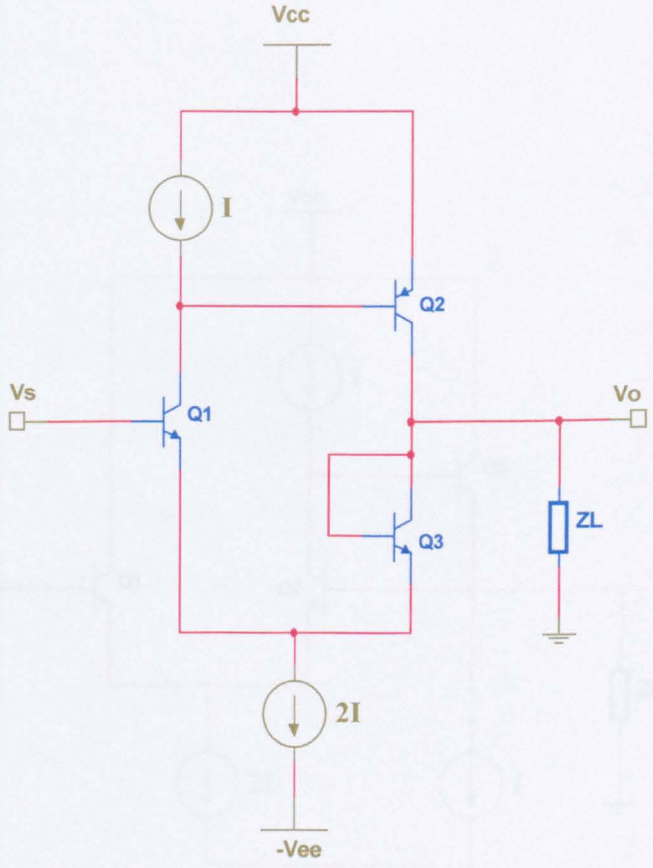


Fig. 2.5 A circuit diagram of VF Type B

2.5.3 Type C, using global feedback

An example of Type C is shown in Figure 2.6. This design happens to use two values of current bias but that is not a necessary feature of this classification.

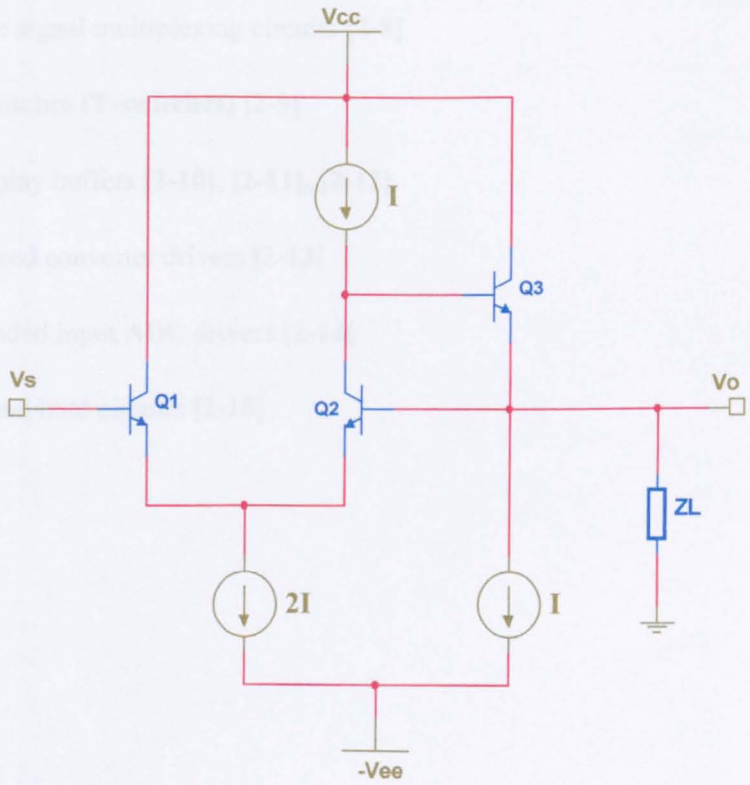


Fig. 2.6 A circuit diagram of VF Type C

2.6 Applications

- Instrumentation amplifiers with high input and low output-impedance **[2-8]**
- Active filters **[2-8]**
- Boot-strapped linear sweep **[2-8]**
- Peak detectors **[2-8]**
- Analogue signal multiplexing circuits **[2-8]**
- Video switches **(T-switches) [2-9]**
- LCD display buffers **[2-10], [2-11], [2-12]**
- Multiplexed converter drivers **[2-13]**
- Single-ended input ADC drivers **[2-14]**
- Sample and hold circuits **[2-15]**

2.7 Summary of Chapter 2

This chapter considered an introduction to the basic voltage-follower, presenting pictorially some of its basic performance parameters.. Practical parameters that will be used to evaluate both the conventional and the proposed configurations have been presented together with a list of the terminal characteristics required by a voltage-follower that meets the specifications required for the circuits in this thesis. Finally, a wide range of typical applications using voltage-followers, has been presented with examples from recent publications by leading semiconductor manufacturers.

References for Chapter 2

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CHAPTER 3

Transistor model characteristics and current biasing schemes

3.1 Introduction

This chapter is divided into two main parts. The first part presents a detailed analysis of the transistor-models used throughout this research, pointing out some of the parameters that are either not explicitly listed in SPICE transistor parameter set or whose values are not appropriate to the operating conditions envisaged. Presenting, at first, the methodology of measurement and, secondly, the results obtained it will be shown that a detailed investigation of these parameters is necessary for accurate design based on hand-calculations and that without them simulated results do not, in some cases, agree with the theoretical analysis. The second part of this chapter presents the analysis of two current-biasing configurations, which have been used to provide the DC supply to conventional and proposed designs. These bias schemes use current-mirrors, so the analysis is concentrated mainly on current-transfer from the input to the output, as well as the output impedance at low frequencies. This section finishes with a reference to several well-established current mirrors and their performances compared with the ones chosen.

It is worthy of mention that the operating current of the proposed designs will be either 1mA or 0.7mA, as is used in subsequent chapters. For that reason, most of the simulations, including current-mirrors and transistor-model characteristics, have been accomplished using both these currents. Furthermore, a wide temperature range is covered during simulations.

3.2 Device characterisation

The main objective of the following paragraphs is to provide an insight to the performance of the transistor models used throughout this research. It will be shown that, for both NPN and PNP devices, some of the transistor parameters supplied by the manufacturer were not appropriate, thus resulting in a considerable difference between hand-calculation and simulated results, when the SPICE values were used. The measurement of transistor parameters is divided into two parts, DC and AC.

3.2.1 DC parameters

3.2.1.1 DC current gain measurement

It is well-known that the transistor DC current gain, β_F, depends on transistor operating conditions **[3-1]**, such as the collector current, I_C, the collector-base voltage, V_{CB}, and the operating temperature, T. The variation of β_F with T has been attributed to the extremely high doping density level in the emitter region. This variation, with I_C and T is indicated in Figure 3.1.

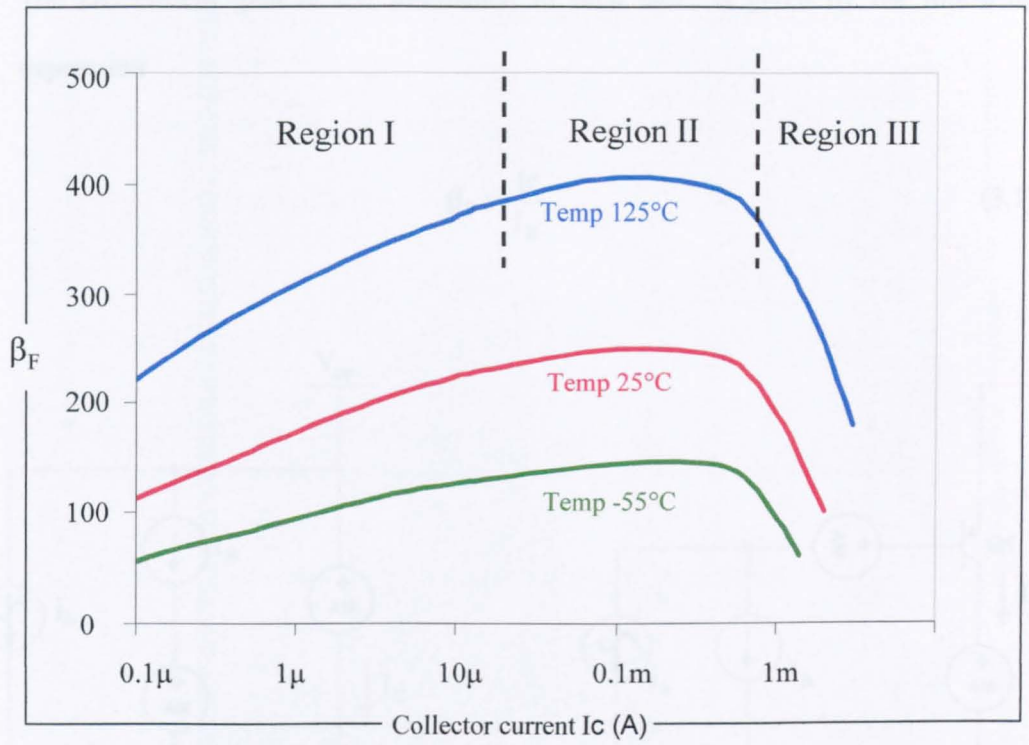

Fig. 3.1 Variation of β_F with temperature and collector current **[3-1]**

In order to proceed with the detailed analysis of the conventional and novel configurations, throughout this thesis, the exact values of β_F should be specified, for all values of T and I_C, for DC and AC operation. The simple circuits adopted for testing β_F of the NPN and PNP transistors are shown in Figures 3.2 and 3.3, respectively. In those Figures, ignoring initially the AC current sources, a DC current is applied to the base of the transistor, so that the collector current is 0.1mA, 0.2mA, 0.3mA etc. The two current probes, one in the base and the other in the collector of the transistor indicate the value of the current in each branch. The testing covers a temperature range from -20°C up to 100°C, and collector currents from 100µA up to 1mA.

The DC current gain of the transistors, in each case, is given by the following expression

$$\beta_F = \frac{Ic}{I_B} \tag{3.1}$$

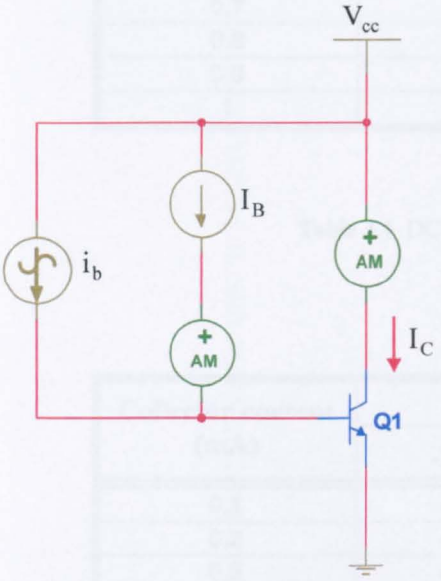

Fig. 3.2 Current gain testing circuit for NPN devices

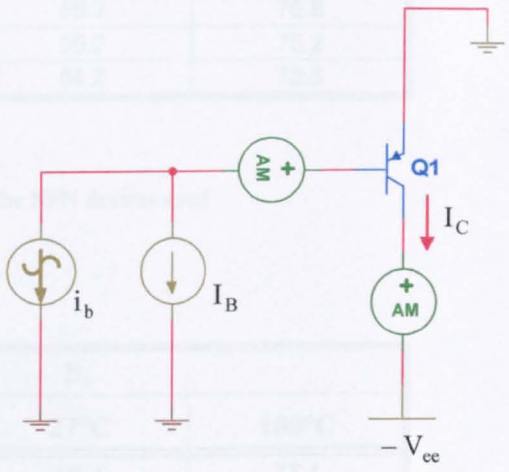

Fig. 3.3 Current gain testing circuit for PNP devices

Table 3.1, shows the DC current gain of the NPN transistor for the whole current and temperature range and similarly, Table 3.2 shows the DC current gain for the PNP device. As mentioned earlier, with increase in operating temperature, the current gain of the device increases due to the increase in the emitter injection efficiency, γ . It is apparent that a low operating temperature offers more constant current gain, for variable collector current, although the current gain is not as great as at higher temperatures.

Collector current (mA)	β_F		
	-20°C	27°C	100°C
0.1	49.3	64.9	92.5
0.2	48.4	63.4	89.6
0.3	47.5	62.0	87.1
0.4	46.8	60.8	84.7
0.5	46.0	59.5	82.6
0.6	45.3	58.4	80.6
0.7	44.6	57.3	78.7
0.8	43.9	56.2	76.8
0.9	43.2	55.2	75.2
1	42.6	54.2	73.5

Table 3.1 DC current gain of the NPN devices used

Collector current (mA)	β_F		
	-20°C	27°C	100°C
0.1	44.4	56.4	77.1
0.2	42.8	53.9	73
0.3	41.4	51.9	69.6
0.4	40.1	50	66.6
0.5	38.9	48.3	64
0.6	37.8	46.7	61.5
0.7	36.6	45.2	59.2
0.8	35.7	43.8	57.1
0.9	34.7	42.4	55.1
1	33.8	41.2	53.3

Table 3.2 DC current gain of the PNP devices used

A similar conclusion can be made regarding the current gain of the PNP devices. In addition, it can be seen that the current gain of the PNP devices is lower, although both devices are supposed to be complementary. This is an important point, considered again later.

The variation of β_F with the collector current obtained above, shows that the transistor operates somewhere between the Region II and the beginning of Region III. Ideally, of course, β_F should be constant. Apart from that, it was proved that the DC current gain of the transistors used was much less than the figure given by the manufacturer $\beta_{NPN} = 74$ and $\beta_{PNP} = 84$ at room temperature. The values obtained are used later, in the analysis of the basic emitter-follower and other circuits.

3.2.1.2 Early-Voltage measurement

The Early-Voltage (V_A) of a transistor is an important parameter in analogue circuit analysis. V_A determined is used later in this chapter as well as in the following chapters for the calculation of circuit incremental output resistance. V_A measurement has been carried out using the circuit shown in Figure 3.4(a) for NPN devices, and Figure 3.4(b) for PNP devices, over a range of temperatures.

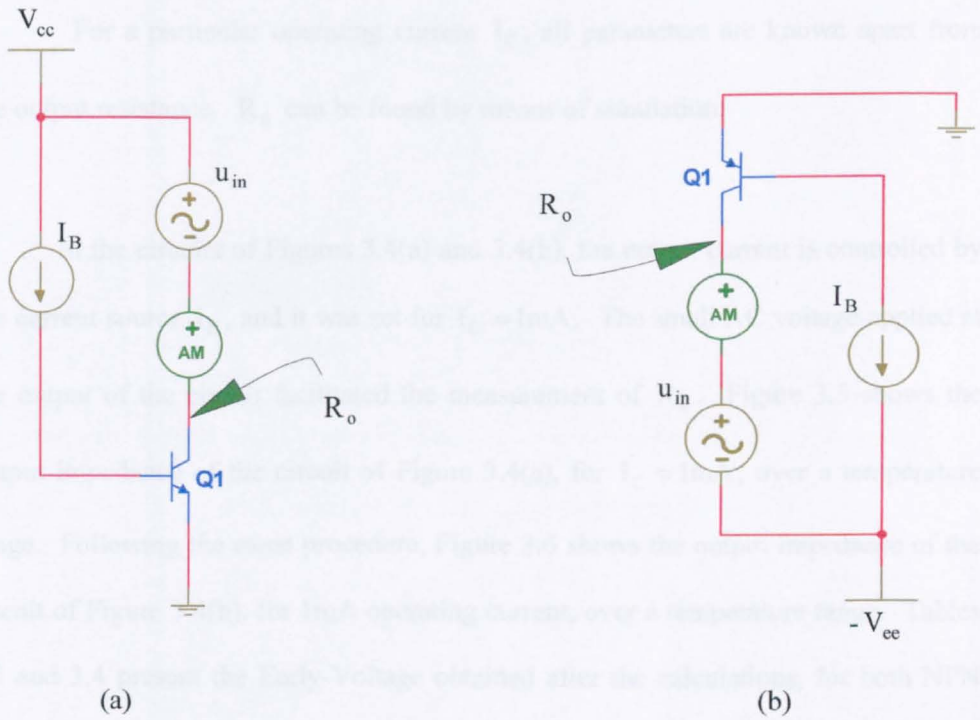

Fig. 3.4 V_A measurement set up;
(a) NPN, and (b) PNP

V_A is given by:

$$\frac{I_C}{V_A} = \frac{1}{R_o} - \frac{(\beta+1)}{r_\mu} \tag{3.2}$$

where, r_μ, is the collector-base internal resistance, which measured **[3-2]** 32.5MΩ for the NPN and worked out at 6MΩ for the PNP devices used, β is the transistor current gain and R_o the output resistance of the transistor. Full details of the analysis are given in Appendix 3.1.

For a particular operating current I_C, all parameters are known apart from the output resistance. R_o can be found by means of simulation.

In the circuits of Figures 3.4(a) and 3.4(b), the output current is controlled by the current source I_B, and it was set for $I_C = 1\text{mA}$. The small AC voltage applied at the output of the circuit facilitated the measurement of R_o. Figure 3.5 shows the output impedance of the circuit of Figure 3.4(a), for $I_C = 1\text{mA}$, over a temperature range. Following the same procedure, Figure 3.6 shows the output impedance of the circuit of Figure 3.4(b), for 1mA operating current, over a temperature range. Tables 3.3 and 3.4 present the Early-Voltage obtained after the calculations, for both NPN and PNP devices.

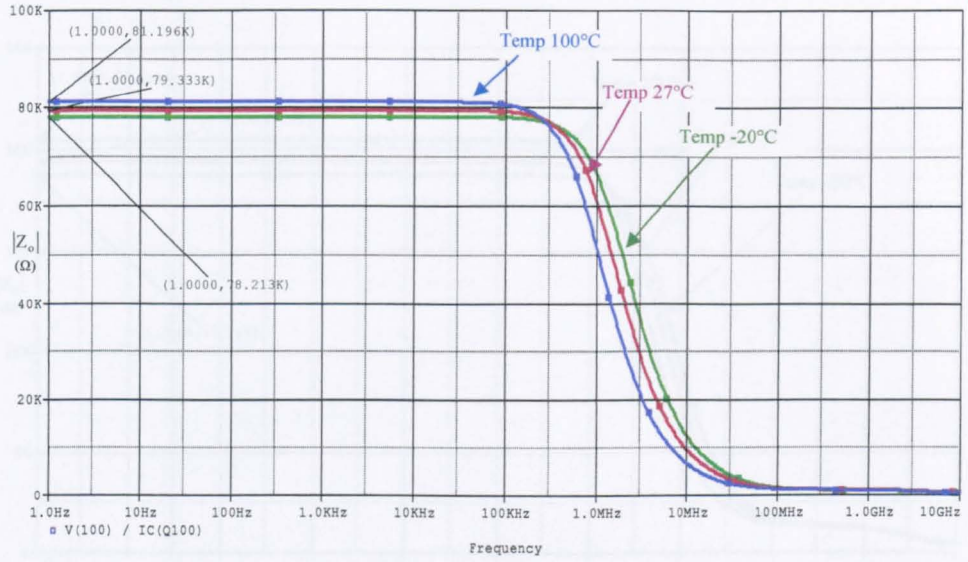

Fig. 3.5 Output impedance of the NPN transistor over the temperature range for $I_C = 1\text{mA}$, $V_{CC} = 5\text{V}$

Output current I_o (mA)	1		
Operating Temperature (°C)	-20	27	100
Early Voltage (V)	86.1	89.61	97.57

Table 3.3 Measured V_A (i.e. V_{AN}) of the NPN devices used

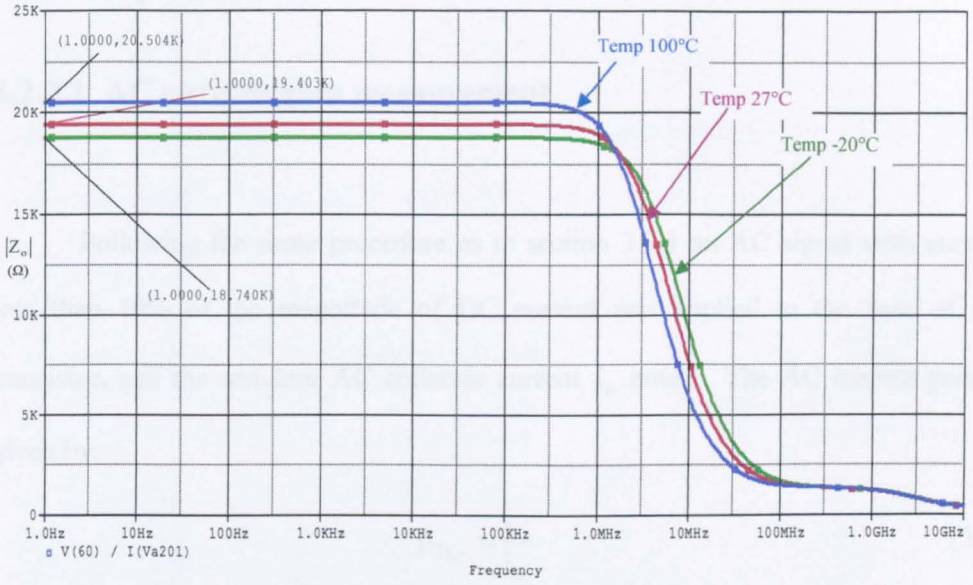

Fig. 3.6 Output impedance of the PNP transistor over the temperature range for $I_C = 1mA$, $V_{CC} = 5V$

Output current I_o (mA)	1		
Operating Temperature (°C)	-20	27	100
Early Voltage (V)	21.2	22.8	26.1

Table 3.4 Measured V_A (i.e. V_{AP}) of the PNP devices used

3.2.2 AC parameters

3.2.2.1 AC current gain measurement

Following the same procedure as in section 3.2.1 an AC signal with current less than 10% of the magnitude of DC current was applied to the base of the transistor, and the resultant AC collector current i_c noted. The AC current gain is given by:

$$\beta_{F_{AC}} = \frac{i_c}{i_b} \tag{3.3}$$

Tables 3.5 and 3.6 illustrate the measured AC current gain for both NPN and PNP devices, respectively, as well as their dependence on I_C and T.

Collector current (mA)	$\beta_{F(AC)}$		
	-20°C	27°C	100°C
0.1	48.3	63.3	89.4
0.2	46.7	60.7	84.5
0.3	45.3	58.3	80.2
0.4	43.9	56.2	76.5
0.5	42.6	54.2	73.1
0.6	41.4	52.3	70
0.7	40.3	50.6	67.2
0.8	39.2	49	64.6
0.9	38.1	47.5	62.2
1	37.1	46	60

Table 3.5 AC current-gain of the NPN devices used

The current gain increases with T but is then less constant with variation in I_C. Another interesting result is that the AC current gain only tends to be almost the same as the DC one for low collector currents. It can be seen that for currents above 0.5mA the difference between the AC and DC values of β_F is significant.

Collector current (mA)	$\beta_{F(AC)}$		
	-20°C	**27°C**	**100°C**
0.1	54.3	68.8	94.2
0.2	51.1	64.8	88.9
0.3	48.4	61.5	84.3
0.4	46	58.4	80.3
0.5	43.8	55.7	76.6
0.6	41.8	53.1	73.2
0.7	39.9	50.8	70.1
0.8	38.2	48.7	67.3
0.9	36.6	46.7	64.6
1	35.1	44.8	62

Table 3.6 AC current gains of the PNP devices used

The results show a grater variation of the current-gain with the collector current (compared to the NPN devices) and a noticeably lower current amplification, especially for collector currents above 0.5mA.

3.2.2.2 Frequency response

For high frequency circuit operation, high f_T devices are required. To test the frequency response of the devices used, the following technique was used. In the circuit of Figure 3.7, a DC current of 1mA is applied to the emitter of the device under test. In parallel with the DC current source is an AC current source, with a signal amplitude less than 10% of the magnitude of the DC current. The ratio, α, of AC collector current to AC emitter current, over the frequency range, gives the common-base frequency response. The f_T of the transistor is almost equal to the -3dB frequency **[3-3]**. Figure 3.8 shows the frequency response for the NPN device used.

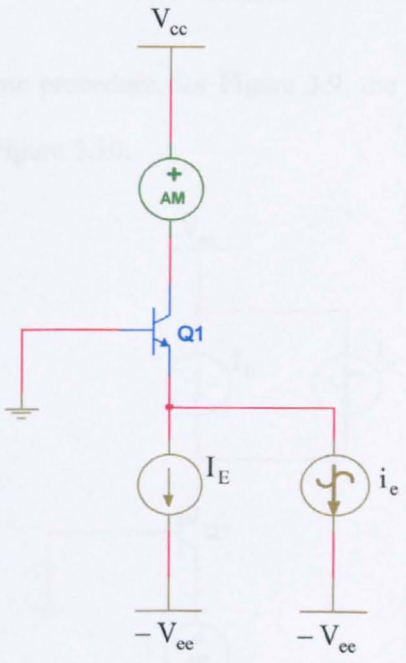

Fig. 3.7 Circuit for the frequency response testing of NPN devices

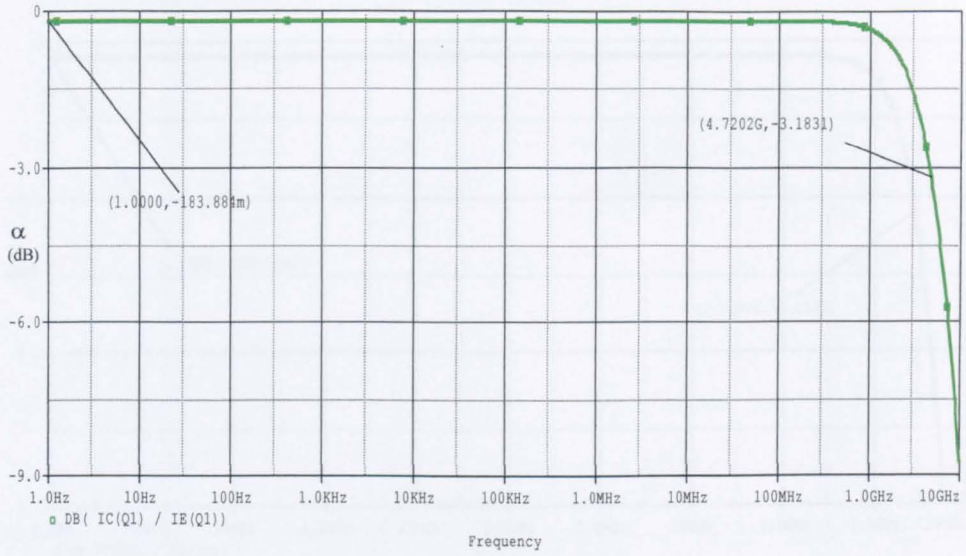

Fig. 3.8 Frequency response of the NPN transistors used ($I_C = 1mA$; $V_{CB} = 5V$)

For NPN devices,

$$f_T \approx 4.7GHz$$

Following the same procedure, for Figure 3.9, the frequency response of the PNP device is shown in Figure 3.10.

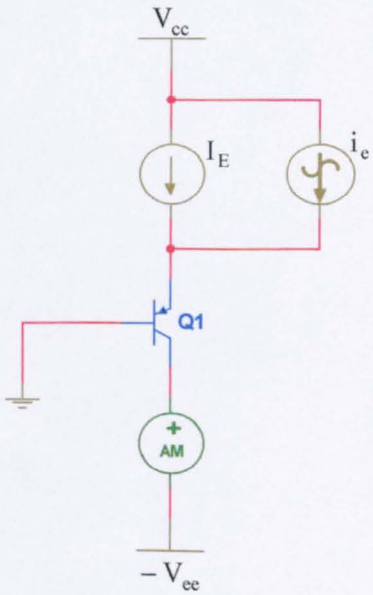

Fig. 3.9 Circuit for frequency-response testing of PNP devices

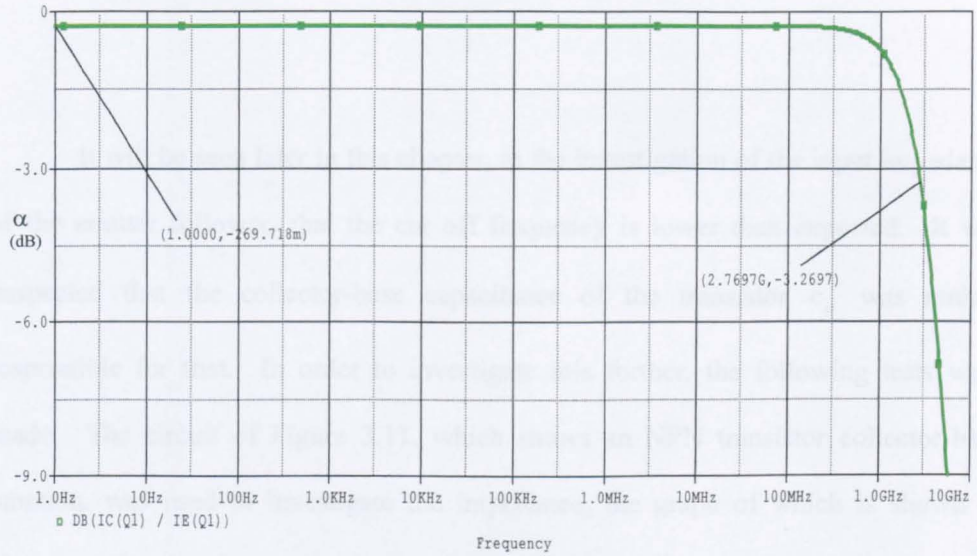

Fig. 3.10 Frequency response of the PNP transistor used ($I_C = 1mA$; $V_{CB} = 5V$)

Note that for PNP,

$$f_T \approx 2.7GHz$$

3.2.2.3 The collector-base capacitance c_μ

It will be seen later in this chapter, in the investigation of the input impedance of the emitter follower, that the cut off frequency is lower than expected. It was suspected that the collector-base capacitance of the transistor c_μ was mainly responsible for that. In order to investigate this further, the following tests were made. The circuit of Figure 3.11, which shows an NPN transistor collector-base junction, was used to investigate the impedance, the graph of which is shown in Figure 3.13 (green line). The impedance at $f = 1\text{MHz}$ was 4.8589MΩ. The value of c_μ is calculated as follows,

$$c_\mu = \frac{1}{2\pi |Z| f} = \frac{1}{2\pi \cdot 4.8589 \cdot 10^6 \cdot 1 \cdot 10^6} = 32.75\text{fF}$$

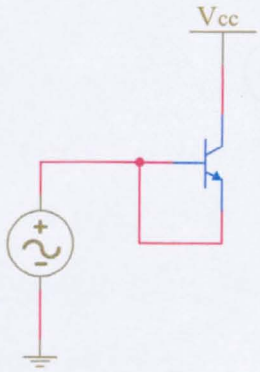

Fig. 3.11 Circuit used to measure the c_μ for NPN devise

In order to check that the measurement of c_μ is correct, in parallel with the base-collector junction another, identical one, was added. Theoretically this should double the c_μ and half the impedance. In a similar manner, a third junction was added in parallel with the other two, with the expectation of reducing the impedance to one third of the first value.

The test has been carried out using the circuits of Figure 3.12.

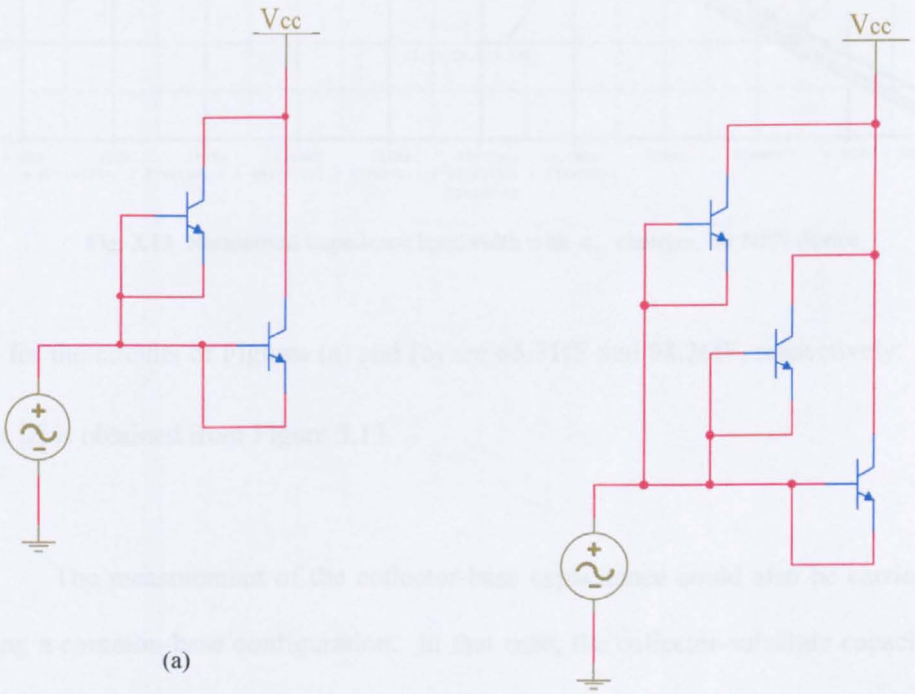

Fig. 3.12 Circuits used to measure the effect of extra c_μ on the impedance

(a) Circuit with an extra added c_μ, and (b) Circuit with two extra added c_μ s

The responses obtained, together with the original one, are illustrated in Figure 3.13. Note that here, and elsewhere, the dB reference level for $|Z_o|$ is 1Ω.

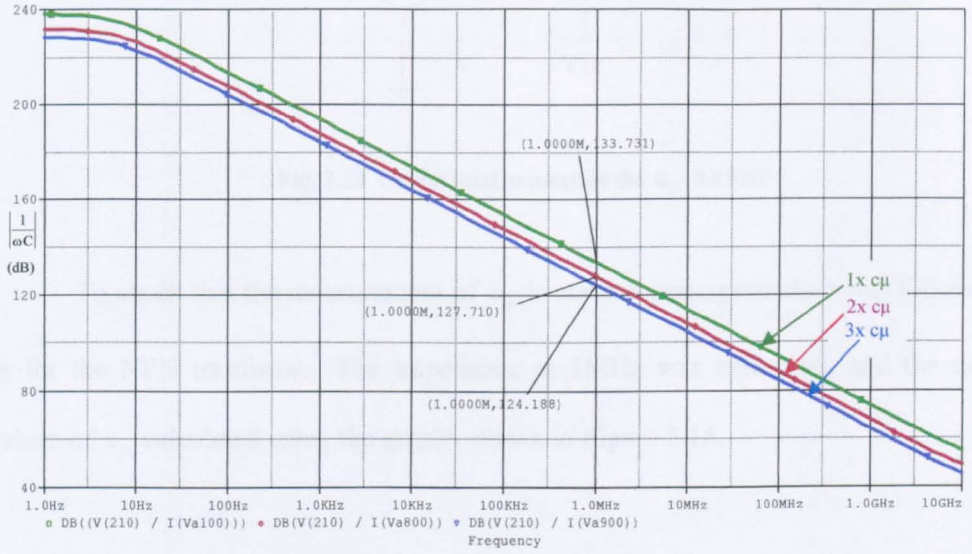

Fig. 3.13 Normalised impedance bandwidth with c_μ changes, for NPN device

c_μ for the circuits of Figures (a) and (b) are 65.51fF and 98.26fF, respectively. Note that $|Z|$ is obtained from Figure 3.13.

The measurement of the collector-base capacitance could also be carried out using a common-base configuration. In that case, the collector-substrate capacitance would be in parallel with c_μ. For evaluation purposes, measuring c_μ using the common-base stage, obtained identical results. Following the same procedure, the collector-base capacitance of the PNP device used was calculated, using Figure 3.14. The impedance at $f = 1\text{MHz}$ was 4.0638MΩ. Consequently, c_μ is equal to 39.16fF.

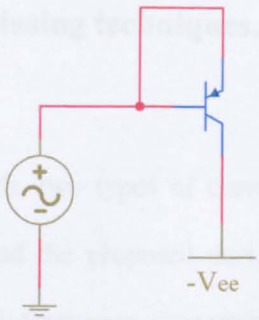

Fig. 3.14 Circuit used to measure the c_μ for PNP

To check that the measurement of c_μ is correct, same procedure was followed as for the NPN transistor. The impedance at 1MHz was measured, and the new values of c_μ calculated using the graphs shown in Figure 3.15.

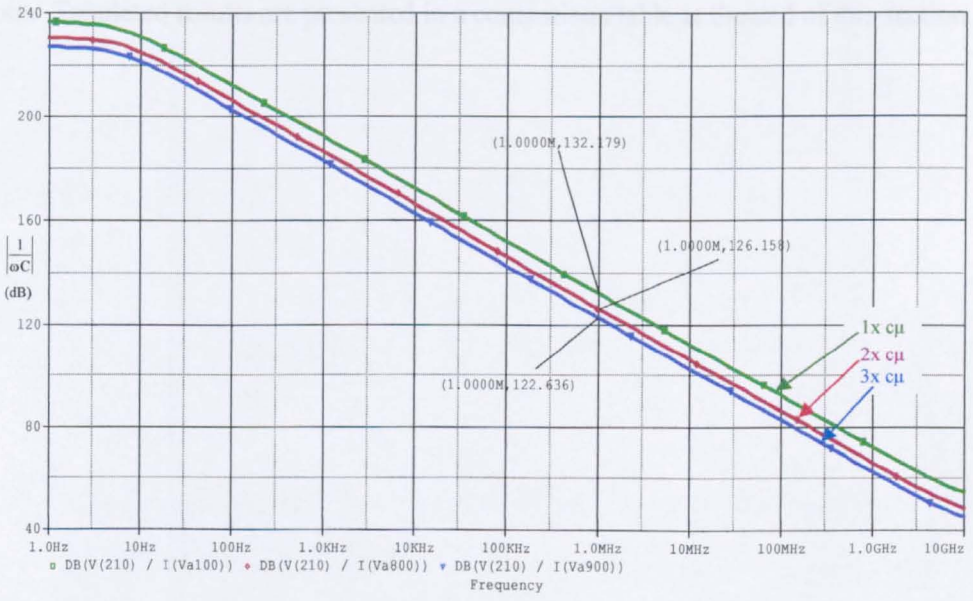

Fig. 3.15 Impedance bandwidth with c_μ changes, for PNP device

The c_μ is equal to 78.32fF and 117.49fF for two and three collector-base junctions in parallel, respectively.

3.3 A review of current biasing techniques, using current-mirrors

Throughout this research, two types of current-mirrors are used to provide biasing for the conventional and the proposed designs. The analysis that follows concentrates mainly on the low-frequency characteristics of the current-mirrors, as they are not used, directly, in the signal paths.

The characteristics that will define which current-mirror is the most desirable are, primarily, the output impedance, which should be as large as possible as well as the current-mirror's current transfer ratio, λ. Apart from the analysis of the two current mirrors, a detailed simulation of several other current mirrors has been carried out. Tabulated results are presented in a comparison table at the end of this section.

3.3.1 Common-base biasing [3-4]

The common-base stage is a well-established configuration that is described in text-books. It is discussed here because of its high output impedance when used in the cascode configuration, as it will be shown later. The common-base stage is illustrated in Figure 3.16. It has been shown in **[3-2]**, that when the operating current is supplied from an ideal current sink (for the NPN model), the output resistance of the stage is:

$$R_o = (\beta + 1) r_o // r_\mu \tag{3.4}$$

where $r_o = \frac{V_{AN}}{I_C}$ and $r_\mu = r_o \frac{\Delta I_C}{\Delta I_B}$

Substituting the values from section 3.2 for 1mA current in the collector of the transistor at 27°C,

$$R_o = (46 + 1)\frac{89.61V}{1mA} // 32.5M\Omega = 3.728M\Omega.$$

Similarly, if the collector current is 0.7mA, supplied by an ideal current sink, the output impedance at 27°C will be,

$$R_o = (50.6 + 1)\frac{89.61V}{0.7mA} // 32.5M\Omega = 5.490M\Omega.$$

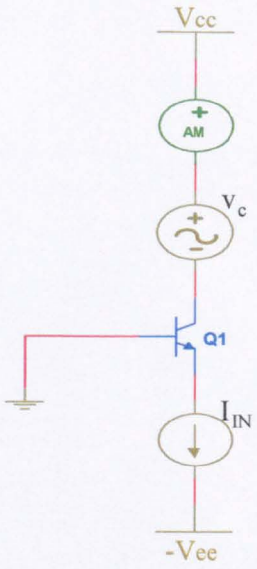

Fig. 3.16 Common-base stage with ideal current sink

Simulation results for $|Z_o|$ for three different operating temperatures and I_C of 1mA for Figure 3.16 is shown in Figure 3.17. The output impedance of 3.82MΩ is observed, at 27°C, which is close to the predicted value of 3.728MΩ, see Figure 3.17. Similarly, for $I_C = 0.7\text{mA}$ $|Z_o|$ is 5.996MΩ which is comparable to the predicted value of 5.490MΩ, see Figure 3.18.

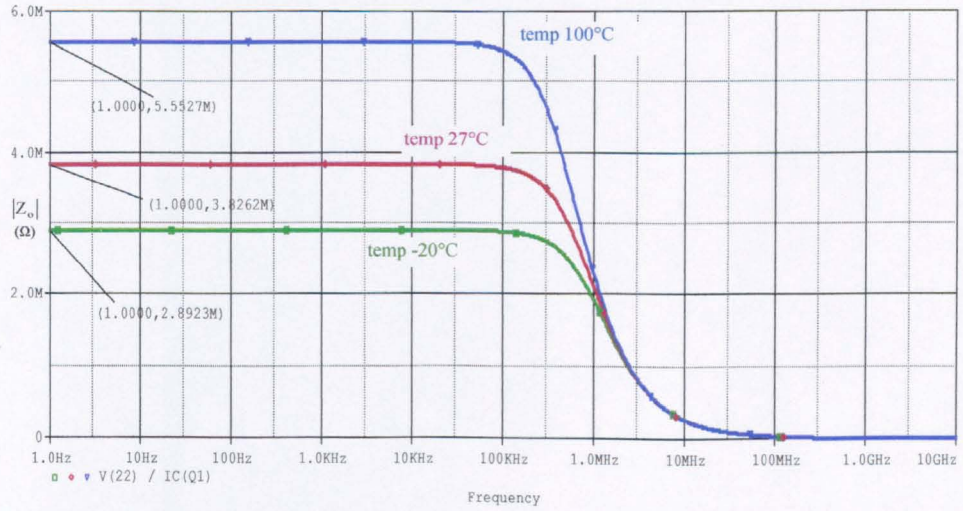

Fig. 3.17 Output impedance of circuit of Figure 3.16, for $I_C = 1\text{mA}$

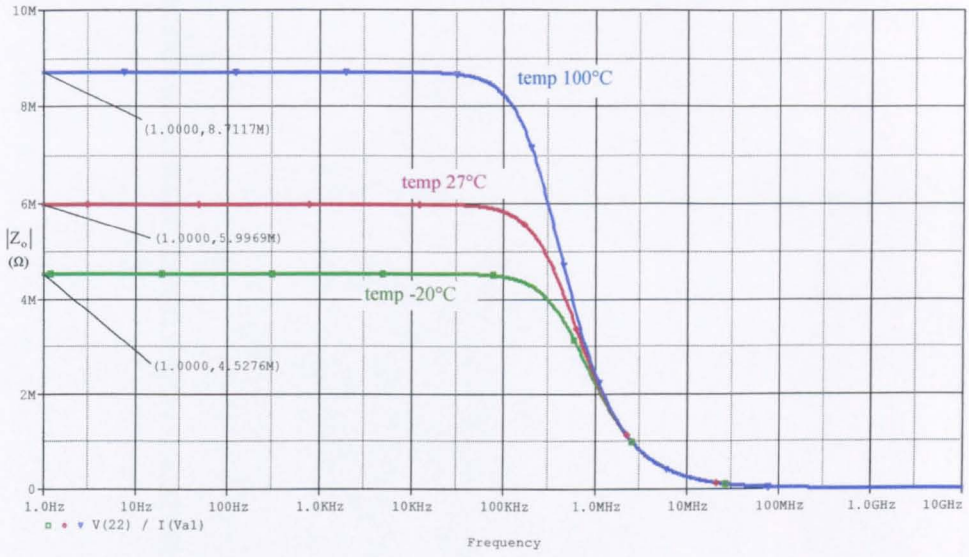

Fig. 3.18 Output impedance of circuit of Figure 3.16, for $I_C = 0.7\text{mA}$

3.3.2 Buffered current-mirror with cascoded output, biasing [3-5], [3-6]

This is a simple current-mirror with buffered input and cascoded output, as shown is Figure 3.19.

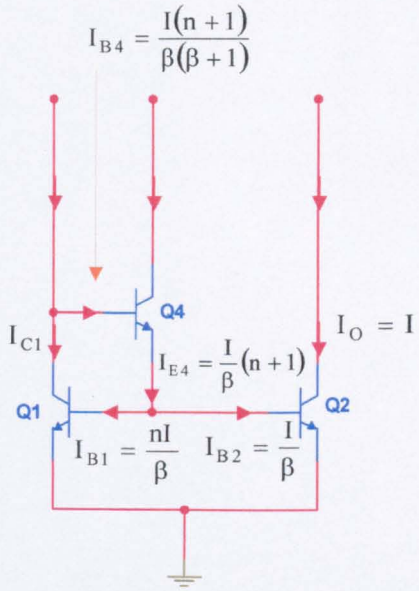

Fig. 3.19 Buffered simple current-mirror with cascoded output

Analysing initially the buffered current mirror, (see Appendix A3.2), the current ratio, λ, defines as,

$$\lambda = \frac{I_O}{I_{IN}} = \frac{1}{1+\frac{2}{\beta^2}} \pm \frac{V_{OS}}{V_T} \tag{3.5}$$

where I_O is the output current, I_{IN} is the input current, V_T is the thermal voltage and V_{OS} is the offset voltage, which relates to the matching of Q_1 and Q_2.

Consequently, cascoding the output with transistor Q_3, is,

$$\lambda = \frac{I_O}{I_{IN}} = \frac{\beta}{(\beta+1)} \frac{1}{1+\frac{2}{\beta^2}} \pm \frac{V_{OS}}{V_T} \tag{3.6}$$

In practice, the term which dominates, making λ slightly greater or smaller than unity, depends on the matching of the two transistors, Q_1 and Q_2. Simulating the circuit, for $I_C = 1\text{mA}$ and $I_C = 0.7\text{mA}$ produced the current transfer ratios shown in Figure 3.20. λ, was almost the same for both operating currents, with that of 0.7mA closer to unity.

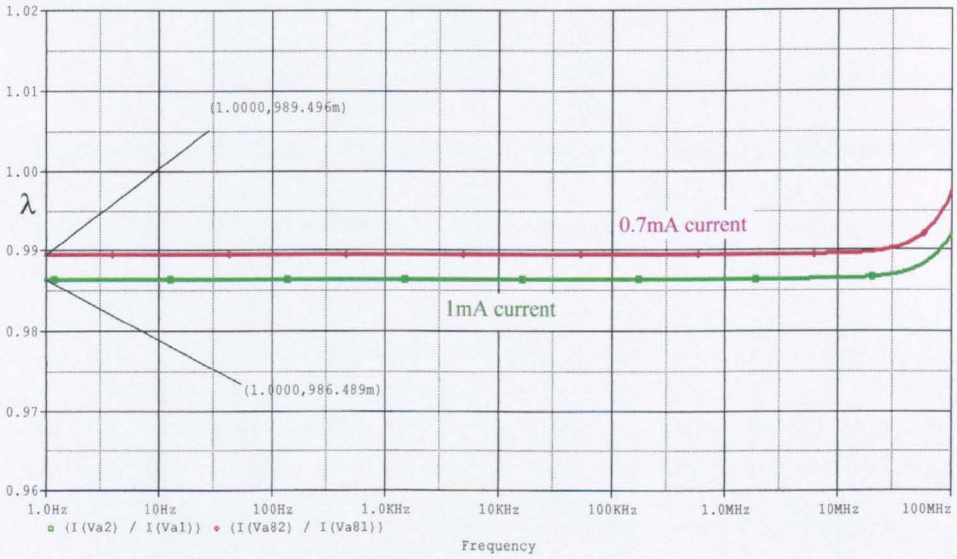

Fig. 3.20 Current transfer ratio, λ, of the buffered NPN mirror with cascoded output

Since $V_{OS} = 0$ in PSICE simulation (identical devices assumed), the reason for $\lambda \neq 1$ is shown below,

for $I_C = 1mA$,

$$\lambda \approx \frac{\beta}{(\beta+1)} = \frac{54.2}{54.2+1} = 0.981$$

and for $I_C = 0.7mA$,

$$\lambda \approx \frac{\beta}{(\beta+1)} = \frac{57.3}{57.3+1} = 0.982$$

where β is the DC current gain of the devises used, investigated in section 3.3.1.1.

Changing the operating current, results in a change in the DC current gain of the transistors, as shown earlier in this Chapter. Consequently, the current transfer ratio for $I_C = 0.7mA$ is closer to unity, since β is greater than at $I_C = 1mA$. In addition, according to (3.6), λ depends on the operating temperature, too, because of the temperature dependence of β. Figure 3.21 shows λ, over the temperature range -20°C to +100°C, with $I_C = 1mA$.

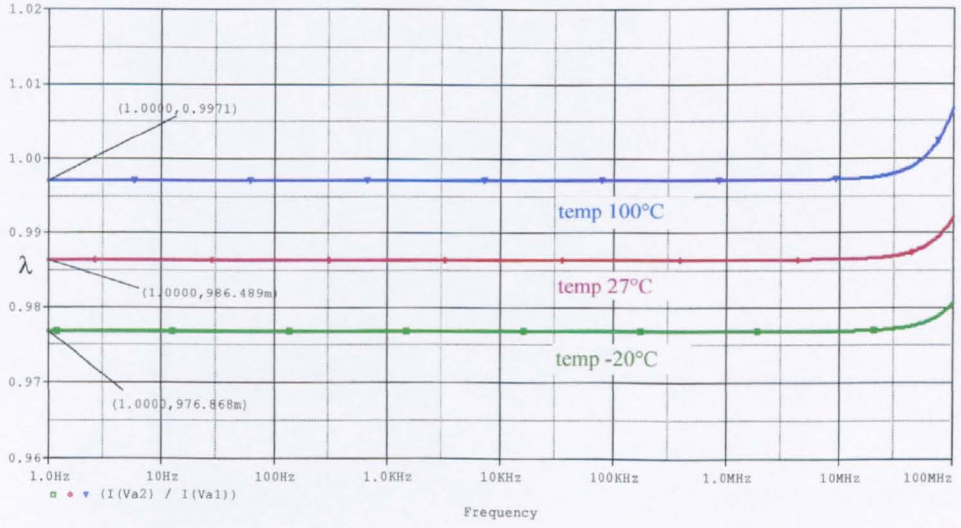

Fig. 3.21 Current transfer ratio, λ, of the buffered NPN mirror with cascoded output over the temperature range

The output resistance of the buffered current-mirror is

$$R_o = r_{ce} = \frac{V_A}{I_C} \tag{3.7}$$

and substituting with the values obtained in the previous paragraphs, for $I_C = 1\text{mA}$ and $I_C = 0.7\text{mA}$, at 27°C

$$R_o = \frac{89.61}{1\text{mA}} \approx 89.6\text{K}\Omega \quad \text{and} \quad R_o = \frac{89.61}{0.7\text{mA}} \approx 128\text{K}\Omega$$

The simulation (Figure 3.22) of the buffered current-mirror gave an output resistance of 83.8KΩ, for $I_C = 1\text{mA}$ and 117.2KΩ, $I_C = 0.7\text{mA}$, results within 10% of hand-calculations.

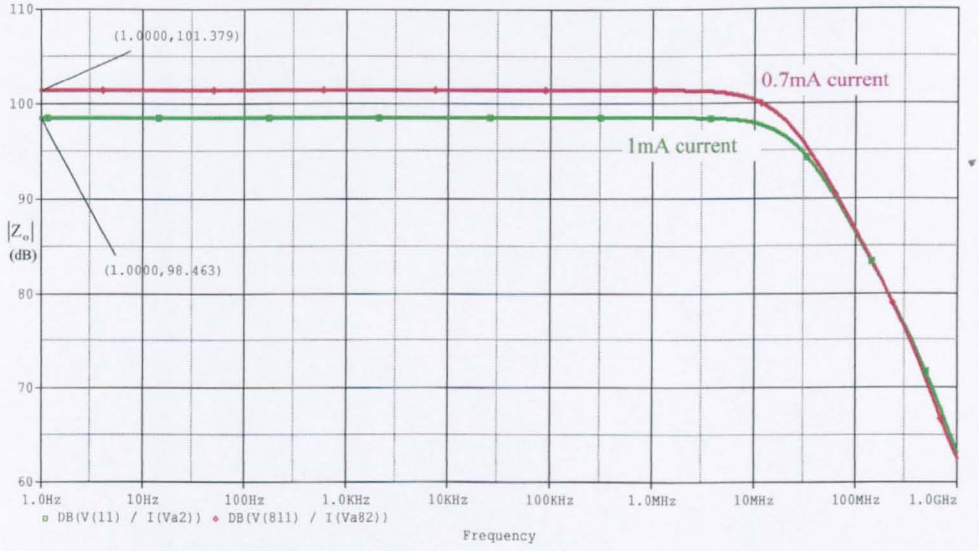

Fig. 3.22 Output impedance of the buffered NPN current mirror

Cascoding the output with transistor Q_3, the output resistance increases at the expense of a current transfer ratio which is reduced by a factor of $\frac{\beta}{\beta+1}$.

The new output resistance is,

$$R_o = (1+\beta)r_o \,//\, r_\mu \tag{3.8}$$

For $I_C = 1\text{mA}$,

$$R_o = (1+\beta)r_o \,//\, r_\mu = (1+\beta)\frac{V_{AN}}{I_C} \,//\, r_\mu = (1+46)\frac{89.61}{1\text{mA}} \,//\, 32.5\text{M} \approx 3.73\text{M}\Omega$$

and for $I_C = 0.7\text{mA}$,

$$R_o = (1+\beta)r_o \,//\, r_\mu = (1+\beta)\frac{V_{AN}}{I_C} \,//\, r_\mu = (1+50.6)\frac{89.61}{0.7\text{mA}} \,//\, 32.5\text{M} \approx 5.49\text{M}\Omega$$

assuming that the collector-base resistance r_μ is 32.5MΩ for both $I_C = 1\text{mA}$ and $I_C = 0.7\text{mA}$.

The simulation of the cascoded output buffered current mirror gave an output resistance of 3.44MΩ, at $I_C = 1\text{mA}$ and 5.4MΩ at $I_C = 0.7\text{mA}$, indicating fair agreement between theoretical analysis and practical results. The simulated output impedance for $I_C = 1\text{mA}$ and for $I_C = 0.7\text{mA}$ is shown in Figure 3.23.

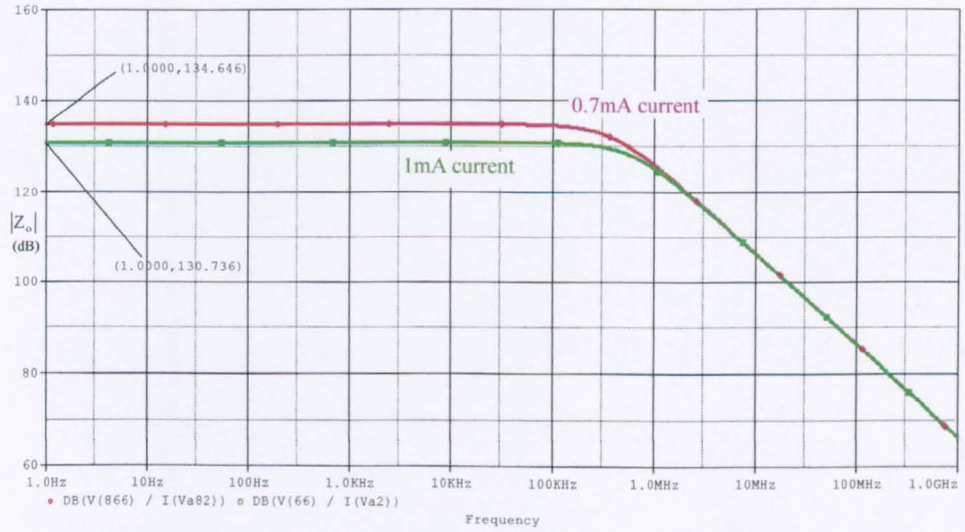

Fig. 3.23 Output impedance of the buffered NPN mirror, with cascoded output, for 1mA and 0.7mA

3.3.3 Precise, multiple-output current-mirror ('6-pack') biasing

The precise multiple-output current-mirror, which will be called the '6-pack' onwards, is a current-mirror that combines high output resistance and excellent current transfer ratio, as well as expandability **[3-7], [3-8]**. The '6-pack' schematic, including the DC currents used for the analysis of the circuit, is shown in Figure 3.24.

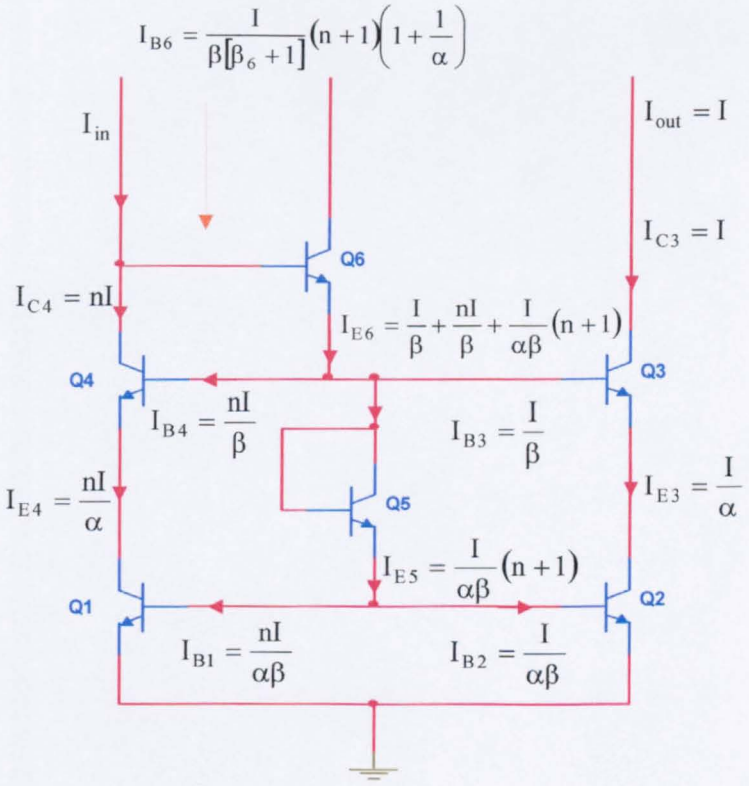

Fig. 3.24 The '6-pack' precise current mirror

It is shown in Appendix 3.3 that the current transfer ratio is,

$$\lambda = \frac{I_{out}}{I_{in}} \approx \frac{1}{n}\left[1 - \frac{\left(2+\frac{2}{n}\right)}{\beta\beta_6}\right] \approx 1 - \frac{4}{\beta^2} \pm \frac{V_{OS}}{V_T} \qquad (3.9)$$

where β_6 is the common-emitter current gain of Q_6, which is different from the other transistors because it operates at lower I_C.

Equation (3.9) is obtained by making the simplifications $\beta_6 = \beta$, $\beta >> 1$, and expressing n in terms of V_{OS}. For $V_{OS} \neq 0$ the third term again dominates, as in the case of the buffered current mirror with cascoded output.

Simulation of the '6-pack' mirror, using $I_C = 1\text{mA}$ and $I_C = 0.7\text{mA}$ at 27°C, gave the transfer ratios illustrated in Figure 3.25.

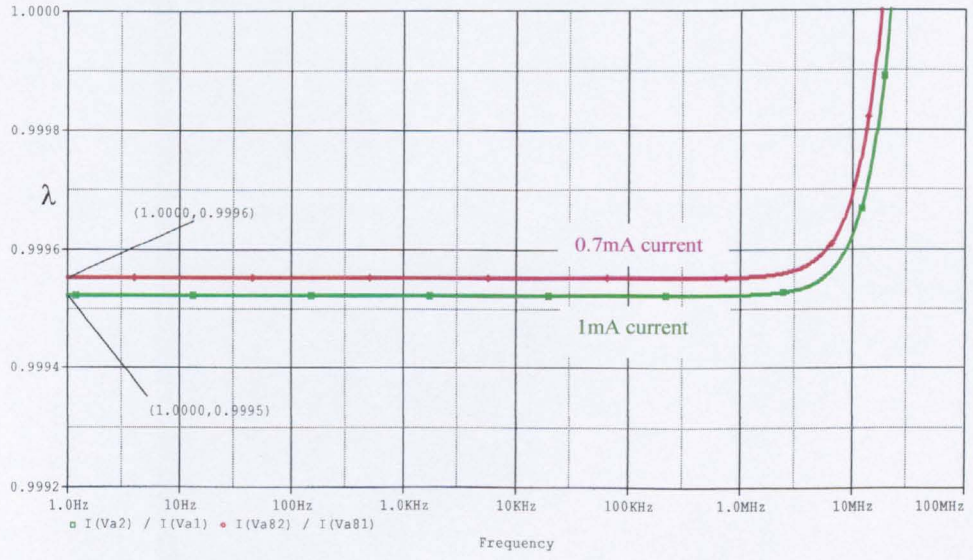

Fig. 3.25 Current transfer ratio, λ, of the '6-pack' for $I_C = 0.7\text{mA}$ and $I_C = 1\text{mA}$

Figure 3.26 shows the λ as a function of T. The very small increase in λ with T is attributable to the increase in transistor's current gain β with T.

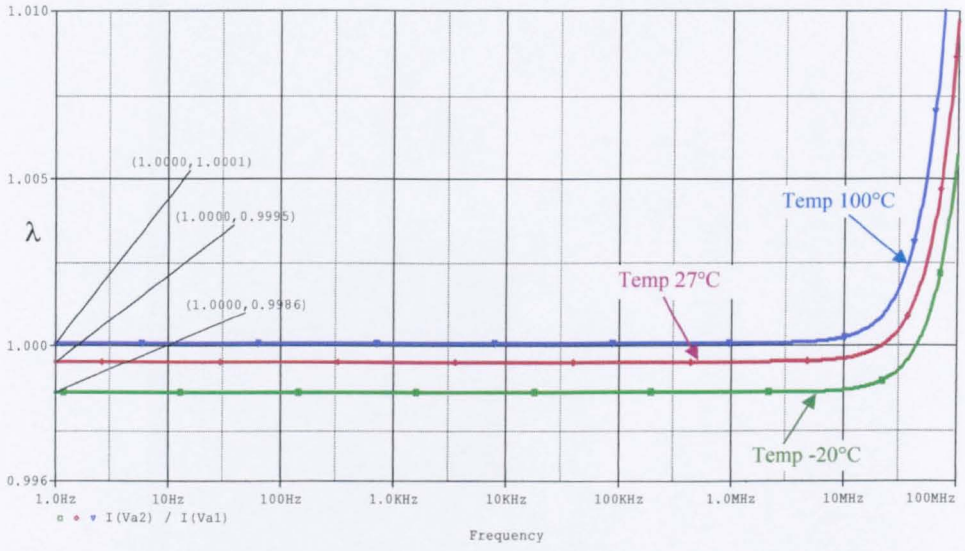

Fig. 3.26 Current transfer ratio, λ, of the '6-pack' for variable T

As mentioned earlier, an advantage of the '6-pack' mirror over conventional designs is its expandability. Thus, the outputs of the circuit can be increased by adding two transistors in parallel with transistors Q_2 and Q_3, as shown in Figure 3.27, without a significant change in λ. It is then technically an '8-pack'.

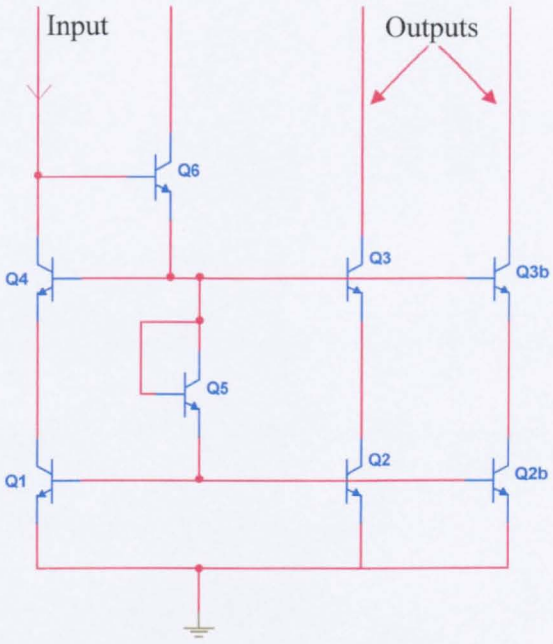

Fig. 3.27 '8-pack' current-mirror

In this case,

$$\lambda = \frac{I_{out}}{I_{in}} \approx 1 - \frac{6}{\beta^2} \pm \frac{V_{OS}}{V_T} \tag{3.10}$$

The output resistance of the '6-pack' mirror can be estimated as shown in Appendix 3.3. Due to the fact that the emitter of transistor Q_6 is connected to a low impedance point, the output resistance is close to that of the common-base stage. Using an infinite impedance current source as the input to the mirror, the output resistance, R_O, is approximated by,

$$R_O \approx \beta r_o \tag{3.11}$$

If the finite output resistance of the current source is taken into account, the output resistance will be

$$R_O = r_o\left[1+\beta\left(1-\frac{1}{\alpha\beta_6\gamma}\right)\right] \tag{3.12}$$

where γ is the ratio between the output resistance of the current source and the resistance seen looking into the base of transistor Q_6. The term $\frac{1}{\alpha\beta_6\gamma}$ cannot always be neglected. Simulation of the '6-pack' current mirror at 27°C for $I_C = 0.7\text{mA}$ and $I_C = 1\text{mA}$ for an infinite output impedance current source drive, gave the output graphs shown in Figure 3.28.

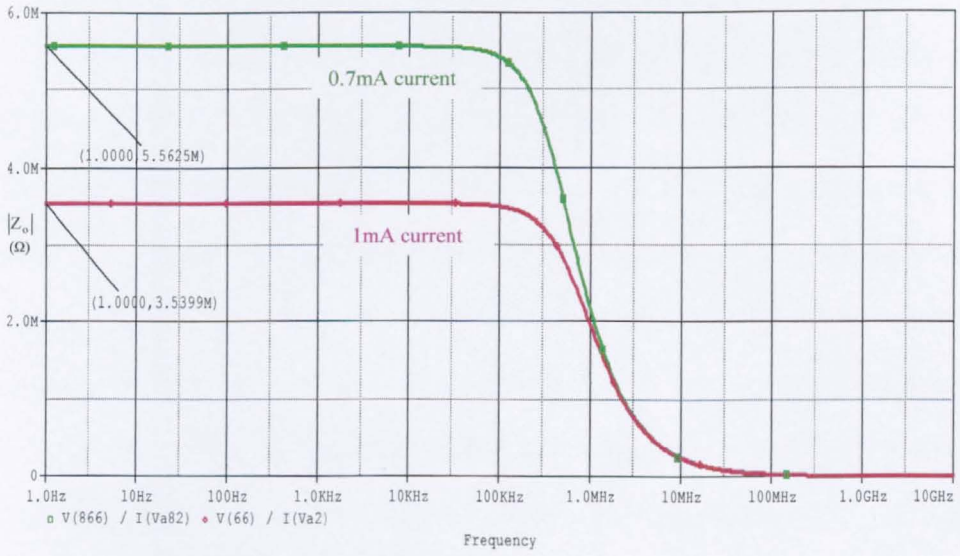

Fig. 3.28 Output impedance of the '6-pack' for $I_C = 0.7\text{mA}$ and $I_C = 1\text{mA}$

A comparison of the output impedance of the common-base stage, the buffered current mirror, with cascoded output, and the precise '6-pack' current mirror

is facilitated by Figure 3.29. The current source used had infinite output resistance, the operation current was 1mA and the temperature 27°C.

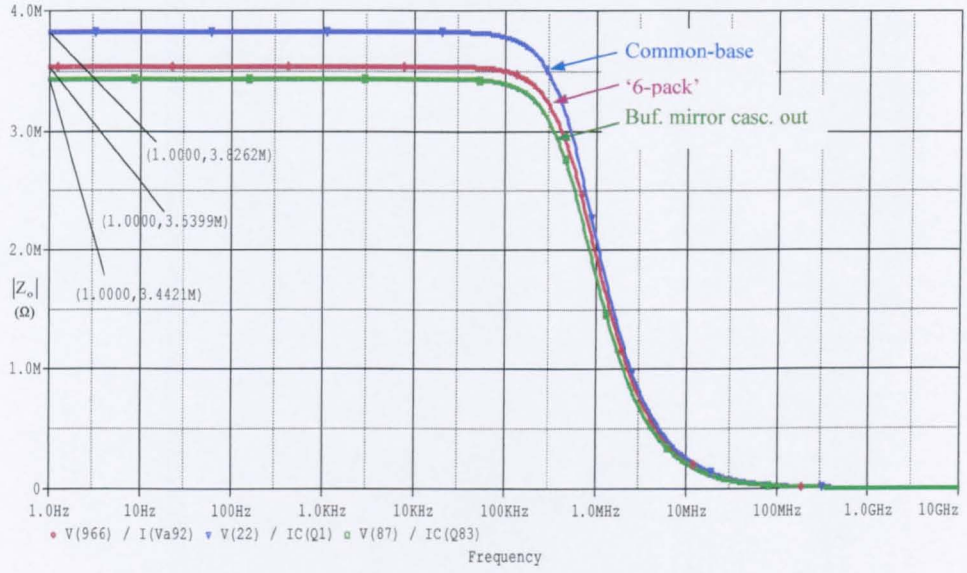

Fig. 3.29 Output impedance for common-base stage, '6-pack' and buffered mirror with cascoded output

Apart from the current mirrors analysed above, several other well-established current mirrors **[3-5 to 3-8]** have been simulated, for research, reference and comparison purposes. The testing was carried out for both output impedance and current transfer ratio, for 1mA input current fed from an infinite output impedance current source, at 27°C. It can be concluded that the buffered mirror with cascoded output as well as the precise current mirror, presented the best results, in both output resistance and current transfer ratio, which is the reason why they are used later throughout the analysis and investigation of conventional and novel voltage-follower designs. The results are shown in Table 3.7.

Configuration	Output current over Input current ratio, λ, for 1mA current	Output Impedance with 1mA current (Ω)
Simple current mirror	1.02	85.9K
Buffered current mirror	1.039	83.77K
Cascoded current mirror	0.929	2.073M
Buffered mirror with cascoded output	0.992	3.442M
Wilson current mirror	0.991	1.835M
Modified Wilson current mirror	1.001	1.804M
Precision '6pack'	0.999	3.539M

Table 3.7 A comparison of several well-established current mirrors and those analysed in the test

3.4 Summary of Chapter 3

This chapter considered a detailed investigation of the transistor-models used throughout this research. It has been identified that some of their parameters listed in SPICE data, were either not appropriate for the operating conditions envisaged or did not correspond to the Spice data at all. Also, other parameters that were not explicitly listed in SPICE parameters obtained, necessary for accurate design based on hand-calculations. Those parameters obtained for a range of different biasing currents and operating temperatures, to allow easier analysis of the proposed designs in the following chapters.

The second part of this chapter considered the analysis of the current-biasing configurations using current mirrors that will be used in the following chapters, for the biasing of the conventional and the proposed voltage-followers. The main criteria for their evaluation were their current-transfer ratio from the input to the output as well as their output impedance at low frequencies. A comparison chart at the end of this chapter justified their performance superiority over several well-established current mirrors.

References for Chapter 3

[3-1] Gray R.P., Hurst J.P., Lewis H.S., and Meyer G.R., 'Analysis and Design of Analog Integrated Circuits', John Wiley and Sons, 4th Edition, New York, 2001, pp.23-28.

[3-2] Terzopoulos N., 'High output resistance current drive circuits for medical applications', Ph.D Thesis, Oxford Brookes University, 2006.

[3-3] Gray R.P., Hurst J.P., Lewis H.S., and Meyer G.R., 'Analysis and Design of Analog Integrated Circuits', John Wiley and Sons, 3rd Edition, New York, 1993, pp.498-500.

[3-4] Greeneich E.W., 'Analog Integrated Circuits', Chapman & Hall, New York, 1997, pp.89-100.

[3-5] Gray R.P., Hurst J.P., Lewis H.S., and Meyer G.R., 'Analysis and Design of Analog Integrated Circuits', John Wiley and Sons, 4th Edition, New York, 2001, pp.260-304.

[3-6] Sedra A., Smith K., 'Microelectronic Circuits', Oxford University Press, 5th Edition, New York, 2004, pp.649-655, pp.567-569.

[3-7] Tammam A.A., 'Novel approaches in current-feedback operational amplifier design', Ph.D Thesis, Oxford Brookes University, 2005.

[3-8] Vere Hunt, M.A., Charles K., 'Design and development of a high slew-rate operational amplifier', Ph.D Thesis, Oxford Brookes University, 1992.

APPENDIX 3

AP3.1 Calculation of the Early-Voltage of the devices used

AP3.2 Analysis of the buffered current mirror with cascoded output

AP3.3 Analysis of the precision multiple-output current-mirror

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Appendix A3.1

Calculation of the Early-Voltage of the devices used

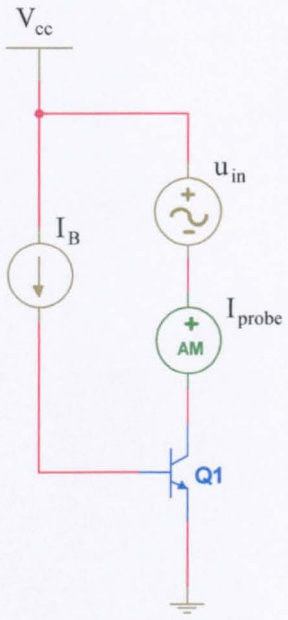


Fig. A3.1 Early-Voltage investigation circuit

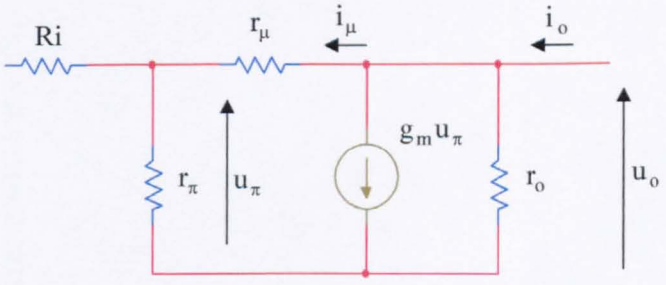


Fig. A3.2 Small-signal low-frequency equivalent model of the transistor Q_1

Figure A3.1 shows the circuit used to calculate the Early-Voltage of the devices used and Figure A3.2 shows the small signal low frequency equivalent circuit of the

transistor Q_1. By inspection,

$$i_o = i_\mu + g_m u_\pi + \frac{u_o}{r_o} \tag{A3.1}$$

where

$$u_\pi = i_\mu r_\pi \tag{A3.2}$$

and

$$i_\mu = \frac{u_o}{r_\mu + r_\pi} \tag{A3.3}$$

and for $r_\mu >> r_\pi$

$$i_\mu = \frac{u_o}{r_\mu} \tag{A3.4}$$

Substituting in (A3.1),

$$i_o = (g_m r_\pi + 1)\frac{u_o}{r_\mu} + \frac{u_o}{r_o} \tag{A3.5}$$

Since $g_m r_\pi = \beta$,

$$i_o = (\beta + 1)\frac{u_o}{r_\mu} + \frac{u_o}{r_o} \tag{A3.6}$$

and,

$$\frac{1}{r_o} = \frac{1}{R_o} - \frac{(\beta + 1)}{r_\mu} \tag{A3.7}$$

The collector-emitter small signal resistance, r_o, is equal to $\frac{V_A}{I_C}$. Thus, the Early-Voltage for a specific operating current can be calculated, since all the rest of the parameters, in (A3.7), are known.

$$\frac{I_C}{V_{AN}} = \frac{1}{R_o} - \frac{(\beta + 1)}{r_\mu} \tag{A3.8}$$

Appendix A3.2

Analysis of the buffered current-mirror

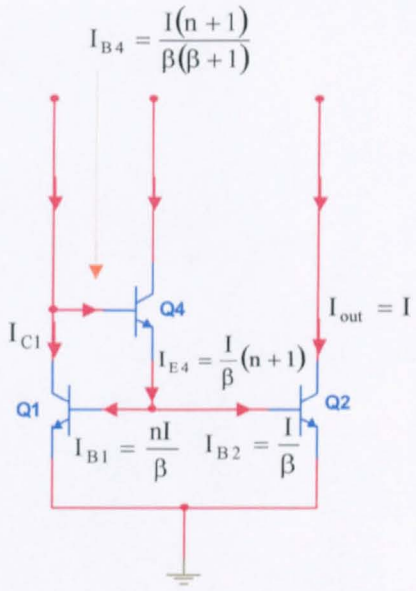


Fig. A3.3 Analysis of the currents of the buffered current-mirror

By inspection, for ideally matched devices,

$$I_{out} = I_{C2} = I \tag{A3.9}$$

since,

and

$$\left.\begin{aligned} I_{C1} &= I_{S1} e^{\frac{V_{BE}}{V_T}} \\ I_{C2} &= I_{S2} e^{\frac{V_{BE}}{V_T}} \end{aligned}\right\} \quad I_{C1} = \frac{I_{S1}}{I_{S2}} I_{C2} \tag{A3.10}$$

if $\frac{I_{S1}}{I_{S2}}$ called **n**, then,

$$I_{C1} = nI_{C2} \tag{A3.11}$$

Also,

$$I_{B2} = \frac{I_{C2}}{\beta} = \frac{I}{\beta} \quad \text{and} \quad I_{B1} = \frac{nI_{C2}}{\beta} = \frac{nI}{\beta}$$

hence,

$$I_{E4} = \frac{I}{\beta} + \frac{nI}{\beta} = \frac{I}{\beta}(n+1) \tag{A3.12}$$

and,

$$I_{B4} = \frac{\frac{I}{\beta}(n+1)}{\beta+1} \tag{A3.13}$$

The input current is,

$$I_{IN} = I_{C1} + I_{B4} = I + \frac{\frac{I}{\beta}(n+1)}{\beta+1} = I\left(1 + \frac{(n+1)}{\beta(\beta+1)}\right) \tag{A3.14}$$

The current transfer ratio, λ, is given by

$$\lambda = \frac{I_O}{I_{IN}} = \frac{I}{I\left(n + \frac{(n+1)}{\beta(\beta+1)}\right)} = \frac{1}{n + \frac{(n+1)}{\beta(\beta+1)}} = \frac{1}{1 + \frac{2}{\beta^2}} \tag{A3.15}$$

Since,

$$V_{BE_1} = V_T \log \frac{I_R}{I_{S1}} \tag{A3.16}$$

and,

$$V_{BE_2} = V_T \log \frac{I_R}{I_{S2}} \tag{A3.17}$$

Expressing the **n** in terms of offset voltage, V_{OS}, (the base-emitter voltage difference for the same collector reference current I_R) , will be

$$V_{OS} = V_{BE_1} - V_{BE_2} \tag{A3.18}$$

or

$$V_{OS} = V_T \log \frac{I_{S2}}{I_{S1}} \tag{A3.19}$$

Rearranging the above equation,

$$\frac{I_{S2}}{I_{S1}} = e^{\frac{V_{OS}}{V_T}} = \frac{1}{n} \tag{A3.20}$$

For $n = 1$, $V_{OS} = 0$, and for **n** close to 1, $V_{OS} << V_T$

Since we can have either of the conditions $I_{S1} > I_{S2}$ or $I_{S2} > I_{S1}$, V_{OS} can have a positive or negative sign

$$\frac{1}{n} \approx 1 \pm \left(\frac{V_{OS}}{V_T} \right) \tag{A3.21}$$

Hence, the final current transfer ratio is

$$\lambda = \frac{I_O}{I_{IN}} = \frac{1}{1 + \frac{2}{\beta^2}} \pm \frac{V_{OS}}{V_T} \tag{A3.22}$$

Appendix A3.3

Analysis of the precision multiple-output current-mirror

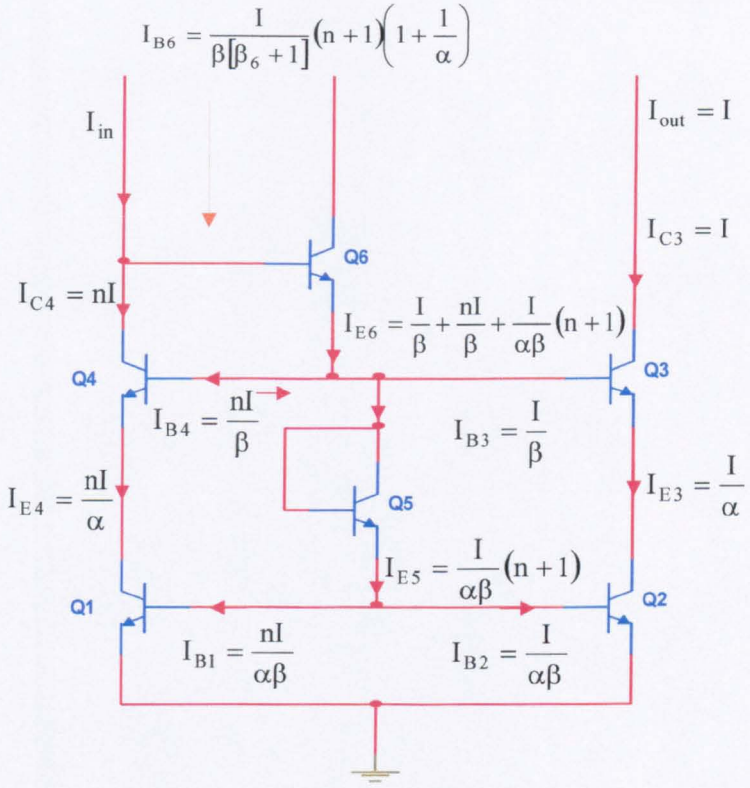


Fig. A3.4 Analysis of the currents of the '6-pack'

By inspection, and using (A3-11),

$$I_{C1} = nI_{C2}$$

By inspection, the currents in each branch of the circuit is,

$I_{out} = I_{C3} = I,$

$$I_{E3} = I_{C3}\frac{\beta+1}{\beta} = \frac{I_{C3}}{\alpha} = \frac{I}{\alpha},$$

$$I_{B3} = \frac{I_{C3}}{\beta} = \frac{I}{\beta},$$

$$I_{B4} = \frac{nI}{\beta},$$

$$I_{C4} = nI,$$

$$I_{E4} = \frac{nI}{\alpha},$$

$$I_{C2} = I_{E3},$$

$$I_{B2} = \frac{I}{\alpha\beta},$$

$$I_{C1} = I_{E4},$$

$$I_{B1} = \frac{nI}{\alpha\beta}, \text{and}$$

$$I_{E5} = \frac{I}{\alpha\beta} + \frac{nI}{\alpha\beta} = \frac{I}{\alpha\beta}(n+1)$$

Hence,

$$I_{E6} = I_{B4} + I_{B3} + I_{E5} = \frac{nI}{\beta} + \frac{I}{\beta} + \frac{I}{\alpha\beta}(n+1) = \frac{I}{\beta}\left(n+1+\frac{1}{\alpha}+\frac{n}{\alpha}\right)$$

and,

$$I_{B6} = \frac{I_{E6}}{\beta_6 + 1} = \frac{I}{\beta(\beta_6 + 1)}(n+1)\left(1+\frac{1}{\alpha}\right) \qquad \text{(A3.23)}$$

$\beta_6 \neq \beta$ due to the much lower collector current of transistor Q_6

The input current is,

$$I_{in} = I_{C4} + I_{B6} = nI + \frac{I}{\beta(\beta_6 + 1)}(n+1)\left(1 + \frac{1}{\alpha}\right) \qquad \text{(A3.24)}$$

and the λ is given by,

$$\lambda = \frac{I_{out}}{I_{in}} = \frac{I}{nI + \frac{I}{\beta(\beta_6 + 1)}(n+1)\left(1 + \frac{1}{\alpha}\right)} = \frac{1}{n + \frac{(n+1)\left(1 + \frac{1}{\alpha}\right)}{\beta(\beta_6 + 1)}} \qquad \text{(A3.25)}$$

since $\frac{1}{\alpha} = \frac{\beta + 1}{\beta}$,

$$\lambda = \frac{I_{out}}{I_{in}} = \frac{1}{n + \frac{(n+1)\left(1 + \frac{\beta+1}{\beta}\right)}{\beta(\beta_6 + 1)}} = \frac{1}{n + \frac{(n+1)\left(2 + \frac{1}{\beta}\right)}{\beta(\beta_6 + 1)}} \qquad \text{(A3.26)}$$

For $\beta >> 1$ and $(\beta_6 + 1) \approx \beta$,

$$\lambda = \frac{I_{out}}{I_{in}} \approx \frac{1}{n + \frac{(n+1)2}{\beta\beta_6}} \approx \frac{1}{n\left[1 + \frac{(n+1)2}{n\beta\beta_6}\right]} \qquad \text{(A3.27)}$$

For $n = 1$,

$$\lambda = \frac{I_{out}}{I_{in}} \approx 1 - \frac{4}{\beta\beta_6} \qquad \text{(A3.28)}$$

Assuming for simplicity that $\beta_6 = \beta$,

$$\lambda = \frac{I_{out}}{I_{in}} \approx 1 - \frac{4}{\beta^2} \qquad \text{(A3.29)}$$

If $n \neq 1$, λ, can expressed in terms of V_{OS}

Then,

$$\lambda \approx \frac{1}{n}\left(1 - \frac{4}{\beta^2}\right) \qquad \text{(A3.30)}$$

The final expression of the current ratio is then,

$$\lambda = \frac{I_{out}}{I_{in}} \approx 1 - \frac{4}{\beta^2} \pm \frac{V_{OS}}{V_T} \qquad \text{(A3.31)}$$

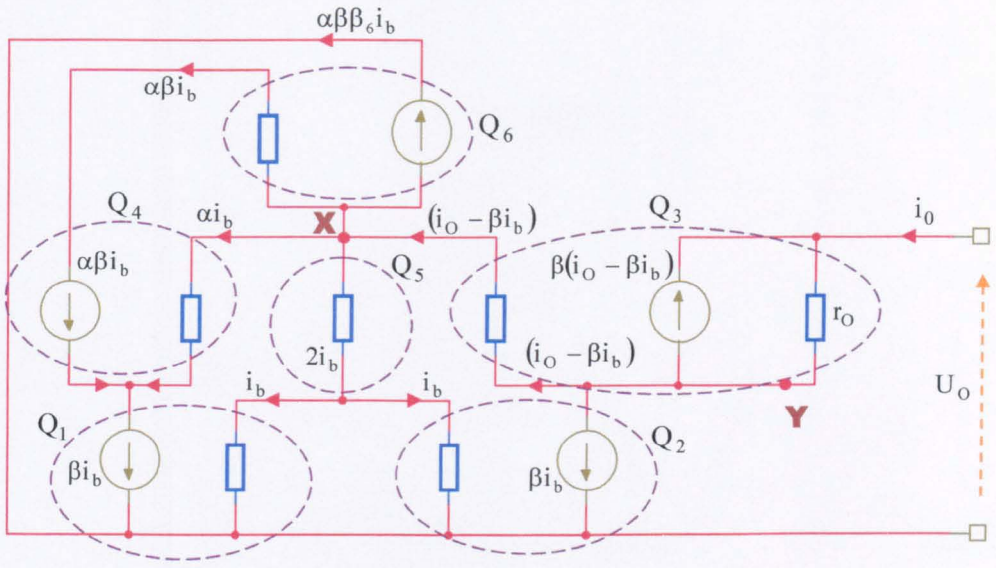


Fig. A3.5 Small signal low-frequency equivalent circuit of 3.41 for infinite impedance current drive

Ignoring initially the r_{ce} of all the transistors apart from Q_3, which in the schematic is named r_o. All the betas apart from β_6 are equal assuming that the transistors work under the same collector current loads. The collector current of transistor Q_6 is much less than the other transistors so the beta of that transistor is not the same as the rest.

At point **X**,

$$(i_o - \beta i_b) = \alpha i_b + 2i_b + \alpha\beta i_b + \alpha\beta\beta_6 i_{b6}$$

$$i_o = i_b(\alpha + 2 + \alpha\beta + \alpha\beta\beta_6 + \beta) \qquad \text{(A3.32)}$$

Since $\alpha\beta\beta_6$ is larger than the sum of the other terms in the bracket,

$$i_o \approx i_b \alpha\beta\beta_6 \tag{A3.33}$$

and,

$$i_b \approx \frac{i_o}{\alpha\beta\beta_6} \tag{A3.34}$$

The current in the r_o is

$$\frac{u_o - u_y}{r_o} = i_o + \beta(i_o - \beta i_b) \tag{A3.35}$$

substituting for i_b,

$$\frac{u_o - u_y}{r_o} = i_o + \beta\left(i_o - \frac{i_o}{\alpha\beta_6}\right) = i_o\left[1 + \beta\left(1 - \frac{1}{\alpha\beta_6}\right)\right] \tag{A3.36}$$

But $\frac{1}{\alpha\beta_6} << 1$

$$\therefore \quad \frac{u_o - u_y}{r_o} = (\beta + 1) i_o \tag{A3.37}$$

and

$$R_O = \frac{u_o}{i_o} = (\beta + 1) r_o + \frac{u_y}{i_o} \tag{A3.38}$$

and because $u_y \geq 0$ the output resistance is

$$R_O \geq (\beta + 1) r_o \approx \beta r_o \tag{A3.39}$$

If the output resistance of the current source feeding the current mirror is not infinite, which is usually the case, some current will pass from the collector of transistor Q_4 to the current source instead of going to the base of Q_6. If the fraction of Q_4's collector current appearing in the base of Q_6 is γ then,

$$i_b \approx \frac{i_o}{\alpha\beta\beta_6\gamma} \tag{A3.40}$$

and

$$\frac{u_o - u_y}{r_o} = i_o\left[1+\beta\left(1-\frac{1}{\alpha\beta_6\gamma}\right)\right] \tag{A3.41}$$

neglecting u_y if compared with u_o

$$\frac{u_o}{r_o} = i_o\left[1+\beta\left(1-\frac{1}{\alpha\beta_6\gamma}\right)\right] \tag{A3.42}$$

and R_O is

$$R_O = r_o\left[1+\beta\left(1-\frac{1}{\alpha\beta_6\gamma}\right)\right] \tag{A3.43}$$

In this case, the term $\frac{1}{\alpha\beta_6\gamma}$ cannot necessarily be neglected.

CHAPTER 4

The conventional emitter–follower / a critical review

4.1 Introduction

The emitter-follower (EF), is at the root of all voltage-follower designs. Dating, as it does, from the earliest days of transistor circuit design and in view of its subsequent ubiquitous use in semiconductor electronics, it might seem that its performance required little discussion beyond a brief reference to textbooks and the technical literature. However, such is not the case. Its treatment in most textbooks is, from a circuit-designer viewpoint, superficial. Most attention seems to be focused on low-frequency small-signal performance with a resistive load. This chapter presents a critical review of emitter-follower operation, with particular reference to high-frequency performance, distortion, and large signal behaviour. Simulated performance results are obtained for specific BJT types and operating conditions.

The analysis of the conventional emitter-follower will be carried out using both ideal and practical current biasing. The precise current-mirror '6-pack', analysed in Chapter 3, will be used as a practical biasing scheme, due to its superiority over similar designs. The same configuration will be used for the biasing of the novel voltage-followers, in the forthcoming chapters. The circuit, using an ideal and a practical current sink, is illustrated in Figures 4.1 and 4.2, respectively.

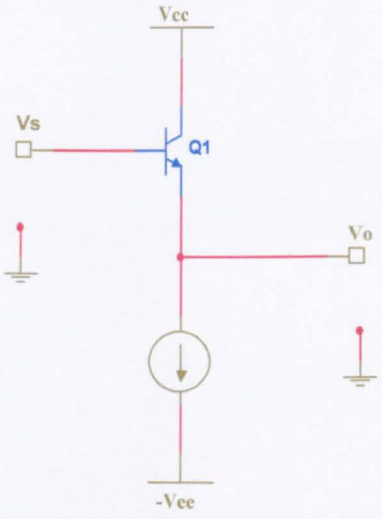


Fig. 4.1 The conventional emitter-follower with ideal current biasing

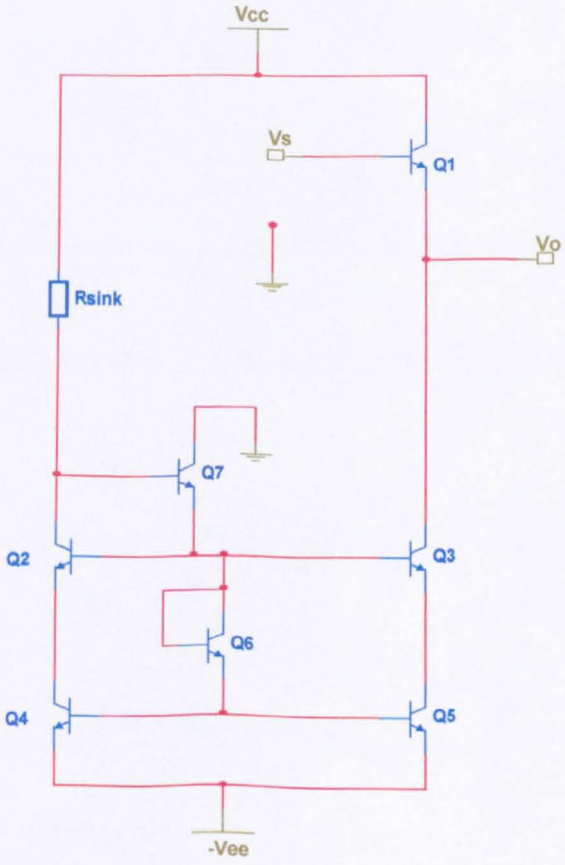


Fig. 4.2 The conventional emitter-follower with '6-pack' current biasing

4.2 DC conditions

Consider the circuit of Figure 4.3, in which the emitter-follower transistor, Q, is biased with a constant current I_o and drives a resistive load R_L.

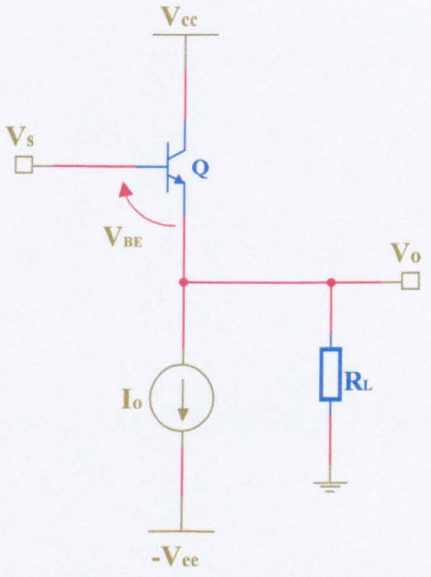


Fig. 4.3 General biasing scheme for a conventional emitter-follower

Two expressions **[4-1]** can be written for the collector current I_C:

$$I_C = I_S\left(1+\frac{V_{CB}}{V_{AN}}\right)\exp\frac{V_{BE}}{V_T} \tag{4.1}$$

and,

$$I_C = \alpha I_E = \alpha\left(I_o + \frac{V_o}{R_L}\right) \tag{4.2}$$

The output voltage V_o is given by,

$$V_o = V_S - V_{BE} \tag{4.3}$$

V_{BE} can be found by equating (4.1) and (4.2)

Thus,

$$I_S\left(1+\frac{V_{CB}}{V_{AN}}\right)\exp\left(\frac{V_{BE}}{V_T}\right)=\alpha\left(I_o+\frac{V_o}{R_L}\right) \tag{4.4}$$

Substituting $(V_{CC}-V_S)$ for V_{CB}, transposing and using the resulting V_{BE} in (4.3)

$$V_o = V_S - V_T \log_e \frac{\alpha\left(I_o+\frac{V_o}{R_L}\right)}{I_S\left[1+\frac{(V_{CC}-V_S)}{V_{AN}}\right]} \tag{4.5}$$

Figure 4.4 shows a graphical interpretation of this condition for $V_S = 0$, for which $V_o = -V_{BE(0)}$

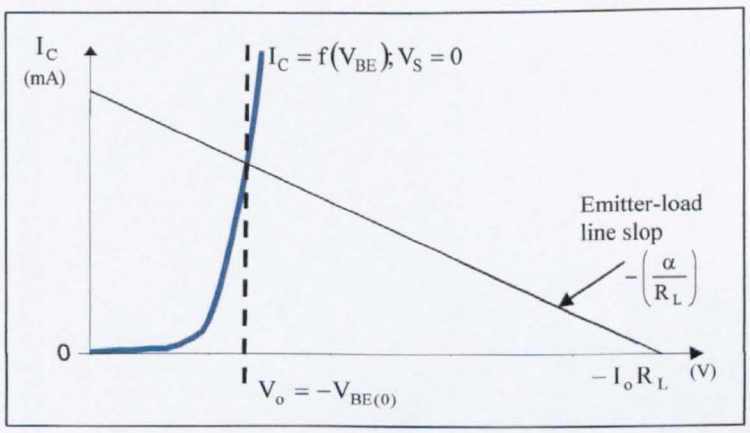


Fig. 4.4 Graphical construction of the operating point for $V_S = 0$

This assumes the source supplying I_o does not saturate.

As V_S changes from zero, the emitter load line slides parallel to itself to the right, for $V_S > 0$, or to the left, for $V_S < 0$. The variation of V_o with V_S can be found from (4.5), when rewritten as,

$$V_o = V_S - V_T\left[\log_e \alpha + \log_e\left(I_o + \frac{V_o}{R_L}\right) - \log_e I_S - \log_e\left[1 + \frac{(V_{CC} - V_S)}{V_{AN}}\right]\right] \quad (4.6)$$

Since α and I_S are not functions of V_S,

$$\left(\frac{dV_o}{dV_S}\right) = 1 - V_T\left[\frac{1}{R_L\left(I_o + \frac{V_o}{R_L}\right)}\left(\frac{dV_o}{dV_S}\right) + \frac{1}{(V_{AN} + V_{CC} - V_S)}\right] \quad (4.7)$$

Transposing and writing G for the slope $\left(\frac{dV_o}{dV_S}\right)$ of the transfer characteristic in the linear region,

$$G = \frac{\left[1 - \frac{V_T}{(V_{AN} + V_{CC} - V_S)}\right]}{\left[1 + \frac{V_T}{(V_o + I_o R_L)}\right]} \quad (4.8)$$

Since $V_T (\approx 25\text{mV}) << V_{AN}$, $I_o R_L$ (or, V_o if $I_o = 0$), G, though not strictly constant is close to unity over a linear range.

A sketch of the theoretical transfer characteristic, not to scale, is shown in Figure 4.5, in which V_γ is the base-emitter threshold of conduction voltage for Q.

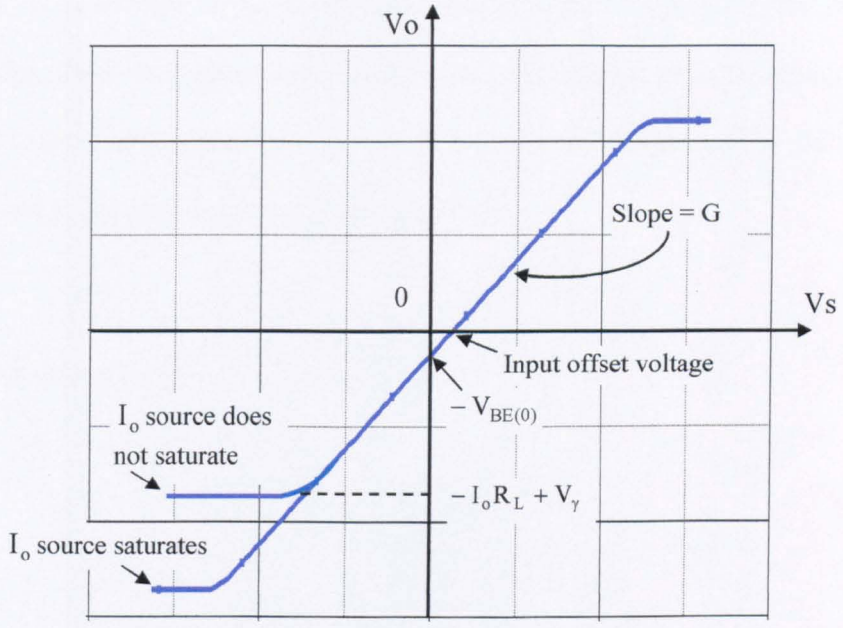


Fig. 4.5 Transfer characteristic for circuit of Figure 4.1

Figure 4.6 shows simulation plots for the circuit of Figure 4.1, for $I_o = 1mA$, and $R_L = \infty$ for three different temperatures (-20°C, 27°C and 100°C).

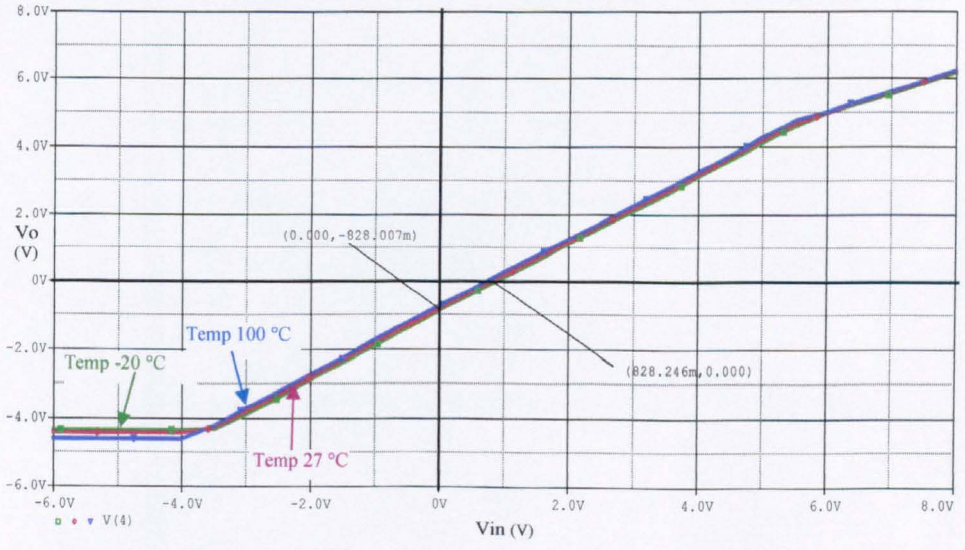


Fig. 4.6 Simulated transfer characteristic for circuit of Figure 4.1 : $V_{CC} = V_{EE} = 5V; I_o = 1mA; R_L = \infty$

These confirm the main conclusion of the foregoing analysis. G is sensibly constant and near to unity (for I_o and R independent of T) over the linear range because V_T, although temperature dependent, is always small compared with the terms with which it is associated. Furthermore, the small shift in the characteristic parallel to itself with change in temperature is due to the approx 2mV/°C decrease in V_{BE}, in (4.3), for each degree of temperature rise.

The input current is I_B,

$$I_B = \frac{\left(I_o + \frac{V_o}{R_L}\right)}{(\beta + 1)} \tag{4.9}$$

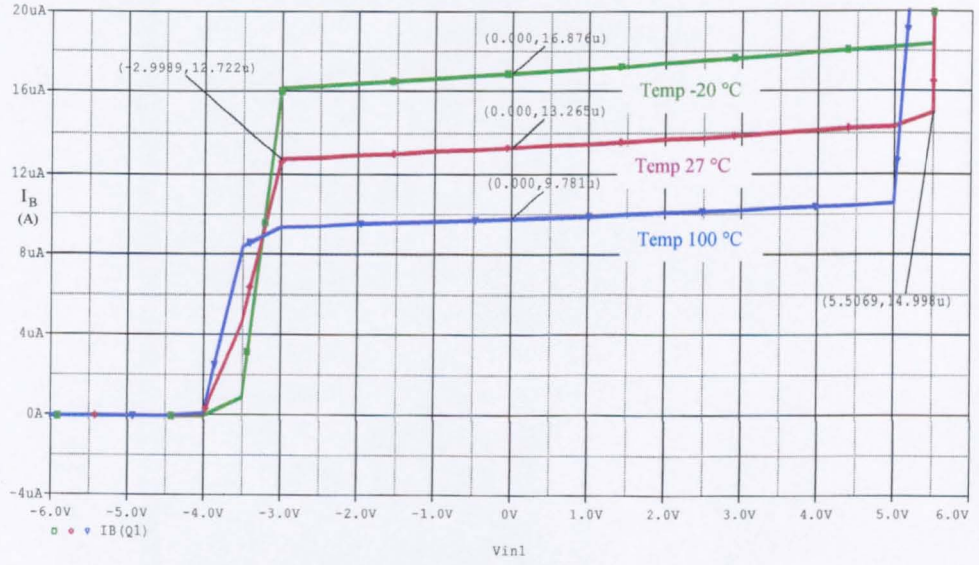


Fig. 4.7 Input current of the circuit of Figure 4.1 for $I_o = 1mA$; $R_L = \infty$

For fixed I_o , I_B still varies with T because of the temp-dependence of V_o and β.

Thus, for Figure 4.7, by logarithmic differentiation,

$$\frac{1}{I_B}\left(\frac{dI_B}{dT}\right) \approx -\frac{1}{\beta}\left(\frac{d\beta}{dT}\right) \tag{4.10}$$

The variation of I_B for $5V > V_S > -3V$ is due to the variation of β with V_{CB}.

$$\frac{dI_B}{dV_S} = \frac{d}{d_\beta}\left[\frac{I_o}{(\beta+1)}\right]\frac{d\beta}{dV_{CB}}\cdot\frac{dV_{CB}}{dV_S} \tag{4.11}$$

$$\frac{dI_B}{dV_S} = -\frac{I_o}{(\beta+1)^2}\cdot\frac{d}{dV_{CB}}\left[\beta_o\left(1+\frac{V_{CB}}{V_{AN}}\right)\right]\frac{dV_{CB}}{dV_S} \tag{4.12}$$

But, $V_{CB} = V_{CC} - V_S$

$$\therefore \quad \frac{dV_{CB}}{dV_S} = -1 \tag{4.13}$$

$$\therefore \quad \frac{dV_{CB}}{dV_S} = \left[-\frac{I_o}{(\beta+1)^2}\cdot\frac{\beta_o}{V_{AN}}\right]\cdot(-1) = \frac{I_o}{(\beta+1)^2}\cdot\frac{\beta}{V_{AN}} \tag{4.14}$$

However,

$$I_C \approx \frac{I_o\beta_o}{(\beta+1)}, \text{ and}$$

$$\frac{V_{AN}}{I_C} = r_o$$

Thus,

$$\therefore \quad \frac{dI_B}{dV_S} = \frac{1}{(\beta+1)r_o} \tag{4.15}$$

or,

$$R_{in} \approx (\beta+1)r_o \tag{4.16}$$

This analysis ignores the existence of r_μ but the expression approximates the incremental input resistance.

The power supplied by V_{CC} to the collector of Q, and hence the collector power dissipation P_C, is given by,

$$P_C = \alpha\left(I_o + \frac{V_o}{R_L}\right)V_{CC} \tag{4.17}$$

The power P_S supplied by the source V_S to the base of Q is,

$$P_S = \frac{\alpha\left(I_o + \frac{V_o}{R_L}\right)}{(\beta+1)}V_S \tag{4.18}$$

Table 4.1 shows the quiescent power dissipation measured for both circuits

Power dissipation (mW)			
Operating temperature (°C)	**-20**	**27**	**100**
Circuit of Fig. 4.1	9.93	9.94	9.96
Circuit of Fig. 4.2	19.7	20.2	21.1

Table 4.1 Power dissipation with ideal and real biasing

4.3 Small-signal voltage-gain with zero source resistance

Figure 4.8 shows the full small-signal equivalent circuit a conventional emitter-follower (EF) driven by an ideal sinusoidal voltage source and driving a parallel $R_E C_L$ load, where R_E is the parallel equivalent of $r_{CE}\left(=\frac{V_{AN}}{I_C}\right)$, the incremental resistance of current bias circuit, and any external load.

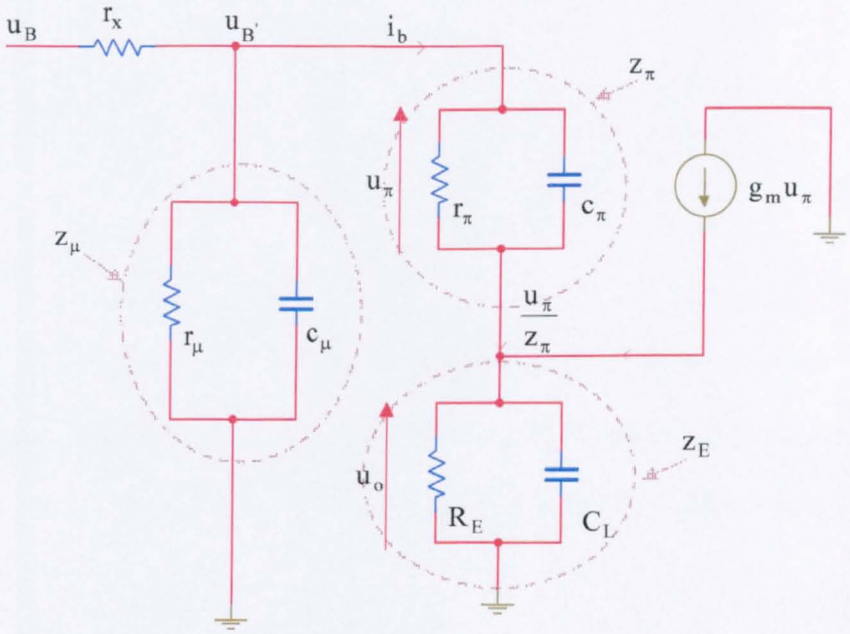


Fig. 4.8 small-signal equivalent circuit of the conventional emitter-follower

It is shown in Appendix 4.1 that if r_x, c_μ, r_μ are neglected, for reasons discussed later, then the frequency response of this EF configuration is given, in terms of the complex frequency variable 's' by,

$$G(s) \approx \frac{\left(g_m + \frac{1}{r_\pi}\right)\left[1 + \frac{sc_\pi}{g_m}\right]R_E}{\left[1 + \left(g_m + \frac{1}{r_\pi}\right)R_E\right]\left[1 + \frac{sR_E(C_L + c_\pi)}{1 + g_m R_E}\right]} \tag{4.19}$$

This has a zero,

$$\omega_z = \frac{g_m}{c_\pi} \tag{4.20}$$

and a pole,

$$\omega_p = \frac{(1 + g_m R_E)}{R_E(C_L + c_\pi)} \tag{4.21}$$

For the usual case $g_m R_E >> 1$,

$$\omega_p \approx \frac{g_m}{(C_L + c_\pi)} \tag{4.22}$$

For $C_L = 0$ and $C_L << c_\pi$, ω_z and ω_p are comparable but if $C_L >> c_\pi$, then ω_p dominates the frequency response. From previous work (Chapter 3) on common-base response at 1mA, $f_T = 4.72\text{GHz}$, $c_\mu = 32.7\text{fF}$ and $c_\pi = 1.277\text{pF}$. Substituting for $C_L = 5\text{pF}$,

$$\omega_p \approx \frac{g_m}{C_L + c_\pi} = \frac{\frac{I_c}{V_\tau}}{C_L + c_\pi} = \frac{\frac{1\text{mA}}{25.8\text{mV}}}{5 \cdot 10^{-12} + 1.27 \cdot 10^{-12}} = 6.174\text{rad/s}$$

Which corresponds to,

$$f_B = 983\text{MHz}$$

For $I_C = 0.7\text{mA}$,

$$\omega_p \approx \frac{g_m}{C_L + c_\pi} = \frac{\frac{I_c}{V_\tau}}{C_L + c_\pi} = \frac{\frac{0.7\text{mA}}{25.8\text{mV}}}{5\cdot10^{-12} + 0.886\cdot10^{-12}} = 4.609\text{rad/s}$$

which corresponds to,

$$f_B = 734\text{MHz}$$

Similarly, for $C_L = 10\text{pF}$, ω_P is given by,

$$\omega_p \approx \frac{g_m}{C_L + c_\pi} = \frac{\frac{I_c}{V_\tau}}{C_L + c_\pi} = \frac{\frac{1\text{mA}}{25.8\text{mV}}}{10\cdot10^{-12} + 1.27\cdot10^{-12}} = 3.439\text{rad/s}$$

Which corresponds to,

$$f_B = 548\text{MHz}$$

and for $I_C = 0.7\text{mA}$,

$$f_B = 397\text{MHz}$$

Figure 4.9 shows $|G|$, in dB, over the frequency range for three loading conditions : $C_L = 0$; $C_L = 5\text{pF}$; $C_L = 10\text{pF}$. The curves apply for both ideal current bias of 1mA and for '6-pack' current biasing. The results show the practical bias scheme did not result in a poorer frequency response. As predicted by the foregoing analysis, f_B decreases with capacitive loading. The comparable figures, both simulated and predicted, are as follows for the case of $C_L = 5\text{pF}$ and $C_L = 10\text{pF}$.

The bracketed figures refer to the predicted values

$$f_B = 1.051\text{GHz}(983\text{MHz}) \quad ; \quad f_B = 551\text{MHz}(548\text{MHz})$$

Some difference between predicted and simulated results is to be expected because r_x and c_μ have been neglected to simplify the analysis. For ideal voltage drive this is a plausible because the product $r_x c_\mu$ implies a pole frequency greater than that expected for the capacitive load conditions.

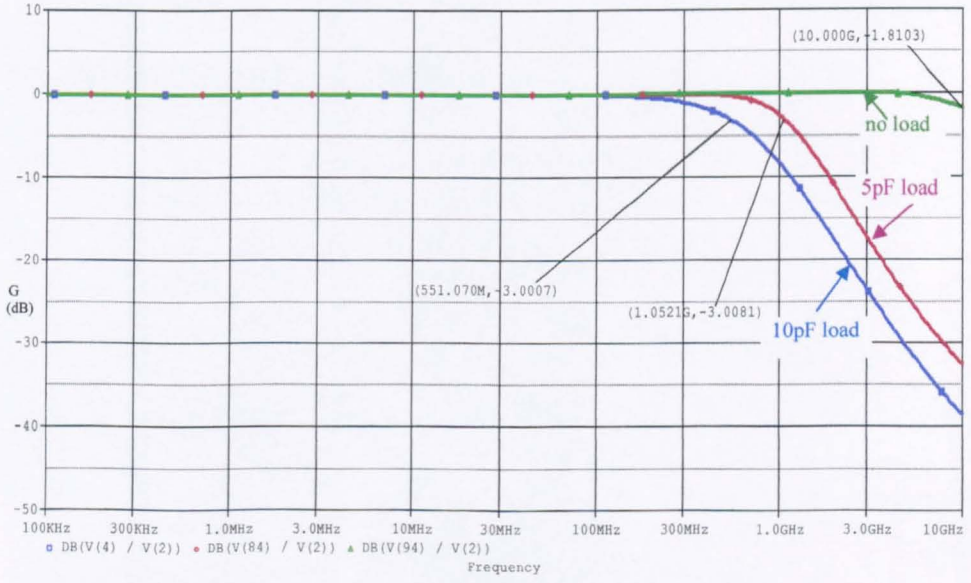


Fig. 4.9 Frequency response for the magnitude of small signal gain G of the conventional emitter-follower with different loads

4.4 Small-signal voltage-gain with finite source resistance

The previous section dealt with the case of the EF with ideal voltage drive. That is an idealisation not encountered in practise but it does produce the best results for frequency response against which the results for other types of drive can be compared. Thus it was claimed that for an ideal voltage drive the effect of c_μ could be ignored. That claim will now be examine, on follow.

Consider the general circuit of Figure 4.10, which is the circuit of Figure 4.8 with the addition of a source resistance R_S

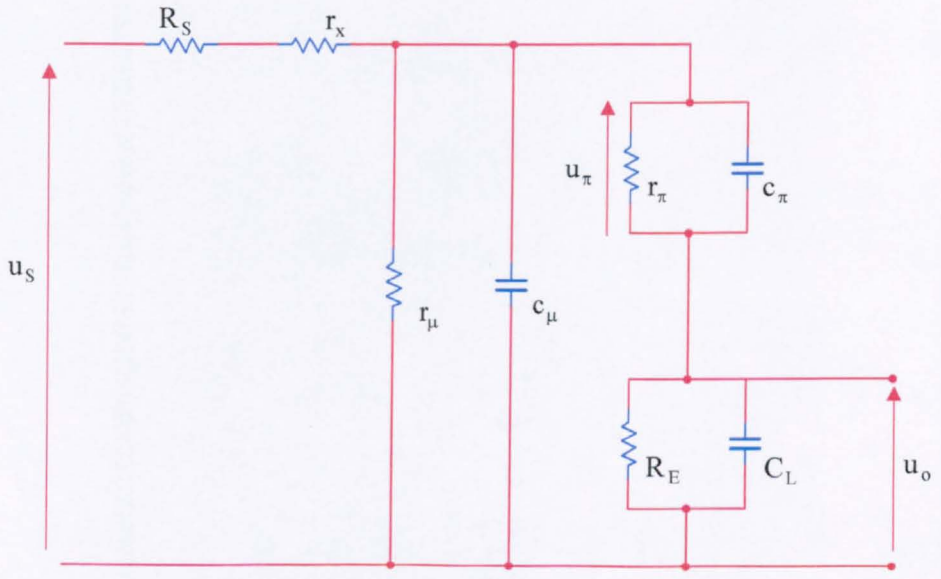


Fig. 4.10 EF with finite source resistance drive and an $R_E C_L$ load

For an arbitrary value of R_S it does not follow that c_μ can be ignored. Because of the presence of three capacitors, an accurate expression for $G(s)$obscures

physical insight. An approximate method to find the cut-off frequency, assuming that a dominant pole exists, is the open-circuit time constant technique **[4-2]**. Thus, suppose the effective resistance $r_{\pi o}$ seen looking between the terminals of c_π, with c_μ and C_L removed. Then the effect of c_π on the frequency response is governed by $r_{\pi o}c_\pi$. Similarly, with c_μ and c_π removed the effective resistance appearing across the terminal of C_L is r_{Lo} and the effect of C_L accounted for by the product $R_{Lo}C_L$. The product $r_{\mu o}c_\mu$ takes care of the effect of c_μ.

The dominant frequency pole in this circuit is given by,

$$\omega_P = \frac{1}{r_{\pi o}c_\pi + R_{Lo}C_L + r_{\mu o}c_\mu} \tag{4.23}$$

where,

$$r_{\mu o}c_\mu = \left[(R_S + r_x)//(r_\pi + (1 + g_m R_E))\right]c_\mu \tag{4.24}$$

$$r_{\pi o}c_\pi = \left[r_\pi // \left(\frac{R_S + r_x + R_E}{(1 + g_m R_E)}\right)\right]c_\pi \tag{4.25}$$

$$R_{Lo}C_L = \left[R_E // \left(\frac{R_S + r_x + r_\pi}{(1 + g_m r_\pi)}\right)\right]C_L \tag{4.26}$$

For $R_S = 0$, $r_{\mu o}c_\mu \approx r_x c_\mu$, which can be ignored compared with either $r_{\pi o}c_\pi$ or $R_{Lo}C_L$.

Taking the case $(R_S + r_x) = 0$ then,

$$(r_{\pi o} c_\pi + R_{Lo} C_L) \approx \frac{(C_L + c_\pi)}{g_m} = \frac{1}{\omega_T} \tag{4.27}$$

This agrees with the expression derived in the previous section.

For R_S in the KΩ range the effect of $r_{\mu o} c_\mu$ might not be negligible. However, results were obtained (Figure 4.11) for $C_L = 5pF$ and $C_L = 10pF$ with $R_S = 0$, $R_S = 25\Omega$, $R_S = 100\Omega$. These show a small decrease in bandwidth with the small values of R_S indicated.

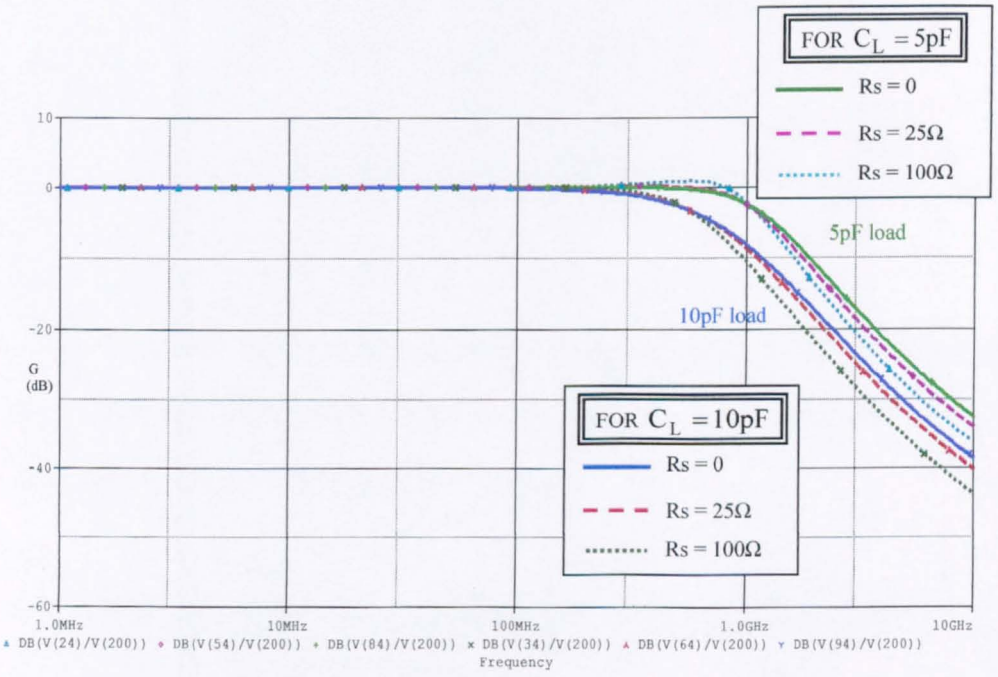


Fig. 4.11 The effect of the finite source resistance on frequency response of the EF

4.5 Input impedance

4.5.1 Theoretical background

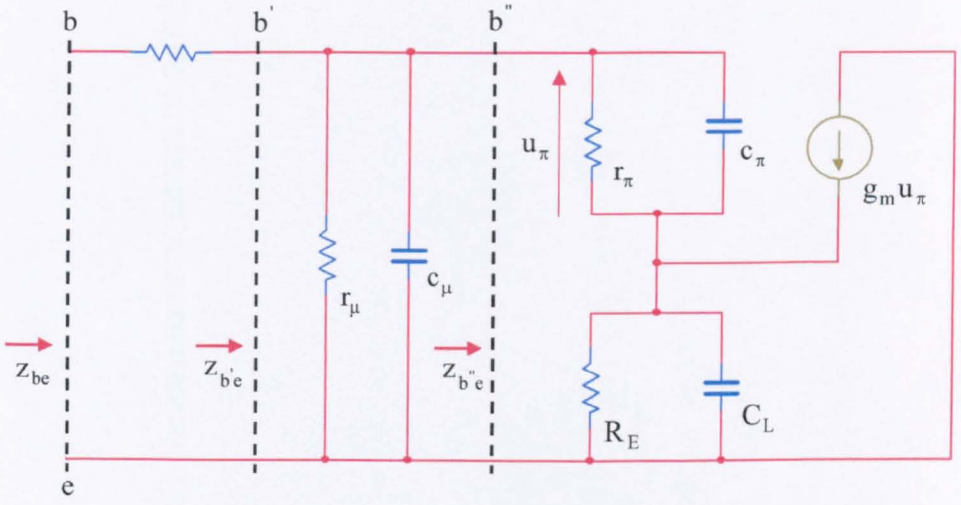


Fig. 4.12 Small-signal equivalent circuit, of the EF, for finding Z_{be}

Figure 4.12 shows a small-signal equivalent circuit of the EF with a capacitive load. The treatment of this circuit in textbooks, seems to have been ignored. The analysis presented here is thought to be original.

Under normal operating conditions it is shown in Appendix AP4.2 that,

$$z_{b"e(j\omega)} \approx \frac{\left[r_\pi + R_E(1+\beta_o)\right]\left(1+\frac{j\omega}{\omega_z}\right)}{\left(1+j\frac{\omega}{\omega_{p1}}\right)\left(1+j\frac{\omega}{\omega_{p2}}\right)} \qquad (4.28)$$

where,

$$\omega_z = \frac{g_m}{(C_E + c_\pi)} \tag{4.29}$$

$$\omega_{p1} = \frac{1}{c_\pi r_\pi} \tag{4.30}$$

$$\omega_{p2} = \frac{1}{C_L R_E} \tag{4.31}$$

Hence,

$$z_{b''e(j\omega)} \approx \frac{\left[r_\pi + R_E(1+\beta_o)\right]\left[1 + j\left(\frac{\omega}{\omega_z}\right)\right]}{\left[1 - \left(\frac{\omega^2}{\omega_{p1}\omega_{p2}}\right)\right] + j\omega\left(\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}}\right)} \tag{4.32}$$

For $\omega << \sqrt{\omega_{p1}\omega_{p2}} << \omega_z$ it follows that,

$$z_{b''e(j\omega)} \approx \frac{\left[r_\pi + R_E(1+\beta_o)\right]}{\left[1 + j\omega(c_\pi r_\pi + C_L R_E)\right]} \tag{4.33}$$

The numerator is the input impedance as $\omega \to 0$ is the incremental input resistance called here R'.

Thus,

$$R' = \left[r_\pi + R_E(1+\beta_o)\right] \approx r_\pi(1 + g_m R_E) \tag{4.34}$$

The approximation holds for the normal condition $\beta_o >> 1$. This is, of course, the value obtained for input resistance by treating the EF from a feedback viewpoint : $g_m R_E$ is the loop-gain.

Re-arranging (4.33),

$$z_{b''e(j\omega)} \approx \frac{R'}{\left[1 + j\omega r_\pi (1 + g_m R_E) \dfrac{\left(c_\pi + \left(\dfrac{R_E}{r_\pi}\right) C_L\right)}{(1 + g_m R_E)}\right]} \tag{4.35}$$

or,

$$z_{b''e} \approx \frac{R'}{(1 + j\omega R' C')} \tag{4.36}$$

where,

$$C' = \frac{c_\pi + \left(\dfrac{R_E}{r_\pi}\right) C_L}{(1 + g_m R_E)} \tag{4.37}$$

The mid-band gain $G(o)$ is given by,

$$G(o) = \frac{g_m R_E}{(1 + g_m R_E)} \tag{4.38}$$

Hence,

$$[1 - G(o)] = \frac{1}{(1 + g_m R_E)} \tag{4.39}$$

Consequently,

$$C' = \left[c_\pi + \left(\frac{R_E}{r_\pi}\right) C_L\right][1 - G(o)] \tag{4.40}$$

Thus, $z_{b''e}$ is given by Figure 4.13,

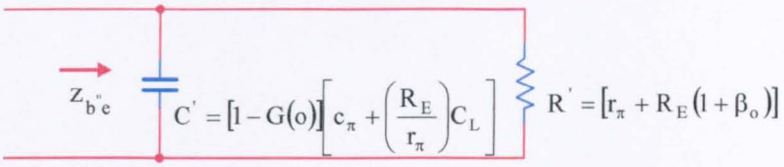


Fig. 4.13 Equivalent circuit for $z_{b''e}$

For the particular case $C_L = 0$,

$$C' = c_\pi[1 - G(o)] \tag{4.41}$$

This demonstrates that the reduction in c_π, as seen between the terminals b'' and e, is due to the EF bootstrap effect.

Incorporating c_μ **[4-3]**, a circuit representation of $z_{b'e}$ is given by Figure 4.14.

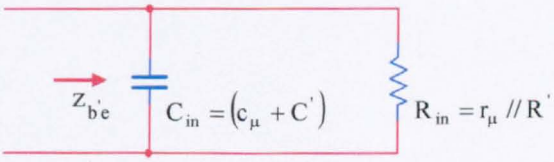


Fig. 4.14 Equivalent circuit for $z_{b'e}$ including c_μ

$$z_{b'e(j\omega)} = \frac{R_{in}}{(1 + j\omega C_{in} R_{in})} \tag{4.42}$$

Allowing now for r_x, z_{be} can be obtained,

$$z_{be(j\omega)} = r_x + \frac{R_{in}}{(1 + j\omega C_{in} R_{in})} \tag{4.43}$$

or,

$$z_{be(j\omega)} = \frac{r_x + j\omega C_{in} R_{in} r_x + R_{in}}{(1 + j\omega C_{in} R_{in})} \tag{4.44}$$

Thus,

$$z_{be(j\omega)} = \frac{(r_x + R_{in})\left[1 + \frac{j\omega C_{in} R_{in} r_x}{(R_{in} + r_x)}\right]}{(1 + j\omega C_{in} R_{in})} \tag{4.45}$$

It is clear that the effect of r_x can be ignored for the case of ideal voltage drive because $R_{in} >> r_x$ and the numerator zero is at $\omega_z \approx 1/C_{in} r_x$ $(>> 1/C_{in} R_{in})$. Driving it from a non-ideal voltage source, with output resistance R_S, the impedance seen by the source is not significantly different from $z_{be(j\omega)}$ provided $(R_S + r_x) << (R_{in} + r_x)$, i.e., $R_S << R_{in}$.

If $R_E C_L >> r_\pi c_\pi$, then ,

$$C' = \frac{\left(\frac{R_E C_L}{r_\pi}\right)}{(1 + g_m R_E)} \tag{4.46}$$

As $g_m R_E >> 1$ and $g_m r_\pi = \beta_o$,

$$C' = \frac{C_L}{\beta_o} \tag{4.47}$$

The equivalent circuit for $z_{be(j\omega)}$ is shown in Figure 4.15.

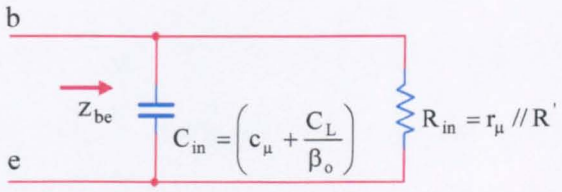


Fig. 4.15 Equivalent circuit for z_{be}

4.5.2 Simulation results

Extensive simulation tests were made to test the applicability of the equations derived for the above practical EF. In the first set of tests $C_L = 0$ and R_L was made infinity, 5KΩ and 1KΩ for both the conditions $I_C = 0.7\text{mA}$ and $I_C = 1\text{mA}$. The test results for $I_C = 1\text{mA}$, only, are discussed here for the case of an NPN BJT. Further results, for $I_C = 0.7\text{mA}$ are given in Appendix AP4.3 together with similar results for a PNP device.

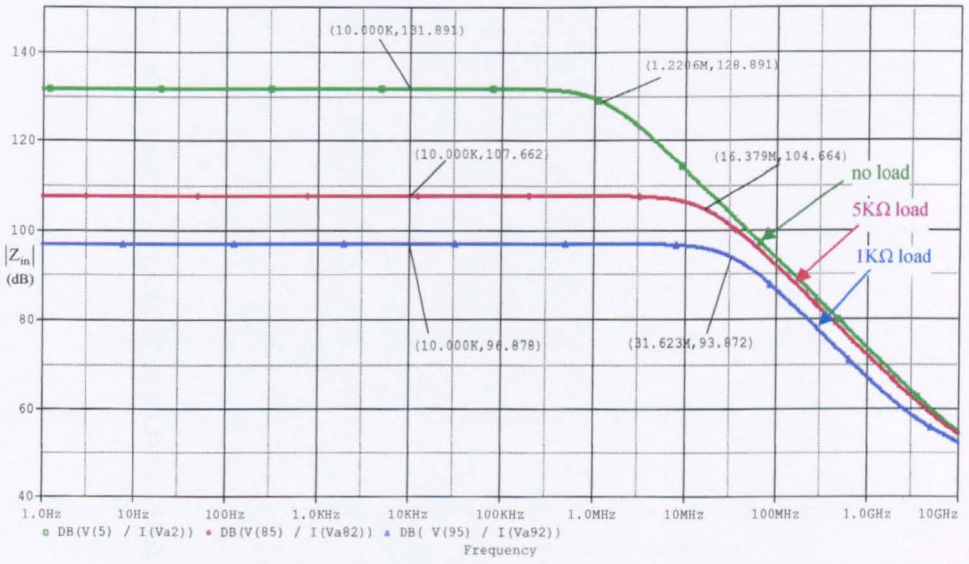


Fig. 4.16 Bode plot for $|Z_{in}|$ for $I_C = 1\text{mA}$ and an NPN BJT (T=27°C)

The predicted value of R_{in} for $R_L = \infty$, based on the use of the formula $R_{in} = [r_\pi + (\beta_o + 1)R_E] // r_\mu$, is within 5% of the value, 3.919MΩ found by simulation, as shown in Figure 4.16. There is a similar agreement for the case $R_L = 5\text{K}\Omega$ and

$R_L = 1K\Omega$. In all cases, the roll-off in $|Z_{in(j\omega)}|$ above the associated cut-off frequency corresponds to -20dB/decade, implying that Z_{in} can be represented by a parallel resistor-capacitor combination up to about 1GHz. This is further confirmed by the shape of the phase shift graph in Figure 4.17.

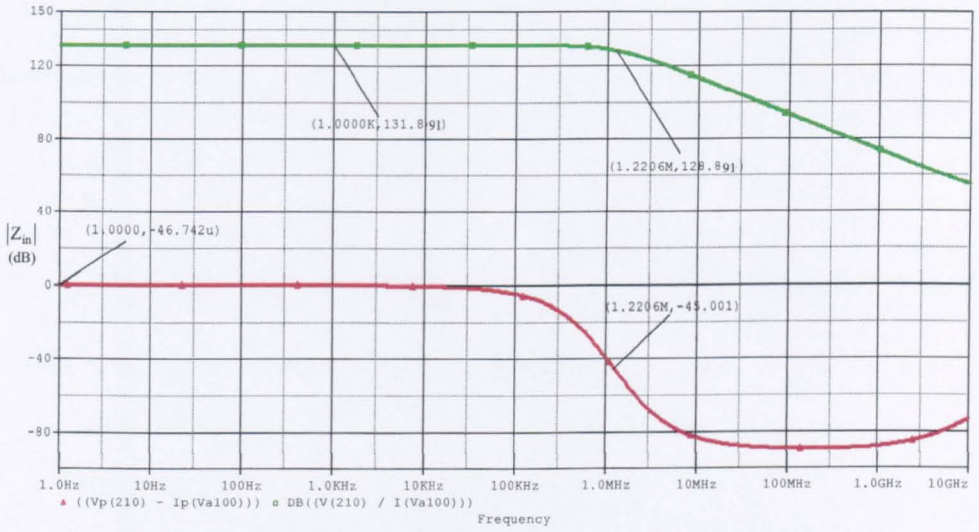


Fig. 4.17 Magnitude (upper curve) and input phase (lower curve) of Z_{in}

Spot values of $|Z_{in}|$, for future reference, for $R_L = \infty$ and $R_L = 5K\Omega$ as a function of f and T are given in Tables 4.2 and 4.3, respectively.

Conditions	$\|Z_{in}\|$ **(Ω)**					
Operating temperature (°C)	**-20**	**27**	**100**	**-20**	**27**	**100**
f = 312.5KHz	2.91M	3.8M	5.3M	2.9M	3.7M	5M
f = 31.25MHz	156K	153K	154K	141K	139K	140K
f = 250MHz	19.5K	19.2K	19.2K	17.5K	17.4K	17.6K
Current source used	Ideal current source/sink			'6-pack' current source/sink		

Table 4.2 $|Z_{in}|$ of the EF, with $R_L = \infty$, as a function of f and T, for $I_C = 1mA$

Conditions	$\|Z_{in}\|$ (Ω)					
Operating temperature (°C)	-20	27	100	-20	27	100
f = 312.5KHz	184K	241K	343K	175K	227K	318K
f = 31.25MHz	106K	112K	118K	98K	104K	109K
f = 250MHz	16.1K	15.8K	15.7K	14.8K	14.6K	14.7K
Current source used	Ideal current source/sink			'6-pack' current source/sink		

Table 4.3 $|Z_{in}|$ of the EF, with $R_L = 5K\Omega$, as a function of f and T for $I_C = 1mA$

The increase of $|Z_{in}|$ with temperature is due to the increase of β with T. Consider, now, in more detail the frequency response for $C_L = 0$.

Theoretically,

$$C_{in} = c_\mu + \frac{c_\pi}{(1 + g_m R_E)} \tag{4.48}$$

Previous measurements (Chapter 3) gave $c_\mu = 32.75fF$. c_π is bigger than c_μ but $g_m R_E \approx \frac{V_{AN}}{V_T} \approx 3500$, it follows that c_μ dominates C_{in}. Consequently, the cut-off frequency for $|Z_{in}|$ should be given, approximately, by,

$$f_B = \frac{1}{2\pi R_{in} c_\mu} = \frac{1}{2\pi \cdot 3.919M\Omega \cdot 32.75fF} = 1.24MHz \tag{4.49}$$

This is very close to the simulation figure of 1.2206MHz.

To prove further that c_μ was the primary cause in the fall-off in $|Z_{in}|$, further tests were carried out in which c_μ was artificially increased by adding extra collector-base capacitance in parallel (see Figure 4.18).

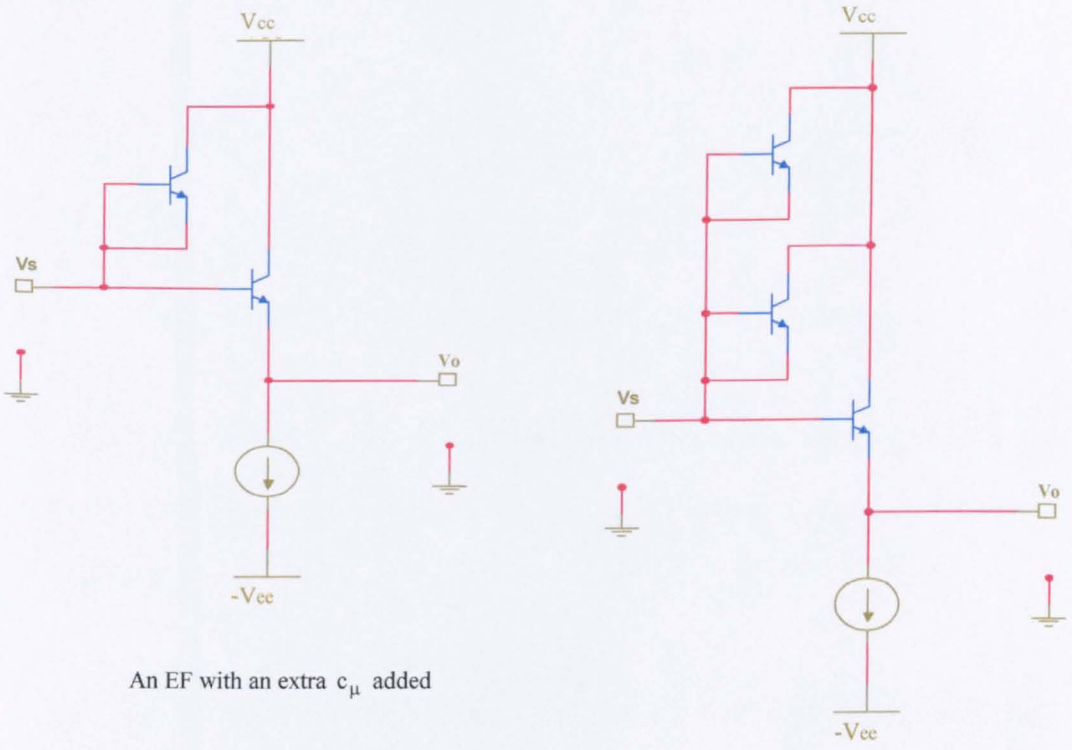


Fig. 4.18 Emitter-followers with added collector-base capacitance

With one added c_μ f_B should be half and with two extra c_μs, f_B should be reduced to one third of the value for no added c_μ.

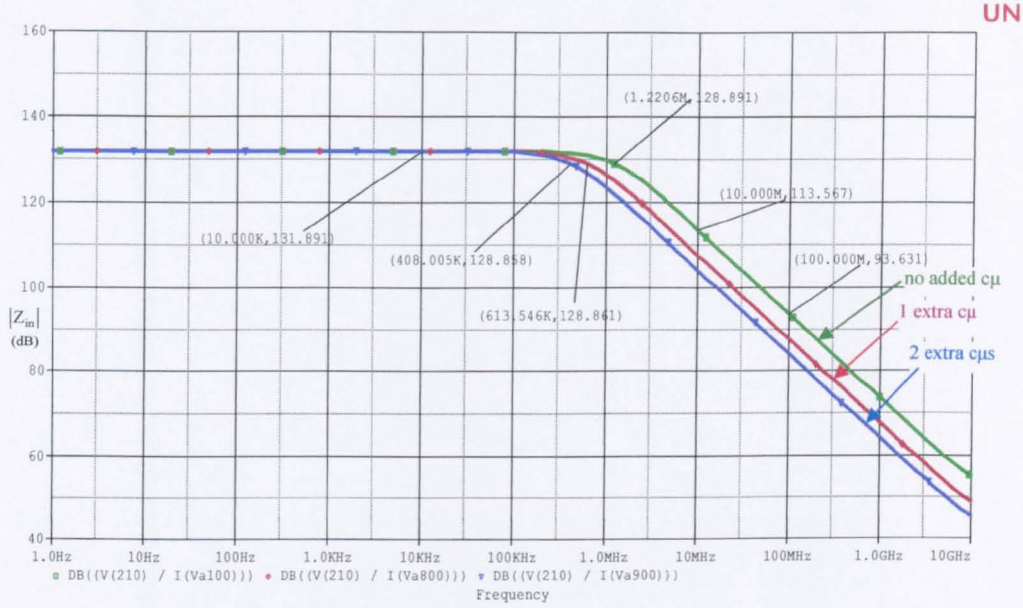


Fig. 4.19 Showing the effect on bandwidth of added c_μ, with $R_L = \infty, C_L = 0$

The simulation results, displayed in Figure 4.19, validate these predictions. At 613KHz and 408KHz, f_Bs are within less than 1% of being exact sub-multiplies of 1.2206MHz.

In a second set of tests the effect of C_L $(>> c_\pi)$ on f_B was investigated for the case of $R_L = \infty$ and $C_L = 5\text{pF}$. It is clear from Figure 4.15 that f_B should be reduced by a factor m where,

$$m \approx \left(1 + \frac{C_L}{\beta_o c_\mu}\right) \tag{4.50}$$

Thus, for $C_L = 5\text{pF}\,(= 5000\text{fF})$, $\beta_o = 46$ and $c_\mu = 32.75\text{fF}$, $m \approx 4.4$

Hence, the new value of f_B should be 277KHz.

In Figure 4.20, showing simulation results for the NPN BJT, for $I_C = 1mA$.

Curve (i) applies for $C_L = 0$, and curve (ii) applies for $C_L = 5pF$.

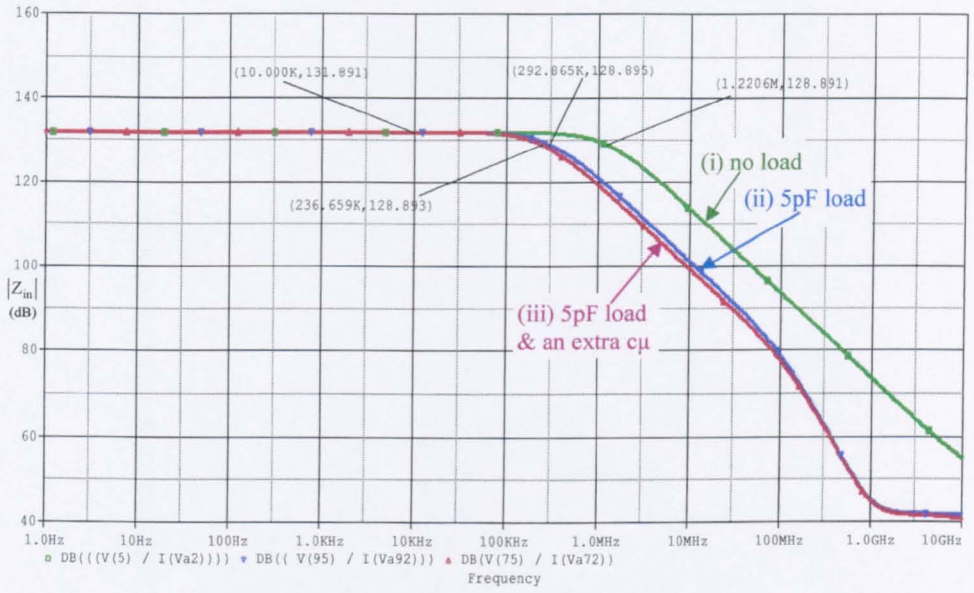


Fig. 4.20 Showing the effect of added C_L on bandwidth

f_B, at approximately 293KHz is just over 5% more than the predicted value. Curve (iii) shows the small effect of the addition an extra c_μ, with $C_L = 5pF$. Further results, for $I_C = 0.7mA$ are shown in Appendix 4.4 together with similar results for the PNP device.

It is worth noting that in a textbook by Wilmshurst **[4-4]** f_B for $C_L = 0$ is given as equal to f_β which is clearly not the case, because of the dominating effect of c_μ, ignored in Wilmshurst's graphical display.

4.6 Output Impedance

Figure 4.21 shows a small-signal equivalent circuit for the calculation of the output impedance Z_o of the emitter-follower: (r_μ is ignored because of its magnitude compared with other resistors in the circuit).

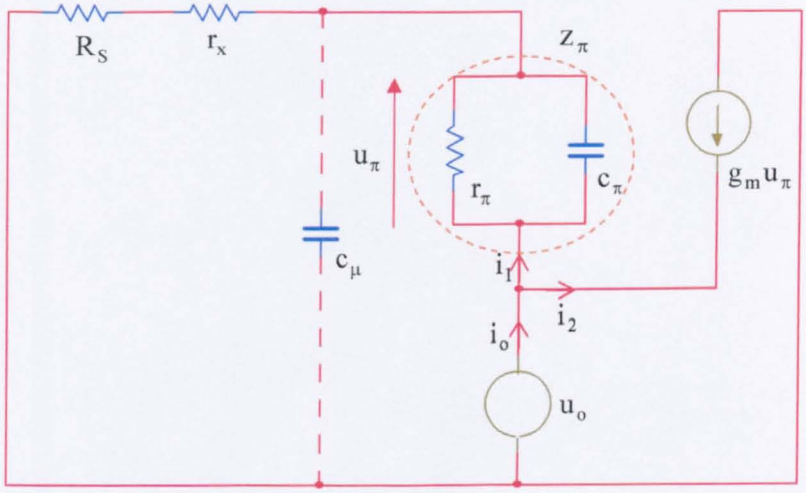


Fig. 4.21 Circuit for calculation of Z_o

For generality, a base source resistance R_S is included. The connections to c_μ are shown dotted because c_μ is ignored in an initial analysis. However, its effect is considered later. The externally applied test voltage u_o gives rise to an output current $i_o = u_o / Z_o$ which comprises two parts i_1, i_2.

By inspection,

$$i_1 = \frac{u_o}{z_\pi + (R_S + r_x)} \tag{4.51}$$

Also,

$$i_2 = \frac{g_m z_\pi}{z_\pi + (R_S + r_x)} \tag{4.52}$$

$$\therefore \quad i_o = (i_1 + i_2) = u_o\left[\frac{1 + g_m z_\pi}{z_\pi + (R_S + r_x)}\right] \tag{4.53}$$

Thus,

$$Z_o = \frac{z_\pi + (R_S + r_x)}{(1 + g_m z_\pi)} \tag{4.54}$$

But,

$$z_\pi = \frac{r_\pi}{1 + j\omega c_\pi r_\pi} \tag{4.55}$$

$$\therefore \quad Z_o = \frac{\left[\dfrac{r_\pi}{1 + j\omega c_\pi r_\pi} + (R_S + r_x)\right]}{\left(1 + \dfrac{g_m r_\pi}{1 + j\omega c_\pi r_\pi}\right)} = \frac{(r_\pi + R_S + r_x) + j\omega c_\pi r_\pi (R_S + r_x)}{(1 + g_m r_\pi) + j\omega c_\pi r_\pi} \tag{4.56}$$

or,

$$Z_o = \frac{\left[1 + \dfrac{j\omega c_\pi r_\pi (R_S + r_x)}{(r_\pi + R_S + r_x)}\right](r_\pi + R_S + r_x)}{(1 + \beta_o)\left(1 + \dfrac{j\omega c_\pi r_\pi}{(1 + \beta_o)}\right)} \tag{4.57}$$

and,

$$Z_o \approx \frac{(r_\pi + R_S + r_x)}{(1 + \beta_o)} \frac{\left[1 + \dfrac{j\omega c_\pi r_\pi (R_S + r_x)}{(r_\pi + R_S + r_x)}\right]}{1 + j\dfrac{\omega}{\omega_T}} \tag{4.58}$$

A linearised Bode magnitude plot for this, shown in Figure 4.22, has a zero at $\omega = \omega_z$ and a pole at $\omega = \omega_{p1}$.

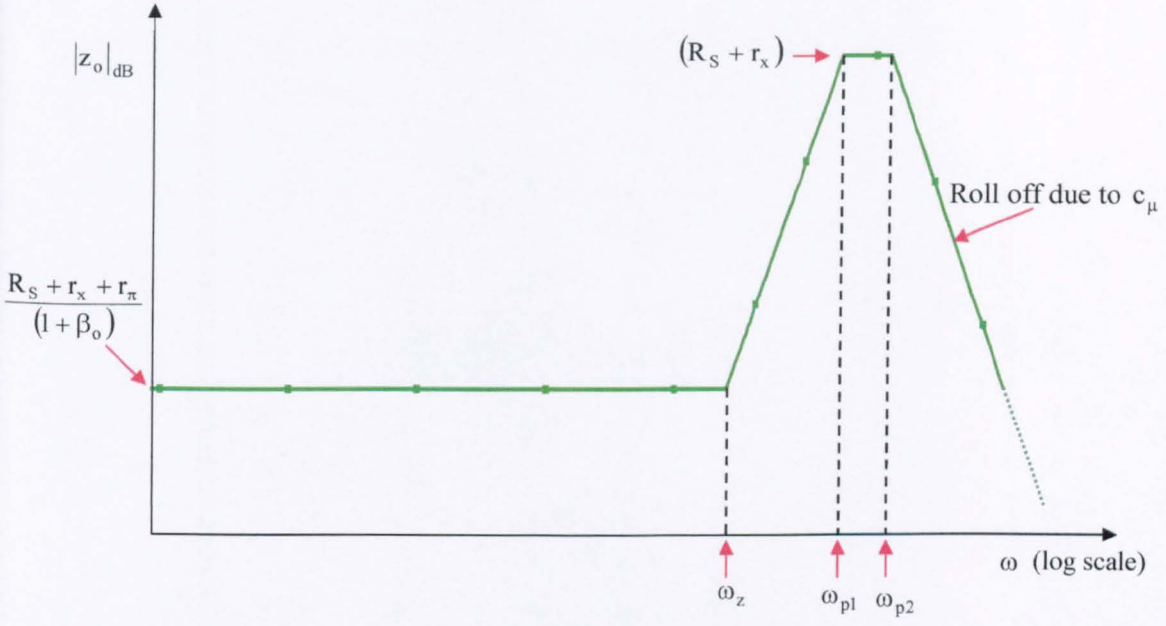


Fig. 4.22 Linearised Bode plot for $|z_o|$

$$\omega_z = \frac{(r_\pi + R_S + r_x)}{c_\pi r_\pi (R_S + r_x)} \tag{4.59}$$

$$\omega_{p1} = \omega_T$$

At frequencies higher than ω_T, the effect of c_μ comes into play and there is an additional pole at $\omega = \omega_{p2}$, where ω_{p2} is dependent on the product $c_\mu(R_S + r_x)$. The details are not given here because this effect occurs at frequencies well above those of interest (It is also questionable whether the simple hybrid-π model, used so

far, is applicable at these frequencies). What is certain is that, because of c_μ, $z_o \to 0$ as $\omega \to \infty$

For frequencies below ω_p, equation 7.60 in **[4-5]** can be re-cast, in the form,

$$z_o = R_o + j\omega L \tag{4.60}$$

where,

$$R_o = \frac{R_S + r_x + r_\pi}{(1+\beta_o)} \approx \frac{1}{g_m} + \frac{R_S + r_x}{(1+\beta_o)} \tag{4.61}$$

and,

$$L = \frac{c_\pi r_\pi (R_S + r_x)}{(1+\beta_o)} \tag{4.62}$$

But,

$$\frac{c_\pi r_\pi}{(1+\beta_o)} \approx \frac{c_\pi}{g_m} \approx \frac{1}{\omega_T} \tag{4.63}$$

$$\therefore \quad L = \frac{(R_S + r_x)}{\omega_T} \tag{4.64}$$

For $R_S = 0$,

$$R_o = \frac{1}{g_m} + \frac{r_x}{(1+\beta_o)} \approx 31.4\Omega \text{ , and} \tag{4.65}$$

$$L = \frac{r_x}{\omega_T} = 8.4\text{nH} \tag{4.66}$$

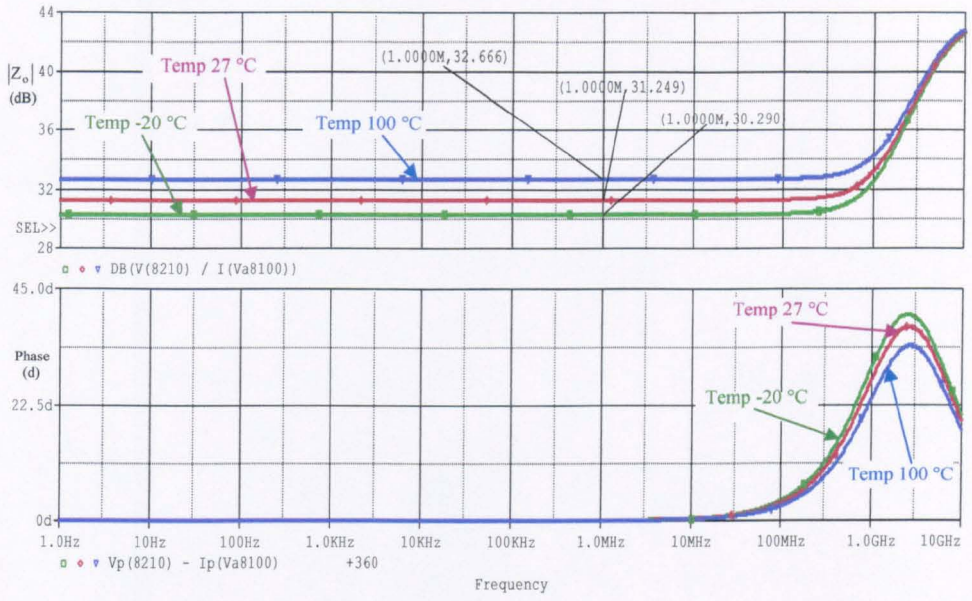


Fig. 4.23 Magnitude (upper curve) and phase (lower curve) of z_o as a function of f and T

Conditions	$\|Z_o\|$ **(Ω)**					
Operating temperature (°C)	**-20**	**27**	**100**	**-20**	**27**	**100**
f = 312.5KHz	32.6	36.5	42.9	33.3	36.5	41.5
f = 31.25MHz	32.6	36.5	42.9	33.3	36.5	41.5
f = 250MHz	33.3	37.1	43.5	34	37.2	42.1
Current source used	Ideal current source/sink			'6-pack' current source/sink		

Table 4.4 $|Z_o|$ of the EF, at $I_C = 1\text{mA}$, as a function of f and T

The significance of L is appreciated if the emitter-follower drives another EF with a capacitive load **[4-6]**, as in Figure 4.24.

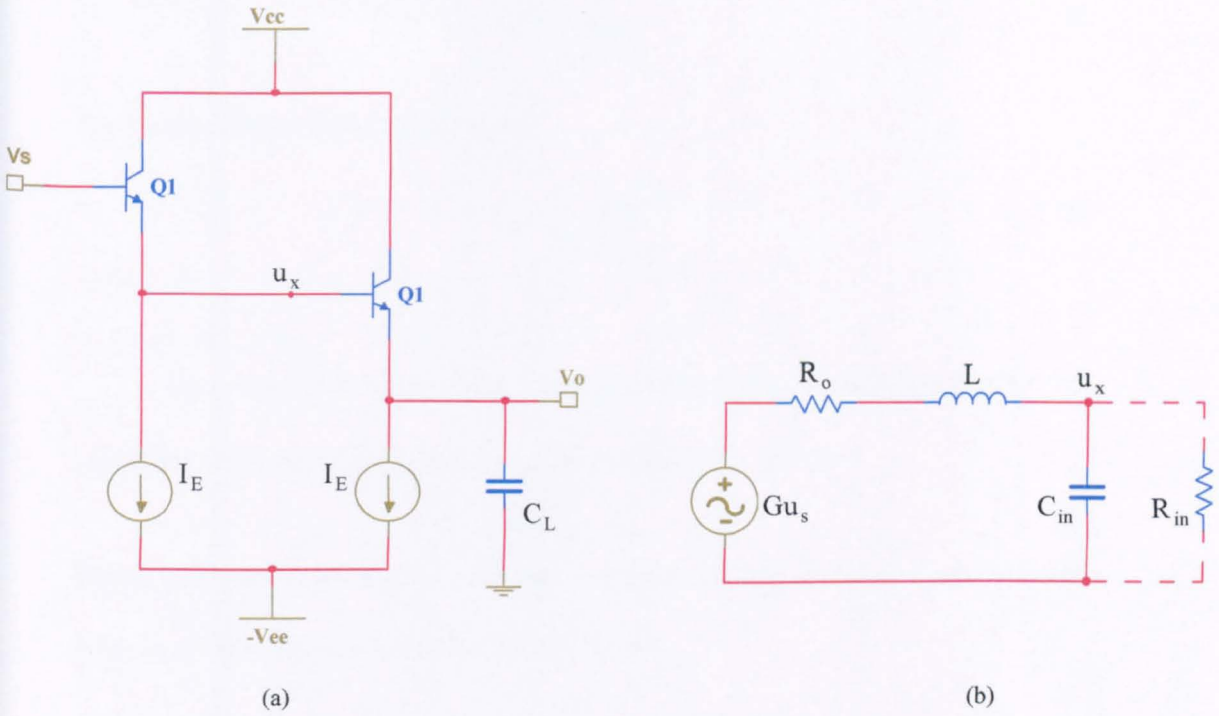


Fig. 4.24 (a) An EF driving another with capacitive load C_L, and, (b) equivalent circuit to find v_x

Using earlier results,

$$C_{in} \approx \left[c_\mu + \frac{C_L}{(\beta+1)} \right] \tag{4.67}$$

and,

$$R_{in} \approx (\beta+1)\frac{V_{AN}}{I_E} \tag{4.68}$$

For $\omega >> \frac{1}{C_{in}R_{in}}$, R_{in} can be neglected : (that is why the connections to it are shown dotted in Figure 4.24(b). The series circuit remaining has a resonant frequency at $\omega = \omega_r$ where,

$$\omega_r = \frac{1}{\sqrt{LC_{in}}} \tag{4.69}$$

The Quality Factor Q **[4-7]** is given by,

$$Q = \frac{1}{R_o}\sqrt{\frac{L}{C_{in}}} \tag{4.70}$$

There is no peak in the small signal frequency for u_x, and no overshoot in the associated small signal step-response at the output of Q_2, if Q<0.5.

Figure 4.25 shows the small signal step response, for the circuit of Figure 4.24(a), with $C_L = 5pF$, for which L (calculated) $\approx 8.4nH$

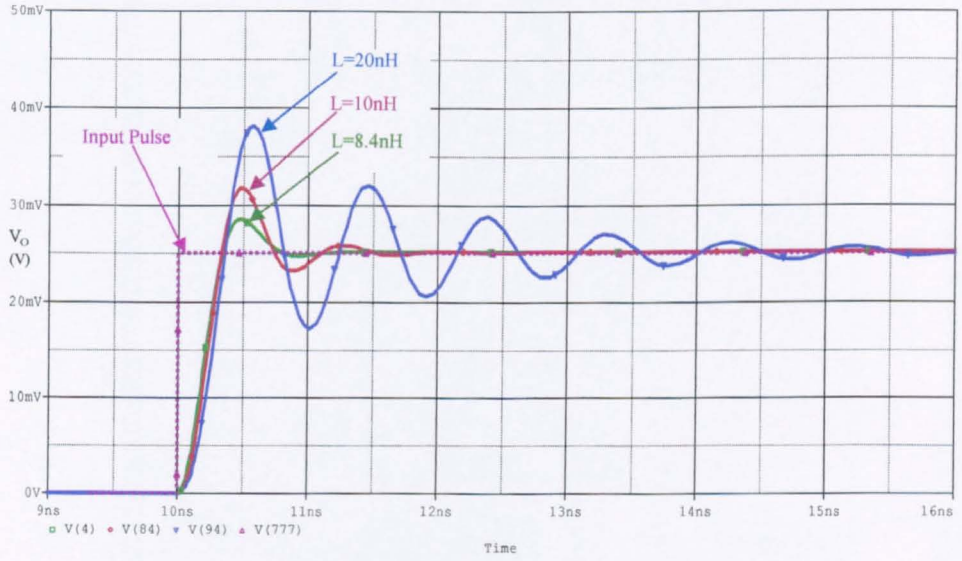


Fig. 4.25 Transient simulation result when a step input is applied

4.7 Emitter-follower distortion

Any difference between the shape of the output signal and input signal in a nominally linear system is considered to be distortion. This may be due to an inadequate frequency response of the system, causing the Fourier frequency components of the input signal waveform to be processed differently from one another. This can be minimised by maximising the bandwidth.

It may also be due to the non-linear nature of the transfer characteristic of the active device(s) in the signal path, in which case it is called non-linear distortion **[4-8]**. Examining, for instance, a typical $i_C - u_{BE}$ characteristic of a transistor, as shown in Figure 4.26, it can be seen that applying a sinusoidal signal in the input of the transistor, will cause a sharpening on the top part and a flattening on the bottom part, which results in generation of distortion.

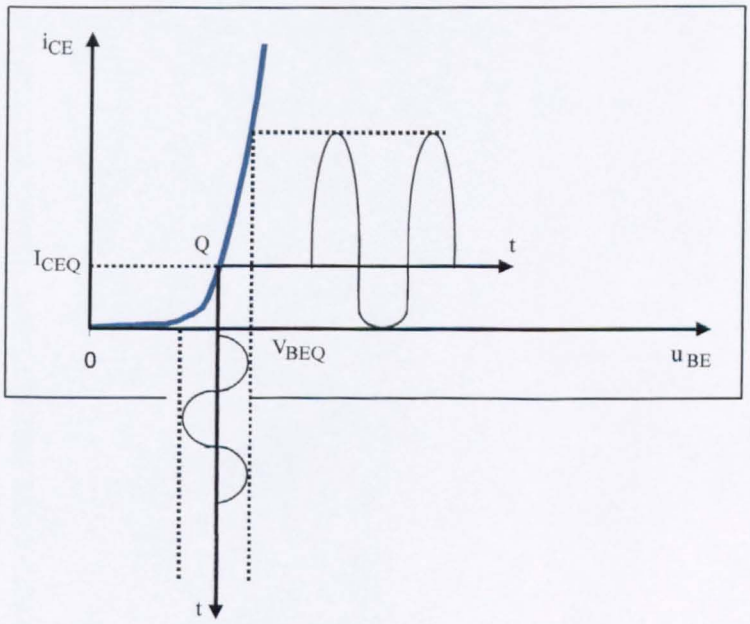


Fig. 4.26 The nonlinear $i_C - u_{BE}$ characteristic

Harmonic distortion (HD) characterises the distortion that arises through the generation of harmonics of the input signal frequency when a single sinusoidal signal is applied to a non-linear device. Intermodulation distortion (IMD) characterises the distortion that rises when two equal in amplitude sinusoidal of frequency ω_1, ω_2 are applied to a non-linear device, giving rise to output signal components of all combinations of ω_1, ω_2 and their multiples. IMD is related to HD, as it will be seen later.

4.7.1 Total harmonic distortion (THD)

When a small signal low frequency voltage, V_{be}, is applied to the base-emitter junction of a BJT in which the current is I, then the output current is given by,

$$i = Ie^{\frac{V_{be}}{V_T}} \tag{4.71}$$

$$i = I\left[\left(\frac{V_{be}}{V_T}\right) + \frac{1}{2}\left(\frac{V_{be}}{V_T}\right)^2 + \frac{1}{6}\left(\frac{V_{be}}{V_T}\right)^3 + ...\right] \tag{4.72}$$

If V_{be} is a sinusoidal with peak value $\hat{V}_{be}$ then,

$$i = I\left[\left(\frac{\hat{V}_{be}}{V_T}\right)\sin\omega t + \frac{1}{2}\left(\frac{\hat{V}_{be}}{V_T}\right)^2 \sin^2\omega t + \frac{1}{6}\left(\frac{\hat{V}_{be}}{V_T}\right)^3 \sin^3\omega t + ...\right] \tag{4.73}$$

By definition **[4-8]** for weak inversion,

HD_2 = amplitude of the 2nd harmonic / amplitude of fundamental

Hence,

$$HD_2 = \frac{1}{4}\left(\frac{\hat{V}_{be}}{V_T}\right) \approx \frac{1}{4}\left(\frac{i_{pk}}{I}\right) \tag{4.74}$$

Similarly,

HD_3 = amplitude of the 3nd harmonic / amplitude of fundamental

Hence,

$$HD_3 = \frac{1}{24}\left(\frac{\hat{V}_{be}}{V_T}\right)^2 \approx \frac{1}{24}\left(\frac{i_{pk}}{I}\right)^2 \tag{4.75}$$

For standard feedback theory the distortion is reduced by a factor (1+T), $T(=g_m R_E)$ being the loop-gain factor associated with the EF **[4-8]**. So,

$$HD_2 \approx \frac{1}{T} \cdot \frac{1}{4}\left(\frac{i_{pk}}{I}\right) \tag{4.76}$$

and

$$HD_3 \approx \frac{1}{T} \cdot \frac{1}{24}\left(\frac{i_{pk}}{I}\right)^2 \tag{4.77}$$

The total harmonic distortion, THD is then given by,

$$THD = \sqrt{HD_2{}^2 + HD_3{}^2 + \ldots} \tag{4.78}$$

Simulation measurements were made and the results are recorded below, in Table 4.5. The calculations show the general agreement between the theory above and the simulated results.

For $I_C = 1mA$, $V_{in} = 1V_p$ and $R_L = 5K\Omega$, substituting in (4.76) and (4.77) respectively,

$$HD_2 \approx \frac{1}{T} \cdot \frac{1}{4}\left(\frac{i_{pk}}{I}\right) = \frac{1}{g_m R_E} \cdot \frac{1}{4}\left(\frac{i_{pk}}{I}\right) = \frac{1}{194} \cdot \frac{1}{4}\left(\frac{0.2}{1}\right) = -71.8dB$$

and

$$HD_3 \approx \frac{1}{T} \cdot \frac{1}{24}\left(\frac{i_{pk}}{I}\right)^2 = \frac{1}{g_m R_E} \cdot \frac{1}{24}\left(\frac{i_{pk}}{I}\right)^2 = \frac{1}{194} \cdot \frac{1}{24}\left(\frac{0.2}{1}\right)^2 = -101dB$$

Combining HD_2 and HD_3 by the following formula gives the THD

$$THD \approx \sqrt{HD_2{}^2 + HD_3{}^2} \approx -71.77dB$$

The simulation results indicated THD of -72.5dB, in fair agreement with the hand calculations, of -71.77dB.

Conditions	**THD (dB) at 312.5KHz**					
Operating temperature (°C)	**-20**		**27**		**100**	
Current source used	Ideal	'6-pack'	Ideal	'6-pack'	Ideal	'6-pack'
$Z_L = 5K\Omega$	-74.1	-73.4	-72.6	-72.5	-71	-70.6
$Z_L = 5K\Omega // 5pF$	-72.3	-64.3	-72.5	-64.5	-69.7	-64.2

Conditions	**THD (dB) at 31.25MHz**					
Operating temperature (°C)	**-20**		**27**		**100**	
Current source used	Ideal	'6-pack'	Ideal	'6-pack'	Ideal	'6-pack'
$Z_L = 5K\Omega$	-73.3	-72.8	-71.9	-71.9	-70.5	-70.2
$Z_L = 5K\Omega // 5pF$	-54.5	-53.3	-53.4	-52.7	-51.8	-51.1

Conditions	THD (dB) at 250MHz					
Operating temperature (°C)	-20		27		100	
Current source used	Ideal	'6-pack'	Ideal	'6-pack'	Ideal	'6-pack'
$Z_L = 5K\Omega$	-51.4	-43	-48.6	-42.7	-45.9	-39.1
$Z_L = 5K\Omega // 5pF$	-37.7	-35.6	-36.8	-35.2	-35.2	-35.1

Table 4.5 THD results for the simple EF as a function of f and T

It is worth noting that at high frequencies, the THD reduces notably, due to the transistor internal capacitances, as well as the output capacitance of the current sink.

4.7.2 Intermodulation distortion (IMD)

The intermodulation distortion is another way of examining the nonlinear distortion of a buffer stage. It has been shown **[4-9]**, that under low-distortion conditions, there is a one-to-one correspondence between the intermodulation distortion and the harmonic distortion, such as,

$$IM_2 = 2HD_2 \tag{4.79}$$

and,

$$IM_3 = 3HD_3 \tag{4.80}$$

Similar to the case of THD, a local feedback loop can decrease the distortion of the design. For a loop-gain greater than 10, the intermodulation components can be written as,

$$IMD_2 \approx \frac{2}{T} \cdot \frac{1}{4}\left(\frac{i_{pk}}{I}\right) \tag{4.81}$$

and,

$$IMD_3 \approx \frac{2}{T} \cdot \frac{1}{24}\left(\frac{i_{pk}}{I}\right)^2 \tag{4.82}$$

where i_p is the relative current swing as described in the previous paragraph and T is the loop-gain which is equal to $g_m R_E$ or $g_m r_o$, respectively, for a resistive load or a transistor current sink as a load.

For $I_C = 1mA$, $V_{in1,2} = 1V_p$ and $R_L = 5K\Omega$, substitution in (4.81) and (4.82) respectively, gives,

$$IMD_2 \approx \frac{2}{g_m R_E} \cdot \frac{1}{4}\left(\frac{i_{pk}}{I}\right) = \frac{2}{194} \cdot \frac{1}{4}\left(\frac{0.2}{1}\right) = -65.7dB$$

and

$$IMD_3 \approx \frac{3}{g_m R_E} \cdot \frac{1}{24}\left(\frac{i_{pk}}{I}\right)^2 = \frac{3}{194} \cdot \frac{1}{24}\left(\frac{0.2}{1}\right)^2 = -91.7dB$$

The simulation results, shown in Table 4.6, indicated IMD of -62.6dB, in fair agreement with the hand calculations, only when ideal current sink used. The non-ideal sink ('6-pack') deteriorates notably the performance of the configuration due to the output capacitance, especially at higher frequencies.

Conditions	**IMD (dB)**					
Operating temperature (°C)	**-20**		**27**		**100**	
Current source used	Ideal	'6-pack'	Ideal	'6-pack'	Ideal	'6-pack'
f = 312.5KHz	-62.5	-52.3	-62.6	-52.1	-62.5	-51.4
f = 31.25MHz	-58.8	-54.1	-57.3	-54.6	-55.4	-55.5
f = 250MHz	-54.4	-49.4	-52.6	-48.3	-50	-48.3

Table 4.7 IMD results for the simple EF as a function of f and T.

4.8 Noise performance

A noise specification was not given for this thesis but for the sake of completeness measurements were made to indicate the level of noise likely to occur in the circuits investigated. This section considers the noise performance of the emitter-follower but detailed comments are not made for subsequent circuits.

Internally and externally generated spurious signals define the minimum amplitude signal that can be used in a circuit. The external noise, which is created from supply ripple, cross-talk, etc, can be modelled by voltage or current sources, in an equivalent circuit. The internal noise, which consists primarily of thermal, shot and flicker noise can be represented as input referred voltage **[4-10]**. Since the follower output is taken from the emitter, which is a low impedance point, the noise due to the output load is attenuated compared with the rest of the noise sources **[4-11]**, and can be omitted. Thermal noise is caused by the mobility of the charge-carriers in the transistor and is proportional to the operating temperature. The shot noise depends on the operating current and is generated in the junctions of the transistor. Flicker noise is caused by surface defects in the semiconductor which arise during the construction process and mainly affect the transistor at low frequencies.

When a transistor is voltage driven, the input noise is given by,

$$\overline{du_{eq}^2} = 4kT\left(r_b + \frac{1}{2g_m}\right)df \qquad (4.83)$$

where du_{eq}^2 is a representation of all noise sources of the transistor

Substituting the values for 1mA operating current, at 27°C, the equivalent input noise is,

$$\overline{du_{eq}^2} = 4kT\left((165) + \frac{1}{2\frac{I_C}{V_T}}\right)df = 2.947 \cdot 10^{-18}\,V^2/Hz$$

which corresponds to,

$$\overline{du_{eq}} = 1.716 \cdot 10^{-9}\,V/\sqrt{Hz}$$

At -20°C the equivalent input noise is,

$$\overline{du_{eq}} = 1.576 \cdot 10^{-9}\,V/\sqrt{Hz}$$

At 100°C the equivalent input noise is,

$$\overline{du_{eq}} = 1.914 \cdot 10^{-9}\,V/\sqrt{Hz}$$

Simulation of the conventional emitter-follower gave the input noise results, shown in Figure 4.27, in good agreement with the calculations.

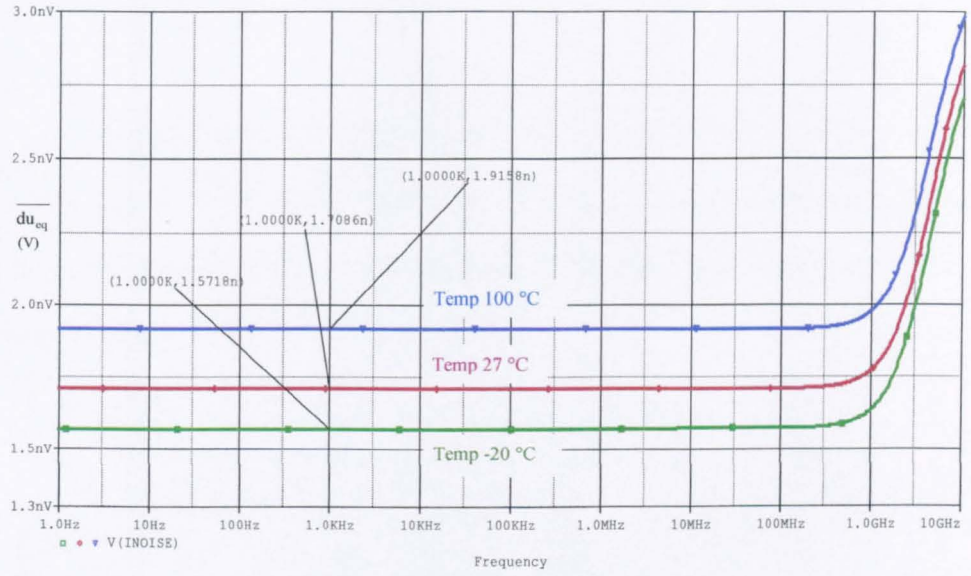


Fig. 4.27 Input noise of the circuit of Figure 4.1

4.9 Pulse response

An approximate analysis of the transient response of an EF, often ignored in textbooks, can be carried out using the charge-control approach pioneered by Beaufoy and Sparkes in 1957 **[4-12]**. A starting point for the charge-control model of a BJT is shown in Figure 4.28.

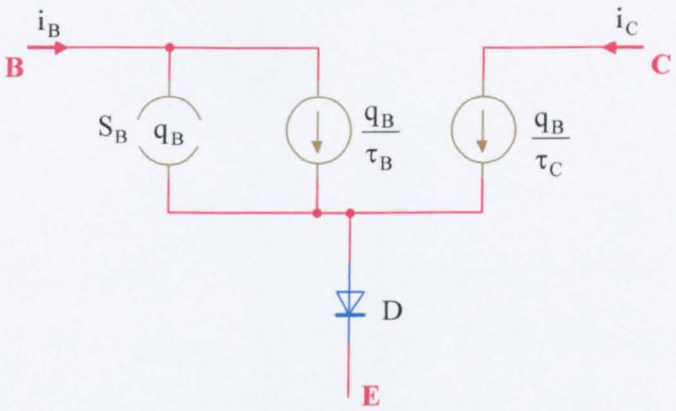


Fig. 4.28 Core of the charge-control model of a BJT

In this S_B is a store for the minority carrier charge q_B in transit across the base region. S_B requires a current (dq_B/dt) to change the collector current but there is no potential drop across it: q_B/τ_B is the component of base current due to base current recombination and the current injected from the base bulk into the emitter region: (q_B/τ_C) it the resulting collector current.

Thus,

$$i_B = \left(\frac{dq_B}{dt}\right) + \frac{q_B}{\tau_B} \tag{4.84}$$

and,

$$i_C = \frac{q_B}{\tau_C} \tag{4.85}$$

Under DC conditions $(dq_B/dt) = 0$ so,

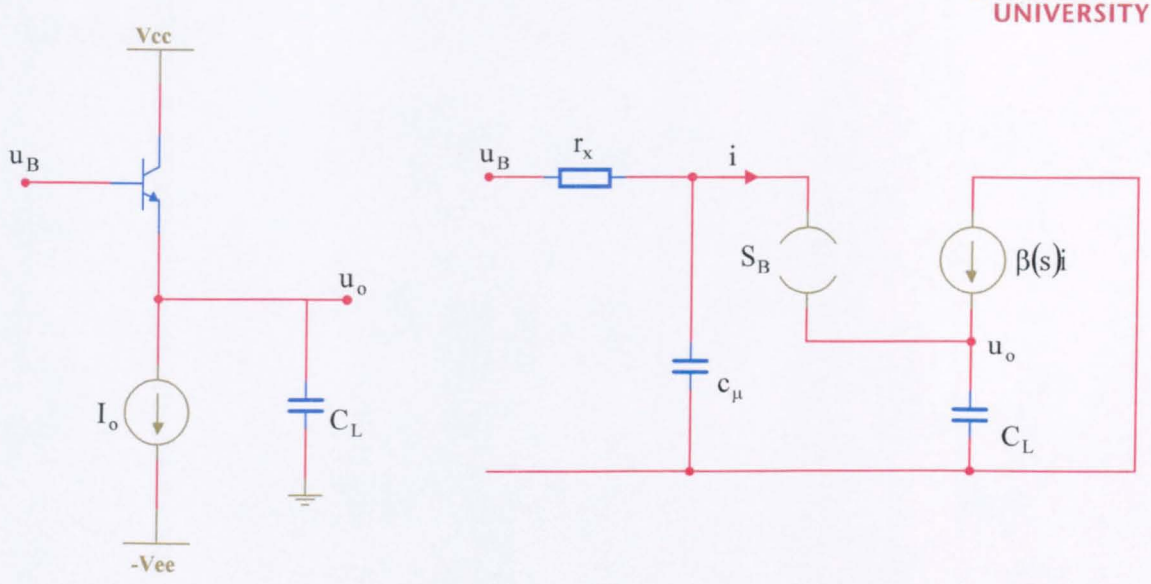
$$\frac{i_C}{i_B} = \frac{\tau_B}{\tau_C} = \beta_o \tag{4.86}$$

In Laplace transform symbolism,

$$\beta(s) = \frac{i_C}{i_B} = \frac{1}{\frac{1}{\beta_o} + s\tau_C} \tag{4.87}$$

The base-emitter drop is modelled by the diode D which is 'ideal' in that it has no other properties than its I-V characteristic. For most practical purposes it can be modelled by a battery since a doubling in collector current is produced by a V_{BE} change of some 18mV which is negligible compared with the voltage change, associated with large signal operation. In an equivalent circuit for changes in circuit conditions batteries are replaced by short-circuits.

Hence, an appropriate circuit for calculating the transient response of circuit of Figure 4.29(a) is shown in Figure 4.29(b) in which r_x is the extrinsic base resistance and c_μ is the collector-base capacitance.



(a) (b)

Fig. 4.29 (a) The basic EF with a capacitive load, and (b) an equivalent circuit of Figure (a)

By inspection,

$$i = [(u_b - u_o)/r_x] - sc_\mu u_o \tag{4.88}$$

To simplify matters it is assumed that the collector current is always much greater than the base current, i.

Then, the current charging C_L is $\beta(s)i$,

Hence,

$$\beta(s)i = sC_L u_o \tag{4.89}$$

Substituting for $\beta(s)$ from (4.90) and i from (4.91) results in,

$$\frac{1}{\left[\left(\frac{1}{\beta_o}\right) + s\tau_C\right]}\left[\frac{(u_b - u_o)}{r_x} - sc_\mu u_o\right] = sC_L u_o \tag{4.90}$$

Rearranging this,

$$\frac{(u_b - u_o)}{r_x} = s\left[c_\mu + \left(\frac{C_L}{\beta_o}\right)\right] + s^2 C_L \tau_C \tag{4.91}$$

Let,

$$\left[c_\mu + \left(\frac{C_L}{\beta_o}\right)\right] = C_k \text{, say}$$

Then,

$$u_b = u_o\left(1 + sC_k r_x + s^2 C_L r_x \tau_C\right) \tag{4.92}$$

or,

$$u_o = \frac{u_b}{\left(1 + sC_k r_x + s^2 C_L r_x \tau_C\right)} \tag{4.93}$$

Now, if u_o has a dominant pole (and associated dominant time constant) it is given by ignoring the s^2 term in the denominator of (4.93). The validity of this assumption must be examined later. Hence,

$$u_o \approx \frac{u_b}{C_k r_x\left(s + \frac{1}{C_k r_x}\right)} \tag{4.94}$$

To proceed further it is necessary to decide on the nature of u_b. Suppose it has the form of a truncated ramp voltage as shown in Figure 4.30(a). The component parts of the leading edge are shown in Figure 4.30(b).

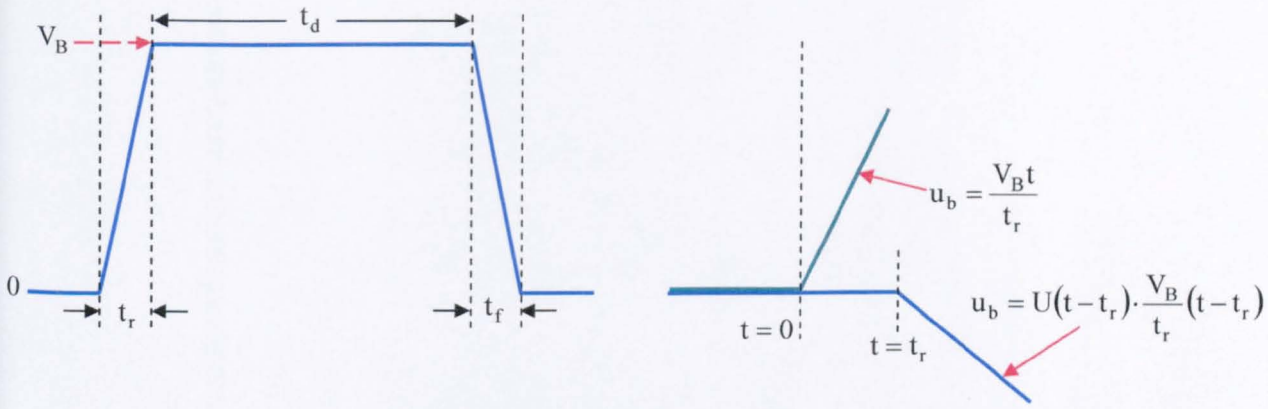


Fig. 4.30 (a) Assumed input voltage signal, and
(b) components of the leading edge

Consider, first, the rising edge. For this,

$$u_b = \frac{V_B t}{t_r} \tag{4.95}$$

In the 's' domain,

$$u_b = \frac{V_B t}{t_r} \cdot \frac{1}{s^2} \tag{4.96}$$

Substituting this into (4.93),

$$u_o = \frac{V_B}{t_r} \cdot \frac{1}{C_k r_x} \cdot \frac{1}{s^2\left(s + \frac{1}{C_k r_x}\right)} \tag{4.97}$$

Using a table of Laplace Transforms, this gives,

$$u_o = \frac{V_B}{t_r}\left[(C_k r_x)e^{-\frac{t}{C_k r_x}} + (t - C_k r_x)\right] \tag{4.98}$$

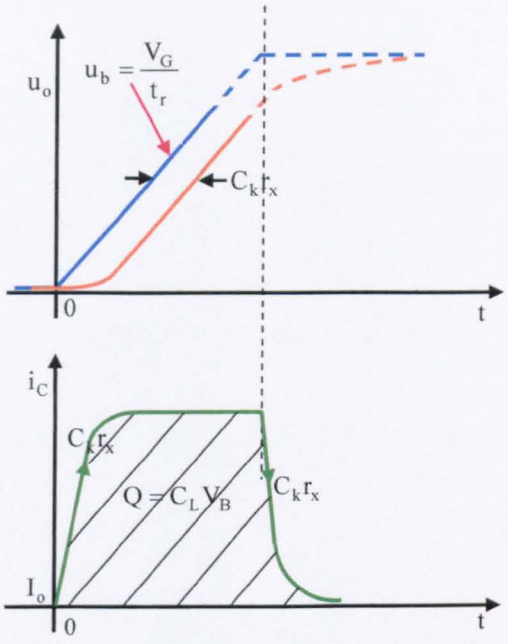


Fig. 4.31 (a) Showing u_b, u_o, for $t_r \geq t \geq 0$, and
(b) Showing i_C for $t_r \geq t \geq 0$

For $t_r > t >> C_k r_x$, u_o has the form of a ramp delayed by a time interval $C_k r_x$ with respect to the input ramp. For $(t_r + t_d) > t > t_r$, u_o changes with a time constant $C_k r_x$, till it reaches a steady value V_B.

The collector current charging C_L is given by,

$$i_C(s) = sC_L u_o \tag{4.99}$$

Hence, from (4.96)

$$i_C(s) = \frac{C_L V_B}{t_r} \cdot \frac{1}{C_k r_x} \cdot \frac{1}{s\left(s + \frac{1}{C_k r_x}\right)} \tag{4.100}$$

for which,

for $t_r > t > 0$,

$$i_C(t) = \frac{C_L V_B}{t_r} \cdot \left(1 - e^{-\frac{t}{C_k r_x}}\right) \tag{4.101}$$

For $t > t_r$,

$$i_C(t) = \frac{C_L V_B}{t_r} \cdot u(t - t_r) e^{-\frac{(t-t_r)}{C_k r_x}} \tag{4.102}$$

where $u(t - t_r)$ is the delayed Heaviside input step function **[4-13]**

For $t_r > t > 0$, $u(t - t_r) = 0$

For $t > t_r$, $u(t - t_r) = 1$

Integrating (4.101) w.r.t. t for the interval $t = 0$ to $t = t_r$, bearing in mind that, $t_r >> 5C_k r_x$, and adding the result to the integral of (4.102) for the time range $t = t_r$ to $t = \infty$ gives the charge Q, shown shaded in Figure 4.31(b). This is in the assumption that $i << i_C$ at all times.

The simulated waveforms of Figure 4.32, were obtained to test the applicability of the theory just presented. The base-line for u_B was offset so that the base-line for u_o was zero: $t_r = t_f = 1ns$; $t_d = 3ns$; $V_B = 0.5V$. For the input edge of u_B the waveform for u_o has the general shape predicted, the ramp delay being in the order of 0.2nS. The waveforms for i_C, capacitor current and i_B, are all similar in shape and appear to have exponential changes associated with them. An estimate of the area under the curve for capacitor current (equal to the sum of areas under the

curves for collector current and base current), found by the squares in Figure 4.32, is

$$1nS \times 2.5mA = 2.5pC$$

corresponding to the charge accumulated by the 5pF load capacitor when its voltage changes by 0.5V.

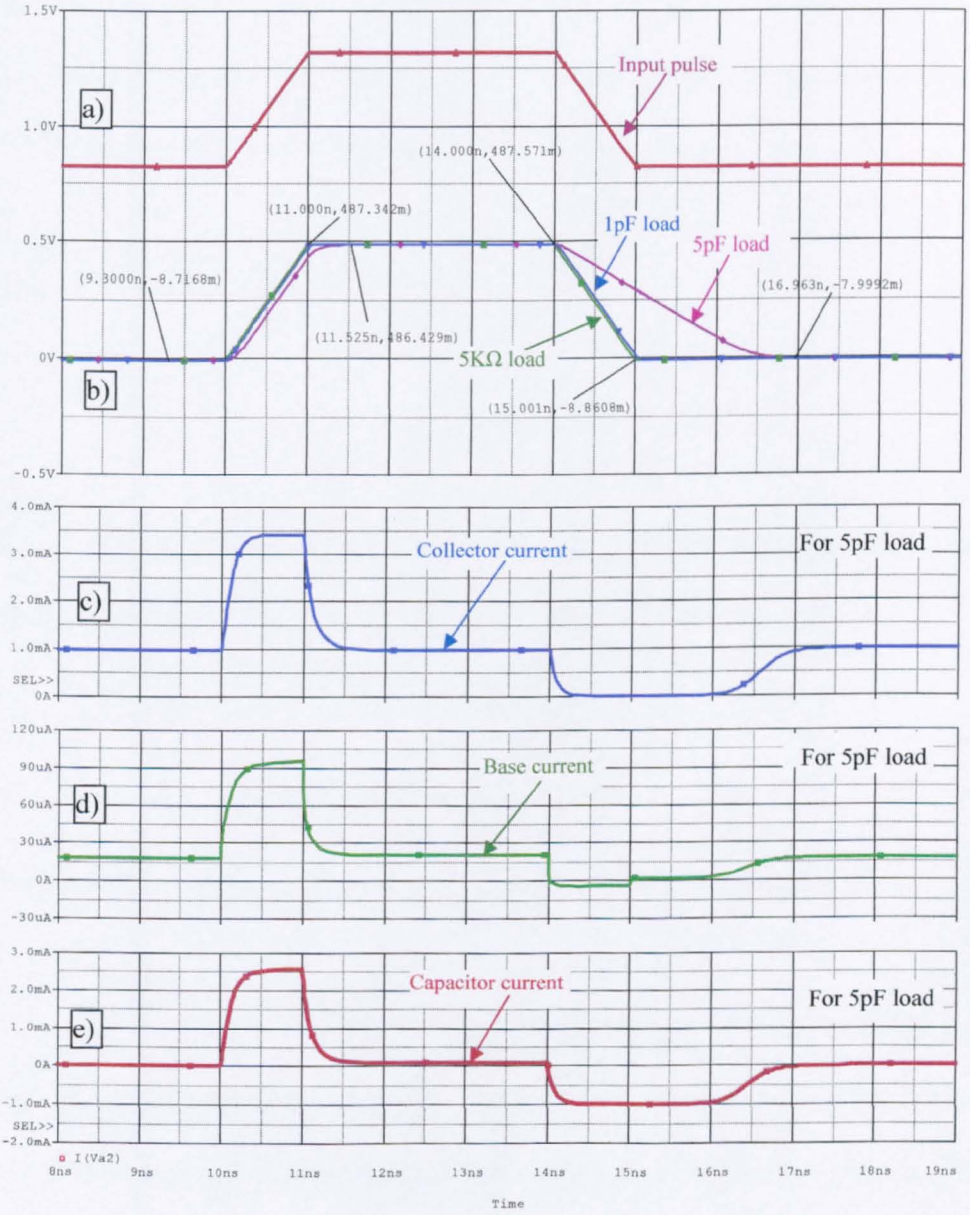


Fig. 4.32 Waveforms for the circuit of Figure 4.29 for 1nS input edges

(a) u_B ; (b) u_o ; (c) i_C ; (d) i_B and (e) Capacitor current

Since i_C reaches its peak value in about 1nS it means that $5C_k r_x = 1nS$, i.e, $C_k r_x = 0.2nS$, in agreement with the delay for u_o in (b): the theoretical value for $C_k r_x$, using the values $r_x \approx 165\Omega$, $c_\mu = 30fF$, $C_L = 5pF$ and $\beta_o = 50$, is 0.21nS. The agreement is unexpectedly good because: c_μ varies with V_{CB}, during the rise edge; β_o is not the same at $I_C = 3.5mA$ as at $I_C = 1mA$; r_x has a different value, from its DC value, under pulse conditions. Safe engineering calculations would assume a maximum value of c_μ and a minimum value of β_o.

At $t = (t_r + t_d)$, the transistor cuts off if,

$$\frac{V_B}{t_f} > \frac{I_o}{C_L} \tag{4.103}$$

This is the case for the 5pF load shown in Figure 4.32(a). As indicated in Figure 4.32(c), i_C falls to zero and I_o discharges C_L so that, for $t > (t_r + t_d)$,

$$u_o \approx V_B - \left(\frac{I_o}{C_L}\right)t \tag{4.104}$$

The discharge time for C_L is approximately 2.5ns, as expected from calculation.

For $(t_r + t_d + t_f) > t > (t_r + t_d)$, the base current reverses as the base charge store $(I_o \tau_C)$ is discharged. However, when $(u_B - u_o)$ is equal to the base-emitter threshold-of-conduction voltage the transistor commences conduction. This is not a sudden process because the collector current is shared between the transistor and C_L.

That accounts for the non-linearity of the curves for i_B and i_C before the transistor reaches its initial d.c. state.

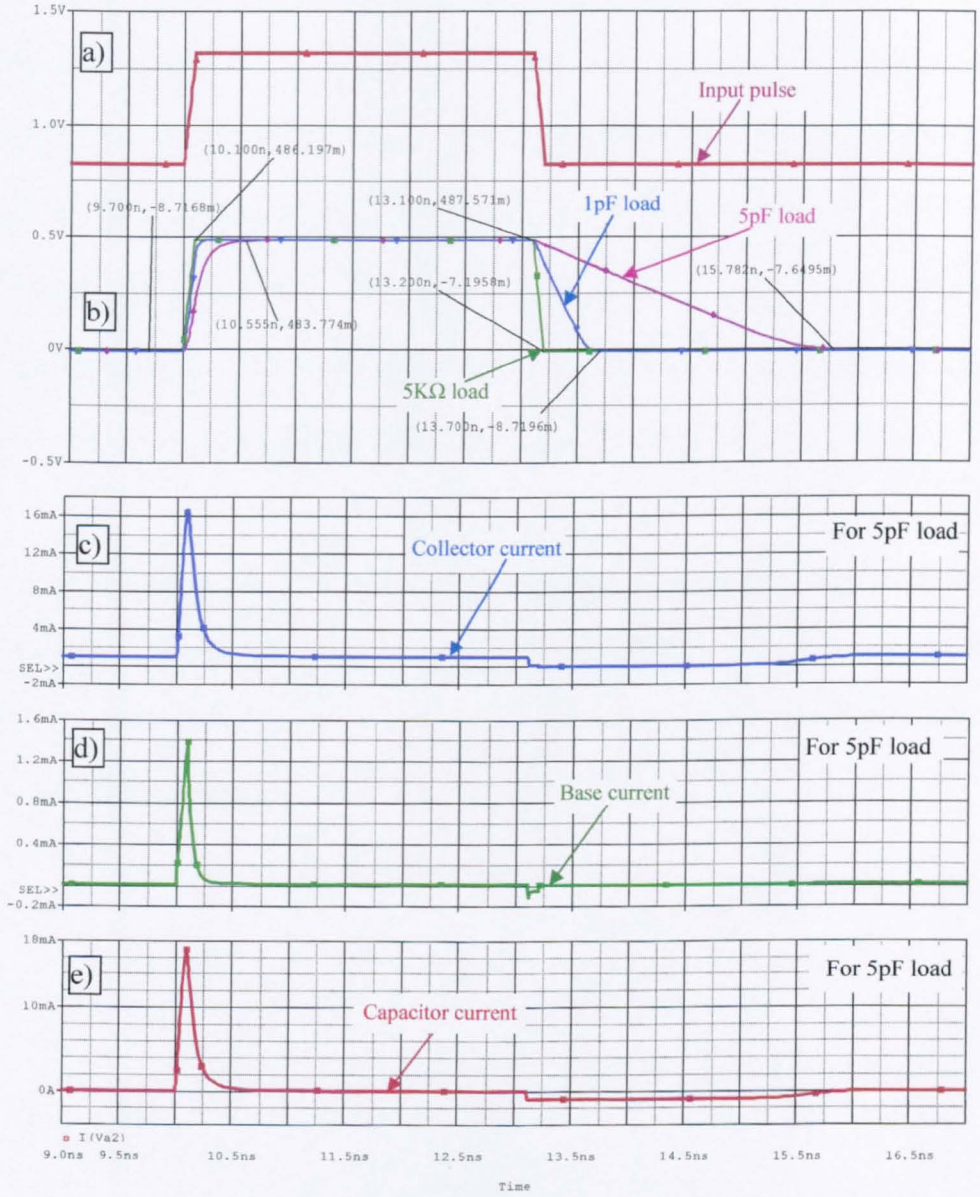


Fig. 4.33 Waveforms for the circuit of Figure 4.29 but, here, for 0.1nS input waveform edges

Figure 4.33, which should be compared with Figure 4.32, shows transient responses for 0.1nS waveform edges. In this case $t_r, t_f < 5C_k r_x$ so there is no flat

top to the waveforms for the capacitor current and i_B.

Accurate prediction of rise and fall times and current maximum amplitudes is not simple. (In practice, it is necessary to ensure from the simulation plots that the transistor does not exceed its $i_{C(max)}$ and $P_{C(max)}$ in the event of small values of t_r, t_f and large values of C_L). However, as an approximation, it might be considered that u_B had ideal step edges in which case u_o shows an exponential rise for the leading edge of u_B. It is significant that u_B does, in fact, reach its maximum value in about 1ns, corresponding to the value given by $5C_k r_x$.

Before leaving the topic of large signal response, it follows that the Slew Rate, which determines the maximum sinusoidal output voltage at a given frequency, is limited by the product $C_k r_x$ or the ratio I_o / C_L, whichever give the greater value for rise and fall times for u_o.

4.10 Summary of Chapter 4

In this chapter the author has analysed the conventional EF in terms of DC performance as well as low-frequency and high-frequency small-signal performance. The treatment undertaken was extensive, compared to the treatment given in textbooks, therefore the analysis presented in this chapter is thought to be original. The attention paid in the investigation of the conventional EF is essential for the analysis of the proposed designs, presented in the following chapters, since it comprises the root of each novel circuit. In addition, this chapter set the benchmark for the analysis of the proposed circuits. The following chapters have been structured in a similar manner to allow a clear insight into the performance of each proposed design and their relative superiority over the conventional EF.

References for Chapter 4

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[4-2] Spencer R.R., Ghausi S.M., 'Introduction to Electronic Circuit Design', Prentice Hall, USA, 2003, pp.564-570

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APPENDIX 4

AP4.1 Calculation of the frequency response of the EF

AP4.2 Analysis of the input impedance

AP4.3 Input impedance simulation results

AP4.4 Investigation of the effect of C_L on f_B - Simulation results

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Appendix AP4.1

Calculation of the frequency response of the EF

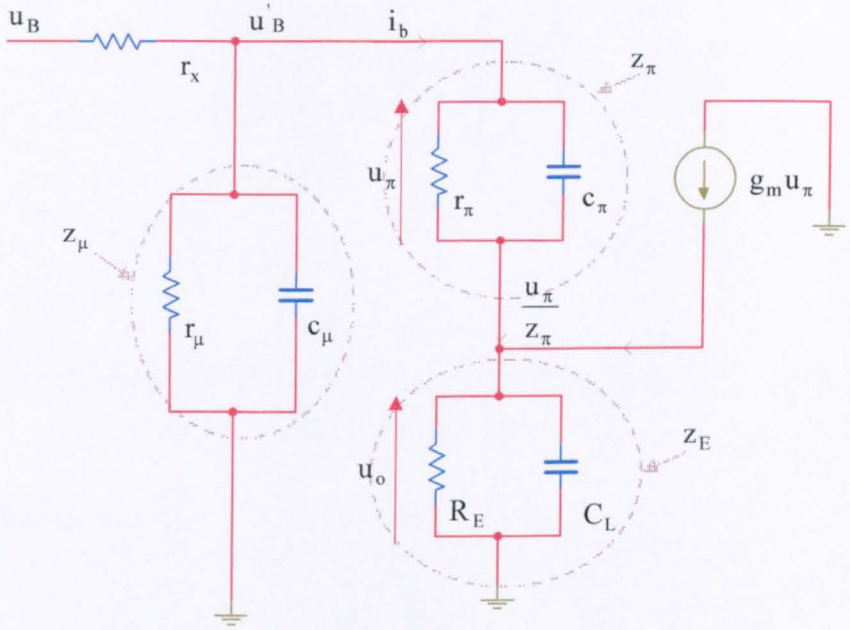


Fig. A4.1 Small-signal equivalent circuit of the EF

By inspection of Figure A4.1

$$u'_B = u_\pi + u_o \tag{A4.1}$$

where,

$$u_o = \left(\frac{u_\pi}{z_\pi} + g_m u_\pi\right) z_E = u_\pi \left(\frac{1}{z_\pi} + g_m\right) z_E \tag{A4.2}$$

Thus,

$$G = \frac{u_o}{u_B} = \frac{u_\pi\left(\frac{1}{z_\pi} + g_m\right)z_E}{u_\pi + u_\pi\left(\frac{1}{z_\pi} + g_m\right)z_E} = \frac{\left(\frac{1}{z_\pi} + g_m\right)z_E}{1 + \left(\frac{1}{z_\pi} + g_m\right)z_E} \qquad \text{(A4.3)}$$

$$G(s) = \frac{\left[g_m + \left(\frac{1}{r_\pi} + sc_\pi\right)\right]\left(\frac{R_E}{1 + sC_L R_E}\right)}{1 + \left(g_m + \frac{1}{r_\pi} + sc_\pi\right)\left(\frac{R_E}{1 + sC_L R_E}\right)} \qquad \text{(A4.4)}$$

or,

$$G(s) = \frac{\left(g_m + \frac{1}{r_\pi} + sc_\pi\right)R_E}{(1 + sC_L R_E) + \left(g_m + \frac{1}{r_\pi} + sc_\pi\right)R_E} \qquad \text{(A4.5)}$$

For low frequencies, $s \to 0$

$$\therefore \quad G(o) = \frac{\left(g_m + \frac{1}{r_\pi}\right)R_E}{1 + \left(g_m + \frac{1}{r_\pi}\right)R_E} = \frac{\left(\frac{\beta_o + 1}{r_\pi}\right)R_E}{1 + \left(\frac{\beta_o + 1}{r_\pi}\right)R_E} = \frac{(\beta_o + 1)R_E}{r_\pi + (\beta_o + 1)R_E} \qquad \text{(A4.6)}$$

or,

$$G(o) \approx \frac{g_m R_E}{1 + g_m R_E} \qquad \text{(A4.7)}$$

since $g_m r_\pi = \beta_o >> 1$

In general,

$$G(s) = \frac{\left(g_m + \frac{1}{r_\pi}\right)\left[1 + \frac{sc_\pi}{\left(g_m + \frac{1}{r_\pi}\right)}\right]R_E}{\left[1 + \left(g_m + \frac{1}{r_\pi}\right)R_E + sR_E(C_L + c_\pi)\right]} \qquad \text{(A4.8)}$$

$$G(s)=\frac{\left(g_m+\frac{1}{r_\pi}\right)\left[1+\frac{sc_\pi}{\left(g_m+\frac{1}{r_\pi}\right)}\right]R_E}{\left[1+\left(g_m+\frac{1}{r_\pi}\right)R_E\right]\left[1+\frac{sR_E(C_L+c_\pi)}{1+\left(g_m+\frac{1}{r_\pi}\right)R_E}\right]} \qquad \text{(A4.9)}$$

since $g_m r_\pi=\beta_o >>1$

$$G(s)\approx\frac{\left(g_m+\frac{1}{r_\pi}\right)\left[1+\frac{sc_\pi}{g_m}\right]R_E}{\left[1+\left(g_m+\frac{1}{r_\pi}\right)R_E\right]\left[1+\frac{sR_E(C_L+c_\pi)}{1+g_mR_E}\right]} \qquad \text{(A4.10)}$$

This means a zero at,

$$\omega=\omega_z=\frac{g_m}{c_\pi} \qquad \text{(A4.11)}$$

and a pole at,

$$\omega=\omega_p=\frac{(1+g_mR_E)}{R_E(C_L+c_\pi)} \qquad \text{(A4.12)}$$

But,

$$g_mR_E >>1$$

hence,

$$\omega_p\approx\frac{g_m}{C_L+c_\pi} \qquad \text{(A4.13)}$$

Appendix AP4.2

Analysis of the input impedance

In the circuit of Figure 4.10, in the text,

$$u_B'' = u_\pi + u_o \tag{A4.14}$$

where,

$$u_o = \left(\frac{u_\pi}{z_\pi} + g_m u_\pi\right) z_E = u_\pi \left(\frac{1}{z_\pi} + g_m\right) z_E \tag{A4.15}$$

and,

$$u_B'' = u_\pi \left(1 + \frac{z_E}{z_\pi} + g_m z_E\right) \tag{A4.16}$$

$$\therefore \quad z_{b''e}(s) = \frac{u_B''}{\frac{u_\pi}{z_\pi}} = \left(1 + \frac{z_E}{z_\pi} + g_m z_E\right) z_\pi = z_\pi + z_E + g_m z_E z_\pi \tag{A4.17}$$

Substituting for z_E and z_π

$$\therefore \quad z_{b''e}(s) = \frac{r_\pi}{(1 + sc_\pi r_\pi)} + \frac{R_E}{(1 + sC_E R_E)} + \frac{g_m R_E}{(1 + sC_E R_E)} \frac{r_\pi}{(1 + sc_\pi r_\pi)} \tag{A4.18}$$

or,

$$z_{b''e}(s) = \frac{r_\pi (1 + sC_E R_E) + R_E (1 + sc_\pi r_\pi) + g_m R_E r_\pi}{(1 + sc_\pi r_\pi)(1 + sC_E R_E)}$$

$$\therefore \quad z_{b''e}(s) = \frac{r_\pi + R_E (1 + g_m r_\pi) + s(C_E R_E r_\pi + R_E c_\pi r_\pi)}{(1 + sc_\pi r_\pi)(1 + sC_E R_E)}$$

and,

$$z_{b''e}(s) = \left[r_\pi + R_E(1+g_m r_\pi)\right]\frac{\left[1+\dfrac{sR_E r_\pi (C_E + c_\pi)}{r_\pi + R_E(1+g_m r_\pi)}\right]}{(1+sc_\pi r_\pi)(1+sC_E R_E)} \qquad \text{(A4.19)}$$

As $g_m r_\pi = \beta_o >> 1$, where β_o is the l.f. ac current gain of the transistor,

$$(\beta_o + 1)R_E >> r_\pi$$

Hence,

$$\frac{sR_E r_\pi (C_E + c_\pi)}{r_\pi + R_E(1+g_m r_\pi)} \approx \frac{sr_\pi (C_E + c_\pi)}{(1+\beta_o)} \qquad \text{(A4.20)}$$

and,

$$z_{b''e}(s) \approx \frac{\left[r_\pi + R_E(1+\beta_o)\right]\left[1+\dfrac{sr_\pi (C_E + c_\pi)}{(1+\beta_o)}\right]}{(1+sc_\pi r_\pi)(1+sC_E R_E)} \qquad \text{(A4.21)}$$

In the frequency domain,

$$z_{b''e}(j\omega) \approx \frac{\left[r_\pi + R_E(1+\beta_o)\right]\left[1+\dfrac{j\omega r_\pi (C_E + c_\pi)}{(1+\beta_o)}\right]}{(1+j\omega c_\pi r_\pi)(1+j\omega C_E R_E)} \qquad \text{(A4.22)}$$

$$\therefore \quad z_{b''e}(j\varpi) \approx \frac{\left[r_\pi + R_E(1+\beta_o)\right]\left(1+\frac{j\omega}{\omega_z}\right)}{\left(1+j\frac{\omega}{\omega_{p1}}\right)\left(1+j\frac{\omega}{\omega_{p2}}\right)} = \frac{z_{(0)}\left(1+\frac{j\omega}{\omega_z}\right)}{\left(1+j\frac{\omega}{\omega_{p1}}\right)\left(1+j\frac{\omega}{\omega_{p2}}\right)} \qquad \text{(A4.23)}$$

where,

$$\omega_z = \frac{(1+\beta_o)}{(C_E + c_\pi)r_\pi} = \frac{g_m}{(C_E + c_\pi)} \qquad \text{(A4.24)}$$

$$\omega_{p1} = \frac{1}{c_\pi r_\pi} \approx \frac{g_m}{\beta_o c_\pi} \approx \frac{\omega_\tau}{\beta_o} \qquad \text{(A4.25)}$$

and,

$$\omega_{p2} = \frac{1}{C_E R_E} \qquad \text{(A4.26)}$$

Appendix AP4.3

Input impedance simulation results

It will be seen in the coming chapters that the operating current of the proposed circuits is either 1mA or 0.7mA. Both the NPN and PNP versions of EF are simulated at these operating currents as the results are vital in the analysis of the new circuits in the following chapters.

Figure A4.2 shows the input impedance of the EF using an NPN BJT, with $I_C = 0.7mA$. The output was initially unloaded and later made to drive 5KΩ and 1KΩ resistive loads, respectively.

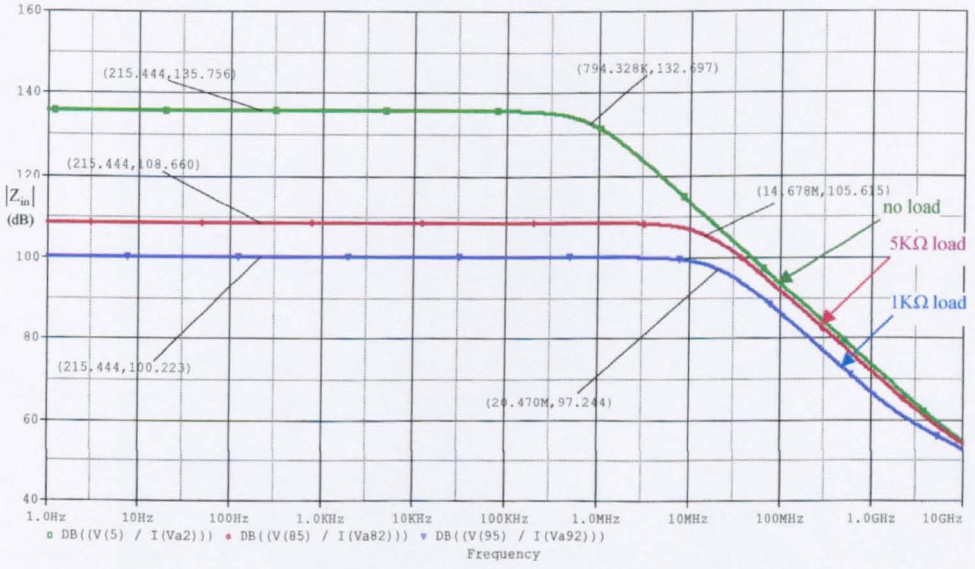


Fig. A4.2 Bode plot for $|Z_{in}|$ for $I_C = 0.7mA$ and an NPN BJT (T=27°C)

Identical tests were made for the PNP version of the EF (Figure A4.3). The input impedance for $I_C = 1mA$ and $I_C = 0.7mA$, is shown in Figures A4.4 and A4.5 respectively. Initially $C_L = 0$ and R_L is infinite and then $R_L = 5K\Omega$ and $R_L = 1K\Omega$.

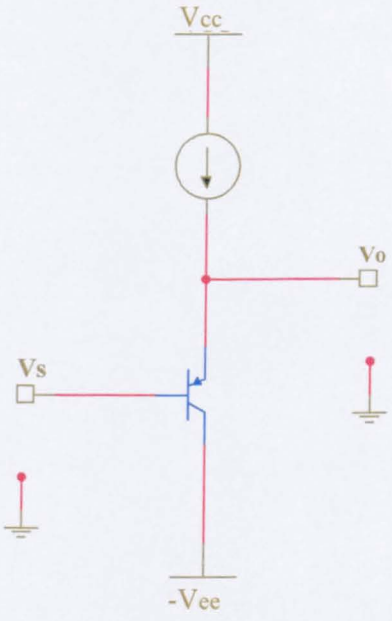


Fig. A4.3 PNP Version of the EF

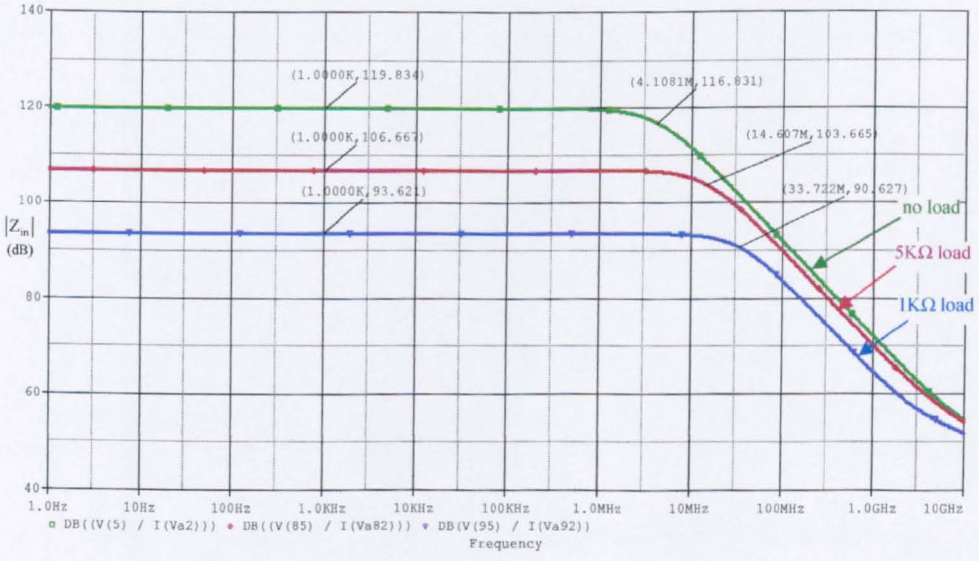


Fig. A4.4 Bode plot for $|Z_{in}|$ for $I_C = 1mA$ and a PNP BJT (T=27°C)

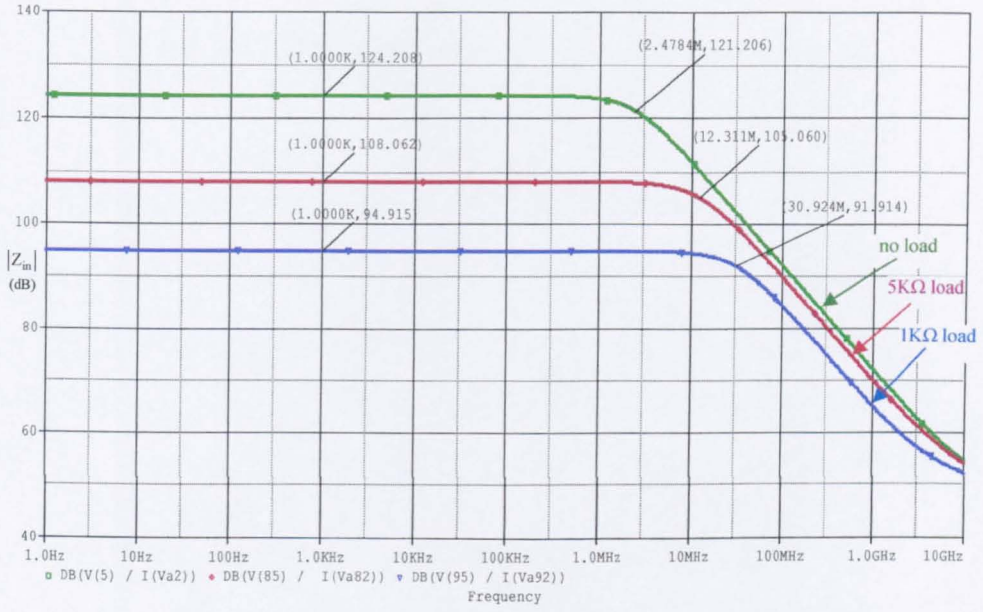


Fig. A4.5 Bode plot for $|Z_{in}|$ for $I_C = 0.7mA$ and a PNP BJT (T=27°C)

Spot values of $|Z_{in}|$, for the PNP version of EF, for $R_L = \infty$ and $R_L = 5K\Omega$ as a function of f and T are given in Table A4.1.

Conditions	$\|Z_{in}\|$ **(Ω)**					
Operating temperature (°C)	**-20**	**27**	**100**	**-20**	**27**	**100**
f = 312.5KHz	758K	978K	1.38M	171K	215K	291K
f = 31.25MHz	126K	127K	128K	88.1K	91.6K	95.3K
f = 250MHz	16.3K	16K	16K	12.8K	12.6K	12.6K
Current source used	Unloaded output			5KΩ load		

Table A4.1 $|Z_{in}|$ of the EF with $R_L = \infty$ and $R_L = 5K\Omega$ as a function of f and T

Appendix AP4.4

Investigation of the effect of C_L on f_B - Simulation results

In this section, the simulation results for the bandwidth of the EF, when using a capacitive load, are presented mainly for reference reasons. It has been shown in section 4.5 that when the EF drives a capacitive load, that load will determine the bandwidth of the circuit. Furthermore, simulation results presented only for $I_C = 1mA$ and for an NPN EF. Figure A4.6 shows the f_B for the NPN BJT, for $I_C = 0.7mA$ and for $C_L = 0$, $C_L = 5pF$ and $C_L = 5pF$ with an extra c_μ.

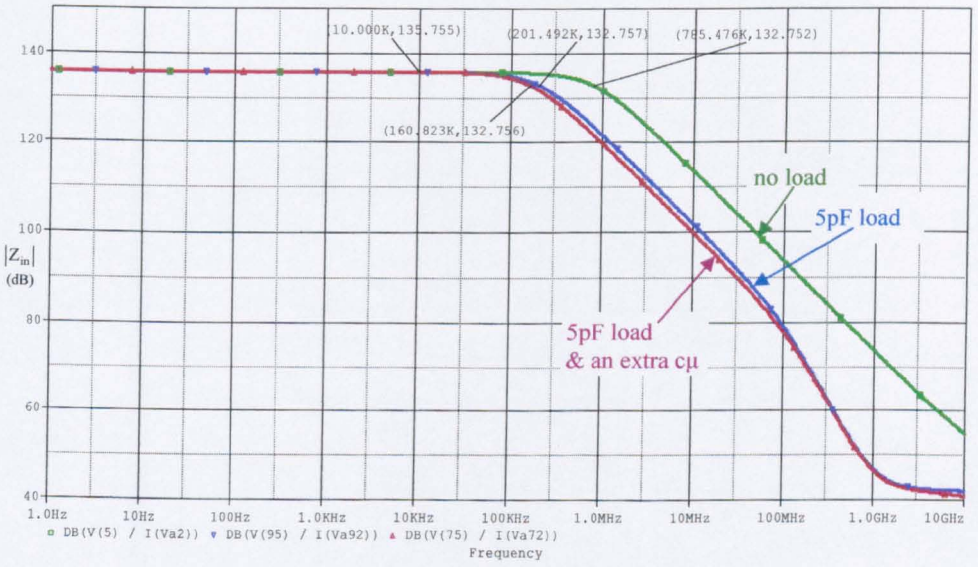


Fig. A4.6 Showing the effect of added C_L on bandwidth for an NPN EF with $I_C = 0.7mA$

Similarly, the PNP version of EF was simulated, using $I_C = 1mA$ and $I_C = 0.7mA$ for the same load conditions as before. Figures A4.7 and A4.8 show the effect on the bandwidth, when driving capacitive loads.

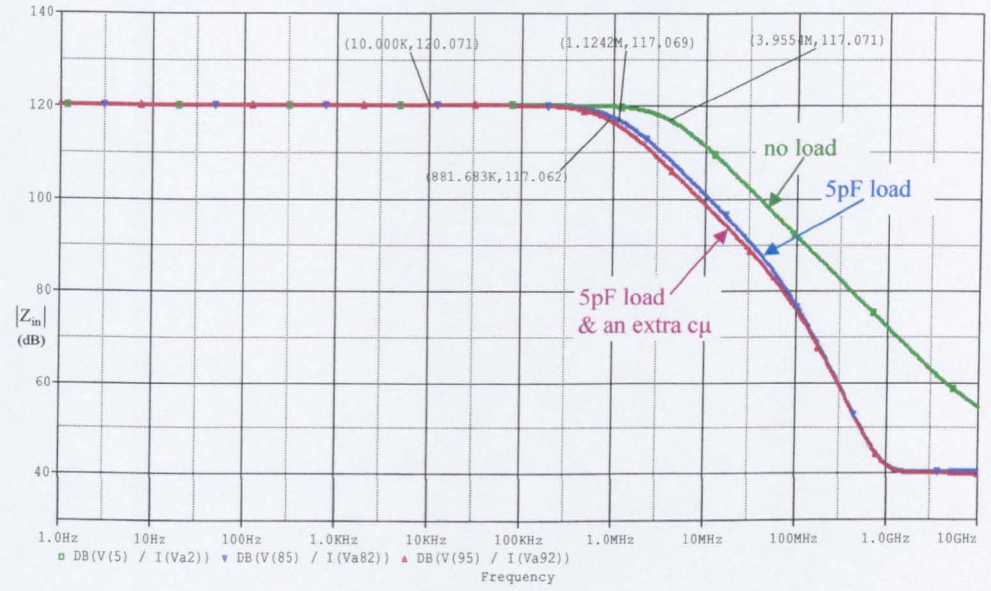


Fig. A4.7 Showing the effect on the PNP EF of added C_L on bandwidth when $I_C = 1mA$

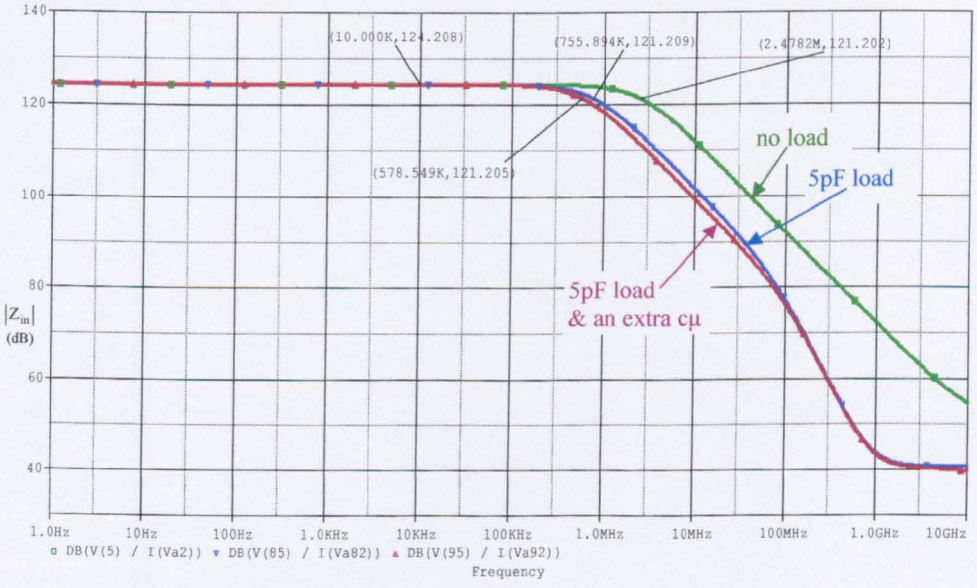


Fig. A4.8 Showing the effect on the PNP EF of added C_L on bandwidth when $I_C = 0.7mA$

CHAPTER 5

V.F. Type A / V.F. with local feedback and single-valued current biasing

5.1 Introduction

Following on from the detailed discussion of the emitter-follower in the previous chapter this chapter describes the evolution and performance of a so-called 'Super-follower' in which emitter followers are extensively used. This Super-follower is, in fact, a class AB high frequency VF based on the original 'LH0002' type buffers developed in the 1970s by National Semiconductors **[5-1]**, **[5-2]**. This circuit has been previously used in the design of IC voltage op-amp output stages, current conveyers and current feedback operational amplifiers. More recently it has been referred to as the 'Diamond' circuit **[5-3]**, a convenient shorthand description that will be used from now on when referring to it.

5.2 The 'Diamond' circuit / DC conditions

The starting point of the proposed design is the circuit shown in Figure 5.1. This is a class AB high frequency VF which has, in the past, been used in the design of current-feedback **[5-3]** operational amplifiers as well as in the first IC current conveyer **[5-4]**. However some features of its operational characteristics (e.g., input impedance) do not appear to have been dealt with in detail in the literature. Since it is the core of the proposed design, the 'Diamond' circuit is considered, critically, first. The simulation results refer to '6-pack' biasing (Figure 5.2), except where indicated.

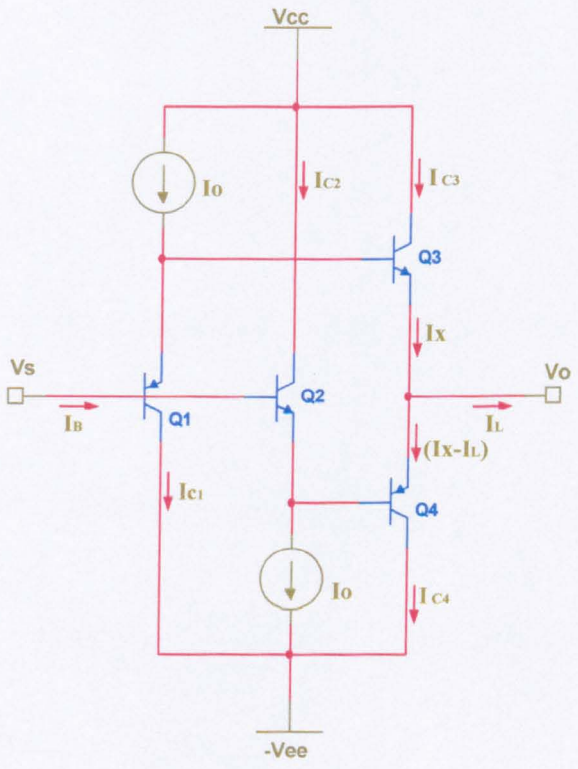


Fig.5.1 The 'Diamond' circuit

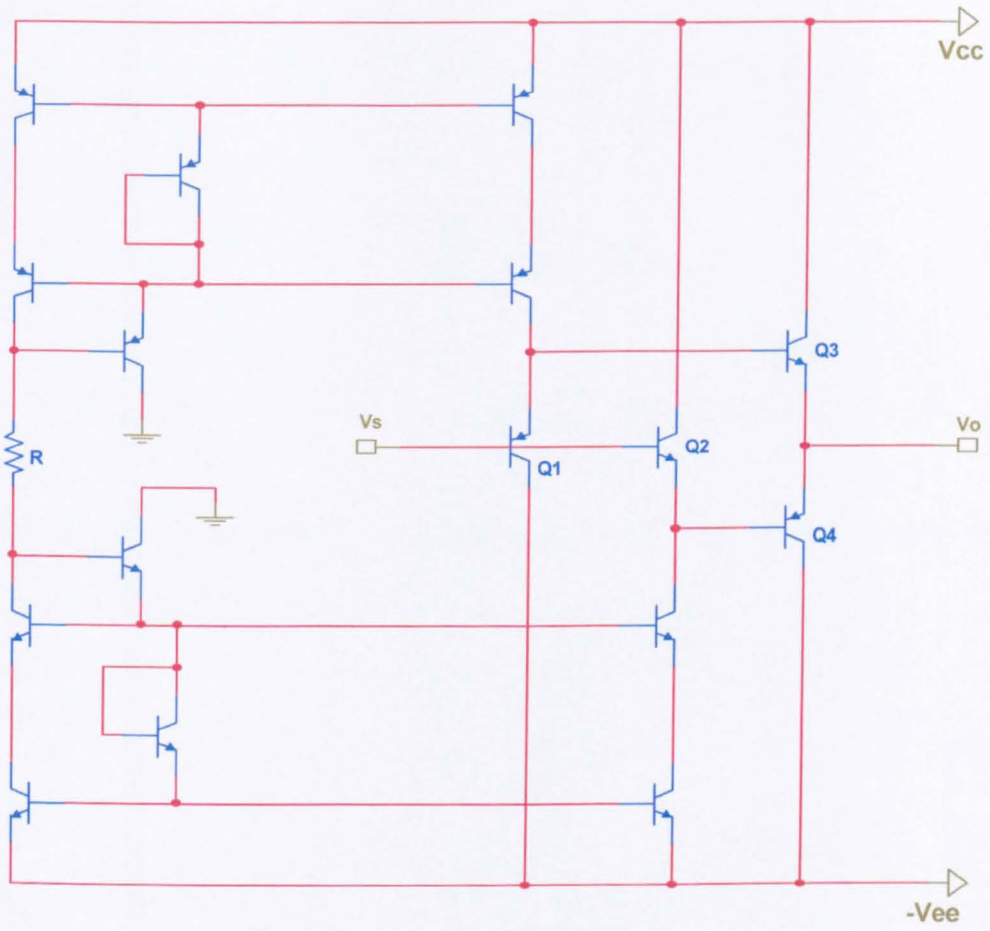


Fig.5.2 The 'Diamond' circuit with '6-pack' biasing

By inspection of Figure 5.1,

$$V_S + V_{EB1} - V_{BE3} = V_S - V_{BE2} + V_{EB4} = V_O \tag{5.1}$$

$$V_{EB1} + V_{EB2} = V_{BE3} + V_{EB4} \tag{5.2}$$

Hence,

$$V_T \log\frac{I_{C1}}{I_{S1}} + V_T \log\frac{I_{C2}}{I_{S2}} = V_T \log\frac{I_{C3}}{I_{S3}} + V_T \log\frac{I_{C4}}{I_{S4}}$$

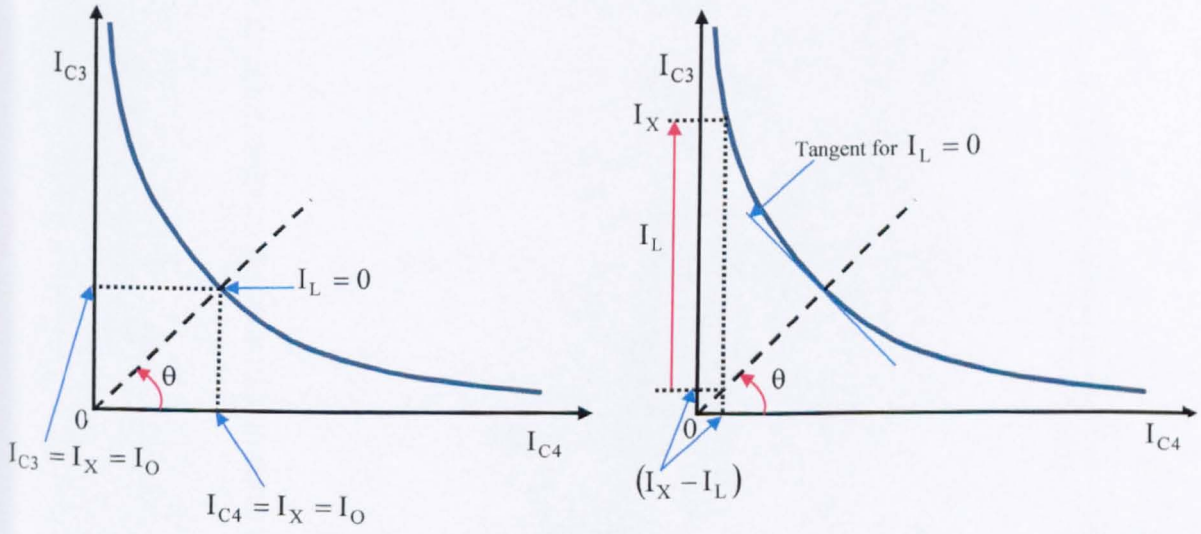
$$\therefore \qquad \frac{I_{C1}I_{C2}}{I_{S1}I_{S2}} = \frac{I_{C3}I_{C4}}{I_{S3}I_{S4}} \qquad (5.3)$$

For well matched BJTs, $I_{S1} = I_{S4}$ and $I_{S2} = I_{S3}$ so for that case, $I_{C3}I_{C4} = I_{C1}I_{C2}$.

To obtain the main properties of the output stage base currents can be ignored, in which case, $I_{C1} = I_O$, $I_{C3} = I_X$, etc.

So,

$$I_X(I_X - I_L) = I_O{}^2 \qquad (5.4)$$



(a) (b)

Fig.5.3 Illustrating DC conditions for Figure 5.1 : $\theta = 45^o$
(a) $I_L = 0$ and (b) $I_L \neq 0$

The rectangular hyperbola in Figure 5.3(a) represents equation (5.4). The condition $I_L = 0$, for which $I_{C3} = I_{C4} = I_O$ is shown. Figure 5.3(b) shows DC conditions for $I_L \neq 0$ and the arbitrarily chosen condition $I_{C3} > I_{C4}$. It is apparent from this graph that if I_L is large compared with I_O then $I_{C3} = I_x \approx I_L$ and $I_{C4} \approx 0$. However, neither I_{C3} nor I_{C4} ever falls completely to zero. Now because $I_{C3}I_{C4} = I_O^2$,

$$\log I_{C3} + \log I_{C4} = 2\log I_O \tag{5.5}$$

Differentiating with respect to I_{C3},

$$\frac{1}{I_{C3}} + \frac{1}{I_{C4}} \cdot \frac{dI_{C4}}{dI_{C3}} = 0 \tag{5.6}$$

Hence,

$$\frac{dI_{C3}}{dI_{C4}} = -\frac{I_{C3}}{I_{C4}} \tag{5.7}$$

For $I_{C4} = I_X = I_O$,

$$\frac{dI_{C3}}{dI_{C4}} = -1 \tag{5.8}$$

Hence if $I_L << I_O$, the changes in I_{C3}, I_{C4} due to a finite I_L are equal and opposite. Thus,

$$I_{C3} \approx I_O + \left(\frac{I_L}{2}\right) \tag{5.9}$$

$$I_{C4} \approx I_O - \left(\frac{I_L}{2}\right) \tag{5.10}$$

This feature of output behaviour is used in the calculations of small signal input and output impedance.

The linear input voltage range depends on the compliances of the current source and sink. Over that range the input current, I_B, is principally determined by Q_1 and Q_2, if $I_L << I_O$, and is given by

$$I_B \approx I_O\left[\frac{1}{(\beta_n+1)}-\frac{1}{(\beta_p+1)}\right] \tag{5.11}$$

or, for the usual case $\beta_n, \beta_p >> 1$

$$I_B \approx I_O\left[\frac{1}{\beta_n}-\frac{1}{\beta_p}\right] \tag{5.12}$$

If $I_L >> I_O$, then from the discussion above,

$I_{C3} \approx I_L$, $I_{C4} \approx 0$, $I_{C1} \approx \alpha_p\left[I_O - \frac{I_L}{\beta_n}\right]$, $I_{C2} \approx \alpha_n I_O$.

Consequently,

$$I_B \approx \frac{\alpha_n I_O}{\beta_n} - \frac{\alpha_p}{\beta_p}\left(I_O - \frac{I_L}{\beta_n}\right) \tag{5.13}$$

$$\approx I_O\left(\frac{1}{\beta_n}-\frac{1}{\beta_p}\right)+\frac{I_L}{\beta_n{}^2} \tag{5.14}$$

The offset voltage, V_{OS}, arises from I_S and I_C mismatches and is given by,

$$V_{OS} = V_{EB1} - V_{BE3} \quad (\text{or, } V_{BE2} - V_{EB4})$$

$$= V_T \log\frac{I_{C1}}{I_{S1}} - V_T \log\frac{I_{C3}}{I_{S3}}$$

or,

$$V_{OS} = V_T \log\left(\frac{I_{C1}}{I_{C3}}\right)\left(\frac{I_{S3}}{I_{S1}}\right) \tag{5.15}$$

The circuit design ensures that the condition $I_{C1} = I_{C3}$ is closely satisfied but $I_{S3} \neq I_{S1}$ because of the different polarities of Q_1 and Q_3. It is this difference that contributes most to V_{OS}. If I_{S3} and I_{S1} differ by, say, as little as 20% then $V_{OS} \approx 5\text{mV}$.

The simulated transfer characteristic (Figure 5.4) of the 'Diamond' circuit appears to have a slope of unity. This is to be expected because, for the case considered, $I_{C1} = I_{C2}(= 0.7\text{mA})$ and $R_L = \infty$,

$$V_O = V_S + V_T \log\left(\frac{I_{S3}}{I_{S1}}\right) \tag{5.16}$$

Hence,

$$\frac{dV_O}{dV_s} = +1 \tag{5.17}$$

This is not quite true because of the small effect of finite Early voltages. This characteristic does not show the extent of the linear input range (considered below). Because of the scales employed the finite V_{OS} does not show up in Figure 5.4. However it is evident in Figure 5.5 which illustrates behaviour in the vicinity of the origin.

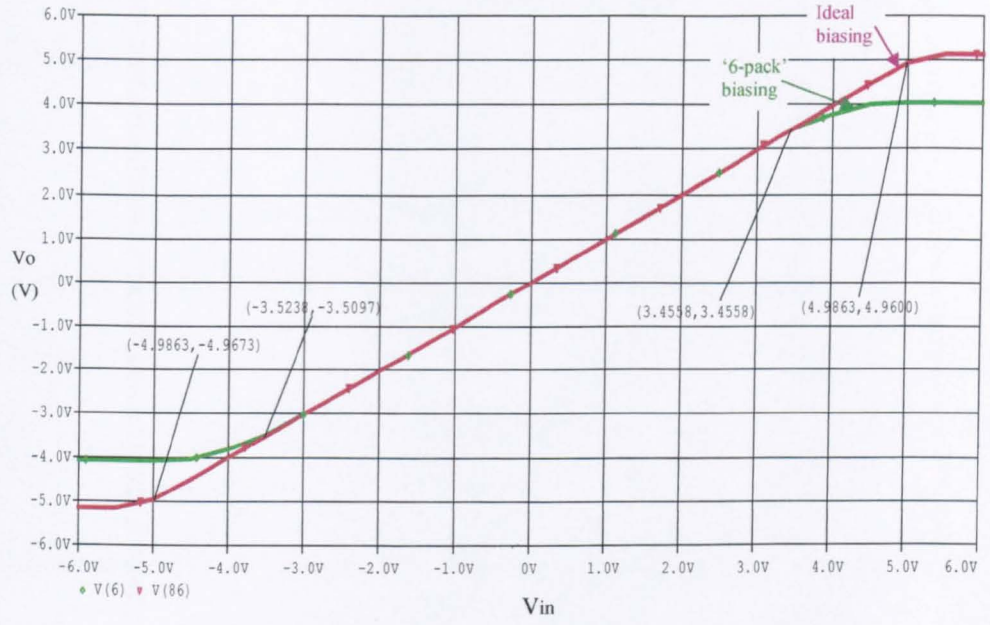


Fig. 5.4 Simulated transfer characteristic for the 'Diamond' circuit
$V_{CC} = 5V; I_O = 0.7mA; R_L = \infty; T = 27\,^{\circ}C$

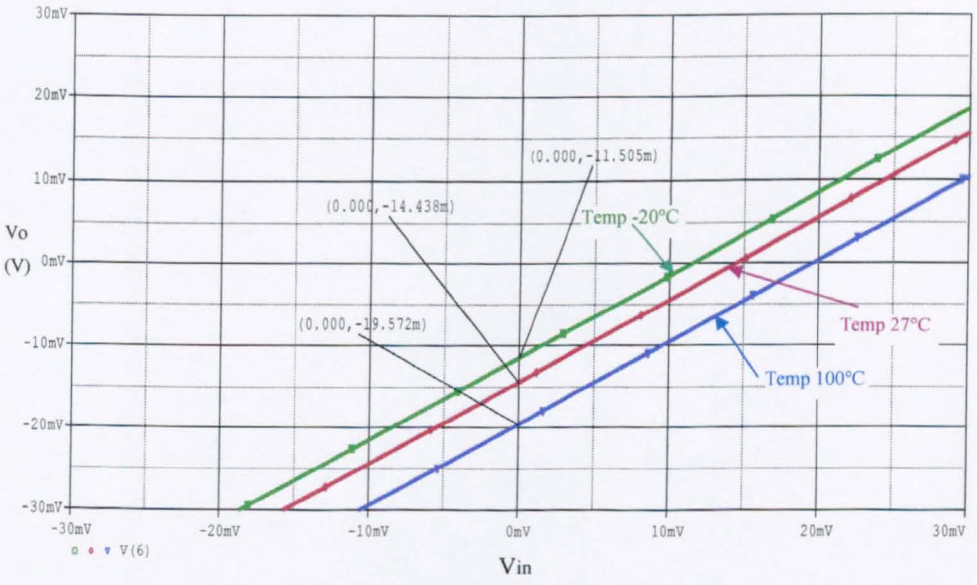


Fig. 5.5 Expanded view of Figure 5.4 in vicinity of $V_S = 0V$

Apparently, $V_{OS} \approx 14.4mV$ at T=27°C.

The plots for T=-20°C and T=100°C are parallel to that for T=27°C because of the effective constancy of (dV_O / dT).

The linear input voltage range is set by the $V_{EB1}(V_{BE2})$ of $Q_1(Q_2)$, and the minimum allowable voltage V_K, say, across the current bias circuits.

Thus,

$$(+V_{CC} - V_{EB1} - V_K)V_S \geq (-V_{CC} + V_{BE2} + V_K) \tag{5.18}$$

From Figure 5.6, $+3V \geq V_S \geq -3V$. The increase in I_B with V_S in Figure 5.6 is attributed to the temperature-variation of β_n, β_p.

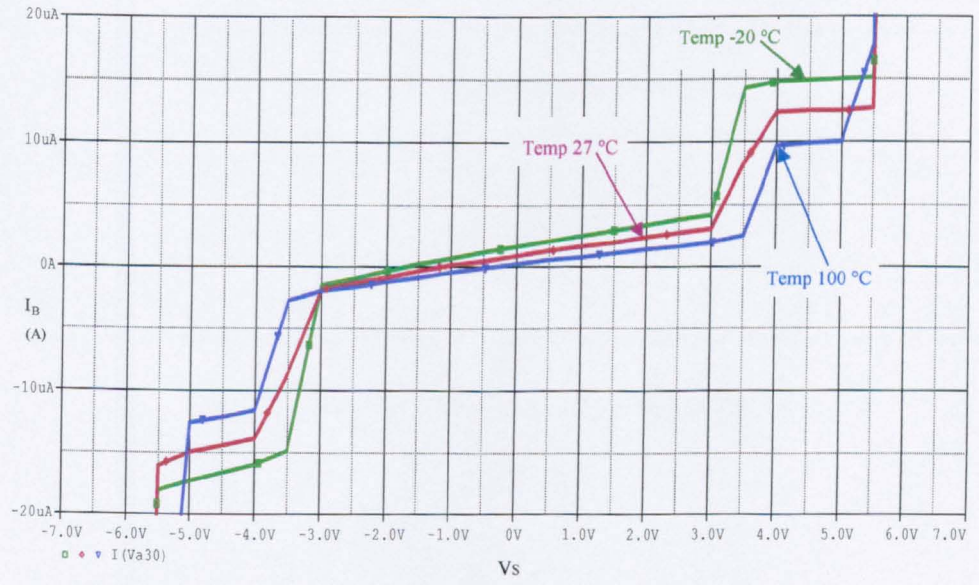


Fig. 5.6 D.C. input characteristic for the circuit of Figure 5.2

$V_{CC} = 5V; I_O = 0.7mA; R_L = \infty$

The quiescent power dissipation of the circuit is,

$$P_Q = (V_{CC} + V_{EE}) \cdot I_Q \cdot n \tag{5.19}$$

where n is the number of vertical conduction paths between the two rail supplies.

Biasing the circuit with ideal sources, at 27°C , $P_Q = (5V + 5V) \cdot 0.7mA \cdot 3 = 21mW$.

Using the '6-pack' for biasing, at 27°C , $P_Q = (5V + 5V) \cdot 0.7mA \cdot 4 = 28mW$.

Simulation of the circuit with both ideal and '6-pack' biasing produced the figures shown in Table 5.1. These show good agreement with the calculated values.

Quiescent power dissipation P_Q **(mW)**			
Operating temperature (°C)	**-20**	**27**	**100**
Circuit with ideal biasing	20.3	20.4	20.5
Circuit with '6-pack' biasing	25.7	28	31.6

Table 5.1 Power dissipation with ideal and '6-pack' biasing

5.3 Small-signal voltage-gain

An analysis of the small-signal low-frequency voltage-gain, G, of the 'Diamond' circuit has not, as far as the author is aware, been presented in the literature. The approach presented here is based on a general property of linear voltage amplifier circuits.

A general schematic of such an amplifier is shown in Figure 5.7.

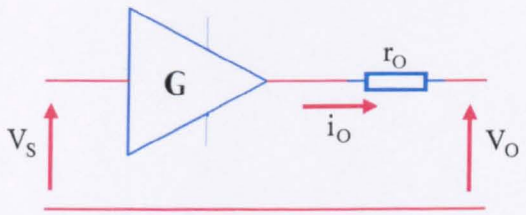


Fig. 5.7 A linear voltage amplifier

where,

G = open circuit voltage-gain,

r_O = incremental output resistance, and

i_O =incremental output current

By inspection,

$$V_O = GV_S - i_O r_O \tag{5.20}$$

If the output is incrementally short-circuited, $V_O = 0$ and $i_O = i_{SC}$

Hence,

$$GV_S = i_{SC} r_O \tag{5.21}$$

Thus,

$$G = \frac{i_{SC} r_O}{V_S} \tag{5.22}$$

For example, with the conventional emitter-follower, the short-circuit output current and the output resistance can be found as follows. (In this analysis base extrinsic resistance r_X is omitted)

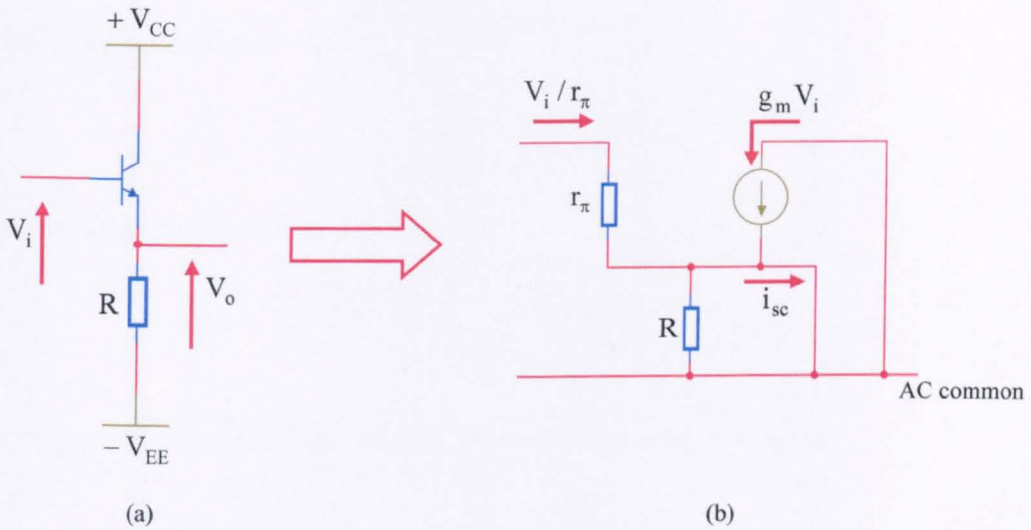


Fig. 5.8 (a) A conventional EF, and
(b) the small signal circuit with incrementally short-circuited output

By inspection of Figure 5.8(b),

$$i_{SC} = \left(g_m + \frac{1}{r_\pi} \right) u \tag{5.23}$$

To find the output resistance r_O a small AC signal is applied in the output of the circuit, with the input potential fixed, as shown below.

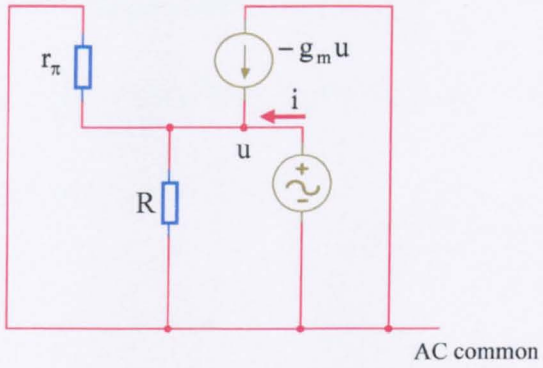


Fig. 5.9 Circuit for finding the output resistance of the EF

By inspection of Figure 5.9,

$$i = \frac{u}{R} + \frac{u}{r_\pi} + g_m u \tag{5.24}$$

Thus, the output impedance is,

$$r_O = \frac{u}{i} = \frac{1}{g_m + \left(\frac{1}{r_\pi} + \frac{1}{R}\right)} \tag{5.25}$$

Consequently, the voltage-gain of the EF can be calculated as follows,

$$G = \frac{i_{SC} r_O}{u_i} = \frac{\left(g_m + \frac{1}{r_\pi}\right) u_i}{u_i} \cdot \frac{1}{g_m + \left(\frac{1}{r_\pi} + \frac{1}{R}\right)} = \frac{(g_m r_\pi + 1)}{r_\pi \left[g_m + \left(\frac{1}{r_\pi} + \frac{1}{R}\right)\right]} = \frac{(\beta + 1)}{\left[\beta + 1 + \frac{r_\pi}{R}\right]} \tag{5.26}$$

Thus, the voltage-gain is,

$$G = \frac{(\beta + 1)R}{r_\pi + (\beta + 1)R} = \frac{1}{1 + \frac{r_\pi}{(\beta + 1)R}} \approx 1 - \frac{\beta \frac{V_T}{I}}{(\beta + 1)R} \tag{5.27}$$

where, I is 0.7mA and, R represents the sink output resistance in parallel with the collector-emitter resistance of the transistor, and the binomial expression has been used since $r_\pi << (\beta + 1)R$ in the normal case.

Following the same technique for the 'Diamond' circuit, shown in Figure 5.10,

the voltage-gains $\frac{V_{C1}}{V_S}$, $\frac{V_{C2}}{V_S}$ of transistors Q_1 and Q_2, respectively, are calculated

individually and used to derive i_{SC}.

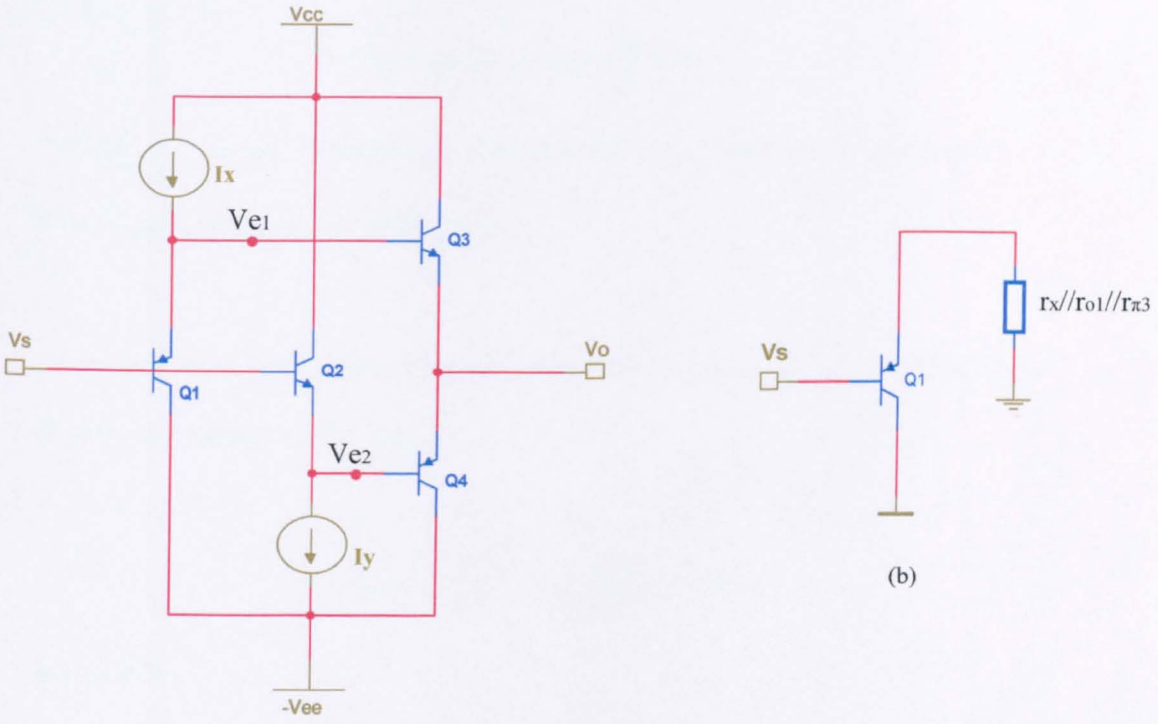


Fig. 5.10 (a)The 'Diamond' circuit, and
(b) the load seen from the emitter of Q_1 with the emitter of Q_3 incrementally earthed

The parameter data of Chapter 3 gives,

$V_{AP} = 22.8, \beta_P = 50.8,\ V_{AN} = 89.61$, and $\beta_N = 50.6$

For transistor Q_1, the gain with the emitter of Q_3 at a.c. earth potential is,

$$G_{Q_1} \approx 1 - \frac{\beta \frac{V_T}{I}}{(\beta+1)R} \tag{5.28}$$

where,

$$R = r_X // r_{O1} // r_{\pi 3} = r_X // \frac{V_{AP}}{I} // \beta_N \frac{V_T}{I}$$

in which: r_X = output resistance of current source ; r_{O1} = collector-emitter resistance of Q_1 ; $r_{\pi 3}$ = input resistance of Q_3.

The output impedance of the current biasing circuit used has been calculated in Chapter 3, at some 3.5MΩ. Thus,

$$R = 3.5M // \frac{22.8}{0.7} // 50.6\frac{25.8}{0.7} = 1.77K\Omega$$

Consequently,

$$G_{Q1} \approx 1 - \frac{50.8\frac{25.8}{0.7}}{51.8 \cdot 1.77K} = 0.979$$

Following the same procedure, the voltage-gain of transistor Q_2 is given by,

$$G_{Q2} \approx 1 - \frac{50.6\frac{25.8}{0.7}}{51.6 \cdot 1.84K} = 0.98$$

where,

$$R = r_y // r_{o2} // r_{\pi 4} = r_x // \frac{V_{AN}}{I} // \beta_P \frac{V_T}{I} = 3.5M // \frac{89.61}{0.7} // 50.8\frac{25.8}{0.7} = 1.84K\Omega$$

Considering the upper part of the 'Diamond' circuit, the output current is calculated as follows,

$$(i_{out})_u = (\beta_N + 1)\frac{u_{e1}}{r_{\pi 3}} = (\beta_N + 1)\frac{0.979u_s}{r_{\pi 3}} \approx 0.98 g_m u_s \qquad (5.29)$$

Similarly, for the lower part of the circuit,

$$(i_{out})_l = (\beta_P + 1)\frac{u_{e2}}{r_{\pi 4}} = (\beta_N + 1)\frac{0.98u_s}{r_{\pi 4}} \approx 0.98 g_m u_s$$

Combining these two parallel contributions,

$$i_{SC} = 2g_m \cdot 0.98u_s \qquad (5.30)$$

The calculation of the output resistance is carried out separately, first for the upper part, then for the lower part. By inspection in Figure 5.10, for the upper half of the circuit,

$$r_{O1} \approx \frac{1}{g_m} + \frac{\frac{1}{g_m}}{\beta_N + 1} \qquad (5.31)$$

For the lower half of the circuit,

$$r_{O2} \approx \frac{1}{g_m} + \frac{\frac{1}{g_m}}{\beta_P + 1}$$

The total resistance is given by r_{o1} in parallel with r_{O2}. Thus,

$$r_O = r_{O1} // r_{O2} \approx \frac{1}{2g_m} \qquad (5.32)$$

Having calculated the short circuit output current and the output resistance, the voltage-gain of the circuit is then calculated,

$$G = \frac{i_{SC} r_O}{u_i} \approx \frac{2g_m \cdot 0.98u_s}{u_s} \cdot \frac{1}{2g_m} \approx 0.98$$

The frequency response for small signal voltage-gain is illustrated in Figure 5.11.

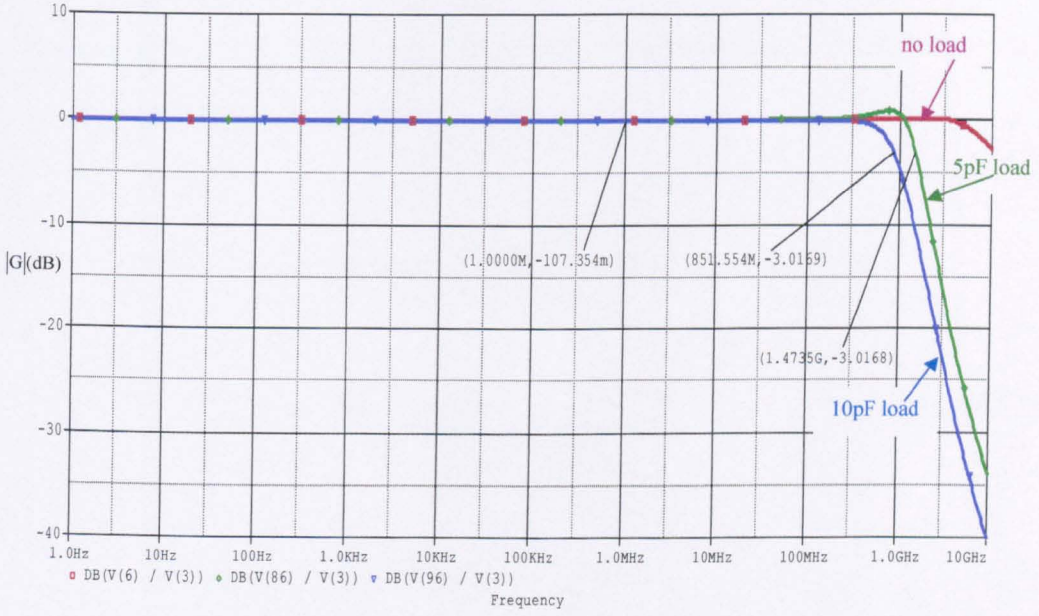


Fig. 5.11 Frequency response for the magnitude of the small signal gain G of the 'Diamond' circuit with '6-pack' biasing , $I_O = 0.7\,\text{mA}$ and different loads

5.4 Incremental input impedance

A recently presented expression **[5-5]** for the incremental input resistance of the 'Diamond' circuit ignored the finite Early-voltages of the transistors used and, to that extent, must be regarded as inaccurate. A more accurate expression is derived here and shown to be validated by simulation results. It was shown in Section 5.2 that for $I_L << I_O$, changes in I_{C3}, I_{C4} are equal in magnitude at $I_L/2$ but opposite in sign. This means that the circuit of Figure 5.1 can be split into two parts, an upper half shown by the full line in Figure 5.12 and a lower half shown by the broken line section, each feeding a load that is now $2R_L$.

Looking into the base of Q_3, the input resistance R_{i3} is given by,

$$\frac{1}{R_{i3}} = \frac{1}{(\beta_n + 1)_{on}}\left(\frac{1}{r_{on}} + \frac{1}{2R_L}\right) \tag{5.33}$$

The effective emitter load of Q_1 is R_{E1} where,

$$\frac{1}{R_{E1}} = \frac{1}{(\beta_n + 1)}\left(\frac{1}{r_{on}} + \frac{1}{2R_L}\right) + \frac{1}{R_p} + \frac{1}{r_{op}} \tag{5.34}$$

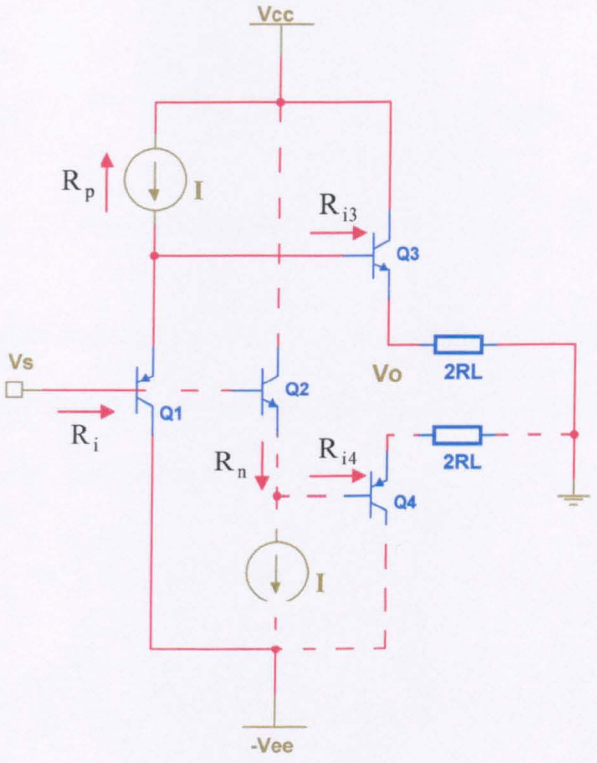


Fig.5.12 Partition of Figure 5.1 for the calculation of R_i

Hence, the input resistance, R_{UH}, of the upper half circuit is given by,

$$\frac{1}{R_{UH}} = \frac{1}{(\beta_p+1)}\left(\frac{1}{r_{op}}+\frac{1}{R_p}\right)+\frac{1}{(\beta_p+1)}\frac{1}{(\beta_n+1)}\left(\frac{1}{r_{on}}+\frac{1}{2R_L}\right) \qquad (5.35)$$

An equivalent circuit for R_{UH} shown in Figure 5.13.

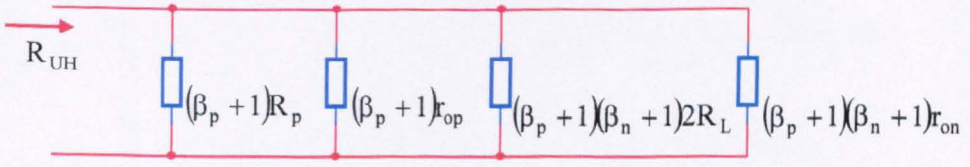


Fig.5.13 The graphical interpretation of R_{UH}

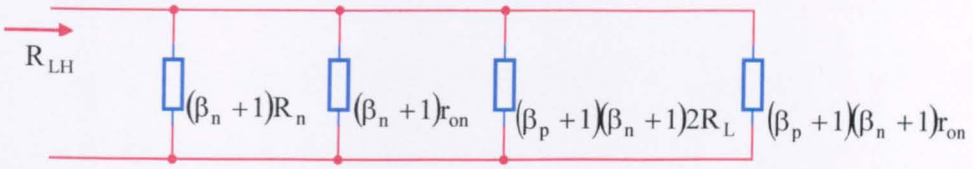


Fig.5.14 The graphical interpretation of R_{LH}

Similarly, an equivalent circuit for R_{LH}, the input resistance of the lower part of the circuit is shown in Figure 5.14. Combining the upper and lower parts, Figure 5.15 is obtained, showing R_i for the complete circuit.

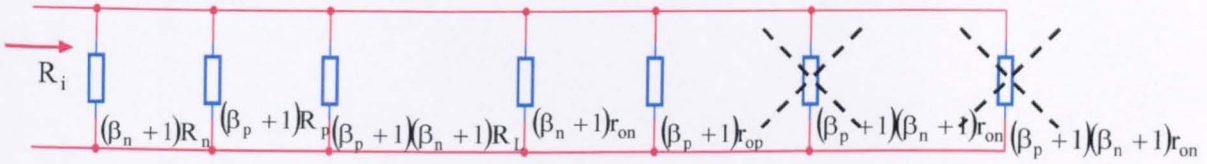


Fig.5.15 Showing The origin of R_i excluding $r_{\mu p}$ of Q_1 and $r_{\mu n}$ of Q_2

The two elements on the right of Figure 5.15 are shown crossed because their magnitudes mean that they can be ignored compared with the other elements.

Incorporating, now, the $r_{\mu p}$ of Q_1 and $r_{\mu n}$ of Q_2 the final equivalent circuit is obtained, as shown in Figure 5.16.

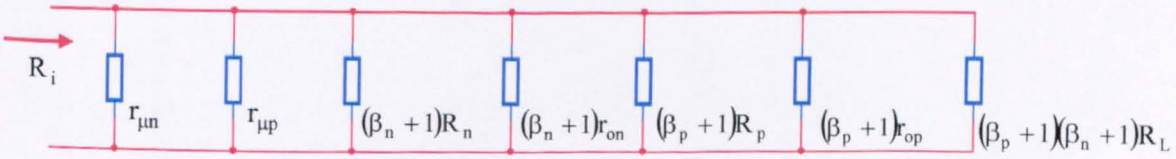
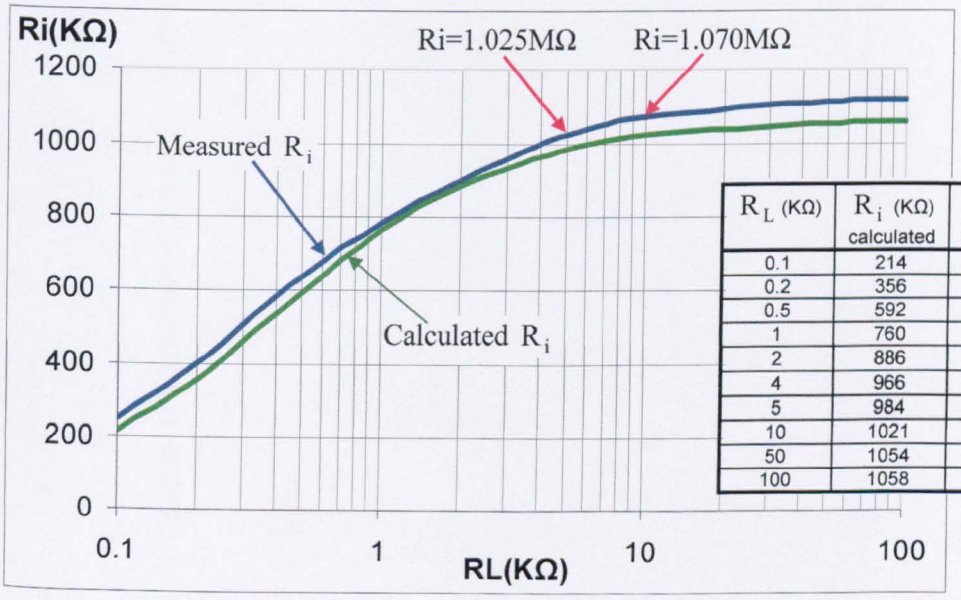


Fig.5.16 A modification of Figure 5.15 that includes $r_{\mu p}$ and $r_{\mu n}$

Substitution of parameter data from Chapter 3, for the case of ideal biasing (i.e., $R_p = R_n = \infty$), $R_L = \infty$ and $I_O = 0.7\text{mA}$, gives $R_i = 1.063\text{M}\Omega$ compared with a simulated value of 1.12MΩ, a difference of some 6%. For '6-pack' biasing R_i falls to 1.08MΩ because of the finite values of R_p, R_n. The agreement between the simulated and calculated values of R_i (as a function of R_L at 27°C) shown for comparison in Figure 5.17, justifies the applicability of the equivalent circuit of Figure 5.16.



R_L (KΩ)	R_i (KΩ) calculated	R_i (KΩ) measured
0.1	214	253
0.2	356	399
0.5	592	632
1	760	780
2	886	900
4	966	1000
5	984	1025
10	1021	1070
50	1054	1110
100	1058	1115

Fig. 5.17 Showing R_i as a function of R_L for ideal biasing and $I_O = 0.7\text{mA}$

It is apparent that R_i is not significantly affected by the magnitude of R_L for $R_L > 10\text{K}\Omega$.

To find the incremental input impedance Z_i, rather than input resistance R_i, it is necessary to measure the effective input capacitance. From the work of Chapter 4 it follows that,

$$C_{in} \approx \left(C_{\mu n} + C_{\mu p}\right) \tag{5.36}$$

Substituting data from Chapter 3, $C_{in} \approx 72\text{fF}$.

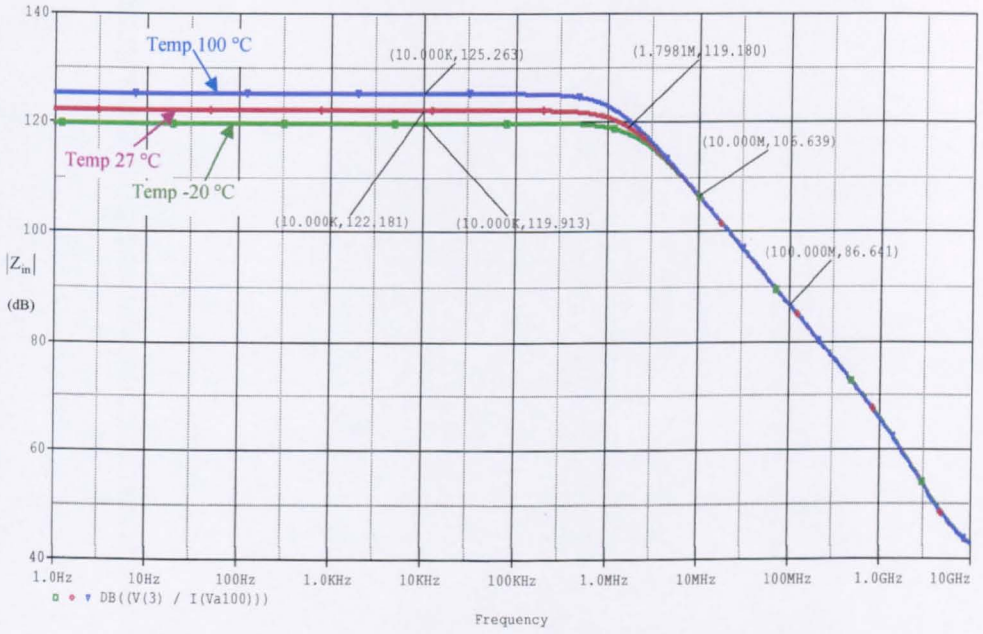


Fig. 5.18 $|Z_i|$ vs f for ideal biasing, $I_O = 0.7\text{mA}$, and three different temperatures

Figure 5.18 shows a 20dB/decade roll-off of $|Z_i|$ with frequency.

From this,

$$C_{in} = \frac{1}{2\pi f_B R_i} \tag{5.37}$$

where f_B is the -3dB frequency.

Substituting data for R_i, f_B obtained from the graph, $C_{in} \approx 78.9\text{pF}$, within 10% of the calculated value.

The variation of $|Z_i|$ with T at low frequencies is due, principally, to the temperature dependence of β_n, β_p. Temperature has little effect above about 3MHz because in this region $|Z_i|$ is dominated by C_{in} which is not significantly temperature-dependent.

Some spot figures for the frequency and temperature dependence of $|Z_i|$ are shown in Table 5.2.

Conditions	$\|Z_{in}\|$ **(Ω)**					
Operating temperature (°C)	**-20**	**27**	**100**	**-20**	**27**	**100**
f = 312.5KHz	0.98M	1.12M	1.77M	1.05M	1.10M	1.49M
f = 31.25MHz	67.3K	66.6K	67.1K	65.6K	65.4K	66.4K
f = 250MHz	8.7K	8.6K	8.5K	8.2K	8.1K	8.2K
Current source used	Ideal current source/sink			'6-pack' current source/sink		

Table 5.2 $|Z_{in}|$ of the 'Diamond' circuit with $I_O = 0.7mA$ and $R_L = \infty$ as a function of f and T

5.5 Incremental output impedance

Taking into consideration that, in the small-signal analysis, the upper part of the circuit is effectively in parallel with the lower part, from a signal standpoint, the incremental output resistance can be calculated using the upper half circuit. Furthermore, since (from Chapter 3) $\beta_n \approx \beta_p$ it can be written $\beta_n = \beta_p = \beta$, where β is the arithmetic average of β_p and β_n in an approximate treatment. In Figure 5.19, r_μ and r_O of Q_1 and Q_3 are ignored, as are base and emitter bulk resistances of Q_1. These resistances are, however, included for Q_3 because of the larger current that they pass.

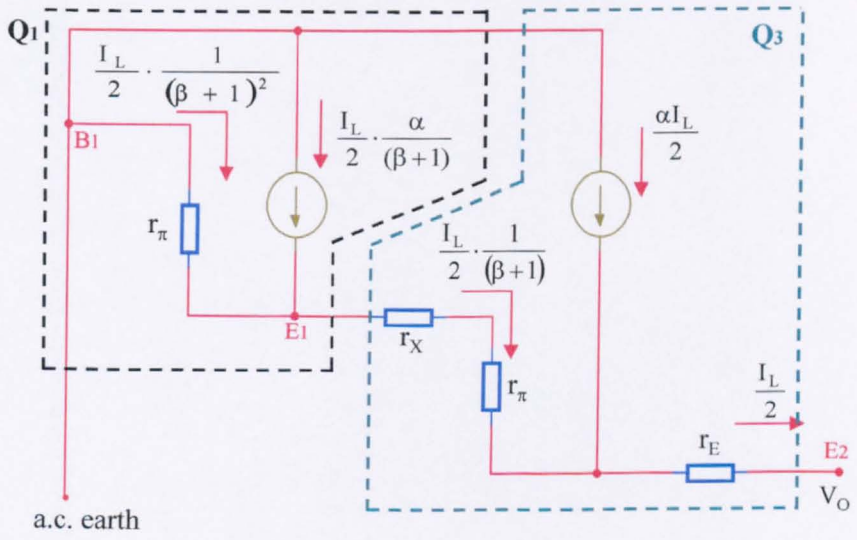


Fig. 5.19 Approximate small-signal circuit for calculating the output resistance, r_O

By inspection of Figure 5.19,

$$-V_o = \frac{I_L}{2}\cdot r_\pi\left[\frac{1}{(\beta+1)}+\frac{1}{(\beta+1)^2}\right]+\frac{I_L r_X}{2(\beta+1)}+\frac{I_L}{2}\cdot r_E \qquad (5.38)$$

Hence, substituting α for $\beta/(\beta+1)$ and $\beta V_T / I_o$ for r_E,

$$r_o = \frac{V_o}{(-I_L)} = \frac{\alpha V_T}{2I_o}\left[1+\frac{1}{(\beta+1)}\right]+\frac{r_X}{2(\beta+1)}+\frac{r_E}{2} \qquad (5.39)$$

Substituting for $\beta = 50.7$ (Chapter 3), and $r_X = 260\Omega, r_E = 5.2\Omega$ from SPICE data,

$$r_o \approx 23.9\Omega$$

In Table 5.3, displaying some spot values of $|Z_o|$, r_o the low frequency value of $|Z_o|$ is shown as 23.6Ω, less than 2% lower than the calculated value at T=27°C.

Conditions	$\|Z_o\|$ **(Ω)**					
Operating temperature (°C)	**-20**	**27**	**100**	**-20**	**27**	**100**
f = 312.5KHz	23.1	23.6	27.7	25.7	24	22.7
f = 31.25MHz	23.1	23.6	27.7	25.7	24	22.7
f = 250MHz	21.9	24.5	28.7	23.5	25	26.7
Current source used	Ideal current source/sink			'6-pack' current source/sink		

Table 5.3 $|Z_o|$ of the 'Diamond' circuit as a function of f and T for ideal and practical biasing

r_o changes only slightly with T via its dependence on V_T, β and, in the case of '6-pack' current biasing, on I_o which increases slightly with T. The curves in Figure 5.20, showing Z_o as a function of f and T, for '6-pack' biasing, have the characteristic shape dealt with in detail in Chapter 4.

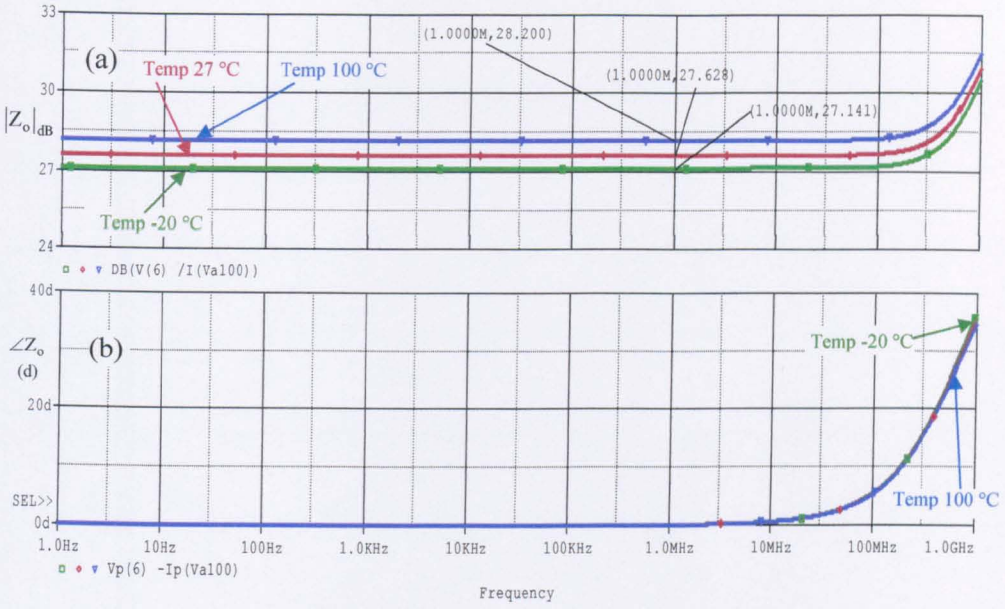


Fig. 5.20 Z_o as a function of frequency for '6-pack' biasing

(a) $|Z_o|$, and (b) $\angle Z_o$

5.6 Total harmonic distortion (THD)

Tables 5.4, 5.5, 5.6 show, respectively, THD under specified conditions at 312.5KHz, 31.25MHz and 250MHz.

Conditions	**THD (dB)**					
Operating temperature (°C)	**-20**		**27**		**100**	
Current source used	Ideal	'6-pack'	Ideal	'6-pack'	Ideal	'6-pack'
$Z_L = 5K\Omega$	-88.1	-86.4	-86	-85.8	-85.4	-85.1
$Z_L = 5K\Omega // 5pF$	-86.9	-88.4	-86.2	-86.7	-89.1	-85.1

Table 5.4 THD at 312.5KHz

Conditions	**THD (dB)**					
Operating temperature (°C)	**-20**		**27**		**100**	
Current source used	Ideal	'6-pack'	Ideal	'6-pack'	Ideal	'6-pack'
$Z_L = 5K\Omega$	-80.8	-71.9	-77.8	-71.9	-74.8	-72
$Z_L = 5K\Omega // 5pF$	-70.1	-61.6	-70.8	-63	-80.5	-57.9

Table 5.5 THD at 31.25MHz

Conditions	**THD (dB)**					
Operating temperature (°C)	**-20**		**27**		**100**	
Current source used	Ideal	'6-pack'	Ideal	'6-pack'	Ideal	'6-pack'
$Z_L = 5K\Omega$	-47.3	-36.6	-53.7	-40	-50	-41.8
$Z_L = 5K\Omega // 5pF$	-46.9	-40.2	-47.2	-45.5	-46.3	-37.5

Table 5.6 THD at 250MHz

The figures for 312.5KHz and 31.25MHz are better than those for the single emitter follower, presented in Chapter 4, because the load current taken by each output transistor is only one half that of a single emitter follower operating at same current. The poorer THD for '6-pack' biasing compared with ideal biasing is attributed to the reduced effective emitter load resistances for the input transistors. The finite output capacitance of the non-ideal current bias circuit becomes increasingly important with increasing frequency because it introduces some frequency distortion. This presumably accounts for the poorer performance in the case of non-ideal biasing at 250MHz.

5.7 Intermodulation distortion (IMD)

IMD as a function of operating frequency and temperature is shown in Table 5.7. Similar to the THD comments apply.

Conditions	**IMD (dB)**					
Operating temperature (°C)	**-20**		**27**		**100**	
Current source used	Ideal	'6-pack'	Ideal	'6-pack'	Ideal	'6-pack'
f = 312.5KHz	-100.4	-94	-108.1	-99	-102.2	-97.9
f = 31.25MHz	-94.6	-83.2	-94	-88.6	-92.8	-86.7
f = 250MHz	-65.8	-48.5	-64.4	-50.3	-63.5	-52.2

Table 5.7 IMD as a function of f , T and biasing conditions

5.8 Noise performance

The noise performance of the 'Diamond' for ideal and '6-pack' current biasing is shown in Figures 5.21 and 5.22, respectively, for the sake of completeness.

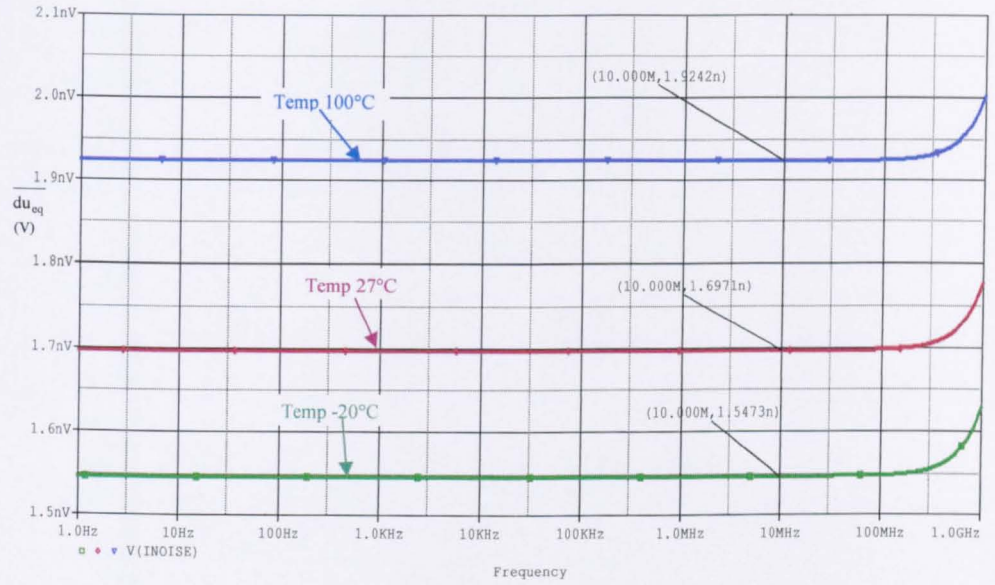


Fig. 5.21 Input noise with ideal biasing for three different temperatures

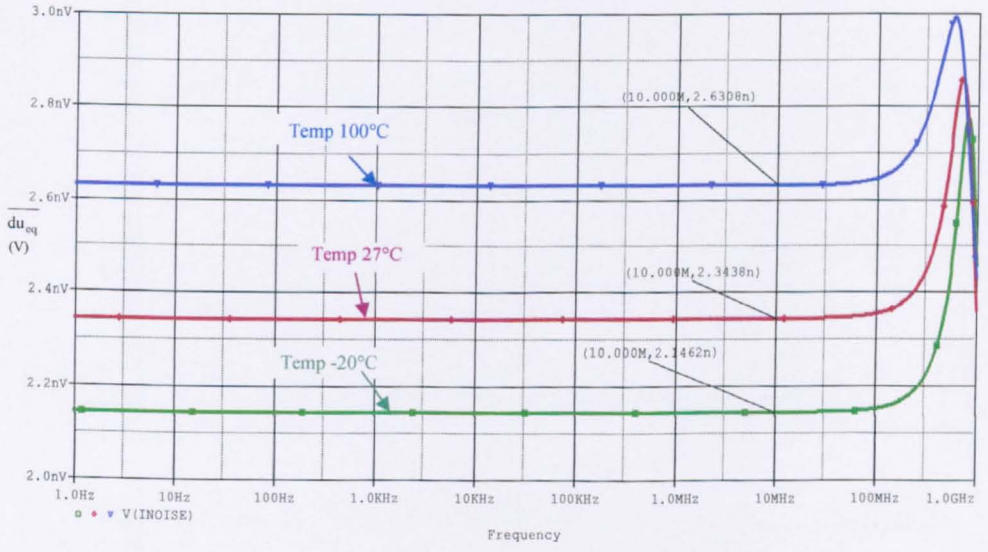


Fig. 5.22 Input noise with '6-pack' biasing for three different temperatures

5.9 Pulse response

The pulse response of the circuit (see Figures 5.23, 5.24) is understandable in the light of the discussion on the pulse response of the conventional EF in Chapter 4.

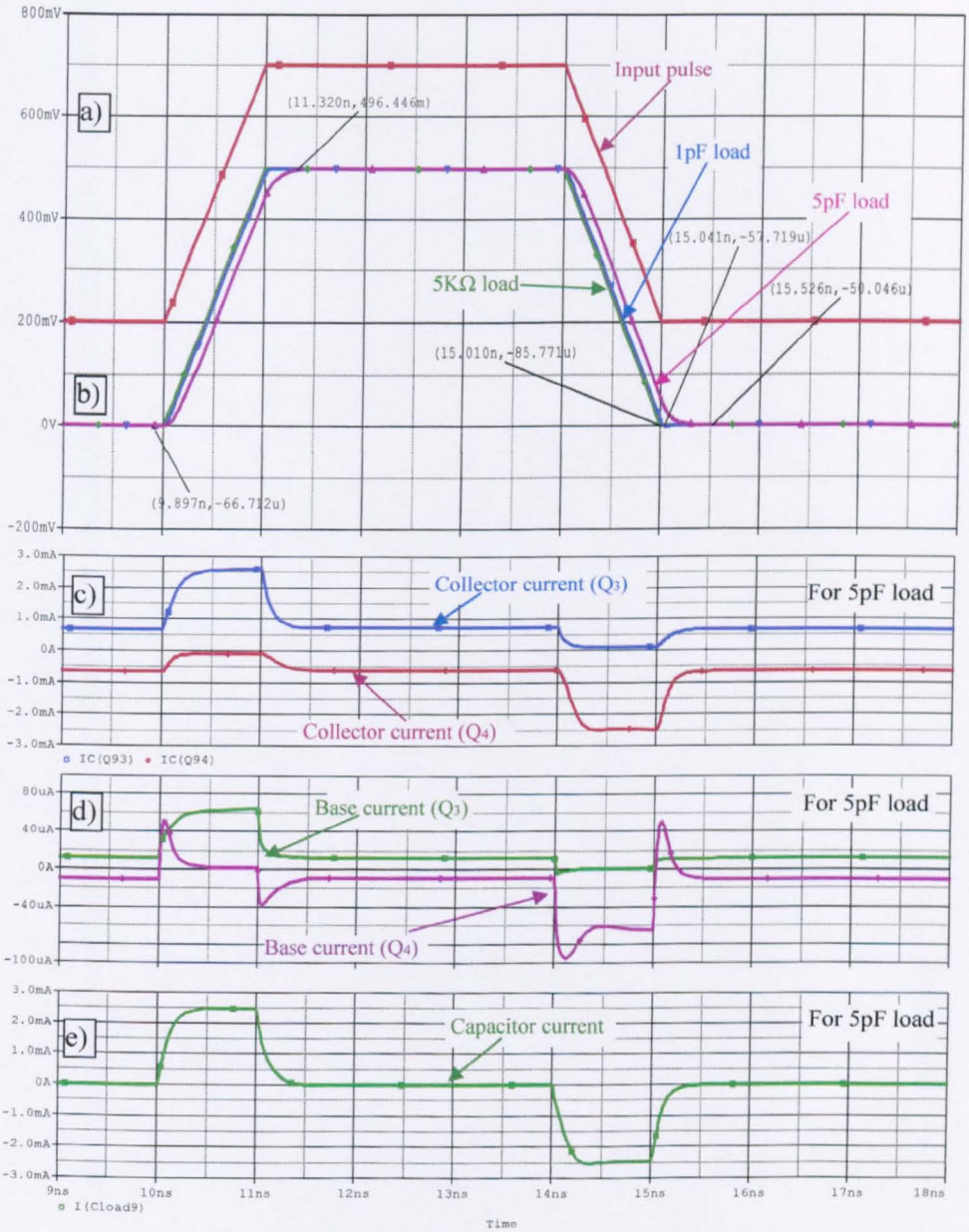


Fig. 5.23 Waveforms for the circuit of Figure 5.1 for 1nS rise & fall times of input pulse (a) u_B ; (b) u_o ; (c) i_C ; (d) i_B and (e) Capacitor current

The horizontal scale used to present the pulse response for 0.1nS rise and fall time is half of that for 1ns rise and fall time for the convenience of the reader.

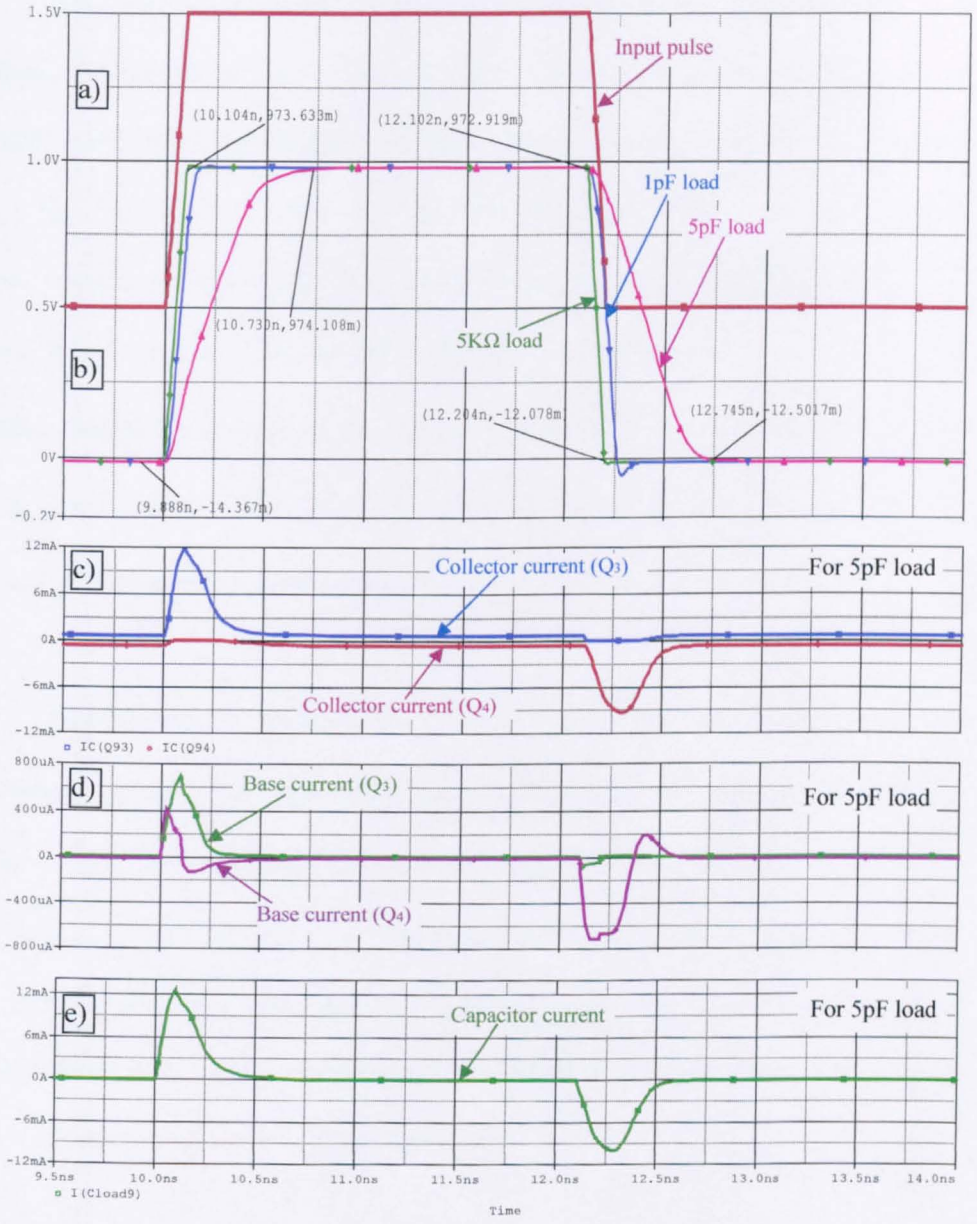


Fig. 5.24 Waveforms for the circuit of Figure 5.2 for 0.1nS rise & fall times of input pulse (a) u_B ; (b) u_o ; (c) i_C ; (d) i_B and (e) Capacitor current

5.10 Progressive modifications up to the final circuit

The deficiencies of the 'Diamond' circuit are overcome successively in the circuit modifications shown in Figures 5.25 to Figure 5.29 inclusive. Modification 1 (Figure 5.25) shows the addition of diode-strapped voltage-level-shifting transistors Q_2 , Q_4, Q_6 and Q_7. These are incorporated with the aim of reducing the overall offset voltage to a level closer to zero than as obtained in the 'Diamond' circuit. The offset voltage reduction comes about because the base-emitter voltage drop of Q_6 matches that of Q_1 and that of Q_2 matches that of Q_5. Similar considerations apply to Q_7 and Q_3 and to Q_4 and Q_8. Note though that the penalty for a reduced offset voltage is an increased output resistance.

Modification 2 (Figure 5.26) now includes the added emitter-follower transistors Q_9 and Q_{10} operating with the same base potential as Q_2 and Q_4, respectively. These bootstrap the collector voltages of input transistors Q_1 and Q_3 and ensure that the collector-base voltage of these devices are effectively zero, over the linear input voltage range and over the ambient temperature range and the power dissipation in these transistors is minimised. However the main reason for doing this is to increase the incremental input impedance.

Modification 3 (Figure 5.27) shows the addition of two more emitter-follower transistors Q_{11} , Q_{12} which reduce the loading effect of Q_2, Q_9 and Q_5 in the current source and Q_{10}, Q_4 and Q_8 in the current sink.

Modification 4 (Figure 5.28) includes two further devices, Q_{13} and Q_{14} which bootstrap the collectors of Q_5 and Q_8 respectively with the aim of achieving even better linearity. However, the penalty is a higher loading on the current source and sink.

Modification 5 (Figure 5.29) shows the final circuit, what is termed here the 'Voltage Super-follower'. The devices paralleling in the output stage halve the output resistance and reduce the signal distortion but in the expense of an increase in quiescent power dissipation of some 30%.

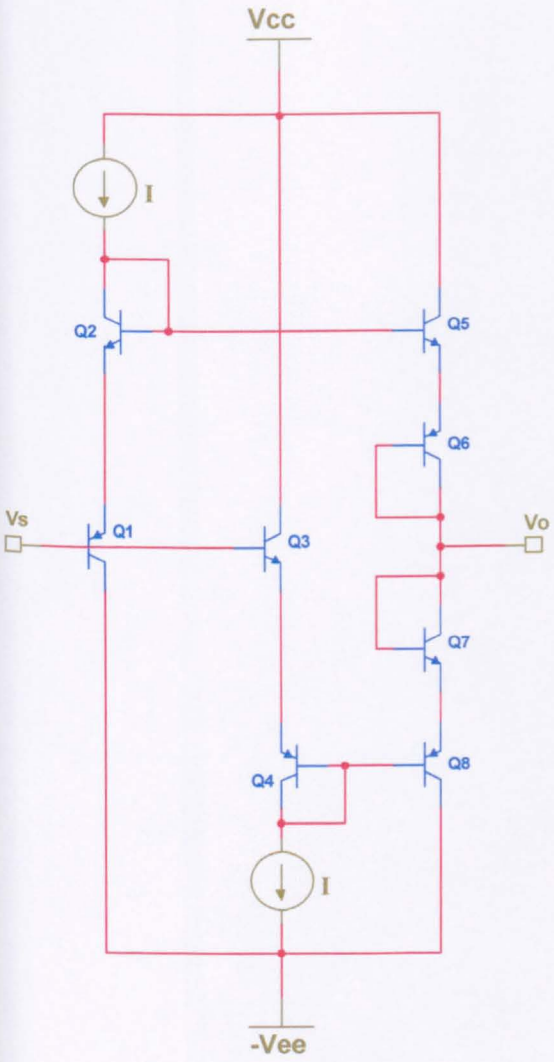


Fig. 5.25 Modification 1 of Figure 5.1

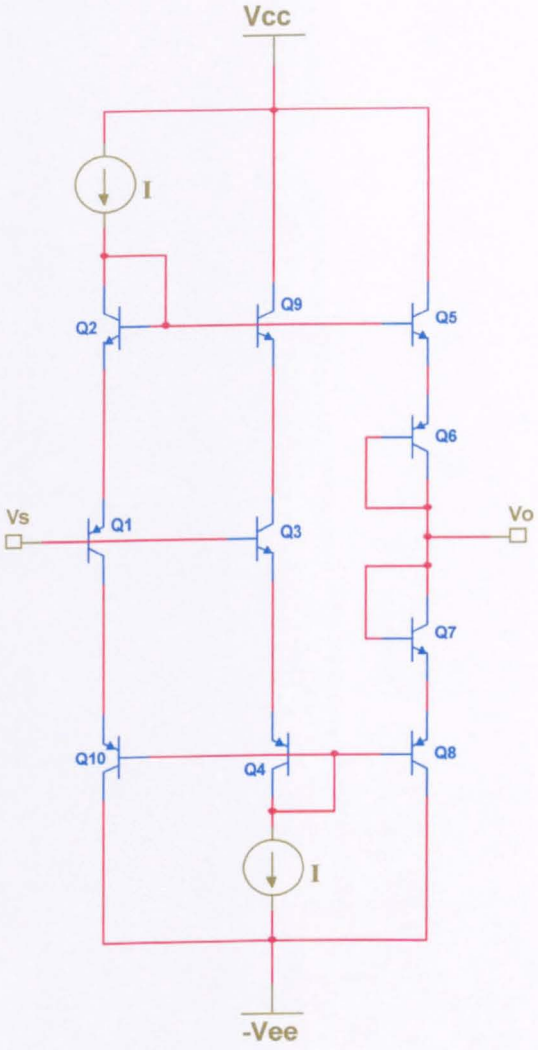


Fig. 5.26 Modification 2 of Figure 5.1

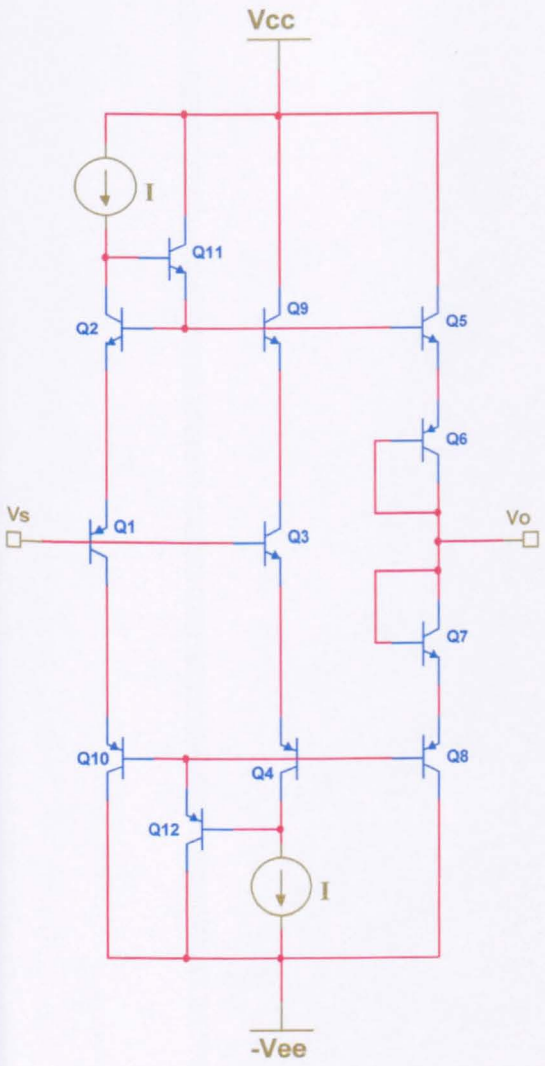


Fig. 5.27 Modification 3 of Figure 5.1

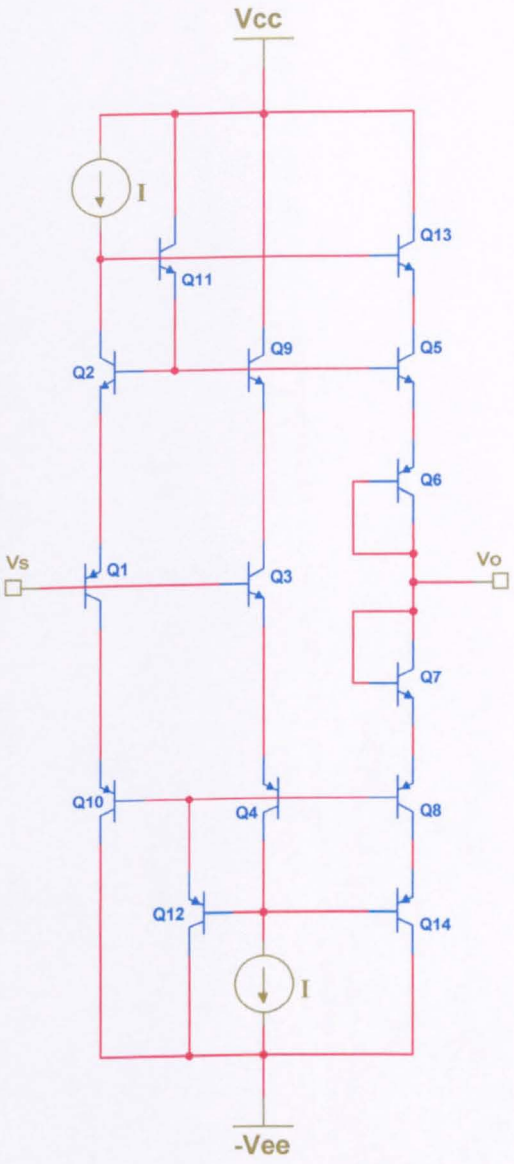


Fig. 5.28 Modification 4 of Figure 5.1

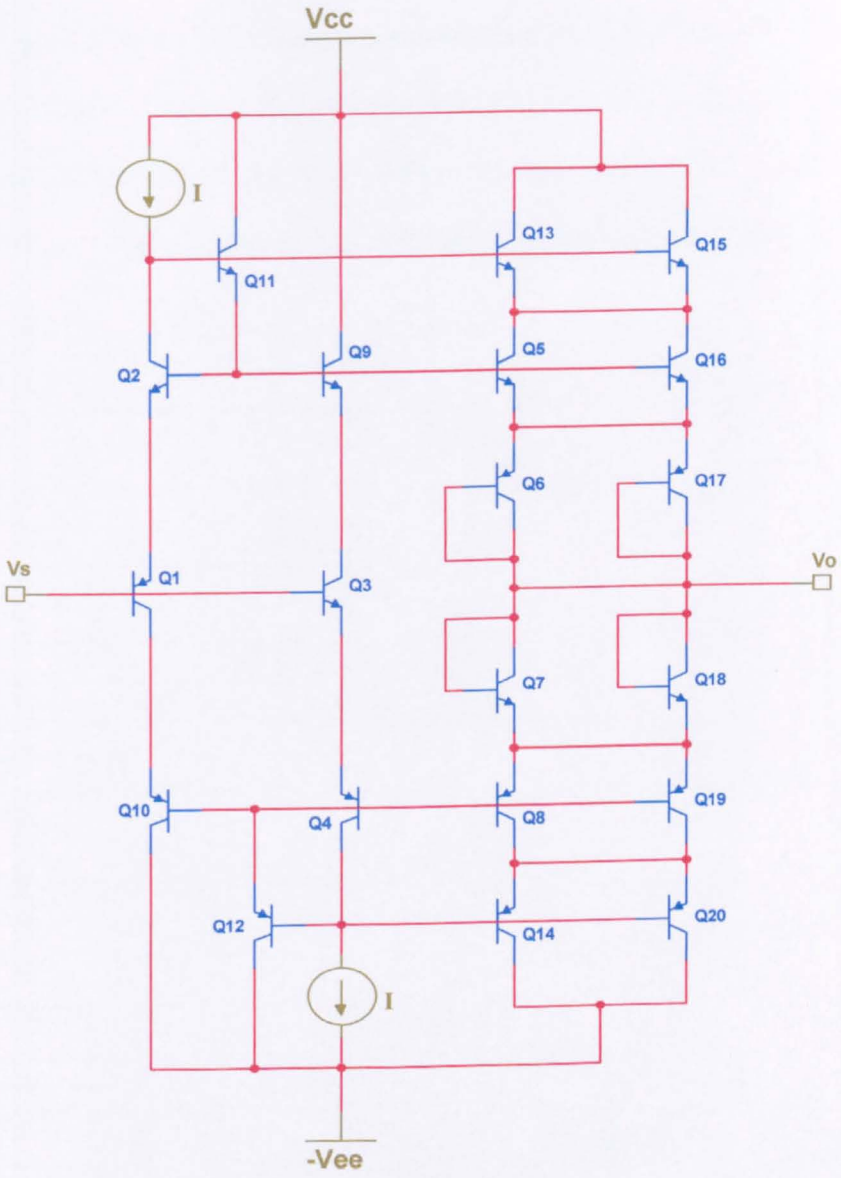


Fig. 5.29 Modification 5 of Figure 5.1 : The final circuit, the 'Voltage Super-follower'

5.11 The 'Super-follower' / DC conditions

Figure 5.30 is a DC transfer characteristic of the Super-follower showing an apparent DC gain of unity. The enlarged plot of Figure 5.31 confirms the expected very small dependence of the offset voltage on temperature. This arise because, although V_{BE} is dependant on T, V_{BE} difference is only weakly dependent on T.

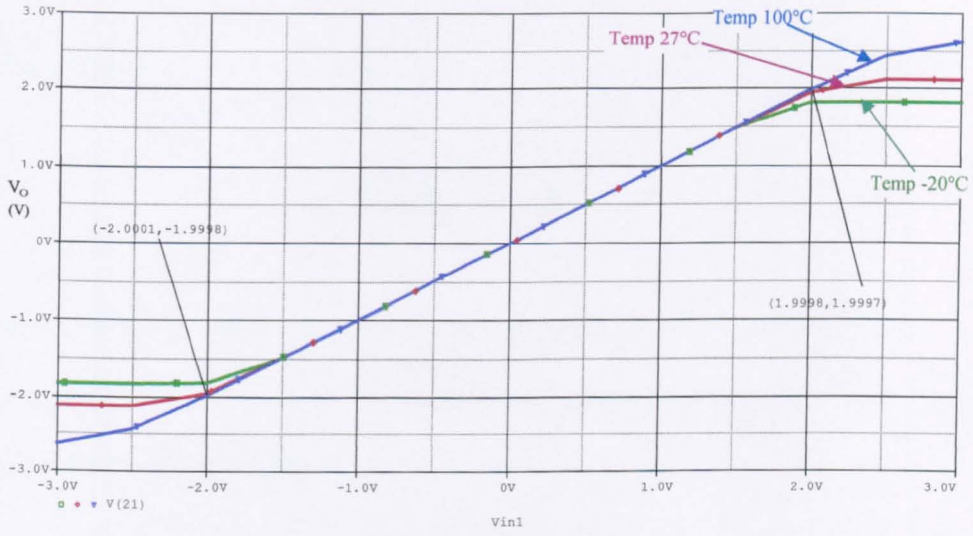


Fig. 5.30 Simulated transfer characteristic for Figure 5.29 : $V_{CC} = V_{EE} = 5V; I_o = 0.7mA; R_L = \infty$

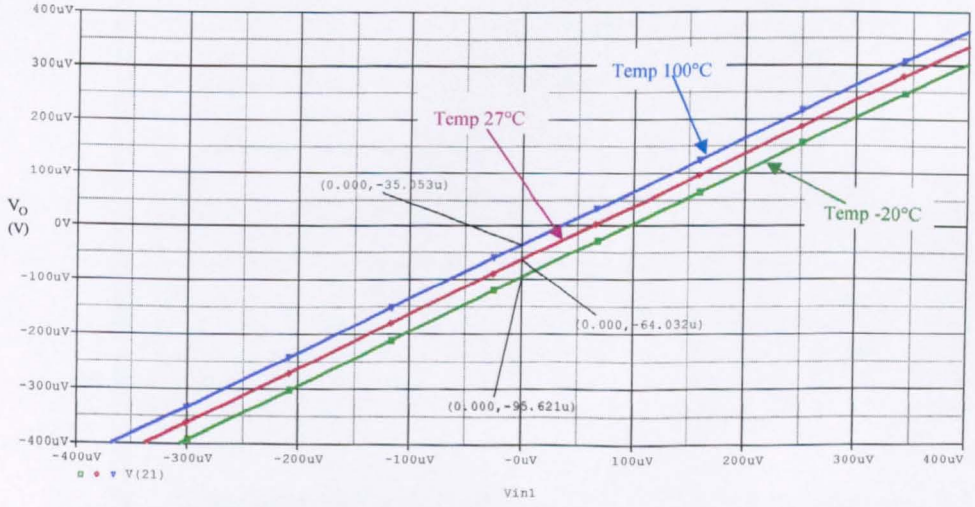


Fig. 5.31 Expanded view Figure 5.30 in the vicinity of the origin

Figure 5.32 shows the DC input characteristic of the Super-follower when the V_S is varied over the range -5V to +5V. Figure 5.33 shows an expanded view of this for the range -3V to +3V. The input current I_B is effectively constant (for a given temperature) for $1V>V_S>-1V$, because this is the range for which the current sink and source operate in the linear range (i.e., $-(V_{EE}-5V_{BE})>V_S>(V_{CC}-5V_{BE})$) and Q_1, Q_3 operate with constant (zero) collector-base voltages.

Theoretically,

$$I_B=\left(\frac{I_{C1}}{(\beta_p+1)}-\frac{I_{C3}}{(\beta_n+1)}\right) \tag{5.40}$$

Consequently, I_B will be zero if both npn and pnp devices have identical current gain. In practice, the difference in the transistors' current gain results the input current offset shown in Figure 5.32.

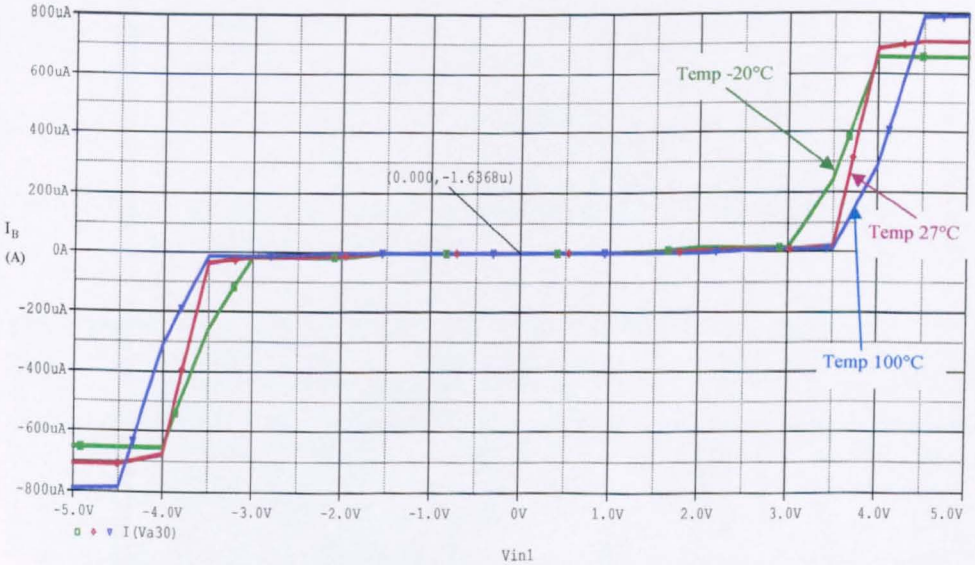


Fig. 5.32 Input current of the circuit for $V_{CC}=V_{EE}=5V; I_o=0.7mA; R_L=\infty$

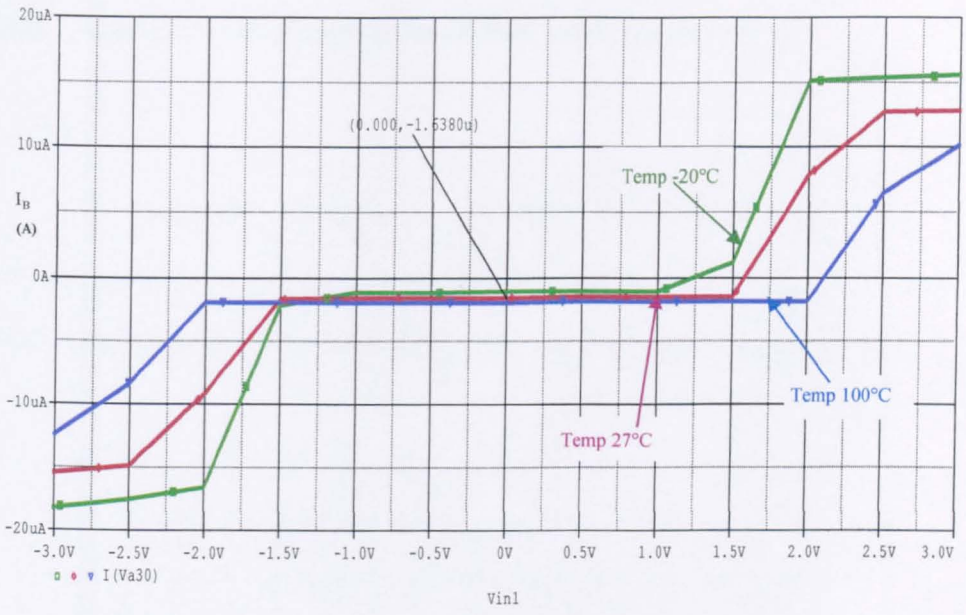


Fig. 5.33 Input current of the circuit, in vicinity of the origin

$$V_{CC} = V_{EE} = 5V; I_o = 0.7mA; R_L = \infty$$

The quiescent power dissipation of the circuit is increased, compared to the 'Diamond' circuit, due to the increased number of vertical conduction paths between the two rail supplies. Consequently, substituting to (5.19) for $V_{CC} = V_{EE} = 5V$ and $I_o = 0.7mA$, at 27°C,

$$P_Q = 35mW$$

This shows good agreement with the simulated values shown in Table 5.8.

Quiescent power dissipation P_Q **(mW)**			
Operating temperature (°C)	**-20**	**27**	**100**
	31.7	34.6	39.2

Table 5.8 Quiescent power dissipation

5.12 Small-signal voltage-gain of the 'Super-follower'

The small signal voltage-gain of the 'Super-follower' is shown in Figure 5.34 over a wide frequency range. This is to be expected from configuration comprising a parallel pair of series connected emitter-followers, for reasons described in Chapter 4.

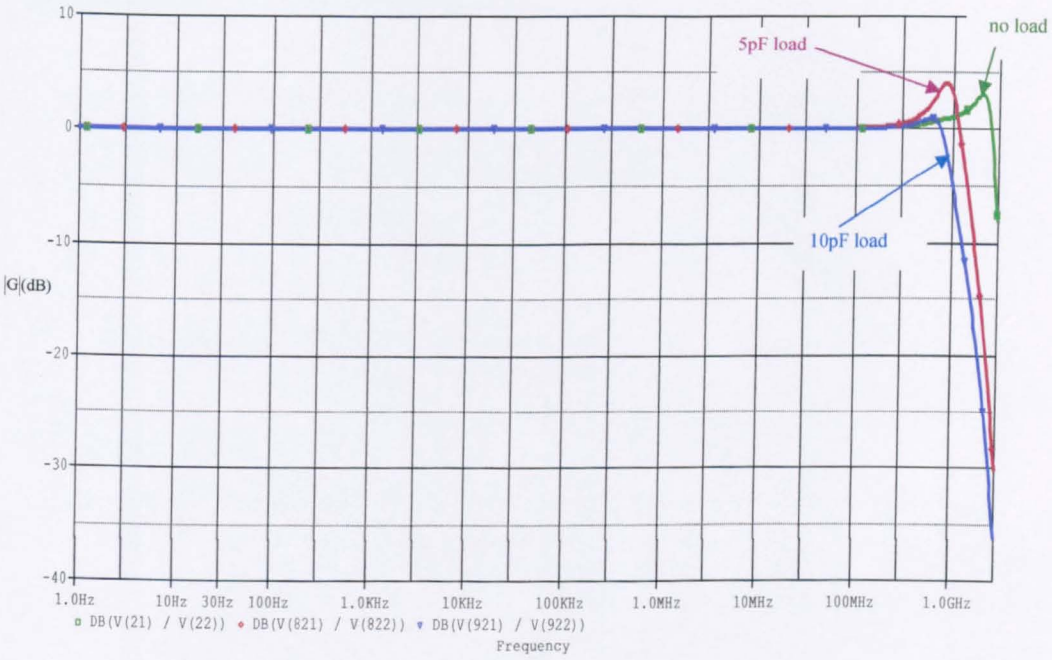


Fig. 5.34 Frequency response for the small signal voltage-gain G with different loads

5.13 Incremental input impedance of the 'Super-follower'

The increased incremental input impedance of the 'Super-follower' compared with the 'Diamond' circuit comes about via bootstrapping of the input stage. The input capacitance, derived from the -3dB frequency (1.05MHz) in Figure 5.35, is $C_{in} = 11.3fF$ compared with 78fF for the 'Diamond' circuit. Spot values for $|Z_i|$ as a function of f and T are shown in Table 5.9.

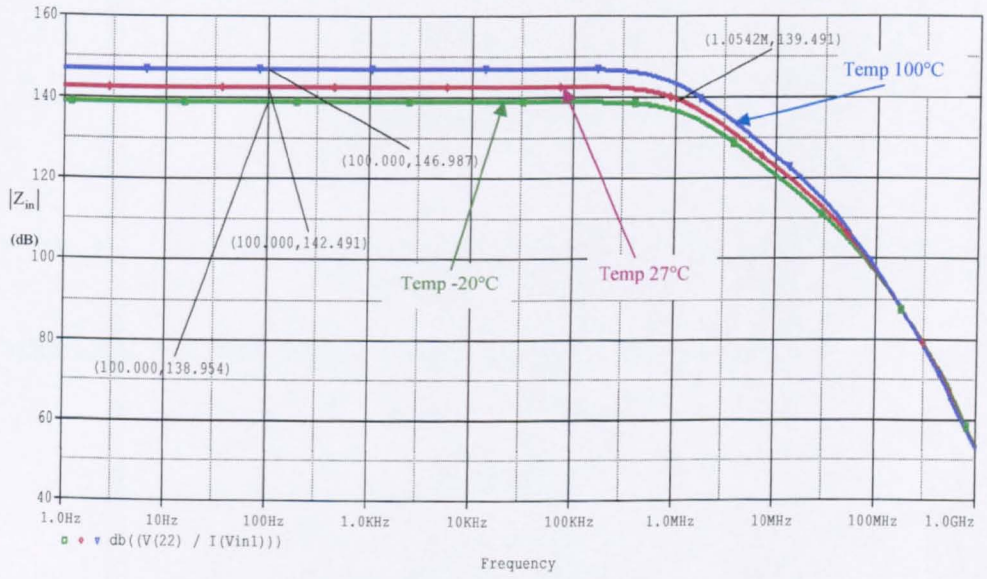


Fig. 5.35 Bode amplitude plot for three operating temperatures

Conditions	$\|Z_i\|$ **(Ω)**		
Operating temperature (°C)	**-20**	**27**	**100**
f = 312.5KHz	8.6M	12.8M	21.1M
f = 31.25MHz	344K	419K	530K
f = 250MHz	12.7K	12.6K	12.7K

Table 5.9 $|Z_i|$ for $I = 0.7mA$ and $R_L = \infty$ as a function of f and T

5.14 Incremental output impedance of the 'Super-follower'

Figure 5.36 shows Z_o and $\angle Z_o$ as a function of frequency. This is resistive over a wide frequency range but exhibits inductive behaviour, the common feature of emitter follower output stages, at high frequencies. Spot values for Z_o as a function of f and T are shown in Table 5.10. Z_o is resistive at low frequencies and theoretically its magnitude is,

$$R_o \approx \frac{\left[\frac{1}{g_m} + \frac{R_{EX}}{2} + \frac{r_X}{2(\beta+1)}\right]}{2} \tag{5.41}$$

where, R_{EX}, r_X represent, respectively, transistor bulk emitter and base resistance.

Substituting data from Chapter 3 and PSICE transistor parameters,

$$R_o \approx 23.6\Omega$$

Which is some 9% lower than the simulated value.

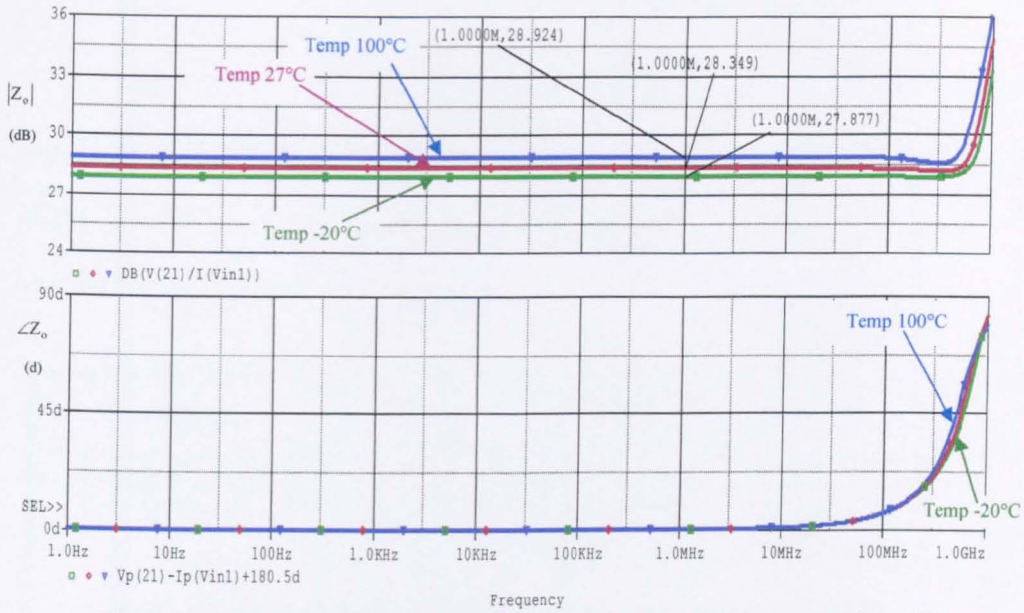


Fig. 5.36 Magnitude (upper curve) and phase (lower curve) for Z_o as a function of T

Conditions	$\|Z_o\|$ **(Ω)**		
Operating temperature (°C)	**-20**	**27**	**100**
f = 312.5KHz	24.8	26	27.9
f = 31.25MHz	24.8	26	27.9
f = 250MHz	24.8	25.6	26.9

Table 5.10 $|Z_o|$ of the 'Super-follower' as a function of f and T

5.15 Total harmonic distortion (THD) of the 'Super-follower'

Tables 5.11, 5.12 and 5.13 show, respectively, THD under specified conditions at 312.5KHz, 31.25MHz and 250MHz. This is understandable in the light of the discussion of emitter follower THD in Chapter 4 and previous sections and need no further concern.

Conditions	**THD (dB)**		
Operating temperature (°C)	**-20**	**27**	**100**
$Z_L = 5K\Omega$	-89.9	-93.9	-93.4
$Z_L = 5K\Omega // 5pF$	-89.6	-89.2	-88.9

Table 5.11 THD at 312.5KHz

Conditions	**THD (dB)**		
Operating temperature (°C)	**-20**	**27**	**100**
$Z_L = 5K\Omega$	-76.8	-75.6	-80
$Z_L = 5K\Omega // 5pF$	-82	-84.4	-82.4

Table 5.12 THD at 31.25MHz

Conditions	**THD (dB)**		
Operating temperature (°C)	**-20**	**27**	**100**
$Z_L = 5K\Omega$	-60.4	-57.4	-57
$Z_L = 5K\Omega // 5pF$	-47	-47.7	-47.4

Table 5.13 THD at 250MHz

5.16 Intermodulation distortion (IMD) of the 'Super-follower'

IMD as a function of operating frequency and temperature is shown in Table 5.14.

Conditions	**IMD (dB)**		
Operating temperature (°C)	**-20**	**27**	**100**
f = 312.5KHz	-93.4	-93.9	-89.9
f = 31.25MHz	-80	-75.6	-76.8
f = 250MHz	-60.4	-57.4	-57

Table 5.14 Simulated IMD results of the circuit as a function of f and T

5.17 Noise performance of the 'Super-follower'

The noise performance of the proposed circuit is shown in Figures 5.37. That is increased by some 60% compared with the 'Diamond' circuit due to the added devices.

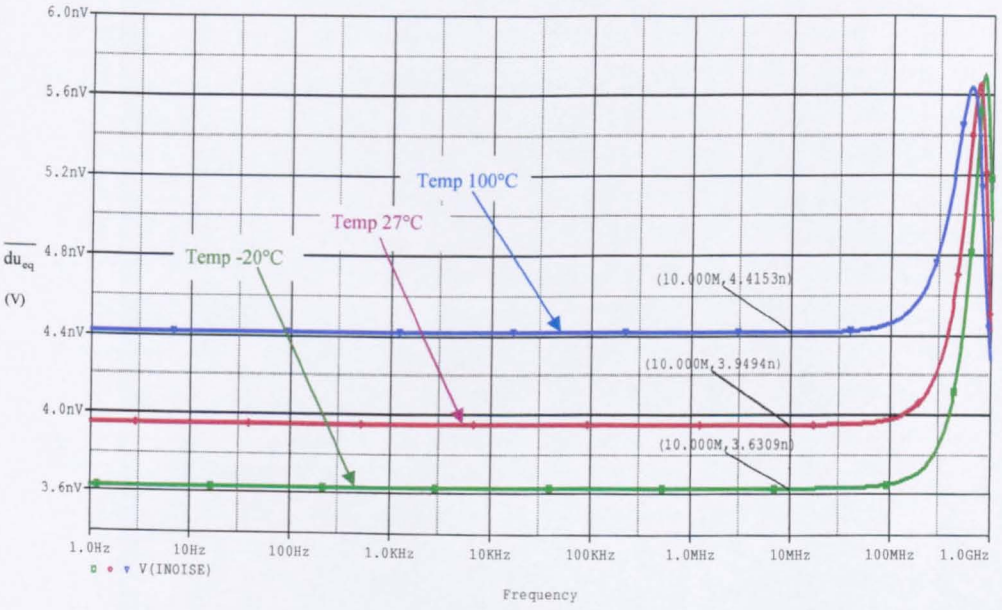


Fig. 5.37 Input noise for three different temperatures

5.18 Pulse response of the 'Super-follower'

The waveforms when a positive going input pulse of amplitude 0.5V and specified rise and fall time that are shown in Figures 5.38 and 5.39, are understandable in the light of the discussion of emitter follower pulse response in Chapter 4 and need no further concern.

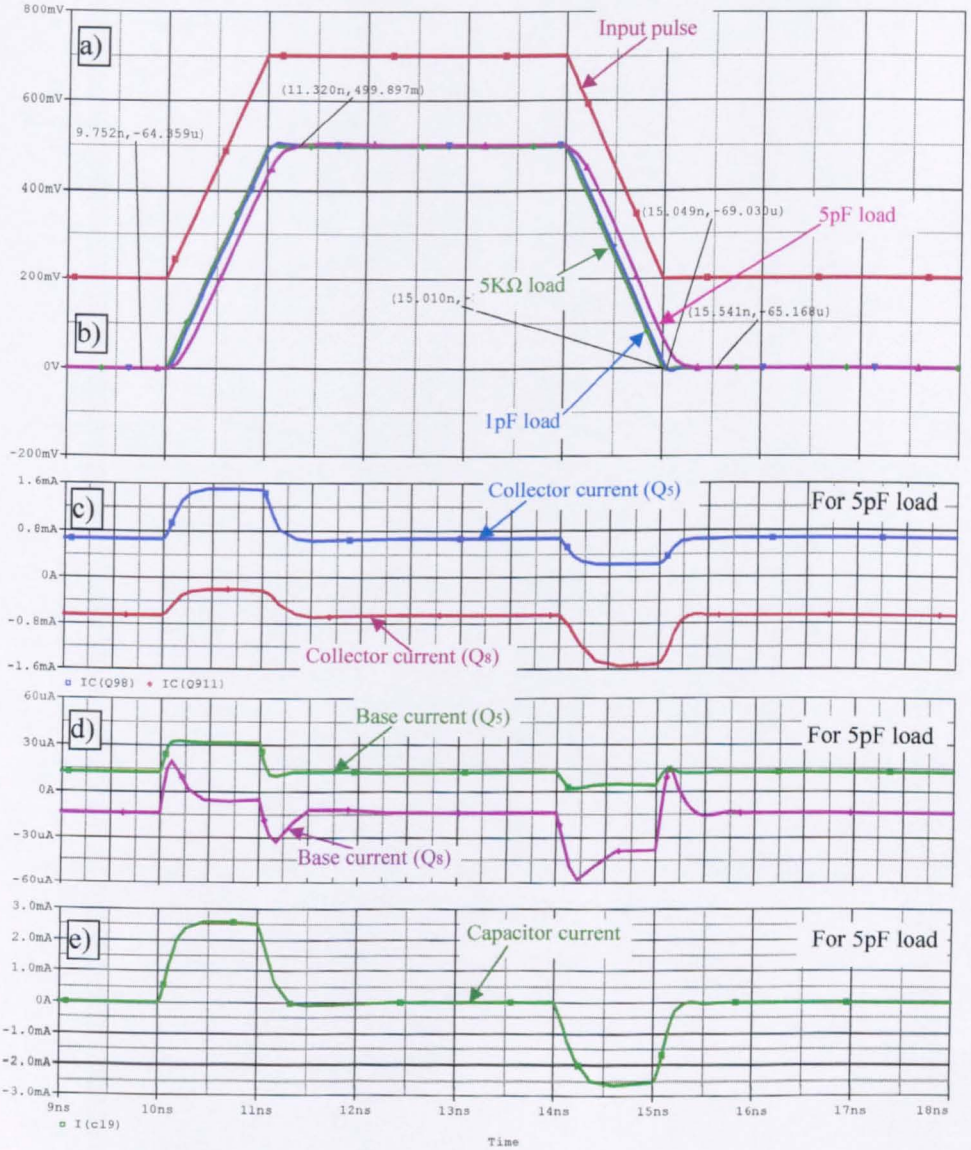


Fig. 5.38 Waveforms for the circuit of Figure 5.29 for 1nS rise and fall times of input pulse (a) u_B ; (b) u_o ; (c) i_C ; (d) i_B and e) Capacitor current

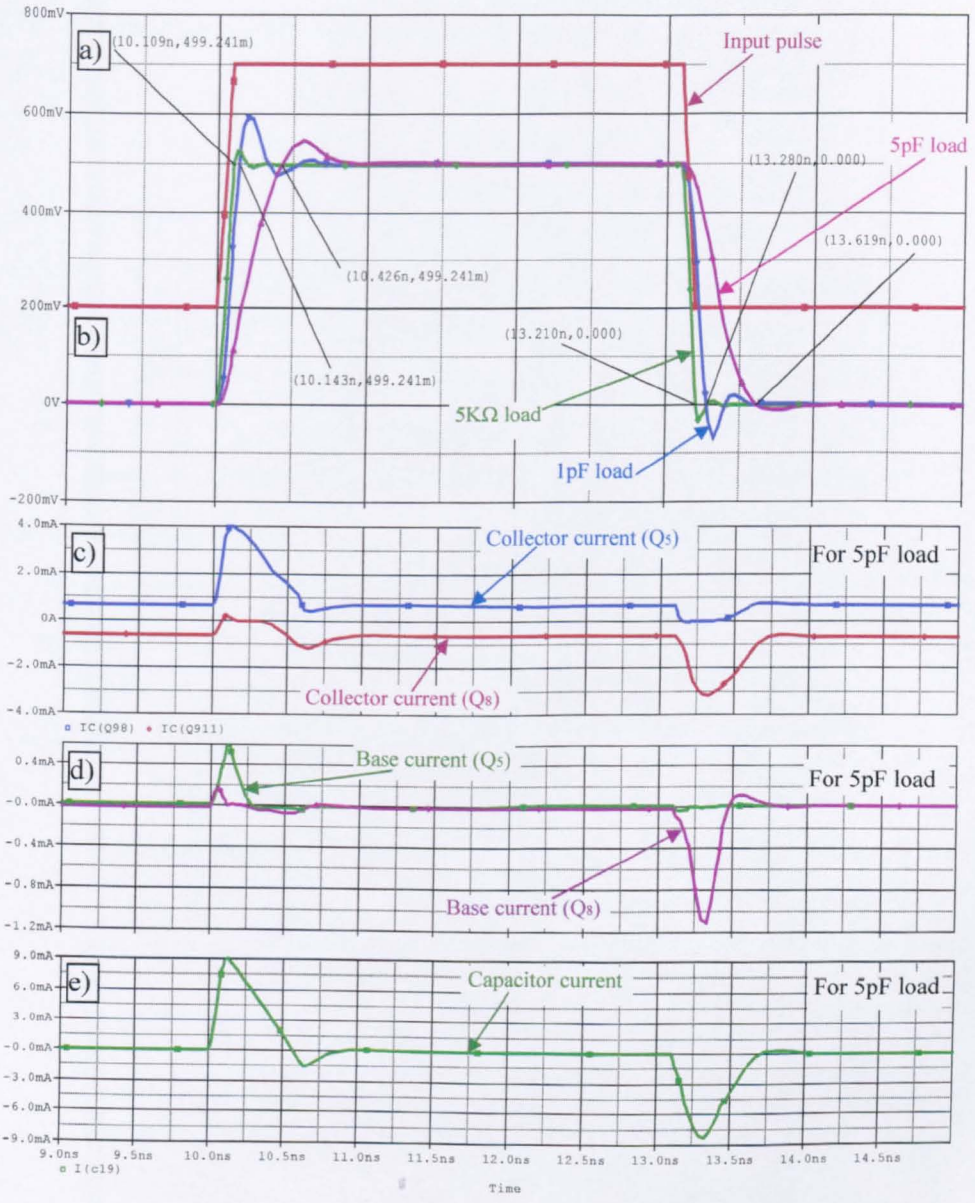


Fig. 5.39 Waveforms for the circuit of Figure 5.29 for 0.1nS rise and fall times of input pulse (a) u_B ; (b) u_o ; (c) i_C ; (d) i_B and e) Capacitor current

As an extra test the input amplitude was increased to 1V as shown in Figure 5.40. The resultant output took some 1.5nS to settle.

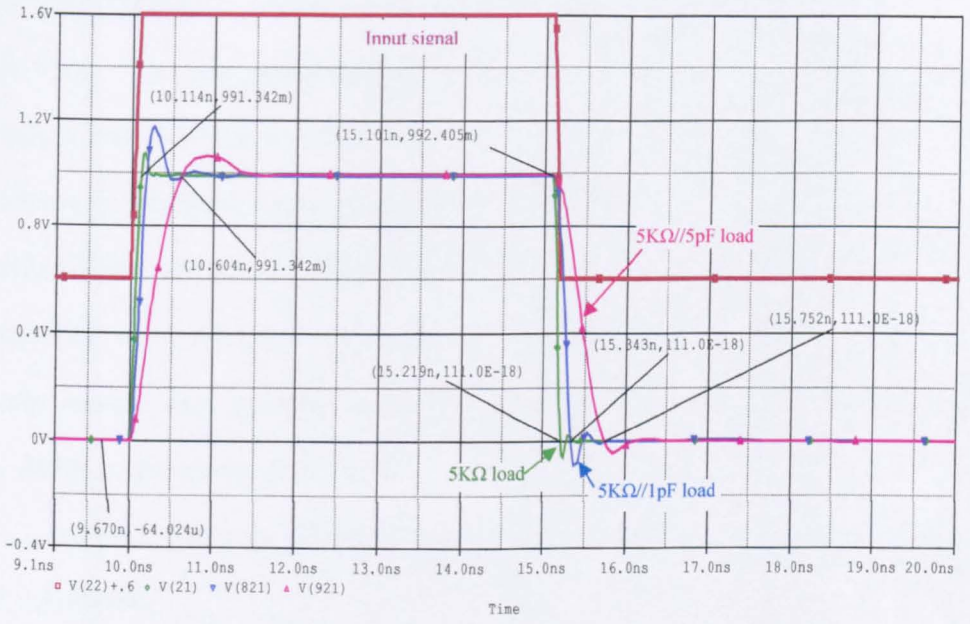


Fig. 5.40 Pulse response for an input signal with 1ns rise and fall times of input pulse and increased amplitude (1V)

5.19 Summary of Chapter 5

This chapter has considered the analysis and progressive modification of the so-called 'Diamond' circuit up to the proposed voltage-follower, named 'Super-follower'. The new design improved many of the performance parameters of the original class AB high frequency VF, introduced by National Semiconductors, at the expense of increased power supply levels. The simulation results showed superior performance over several recently published VFs **[5-5 to 5-9]** as far as bandwidth, distortion, input impedance and offset voltage are concerned. Its performance, in some aspects, was comparable, at the worse case, to similar designs currently available in the market **[5-10 to 5-13]** as far as the distortion and the pulse response are concerned. The new VF has been reported by the author in the technical literature **[5-14], [5-15].**

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CHAPTER 6

V.F. Type B / V.F. with local feedback and double-valued current biasing

6.1 Introduction

This chapter considers the evolution and operating characteristics of two related types of voltage-follower, VFB/1 and VFB/2, that depend on the use of two levels of current bias, one being the basic bias current and the other double that. Emitter followers are extensively used and the matching in the base-emitter voltage of two, or more, BJTs of the same polarity and operated at the same collector current level is exploited. The analysis is carried out in a similar, to the previous chapters, way investigating initially on the basic circuit and introducing the modifications that improve its performance. The precise current-mirror '6-pack', analysed in Chapter 3, is used as a practical biasing scheme.

6.2 Half-circuit of the VFB/1

The upper half-circuit of Figure 6.1 serves to show the starting point in the design of VFB/1. It shows an enhanced EF. If base currents are ignored the feedback action ensures that $I_1 = I_2 = I$. The matched V_{BE} drops of Q_1, Q_2, Q_3, Q_4 and the action of the cascode transistor Q_2 see to it that over the linear input voltage range, $V_{CQ3} = (V_S + V_{BE})$ and $V_{CQ1} = V_S$.

V_o depends on the base-emitter voltage of Q_5: if the load current, I_L, is equal to I then $V_o = V_S$. In practice I_1 and I_2 are not precisely equal to I because of base currents. Thus, if the load current in R_L is I_L,

$$I = I_1 + \frac{I_2}{(1+\beta)} + \frac{I_L}{(1+\beta)} \tag{6.1}$$

$$2I = I_1 + I_2\left(1 + \frac{1}{\beta}\right) \tag{6.2}$$

These yield,

$$I_1 = \frac{-I_L(1+\beta) + I(1+\beta^2)}{1+\beta+\beta^2} \tag{6.3}$$

and,

$$I_2 = \beta\left[\frac{I(1+\beta) + I_L}{1+\beta+\beta^2}\right] \tag{6.4}$$

The difference between I_1 and I_2, as well as the difference between the base-emitter voltages of Q_5 and Q_3, leads to a finite offset voltage.

Bootstrapping **[6-1]** the collector of Q_1 increases the input impedance above that obtained with the conventional EF. However, the circuit is not, as it stands, suitable for use with fast negative-going input transitions for the reasons discussed in Chapter 4, for the conventional EF. This is generally true even if the lower end of R_L is connected to $-V_{ee}$. This difficulty is overcome in the full circuit of the VFB/1 shown in Figure 6.2.

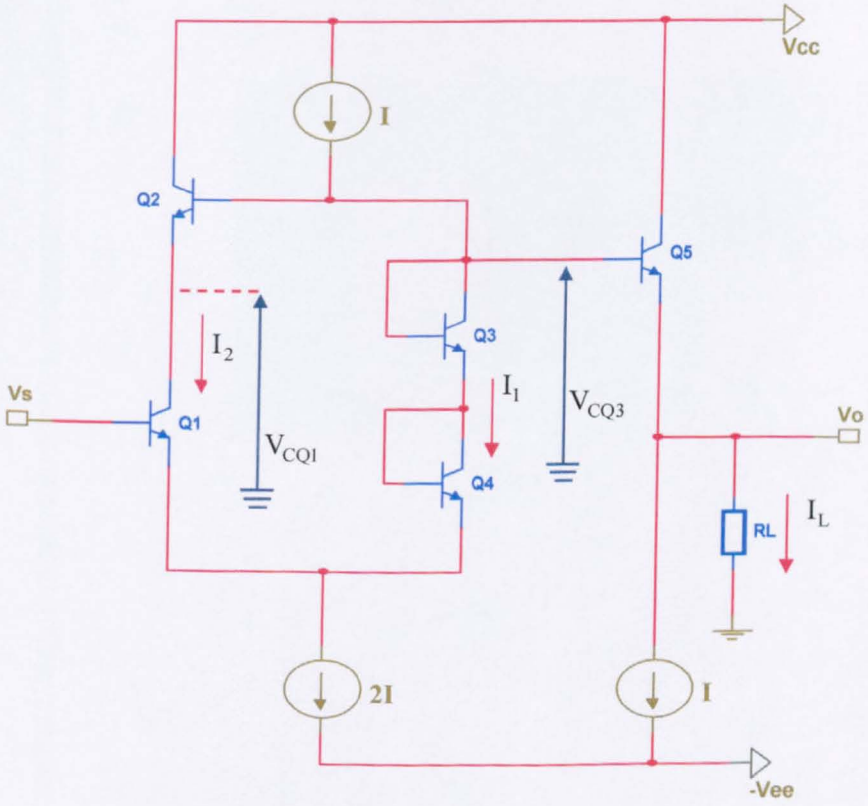

Fig. 6.1 Upper half-circuit of proposed VFB/1

6.3 The VFB/1 / DC Conditions

Figure 6.2 shows the full circuit of the proposed VFB/1. The shaded region shows the upper half circuit of Figure 6.1 and a complementary version of this. On this way the current can respond equally well to input signal of both polarities. DC conditions are shown in Figures 6.3 and 6.4.

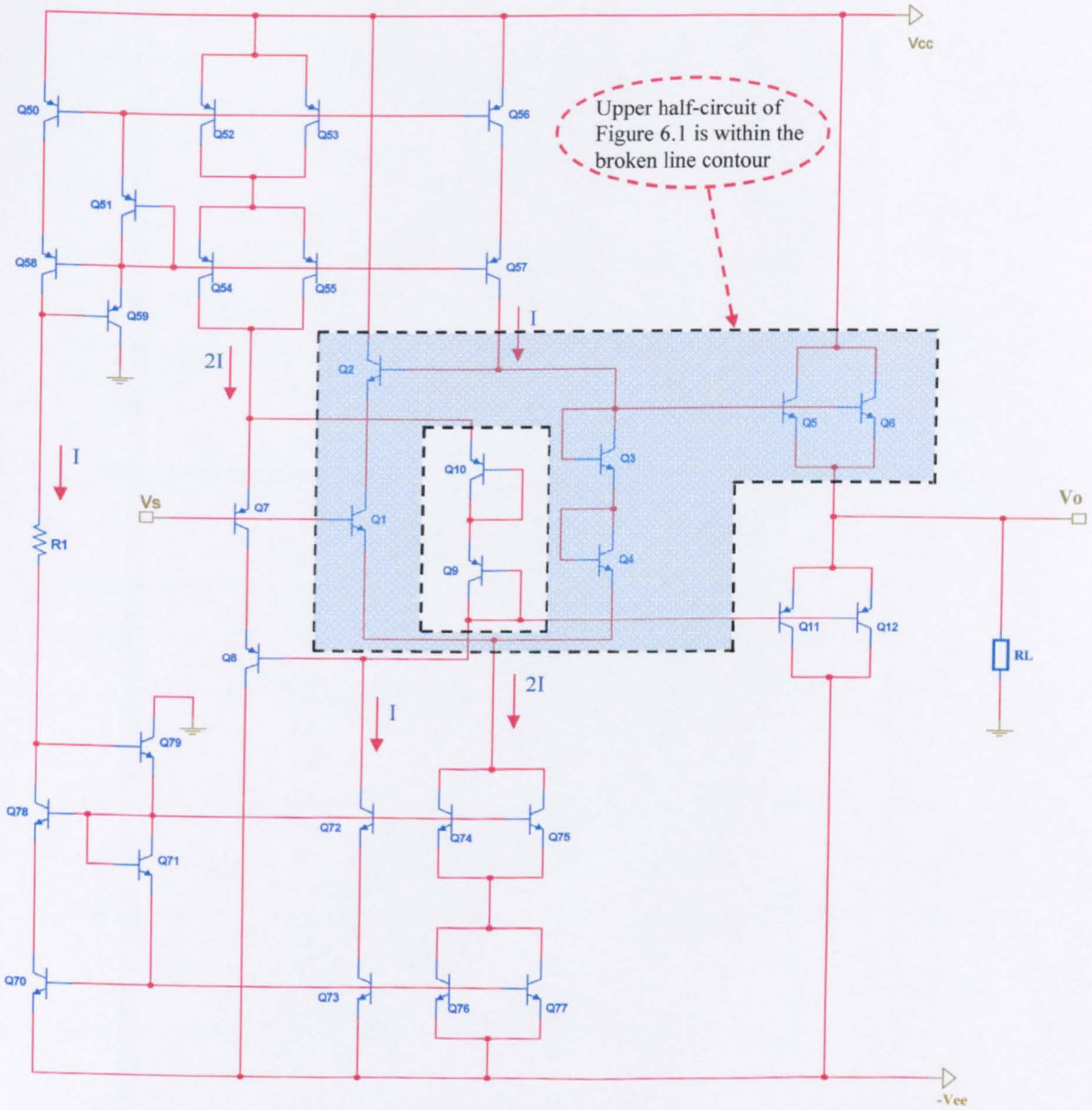

Fig. 6.2 Full circuit of VFB/1

The simulated transfer characteristic of the VFB/1 is shown in Figure 6.3 and has a slope of unity as expected. Figure 6.4 shows that the linear input range is approximately ±1V. This corresponds to: $(V_{CC} - 3V_{BE}) > V_S > -(V_{EE} - 3V_{BE})$ if substitute $V_{CC} = V_{EE} = 3.3V$, $V_{BE} = 0.75V$.

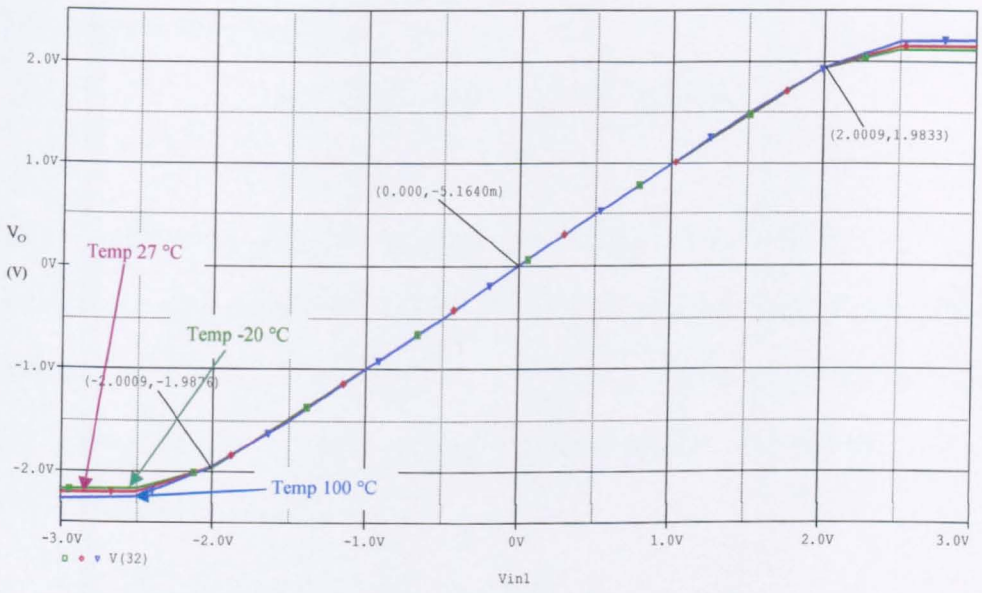

Fig. 6.3 Simulated transfer characteristic for circuit of Figure 6.2 : $V_{CC} = 3.3V; I_o = 1mA; R_L = \infty$

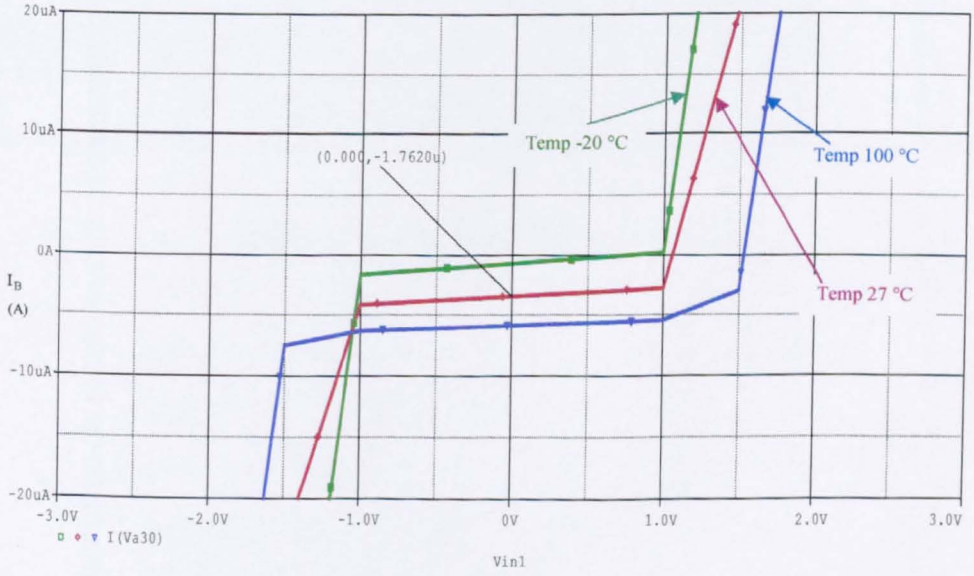

Fig. 6.4 Input current of the circuit of Figure 6.2 for $V_{CC} = 3.3V; I_o = 1mA; R_L = \infty$

The quiescent power dissipation of the circuit is,

$$P_Q = (V_{CC} + V_{EE}) \cdot I_Q \cdot n \tag{6.5}$$

where n is the number of vertical conduction paths between the two rail supplies.

Substituting on (6.5) for 27°C ,

$$P_Q = (3.3V + 3.3V) \cdot 1mA \cdot 8 = 52.8mW$$

Table 6.1 shows the simulated quiescent power dissipation of Figure 6.2 for three different operating temperatures. This shows good agreement with the calculated value at T=27°C. Increasing/decreasing the operating temperature affects the current gain of the transistors, resulting different operating currents, consequently different power dissipation.

Quiescent power dissipation P_Q **(mW)**			
Operating temperature (°C)	**-20**	**27**	**100**
	47.8	53.6	62.8

Table 6.1 Quiescent power dissipation of the circuit

6.4 Small-signal voltage-gain

The frequency response for the voltage-gain shows peaking even with no load. This is attributed to feedback in the half-circuits and the cascade of the emitter-followers.

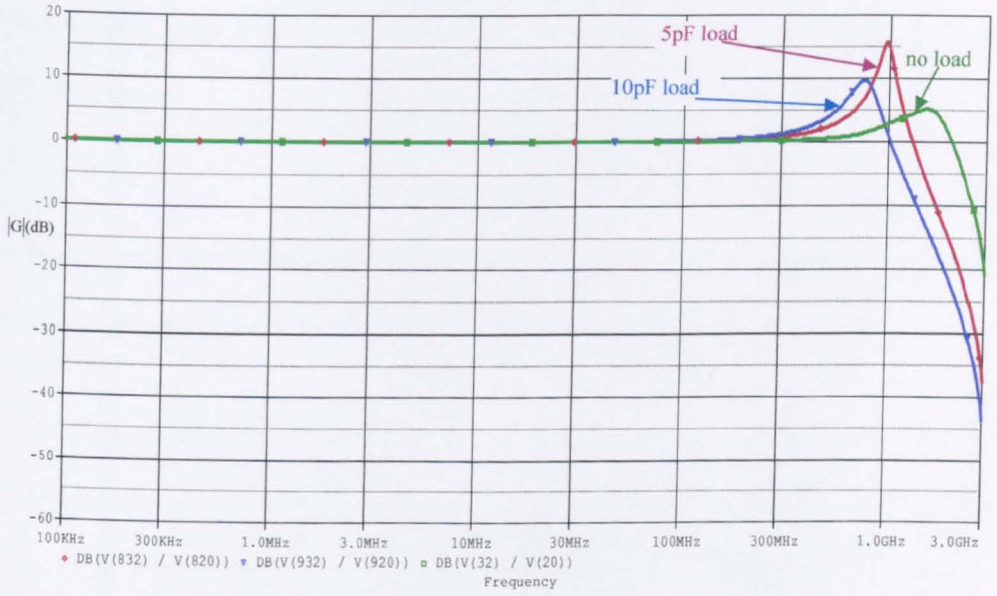

Fig. 6.5 Frequency response for the small-signal voltage-gain $|G|$ of VFB/1, with different loads

6.5 Incremental input impedance

The incremental input impedance of the VFB/1 is shown in Figure 6.6. Theoretically, its magnitude is given by,

$$Z_i = (\beta_n + 1)[(\beta_n + 1)R_L // R_{source} // R_{sink}] // (\beta_p + 1)[(\beta_p + 1)R_L // R_{source} // R_{sink}] \quad (6.6)$$

Substituting data from Chapter 3, sections 3.2.2 and 3.3.3, the theoretical input impedance is,

$$Z_i \approx 2.96M\Omega$$

which is in good agreement with the simulated value at T=27°C as shown in Table 6.2 which displays spot values for $|Z_i|$ as a function of f and T.

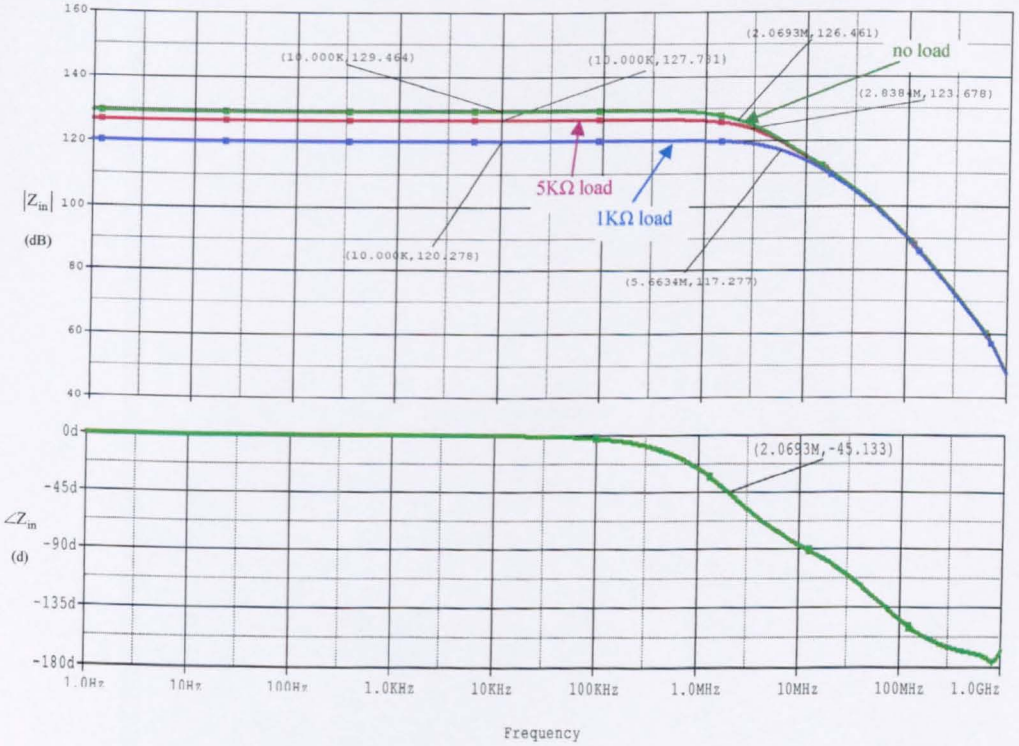

Fig. 6.6 Bode plots for $|Z_i|$ and $\angle Z_i$ for $I_C = 1mA$ for several loads

The input capacitance, derived from the -3dB frequency (2.069MHz), is now $C_{in} \approx 35fF$, due to the bootstrapping of the input transistors.

Conditions	$\|Z_i\|$ **(Ω)**					
Operating temperature (°C)	**-20**	**27**	**100**	**-20**	**27**	**100**
f = 312.5KHz	2.06M	2.94M	4.62M	1.67M	2.45M	4.02M
f = 31.25MHz	150K	181K	222K	150K	180K	220K
f = 250MHz	6.6K	6.5K	6K	6.5K	6.4K	5.9K
Output load	$R_L = \infty$			$R_L = 5K\Omega$		

Table 6.2 $|Z_i|$ of the VFB/1; $V_{CC} = V_{EE} = 3.3V$; $R_L = \infty$; $R_L = 5K\Omega$, as a function of f and T

6.6 Incremental output impedance

Figure 6.7 shows Z_o and $\angle Z_o$ as a function of frequency. Due to the emitter-follower output stage, the behaviour of the output is resistive at low frequencies and inductive at high frequencies. Spot values for Z_o as a function of f and T are shown in Table 6.3.

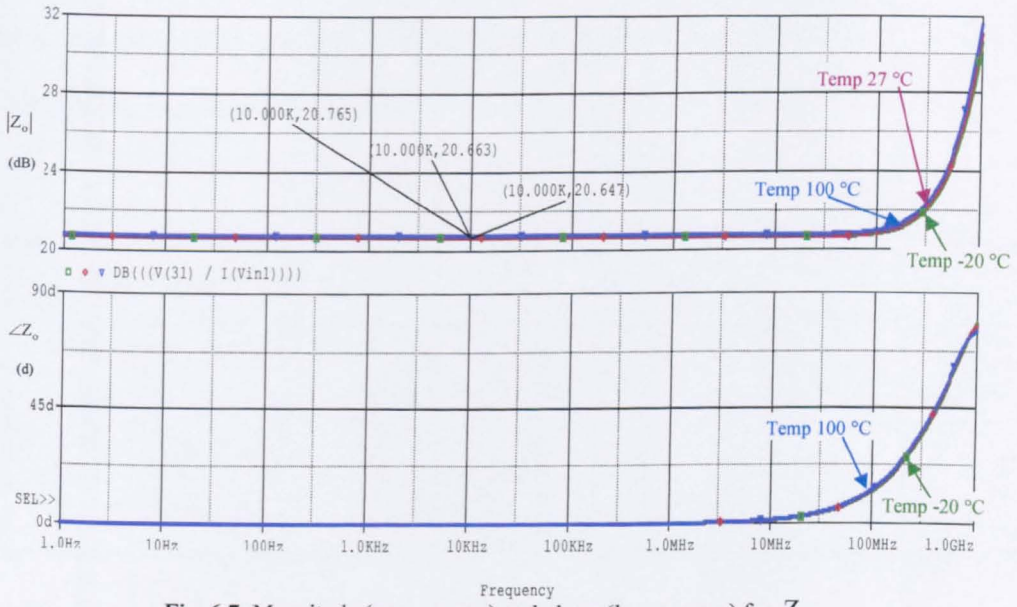

Fig. 6.7 Magnitude (upper curve) and phase (lower curve) for Z_o

Conditions	$\|Z_o\|$ **(Ω)**		
Operating temperature (°C)	**-20**	**27**	**100**
f = 312.5KHz	10.7	10.8	10.9
f = 31.25MHz	10.7	10.8	10.9
f = 250MHz	12	12.2	12.4

Table 6.3 $|Z_o|$ of the VFB/1 as a function of f and T

6.7 Total harmonic distortion and intermodulation distortion

Tables 6.4 to 6.6 show, respectively, THD under specified conditions at 312.5KHz, 31.25MHz and 250MHz. The performance is superior to the 'Super-follower' circuit, considered in the previous chapter. It can be observed that the circuit performance is poorer at higher frequencies mainly due to the finite output capacitance of the bias circuits which increase with the operating frequency. IMD performance results for the VFB/1, as a function of operating frequency and temperature, are shown in Table 6.7.

Conditions	**THD (dB)**		
Operating temperature (°C)	**-20**	**27**	**100**
$Z_L = 5K\Omega$	-92.1	-91.2	-90.2
$Z_L = 5K\Omega // 5pF$	-91	-86.8	-84.2

Table 6.4 THD at 312.5KHz

Conditions	**THD (dB)**		
Operating temperature (°C)	**-20**	**27**	**100**
$Z_L = 5K\Omega$	-73.3	-72.7	-76.9
$Z_L = 5K\Omega // 5pF$	-73.4	-75.8	-73.3

Table 6.5 THD at 31.25MHz

Conditions	THD (dB)		
Operating temperature (°C)	-20	27	100
$Z_L = 5K\Omega$	-66.6	-67	-67.6
$Z_L = 5K\Omega // 5pF$	-69.3	-70	-69.6

Table 6.6 THD at 250MHz

Conditions	IMD (dB)		
Operating temperature (°C)	-20	27	100
f = 312.5KHz	-64.4	-64.4	-64.3
f = 31.25MHz	-67.8	-67.3	-67.7
f = 250MHz	-60.1	-61.3	-62.1

Table 6.7 IMD results for the VFB/1, as a function of f and T.

6.8 Noise performance

The noise performance of the VFB/1 is shown in Figure 6.8. It is worth noting that the input referred noise is considerably low, compared to the input signal.

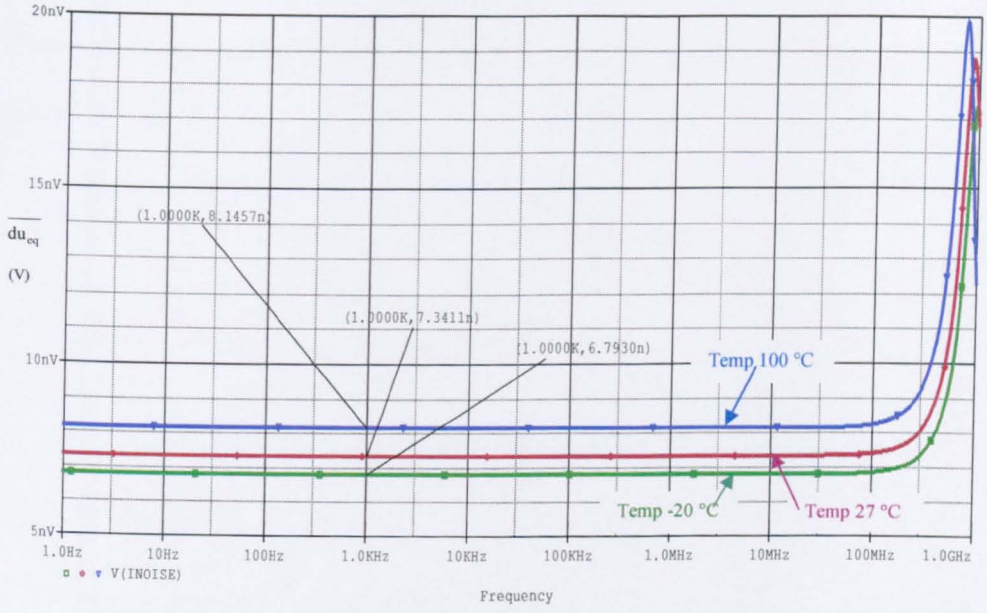

Fig. 6.8 Input noise of the circuit

6.9 Pulse response

Figures 6.9 and 6.10 show, respectively, the pulse response of the VFB/1, for 1nS and 0.1nS rise and fall times. The circuit performance is understandable in the light of the discussion on the pulse response of the conventional EF in Chapter 4. The horizontal scale used to present the pulse response for 0.1nS rise and fall times (Figure 6.10) is half of that for 1ns rise and fall times for the convenience of the reader.

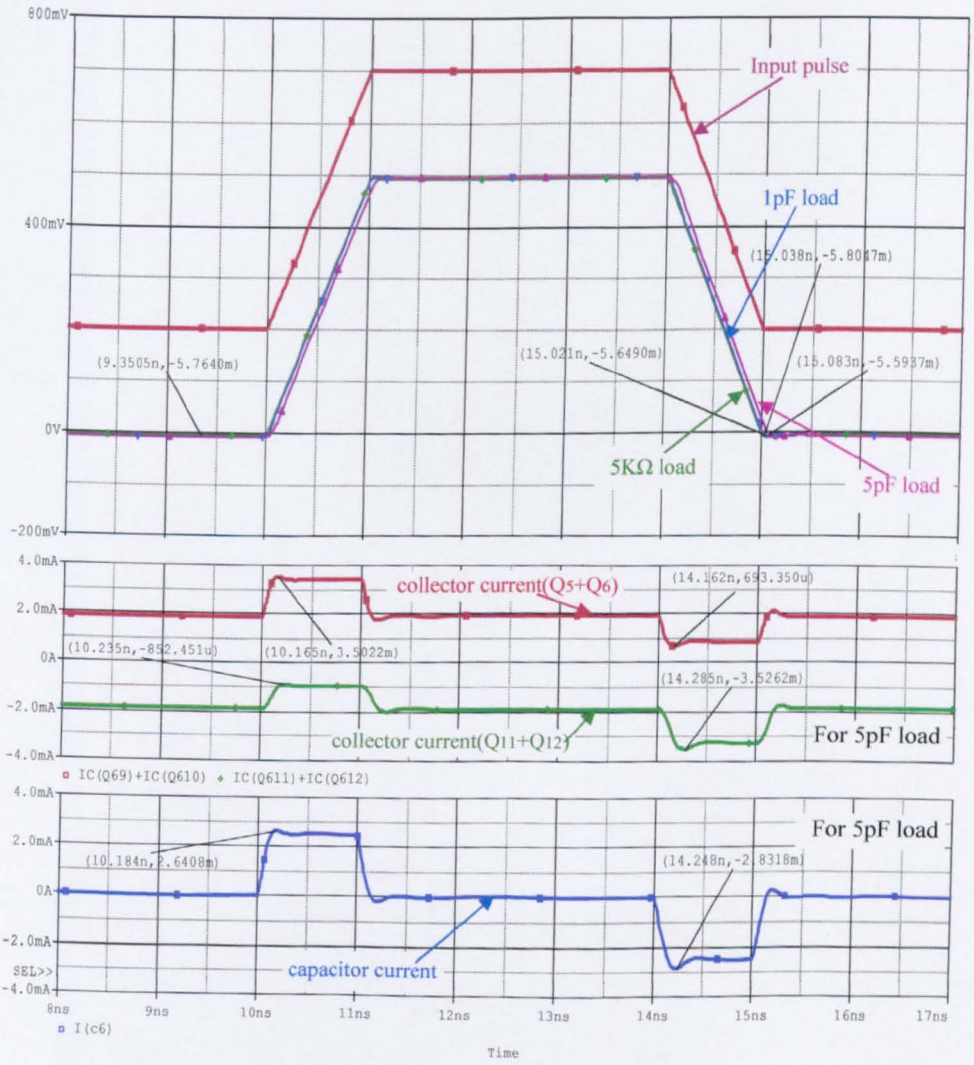

Fig. 6.9 Pulse response for an input signal with 1nS rise and fall times

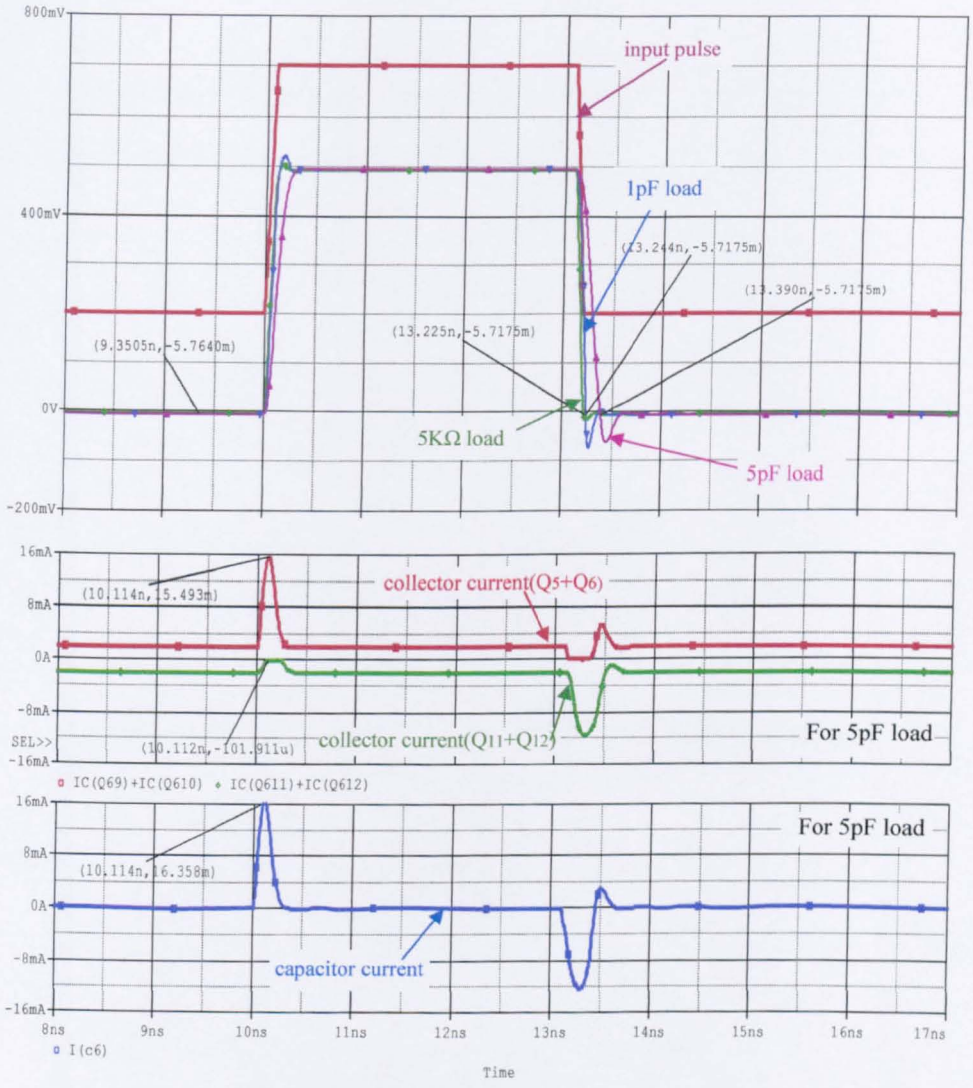

Fig. 6.10 Pulse response for an input signal with 0.1nS rise and fall times

6.10 Basis of the VFB/2

The starting point for the design of the VFB/2 is shown in Figure 6.11. This differs from the circuit in Figure 6.1 in that the collector of Q_1 is not bootstrapped.

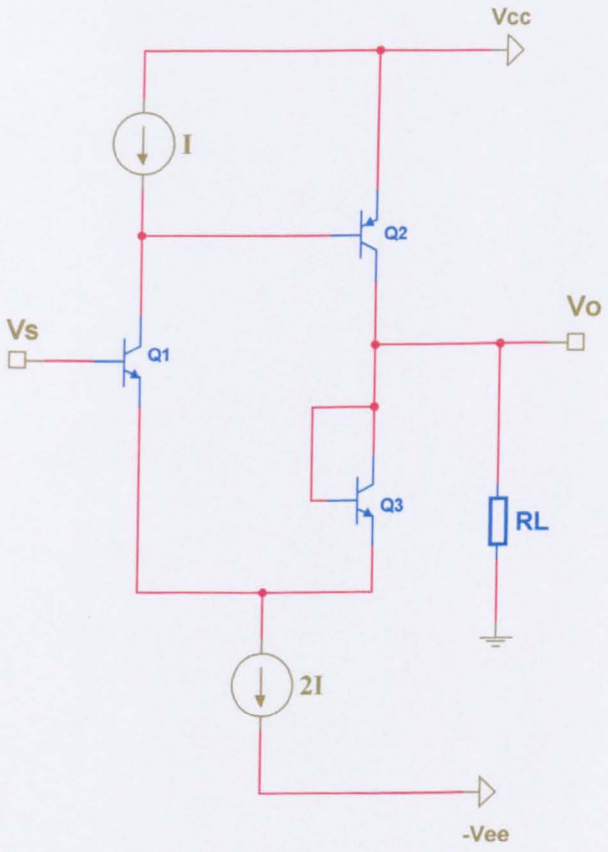

Fig. 6.11 Starting point for VFB/2

6.11 The VFB/2 / DC conditions

The full circuit of the VFB/2, shown in Figure 6.12, utilizes the circuit of Figure 6.1 and its complementary counterpart.

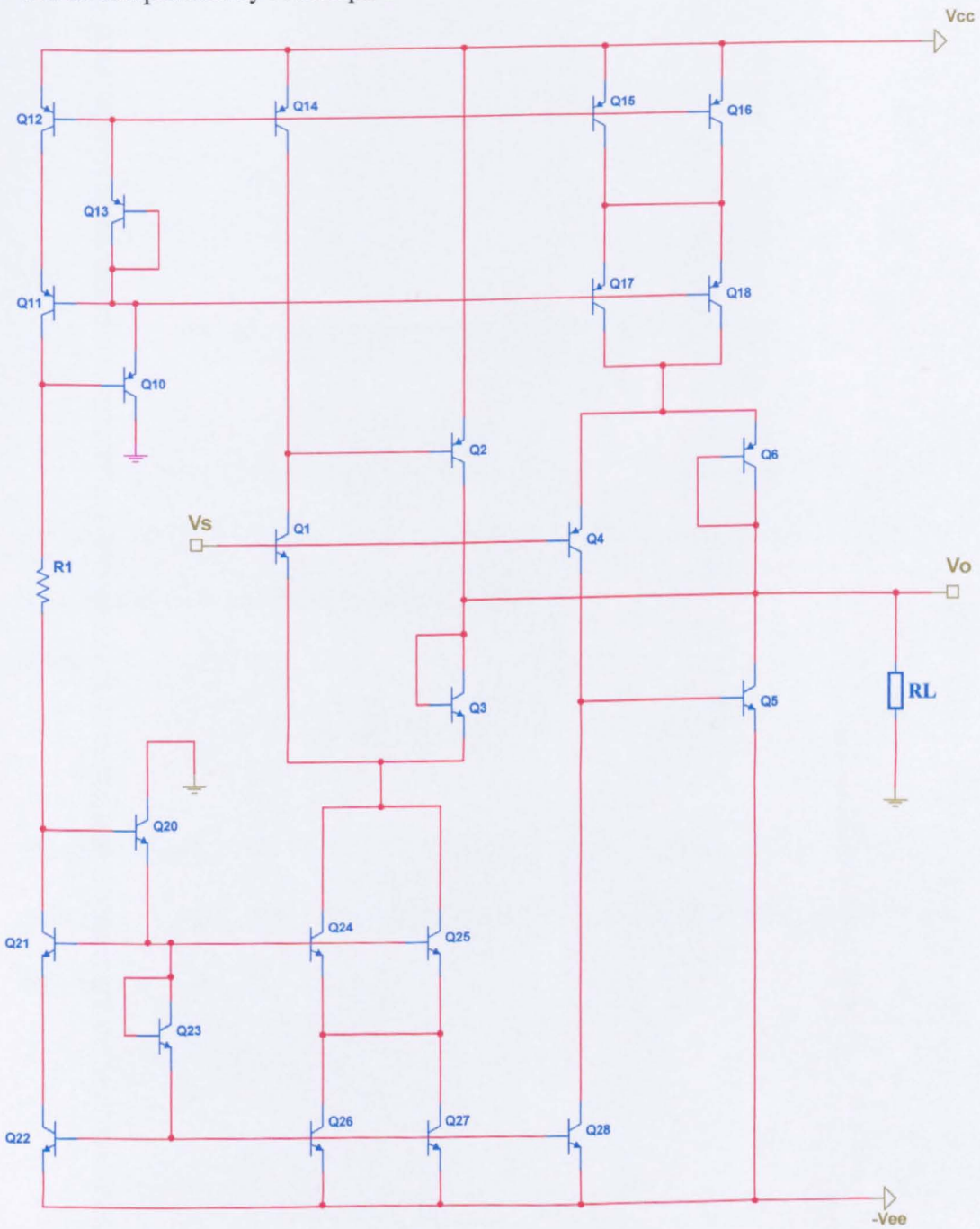

Fig. 6.12 Full circuit of VFB/2

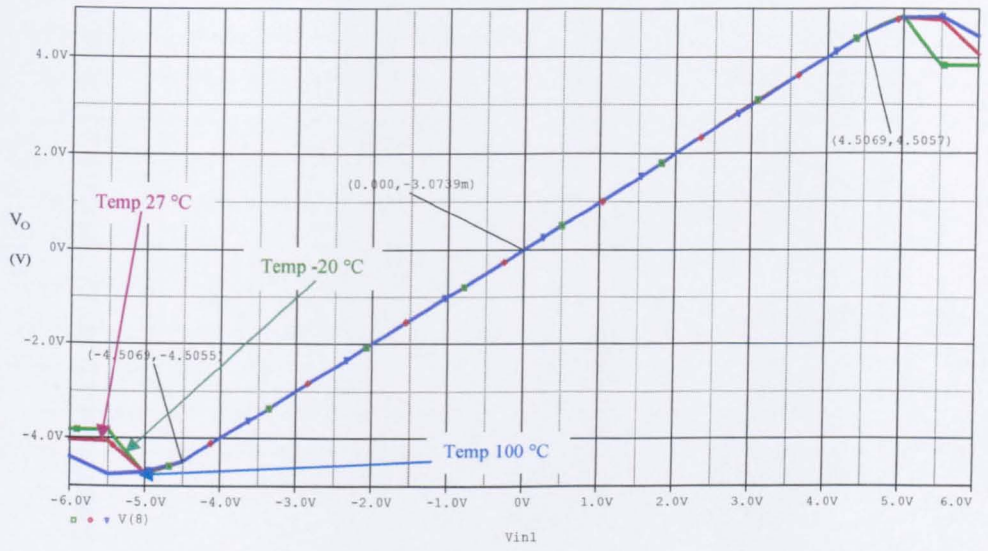

Fig. 6.13 Simulated transfer characteristic for circuit of Figure 6.12

$V_{CC} = V_{EE} = 5V; I_o = 1mA; R_L = \infty$

The linear input voltage range, shown in Figure 6.13, is set by the V_{BE1} of Q_1 (or V_{EB2} of Q_2), and the minimum allowable voltage V_K, say, across the current bias circuits, for them to operate outside saturation.

Thus,

$$(+V_{CC} - V_{EB1} - V_K) > V_S \geq (-V_{CC} + V_{BE2} + V_K) \qquad (6.7)$$

Figure 6.14 shows $+3V \geq V_S \geq -3V$, which is in fair agreement with the theoretical values for $V_{BE} \approx 0.75V$. The increase in I_B with V_S is attributed as in previous circuits to the temperature-variation of β_n and β_p.

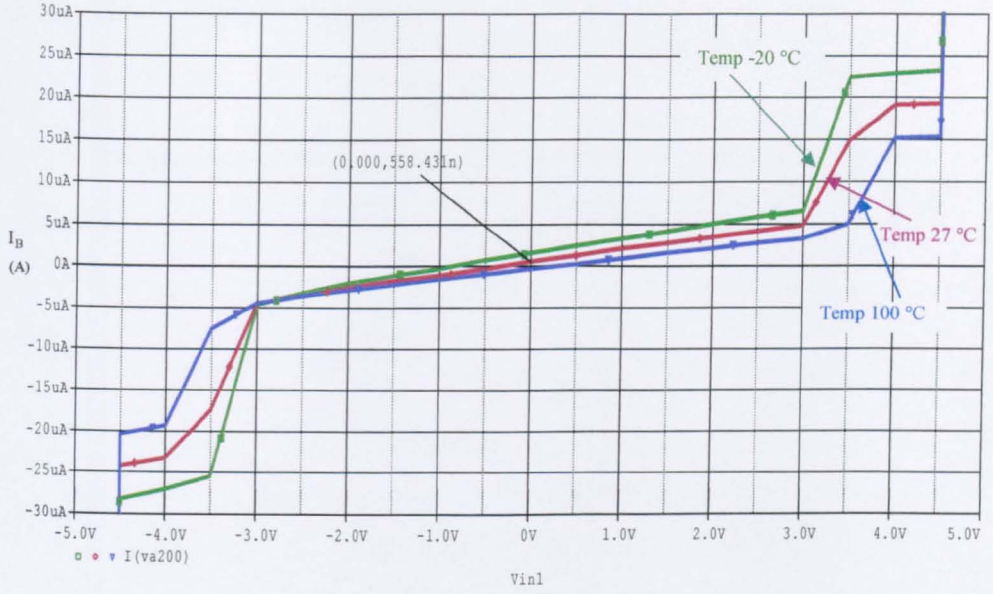

Fig. 6.14 Input current of the circuit of Figure 6.12 for $V_{CC} = V_{EE} = 5V; I_o = 1mA; R_L = \infty$

The quiescent power dissipation of the VFB/2 is,

$$P_Q = (V_{CC} + V_{EE}) \cdot I_Q \cdot n \tag{6.8}$$

where n is the number of vertical conduction paths between the two rail supplies.

Biasing the circuit with ideal sources, at 27°C , $P_Q = (5V + 5V) \cdot 1mA \cdot 5 = 50mW$.

Simulated values for P_Q is shown in Table 6.8. This shows fair agreement with the calculated values at T=27 °C.

Quiescent power dissipation P_Q **(mW)**			
Operating temperature (°C)	**-20**	**27**	**100**
	46	55.4	70.4

Table 6.8 Quiescent power dissipation of the VFB/2

6.12 Small-signal voltage-gain

The small signal voltage-gain of the VFB/2 is shown in Figure 6.15 over the frequency range. The cascade of the emitter-followers results in peaking, similar to the VFB/1 circuit. This peaking is a typical characteristic of voltage-follower designs.

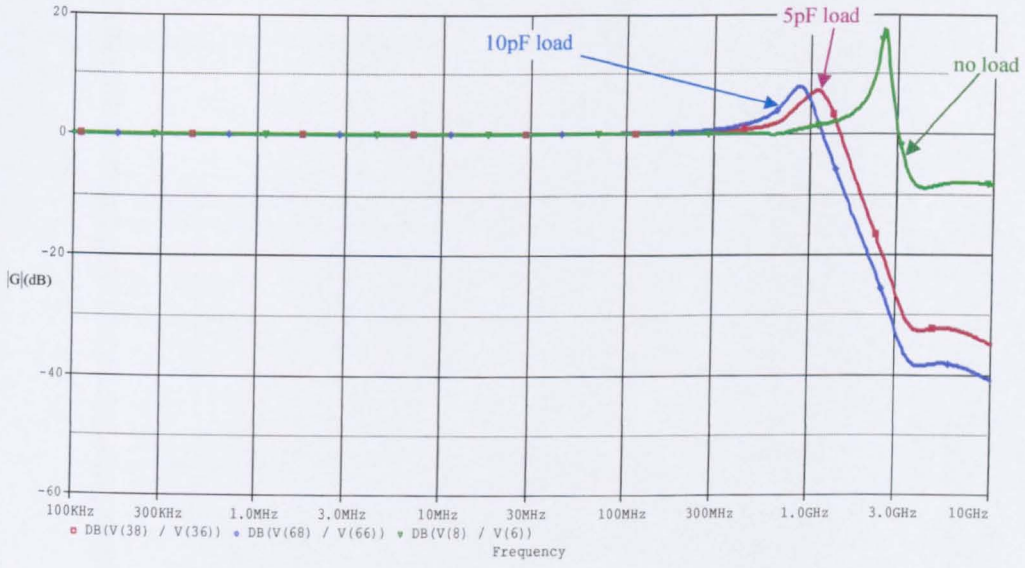

Fig. 6.15 Frequency response for the small signal gain G of the VFB/2 with different loads

6.13 Incremental input impedance

The incremental input impedance of the VFB/2 is shown in Figure 6.16. This is poor compared with the VFB/1 because of the nature of the path between input and output. The input capacitance, derived from the -3dB frequency (2.838MHz), is $C_{in} \approx 85fF$, over double of VFB/1 because of the absence of bootstrapping of the input transistors. Spot values for $|Z_i|$ as a function of f and T are shown in Table 6.9.

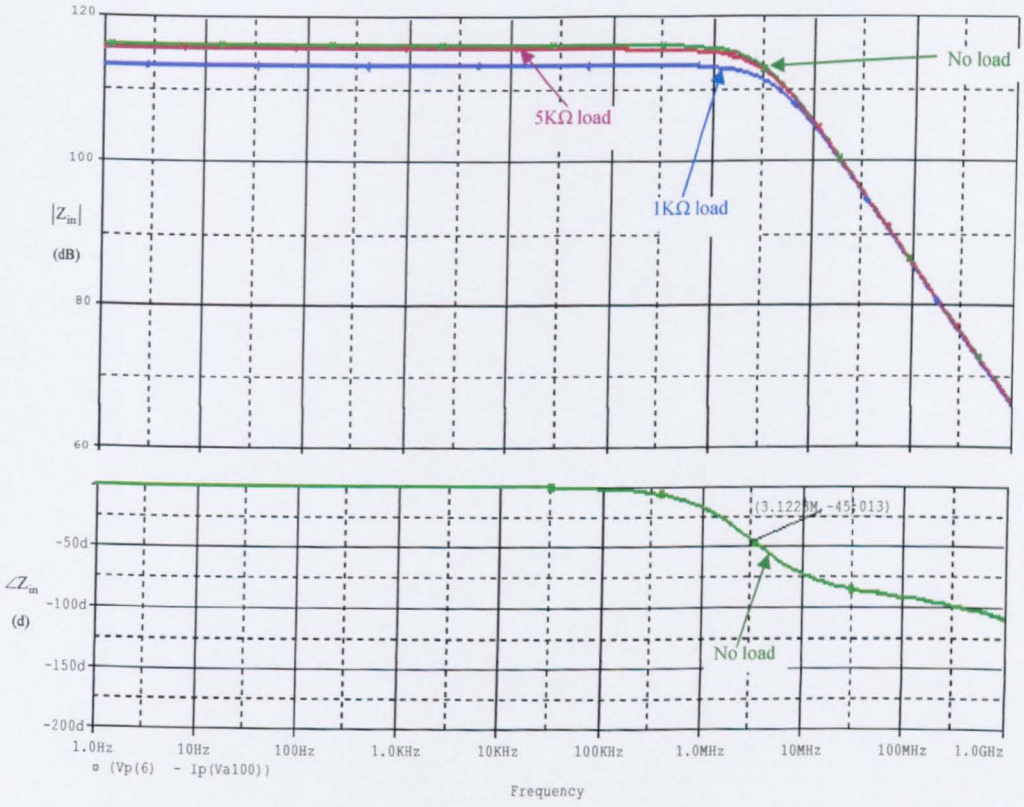

Fig. 6.16 Bode plots for $|Z_i|$ and $\angle Z_i$ for $I_C = 1mA$ and several loads

Conditions	$\|Z_i\|$ **(Ω)**					
Operating temperature (°C)	**-20**	**27**	**100**	**-20**	**27**	**100**
f = 312.5KHz	533K	637K	797K	510K	593K	721K
f = 31.25MHz	63.6K	63.7K	64.4K	63.2K	63K	63.7K
f = 250MHz	8K	8K	8K	8K	7.9K	7.9K
Output load	$R_L = \infty$			$R_L = 5K\Omega$		

Table 6.9 $|Z_i|$ of the VFB/2 with $R_L = \infty$ as a function of f and T

6.14 Incremental output impedance

Figure 6.17 shows Z_o and $\angle Z_o$ as a function of frequency. This is resistive at low frequencies and inductive, at higher frequencies, because of the emitter-follower output stage. Spot values for $|Z_o|$ as a function of f and T are shown in Table 6.10.

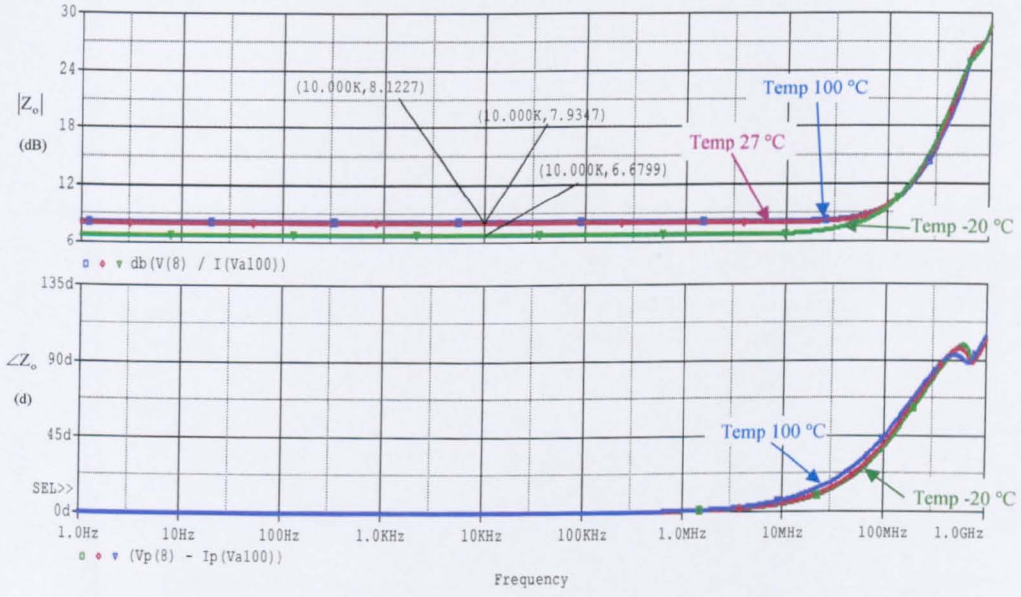

Fig. 6.17 Magnitude (upper curve) and phase (lower curve) for Z_o

Conditions	$\|Z_o\|$ **(Ω)**		
Operating temperature (°C)	**-20**	**27**	**100**
f = 312.5KHz	2.1	2.4	2.5
f = 31.25MHz	2.3	2.5	2.6
f = 250MHz	5.5	5.3	5.1

Table 6.10 $|Z_o|$ of the VFB/2 as a function of f and T

6.15 Total harmonic distortion and intermodulation distortion

Tables 6.11, 6.12 and 6.13 show, respectively, THD of the VFB/2 under specified conditions at 312.5KHz, 31.25MHz and 250MHz. It is worth noting that the distortion is kept in low levels, even at higher frequencies, due to the wide linear input voltage range. Table 6.14 shows IMD performance results as a function of operating frequency and temperature..

Conditions	**THD (dB)**		
Operating temperature (°C)	**-20**	**27**	**100**
$Z_L = 5K\Omega$	-89.4	-89.9	-88
$Z_L = 5K\Omega // 5pF$	-78.3	-79.9	-79.8

Table 6.11 THD at 312.5KHz

Conditions	**THD (dB)**		
Operating temperature (°C)	**-20**	**27**	**100**
$Z_L = 5K\Omega$	-80.3	-86.8	-82
$Z_L = 5K\Omega // 5pF$	-67.4	-63.9	-61.2

Table 6.12 THD at 31.25MHz

Conditions	THD (dB)		
Operating temperature (°C)	-20	27	100
$Z_L = 5K\Omega$	-74.9	-70.8	-65.6
$Z_L = 5K\Omega // 5pF$	-71.1	-62	-56.4

Table 6.13 THD at 250MHz

Conditions	IMD (dB)		
Operating temperature (°C)	-20	27	100
f = 312.5KHz	-88.2	-87.6	-88.7
f = 31.25MHz	-84.4	-84.4	-84.2
f = 250MHz	-59.2	-66	-56.8

Table 6.14 IMD results for the VFB/2 as a function of f and T.

6.16 Noise performance

The input referred noise of the VFB/2 is shown in Figure 6.18. This is reduced, compared with the VFB/1 of Figure 6.2, mainly due to the reduced amount of devices used throughout the signal path.

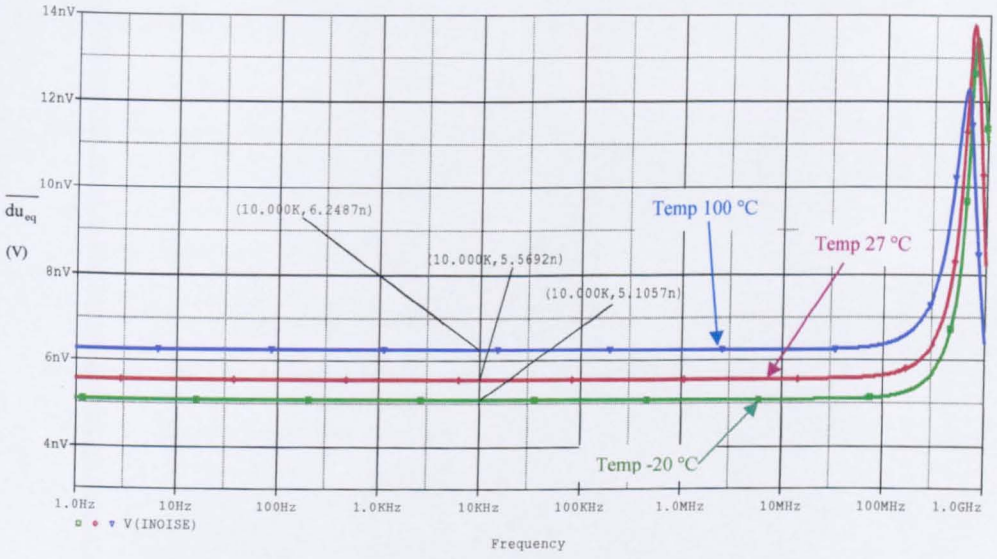

Fig. 6.18 Input noise of the VFB/2

6.17 Pulse response

Figures 6.19 and 6.20 show the pulse response of the VFB/2, for 1nS and 0.1nS rise and fall times, respectively. The performance can be understood by reference to the discussion of the pulse response of the conventional EF in Chapter 4. In addition, the ringing observed is contributed to the output stage of the circuit which comprises two low impedance points joint together.

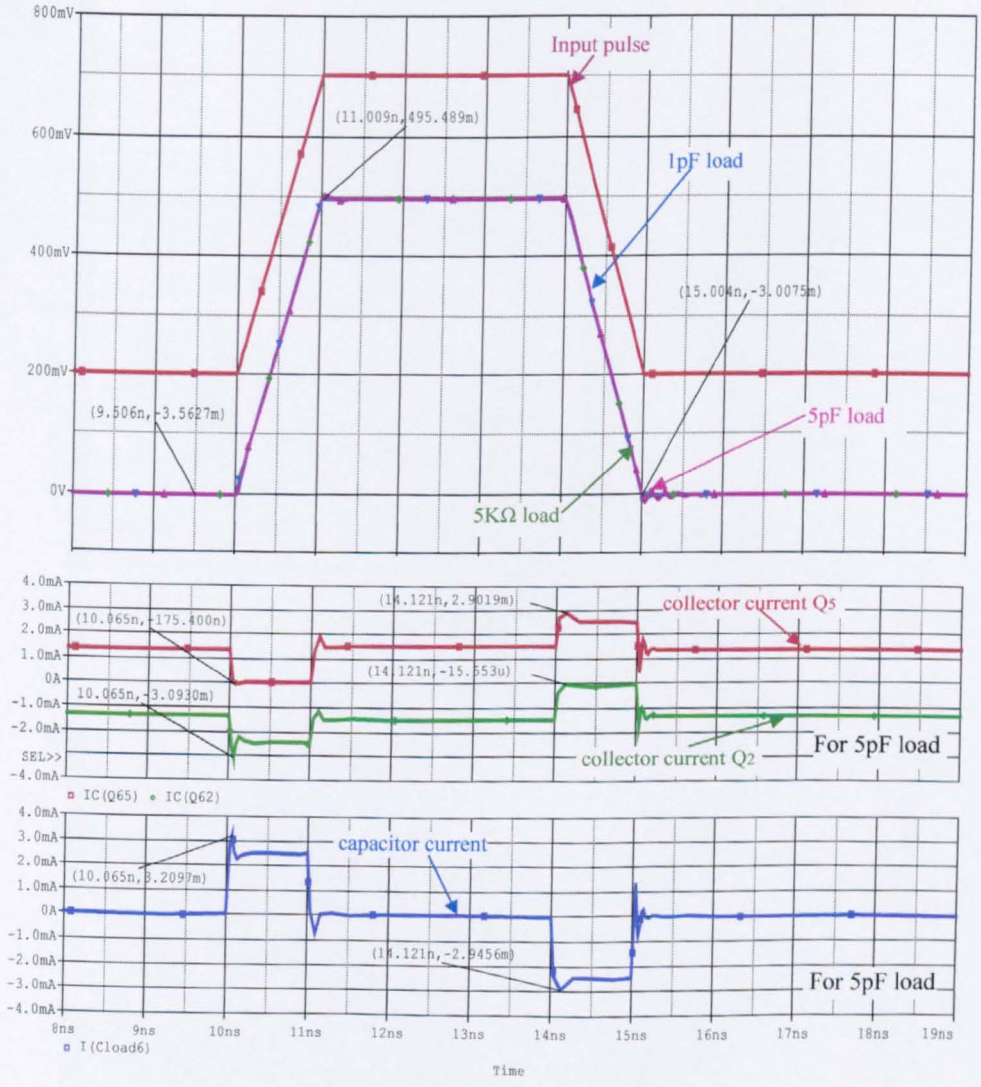

Fig. 6.19 Pulse response for an input signal with 1nS rise and fall times

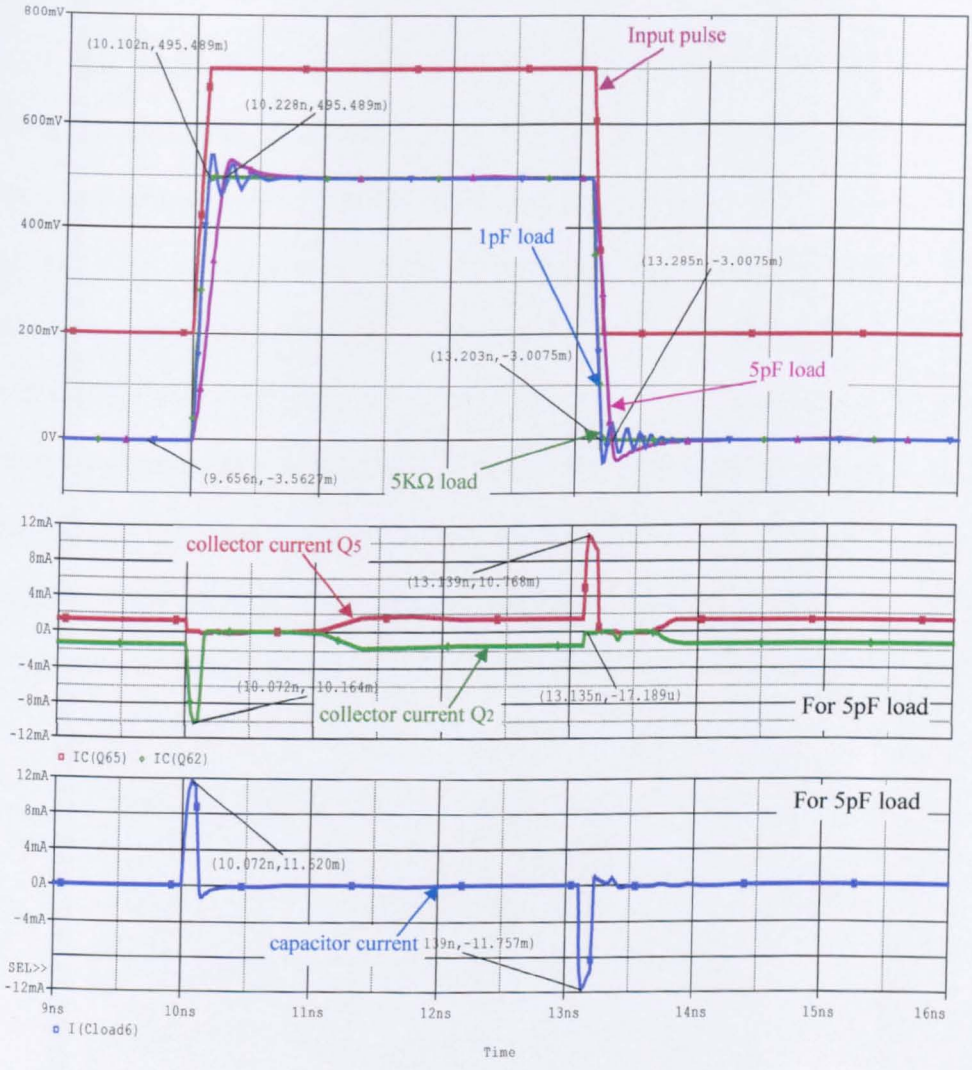

Fig. 6.20 Pulse response for an input signal with 0.1nS rise and fall times

6.18 Summary of Chapter 6

This chapter has considered the design and performance of two new types of voltage-followers, the VFB/1 and VFB/2. The two types are similar in that they both use complimentary half-circuits but differ in the configuration of the half-circuit and the way they are connected. This accounts for their difference in their input impedance, output impedance and pulse response. The half circuit design, in each case, requires the use of two levels of current bias, one twice the other. A low offset voltage is achieved by matching in the base-emitter voltage drops of transistors of the same polarity rather than matching in the voltage drops of a diode pair comprising one transistor of each polarity as in the 'Super follower' of the previous chapter. Both new designs have been reported by the author in the technical literature **[6-2 to 6-5]**.

References for Chapter 6

[6-1] Gray R.P., Hurst J.P., Lewis H.S., Meyer G.R., 'Analysis and Design of Analog Integrated Circuits', John Wiley and Sons, 4th Edition, New York, 2001, pp.309-313.

[6-2] Charalampidis N., Hayatleh K., Hart B.L., Lidgey F.J., 'A low distortion, high slew rate, voltage-follower', IEEE Proceedings of International Technical Conference on Circuits/Systems, Computers and Communications, ITC-CSCC 2006, Chiang Mai, Thailand, July 2006, Vol. III, pp.761-764.

[6-3] Charalampidis N., Hayatleh K., Hart B.L., Lidgey F.J., 'A high-speed low-distortion voltage-follower', IEEE Proceedings of International Conference on Electrical and Electronics Engineering, ICEEE 2006, Veracruz, Mexico, Sept. 2006, pp.178-181.

[6-4] Charalampidis N., Hayatleh K., Hart B.L., Lidgey F.J., 'A wide bandwidth voltage-follower with low distortion and high slew rate', IEEE Proceedings of International Conference on Electronics, Circuits and Systems, ICECS 2006, Nice, France, Dec. 2006.

[6-5] Charalampidis N., Hayatleh K., Hart L.B., Lidgey F.J., 'High-frequency voltage-follower designs based on local feedback techniques', IEEE Proceedings of IEE ASP2006, Oxford, UK, 2006, pp.poster2-1 to poster2-6.

CHAPTER 7

V.F. Type C / V.F with global feedback

7.1 Introduction

The previous chapters have dealt with VFs using local feedback. This chapter discuss the design and development of a different type of VF, one using global feedback and called here, for convenience, a VF Type C or VF/C. A popular form for a VF with global feedback is a voltage operational amplifier ('op-amp') with 100% negative feedback. Unfortunately, such a scheme is unable to meet the VF specifications of this thesis with currently available op-amps. However a stripped-down version of an op-amp, using a long-tailed pair input stage followed by a 'Diamond' circuit output stage suggests itself as a possibility. It is that configuration that is pursued further now.

The chapter starts with an analysis of the core of the proposed circuit, presenting some of its performance parameters, followed by the proposed circuit and the modifications adopted to improve performance. A thorough investigation of the stability of the proposed circuit is carried out and the final circuit is evaluated similarly to the circuits of the previous categories. The chapter finishes with a comparison of the VF designs presented in this work and comments about their performance and trade-offs.

7.2 Starting point of the proposed design / DC and AC conditions

The starting point of the proposed design is shown in Figure 7.1. A single stage, long-tailed pair amplifier is followed by an emitter-follower which provides the required feedback **[7-1]**, **[7-2]**. Relevant voltage and currents are labelled for the DC analysis that follows.

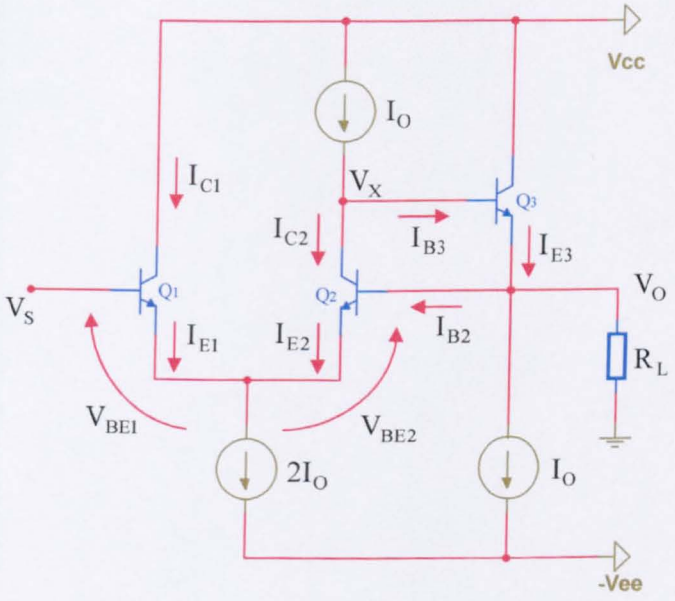

Fig. 7.1 Core circuit of the proposed follower, labelled for a DC analysis

I_{E2} cannot exceed $2I_O$ because that would mean that Q_1 is cut off. Hence,

$$I_{B2} < \frac{2I_O}{(1+\beta)} \tag{7.1}$$

But,

$$I_{E3} = I_{B2} + I_O + \frac{V_O}{R_L} \tag{7.2}$$

Hence,

$$I_{B3} < \frac{2I_O}{(1+\beta)^2} + \frac{I_O}{(1+\beta)} + \frac{V_O}{(1+\beta)R_L} \tag{7.3}$$

Assuming that V_O is very small (checked later for consistency) and ignoring the first term in (7.3) compared with the second term,

$$I_{B3} \approx \frac{I_O}{(1+\beta)} \tag{7.4}$$

Consequently,

$$I_{C2} = I_O - \frac{I_O}{(1+\beta)} = \alpha I_O \tag{7.5}$$

and,

$$I_{E2} = \frac{1}{\alpha}(\alpha I_O) = I_O \tag{7.6}$$

$$\therefore \quad I_{E1} = I_O \tag{7.7}$$

and,

$$\therefore \quad I_{C1} = \alpha I_O \tag{7.8}$$

On the basis of the approximations made $I_{C1} = I_{C2}$

But,

$$V_{OS} = V_{BE1} - V_{BE2} = V_T \log_e \frac{I_{C1}}{I_{C2}} \tag{7.9}$$

Hence,

$$V_{OS} = 0$$

In practise $V_{OS} \neq 0$ because of the approximations made but, as can be calculated from (7.9), it will approximately be of the order of 1mV or less.

7.2.1 Small-signal low-frequency gain, input resistance and output resistance

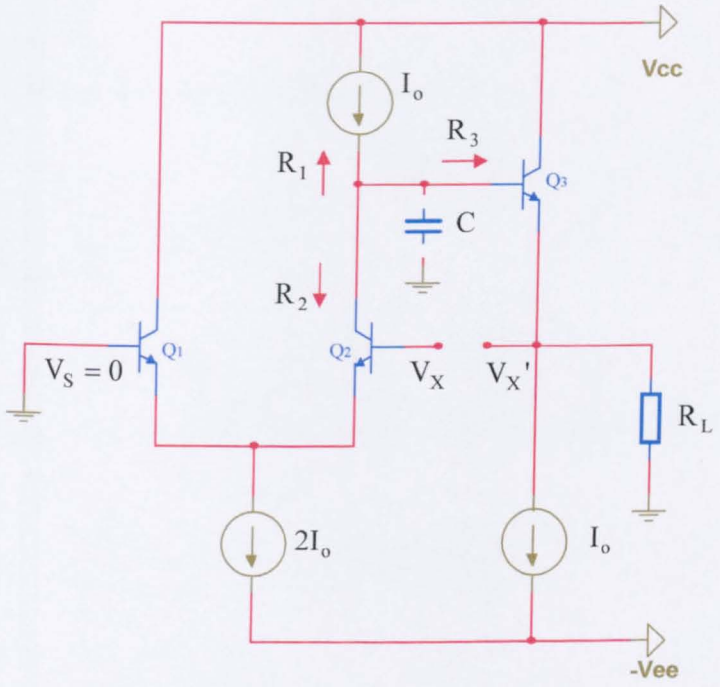

Fig. 7.2 Core circuit of the proposed follower, labelled for a small-signal low-frequency analysis

Figure 7.2 shows the circuit of Figure 7.1 labelled for an analysis of small-signal closed-loop gain G(0) and frequency response. At low frequencies all device, stray and any added capacitance (such as C) can be ignored. I_O determines the loop gain (the input is earthed) and the loop is broken at the point marked by the line cut. How this may be done in practice, or in simulation, and the precautions that must be taken are discussed later (See section 7.6).

R_1, R_2, R_3 represent, respectively, the incremental resistances looking into the collector current source for Q_2, the collector of Q_2, and the base of Q_3. A test voltage V_X applied at the base of Q_2, and voltage generated at point x' is observed.

By definition, the loop gain (L.G.) is given by,

$$\text{L.G.} = \frac{V_X'}{V_X} \tag{7.10}$$

By inspection,

$$\text{L.G.} = -A(0) \cdot G_V(0) \tag{7.11}$$

in which, $A(0)$ = l.f. differential voltage gain of the long-tailed pair

$$A(0) = -\frac{g_m R_X}{2} \tag{7.12}$$

where,

$$R_X = (R_1 // R_2 // R_3) \tag{7.13}$$

and, $G_V(0)$ = l.f. voltage gain of the emitter-follower stage.

Since $G_V(0)$ is close to unity it will be taken as such, for the time being,

$$\therefore \quad \text{L.G.} \approx -\frac{g_m R_X}{2} \tag{7.14}$$

From standard feedback theory **[7.3]** the low frequency gain $G(0)$ of the feedback amplifier is given by,

$$G(0) = \frac{A(0)}{[1 + A(0)]} \approx 1 \tag{7.15}$$

It is shown in Appendices AP7.1 and AP7.2 that the input R_{if} and output R_{of} resistances with feedback in terms of the input and output resistances without feedback are given as,

$$R_{if} = R_i[1 + A(0)] >> R_i \tag{7.16}$$

$$R_{of} = R_o/[1 + A(0)] << R_o \tag{7.17}$$

7.2.2 Frequency response

If C is large enough the open-loop frequency response is determined by R_X and C and the cut-off frequency, f_c, for small-signal gain is,

$$f_c = \frac{1}{2\pi R_X C} \tag{7.18}$$

This is true if f_c is well below the cut-off frequency of the transistors used.

The closed loop bandwidth is then given by,

$$f_c' = f_c[1 + A(0)] \tag{7.19}$$

The circuit of Figure 7.2 is not, as it stands, suitable for handling fast negative-going pulse edges for reasons given in Chapter 4 in the discussion of the emitter-follower response. This limitation is overcome in the proposed circuit, dealt with next, that incorporates a 'Diamond' output stage.

7.3 The proposed circuit, VF/C

The full circuit of the proposed circuit type VF/C is shown in Figure 7.3. The part within the dotted contour is the circuit core which is a development of Figure 7.1 and the currents shown labelled in the core apply for $V_S = 0$. The part outside the contour is the '6-pack' current biasing scheme, analysed in Chapter 3.

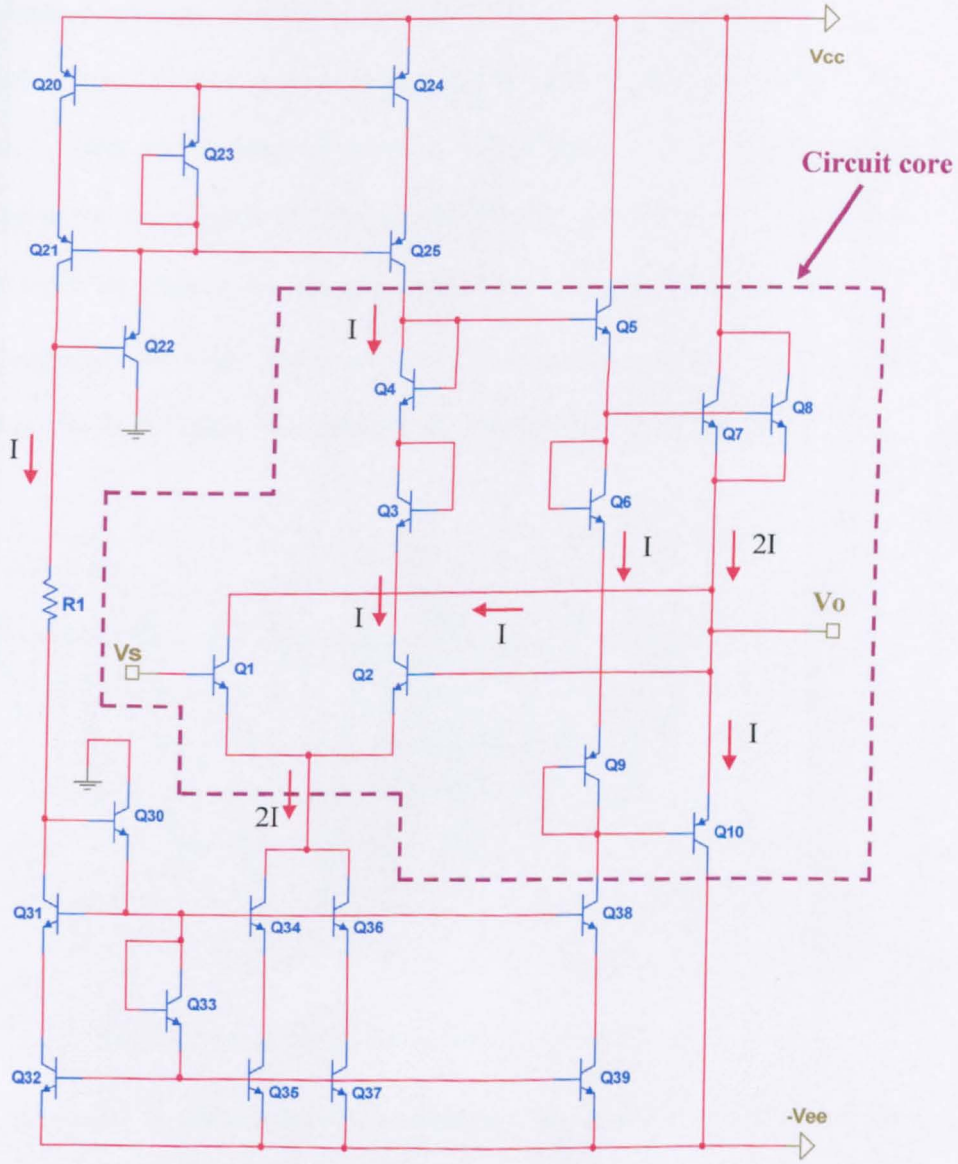

Fig. 7.3 Full circuit of VF/C ($V_{CC} = V_{EE} = 5V$; I = 1mA)

Comparing Figure 7.3 with Figure 7.1, Q_6 and Q_9 are added to provide suitable biasing for the complementary output stage. With $V_S = 0$, negative feedback ensures that $V_O \approx 0$ also, providing the transistors operate in the forward-active mode, with the DC current distribution shown. Now if $V_O = 0$, then the base of Q_5 is $2V_{BE}$ above earth potential. The inclusion of the diode-strapped transistor Q_3 and Q_4 ensures that the collector voltage of Q_2 is zero. Connecting the collector of Q_1 to the output terminal makes the collector voltage of Q_1 zero also. Q_7 and Q_8 are connected in parallel so that their base-emitter voltage is the same as the other transistors and each has a collector current of 1mA. The connections, indicated, provide bootstrapping for the collector of both Q_1 and Q_2, with the intention of providing an increased input impedance. The proposed circuit was simulated with $V_S = 0$ to check the DC conditions. However the output revealed the presence of sustained sinusoidal oscillations, shown in Figure 7.4, occurring at a frequency of approximately 4.2GHz.

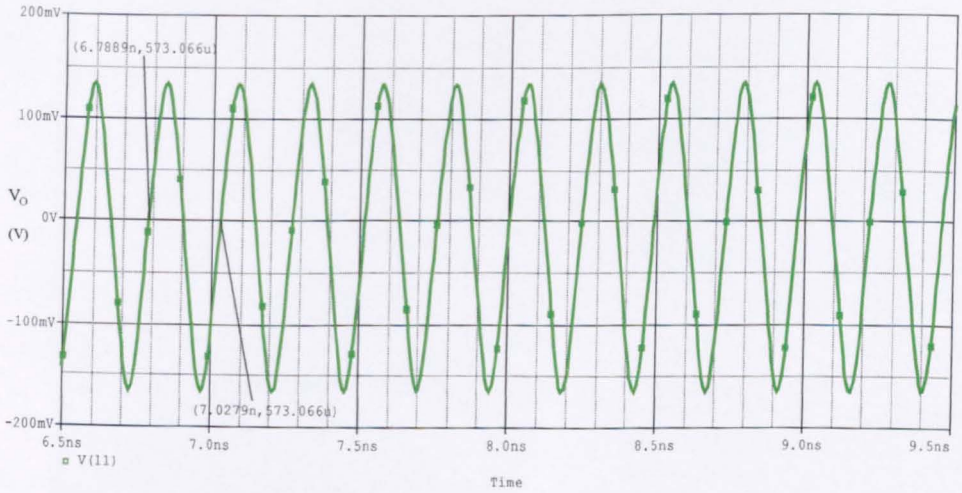

Fig. 7.4 Oscillations at the output of the circuit with $V_S = 0$

Accordingly, it was decided to investigate the stability of the circuit by examining the frequency variation of the magnitude and phase of the loop-gain.

7.4 Investigation of stability

Figure 7.5 shows the set-up used to plot the frequency variation of the loop-gain magnitude and phase.

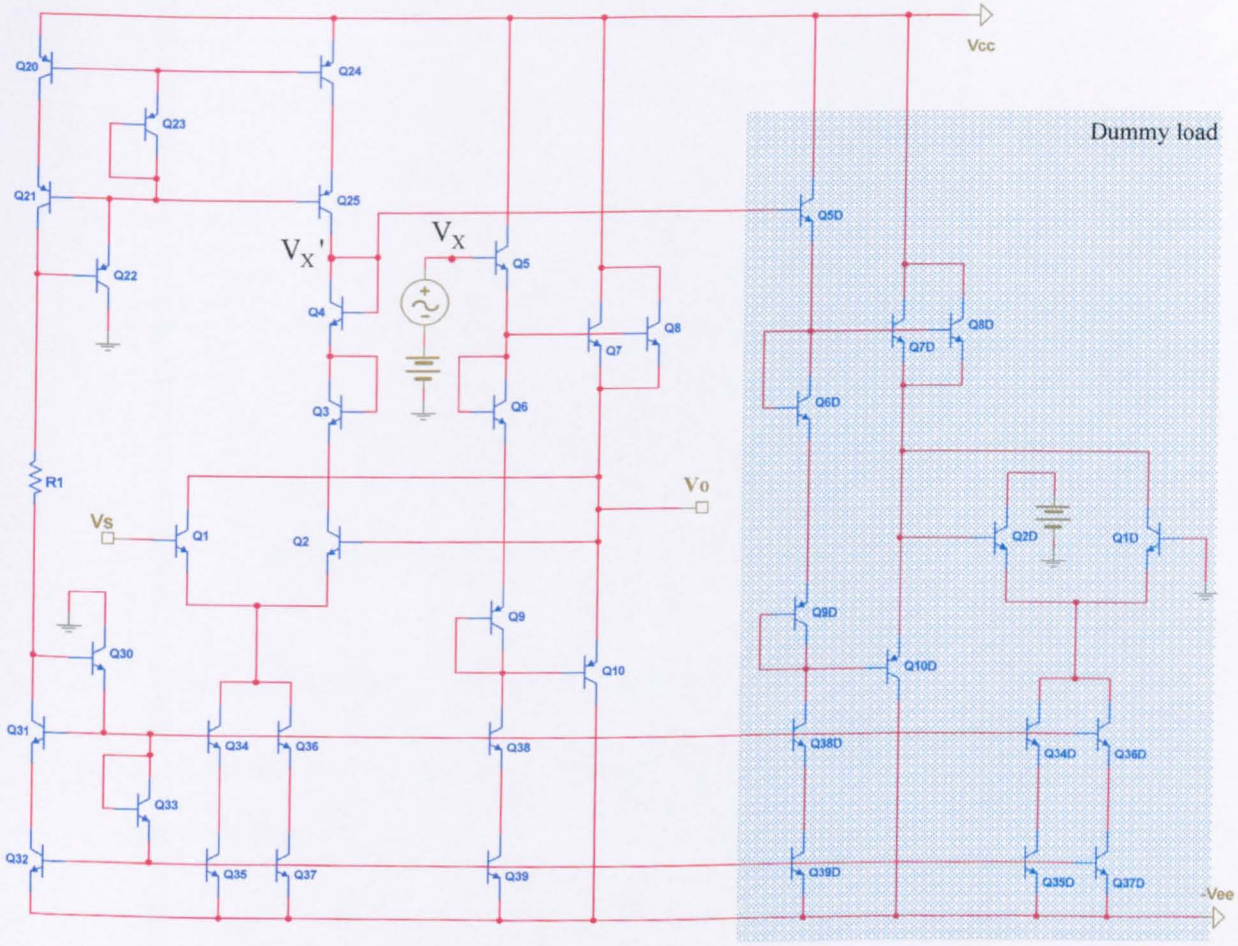

Fig. 7.5 Circuit used for the evaluation of loop-gain magnitude and phase

A cut was made between the collector of Q_{25} and the base of Q_5, but provision was made to ensure that the DC conditions and impedance levels at that point remained unaltered. This necessitated a DC voltage being applied to the base of Q_5

and a 'dummy load', shown shaded in Figure 7.5, being attached to the collector of Q_{25}. A small test voltage V_X applied at the base of Q_5 produces a voltage V_X'. The loop-gain magnitude is $|V_X'/V_X|$ and the loop-gain phase is $\angle V_X'/V_X$.

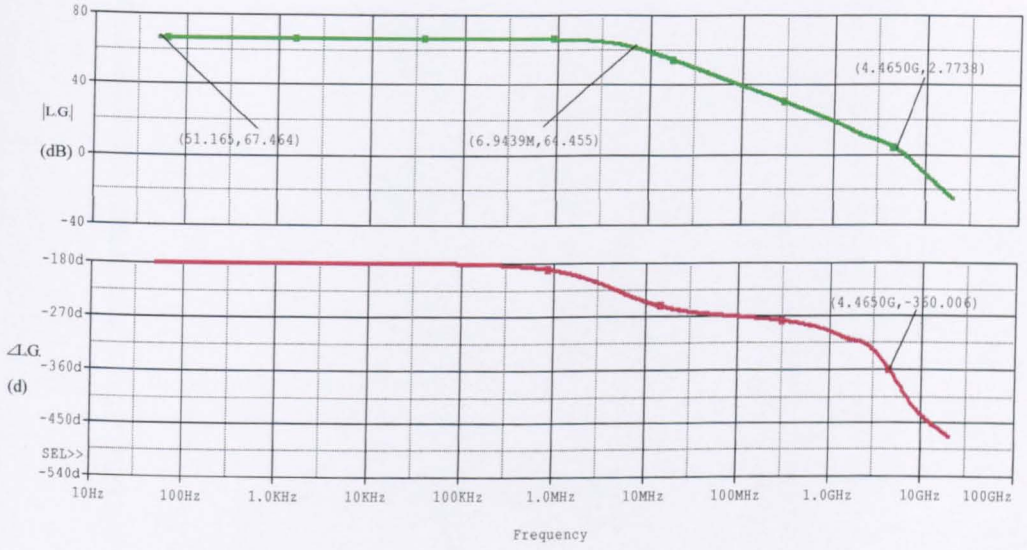

Fig. 7.6 Loop-gain magnitude (top trace) and phase (bottom trace)

The result is shown in Figure 7.6. It is clear that $|L.G| = 2.77dB$ (i.e., $> 0dB$) when $\angle L.G = 0^\circ$, at $f = 4.46GHz$ (i.e., close to the figure of 4.2GHz found for the oscillations in Figure 7.4).

To achieve stability the 'dominant-pole' approach was adopted **[7-4]**. A small capacitor C_1 was connected to the collector of Q_{25} as shown in Figure 7.7 because this point has a comparatively high incremental resistance associated with it.

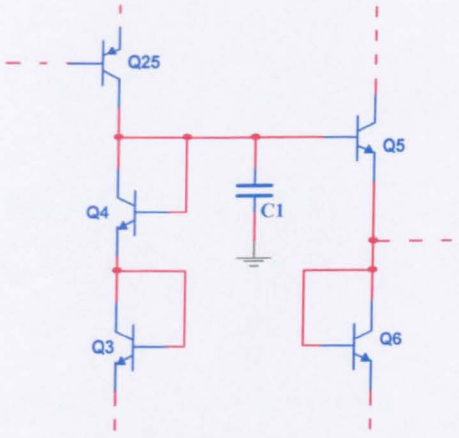

Fig. 7.7 The 'dominant-pole' compensation technique

C_1 has the effect of reducing the bandwidth with the result that $|L.G| < 0dB$ when $\angle L.G = 0^\circ$. Trial and error revealed that $C_1 = 0.2pF$ was just enough to achieve this but, in order to produce a gain and phase margin that would not only take account of circuit tolerances but also to provide acceptable peaking in the frequency response of the closed-loop gain, a value of 0.35pF was decided on. This provides a gain margin of 2.26dB as shown in Figure 7.8.

A higher gain margin could be achieved with a larger value of C_1 but that would be at the expense of closed-loop bandwidth. Furthermore in practical design the smaller C_1 the smaller is the IC chip area consumed.

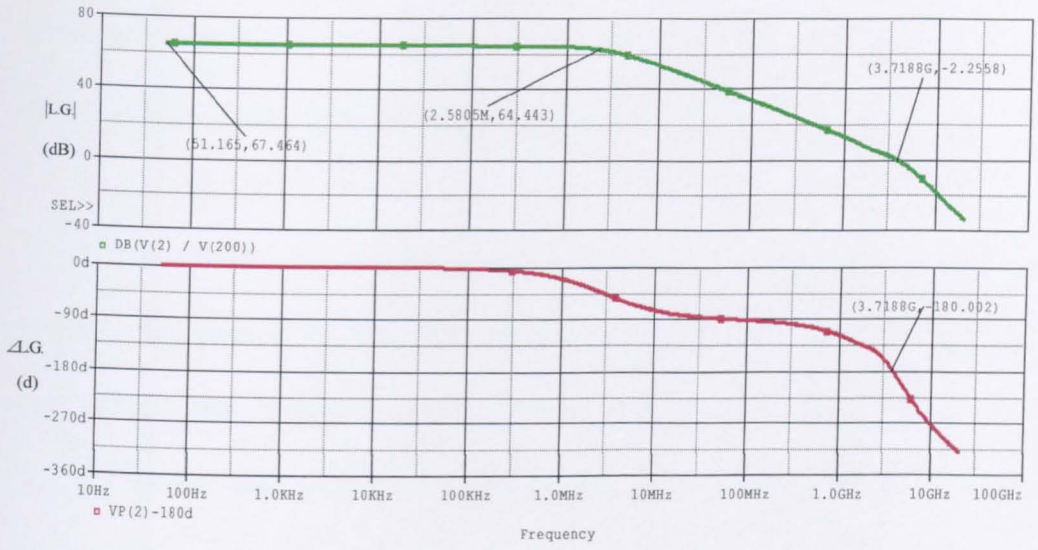

Fig. 7.8 Loop gain magnitude (top trace) and phase (bottom trace) after stabilisation with $C_1 = 0.35\text{pF}$

The theoretical background and justification for the choice $C_1 = 0.35\text{pF}$ is as follows. Referring to Figure 7.5, $|\text{L.G.}(0)|$, the loop-gain magnitude at very low frequencies, is given by,

$$|\text{L.G.}(0)| = \left(\frac{V_X'}{V_X}\right) = -G_V(0)\frac{g_m R_{eq.}}{2} \qquad (7.20)$$

in which, $G_V(0) = \dfrac{V_O}{V_X}$, the low frequency cascaded emitter-follower gain and

$R_{eq.} = R_1 // R_2 // R_3$, where R_1, R_2, R_3 are, respectively, the incremental resistances looking from the collector of Q_2, the output of Q_{25} and the base of Q_5.

A calculation using (7.19) and theoretical values for R_1, R_2, R_3 did not give good agreement with the simulated value of 2362 for $|L.G(0)|$. The reason for this was found, principally, to be due to the values used for R_1, R_2.

Theoretically R_1 should be $(2V_A / I)$, which is approximately 180KΩ. However this assumes V_A to be 90V (using data from Chapter 3). In the vicinity of zero collector-base voltage the slope of the transistor output characteristic, I_C versus V_{CE}, is not the same as that at, say 5V, where Early-voltages are measured. A simulated measurement to find R_1 using the set up of Figure 7.9 gave the curve shown in Figure 7.10.

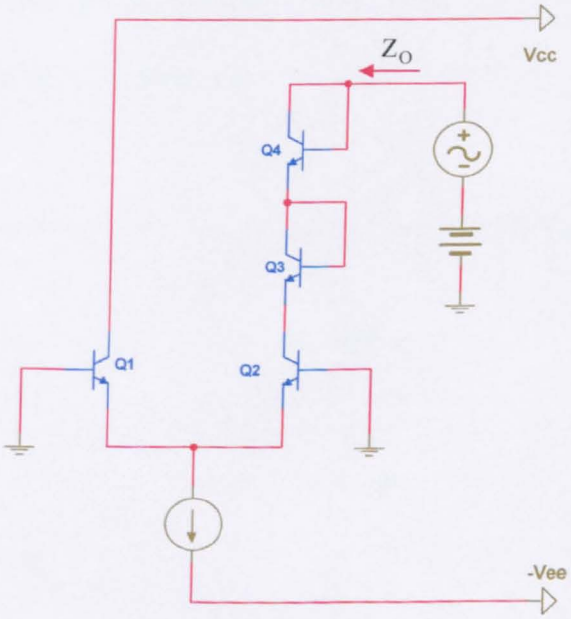

Fig. 7.9 Set up for measuring R_1 ($|Z_O|$ at l.f.)

Fig. 7.10 Collector output impedance (Q_2) of the long-tailed pair of Figure 7.9

From Figure 7.10, $R_1 = 163K\Omega$ and C_{Q2} (output capacitance of Q_2) $= 78.5fF$.

A similar measurement for R_2 gave $R_2 = 567K\Omega$ and $C_{Q25} = 40fF$.

For the base of Q_5, $R_3 = 3.13M\Omega$ and $C_{Q5} = 33fF$.

Thus the total capacitance at the base of Q_5 for $C_1 = 0.35pF$ in Figure 7.7 is,

$$C_T = 0.501pF$$

and,

$$R_{eq.} = 123.7K\Omega$$

Also from simulation,

$$G_V = 0.978$$

Consequently, substituting values in (7.20),

$$|L.G.(0)| = 2345$$

in good agreement with the simulated figure of 2360.

The calculated -3dB frequency for $|L.G.|$ is f_C,

$$f_C = \frac{1}{2\pi \cdot 123.7K\Omega \cdot 0.501pF} = 2.569MHz \qquad (7.21)$$

The simulated value was 2.580MHz, a good agreement with the calculated value.

The final circuit, incorporating the compensation capacitor, C_1, is shown in Figure 7.11.

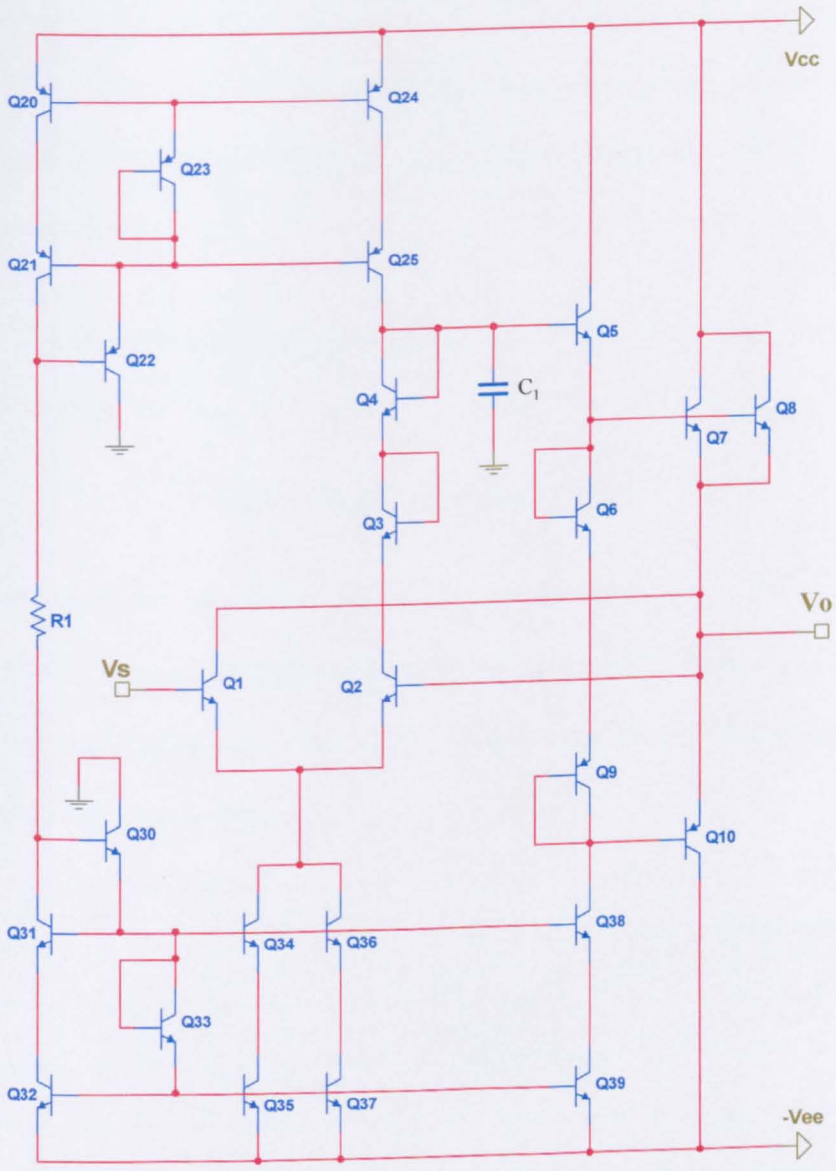

Fig. 7.11 Full circuit of VF/C (including the compensation capacitor) $V_{CC} = V_{EE} = 5V$; I = 1mA

7.5 DC conditions of the VF/C

The simulated transfer characteristic of the VF/C circuit, shown in Figure 7.12, has good linearity and unity slope, a consequence of the overall feedback **[7-5]**. The enlarged plot of Figure 7.12 in the vicinity of the origin, shown in Figure 7.13, confirms the existence of a very small offset voltage, for reasons described earlier in Section 7.2.

Figure 7.14 shows a linear range extending from -3V to +2V. Theoretically, the linear input range is,

$$(V_{CC} - 4V_{BE}) > V_S > -(V_{EE} - 3V_{BE})$$

This confirms the simulated figures if we substitute $V_{CC} = V_{EE} = 5V$ and $V_{BE} = 0.75V$. The slope of the characteristics in this region is indicative of the high incremental input resistance. The slope variation with temperature is due to the temperature dependence of β_n, β_p.

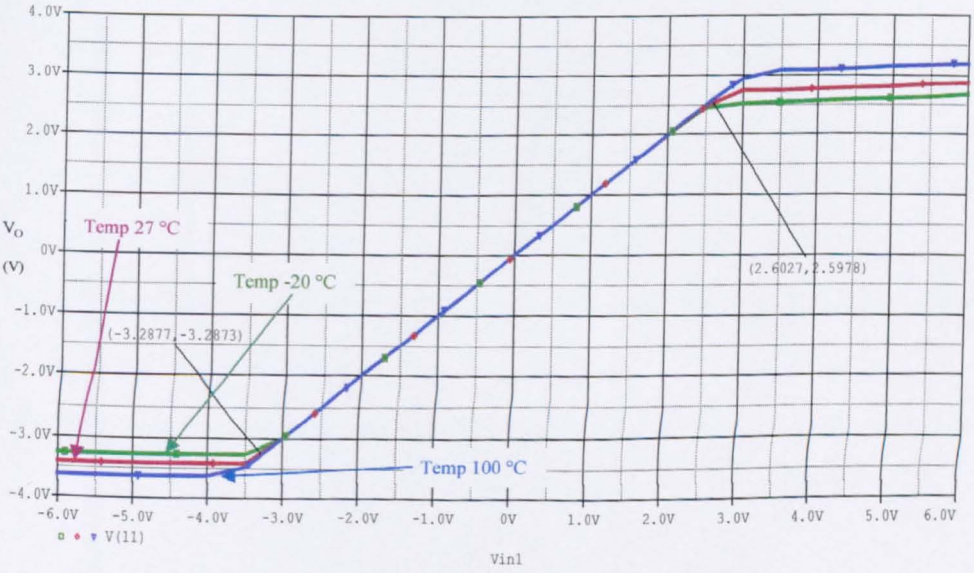

Fig. 7.12 Simulated transfer characteristic for circuit of Figure 7.11 : $V_{CC} = 5V; I_o = 1mA; R_L = \infty$

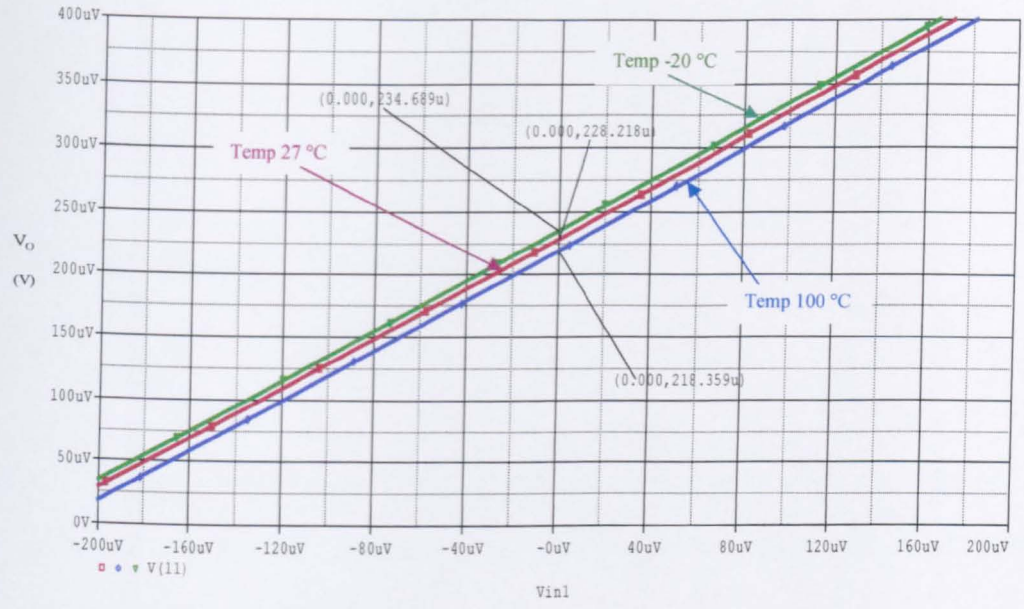

Fig. 7.13 Expanded view of the transfer characteristic in the vicinity of the origin

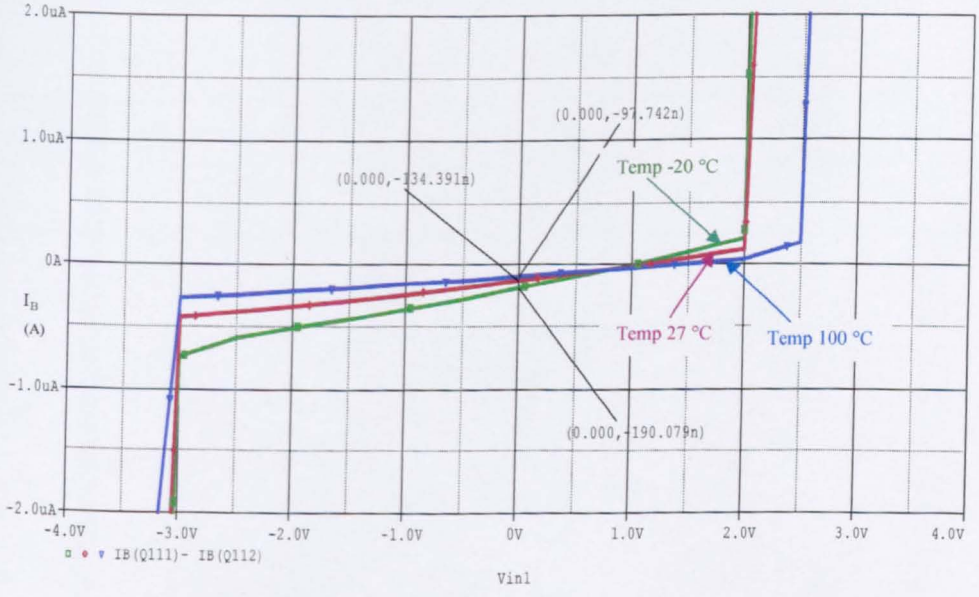

Fig. 7.14 Input characteristic of the circuit of Figure 7.11 for $V_{CC} = V_{EE} = 5V; I_o = 1mA; R_L = \infty$

The quiescent power dissipation of the circuit is,

$$P_Q = (V_{CC} + V_{EE}) \cdot I_Q \cdot n \tag{7.22}$$

For $V_{CC} = V_{EE} = 5V$, $I_Q = 1mA$ and $n = 5$, at 27°C,

$$P_Q = (5V + 5V) \cdot 1mA \cdot 5 = 50mW$$

Table 7.1 shows the quiescent power dissipation produced from the simulation of the circuit at three different operating temperatures. Good agreement is shown for the calculated value at 27°C.

Quiescent power dissipation P_Q **(mW)**			
Operating temperature (°C)	**-20**	**27**	**100**
	48.6	52.6	59.2

Table 7.1 Quiescent power dissipation of the circuit

7.6 Small-signal voltage-gain of the VF/C

Figure 7.15 shows the frequency response of the VF/C circuit. Compared to the VFs considered in the previous chapters, the VF/C presents considerably reduced peaking, due to the feedback loop and the stability that the negative feedback offers. The bandwidth of the circuit is slightly reduced due to the compensation capacitor used for the stability of the circuit. Simulation shows that the reduction in bandwidth is in the range of 7-10%, depending on the output load.

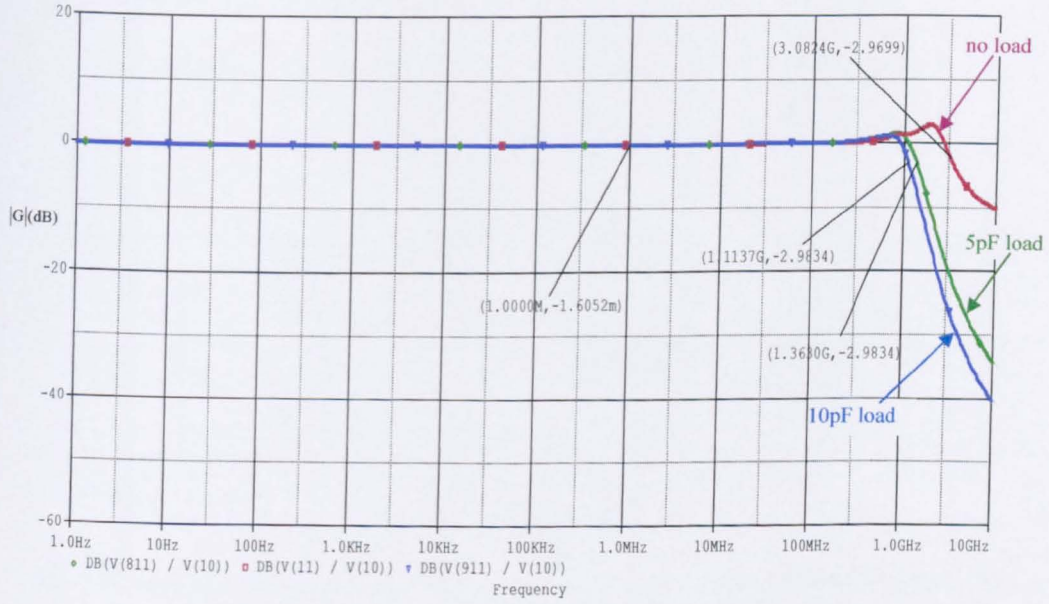

Fig. 7.15 Frequency response for the small-signal gain |G| of the VF/C with different loads

7.7 Incremental input impedance of the VF/C

The incremental input impedance as a function of frequency is shown in Figure 7.16. Spot values are shown in Table 7.2. The high input impedance results from the bootstrapping of the collector of Q_1.

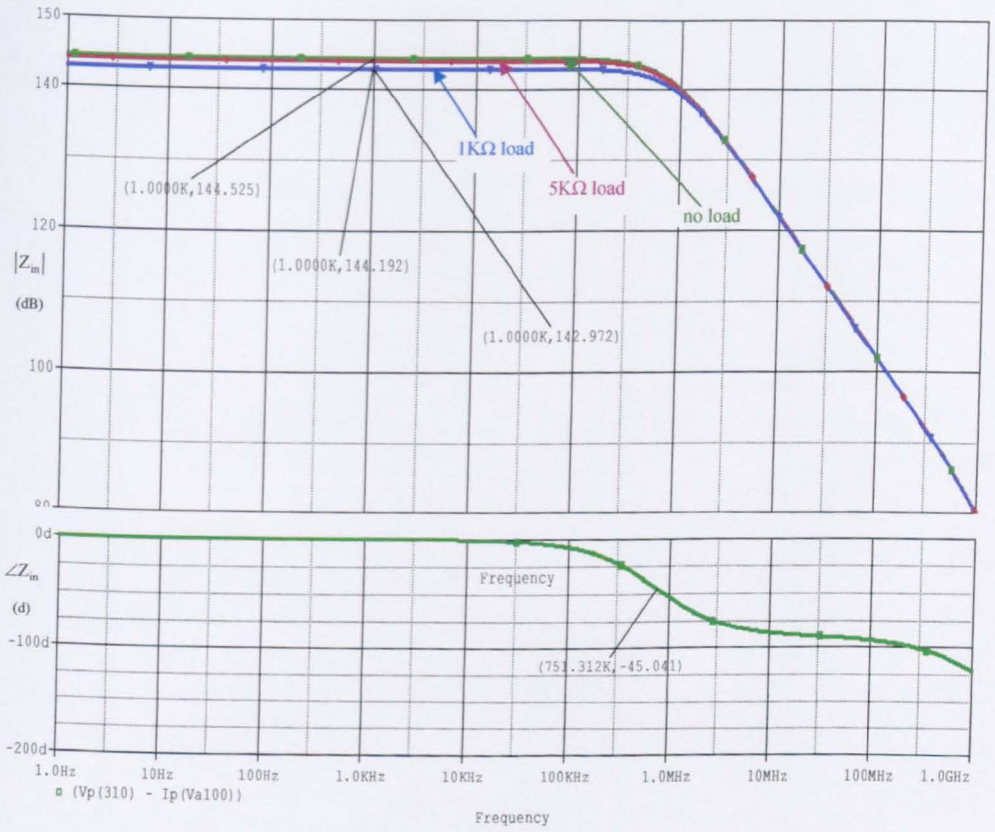

Fig. 7.16 Bode plots for $|Z_{in}|$ for $V_{CC} = V_{EE} = 5V$ and $I_C = 1mA$ for several loads and input phase

Conditions	$\lvert Z_{in} \rvert$ **(Ω)**					
Operating temperature (°C)	**-20**	**27**	**100**	**-20**	**27**	**100**
f = 312.5KHz	10.2M	15.5M	25.9M	9.8M	15.1M	25.3M
f = 31.25MHz	309K	401K	552K	307K	398K	549K
f = 250MHz	38.6K	49.3K	66.5K	38.4K	49.2K	66.4K
Output load	$R_L = \infty$			$R_L = 5K\Omega$		

Table 7.2 $\lvert Z_{in} \rvert$ of the VF with $R_L = \infty$ and $R_L = 5K\Omega$, as a function of f and T

7.8 Incremental output impedance of the VF/C

The approach presented here, to calculate the incremental output impedance of the circuit, is based on a general property of linear voltage amplifier circuits, as described earlier in Chapter 5, and characterised by equation (5.20). If the output is incrementally short-circuited, $V_O = 0$ and $i_O = i_{SC}$.

Hence,

$$GV_S = i_{SC} r_O \tag{7.23}$$

By inspection in Figure 7.11, looking into the base of Q_5, the incremental resistance is,

$$R_{B5} = r_{X5} + r_{\pi 5} + \left[(\beta_5 + 1) \left[\left(\frac{r_{X7} + r_{\pi 7}}{2} \right) // r_{O5} \right] \right] \tag{7.24}$$

where r_X, with appropriate second subscript, represents the transistor base bulk resistance.

Although the current gain β of the transistor models used throughout this research was investigated in Chapter 3, it has been identified that an extra measurement of this parameter, under new operating conditions, was necessary. The reason was the reduced V_{CE} across transistor Q_5 which, in this circuit is equal to $V_{CC} - V_{BE7} \approx 4.2V$ rather than the 5V of Chapter 3. Following the same measurement technique described there, the current gain of Q_5 came to 44.4. Substituting in (7.24), using data from Chapter 3, and for $r_{X5} = 260\Omega$, $r_{\pi 5} = 1146\Omega$,

$$R_{B5} \approx 34K\Omega$$

Thus, the current flowing into the base of Q_5 is,

$$i_{B5} = \frac{g_m V_S}{2} \frac{R_{eq.}}{R_{eq.} + R_{B5}} \approx 0.015\text{mA} \tag{7.25}$$

where $R_{eq.}$ was defined in (7.13).

Consequently,

$$r_O = \frac{V_S}{i_{SC}} = \frac{V_S}{i_{B5}(\beta_5 + 1)(\beta_7 + 1)} \approx 31.3\text{m}\Omega$$

Figure 7.17 shows $|Z_o|$ and $\angle Z_o$ as a function of frequency for three different operating temperatures. Spot values for $|Z_o|$ as a function of f and T are shown in Table 7.3. The difference between theoretical and simulated value is partly accounted for the extra components of i_{SC} that have been ignored. These are the current flowing to the collector of Q_1 and the current reaching the output via the base of Q_1 and Q_2.

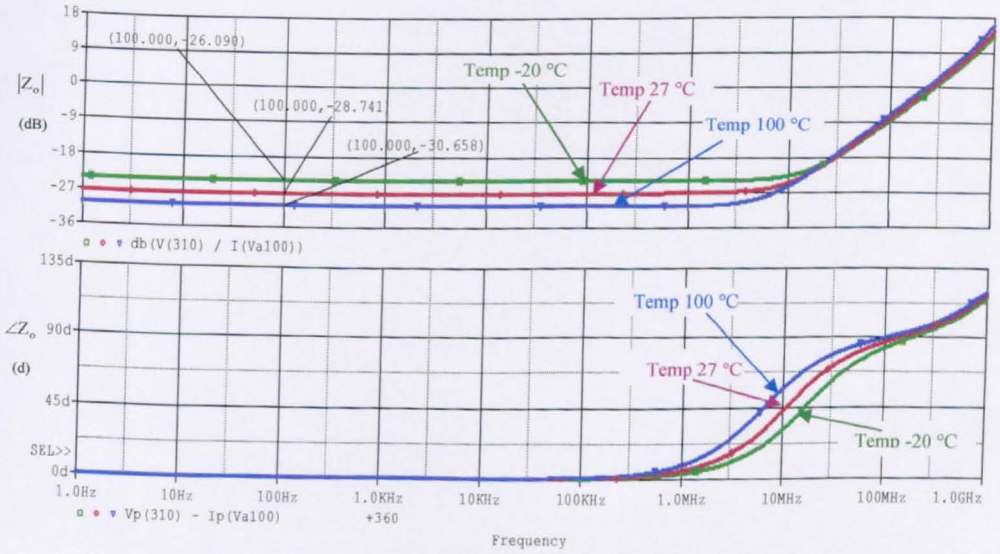

Fig. 7.17 Magnitude (upper curve) and phase (lower curve) for Z_o

Conditions	$\|Z_o\|$ **(Ω)**		
Operating temperature (°C)	**-20**	**27**	**100**
f = 312.5KHz	49m	36m	29m
f = 31.25MHz	130m	131m	133m
f = 250MHz	923m	990m	1130m

Table 7.3 $|Z_o|$ of the VF as a function of f and T

As mentioned previously in connection with emitter-follower outputs, Z_o is inductive at high frequencies.

7.9 Total harmonic distortion and intermodulation distortion of the VF/C

Tables 7.4, 7.5 and 7.6 show, respectively, THD under specified conditions at 312.5KHz, 31.25MHz and 250MHz. The performance of the circuit at higher frequencies was poorer than the VFB/1 and VFB/2 mainly due to the compensation capacitor and the collector current of the output transistor. Table 7.7 shows the IMD performance results for the VF/C, as a function of operating frequency and temperature.

Conditions	**THD (dB)**		
Operating temperature (°C)	**-20 °**	**27**	**100**
$Z_L = 5K\Omega$	-90.8	-90.9	-90.9
$Z_L = 5K\Omega // 5pF$	-78.4	-80.9	-79.6

Table 7.4 THD at 312.5KHz

Conditions	**THD (dB)**		
Operating temperature (°C)	**-20 °**	**27**	**100**
$Z_L = 5K\Omega$	-74.5	-72.4	-70.8
$Z_L = 5K\Omega // 5pF$	-60.9	-60.7	-59.2

Table 7.5 THD at 31.25MHz

Conditions	THD (dB)		
Operating temperature (°C)	-20 °	27	100
$Z_L = 5K\Omega$	-53.5	-54.2	-54.7
$Z_L = 5K\Omega // 5pF$	-49.8	-52.4	-51.1

Table 7.6 THD at 250MHz

Conditions	IMD (dB)		
Operating temperature (°C)	-20 °	27	100
f = 312.5KHz	-104.9	-108.5	-110.1
f = 31.25MHz	-87.1	-87.5	-88.9
f = 250MHz	-53.7	-54.3	-61.2

Table 7.7 IMD results for VF/C as a function of f and T.

7.10 Noise performance of the VF/C

The noise performance of the VF/C is shown in Figure 7.18. This is in the same region as the VF designs presented in Chapter 5 and Chapter 6.

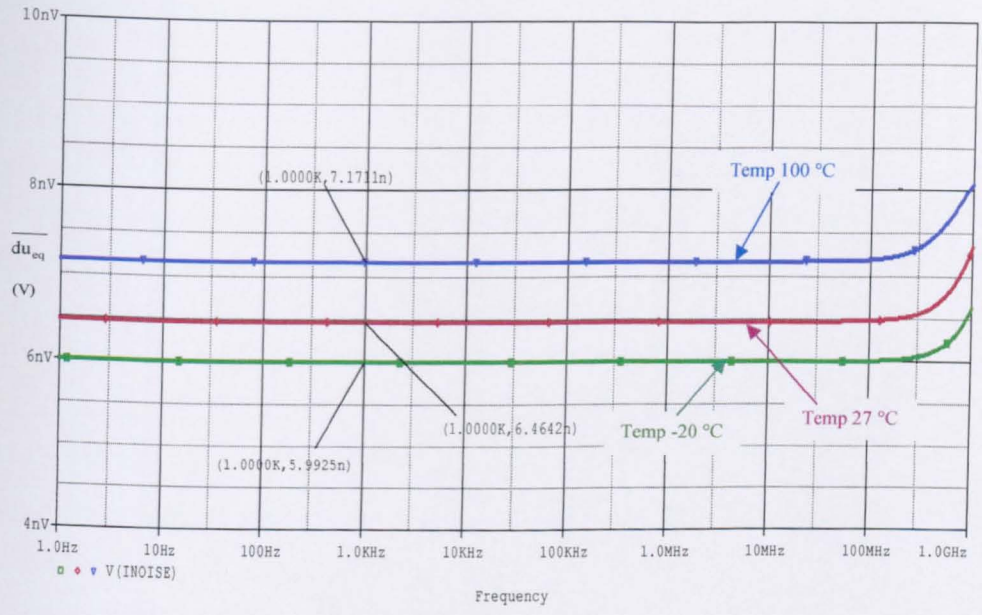

Fig. 7.18 Input noise of the circuit

7.11 Pulse response of the VF/C

Figures 7.19 and 7.20 show the waveforms when a positive going input pulse of amplitude 0.5V and rise and fall times of 1nS and 0.1nS, respectively, is applied. These are understandable in the light of the discussion of emitter-follower pulse response presented in Chapter 4.

Fig. 7.19 Pulse response for an input signal with 1nS rise and fall times

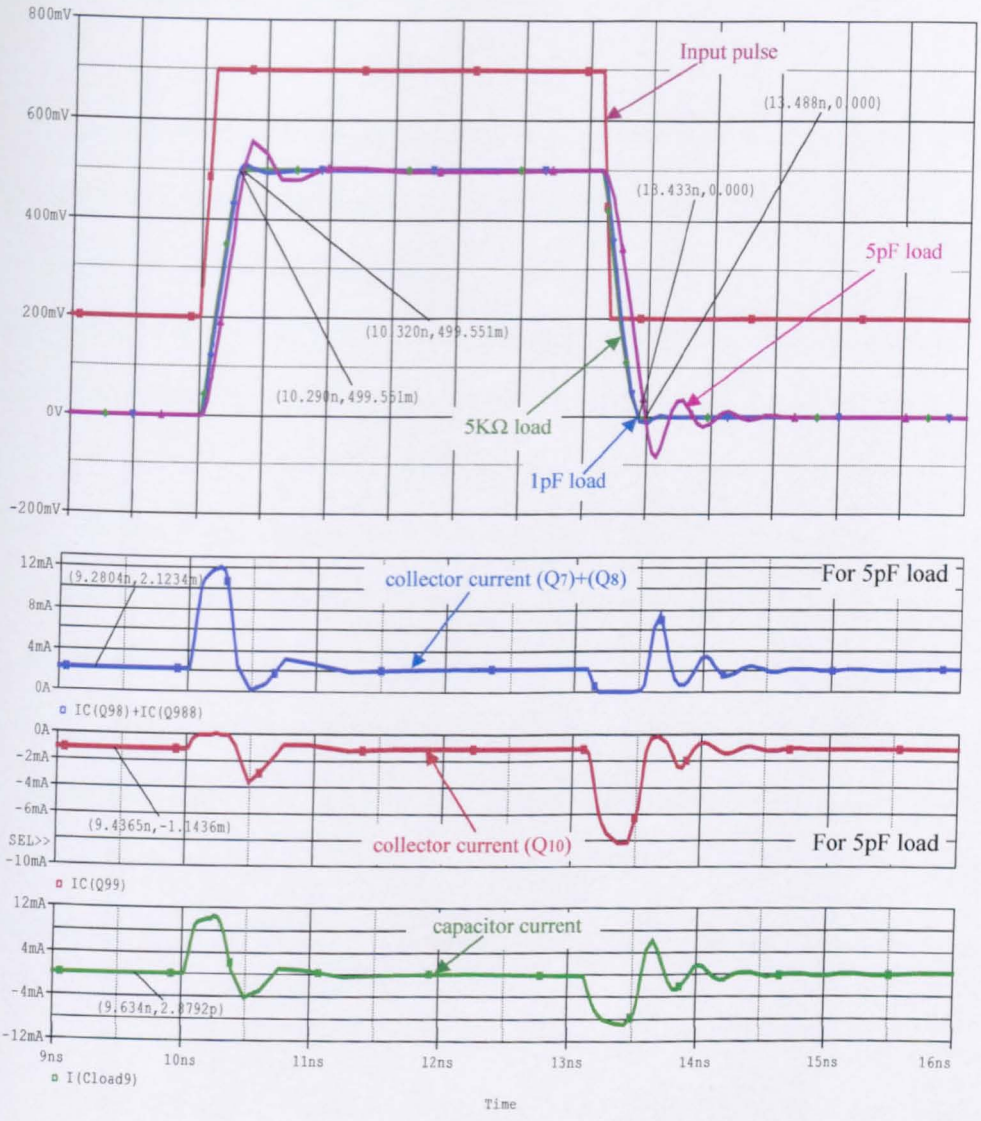

Fig. 7.20 Pulse response for an input signal with 0.1nS rise and fall times

7.12 A comparison of the VF designs

The analysis and simulation of the conventional and the proposed circuits in the same way gives the reader the advantage of comparing their performance parameters and deciding which of the proposed designs is most suitable for the application. This section presents a comparative assessment of the most important parameters of the voltage-followers investigated. Choosing the best voltage-follower is subject to trade-offs between power consumption, distortion, impedance levels, bandwidth etc. Consequently, as an example, the Type B (VFB/2) voltage-follower of Chapter 6 presents low distortion at high frequencies, high voltage swing and bandwidth and requires less silicon area due to the six-transistor core. Nevertheless, its power dissipation is 63% higher than the Type A ('Super-follower') of Chapter 5, its output impedance is sixty times bigger than the Type C (VF/C) follower with global feedback of Chapter 7, while its input impedance is more than four times smaller than that of the Type B (VFB/1), the first proposed circuit of Chapter 6.

Tables 7.8 and 7.9 show, respectively, the comparison of THD and IMD results for the conventional and the new VFs as a function of operating frequency at room temperature. Figures 7.21, 7.22 and 7.23 show the same comparison graphically.

Configuration	Total Harmonic Distortion (THD) at 27°C (dB)				
	Conv. EF	VF/A	VFB/1	VFB/2	VF/C
f = 312.5KHz $Z_L = 5K\Omega$	-72.5	-93.9	-91.2	-89.9	-90.9
$Z_L = 5K\Omega // 5pF$	-64.5	-89.2	-86.8	-79.9	-80.9
f = 31.25MHz $Z_L = 5K\Omega$	-71.9	-75.6	-72.7	-86.8	-72.4
$Z_L = 5K\Omega // 5pF$	-52.7	-84.4	-75.8	-63.9	-60.7
f = 250MHz $Z_L = 5K\Omega$	-42.7	-57.4	-67	-70.8	-54.2
$Z_L = 5K\Omega // 5pF$	-35.2	-47.7	-70	-62	-52.4

Table 7.8 Comparison of THD results for the conventional and the proposed VFs as a function of frequency at 27°C for two different loads

Configuration	Intermodulation Distortion (IMD) at 27°C (dB)				
	Conv. EF	VF/A	VFB/1	VFB/2	VF/C
f = 312.5KHz $Z_L = 5K\Omega$	-52.1	-93.9	-64.4	-87.6	-108.5
f = 31.25MHz $Z_L = 5K\Omega$	-54.6	-75.6	-67.3	-84.4	-88.9
f = 250MHz $Z_L = 5K\Omega$	-48.3	-57.4	-61.3	-66	-61.2

Table 7.9 Comparison of IMD results for the conventional and the proposed VFs as a function of frequency at 27°C

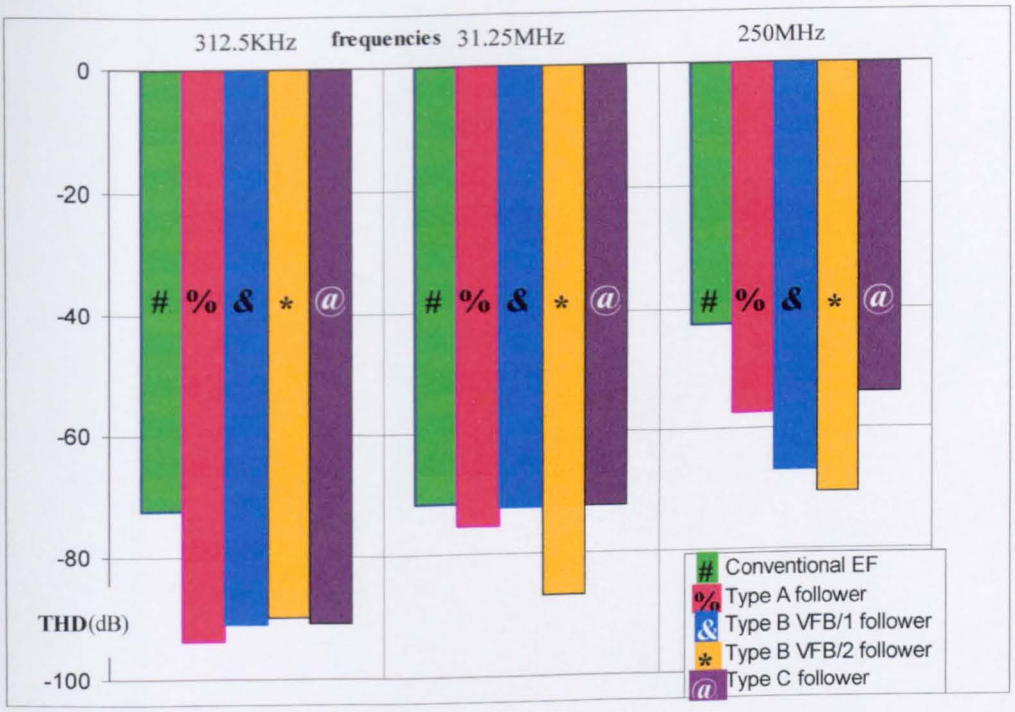

Fig. 7.21 Comparison of THD results for the conventional and the proposed VFs as a function of frequency at 27°C for resistive load (5KΩ)

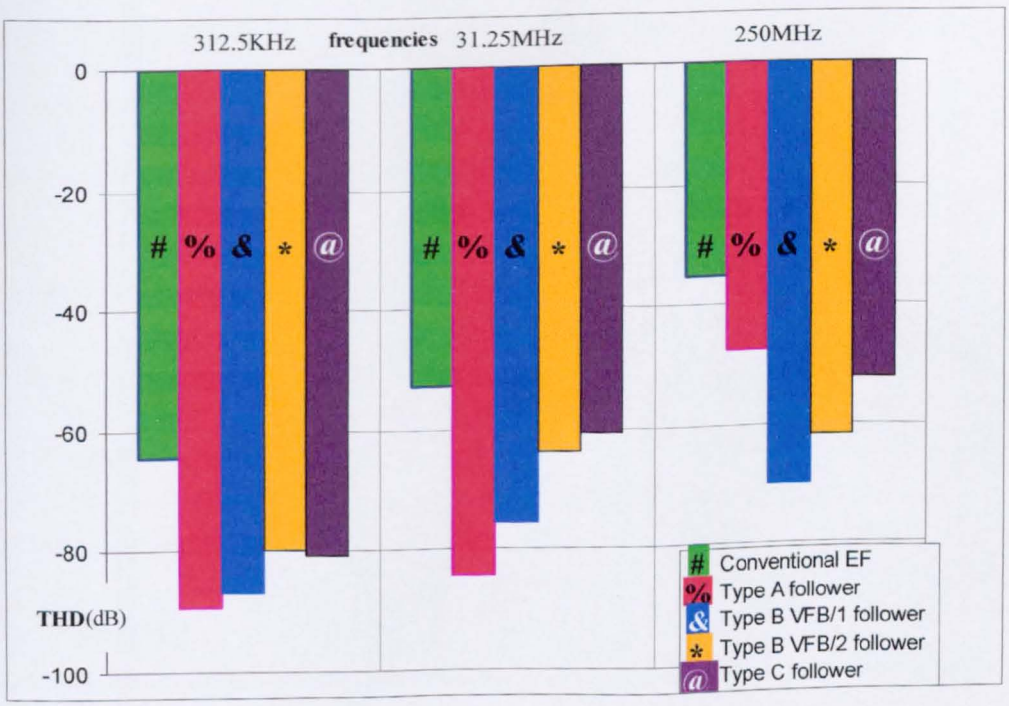

Fig. 7.22 Comparison of THD results for the conventional and the proposed VFs as a function of frequency at 27°C for resistive/capacitive load (5KΩ//5pF)

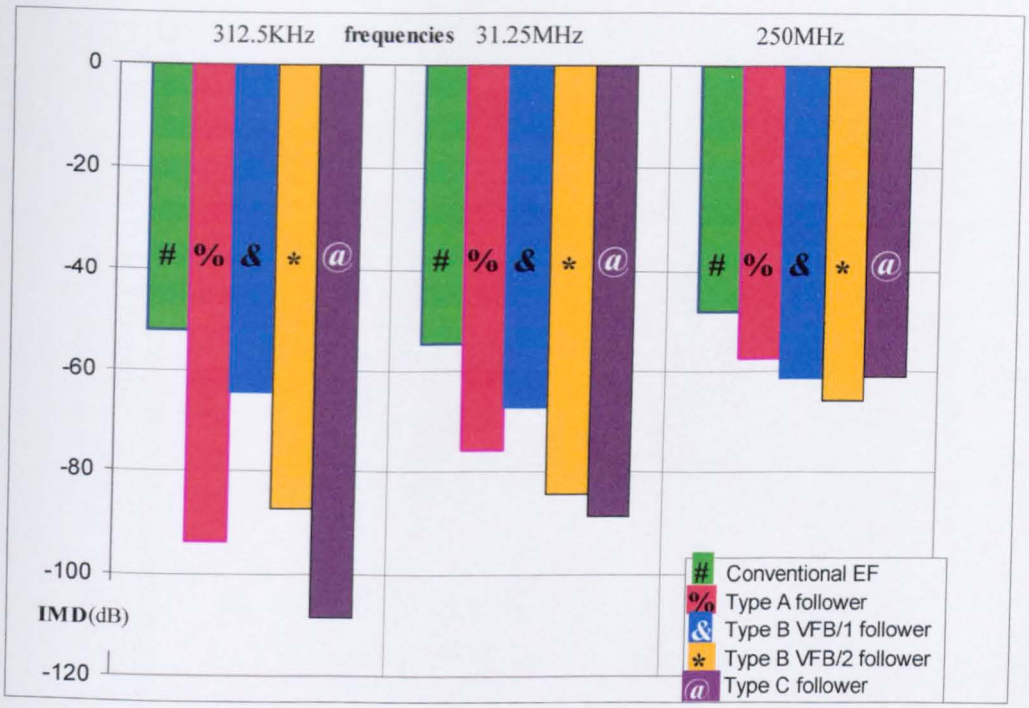

Fig. 7.23 Comparison of IMD results for the conventional and the proposed VFs as a function of frequency at 27°C

For comparative assessment the input and output impedance of the new VFs tabulated and shown in Tables 7.10 and 7.11 respectively. In addition, Figures 7.24 and 7.25 show, respectively, their comparison graphically.

Configuration	Input Impedance at 27°C(Ω)			
	VF/A	VFB/1	VFB/2	VF/C
f = 312.5KHz	12.8M	2.94M	637K	15.5M
f = 31.25MHz	419K	181K	63.7K	401K
f = 250MHz	12.6K	6.5K	8K	49.3K

Table 7.10 $|Z_i|$ for all types of VFs as a function of frequency at room temperature

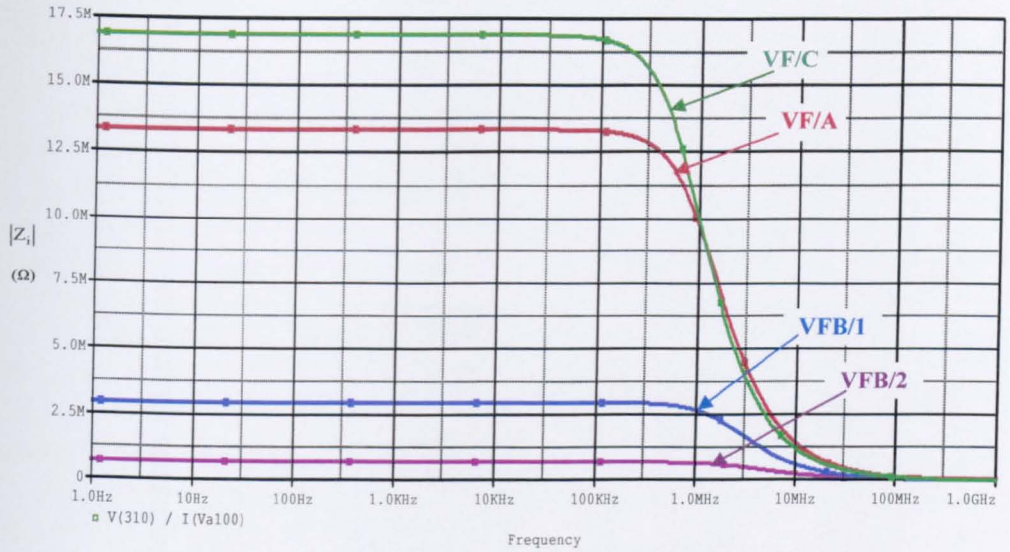

Fig. 7.24 Graphical comparison of $|Z_i|$ for all types of VFs as a function of frequency at room temperature

Configuration	Output Impedance at 27°C (Ω)			
	VF/A	VFB/1	VFB/2	VF/C
f = 312.5KHz	26	10.8	2.4	0.036
f = 31.25MHz	26	10.8	2.5	0.131
f = 250MHz	25.6	12.2	5.3	0.99

Table 7.11 $|Z_o|$ for all types of VFs as a function of frequency at room temperature

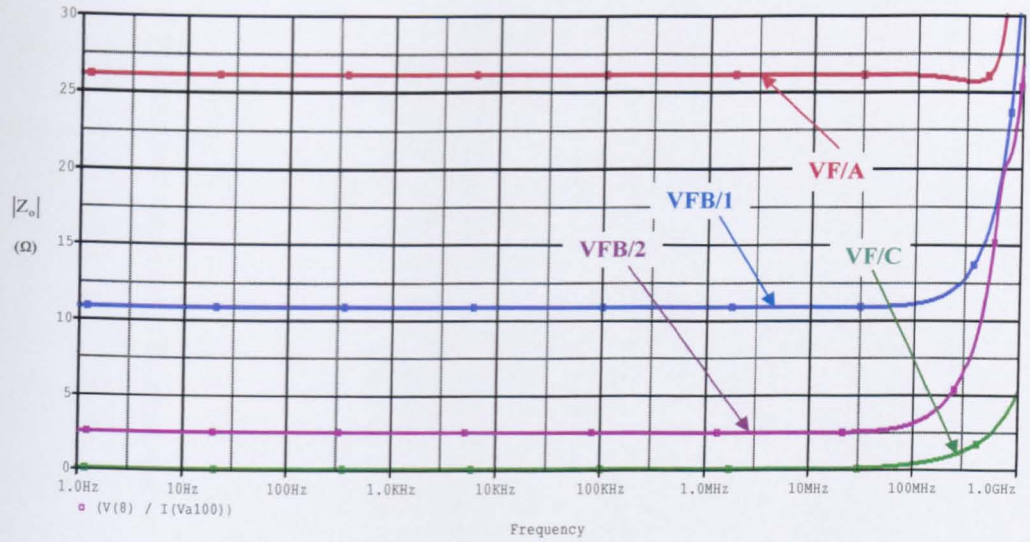

Fig. 7.25 *Graphical comparison of* $|Z_O|$ for all types of VFs

as a function of frequency at room temperature

A summary of the key performance parameters of all four VF designs is shown in Table 7.12.

Configuration	Parameters at 27°C			
	VF/A	VFB/1	VFB/2	VF/C
Power supply	±5V	±3.3V	±5V	±5V
Power dissipation	34.6mW	53.6mW	55.4mW	52.6mW
Output voltage swing	±2V	±2V	±4.5V	-3.2V to +2.6V
Offset voltage	64μV	5.16mV	3.07mV	228μV
Slew rate	4250V/μs	4810V/μs	4950V/μs	2015V/μs
Small-signal bandwidth (-3dB) (5KΩ Load)	2.7GHz	2.2GHz	3.12GHz	3.08GHz
Small-signal bandwidth (-3dB) (5pF Load)	1.3GHz	1.4GHz	1.58GHz	1.36GHz
Gain-flat to within 0.1dB (5KΩ Load)	330MHz	280MHz	728MHz	184MHz
Gain-flat to within 0.1dB (5pF Load)	163MHz	125MHz	184MHz	171MHz
Input-Referred voltage noise (f≤10MHz)	3.94nV²/Hz	7.34nV²/Hz	5.56nV²/Hz	6.46nV²/Hz
Input offset current	1.63μA	1.76μA	558nA	134nA
No of devices used (core)	20	12	6	10

Table 7.12 Performance parameters of all four new VF designs

Table 7.13 shows the performance parameters that met the specifications set in the beginning of this work for each new circuit.

Configuration	VF/A	VFB/1	VFB/2	VF/C
$\|V_{CC}\| \leq 5V$	✓	✓	✓	✓
$P_D \leq 35mW$	✓	X (53.6mW)	X (55.4mW)	X (52.6mW)
$\|Zi\| > 5M\Omega$ for $f \to 0$	✓	X (2.96MΩ)	X (642KΩ)	✓
$\|Zo\| < 10\Omega$ for $f \to 0$	X (26Ω)	✓	✓	✓
$V_{S(min)} = 2V_{P-P}$	✓	✓	✓	✓
$\|G\| = (1-\varepsilon)$, where $\varepsilon < 0.1$ up to 250MHz	✓	✓	✓	✓
THD ≤ −80dB at 5MHz	✓	✓	✓	✓
THD ≤ −60dB at 250MHz	X (-57.4dB)	✓	✓	X (-54.2dB)
IMD ≤ −55dB at 250MHz	✓	✓	✓	✓

Table 7.13 Performance parameters met by each new VF

7.13 Summary for Chapter 7

This chapter has presented a voltage-follower different from those considered in the two previous chapters, Chapter 5 and Chapter 6. In this chapter overall feedback is used in addition to local feedback. This is lay to a number of improvements in the VF performance, notably with respect to input and output impedance, offset voltage and pulse response. However these improvements have, only, been incurred of an added capacitor to ensure Nyquist stability. In addition, this chapter has presented a comparative assessment of the most important parameters of the VFs investigated. According to that, choosing the best voltage-follower is subject to trade-offs.

References for Chapter 7

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APPENDIX 7

AP7.1 Analysis of incremental input resistance of circuit of Figure 7.2

AP7.2 Analysis of incremental output resistance of circuit of Figure 7.2

Appendix AP7.1

Analysis of incremental input resistance of circuit of Figure 7.2

Figure A7.1 shows the equivalent impedance seen at the input of the circuit.

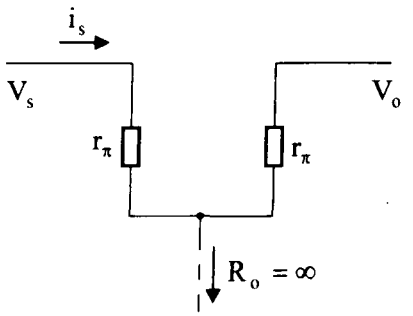

Figure A7.1 Input impedance of the long-tailed pair

By inspection,

$$i_s = \frac{V_s - V_o}{2r_\pi} = \frac{V_s\left(1 - \frac{V_o}{V_s}\right)}{2r_\pi} \qquad \text{(A7.1)}$$

Thus, the input impedance is,

$$\therefore \text{Rin} = \frac{V_s}{i_s} = \frac{V_s \cdot 2r_\pi}{V_s\left(1 - \frac{V_o}{V_s}\right)} = \frac{2r_\pi}{\left(1 - \frac{V_o}{V_s}\right)} = \frac{2r_\pi}{(1-G)} \qquad \text{(A7.2)}$$

For Op-Amp as a V.F.,

$$G = \frac{A}{(1+A)} \qquad \text{(A7.3)}$$

Thus,

$$\therefore \qquad (1-G) = \left[1 - \frac{A}{(1+A)}\right] = \frac{1}{(1+A)} \qquad \text{(A7.4)}$$

Consequently, the input impedance is,

$$\text{Rin} = (1+A)\cdot 2r_\pi \approx A \cdot 2r_\pi \qquad \text{(A7.5)}$$

Appendix AP7.2

Analysis of incremental output resistance of circuit of Figure 7.2

The analysis of the output impedance can be carried out using the equivalent circuit in Figure A7.2, which represents the output transistor Q_3 of Figure 7.2.

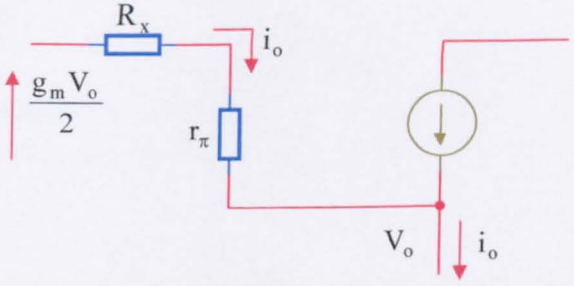

Figure A7.2 Equivalent circuit for the calculation of Z_O

If the output voltage decreases by V_o, then the voltage at the collector of Q_2 increases by,

$$V_o \frac{g_m}{2} R_x \tag{A7.6}$$

The base current of Q_3 is,

$$i_b = \frac{\left(\frac{g_m}{2} R_x + 1\right) V_o}{(R_x + r_\pi)} \tag{A7.7}$$

Thus,

$$i_o = \frac{(\beta_n + 1)\left(\frac{g_m}{2} R_x + 1\right) V_o}{(R_x + r_\pi)} \tag{A7.8}$$

Thus, the output resistance is,

$$r_o = \frac{V_o}{i_o} = \frac{(R_x + r_\pi)}{(\beta_n + 1)\left(\frac{g_m}{2} R_x + 1\right)} \approx \frac{\left[r_e + \frac{R_x}{(\beta_n + 1)}\right]}{\left(\frac{g_m}{2} R_x + 1\right)} \approx \frac{\left[r_e + \frac{R_x}{(\beta_n + 1)}\right]}{(A + 1)} \tag{A7.10}$$

CHAPTER 8

Conclusions and future work

8.1 Conclusions

The field of RF circuit design is currently going through a massive development mainly due to the exponential growth of wireless applications. The overall system performance is very much dependent on the high frequency front-end component characteristics which generally set the performance limits of the system [8-1]. Maintaining low distortion levels at higher frequencies is critical for it sustains the quality, the dynamic range and signal-to-noise ratio of the design. Environmental factors, including thermal effects, need to be taken into account in circuit and system design to ensure the design meets the specification under all operating conditions.

In a similar manner, several other factors such as power consumption, signal gain, input and output impedance need to be investigated as these contribute equally in developing a clear statement of the design requirements, before proceeding with detailed design. Additionally, detailed research of the market and literature also needs to be carried out, to investigate what is currently available and the latest techniques used. With this information the limitations and deficiencies of existing designs can be evaluated in the light of design requirements for a particular application.

The above procedure has been followed throughout the course of this work. The objectives of the project were defined in Chapter 2, after a short presentation of the ideal voltage-follower design and its practical limitations. Three different possible approaches to achieve the stated goals have been identified, concerning the bias

current and the type of feedback that has been used. Finally, some application examples demonstrate the reason why a high performance design is necessary and how it can improve the overall performance of the system.

In Chapter 3 the author follows an investigation on the transistor models used throughout the research, as well as a review on the current bias schemes used to support the operation of the conventional and proposed voltage-follower designs. In the beginning of this project thorough investigation was carried out on transistor models. An appropriate transistor technology is required for the designs that has a sufficiently high operating frequency, complementary devices with similar characteristics and ready availability. During the investigation of any circuit in this project, prior to simulation being carried out, a detailed theoretical analysis was undertaken. During the early stages in this research simulation results did not always match the small-signal analysis results. It became clear that more precise small-signal parameter extraction needed to be undertaken. Consequently, in Chapter 3 several different methods are described to obtain better values of the transistor parameters at the appropriate operating bias voltage and current levels. These include using the AC and DC current gain for β, the Early-Voltage, V_A, for r_{ce}, the frequency response to obtain transistor cut-off frequency f_T, and the collector-base internal capacitance. This investigation proved useful as it gave values for the transistor parameters different from those listed by the manufacture. On re-working the analysis there was much closer correlation between the simulation and analytical results obtained, confirming the validity of this work. In the same chapter a critical review of current biasing techniques using current-mirrors has been carried out, heading to the scheme adopted for the biasing of both the conventional and proposed designs. The

current-mirror chosen, not only improved the current transfer ratio, λ, but also offered higher output impedance, well above conventional mirrors such as the Wilson and the cascoded buffered current-mirror, justifying why it was chosen for biasing circuitry.

Although the following chapter, Chapter 4, concerns the conventional emitter-follower, the author treats it critically and considers some of this work to be novel. In this chapter, a thorough and detailed analysis and review of the conventional emitter-follower is undertaken to evaluate the circuit performance and reveal its limitations using both DC and AC analysis. According to the author, the treatment presented here is well beyond that given in textbooks, and makes a considered original contribution to the design and development of voltage-followers. Chapter 4 'sets a bench-mark' in both analysis and presentation for the next three chapters, all of which have the same outline and style. Consequently, the reader can appreciate the relative superiority of the proposed circuits over conventional designs. Also, this approach simplifies the decision process in selecting the most suitable of the proposed designs for a particular application, according to the trade-offs of each.

Chapter 5 presents a novel voltage-follower based on the input stage of the current feedback operational amplifier, which is known as the 'Diamond' circuit. This circuit was part of the first category of circuits investigated in this project, the voltage-followers with local feedback and single-valued current biasing. The initial circuit has been thoroughly analysed theoretically, it has been simulated according to the benchmark set in the previous chapter, and several ways of improving its performance have been identified. Progressive modifications of the circuit have been

described which significantly improved almost every performance parameter. This novel circuit has been reported by the author in the technical literature **[8-2]**, **[8-3]**.

In Chapter 6, two novel voltage-follower circuits with local feedback and double-valued current biasing have been presented. In common with the majority of the voltage-follower designs reported in this thesis, both are complementary designs, exhibit good load drive capability for positive or negative-going input signals, and low distortion is achieved. The theoretical analysis, the simulation and the transistor models used were identical to those used on circuits of the previous chapters, enabling convenient relative performance comparison between the circuits to be made. Most of the performance parameters of both new designs in this chapter are better than the voltage-follower described in Chapter 5, except for slightly higher power consumption and reduced input impedance. The work has been presented in IEEE proceedings **[8-4]**, **[8-5]**, **[8-6] and [8-7]**.

Chapter 7 considers the voltage-follower using global feedback. A novel circuit has been designed and analysed, presenting merits and demerits of the technique. In general, the use of negative feedback can provide several advantages in a circuit, such as smaller output and higher input impedance as well as gain control, which are desirable parameters when designing voltage-followers. However, it has been shown that using negative feedback globally, can cause serious operating problems particularly in respect of instability and oscillation, mainly at high frequencies. In addition, this chapter has presented a comparative assessment of the most important parameters of the VFs investigated in this work. The assessment clearly stated that the best voltage-follower is subject to trade-offs.

8.2 Future work

Throughout this research on voltage-followers it emerged that the internal capacitances of the transistor significantly influenced the distortion of the signal at high frequencies. It has been found that these capacitances limit the slew-rate of the circuit and also affect its input impedance. On the other hand, the non-zero input current of a BJT limits the maximum input impedance that can be achieved in a voltage-follower configuration. Although the author's work, reported here, demonstrates that the conventional bipolar voltage-follower can be improved in performance, this has generally been achieved at the expense of increasing power consumption and also increasing power supply voltage requirements, due to use of additional devices with their necessary base-emitter voltage drops.

These reasons suggest that future developments should be undertaken using a different high frequency-transistor technology. A suitable contender would be SiGe/BiCMOS, which offers increased operating bandwidth with reduced supply voltage demands, combining the high-performance heterojunction bipolar transistors (HBTs) with state-of-the-art CMOS technology **[8-8]**. Although the manufacturing process is more complicated, the combination of both technologies require smaller silicon area circuits, extending their applicability.

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CHAPTER 9

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