Analysis and Design of High-Transconductance RF MOSFET Voltage-to-Current Converters

by

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A thesis submitted in partial fulfilment of the requirements of Oxford Brookes University for the degree of

Doctor of Philosophy

October 2009

OXFORD BROOKES UNIVERSITY

Acknowledgment

I would like to thank my director of research, Dr. Khaled Hayatleh, for his guidance and support throughout the Ph.D. Dr. Hayatleh has dedicated a significant amount of time, in a regular basis, on technical discussions with me and he was always been a great source of advice and inspiration as well as psychological support during the difficult period.

It has been a privilege as well as tremendous honour to learn a great deal from Dr.Bryan Hart's wide experience in analogue circuit design.

Special thanks go to my second supervisor, Prof. John Lidgey for his positive criticism and his support. His speaking and writing ability and his depth and speed of technical mind were really valuable.

I would like to thank my parents, sister and brother for their continuous support. Their love and faith in my abilities gave me the strength to complete this program. I dedicate this work to them. It is the least that I could do to express my sincere appreciation.

Finally special thanks are due to my dear friends: Qi Wang, Ke Chen, Dr. Ling Yang and Koyn Hsiao for their long lasting support throughout this research work.

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October 2009

Abstract

The research described in this thesis is concerned with analysis and design of "High-Transconductance RF MOSFET Voltage-to-Current (V-I) Converters". Various V-I converter circuits published in the past have been reviewed by the author in order to understand the different techniques employed to improve transconductance (G_t), linear operating range and total harmonic distortion (THD). Throughout this research, the emphasis has been to improve the above mentioned parameters. All the V-I converter circuits reported have been simulated using PSPICE and the results compared with the values obtained by theoretical analysis. Some of the results of this work have been already reported by the author in the technical literature. (See Chapter 9, at the end of this thesis, where reference to two publications by the author is given.)

It was essential to obtain accurate CMOS device parameters values, such as Early Voltage, transconductance parameter ratios μ (g_m/g_{ds}), χ (g_{mb}/g_m) and inter-electrode capacitances, to facilitate the design the process. This was achieved using an extensive set of simulations for the transistor operating under different bias conditions. Furthermore, a measurement technique, thought to be novel, for the direct determination of the transconductance ratios μ and χ is proposed.

In the next part of the work several types of current mirror are compared against the standard current mirrors, using analytical and simulation methods. Furthermore several MOSFET V-I converter designs were critically reviewed to understand the various existing techniques and their limitations.

Two novel techniques, Drain-Source Feedback Circuits (DSFCs) and Drain-Gate Feedback Circuits (DGFCs) ere implemented with a new temperature-compensation scheme, designed to operate well in an industrial environment (-40°C ~ +85°C). It is found that the best types of V-I converters were the DSFCs which, offer a more accurate value of G_t (3.386mS) and the THD less than -57dB for a differential input operating range 500mV at 1GHz with a 3V total rail voltage. The DGFC circuits were also meet the initial design targets, the value of THD is less then -50dB, and operating in the Giga hertz frequency range is possible. Preliminary investigation on future work shows promising results.

List of acronyms and principal MOSFET symbols

Acronyms

CMOS	Complementary Metal Oxide Silicon
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
THD	Total Harmonic Distortion
V-I	Voltage-to-Current

MOSFET symbols

Av	Voltage gain
β	Transconductance parameter
C_{db}	Intrinsic Drain-Body capacitance
C_{gd}	Intrinsic Gate-Drain capacitance
C_{gs}	Intrinsic Gate-Source capacitance
f	Frequency
f_{-3dB}	Cut-off frequency
f_T	Transistor unity-gain frequency
g_m	Transconductance
g_{mb}	Body-effective transconductance
G_t, G_m	Transconductance
I_D	Drain current
λ	Channel modulation factor
m	Current mirror transfer ratio
r_{ds}	Small-signal drain-source resistance
r_o	Small-signal output resistance
V_A	Early Voltage
V_{DS}	Drain-Source Voltage
V_{GS}	Gate-Source Voltage
V_{SB}	Sourece-Substarte Voltage.
V_T	Threshold Volatge

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CHAPTER 1

THESIS INTRODUCTION

1.1 Introducing the Voltage-to-Current Converter and its applications

This thesis is concerned with Voltage-to-Current (V-I) converters, also referred to as Transconductors, usually referred to symbolically by either G_t or G_m. They are commonly used as active elements in analogue signal processing circuits, such as: filters, amplifiers, mixers and oscillators [1.1-1.4]. An ideal V-I converter should provide either a single-ended or a differential output current linearly proportional to the differential input voltage [1.5]. Fig.1.1(a) shows the ideal transfer function of a V-I converter and Fig.1.1(b) a simplified block diagram of a typical V-I converter.

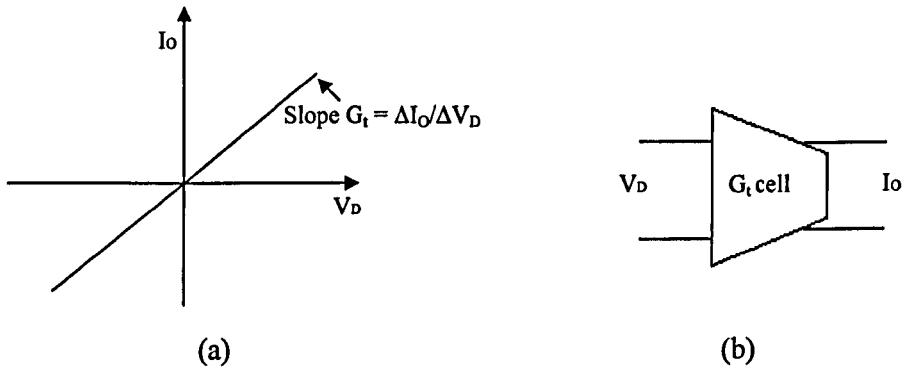

Figure 1.1 (a) Ideal transfer function of a V-I converter
(b) A block diagram of a V-I converter

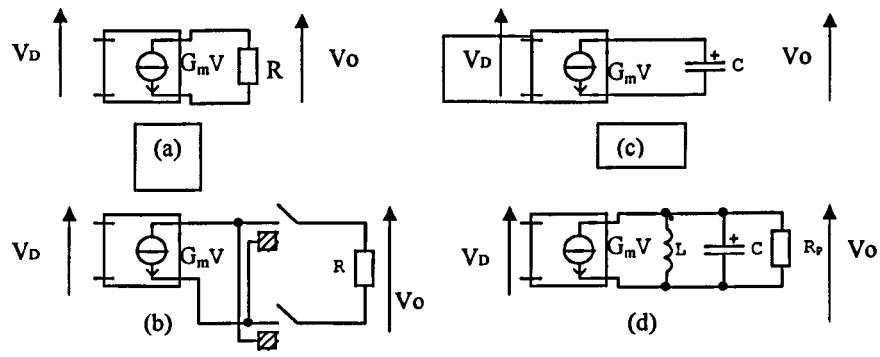

Figure 1.2 Typical V-I applications

(a) G_m-R variable gain amplifier **(c) G_m-C integrator filter**

(b) Active mixer with G_m and switches **(d) G_m-LC filter**

Fig.1.2 shows four typical applications using V-I converters, as shown in [1.3]. Fig.1.2(a) shows a V-I converter used as a voltage amplifier, where the gain of the amplifier is given by,

$$Av = \frac{V_O}{V_D} = G_m \cdot R \qquad (1.1)$$

Clearly, varying either G_m of R gives linear gain control.

Fig.1.2(b) is another application, used extensively in mixers as a part of a Radio Frequency (RF) circuit [1-6]. The maximum conversion gain of a conventional mixer for two square wave inputs is given by

$$Av = \frac{V_O}{V_D} = G_m \cdot 2/\pi \qquad (1.2)$$

Fig.1.2(c) shows a typical integrator used in filters. The gain can be expressed by the following:

$$Av = \frac{V_O}{V_D} = \frac{1}{s(C/G_m)} \qquad (1.3)$$

and a parallel inductor has been added in Fig 1.2(d) creating a 2nd-order band-pass filter for which the gain can be described as:

$$Av = \frac{V_O}{V_D} = G_m \cdot R_P \cdot \frac{\frac{s}{CR_P}}{\left(s^2 + \frac{s}{CR_p} + \frac{1}{LC}\right)} \qquad (1.4)$$

where s is the complex frequency variables used in Laplace Transfer analysis.

1.2 Voltage-to-Current converter design specifications

The trends towards system-on-a-chip as well as mixed-mode (analogue and digital design) solutions mean that the majority of integrated circuit developments are undertaken in MOSFET. Also with the reducing feature size of modern high frequency CMOS transistors, these devices are now capable of matching and exceeding the f_t of BJTs. With this in mind, the focus of this research work is on V-I converters designed for MOSFET implementation and the CMOS model for this research work is IBM 8RF_DM 0.13μm technology. Table 1.1 gives the target parameters and values chosen to be used for all of the V-I converters designed and developed in this research work. In the interests of minimizing power dissipation and voltage rail supply levels, the maximum device-operating current was chosen to be 1mA and the rail supplies not to exceed 5V total.

This research work focuses on combining between high G_t and good linearity with a typical bias current of 1mA. The classical V-I converter is a long-tailed pair amplifier with source degeneration. The value of the source degeneration resistor determines both the G_t value and the linear range of input voltages. This work will focus on discussion of determining the value of resistance we used. The most optimistic linear range of operation that could be achieved would be ±500mV and the transconductance value to be obtained for the ideal case would be 3.33mS with a source degeneration resistance of 600Ω [1-7]. A THD should better than -50dB and

the temperature range has been set from -40°C to +85°C, this being the standard industrial range. The technology selected for all of the work in this thesis is enhancement CMOS.

Table 1.1 Target specification

	Parameters	Values
1	Total supply voltage	3V to 5V
2	Linear range of operation	-500mV to +500mV
3	Typical transconductance	3.33mS
4	THD	< -50dB at 1GHz
5	Temperature range	-40°C to +85°C
6	Technology	MOSFET(CMOS)

1.3 Structure of the thesis

The thesis is divided into 7 chapters and, to make the reading straightforward, only the results of longer mathematical derivations are included in the relevant text, with the full working given in an appendix linked directly to the end of each chapter. In addition, chapter references are laid out at the end of each chapter as well as in a complete list in alphabetical order at the end of the thesis.

A detailed analysis of the transistor-models used throughout this research, is presented in Chapter 2. The process of developing a new circuit is supported by theoretical analysis. Unfortunately, analytical device model parameters are not easily obtained directly from simulation model parameters. A key part of this chapter is extraction of these model parameters from PSPICE device characteristics, at the particular operating conditions required for each design. It will be shown that a thorough analysis of these parameters is necessary for accurate design, based on 'hand-calculations', and several novel circuits of measuring the parameters of a single transistor are presented and analyzed in this chapter. Without them, in some conditions, the simulation results do not match the theoretical analysis.

In Chapter 3, a review of biasing techniques is included together with an introduction to current-biasing circuitry that has been chosen because of its superior performance over other similar configurations [1.8] and [1.9]. A critical review of the source follower [1.10], including analysis of both DC and small-signal conditions is presented. The theoretical performance described in Chapter 3 is developed further in Chapter 5, where a novel V-I circuit described.

A critical review of two existing MOSFET V-I converter techniques, [1.11-1.13], currently used to improve the linearity of differential V-I converters, is presented in Chapter 4. Both system level and transistor level V-I design implementations are included in this chapter. The operating principle of each of these techniques is reviewed, with examples of circuits, and a comparison made.

In Chapters 5 and 6 detailed circuits exemplifying each novel technique, described in Chapter 4, are presented with analysis and discussion of the results of simulation with respect to transconductance, linear range of operation, total harmonic distortion and frequency response.

Finally, the concluding chapter of the thesis, Chapter 7, contains an overview and reflection of the main body of work of the thesis, and outlines a circuit, thought to contain novel features, intended for future work.

Appended to the end of the thesis are conference and journal papers produced by the author on the various voltage-to-current converters described here-in.

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CHAPTER 2

DEVICE CHARACTERISATION

2.1 Introduction

This chapter deals with the measurement, by simulation, of some of the parameters of the N and P short-channel (0.13μm) IBM BSIM3 model MOSFETs used in the circuits described in this thesis.

Much information is, of course, given in the SPICE files for the devices, but not always presented in a manner, such as pictorially, that makes it easy to use by a circuit designer for initial hand calculations for a proposed design.

In the interests of minimizing power dissipation and rail supply levels, the maximum device-operating current was chosen to be 1 mA and the rail supplies not to exceed 2.5V.

To minimize device areas, a device width of 10μm is used, as some preliminary circuit investigations revealed its suitability.

Wherever possible the information obtained from the measurements, whether DC or AC, is presented graphically.

2.2 DC characteristics

2.2.1 Background to the measurements

In analogue circuit design, operation is normally in the saturated region of the drain characteristics. For both N and P channel devices this corresponds to $|V_{DS}| \geq |V_{GS}-V_T|$ where the symbols have their usual meanings. (See Appendix 2.1 for symbol definitions)

For an N channel device, operating in strong inversion, a first-order model that is good enough for hand calculation is [2.1],

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \qquad (2.1)$$

It follows from this that there is a separate family of curves for I_D vs.V_{GS}, for each value of V_{DS}.

However, for standardisation purposes, and because measurements are required for low values of V_{DS}, these were made with $|V_{GD}|=0$, corresponding to the circuit condition in which a MOSFET is used as a 'diode'. This gives I_D, V_{DS} curves that have a slightly larger V_{GS}, for a given I_D, than is the case for $V_{DS} > V_{GS}$ and this gives data that errs on the safe side for circuit estimations of maximum likely gate-source voltage drops.

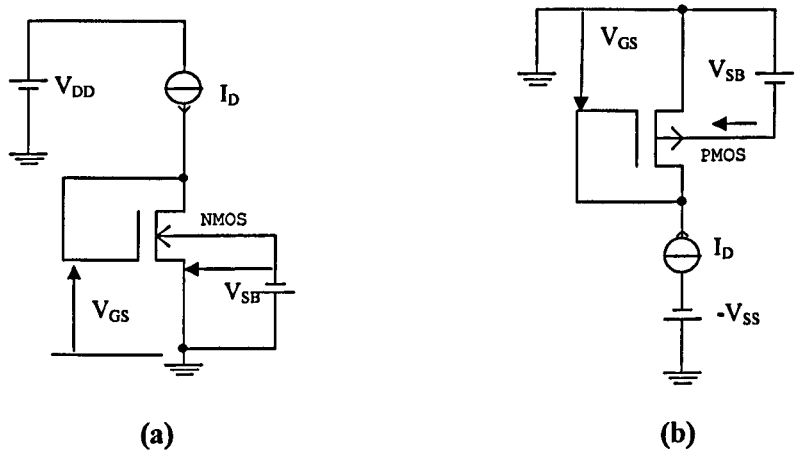


Figure 2.1 Test circuits for DC characteristics (a) NMOS (b) PMOS

The curves for I_D vs.V_{GS} for given values of V_{SB} are useful for two reasons. They present, visually, useful information for design and they permit evaluation of the parameters β and V_T in eqn. (2.1)

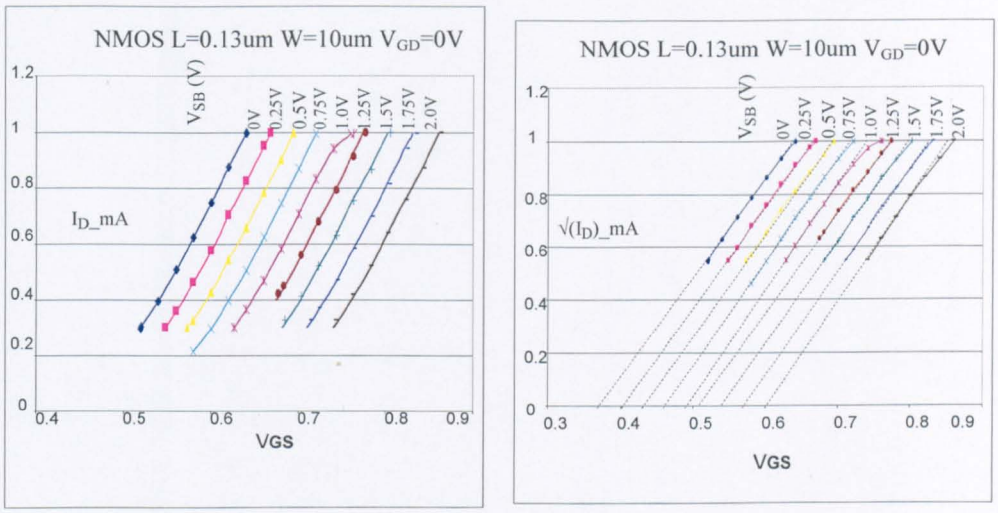
This, from eqn. (2.1), the 'effective' value of β for $V_{DG}=0$ is obtained from,

$$\sqrt{I_D} = \sqrt{\frac{\beta}{2}}(V_{GS} - V_T) \qquad (2.2)$$

To the extent that eqn. (2.1) is applicable, a plot of $\sqrt{I_D}$ versus V_{GS} should be a straight line with a slope $\sqrt{\beta/2}$ and a projected back V_{GS} intercept for the effective of V_T, at each value of V_{SB}.

2.2.2 Results

N channel results are presented in Figs2.2, 2.3 and Table1.1

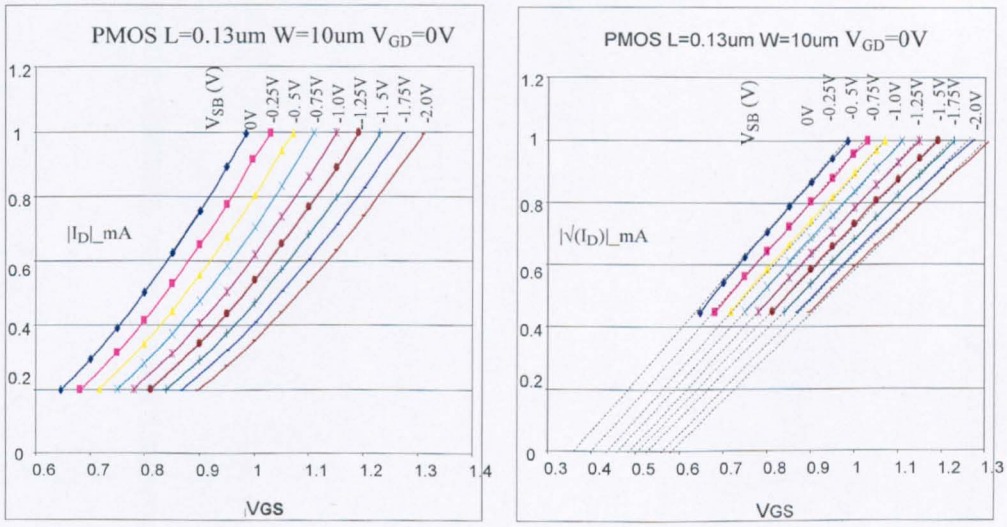


(a) (b)

Figure 2.2 DC Characteristics of NMOS

(a) I_D vs V_{GS}

(b) $\sqrt{I_D}$ vs V_{GS}



(a) (b)

Figure 2.3 DC Characteristics for PMOS

(a) $|I_D|$ vs V_{GS}

(b) $|\sqrt{I_D}|$ vs V_{GS}

	β (mA/V^2)			
W(u)	V_{SB}(V)	NMOS	V_{SB}(V)	PMOS
10	0	28.657	-0	5.308
	0.25	28.347	-0.25	5.103
	0.5	28.298	-0.5	4.861
	0.75	29.399	-0.75	4.715
	1	24.611	-1	4.453
	1.25	27.759	-1.25	4.212
	1.5	28.297	-1.5	3.981
	1.75	28.435	-1.75	3.76
	2	28.532	-2	3.574

Table 2.1 β as a function of V_{SB} (found from Fig. 2.2 and 2.3)

The variation of V_T(V)with V_{SB}(V) is shown in Fig.2.4

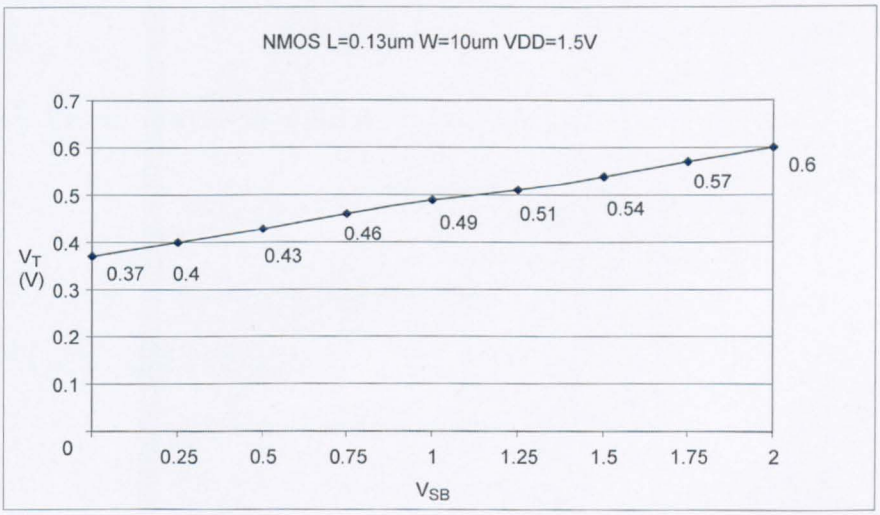


Figure 2.4 Variation of V_T with V_{SB}: N channel

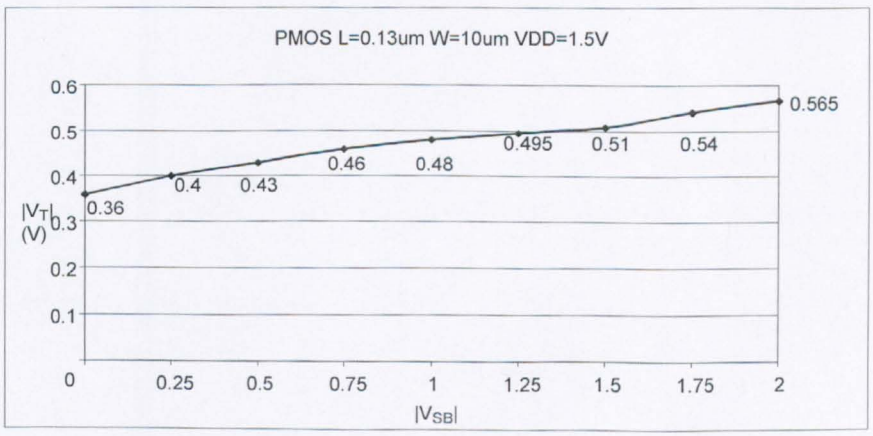


Figure 2.5 Variation of $|V_T|$ with $|V_{SB}|$: P channel

It is evident from Fig.2.2b and Table2.1 that for the case of the NMOS there is a straight line relationship between $\sqrt{I_D}$ and V_{GS} over the simulated range and the lines are sensibly parallel indicating that β is, to a first order, independent of V_{SB}.

In Fig.2.3(b), for the PMOS device, there is also a straight line relationship between $\sqrt{I_D}$ and $|V_{GS}|$ but these lines are not parallel indicating a variation of β with V_{SB}.

Figs2.4, 2.5 show the variation of the threshold voltage V_T with V_{SB}.

Theoretically [2.2],

$$V_T = V_T(V_{SB} = 0) + \gamma\left(\sqrt{|2\varphi_F + V_{SB}|} - \sqrt{|-2\varphi_F|}\right) \qquad (2.3)$$

However, in both cases there is an approximate linear relationship between V_T and V_{SB}.

In the case of the NMOS this is,

$$V_T(V) = 0.37 + \frac{(0.6 - 0.37)}{2} \cdot V_{SB}$$

or, $$V_T(V) \cong 0.37 + (0.115)\, V_{SB} \qquad (2.4)$$

For the PMOS the formula is,

$$V_T(V) \cong 0.36 + (0.103)\, V_{SB} \qquad (2.5)$$

2.2.3 Output Characteristics

Eqn.2.1 indicates that I_D depends on V_{DS}, as well as V_{GS}, but to proceed further and draw conclusions about the output incremental output resistance it is necessary to consider the nature of λ.

It is usually assumed that, in the saturated region of operation, λ is constant for a given V_{GS}.

This means that incremental output resistance is independent of V_{DS}.

$$r_{ds} = \left(\frac{\partial V_{DS}}{\partial I_D}\right)\Bigg|_{V_{DQ}} = \frac{(1+\lambda V_{DQ})}{I_D \lambda} \qquad (2.6)$$

The assumption $\lambda \neq f(V_{DS})$ is based on experimental observation of the output characteristics of MOSFETs, operating over a V_{DS} range suitable for analogue applications, and a (limited) amount of theoretical reasoning based on device physical electronics.

Fig.2.6 illustrates the approximation involved

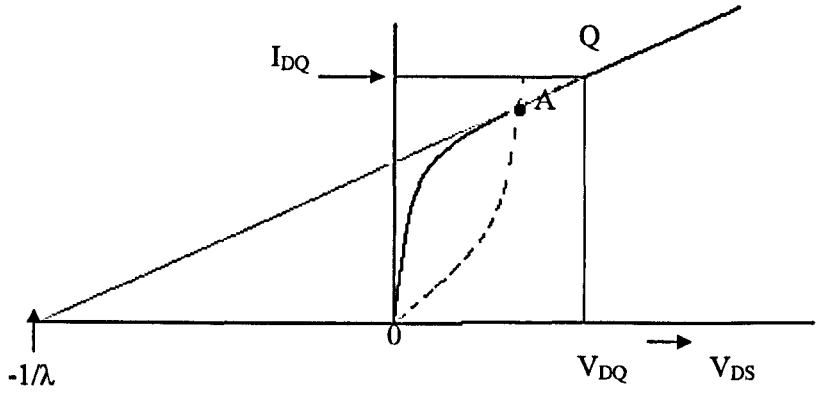


Figure 2.6 Illustrating eqn (2.6) for $\lambda \neq f(V_{DS})$ in the saturated region of an NMOS

The saturation region lies to the right of the dotted curve A for which the equation is

$$I_D = \frac{\beta}{2} V_{DS}^{\ 2} \ . \qquad (2.7)$$

The next step, one made in a number of older textbooks (e.g., See [2.3]) is to assume not only that λ is independent of V_{DS} but also of V_{GS}, with the result that the characteristics have been presented in the manner shown is Fig.2.7.

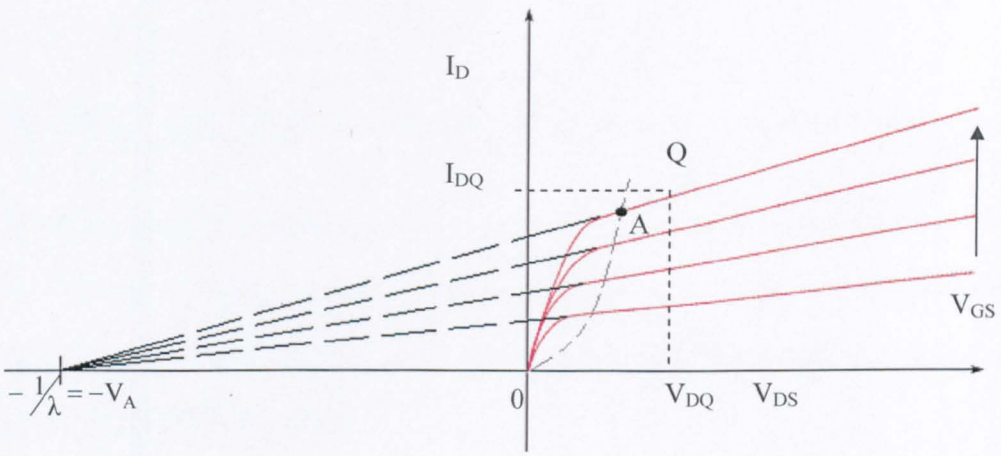


Figure 2.7 Output characteristics for $\lambda \neq f$ (V_{DS}, V_{GS}) in the saturated region

related Fig. 2.11

The common intersection point $V_{DS} = -1 / \lambda$ as been designated the Early Voltage, by analogy with the BJT parameter, and given the symbol V_A.

Simulation measurements were made at the output characteristics of an N channel MOSFET using the circuit of Fig.2.8

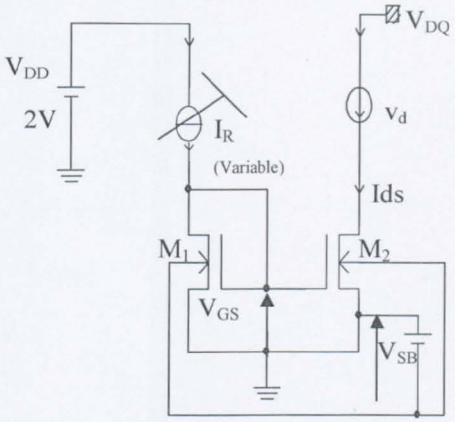


Figure 2.8 Circuit used to determine output characteristics of an NMOS

The reason for choosing this type of circuit rather than a amplifier for the common-source configuration is that it also supplies information on current –mirror operation described in the next chapter. A similar circuit, with reverse bias polarities, is applicable for P type MOSFETs.

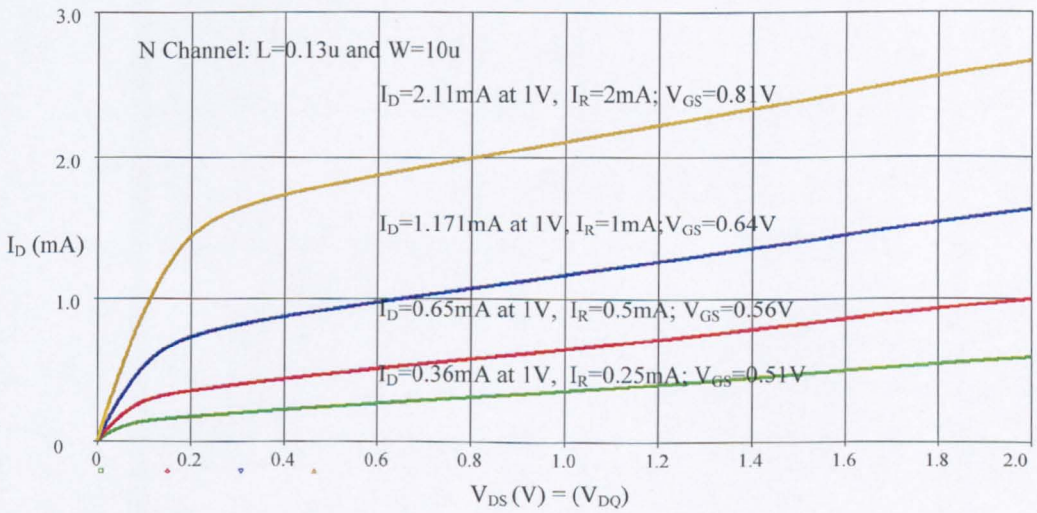


Figure 2.9 NMOS output characteristics for the circuit of Fig 2.8 with V_{SB}=0V. The data for each curve is given above it.

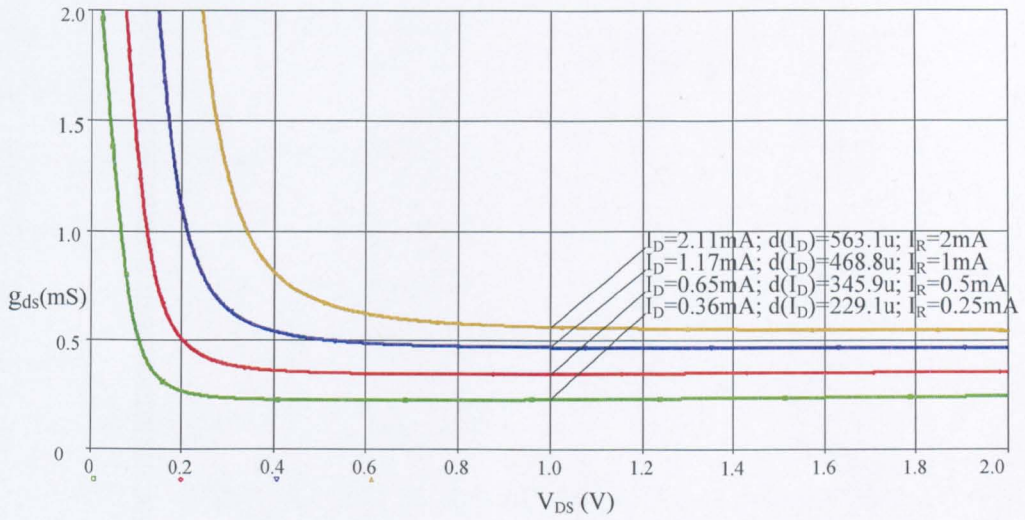


Figure 2.10 Incremental output conductance curves obtained from Fig 2.9

Figs2.9, 2.10 show the results of the simulation measurements and reveal unexpected features, which were confirmed by repetition, because they do not indicate a unique Early Voltage.

The DC characteristics of Fig.2.9 appear to show a linear dependence of I_D on V_{DS} for each value of V_{DS} (> 0.8V). Fig.2.10, showing g_{ds} as a function of V_{DS} for specified value of V_{GS}, confirms this because the resulting graphs are sensibly parallel to the V_{DS} axis for $V_{DS} > 0.8V$.

The variable slope of the curves for $V_{DS} > 0.8V$ (approx.) is characteristic of operation of the MOSFET on the voltage–saturation region. What the graph set of Fig.2.9 does not confirm is the existence of the common intersection point, for tangents at a given V_{DS} when extrapolated back, on the negative V_{DS}, such as that shown in Fig.2.7, i.e., it does not prove that $\lambda \neq f(V_{GS})$.

For it to be so, it requires $I_{DQ}\, r_{ds}$ to be constant for all values of V_{GS}. To investigate the matter further the following calculations were made.

I_R=0.25mA:

V_{A1}=[(1/229.1uA/V)×0.36mA]-1V=0.57V

I_R=0.5mA:

V_{A2}=[(1/345.9 uA/V)×0.65mA]-1V=0.87V

I_R=1mA:

V_{A3}=[(1/468.8 uA/V)×1.17mA]-1V=1.5V

I_R=2mA:

V_{A4}=[(1/563.1 uA/V)×2.11mA]-1V=2.75V

These results indicate that $\lambda \neq f(V_{DS})$ for a given V_{GS} but $\lambda = f(V_{GS})$, a fact that is not apparent from a cursory inspection of Fig.2.9

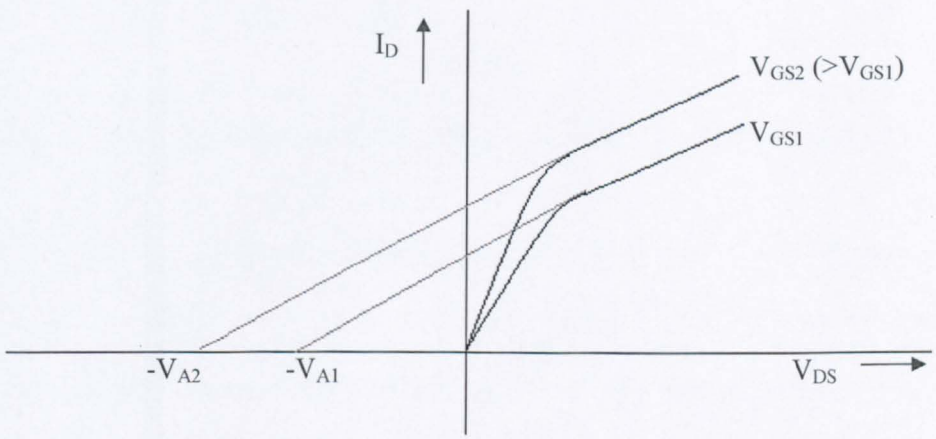


Figure 2.11 Showing the implications of NMOS measurements

Fig.2.11 shows the implication of the measurements for just two values of V_{GS} and Fig.2.12 shows a plot of V_A vs.V_{GS}.

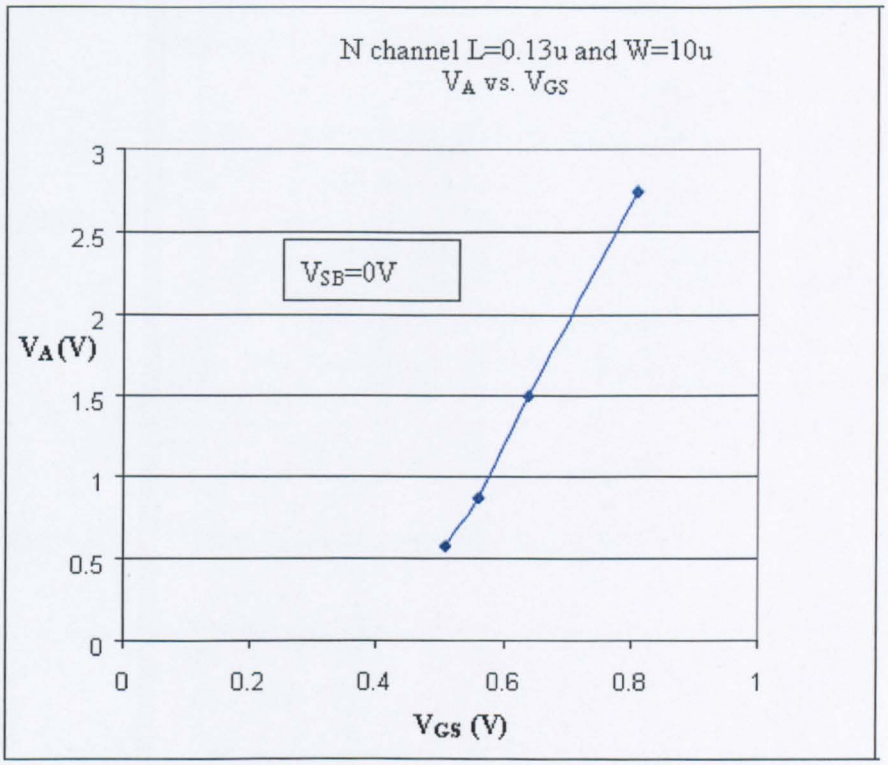


Figure 2.12 Variation of Early Voltage, V_A, with V_{GS} for NMOS device

For first-order design calculations it is reasonable to assume V_A is linearly related to V_{GS}. The reason for this behaviour was not investigated because it involves the physical electronics of MOSFETs with sub-micron channel lengths and that was considered to be outside the scope of this thesis.

Comparison figures for Figs2.9, 2.10, 2.12 for the case of the PMOS are shown in Figs2.13, 2.14, 2.15 respectively.

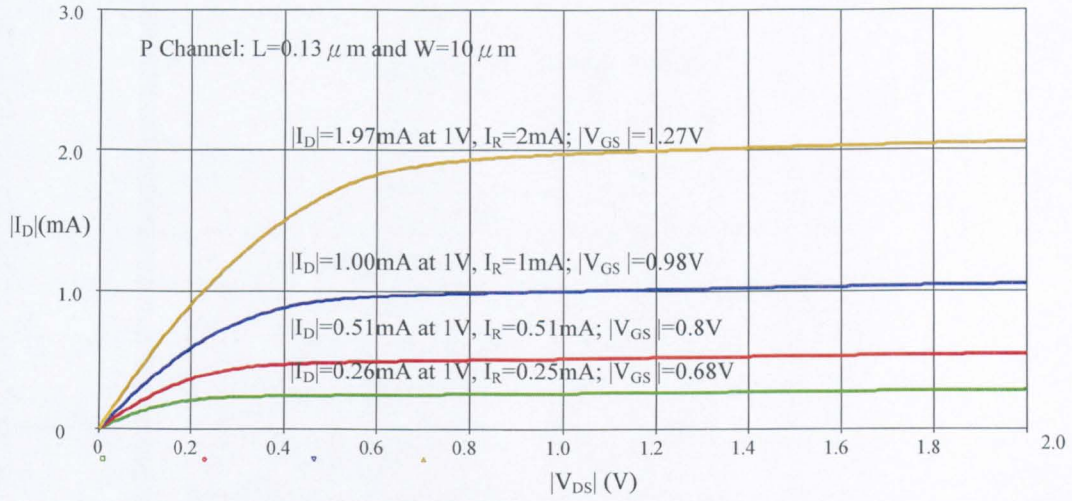


Figure 2.13 PMOS output characteristics for V_{SB}=0V

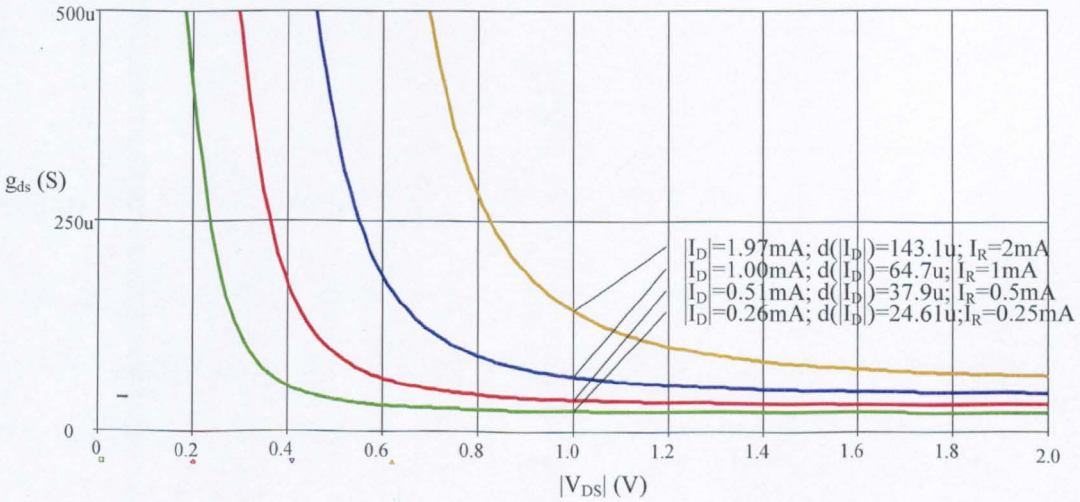


Figure 2.14 Incremental output characteristics curves obtained from Fig 2.13

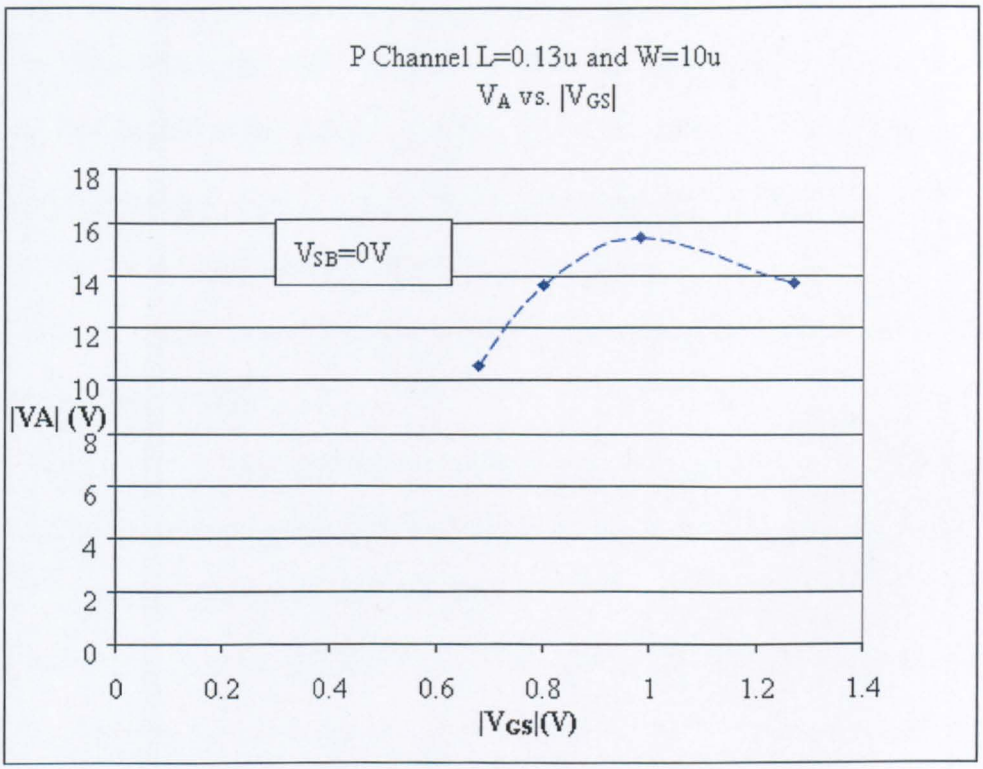


Figure 2.15 Variation of $|V_A|$ with $|V_{GS}|$ for a PMOS device

Comparing Fig.2.15 with Fig.2.10 it is apparent that the PMOS device affects a lower output conductance than the NMOS, for a given I_R, but this requires a much larger $|V_{GS}|$ (1.27V compared to 0.81V)

2.2.4 Transconductance ratios (g_m/g_{ds}) and (g_{mb}/g_m)

The transconductance ratios (g_m/g_{ds}), denoted by the symbol μ (but without a subscript in order to distinguish it from the symbol for carrier mobility), and (g_{mb}/g_m), denoted by the χ [2.4], appear in the analysis and design of V-Is via the dependence of the latter on feedback amplifiers and current generators.

Parameter μ characterises the theoretical maximum voltage gain of a single-stage common-source amplifier.

Parameter χ sets a limit to the maximum theoretical voltage gain of a source-follower in which the substrate of the MOSFET used is not connected to its source terminal.

Neither μ nor χ are specified in SPICE data.

A novel circuit method of determining their dependencies on DC bias conditions is presented in the next two sections. A third section validates the results obtained.

2.2.4(a) μ measurements

A test set-up for the measurement of μ is shown in Fig.2.16: a similar set up, but with reversed DC biasing, applies to PMOS devices.

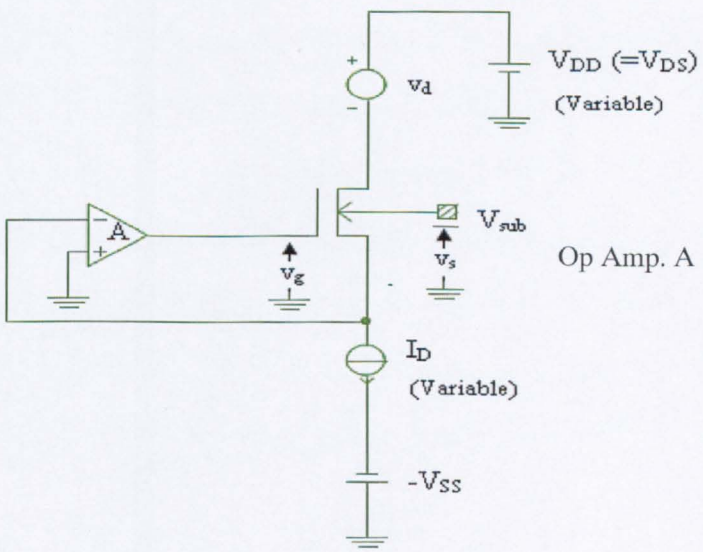


Figure 2.16 Test set-up for μ of an N channel MOSFET

In Fig.2.16, A is an op. amp. with a gain A_V (>>1) and a MOSFET input stage. Its purpose is to maintain constant, at earth potential, the source voltage of the MOSFET for different settings of I_{DS} and V_{DD} (=V_{DS}) and for any signal variations elsewhere in the circuit. Because the source is at earth the potential, V_{sub} applied to the substrate is a direct measure of the substrate-source voltage. Applying a small-signal (100mV peak) low-frequency (1KHz) sinusoidal signal, v_d, to the drain of the MOSFET does not causes a change in the source voltage or drain current because of the operation of A, which generates an opposing signal, v_{gs}, at the gate terminal: $v_d = v_{ds}$ and $v_{gs} = v_g$.

$$\text{Thus,} \quad i_d = g_m v_g + \frac{v_d}{r_{ds}} = 0 \tag{2.8}$$

$$\text{Hence,} \quad v_g = -\frac{v_d}{g_m r_{ds}} \tag{2.9}$$

$$\text{and,} \quad \mu = \frac{g_m}{g_{ds}} = g_m r_{ds} = \left|\frac{-v_d}{v_g}\right| \tag{2.10}$$

This analysis assumes $A_V = \infty$. However, a full analysis in Appendix 2.2 shows that μ is in error by not more than 0.1% if $A_V > 10^3$ at the test frequency used.

Before simulation measurements were made, the circuit was checked for frequency stability and was found to be stable and it was also established that the op amp. gain exceeded 60dB [2.5] at the operating frequency chosen for tests.

In the tests it was noted that v_s was only a few μV for each reading, i.e., negligible in comparison with the observed v_g, thus validating the assumption that $v_g = v_{gs}$.

Tabulated data for μ as a function of I_D for two values of V_{DS} (1V and 2V) and for two values of V_{sub} (0V and -2V) are given in Appendix2.3.

These data are presented graphically in Figs2.17, 2.18

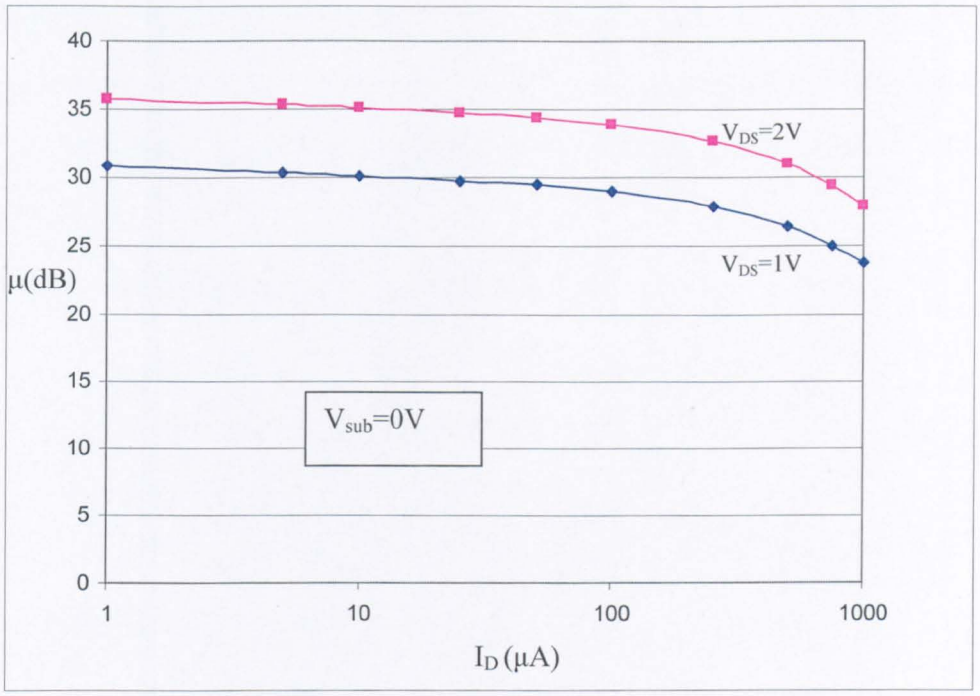


Figure 2.17 μ as a function of I_D vs. V_{DS} with V_{sub}=0V

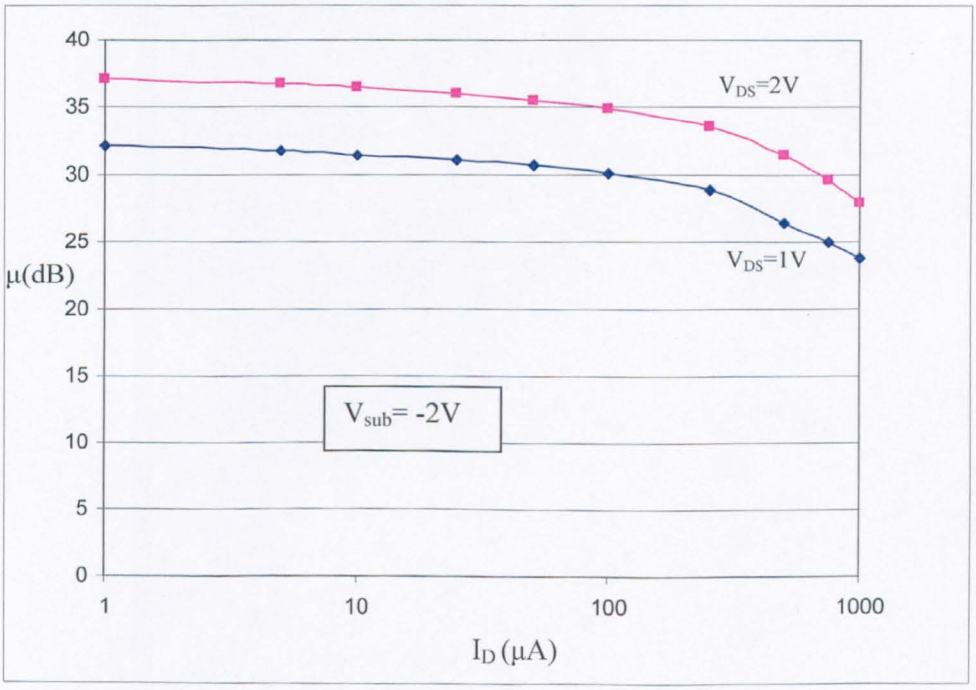


Figure 2.18 μ as a function of I_D vs. V_{DS} with V_{sub}= -2V

It appears that the two curves for V_{DS} in Fig.2.17 differ by a constant amount throughout the range of I_D under test. To check to see of this was, in fact, the case one of the curves was displaced vertically to see if the two graphs could be made to coincide.

The result is displayed in Fig.2.19 for ease V_{sub}=0V.

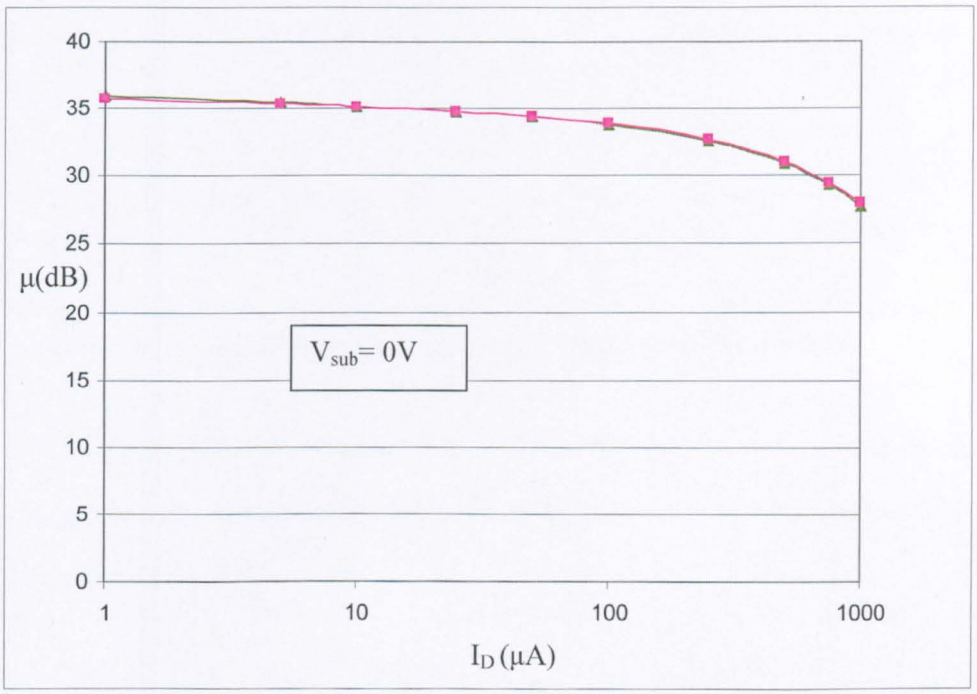


Figure 2.19 Showing the apparent coincidence of the two curves in Fig 2.17 when one of them is displaced vertically.

A similar displacement procedure was carried out for the plots of Fig.2.18: the result is shown in Fig.2.20

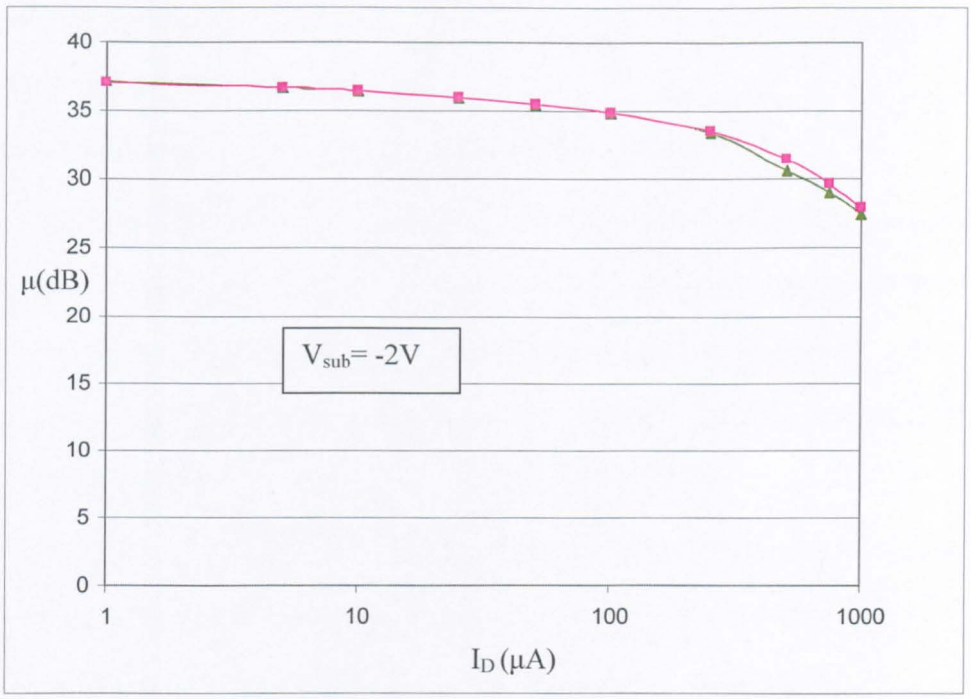


Figure 2.20 Showing the near coincidence of the curves in Fig.2.18

The general nature of the variation of μ with I_D and V_{DS} in the strong inversion region of operation can be explored theoretically by replacing λ by $(1 / V_A)$ in eqn (2.1) and proceeding as follows

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2 \cdot \left(1 + \frac{V_{DS}}{V_A}\right) \tag{2.11}$$

By simple differentiation, and re-arrangement of terms,

$$r_{ds} = \left.\frac{dV_{DS}}{dI_{DS}}\right|_{V_{GS}} = \frac{V_A + V_{DS}}{I_D} \tag{2.12}$$

and, $$g_m = \left.\frac{dI_{DS}}{dV_{DS}}\right|_{V_{DS}} = \sqrt{2I_D\beta\frac{(V_A + V_{DS})}{V_A}} \tag{2.13}$$

Hence, $$\mu = \sqrt{\frac{2\beta}{I_D V_A}}(V_A + V_{DS})^{3/2} \tag{2.14}$$

At low values of I_D the MOSFET enters the region of weak conversion where I_D is exponentially dependent on V_G [2.6].

In that case μ takes on a constant maximum value.

Considering, now, Fig 2.17 it is apparent that, for both values of V_{DS}, μ is inversely related to I_D and tends toward a constant value at low currents. At higher currents, in the strong inversion region, eqn 2.13 predicts that $\log \mu \propto \log I_D$ for a given V_{DS} (i.e., μ. in dB is linearly dependent on I_D plotted to a log scale) and this is not precisely true for the NMOS tested.

However, eqn (2.13) does predict a constant separation of the two curves in Fig 2.17 with variation in I_D. In assessing this it must be borne in mind that, for a given I_D, V_{GS} decreases as V_{DS} increases and for each V_{GS} there is a different V_A.

Thus, $$\mu_1 = \sqrt{\frac{2\beta}{I_D V_{A1}}}(V_{A1} + V_{DS1})^{3/2} \qquad (2.15a)$$

and $$\mu_2 (> \mu_1) = \sqrt{\frac{2\beta}{I_D V_{A2}}}(V_{A2} + V_{DS2})^{3/2} \qquad (2.15b)$$

Hence, $$\left(\frac{\mu_2}{\mu_1}\right) = \sqrt{\frac{V_{A1}}{V_{A2}}}\left(\frac{V_{A2} + V_{DS2}}{V_{A1} + V_{DS1}}\right)^{3/2} \qquad (2.16)$$

The maximum observed values of μ for the NMOS is well over an order of magnitude lower than that of a BJT operating under the same DC bias conditions. For the BJT, $\mu=(V_A/V_t)$ where V_t = 'Thermal voltage' $(KT/q) \approx 25mV$ at room temp : for $V_A > 75V$, and an operating current of 1mA $\mu \approx 3000$ for a BJT compared with $\mu < 25$ for the NMOS.

2.2.4(b) χ measurements

A variation of the set-up of Fig.2.16, shown in Fig.2.21, facilitates the measurement of (g_{mb}/g_m). A similar set-up with reversed bias polarities applies to PMOS devices.

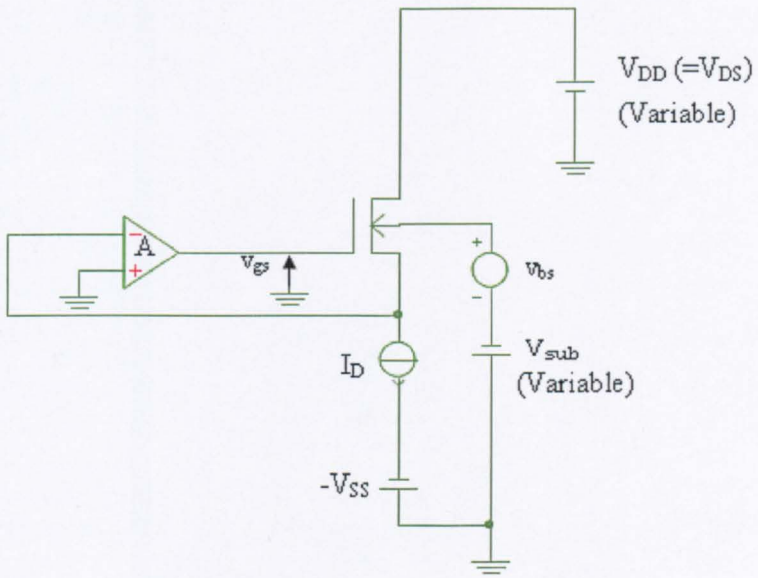


Figure 2.21 Set-up for finding (g_{mb}/g_m) for an NMOS

In this case a small amplitude (50mV) low frequency (1 KHz) sinusoidal signal, v_{bs}, is applied to the substrate in series with a variable (negative) substrate voltage V_{sub}. The amplifier A maintains the source of the MOSFET at earth potential and there is no change in drain current because the amplifier's output voltage v_{gs} nullifies any effect produced by v_{bs}

$$i_d = 0 = g_m v_{gs} + g_{mb} v_{bs} \tag{2.17}$$

$$\therefore \quad \left|\frac{g_{mb}}{g_m}\right| = \left|\frac{v_{gs}}{v_{bs}}\right| \tag{2.18}$$

Tabulated data for χ as a function of I_D for two values of V_{DS} (1V and 2V) and two values of V_{sub} (0V and 2V) are given in Appendix2.4

These data are presented graphically in Fig.2.22

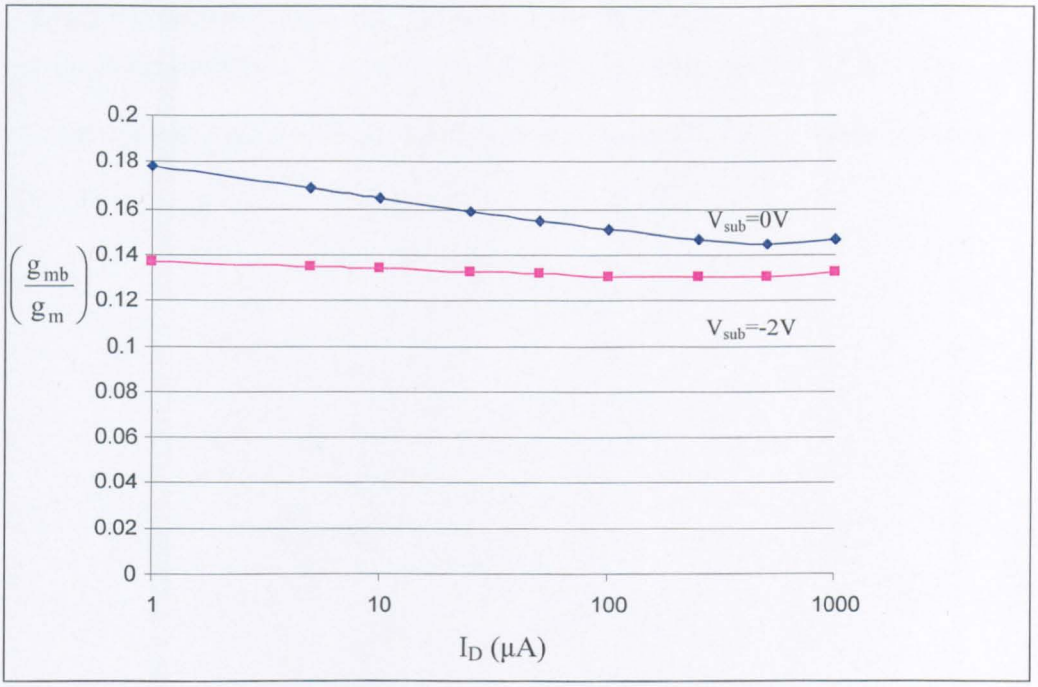


Figure 2.22 Variation of (g_{mb}/g_m) with I_D for an NMOS MOSFET for V_{DS}= 1V and two values of V_{sub}

The variation of (g_{mb}/g_m) with V_{sub} is to be expected since, theoretically [2.7],

$$\left(\frac{g_{mb}}{g_m}\right) = \frac{\gamma}{2\sqrt{2\varphi_F + V_{SB}}} \tag{2.19}$$

where the symbol have the meanings defined in Appendix2.1.

2.2.4(c) Validation of parameter measurement techniques

To check the validity of the measurement techniques described in 2.2.4(a) for μ and 2.2.4(b) for $\chi(g_{mb}/g_m)$ an independent test was made, the circuit for which in shown in Fig.2.23.

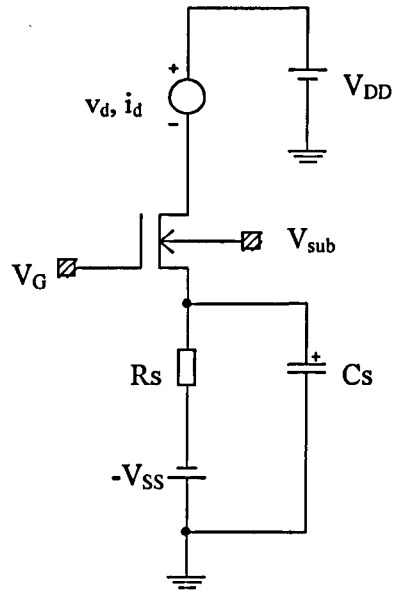


Figure 2.23 Test circuit for output resistance measurement

The procedure was as follows. With V_{DD}=1V, V_{SS}=2V and R_S=4KΩ (arbitrary but convenient choices) V_G was adjusted at that, with V_{sub}=0V, V_S=0V: hence, V_{DS}=V_{DD}, and I_D=0.5mA. The incremental output resistance v_{ds}(=v_d/i_d) was measured for the case of a decoupled source. This requires the use of a capacitor C (1F, totally impractical in a laboratory but acceptable in a simulation) having effectively zero reactance at the frequency of measurement. (1KHz).

The output resistance Ro was then found when C was absent.

The process was repeated for V_{sub}=-2V.

For calculation proposes [2.8],

$$R_O = R_S + r_{ds}[1 + (g_m + g_{mb})R_S] \qquad (2.20)$$

Rearranging and substituting μ for $g_m r_{ds}$ gives,

$$R_O = r_{ds} + R_S\left[1+\mu\left(1+\frac{g_{mb}}{g_m}\right)\right] \qquad (2.21)$$

For the case V_{sub}=0V, Appendix 2.3 gives μ=21.04 at I_D=0.5mA, and Appendix2.4 gives (g_{mb}/g_m)=0.1446

Substituting in eqn.2.21,

$R_O(K\Omega)$=3.67(measured value) + 4 [1+ {(1.1446)×21.04}]

or, $R_O(K\Omega)$=103.99 (calculated)

This compares with 103.27KΩ (simulation test).

For the case V_{sub}=-2V, Appendix2.3 gives μ=23.2 at I_D=0.5mA and Appendix2.4 gives (g_{mb}/g_m)=0.13097

Substituting in eqn.2.21,

$R_O(K\Omega)$=4.05(measured value) + 4 [1+ {(1.13097)× 23.2}]

or, $R_O(K\Omega)$=113 (calculated)

This compares with 113.8KΩ (simulation result)

The excellent agreement between the two values of R_O in each case validates the accuracy of the measurement techniques described in sections 2.2.4(a) and 2.2.4(b)

2.2.5 Inter-electrode capacitor

Fig.2.24 shows a small signal equivalent circuit of a NMOS transistor [2.8] presented in Appendix2.1 and repeated here for convenience in the present discussion.

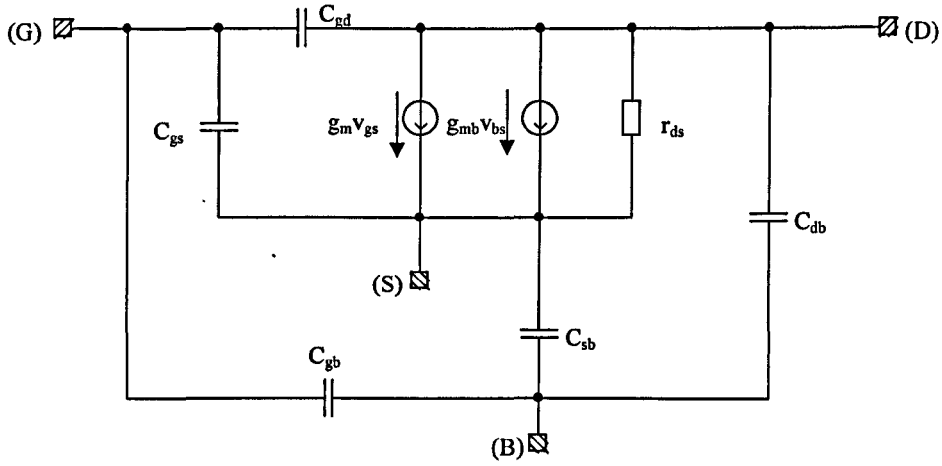


Figure 2.24 Small signal equivalent circuit of an NMOS transistor

Fig.2.25 shows a simplified version, which applies when the substrate (B) is connected to the source terminal (S). As C_{gb} can not be separated from C_{gs} in normal MOSFET operation it is taken to be lumped in with C_{gs} in Fig.2.25 and henceforth.

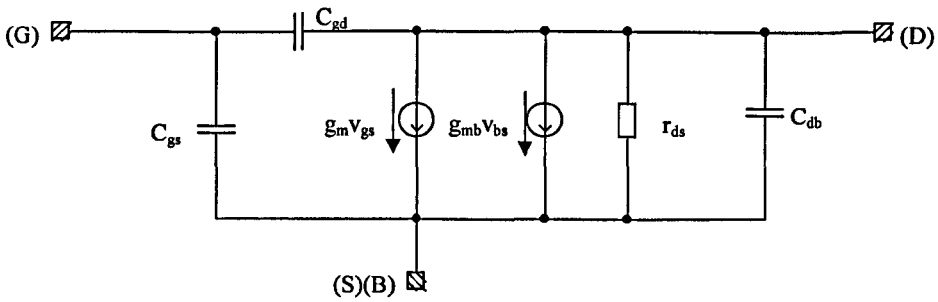


Figure 2.25 Simplified version of Fig 2.24 when (S) and (B) are connected together.

The problem of measuring the three capacitances C_{gs}, C_{gd} and C_{db} requires same ingenuity but can be solved by performing a sequence of tests that determines separately the following combinations: $(C_{gs}+C_{gd})$; $(C_{gd}+C_{db})$; $(2C_{gs}+C_{gd}+C_{db})$.

2.2.5(a) Test 1: Determination of $(C_{gs}+C_{gd})$

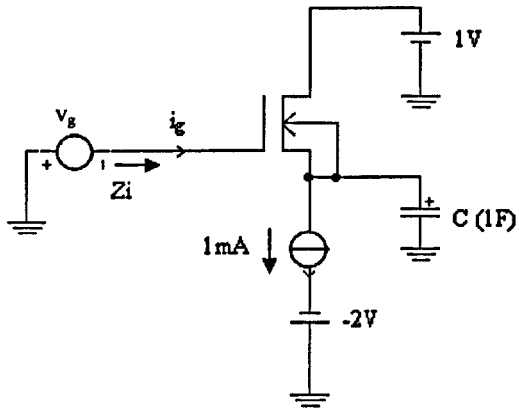


Figure 2.26 Test circuit for $(C_{gs}+C_{gd})$

In the test circuit of Fig.2.26 a small amplitude (20mV) swept frequency sinusoidal test signal v_g applied to the gate of the test MOSFET produces a gate current i_g. The capacitor C (1F) is a source decupling capacitor. Cut frequencies for which its impedance is negligible we can write,

$$Zi = \frac{v_g}{i_g} = \frac{1}{j\omega(C_{gs}+C_{gd})} \qquad (2.22)$$

On a plot of |Z|, to a dB scale with a reference value of 1Ω, against frequency on a log scale the point at which |Zi| = 1Ω corresponds to f_o, say

Thus, $(C_{gs}+C_{gd}) = 1/2\pi f_o$ (2.23)

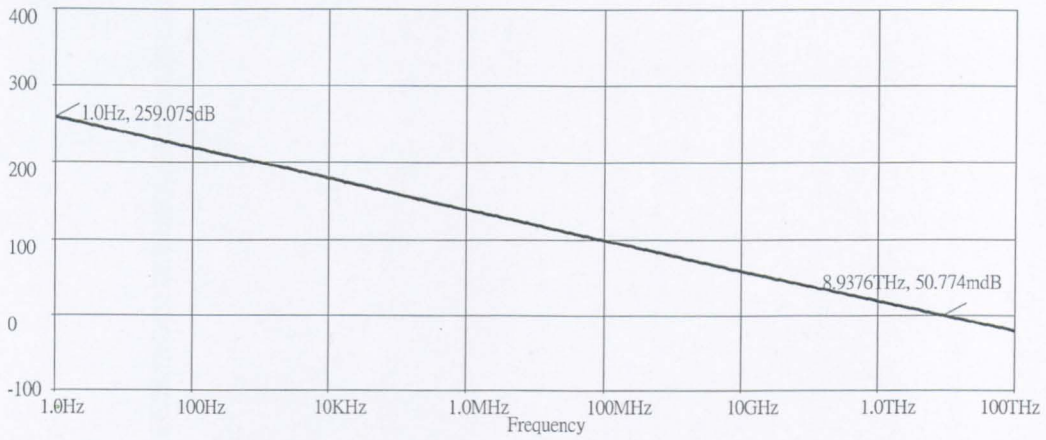


Figure 2.27 |Zi| vs. f for the circuit of Fig. 2.26

From Fig.2.26, $|Zi| \approx 0$ dB (actually, $50.77 \times 10\text{-}3$) at $f_o = 8.9376$THz

Hence, $(C_{gs}+C_{gd}) \approx 17.8$fF

2.2.5(b) Test 2: Determination of (C_{gd}+C_{db})

Fig.2.28 shows a test circuit for (C_{gd}+C_{db}), for which the test procedure mirrors that of the precious section.

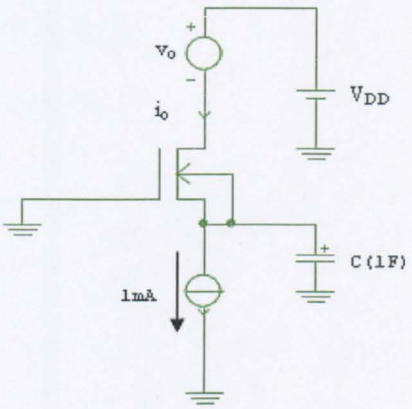


Figure 2.28 Test circuit for (C_{gd}+C_{db})

By inspection the admittance at the drain of the MOSFET

is, $$Y_o = \frac{i_o}{v_o} = g_{ds} + j\omega(C_{gs} + C_{db}) \qquad (2.24a)$$

or, $$Z_o = \frac{1}{g_{ds} + j\omega(C_{gs} + C_{db})} \qquad (2.24b)$$

A plot of |Zo| vs. f is shown in Fig.2.29

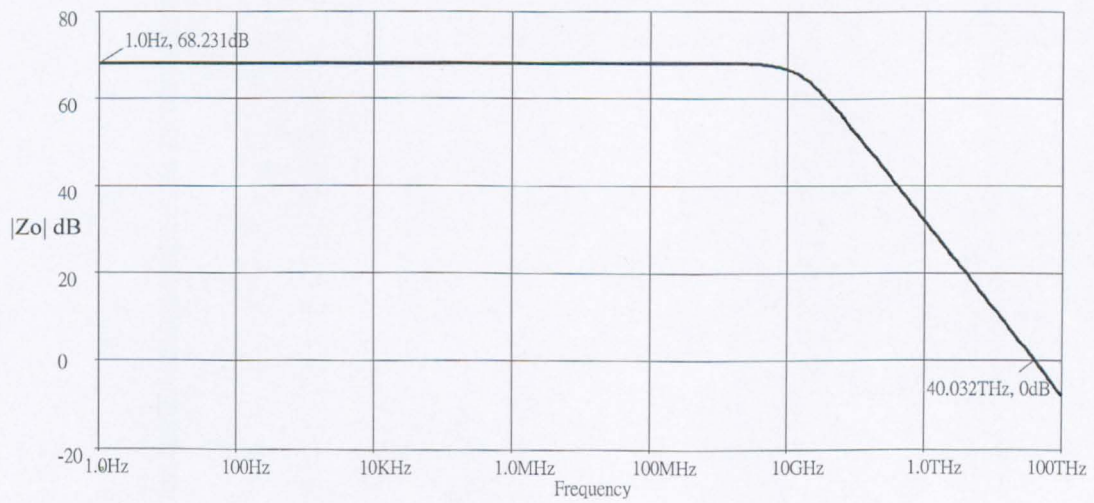


Figure 2.29 |Zo| vs. f for circuit of Fig 2.28

The 'constant' value of |Zi| at low frequencies gives $g_{ds} = 6.1677\text{mS}$

Above $f \approx 10\text{GHz}$ the slope of the graph is -40dB / decade indicating a dominance of susuceptamce over conductance in the expression for admittance.

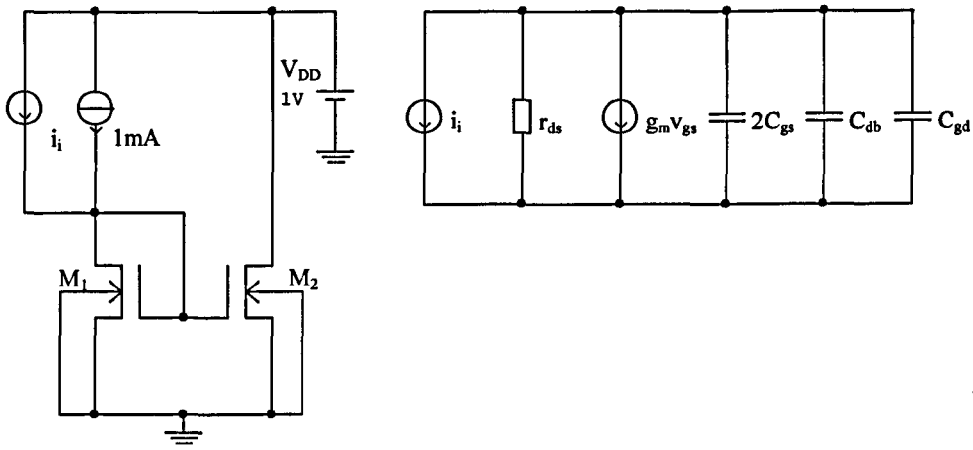
For $f_o = 40.032\text{THz}$

$$|Z_o| \approx 1\Omega$$

so, $$(C_{gd} + C_{db}) = \frac{1}{2\pi \times 40.032 \times 10^{12}}\text{F} = 3.97\text{fF}$$

2.2.5(c) Test 3: Determination of ($2C_{gs}+C_{gd}+C_{db}$)

The test circuit for this is a simple 1:1 current mirror (Fig.2.30a) driven by a small swept frequency test current i_i.



(a) (b)

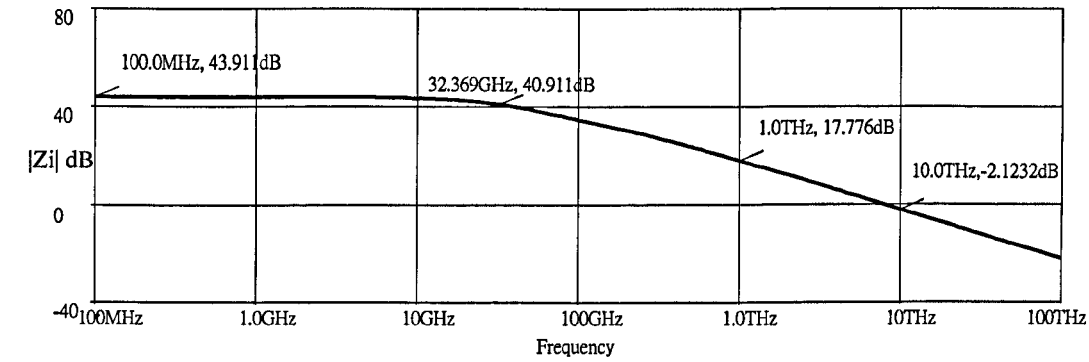
Figure 2.30 (a) Test circuit (b) Small signal equivalent circuit

In choosing this advantage was made of the fact that the gate-source capacitance, C_{gs}, is doubled but the C_{db} of M_2 is not 'seen' by the input current. By inspection of Fig.2.31b,

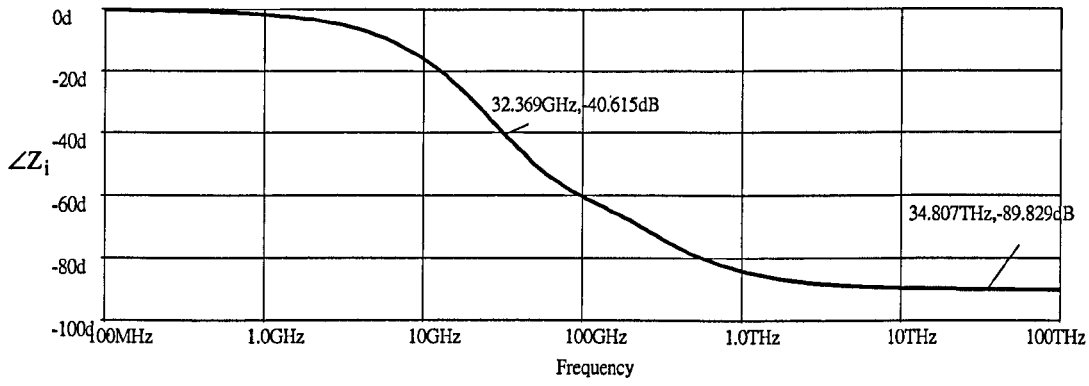
$$Y_i = v_g\left|(g_{ds}+g_m)+j\omega(2C_{gs}+C_{db}+C_{gb})\right| \qquad (2.25)$$

A plot of |Zi| vs. f, both on log values should give a -3dB point at,

$$f_o = \frac{(g_{ds}+g_m)}{2C_{gs}+C_{db}+C_{gb}} \qquad (2.26)$$



(a)



(b)

Figure 2.31 (a) |Zi| vs. f (b) $\angle Z_i$ vs. f for Fig 2.30a

Fig.2.31a shows a plot of |Zi| vs. f and it appears that after an apparent -3dB at 32.369GHz the role off is -20dB. (The fall between 1THz and 10THz is actually 19.89dB)

However, the phase curve (Fig.2.31b) shows an inexplicable kink so the value of f_o must be regarded as approximate.

Using the data on Fig.2.31a,

$$2C_{gs}+C_{db}+C_{gd} = 33fF$$

2.2.5(d) Calculations of C_{gs}, C_{gd} and C_{db} from tests

We now have three equations and three unknowns.

Thus, $C_{gs}+C_{gd} = 17.8fF$

$C_{gd}+C_{db} = 3.97fF$

and, $2C_{gs}+C_{gd}+C_{db} = 33fF$

Solving these eqns gives,

$C_{gs}=14.5fF$; $C_{gd}=3.33fF$; $C_{db}=0.64fF$.

In the case of the P channel MOSFET, the values obtained by simulation are follows:

$C_{gs}+C_{gd} = 18.6fF$

$C_{gd}+C_{db} = 4.095fF$

$2C_{gs}+C_{gd}+C_{db} = 34.09fF$

Solving above eqns. gives,

$C_{gs}=15fF$; $C_{gd}=3.6fF$; $C_{db}=0.495fF$.

2.2 Summary

In this chapter the DC and some small-signal parameters of both N and P channel MOSFETs with channel length (L) of 0.13μm and channel width (W) of 10um have been determined by simulation on test circuits and the results have been presented in tabular and/or graphical from.

Some interesting results were obtained. In particular; the threshold voltage, V_T, was found to be approximately linearly related to the source-substrate voltage, V_{SB}, rather than to the square root of V_{SB}, as stated in standard test books [2.10] (dealing with devices for which L >1u); the DC output characteristics did not display a unique Early Voltage. A measurement technique thought to be novel for the direct determination of the dependence of the transconductance ratios (g_m/g_{ds}) and (g_{mb}/g_m) was proposed. Finally, tests we made to find the values of the inter-electrode capacitances C_{gs}, C_{gd}, C_{db}. The value of C_{gd} was not insignificant, and might be expected from the textbook discussion on 'long channel devices' (L >> 1um)

*This conclusion was subsequently confirmed by a note in a book. (Fundamentals of High Frequency CMOS Analog Design, D. Leblibici and Y. Leblibici, Cambridge University Press, 2009, pp.24). However, no explanation is given for the phenomenon.

2.3 References

[2.1] Allen P. E. and Holberg D. R., 'CMOS Analog Circuit Design', Oxford University Press, Second Edition, New York, 2002, pp. 76

[2.2] Allen P. E. and Holberg D. R., 'CMOS Analog Circuit Design', Oxford University Press, Second Edition, New York, 2002, pp. 40

[2.3] Gray P. R., Hurst P. J., Lewis S. H. and Meyer R. G., 'Analysis and Design of Analog Integrated Circuits', John Wiley & Sons, Inc., Fourth Edition, New York, 2001, pp. 43-44

[2.4] Gray P. R., Hurst P. J., Lewis S. H. and Meyer R. G., 'Analysis and Design of Analog Integrated Circuits', John Wiley & Sons, Inc., Fourth Edition, New York, 2001, pp. 53

[2.5] National Semiconductor, 'LMC660 CMOS Quad Operational Amplifier General Description', Datasheet, 2006

[2.6] Smith S.,'Microelectronic Circuits', Oxford University Press, Third Edition, New York, 1991, pp. 308-311

[2.7] Gray P. R., Hurst P. J., Lewis S. H. and Meyer R. G., 'Analysis and Design of Analog Integrated Circuits', John Wiley & Sons, Inc., Fourth Edition, New York, 2001, pp. 54

[2.8] Gray P. R., Hurst P. J., Lewis S. H. and Meyer R. G., 'Analysis and Design of Analog Integrated Circuits', John Wiley & Sons, Inc., Fourth Edition, New York, 2001, pp. 55

[2.9] Gray P. R., Hurst P. J., Lewis S. H. and Meyer R. G., 'Analysis and Design of

Analog Integrated Circuits', John Wiley & Sons, Inc., Fourth Edition, New York, 2001, pp. 195-197

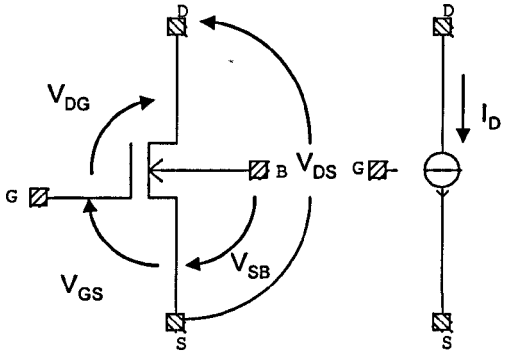
[2.10] Allen P. E. and Holberg D. R., 'CMOS Analog Circuit Design', Oxford University Press, Second Edition, New York, 2002, pp. 73-79

[2.11] Gray P. R., Hurst P. J., Lewis S. H. and Meyer R. G., 'Analysis and Design of Analog Integrated Circuits', John Wiley & Sons, Inc., Fourth Edition, New York, 2001, pp. 74

2.4 Appendix 2

Appendix 2.1 MOSFET Symbol definition and parameter relationships. (Based on [2.11])

DC Relationship (Strong inversion region)



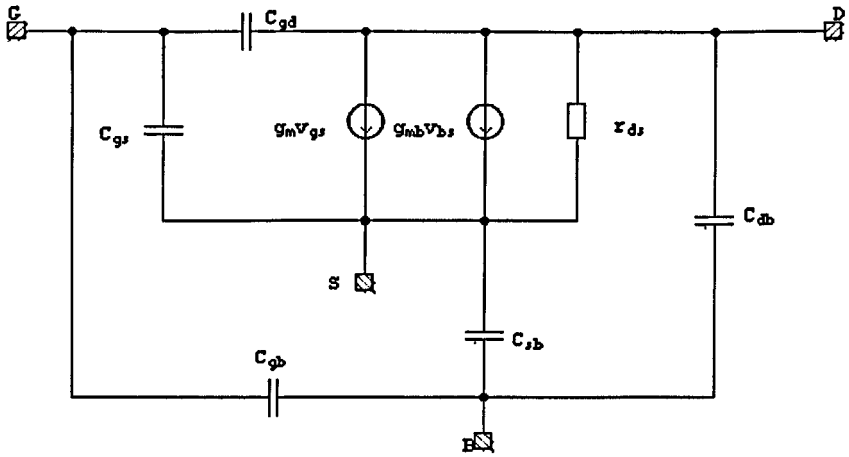
Saturated region (Current saturation)	'Triode region' (Voltage Saturation)
$V_{GS} > 0$ and $V_{GD} < V_T$ ($V_{DG} > V_T$)	$V_{DS} < (V_{GS}-V_T)$ or $V_{GD} > V_T$
$I_D(=I_{DS}) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS})$	$I_D(=I_{DS}) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2(V_{GS}-V_T)V_{DS}-V_{DS}^2\right]$
or, $I_D = \frac{\beta}{2}(V_{GS}-V_T)^2(1+\lambda V_{DS})$	or, $I_D = \frac{\beta}{2}\left[(V_{GS}-V_T)^2(V_{GD}-V_T)^2\right]$
where $\beta=(\mu_n C_{ox} W/L)$	
W= gate width; L= gate length	

Threshold voltage: $$V_T = V_{T0} + \gamma\left[\sqrt{2\varphi_f + V_{SB}} - \sqrt{2\varphi_f}\right]$$

Threshold voltage parameter: $$\gamma = \frac{1}{C_{ox}}\sqrt{2q\varepsilon N_A}$$

Oxide capacitance: $$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = 3.45\text{fF/um}^2 \text{ for } t_{ox} = 100\text{ Å}$$

Small-signal relationships



Small-Signal Operation (Active Region) Parameters

Top-gate transconductance:

$$\left(\frac{\partial I_D}{\partial V_{GS}}\right) = g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)(1+\lambda V_{DS}) = \sqrt{2I_D\mu_n C_{ox}\frac{W}{L}}(1+\lambda V_{DS}) = \sqrt{2I_D\beta}(1+\lambda V_{DS})$$

Transconductance-to-current ratio:

$$\frac{g_m}{I_D} = \frac{2}{V_{GS}-V_T}$$

Body-effect transconductance:

$$g_{mb} = \frac{\gamma}{2\sqrt{2\varphi_f + V_{SB}}}g_m = \chi g_m\left(=\frac{\partial I_D}{\partial V_{BS}}\right)\Bigg|_{V_{GS}=\text{constant}}$$

Channel-length modulation parameter:

$$\lambda = \frac{1}{V_A} = \frac{1}{L_{eff}}\frac{dX_d}{dV_{DS}}$$

where X_d is the depletion-layer width.

Output resistance:

$$r_{ds} = \frac{(1+\lambda V_{DS})}{\lambda I_D} = \frac{L_{eff}}{I_D}\left(\frac{dX_d}{dV_{DS}}\right)^{-1}$$

Effective channel length:

$$L_{eff} = L_{drwn} - 2L_d - X_d$$

Maximum gain:

$$\mu \triangleq g_m r_{ds} = \frac{1}{\lambda}\frac{2}{V_{GS}-V_T} = \frac{2V_A}{V_{GS}-V_T}$$

Source-body depletion capacitance:

$$C_{sb} = \frac{C_{sb0}}{\left(1+\frac{V_{SB}}{\psi_0}\right)^{0.5}}$$

Drain-body depletion capacitance:

$$C_{db} = \frac{C_{db0}}{\left(1+\frac{V_{DB}}{\psi_0}\right)^{0.5}}$$

Gate-source capacitance:

$$C_{gs} = \frac{2}{3} WLC_{ox}$$

Transition frequency:

$$f_T = \frac{g_m}{2\pi\left(C_{gs}+C_{gd}+C_{gb}\right)}$$

Appendix 2.2 Analysis of the μ measurement circuit

Fig.A2.2 shows a small signal low-frequency equivalent circuit of Fig.2.21 in the text and the condition that exist when a signal, v_d, is applied to the drain of the MOSFET. The op-amp. voltage gain, A_V, and incremental output resistance, R_S, of the current sink, I_{DS}, are considered to be finite.

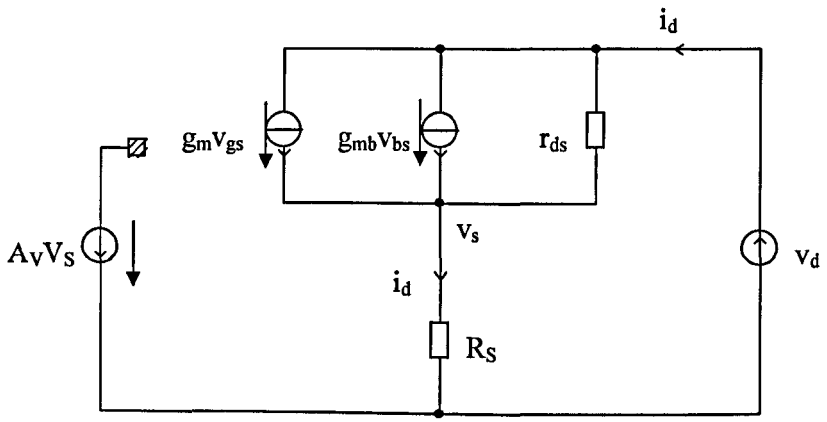


Figure A2.2 Small signal equivalent circuit for Fig 2.21 of the text

$$g_m v_{gs} = g_m(v_g - v_s) = g_m(-Av_s - v_s) = -(A_V + 1)g_m v_s$$

$$g_{mb} v_{bs} = g_{mb}(v_b - v_s) = -g_{mb} v_s \text{ (since } v_b = 0v).$$

KCL at the drain gives,

$$i_d = g_m v_{gs} + g_{mb} v_{bs} + (v_d - v_s)/r_{ds}$$

Substituting for v_{gs} and v_{bs},

$$i_d = -(A_V + 1)g_m v_s - g_{mb} v_s + (v_d - v_s)/r_{ds}$$

KCL at the source gives,

$$\therefore \frac{v_s}{R_S} = -[(A_V + 1)g_m + g_{mb}]v_s + \frac{v_d - v_s}{r_{ds}}$$

Transposing,

$$v_s = \left[\frac{1}{R_S} + (A_V + 1)g_m + g_{mb} + \frac{1}{r_{ds}}\right] = \frac{v_d}{r_{ds}}$$

or,

$$\frac{v_s}{v_d} = \frac{1}{r_{ds}\left[\frac{1}{R_S} + (A_V + 1)g_m + g_{mb} + \frac{1}{r_{ds}}\right]}$$

$$\frac{v_s}{v_d} = \frac{1}{\left(\frac{r_{ds}}{R_S}+1\right)+r_{ds}[(A_V+1)g_m+g_{mb}]}$$

But, $v_g = -A_V v_s$

$$\therefore v_g = \frac{-A_V v_d}{\left(\frac{r_{ds}}{R_S}+1\right)+r_{ds}[(A_V+1)g_m+g_{mb}]}$$

For $R_S >> r_{ds}$, the first bracketed term is the denominator is insignificant compared with the second bracketed term so this reduces to,

$$v_g = \frac{-A_V v_d}{(A_V+1)g_m r_{ds}+g_{mb}r_{ds}}$$

or, $$\frac{v_d}{v_g} = -\frac{(A_V+1)g_m r_{ds}+g_{mb}r_{ds}}{A_V}$$

$$\therefore \left|\frac{v_d}{v_g}\right| = \left(1+\frac{1}{A_V}\right)\mu+\left(\frac{g_{mb}}{g_m}\right)\frac{\mu}{A_V}$$

But $(g_{mb}/g_m) < 1$

$$\left|\frac{v_d}{v_s}\right| < \left(1+\frac{2}{A_V}\right)\mu$$

For $A_V > 2000$, $\left|\frac{v_d}{v_s}\right|$ gives μ with an accuracy better than 0.1 %

Appendix 2.3

Listed below in Table.2.1 are data for μ as a function of I_D for two values of V_{DS} (1V and 2V), for V_{sub}=0V

Table A2.1 $\mu = f(I_D, V_{DS})$

ID(μA)	VDS(V)	μ	μ dB
1	1	34.82	30.84
	2	61.34	35.75
5	1	33.2	30.42
	2	58.88	35.4
10	1	32.9	30.18
	2	57.35	35.17
25	1	30.96	29.81
	2	54.84	34.78
50	1	29.81	29.49
	2	52.54	34.41
100	1	28.83	29.04
	2	49.58	33.91
250	1	25	27.96
	2	43.35	32.74
500	1	21.04	26.46
	2	35.6	31
750	1	18	25.11
	2	29.64	29.44
1000	1	15.5	23.8
	2	24.86	27.91

Appendix 2.4 Tabular data on (g_{mb}/g_m)

Table A2.2

	(g_{mb}/g_m)	(g_{mb}/g_m)
I_D(μA)	Vsub=0V	Vsub= -2V
1	0.178	0.137
5	0.169	0.135
10	0.165	0.134
25	0.159	0.133
50	0.155	0.132
100	0.151	0.131
250	0.147	0.131
500	0.145	0.131
1000	0.147	0.133

CHAPTER 3

DESIGN CONSIDERATIONS FOR BASIC SUB-CIRCUITS

3.1 Introduction

The current mirror, in its basic form or in a variant of it, together with the source-follower are basic sub-circuits in CMOS analogue design. A glance at the literature shows that they certainly feature widely in existing V-I designs.

Conventional textbook treatments deal with the analysis of both types of circuit using MOSFETs with channel lengths greater than about 1μm.

This chapter includes simulated measurements made to assess, for future use and reference, the performance of a number of types of current mirror and the performance of the source-follower incorporating MOSFETs with a channel length of 0.13 μm.

3.1(a) The simple current mirror (CM)

The simple of 1:1 current mirror, comprising two MOSFETs with

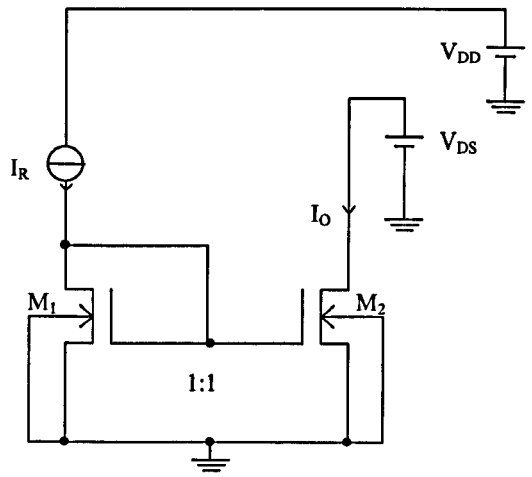
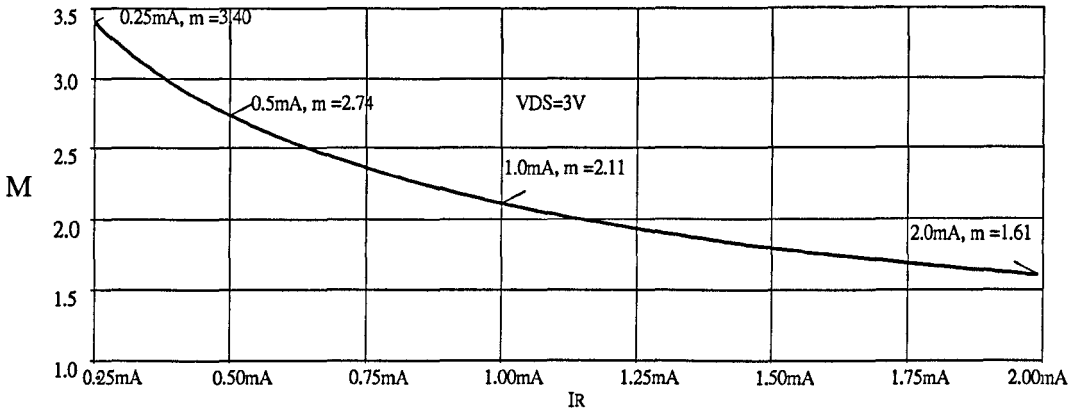


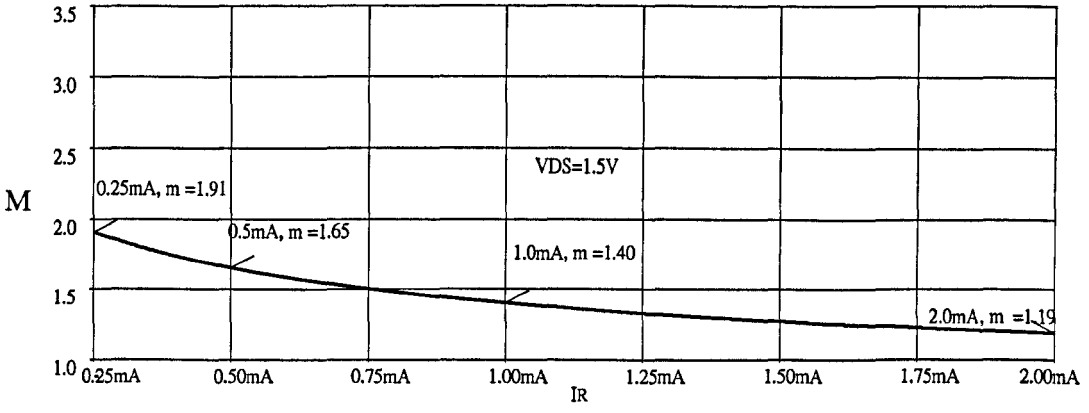
Figure 3.1 Simple (1:1) Current Mirror

identical characteristics, driven by an input reference current I_R (See Fig.3.1) has been touched-on in Chapter 2 in the discussion on MOSFET output characteristics (See Section2.2.3) where it was established that incremental output resistance in the

'current saturation' region, for the devices under test, was small, 2KΩ (approx.) for I_R=1mA. This makes the CM of extremely limited use if the output circuit of M_2 is to approximate a good, predicable current sink. The poor performance of the circuit of Fig.3.1 is clearly evident from Fig.3.2 which shows the DC current transfer ratio M(=I_O/I_R) as a function of I_R for two values of V_{DS}.



(a)



(b)

Figure 3.2 DC current transfer ratio M for Fig 3.1, as a function of I_R and V_{DS} (a) for V_{DS}=3V; (b) V_{DS}=1.5V

For a 1: x (>1) CM, in which L is the same for M_1 and M_2 but W for M_2 is a factor x greater than that of M_1, additional measurements (not included here) for x = 2 show, as expected, that for a given I_R and V_{DS}, I_D and g_{ds} are both double the Figure for x=1.

The DC performance the PMOS 1:1 CM using MOSFETs with L=0.13μm and W=10μm is better because of the higher output resistance obtainable with these devices.

It has been assumed above that the characteristics of M_1 and M_2 are identical. Simulations of current mirrors automatically assume this unless provisions are made for them to be different.

In practice, of course, doping and lithographic variations mean that even with the same V_{DS} [3.1].

$$M = \frac{I_O}{I_R} = 1 \pm \frac{\Delta\beta}{\beta} \pm \frac{2\Delta V_T}{(V_{GS} - V_T)} \tag{3.1}$$

where $\Delta\beta/\beta$ is the fractional variation in β and ΔV_T is the Threshold Voltage difference. Eqn.3.1 suggests closer matching for higher V_{GS}, i.e. higher I_D.

By simple inspection the input impedance of a 1:1 CM is,

$$Z_i = \frac{1}{(g_{ds} + g_m) + (2C_{gs} + C_{ds} + C_{gd})s} \tag{3.2}$$

Fig.2.2.5(c) in the previous Chapter shows $|Z_i|$ vs. f for I_D =1mA and V_{DS} = 1V

A straightforward small signal analysis shows that the current gain m (jω) = (i_o/i_r) has a pole at,

$$\omega_p = \frac{(g_m + g_{ds})}{(2C_{gs} + C_{db} + C_{gd})} \tag{3.3}$$

There is also a zero at,

$$\omega_z = \frac{g_m}{C_{gd}} \tag{3.4}$$

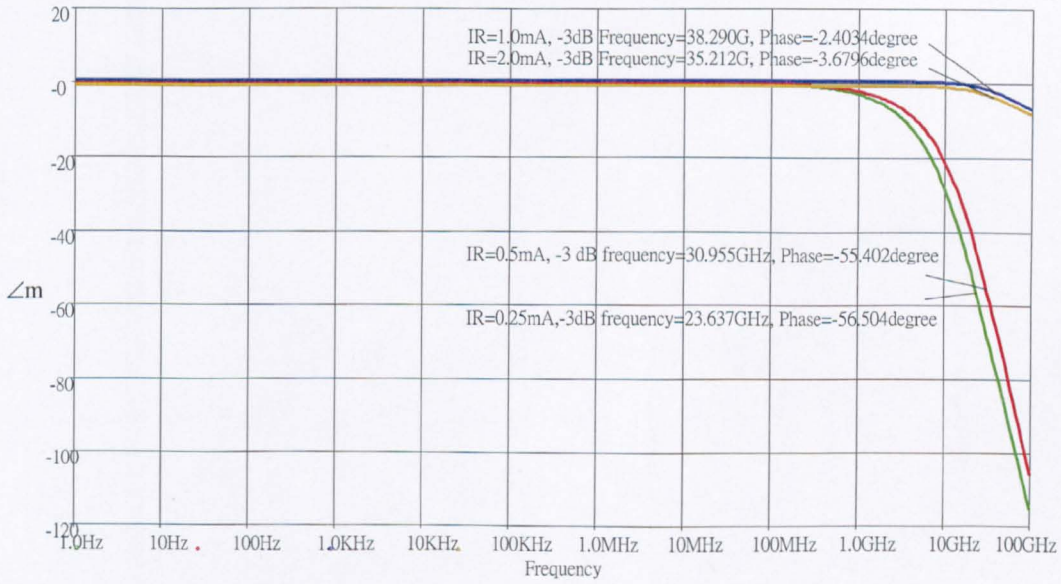
This zero is not mentioned in [3.1], presumably because $\omega_z >> \omega_p$

A plot of m(jω) for the circuit of Fig.3.1 is given in Fig.3.3

Surprisingly, the output impedance (as compared with the output resistance) is not treated in generally available textbooks. A full treatment is given in Appendix3.1

where it is shown that the expression for Z_o contains a zero in addition to two poles. Representing the output by the parallel combination of a resistor and a capacitor is, thus, not generally valid.

(a)



(b)

Figure 3.3 Current transfer ratio 'm' as a function of frequency for Fig 3.1. V_{DS}=1.5V. (a) Magnitude (b) Phase

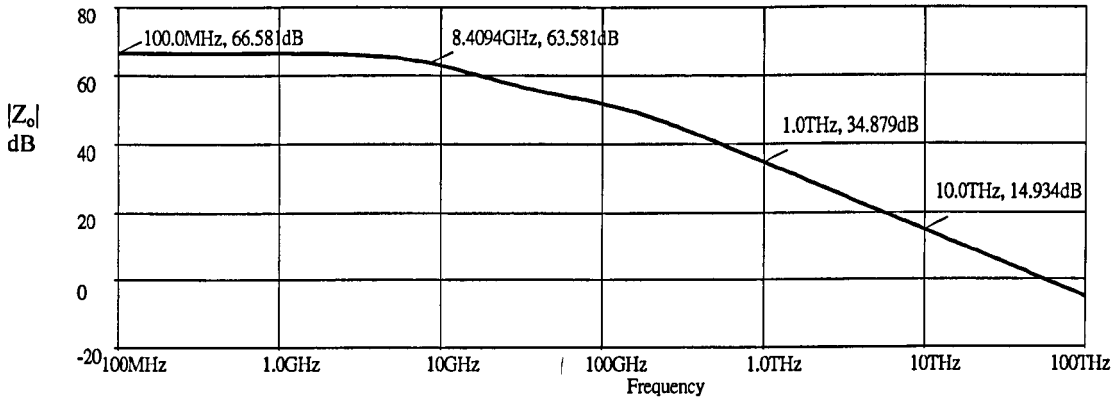


Figure 3.4 |Zo| for Fig 3.1. Reference resistance = 1Ω, here and elsewhere

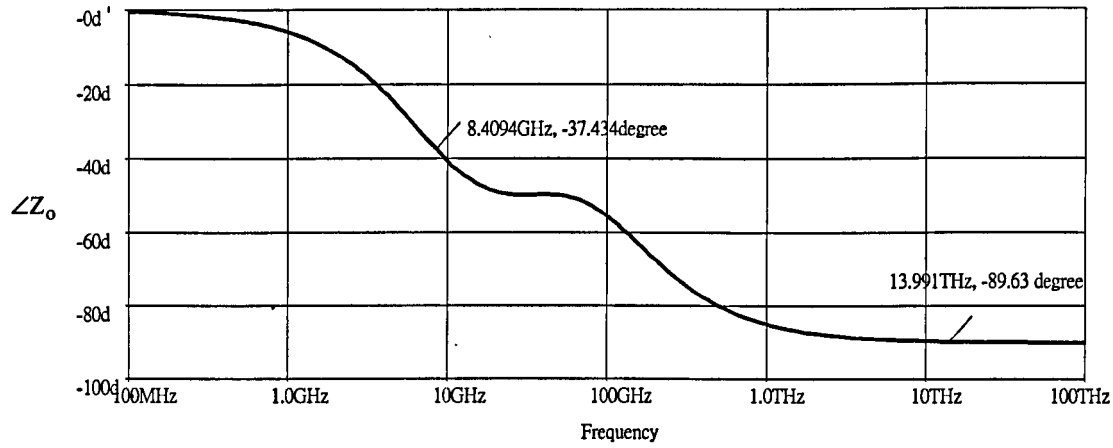


Figure 3.5 $\angle Z_o$ for Fig 3.1

Figs3.4, 3.5 respectively show $|Z_o|$ vs. f and $\angle Z_o$ vs. f.

From the analysis, a predicted value for -3dB frequency is 7.6GHz.

In Fig.3.4 the -3dB point for $|Z_o|$ is at the higher value of 8.4 GHz. The difference can be accounted for by a zero at a lower frequency.

This shows itself more clearly in the flattened phase characteristic (Fig.3.5) between 10GHz and 100GHz. This causes a fall-off in $|Z_o|$ by less than 20dB/decade and results in a higher -3dB point for $|Z_o|$. The final fall-off rate of 20dB/decade is as predicted.

3.1(b) The Widlar CM

The purpose of the Widlar CM, shown in Fig.3.6, in which M_1 and M_2 are assumed to have identical characteristics, is to produce an output current Io that is a fraction, usually small, of the input current I_R. This is set by choice of the source degeneration resistor R_S.

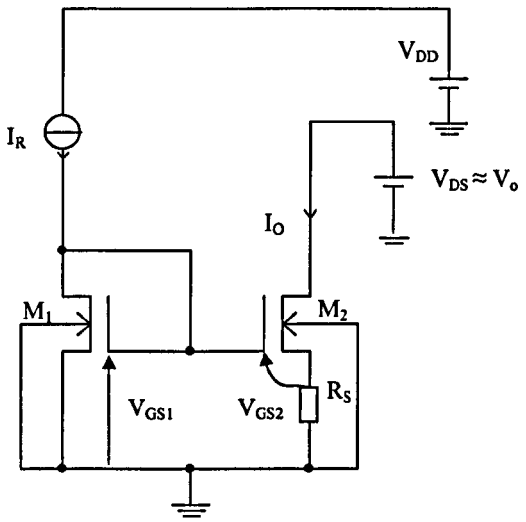


Figure 3.6 The Widlar CM

Assuming a simple square-law relationship between I_D and V_{GS}, and ignoring differences in V_{DS} between M_1 and M_2 and threshold voltage differences.

$$V_{GS1} = \sqrt{\frac{2\beta}{I_R}} + V_T \tag{3.5}$$

and, $$V_{GS2} = \sqrt{\frac{2\beta}{I_O}} + V_T \tag{3.6}$$

Hence, $$R_S = \frac{(V_{GS1} - V_{GS2})}{I_O} = \frac{\sqrt{2\beta}}{I_O}\left[\frac{1}{\sqrt{I_R}} - \frac{1}{\sqrt{I_O}}\right] \tag{3.7}$$

Given I_O, R_S can be chosen for a given I_R and known β.

The V_{SB} of M_2 can be allowed for, in an iterative design process, as can the non-identical V_{DS} of M_1 and M_2.

However, the graphical approach proposed here and shown in Fig.3.7 is simpler in practice.

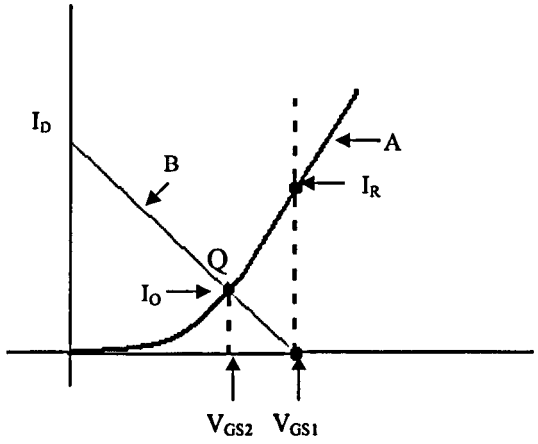
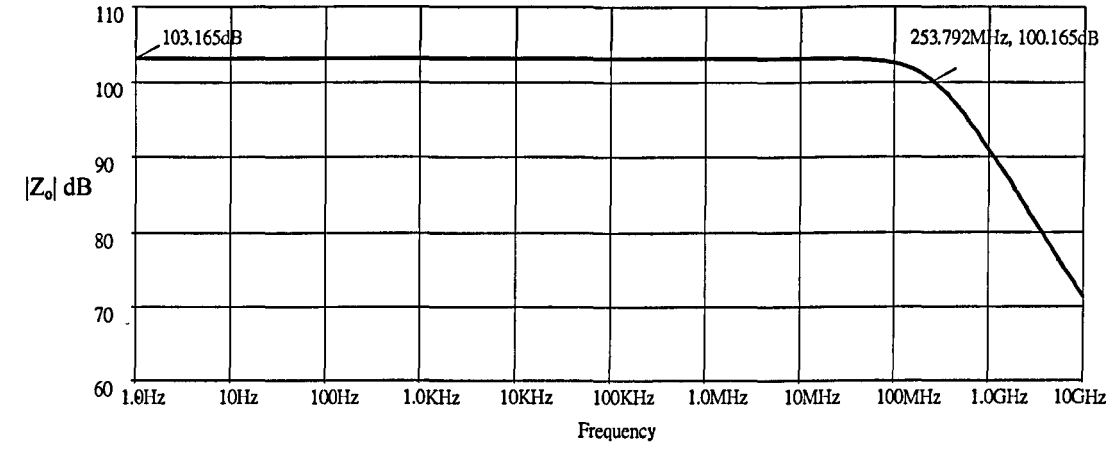


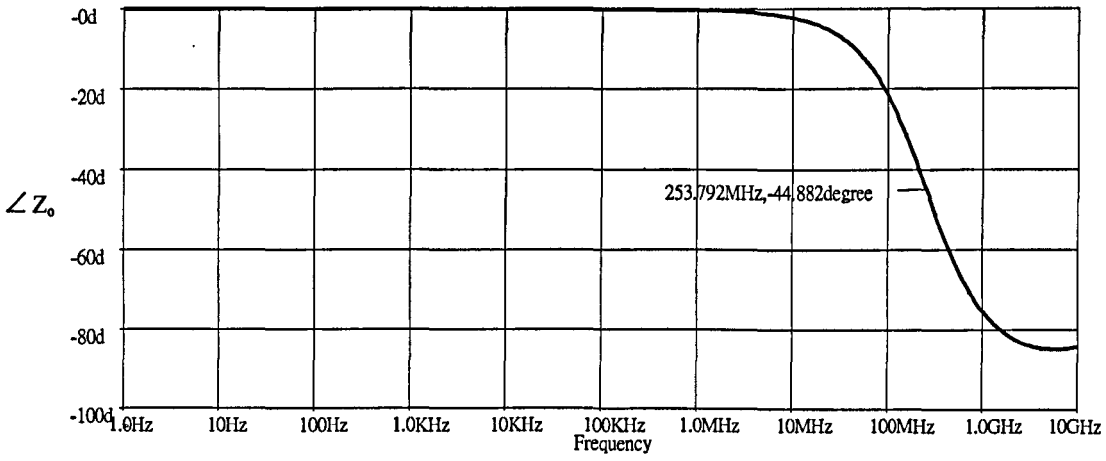
Figure 3.7 Graphical construction to find R_S for a specified I_O

Curve 'A' represents the I_D vs. V_{GS} characteristic for both M_1 and M_2. V_{GS1} and V_{GS2} correspond, respectively, to $I_D = I_R$ and $I_D = I_O$ (at the point Q). Line B, passing through Q, has a slope $-1/R_S$: hence, R_S can be determined.

Using this approach R_S was found to be 4KΩ for a specified value of I_O of 50μA (approx.) with I_R =1mA and V_{DS} = 1.0 V. The simulated value of 51.34μA is slightly higher than the specified value because of the V_{DS} of M_2 exceeds that of M_1. (i.e., $V_O > V_{GS}$).



(a)



(b)

Figure 3.8 Output characteristics of the Widlar CM: (a) $|Z_o|$ (b) $\angle Z_o$

Fig 3.8 shows variation of output impedance, Z_o, with frequency. Over its 'constant' region $|Z_o| = R_o = 103.165$dB (for a dB reference value of 1Ω), corresponding to an incremental output resistance of 144KΩ.

As in the case of a simple CM, a general expression for Z_o, in terms of the frequency variable s, in complex.

However, because of the large Ohmic value of R_o, there is a dominant pole at the output, for it is an apparent that the roll-off occurs at a rate of -20dB/decade (approx.) up to 10GHz.

The -3dB cut off frequency ($1/2\pi R_oC_o$) is 273.5 MHz, indicating an output capacitance of 4fF that corresponds precisely with the already determined 4fF output capacitance of M_2.

The current fed back via C_{gd} from the drain of M_2 to its gate is not mirrored by M_2 because of the presence of R_S in its source lead.

3.2 Multiple transistor CMs

The observed limitations of the simple CM, using MOSFETs with channel lengths of 0.13μm, with respect to source/sink/repeater operation make it necessary to employ multiple transistor CMs for predictability in DC current transfer ratio, M, and increased incremental output resistance.

Those popular choices are: the Cascode CM (CCM), Fig.3.9; the Modified Wilson CM (MWCM), Fig.3.10; and the so-called High Output Compliance CM (HCCM), Fig.3.11.

3.2.1 DC Characteristics

The DC and incremental performance of these are compared in this section, with a view to their application in V-I design, starting with the DC characteristics in Figs3.12, 3.13, 3.14.

For the CCM and MWCM the gate of M_3 is held at ($V_{T4}+V_{T3}+2V_{on}$),

where $V_{on} = (V_{GS} - V_T) = \sqrt{2I_R/\beta}$ and is the minimum V_{DS} for operation in the current saturation region. Hence $V_o(min)=V_{T4}+V_{T3}+2V_{on}-V_{T3}=V_T+2V_{on}$. The interesting conclusion is that $V_o(min)$ is the same as it would be if the substrate of M_1, M_3 were connected to their respective sources. In the case of the WCM, $I_O=0$ for $V_I <$ ($V_{T3}+V_T$).

The HCCM uses six MOSFETs to obtain the theoretical value $V_o(min) \approx 2V_{on}$. Working back from the gate of M_3, the nodal voltage labelling shows that that this is achievable if all the MOSFETs expect M_1 have identical characteristic with a common beta parameter 'β' and common threshold voltage, V_T.

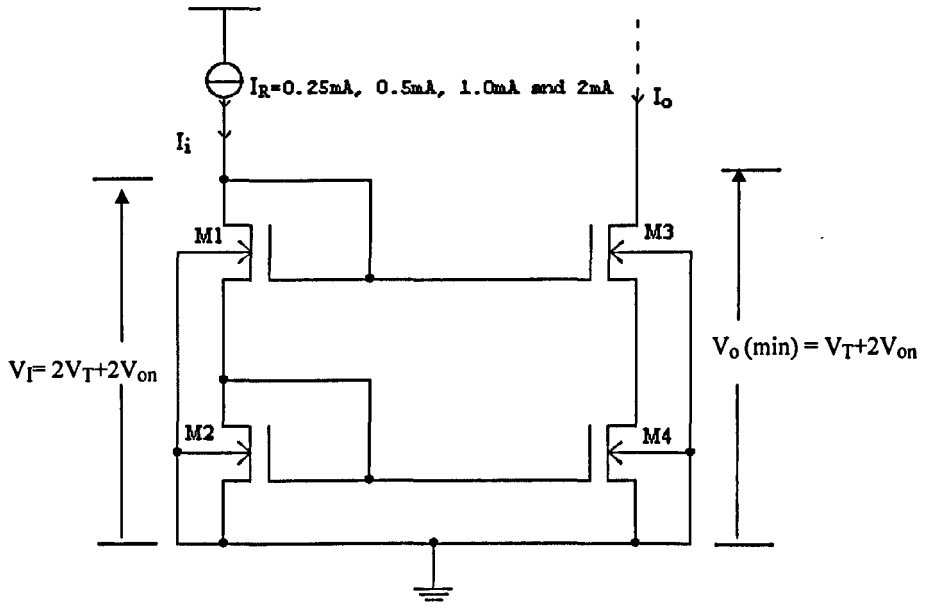


Figure 3.9 The Cascode CM (CCM): V_{on} is defined on p 3.10

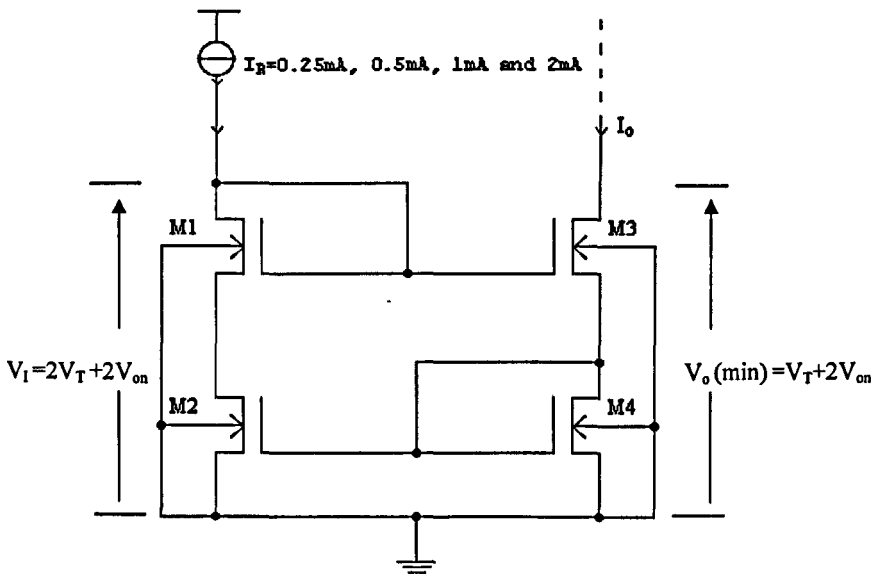


Figure 3.10 The Modified Wilson CM (MWCM)

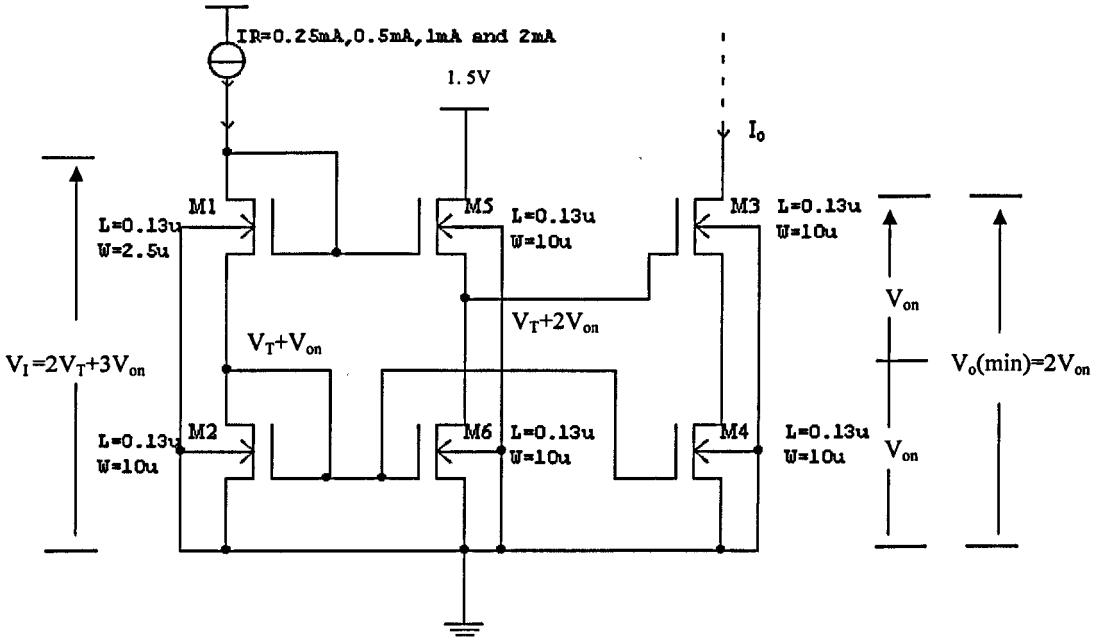


Figure 3.11 'High Output Compliance' CM (HCCM): Theoretical Design

M_1 must have the same V_T as all the other MOSFETs but a beta parameter β_4: $\beta_4 \neq \beta$ because we require the V_{on} of M_1 to be twice the common value of the other devices.

Thus, $$\sqrt{\frac{2I_R}{\beta_4}} = 2\sqrt{\frac{2I_R}{\beta}} \qquad (3.8)$$

Hence, $\beta_4 = \beta/4$. This happens if, for a common channel length, the gate width if M_1 is one-quarter of the other transistors, i.e., 2.5μ in the present design.

The theoretical performance of the HCCM is not borne out in practice. The higher than expected $V_o(min)$ can be attributed to the fact that the drain current of M_6 exceeds I_R, because its drain voltage is greater than that of M_2 by V_{on}, and thus the gate-source voltage of M_5 exceeds the theoretical value ($V_T + \sqrt{2I_R/\beta}$).

In the current saturation region, the design figure of unity for the DC current transfer ratio is closely met by the CCM and MWCM but not so well with HCCM. This is attributed to the unequal drain voltages of M_2 and M_4.

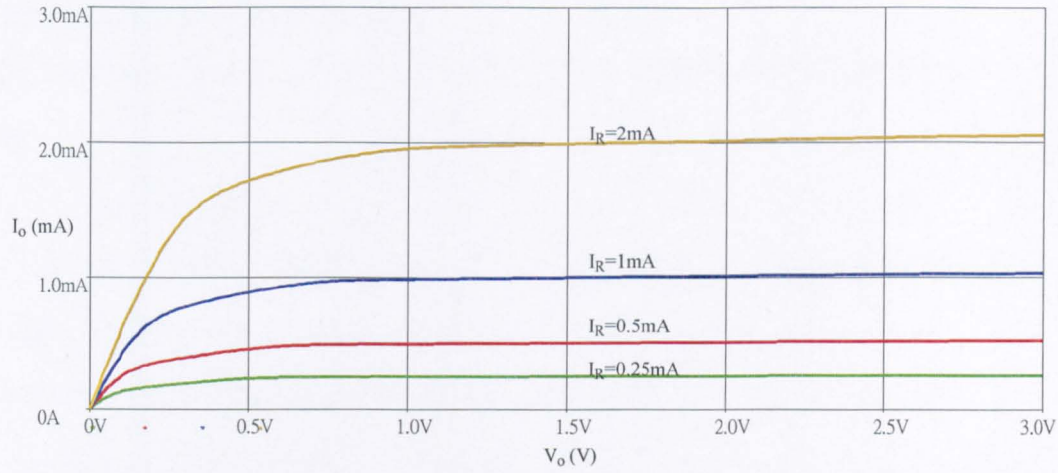


Figure 3.12 DC output characteristics of the CCM

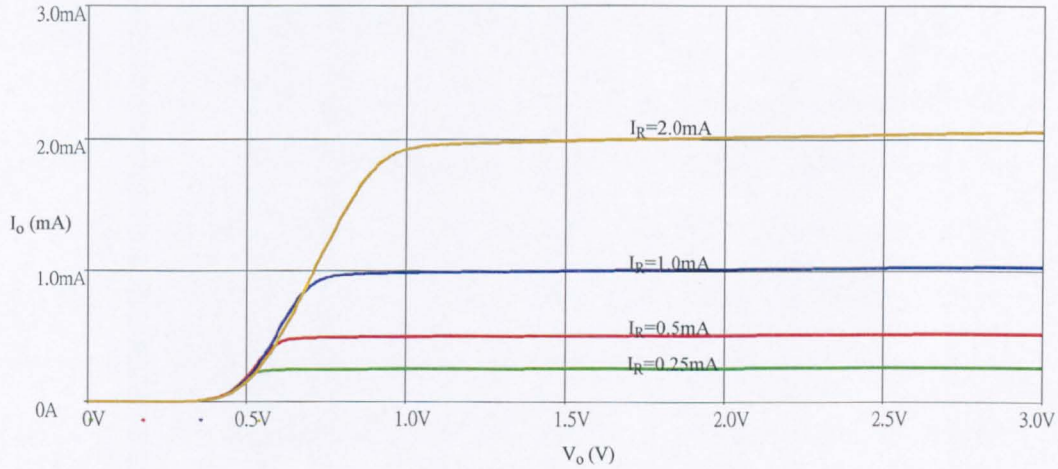


Figure 3.13 DC output characteristics of the MWCM

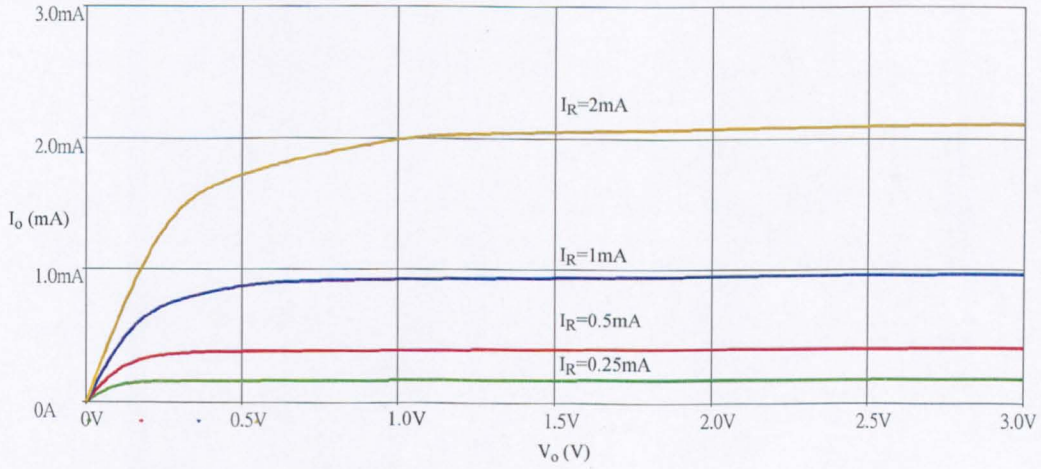


Figure 3.14 DC output characteristics of the HCCM

3.2.2 Incremental performance

The incremental output resistances of the these circuits should all be similar and given by,

$$R_o \cong \mu(1+\chi)r_{ds} \qquad (3.9)$$

Substituting simulated data, this gives $R_o \approx 37.6K\Omega$ for the CCM compared with a value of $38K\Omega$ (91.597dB with respect to a reference value of 1Ω) in Fig.3.15(a) The values for the MWCM and HCCM are, respectively, $35.76K\Omega$ and $41.02K\Omega$.

In all of these circuits the input drive current was supplied by an ideal current source for test proposes. The use, in practice, of a non-ideal current source does not affect the output resistance of the CCM and HCCM but it does have a major effect on the MWCM because the drive current is in the feedback loop. Thus, suppose the resistance of the current drive circuit is r_{ds}, i.e., the same as the output resistance of a simple CM. Then the loop-gain magnitude, |LG|, in the MWCM is reduced by 50% and, with it, the output resistance because it is given by (Output resistance without feedback $\times$|LG|). The drive current output resistance could be increased by making it that of a p-channel Wilson configuration but that is at the expense of greater circuit complexity.

The input impedances for the CCM, MWCM and HCCM shown for comparison, respectively, in Figs3.14, 3.15, 3.16 all display a fall-off in $|Z_o|$ of approximately 20dB/decade between 100MHz and 10GHz, indicating that, to a first approximation, they can be modelled by a resistance in parallel with a capacitance. However, because of the different values of $|Z_o|$ at low frequencies, they exhibit differing cut-off frequencies. The effective output capacitances calculated from them are 9.84fF, 10fF, 5.17fF for, respectively, the CCM, MWCM and HCCM. Those for the CCM and MWCM are comparable with a figure of 8.16fF obtained by substituting parameter data into the expression for output capacitance derived in Appendix3.1

$$C_o \approx \frac{2C_{gs}}{(1+\mu)} + 2C_{gd} + C_{db} \qquad (3.10)$$

The output capacitance for the HCCM is somewhat higher than the 4fF expected of a common-gate-output stage.

In this case the current in the C_{gs} of the output MOSFET is not magnified by current-mirror action as it is for the CCM and MWCM.

The frequency response of the small-signal current gain magnitude, |m|, is shown in Figs3.18, 3.19, 3.20 for the three types of CM under review.

A simplified equivalent circuit for the calculation the incremental short-circuit value of |m| for the CCM is shown in Fig.3.21

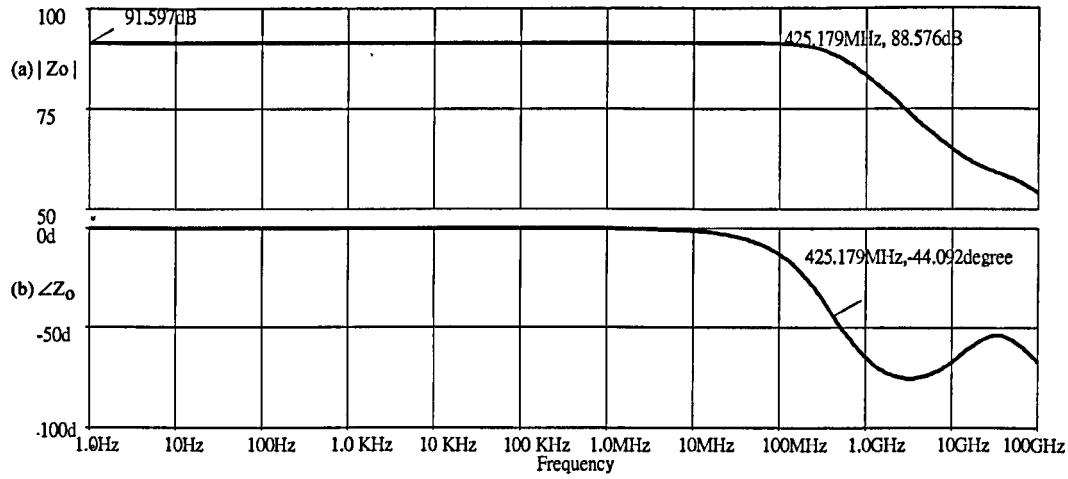


Figure 3.15 Zo in (a) dB and (b) phase of the CCM: V_o=1.5V; I_R=1mA

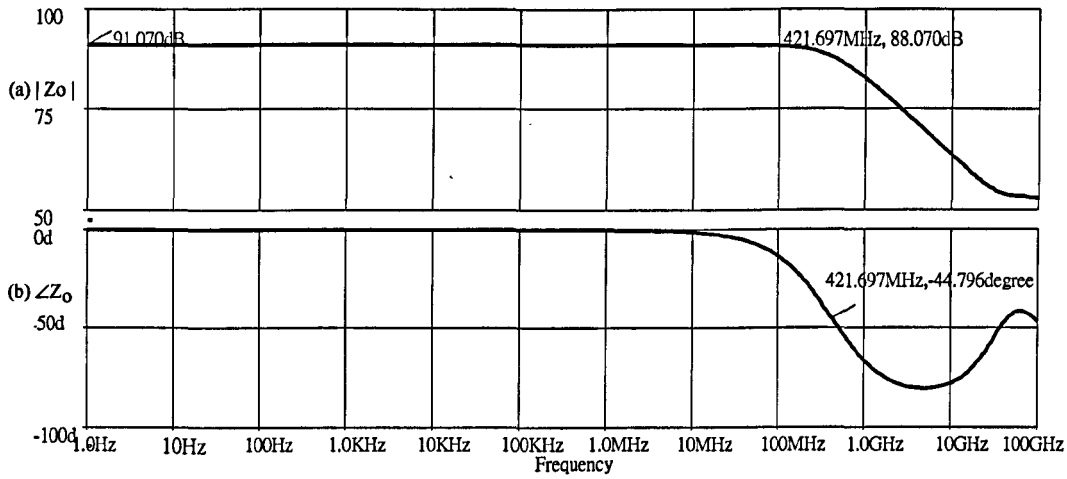


Figure 3.16 Zo in (a) dB and (b) phase of the MWCM: V_o=1.5V; I_R=1mA

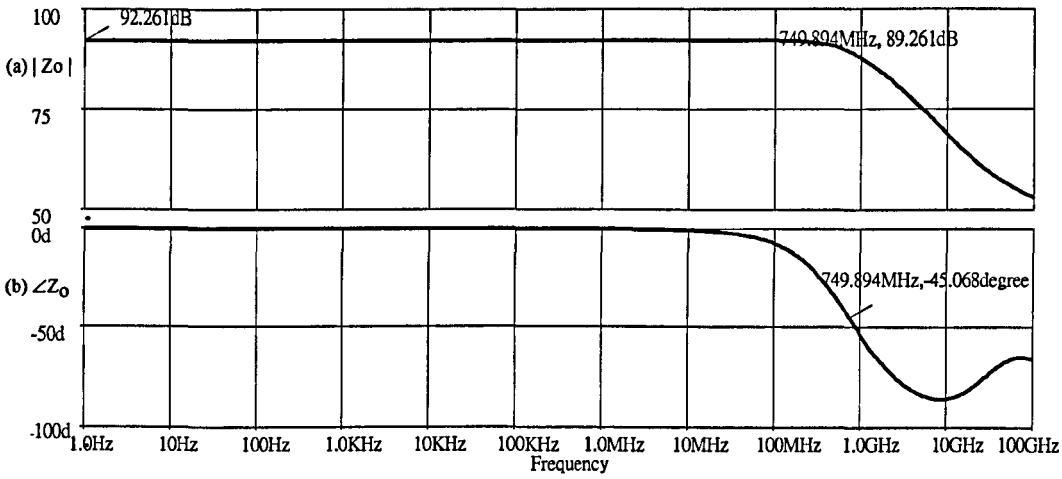


Figure 3.17 Zo in (a) dB and (b) phase of the HCCM: V_o=1.5V; I_R=1mA

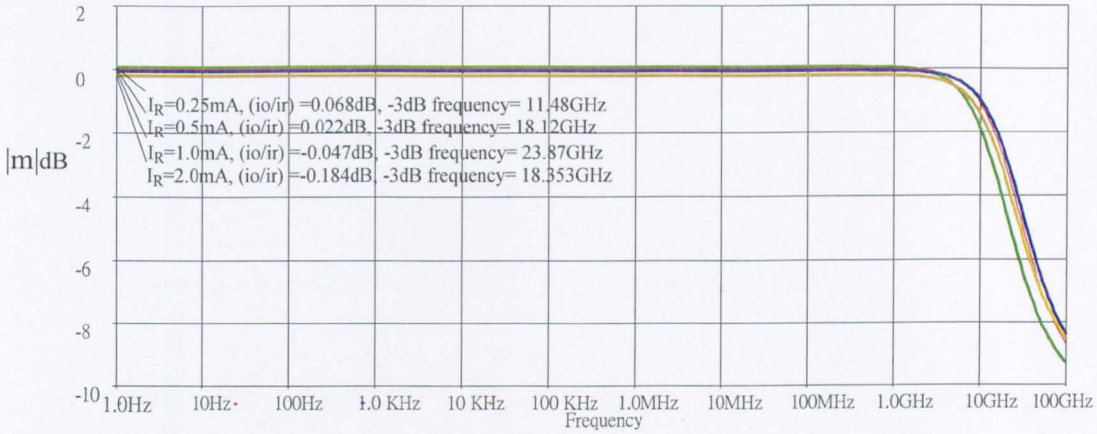


Figure 3.18 Current gain magnitude vs. frequency for the CCM

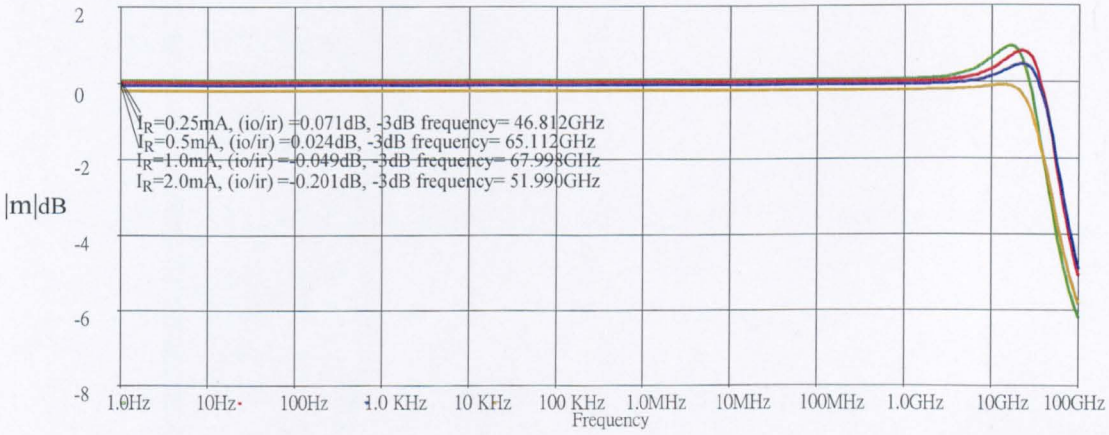


Figure 3.19 Current gain magnitude vs. frequency for the MWCM

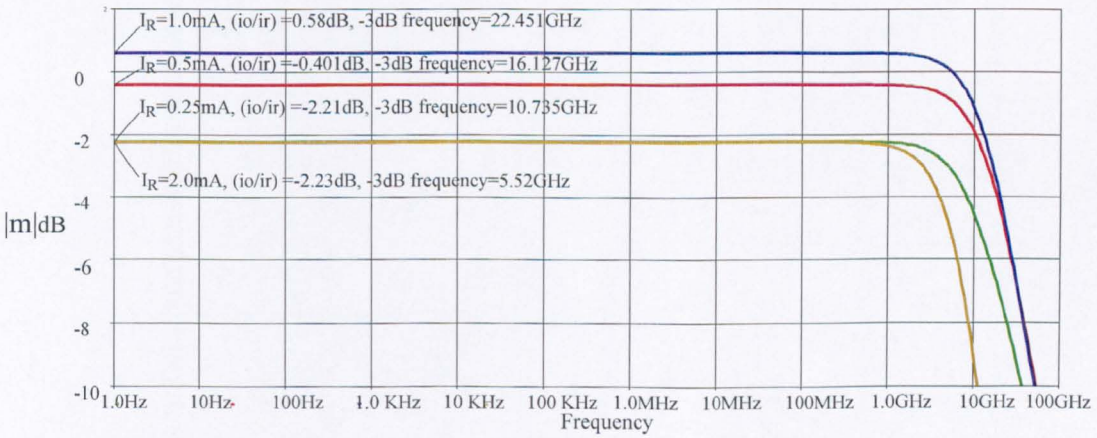


Figure 3.20 Current gain magnitude vs. frequency for the HCC

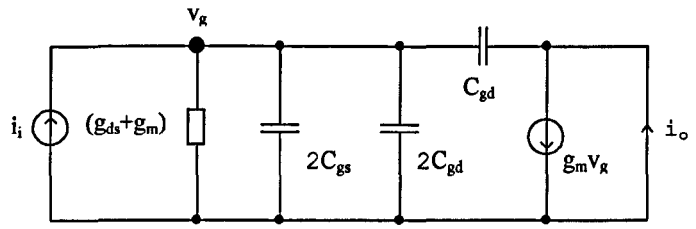


Figure 3.21 Circuit for finding $|m| = i_o/i_i$ for the CCM

This resembles the circuit for the simple 1:1 CM but, in this case, the capacitance in parallel with $2C_{gs}$, in the input, is $2C_{gd}$ instead of C_{gd} because of 'Miller magnification' of the C_{gd} of M_4 in Fig.3.9

The -3dB cut-off frequency is given by,

$$f \cong \frac{(g_m + g_{ds})}{2\pi(2C_{gs} + 3C_{gd} + C_{db})} \qquad (3.11)$$

Substituting measured capacitance values, $(2C_{gs}+3C_{gd}+C_{db})$ =39fF and for operation at 1mA, $1/(g_{ds}+g_m) = 157\ \Omega$.

Hence, $f \approx 25.6$GHz (3.12)

This value of f is in fair agreement with the observed value of 23.87GHz.

In the case of the HCCM the -3dB cut-off frequency is somewhat lower, at 22.4GHz, because the gate terminals of three MOSFETs are connected together rather than two.

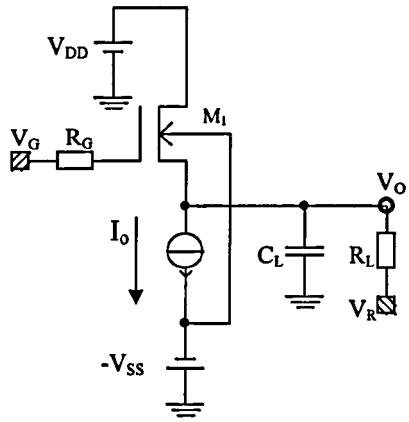
For the MWCM there is peaking in the frequency response of |m|, for some values of I_D: this would be attributed to complex poles in the expression for loop-gain. This was not investigated further, for reasons given in the concluding section of this chapter.

3.3 Source-Follower

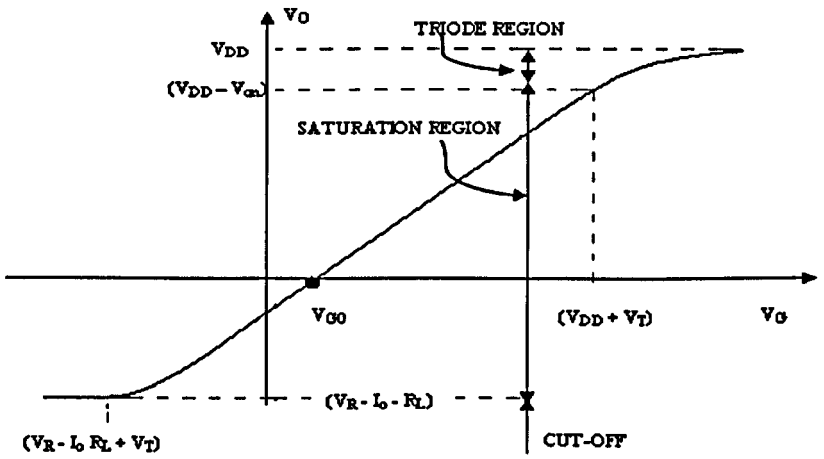
In this section the simulated performance of the source-follower under anticipated operating conditions is examined to see what simplifications, if any, can be made in modelling it for use in calculations for an initial paper design of V-I circuits incorporating it.

3.3.1 DC characteristic

In the generalised N channel source-follower circuit of Fig.3.22(a), the load resistor R_L is connected to a chosen reference voltage, V_R (>-V_{SS})



(a)



(b)

Figure 3.22 (a) A generalised source-follower configuration
(b) DC voltage transfer characteristic of (a)

Assuming a square-law mutual characteristic for M_1, i.e., operation in the saturation region, we can write,

$$I_O = \frac{\beta}{2}(V_{GS} - V_T)^2[1 + \lambda(V_{DD} - V_O)] \tag{3.13}$$

But, $V_{GS} = (V_G - V_O)$ and, from [3.2],

and, $$V_T = V_{T0} + \gamma\left[\sqrt{2\varphi_F + (V_{SS} + V_O)} - \sqrt{2\varphi_F}\right] \tag{3.14}$$

Substitution in eqn.3.13 and the subsequent re-arrangement of terms gives,

$$V_G = V_O + V_{T0} + \gamma\left(\sqrt{2\varphi_F + V_{SS} + V_O} - \sqrt{2\varphi_F}\right) + \sqrt{\frac{2\left[I_O + \frac{(V_O - V_R)}{R_L}\right]}{[1 + \lambda(V_{DD} - V_O)]\cdot\beta}} \tag{3.15}$$

This equation determines points on the DC transfer characteristic shown in Fig.3.22(a).

In particular, the point V_{GO} at which the characteristic crosses the horizontal axis is found by substituting V_O=0 in eqn 3.15. This equation shows, also, that the slope (dV_O/dV_G) is not constant but dependent on V_O.

DC simulations were made on the circuit of Fig.3.23(a) for $V_{DD} = V_{SS} = 1.5V$ and two conditions of source loading.

In the first condition tests $R_L = \infty$ and I_O was set, successively, at 0.5mA, 1mA and 1.5mA, obtained from an ideal current sink. This was to find the 'best' transfer characteristic. Of course, ideal current sinks do not exist in practice but can be approximated using current generators with cascoded output stages.

In the second set of simulations I_O=0, V_R=-V_{SS} and R_L was set, successively, at 1KΩ, 2KΩ, 4KΩ, values likely to be used in a practical design.

Results of the first set of simulation tests are shown in Fig 3.23. Included on the plot, for reference purposes, is the ideal curve for any type of follower circuit

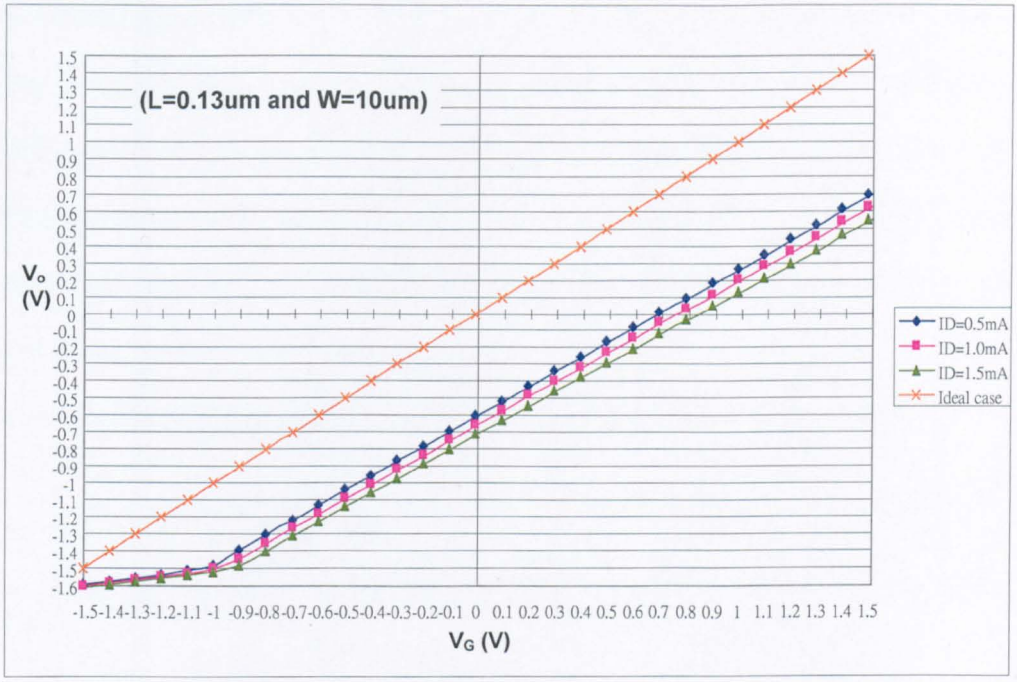


Figure 3.23 DC transfer characteristics for circuit of Fig 3.22(a) with $R_L=\infty$, $V_{DD}=V_{SS}=1.5V$

viz., a straight line through the origin with a slope of unity.

The point $V_G = V_{G0}$ for I_O=1mA appears to be mid-way between that for 0.5mA and that for 1.5mA, and that could be a useful approximation, but it does not quite agree with what is predicted from eqn.3.16, the last term of which controls the variation of V_{G0} with I_O.

This term can be written in the form $x = S\sqrt{I}$ where $S \underset{\equiv}{\Delta} 1/\sqrt{(1+\lambda V_{DD})\beta}$

Using subscripts 1, 2, 3 to represent conditions for 0.5mA, 1mA, 1.5mA, respectively, then,

$$(x_2 - x_1) = S(1 - \sqrt{0.5}) = 0.291S \qquad (3.16a)$$

and, $$(x_3 - x_2) = S(\sqrt{0.5} - 1) = 0.224S \qquad (3.16b)$$

Obviously, $(x_2-x_1) > (x_3-x_2)$ (3.17)

A straight-edge, applied to each of the curves in Fig.3.23 indicates that, to a good approximation, they may be considered linear, though with a slope noticeably different from unity. The apparent linearity could be regarded as surprising in view of the dependence of the slope on V_O. However, it is understable if we consider a small signal representation of low-frequency voltage gain and the variation of the model parameters with DC conditions.

In saturation, with I_D = constant = I_O, it is shown in Appendix3.2 that, for $R_L=\infty$,

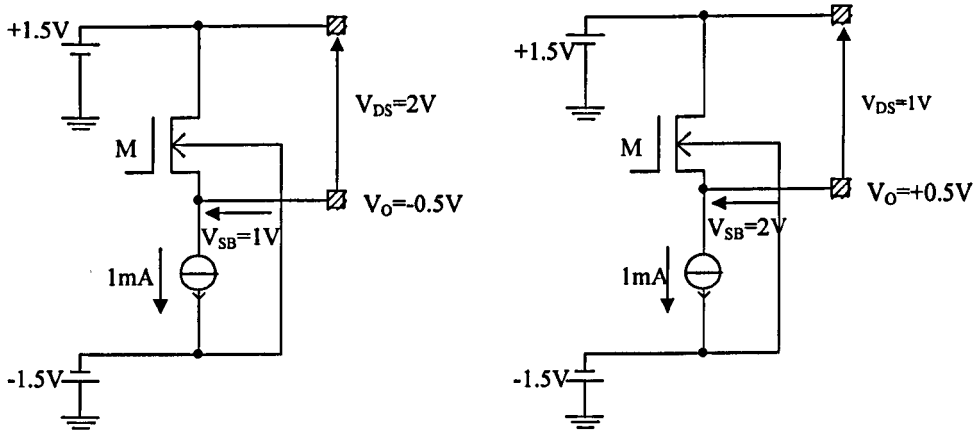
$$A = \frac{v_o}{v_g} = \frac{g_m}{g_m + g_{mb} + g_{ds}} \tag{3.18}$$

In terms of the symbols μ, χ defined in Chapter 2, we can re-cast this equation in the form,

$$A = \frac{\mu}{1 + \mu[1 + \chi]} \tag{3.19}$$

We can now estimate the variability of A with the input voltage V_G by calculating it for (say) two well-separated output voltages.

A convenient pair of points is V_O=-0.5V and V_O=+0.5V, because we already have data for μ and χ that is applicable to these.



μ = 24.86
χ =0.14
A =0.847
(a)

μ=15.5
χ =0.133
A =0.835
(b)

Figure 3.24 Determination of A for two circuit conditions
(a) V_O=-0.5V (b) V_O=+0.5V

Fig.3.24 shows values of μ, χ (from Appendices2.3, 2.4) obtaining for (a) V_O=-0.5V and (b) V_O=+0.5V and the respective values of A calculated from eqn.3.19.

These results show that there is a little variation in A over the input voltage range considered. Some of this is due to the opposite effects on V_O of V_{SB} and V_{DS}.

The temperature dependence of V_T [3.3], normally in the range -0.5mV/°C and -4mV/°C, together with the decrease in β (due to mobility decrease) with temperature causes a change in V_O for a given V_G. Fig.3.25 indicates that $|dV_O/dT| <$ 100mV/125°C i.e., < 1mV/°C.

Before leaving the case of an ideal current sink as a load, a test was made with V_{SB}=0. The transfer characteristic (Fig.3.26) now has a slope close to unity because g_{mb}=0. Hence, χ = 0 and eqn.3.19 becomes,

$$A = \frac{\mu}{(1+\mu)} \qquad (3.20)$$

Fig.3.25 shows simulation results for a second series of tests in which the source load is a resistor, R_L, see Fig 3.22 (a).

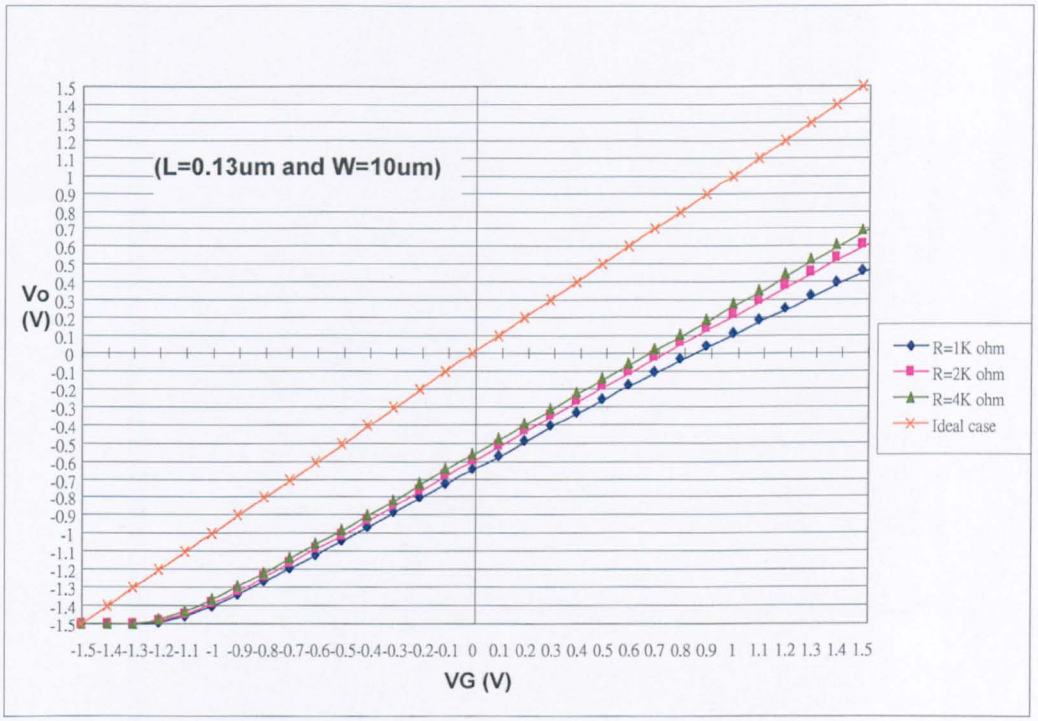


Figure 3.25 Source-Follower transfer characteristic for varying resistive loads

The equation for a particular value of R_L is, from eqn.3.15,

$$V_O = V_G - V_{T0} - \gamma\left(\sqrt{2\varphi_F + V_{SS} + V_O} - \sqrt{2\varphi_F}\right) - \sqrt{\frac{2(V_O + V_{SS})}{\beta R_L\left[1 + \lambda(V_{DD}) - V_O\right]}} \qquad (3.21)$$

Thus, for a fixed V_G, V_O decreases as R_L decreases.

Figs.3.23 and 3.25 are combined on the same graph-sheet in Appendix3.3 to enable a direct comparison. This Appendix also shows the effect of temperature in the particular case of a 2KΩ load.

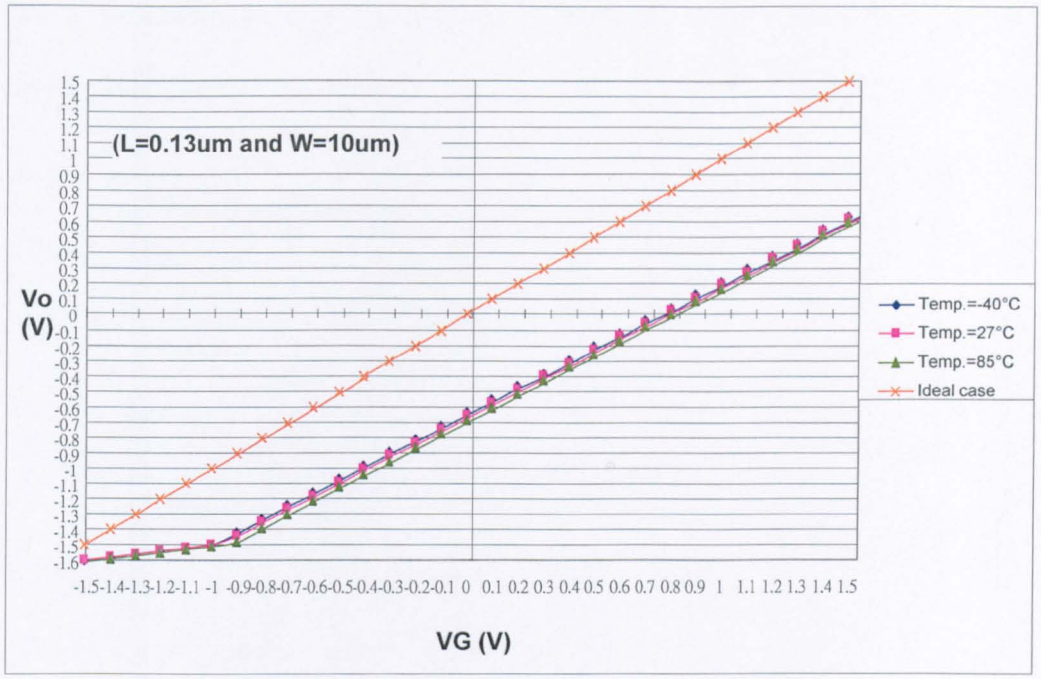


Figure 3.26 Temperature variation of Source-Follower transfer characteristic I_O=1mA

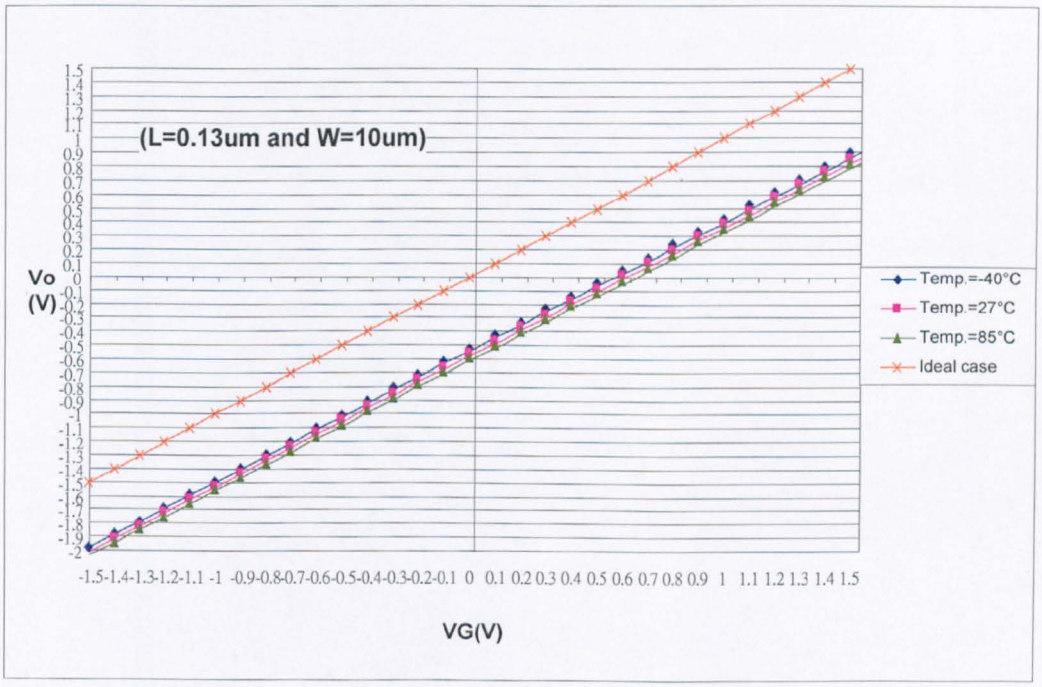


Figure 3.27 Temperature variation of Source-Follower transfer characteristic : I_O=1mA Substrate tied to source

The poor gain-magnitude and linearity in the case of a resistive load can be appreciated by modifying eqn.3.18.

Now, $$A = \frac{g_m}{(g_m + g_{mb}) + g_{ds} + g_L} \qquad (3.22)$$

where $g_L=1/R_L$

Equation 3.22 can be written in the form,

$$A = \frac{\mu}{1+\mu(1+\chi)+\left(\frac{r_{ds}}{R_L}\right)} \qquad (3.23)$$

With change in input voltage I_D and V_O change and so does r_{ds}.

The worst case (R_L=1KΩ) occurs for R_L comparable with r_{ds}.

3.3.2 Incremental performance

This section deals with the simulated incremental or small-signal performance of the circuit of Fig.3.22(a) and the way it relates to the theoretical analysis given in Appendix3.2.

In the simulations, the DC level of the gate voltage of the MOSFET under test was set at earth potential in all cases. For the measurement of voltage gain a small amplitude signal voltage of varying frequency was superimposed on this. In the case of the gain the resulting source voltage was measured and for the input impedance the gate current monitored. To measure the input impedance a small amplitude a.c current of varying frequency was applied to the source and the resulting source voltage measured.

Fig.3.28(a) shows the gain magnitude, |A|, and the phase, $\angle A$, as a function of frequency for the special case R_G=0 and two conditions of source load. The first source load is a 1KΩ resistor connected to $-V_{SS}$ (-1.5V): the second source load is

1KΩ resistor with a capacitor (C_L=50fF) connected from source to earth. The purpose of this second test is to assess the extent to which capacitive loading affects the frequency response. The choice of 50fF was made because it was thought to represent the maximum capacitive loading in a potential V-I design.

In the case of a resistive load,

$$A(s) = \frac{v_o}{v_g} = \frac{g_m + sC_{gs}}{(g_m + g_{mb} + g_{ds} + g_L) + sC_{gs}} \tag{3.24}$$

This has a low frequency gain A(o) given by,

$$A(o) = \frac{g_m}{(g_m + g_{mb} + g_{ds} + g_L)} \tag{3.25}$$

There is a zero at, $\omega_z = \frac{g_m}{C_{gs}}$ (3.26)

and a pole at, $\omega_p = \frac{g_m + g_{mb} + g_{ds} + g_L}{C_{gs}}$ (3.27)

Since $(g_m+g_{mb}+g_{ds}+g_L) > g_m$, the zero is at a lower frequency than the pole.

For $s \to \infty$ (i.e. $\omega \to \infty$), $A \to 1$

These predictions are borne out by in the green curve in Fig.3.28

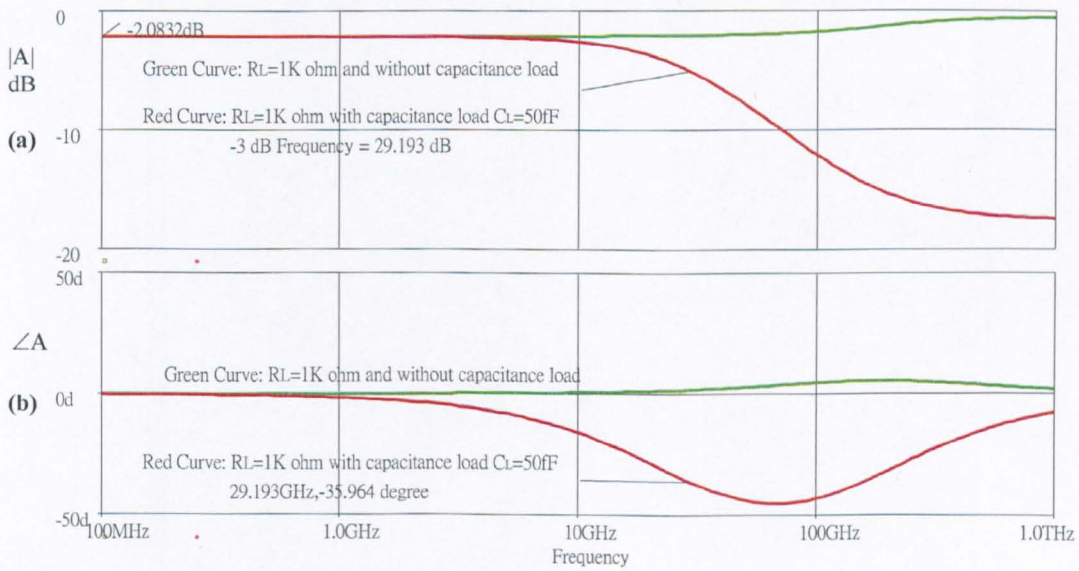


Figure 3.28 (a) Source-Follower gain magnitude |A|; (b) phase

The low value of R_L produces a poor value for |A(o)|.

In fact, $|A(o)|_{dB}$ = -2.0832dB, i.e. |A(o)| = 0.787.

For the case of capacitance loading,

$$A(s) = \frac{g_m + sC_{gs}}{(g_m + g_{mb} + g_{ds} + g_L) + s(C_{gs} + C_L)} \tag{3.28}$$

$$\omega_z = \frac{g_m}{C_{gs}} \tag{3.29}$$

and, $$\omega_p = \frac{(g_m + g_{mb} + g_{ds} + g_L)}{(C_L + C_{gs})} \tag{3.30}$$

or, $$\omega_p = \frac{g_m}{C_{gs}}\left[1 + \frac{(g_m + g_{mb} + g_{ds} + g_L)}{1 + \frac{C_L}{C_{gs}}}\right] \tag{3.31}$$

For $$\frac{C_L}{C_{gs}} > \frac{(g_m + g_{mb} + g_{ds} + g_L)}{g_m} \tag{3.32}$$

$$\omega_z > \omega_p \tag{3.33}$$

For $$\omega \to \infty, A \to \frac{C_L}{(C_{gs} + C_L)} \tag{3.34}$$

These results are applicable to the red curve in Fig.3.28(a).

It is apparent that the source-follower in useable up to a frequency of about 10GHz with a combined 1KΩ and 50fF load in parallel.

The input impedance shown in Fig.3.29 for the same two loading conditions as

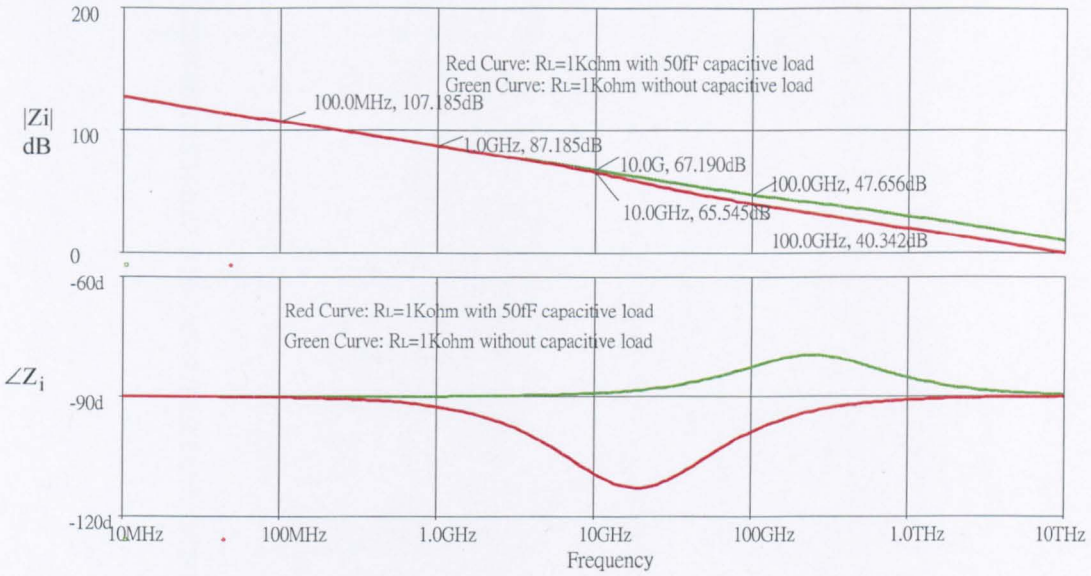


Figure 3.29 Input impedance of source follower for two loading conditions and R_G=0

discussed above.

From f =1GHz to f =10GHz the plot for |Zi| falls from 107.185dB to 87.185dB. This 20dB/decade fall shows that the input can be modelled by a single capacitor, for both values of loading, up to about 10GHz.

This bears out a prediction in Appendix3.2 where the bootstrapping effect on C_{gs} is mentioned.

Finally, the output impedance, Z_o, is shown in Fig.3.30, again for the special case R_G=0, considered.

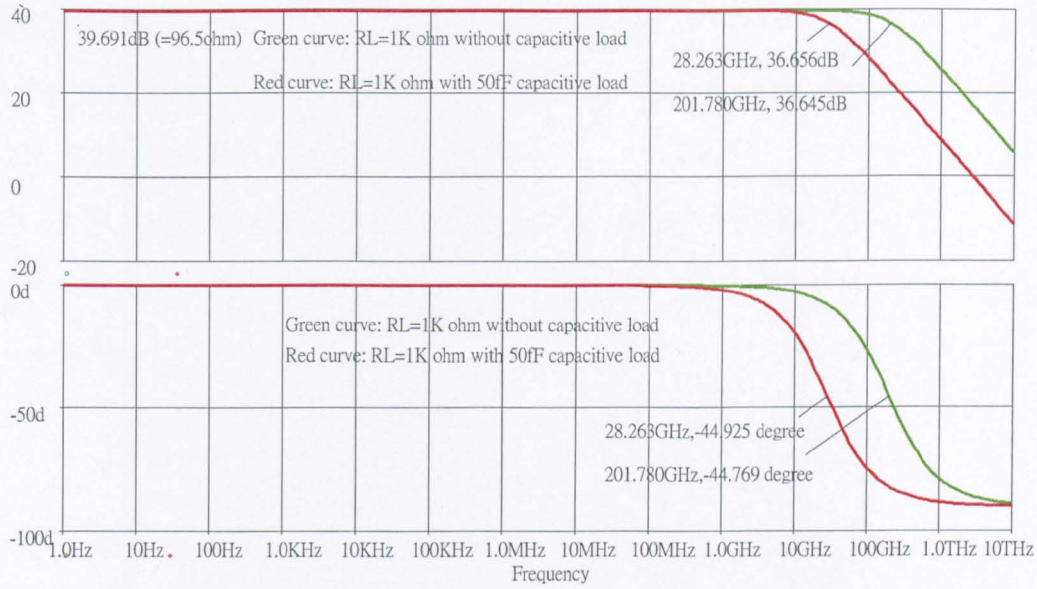


Figure 3.30 Source-follower output impedance: RG=0 (a) |Zo| :(b) $\angle Z_o$

Z_o follows the prediction of the simple formula

$$Z_O = \frac{1}{(g_m + g_{mb} + g_{ds} + g_L) + s(C_{gs} + C_L)} \qquad (3.35)$$

3.4 Summary and conclusions

Tests showed that the simple current mirror (CM) was very limited in its application potentialities because of its poor incremental output resistance. This could be improved by the use of more MOSFETs. Three schemes were investigated, the cascode (CCM) and the Modified Wilson CM (MWCM), both comprising four MOSFETs, and the so-called 'High Compliance CM' (HCCM) comprising six MOSFETs. It was decided to adopt the CCM in preference to the other two for a number of reasons. First it gave comparable small signal performance to that of the MWCM but had a major advantage over it, namely, that the output impedance was independent of the resistance of the circuit driving it. The HCCM had the best

frequency response but was not regarded as acceptable for two reasons. First, for a reason not discovered, its DC output characteristic was no better than that of the CCM or MWCM. Second, it requires six MOSFETs.

It does have one major advantage over the other two circuits in its bandwidth.

This suggests the use of the configuration shown in Fig.3.31 for best overall CM performance.

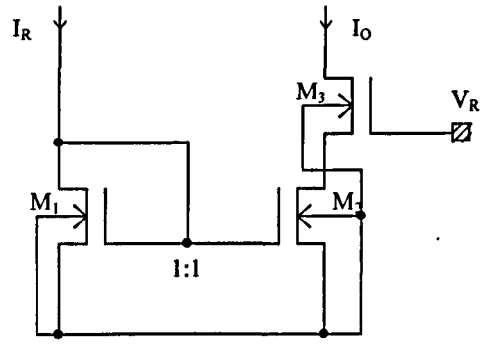


Figure 3.31 CM scheme for best overall output performance

In this, the gate bias voltage, V_R, for the cascode transistor M_3 in such that the drain voltage of M_2 is the same as that of M_1. As in the case of the HCCM the C_{gs} of M_3 does not feed current back to the input circuit.

Work on the source-follower showed the general desirability of using a constant current generator, for biasing purposes, to achieve the maximum low-frequency voltage gain, |A(o)|.

The best value for this is obtainable with the substrate of the MOSFET connected to its source. However, this is not a preferred option in practice because it means extra complication in an N-well diffusion process.

Despite variations in V_{DS} and V_{SB} with V_O, the linearity of the DC transfer characteristic was good. The temperature variation of this characteristic was very

small for both current and resistive loads amounting to parallel shift to the right with temperature increase by no more than about 1mV/°C over the range -40°C to +85°C. There was little change in small signal behaviour up to about 10GHz, even with non-negligible capacitive loading by the circuits likely to be driven.

3.5 References

[3.1] Allen P. E. and Holberg D. R., 'CMOS Analog Circuit Design', Oxford University Press, Second Edition, New York, 2002, pp. 136-137

[3.2] Allen P. E. and Holberg D. R., 'CMOS Analog Circuit Design', Oxford University Press, Second Edition, New York, 2002, pp. 40

[3.3] Tsividis Y. P., 'Operation and Modelling of the MOS transistor', McGraw-Hill, New York, 1987, pp. 148

3.6 Appendix 3

Appendix 3.1 Output impedance of a 1:1 CM

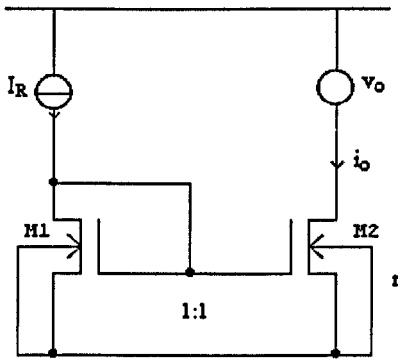


Fig A 3.1.1 A 1:1 CM

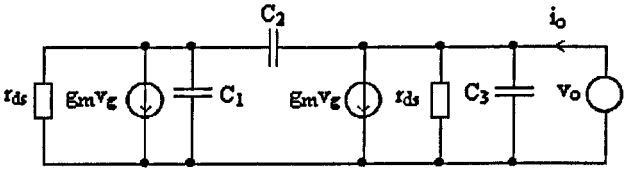


Fig A 3.1.2 Small-signal equivalent of Fig 3.1.1

In the small-signal equivalent circuit of Fig.A3.1.2, $C_1 = (2\,C_{gs} + C_{db})$, $C_2 = C_{gd}$ and $C_3 = C_{db}$.

We require to find $Z_o = (v_o / i_o)$ in terms of the complex frequency variables s.

KCL at the output node gives,

$$i_o = (g_{ds} + sC_3)v_o + g_m v_g + (v_o - v_g)sC_2 \qquad \text{(A 3.1.1)}$$

KCL at the gate node gives,

$$sC_2(v_o - v_g) = (g_m + g_{ds})v_g + sC_1 v_g \qquad \text{(A 3.1.2)}$$

or, $$sC_2 v_o = v_g[(g_m + g_{ds}) + s(C_1 + C_2)] \qquad \text{(A 3.1.3)}$$

and, $$v_g = \frac{sC_2 v_o}{(g_m + g_{ds}) + s(C_1 + C_2)} \qquad \text{(A 3.1.4)}$$

Substituting v_g, in eqn.A 3.1.4, into eqn.A 3.1.1 gives,

$$i_o = v_o\left[g_{ds} + s(C_2 + C_3) + \frac{(g_m - sC_2)sC_2}{(g_m + g_{ds}) + s(C_1 + C_2)}\right] \qquad \text{(A 3.1.5)}$$

$$\therefore Z_o = \frac{v_o}{i_o} = \frac{(g_m + g_{ds}) + s(C_1 + C_2)}{[g_{ds} + s(C_2 + C_3)] + [(g_m + g_{ds}) + s(C_1 + C_2)] + (g_m - sC_2)sC_2} \qquad \text{(A 3.1.6)}$$

$$Z_o = \frac{(g_m + g_{ds}) + s(C_1 + C_2)}{g_{ds}(g_m + g_{ds}) + s[(g_m + g_{ds})(C_2 + C_3) + g_{ds}(C_1 + C_2) + g_m C_2] + s^2[(C_1 + C_2)(C_2 + C_3) - C_2^2]} \quad \text{(A 3.1.7)}$$

$$Z_o = \frac{1 + s\dfrac{(C_1 + C_2)}{(g_m + g_{ds})}}{g_{ds} + s\left[(C_2 + C_3) + \dfrac{g_{ds}}{(g_m + g_{ds})}(C_1 + C_3) + \dfrac{g_m C_2}{(g_m + g_{ds})}\right] + s^2\left[\dfrac{C_1C_2 + C_1C_3 + C_2C_3}{(g_m + g_{ds})}\right]} \quad \text{(A 3.1.8)}$$

$$Z_o = \frac{1 + \dfrac{s(C_1 + C_2)}{(g_m + g_{ds})}}{g_{ds}\left\{1 + s\left[\dfrac{C_1}{(g_m + g_{ds})} + \dfrac{2C_2 + C_3}{g_{ds}}\right] + s^2\left[\dfrac{C_1C_2 + C_1C_3 + C_2C_3}{g_{ds}(g_m + g_{ds})}\right]\right\}} \quad \text{(A 3.1.9)}$$

This has the form

$$Z_o = \frac{\left[1 + \dfrac{s(C_1 + C_2)}{(g_m + g_{ds})}\right]}{g_{ds}[1 + a_1 s + a_2 s^2]} \quad \text{(A 3.1.10)}$$

where, p_1 and p_2 are the poles, assumed real, of Z_o

$$a_1 = \frac{1}{p_1} + \frac{1}{p_2} \quad \text{(A 3.1.11)}$$

$$a_2 = \frac{1}{p_1 p_2} \quad \text{(A 3.1.12)}$$

For $p_2 >> p_1$, there is dominant pole p_1

$$p_1 \cong \frac{1}{a_1} \quad \text{(A 3.1.13)}$$

and, $$p_2 \cong \frac{a_1}{a_2} \quad \text{(A 3.1.14)}$$

Comparing eqns(A 3.1.9) and (A 3.1.10)

$$p_1 = \frac{1}{a_1} = \frac{1}{\left[\dfrac{C_1}{(g_m + g_{ds})} + \dfrac{(2C_2 + C_3)}{g_{ds}}\right]} \quad \text{(A 3.1.15)}$$

There is a zero in the numerator at,

$$Z_1 = \frac{(g_m + g_{ds})}{(C_1 + C_2)} \qquad \text{(A 3.1.16)}$$

Consider the denominator of (A 3.1.15)

$$\left[\frac{C_1}{(g_m + g_{ds})} + \frac{(2C_2 + C_3)}{g_{ds}}\right] = \frac{1}{g_{ds}}\left[\frac{C_1 g_{ds}}{(g_m + g_{ds})} + (2C_2 + C_3)\right] \qquad \text{(A 3.1.17)}$$

$$= \frac{1}{g_{ds}}\left[\frac{C_1}{(1+\mu)} + (2C_2 + C_3)\right] \qquad \text{(A 3.1.18)}$$

where $\mu = g_m r_{ds}$ (>>1)

The output circuit defining the dominant pole can than be shown as in Fig A 3.3

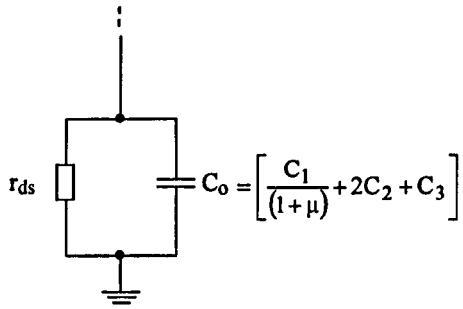


Figure A 3.1.3 First-order approximation for equivalent output circuit

Of interest is the fact that C_2, which is the C_{gd} of M2, is effectively doubled. This results from current mirror action.

Substituting measured parameters data for g_{ds}, μ, C_1, C_2, C_3 in (A 3.1.19)

gives,

$$f_p = \frac{\omega_{p_1}}{2\pi} \cong 7.6\text{GHz} \qquad \text{(A 3.1.19)}$$

Appendix 3.2 Source-Follower analysis

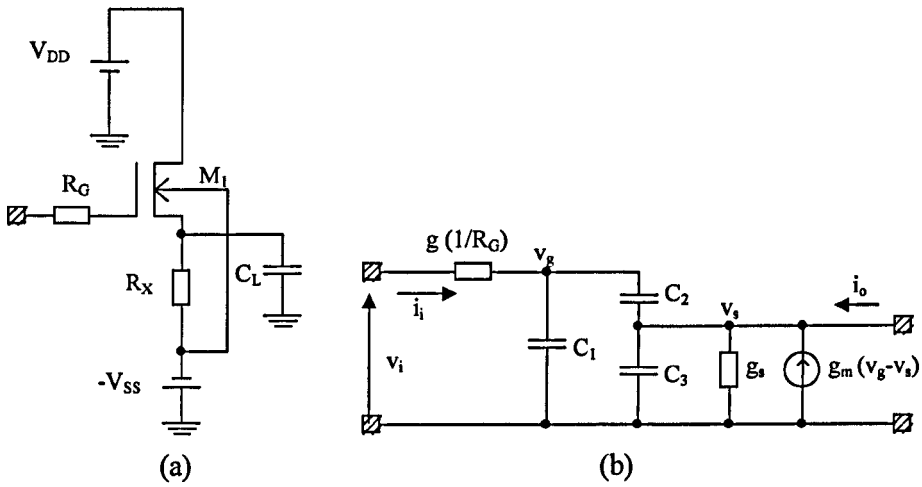


Figure A 3.2.1 (a) General circuit configuration for a source-follower

(b) Small-signal equivalent of (a)

The small-signal equivalent circuit of Fig.A 3.2.1 permits the determination of small-signal voltage gain, A, input impedance Z_i and output impedance Z_o, of the source-follower configuration shown in (a): $g_s = (g_x + g_{ds} + g_{mb})$, where $g_x = 1/R_x$

$C_1=C_{gd}$; $C_2=C_{gs}$; $C_3=C_L$ (external capacitive load) $+C_{sb}$

Thus, $$A = \left.\frac{v_s}{v_i}\right|_{i_o=0} \qquad \text{(A 3.2.1)}$$

$$Z_i = \left.\frac{v_i}{i_i}\right|_{i_o=0} \qquad \text{(A 3.2.2)}$$

and, $$Z_o = \left.\frac{v_s}{i_o}\right|_{v_i=0} \qquad \text{(A 3.2.3)}$$

(a) Determination of A

KCL at the input gives,

$$g_g(v_i - v_g) = sC_1v_g + sC_2(v_g - v_s) \quad \text{(A 3.2.4)}$$

or, $$g_g v_i = [g_g + s(C_1 + C_2)]v_g - sC_2v_s \quad \text{(A 3.2.5)}$$

KCL at output gives,

$$sC_2(v_g - v_s) + g_m(v_g - v_s) = v_s(g_s + sC_3) \quad \text{(A 3.2.6)}$$

or, $$v_g[g_m + sC_2] = v_s[(g_s + g_m) + s(C_2 + C_3)] \quad \text{(A 3.2.7)}$$

Substituting for v_g from eqn. (A 3.2.7) into eqn. (A 3.2.5)

$$g_g v_i = \frac{[g_g + s(C_1 + C_2)][(g_s + g_m) + s(C_2 + C_3)]v_s}{(g_m + sC_2)} - sC_2v_s \quad \text{(A 3.2.8)}$$

$$\frac{g_g v_i}{v_s} = \frac{g_g(g_s + g_m) + s[(g_s + g_m)(C_1 + C_2) + g_g(C_2 + C_3) - g_mC_2] + s^2[C_1C_2 + C_1C_3 + C_2C_3]}{g_m + sC_2}$$

(A 3.2.9)

or,

$$A(s) = \frac{v_s}{v_i} = \frac{g_g(g_m + sC_2)}{g_g(g_s + g_m) + s[(g_s + g_m)C_1 + (g_s + g_m)C_2 + g_g(C_2 + C_3) - g_mC_2] + s^2[C_1C_2 + C_1C_3 + C_2C_3]}$$

(A 3.2.10)

$$A(s) = \frac{g_g(g_m + sC_2)}{g_g(g_s + g_m) + s[(g_s + g_m)C_1 + g_sC_2 + g_g(C_2 + C_3)] + s^2[C_1C_2 + C_1C_3 + C_2C_3]}$$

(A 3.2.11)

This expression indicates a zero at $s_z = -g_m/C_{gs}$ and a dominant pole (assuming there is one)

at, $$s_p = \frac{-g_g(g_s + g_m)}{(g_s + g_m)C_1 + g_sC_2 + g_g(C_2 + C_3)} \quad \text{(A 3.2.12)}$$

$$\text{or,} \quad s_p = -\frac{1}{\frac{C_1}{g_g} + \frac{g_s C_2}{g_g(g_s+g_m)} + \frac{(C_2+C_3)}{(g_s+g_m)}} \tag{A 3.1.13}$$

$$\text{or} \quad s_p = -\frac{1}{C_{gd}R_G + \frac{C_{gs}R_S{}^2R_G}{(1+g_mR_S)} + \frac{(C_{gs}+C_L+C_{sb})R_G}{(1+g_mR_S)}} \tag{A 3.1.14}$$

The l.f value of A(s), gives by putting s = 0 in eqn.3.2.11, is,

$$A(s) = \frac{g_m}{(g_s+g_m)} \tag{A 3.2.15}$$

(b) Determination of Zi

Consider the section of Fig.A3.2.1 (b) v_s to the right of the junction with C_L,

From eqn.(A 3.2.7),

$$v_s = \frac{(g_m+sC_2)}{(g_s+g_m)+s(C_2+C_3)} v_g \tag{A 3.2.16}$$

$$\therefore (v_g - v_s) = \left[1 - \frac{(g_m+sC_2)}{(g_s+g_m)+s(C_2+C_3)}\right] \cdot v_g \tag{A 3.2.17}$$

The current in C_2 is $$sC_2\left[1 - G(o)\frac{1+\frac{sC_2}{g_m}}{1+\frac{s(C_2+C_3)}{(g_s+g_m)}}\right] \tag{A 3.2.18}$$

Thus, provided $\omega << \frac{g_m}{C_2}$ and $\omega << \frac{(g_s+g_m)}{(C_2+C_3)}$, whichever is the smaller, the input can be modelled as shown in Fig.A 3.2.2, which illustrates the section of bootstrapping.

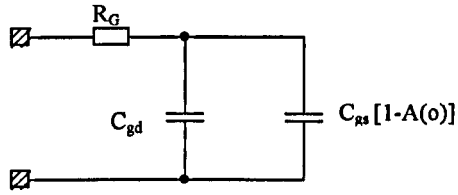


Figure A 3.2.2 Simplified representation of the input circuit

(c) Determination of Z_o

Referring to Fig A3.2.1 (b), for the case $v_i=0$, we can write

$$-g_g v_g = sC_1 v_g + sC_2(v_g - v_s) \quad \text{(A 3.2.19)}$$

or, $$[g_g + s(C_1 + C_2)]v_g = sC_2 v_s \quad \text{(A 3.2.20)}$$

Furthermore,

$$i_o(s) + g_m(v_g - v_s) + sC_2(v_g - v_s) = v_s(g_s + sC_3) \quad \text{(A 3.2.21)}$$

or, $$i_o(s) = v_s[g_s + g_m + s(C_2 + C_3)] - v_g[g_m + sC_2] \quad \text{(A 3.2.22)}$$

From this equation $Z_o(s)$ is calculated for a given $s(= j\omega)$.

However, the general expression in complex: for the special case $R_S=0$ the equivalent output circuit is shown in Fig.A 3.2.3

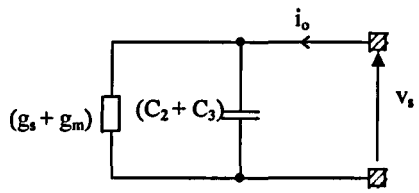


Figure A 3.2.3 Small signal output circuit for $R_G = 0$

Appendix 3.3 Additional Source-Follower characteristics.

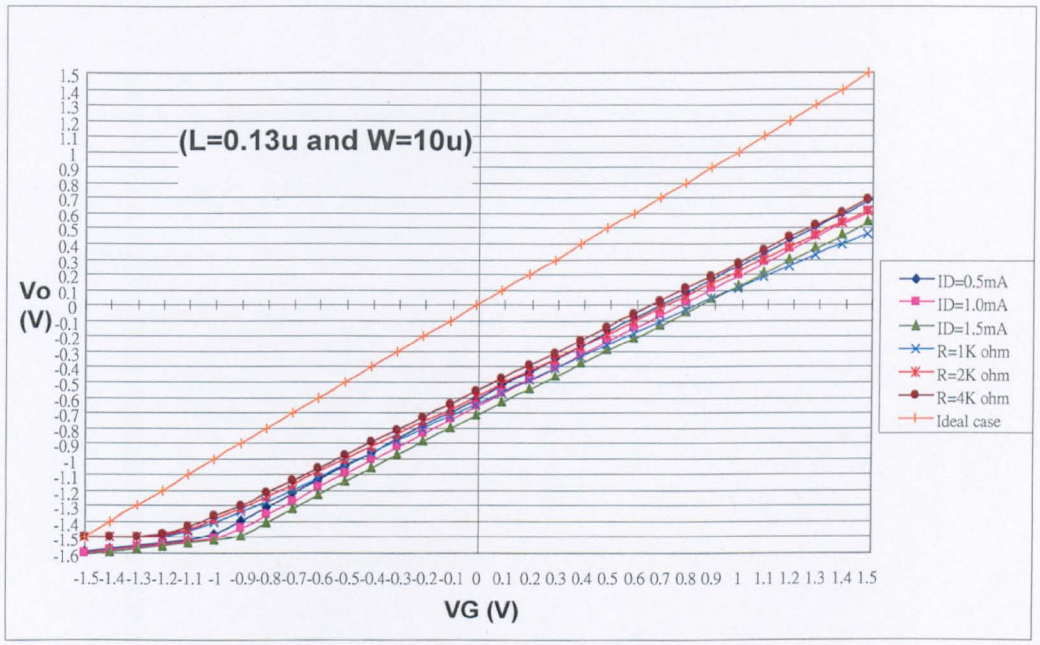


Figure A 3.3.1 Combined source-follower transfer characteristic: V_{SS}=V_{DD}=1.5V

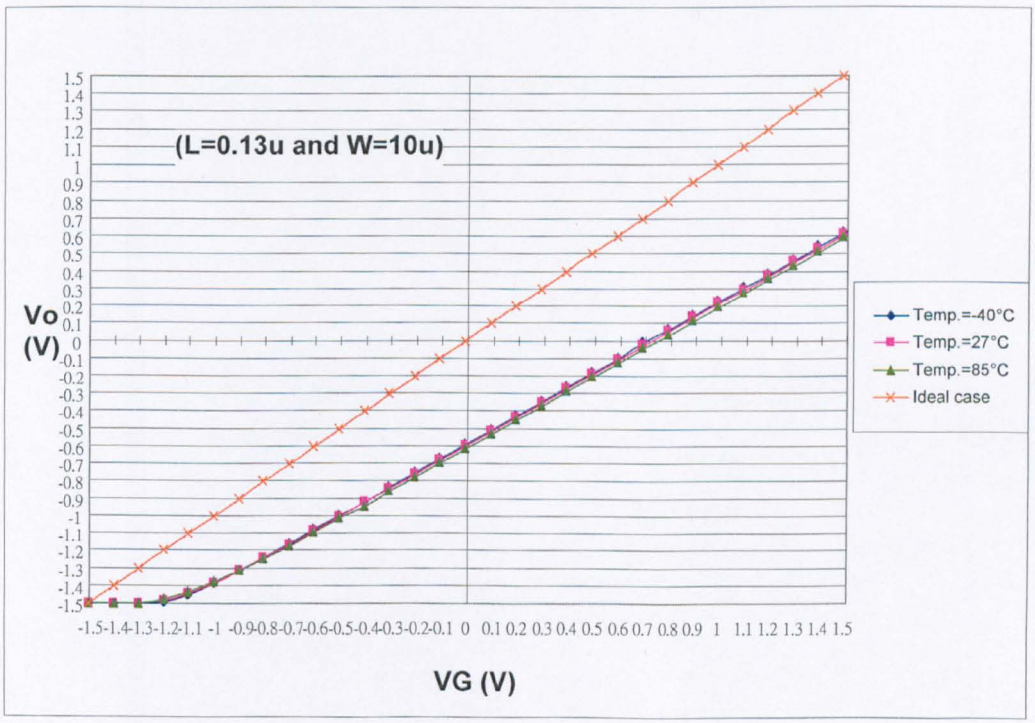


Figure A 3.3.2 Temperature effect on a source-follower with a 2KΩ load: V_{SS}=V_{DD}=1.5V

CHAPTER 4

A CRITICAL REVIEW OF EXISTING V-I CONVERTER DESIGNS

4.1 Introduction

This chapter presents a critical review of existing V-I designs and outlines the design approach that will be adopted for the remainder of this thesis.

Bipolar V-Is have a long history so it is an obvious approach to see how they could be adapted for use with MOSFETs, when these seem to offer some performance advantages, e.g., higher input impedance and use in MOSFET mixed-signal circuitry.

Two types of BJT design became established. In the first [4.1], and more popular technique, called here, Type A, the non-linearity in the relationship between the collector current and base-emitter voltage of a BJT is taken care of by the use of negative feedback and the transconductance is defined by a resistor.

The second, and seemingly little-used technique [4.2], called here Type B, purposely makes use of the exponential relationship between the collector current and base-emitter voltage and the close parameter matching possible with bipolar devices: no resistor is used to define the transconductance, that is set by transistor geometry.

Two design philosophies have emerged for MOSFETs.

The first resembles that for BJTs in that negative feedback is employed to circumvent the non-linear relationship between drain current and gate-source voltage, and a resistor is used to define the transconductance.

The second exploits the square-law relationship between drain current and gate-source voltage, and a resistor is not required to define the transconductance. As in the case of BJTs it is set by device geometry and a bias current.

The next section outlines the system-level implementation of the two approaches. After that some typical circuits are reviewed.

4.2 System-level approached to V-I design

4.2.1 Type A

Fig.4.1 [4.1] is a system diagram for Type A design.

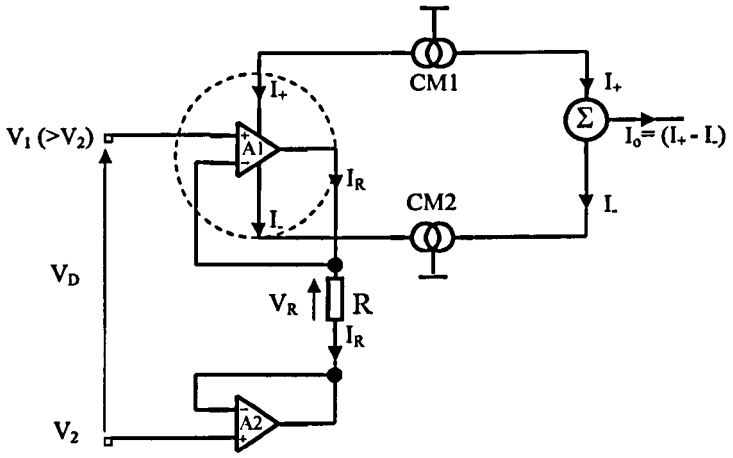


Figure 4.1 A system-level implementation of a Type A V-I

A1 and A2 are operational amplifiers, with a high voltage gain, strapped to operate as voltage-followers. They are driven by input voltage signals V_1, V_2, respectively, and their outputs are connected by a resistor, R. The potential difference, V_R, across R for the ideal case of infinite amplifier voltage gain is equal to, and has the same polarity as, the differential input voltage, $V_D=V_1-V_2$. The current I_R, in R, is thus V_D/R and has the direction shown for $V_D > 0$ (i.e., $V_1>V_2$).

Now consider the dotted contour surrounding amplifier A1. If the amplifier input currents are neglected (a justifiable assumption, particularly with amplifiers having MOSFET input stages) then Kirchhoff's Current Law (KCL) demands that I_R and the amplifier supply-terminal currents are related by,

$$I_R = I_+ - I_- \qquad (4.1)$$

The unity-gain current mirrors CM1, CM2, repeat I_+, I_-, respectively, and the current mirror outputs are combined, with the result that,

$$I_o = I_R = \frac{V_D}{R} \tag{4.2}$$

or, $$G_t \overset{\Delta}{=} \frac{dI_o}{dV_D} = \frac{1}{R} \tag{4.3}$$

An alternative system-level implementation involves the use of a current conveyor type CCII +.

A block representative of this [4.2] is given in Fig.4.2

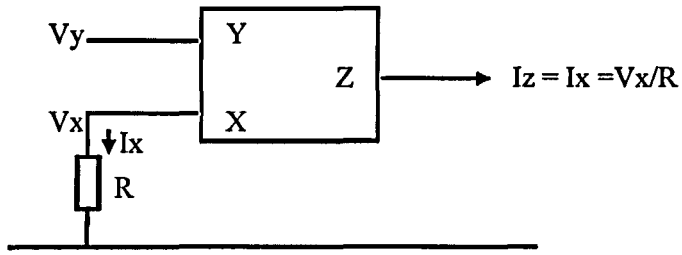


Figure 4.2 Alternative system-level implementation of a Type A V-I

The defining matrix for the CCII+ is,

$$\begin{pmatrix} I_y \\ V_x \\ I_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix} \begin{pmatrix} V_y \\ I_x \\ V_z \end{pmatrix} \tag{4.4}$$

With a resistor connected to terminal X, as shown, eqn.(4.3) is, again, applicable.

4.2.2 Type B

Fig.4.3 illustrates the basis of this. The circuit combining I_1 and I_2,

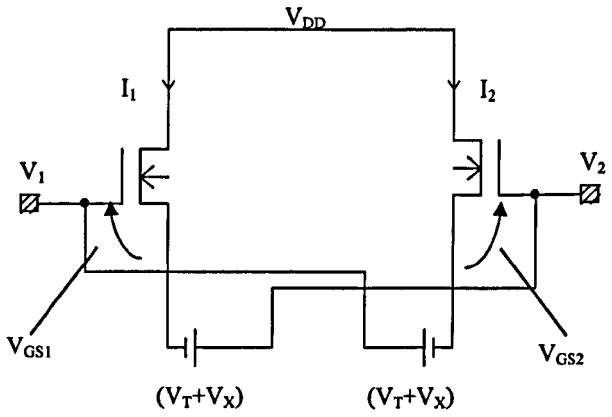


Figure 4.3 Showing the operating principle of Type B V-I

is, however, omitted because it involves no new principle, only the use of current mirrors.

(V_T+V_X) is a floating voltage source.

Assuming M_1 and M_2 have identical square-law characteristics when operated in the saturation region, we can write,

$$I_1 = \frac{\beta}{2}(V_{GS1} - V_T)^2 \qquad (4.5)$$

and, $$I_2 = \frac{\beta}{2}(V_{GS2} - V_T)^2 \qquad (4.6)$$

But, $$V_1 - V_{GS1} + (V_T + V_X) = V_2 \qquad (4.7)$$

or, $$V_{GS1} = V_D + (V_T + V_X) \qquad (4.8)$$

Similarly, $$V_{GS2} = -V_D + (V_T + V_X) \qquad (4.9)$$

Substituting for V_{GS1}, from eqn.4.8, in eqn.4.5 gives,

$$I_1 = \frac{\beta}{2}(V_X + V_D)^2 \qquad (4.10)$$

Similarly, substituting for V_{GS2}, from eqn.4.9, in eqn.4.6 gives

$$I_2 = \frac{\beta}{2}(V_X - V_D)^2 \tag{4.11}$$

Hence, $$(I_1 - I_2) = \frac{\beta}{2}\left[(V_X + V_D)^2 - (V_X - V_D)^2\right] \tag{4.12}$$

$$\therefore G_t = \frac{d(I_1 - I_2)}{dV_D} = \frac{\beta}{2}(2V_X)(2V_D) \tag{4.13}$$

or, $$G_t = 2\beta \cdot V_X \tag{4.14}$$

Fig.4.4 illustrates the meaning of eqn.4.14:

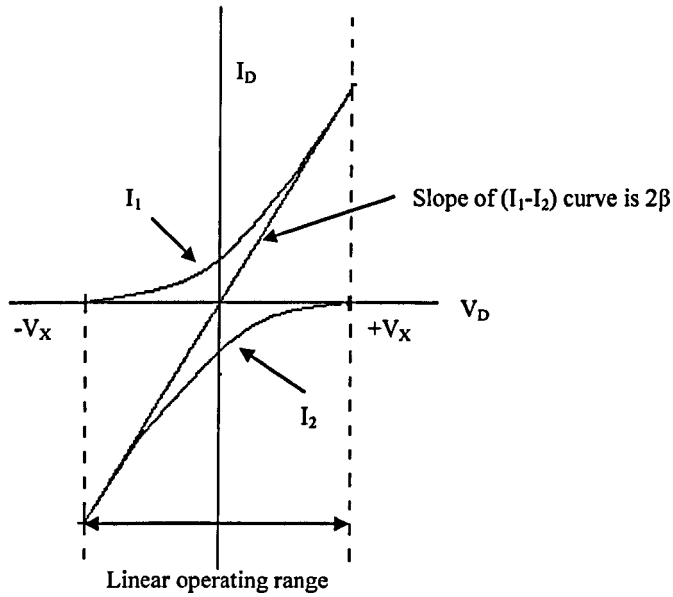


Figure 4.4 Graphical interpretation of eqn (4.14)

4.3 Limitation of Type B designs

It was decided to conduct further research only into Type A circuits.

To understand why it is necessary to indicate the fundamental limitations of Type B circuits.

Fig.4.5 shows a version of Fig.4.3 proposed by Negungadi and Visvanathan [4.3]. In this, the floating voltage sources of Fig.4.3 are provided by the source-follower transistors M_3 and M_4, which have gate widths n times larger than those of the input transistors M_1, M_2.

If n is 'large' (>5) and the input signal voltages V_1 and V_2 are 'small', the gate source voltage of M_3 and M_4 are both constant at $\left(V_T + \sqrt{\frac{2I_B}{\beta}}\right)$, i.e.,. $V_X = \sqrt{\frac{2I_B}{\beta}}$

If n is not large the bias current through M_3 and M_4 changes and the linear relationship between I_o (= I_1-I_2) and V_D (= V_1-V_2) suffers.

A disadvantage of this arrangement is that large bias currents pass through M_1 and M_2.

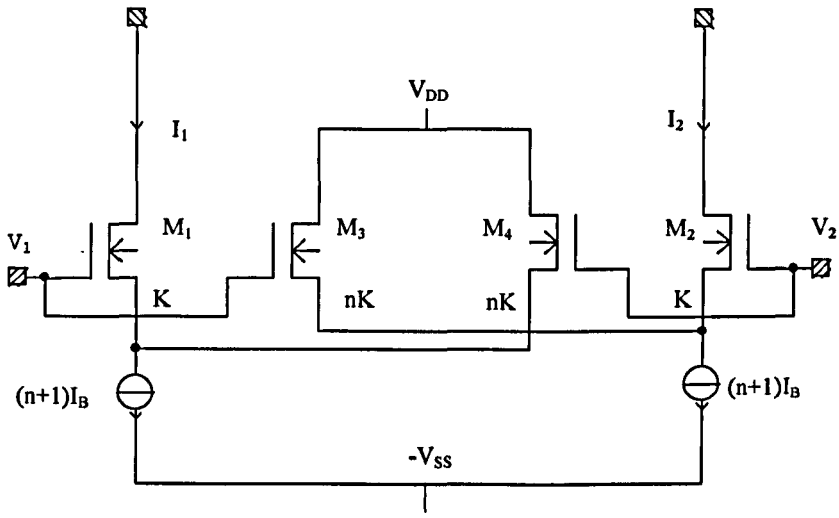
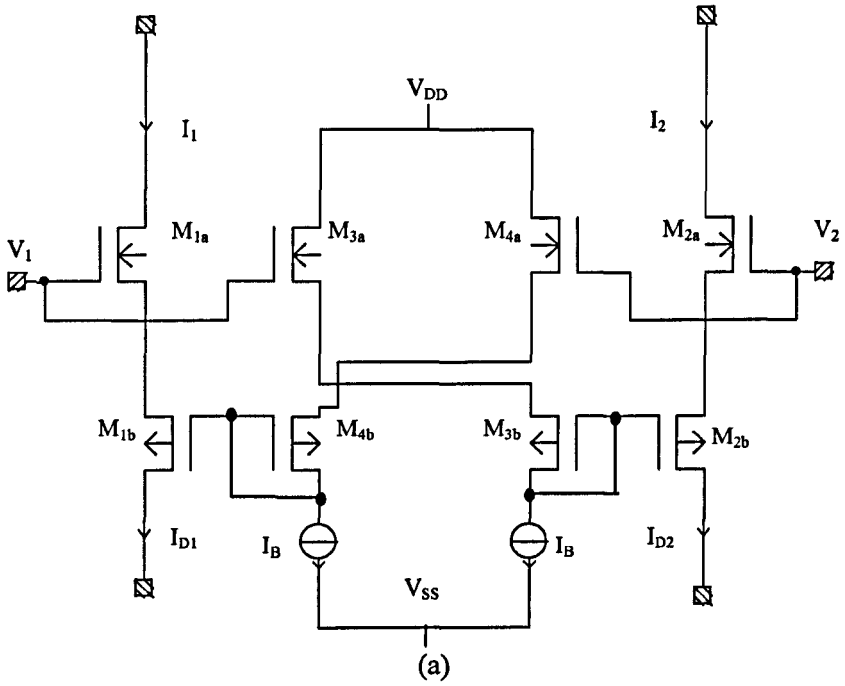


Figure 4.5 Circuit of Negungadi and Viswanathan [4.3]



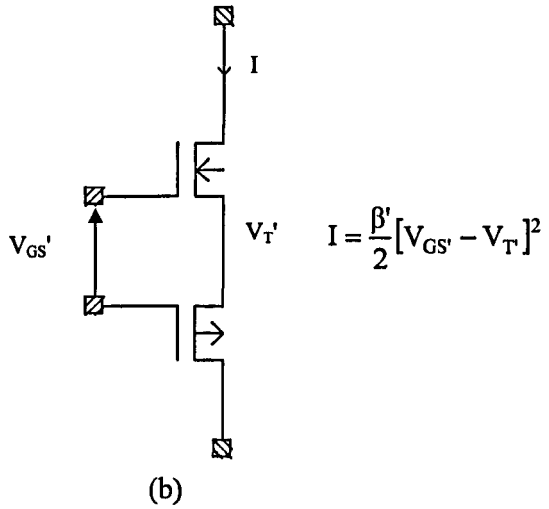


Figure 4.6 **(a) Circuit of Seevinck and Wassenaar [4.4]**
(b) Operation of a CMOS double-pair (See text)

Seevinck and Wassenaar [4.4] improved on the previous circuit with the arrangement of Fig.4.6.

In this ingenious scheme, the current for the floating voltage sources (the n-p combinations M_{3a}+M_{3b}, M_{4a}+ M_{4b}) is fixed by independent bias sources (I_B) and does not flow through the output transistors.

Its operation can be understood by realising that a CMOS double pair such as (M_{1a}+M_{1b}) in Fig.4.6 behaves as a single n channel MOSFET characterised by,

$$V_T' = V_{Tn} + V_{Tp} \tag{4.15}$$

$$\frac{1}{\sqrt{\beta'}} = \left[\frac{1}{\sqrt{\beta_n}} + \frac{1}{\sqrt{\beta_p}}\right] \tag{4.16}$$

and, $$V_{GS}' = V_T' + \sqrt{\frac{2I_B}{\beta'}} \tag{4.17}$$

In this case, $$V_X = \sqrt{\frac{2I_B}{\beta'}} \tag{4.18}$$

Demosthenous and Panovic [4.5] have proposed the simpler scheme shown in Fig.4.7

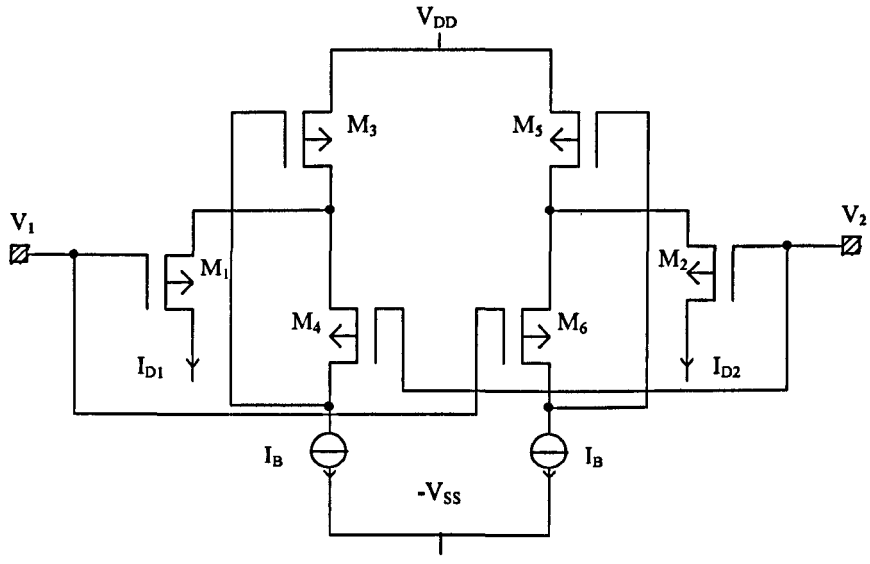


Figure 4.7 Circuit of Demosthenous and Panovic [4.5]

This uses a so-called 'Flipped Voltage Follower' (discussed in more detail in a later chapter). Here, M_4 and M_6 provide the floating voltage sources. The V_{GS} of each is $\left[V_T + \sqrt{\frac{2I_B}{\beta}}\right]$ because feedback in the combination M_3, M_4 and M_5, M_6 ensures that M_4, M_5 operate with a constant drain current.

As before, $$V_X = \sqrt{\frac{2I_B}{\beta}} \qquad (4.19)$$

The deficiencies of the circuit of Fig.4.5 have already been mentioned.

The circuit of Fig.4.6 is superior in respect of the provision of the floating voltage sources: the bias currents for them no longer pass through the output transistors. Additionally, the circuit is able to accommodate a wide input signal range.

However, the vertical stacking of the transistors counts against operation at low rail voltages. This is not a problem with the circuit of Fig.4.7.

All three of the circuits discussed so far in this section are open to criticisms on two counts. First is their dependence on the close parameter matching of the MOSFETs. Second, they assume a perfect square-law relationship between drain current and gate-source voltage. For MOSFETs with channel lengths of 0.13μm, the effect of varying drain voltage is significant.

Because of these shortcomings it was decided to conduct research only into Type A circuits.

4.4 Type A development choices

4.4.1 The differential amplifier with degeneration

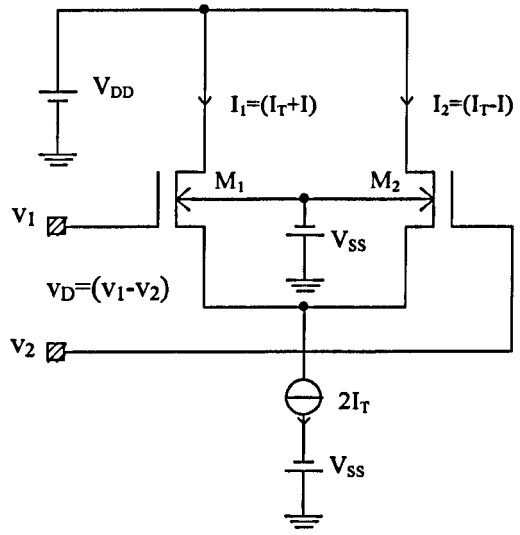


Figure 4.8 A differential amplifier: $V_D > 0$

The differential amplifier of Fig.4.8 is capable of offering only a small differential input range V_D for linear V-I conversion.

This can be seen from the following argument.

Adopting an approach employed elsewhere [4.6], but using different symbols, it can be shown that,

$$(I_2 - I_1) = 2I = 2\sqrt{\frac{2I_T}{\beta}}V_D\sqrt{1-\left(\frac{\beta V_D{}^2}{8I_T}\right)} \qquad (4.20)$$

provided $|V_D| \le \sqrt{\frac{4I_T}{\beta}}$ (4.21)

Let $V_b = \sqrt{\frac{2I}{\beta}}$, $x = \frac{V_D}{V_b}$, and $y = \frac{I}{I_T}$

Then eqn.4.20 can be re-written as,

$$y = 2x\sqrt{1-\frac{x^2}{4}} \tag{4.22}$$

For x <<1 (i.e. $|V| << \sqrt{\frac{2I_T}{\beta}}$) we obtain an almost linear characteristic with,

$$G_t = \sqrt{2 \cdot \beta \cdot I_T} \tag{4.23}$$

For a linearity not worse than 1%, $V_D < 0.28V_b$. i.e. $V_D < 0.28\sqrt{\frac{2I_T}{\beta}}$.

Fig 4.9 shows the transfer characteristic for three values of $2I_T$, viz., 0.5mA, 1mA, 2mA and illustrates the small input range for constant transconductance.

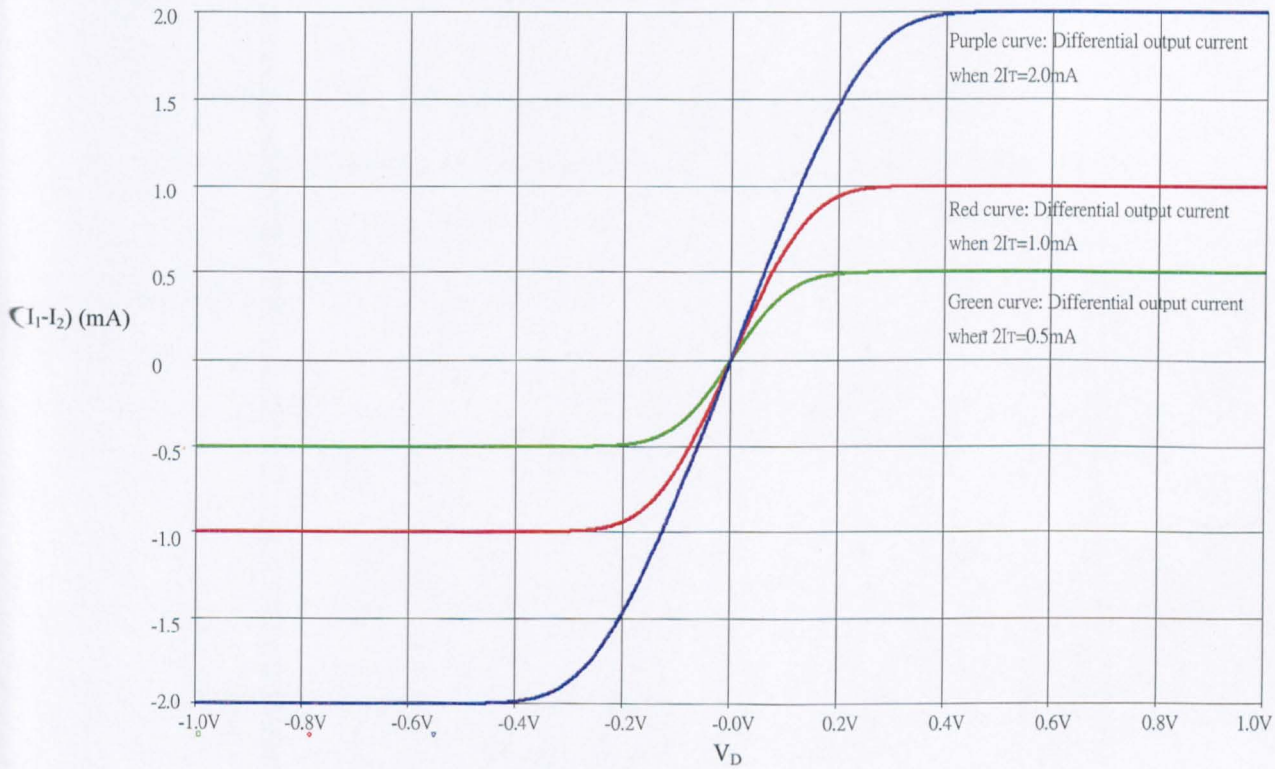


Figure 4.9 Transfer characteristics for the circuit of Fig 4.8

The transfer characteristic can be made more linear using a source degeneration resistor, shown as R in Fig 4.10.

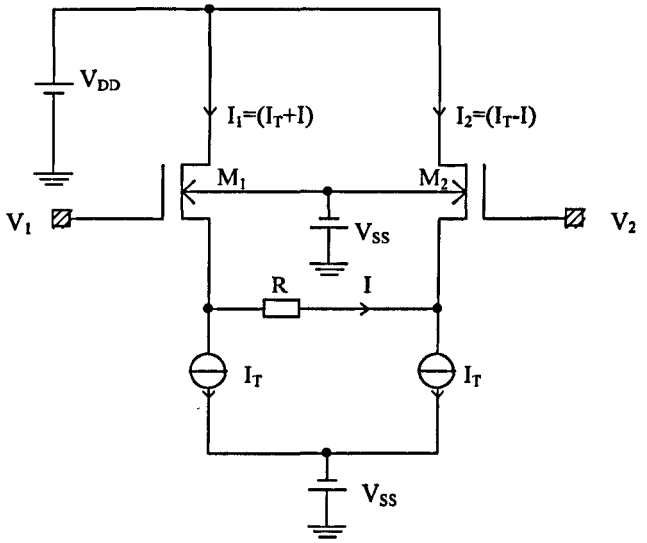


Figure 4.10 Differential amplifier with source degeneration

Apart from the omission of current mirrors at the output, this is the simplest practical implementation of Fig.4.1.

By inspection,

$$V_D = (V_1 - V_2) = V_{GS1} - V_{GS2} + IR \tag{4.24}$$

or, $$V_D = \sqrt{\frac{2(I_T + I)}{\beta}} - \sqrt{\frac{2(I_T - I)}{\beta}} + IR \tag{4.25}$$

$$\therefore \frac{dV_D}{dI} = \frac{1}{2}\sqrt{\frac{2}{\beta}}\frac{1}{\sqrt{I_T + I}} + \frac{1}{2}\sqrt{\frac{2}{\beta}}\frac{1}{\sqrt{I_T - I}} + R \tag{4.26}$$

$$\therefore G_t = \frac{d(2I)}{dV_D} = \frac{2}{R + \sqrt{\frac{1}{2I_T\beta}}\left(\frac{1}{\sqrt{1+x}} + \frac{1}{\sqrt{1-x}}\right)} \tag{4.27}$$

where, $x \overset{\Delta}{=} \frac{I}{I_T}$

When $x \ll 1$, $G_t \rightarrow 2/R$ for any I_T.

G_t can still approach this value for x comparable with unity if R is large enough. This is illustrated in Fig.4.11.

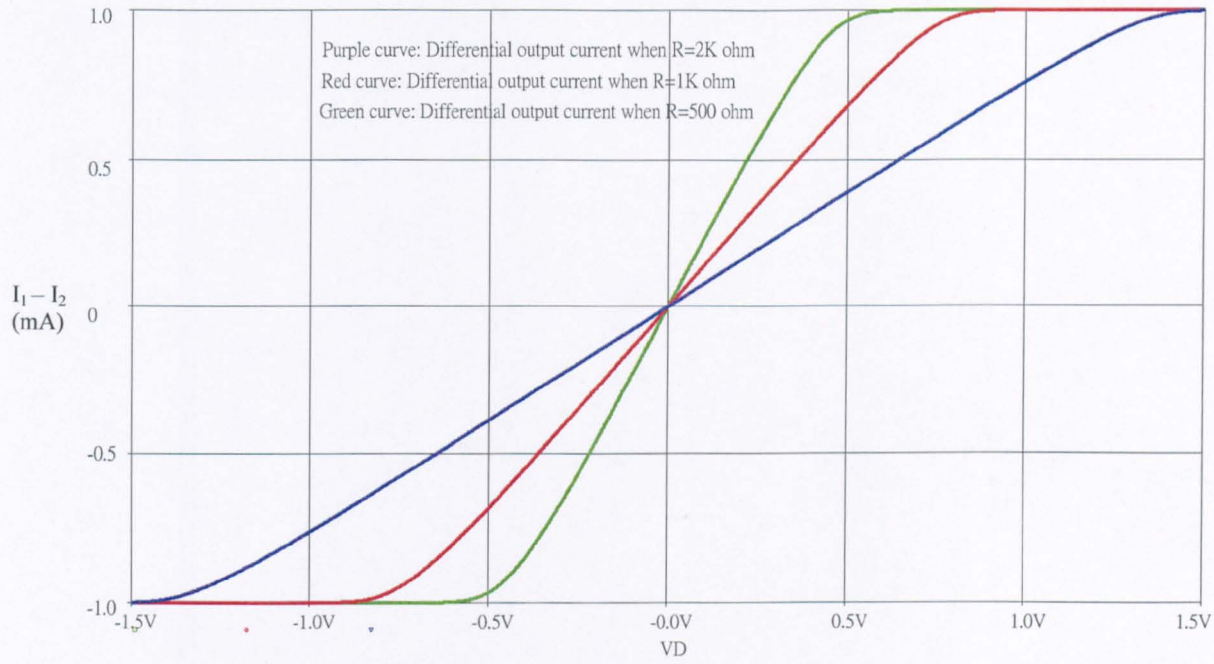


Figure 4.11 Differential amplifier transfer characteristic with source degeneration.

The problem is that making R large for good linearity results in a lower G_t.

Before leaving this section it is worth noting that eqn (4.27) may be re-written in the form,

$$G_t = \frac{2}{R + \frac{1}{g_{m1}} + \frac{1}{g_{m2}}} \qquad (4.28)$$

where g_{m1},g_{m2} are, respectively, the mutual where conductance of M_1 and M_2 at operating currents (I_T+I), (I_T-I) respectively.

4.4.2 The cross-coupled scheme

This technique follows directly that first proposed by Caprio [4.7] for BJTs: it was used later by Khumsat and Worapishet [4.8]. Fig.4.12 shows two circuit configurations but the operation of the circuits was not dealt with in detail(it is below) , with MOSFETs.

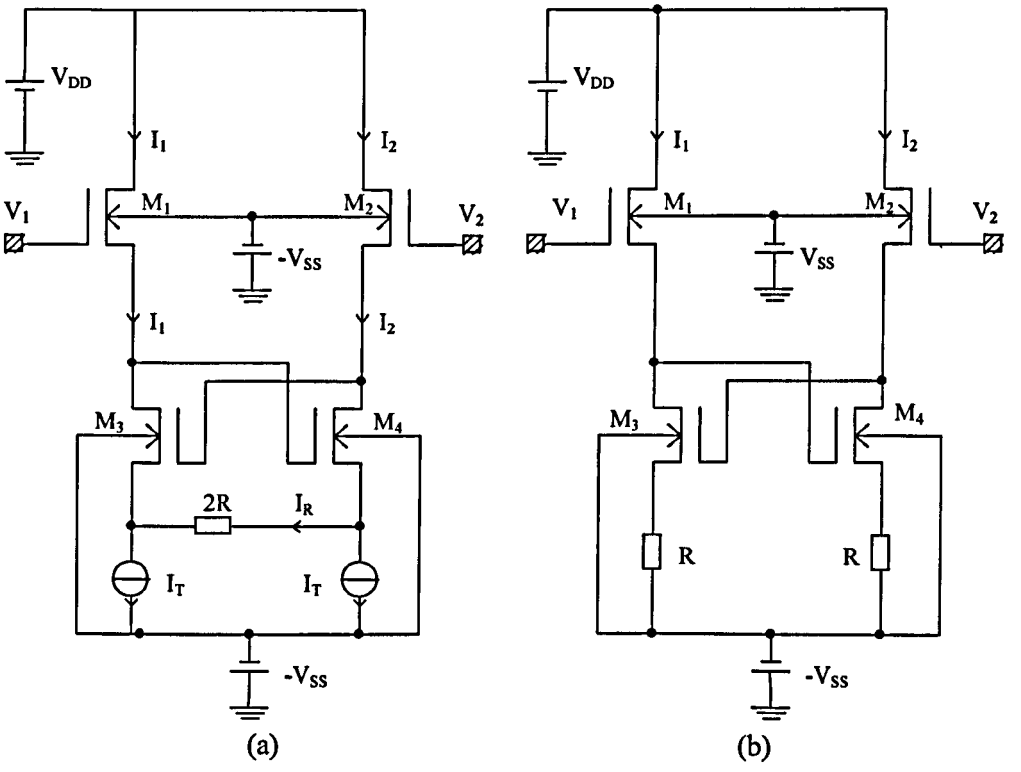


Figure 4.12 Showing two forms of the cross-coupled scheme

(a) Using two current sinks; (b) Using two resistors

Consider, first, the operation of the circuit of Fig.4.12(a).

By inspection,

$$V_A = V_2 - V_{GS2} - V_{GS3} \tag{4.29a}$$

and,

$$V_B = V_1 - V_{GS1} - V_{GS4} \tag{4.29b}$$

$$\therefore (V_B - V_A) = (V_1 - V_2) - V_{GS1} + V_{GS2} - V_{GS4} + V_{GS3} \tag{4.30}$$

But, $V_{GS1}=V_{GS3}$ because of $I_{D1}=I_{D3}=I_1$. Similarly $V_{GS2}=V_{GS4}$ because $I_{D2}=I_{D4}-I_2$.

Hence, $$I_R = (V_1 - V_2)/2R = V_D/2R \tag{4.31}$$

So, for $V_D>0$,

$$I_2 = I_T + I_R \tag{4.32a}$$

$$I_1 = I_T - I_R \tag{4.32b}$$

and, $$G_t = \frac{d(I_2 - I_1)}{dV_D} = \frac{2}{2R} = \frac{1}{R} \tag{4.33}$$

For Fig.4.12(b), also,

$$G_t = \frac{1}{R} \tag{4.34}$$

The same total resistor value is used in both circuits of Fig.4.12. The two circuits are operationally equivalent because for differential drive, with $V_1 = + V_D/2$ and $V_2 = - V_D/2$, the mid point of resistor 2R is at signal earth potential.

4.4.2(a) Circuit implementation and operation

The circuit of Fig.4.12(b) appears in a re-drawn version, as shown in [4.8], with corresponding MOSFET numbering, in Fig.4.13

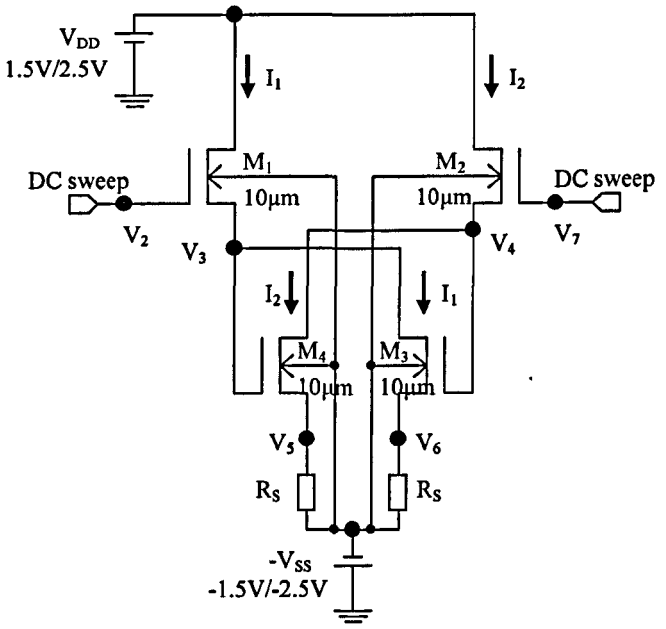


Figure 4.13 Redrawn version of Fig 4.12(b), as shown in [4.8]

This was investigated to determine its limitations, for supply voltages ±1.5V, and two values of R_S, 600 Ω and 1.2KΩ.

The discussion here focuses on the case R= 600 Ω.

The operation is best understood by reference to the voltage and current traces in Figs4.14, 4.15, respectively and a consideration of what happens when a DC sweep voltage is applied to V_2 and V_7. Suppose, initially, $V_2=V_7=0$ then from Fig.4.14, $V_3=V_4 \approx -0.7V$ and M_3, M_4 are in the saturated state, as are M_1 and M_2.

Then $I_1=I_2=I_Q$ where,

$$I_Q R + V_T + \sqrt{2I/\beta} = V_{SS} \qquad (4.35)$$

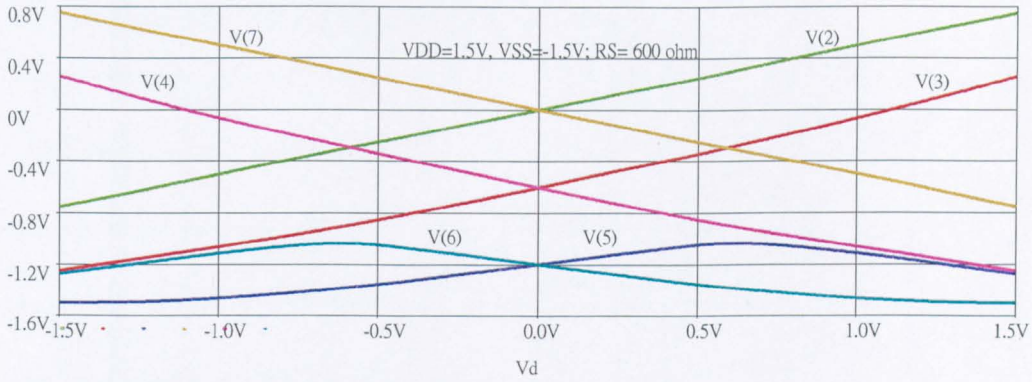


Figure 4.14 Voltage traces for Fig 4.13

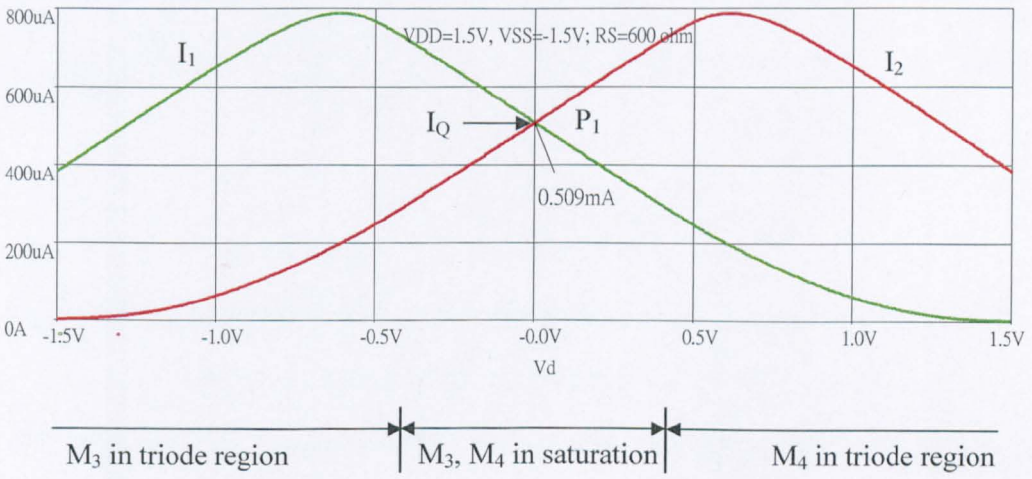


Figure 4.15 Current traces for Fig 4.13

For R=600 Ω, I_Q=0.509mA as indicated in Fig.4.15. As V_D increases, such that V_2= +V_D/2 and V_1= -V_D/2, V_3 and V_5 both increase by source-follower action, thus causing an increase in I_2. Meanwhile V_4 and V_6 both decrease, causing a decrease in I_1.

This process continues till M_4 enters the triode region. This occurs when $(V_3-V_4)=V_T$ or, since $(V_3-V_4)\approx(V_1-V_2)=V_D$, when $V_D=V_T\approx0.4V$.

A further increase in V_D causes I_2 to decrease, as well as I_1.

The mechanism for this is made clearer by reference to *Fig.4.16.*

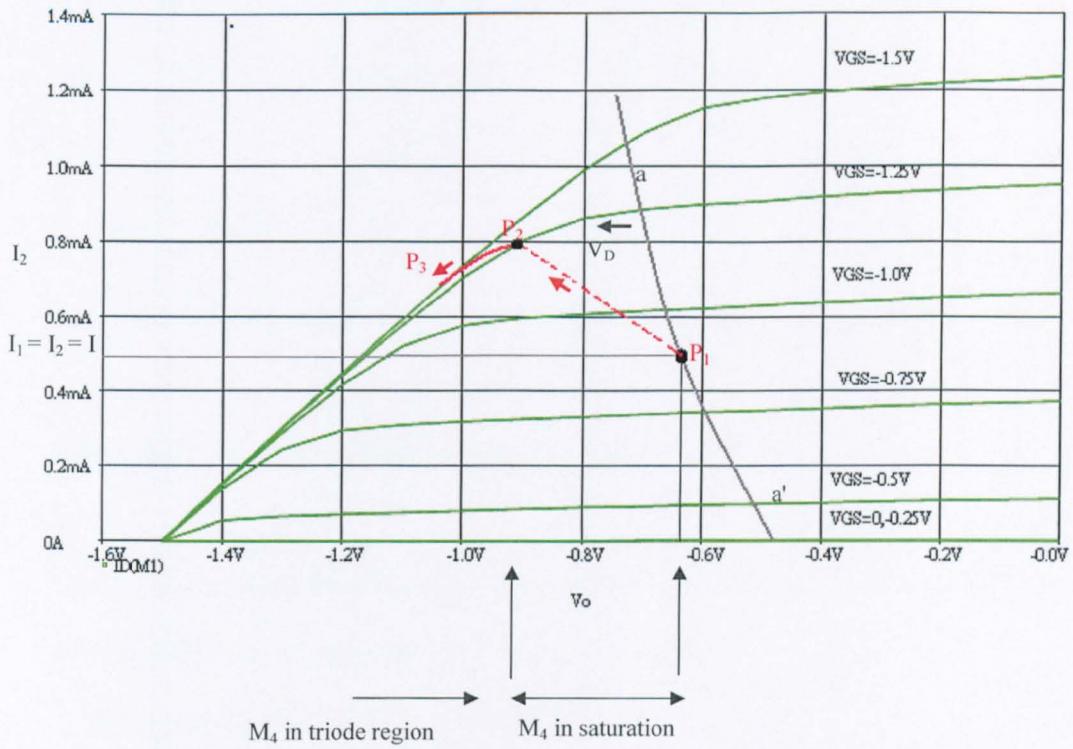


Figure 4.16 Showing the output characteristics of M_4 and current change in I_2 when V_D changes positively from zero, corresponding to P_1

This shows the output characteristics of M_4, with a 600 Ω source load, and the drain load characteristic, aa', for the source-gate circuit of M_2 when V_D=0. At P_1, I_1=I_2=I. Consequent decrease in V_4, and increase in V_3, causes the characteristic aa' to move to the left and the operating point to move to P_2 corresponding to the linear limit of the saturation region for M_4.

Subsequent increase in V_D causes a decrease in I_2. Throughout this process M_1 and M_2 always operate in the saturation region.

The voltage and current traces for $V_D < 0$ are mirror images, about the vertical axis, of the these for $V_D > 0$.

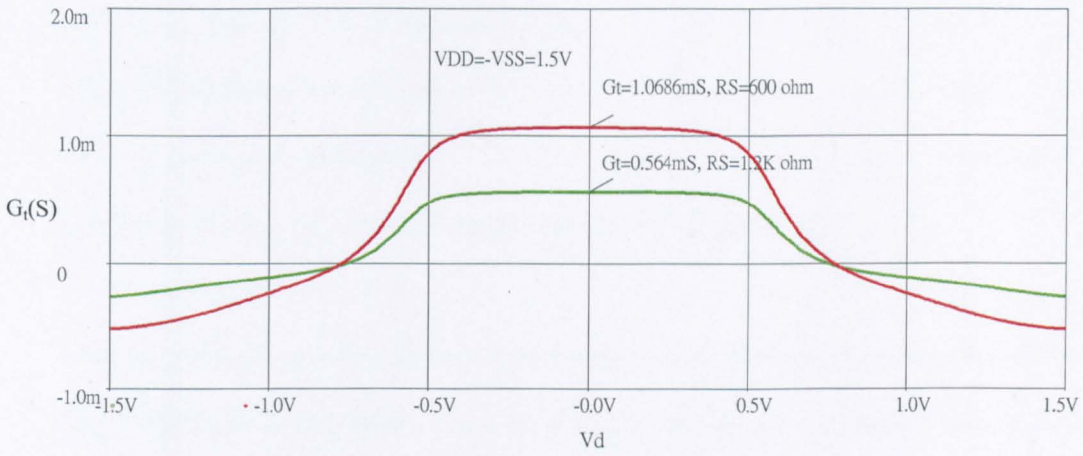


Figure 4.17 Transconductance characteristic for Fig 4.13

Fig.4.17 shows the transconductance characteristic derived from Fig.4.14 and Fig.4.15.

Using eqn.4.34, the ideal design value of G_t is 1.666mS.

However, the observed value is only 1.069mS.

The difference can be explained most simply by a simple small-signal voltage-gain analysis.

Referring to Fig 4.13, suppose the voltage-gain of the source-followers M_1 and M_2 is m and that of M_3,M_4 is n.

Then, in the vicinity of V_D=0,

$$v_3=mv_2;\ v_5=nv_3 \text{ so } v_5=mnv_2 \tag{4.36}$$

Similarly,

$$v_4=mv_7;\ v_6=nv_4 \text{ so } v_6=mnv_7 \tag{4.37}$$

Hence, $$G_t = \frac{mn}{R} \tag{4.38}$$

Looking at the voltage traces in Fig.4.41 it is apparent that 1> m > n because the graph for V_4 is more nearly parallel to V_7 than V_6 is to V_4. This is understandable because M_2 (M_1) has a source load with a higher incremental resistance than that of M_4 (M_3).

It is evident that, $mn \approx 1.0686/1.6666=0.64$ (4.39)

Theoretically [See Chapter 3], $m \approx 1/(1+\chi)$ (4.40)

and, $n = \mu/[1+\mu(1+\chi)+(r_{ds}/R)]$ (4.41)

Substituting data from Chapter 2 on χ, μ and r_{ds}, at I=0.5mA gives,

$$mn \approx 0.62 \quad (4.42)$$

There is, thus, fair argument between the theoretical value of mn given by eqn.4.42 and that determined by simulation, eqn.4.39. Towards the edge of the 'linear' region it is no longer true that the voltage gains of M_1 and M_2 are equal or that those of M_3 and M_4 are equal. This is a cause of non-constancy of G_t.

From eqn (4.33) it follows that $G_t > 0$ if,

$$\frac{dI_2}{dV_D} > \frac{dI_1}{dV_D} \quad (4.43)$$

$G_t < 0$ for M_3 in the triode region because I_1 increases more rapidly than I_2.

Similarly, $G_t < 0$ for M_4 in the triode region because I_2 decays more rapidly than I_1.

Total Harmonic Distortion (THD) as a function of amplitude and frequency is displayed in Fig.4.18. Spot values are given in Appendix4.1

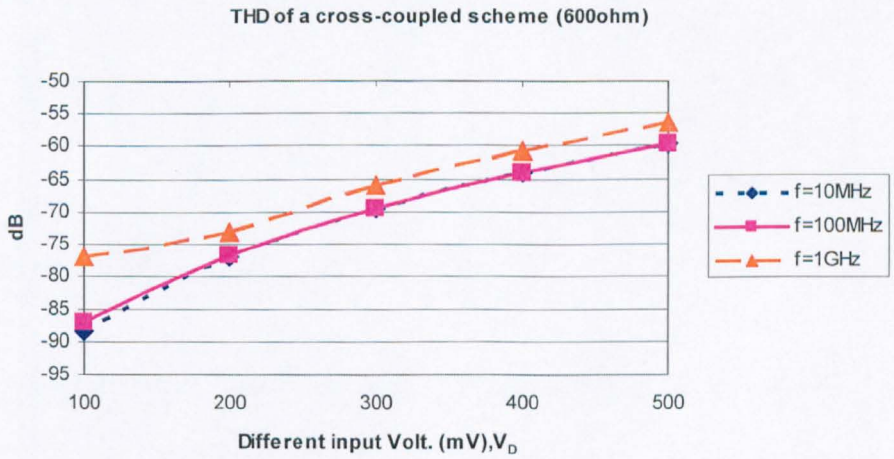


Figure 4.18 Total Harmonic Distortion as a function of amplitude and frequency.

Under the worst conditions (v_D=500mV, f=1GHz) the THD is better than 0.15%.

There are two types of distortion, amplitude distortion, resulting from the non-constancy of the G_t characteristic for varying v_D, and frequency distortion caused by the variation in the magnitude and phase of G_t due to circuit capacitances.

A general discussion of amplitude distortion is well-covered in [4.9].

The third-harmonic component of this most important in the present case. This is inversely related to the open loop-gain, A_{OL}, in a feedback system, and also increases with input signal amplitude.

For a source-follower the loop-gain is given by,

$$A_{OL} = \frac{g_m}{g_m + g_{mb} + g_L + g_{ds}} \tag{4.44}$$

In the cross-coupled scheme under discussion, this cannot exceed g_mR. Furthermore, gm ≈ 5mS at 0.5mA and R=600 Ω, so $g_mR \approx 3$. This small value limits the distortion performance. Frequency distortion causes a worsening in the distortion figure.

Fig.4.19 shows acceptable operation for small-amplitude differential input signals at a frequency of 1GHz.

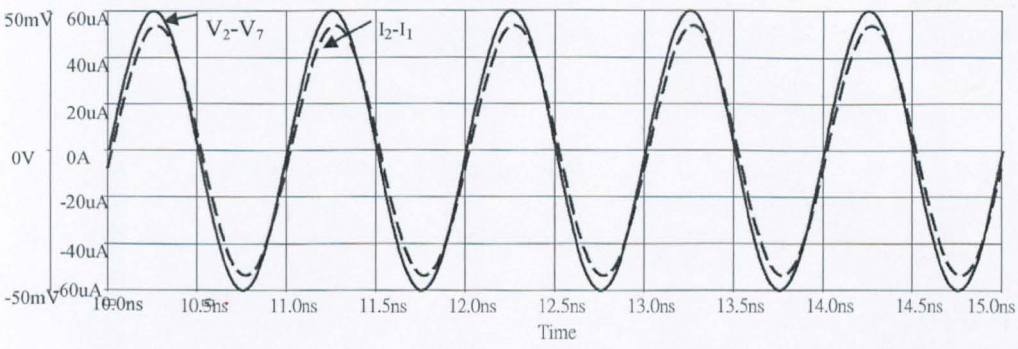


Figure 4.19 Showing differential input voltages (full line curve) and differential output current (dotted-line curve) at 1GHz

An assessment of the suitability of this configuration for further development is given in the Conclusions section of this chapter.

4.4.2(b) Limitations of the cross-coupled scheme

The operation of the two circuits in Fig.4.12 is not dependent on the nature of the mutual characteristics of the MOSFETs used, only on the matching in the respective characteristic of the devices.

The circuit technique employed did, after all, have its origins in a bipolar version. However, MOSFETs do not exhibit the close matching possible with bipolar transistors.

For G_t in the mS range, R must be less than 1KΩ. Consequences of a substrate bias dependent on input voltage, and an r_{ds} comparable with R, are a G_t value that is not accurately predictable and a THD figure that is only modest (typically, 0.1%) because of limited source-follower open-loop gain. The circuit of Fig.4.12(a) is preferable to that of Fig.4.12(b), in that it does not rely on the close resistor matching necessary with the configuration Fig.4.12(b).

However, Fig.4.12(b) can operate with lower supply rails because the simplest current sinks in Fig.4.12(a) would be the outputs of current mirrors, the minimum voltage across which, in saturation, would be about 0.4V.

A limitation of both circuits in Fig.4.12 is that the linear range for G_t is determined by MOSFET threshold voltage.

The range can be extended by use of the modified arrangement of Fig.4.20, in which R=1KΩ and I_B=0.5mA.

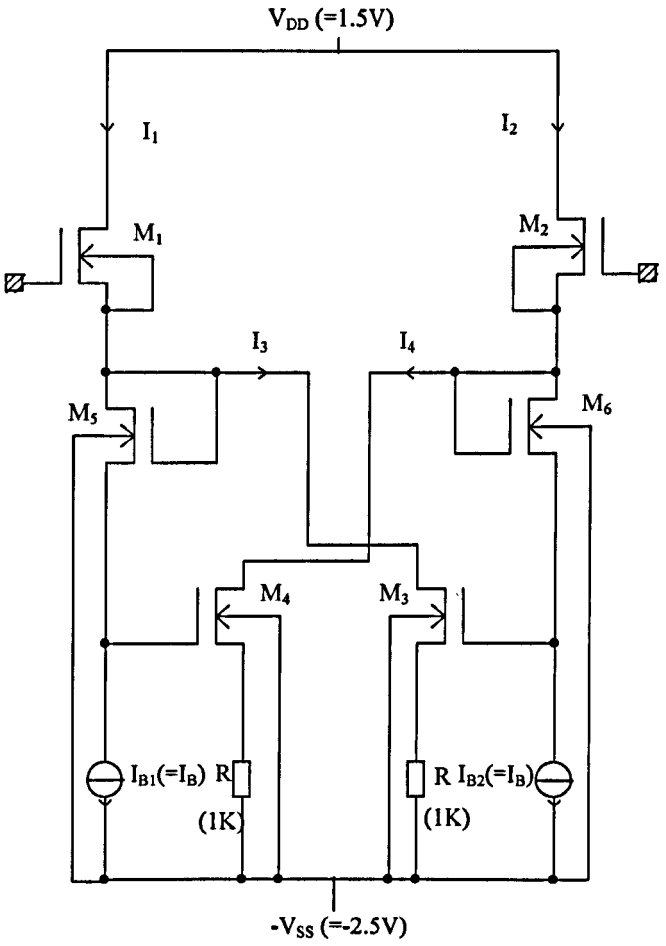


Figure 4.20 Modification of Fig 4.12(b) for extended linear range

I_B= 0.5mA

The extra range, provided by the voltage drops across M_5 and M_6, is evident in Fig 4.21.

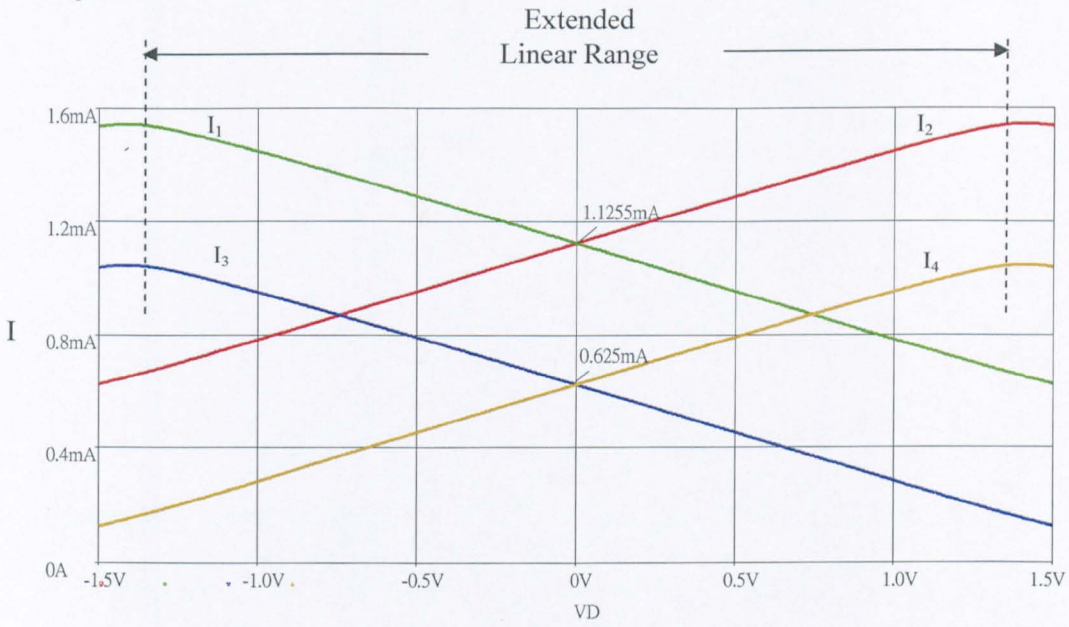


Figure 4.21 Current traces for Fig 4.20 showing extended linear range

The disadvantages incurred are the necessity for a higher value of V_{SS} (increased to 2.5V) to accommodate the voltage drops across M_5 and M_6 and the current sinks, shown here as ideal (but in linear simplest case the output of current mirrors), and matching in the current sinks I_{B1} and I_{B2}.

$I_1=I_3+I_{B1}$ and $I_2=I_4+I_{B2}$ so, for $I_O=(I_1-I_2)$ it is required that $I_{B1}=I_{B2}$.

Finally, it should be noted that there is an unwanted positive feedback loop in the circuit which could give rise to parasitic oscillations.

A small-signal low-frequency equivalent circuit of the loop is shown in Fig 4.22.

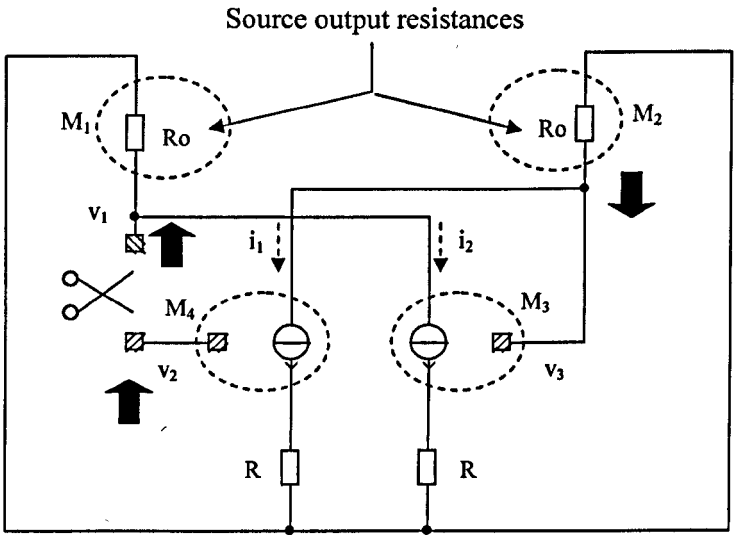


Figure 4.22 Showing the existence of a small-signal positive feedback loop

In this R_o is the source output resistance of M_1 and of M_2. The loop is 'cut' at the gate of M_4 and a small positive-going test signal, v_2, applied. This causes changes v_3 and v_1 to occur in the directions indicated. It can be seen, by inspection of the circuit, that the loop-gain of the circuit is guaranteed to be less unity, with the result that parasitic oscillations cannot occur, if $R>R_o$.

4.4.3 The current-feedback configuration

This scheme is similar to that of Fig.4.12(a), in the previous section, in that a version of one of the inputs of a differential voltage drive signal appears at one end of a transconductance-determining resistor after passage through two cascaded source-followers and a similar version of the second input of the drive appears at the other end of the resistor, again after passing through two cascaded source-followers.

The difference between this and the previous scheme lies in the in the way the differential output current is obtained.

The circuit, shown schematically in Fig.4.23 [4.10], comprises two half-circuits, one each side of the line aa' bisecting the degeneration resistance R.

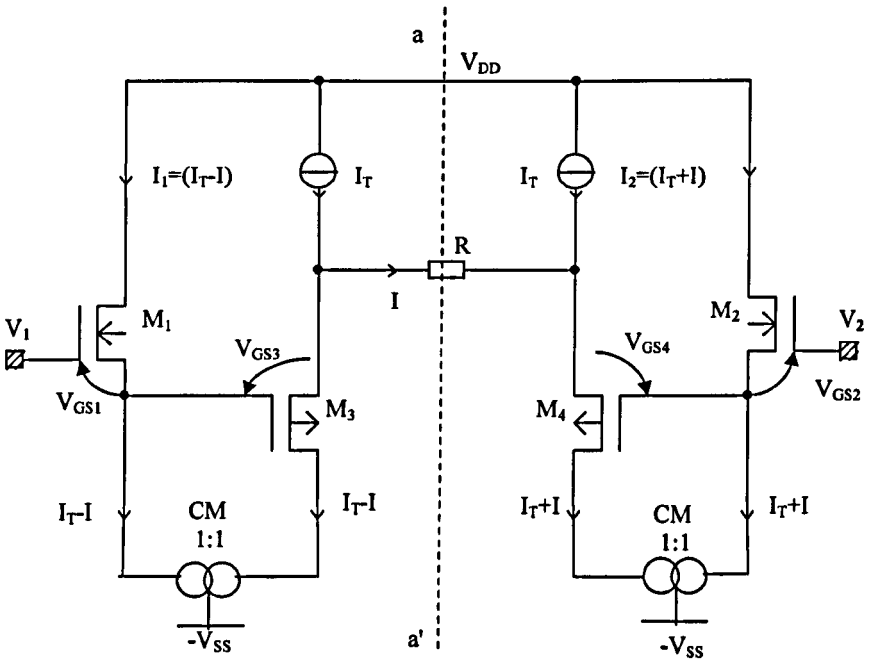


Figure 4.23 Current-feedback V-I [4.10]

A DC analysis of the circuit is given in full in Appendix 4.1 so only a brief, alternative analysis is given here.

By inspection,

$$V_1 - V_{GS1} + V_{GS3} - V_A - V_{GS4} + V_{GS2} = V_2 \qquad (4.45)$$

or, $$V_R = IR = V_D - V_{GS1} + V_{GS3} - V_{GS4} + V_{GS2} \qquad (4.46)$$

$$R = \frac{dV_D}{dI} - \frac{d}{dI}\left(V_{GS1} - V_{GS3} + V_{GS4} - V_{GS2}\right) \qquad (4.47)$$

Let us suppose we can make the bracketed term on the r.h.s of eqn.4.47 equal to zero.

This requires that, $$\frac{dV_{GS1}}{dI} - \frac{dV_{GS3}}{dI} = 0 \qquad (4.48a)$$

and, $$\frac{dV_{GS4}}{dI} - \frac{dV_{GS2}}{dI} = 0 \quad (4.48b)$$

These conditions are met if,

$$g_{m1}=g_{m3} \quad (4.49a)$$

$$g_{m2}=g_{m4} \quad (4.49b)$$

where $g_{mr}(r=1...4)$ is the transconductance of MOSFET M_r.

Now, $g_{mr} = \sqrt{2\beta_r I_r}$

So we require that,

$$\sqrt{2\beta_n(I_T - I)} = \sqrt{2\beta_p(I_T - I)} \quad (4.50a)$$

$$\sqrt{2\beta_n(I_T + I)} = \sqrt{2\beta_p(I_T + I)} \quad (4.50b)$$

Both eqn (4.55a), (4.55b) are satisfied if,

$$\beta_n = \beta_p \quad (4.51)$$

For MOSFETs with the same channel length this requires that,

$$\mu_e W_n = \mu_h W_p \quad (4.52)$$

or, $$\frac{W_p}{W_n} = \frac{\mu_e}{\mu_h} \ (>1) \quad (4.53)$$

in which μ_e, μ_h, are electron and hole nobilities in the n and p MOSFET, respectively.

When eqn (4.51) is valid,

$$G_t = \frac{d(I_2 - I_1)}{dV_D} = \frac{d(2I)}{dV_D} = \frac{2}{R} \quad (4.54)$$

The intended linear range for G_t is $I_T R$ because the condition $|I|=I_T$ means that either M_3 is cut off or M_4 is cut off.

4.4.3(a) Circuit implementation and operation

Fig.4.24 shows the circuit used in simulation tests.

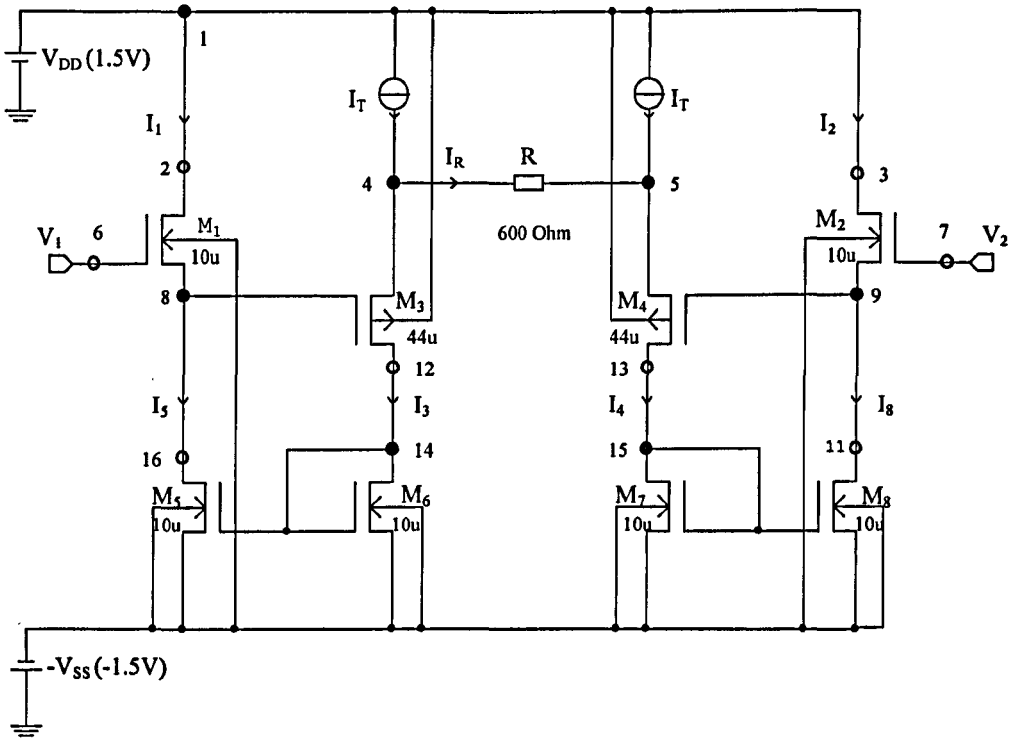


Figure 4.24 Circuit for simulation tests

From SPICE data (μ_e/μ_h) = 4.40, so W_p was made 44μ to satisfy eqn.4.53 with L_n=10μ. To achieve the desired linear range I_T was made 1mA. With V_1=V_2=0, I_5=I_6(I_1=I_2) =1.093mA, i.e. some 10% more than I_T. The reason for this small difference, with the simple 1:1 current mirrors (M_6+M_5 and M_7+M_8), is the small difference between the drain voltage of input MOSFET (-0.8607V) and the output MOSFETs (-0.6653V).

Nodal voltage traces for the condition V_6=-V_7=V_D/2 are shown in Fig.4.25, and accompanying current traces in Fig.4.26. To understand the circuit operation most easily we consider what happens to one half of the circuit (that encompassing M_1, M_3, M_6 and M_5) when V_D increases from zero: V_8 follows V_6 but the follower action is less than ideal because of the increasing inequality in the drain voltages of the current

mirror transistors M_6 and M_5. The source voltage, V_4, of M_5 attempts to followers V_8 but the follower action is poor. This is because the follower incremental load is only 300 Ω. (The mid-point of R is at signal earth for the applied input voltages) Cut-off in M_3 is accompanied by a decrease in the gate-source voltage of M_1 and the condition $I=I_T$. Subsequent increase in V_D now causes equal decreases in V_4 and V_5 since $(V_4-V_5) = I_T R = 0.6V$.

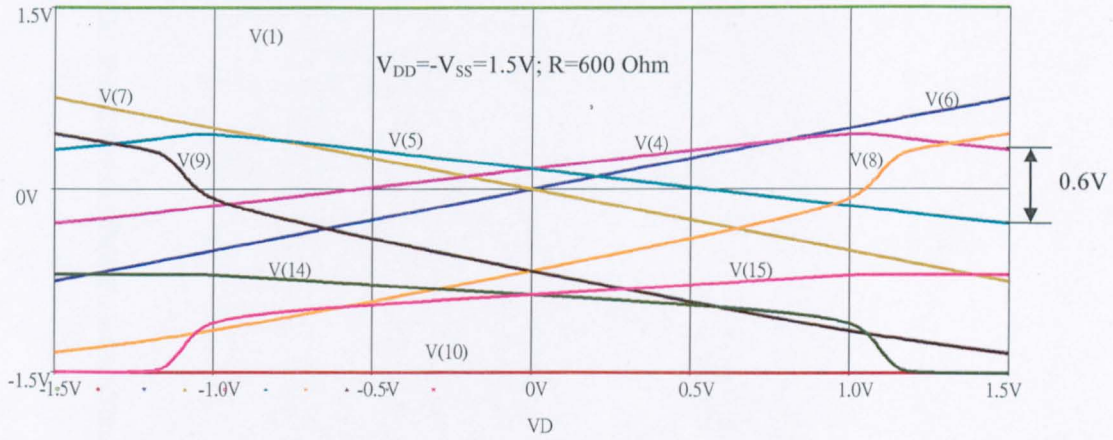


Figure 4.25 Voltage traces for Fig 4.24

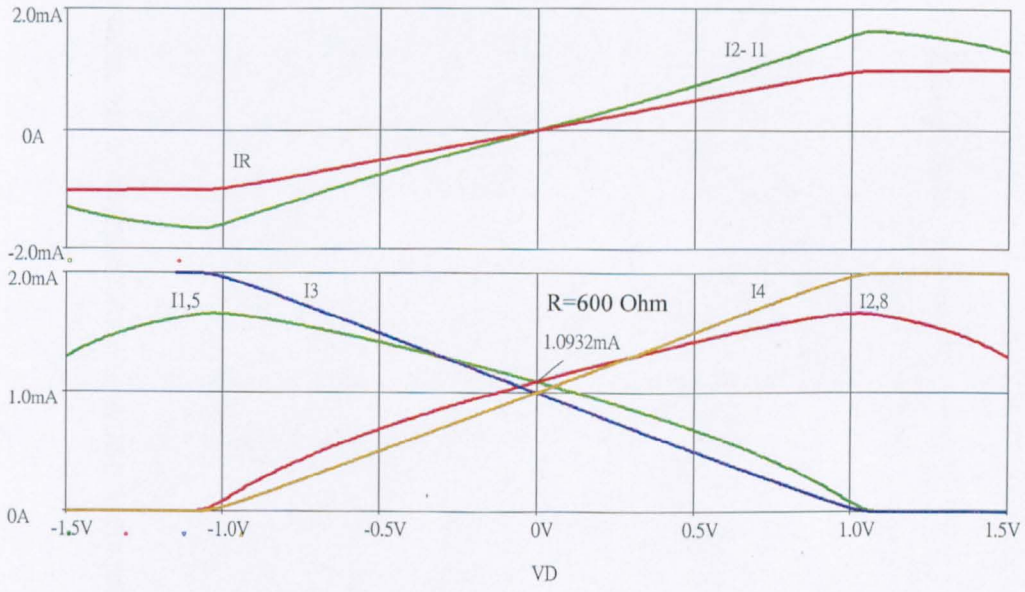


Figure 4.26 Current traces for Fig 4.24

The voltage and current traces for $V_D < 0$ are mirror images, about the axis $V_D=0$, of these for $V_D > 0$.

Application of straight edge to the graph of I in Fig.4.26 shows it to be a straight line. However, the same cannot be said for (I_2-I_1).

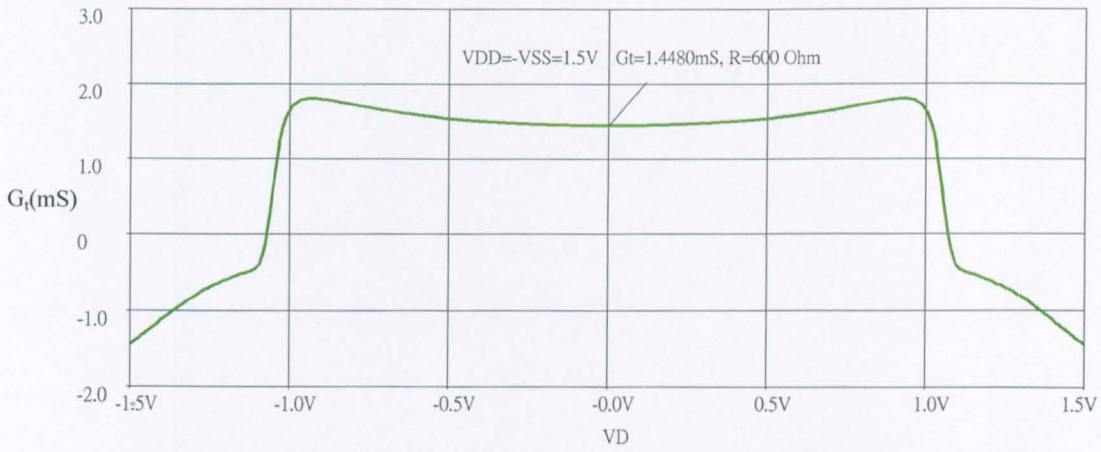


Figure 4.27 G_t characteristic for Fig 4.24

This accounts for the shoulders on the G_t characteristic of Fig.4.27. At $V_D=0$, $G_t=1.448$ which is much less than the desired value of 3.33mS.

The reason for this is the same as that for the circuit of the cross-coupled scheme of Section 4.42, i.e., limited source-follower gain.

For $1.5V > V_D > 1V$, $G_t < 0$ because of $I_1=0$ and I_2 is decreasing.

A plot of THD versus V_D for the three different input signal frequencies is shown in Fig.4.28. Spot values are given in Appendix 4.3.

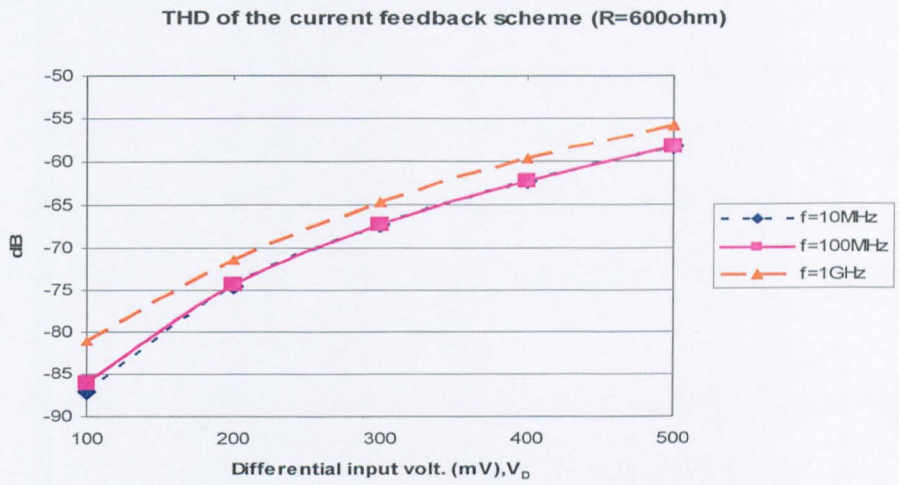


Figure 4.28 THD characteristic for Fig 4.24

Fig.4.29 shows input and output waveforms for a small-amplitude differential voltage signal at 1GHz.

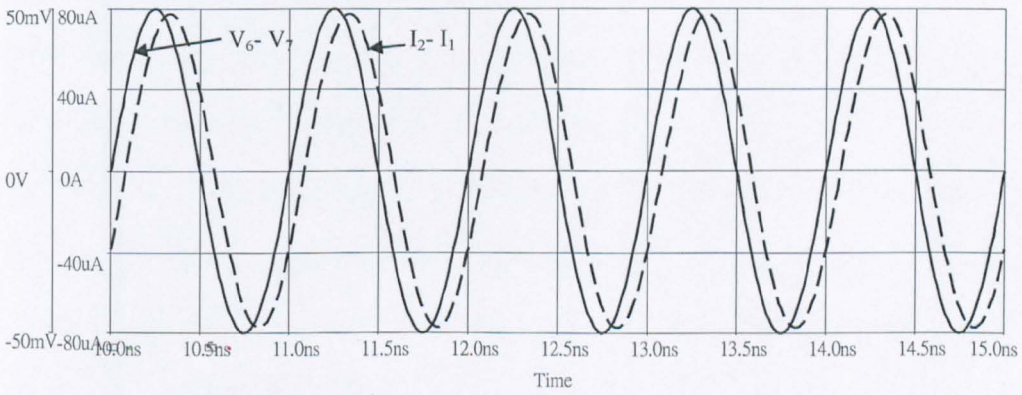


Figure 4.29 Showing differential input voltage (full line curve) and differential output current (dotted-line curve) at 1GHz

4.4.3(b) Limitations of the current-feedback scheme

The performance of the current feedback scheme is limited by: matching in the β values of n and p channel devices; source-follower gain; current-mirror performance.

Matching β values requires an accurate knowledge of the mobility ratio (μ_e/μ_h) for the n and p channel MOSFETs. For a given channel length (i.e., $L_p=L_n$) the design requires unequal channel widths ($W_p > W_n$).

Source-follower gain is less than unity, because of substrate bias, and much less unity for the p channel MOSFET because each 'sees' an incremental source load of only 300Ω for the design value of G_t.

The variable performance of the simple 1:1 current mirror used has been discussed in Chapter 3. More sophisticated mirrors require $V_{SS} > 1.5V$.

4.5 Summary and Conclusions

This chapter has reviewed, critically, two types of MOSFET V-I converter design, designated here, for convenience, Type A and Type B.

In Type A the transconductance, G_t, is determined by a chosen resistor: in Type B, G_t is set by MOSFET parameters and a chosen bias current.

Type B designs require an accurate square-law relationship between I_D and V_{GS} and close device parameter matching.

Consequently, it was decided to concentrate on Type A designs.

A number of possible circuit configurations exist, three of which were the subject of detailed analysis. Two of these, the cross-coupled scheme (based on an existing BJT circuit) and a current-feedback scheme were shown, by simulation measurements, not to produce an easily designable G_t, especially for G_t in the mS range. This was because of the relatively poor performance of the source-followers involved when working with

resistive loads necessarily less than 1KΩ, and the effect of variable source-substrate bias.

In the cross-coupled case the proposed constant range for G_t was limited by MOSFET threshold voltage.

In both the cross-coupled circuit and the current-feedback circuit an undesirable positive feedback loop existed.

It was decided to look again at the long-tailed pair stage ,with its associated degeneration resistor, to see what improvement would be made in order to obtain acceptable and predictable performance for $G_t > 1$mS.

The circuits that result from this investigation are the subject of the chapters that follow.

4.6 References

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4.7 Appendix 4

Appendix 4.1 A DC analysis of the current-feedback V-I

Ideal transconductance analysis for Fig.4.24:

$$V_1 - V_{GSN1} + V_{SGP1} - I \cdot R_E - V_{GSP2} + V_{GSN2} = V_2$$

$$\therefore V_D = (V_1 - V_2) = (V_{GSN1} - V_{GSN2}) + (V_{SGP2} - V_{SGP1}) + I \cdot R_E$$

$$I_{DS1} = \frac{\beta_N}{2} \cdot (V_{GSN1} - V_{TN1})^2 = I_{OUT1} \qquad \text{(A 4.1)}$$

$$I_{DS2} = \frac{\beta_N}{2} \cdot (V_{GSN2} - V_{TN2})^2 = I_{OUT2} \qquad \text{(A 4.2)}$$

$$\text{Where, } \beta_N = \mu_N \cdot C_{OX}\left(\frac{W_N}{L}\right) \qquad \text{(A 4.3)}$$

$$\therefore V_{GSN1} = \sqrt{\frac{2(I_T - I)}{\beta_N}} + V_{TN1}$$

$$V_{SGP1} = \sqrt{\frac{2(I_T - I)}{\beta_P}} + V_{TP1}$$

$$V_{GSN2} = \sqrt{\frac{2(I_T + I)}{\beta_N}} + V_{TN2}$$

$$V_{SGP2} = \sqrt{\frac{2(I_T + I)}{\beta_P}} + V_{TP2}$$

$$\therefore V_D = I \cdot R_E + \sqrt{\frac{2(I_T - I)}{\beta_N}} + V_{TN1} - \sqrt{\frac{2(I_T + I)}{\beta_N}} - V_{TN2} + \sqrt{\frac{2(I_T - I)}{\beta_P}} + V_{TP1} - \sqrt{\frac{2(I_T + I)}{\beta_P}} - V_{TP2}$$

(A 4.4)

where, if we use the same parameters of N channel and P channel MOSFET devices.

the equation can be simplified as:

$$V_D = I \cdot R_E + \sqrt{\frac{2(I_T - I)}{\beta_N}} - \sqrt{\frac{2(I_T + I)}{\beta_N}} + \sqrt{\frac{2(I_T - I)}{\beta_P}} - \sqrt{\frac{2(I_T + I)}{\beta_P}}$$

And if β_N and β_P are well matched, the expression shows as following:

$$V_D = I \cdot R + 0$$

$$\therefore \frac{dV_D}{dI} = R, \text{or} \frac{dI}{dV_D} = \frac{1}{R}$$

Because $I_O = I_{DS2} - I_{DS1} = (I_T + I) - (I_T - I) = 2I$

$$\text{so, } \frac{dI_O}{dV} = \frac{d(2I)}{dV_D}$$

The output transconductance is thus:

$$G_{t(ideal)} = \frac{d(2I)}{dV_D} = \frac{2}{R} \qquad \text{(A 4.5)}$$

Appendix 4.2 Data for Total Harmonic Distortion of the cross-coupled scheme

Table A 4.1 Data of Fig.4.18

Cross-coupled scheme		600 Ohm
Frequency(MHz)	Amplitude(mV)	dB
10	100	-88.5
	200	-76.9
	300	-69.5
	400	-64.1
	500	-59.6
100	100	-87.1
	200	-76.7
	300	-69.5
	400	-64.1
	500	-59.6
1000	100	-77
	200	-73
	300	-66
	400	-60.7
	500	-56.4

Appendix 4.3 Data for Total Harmonic Distortion of the current-feedback scheme

Table A 4.2 Data of Fig 4.28

Current-feedback scheme		600 Ohm
Frequency(MHz)	Amplitude(mV)	dB
10	100	-87.1
	200	-74.4
	300	-67.3
	400	-62.3
	500	-58.3
100	100	-86
	200	-74.3
	300	-67.3
	400	-62.2
	500	-58.3
1000	100	-81.1
	200	-71.3
	300	-64.6
	400	-59.7
	500	-55.8

CHAPTER 5

DESIGN OF A V-I CONVERTER USING VOLTAGE FOLLOWERS WITH DRAIN-SOURCE FEEDBACK

5.1 Introduction

Section4.41 considered the transfer characteristic of a basic long-tailed-pair V-I converter with source degeneration.

It was noted in eqn.4.28, repeated here for convenience, that the mutual conductance G_t could be written in the form,

$$G_t = \frac{2}{R + \frac{1}{g_{m1}} + \frac{1}{g_{m2}}} \qquad (5.1)$$

To achieve the ideal relationship $G_t = \frac{2}{R}$ necessitates the condition $g_{m1}=g_{m2}=\infty$.

There are two other equivalent ways of appreciating what this means. We can say that the resistance looking into the source of each MOSFET is reduced to zero, or that the gate-source voltage of each MOSFET remains constant over the operating range.

To produce an apparent increase in the g_m, of each of the MOSFETs used in a source-degenerated long-tailed pair, we can make use of experience gained with BJTs and employ a complementary Darlington-type circuit in a drain-source feedback configuration. The use of this in the design of a V-I is the subject of this chapter.

5.2 Half-circuit structure

The circuit that emerges and is the starting point in the proposed V-I design, when N channel MOSFETs are used in the long-tailed pair, is shown in Fig 5.1. In this: I_T is a constant tail current; V_{GS} is the gate-source voltage of M_A and I_D its drain current, supplied by a current source with an incremental output resistance r_{op}; I_F, the drain current of additional MOSFET, M_B, provides feedback ; and, I_L is a load current.

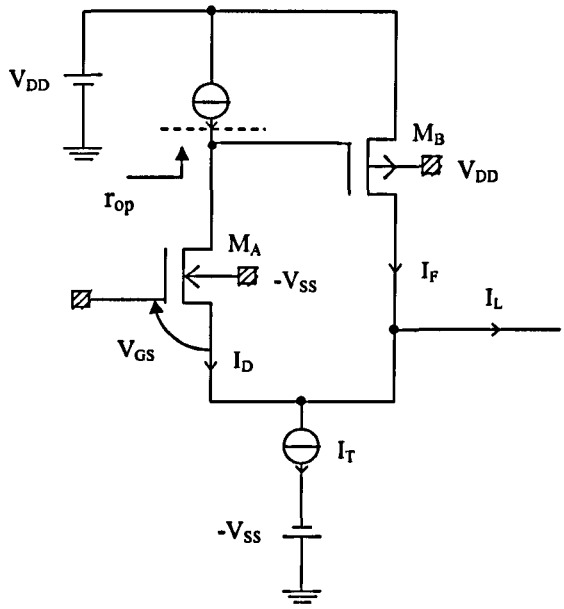


Figure 5.1 Schematic of a complementary MOSFET source-follower half-circuit

A first-order small-signal analysis, in which substrate effects and MOSFET drain-source incremental resistance are ignored, serves to highlight the essential operating mechanism of the circuit.

Suppose i_d, i_f, i_l are small changes in I_D, I_F, I_L brought about by a small change, v_{gs}, in V_{GS}.

Then, $i_d = g_{mA} v_{gs}$ (5.2)

$i_f = i_d r_{op} g_{mB}$ (5.3)

and, $i_l = i_d + i_f = g_{mA} v_{gs} [1 + g_{mB} r_{op}]$ (5.4)

where g_{mA}, g_{mB} are respectively the mutual conductances of M_A (at drain current I_D) and M_B (at the drain current I_F). In general $g_{mA} \neq g_{mB}$.

It follows from eqn (5.2) to (5.4) that the apparent mutual conductance, g_{mT}, is given by,

$$g_{mT} \stackrel{\Delta}{=} \frac{i_d}{v_{gs}} = g_{mA}\left(1 + g_{mB} r_{op}\right) \quad (5.5)$$

Furthermore, $\frac{i_d}{i_1} = \frac{1}{(1 + g_{mB} r_{op})}$ (5.6)

Hence, $g_{mT} \rightarrow \infty$ and $i_d \rightarrow 0$ as $g_{mB} r_{op} \rightarrow \infty$.

For this ideal case an equivalent representation of Fig.5.1 is shown in Fig.5.2

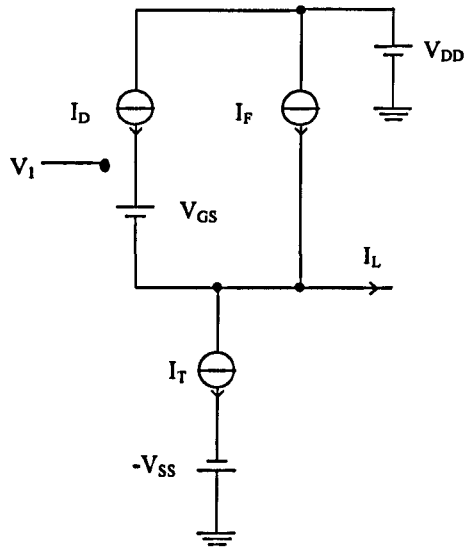


Figure 5.2 Ideal representation of circuit operation of Fig.5.1

By inspection, $I_F = I_L + (I_T - I_D)$ (5.7)

Since I_T, I_D are constant it follows that, as V_I changes,

$$\Delta I_F = \Delta I_L \quad (5.8)$$

To obtain an output current, I_O, that is linearly related to I_L we add a further MOSFET, M_C, as shown in Fig 5.3.

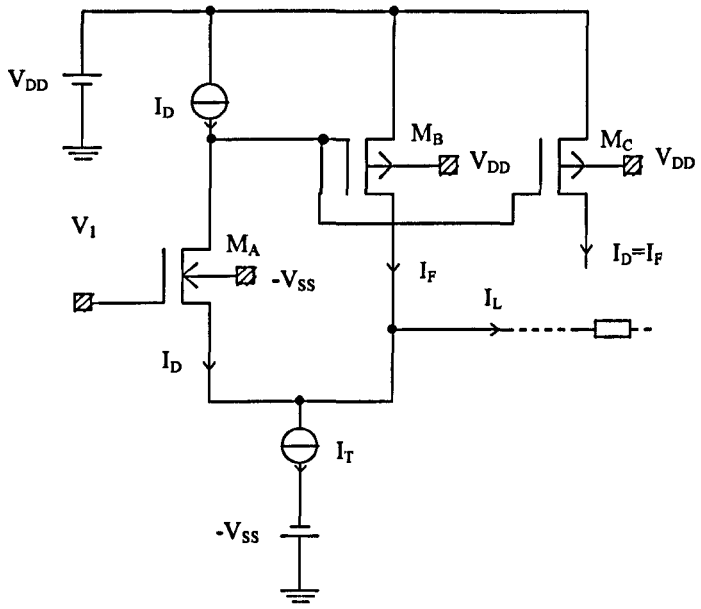


Figure 5.3 Obtaining an output current, I_O, directly related to I_L

5.3 The proposed V-I in schematic form

In a V-I intended to interface directly with a Gilbert mixer cell [5.1] using n-channel MOSFETs it is beneficial to use a complementary version of the half-circuit of Fig.5.3, as in Fig.5.4.

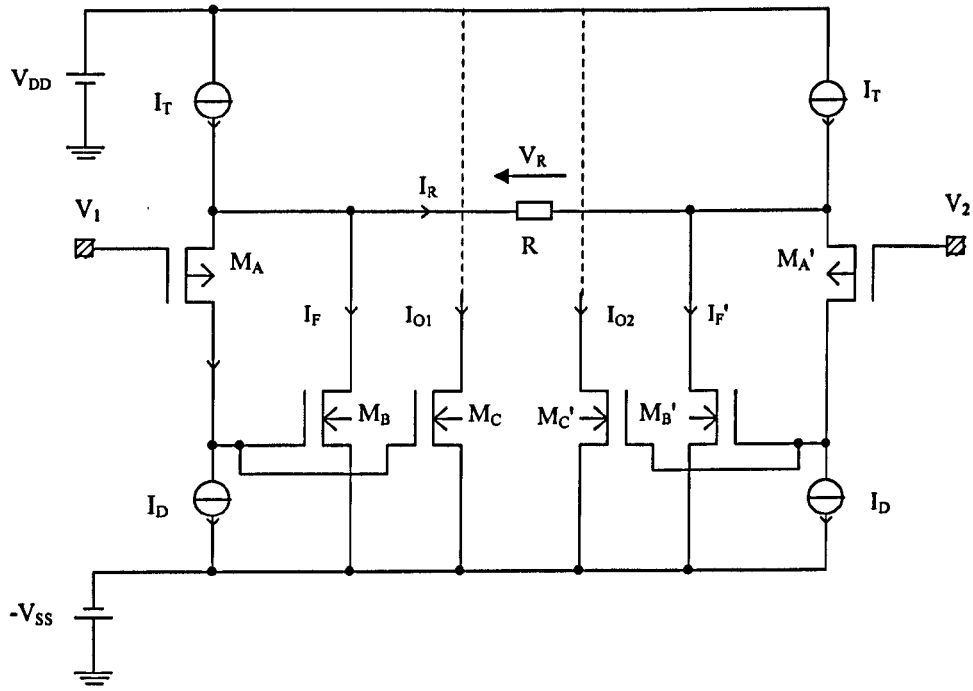


Figure 5.4 Schematic representation of proposed V-I with the condition $V_D(=V_1-V_2) > 0$

5.3.1 Ideal circuit operation

The following brief description of circuit operation assumes constancy in the drain currents of M_A and $M_{A'}$ and perfect source-follower performance, so

$V_R = (V_1-V_2) = V_D = I_R R$

For $V_D=0$ it follows that $V_R=0$, $I_R=0$, $I_{O1}=I_{O2}=I_F=I_{F'}=(I_T-I_D)$.

$I_R>0$ when $V_D>0$ and has the direction shown in Fig 5.4. Then $I_{O1}=I_F=(I_T-I_D)-I_R$, and I_R adds to the current already in $M_{B'}$, so $I_{O2}=I_{F'}=(I_T-I_D)+I_R$.

For $V_D < 0$ the roles of M_B, $M_{B'}$ are inter-changed

$$\text{Hence, } G_t = \frac{d(I_{O2}-I_{O1})}{dV_D} = \frac{2}{R} \qquad (5.9)$$

The maximum operating, V_{DM}, i.e., the input voltage range over which G_t is intended to be constant, is governed by the condition $I_F \geq 0$, or $I_{F'} \geq 0$, for which

$|I_R| = (I_T - I_D)$.

Consequently, $V_{DM} = (I_T - I_D)R$ (5.10)

Combining eqns5.9 and5.10 gives the following fundamental relationship for this type of circuit,

$$G_t \times V_{DM} = 2(I_T - I_D) \quad (5.11)$$

In the idealised description of circuit operation, just presented, M_A and $M_{A'}$ can be regarded as current-steering devices.

In practice, of course, I_D cannot be constant, though it may vary by only a small amount, because of the necessary control action that the steering process requires.

The way in which the non-ideal performance of M_A and $M_{A'}$ affects the magnitude of G_t can be calculated by analysis of the half-circuit of Fig 5.4 when loaded with a resistor R/2. This is because the mid-point of R appears at signal earth for the condition $V_1 = V_D/2$, $V_2 = -V_D/2$.

5.3.2 Calculation of non-ideal value of G_t

Fig.5.5 is a re-drawn section of that part of Fig.5.4 that involves M_A and M_B. They are labelled here M_1, M_2 and their parameters subscripted accordingly. A MOSFET corresponding to M_C does not appear on this diagram because it does not affect low-frequency calculations.

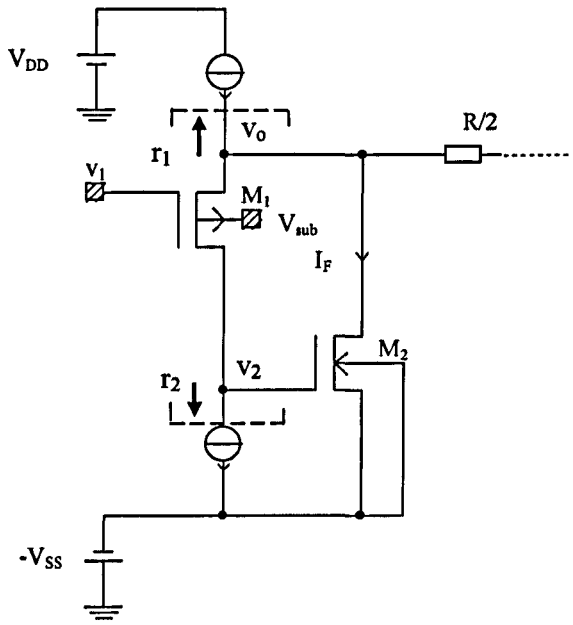


Figure 5.5 Half-circuit used in analysis

A small-signal low-frequency equivalent circuit of Fig.5.5 is shown in Fig.5.6

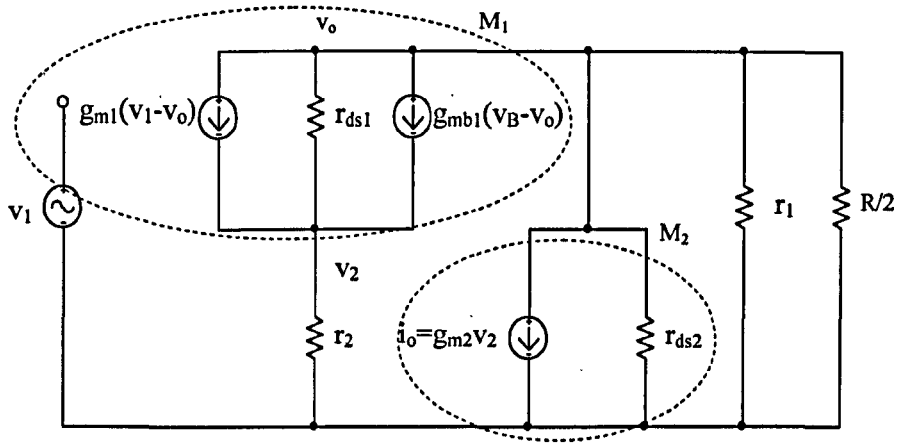


Figure 5.6 Small-signal low-frequency equivalent circuit of Fig 5.5

KCL at the source of M_1 gives,

$$v_o\left[\frac{1}{r_1}+\frac{1}{r_{ds2}}+\frac{2}{R}\right]+v_2\left[g_{m2}+\frac{1}{r_2}\right]=0 \qquad (5.12)$$

$$\text{or,} \quad v_o = \frac{-\left[g_{m2} + \frac{1}{r_2}\right] v_2}{\left[\frac{1}{r_1} + \frac{1}{r_{ds1}} + \frac{2}{R}\right]} \tag{5.13}$$

KCL at the drain of M_1 gives,

$$v_2\left[\frac{1}{r_2} + \frac{1}{r_{ds1}}\right] + g_{m1}v_1 = v_o\left[g_{m1} + g_{mb1} + \frac{1}{r_{ds1}}\right] \tag{5.14}$$

Substituting for v_o from (5.13) in (5.14), to find v_2 in terms of v_1, gives

$$v_2 = \frac{-g_{m1}v_1}{\left[\frac{1}{r_2} + \frac{1}{r_{ds1}}\right] + \frac{\left(g_{m2} + \frac{1}{r_2}\right)}{\left(\frac{1}{r_1} + \frac{1}{r_{ds}} + \frac{2}{R}\right)} \cdot \left(g_{m1} + g_{mb1} + \frac{1}{r_{ds1}}\right)} \tag{5.15}$$

Making the assumptions (later to be justified) that $r_2 >> r_{ds1}$, $1/g_{m2}$, and $(2/R) >> (1/r_1 + 1/r_{ds2})$, we find that

$$i_o = g_{m2}v_2 \cong \frac{-g_{m1}g_{m2}v_1}{\left[\frac{1}{r_{ds1}} + \frac{g_{m2}R}{2}\left(g_{m1} + g_{mb1} + \frac{1}{r_{ds1}}\right)\right]} \tag{5.16}$$

$$\text{or,} \quad i_o = \frac{-v_1}{\frac{1}{g_{m1}r_{ds1}g_{m2}} + \frac{R}{2}\left(1 + \frac{g_{mb1}}{g_{m1}} + \frac{1}{g_{m1}r_{ds1}}\right)} \tag{5.17}$$

But, $\mu_1 \overset{\Delta}{=} g_{m1}r_{ds1}$ and $\chi \overset{\Delta}{=} \frac{g_{mb1}}{g_{m1}}$

$$\text{so,} \quad i_o = \frac{-2v_1}{\frac{2}{\mu_1 g_{m2}} + R\left(1 + \chi + \frac{1}{\mu_1}\right)} \tag{5.18}$$

Now, $v_1 = v_d/2$ and $(i_{o2} - i_{o1}) = -2i_o$

$$\text{Hence,} \quad G_t = \frac{2}{R\left(1 + \chi + \frac{1}{\mu_1}\right) + \frac{2}{\mu_1 g_{m2}}} \tag{5.19}$$

For the ideal case $\chi=0$ and $\mu_1=\infty$, this reduces to eqn.5.9)

5.3.3 Design choices for a given specification

The following proposed design steps are based upon the equations of the previous section. In the design example chosen: $G_t=3.3mS$; $V_D=0.5V$.

(a) Choose $V_{DM}=0.6V$, instead of the 0.5V specified, to allow for uncertainties in (I_T-I_D) and possible ambient temperature charges.

(b) Select R for $G_t=3.3mS$ with the assumptions $\chi=0$ and $\mu_1=\infty$.

$G_t=2/R=3.33mS$, so, $R=600\ \Omega$

(c) Calculate (I_T-I_D).

From eqn (5.11), $G_t \times V_{DM}= 3.3mS \times 0.6V = 2(I_T-I_D)$

Say, $(I_T-I_D) =1mA$.

(d) Choose the ratio (I_T/I_D)

There would appear to be no obvious choice for (I_D/I_T) so a default value of unity might seem acceptable.

However, three factors which affect the choice of I_D are: the desirability of maximising μ_1 in eqn.5.19; the minimisation of circuit power dissipation; the maximisation of the frequency response of G_t.

The first two of these factors are achieved by operating with a low value for I_D, but a very low value (e.g. $1\mu A$) is undesirable because of the circuit design complexity in producing it, if large resistor values are ruled out. Furthermore, the third factor detracts from such a choice for I_D because the f_T of a MOSFET decreases with drain current.

The arbitrary, but circuit-wise convenient, choice I_D=50μA is chosen. Thus I_T=1.05mA, I_D=50μA.

If the choice of this does not give an acceptable frequency response it can be changed (Practical designs sometimes involve changed initial choices in the light of experimental results.)

5.4 Circuit implementation

There are four versions of the circuit to suit different user requirements.

The family name given here is DSFC (Drain Source Feedback Circuit) and the various versions are coded DSFC1(a), DSFC1(b), DSFC2(a), DSFC2(b).

DSFC1(a), shown in Fig.5.7 is the basic scheme and is dealt with first.

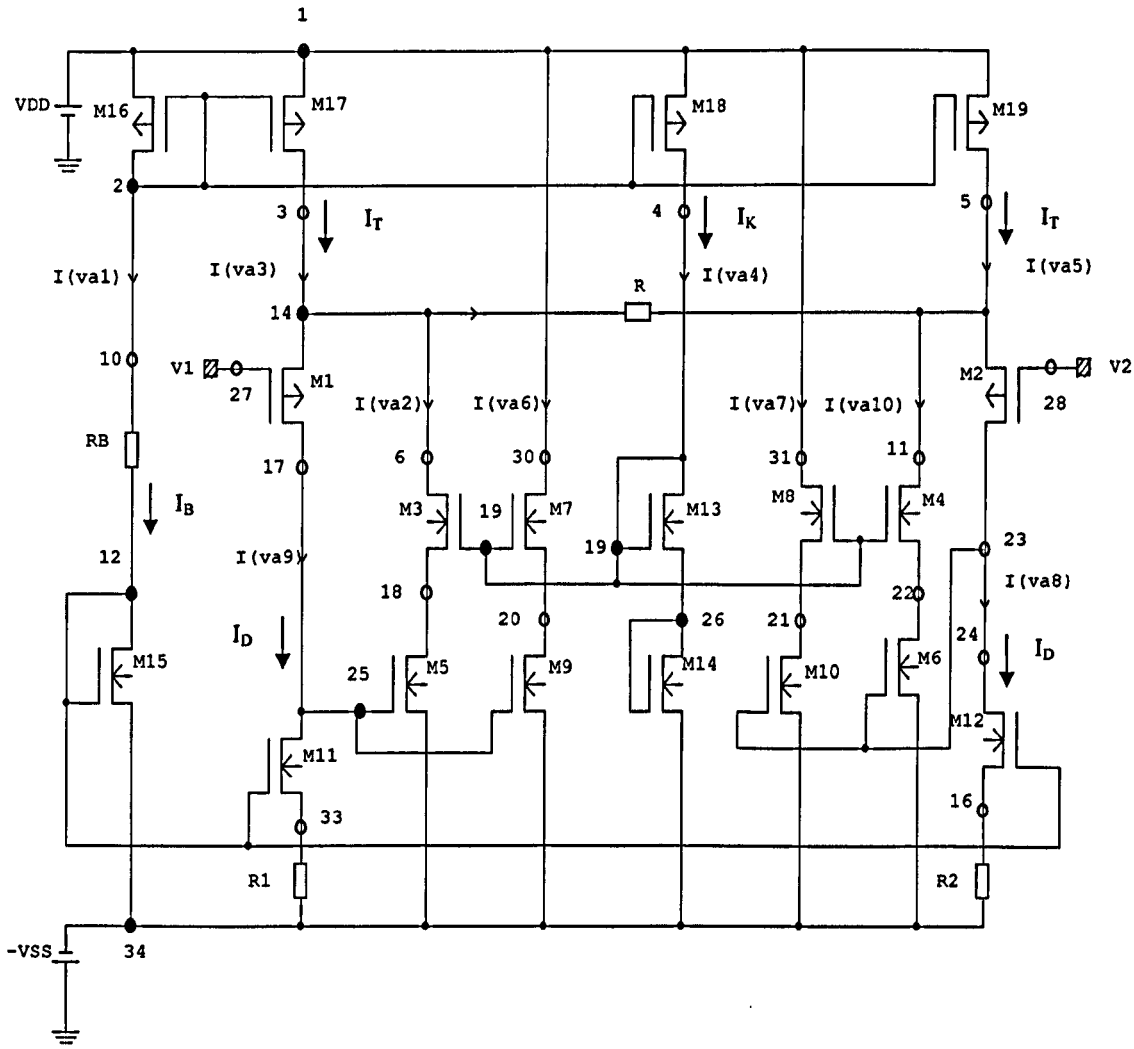


Figure 5.7 DSFC1(a) The proposed basic circuit: V_{DD}=-V_{SS}=1.5V; R=600Ω; R_1=R_2=4KΩ; I_B=1mA; I_D=50μA. Substrates are connected to the appropriate rail supplies.

R_B sets the reference bias current in the circuit at 1mA.

M_{16} is the input MOSFET of simple triple-output current mirror, supplying I_T(1mA, non-ideal) to M_1 and M_3 and a bias current, I_K (=1mA) to the series connected 'diode'-strapped MOSFETs M_{13},M_{14} the purpose of which is mentioned shortly.

M_{15} is the input MOSFET of a dual-output Widlar-type current mirror, as described in Chapter 3. The source resistors R_1, R_2, both 4KΩ, produce 50μA drain currents in M_{11} and M_{12}.

The MOSFETs M_5, M_9 in Fig.5.7 correspond, respectively, to M_B, M_C in the schematic diagram of Fig.5.4, and M_6, M_{10} correspond, respectively, to M_B', M_C'. In Fig.5.7, however, the outputs of M_5, M_9 are cascoded by M_3, M_7 and the outputs of M_6, M_{10} are cascoded by M_4, M_8.

The purpose of these cascode transistors is : to equalize the drain voltages of M_5 and M_9, and of M_6 and M_{10} so that their respective drain currents are close in value and track over the linear range as V_D changes; to produce an increased output impedance (indicating a higher r_{ds2} in Fig.5.6.

The gate voltage of the cascode transistors is set by the voltage drop across the series-connected MOSFETs, M_{13}, M_{14} which are supplied with the bias current I_K, mentioned above. I_K is chosen to be 1mA for circuit simplicity, but it could be smaller, with a consequent small saving in circuit power dissipation, at the cost of a narrower gate width for M_{18}, or the inclusion of a resistor in its source lead.

5.5 DC Conditions

The DC conditions in the circuit for $V_1=V_2=0V$ are given, for completeness, in Appendix5.1 from which it is evident that the circuit will only just work for $V_{DD}=1.5V$ and $V_{DM}/2=0.5V$ because the gates of M_{17}, M_{19} are at 0.5153V and their drains are at 0.6082V.

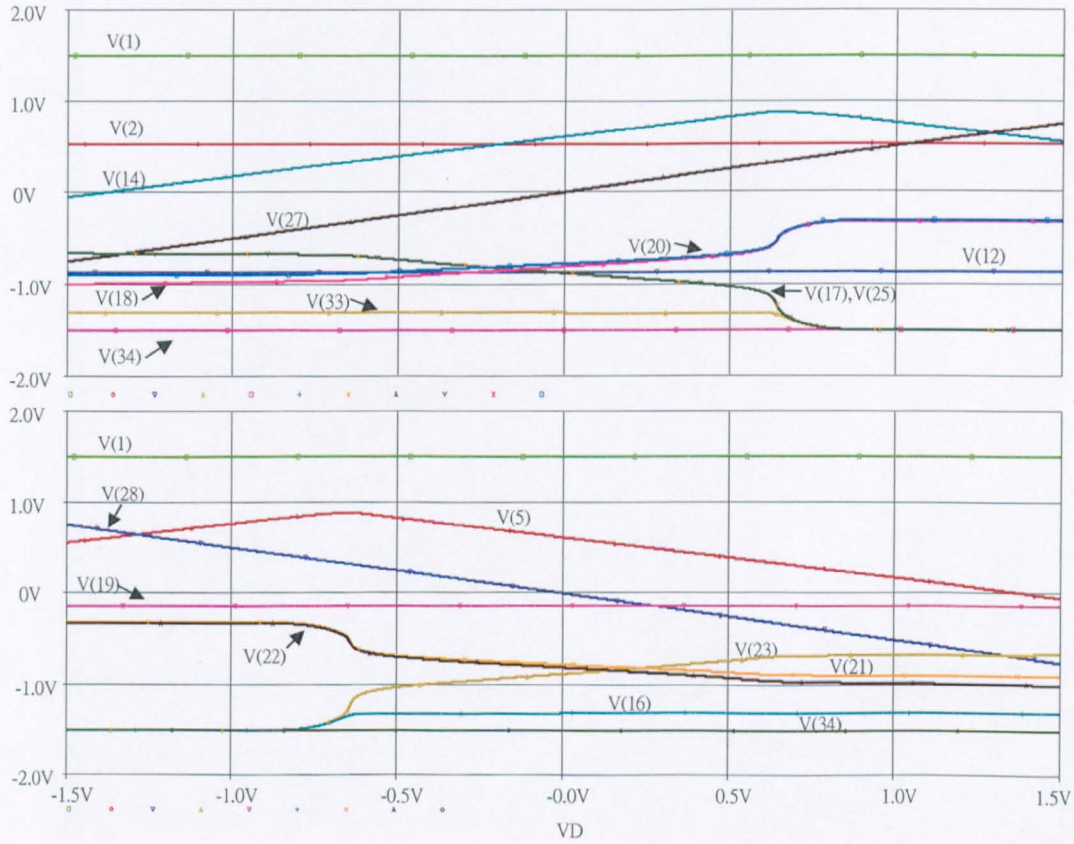


Figure 5.8 Voltage traces for DSFC1(a)

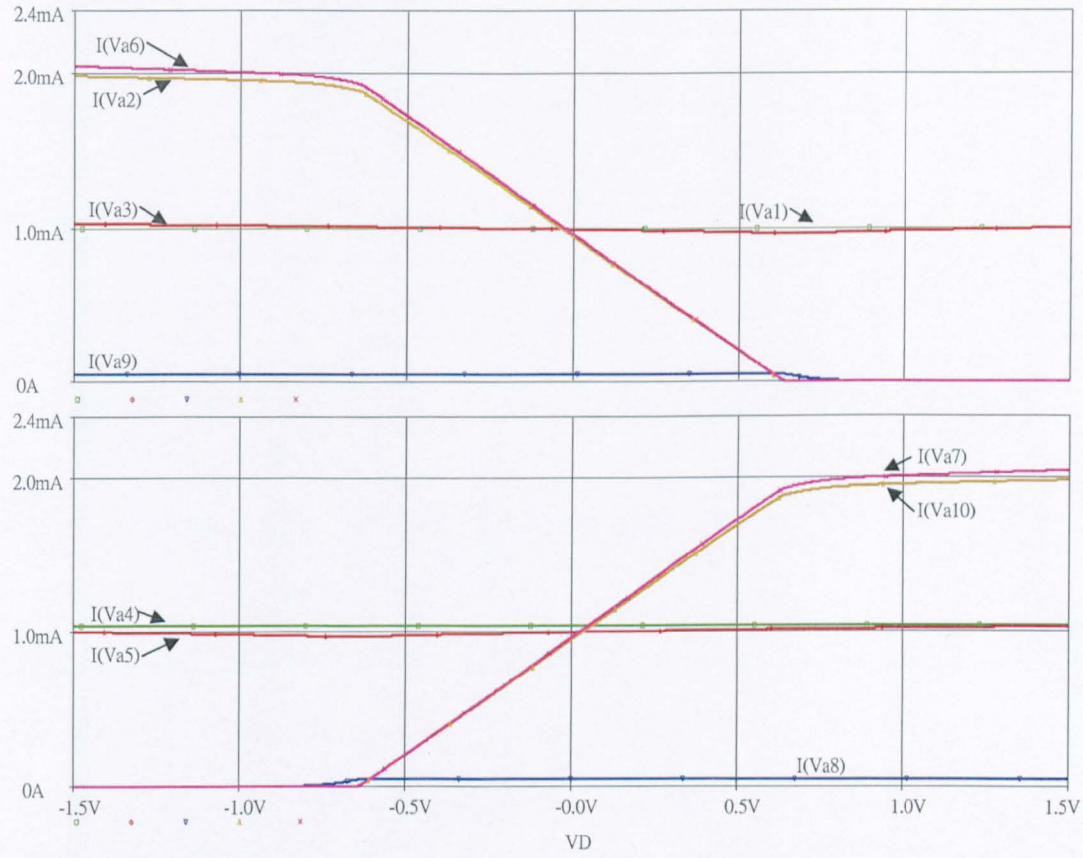


Figure 5.9 Current traces for DSFC1(a)

The voltage traces of Fig.5.8 and the current traces of Fig.5.9 illustrate circuit action when a DC sweep voltage is applied in such a way that $V_1=+V_D/2$, $V_2=-V_D/2$.

The voltage traces show good source-follower action in M_1, M_2 over the linear range but an incremental voltage gain less than unity. This is to be expected since the substrates of the transistors are not connected to their sources. The drain current of M_7 is slightly greater than that of M_3 because the drain voltage of M_7 is connected to V_{DD} for tests, and thus at a higher potential than that of M_3. Similar comments apply to the drain currents of M_8 and M_4.

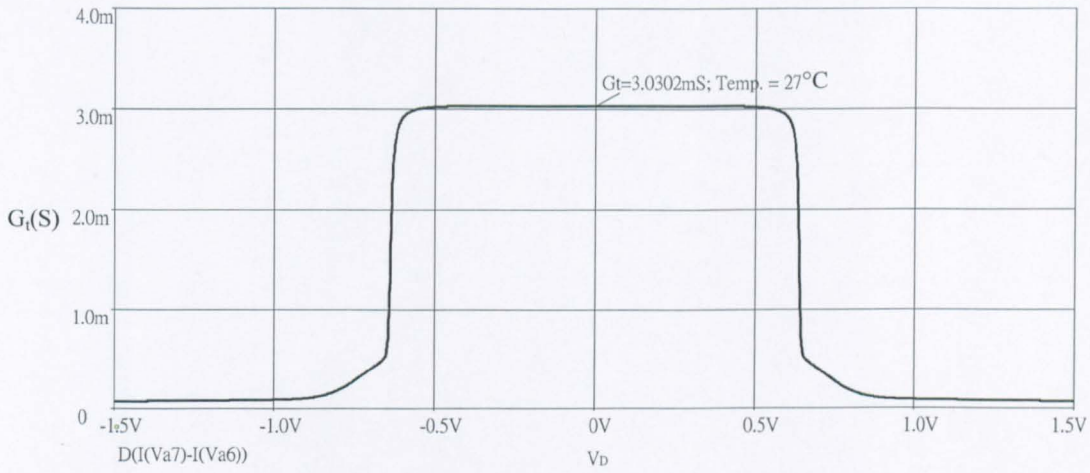


Figure 5.10 G_t vs. V_D at 27°C for DSFC1(a)

The room temperature (27°C) G_t vs. V_D plot of Fig.5.10 shows the specified linear range and a G_t, measured at V_D=0V, of 3.03mS. This is somewhat higher than the value expected for $\chi \neq 0$ (and a measured half-circuit voltage gain, on load, of 0.871) and is attributable to the greater than unity current transfer ratios of M_7, M_3 and M_8, M_4 mentioned above. G_t appears to be constant in the linear range on the scale used. It does not eventually fall to zero, in Fig.5.10, outside the linear range because of the finite output resistance of M_{17} and M_{19}. Thus, when M_1 is cut off the incremental source load for M_2 is the output resistance of M_{19} in parallel with the series combination of the output resistance of M_{17} added to R. This causes the maximum drain current of M_4, and thus M_8, to rise above the 2mA to be expected when M_{17}, M_{19} have infinite output resistances.

In circuit variation DSFC1(b), not shown, the substrates of M_1 and M_2 are connected to their sources. This makes $\chi = 0$ in eqn.5.9. The measured half-circuit voltage gain was 0.974 so G_t should be 3.243mS. The higher value shown in Fig.5.11 is, again, due to the slight greater than unity current transfer ratios of the output current mirrors.

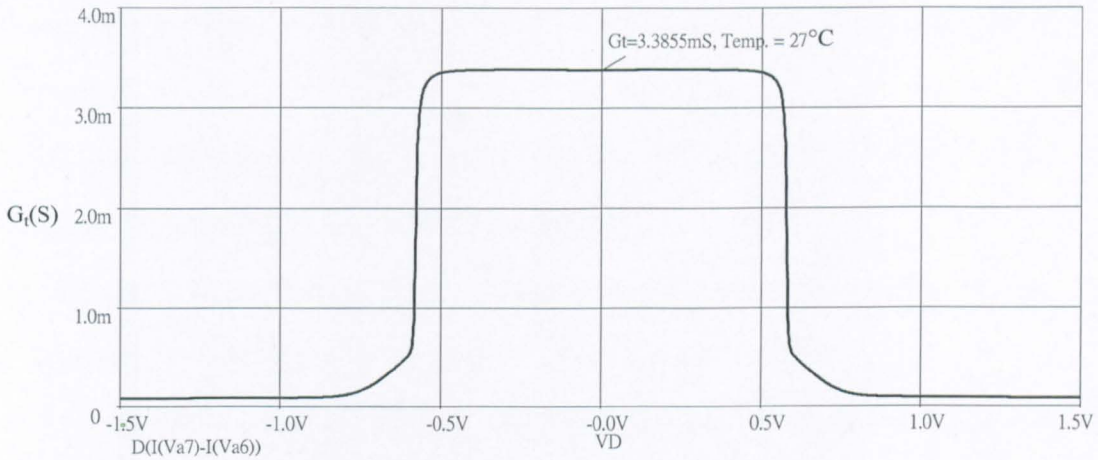


Figure 5.11 G_t vs. V_D, at 27°C, for DSFC1(b)

The variation of G_t with temperature, T, is shown in Fig.5.12

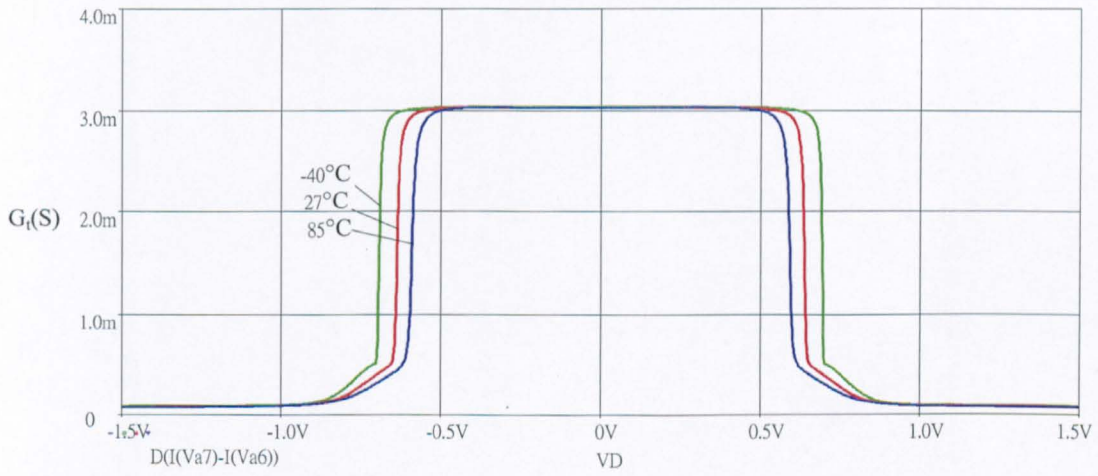


Figure 5.12 Showing the temperature-dependence of G_t

The value of G_t in the linear range is not noticeably dependent on temperature. This is to be expected since it is mainly dependent on R, which is assumed in this design to be temperature insensitive, and only marginally dependent on the temperature

variation of the parameters χ and μ in the small error terms in the denominator of eqn.5.9.

The main effect of temperature variation is to alter the width of the linear range. This comes about through change in I_T via change in I_B.

That occurs because of variation in the gate-source voltage of M_{15} and M_{16}. It was assumed that if I_B was made independent of T then so also would be V_{DM}.

To check whether this was so, simulation measurements were made on Fig.5.13. In this the currents supplying M_{15}, M_{16} do not vary with T.

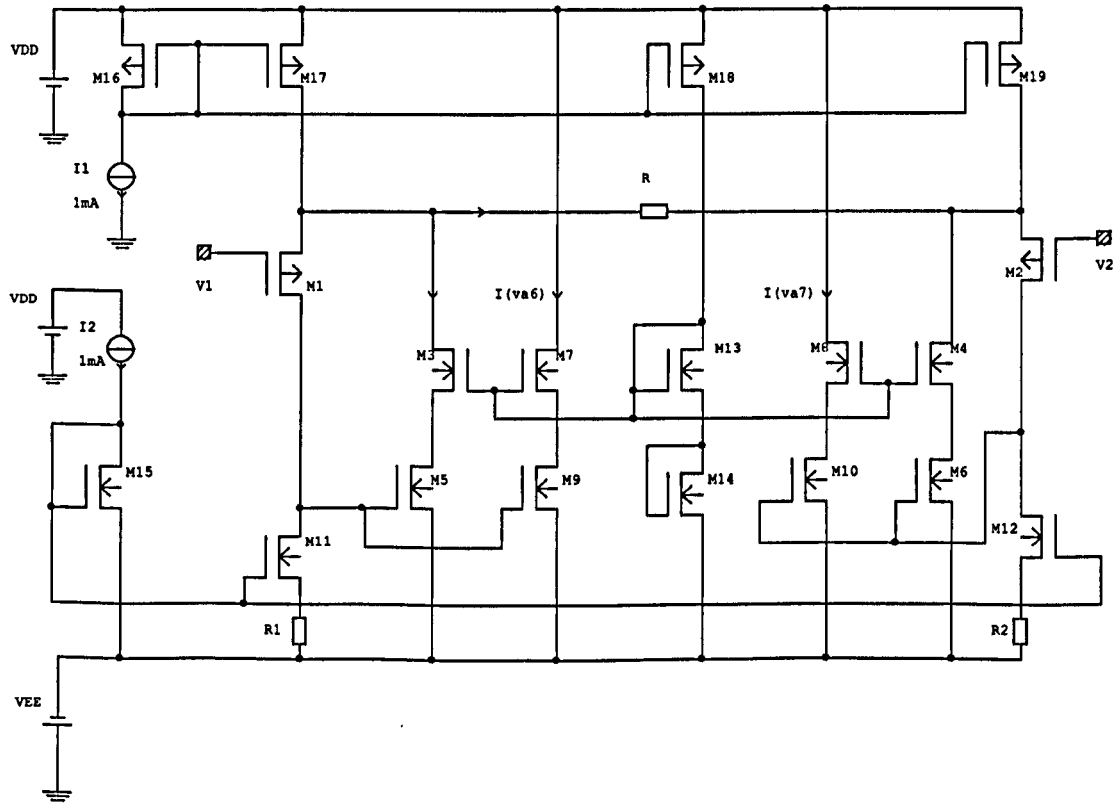


Figure 5.13 Test set-up for V_{DM} with $I_B \neq f(T)$

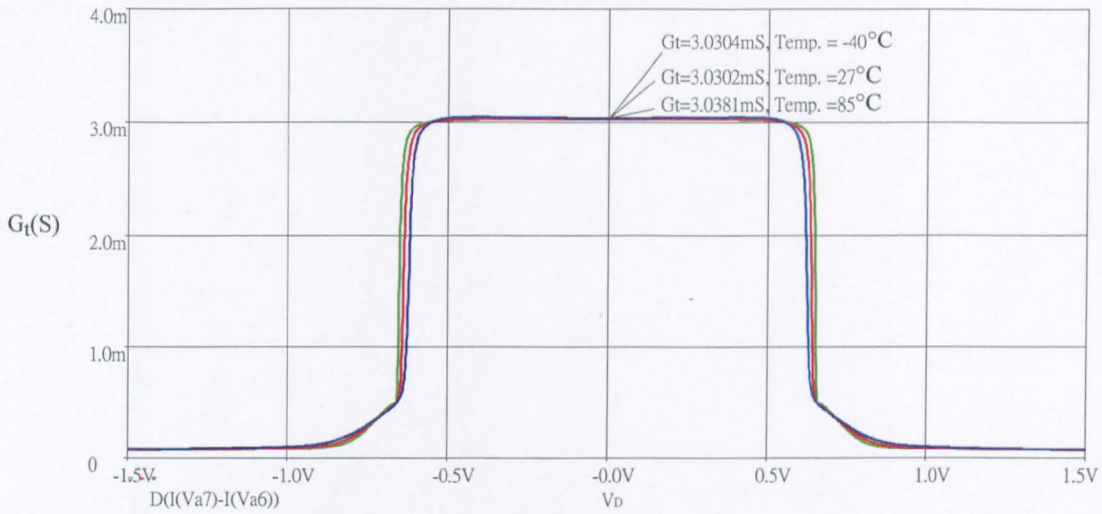


Figure 5.14 Showing G_t as a function of T for Fig 5.13

Fig.5.14 shows that perfect temperature compensation is not achieved, indicating some other factor at work. This was not investigated further, because the results of Fig.5.14 were considered to be good enough to design a practical scheme for keeping I_T constant.

In DSFC1(a), a temperature-insensitive version of DSFC1(b), R_B in Fig.5.7 is replaced by two practical current generators. One supplies a (nominally) temperature-independent current of 1mA to the drain of M_{16}; the other a complementary version of the first supplies a (nominally) temperature-independent current of 1mA to the drain of M_{15}.

The principle of operation of the current generator (see Appendix5.2) supplying current to M_{16} is made clear by the annotated voltage diagram of Fig.5.13. In this, the effects of MOSFET substrate voltage and Early voltage are ignored and the MOSFETs are assumed to operate at the same current. (i.e. $I_1=I_2$) Consequently, in a first-order calculation their gate-source voltages are identical.

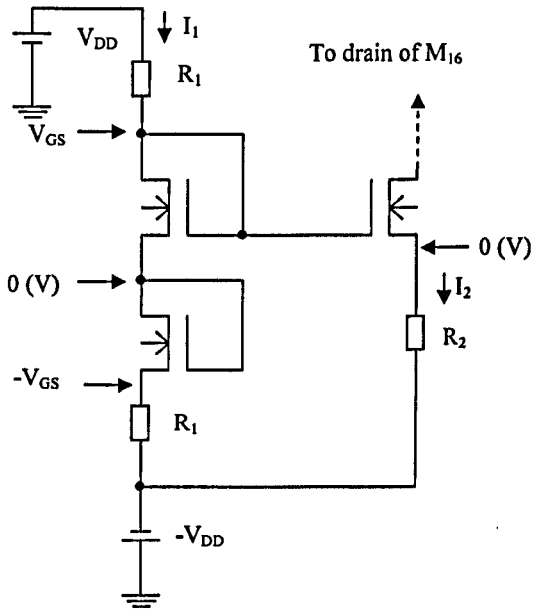


Figure 5.15 A current sink with a temperature insensitive output current, $I_2(=V_{DD}/2)$

It follows that the output current I_2 is sensibly independent of V_{GS} and hence T, as R_2 is assumed to have a zero temperature coefficient.

The design of the current source supplying the drain of M_{15} parallels that described for the current sink.

Fig 5.16 shows the full circuit of DSFC2(a)

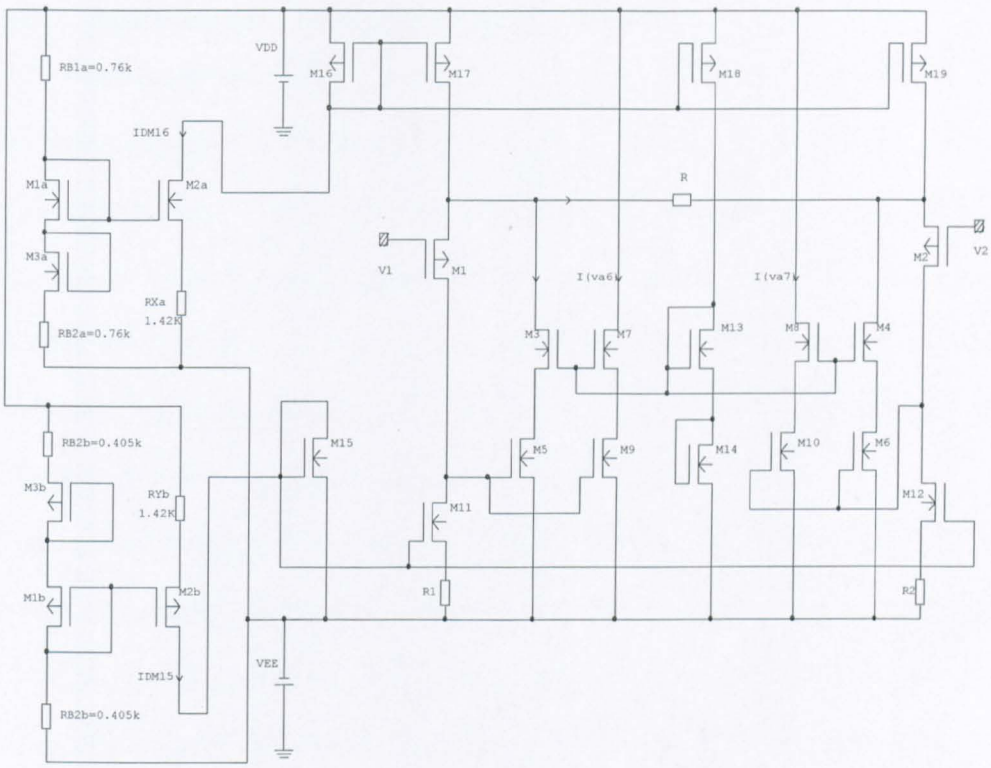


Figure 5.16 DSFC2(a), a temperature-insensitive version of DSFC1(a)

The simulated temperature variation of DSFC2(a) is shown in Fig.5.17, which is virtually identical with Fig.5.14

The DSFC2(b), not shown, is a temperature insensitive version of the DSFC1(b)

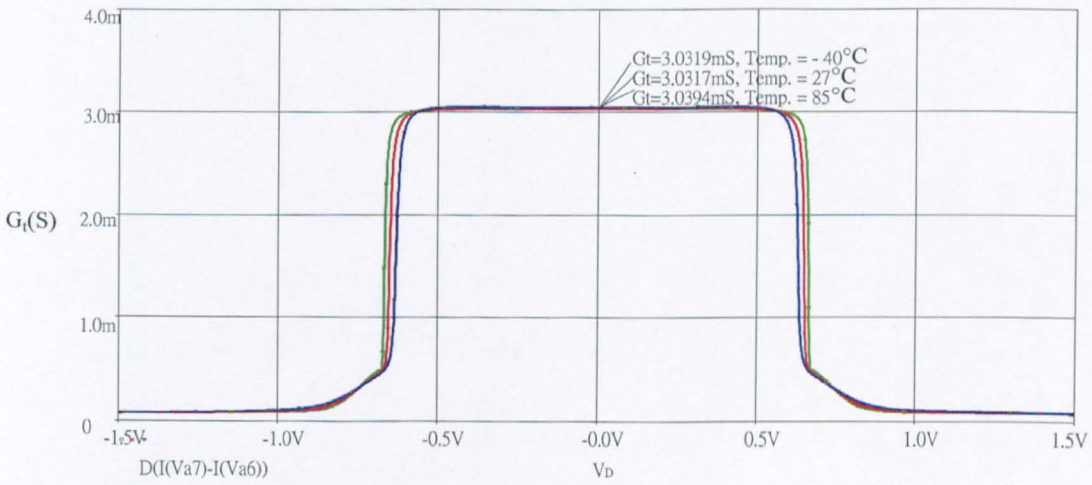


Figure 5.17 Showing the temperature-dependence of DSFC2(a)

5.6 Small-signal high-frequency performance

The small-signal frequency response of G_t, for the DSFC, is dependent on the frequency response of each half-circuit since R is considered to be purely resistive. Theoretically, this can be found by replacing each resistance in eqn.5.15 by an impedance comprising the resistance itself in parallel with an associated capacitance. Considering the number of resistors involved this produces an expression which tends to obscure physical insight into the operating mechanism, so a different approach was adopted, viz., establishing the existence of a dominant pole.

Thus in the left-hand half-circuit of Fig.5.7 the choice I_D=50μA, and the design of the Widlar-type current-mirror to produce it, guarantees that the largest incremental circuit resistance, R_T say, exists at the gate terminal of M_5. This is also the terminal where the greatest capacitance C_T exists since $C_T=(C_{gd1}+2V_{gs5}+4C_{gd5})$, where the number subscripts referring to the transistor numbers and the factor 4 arises because the 'Miller-multiplication' of the C_{gd} of both M_5 and M_9.

Consequently, C_TR_T represents the dominant time constant in the circuit.

To investigate the matter further and check for loop stability, the circuit arrangement of Fig.5.18 was used in simulation measurements.

In this, R_D(300Ω) and C_D (=10F) provide a load which is effectively resistive for $\omega >> 1/R_DC_D$.

A small constant amplitude a.c. current of variable frequency is applied at the source terminal of M_1 and gives rise to a source current I_{s1}. This is amplified by M_5, which produces a drain current I_{d5} that is fed back to the source of M_1.

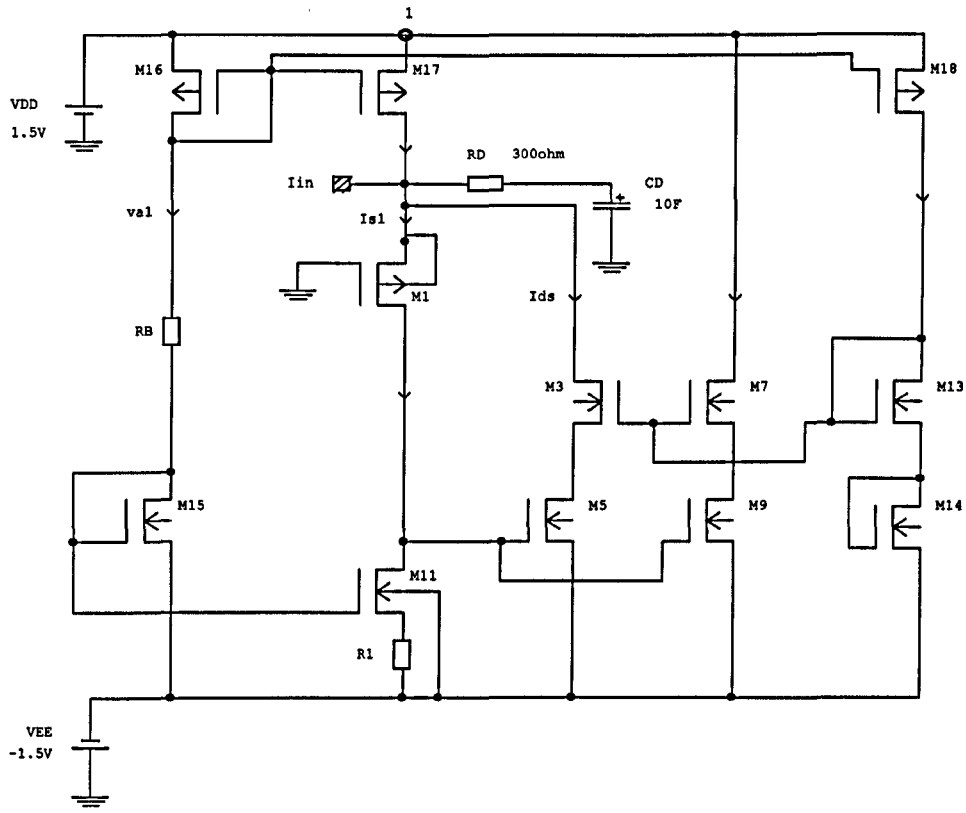


Figure 5.18 Measurement of current loop gain (I_{d5}/I_{s1}) for a half-circuit

A plot of loop gain (I_{ds}/I_{s1}) is shown in Fig.5.19, from which it is evident that the loop is stable.

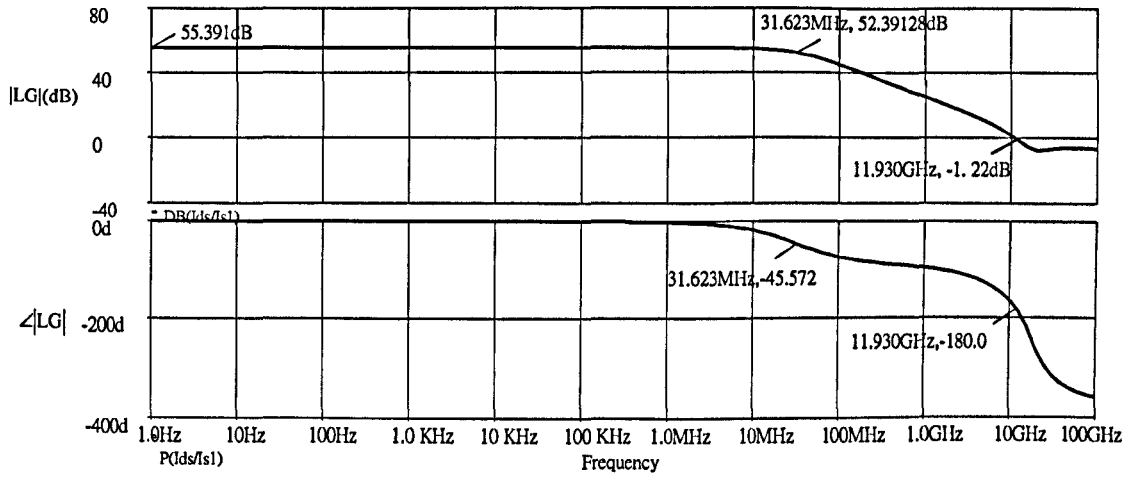


Figure 5.19 Current loop-gain (I_{d5}/I_{s1}) of half-circuit (a)Magnitude ;(b) Phase

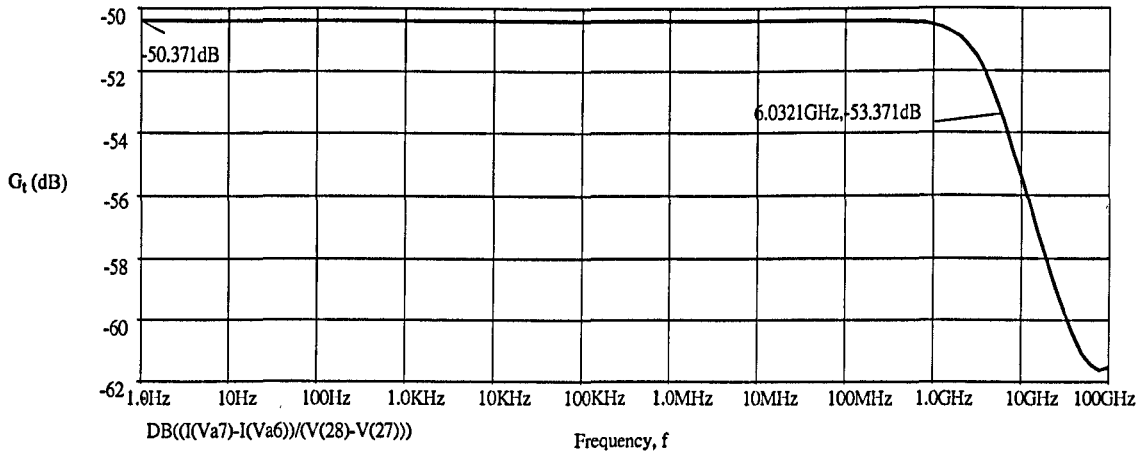


Figure 5.20 G_t vs. f for the DSFC

The resultant frequency response for G_t of the DSFC is shown in Fig.5.20, which indicates a bandwidth exceeding 6GHz.

5.7 Distortion

A plot of the THD versus V_D for three different input frequencies is shown in Fig.5.21

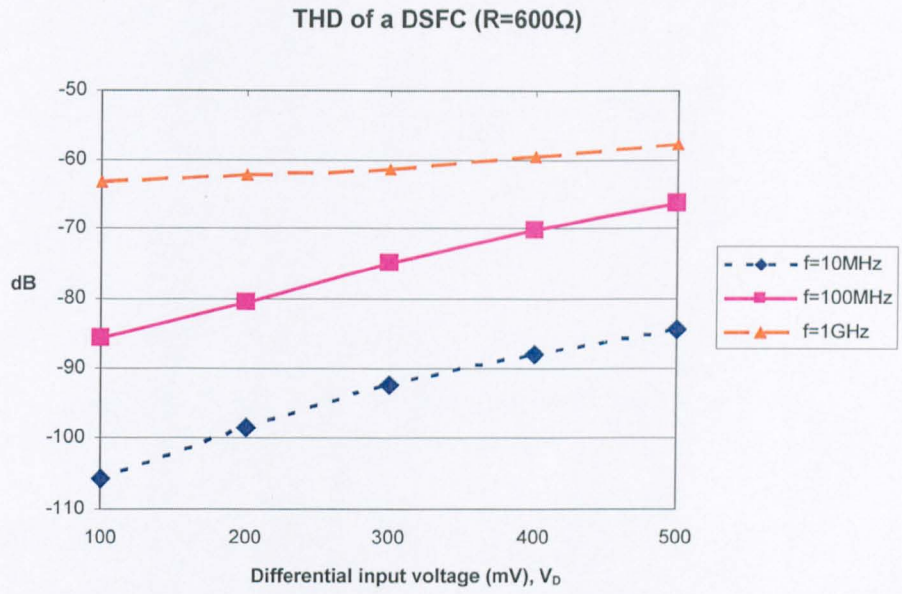


Figure 5.21 THD vs. V_D for a DSFC

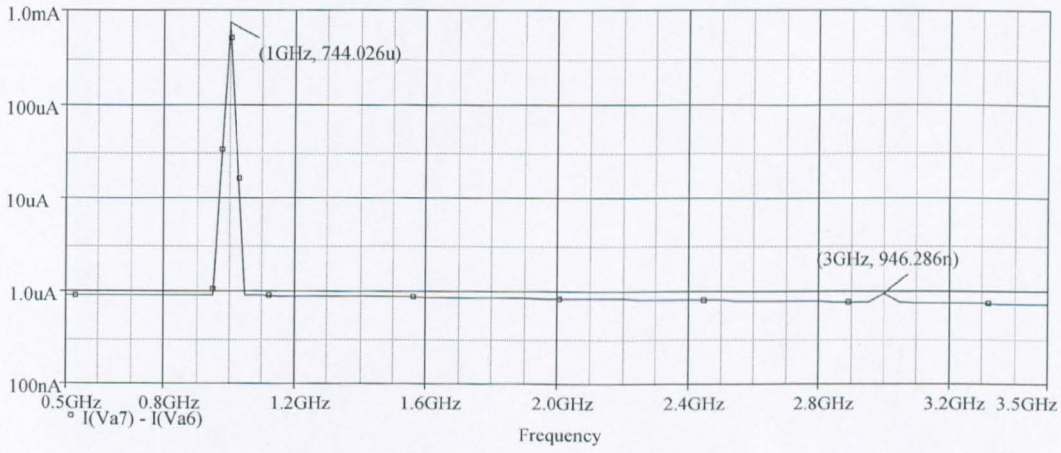


Figure 5.22 Output frequency Spectrum at 1GHz. (500mVp-p input signal.)

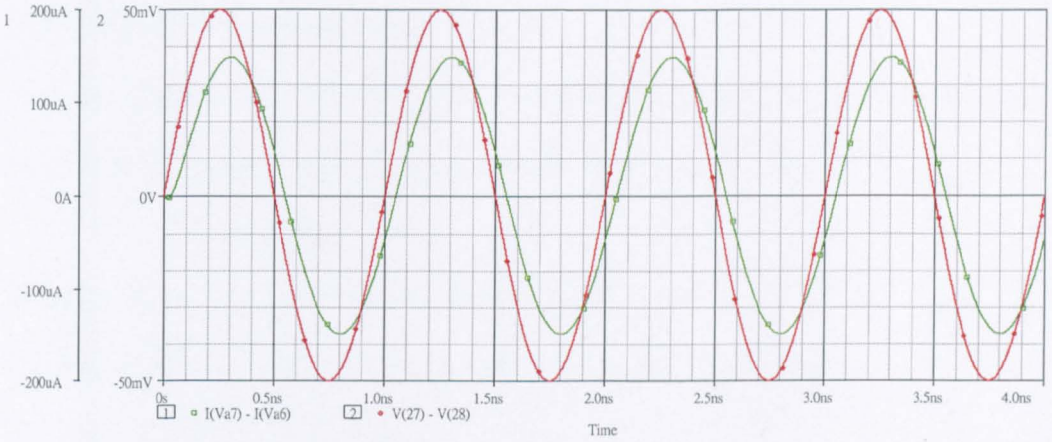


Figure 5.23 Upper curve shows a 1GHz differential input voltage signal. Lower curve shows the resulting differential output current.

Fig.5.22 indicates that for a 500mV, 1GHz, input voltage signal there is a third harmonic component of output current of amplitude 946.286nA.

Now the spot figure for THD for this input signal is -57.84dB [See Appendix5.3] corresponding to 0.128%. If this were only due to third harmonic distortion the third harmonic component would be 952.35nA. Comparing the two figures shows that third harmonic distortion dominates the THD figure.

An impression of the quality of the output signal current for a 1GHz input signal is conveyed by the waveform in Fig.5.23.

5.8 Terminal impedances

With reference to Fig.5.7, in the linear operating region the impedance looking into the gate of M_1 is expected to be solely attributable to the input capacitance C_I.

$$C_I = C_{gd1} + C_{gs1}(1 - A_V) \qquad (5.20)$$

where A_V is the source-follower incremental voltage gain.

Since $A_V \approx 0.9$ (for the substrate of M_1 connected to V_{DD}) it follows that

$$C_I \approx C_{gd1} + 0.1C_{gs1}$$

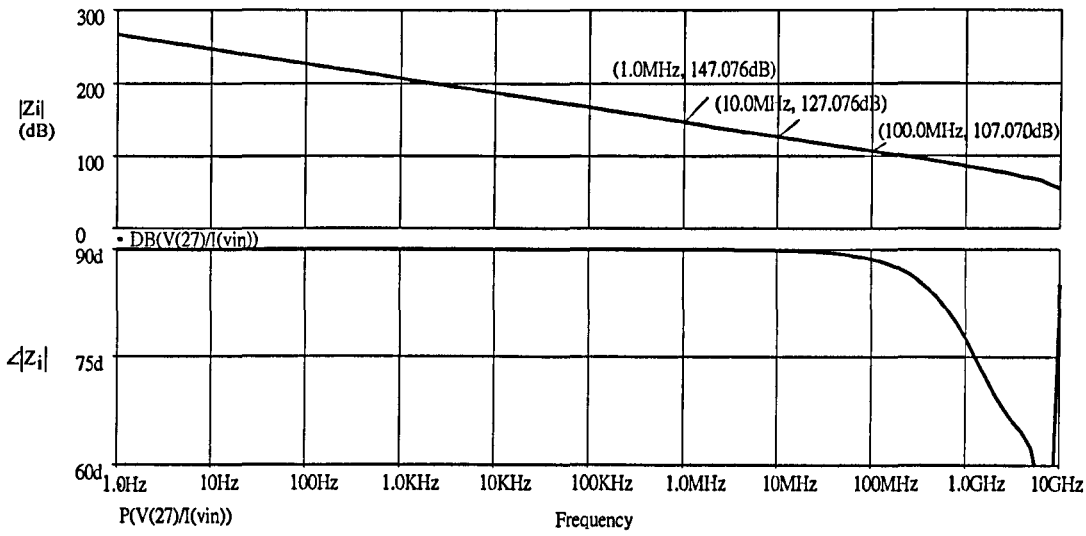


Figure 5.24 Showing the impedance looking into the gate of M_1 in Fig 5.7: (a) Magnitude; (b) Phase

From the simulation measurements in Fig.5.24, C_I is calculated to be 7.05fF which is close to the expected value. This is also, of course, the capacitance looking into the gate of M_2.

The output impedance seen looking into the drain of M_7 and M_8, of Fig.5.7, with the input terminals of the DSFC earthed, is shown in magnitude and phase in Fig.5.25.

From this it appears that the output impedance can be represented by an incremental resistance to earth of 76KΩ in parallel with a capacitance of 6.8fF. These figures agree with what was found for a cascode output stage in Chapter 3.

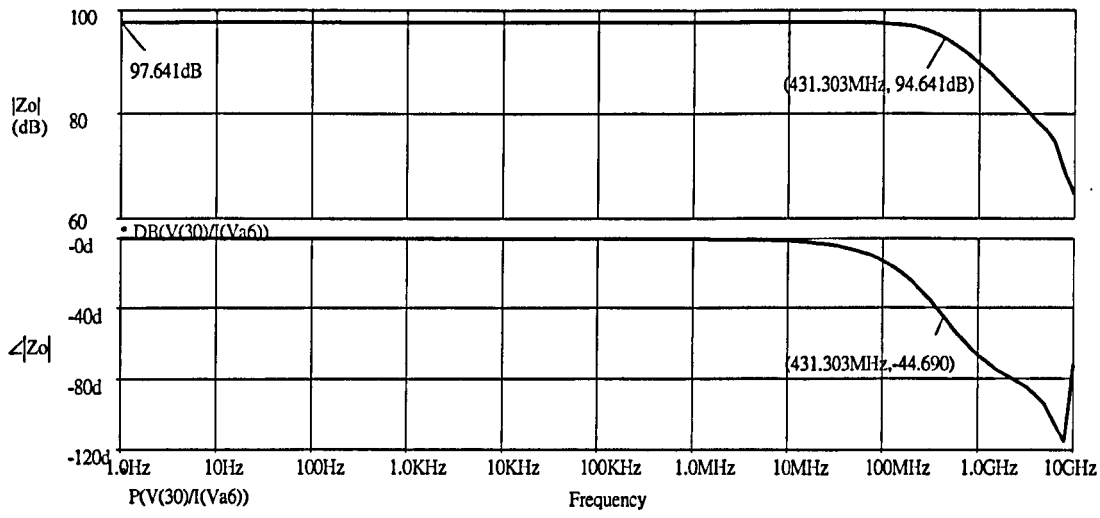


Figure 5.25 DSFC output impedance (at the drains of M_7 and M_8)

5.9 Summary and Conclusions

In this chapter an analysis of the operation of a MOSFET DSFC V-I converter has been presented and a proposed design procedure has shown that a given specification regarding transconductance can be met.

The converter comprises a resistor-linked pair of half-circuits using drain-source feedback. This half-circuit structure has been called a Super Source-Follower [5.2], though it is more simply regarded as a complementary source-follower, analogous to its historical cousin the complementary emitter-follower.

A fundamental relationship was shown to exist between the transconductance, G_t, and the maximum input voltage range over which G_t is intended to be constant: thus, $G_t \times V_D(max)=2(I_T-I_D)$, in which I_T,I_D are design-selectable DC bias currents, I_D being the operating current of the input MOSFETs.

A novel temperature compensation scheme has been proposed which makes $V_D(max)$ temperature-insensitive.

Two topics which were not pursued further but deserve investigation in the future are: the optimisation of the ratio (I_D/I_T) for a given (I_T-I_D); the development of a sub-circuit that avoids the need for close matching in the grounded-source transistors in the cascode feedback and output stages.

With regard to the latter, the basis of a possible scheme has been proposed in a paper by Acosta, Carvajal and Jimenez [5.3]. Working independently, and at the same time as the author of this thesis, they managed to obtain prior publication.

The configuration they proposed for avoiding close MOSFET matching, mentioned above, used a long-tailed pair as a unity-gain current transfer stage.

A modified version of the left-hand half-circuit of Fig.5.7 that incorporates the idea is shown Fig.5.26

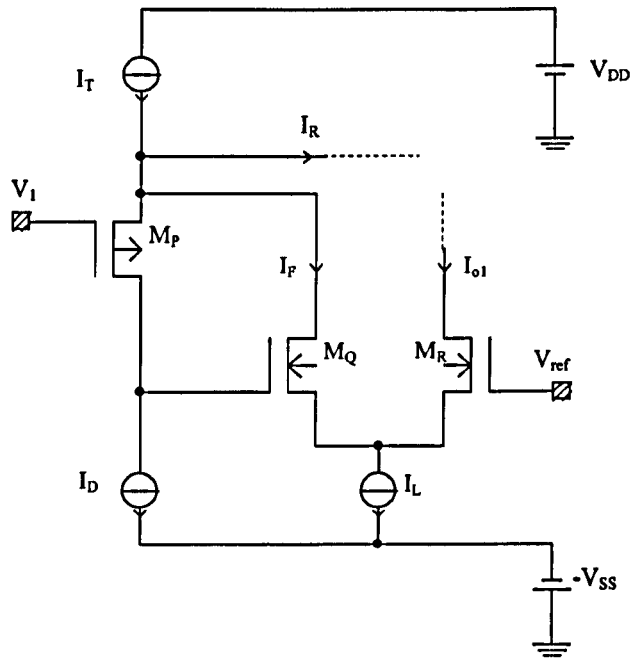


Figure 5.26 Modified version of the left-hand half-circuit of Fig 5.4

Poor matching in the gate widths of M_Q and M_R only affects circuit DC offset because if the current sink I_L, normally equal to $2(I_T-I_D)$, is perfect then $|\Delta I_{O1}|=|\Delta I_F|=|\Delta I_R|$. However, I_L is for from ideal in practice. The simplest current sink, with I_L in the mA range, is the output of a current mirror, the incremental output of which is using in the low KΩ region. A higher output resistance is obviously possible using a current mirror with a cascode output stage but the problem then is that the sum of three vertically stacked gate-source voltage drops (M_Q plus cascoded transistors) rules out operation with V_{SS}=1.5V.

There is yet another problem in that the drain voltages of M_Q, M_R are unequal. If M_Q, M_R are cascoded then V_{SS} has to be even greater for the cascode transistors to operate in saturation.

5.10 References

[5.1] Gilbert B., 'The micromixer: A Highly Linear Variant of the Gilbert Mixer Using a Bisymmetric Class-AB Input Stage', IEEE J. Solid State Circuit, Vol.32, No.9, Sept. 1997, pp. 1412-1423

[5.2] Gray P. R., Hurst P. J., Lewis S. H. and Meyer R. G., 'Analysis and Design of Analog Integrated Circuits', John Wiley & Sons, Inc., Fourth Edition, New York, 2001, pp. 213-215

[5.3] Acosta L., Carvajal G. and Jimenez M., 'A CMOS Transconductor with 90dB SFDR Low Sensitively to Mismatch', Circuit and System, 2006 ISCAS, pp.69-72

5.11 Appendix 5

Appendix 5.1 DC Conditions (for the DSFC with both inputs earthed).

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	1.5000	(2)	.5153	(3)	.6085	(4)	-.1401
(5)	.6085	(6)	.6085	(10)	.5153	(11)	.6085
(12)	-.8607	(14)	.6085	(15)	.6085	(16)	-1.3069
(17)	-.8744	(18)	-.8036	(19)	-.1401	(20)	-.7730
(21)	-.7730	(22)	-.8036	(23)	-.8744	(24)	-.8744
(25)	-.8744	(26)	-.8552	(27)	0.0000	(28)	0.0000
(30)	1.5000	(31)	1.5000	(33)	-1.3069	(34)	-1.5000
(100)	0.0000	(101)	0.0000				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VD	0.000E+00
Vcm	0.000E+00
VDD	-5.941E-03
Vss	5.941E-03
Va1	1.000E-03
Va2	9.452E-04
Va3	9.935E-04
Va4	1.035E-03
Va5	9.935E-04
Va6	9.593E-04
Va7	9.593E-04
Va8	4.828E-05
Va9	4.828E-05
Va10	9.452E-04

Appendix 5.2 Theory of the temperature compensation scheme

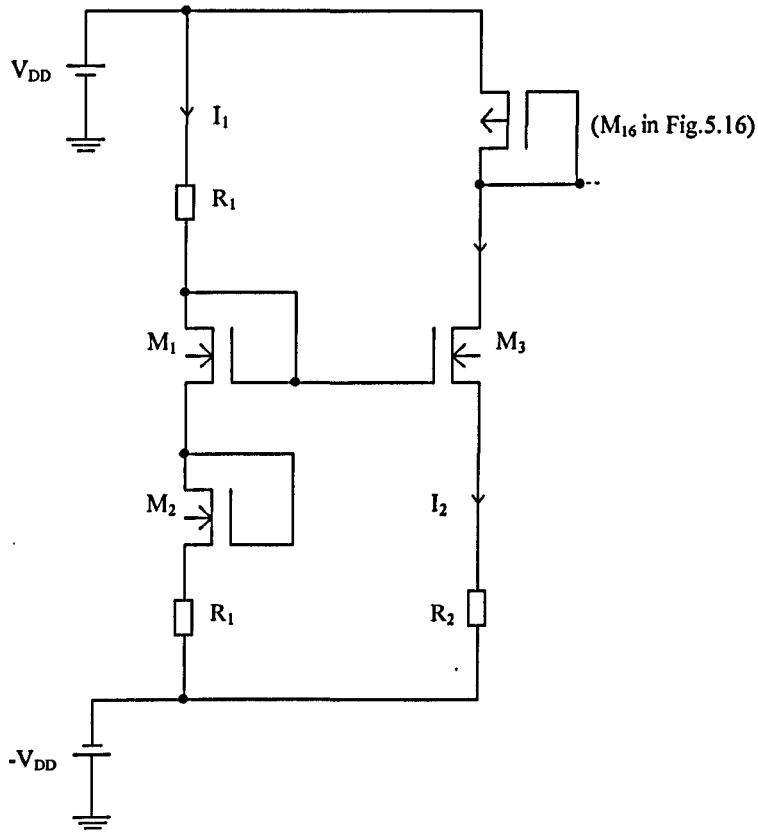


Figure A 5.1 N channel MOSFET temperature compensation scheme

$$I_1 = \frac{2V_{DD} - V_{GS1} - V_{GS2}}{2R_1} = \frac{V_{DD}}{R} - \frac{(V_{GS1} + V_{GS2})}{2R}$$

$V_{GS1}=V_{GS2}$ if M_1, M_2 work at the same I_D

$$\therefore I_1 = \frac{V_{DD} - V_{GS1}}{R_1}$$

The voltage at the gate of M3 is

$-V_{DD}+R_1I+2V_{GS1}$

$=-V_{DD}+V_{DD}-V_{GS1}+2V_{GS1}$

$= +V_{GS1}$

The voltage at source of M_3 is $V_{GS1}-V_{GS3}$. Now if $I_2=I_1$, then $V_{GS3}=V_{GS1}$

The voltage at the source of M_3 is zero (i.e. earth potential) and remains so as V_{GS} varies with temp.

$\therefore$ P.D. across R_2 is V_{DD} and the current in it is $V_{DD}/R_2 \neq f(T)$.

This analysis is only approximate because $V_{G1} \neq V_{G2}$ because of different substrate-source voltages (which affect threshold voltage). Similarly $V_{G3} \neq V_{G1}$, again because of different substrate-source voltages.

Similar considerations apply to the P channel section of the compensation scheme.

Appendix 5.3 THD data: spot figures

Table A 5.1 Spot figures of Fig.5.21

Drain Source Feedback Circuit		R=600 Ohm
Frequency(MHz)	Amplitude(mV)	dB
10	100	-105.48
	200	-98.24
	300	-92.42
	400	-87.92
	500	-84.31
100	100	-85.77
	200	-80.52
	300	-74.94
	400	-70.19
	500	-66.2
1000	100	-63.08
	200	-62.25
	300	-61.36
	400	-59.58
	500	-57.84

CHAPTER 6

DESIGN OF A V-I CONVERTER USING VOLTAGE FOLLOWERS WITH DRAIN-GATE FEEDBACK

6.1 Introduction

Chapter 5 dealt with the design of a type of V-I converter employing source-followers using drain to source feedback in a complementary circuit configuration. By contrast, this chapter considers the design of a V-I converter employing source-followers using drain to gate feedback in a circuit configuration that is a modification of the so-called 'Flipped Voltage Follower' (FVF).

First of all the characteristics and limitation of the FVF are reviewed, then the 'Folded Flipped Voltage Follower' (FFVF) introduced.

The proposed V-I comprises two half-circuits, each using an FFVF, linked by a transconductance-determining resistor. The performance characteristics of this V-I are fully explored in the remainder of the chapter.

6.2 Evolution of the half-circuit structure

The name 'Flipped Voltage Follower' (FVF) was coined by Carvajal et al [6.1] to describe a class of pre-existing [6.2] and new, low power/ low voltage analogue circuits.

A prototype FVF is a two transistors source-follower in which the input MOSFET is forced to operate at a sensibly constant DC drain current, set by ancillary circuitry, despite variation in input voltage or load current. This is achieved by the action of shunt negative feedback.

The overall result is a source-follower with decreased output impedance and increased linearity in its voltage transfer characteristic. The so-called 'Super Source-Follower' [6.3] the subject of the design in Chapter 5, can even be regarded as a member of the FVF family.

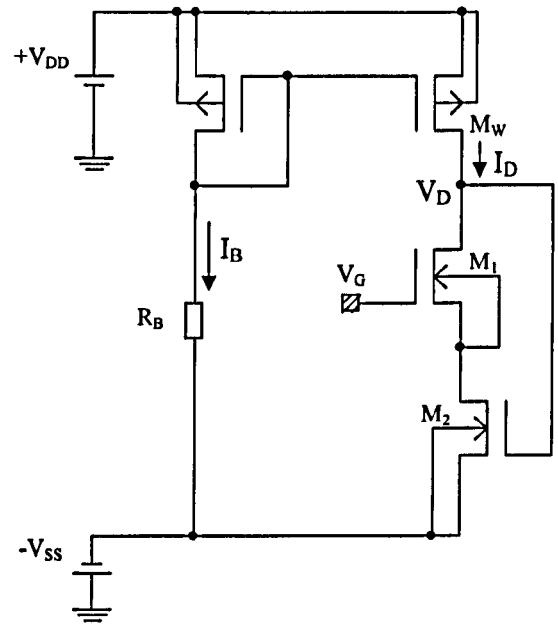


Figure 6.1 A prototype 'Flipped Voltage Follower' (FVF)

In Fig 6.1, M_1 and M_2 are inter-connected to form an N-channel FVF the operating current for which in supplied by M_W, the output MOSFET of a simple 1:1 current mirror. The mirror input current, I_B is set by choice of R_B.

M_1 passes an effectively constant current so its V_{GS} is sensibly constant and the incremental voltage gain, $\Delta V_S/\Delta V_G$, of the FVF is close to unity, providing it operates in its linear region. Unfortunately, as has been noted in [6.1], the valid linear range decreases with threshold voltage. This is most easily seen by applying eqns6.1, 6.2, which follow, to the case in which the characteristic of M_1 and M_2 are identical.

$$I_D = \frac{\beta_N}{2}(V_{GS} - V_{TN})^2 \qquad (6.1)$$

and, $$V_{DS(min)} = \sqrt{\frac{2I_D}{\beta_N}} \qquad (6.2)$$

Linear operation requires both M_1 and M_2 to operate in the saturation region. Using eqns 6.1, 6.2 the conditions for this for the circuit of Fig.6.1 are,

$$V_G \geq -V_{SS} + 2\sqrt{\frac{2I_D}{\beta_N}} + V_{TN} \tag{6.3}$$

and, $$V_G \leq -V_{SS} + \sqrt{\frac{2I_D}{\beta_N}} + 2V_{TN} \tag{6.4}$$

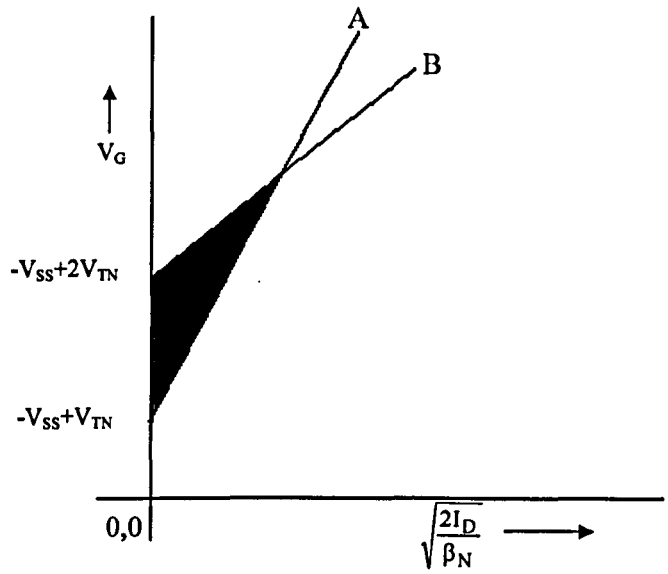


Figure 6.2 The hatched area shows the limited range for V_G for the circuit of

In Fig.6.2, line A with a slope of +2 represents the lower limit for V_G, as specified in eqn.6.3, and line B with a slope of unity indicates the upper limit for V_G, as specified by eqn.6.4. The shaded region in between, indicates the allowable region for linear operation, which obviously decreases with increase in I_D.

In general, the linear range ΔV_G, for V_G, is given by,

$$\Delta V_G = V_{TN} - \sqrt{\frac{2I_D}{\beta_N}} \tag{6.5}$$

This analysis applies to the particular case of equal values of (W/L) for M_1 and M_2 that is relevant to the work of this chapter. Carvajal et al [6.1] consider the more general case of unequal values of (W/L) for these MOSFETs but it is a shortcoming of their work that they did not consider the effects of loading at the source of M_1 and its effect on the magnitude of the linear range.

There are two cases to consider: with M_1 supplying an external load, with all of its drain current, and M_2 just cut off; with M_2 sinking a current in I_D from the load.

The first case is illustrated in Fig.6.3 (a), from which it follows that,

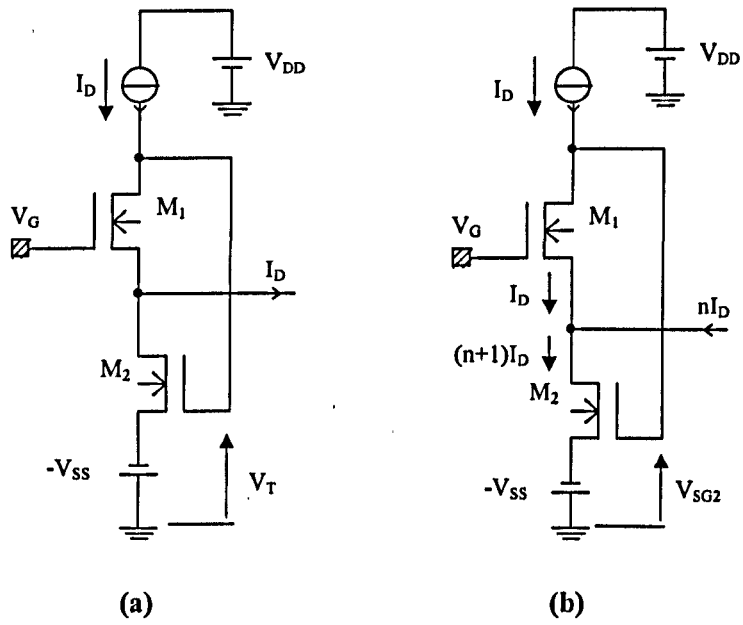


Figure 6.3 **V_G limit condition with loading**

(a) M_1 sourcing I_D and M_2 at the edge of cut-off

(b) M_2 sinking (n+1) I_D

$$V_G \leq -V_{SS} + 2V_T \tag{6.6}$$

The second case is shown in Fig.6.3 (b), from which it follows that,

$$V_G \geq -V_{SS} + V_{TN} + \sqrt{\frac{2I_D}{\beta_N}} + \sqrt{\frac{2(n+1)I_D}{\beta_N}} \tag{6.7}$$

Equations 6.6 and 6.7 are, respectively, more restrictive than eqns 6.4 and 6.3, so ΔV_G is reduced.

Thus, $$\Delta V_G = V_{TN} - \sqrt{\frac{2I_D}{\beta_N}} - \sqrt{\frac{2(n+1)I_D}{\beta_N}} \tag{6.8}$$

The linear range can be extended by using a floating DC voltage generator, V_B, shown in Fig.6.4 (a). An approximate way of achieving this is by the use of source-follower coupling [6.3], as indicated in Fig.6.4 (b).

For this a current sink I_x is required for source-follower biasing.

The equivalent V_B for Fig.6.4 (b) is $V_T + \sqrt{2I_x/\beta_P}$ so eqn.6.6

so now replaced by eqn.6.9

$$V_G \leq -V_{SS} + 3V_T + \sqrt{\frac{2I_X}{\beta_P}} \tag{6.9}$$

There is also an additional constraint imposed by the current source supplying I_D. If the minimum voltage across this for saturated region operation in V_M then,

$$V_G \leq (V_{DD} - V_M) + V_{TN} \tag{6.10}$$

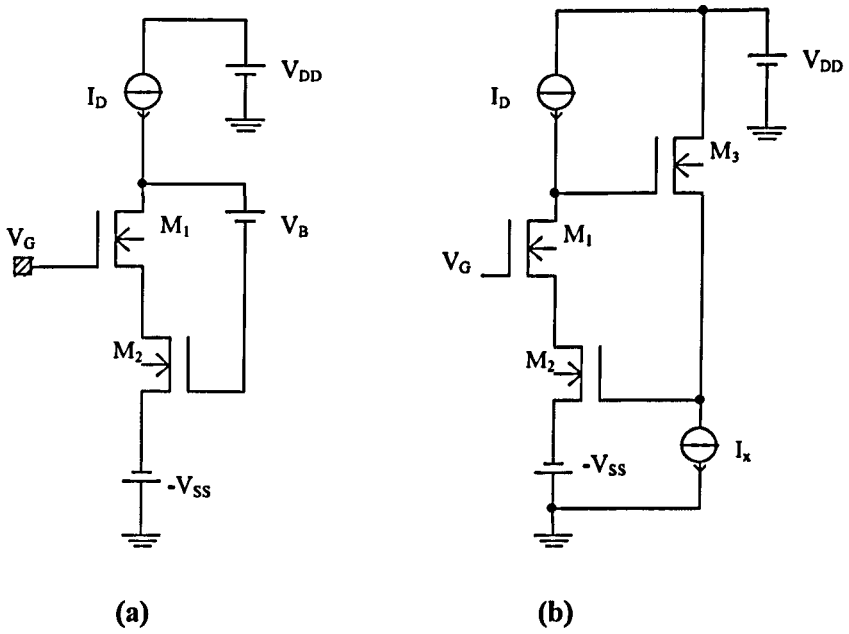


Figure 6.4 **(a) Extending $V_{G(max)}$ using a floating source**

(b) A practical implementation of (a)

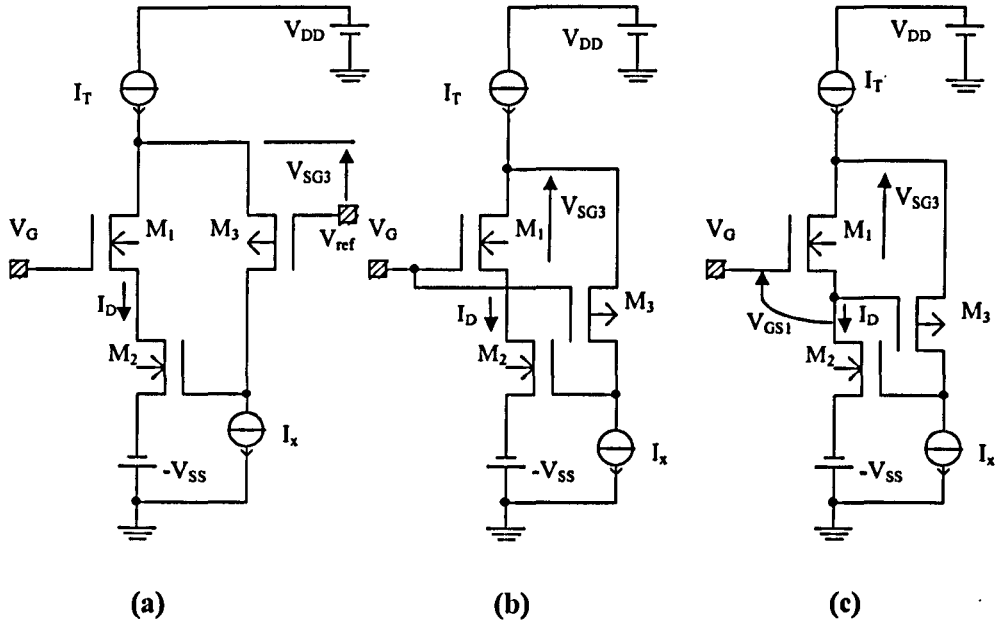


Figure 6.5 **Variations on the Folded Flipped Voltage Follower (FFVF)**

(a) Basic scheme: $V_{SG3}=V_{TP}+\sqrt{2I_x/\beta_p}$

(b), (c) Avoiding the use of a separate V_{ref}

Once it is appreciated that an extra MOSFET, M_3, and the associated sink, I_x, are required to extend the linear operating range an alternative scheme, a MOSFET version of a bipolar configuration [6.4], and shown in Fig.6.5(a), becomes attractive [6.5].

Now, the third transistor M_3 is opposite in polarity to that of M_1 and M_2.

For Fig.6.5(a), the maximum value of V_G is limited by whichever of the relationship is eqns 6.11a and 6.11c is the more restrictive.

$$V_G \le V_{TN} + V_{ref} + V_{SG3} \tag{6.11a}$$

or, $$V_G \le V_{TN} + V_{ref} + \sqrt{\frac{2I_x}{\beta_P}} + V_{TP} \tag{6.11b}$$

provided, $$(V_{ref} + V_{SG3}) < (V_{DD} - V_M) \tag{6.11c}$$

The negative rail voltage $-V_{SS}$ does not now limit the maximum allowable value of V_G.

A disadvantage of the circuit of Fig.6.5(a) is that it requires a reference voltage, V_{ref}.

As far as the author of this thesis is aware there has, so far, been no published FFVF circuit in which, the gate of M_3 is directly connected to that of M_1, as proposed here and shown in Fig.6.5(b). This has the obvious advantage of avoiding the use of V_{ref} and brings with it the bootstrapping of the drain of M_1 to its gate, with consequent reduction in follower input capacitance.

Now, $$V_G \le (V_{DD} - V_M) - V_{SG3} \tag{6.12a}$$

i.e, $$V_G \le (V_{DD} - V_M) - \sqrt{\frac{2I_x}{\beta_P}} - V_{TP} \tag{6.12b}$$

Fig.6.5(c) [6.6] offers the possibility of achieving the maximum range for V_G because,

$$V_G - V_{GS1} + V_{SG3} \le (V_{DD} - V_M) \tag{6.13a}$$

or, $V_G \leq (V_{DD} - V_M) + (V_{GS1} - V_{SG3})$ (6.13b)

But, $(V_{GS1} - V_{SG3}) = V_{GD1}$ and M_1 does not leave the saturated state till $V_{DS1} > V_{TN}$

Hence, theoretically, the limiting value of V_G is now given by,

$$V_G < (V_{DD} - V_M) + V_{TN} \quad (6.14)$$

To achieve this condition it is necessary that V_{SG3} just exceeds the minimum V_{DS1} for saturation. This is given by,

$$\sqrt{\frac{2I_x}{\beta_P}} + V_{TP} = \sqrt{\frac{2(I_T - I_x)}{\beta_N}} \quad (6.15)$$

Chip processing variations and their effect on parameter tolerances require that, for reproducible design, the equality sign in eqn.6.15 be replaced by a 'greater than' sign

$$(V_{DD} - V_M) + V_{TN} \geq V_{G(max)} \geq (V_{DD} - V_M) \quad (6.16)$$

The allowed operating area for saturation-region operation is shown shaded in Fig.6.6. On this line C has a slope $[1+\sqrt{(n+1)}]$, which takes into account the requirements of eqn.6.8, rather than eqn.6.3

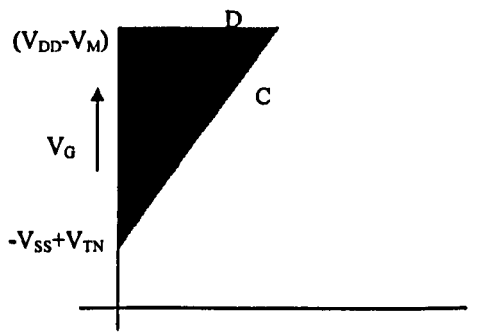


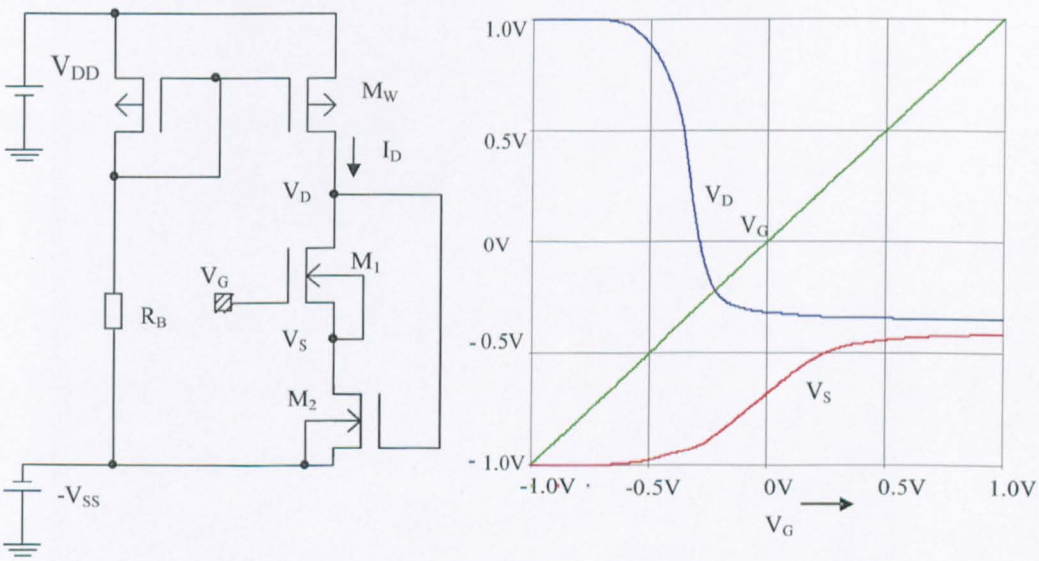
Figure 6.6 The shaded area shows the extended operating range possible with the circuit of Fig 6.5 (c)

The circuit of Fig.6.1 is shown again, for convenience in discussion as Fig.6.7(a).

A practical version of Fig.6.5 (c) is shown in Fig.6.8 (a). In simulation tests at 27°C all the MOSFET, except M_3, had L=0.13μm and W=10μm. It was assumed that for low voltage operation V_{DD} and V_{SS} would not generally exceed 1.5V and I_D would not exceed 1mA. , so these values were used. For a fair comparison, M_1 was made to operate at the same current in both circuits.

M_X and R_X (=4K) in the output circuit of a Widlar current mirror, provide I_x.

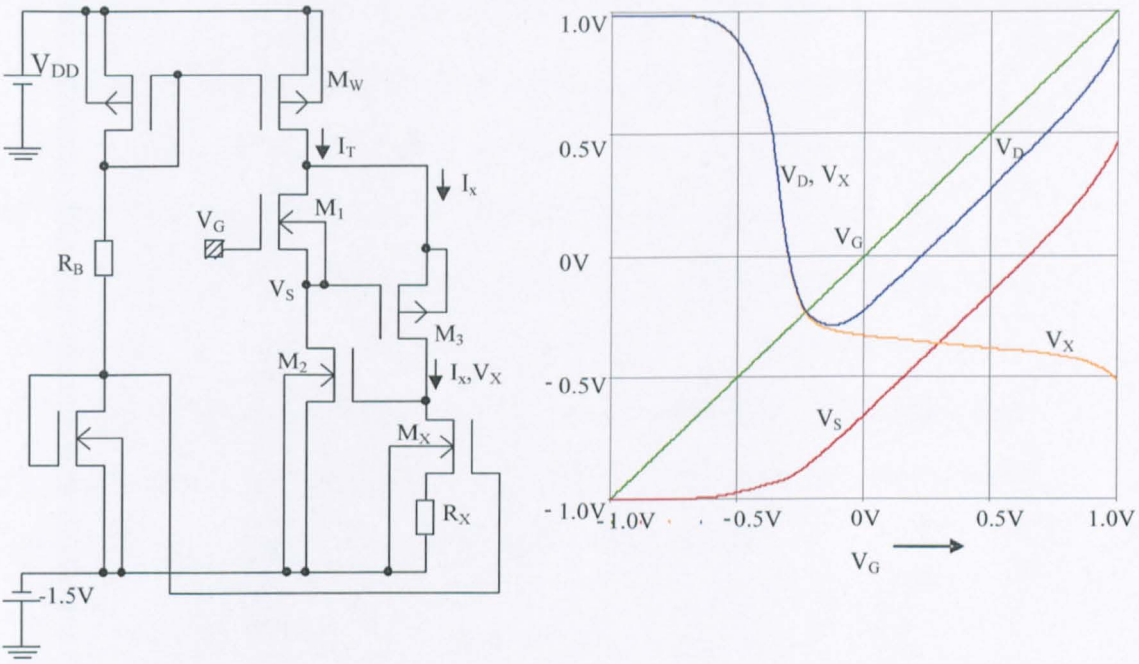
For M_3, the choices I_X=50μA (so I_T=1.05 mA), L=0.13μm W=50μm guaranteed that its gate-drain voltage exceed zero.



(a) **(b)**

Figure 6.7 The FVF

(a) Circuit ; (b) Voltage traces



(a) **(b)**

Figure 6.8 The proposed FFVF

(a) Circuit; (b) Voltage traces

The simulated tests results for the circuit of Fig.6.7(a) are shown in Fig.6.7 (b) and those for Fig.6.8(a) in Fig.6.8(b)

When V_G is such than M_1 is passing only a small leakage current the curves for V_D in Figs 6.7(b) and 6.8(b) are similar, as are those for V_S.

However, once M_1 commences conduction differences appear. In Fig.6.8(b) there is no region for which the voltage trace for V_S is parallel to that for V_G as would be the case for M_1, M_2 both operating in their saturated regions.

In Fig.6.8(b) there is an extended region, above $V_G \cong 0.5V$ where the voltage traces for V_D ($<V_G$) and V_S are parallel to that of V_G, in accordance with the theory presented. (Above V_G=1V the onset of triode behaviour in M_W causes non-linearity)

The superior DC performance of the proposed FFVF, compared with that of the FVF in respect of the linearity and range of the operating region, is clearly evident.

The current traces for the two circuits, shown in Figs 6.9, 6.10, illustrate further the operation of the circuit and point to a limitation in the performance of the FFVF.

Consider first Fig.6.9. With I_B=1mA, I_D rises to a maximum value of 1.05mA (approx) with increase in V_G form its initial value of -1.5V. This is because of the non-unity current transfer ratio of the current mirror supplying it. [From Fig.6.7(b) the drain voltage of M_W is about -0.4V so its V_{DS} is 1.9V I_D is then sensibly constant because the drain voltage does not change appreciably with V_G.

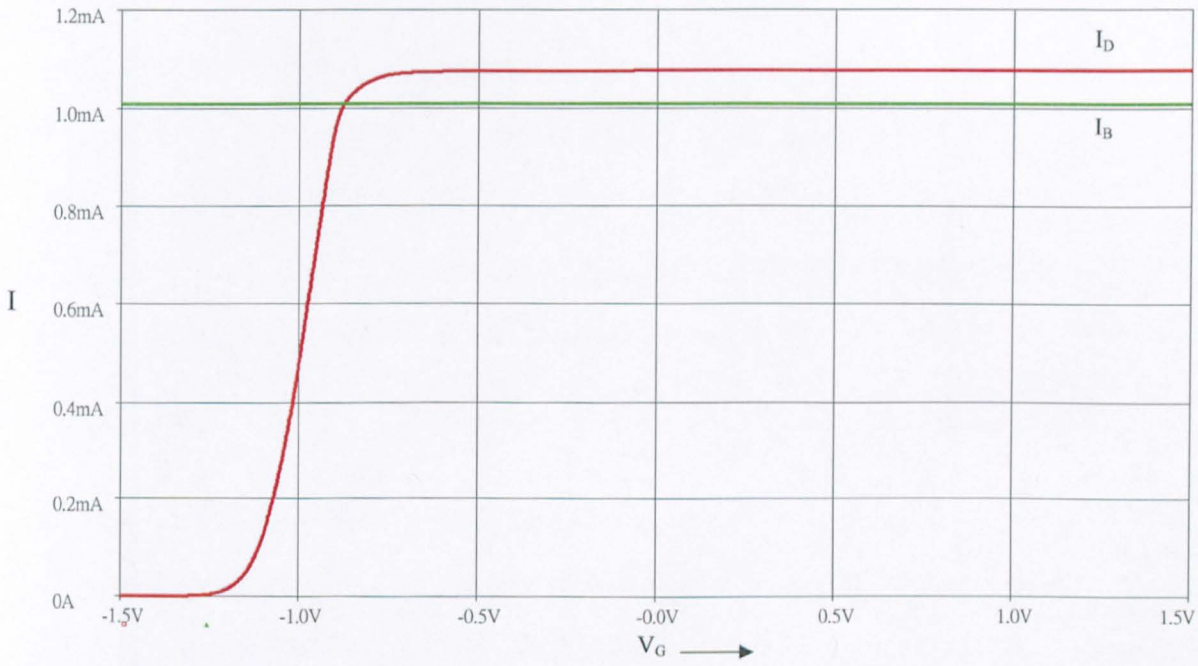


Figure 6.9 Current traces for the FVF

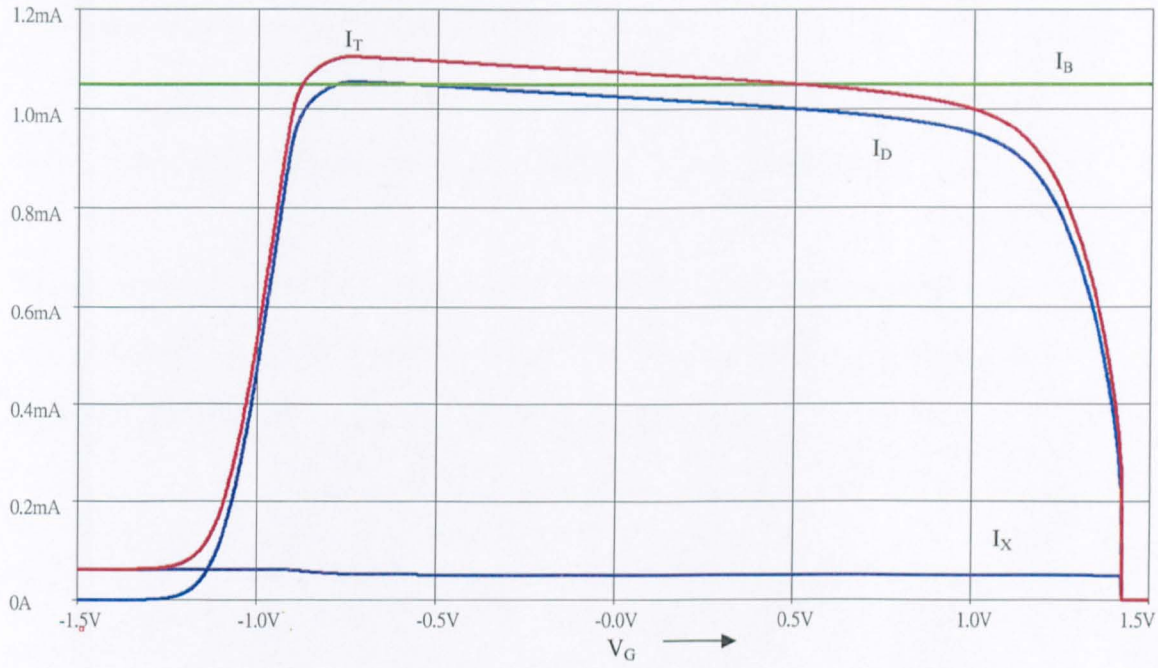


Figure 6.10 Current traces for the FFVF

Consider next Fig.6.10. I_T rises to a maximum value slightly greater than I_D in Fig.6.9 because I_B is now 1.05mA. However, in this case, I_T does not stay constant as V_G changes. Thus, an increase in V_G causes an increase in V_S, by source-follower action in M_1, and V_D consequently increases because of source-follower action in M_3.

Hence, $$\frac{dI_T}{dV_G} \cong \frac{1}{r_{dsw}} \qquad (6.17)$$

where r_{dsw} is the incremental output resistance of M_W.

I_X stays constant, after M_3 enters its saturation region, because the change in V_X with V_G is small, and the output resistance of M_X is high because of the presence of the source degeneration resistor R_X. As a result, the fall in I_D ($=I_T-I_X$) with increase in V_G parallels that of I_T until M_W enters its triode operating region.

The existence of the feedback loop from the drain of M_1 to the gate of M_2 gives rise to the description DGFC (Drain- Gate Feedback Circuit) to the V-I converters family of schemes making use of the FFVF circuit described in this section.

The first of these schemes is considered next.

6.3 The basic V-I converter type DGFC in schematic form

The proposed V-I, shown in Fig.6.11, comprises two half-circuits, each a FFVF of the type described in the previous section, linked by a resistor R, which is a common load for them. Added transistors (M_4, M_4') provide output currents.

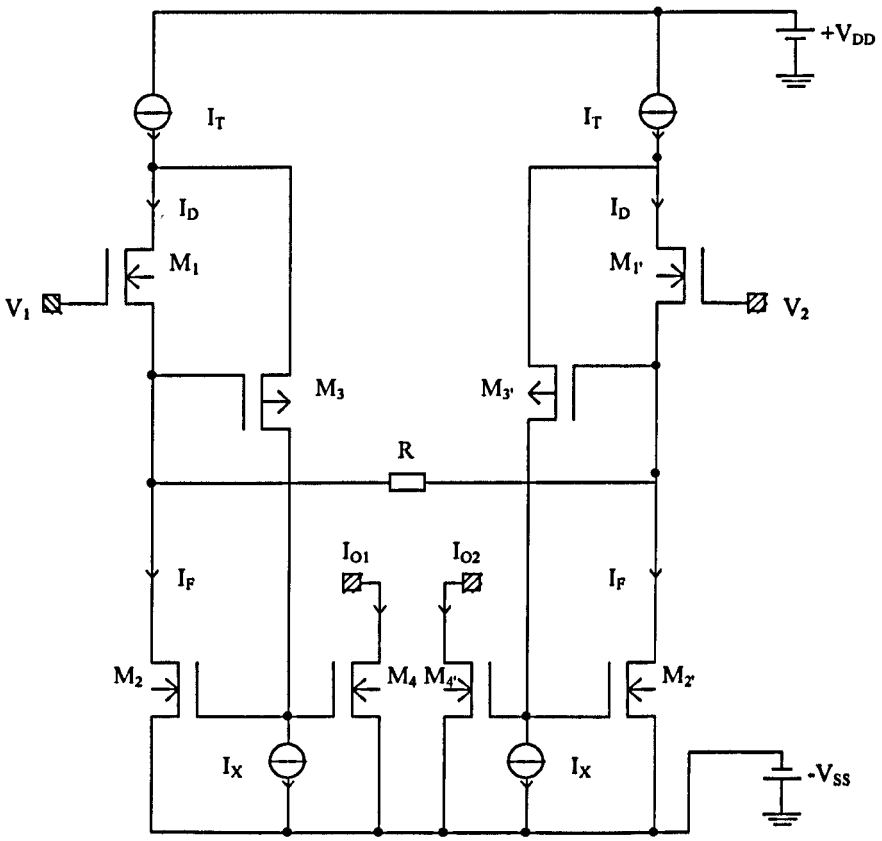


Figure 6.11 Schematic of proposed V-I converter

6.3.1 Ideal circuit operation

An idealised equivalent circuit for explaining circuit operation is shown in Fig.6.12

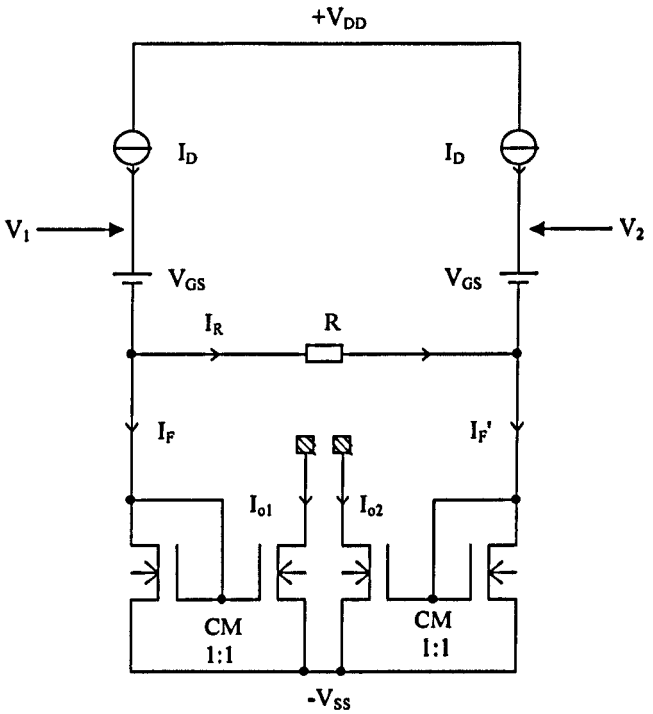


Figure 6.12 Idealised representation of circuit operation

The gate-source voltage, V_{GS} of each of the input transistors is assumed constant because their drain currents are held constant.

Hence,

$$I_R = (V_1 - V_2)/R = V_D/R \tag{6.18}$$

But, $$I_D = I_F + I_R = I_F' - I_R \tag{6.19}$$

Also by 1:1 current mirror action $I_{o1}=I_F$ and $I_{o1}=I_F'$.

Therefore, $$G_t = \frac{\Delta I_D}{\Delta V_D} = \frac{2}{R} \tag{6.20}$$

As in the case of the DSFC, the maximum linear range, V_{DM}, over which G_t is intended to be constant is $V_{DM}= (I_T-I_D)R$ and eqn.5.11 is applicable.

6.3.2 Non-ideal performance

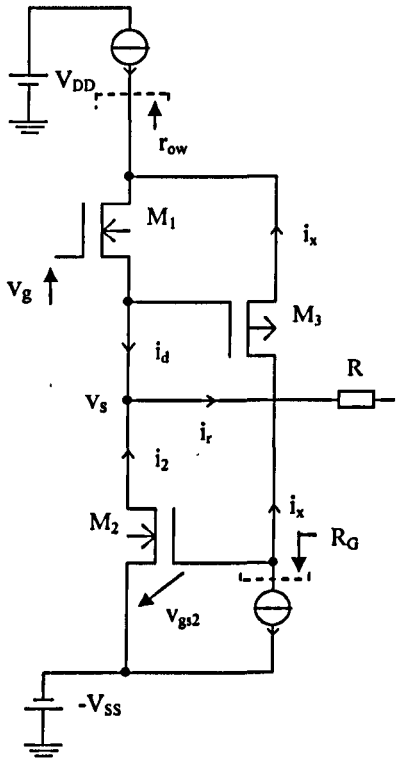


Figure 6.13 Showing current changes for an incremental positive increase, v_g, in input signal voltage

A qualitative understanding of what happens when V_G changes by a small positive increment from a quiescent value of zero can be appreciated by reference to Fig.6.13. This shows the consequent signal changes that occur, in the directions indicated. The current i_x is smaller than i_d because of current loss at the drain of M_1 but it gives rise to a significant change, $i_x R_G$ in the gate-source voltage of M_2, with the result that $i_2=mi_d$, where $m>1$.

However, $$i_r = (i_d + i_2) = (m+1)i_2 \qquad (6.21)$$

Thus, $$i_d = \frac{i_r}{(m+1)} \quad (6.22a)$$

and, $$i_2 = \frac{mi}{(m+1)} \quad (6.22b)$$

Furthermore, $$v_s = i_r R = (m+1) i_d R \quad (6.23)$$

and, $$v_g = v_s + v_{gs1} = \left(v_s + \frac{i_d}{g_{m1}} \right) \quad (6.24)$$

so, $$\frac{v_s}{v_g} = \frac{g_{m1}(m+1)R}{[1+(m+1)g_{m1}R]} \quad (6.25)$$

By design, m>>1 so we can draw the following conclusions from the above equations.

(a) The change in i_r is brought about mainly by a reduction in the drain current of M_2.

(b) There is little change in i_d, and hence V_{GS1}.

Initially, $$V_{GS1} = \sqrt{\frac{2I_D}{\beta}} \quad (6.26)$$

After the charge $$V_{GS1} + \Delta V_{GS1} = \sqrt{\frac{2(I_D + i_d)}{\beta}} \quad (6.27)$$

Suppose $$i_d = yI_D \quad (6.28)$$

where, $y \ll 1$

From eqns 6.21, 6.26, 6.27, 6.28, with the condition $(y/m) \ll 1$, the binomial expansion gives,

$$\Delta V_{GS1} \cong V_{GS1} \left[\frac{y}{2(m+1)} \right] \quad (6.29)$$

For the cases $m > 50$, $y \ll 1$, it is apparent that

$$\Delta V_{GS1} < (1\% \text{ of } V_{GS1}) \quad (6.30)$$

(c) $$\frac{v_s}{v_g} \cong 1$$

This also follows, of course, from eqn.6.30

Fig 6.14, a re-drawn version of Fig 6.13, allocates the nodal voltage lettering used in the small-signal equivalent circuit of Fig 6.15, when the V-I converter is driven in such a way that $V_1=V_D/2$, $V_2=-V_D/2$.

Subsequent analysis is straight-forward but somewhat lengthy. That is presented in Appendix6.1, so the results only are presented here.

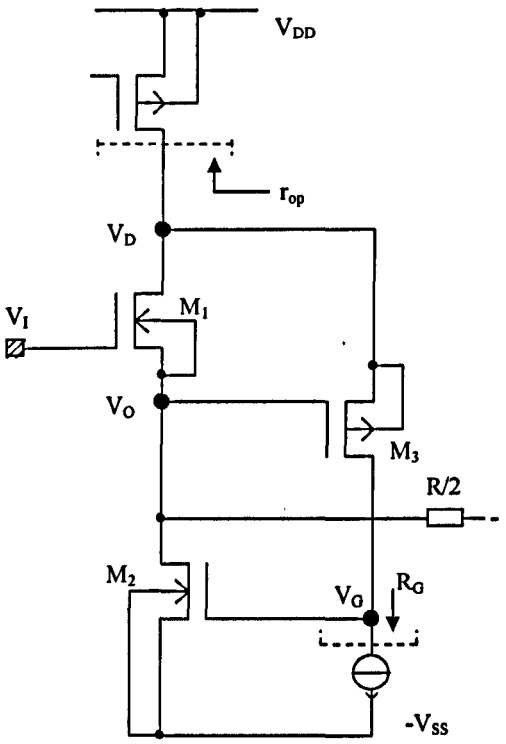


Figure 6.14 Half-circuit used in analysis

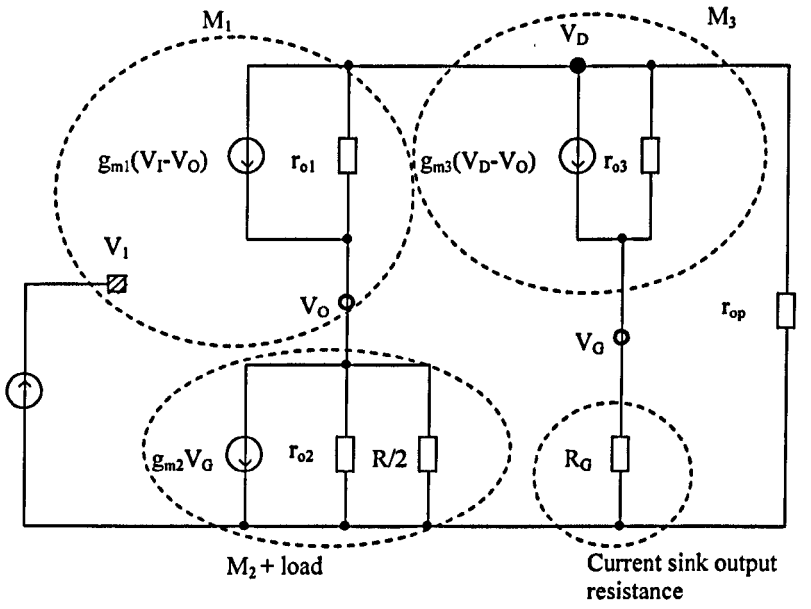


Figure 6.15 Small-signal low-frequency equivalent circuit of Fig 6.14

6.4 Circuit implementation of the DGFC1

The design steps for the proposed V-I converter are identical to those listed in Section5.3.3.

Fig.6.16 shows the DGFC1, the basic V-I converter version, simulated for general assessment. Note that the transistor numbering is different from that used so far and starts with the current sources supplying I_T (1mA).

Ignore, for the present, the capacitors C_1, C_2. (Their location and value are dealt with in a later section.)

In this particular circuit the substrate of M_6 is taken to V_{DD}. The voltage traces of Figs6.17, 6.18 show that M_4 and M_5 provide good source follower action. However, the source-follower action of M_6, M_7 is not so good because their substrates are not tied to their sources.

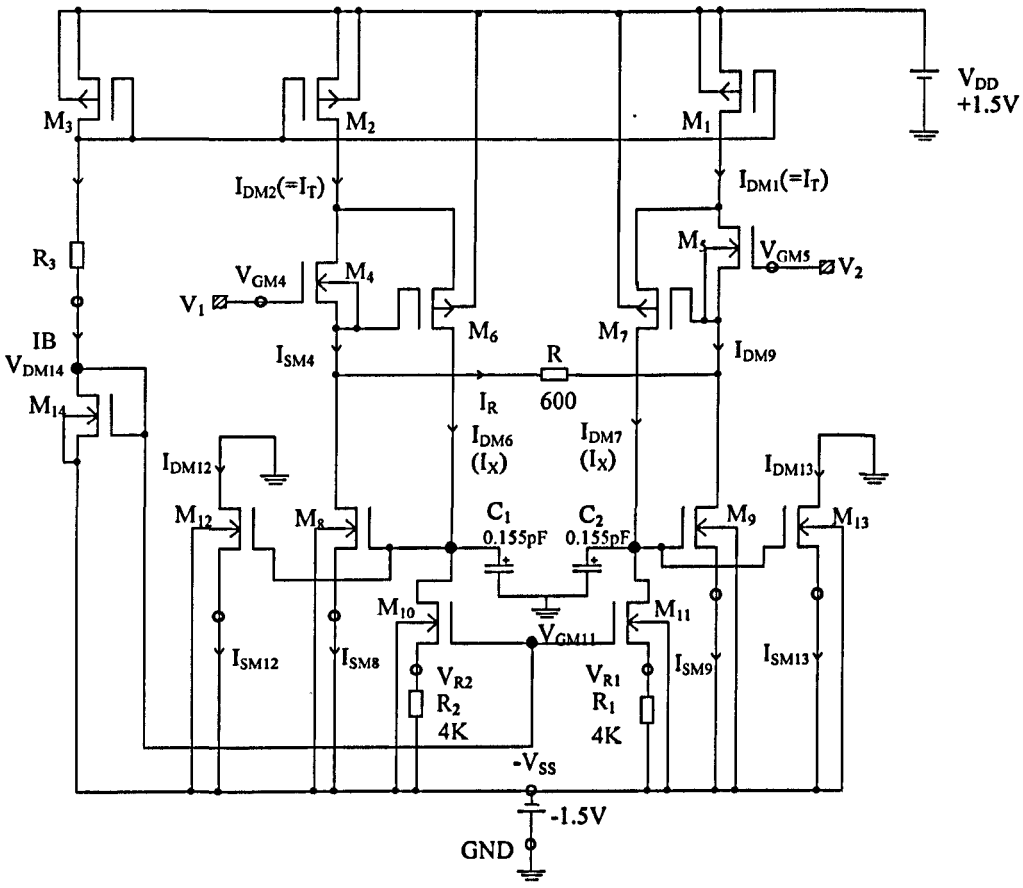


Figure 6.16 The V-I converter type DGFC1

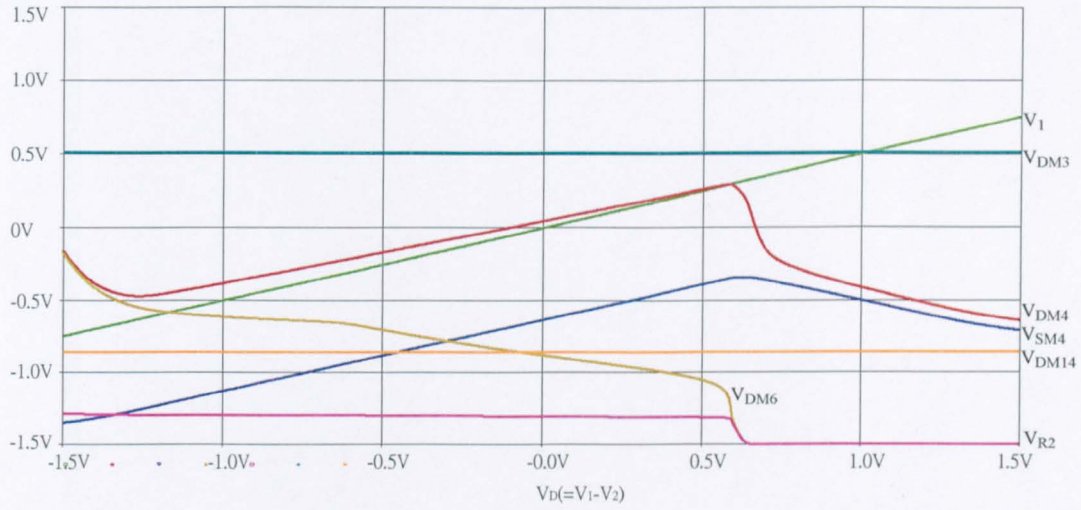


Figure 6.17 Voltage traces For Fig 6.16

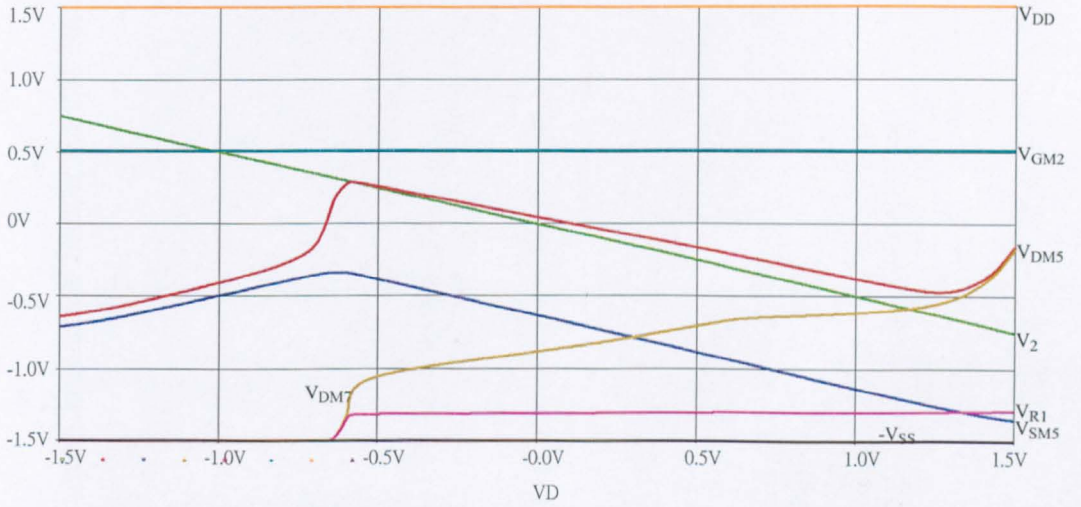


Figure 6.18 Further voltage traces of Fig 6.16

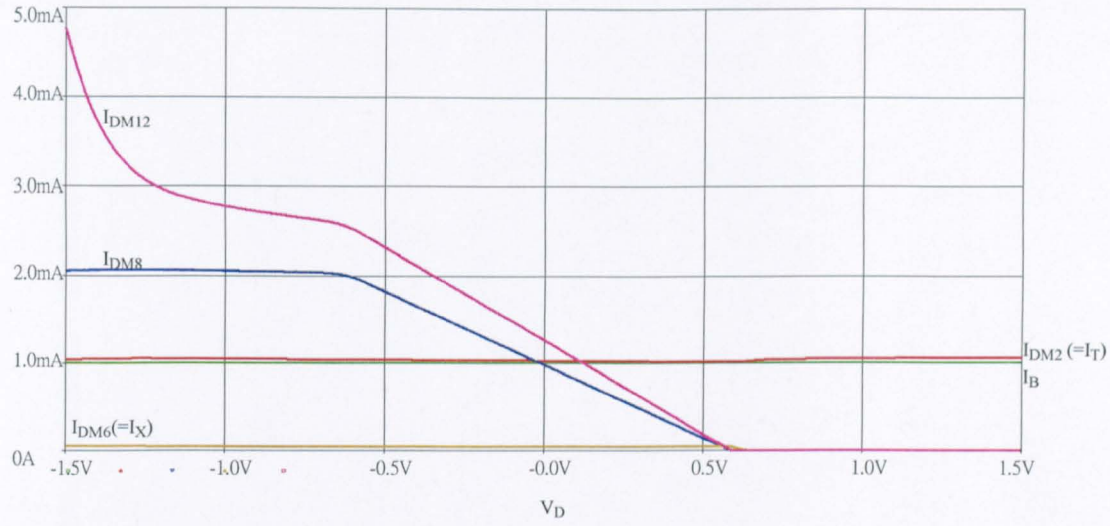


Figure 6.19 Current traces for Fig 6.16

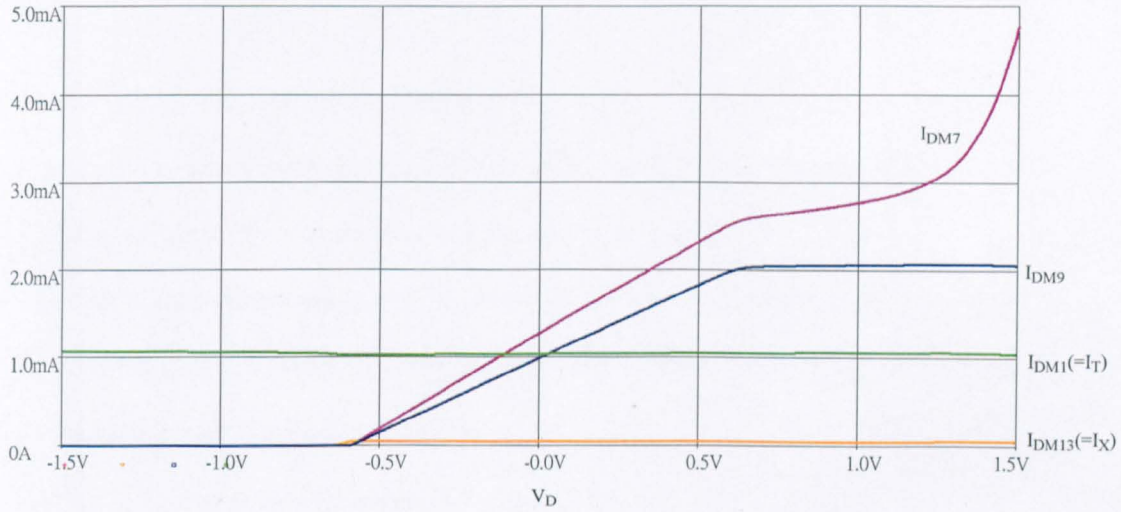


Figure 6.20 Further current traces for Fig 6.16

The current traces of Figs 6.19, 6.20 show that I_T and I_X remain sensibly constant at 1mA and 50μA, respectively. However, I_{DM12} is significantly larger than I_{DM8} because, although M_{12} and M_8 have the identical output characteristics and the same V_{GS}, they have different values of V_{DS}. Similar comments apply to M_4 and M_{13}.

The way the current increase comes about can be understood by reference to Fig 6.21.

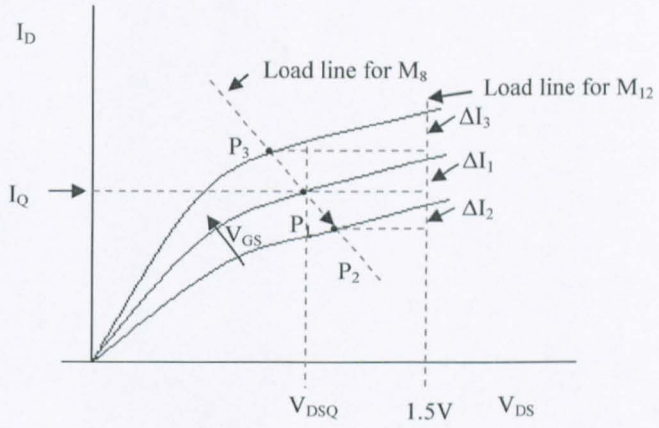


Figure 6.21 Showing how $I_{DM12} > I_{DM8}$

On the output characteristics of M_8, point P_1, with co-ordinates V_{DSQ}, I_Q defines the quiescent condition with V_1=0V, P_2 (for V_1>0) and P_3 (for V_1<0) represent two arbitrary points in the intended linear operating range for G_t.

The line $P_2P_1P_3$ represents a section of the dynamic load line for a resistive load of R/2, corresponding to the load seen by a half-circuit when the V-I converter is driven differentially with $V_1=V_D/2$ and $V_2=-V_D/2$.

At P_1, P_2, P_3, I_{DM12} exceeds I_{DM8} by ΔI_1, ΔI_2, ΔI_3 respectively.

The apparent current magnification in the output stages produces the characteristic shown in Fig.6.12. G_t, at 4.27mS, is unacceptable, for an intended design value of 3.33mS.

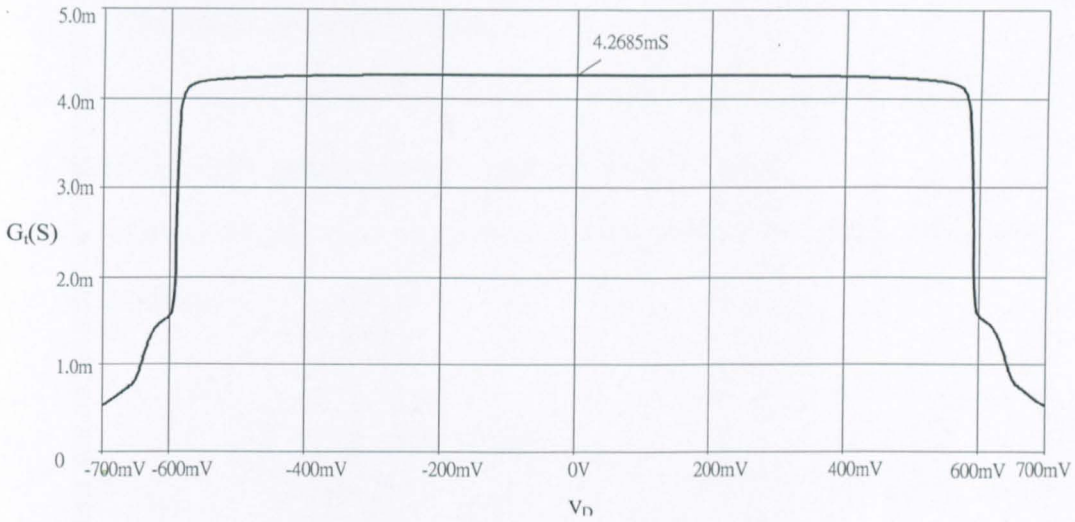


Figure 6.22 The transconductance characteristic for Fig 6.16

Proposed modifications, described in the next section, lead to the DGFC2.

6.5 The DGFC2 and DGFC3

The first modification to the circuit of Fig 6.16 is the connection of the substrate of M_6 and M_7 to theirs sources for improved source-follower action.

The second modification involves a reduction in the apparent, undesired, current gain in the output stages.

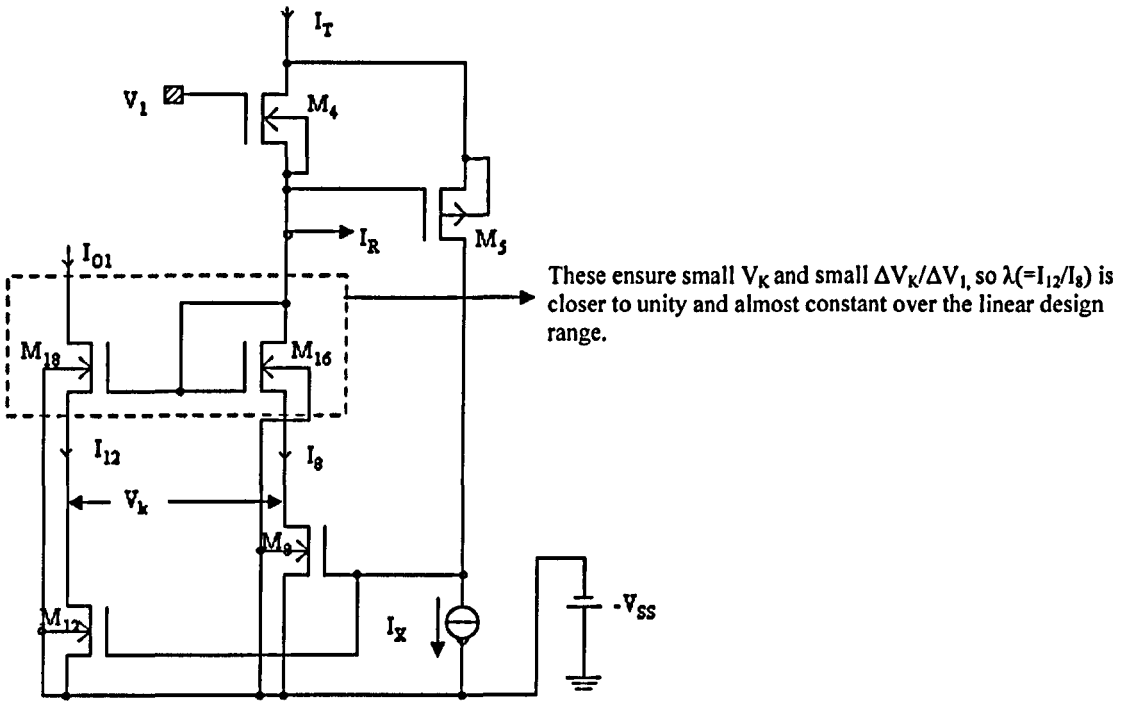


Figure 6.23 Showing modifications to the DGFC1

Both these modifications are shown in the half-circuit of Fig.6.23.

An unfortunate consequence of the inclusion of M_{16} is an increased V_{SS} to allow for the extra voltage drop involved.

Fig.6.24 which showed be compared with Fig.6.21, is a graphical interpretation of the effect of the second modification.

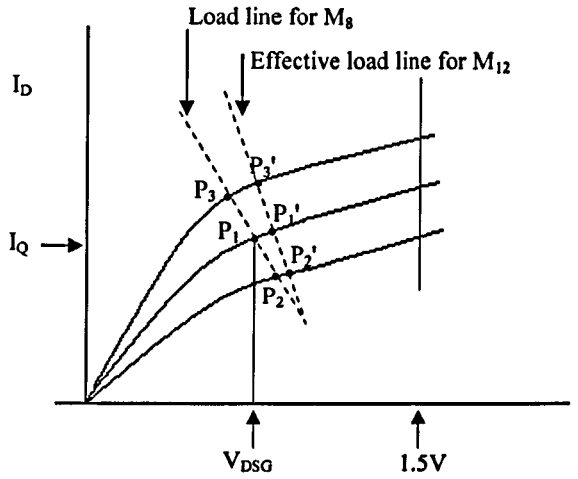


Figure 6.24 Load-line re-location explains the reason for the presence of M_{16}, M_{18} in Fig.6.23

The vertical load line for M_{12} in Fig.6.21 is effectively re-located, to appear as $P_2'P_1'P_3'$ in Fig.6.24. Ideally, this would be coincident with $P_2P_1P_3$ but it is not so for two reasons: first, V_k (Fig.6.23) $\neq 0$ because the drain voltage of M_{18} exceeds that M_{16}; second, the incremental voltage gain of the source-follower of which the input transistor is M_{18} is not unity. (Furthermore it varies slightly over the linear voltage range because its μ is dependent on I_{12}. This is a source of non-linearity, which, though small, contributes to distortion.)

The complete circuit of the V-I, now designated DGFC2, is shown in Fig.6.25. The DGFC 3 is a temperature-insensitive reason of DGFC 2: the only difference between it and the DGFC 2 is the biasing scheme, which is considered later.

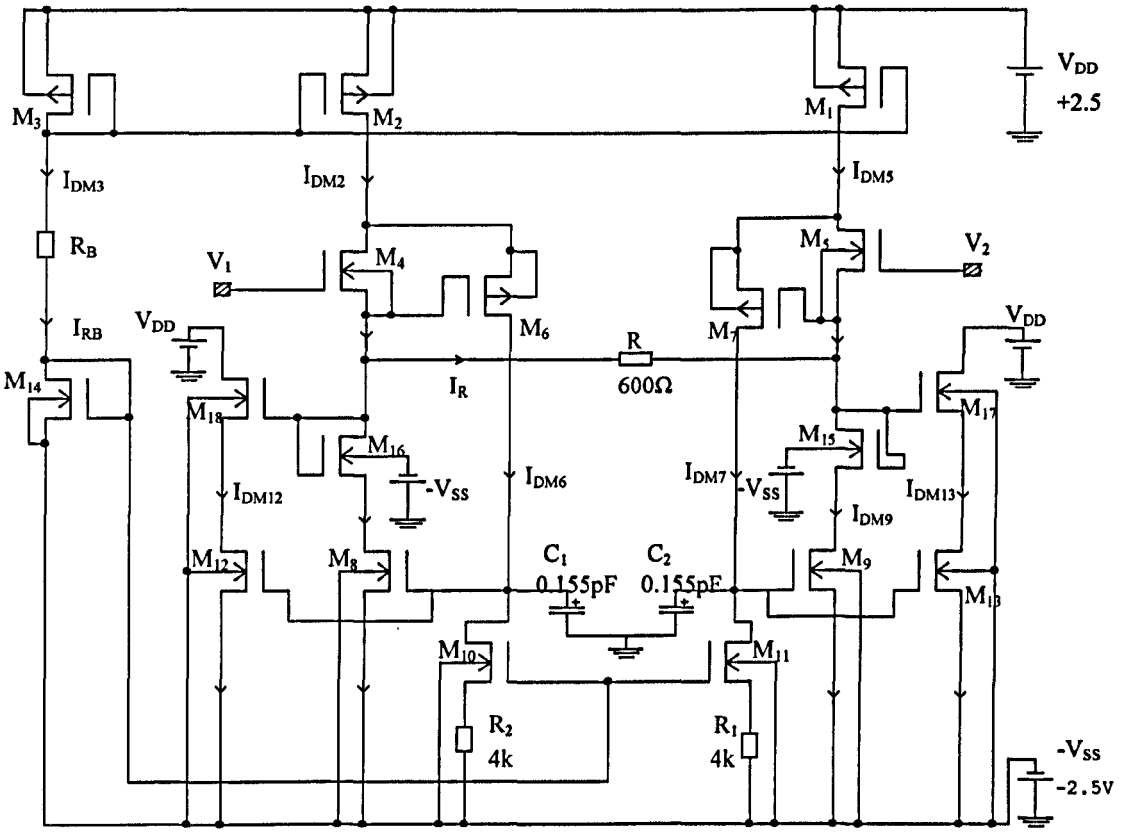


Figure 6.25 The DGFC 2

6.5.1 DC Conditions

The DC Conditions in the circuit for the case $V_1=V_2=0$ are given in Appendix6.2

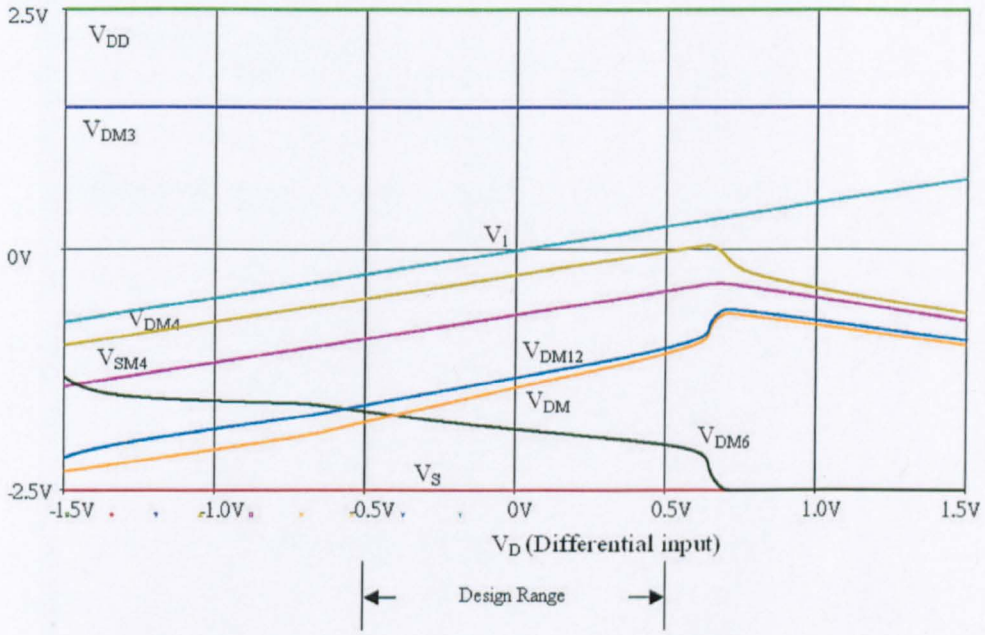


Figure 6.26 Voltage traces for Fig 6.25

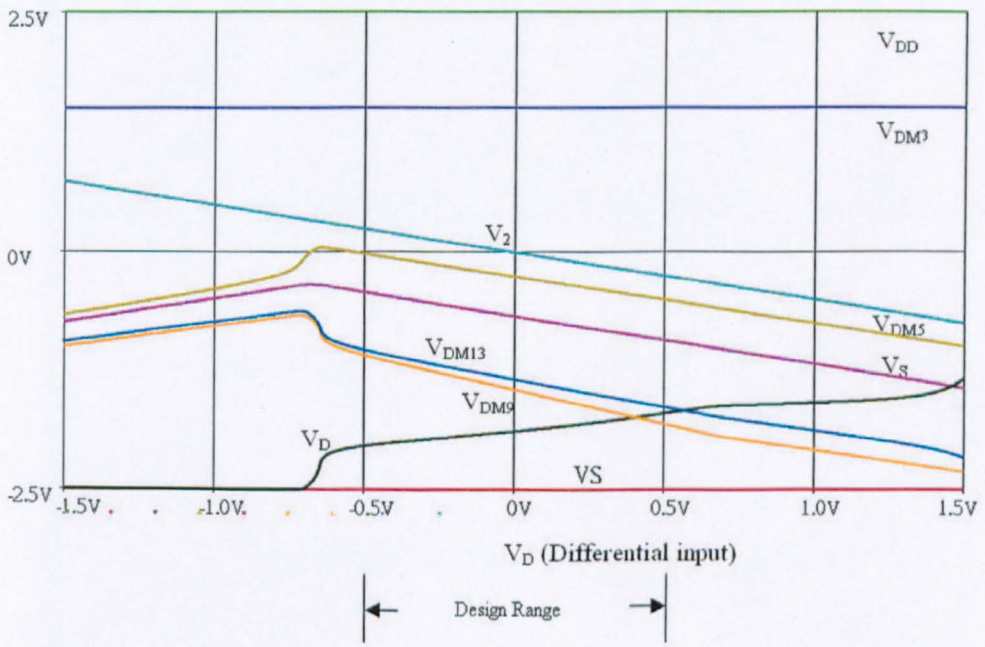


Figure 6.27 Further voltage traces for Fig 6.25

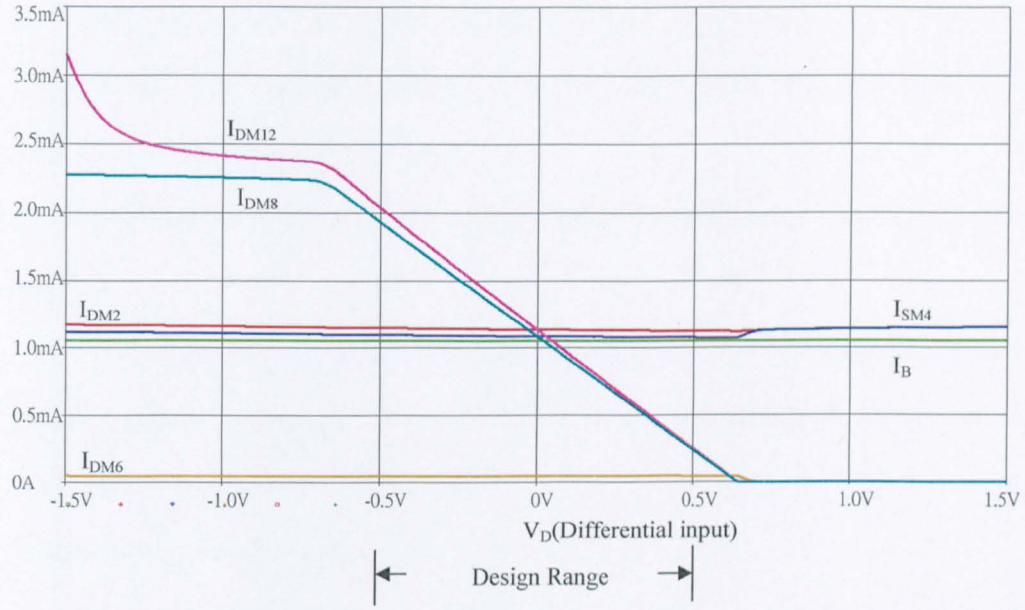


Figure 6.28 Current traces for Fig 6.25

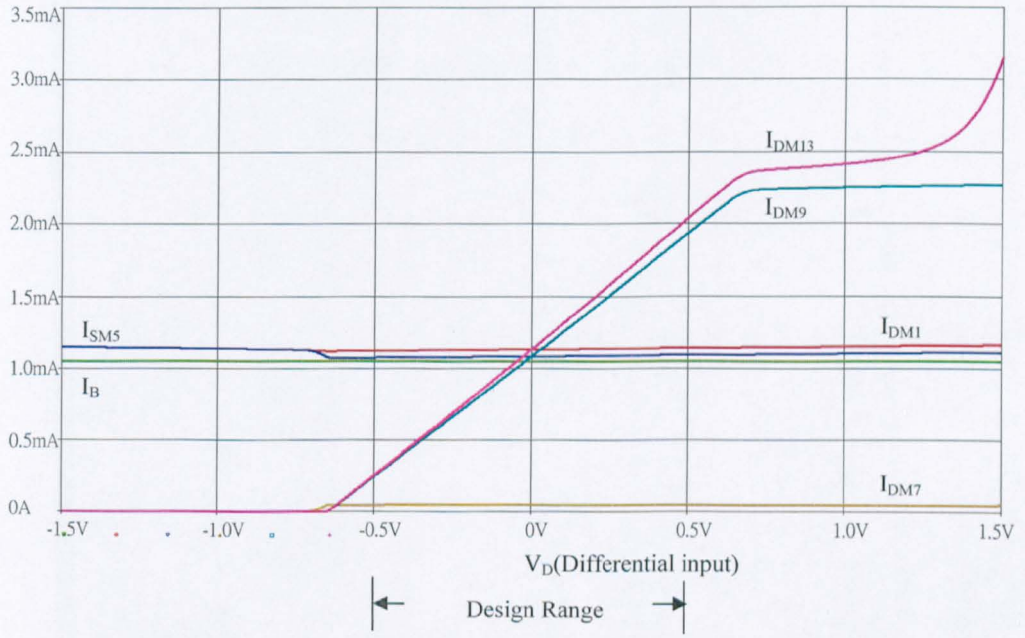


Figure 6.29 Further current traces for Fig 6.25

In Fig.6.26 the voltage traces show very good voltage-follower action by M_4 over the linear design range and the tracking in V_{DM12} and V_{DM8} that is a consequence of the second modification referred to above.

The voltage traces in Fig.6.27 are a mirror image, about the line V_D=0, of those in Fig.6.26.

The current traces in Fig.6.28 show a distinct improvement over those in Fig.6.19. From Appendix6.2, I_{12}/I_8=1.045, i.e., the current gain of the output stages exceeds unity by less than 5%.

The constancy of I_X (I_6) is apparent.

As with the voltage traces, the current traces of Fig.6.29 are a mirror images, about the line V_D=0, of those of Fig.6.28.

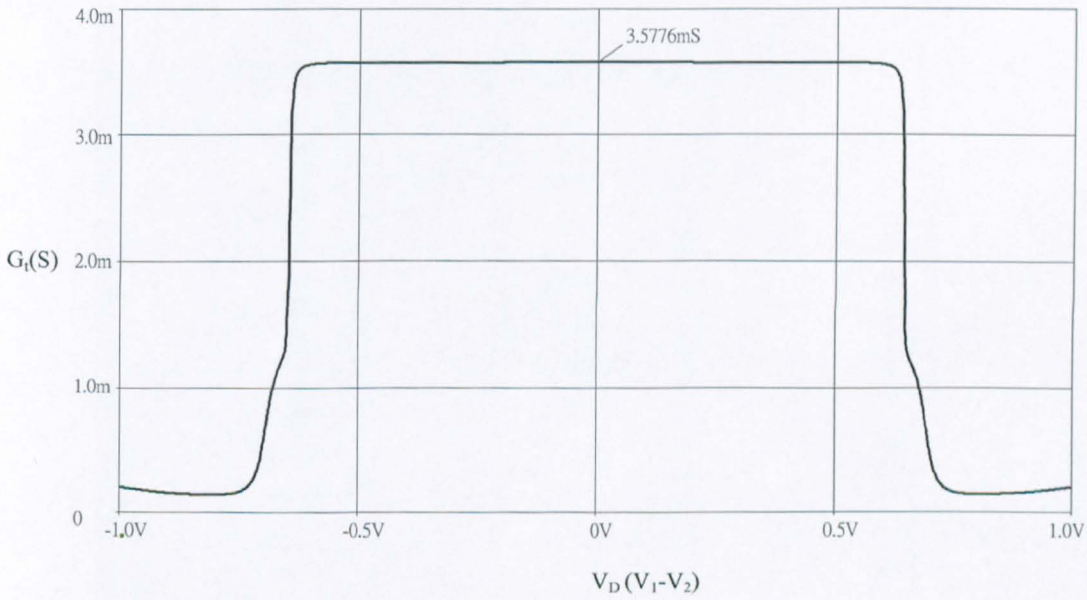


Figure 6.30 The G_t characteristic for the DGFC 2 at T=27 °C

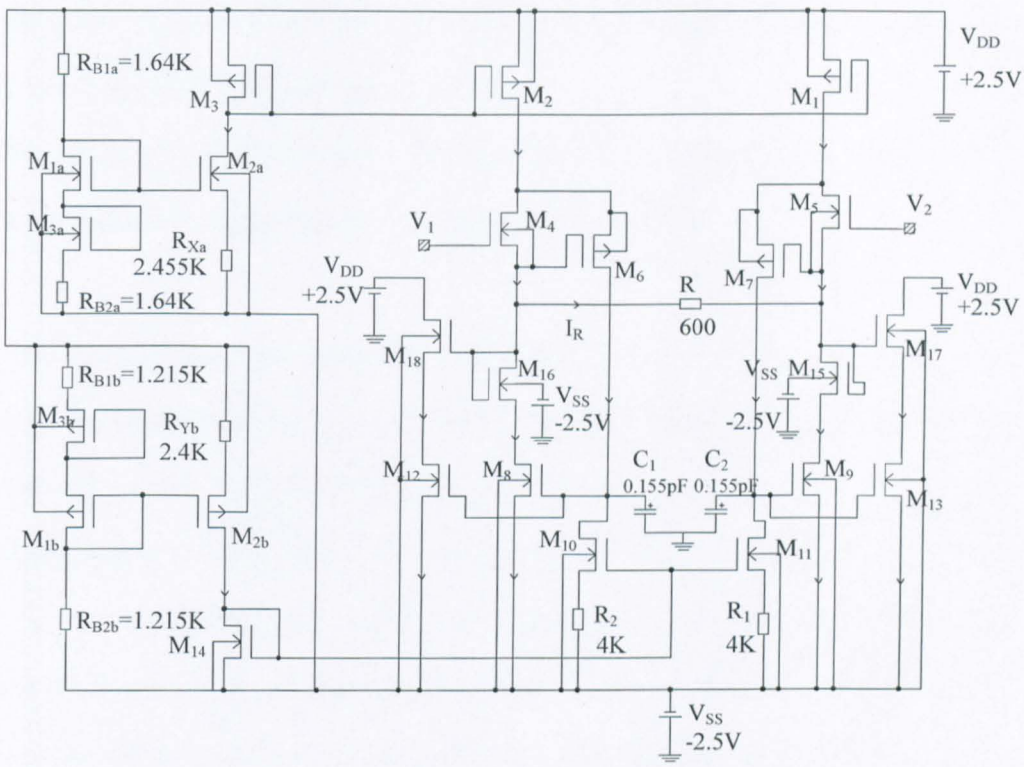


Figure 6.31 The DGFC 3 (A temperature insensitive version of the DGFC 2)

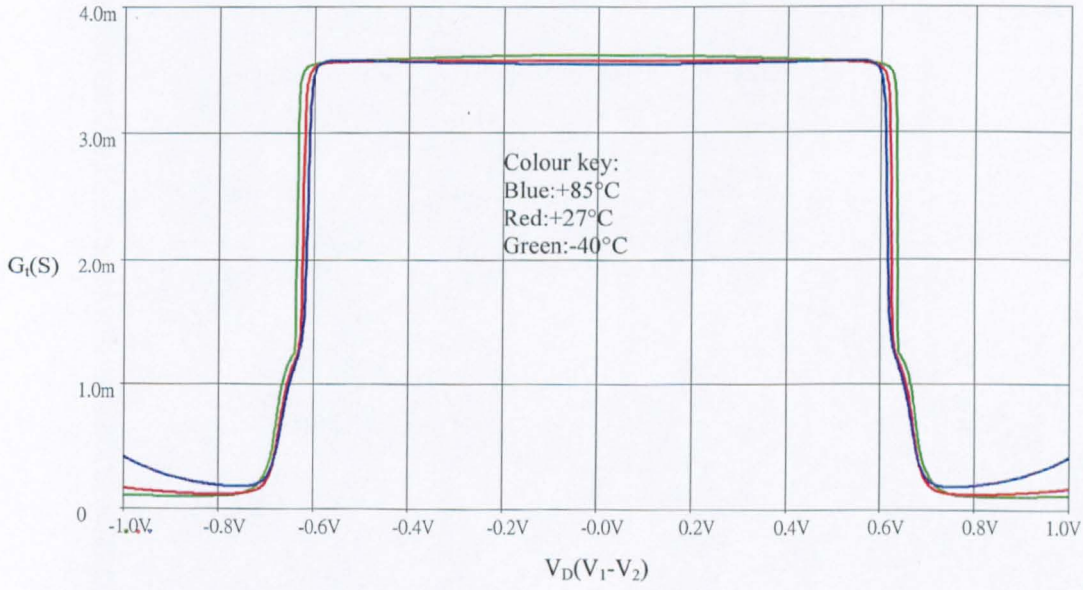


Figure 6.32 Temperature performance of the DGFC 3

Fig.6.30 shows the G_t characteristic at 27°C.

The design theory for the DGFC 3, shown in Fig.6.31 is identical to that employed in Chapter 5.(pp 19, 20 and Appendix5.2)

The resulting G_t characteristic for three different temperatures, -40°C, 27°C, 85°C, shown in Fig.6.32, demonstrates good temperature-insensitivity.

6.5.2 Small-signal high-frequency performance

As in the DGFC schemes the small-signal frequency response is dependent on the frequency response of each loaded half-circuit.

An assessment of the impedance levels associated with each mode in the left-hand half-circuit of Fig.6.25 suggested that the dominant time constant would exist at the gate of M_8 (and M_{12}) and that even if this did not guarantee feedback-loop stability then capacitance could be added at this point to ensure that stability did exist.

Fig.6.33 shows a simulated test circuit for loop-gain measurement.

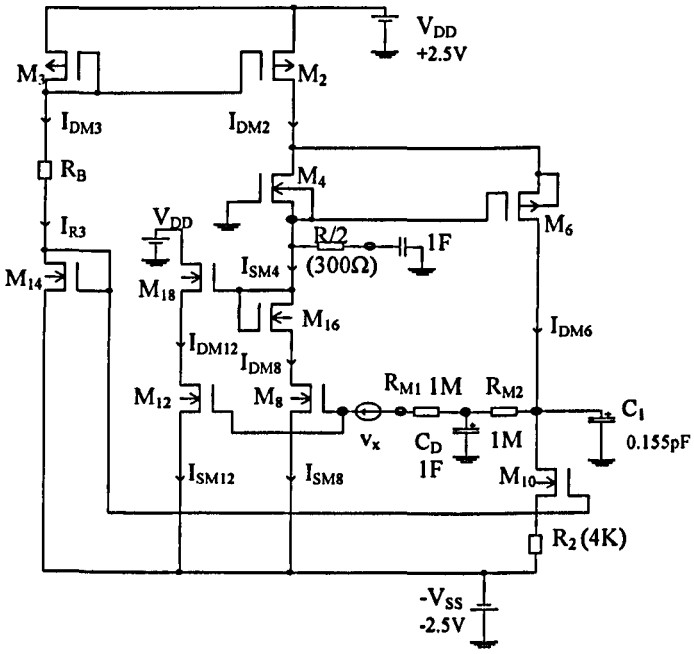


Figure 6.33 Loop-gain test circuit

The 1F capacitor guarantees that the external a.c. load at the source of M_4 is the 300Ω, with which it is in series, for all frequencies of interest.

The feedback loop is imagined to be 'cut' at the gate of M_8 but in so-doing it is necessary to preserve the DC conditions impedance levels that existed before the cut was made.

This is the reason for incorporating the network comprising R_{M1}, R_{M2} and C_D.

A small (≈ 1mV peak) a.c. test signal, v_x, applied at the gate of M_8(and M_{12}) produces a feedback signal v_x' at the drain of M_6. The capacitor C_D isolates the two signals. The loop-gain, L.G., is v_x'/v_x. To ensure stability with an adequate phase margin it was necessary to affix a capacitor C_1.(and C_2)

A value of 0.155pF for C_1 and C_2, gave a phase margin of some 55°. (see Fig.6.35)

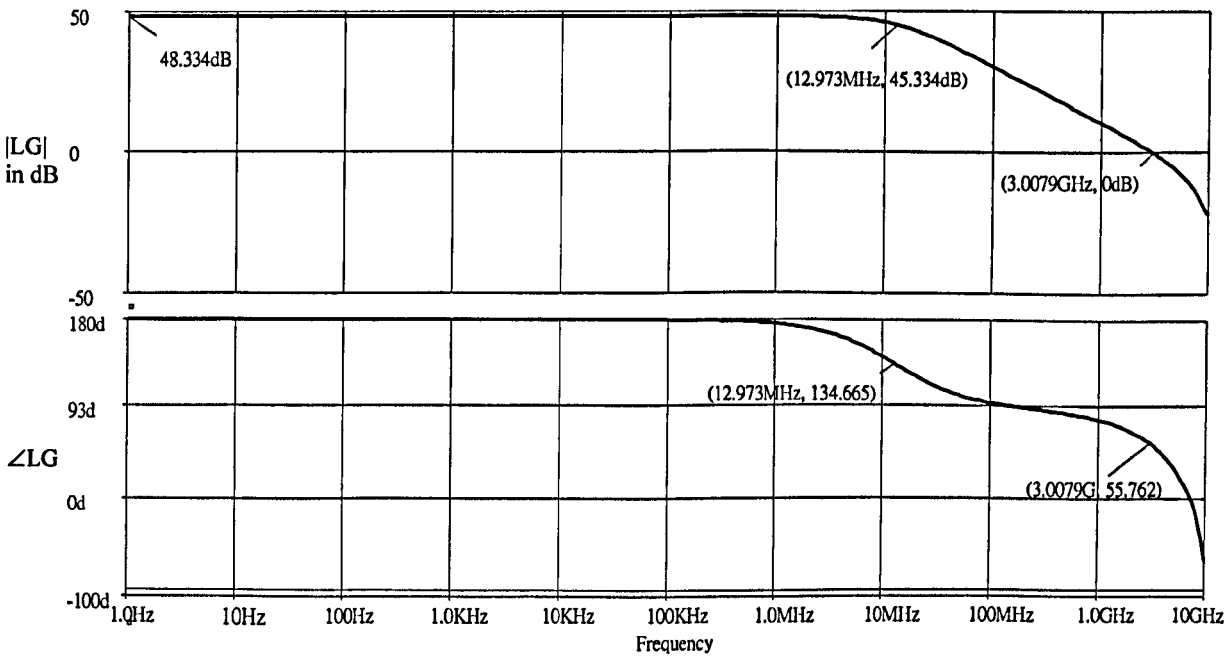


Figure 6.34 Loop-gain magnitude and phase plots for Fig 6.33

In Fig 6.25 the capacitance associated with the gate of M_8 is actually greater then 0.155pF because of the gate input capacitance.

This was intentionally discounted because the gate capacitance could not be calculated with a great deal of accuracy.

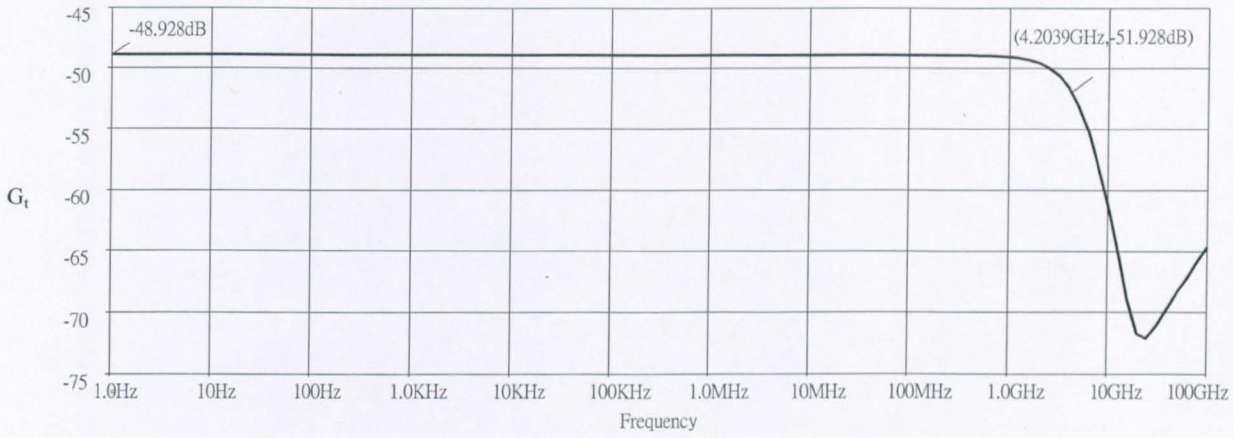


Figure 6.35 G_t vs. f for the DGFC 2 and DGFC 3

The resultant small signal frequency response, shown in Fig 6.35 indicates a bandwidth of 4.2GHz.

6.5.3 Distortion

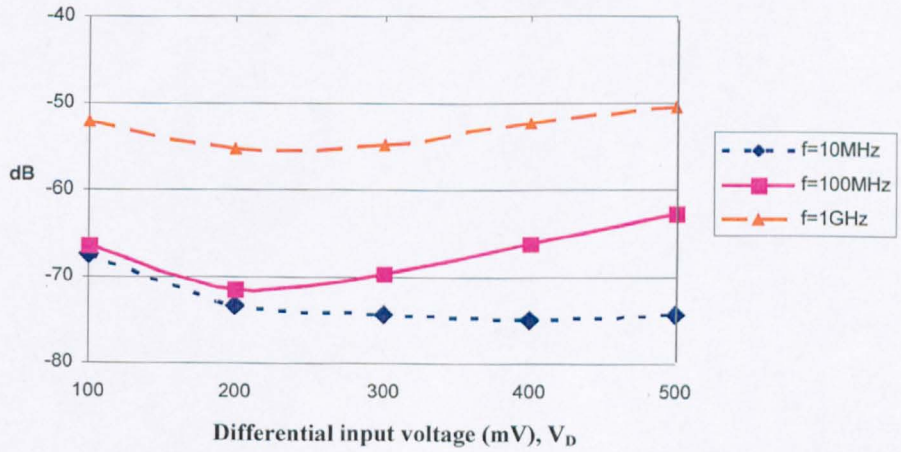


Figure 6.36 THD vs. V_D for the DGFC 2 and DGFC 3

From Fig.6.36, which shows the variation of THD with V_D and frequency it is evident that in the worst case (V_D=500mV and f=1GHz) the THD is -50dB. An output frequency spectrum is shown in Fig.6.37.

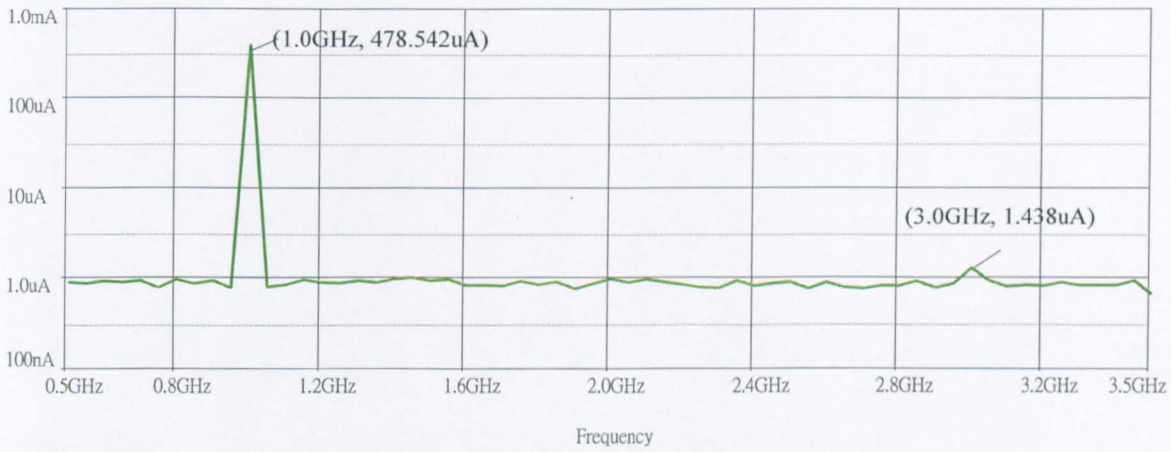


Figure 6.37 Output Frequency spectrum for f=1GHz, V_D=500mV.

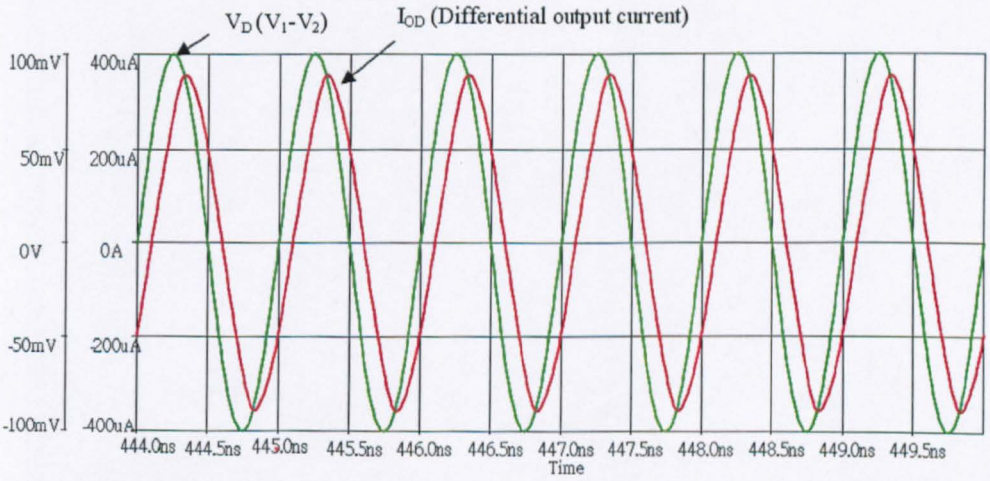


Figure 6.38 Showing I_{OD} for V_D=100mV, f=1GHz

Fig.6.38 shows the quality of the differential output current (I_{OD}) for a 100mV differential input signal at f=1GHz.

6.5.4 Terminal impedances

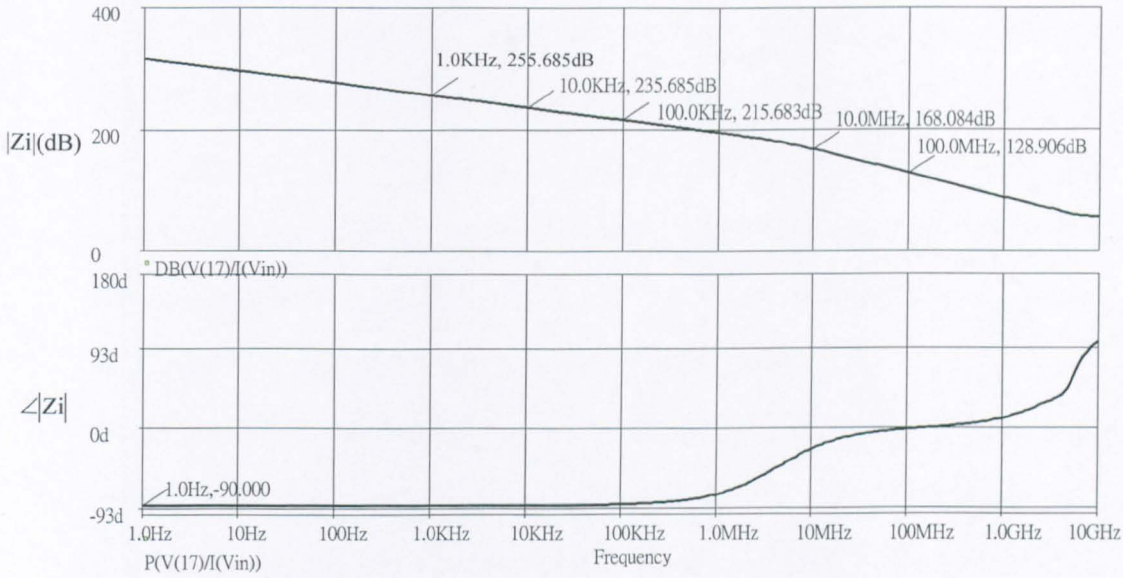


Figure 6.39 The input impedance at the gate of M_4 with the gate of M_5 earthed.

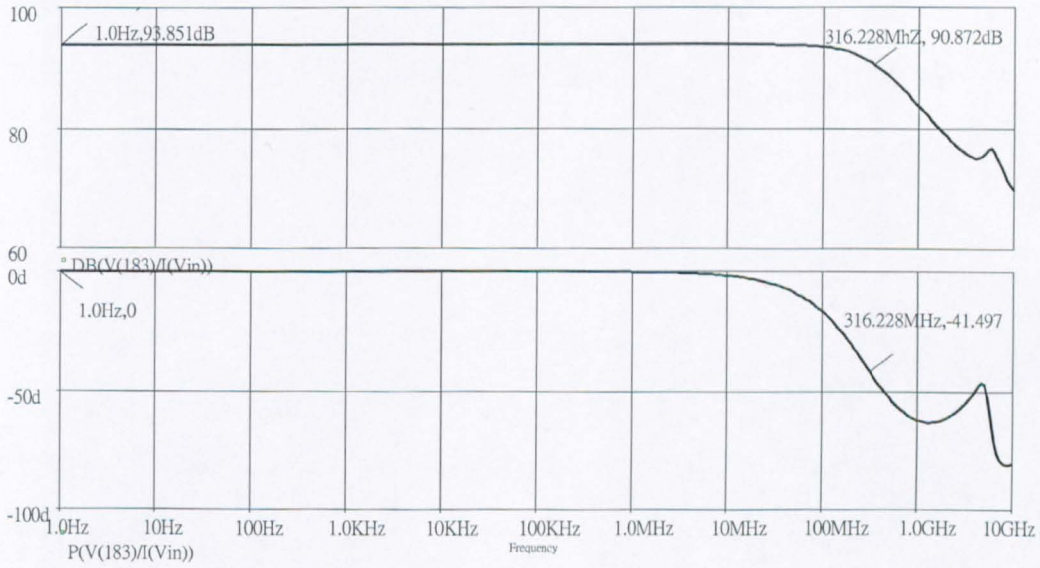


Figure 6.40 Output impedance of M_{17} and M_{18} with $V_1=V_2=0V$

6.6 Summary and conclusions

Shortly before the research work described in this chapter was done, the word 'Flipped' had been employed to categorize a type of source-follower in which the drain current was held constant, by the use of some negative feedback scheme, in order to improve the linearity in its DC voltage transfer characteristic and decrease its incremental output impedance: hence, the short-form description FVF (Flipped Voltage Follower) has been used in published papers using it.

The first part of the chapter demonstrated two shortcomings of the prototype FVF, namely, the limited (and, in some applications, unacceptably small) linear input voltage range or the requirement for an ancillary voltage bias circuit, and showed how these could be overcome by proposed circuit modifications that are thought to be novel.

The resulting circuit comes under the classification FFVF.(Folded Flipped Voltage Follower)

In this the input voltage range is maximised for given sail supplies. This makes the circuit potentially useful, as a unit or 'cell' in the design of a variety of low-voltage systems.

The second part of the chapter considered the particular use of the proposed FFVF in the design of a V-I converter. The first circuit to emerge, the DGFC1, showed a current gain in the output stages that was not considered sufficiently predictable.

The DGFC 2 overcome this problem but at the cost of higher rail voltages, +/-2.5V instead of +/-1.5V.

A development of this, the DGFC 3, showed a temperature-insensitive linear input voltage range.

Future work could involve the development of a circuit with the performance characteristics of DGFC 2, or DGFC 3, but using +/- 1.5V rail supplies.

6.7 References

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[6.3] Gray P. R., Hurst P. J., Lewis S. H. and Meyer R. G., 'Analysis and Design of Analog Integrated Circuits', John Wiley & Sons, Inc., Fourth Edition, New York, 2001, pp. 213-215

[6.4] Behbahani F., Fotowat A., Navid S., Gaethke R. and Delurio M., 'A Low Distortion Bipolar Mixer for Low Voltage Direct Up-Conversion and High IF Systems', IEEE Transactions on Solid-State Circuits, Vol. 32, No.9, Sept. 1997, pp. 1446-1450

[6.5] Huang H. W., Hsieh W. L., Chen K. H., 'Programmable Voltage-to-Current Converter with Linear Voltage Control Resistor', IEEE, Circuits and systems, ISCAS 2008, May 2008, pp. 2310-2313

[6.6] Chen C. M., Hayatleh K., Hart B. L. and Lidgey F. J., 'Wideband differential V/I converter ', Accepted and awaiting publication in International Journal of Electronics

6.8 Appendix 6

Appendix 6.1 Small Signal calculations for a half-circuit

Calculation of G_t

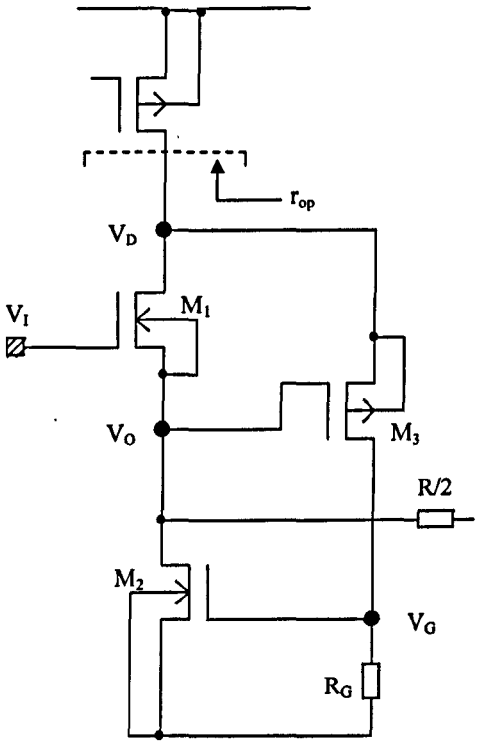

Figure A 6.1 Half-circuit of a DGFC

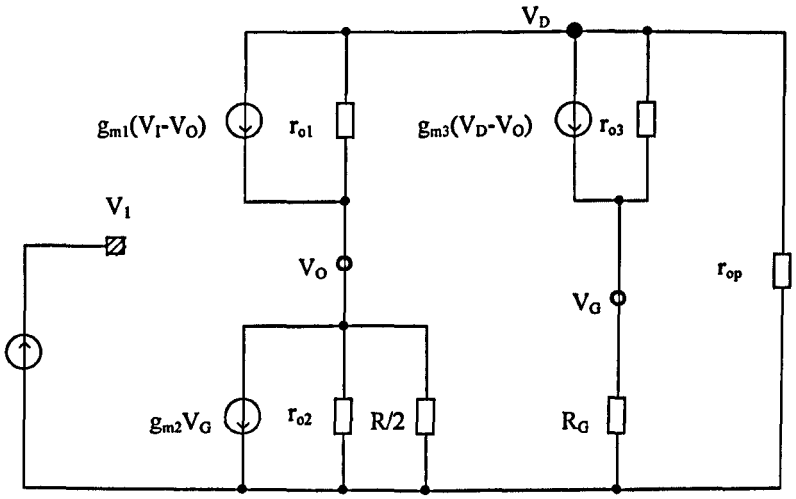

Figure A 6.2 Small-signal equivalent circuit for transconductance analysis

Referring to Figs. A 6.1, A6.2, Kirchhoff's Current Laws give:

$$g_{m1}(V_I - V_O) + \frac{V_D - V_O}{r_{o1}} - g_{m2}V_G - \left(\frac{1}{r_{o2}} + \frac{2}{R}\right)V_O = 0 \qquad \text{(A 6.1)}$$

$$-\left(g_{m1} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} + \frac{2}{R}\right)V_O + \frac{1}{r_{o1}}V_D - g_{m2}V_G = -g_{m1}V_I \qquad \text{(A 6.1.1)}$$

$$g_{m3}(V_D - V_O) + \frac{V_D - V_G}{r_{o3}} - \frac{V_G}{R_G} = 0 \qquad \text{(A 6.2)}$$

$$-g_{m3}V_O + \left(g_{m3} + \frac{1}{r_{o3}}\right)V_D - \left(\frac{1}{r_{o3}} + \frac{1}{R_G}\right) = 0 \qquad \text{(A 6.2.1)}$$

$$g_{m2}V_G + \left(\frac{1}{r_{o2}} + \frac{2}{R}\right)V_O + \frac{V_G}{R_G} + \frac{V_D}{r_{op}} = 0 \qquad \text{(A 6.3)}$$

$$\left(\frac{1}{r_{o2}} + \frac{2}{R}\right)V_O + \frac{1}{r_{op}}V_D + \left(g_{m2} + \frac{1}{R_G}\right)V_G = 0 \qquad \text{(A 6.3.1)}$$

Putting eqns A 6.1.1, A6.2.1 and A 6.3.1, into determinant form,

$$\begin{vmatrix} -\left(g_{m1} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} + \frac{2}{R}\right) & \frac{1}{r_{01}} & -g_{m2} \\ -g_{m3} & +\left(g_{m3} + \frac{1}{r_{o3}}\right) & -\left(\frac{1}{r_{03}} + \frac{1}{R_G}\right) \\ \left(\frac{1}{r_{02}} + \frac{2}{R}\right) & \frac{1}{r_{op}} & \left(g_{m2} + \frac{1}{R_G}\right) \end{vmatrix} \cdot \begin{vmatrix} V_O \\ V_D \\ V_G \end{vmatrix} = \begin{vmatrix} -g_{m1}V_I \\ 0 \\ 0 \end{vmatrix} \qquad \text{(A 6.4)}$$

This is of the form [5.4],

$$\begin{vmatrix} a_1 & b_1 & c_1 \\ a_2 & b_2 & c_2 \\ a_3 & b_3 & c_3 \end{vmatrix} \cdot \begin{vmatrix} V_O \\ V_D \\ V_G \end{vmatrix} = \begin{vmatrix} k_1 \\ k_2 \\ k_3 \end{vmatrix} \qquad \text{(A 6.5)}$$

where, $a_1 = -\left(g_{m1} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} + \frac{2}{R}\right)$

$a_2 = -g_{m3}$

$a_3 = \left(\frac{1}{r_{01}} + \frac{2}{R}\right)$

$b_1 = \frac{1}{r_{01}}$

$b_2 = \left(g_{m3} + \frac{1}{r_{o3}}\right)$

$b_3 = \frac{1}{r_{op}}$

$c_1 = -g_{m2}$

$c_2 = -\left(\frac{1}{r_{03}} + \frac{1}{R_G}\right)$

$c_3 = \left(g_{m2} + \frac{1}{R_G}\right)$

$k_1 = -g_{m1}V_G$

$k_2 = 0$

$k_3 = 0$

The voltage gain (V_G/V_I) is given:

$$\frac{V_G}{V_I} = \frac{-g_{m1}(a_2b_3 - a_3b_2)}{a_1b_2c_3 + a_3b_1c_2 + a_2b_3c_1 - a_3b_2c_1 - a_1b_3c_2 - a_2b_1c_3} \qquad \text{(A 6.6)}$$

If we assume that r_{o1}, r_{o2} are infinite then the variables become:

$a_1 = -\left(g_{m1} + \frac{2}{R}\right)$

$a_2 = -g_{m3}$

$a_3 = \frac{2}{R}$

$b_1 = 0$

$b_2 = \left(g_{m3} + \frac{1}{r_{o3}}\right)$

$b_3 = \frac{1}{r_{op}}$

$c_1 = -g_{m2}$

$c_2 = -\left(\frac{1}{r_{03}} + \frac{1}{R_G}\right)$

$$c_3 = \left(g_{m2} + \frac{1}{R_G}\right)$$

Equation A6.6 rearranged gives:

$$\frac{V_G}{V_I} = \frac{-g_{m1}(a_2b_3 - a_3b_2)}{a_1b_2c_3 + a_2b_3c_1 - a_3b_2c_1 - a_1b_3c_2} = \frac{-g_{m1}(a_2b_3 - a_3b_2)}{a_1(b_2c_3 - b_3c_2) + c_1(a_2b_3 - a_3b_2)}$$

(A6.6.1)

Substituting for a1, etc. into A6.6.1 is gives:

$$\frac{V_G}{V_I} = \frac{-g_{m1}\left[-(g_{m3})\cdot\left(\frac{1}{r_{op}}\right) - \left(\frac{2}{R}\right)\cdot\left(g_{m3} + \frac{1}{r_{03}}\right)\right]}{-\left(g_{m1} + \frac{2}{R}\right)\cdot\left[\left(g_{m3} + \frac{1}{r_{03}}\right)\cdot\left(g_{m2} + \frac{1}{R_G}\right) + \left(\frac{1}{r_{op}}\right)\cdot\left(\frac{1}{r_{03}} + \frac{1}{R_G}\right)\right] + (g_{m2})\left[(g_{m3})\cdot\left(\frac{1}{r_{op}}\right) + \left(\frac{2}{R}\right)\cdot\left(g_{m3} + \frac{1}{r_{03}}\right)\right]}$$

(A6.6.2)

But, $G_t = 2g_mV_G$. Using A 6.6.1 and the output current becomes:

$$I_o = 2\cdot g_m \cdot \frac{V_I\cdot[-g_{m1}(a_2b_3 - a_3b_2)]}{(a_1b_2c_3 + a_2b_2c_1 - a_3b_2c_1 - a_1b_3c_2)} \qquad \text{(A 6.7)}$$

The input voltage of the full circuit is $(V_1\text{-}V_2)$

The G_t is given by,

$$G_t = \frac{I_o}{V_1 - V_2} = \frac{-g_{m2}\cdot g_{m1}(a_2b_3 - a_3b_2)}{(a_1b_2c_3 + a_2b_2c_1 - a_3b_2c_1 - a_1b_3c_2)} \qquad \text{(A 6.7.1)}$$

Hence,

$$G_t = \frac{g_{m2}\cdot g_{m1}\left[(g_{m3})\cdot\left(\frac{1}{r_{op}}\right) + \left(\frac{2}{R}\right)\cdot\left(g_{m3} + \frac{1}{r_{03}}\right)\right]}{-\left(g_{m1} + \frac{2}{R}\right)\cdot\left[\left(g_{m3} + \frac{1}{r_{03}}\right)\cdot\left(g_{m2} + \frac{1}{R_G}\right) + \left(\frac{1}{r_{op}}\right)\cdot\left(\frac{1}{r_{03}} + \frac{1}{R_G}\right)\right] + (g_{m2})\left[(g_{m3})\cdot\left(\frac{1}{r_{op}}\right) + \left(\frac{2}{R}\right)\cdot\left(g_{m3} + \frac{1}{r_{03}}\right)\right]}$$

(A 6.7.2)

For the normal case $g_{m3} >> 1/r_{o3}$ (since $\mu_3 >> 1$) and the special case $r_{op} \rightarrow \infty$,

$$G_t = \frac{g_{m2} \cdot g_{m1} \cdot g_{m3} \cdot \frac{2}{R}}{-\left(g_{m1} + \frac{2}{R}\right) \cdot \left[(g_{m3}) \cdot \left(g_{m2} + \frac{1}{R_G}\right)\right] + (g_{m2}) \left[\left(\frac{2}{R}\right) \cdot (g_{m3})\right]} \qquad \text{(A 6.7.3)}$$

Dividing by $\left(g_{m2} \cdot g_{m3} \cdot \frac{2}{R}\right)$

$$G_t = \frac{g_{m1}}{2 + \frac{1}{g_{m2} R_G} - \frac{g_{m1} \cdot R}{2} - \frac{g_{m1} \cdot R}{2 \cdot R_G g_{m2}}} \qquad \text{(A 6.7.4)}$$

Since $(g_{m1}R/2) >> 2$, $(1/g_{m2}R_G)$, $(g_{m1}R/2R_G g_{m2})$,

$$G_t \cong \frac{2}{R} \qquad \text{(A 6.7.5)}$$

Calculation of open-loop gain

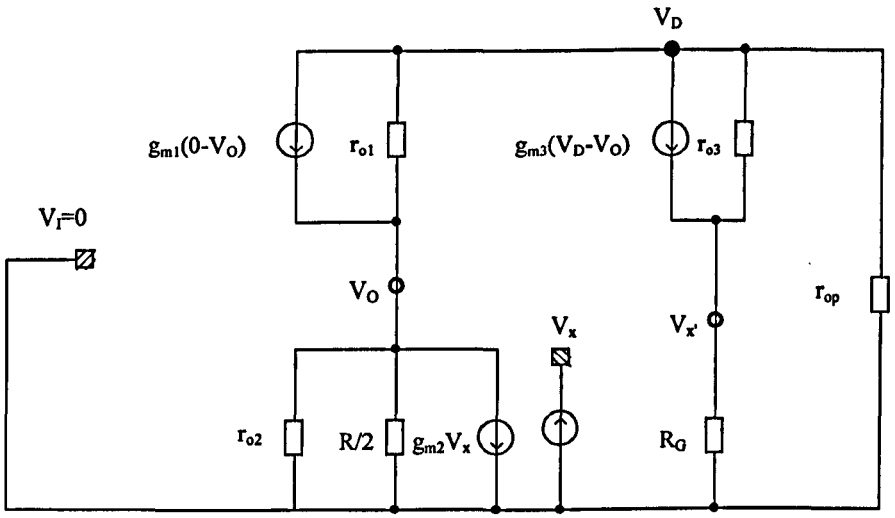

Figure A 6.3 small-signal equivalent circuit for open-loop gain analysis

Referring to Fig A6.3, and applying KCL gives:

$$-g_{m1} V_O + \frac{V_D - V_O}{r_{01}} - \left(\frac{1}{r_{o2}} + \frac{2}{R}\right) V_O = g_{m2} V_x \qquad \text{(A 6.8)}$$

$$\therefore -\left(g_{m1} + \frac{1}{r_{o1}} + \frac{1}{r_{02}} + \frac{2}{R}\right) V_O + \left(\frac{1}{r_{o1}}\right) V_D = g_{m2} V_x \qquad \text{(A 6.8.1)}$$

$$g_{m3}(V_D - V_O) + \frac{V_D - V_x'}{r_{o3}} - \frac{V_x'}{R_G} = 0 \qquad \text{(A 6.9)}$$

$$\therefore -g_{m3}V_O + \left(g_{m3} + \frac{1}{r_{o3}}\right)V_D - \left(\frac{1}{r_{o3}} + \frac{1}{R_G}\right)V_x' = 0 \qquad \text{(A 6.9.1)}$$

$$\left(\frac{1}{r_{o2}} + \frac{2}{R}\right)V_O + \frac{V_D}{r_{op}} + \frac{V_x'}{R_G} = -g_{m2}V_x \qquad \text{(A 6.10)}$$

Putting eqns A 6.8.1, A 6.9.1 and A 6.10, into determinant form:

$$\begin{vmatrix} -\left(g_{m1} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} + \frac{2}{R}\right) & \frac{1}{r_{o1}} & 0 \\ -g_{m3} & \left(g_{m3} + \frac{1}{r_{03}}\right) & -\left(\frac{1}{r_{03}} + \frac{1}{R_G}\right) \\ \left(\frac{1}{r_{o2}} + \frac{2}{R}\right) & \frac{1}{r_{op}} & \frac{1}{R_G} \end{vmatrix} \cdot \begin{vmatrix} V_O \\ V_D \\ V_x' \end{vmatrix} = \begin{vmatrix} g_{m2}V_x \\ 0 \\ -g_{m2}V_x \end{vmatrix} \qquad \text{(A 6.11)}$$

A simplified determinate matrix is given;

$$\begin{vmatrix} a_1' & b_1' & c_1' \\ a_2' & b_2' & c_2' \\ a_3' & b_3' & c_3' \end{vmatrix} \cdot \begin{vmatrix} V_O \\ V_D \\ V_x' \end{vmatrix} = \begin{vmatrix} k_1' \\ 0 \\ k_3' \end{vmatrix} \qquad \text{(A 6.12)}$$

We now calculate the open loop gain from eqn. A 6.11 and A 6.12 ($k_1'=-k_3'=g_{m2}V_x$)

$$\frac{V_x'}{V_x} = \frac{g_{m2}(a_2'b_1' + a_2'b_3' - a_1'b_2' - a_3'b_2')}{a_1'b_2'c_3' + a_3'b_1'c_2' + a_2'b_3'c_1' - a_3'b'c_1' - a_1'b_3'c_2' - a_2'b_1'c_3'} \qquad \text{(A 6.13)}$$

where, $a_{1'} = -\left(g_{m1} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} + \frac{2}{R}\right)$

$a_{2'} = -g_{m3}$

$a_{3'} = \left(\frac{1}{r_{02}} + \frac{2}{R}\right)$

$b_{1'} = \frac{1}{r_{01}}$

$$b_{2'} = \left(g_{m3} + \frac{1}{r_{o3}}\right)$$

$$b_{3'} = -\frac{1}{r_{op}}$$

$$c_{1'} = 0$$

$$c_{2'} = -\left(\frac{1}{r_{03}} + \frac{1}{R_G}\right)$$

$$c_{3'} = \frac{1}{R_G}$$

$$k_1' = g_{m2}V_x$$

$$k_2' = 0$$

$$k_3' = -g_{m2}V_x$$

Because $c_{1'} = 0$ eqn.A 6.13 is simplified as below,

$$\frac{V_x'}{V_x} = \frac{g_{m2}(a_2'b_1' + a_2'b_3' - a_1'b_2' - a_3'b_2')}{a_1'b_2'c_3' + a_3'b_1'c_2' - a_1'b_3'c_2' - a_2'b_1'c_3'} \qquad \text{(A 6.13.1)}$$

If we assume that r_{o1} and r_{o2} are infinite then eqn A 6.13.1 becomes

$$\frac{V_x'}{V_x} = \frac{g_{m2}[a_2'(b_1' + b_3') - b_2'(a_1' + a_3')]}{a_1'[b_2'c_3' - b_3'c_2'] + b_1'[a_3'c_2' - a_3'c_3']} = \frac{g_{m2}[a_2'b_3' - b_2'(a_1' + a_3')]}{a_1'[(b_2'c_3') - (b_3'c_2')]} \qquad \text{(A 6.14)}$$

Substituted those variables into A 6.14 then the loop gain is given,

$$\frac{V_x'}{V_x} = \frac{g_{m2}\left[\frac{g_{m3}}{r_{op}} + \left(g_{m3} + \frac{1}{r_{o3}}\right)\cdot\left(g_{m1} + \frac{4}{R}\right)\right]}{-\left(g_{m1} + \frac{2}{R}\right)\left[\left(g_{m3} + \frac{1}{r_{o3}}\right)\cdot\left(\frac{1}{R_G}\right) - \left(\frac{1}{r_{op}}\right)\cdot\left(\frac{1}{r_{o3}} - \frac{1}{R_G}\right)\right]} \qquad \text{(A 6.15)}$$

Assuming again that $r_{op}=\infty$ and $g_{m3} >> 1/r_{o3}$ then,

$$\frac{V_x'}{V_x} = \frac{g_{m1}\cdot g_{m2} + g_{m2}\cdot\frac{4}{R}}{-g_{m1}\cdot\frac{1}{R_G} + \frac{2}{R}\cdot\frac{1}{R_G}} \qquad \text{(A 6.16)}$$

Appendix 6.2 DC conditions in the DGFC2 and DGFC3 (with both inputs earthed)

DC conditions in DGFC 2 at 27°C:

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	2.5000	(2)	-2.5000	(3)	1.5811	(4)	-.2300
(5)	-.2300	(6)	0.0000	(7)	-.6471	(8)	-1.4026
(9)	-1.9126	(10)	-1.9126	(11)	-2.5000	(12)	-2.5000
(13)	-2.3235	(14)	-1.8834	(16)	-2.3235	(17)	0.0000
(18)	-.6471	(19)	-.2300	(20)	-.2300	(21)	-1.4026
(22)	-1.9126	(23)	-2.5000	(24)	-2.5000	(25)	-1.8834
(26)	1.5811	(28)	-1.9126	(71)	-.6471	(81)	-1.4026
(100)	0.0000	(101)	0.0000	(181)	-.6471	(182)	-.6471
(201)	-1.2940	(202)	-1.2940	(203)	-1.2940	(204)	-1.2940
(210)	-1.4026						

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VDD	-5.882E-03
VSS	5.882E-03
VD	0.000E+00
Vcm	0.000E+00
va1	1.193E-03
va2	1.193E-03
va3	1.086E-03
va4	1.149E-03
va5	4.412E-05
va6	-9.148E-19
va7	1.205E-03
va8	1.086E-03
va9	1.149E-03
va10	4.412E-05
va11	1.149E-03
va12	1.149E-03
va13	1.205E-03
va14	1.149E-03
va15	1.205E-03
va16	1.149E-03
va17	1.205E-03

DC conditions in DGFC 3 at 27°C:

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	2.5000	(2)	-2.5000	(3)	1.6002	(4)	-.2196
(5)	-.2196	(6)	0.0000	(7)	-.6347	(8)	-1.3815
(9)	-1.9241	(10)	-1.9241	(11)	-2.5000	(12)	-2.5000
(13)	-2.3311	(14)	-1.8933	(16)	-2.3311	(17)	0.0000
(18)	-.6347	(19)	-.2196	(20)	-.2196	(21)	-1.3815
(22)	-1.9241	(23)	-2.5000	(24)	-2.5000	(25)	-1.8933
(26)	1.6002	(28)	-1.9241	(2a)	.8457	(2b)	.0950
(3a)	-.0454	(3b)	-1.2204	(4a)	-.8457	(4b)	1.2204
(5a)	-.0088	(5b)	.0547	(6b)	-1.2204	(71)	-.6347
(81)	-1.3815	(100)	0.0000	(101)	0.0000	(181)	-.6347
(182)	-.6347	(201)	-1.2785	(202)	-1.2785	(203)	-1.2785
(204)	-1.2785	(210)	-1.3815	(21a)	1.6002	(21b)	-1.8933

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VDD	-8.590E-03
VSS	8.590E-03
VD	0.000E+00
Vcm	0.000E+00
va1	1.119E-03
va2	1.119E-03
va3	0.000E+00
va4	1.077E-03
va5	4.223E-05
va6	0.000E+00
va7	1.128E-03
va8	0.000E+00
va9	1.077E-03
va10	4.223E-05
va11	1.077E-03
va12	1.077E-03
va13	1.128E-03
va14	1.077E-03
va15	1.128E-03

va16	1.077E-03
va17	1.128E-03
va18	1.053E-03
va19	1.019E-03
va20	1.015E-03

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

This thesis has described novel MOSFET V-I converters and also explored some novel measurement techniques. Although the body effect in the MOSFET has been discussed in some text books [7.1,7.2], none of these sources illustrate clearly the relationship between threshold voltage and the substrate (body) voltage for short channel N and P channel MOSFET. Furthermore, the Early Voltage in the short channel length design of very high frequency MOSFET devices has been discussed in some papers [7.3, 7.4] but unfortunately there have been no detailed explanations of how to calculate the equivalent Early voltage from device simulation parameters. Therefore in Chapter 2 the DC and small-signal parameters of both N and P channel MOSFETs with a short channel length (L) of 0.13μm and channel width (W) of 10μm have been determined by simulation on test circuits and the results have been presented in tabular and/or graphical form. In addition, a measurement technique thought to be novel for the direct determination of the dependence of the transconductance ratios (g_m/g_{ds}) and (g_{mb}/g_m) has been proposed. Furthermore, tests were conducted to find the values of the inter-electrode capacitances C_{gs}, C_{gd}, C_{db}. Interestingly, textbook discussion on 'long channel devices' (L >> 1μm) generally neglect C_{gd}. However, for much shorter channel devices the value of C_{gd} was found to be significant, and therefore cannot be ignored.

Chapter 3, investigated three different types of current mirrors, (i) the Cascade, (ii) the Modified Wilson, and (iii) the 'High Compliance'. It was decided to adopt the cascode in preference to the other two because it gave comparable small-signal performance to that of the Modified Wilson but had a major advantage over it, namely, that the output impedance was independent of the resistance of the circuit driving it. However, the 'High Compliance' current mirror had the best frequency

response but was not regarded as acceptable for two reasons. First, because its DC output characteristic was no better than that of the other two. Second, it requires more MOSFETs (a minimum of 6) compared with the other current mirrors. Furthermore, in this chapter both the substrate and the temperature variation effects for a source follower are described in detail.

In Chapter 4, two types of MOSFET V-I converter designs (Type A and Type B) were critically reviewed. In Type A the transconductance, G_t, is determined by a chosen resistor whereas Type B designs require an accurate square-law relationship between I_D and V_{GS} and close device parameter matching. Therefore it was decided to concentrate on Type A designs. Two circuit configurations, the cross-coupled scheme, and a current-feedback scheme were investigated by simulation. In the cross-coupled case, the proposed constant range for G_t was limited by the MOSFET threshold voltage. Furthermore, both the cross-coupled circuit and the current feedback circuit suffered from an undesirable positive feedback loop. Then it was decided to revisit the long-tailed pair stage, with its associated degeneration resistor, to assess what improvements could be made in order to obtain acceptable and predictable performance for $G_t > 1$mS.

In Chapter 5 and 6, the design techniques for both DSFC and DGFC V-I circuits, were presented and described in detail. For fair comparison of these circuits, the bias current was chosen to be 1mA and the value of source degeneration resistor 600Ω [7-5]. Table7.1 below shows the comparative results for two novel V-I converters, namely, DSFC1(b) and DGFC3.

Table 7.1 A comparative table of two novel V-I converters

	DSFC 1(a)	DSFC 1(b)*	DGFC2	DGFC3
Gt (mS)	3.0302	3.3855	4.2685	3.5776
Gt at -3dB frequency		6.0321GHz		4.2039GHz
Zi at1GHz		21.226K		28.435K
Zo at 1GHz		30.613K		15.291K
THD at 1GHz (dB)		-57.84		-50.44
Power Dissipation(mW)		17.9		28

All those simulation results shown in Table 7.1 are based on linear operational range of V_D at +/- 500mV.

* This circuit works at +/- 1.5 rail voltages.

It is apparent that DSFC 1(b) has the most accrate value of transconductance because it is closer to the ideal G_t value of 3.3mS. Also the AC performance of DSFC 1(b) is clearly better than DGFC 3 because its -3dB cut-off frequency is more than 6 GHz and the THD performance is nearly 8dB lower than -50dB. However, both V-I converters do meet the target specification for this research work.

Both the (novel) circuits, DSFC 1(b) and DGFC 3, were designed are implemented with a new temperature compensation scheme [7.6] suitable for an industrial environment. This scheme is scheduled for publication in due course (40°C ~ +85°C).

7.2 Future work

Since competing the work described in this thesis, the author has started to explore some new ideas using a V-I converter technique employing a different type of follower. The work is on-going but early results show that the technique has considerable promise. In this section the underlying idea of the triple feedback

technique is presented, and brief circuit analysis gives step by step development from the initial sub-circuit to the final full circuit design.

7.2.1 Circuit outline and problems

Fig.7.1 shows a voltage amplifier with a differential long-tailed pair input stage with 100% negative feedback configured to operate as a unity-gain amplifier.

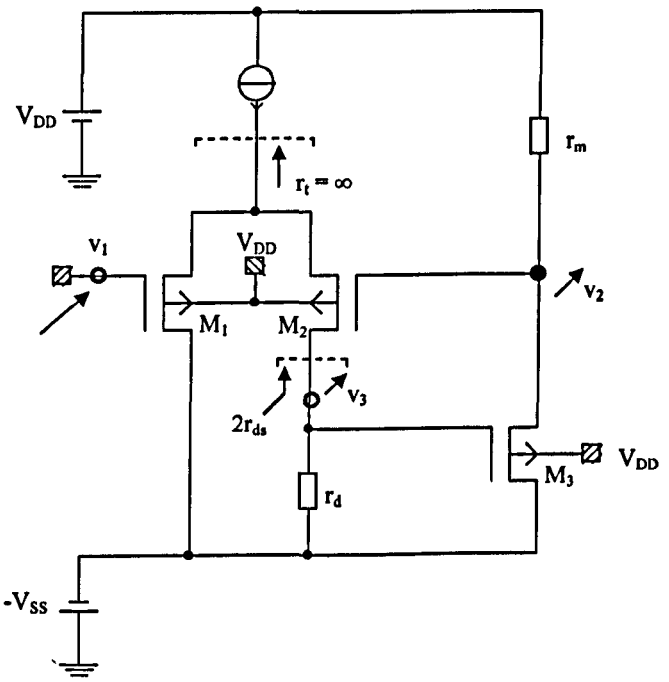

Figure 7.1 Long-tailed pair stage with feedback

Current change in M_1, M_2 when v_1 is applied is $g_m(v_1-v_2)$. Initially g_{mb} is ignored. The justification for this assumption will be given later.

$$v_3 = \frac{g_m}{2}(v_1 - v_2)[2r_{ds}//r_d] \qquad (7.1)$$

where, $2r_{ds}$ is the output resistance at drain of M_2 and r_d is the drain load resistance. The best we can get is $r_d \approx \infty$, or in practice, $r_d >> 2r_{ds}$ so r_d can be ignored.

Then, $v_3 = \frac{g_m}{2}(v_1 - v_2)2r_{ds} = g_m r_{ds}(v_1 - v_2)$ (7.2)

Get the voltage gain of the source follower based on M_3 be G_f

Then,

$$v_2 = G_f g_m r_{ds}(v_1 - v_2) = G_f \mu (v_1 - v_2) \text{ since } \mu \triangleq g_m r_{ds}$$

$$\therefore \quad v_2 = G_f \mu v_1 - G_f \mu v_2 \tag{7.3}$$

or $$\left(\frac{v_2}{v_1}\right) = \frac{G_f \mu}{1 + G_f \mu} = \frac{1}{1 + \frac{1}{G_f \mu}} \tag{7.4}$$

Now $$G_f = \frac{g_{m3}}{g_{m3} + g_{ds3} + \frac{1}{r_m}} = \frac{\mu_3}{1 + \mu_3 + \left(\frac{r_{ds3}}{r_m}\right)} \tag{7.5}$$

Note that $\mu_3 (=g_{m3}r_{ds3}) \neq \mu$, because M_3 operates at a different current, which affects the value of μ.

$$\frac{v_2}{v_1} = \frac{1}{1 + \left[\frac{1 + \mu_3 + \left(\frac{r_{ds3}}{r_m}\right)}{\mu_3}\right]\frac{1}{\mu}} \tag{7.6a}$$

$$\frac{v_2}{v_1} = \frac{1}{1 + \frac{1}{\mu} + \frac{1}{\mu\mu_3} + \left(\frac{r_{ds3}}{r_m}\right)\left(\frac{1}{\mu\mu_3}\right)} \tag{7.6b}$$

If $\left(\frac{r_{ds3}}{r_m}\right) \geq 1$ then,

$$\frac{v_2}{v_1} > \frac{1}{1 + \frac{1}{\mu} + \frac{2}{\mu\mu_3}} \tag{7.7a}$$

$$\frac{v_2}{v_1} > \frac{1}{1 + \frac{1}{\mu}\left(1 + \frac{2}{\mu_3}\right)} \tag{7.7b}$$

For $\mu_3 >> 2$

$$\frac{v_2}{v_1} \cong \frac{\mu}{1+\mu} \tag{7.8}$$

For $\mu_3 >> 30$, $\frac{v_2}{v_1} > \frac{30}{31}$

$$\frac{v_2}{v_1} \cong 0.97 \tag{7.9}$$

This analysis is only true for the un-loaded amplifier.

Suppose it is loaded by a resistance R (=300 Ω) then r_m (>>300 Ω)

in the expression for (v_1/v_2) must be replaced by R.

Now suppose $r_{ds3} \cong$ 1K Ω, then $r_{ds3}/R \cong 3$

Then, $$\left(\frac{v_1}{v_2}\right) = \frac{1}{1+\frac{1}{\mu}+\frac{1}{\mu\mu_3}+\frac{3}{\mu\mu_3}} \approx \frac{1}{1+\frac{1}{\mu}+\frac{4}{\mu\mu_3}} \tag{7.10}$$

Again, $$\left(\frac{v_1}{v_2}\right) \cong \frac{\mu}{(1+\mu)} = A, \text{ say} \tag{7.11}$$

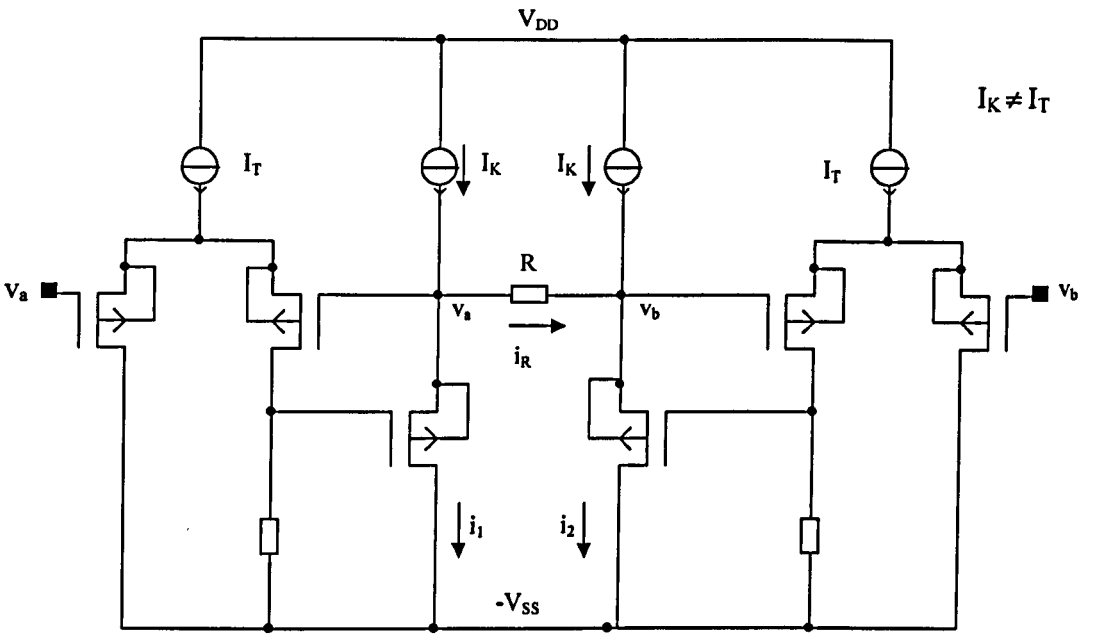

Figure 7.2 Schematic of the proposed V-I converter

$$\text{But,} \quad G_t \overset{\Delta}{=} \frac{d(i_2 - i_1)}{d(v_a - v_b)} = \frac{di_{out}}{dv_d} \tag{7.12}$$

where, $i_{out} \overset{\Delta}{=} (i_2 - i_1)$ and $v_d \overset{\Delta}{=} (v_a - v_b)$

But, $i_R = (v_a - v_b)/R$ and $i_2 = i_R$, $i_1 = -i_R$

$$\therefore, \quad G_t \cong \frac{2A}{R} \cong \frac{2}{R} \text{ if } A \cong 1 \tag{7.13}$$

Because $i_R = (v_a - v_b)/R$ and $i_2 = i_R$, $i_1 = -i_R$

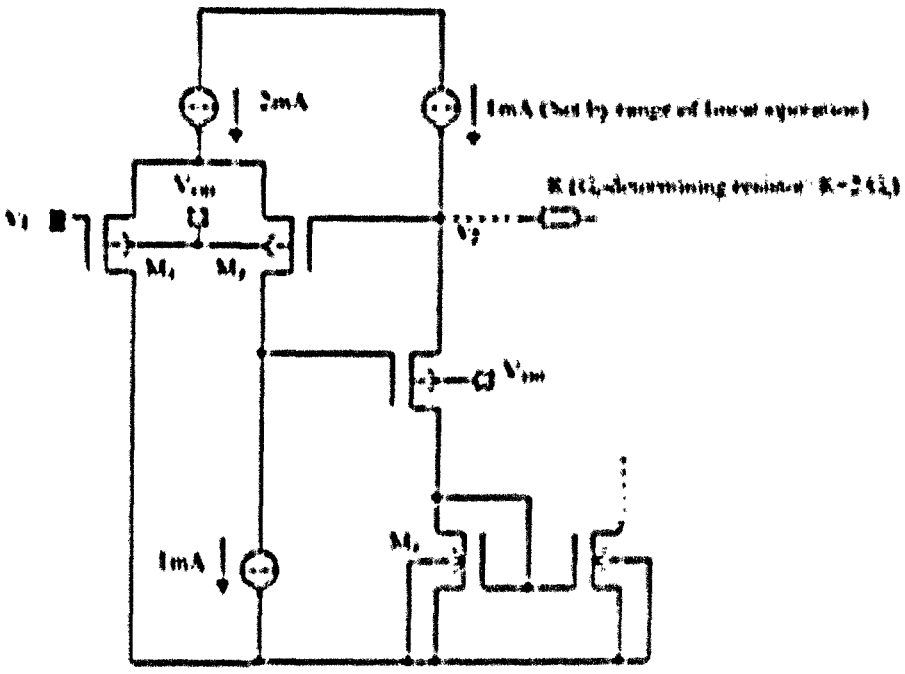

Figure 7.3 A half-circuit of the proposed V-I converter

Problems: (1) Substrate connections to V_{in} causes large V_{sb} for M_3, so insufficient drain voltage for current sink supplying 1mA to drain of M_2. Also g_{mb} problem.

(2) Operation with M_1, M_2 at 1mA means poor μ for these devices.

(3) Drain voltage of M_1 are always unequal.

(4) Simple current mirrors at the output do not give good, predictable current-transfer ratio. With 1mA current sink for M_2 drain its output resistance is only moderate, thus restricting follower loop-gain and overall closed-loop gain to be further from unity.

To minimise these problems we tie the p type substrates to their sources, operate at a low current in the I to p for higher μ. Equalise the drain voltage of M_1, M_2, (making

the theoretical analysis more accurate) Use +/- 2.5V supply rails instead of +/- 1.5V in order to accommodate the voltage requirement of cascode current mirror output stage.

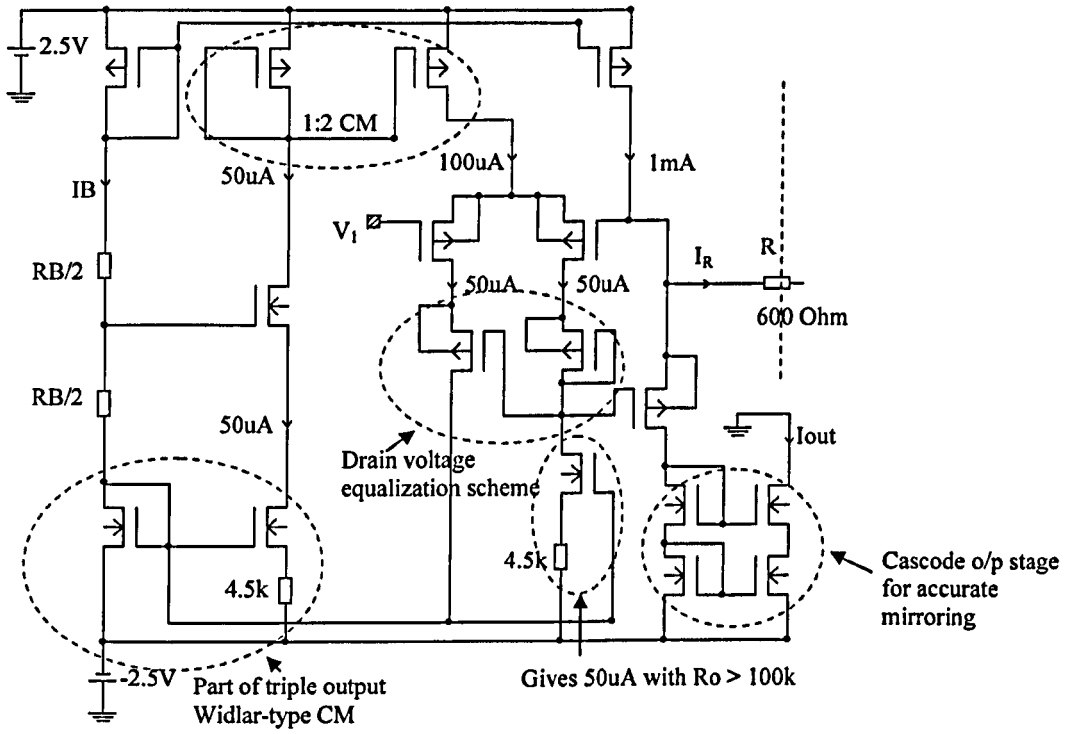

Figure 7.4 A detailed half-circuit of the proposed V-I converter

The G_t of the V-I converted described in this Future Work section is better than DSFC 1(b) and DGFC 3 circuits. Early results confirming this are shown in comparison Table7.2. In addition, some of the simulation results are contained in the appendices of this chapter to further establish that the circuit has potential.

Table7.2 A comparative table of two novel V-I converters and the future work

	DSFC 1(a)	DSFC 1(b)	DGFC2	DGFC3	Future Work
Gt (mS)	3.0302	3.3855	4.2685	3.5776	3.2908
Gt @-3dB frequency		6.0321GHz		4.2039GHz	1.6850GHz
Zi @1GHz		21.226K		28.435K	20.056K
Zo @1GHz		30.613K		15.291K	16.236K
THD @1GHz (dB)		-57.84		-50.44	
Power Dissipation(mW)		17.9		28	

All those simulation results in Table7.2 are based on linear operational range of V_D at +/- 500mV. *The circuit works at +/-1.5V rail voltages.

7.3 References

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[7.4] Galup-Montoro C.,Scgneider M. C. and Coitonho R. M., 'Resixing Rules for MOS Analog-Design Reuse', Design and Test of computers, IEEE, Vol. 19,Issue 2, Mar. 2002 pp.50-58

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7.4 Appendix 7

Appendix 7.1 Proposed full circuit and preliminary performance

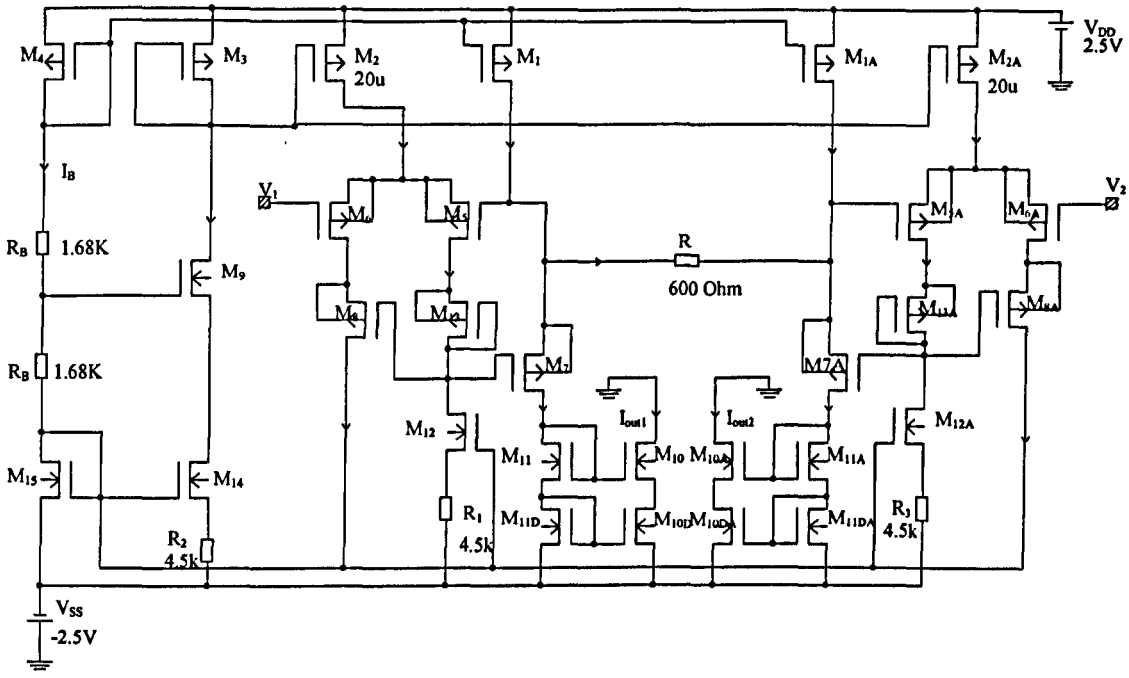

Figure A 7.1 A full proposed V-I converter

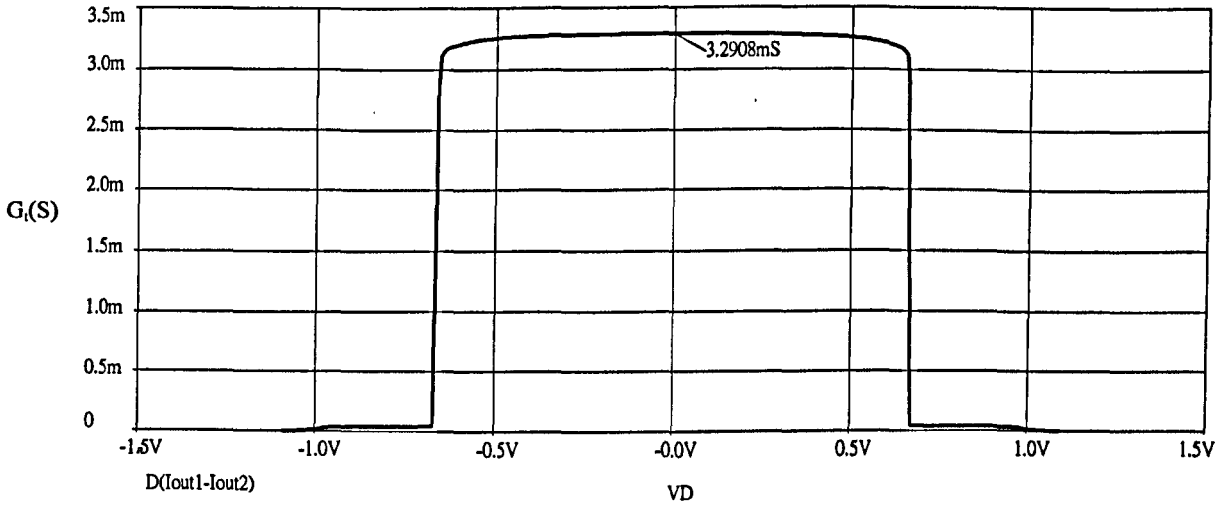

Figure A 7.2 Transconductance G_t of Fig. A 7.1

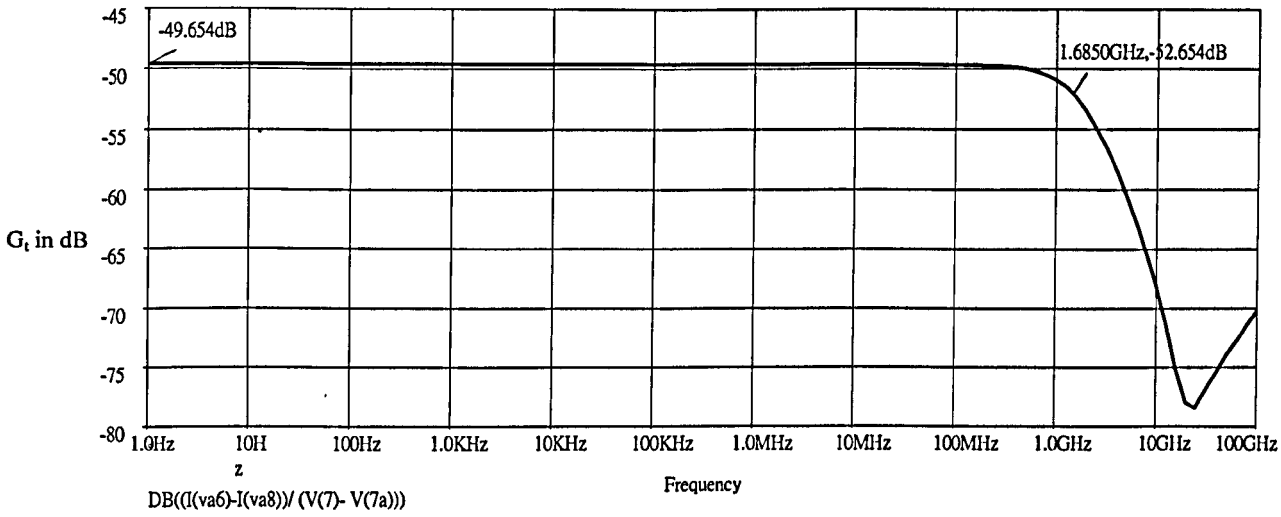

Figure A 7.3 Transconductance G_t vs. f of Fig. A7.1

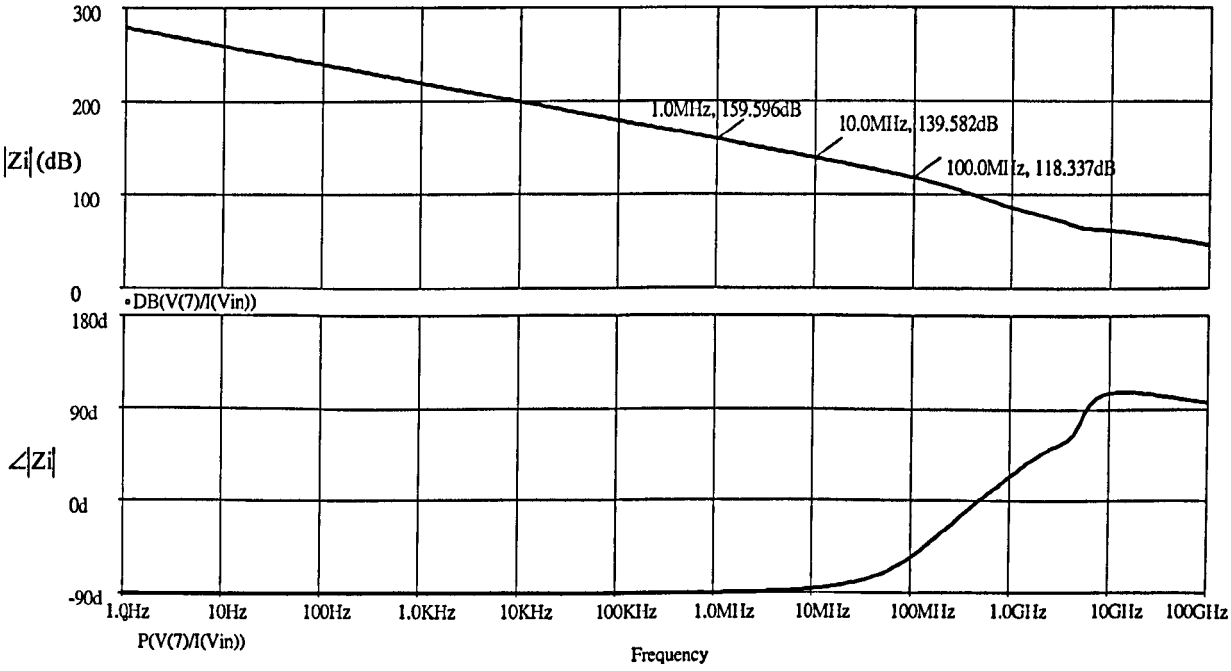

Figure A 7.4 Input impendence of Fig. A7.1

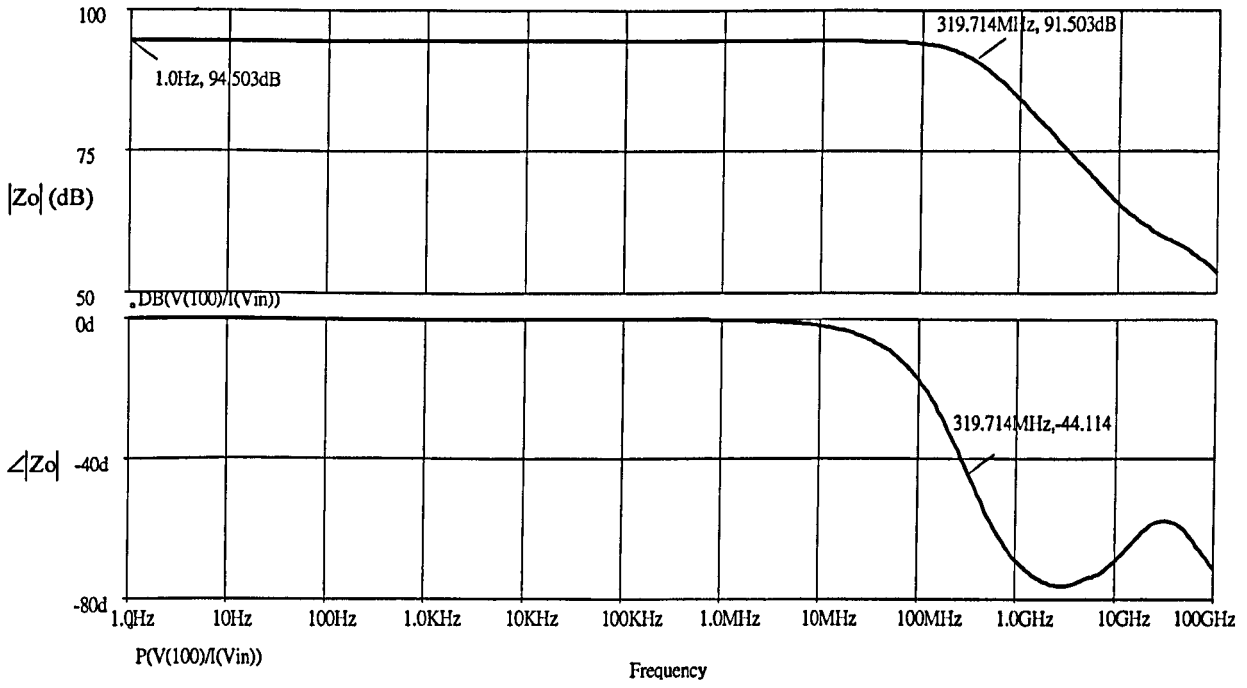

Figure A 7.5 Output impendence of Fig. A7.1

CHAPTER 8

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CHAPTER 9

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