Paper

Impact of Crosstalk into High Resistivity Silicon Substrate on the RF Performance of SOI MOSFET

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Abstract—Crosstalk propagation through silicon substrate is a serious limiting factor on the performance of the RF devices and circuits. In this work, substrate crosstalk into high resistivity silicon substrate is experimentally analyzed and the impact on the RF behavior of silicon-on-insulator (SOI) MOS transistors is discussed. The injection of a 10 V peak-to-peak single tone noise signal at a frequency of 3 MHz (f_{noise}) generates two sideband tones of −56 dBm separated by f_{noise} from the RF output signal of a partially depleted SOI MOSFET at 1 GHz and 4.1 dBm. The efficiency of the introduction of a trap-rich polysilicon layer located underneath the buried oxide (BOX) of the high resistivity (HR) SOI wafer in the reduction of the sideband noise tones is demonstrated. An equivalent circuit to model and analyze the generation of these sideband noise tones is proposed.

Keywords— crosstalk, high resistivity Si, mixing products, passivation layer, polysilicon.

1. Introduction

During the last 50 years the performance of silicon integrated circuits (ICs) has been growing exponentially thanks to the continuous downscaling of the transistors and components size. CMOS transistors have greatly increased their operating frequency and today ICs reach a high integration level of analog and digital circuits on the same silicon chip [1]. However, due to such extremely small dimensions the conventional bulk devices are facing many challenges, such as short-channel effects (SCE), junction capacitances and doping fluctuation [2].

In the recent years, silicon-on-insulator (SOI) technology, and more particularly SOI MOSFET, has attracted more attention due to its better scaling capability, higher isolation, reduced parasitic components and higher performance compared to bulk Si technology. As it is shown in Fig. 1, the buried oxide film (BOX) in SOI prevents the latch-up effect observed in bulk technology and reduces the substrate coupling mechanisms at low frequencies [2]. However, SOI technology suffers from parasitic effects such as floating body effect and self heating. These effects can be more or less pronounced depending on the SOI CMOS technology: fully (FD) or partially depleted (PD). The difference between these two families is the thickness of the maximum depletion zone above the buried oxide called the body. The fabrication and modeling of PD devices present substantially lower cost and complexity than those of FD devices, which is essentially related to the higher compatibility between bulk and PD SOI devices processing techniques. One of the main challenges that are associated with the PD SOI technology is the control of the floating body effect, which results from the generation of excess charges in the SOI body, which changes the channel potential, and changes the behavior of the MOSFET [3].

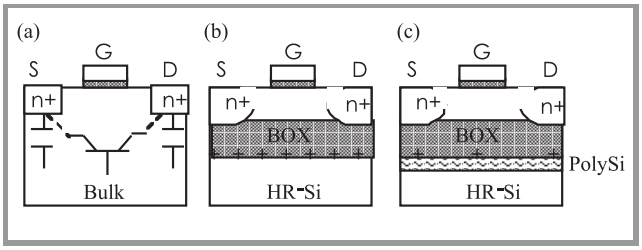

Fig. 1. nMOSFET cross section: (a) bulk technology, (b) HR-SOI, and (c) passivated HR-SOI technology.

The integration of CMOS and non-CMOS technologies into the same chip (systems-on-chip, SoC) is foreseen as a way to reduce the cost of each IC, and to fabricate smaller devices with higher performance and less power consumption [1]. A limiting factor of highly integrated electronics is the coupling through the common silicon substrate between the digital and the analog circuitries. In that sense, the main advantage of SOI compared to bulk Si is its compatibility with the use of high resistivity substrates to reduce substrate coupling and RF losses.

The introduction of high resistivity Si (HR-Si) substrate has converted silicon into a suitable technology for high frequency applications [4]. However, it is known that oxidized high resistivity substrate suffers from parasitic surface conduction (PSC) effect. Positive fixed charges inside the oxide attract electrons to the interface, creating an inversion/accumulation layer at the Si SiO_2 interface [5]. This thin highly conductive layer is responsible for the substrate losses. This issue can be overcome by introducing a trap-rich passivation layer between the oxide and the HR-Si substrate which captures the free carriers and locally depletes the HR-Si substrate. Several techniques can be used to generate such trap-rich layer: micromachined structures [6], ion implantation [7], and deposition of an amorphous silicon [8] or polycrystalline silicon layer [4].

In this paper, we investigate the RF behavior of a PD SOI MOSFET when a sinusoidal noise signal is injected through

a metallic pad close to the transistor. The introduction of a trap- rich polysilicon (PolySi) layer at the Si/SiO_2 interface of an oxidized HR-Si, as a way to reduce substrate crosstalk, is analyzed.

This paper is structured as follows. Firstly, a theoretical analysis of substrate crosstalk in bulk Si and SOI technologies is presented. Secondly, the impact of PSC effect in oxidized HR-Si and its reduction by using a polySi layer is demonstrated. Next, we describe the CMOS device and technology under analysis, as well as the measurement setup. Finally, we show and discuss the results obtained from the MOS structures lying on HR-Si substrates with and without passivation layer.

2. Theoretical Analysis of Substrate Crosstalk in Bulk Si and SOI Substrates

Crosstalk can be defined, in a more general way, as the electromagnetic disturbance induced by a circuit in another one, located nearby. From this general definition it can be deduced that any mechanism that creates such type of interference from a circuit into another falls into the crosstalk definition. In the case of mixed-mode high-frequency ICs, coupling through the substrate – the so-called substrate crosstalk – is one of the main origins of interferences. It is recognized as one of the most limiting factors in the performance of RF ICs [6].

For semiconductor substrates, crosstalk can be divided into two different mechanisms:

– injection into the substrate,

– propagation of this noise signal through the substrate.

It can be easily deduced that regardless of circuit design solutions, two different ways to reduce substrate crosstalk exist:

– substrate isolation,

– substrate coupling reduction.

As it is shown in [6], SOI substrate provides a higher isolation from the lossy Si thanks to its buried oxide layer (BOX) underneath the active layer. In combination with HR-Si it also effectively reduces conductive coupling through the substrate.

An extensive analysis of crosstalk in Si and SOI substrates has been presented in [6]. Hereafter, we briefly introduce some of the considerations related to crosstalk in Si substrates.

2.1. Crosstalk in Bulk Si Substrate

Silicon, as any semiconductor material, exhibits both conductive and dielectric characteristics, which can be translated into a resistive and a capacitive effect, respectively.

Resistive effect. At frequencies below a certain crossover frequency (f_s) the conductive nature of the semiconductor dominates over the dielectric behavior. Thus, the substrate can be modeled as purely resistive. The conductivity for a doped semiconductor is given by:

$$\sigma = q(p\mu_p + n\mu_n), \tag{1}$$

where q is the electron charge, and μ_n and μ_p represent the mobility of the electrons and holes carriers, respectively, and n and p stand for respective carrier densities.

While the effective carrier mobility depends also on the number of carriers (scattering effect), the expression (1) is dominated by the carrier concentration. We can say, as a first-order approximation, that the conductivity is an increasing function of the carrier densities.

Capacitive effect. At frequencies above the crossover frequency, the dielectric behavior of the semiconductor can no longer be neglected, thus the substrate must be modeled as a resistive and capacitive network as shown in Fig. 2.

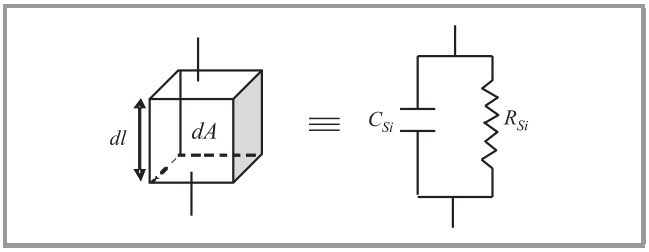

Fig. 2. Equivalent R-C model of a small piece of a homogeneous semiconductor substrate.

In the frequency domain the equivalent admittance Y_s for a piece of substrate is given by:

$$Y_S = \frac{1 + j\omega R_S C_S}{R_S} = \frac{1 + j\omega T_S}{R_S}, \tag{2}$$

where C_S is the associated substrate capacitance, R_S is the substrate equivalent resistance and T_S is the substrate time constant given by:

$$T_S = R_S C_S = \frac{\rho_S dl}{dA}\,\frac{\varepsilon_0 \varepsilon_{Si} dA}{dl} = \frac{\varepsilon_0 \varepsilon_{Si}}{q(p\mu_p + n\mu_n)}, \tag{3}$$

where ε_0 is the vacuum permittivity, ε_{Si} is the silicon permittivity, ω is the angular velocity, dl is the elementary length of the small piece of homogenous substrate and dA is its elementary area.

As it can be seen in Eq. (3), T_S is not related to the dimensions of the considered semiconductor volume but only to the substrate electrical properties.

At low frequencies, substrate resistance, R_S, is more important and the associated capacitance, C_S, can be neglected. As the pulsation ω increases, the impedance relative to the capacitive effect decreases to become equal to the that of the resistive effect at the crossover frequency, f_T, defined by:

$$f_T = \frac{1}{2\pi T_S} = \frac{Q(p\mu_p + n\mu_n)}{2\pi\varepsilon_0\varepsilon_{Si}}. \tag{4}$$

The lumped equivalent circuit representing the coupling between two metallic pads of same size lying on a bulk Si or a SOI substrate is shown in Fig. 3, where C_{Si} and R_{Si} describe the coupling effect between each pad and the back

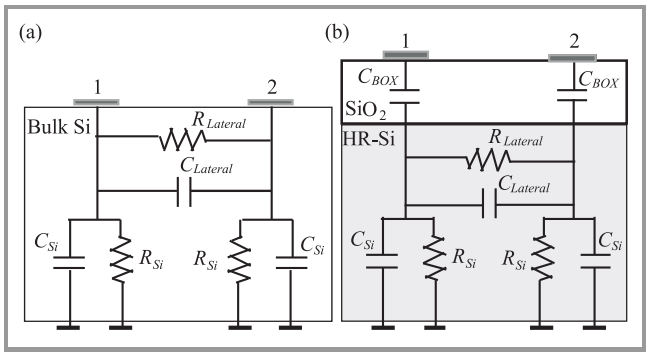

Fig. 3. Lumped equivalent R-C model substrate crosstalk in the case of (a) bulk Si and (b) SOI substrates.

side metallization. The propagation through the substrate is modeled by the elements $R_{Lateral}$ and $C_{Lateral}$. For identical pads with an area of $S_{pad} = W \times W$ and a spacing width d, the expressions of R_{Si}, C_{Si}, $R_{Lateral}$ and $C_{Lateral}$ derived from [6], are given by:

$$R_{Si} = \left[K \frac{\sigma_{Si} S_{pad}}{t_{Si}} \right]^{-1} \quad [\Omega], \tag{5}$$

$$C_{Si} = K \frac{\varepsilon_0 \varepsilon_{Si} S_{pad}}{t_{Si}} \quad [\mathrm{F}], \tag{6}$$

$$R_{Lateral} = \left[K \frac{\pi \sigma_{Si}}{4 \ln\left[\frac{\pi(d-W)}{W+t} + 1 \right]} W \right]^{-1} \quad [\Omega], \tag{7}$$

$$C_{Lateral} = K \frac{\pi \varepsilon_0 (\varepsilon_{Si} + 1)}{4 \ln\left[\frac{\pi(d-W)}{W+t} + 1 \right]} W \quad [\mathrm{F}], \tag{8}$$

where K is the fringing factor, t is the thickness of the conductors, t_{Si} is the Si substrate thickness and σ_{Si} is the Si substrate conductivity.

2.2. Crosstalk in SOI Substrate

Thanks to the presence of the buried oxide (BOX), the injection of signal to the silicon substrate is well reduced especially at low frequencies. As it can be seen in Fig. 3b, this can be modeled in the lumped equivalent circuit by a capacitance C_{BOX} between the pad and the silicon substrate, defined as:

$$C_{BOX} = K \frac{\varepsilon_0 \varepsilon_{ox} S}{t_{ox}}, \tag{9}$$

where ε_{ox} and t_{ox} are, respectively, the permittivity and thickness of the oxide layer.

As explained before, the propagation through the silicon substrate is modeled by the $R_{Lateral}$ and $C_{Lateral}$, which depend only on the Si properties. By reducing the conductivity of the silicon substrate in Eq. (7) we reduce this conductive coupling path through the substrate. This can be achieved by the use of a high resistivity (HR) SOI substrate.

However, because the buried oxide layer presents a low but not null density of oxide fixed charges and interface charges at the BOX/HR-Si interface region, a parasitic surface conduction (PSC) will greatly affect the equivalent resistance $R_{Lateral}$ in Eq. (7) by increasing the effective conductivity of silicon. In fact, an electron inversion layer is created producing a highly conductive surface layer. If a highly trap-rich layer (such as polysilicon) is deposited below the BOX and the Si substrate, these free carriers will be trapped and the parasitic conduction effect will be reduced. The nominal value of silicon resistivity is then recovered.

3. Impact of PSC Effect in HR-Si with and without a Trap-Rich Passivation Layer

To analyze the impact of the PSC effect in oxidized HR-Si we measure the attenuation of a coplanar waveguide (CPW) transmission line. CPW lines are used to characterize the interface properties due to their high sensitivity to the properties of the substrate surface they are printed on.

As explained before, the presence of fixed oxide charges in the silicon dioxide creates an inversion/accumulation layer at the Si/SiO_2 interface, hence increasing the conductivity at that zone. It has been demonstrated [9] that, for a CPW line, when a highly conductive layer is located between the top insulator and a high-resistivity substrate, the electric field is mainly located in the conductive layer, instead of going deeper into the substrate. The effective resistivity of the substrate is no longer the nominal value but a much lower value, typically one order of magnitude lower [7].

It has been demonstrated [7], [8], [10] that the impact of the PSC effect can be reduced by introducing traps at the Si/SiO_2 interface. These traps will freeze the free carriers, and by reducing their mobility, the nominal resistivity of the substrate will be recovered. The introduction of such a trap-rich passivation layer can be easily done by deposition of a polysilicon layer between the top oxide and the HR-Si substrate. This solution has the advantage that it is thermally stable and compatible with CMOS processes [9].

The extracted attenuation constants of a CPW line lying on different substrates are shown in Fig. 4. The CPW dimensions are 26 þm for the width (W) of the central conductor, 12 μm for the slot width (S), and 208 μm for the width of the planar ground conductors (Wg). Three different substrates are measured: a bulk Si with standard resistivity ($\rho = 20$ Ωcm), one HR-Si substrate with $\rho = 5$ kΩcm

and the same HR-Si substrate but including a sandwiched polySi layer of 287 nm-thick. In all cases front and back metal layers are 1 μm-thick aluminum and the thermal SiO_2 top layer is of 50 nm. As it can be observed, the CPW with the passivation layer is the line which presents the lowest attenuation level, at least 0.2 dB/mm lower than that of the same HR-Si substrate without passivation.

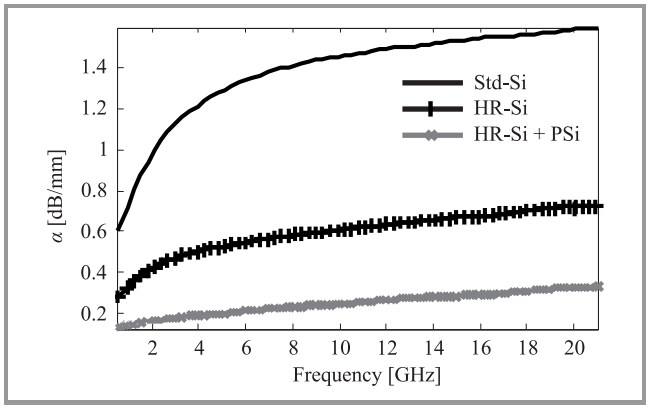

Fig. 4. Measured losses as a function of frequency for CPW line lying on three different Si substrates.

To have a more clear representation of the impact of the resistivity variation at the interface we can compare the effective resistivity of each substrate. It is calculated as described in [11], by comparing the extracted conductance of the RLCG equivalent circuit of the CPW transmission line with the one of a theoretical line with the same dimensions lying on a lossless Si substrate. The effective resistivity for the three different substrates is presented in Fig. 5. It can be clearly seen that the effective resistivity of the standard Si substrate remains closer to its nominal

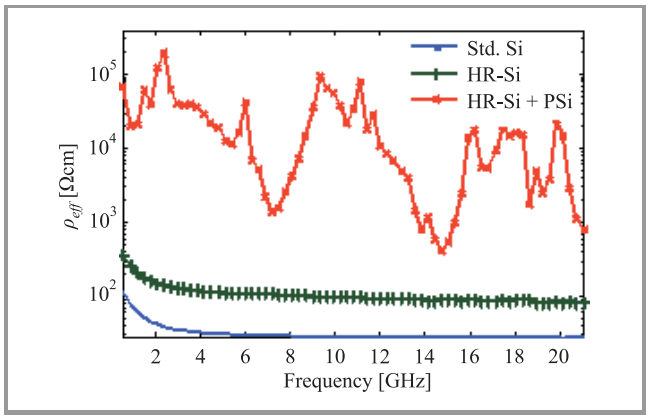

Fig. 5. Effective resistivity as a function of frequency for CPW line lying on three different Si substrates.

value, as expected since the PSC effect has a low impact on such type of substrate that already presents intrinsically a certain concentration of free carriers. However, for the HR-Si substrate the effective resistivity (p_{eff}) is approximately equal to 100 Ωcm. This value is 50 times lower than its nominal value. On the other hand, the same HR-Si substrate with a trap-rich passivation layer exhibits an effective resistivity which is kept higher than 1 kΩcm. The efficiency of the passivation layer to reduce the PSC effect is demonstrated as the high-resistivity characteristic of the oxidized HR-Si substrate is recovered. Similar conclusions can be extrapolated to substrate crosstalk, where thanks to the introduction of a trap-rich passivation layer the impact of the conductive layer below the oxide will effectively vanish, hence reducing the conductive coupling through the substrate.

4. Device and Measurement Setup Description

Two partially depleted PD SOI MOSFETS with gate lengths of 0.13 and 0.24 μm are used to analyze the impact of substrate crosstalk in their RF performance. Both PD MOSFETS are fabricated using a commercial 0.13 and 0.24 μm, respectively, SOI CMOS process by ST-Microelectronics. This is a single poly CMOS process using SOI UNIBOND wafers with high resistivity Si ($\rho_{Si} > 3$ kΩcm) as starting substrate material, and 450 nm-thick BOX. This process features lines with six copper metal layers (M1 to M6) and one top aluminium layer to reduce conductor losses [9].

To compare their performance when a passivated wafer is used, a second set of identical PD SOI MOSFETS is obtained by transferring the processed layers onto a passivated HR Si wafer, with a 300 nm-thick polysilicon layer, with the method presented in [9] and patented by TraciT Technologies. It must be mentioned that an additional 525 nm-thick PECVD oxide, needed for the transfer process, increases the final BOX thickness of the passivated wafer to 975 nm.

The aim of our experimental setup is to assess the impact on the RF performance of the PD SOI MOSFETs when a noise signal is injected in the vicinity of the transistor, for passivated and unpassivated substrates. This can be achieved by comparing the spectral response (output signal) of the device with and without the injection of a known signal noise. On-wafer measurements are performed using a probe station, a WILTRON 68147A (10 MHz – 20 GHz) sweep generator for the generation of the 1 GHz RF input

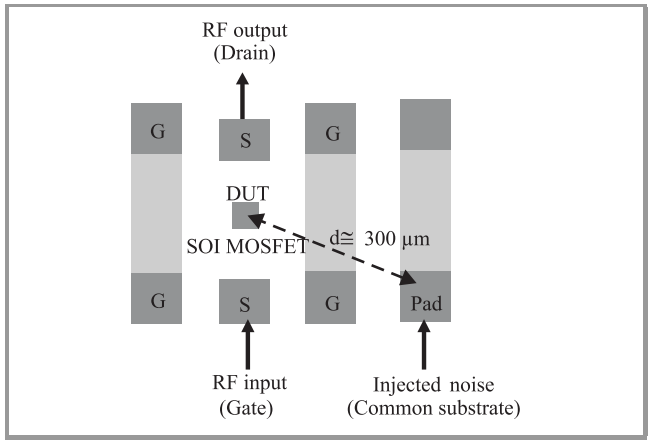

Fig. 6. SOI MOSFET crosstalk structure, S and G stand for signal and ground, respectively.

signal, and a HP33120 low frequency generator for the injection of a noise signal through a metallic pad near the device under test and lying on the same substrate. The RF output of the transistor is visualized using an Agilent E4440 wideband spectrum analyzer. A top view of the measured device, shown in Fig. 6, demonstrates that the distance between the device and the noise source is 300 μm.

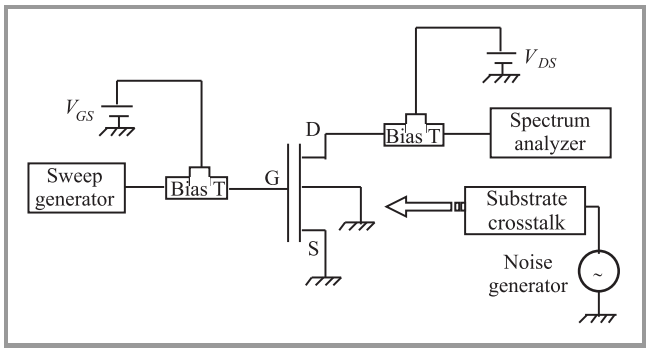

Fig. 7. Measurement setup of a transistor spectral response with injected noise signal.

A diagram of the measurement setup is presented in Fig. 7. It shows the biasing of the transistor, the RF input signal at the gate node, and the output spectral response at the drain node of the transistor.

5. Results and Discussion

Without injection of a noise signal, Fig. 8 shows the output signal spectrum, (a) without and (b) with a passivation layer, for a 0.24 μm SOI MOSFET biased at $V_{GS}=1$ V and $V_{DS}=1$ V for an input power of +10 dBm applied at the gate of the transistor. We can see that the generated intrinsic noise levels of the transistor are similar for both wafers. The amplitude of the output single tone for the transistor on the passivated substrate is slightly better (2 dB).

When a noise signal of a 10 V peak-to-peak at a frequency of 3 MHz (f_{noise}) is injected near the transistor we observe harmonics at 1 GHz $-f_{noise}$ and 1 GHz $+f_{noise}$ as shown in Fig. 9a. The amplitude of these sideband tones is -56 dBm.

The generation of these mixing products of the RF input and the noise signal at the RF output can be explained by the substrate coupling of the noise signal into the MOSFET. Although it was expected that at such low frequencies the BOX layer of the SOI provides a high enough level of isolation, the presence of a highly conductive surface at the BOX/HR-Si interface allows an efficient coupling of the large noise signal. As it is shown in Fig. 10, two possible coupling paths can be identified:

– one, that goes from the metallic pad of the noise injection to the RF input pad of the MOSFET and to the pad-to-gate interconnection,

– and a second one, that goes from the metallic pad of the noise injection to the back gate of the transistor.

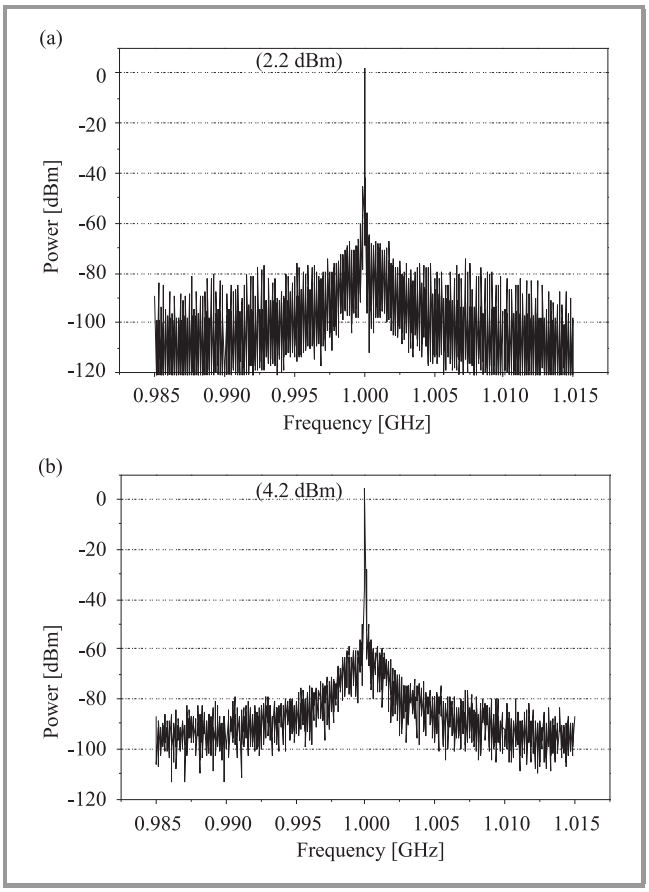

Fig. 8. Spectral response at 1 GHz without injected noise signal for a SOI PD MOSFET ($L_g = 0.24$ μm) on a (a) unpassivated and (b) passivated HR SOI substrate.

These paths are labelled as "front gate coupling" and "back gate modulation", respectively. As it is known the transconductance of the transistor from the back gate is lower than that from the front gate, we can assume that the "front gate coupling" is more important than the "back gate modulation", and thus that the sum of the noise and the RF input signals reach the gate of the MOSFET, and are mixed inside the transistor.

These assumptions are well confirmed when a passivation layer underneath the BOX is introduced. In fact, as it can be seen in Fig. 9b, the mixing products due to the presence of the noise signal fall below the noise floor of our measurement. A reduction of at least 15 dB is then measured for the sideband tones induced by the low frequency noise signal. The decrease of the noise level can be explained by the reduction of free carriers at the Si/SiO_2 interface. Indeed, the introduction of a high density of traps into the silicon surface will pin the surface potential and minimize the creation of a conductive inversion layer. Thus, the passivated SOI HR-Si substrate proved to have better crosstalk immunity.

Table 1 shows the detected power levels of the mixing products due to the noise signal for the two SOI MOSFETs (0.13 μm and 0.24 μm) when the frequency of the noise signal varies from 100 kHz to 3 MHz. These levels are

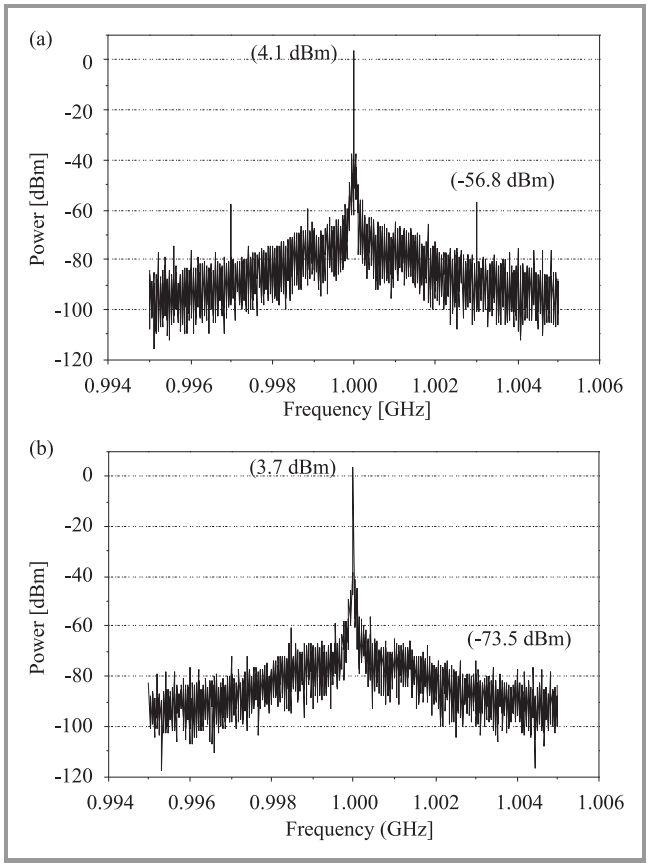

Fig. 9. Ouput spectrum around 1 GHz for a SOI PD MOSFET (0.24 μm), $f_{noise} = 3$ MHz: (a) unpassivated and (b) passivated HR SOI substrates.

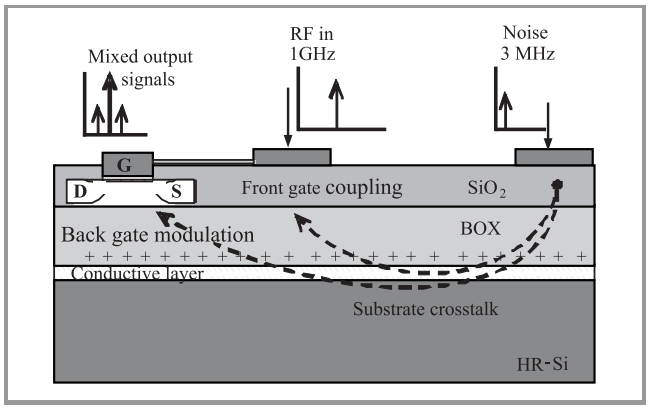

Fig. 10. Substrate crosstalk schematic between the SOI MOSFET and the metallic pad at which the noise signal is injected.

Table 1
Harmonics levels in dB at 1 GHz $\pm f_{noise}$ for two PD SOI MOSFETs

Freq. [MHz]	$L_g = 0.13$ μm		$L_g = 0.24$ μm	
	Unpassivated	Passivated	Unpassivated	Passivated
0.1	–63	–62	–56	–64.4
0.5	–53.7	–71	–56.7	–69.6
1	–52.8	–61.4	–52.8	–64.3
3	–58.1	–71.7	–56.8	–73.5

similar for both technologies, and in the case of passivated wafer they are below the noise floor of the measurement.

This improvement confirms that the use of the trap-rich passivation layer under the BOX act as a very effective stabilizing layer for SOI HR-Si wafers.

In order to model the coupling effect through the high resistivity SOI substrate a simple equivalent circuit that is presented in Fig.3b is proposed. The substrate is modeled as R-C networks where the elements $R_{Lateral}$ and $C_{Lateral}$ model the substrate crosstalk. As explained before, the use of the polysilicon layer can improve the effective resistivity of the substrate and hence reduce the coupling effect. This translates to the increase of the values of $R_{Lateral}$ as seen in Table 2.

Table 2
$R_{Lateral}$ with varying substrate effective resistivities

ρ_{eff} [Ωcm]	$R_{Lateral}$ [kΩ]
20	5.05
200	50.5
5,000	1,250

These values derive from Eq. (7) where the distance between the two devices is $d = 300$ μm and the width of the metallic pad is $W = 100$ μm.

To assess the attenuation of the noise levels with and without the passivation layer, this equivalent circuit is then connected to the small-signal equivalent circuit of the SOI MOSFET transistor and simulated with SPICE Eldo software.

In Fig. 11, dual-tone input signals are introduced at the gate node of the transistor. The output signal shows a mixing product of the low frequency noise and the RF 1 GHz signals. Mitigation of R-C networks modeling the transfer function of the substrate is calculated in the case of unpassivated SOI substrate, and then introduced in terms of noise signal amplitude.

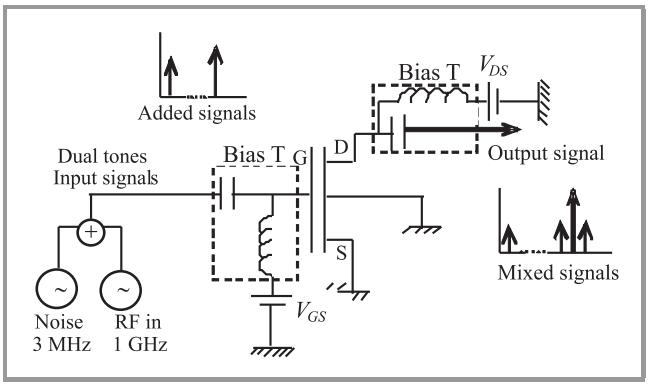

Fig. 11. Simulated equivalent circuit.

Using a noise signal level of 0.01 V peak-to-peak at 3 MHz we simulate sideband tones with an amplitude of –56 dBm which was previously observed experimentally in Fig. 9a.

When a passivated layer is introduced the effective resistivity of the wafer is improved. This is translated into the increase of $R_{Lateral}$ and hence an attenuation of the sideband tones levels due to the noise signal. This reduction is assumed to be more than 15 dB as presented in the measurement results.

6. Conclusions

The significance of the noise crosstalk through the Si substrate and the related effects on RF circuit are highlighted. Our measurements demonstrate the efficiency of a trap-rich layer, e.g., the polycrystalline silicon, to reach a very high recombination rate at the Si substrate-BOX interface and thus minimize the impact of crosstalk and surface conduction. A model of the substrate losses and propagated noise signal at the circuit level is proposed. Measurement and simulation results depict a reduction of the noise level by more than 15 dB when the substrate is passivated. In fact, a thin polycrystalline silicon surface layer acts as a very effective stabilizing layer for HR SOI substrate. Theses results are of importance for mixed-mode ICs in which coupling phenomena between digital and sensitive analog parts must be minimized. Thus high-resistivity SOI substrate with a polysilicon surface layer underneath the BOX is a viable substrate for low loss RF and mixed-mode applications.

Acknowledgments

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