Analysis and design of defected ground structure for EMC improvement in mixed-signal transceiver modules

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Abstract: In this research, the return path discontinuity (RPD), located under the power amplifier (PA) substrate, of X-band transceiver module (Base), mounted on a four-layer printed circuit board (PCB), is investigated to improve the signal integrity by reducing the difference in the reference potential. This study is performed by initially employing the wirebond method, through the assessment of both numbers and sizes of bondwires by advanced design system (ADS). Six bondwires of 25 μm are added, producing an improvement of 6.82 dB for the reflection coefficient and 1.19 dB for the isolation and insertion loss. For further improvement, spiral shape defected ground structure (DGS) is implemented in the inner ground layer (layer 2) without using bond wires. The DGS simulation results illustrate an improvement of 3 dB for S_{11} and 0.6 dB for S_{12}. To improve the electromagnetic compatibility (EMC), the authors propose combination and integration of both wirebond and DGS methods, called wirebond–DGS method, which results in an improvement of 11.86 dB for S_{11}, 1.34 dB for S_{12} and S_{21}, and 12.03 dB for S_{22}. Finally, the wirebond–DGS RF module was fabricated and the measurement results exhibit an improvement of 8.07 dB for S_{11} and 9.39 dB for S_{22} in comparison with the fabricated Base module. In addition, 0.53 dB improvement for both S_{12} and S_{21} is also achieved.

1 Introduction

Today by emigrating from simple PCBs to complex designs, the signal integrity (SI) and power integrity must be taken into consideration more accurately. The PCBs have to be made in small sizes and uniform, containing a combination of both analogue and digital signals, referred to as mixed-signal PCBs.

In order to design a reliable PCB, electromagnetic compatibility (EMC) is known to be the most common and effective factor in terms of analogue, digital and mechanical aspects [1]. The performance of any PCB is dependent on its EMC, stability, reliability and the sensitivity of the design [2–4].

A four-layer PCB design, as the least number of layers for a complex multilayer PCB [2, 5], is considered in the current research, whereby creating a return path close to its corresponding signal path is a design challenge. To overcome such limitations, many verified techniques have been introduced to improve the EMC, such as trace routing, shielding and grounding methods [6, 7]. A reliable return path is considered as a low impedance path far away from radiation sources. Such a path can provide an eligible path for the desired EMC performance [8].

Due to space limitations, when dealing with mixed-signal integrated PCBs, the metal wall shielding cannot be an appropriate approach for EMC design considerations [9]. In addition, providing analogue and digital grounds divides the return path and increases the path inductance. This, therefore, escalates the noise effect and is not recommended by most of the high-technology designs [10].

To choose an appropriate method for further EMC improvement, the return signal path can be modified by etching [11]. In doing so, the defected ground structure (DGS) is adopted in the present paper; this technique can minimise reflections and controls the signal return path. Such structure can be recognised as a suppression filter, which can improve SI, reliability and efficiency [12]. DGS directly affects the insertion loss, electrical and magnetic fields distribution generated by the pattern of the ground structure, and therefore, it is necessary to analyse the electromagnetic (EM) field behaviour and control its distribution. Such an effective method of controlling EM fields is to design the DGS structure within the return path, which can minimise the parasitic inductance, capacitance and resistance.

Another method of controlling the destructive EM fields via DGS is to directly modify the stop-band position and the effects of second and third harmonics of the band-pass filter [13]. Therefore, the objective of employing an explicitly designed DGS in our current research is to provide a PCB return path platform, with a wide bandwidth performance.

Typical DGS models such as spiral, U-shaped, H-shaped, array model and dumbbell shaped are compact microstrip filters used for wider bandwidth and can provide desired changes for common-mode current suppression [14]. The presence of common-mode noise problem for an integrated PCB causes electromagnetic interference (EMI) or radio frequency interference (RFI) [15]. Effects and distribution of such noise in a ground metallic plane are suppressed by etching return path within a DGS.

In the present work, a spiral-shaped DGS for an operating frequency band of 8–12 GHz is investigated. The selected frequency is centred at 9 GHz that can be applied in satellite communications, sensors in vehicle parking, phased array and frequency-modulated continuous-wave (FMCW) radars [16].

The current research focuses on designing a reliable return path for a mixed-signal multilayer PCB, with appropriate EMC considerations. This design has been optimised to be cost effective by and yet without shielding walls, absorbing components and ground splitting techniques. The method, however, has relied on creating a steady and uniform return path, with minimum fluctuations, and can further protect the structure from the internal noise.

In this paper two methods, namely wirebond and DGS, are combined and employed to improve the EMC of an radio frequency (RF) design. The wirebond method with either round
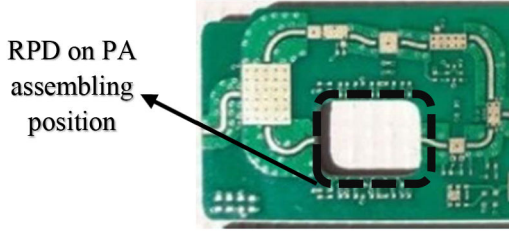
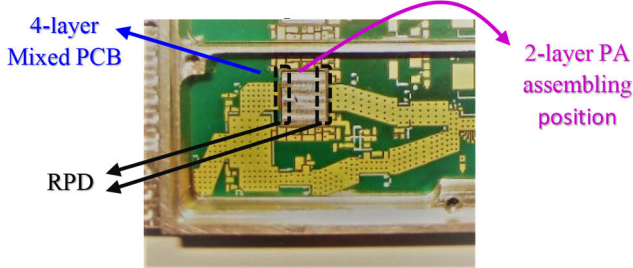**Fig. 1** *Photo of T/R module, where PA housing can cause RPD*

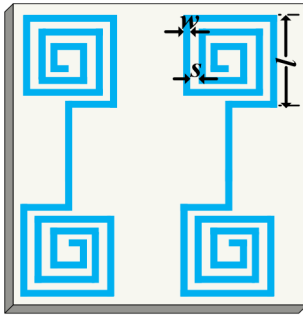**Fig. 2** *Assembled PA housing on the fabricated T/R module*

Fig. 3 *Geometrical parameters of a periodic DGS cell*

wire or ribbon bond can be used for connecting die packages on PCBs. The measurement results from researches carried out in [17, 18] have illustrated that employing both methods of wirebonding and DGS can improve the impedance matching, and reduce the insertion loss by further extending the range of operating frequencies.

This paper focuses on the analysis and design of combined wirebond–DGS PCB in a mixed-signal application to improve EMC. In Section 2, the design of DGS for return path discontinuity (RPD) will be discussed and analysed numerically. Next, in Section 3, simulations using finite element method (FEM) through ADS for the individual wirebond and DGS methods are carried out, and then the results of combining the two mentioned methods are also illustrated. This section also includes an impedance and EM interface analysis. Section 4 provides the measurement results, comparisons and discussions with and without wirebond–DGS fabricated circuit modules. Finally, Section 5 concludes this paper and the novelties with the proposed method.

2 Design of DGS for RPD

One of the most crucial and challenging components used in the majority of high-frequency mixed-signal transceivers is the power amplifier (PA). Most of PAs are assembled as a die-on-board, and hence the continuity of the board is affected by the PA output bondwires. A disruption to the return path is occurred by changing the reference plane of the signal, or presence of any discontinuities within the reference plane, which is recognised as RPD. The unwanted produced slot on the board ground plane (named as 'the reference plane') causes a deviation to the return path and hence any transfer of signal. Fig. 1 depicts a sample photo of a T/R module (transceiver), where the location of the PA has been annotated. As can be seen, such discontinuity has been created on the return path signal.

Fig. 2 depicts a photo of the developed PA housing and ground plane discontinuity on a fabricated multilayered mixed-PCB T/R module. The PA component is selected in the form of a die as two layers PCB. The mentioned die component is placed on metal housing located in the hole (as annotated in Fig. 1), which in turn creates a discontinuity in the transmitted signal return path.

Hence, we are faced with the connection of two individual PCBs; a two-layer PA PCB which is connected through bondwires to a multilayer PCB. Furthermore, the second layer of the PA PCB as the PA ground plane is connected to the multilayer PCB ground plane (the reference ground). In PCBs, such limitations yield unbalanced ground structures which result in EMC issues.

In this paper, a parallel-paired spiral-shaped DGS is designed to reject the non-linearity effects of active components such as PA and to improve the S-parameters, without any increase in the size or cost of the PCB. This process is based on a conventional microstrip method, which uses DGS as a design filter in return path [19].

DGS unit cells are typically designed periodically [20]. As shown in Fig. 3, the defects are designed to be in a spiral shape that are paired together; they are different in terms of material from the main copper plane. When the operating frequency increases, the inductance for the return path is correspondingly increased. Therefore, by increasing the length of the return path, an increased inductance is expected.

The most important parameters within a defected ground plane model are resistance and inductance of the return path. However, it should be noted that above the operating frequency of 1 GHz, the parasitic capacitance of the path model should also be taken into consideration [21]. In the DGS design, one challenging issue is variations of inductive and capacitive effects of the return path at higher frequencies.

According to Mohan *et al*. [22], the equivalent LC model can be related to a symmetrical planar spiral geometric structure (Fig. 3), where the inductance is calculated as

$$L_{\text{DGS\_eq}} = \frac{\mu_0}{2\pi} l_{\text{avg}} \left[\frac{1}{2} + \ln\left(\frac{l_{\text{avg}}}{2w}\right) \right] \tag{1}$$

where μ_0 is the free space permeability, l is the side length of the external ring in mm, w is the width of the strips in mm, s is the separation of two adjacent strips (in mm), N is the number of rings and l_{avg} is the average total length given by

$$l_{\text{avg}} = \frac{4lN - [2N(1 + N) - 3](w + s)}{N} \tag{2}$$

Furthermore, according to the authors in [23, 24], the distributed capacitance between any pair of adjacent rings is calculated as

$$C_{\text{DGS-eq}} = C_0 \frac{l}{4(w + s)} \frac{N^2}{N^2 + 1} \sum_{n=1}^{N-1} \left[l - \left(n + \frac{1}{2}\right)(w + s) \right] \tag{3}$$

where C_0 is the per unit-length capacitance.

To find an optimised number of rings (N) and to design each DGS cell through the calculation of $N_{\text{max}} = \text{Integer}[(l - (w + s))/2(w + s)] > 0$, the point of resonance can be obtained as

$$\frac{\partial L_{\text{DGS\_eq}}}{\partial N} = \frac{\mu_0}{2\pi} \frac{[6N^2 - 3](w + s)}{N^2} \left[\frac{3}{2} + \ln\left(\frac{l_{\text{avg}}}{2w}\right) \right] \tag{4}$$

Similarly, to obtain the critical point for the capacitance

$$\frac{\partial C_{\text{DGS\_eq}}}{\partial N} = C_0 \frac{l}{4(w + s)} \frac{2N}{(N^2 + 1)^2} \sum_{n=1}^{N-1} \left[l - \left(n + \frac{1}{2}\right)(w + s) \right] \tag{5}$$

Furthermore, according to the instruction provided by ADS to design a spiral square filter [25], to find an appropriate number of rings N, the design constraint (6) between l, w and s should also be taken into consideration:

Table 1 Optimisation of number of rings (N) in the spiral DGS

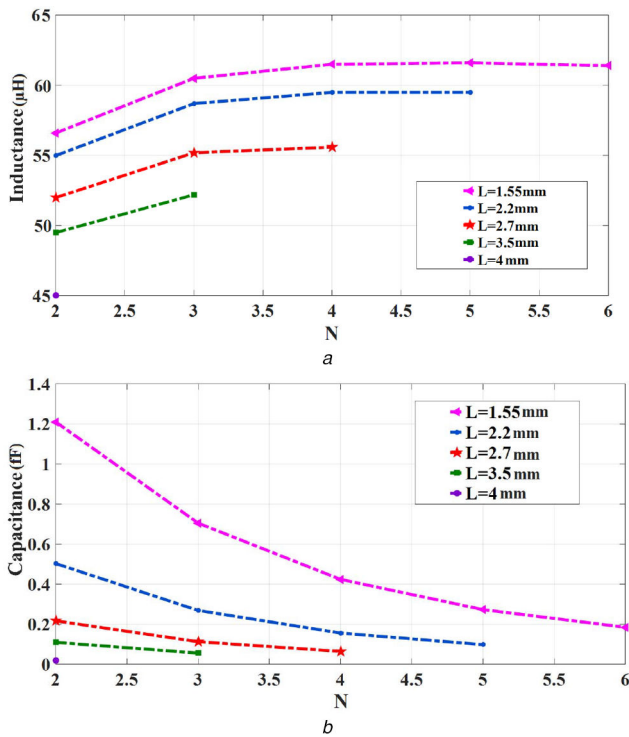|	N	l	$\dfrac{\partial L_{\text{DGS\_eq}}}{\partial N}$	$\dfrac{\partial C_{\text{DGS\_eq}}}{\partial N}$
$w = s = 0.15$	2	1.55	4.50×10^{-5}	1.87×10^{-17}
		2.2	4.95×10^{-5}	1.10×10^{-16}
		2.7	5.20×10^{-5}	2.17×10^{-16}
		3.5	5.50×10^{-5}	5.03×10^{-16}
		4	5.66×10^{-5}	1.21×10^{-15}
	3	2.2	5.22×10^{-5}	5.59×10^{-17}
		2.7	5.52×10^{-5}	1.13×10^{-16}
		3.5	5.87×10^{-5}	2.69×10^{-16}
		4	6.05×10^{-5}	7.05×10^{-16}
	4	2.7	5.56×10^{-5}	6.44×10^{-17}
		3.5	5.95×10^{-5}	1.56×10^{-16}
		4	6.15×10^{-5}	4.24×10^{-16}
	5	3.5	5.95×10^{-5}	9.83×10^{-17}
		4	6.16×10^{-5}	2.73×10^{-16}
	6	4	6.14×10^{-5}	1.85×10^{-16}

Fig. 4 Numerical data analysis for different values spiral DGS number of rings (N)
(a) Inductance,
(b) Capacitance

$$L > (2N + 1)(w + s) \qquad (6)$$

Table 1 illustrates the numerical data obtained from the designed DGS for different values of N and l, where the acceptable values are achieved from (6).

Table 1 shows that the derived values of L and C are at their minimum when $N = 2$, $l = 1.55$ mm and $w = s = 0.15$ mm. However, there is an apparent limitation on N due to the lack of space between vias on the return path layer and manufacturing restrictions. Table 1 tabulates the variation of inductance and capacitance values versus N. MATLAB has been used to extract the optimised and minimum values for each spiral DGS as shown in Fig. 4. As illustrated in Fig. 4, the minimum derived values for L and C occur when $N = 2$, which makes the design more reliable.
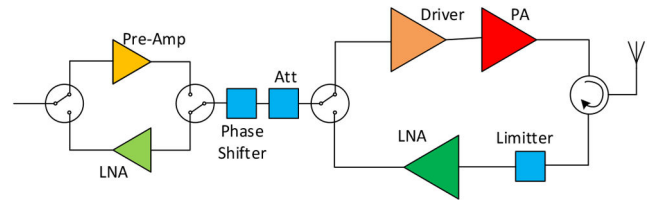

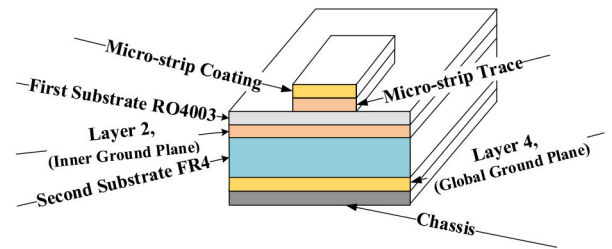**Fig. 5** *System block diagram illustrating one out of four channels of the T/R module*

Fig. 6 *PA output microstrip on a four-layer PCB*

3 Finite element analysis

The operating frequency for the T/R module is within the X-band (8–12 GHz).The block diagram for one of the channels of a typical T/R module is shown in Fig. 5.

As mentioned earlier, the focus of this research is on the EMC of the last PA stage shown in Fig. 5, with an output power of 40 dBm at saturation point. Considering the insertion loss of circulator as 0.5 dB, the output shall be 40.5 dBm, fulfilling the requirement of output power of ≥40 dBm. The PA component, which comprises a two-layer Rogers 4003 PCB ($\varepsilon_{\text{r}} = 3.55$, $\tan \delta = 0.0022$) is assembled on a rectangular-shaped groove and is directly connected to the chassis.

The PA output bondwires are connected to the four-layer PCB of the T/R module, where the output signal faces a discontinuity in its return path. Fig. 6 illustrates the output microstrip on a four-layer PCB using Rogers 4003 for the top layer, and FR4 ($\varepsilon_{\text{r}} = 4.6$, $\tan \delta = 0.01$) on the bottom layer.

A sample PCB for the PA structure of the T/R module was designed and then analysed using ADS (FEM) which is illustrated in Fig. 7. As can be observed from Fig. 7a, the total length and width of the structure are 40.2 and 8 mm, respectively. The PA output path as a form of Coplanar Waveguide (CPW) has been connected to the multi-layer PCB by bondwires, as shown by the blue mark in Fig. 7b. As annotated, lumped ports P_1 on the top
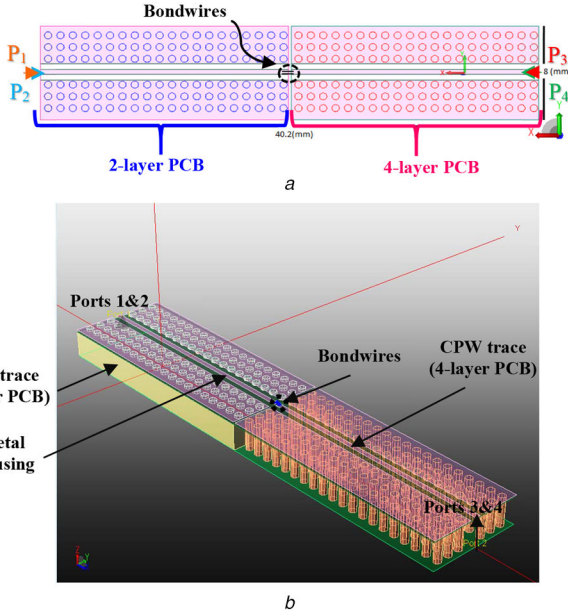
Fig. 7 *Sample PCB for the PA structure of the T/R module*
(a) 2D view of PA return path,
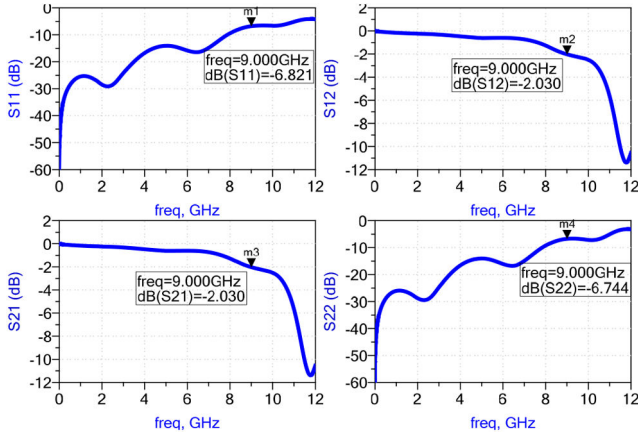*(b)* 3D view of PA return path

Fig. 8 *S-parameter results for the initial PA sample design*

Table 2 Equivalent RLC filter characterisation for the initial PA module (Base)

	N	C, pF	L, nH
RLC filter	1	0.271	0.89
	2	0.6483	1.98
	3	0.417	0.235
	4	0.0161	0.595

layer and P_2 on the second ground layer are employed at PA assembling position; in the same way P_3 and P_4 are employed for multi-layer (four-layer) PCB.

As the first step of simulations, the PA output has been considered individually. Fig. 8 illustrates the SI results for *S*-parameters. By considering the operation of PA at the central frequency 9 GHz, the response of the system is found to be $S_{11} = -6.82$ dB, $S_{12} = S_{21} = -2.03$ dB and $S_{22} = -6.74$ dB.

As can be observed in Fig. 8, there is a significant return loss for frequencies above 7 GHz.

An RLC equivalent filter can be modelled using a Π model (low-pass filter), consisting of an L series with C parallel circuit; such a configuration is repeated four times based on the data presented in Table 2.
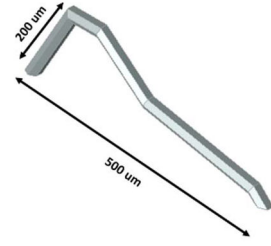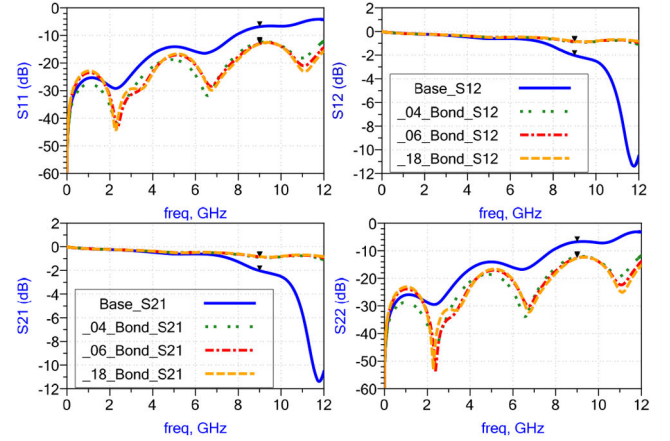

Fig. 9 *Bondwire model for shape 1*

Fig. 10 *S-parameter results for employing 4, 6 and 18 bondwires*

3.1 Wirebond technique

At this stage, the wirebonding technique has been employed with initially adding 4 bondwires, then 6 and later 18 were employed between CPW ground planes of PA housing and the mixed-signal PCB.

The RF bondwires can affect the impedance matching of the path by having an influence on equivalent RLC filter values (Table 2). By inserting bondwires on the RPD and connecting the CPW grounds together a wider operational bandwidth will be expected.

The bondwire dimensions and shape employed in our design are depicted in Fig. 9.

By employing bondwires of Fig. 9, the distance of signal return path is comparatively minimised. To achieve the optimised characteristics, i.e. different numbers and radii of bondwires, various alternatives were considered and simulated using ADS. Fig. 10 illustrates the *S*-parameter results using 4, 6 and 18 bondwires. As illustrated, at 9 GHz a minimum improvement of 5.68 dB for S_{11} and 1.14 dB for S_{12} are obtained compared to the non-bondwires case (Base model).

Considering Fig. 10, one may conclude that there is not much difference in the *S*-parameter responses when 6 or 18 bondwires are employed. Therefore, the six-bondwire scheme is selected as a default for this system. When six bondwires are employed at 9 GHz, an improvement of 6.15 dB in S_{11} and 1.18 dB in S_{12} were observed resulting in $S_{11} = -12.97$ dB and $S_{12} = -0.84$ dB.

To obtain further EMC improvement, for six bondwires, different radii (17, 25, 50 and 75 μm) were analysed and results of which are illustrated in Fig. 11.

According to Fig. 11, the *S*-parameters are further improved for radii of 75 μm which create wider path, but according to manufacturer limitations, 25 μm is selected as the radii, producing $S_{11} = -12.97$ dB, with 1.19 dB improvement for S_{21}.

3.2 DGS implementation

Preliminary simulations revealed that the spiral structure shows a better fit to the desired response. As it was mentioned in Section 2, for this structure, $N = 2$, $l = 1.55$ mm and $w = s = 0.15$ mm were selected. Fig. 12*a* illustrates a DGS cluster which consists of two cells; the width of each is 1.55 mm with a height of 1.32 mm. Each
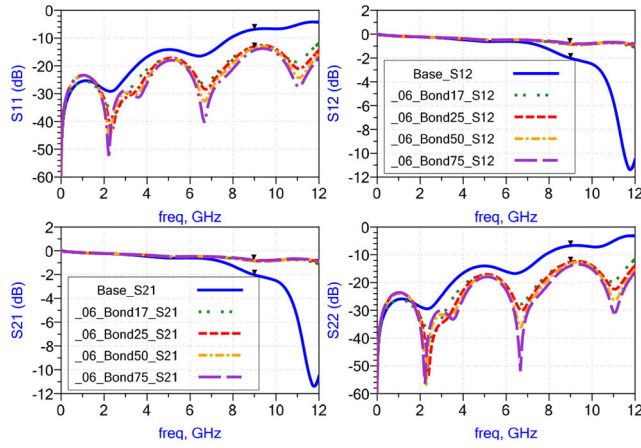
Fig. 11 *S-parameter results of the PA output microstrip on the four-layer PCB for: 6 bondwires with different radii size: 17, 25, 50 and 75 μm*
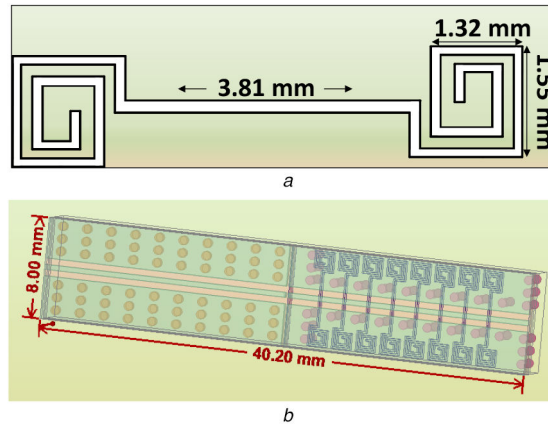

Fig. 12 *Employed spiral shape DGS*
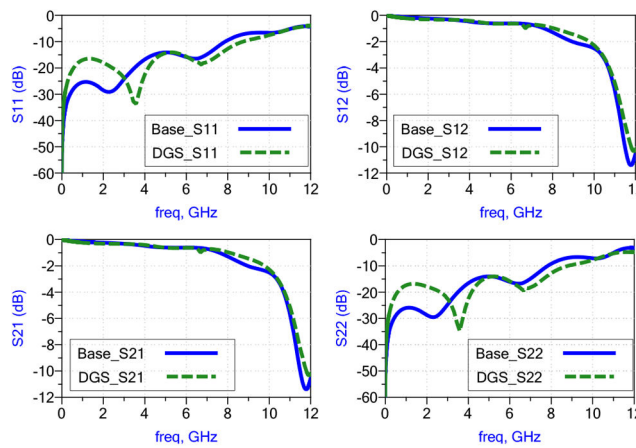*(a)* DGS cluster,
(b) DGS 3D structure for PA return path

Fig. 13 *Comparison of S-parameters responses with and without employing DGS*

cell has two turns and is connected to the neighbouring cell via a track length of 3.81 mm. Such a structure repeats eight times on the bottom layer of PA return path and has a distance of 0.25 mm from the neighbouring cell of a cluster. Fig. 12*b* depicts a 3D structure of eight clusters in the design. Fig. 13 presents the result of the designed DGS, which shows an improvement of about 3 dB for the input/output reflection coefficients, and subsequently about 0.6 dB for the reverse/forward gains.

According to the results presented in Table 3, the presence of DGS reduces the module's radiated power to about 0.04×10^{-4} (Watts) for input power 0.002 W in 9 GHz.

3.3 Implementation of the combined wirebond and DGS techniques

By analysing the results for implementation of the wirebond (Fig. 11) and DGS (Fig. 13) techniques, it can be stated that neither of the two techniques can independently solve the SI problems. Therefore, both techniques are combined, the response of which is illustrated in Fig. 14. The results for the centre frequency of X-band region, i.e. 9 GHz, are $S_{11} = -18.68$ dB, $S_{22} = -18.77$ dB and $S_{12} = S_{21} = -0.69$ dB. Moreover, a considerable improvement is obtained for S_{11} and S_{22} as 11.86 and 12.03 dB, respectively. In addition, an improvement of 1.34 dB for both S_{12} and S_{21} is also achieved.

Table 3 Comparison of the radiation power before and after employing DGS frequency = 8, 9, 10, 12 GHz, input power = 0.002 W

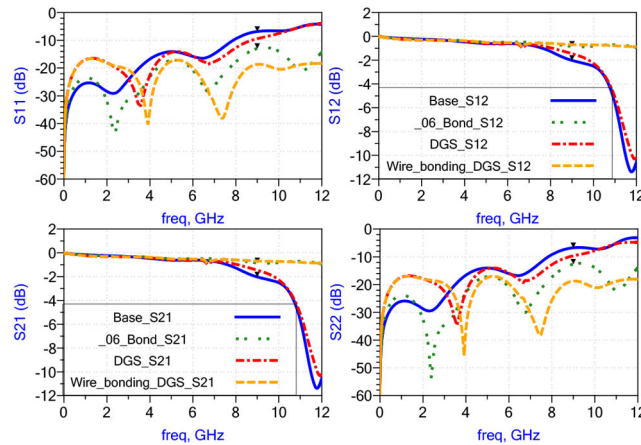|	Module	Radiated power, W
8 GHz	before employing DGS	6.52×10^{-5}
	after employing DGS	6.18×10^{-5}
9 GHz	before employing DGS	1.18×10^{-4}
	after employing DGS	1.14×10^{-4}
10 GHz	before employing DGS	2.04×10^{-4}
	after employing DGS	2.36×10^{-4}
12 GHz	before employing DGS	7.60×10^{-4}
	after employing DGS	9.42×10^{-4}

Fig. 14 *Comparison of the responses for: Base, six bondwires size 25 μm, DGS and wirebond–DGS modules*
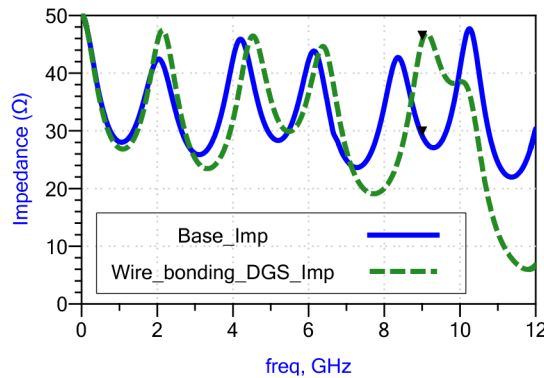

Fig. 15 *Impedance analysis with and without wirebond–DGS*

Table 4 Comparison of *E*-field and *H*-field before and after employing wirebond–DGS

Module	PCB position, mm	*E*-field, dB, V/m	PCB position, mm	*H*-field, dB, A/m
before employing wirebinding–DGS	*X*: 13.98, *Y*: 0.21, *Z*: 1.66	18,830.8	*X*: 9.48, *Y*: −0.1, *Z*: 1.50	103.47
after employing wirebinding–DGS	*X*: 13.98, *Y*: 0.21, *Z*: 1.66	21,491.4	*X*: 14.38, *Y*: 0.00, *Z*: 1.50	69.06

Fig. 15 illustrates the impedance response of the inner ground layer, before and after employing the combined wirebond–DGS technique. As it can be seen, this method results in a more stable impedance and the impedance decreases from 45.7 to 29.08 Ω in 9 GHz, when there is no wirebond–DGS.

As illustrated in Table 4, the reduction of *H*-field has been minimised by adding the DGS structure and minimising the EM interferences.

For further validation of the wirebond–DGS reliability, the critical points at higher temperatures and maximum EM radiation are recognised within the RF layer 2, and are illustrated in Fig. 16. From this simulation, the locations for the DGS cells can be predicted. Figs. 16*a* and *b* present the *E*-field response and Figs. 16*c* and *d* illustrate the *H*-field response before and after the defect is applied, respectively.

In addition, the increase in the *E*-field after the addition of DGS may indicate that there is more return path current dissipation in this layer, which in turn prevents the current transfer within layer 4 and provides a small current loop inside the entire module; and this is depicted in Figs. 16*e* and *f*.

In order to accurately design and fabricate a microstrip filter, the RLC equivalent circuit is typically modelled to design a DGS. To develop a DGS-RLC filter, elliptic Cauer filter in the form of RLC ladder model has been synthesised, for S_{11} and S_{22}. The accuracy of this model has been increased by optimising and tuning primary parameters using ADS. A simple DGS-RLC equivalent filter can be modelled using a Π model, consisting of a resistor which is connected in series with an LC circuit; and such a configuration is repeated six times based on the data presented in Table 5. The comparison of S_{11} simulation response and its
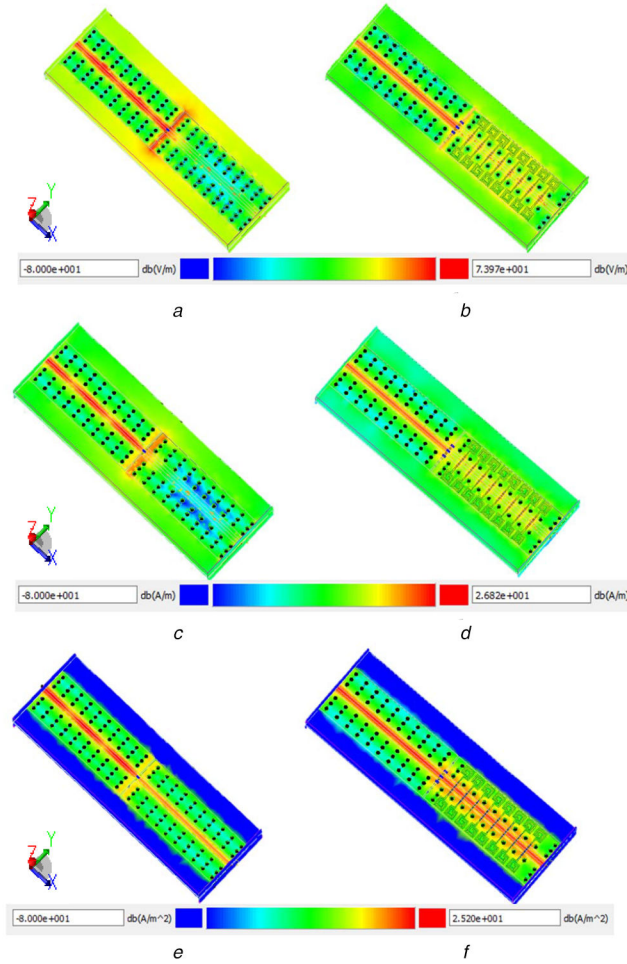
Fig. 16 *RF layer 2 return path simulation response*

(a) E-field before employing wirebond–DGS,

(b) E-field after employing wirebond–DGS,

(c) H-field before employing wirebond–DGS,

(d) H-field after employing wirebond–DGS,

(e) Current density before employing wirebond–DGS,

(f) Current density after employing wirebond–DGS

Table 5 Equivalent RLC filter characterisation

	N	R, Ω	L, nH	C, pF
RLC filter	1	33.75	4.903	1700
	2	0.2	4.703	0.01
	3	8.15	2.911	0.210
	4	6.7	0.001	0.422
	5	1.1	2.6	0.8
	6	0.25	156.8	5 70 000
	7	0.25	—	—

equivalent RLC circuit model for the designed DGS is shown in Fig. 17, where it can be seen that simulation response is following similar trend as the equivalent circuit model response.

According to the results presented in Table 6, the presence of the wirebond–DGS reduces the module's radiated power to about 1.08×10^{-4} W for input power 0.002 W, at centred frequency of 9 GHz, which improves the EMC effectively.

4 Experimental result

Following the analytical and simulation responses, it was found that six bondwires of 25 μm each, along with spiral shape DGS, $N = 2$, provide the most improved response for EMC.

In order to verify the results and novelty of this work, a module with two separate PCBs, as illustrated in Fig. 7*b*, was designed and fabricated.

Fig. 18*a* illustrates the fabricated module, where the left segment is a two-layer PCB, 8 mils on Rogers 4003, and the right segment is a mixed four-layer PCB with the top layer on 8 mils Rogers 4003, and the bottom layer on FR4 standard TG 140°C and 47.24 mils. The top copper thickness for both segments is 17 μm. The electroless nickel immersion gold technique was used for coating the top layer of PCBs, which was done to enable the assembling of the bondwires. The magnified photo of the fabricated bondwires on the top layer between two PCBs is annotated in this photo. The second layer of a mixed four-layer PCB which consists of the spiral DGS pattern is shown in Fig. 18*b*.

Fig. 19 illustrates the measurement and simulation results with and without wirebond–DGS fabricated modules. It is clear that the measurement response from the fabricated module verifies the simulation results. For the centre frequency of 9 GHz the fabricated wirebond–DGS module shows considerable improvements of 8.07
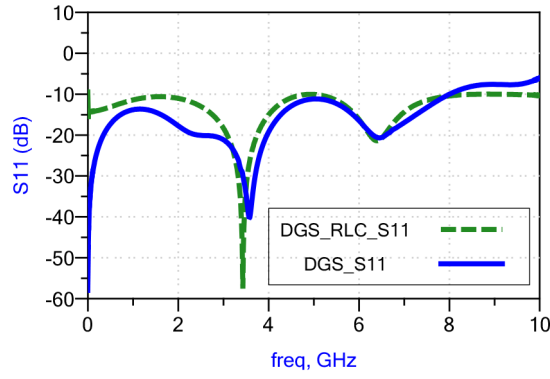
Fig. 17. *Calibrated RLC circuit model for S_{11} result*

Table 6 Comparison of radiation power before and after employing wirebond–DGS frequency = 8, 9, 10, 12 GHz, input power = 0.002 W

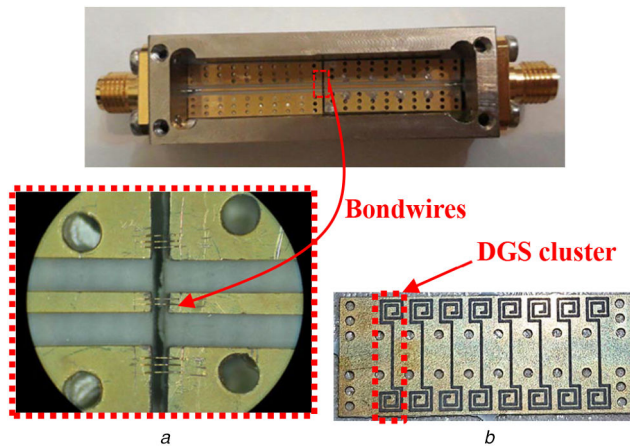|	Module	Radiated power, W
8 GHz	before employing wirebond–DGS	6.52×10^{-5}
	after employing wirebond–DGS	9.89×10^{-6}
9 GHz	before employing wirebond–DGS	1.18×10^{-4}
	after employing wirebond–DGS	9.90×10^{-6}
10 GHz	before employing wirebond–DGS	2.04×10^{-4}
	after employing wirebinding–DGS	1.07×10^{-5}
12 GHz	before employing wirebond–DGS	7.60×10^{-4}
	after employing wirebond–DGS	1.87×10^{-5}

Fig. 18 *Fabricated wire-bonding-DGS module*
(a) Fabricated wirebonding–DGS module,
(b) Second layer of module

dB for S_{11} and 9.39 dB for S_{22} in comparison to a fabricated module without wirebond–DGS (Base). In addition, an improvement of 0.53 dB for both S_{12} and S_{21} is also achieved.

As shown in Fig. 19, the differences between simulation and measurement results at the centre frequency of 9 GHz are 1.48 dB for S_{11}, 0.4 dB for S_{22} and 0.38 dB for both S_{12} and S_{21}.

Table 7 compares of the results obtained in this work for S_{11}, S_{12}, S_{21}, and S_{22} with those of similar researches.

Analysis of SI for the designed wirebond–DGS indicates merging the wirebonding and the DGS techniques, improves all S-parameters results and consequently the EMC reliability of the module.

5 Conclusion

In this research, a combination of wirebond and DGS techniques in a mixed-signal transceiver module has been analysed in order to improve SI and EMC. The design of both wirebond and DGS has been optimised for different dimensions and shapes in the current research, and as a result, an equivalent RLC filter has been calibrated and employed to model the DGS.

Simulation results show that adding six bondwires of 25 μm width improved the reflection coefficient, the isolation and the insertion loss by 90.17 and 58.42%. Furthermore, the simulation result for the compact eight-paired cluster defected structure independently improved the reflection coefficient, the isolation and the insertion loss by about 38.06 and 28.37%. With combination of both methods, further improvement on simulation response was observed with 173.83% for S_{11}, 66.05% for both S_{12} and S_{21} and 178.28% for S_{22}. A wirebonding–DGS module was then fabricated with an improvement of 88.77% for S_{11} and 104.80% for S_{22} in comparison with a fabricated Base module. In addition, 33.12% improvement for both S_{12} and S_{21} was achieved. The obtained results illustrated a significant improvement in comparison to previous works presented in the literature.
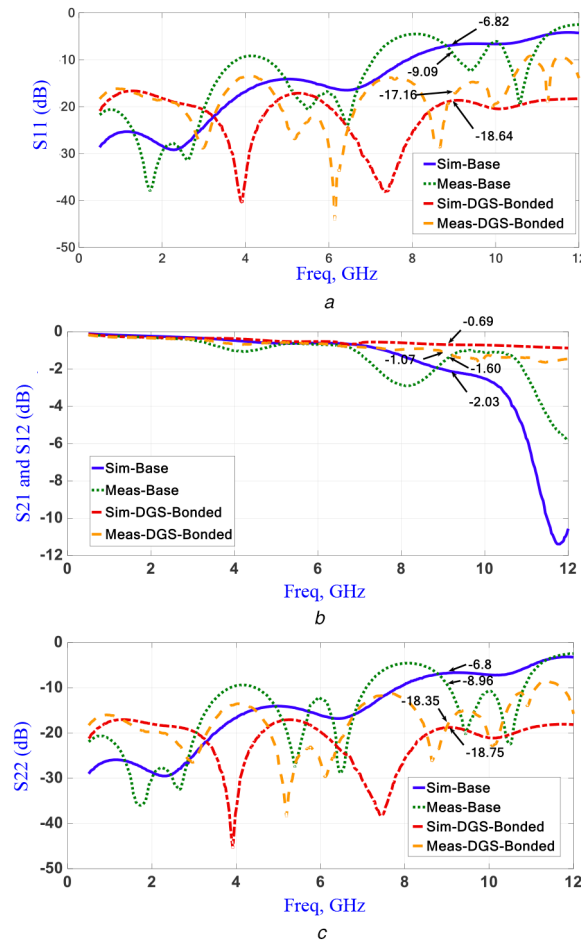
Fig. 19 *Comparison of fabrication and simulation responses for different cases: wirebond–DGS and without wirebond–DGS*

(a) S_{11} (dB),

(b) S_{21} and S_{12} (dB),

(c) S_{22} (dB)

Table 7 Comparison results

	Operation frequency, GHz	Output return loss, dB	Input return loss, dB	Insertion loss, dB	Isolation, dB
[26]	1–10	—	—	Avg: 10, Max: 25 at 3.5 GHz	—
[27]	0–20	—	—	Avg CM: 10	Avg DM: 15, Avg CM: 12
[28]	3–9	—	Avg: 10, Min: 35 at 6.3 GHz	Avg: 10, Min: 1.15 at 5.75 GHz	—
[29]	5.4–11.4	—	—	Avg DM: ∼0 Avg CM: 15	—
[30]	0–10	Avg: 14	—	Avg: 3, Min: 0.65	25–35
[31]	0–12	—	Avg DM: 15, Avg CM: 0	Avg DM: ∼0 Avg CM: 15	—
measurement of current research (at 9 GHz)	0–12	17.16 Avg: **20**, Min: **38** at **5** GHz	18.35 Avg: **20**, Min: **44** at **6** GHz	**1.07**	**1.07**

DM: differential mode; CM: common mode.

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7 References

[1] Bruce Archambeault, F.I.: 'Review of printed-circuit-board level EMI/EMC issues and tools', *IEEE Trans. Electromagn. Compat.*, 2010, **52**, (2), pp. 455–461

[2] Khorrami, M.A.: 'Effective power delivery filtering of mixed-signal systems with negligible radiated emission', *Electromagn. Compat. Mag.*, 2016, **5**, (4), pp. 128–132

[3] Armstrong, M.K.: 'PCB design techniques for lowest-cost EMC compliance. 1', *Electron. Commun. Eng. J.*, 1999, **3311**, (4), pp. 185–194

[4] Heidari, S., Mehri, M., Masoumi, N.: 'System level estimation of a PCB electromagnetic radiated emission'. 20th Workshop on Signal and Power Integrity (SPI), Turin, Italy, May 2016

[5] Karl-Heinz Gonschorek, R.V.: 'Electromagnetic compatibility for device design and system integration'. Springer Science & Business Media, September 18, 2009

[6] Bogar, J., Vanderheyden, E.: 'Interconnection and circuit packaging for electromagnetic compatibility', *IEEE Trans. Compon. Hybrids Manuf. Technol.*, 1982, **5**, (4), pp. 470–478

[7] Masoumi, N., Elmasry, M.I., Safavi-Naeini, S.: 'Fast and efficient parametric modeling of contact-to-substrate coupling', *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, 2000, **19**, pp. 1282–1292

[8] Chen, I.-F., Peng, C.-M., Hsue, C.-W.: 'Circuit-concept approach to radiated emissions of printed circuit boards', *IEE Proc. Sci. Meas. Technol.*, 2004, **151**, (3), pp. 205–210

[9] Lin, L., Zhou, L., Zhu, Y., et al.: 'Improvement in cavity and model designs of LDMOS power amplifier for suppressing metallic shielding cover effects', *IEEE Trans. Electromagn. Compat.*, 2016, **58**, (5), pp. 1617–1628

[10] Kollia, V., Cangellaris, A.C.: 'A domain decomposition approach for efficient electromagnetic analysis of the power distribution network of packaged electronic systems', *IEEE Trans. Electromagn. Compat.*, 2010, **52**, (2), pp. 320–331

[11] Sadr, A., Masoumi, N.: 'Lower cutoff frequency improvement of planar EBG-patterned PDN using edge termination', *Electron. Lett.*, 2015, **51**, (16), pp. 1270–1272

[12] Apriyana, A.A.A., Zhang, Y.P., Chang, J.S., et al.: 'Single-pole multiple-throw switches with defected ground structure low-pass filter', *IET Microw. Antennas Propag.*, 2014, **8**, (14), pp. 1241–1249

[13] Woo, D.-J.: 'Novel U-slot and V-slot DGSs for bandstop filter with improved Q factor', *IEEE Trans. Microw. Theory Tech.*, 2006, **54**, (6), pp. 2840–2847

[14] Wu, J.: 'A novel wideband common-mode suppression filter for gigahertz differential signals using coupled patterned ground structure', *IEEE Trans. Microw. Theory Tech.*, 2009, **57**, (4), pp. 848–855

[15] Wu, T.-L.: 'Overview of power integrity solutions on package and PCB: decoupling and EBG isolation', *IEEE Trans. Electromagn. Compat.*, 2010, **52**, (2), pp. 346–356

[16] Ahn, D.: 'A novel dual microwave Doppler radar based vehicle detection sensor for parking lot occupancy detection', *IEICE Electron. Express*, 2017, **14**, (1), p. 20161087

[17] Lin, Y.-C., Lee, W.-H., Homg, T.-S., et al.: 'Full chip-package-board Co-design of broadband QFN bonding transition using backside via and defected ground structure', *IEEE Trans. Compon. Packag. Manuf. Technol.*, 2014, **4**, (9), pp. 1470–1479

[18] Chan, C.-H., Chou, C.-C., Chuang, H.-R.: 'Integrated packaging design of low-cost bondwire interconnection for 60-GHz CMOS vital-signs radar sensor chip with millimeter-wave planar antenna', *IEEE Trans. Compon. Packag. Manuf. Technol.*, 2018, **8**, (2), pp. 177–185

[19] Lim, J.-S.: 'Design of low-pass filters using defected ground structure', *IEEE Trans. Microw. Theory Tech.*, 2005, **53**, (8), pp. 2539–2545

[20] Liu, H.-W.: 'An improved 1D periodic defected ground structure for microstrip line', *IEEE Microw. Wirel. Compon. Lett.*, 2004, **14**, (4), pp. 180–182

[21] Kiang, J.F.: '*Novel technologies for microwave and millimeter wave applications*' (Kluwer Academic, Boston, MA, 2004), pp. 205–206

[22] Mohan, S.S., Hershenson, M., Boyd, S.P., et al.: 'Simple accurate expressions for planar spiral inductances', *IEEE J. Solid-State Circuits*, 1999, **34**, (10), pp. 1419–1424

[23] Bilotti, F.: 'Design of spiral and multiple split-ring resonators for the realization of miniaturized metamaterial samples', *IEEE Trans. Antennas Propag.*, 2007, **55**, (8), pp. 2258–2267

[24] Bilotti, F.: 'Equivalent-circuit models for the design of metamaterials based on artificial magnetic inclusions', *IEEE Trans. Microw. Theory Tech.*, 2007, **55**, (12), pp. 2865–2873

[25] Keysight Technologies.: 'Advanced design system documentation', accessed on 9 July 2018

[26] Safwat, A.M.E., Tretyakov, S., Raisanen, A.V.: 'Defected ground and patch-loaded planar transmission lines', *IET Microw. Antennas Propag.*, 2009, **3**, (2), pp. 195–204

[27] Sawyer, E.: 'Using common-mode filtering structures with microstrip differential lines in a multilayer printed circuit board environment'. 44th European Microwave Conf., Rome, Italy, 2014

[28] Avinash, K.G.: 'Design of microstrip wideband bandpass filter using U shaped defected ground structure'. Int. Conf. on Microwave, Optical and Communication Engineering (ICMOCE), Bhubaneswar, India, 2015

[29] Gao, X.-K.: 'A compact common-mode noise suppression filter for high speed differential signals using defected ground structure'. 2015 Asia-Pacific Symp. on Electromagnetic Compatibility (APEMC), Taiwan, 2015

[30] Packiaraj, D.: 'Miniaturized defected ground high isolation crossovers', *IEEE Microw. Wirel. Compon. Lett.*, 2013, **23**, (7), pp. 347–349

[31] Zeng, Z.: 'A wideband common-mode suppression filter with compact-defected ground structure pattern', *IEEE Trans. Electromagn. Compat.*, 2015, **57**, (5), pp. 1277–1280