International Institute for
Applied Systems Analysis
IIASA www.iiasa.ac.at

Managing the Development and Transfer of Process Technologies in the Semiconductor Manufacturing Industry

Appleyard, M.M., Hatch, N.W. and Mowery, D.C.

IIASA Working Paper

WP-96-043

April 1996

Working Paper

Managing the Development and Transfer of Process Technologies in the Semiconductor Manufacturing Industry

Melissa M. Appleyard, Nile W. Hatch and David C. Mowery

WP-96-43
April 1996

IIASA International Institute for Applied Systems Analysis □ A-2361 Laxenburg □ Austria
Telephone: +43 2236 807 □ Fax: +43 2236 71313 □ E-Mail: info@iiasa.ac.at

Managing the Development and Transfer of Process Technologies in the Semiconductor Manufacturing Industry

Melissa M. Appleyard, Nile W. Hatch and David C. Mowery

WP-96-43
April 1996

International Institute for Applied Systems Analysis □ A-2361 Laxenburg □ Austria
Telephone: +43 2236 807 □ Fax: +43 2236 71313 □ E-Mail: info@iiasa.ac.at

Preface

The research project on *Systems Analysis of Technological and Economic Dynamics* at IIASA is concerned with modeling technological and organisational change; the broader economic developments that are associated with technological change, both as cause and effect; the processes by which economic agents – first of all, business firms – acquire and develop the capabilities to generate, imitate and adopt technological and organisational innovations; and the aggregate dynamics – at the levels of single industries and whole economies – engendered by the interactions among agents which are heterogeneous in their innovative abilities, behavioural rules and expectations. The central purpose is to develop stronger theory and better modeling techniques. However, the basic philosophy is that such theoretical and modeling work is most fruitful when attention is paid to the known empirical details of the phenomena the work aims to address: therefore, a considerable effort is put into a better understanding of the 'stylized facts' concerning corporate organisation routines and strategy; industrial evolution and the 'demography' of firms; patterns of macroeconomic growth and trade.

From a modeling perspective, over the last decade considerable progress has been made on various techniques of dynamic modeling. Some of this work has employed ordinary differential and difference equations, and some of it stochastic equations. A number of efforts have taken advantage of the growing power of simulation techniques. Others have employed more traditional mathematics. As a result of this theoretical work, the toolkit for modeling technological and economic dynamics is significantly richer than it was a decade ago.

During the same period, there have been major advances in the empirical understanding. There are now many more detailed technological histories available. Much more is known about the similarities and differences of technical advance in different fields and industries and there is some understanding of the key variables that lie behind those differences. A number of studies have provided rich information about how industry structure co-evolves with technology. In addition to empirical work at the technology or sector level, the last decade has also seen a great deal of empirical research on productivity growth and measured technical advance at the level of whole economies. A considerable body of empirical research now exists on the facts that seem associated with different rates of productivity growth across the range of nations, with the dynamics of convergence and divergence in the levels and rates of growth of income, with the diverse national institutional arrangements in which technological change is embedded.

As a result of this recent empirical work, the questions that successful theory and useful modeling techniques ought to address now are much more clearly defined. The theoretical work has often been undertaken in appreciation of certain stylized facts that needed to be explained. The list of these 'facts' is indeed very long, ranging from the microeconomic evidence concerning for example dynamic increasing returns in learning activities or the persistence of particular sets of problem-solving routines within business firms; the industry-level evidence on entry, exit and size-distributions – approximately log-normal – all the way to the evidence regarding the time-series properties of major economic aggregates. However, the connection between the theoretical work and the empirical phenomena has so far not been very close. The philosophy of this project is that the chances of developing powerful new theory and useful new analytical techniques can be greatly enhanced by performing the work in an environment where scholars who understand the empirical phenomena provide questions and challenges for the theorists and their work.

In particular, the project is meant to pursue an 'evolutionary' interpretation of technological and economic dynamics modeling, first, the processes by which individual agents and organisations learn, search, adapt; second, the economic analogues of 'natural selection' by which inter-

active environments – often markets – winnow out a population whose members have different attributes and behavioural traits; and, third, the collective emergence of statistical patterns, regularities and higher-level structures as the aggregate outcomes of the two former processes.

Together with a group of researchers located permanently at IIASA, the project coordinates multiple research efforts undertaken in several institutions around the world, organises workshops and provides a venue of scientific discussion among scholars working on evolutionary modeling, computer simulation and non-linear dynamical systems.

The research focuses upon the following three major areas:

1. Learning Processes and Organisational Competence.
2. Technological and Industrial Dynamics
3. Innovation, Competition and Macrodynamics

Managing the Development and Transfer of Process Technologies in the Semiconductor Manufacturing Industry

Melissa M. Appleyard*

Nile W. Hatch**

David C. Mowery***

* Economics Department, University of California, Berkeley.
** Agricultural and Resource Economics Department, University of California, Berkeley.
*** Haas School of Business, University of California, Berkeley, and Canadian Institute of Advanced Research.

A revised version of this paper will eventually be published in Firm Capabilities and Strategy (tentative title), edited by G. Dosi, R.R. Nelson, and S. Winter. The research for this paper was supported by the Alfred P. Sloan Foundation, the U.S. Air Force Office of Scientific Research, and the Canadian Institute for Advanced Research. The support and advice of Dean David Hodges and Professor Robert Leachman of the U.C. Berkeley College of Engineering, Professor Clair Brown of the U.C. Berkeley Economics Department and Professor Neil Berglund of the Oregon Graduate Institute was invaluable in this project. The cooperation of managers from firms throughout the global semiconductor industry was also essential to this research project, and we appreciate their willingness to provide data and insights.

I. Introduction

During the last decade, scholars have developed a resource-based framework for analyzing the behavior and competitive strategy of the firm. This framework (which is also known as the theory of core competence, firm capabilities, etc.) was developed by Wernerfeldt (1984), Teece and colleagues (Teece 1989, 1988, 1993; Teece, Pisano, & Shuen, 1994) and Prahalad and Hamel (1990), among others, largely as a reaction against the dominant "competitive forces" analysis of firm strategy.[1] The resource-based theory of the firm suggests that a business enterprise is best viewed as a collection of sticky and difficult-to-imitate resources and capabilities that enable it to compete against other firms (Penrose 1959, Barney 1986, Wernerfelt 1984).[2] Rather than optimizing subject to some web of external constraints, the "capabilities" view argues, firms should seek to create rents through creating new capabilities that effectively relax such external constraints.

These resources can be physical, such as production techniques protected by patents or trade secrets, or intangible, such as brand equity or operating routines. Of particular importance is the specificity inherent in such resources: the same characteristics that enable a firm to extract a sustainable rent stream from these assets often make it difficult for the firm to "transplant" them and utilize them effectively in a new context. Thus, a firm that has developed an advantageous position is protected to the extent that its capabilities are specific and therefore difficult for others

---

[1] The "competitive forces" approach to the analysis of firm strategy is rooted in the neoclassical economics of industrial organization, and emphasizes the influence of industry structure on the profitability and performance of a firm, whose internal structure and history are of little consequence. Nelson (1994) argues that in neoclassical economics, "Firms facing different markets will behave and perform differently, but if the market conditions were reversed, firm behaviors would be too. Where the theory admits product differentiation, different firms will produce different products, but in the theoretical literature any firm can choose any niche. Thus there are firm differences, but there is no essential autonomous quality to them." (p. 253).

[2] "The capabilities approach sees value implementing strategic change as being difficult and costly. Moreover, it can generally only occur incrementally." (Teece, Pisano, & Shuen, 1994, p. 34).

to imitate, but this very specificity may constrain the firm's ability to transfer these resources to new uses, to apply them in unrelated lines of business, or to sell them in market transactions.

One area in which firm-specific competencies or capabilities appear to be significant is in the management of innovation within the firm. A considerable literature on firm-level differences in capabilities deals with product innovation. Intrafirm management of process innovation, however, has received less attention. Clark and Fujimoto (1991), as well as other scholars of the Japanese automobile industry, note the complementary relationship of process and product innovation, but the bulk of their analysis concerns product innovation.

This paper analyzes the management of new process technologies in the semiconductor industry, one in which the relationship between process and product innovation is far stronger than is true of automobiles. New process development relies on the replication of complex "routines" within a firm, since in many cases, a new manufacturing process is developed in an R&D facility and then transferred to a manufacturing site. Firm-specific differences in the management and organization of process innovation appear to be significant and influence performance.

Immediately below, we develop a conceptual framework for evaluating the role of firm-specific capabilities in the development and introduction of new manufacturing processes. The subsequent section establishes the importance for competitive performance of successful development and introduction of new manufacturing processes in the semiconductor industry, and presents data that characterize some of the consequences of poor performance in this activity. The case studies in Section IV provide a more detailed firm-level view of the activities that underpin the development and introduction of new manufacturing processes in this industry. The case studies suggest some managerial and organizational reasons for differential performance that complement the findings of other empirical models of new process introduction in semiconductor manufacturing. In Section V, we summarize the important themes that emerge from these case

studies for the "capabilities view" of the firm and discuss these and possibilities for further research in the conclusion.

II. The Creation and Replication of Firm-Specific Capabilities

According to Teece et al. (1992), the internal development of capabilities relies on organizational learning. Organizational learning is influenced by the environment of technological opportunities, but interfirm differences in skills, management, and organization may produce very different rates of learning among firms that are in the same industry and that face the same opportunity environment. The organizational learning that underpins the internal development of capabilities is path-dependent and localized. Development of its capabilities are constrained by a firm's current and historic activities, capabilities, and resources, reflecting the irreversibilities within this process. In addition, firms are not easily able to develop technological or other capabilities in markets or products that have little or no relationship to their current portfolio.

Technological resources are one of the most frequently cited firm-specific capabilities. Since these frequently rest on tacit knowledge and are often subject to considerable uncertainty concerning their characteristics and performance, they often cannot be purchased through arms-length, conventional contracts (Mowery, 1983). Other forms of firm-specific capabilities include knowledge of specific markets or user needs; idiosyncratic, firm-specific "routines," such as decisionmaking and problem-solving techniques; management information systems;[3] and complex networks for handling the marketing and distribution of products that include procedures for the systematic capture and analysis of user feedback. But empirical evaluation of the influence of

[3] The point-of-sale data collection and distribution systems of the U.S. discount store chain Wal-Mart is one example of an organizationally embedded system that has proven to be very difficult for competitors to imitate.

these factors on firms' behavior requires more detailed characterization of firm-specific knowledge, rather than measures that rely solely on inputs, such as R&D or marketing expenditures.

In the next two sections of this paper, we attempt an analytic description and characterization of the nature and influence of firm-level capabilities in new process introduction. The introduction of a new manufacturing process into high-volume production of semiconductor components provides an excellent example of the costs and complexities of the intrafirm "replication" of critical capabilities. As we note below, the complexities associated with the introduction of a new manufacturing process are nearly as forbidding as those associated with transferring mature manufacturing technologies among commercial production facilities within a single firm.

III. New Process Introduction in Semiconductor Manufacturing

The speed and effectiveness with which new products are developed and introduced into large-volume production is an important influence on competitive performance in a number of manufacturing industries. For example, new product development figured prominently in recent studies of international competitiveness in automobiles (Womack, et al., 1990; Clark and Fujimoto, 1991). There are good reasons, however, to suspect that the management of new process introduction is if anything even more important to competitive performance in semiconductors than is true in automobiles or most other manufacturing industries.[4] Semiconductor manufacturing processes are among the most complex commercial production processes in industry. The

[4] Pisano and Wheelwright (1995) argue that "...manufacturing-process innovation is becoming an increasingly critical capability for production innovation." Although these authors assert that "Few managers of high-technology companies view manufacturing as a primary source of competitive advantage," we found no evidence to support this statement in our fieldwork. Indeed, virtually all of the corporate managers in the U.S. and non-U.S. firms included in our study were deeply concerned with improving their management of the development and transfer of manufacturing process technologies, and devoted considerable resources to these activities.

fabrication of an integrated circuit with feature sizes and linewidths of less than one micron requires more than one hundred steps (e.g., patterning, coating, baking, etching, cleaning, etc.). Underpinning the principal steps are hundreds of individual manufacturing operations. The development of many of these steps is based on art and know-how rather than science; they are not well-understood and easily replicated on different equipment or in different facilities; and they impose demanding requirements for a particle-free manufacturing environment.

Product innovation in semiconductors depends on process innovation to a much greater extent than is true of automobiles. The introduction of a new automobile requires substantial time and investment to manufacture dies and tooling for stamping and forming body parts and components, but a new model rarely demands significant change in the overall manufacturing process. Semiconductor product innovations, on the other hand, often require major changes in manufacturing processes, because of the tighter link between process and product characteristics that typifies semiconductors. Moreover, imperfect scientific understanding of semiconductor manufacturing means that changes in process technologies demand a great deal of experimentation. New equipment, with operating characteristics that are not well understood, often must be introduced along with a new "recipe," also not well understood, in order to manufacture a new product. The complexity of the manufacturing process also means that isolating and identifying the causes of yield failures requires considerable time and effort.

The final reason to hypothesize that new process introduction plays a more important competitive role in semiconductors than automobiles is the nature of competition in the semiconductor industry--management of process technology is critical to firm strategy. Particularly in "commodity product" segments of the industry like memory chips, a new product commands a price premium for a relatively brief period, and being first to market is important to

profitability. Rapid "ramping" (growth in production volume) of a new product affects the returns to the large investments in product development and manufacturing facilities.[5]

Although the intensity of competition and the brevity of product life cycles arguably are greatest in the memory segment of the industry, the semiconductor industry overall faces shorter product life cycles and greater threats to individual firms' dominance from the entry of producers of close substitutes (e.g., the "cloners" of Intel's successful 80386 microprocessor) than is true of automobiles. Alvarez (1994) notes that the shrinkage of these product cycles means that rapid and smooth introduction of new manufacturing processes is becoming more and more important to competitive performance.[6] Indeed, the failure thus far of the PowerPC's challenge to Intel's dominance of desktop computers has been directly affected by Motorola's inability to expand output of the PowerPC microprocessor more rapidly. Simultaneously, Intel has relied on rapid development and "ramping" of new manufacturing processes to accelerate its introduction of a succession of improved versions of the Pentium and "Pentium Pro" microprocessors, making Motorola's challenge even greater.[7] Rather than a "capacity race," which was hypothesized to characterize US-Japan competition in DRAM manufacture (e.g., Steinmueller, 1982), this competition between architectures is driven by capacity utilization, which in turn is a function of success in new process introduction.

---

[5] Flaherty (1991) presents a model of capacity expansion races in the production of 64K DRAM memory chips that includes firm-specific constraints on capacity expansion and argues for the importance of such capacity expansion in the decisions of U.S. to exit the memory segment of the semiconductor industry. Although Flaherty identifies firm-specific differences in the "ramping" of new product volumes, she does not attempt to explain them.

[6] According to A.R. Alvarez, the vice president for R&D of Cypress Semiconductor, "Industrial success in the year 2001 will depend as much on the methods by which process development is conducted as it will on the results of process development." (Alvarez, 1994, p. 1).

[7] See Carlton (1995, p. B3), who notes that "...the PowerPC initiative has been hampered..." by "Motorola's inability to quickly produce PowerPC chips in volume quantities," while "...Intel has been making such advances in its Pentium technology that it has all but erased the advantage PowerPC was supposed to have in terms of lower price and greater performance."

A. *Semiconductor manufacturing technology*

A brief overview of the technology of semiconductor manufacturing processes will illustrate the complexities and importance of careful management of new process development and transfer. Semiconductor chips are produced on wafers of silicon by constructing layers of insulating and conductive materials in intricate patterns that define the function of the integrated circuit. Each wafer contains from dozens to thousands of identical chips with features as small as 0.35 μm.[8] Manufacturing facilities ("fabs") house the ultra-clean manufacturing environments, called cleanrooms, that limit particle contamination. The manufacturing process for semiconductor devices consists of hundreds of operations that are undertaken on a wide variety of processing equipment types. These operations are categorized into broader categories, known as modules, that correspond to the particular set of steps used to perform the manufacturing activities in each area of the fab, such as photolithography, etch, implantation, and metallization. The modules currently or previously used in the fab represent its manufacturing know-how and define its technical capabilities.

The microscopic dimensions of their features and their complex designs mean that particle contamination can severely impair the functionality of finished chips, leading to scrapping, which in turn affects the yield of the manufacturing process. There are two types of yield loss in semiconductor manufacturing: line yield is the fraction of wafers that survive the manufacturing process; die yield refers to the fraction of chips on surviving wafers that pass tests for functionality and performance at the end of the manufacturing process. In some cases, as when a wafer contains a number of very costly die that are produced through a large number of complex steps, manufacturers will aggressively pursue wafer scrapping, which reduces line yield, in order to

---

[8] To provide some sense of the size of these features, the average human hair is about 100 μm in width.

achieve higher die yield and reduce the number of processing steps carried out on nonfunctional wafers.

Although the firms in our study have organized their new process development activities in different ways, all of them employ the same general modules, and development and introduction of a new manufacturing process requires a common set of steps. Design of new process modules typically begins before the design of the new product that will use them, because a firm's existing process capabilities limit the nature of the new product designs that it can produce. In this phase of the development of a new process, new steps are developed and refined until they are consistently reproducible. Eventually, the new process steps are integrated into a complete process flow for which development continues to work on problems created by interactions among steps. Before the new product can be introduced to the market, it has to undergo a variety of performance and endurance tests collectively called qualification. Qualification is followed by a period of "ramping" output to commercial volumes.

A new process requires three types of process modules: existing modules, new modules using existing equipment, and new modules using new equipment. All of these modules must be integrated to support the new process flow. Although the incorporation of existing modules into the new process flow appears to be the simplest of the development activities needed for a new process, even this task often encounters unexpected results produced by the interaction of existing and new process modules. Developing and integrating new modules is even more difficult. As a manager from one of the fabs in our study noted, "Every new module will have at least one major problem to solve." In order to develop a new module on existing equipment within a production fab, managers must make tradeoffs between the new module's needs for experimentation and analysis and the manufacturing requirements of the other production processes. The most difficult activity in process development is the development of a new module that uses new equipment. In

this case, the problems of learning the physical parameters of the process are heightened by the need to learn the peculiar characteristics and parameters of the new equipment.

The challenges associated with developing new modules and incorporating existing modules into new processes are such that careful planning and coordinated development of product and process technology development are essential. For example, if a new process technology is introduced for the manufacture of modifications of existing designs, rather than for an entirely new product design, the introduction of the new process technology is simplified. Effective technology planning should also result in a new process that will accommodate as many future product generations as possible, using modules that can be incorporated into as many future processes and products as possible. This is especially important for modules that require new equipment; their high development costs need to be amortized by use in the manufacture of many subsequent product generations. Finally, the relationship depicted in Figure 1 indicates that new processes that incorporate a high percentage of new steps require more time for their development. Shorter development cycles therefore require better planning for the introduction of new products and processes, so that each new process utilizes a substantial share of the steps and modules associated with its predecessor.

B. Elements of "best practice" in new process development and implementation

Our field research led us to distinguish at least three general approaches to managing new process introduction. In our sample, one group of fabs introduces new processes that are well-understood, exhibiting relatively low defect densities at their inception. A second group of fabs introduces new processes that are less well-characterized,[9] and attempts to improve their

[9] Process characterization refers to the degree to which the firm understands the physical parameters and their interactions in the process. A process that is highly characterized, is well understood and has reproducible manufacturing results in all steps.

performance through learning by doing in the manufacturing fab. A third group of fabs focuses on the incremental development and modification of manufacturing processes, frequently introducing new processes and constraining the development of new products to conform to the constraints imposed by the development of their manufacturing process technologies. This last group of fabs consists mainly of producers of application-specific integrated circuits (ASICs) that operate as "foundries."

The uncertainties of many aspects of semiconductor manufacturing mean that most non-ASIC producers employ a dedicated development fabrication facility for new process development. The "development fab" serves a function in this industry that resembles that of the "pilot plant" in the chemicals industry. "Debugging" a new process in a development fab is more effective when the development fab resembles the manufacturing fab in as many aspects as possible, particularly in the equipment and materials used. Reflecting the complexity of semiconductor manufacturing, as well as the frequent need to alter production equipment as part of new process introduction, differences between the development facility and the manufacturing fab in their equipment sets and configurations can impede new process introduction. In response to this, a number of the fabs in our sample have adopted policies that require that the receiving fab have an equipment set that is identical to that on which a new process is developed in the development facility.

Even stringent requirements for equipment duplication, however, cannot eliminate all significant differences between the manufacturing environment and that of the development fab for some products or processes. In the case of DRAM products, the differences in manufacturing volumes between the development and manufacturing facilities of leading producers are so great that development fabs cannot fully replicate manufacturing conditions. This factor has contributed to the efforts of some DRAM manufacturers to move new processes out of their development fabs and into manufacturing more rapidly and at lower levels of process characterization.

C. *Measuring the costs of poor performance in new process introduction*

To further illustrate the importance of new process introduction for competitive performance, we simulate the penalties associated with a poor start with data from the U.C. Berkeley Competitive Semiconductor Manufacturing (CSM) study. [10] The losses associated with late introduction of a new process relative to one's competitors are largely opportunity costs. They include the lost revenues from the periods before the process is introduced, as well as the revenue premiums that are foregone because prices fall over the commercial life of a specific device. In contrast, the penalties associated with poor starting yields are primarily the higher manufacturing costs that result from lower line and die yields.

Figure 2 shows price trends for four recent DRAM products, from the 256K DRAM to the 16MB DRAM. The precipitous decline in prices observed here is not restricted to memory products, but applies to most semiconductor products. Early innovators enjoy a substantial price premium, but as additional firms enter the market and fabs reduce costs through learning, production expands and prices fall rapidly. Later entry imposes large penalties in the form of lost revenues.

To see this effect in more detail, consider the case of 4 MB DRAM products. Figure 3 shows the price path for this product through time, along with the dates at which each of eight new 4 MB DRAM manufacturing processes were introduced into manufacturing within the CSM sample. Our small sample of DRAM manufacturing producers does not include the earliest innovators in this product market and therefore excludes the "first-movers" that obtained very large price premiums in 1989. We can estimate the penalty that firms in our sample incurred through late entry, however, by calculating the difference between the prices they would have obtained in

---

[10] Funded by the Alfred P. Sloan Foundation, the CSM study is an interdisciplinary project at U.C. Berkeley with the goal of measuring and comparing semiconductor manufacturing performance in fabs around the world.

each period had they been the first to introduce the process, versus the prices obtained when they actually entered. For example, the penalty of delay in the first period of production in our sample is the difference between the price of the product in 1989, when the 4MB DRAM was first introduced, and the price obtained by the first entrant in our sample in its first period of production. The penalty of delay in the firm's second period of production is the price of the product in its second period in the market less the price the firm receives in its second period of production, and so on. Table 1 presents estimates of the monthly price penalties associated with delayed entry into manufacture in the 4 MB DRAM processes in our sample in the left-hand column for each process.

The high costs of delayed entry into a new product market mean that firms face significant incentives to be first to market with new products. But early entry has its costs, which may offset the higher unit revenues for "good die" that are associated with early entry. The most obvious reason to postpone entry is the need for additional time to develop and "debug" a product design or the new process sufficiently for volume manufacturing.[11] Firms have considerable discretion in the extent to which they characterize a new process in development before transferring it to a high-volume manufacturing environment. A poorly characterized process typically suffers serious yield problems in the manufacturing facility.

To illustrate the penalty associated with poor starting yields, we present another simulation based on the sample of 4 MB DRAM processes from the CSM study. The basis for this simulation is the widely held belief among semiconductor firms that the cost of manufacturing a wafer on a particular process is not affected by the number of die on the wafer. Therefore, the cost of producing an individual chip, whether it functions or not, depends on the wafer size and the die size. Let the wafer size be A cm^2 and the die have an area of a cm^2. Then the gross number of

11 Our data suggest that problems in process development dominate product design problems in delaying entry.

dice on the wafer x is A/a.[12] If we denote the manufacturing cost of a wafer as W, then the unit cost per die is

$$w = \frac{W}{x} = \frac{W \cdot a}{A}. \quad (1)$$

Now we introduce the influence of yield losses on manufacturing cost. If we let $y(t)$ denote the die yield at time t and q denote the number of functional dice produced, then $x \cdot y(t) \equiv q$.[13] Since the good output must bear the cost of yield losses, the manufacturing cost can be represented as $w \cdot x = c \cdot q$, where c is the average variable cost of good output. Thus, the unit cost of production, including the cost of yield losses, is

$$c = \frac{w}{y(t)}. \quad (2)$$

Equation 2 shows that the additional costs associated with yield losses are not trivial; a 20% loss in yield results in a 25% increase in unit cost.

Using our sample of new 4 MB DRAM processes, we simulate the cost penalties associated with the actual yields obtained after the processes are introduced into the manufacturing environment. This requires the simplifying assumption that all the processes have a manufacturing cost of $1000 per eight-inch equivalent wafer.[14] Using actual process yield data and the assumed wafer cost, we simulate the cost penalty associated with poor starting yields. This penalty is defined as the additional cost incurred by a producer whose yields are below those of the best of

---

[12] This calculation assumes that all the area on the wafer is utilized by chips. Actually, since the wafers are circular and the dice are rectangular, there is some lost area. For our purposes, we ignore the lost silicon at the edges of the wafer.

[13] We assume that yield is a function of time alone to allow for yield improvements. In fact, yield is not solely a function of time; its improvement depends on product and process design, process development and transfer characteristics, and manufacturing practices (see Hatch and Mowery, 1995).

[14] The assumed wafer cost is consistent with the estimated wafer costs reported by Reichelstein and Hatch (1993) that are based on data from the firms participating in the U.C. Berkeley CSM project.

our eight DRAM producers in each period. These penalties are computed only for the processes in our sample,[15] and the results are presented in Figure 4.[16]

Figure 4 shows that the differences in yield and the resulting cost penalties are volatile and occasionally large. The average cost of a die, ignoring yield losses, is $15. Thus, the yield penalty of almost $14 faced by an early entrant with a poor yield effectively doubles the manufacturing cost relative to the process with the best yields. These results show that the penalty for poor yields often is substantial in the early operation of a new process, and the variation among firms in cost differentials is largest early in the life of the process. The costs of different producers appear to converge somewhat over time, although even after three years the differences persist. Comparison of the two columns for each manufacturing process in Table 1, however, makes it clear that the penalties associated with late entry dominate those associated with poor starting yields. Time to market is critical to competitive advantage in DRAMs and, we believe, in other products. Nonetheless, the penalties associated with poor starting yields are considerable.

D. Modeling the determinants and effects of successful new process introduction

Hatch and Mowery (1995) use data on "defect densities" of new semiconductor manufacturing processes to model performance in new process introductions.[17] Longitudinal data on defect densities in new manufacturing processes point out several interesting characteristics of the learning processes that lead to improvement over time (i.e., declines) in defect densities. First, consistent with the views of scholars who emphasize the importance of firm-level differences in

---

15 There were many other 4 MB DRAM processes in production during this period that are not in our sample, some of which potentially had higher yields than any in our sample.

16 One of the processes in the sample began with extraordinarily low yields, resulting in a cost differential as high as $1465.63 per unit. To better illustrate the cost variation in most of the processes, the scale of the figure is chosen such that the early cost penalties of this unusual process are not visible.

17 The defect density of a new manufacturing process is simply the number of defects per square centimeter on the silicon wafer from which individual semiconductor chips are cut; it is inversely correlated with die yield.

capabilities, Table 2 reveals substantial performance differences among manufacturing facilities in the U.C. Berkeley CSM database (a group that includes producers of DRAMs and other memory products, logic, and ASIC products), measured as either the initial defect density for a new manufacturing process (the defect density reported for the first quarter of operation of a process in the manufacturing facility) or the average quarterly rate of improvement of defect density. Second, the penalties associated with a "poor start," a high defect density, are often very difficult to overcome. The data in Figures 5-6 reveal that manufacturing facilities that began with very high defect densities in new manufacturing processes found it very difficult to close the gap with the facilities that began with much lower defect densities. Third, manufacturing processes that are closer to the "technological frontier," which in this case are associated with smaller linewidths on semiconductor chips, display an even more pronounced "poor start" penalty. The data summarized in Figure 5 suggest that firms that begin with poor defect densities in submicron linewidth semiconductor manufacturing processes find it much harder to close the performance gap with the leaders. This result, of course, is precisely what one would expect--labor turnover, technical journals, and other sources of interfirm spillovers take time to transmit knowhow among competitors, and a superior starting point in the most advanced manufacturing processes therefore yields more enduring competitive advantages.

Statistical analysis of new process introduction (Hatch and Mowery, 1995) revealed several interesting findings. The rate of improvement or learning associated with a new manufacturing process was not solely determined by expansion in volume, but could be increased by allocating more engineering resources to the experiments and organized problem-solving activities that are necessary to reduce "parametric" defect densities.[18] These results suggest that

---

[18] Defects that cause die yield losses can generally be categorized as coming from unwanted particles or from exceeding the physical tolerance limits of a manufacturing step. The latter type of defects is commonly referred to as parametric processing errors and is a more serious problem in new processes whose parameters are not as well understood as mature processes.

in semiconductor manufacturing, "learning by doing" is not exogenous, but can be increased by management decisions. The allocation of engineering resources to problem-solving activities for a new process, however, affects the rate of improvement in other manufacturing processes being operated in the same facility.

Since most new semiconductor manufacturing processes are introduced into facilities that are simultaneously operating other, more mature processes, a poorly managed new process introduction can have broader effects on a firm's competitive performance. Yields and output of both a new product and existing products manufactured with more mature processes may all be reduced by an unsuccessful new process introduction. The negative effects of a new process introduction on manufacturing performance for existing products thus may increase the costs associated with the introduction of a poorly characterized manufacturing process into a commercial-volume fab. Because of their complexity, the previous section's simulation analysis did not include these costs, but their presence increases the costs and reduces the profits associated with a "first-to-market" strategy that it relies on extensive characterization of a new manufacturing process in a production fab that is operating older manufacturing processes.[19]

The analysis of management techniques for new process introduction also yielded some interesting results. The use of a dedicated development fab was associated with superior performance in improving defect densities, and locating this development facility on the same site as the high-volume manufacturing facility that was to receive the new process improved performance. Finally, identical production equipment in the development and manufacturing facilities was associated with better performance. Our model also suggests that there are important differences among product classes in the management and learning behavior associated with new

[19] The negative effects of new process introduction on existing processes will be higher still when more than one new manufacturing process is introduced simultaneously, something that was attempted in several of the fabs in the Berkeley CSM study.

process technologies. As we noted earlier, ASIC producers are more likely to introduce incremental modifications of their process technologies much more frequently, and are less likely to utilize development facilities. The "management" variables that were important in explaining interfirm differences for our broader sample were much less powerful for this product class. In DRAM manufacturing, we find that most of the critical problem-solving and learning associated with new manufacturing processes takes place in the "first generation" of a new family of DRAMs, e.g., the first product design and associated process for a 4MB DRAM. Later "shrinks"[20] of that DRAM product experience fewer problems in process development and transfer.

Although the statistical analysis revealed some generic practices that contributed to superior performance, firm-specific effects remained significant, as a fixed-effects model showed. These statistical results are consistent with a view of new process introduction that emphasizes interfirm differences in performance, especially in the most advanced products, and that stresses the role of management techniques in improving or degrading the smoothness of the transfer and the rate of learning. Semi-scale development facilities improve firms' performance in products other than ASICs, while significant differences among product classes affect firms' new process introduction. But considerable firm-specific variance remains unexplained, and requires a more detailed examination. In order to examine the sources of these interfirm differences in management and performance in greater detail, we undertook case studies of new process introduction in two firms in the CSM sample.

IV. Case studies of management of new process introduction

This section compares the management by two semiconductor companies of new process development and transfer to a commercial-volume fab. The comparison of new process

[20] A "shrink" refers to a redesigned chip with a smaller area, which increases die yields and may improve chip performance.

introduction strategies provides a sense of the similarities and differences among semiconductor firms in the capabilities and routines used to manage new process introduction. The firms are disguised as Supreme Technologies (ST) and Multiplex Electronics (ME). We focus on the introduction of one process flow for each company--memory for ST and logic for ME.

These cases seek to compare the new process introduction strategies of different companies facing different market conditions. Some products, such as DRAMs, are not differentiated significantly from one another; competition is driven largely by price. Competition among some types of logic devices, such as microprocessors, is driven by the attractiveness and the size of the installed base of the hardware architectures and software libraries associated with each--different product families are sharply differentiated from one another. These contrasts in product market environments may produce different approaches to management of new process introduction. Nevertheless, the technical challenges, and therefore, the metrics used to evaluate the success of new process introduction—yields and reliability—are consistent across the products of the firms in our sample. Furthermore, both firms participate in a number of product markets and neither company suggested that its strategy for new process introduction varied markedly across its product families. The differences in management of new process introduction among these firms thus appear to be largely the result of firm-level, rather than product-level, differences in technology and competitive strategies.

A. Supreme Technologies

Our first case study examined Supreme Technologies' introduction of a new process for a new memory product. The new process presented numerous technical and organizational challenges to ST, since it included a very high proportion of new steps and was eventually transferred to recipient fab that used wafers of a different diameter than the development fab. Prior to undertaking the development and transfer of this process technology, ST had conducted an

internal study of previous process transfers, and adopted policies to improve its performance and to impose greater discipline on modifications in the recipient fab following process transfer. But these reforms in ST's new process introduction policies did not produce a smooth process development and transfer. In particular, ST's plans for new process development were not well integrated with its product planning. The result was an overly ambitious project to develop a process technology that encountered serious delays, impeding the timely introduction of a commercially attractive product.

Among the new practices adopted by ST in the wake of its internal study were the assignment of a full-time leader to the project; the scheduling of regular meetings among project team members and between the team and representatives from other divisions in the company; the decomposition of the new process into modules to facilitate transfer to the volume manufacturing as each module was completed; the designation of a team in the recipient fab dedicated to the process hand-off; and the maintenance of a baseline process that would continue to run in the development fab for a year or two after the transfer to a volume fab. ST also attempted to align the incentives of engineers in its development fab more closely with those of engineers and managers in the recipient fab, recognizing that this could facilitate a smoother transfer of the process technology. The firm sought to create such alignment by rewarding its manufacturing fab for accepting the new process, rather than penalizing it for declines in performance or capacity utilization in the operation of existing processes. ST brought engineers from the recipient fab to the development site in the weeks prior to hand-off, encouraging them to learn the new process and accept responsibility for its successful transfer.[21] Relative to other firms we studied, however,

---

21 Volume fabs often resist the introduction of new semiconductor processes, since they can cause major upheavals, as people are trained on the new process and new equipment is calibrated and deployed. In some process steps, technical improvements contained in a new process are "backward compatible" and can improve yields of the existing process flow. The initial net effect nevertheless is negative, with the volume fab experiencing yield declines as it "ramps up" the new process to high volume.

fewer representatives from ST's recipient fab were rotated to its development fab, and they visited the development site for shorter periods of time.

The new process differed dramatically from that associated with ST's previous advanced manufacturing process for memory chips. Of the more than one hundred process steps involved in the new manufacturing process, approximately 90% were new, compared with a more typical share of 50-55% in a new process. Moreover, several of these new steps and modules, particularly in the etch module, had not previously been used in commercial-volume manufacturing and presented serious technical challenges. ST needed the new etch operations to pack more transistors into a smaller die area, but this module required new chemical and thermal specifications, as well as modifications in the equipment that exceeded the capabilities of currently available technology. ST had to enter into a co-development project with its vendor to ensure that the hardware would meet the new process specifications.

ST's development schedule assumed that the firm would have a baseline process running in the development fab two years after top management approved the process development project. Eighteen months after the project's inception, however, ST had to reorganize the core development team. The reorganized team retained only one person from the original team, and another year and a half was required to "qualify" the new process in the development fab.[22] The project thus was delayed by roughly one year. As we noted earlier, the costs of late entry in most segments of the semiconductor industry are high, and these delays in the process development project ultimately imposed serious commercial penalties on ST.

In retrospect, ST management acknowledged that the decision to pursue such an ambitious new process technology for this particular product was a mistake. Rather than developing a

---

22 Within ST, "qualification" of the process meant that the process was meeting its die and line yield targets. It also indicated that all modules were characterized sufficiently to facilitate the operation of the process within the development fab as a benchmark and to support its transfer to the manufacturing site.

technically demanding new process and new product simultaneously, managers argued that a "shrink" of an existing product should have been the focus of a less ambitious process development project, enabling the manufacture of a new product on a process with fewer radically new steps. Some of the new steps thus could have been incorporated into ST's volume manufacturing operations before the development of this new product began, and ST would have entered the market sooner. Rather than approaching the development of this process as one part of a portfolio of process and product capabilities that would be enhanced over the next several years, ST undertook an ambitious "moon-shot" effort for this single process and product.

Development and transfer to manufacturing of a less radically new process into its volume manufacturing facilities also would have permitted more rapid learning and debugging of the new process. ST's development facility was small, with no more than one of several critical pieces of equipment. Capacity constraints quickly appeared and often increased the cycle time for completion of a manufacturing lot or an experiment, slowing the evaluation of new process steps. The need to send chips to foreign facilities for packaging[23] produced other delays. The development fab occasionally was remiss in shipping finished die to the assembly stage, and the distant packaging operation failed to assign a sufficiently high priority to the very small lots of test wafers and die shipped by ST. These problems delayed reliability and "burn-in" testing, which required packaged chips. The development team felt that the long cycle times of ST's development fab and assembly operations were a critical impediment in developing the new process.

Development fab capacity was also constrained by the decision of ST senior management during the third year of the project to rely on this facility for production of small volumes for sale of the product that relied on the new process. ST sought through this policy to overcome some of

---

23 "Packaging" refers to the insertion of a die into a casing, usually made of plastic or ceramic, that can be inserted into a computer "motherboard" or some other board-level assembly for incorporation into an electronic systems product.

the commercial penalties resulting from the delays in the development of the new process. The policy nevertheless may have produced further delays, since the new process had not yet been fully characterized, the installation of new equipment in the development fab diverted engineering effort, and as new operators were hired and trained.

Although its internal study of previous new process development projects did not prevent the firm from pursuing a project that was technically too ambitious, ST used the study's findings to impose discipline over equipment selection and problem-solving within its process development activities. In parallel with the development of the new process, a senior ST manager formed an equipment group with representatives from both the development and manufacturing facilities to consolidate and rationalize the company's production equipment set. Consolidation entailed coordinating all future equipment purchases across ST's fabs down to the model number, as well as the imposition of identical specifications for the fabs' chemicals, gases, and temperature settings. During its monthly meetings, the equipment group reviewed the new equipment requirements of the process under development. The equipment group afforded the manufacturing facilities' engineers a voice in equipment selection, in order to increase their commitment to the success of the new process, while also providing them with a preview of the new process technology.

In addition to their involvement in equipment decisions, ST's development engineers participated in three regularly scheduled meetings that dealt specifically with the process development project. A daily morning meeting was brief and informal, and consisted largely of reports from each of the engineers in the core development group on findings and new problem areas uncovered during the previous day. A second, weekly meeting was attended by ST's top management and representatives from the development team. The leader of the development team presented a formal status report on the team's progress against intermediate and long-term

milestones and the primary obstacles. Managers from each process module attended the weekly meeting to field specific technical questions, and as the date of "qualification" of the process approached, managers from marketing and back-end operations, such as packaging, began to attend these meetings. A third regular meeting was a quarterly review attended by representatives from all of the company's manufacturing fabs, and was intended to provide detailed technical information on both the characteristics of the new process technology and its state of completion. At the quarterly review, the development team leader presented the results from the electrical and reliability tests, described the progress in developing each step of the new process, and responded to questions and requests for action from the previous quarterly meeting. Manufacturing fab representatives provided a number of suggestions, most of which sought to eliminate steps.[24]

Although this description of the number of meetings indicates the importance assigned by senior ST managers to the maintenance of good communications between the development engineers and their counterparts at the volume fabs, cross-functional communication often was deficient. Serious communication failures occurred between marketing and engineering and between "front-end" engineering (making the chip) and "back-end" engineering (packaging and testing the chip).

Well into the second year of developing this new process, ST had yet to fully commit to a specific size or capacity for the "cells," the building blocks within the chip that would be produced with the process. Although this key commitment usually is made by engineering and marketing staff at the outset of a project, as late as the beginning of the transfer of the new process technology from the development fab to the manufacturing site, discussions continued over possible changes in the size of the cell. The cell architecture for this memory chip was relatively simple by

---

24 According to one of ST's manufacturing fab managers, the ability of a manufacturing facility to absorb, learn, and "ramp" a new process declines significantly as a function of the number of steps in the process, and presumably does so even more dramatically as the number of new process steps grows.

comparison with that of other products, such as microprocessors, and changes in its architecture therefore were less disruptive. Nonetheless, ST's delays in committing to a specific cell design added another layer of uncertainty to an already complex project. Engineering resources were diverted from the technical problems associated with the process flow and committed instead to studies of the technical tradeoffs associated with each proposed cell type, with little participation from marketing personnel.

Another critical decision that was deferred or changed late in the process development project concerned the identity of the recipient production fab for this new process. The recipient fab was shifted no more than 6 months before transfer commenced, an especially risky policy in view of the fact that the newly chosen recipient fab was equipped to process wafers of a different diameter than the development fab.

This development project violated a number of the procedures that had been recommended in ST's internal study, including the directive to avoid shifting the identity of the recipient fab late in the development project, and the requirement for maximum compatibility in equipment sets between recipient and development fab, including comparable wafer diameters. The firm plans to conduct a more extensive "post-mortem" study of the project that will develop another set of guidelines for the next project. But ST's difficulties with this project suggest that additional study will not suffice to improve its management of new process development and introduction. The project suffered from overly ambitious goals and a failure to link process and product development strategies more effectively in a timely fashion. Coordination between marketing and engineering at an earlier stage in the development cycle remains a major challenge. Although the development project ultimately succeeded, poor cross-functional communication reflects another longstanding problem at ST: its reliance on heroic efforts by individuals, rather than team-based problem-solving throughout the development cycle.

B. *Multiplex Electronics*

A central characteristic of new process introduction at ME is the breadth and depth of the firm's efforts to achieve precise duplication of process and equipment specifications between development and manufacturing and across all sites running a particular process.[25] By instituting company-wide duplication of equipment, materials, automation systems, and statistical process control procedures, ME ensures the reliability of its chips and manufacturing processes. Achieving this level of duplication was costly; the company took approximately six years to fully implement its duplication strategy. To facilitate the acceptance of its duplication strategy, ME formed teams with multi-site membership to select equipment and approve process changes. ME also has overlapped development with manufacturing to the greatest degree of any of the companies whose new process development practices we studied in detail, in order to support more precise duplication between development and production, while cutting the ramp time at the volume recipient fab.

ME strives to avoid the difficulties that ST experienced with the simultaneous introduction of a new process and a new product design by following strict new process introduction procedures that extend across multiple generations of a given product and process. The first version of a new product design typically is a relatively large die size, and it is manufactured with a process that has been developed for a prior-generation device. The first "shrink" of this new product, however, is designed under the supervision of the development staff, and its production relies on a process that incorporates more new steps. Thus, an all-new product relies on a process that is relatively well-understood, and a substantially new process is used only for the manufacture of a product design whose general performance and manufacturability are relatively well-understood. Another stark contrast with ST is ME's effort to attain at least 70% overlap in steps and in equipment

---

[25] Due to altitude and temperature differences between their fabs, ME permits some variation in the process specifications across its sites.

requirements across process generations. ME generally undertakes major technical revisions of process modules only with the inception of a new process development project. ME managers stated that forecasting design rules and process technology requirements more than one generation into the future is simply too difficult.

ME has adopted an unusual approach to new process development that combines the process development and early-stage, commercial-scale manufacturing activities in a single "hybrid" facility. The development and early-stage volume production of each successive new product take place within a fab constructed specifically for that process. Rather than developing a new process in a specialized development facility and then transferring it to a volume manufacturing site, ME develops a new process in the hybrid facility, where it is eventually implemented at commercial scale. No transfer therefore is needed prior to the achievement of commercial production volumes; complete equipment duplication between the development and early-stage volume manufacturing is guaranteed; and several members of the development team for each project typically remain with the process once it is "ramped up" in this new facility. Eventually, several months after the process has been ramped up in the hybrid facility, it is transferred to a very high-volume production facility. This transfer requires substantial personnel rotation and equipment duplication. The new process remains in operation in the hybrid facility for at least 12 months after the transfer, in order to provide a production baseline for the very high-volume facility.

The ME strategy for new process introduction has shifted power and responsibility for a broad range of activities within the firm to its process development group. Development within ME now is responsible for designing and constructing new manufacturing capacity both at the development site and the high-volume manufacturing site, and for hiring technicians and engineers to sustain the process baseline. Surprisingly, in view of its large investment in policies for ensuring

a relatively smooth development and transfer of new process technologies, ME does not emphasize design for manufacturability in the first generation of a new product offering. ME's circuit design group finalizes the design rules at an early stage in the development of manufacturing process technology, and the development group is charged with developing a process to meet those rules (the design of "shrinks" of a new product, as we noted earlier, nonetheless is the responsibility of the process development group). The manufacturing fabs contribute very little to changes in design rules, since development and early commercial-scale production occur at the development site. Although the high-volume manufacturing sites eventually do become involved in negotiating with the development group over the transfer, the development group has selected and developed the new modules for a new product well before manufacturing engineers become involved.

For each new process, ME brings production personnel from its very high-volume commercial manufacturing facilities to the development site for six months to a year to assist in "ramping" the new process in the hybrid fab. The integration engineers from the recipient fab are the first to make the trip, followed by engineers and technicians from each equipment module. Compared with the development fabs at ST, ME's development fab produces up to seven times more wafers per week at the time of the transfer to the production facility. Indeed, the peak capacity of ME's dedicated hybrid fab for some processes is comparable to that of several of ST's commercial-volume facilities.

"Ramping" production volume in its development fab has several advantages for ME. Personnel from the production fabs acquire the experience at the hybrid fab to run a high-volume ramp more efficiently when they return to their very high-volume facility. Requests from the recipient fab for changes in the equipment set or the process recipes are reduced by the involvement of many of the fab's engineering staff on the first ramp of the process. The otherwise detrimental effects of the geographic separation of the very high-volume commercial manufacturing facility

from the development site are reduced through rotation of personnel between these sites. Since the first production ramp occurs at the hybrid fab, development engineers stay involved with the new process through a ramping exercise and are able to resolve manufacturing problems that are revealed only at commercial-scale volumes. The high costs of new equipment for the development facility are charged to manufacturing, rather than to development, and purchases of multiple pieces of each type of equipment are amortized across these relatively high production volumes. The ability to effectively develop a new process in the relatively large-volume hybrid facility thus reduces many of the capacity constraints that slowed the rate of learning for ST in its process development, and the higher volumes reveal certain classes of problems that otherwise would remain hidden from the development engineers. Finally, ME's strategy accelerates the achievement of sufficient production volumes of reliable chips that can be marketed to select customers and provided as samples to other purchasers.

The hand-off to the high-volume manufacturing fab commences when the hybrid fab has begun increasing its own production volume. Before the hand-off, the source and recipient fabs negotiate "boundary guidelines and conditions" that guide each step of the transfer, describing all procedures and recipes in detail. Discussions between development and manufacturing over the process transfer center on recipe optimization, maintenance procedures, manufacturing goals, and transfer deliverables, and include extensive documentation. By the time of transfer, a large binder containing all of the specifications of the new process is compiled, based in part on the experience of the development team in ramping the new process in this hybrid fab. An important section of the binder describes failure patterns, in order to provide guidance in trouble-shooting to manufacturing fab engineers.

During the transfer, the recipient fab can apply for a waiver to a particular "boundary condition," but without compelling data, waivers related to process steps or recipes are not

allowed. Equipment changes are rarely allowed under the waiver system, although changes in materials or chemical inputs are allowed more frequently. When the source and the recipient fab reach an impasse regarding the specifications of a step, a corporate oversight committee resolves the conflict. This committee also oversees transfers of process technologies among the very high-volume production fabs operated by ME.

ME typically organizes the transfer team responsible for moving a new process from the hybrid to the commercial production fab six to eight months prior to certification of a new process in the hybrid fab. Both the development and recipient fabs contribute members to the team, which has twenty to thirty members. The core team is divided into five subteams that focus on the major equipment modules: photo, implant, thin films, etch, and metallization. Both the team and subteams are cross-functional ones; each subteam has at least one equipment engineer and at least one process engineer. A test engineer is also a member of the team. In addition, one to two team members concentrate on human resources issues such as what training will be needed by operators at the recipient fab in order to run the new process. In contrast to this practice, ST did not assign a high priority to the training of operators or technicians within their process hand-off regimen.

ME has aggressive goals for new process hand-offs: the very high-volume recipient fab is expected to attain yields that are within 1% of the hybrid development fab's last yield at the time of the transfer.[26] This aggressive goal relies on the extensive overlap of manufacturing and development activities and personnel described above. Over two hundred test wafers are partially processed by both the source and recipient fabs during the transfer, to verify the process and its transfer. ME also closely monitors the rate at which the volume production fab expands its weekly wafer starts.

---

26 At the time of release to volume manufacturing, ME wishes to achieve a defect density of 0.2 per cm^2 at its development site.

ME seeks precise duplication of all aspects of manufacturing processes among its very high-volume production facilities operating a given process. ME's equipment group began a program more than six years ago to develop a consistent equipment set across its very high-volume fabs and to present a united corporate front in negotiations with equipment vendors. The equipment group looks five years behind and ten years ahead when making equipment recommendations to the company. When the equipment group receives a request from development to purchase a new machine, a selection team is designated. The selection team contacts the major suppliers and determines which supplier can best deliver the desired processing capability. ME prefers buying equipment "off the shelf," and will resist modifications in some pieces of equipment that threaten exact duplication among its production sites--in some instances, this policy has delayed adoption of equipment advances. When negotiating with one of its primary vendors, ME coordinates discussion across process generations, discussing both future needs and the performance of the vendor's equipment currently installed in ME's manufacturing and development sites. Sending their vendors a "single message" has strengthened the firm's "engagement" with their vendors, according to ME managers. Complementing the efforts of the company-wide equipment group, user groups are formed with membership drawn from ME's production sites. The user group for a particular tool decides on upgrades and negotiates with the vendor on how to implement them.

ME's efforts to achieve precise duplication of manufacturing processes across its fabs rely on tight, committee-based control of changes in any aspect of these processes. The recipient fab and all of ME's fabs that subsequently receive the process can propose changes resulting from experimentation in the manufacturing facilities, but the process-change committee must approve all changes before their adoption. The committee then disseminates the new process specification to all fabs running the process. The composition of the committee changes over the life of a specific

manufacturing process. Initially, the development organization plays a major role, but as the new process migrates to several high-volume manufacturing facilities, one is designated as the custodian of the baseline process and the development organization's role within the committee is reduced.[27]

The evolution of ME's approach to new process development and introduction has relied in part on systematic efforts to learn from successive projects. ME follows a rigorous "post-mortem" exercise by which they review each phase of the development cycle to learn how they can improve. The post-mortem team drafts a memo detailing the issues and corrective actions, and distributes it to the team working on the next new process development project.

V. Capabilities, routines and common themes in management of new process introduction

The focus of this paper is the firm-level capabilities or routines that influence performance in new process introduction, a classic case of the creation and replication of a very complex, uncertain set of procedures within the boundaries of the firm. The procedures involve phenomena that are not well understood and knowledge that is highly tacit. Moreover, management of the transfer of new process technologies is a relatively new requirement within the semiconductor industry. Significant increases in the complexity of this industry's process and product technologies during the past 15 years have intensified the need for a more systematic approach to new process development and transfer--indeed, the very concept of a separate development facility has become widespread within the industry only since the mid-1970s.

We find little evidence within the U.S. and non-U.S. semiconductor manufacturing industries to support the view that process technology is ignored by managers concerned with

---

[27] The development fab runs the baseline for at least a year after the transfer to the initial high-volume site. Then the process is likely transferred to an additional very high-volume site, and the initial recipient maintains the baseline process.

competitive performance; managers in this industry devote considerable effort and attention to improving their management of new process development and introduction. Rather than managerial inattention, we believe that it is the sheer complexity of managing intrafirm development and replication of process technologies that is responsible for significant interfirm performance differences. In this section, we analyze the approaches taken by semiconductor producers to manage new process introduction, in order to better illustrate the sources and nature of the firm-level capabilities or routines that may underpin them.

A striking element of similarity between the firms that we studied in detail was their focus on avoiding repetition of past mistakes by learning from them. Both ST and ME had conducted studies of previous new process development and transfer projects and had implemented changes based on the conclusions of those studies. ME was far more systematic in this self-study process, conducting detailed retrospective reviews of each major project and continuously adjusting the structure of their policies for management of new process introduction in response. ST, on the other hand, had undertaken only one comprehensive retrospective study that spanned a number of projects. Although this study led to significant changes and improvements in ST's management of new process introduction, it did not address several fundamental issues, and the resulting pressures on ST's process development project may have contributed to the firm's failure to adhere strictly to the study's guidelines. One normative conclusion about the development of firm-level capabilities that seems to be supported by this small sample of cases is the importance of continuous efforts to learn from experience--the firms that have performed best in this complex activity are those that have systematically gathered retrospective performance data on a series of projects.

ME's internal studies emphasized the importance of strategic integration of new process and new product development programs through a plan that spanned a number of product and process generations. Semiconductor producers need product and equipment "roadmaps," which

lay out the next several generations of a company's products in a given line of business or product line, detailing plans for alternating between the introduction of "shrinks" of established products and entirely new product designs. At the same time, such a plan must guide the development and introduction of new generations of process technologies, which in turn impose requirements for equipment purchases that will span multiple generations.[28] Implementing the roadmaps requires support from senior management, as well as close coordination among integration engineers, module developers, and a company-wide equipment group.

Because the integration of these functions is most logically undertaken by the process development organization, the increasing importance of effective management of new process introduction appears to be expanding the power and authority of the process development organizations, relative to both product design and manufacturing, within both of the firms we studied in detail. This expansion of the power of the development organization seems particularly noteworthy in the sphere of manufacturing. Engineers at the recipient fabs in both firms are expected to avoid any undocumented "tweaking" of the process once it has been transferred to their facilities. Moreover, both firms exercise controls of varying degrees of stringency over equipment choices in their recipient fabs. The controls enable the firms to maintain high levels of equipment duplication between the development and recipient fab, and among the various manufacturing facilities that are operating identical pieces of equipment.

The effort to maintain discipline within new process introduction thus can discourage creativity and problem-solving activities within the manufacturing operations of these firms, an outcome that could be very detrimental to manufacturing performance. In addition, of course, the ability of a development facility to replicate all aspects of the high-volume manufacturing environment is limited. ME insisted on precise duplication of all process steps and equipment to

---

[28] A large share of capital expenditures goes to equipment. Currently, high volume fabs cost around $1 billion, with 85 percent spent on equipment and 15 percent on facilities.

the greatest degree, but even ME permits changes to the process specifications that are approved by a corporate review committee. Nonetheless, the resulting disincentives for creativity within the manufacturing fabs may eventually create problems in recruiting and retaining engineering talent in these operations. Similarly, the insistence on equipment duplication has high costs--when a new process is introduced, older equipment may be scrapped before the end of its useful life. Moreover, delaying the use of new equipment until a complete set can be installed in both the development and recipient fabs, or until precise duplication is possible among all of a firm's manufacturing fabs, may slow the adoption of state-of-the-art equipment. The fact that firms are willing to incur these potentially high costs is indicative of the importance assigned to equipment duplication, which in turn indicates the extraordinary uncertainty that attends process development and transfer.

The increased importance of effective management of new process development and transfer that is responsible for the growing authority of the development organizations within these firms has important implications for the organization of the development organization itself. We noted in our earlier discussion that development fab capacity constraints are a serious problem in the development of a new manufacturing process, since they can slow the rate of learning. But these constraints are exacerbated by the requirement within many firms that a new process be operated within the development fab as a "benchmark" for months after its transfer to a volume manufacturing site. Operation of a new manufacturing process as a benchmark in the same facility that has responsibility for developing the next one requires a substantial investment in equipment and trained operators. The firms in our case studies addressed this requirement in different ways. The ST development fab was ordered to begin to show a positive revenue stream by manufacturing larger quantities of products from the new process in a far more disciplined fashion. But the complexity of this new manufacturing process meant that the development team simultaneously had to complete development of the process while producing commercially viable components.

Rather than a benchmark, ST's new process was still under development when it first began producing components for sale, and the rate of learning suffered. ME overcame development fab capacity constraints by developing the new process in a hybrid commercial-scale facility and continued operation of the new process in that facility for some months after its development and transfer to a very high-volume production facility.

All of the companies we studied in detail, and most of the firms in the larger CSM project, exchange personnel among their research group, their development group, and their manufacturing fab receiving the new process. Although documentation with detailed process specifications often travels with the people between each stage, the written word cannot serve as a perfect substitute for personal experience. Frequently the documentation provides details on only a single process step and does not describe all of the unsuccessful experiments leading to the adopted recipe. The details of the experiments that did not work are often only logged in an individual engineer's lab book or memory, requiring that person's presence during transfer.

Generally, the hand-off between development and manufacturing poses a more difficult problem of acceptance than the hand-off between fundamental research and the development organization. The realities of a high-volume manufacturing fab rarely match those of a small scale development fab, as we noted earlier--up to ten times as many wafers run through a volume fab relative to a development fab, requiring possible revisions to the new process, particularly in the equipment calibration and maintenance areas. By bringing manufacturing engineers to the development fab before the new process is frozen for transfer, a company can incorporate the suggestions of the manufacturing personnel and heighten the likelihood that the manufacturing staff will accept ownership of the new process. The complexities of long-distance transfer of a new process from development to recipient fab have led an increasing number of semiconductor firms now to co-locate their development and manufacturing facilities; the results of our statistical

analysis suggest that this policy should improve performance. If this strategy is widely adopted, centers for semiconductor R&D, such as California's Silicon Valley, could witness the departure of development organizations for the rapidly growing manufacturing sites in Texas, the Southwest, or the Pacific Northwest.

VI. Conclusion

Students of firm-level capabilities emphasize the persistence of differences in performance, as well as behavior, among firms in the same industry that are not well addressed by other approaches, such as neoclassical economics or the structure-conduct approach to strategy developed by Porter (1980). This view also stresses the "embedded" nature of such capabilities--they develop out of idiosyncratic investments and processes, and competitors find it difficult to duplicate them through imitation or other types of interfirm "spillovers." Although this view of the firm appeals to intuition and casual empiricism, it is difficult to prove or disprove through empirical testing. Measures of firm-specific capabilities are difficult to collect on a large scale, and the performance consequences of differences in such capabilities are not easily determined.

This paper has examined one of the most important firm-specific capabilities for competition in the semiconductor industry: the ability of firms to develop, introduce, and expand production with new processes. A firm that is slow to expand the output of a new product, or introduces a new product with a very poorly characterized manufacturing process, faces severe cost and profit penalties. Despite its legitimate claim to be a high-technology industry, knowledge of the precise details of many semiconductor manufacturing processes is so limited that their performance cannot be predicted without extensive experimentation. This characteristic of the process technology makes it highly tacit and means that firm-level differences in managing new process introduction are likely to persist and will have important consequences for performance.

One of the major challenges in new process introduction is the intrafirm transfer of a complex technology. The movement of a new manufacturing process from its origins in a dedicated development facility to a commercial production site is very demanding, and requires extensive planning and investment. The transfer of a manufacturing process among commercial-scale production facilities, which involves a process technology that is more mature, well-understood, and stable, also is a major challenge. Moreover, the capabilities that are exploited by firms to manage new process introduction cannot be reduced to differences in human capital. The skills seem to be organizational, rather than exclusively individual. One firm's hiring the most skilled process engineers of another firm may be necessary, but it is not sufficient, to "reverse engineer" and introduce a new manufacturing process.

Like new product development, new process introduction is an element of high-technology competition in which management and organization matter at least as much as basic technological knowledge or even the technical skills of the workforce. Moreover, one of the most important characteristics of firms that are relatively successful in new process introduction is precisely the coordination of new product and new process development strategies. The case studies of individual firms' management of new process introduction emphasize the importance of developing a strategy for both process and product technologies at the very early stages of "product definition" (Bacon et al., 1994). But these plans also must extend across several generations or even several families of products, so as to avoid the requirement to develop an ambitious new product and process simultaneously. The demands of new process introduction for equipment selection, characterization, and standardization within a firm also mean that collaboration between manufacturers and their equipment suppliers can yield significant payoffs. Indeed, this type of "vertical" collaboration now is a central mission of the U.S. semiconductor R&D consortium,

SEMATECH, and has proven to be easier to sustain than collaboration among manufacturers on developing a "benchmark" process technology (Grindley et al., 1994).

An important issue for further research concerns the apparent contrast between the development of process technologies in the chemicals and semiconductor industries. U.S. chemicals manufacturers relied heavily on semi-scale "pilot plants" during the 1920-60 period for developing new manufacturing processes, because they were operating with technologies characterized by high levels of uncertainty. During the past 25 years, however, more extensive use of computer simulations and other techniques appear to have reduced the importance of pilot plants. The chemicals industry also is characterized by high levels of interfirm licensing of process technologies. The pattern of development of process technology in the semiconductor industry presents a significant contrast--semi-scale development plants have become much more important as the process technologies have become more complex. Moreover, licensing of process technologies (as opposed to designs) appears to be less widespread. The reasons for these contrasting patterns of development in two of the most technology-intensive modern manufacturing industries merit further investigation.

Evaluation of the strategies through which firms strengthen or erode their capabilities in such critical functions as new process introduction also merits additional work. Longitudinal data on the performance of a single firm or group of firms, along with more detailed data on the management and organization of their process development activities, are needed to answer this question. Our case studies provide a snapshot, rather than a history of new process development in two semiconductor manufacturers, but they do strongly suggest that one of the most important factors in firms' improvement of their management of new process introduction is the ability to learn through systematic retrospective assessments of previous projects. Both of the firms in our

case studies had undertaken systematic studies of their previous performance, and both attempted, with varying degrees of success, to learn from past successes and failures.

Systematic collection and assessment of performance data are critical to the day-to-day management of mature semiconductor manufacturing processes. Our research suggests that such data collection, review, and learning are no less essential to improving performance in new process introduction, an activity of growing competitive importance in this industry. Inasmuch as the technology of semiconductor manufacturing recently has "outrun" the progress of scientific understanding of the underlying properties of these complex processes, manufacturers must develop capabilities to support incremental learning and reduce the risks attendant on the development and transfer of the new process technologies that are indispensable to competitive success in this industry.

REFERENCES

Alchian, A. (1950) "Uncertainty, Evolution and Economic Theory," Journal of Political Economy 58:211-221.

Alvarez, A.R., "Process Requirements Through 2001," presented at the Second International Rapid Thermal Processing Conference, Monterey, CA, August 31, 1994.

Argyres, N.S. (1995) "Technology Strategy, Governance Structure and Interdivisional Coordination," Journal of Economic Behavior and Organization, forthcoming.

Bacon, G., S. Beckman, D.C. Mowery, and E. Wilson, "Managing Product Definition in High-Technology Industries: A Pilot Study," California Management Review, 1994.

Carlton, J., "Apple, IBM, Motorola PowerPC Group Issues Blueprint for a Common Computer," Wall Street Journal, 11/15/95, p. B3.

Clark, K.B., and T. Fujimoto, Product Development Performance: Strategy, Organization and Management in the World Auto Industry (Boston, MA: Harvard Business School Press, 1991).

Clark, K.B., and T. Fujimoto, "Reducing Time to Market: The Case of the World Auto Industry," Design Management Journal, 1991.

Competitive Semiconductor Manufacturing Program, The Competitive Semiconductor Manufacturing Survey: First Report on Results of the Main Phase (University of California, Berkeley: Engineering Systems Research Center, 1993).

Dertouzos, M.L., R.K. Lester, and R.M. Solow, Made in America (Cambridge: MIT Press, 1989).

Dierickx, I. and K. Cool (1989) "Asset Stock Accumulation and Sustainability of Competitive Advantage," Management Science, 35(12):1504-1514.

Flaherty, M.-T., "Manufacturing and Firm Performance in Technology-Intensive Industries: U.S. and Japanese DRAM Experience," unpublished MS., 1992.

Grindley, P., D.C. Mowery, and B. Silverman, "Lessons of SEMATECH for the Design of High-Technology Consortia," Journal of Policy Analysis and Management, 1994.

Hatch, N.W., and D.C. Mowery, "Process Innovation and Learning by Doing in Semiconductor Manufacturing," presented at the American Economic Association meetings, Washington, D.C., January 4-6, 1995.

Nelson, R.R. and S.G. Winter (1982) An Evolutionary Theory of Economic Change. Cambridge: Harvard University Press.

Penrose, E. T. (1959) The Theory of the Growth of the Firm. New York: Wiley & Sons.

Pisano, G.P. (1990) "The R&D Boundaries of the Firm: An Empirical Analysis," Administrative Science Quarterly 35: 153-176.

Pisano, G.P., and S.C. Wheelwright, "The New Logic of High-Tech R&D," Harvard Business Review, September-October 1995, 93-105.

Porter, M.E. (1980) Competitive Strategy (New York: Free Press).

Porter, M.E. (1994) "Towards a Dynamic Theory of Strategy," in R.P. Rumelt, D.E. Schendel, and D.J. Teece, eds., Fundamental Issues in Strategy. Boston, MA: Harvard Business School Press.

Porter, M.E. & M.B. Fuller (1986) "Coalitions and Global Strategy," in M.E. Porter (ed.) Competition in Global Industries. Boston, MA: Harvard Business School Press.

Prahalad, C.K. and G. Hamel (1990) "The Core Competence of the Corporation," Harvard Business Review 68: 79-91.

S. Reichelstein and N. Hatch, "Defectives, Learning, and Relevant Costs," unpublished MS, October 1992.

Silverman, B.S. (1994), "Technical Assets and the Logic of Corporate Diversification," unpublished manuscript, University of California, Berkeley, Haas School of Business.

Teece, D.J. (1980) "Economies of Scope and the Scope of the Enterprise," Journal of Economic Behavior and Organization 1:223-247.

Teece, D.J. (1982) "Towards an Economic Theory of the Multiproduct firm," Journal of Economic Behavior and Organization 3:39-63.

Teece, D.J. (1986a) "Profiting from Innovation," Research Policy 15:286-305.

Teece, D.J., R.P. Rumelt, G. Dosi, and S.G. Winter (1994) "Understanding Corporate Coherence: Theory and Evidence," Journal of Economic Behavior and Organization 23(1): 1-30.

Teece, D., G. Pisano, & A. Shuen (1994) "Dynamic Capabilities and Strategic Management," Working Paper, Center for Research in Management, University of California at Berkeley

Womack, J.P., D.T. Jones, and D. Roos, The Machine that Changed the World (New York: Rawson Associates, 1990).

Figure 1: Time to Market vs Relativity Complexity

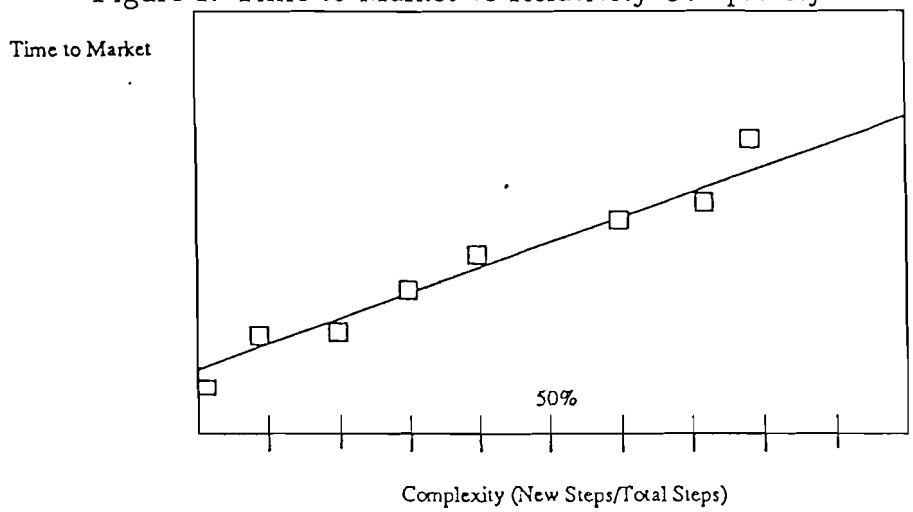

Figure 2: Price Trends for DRAM Products

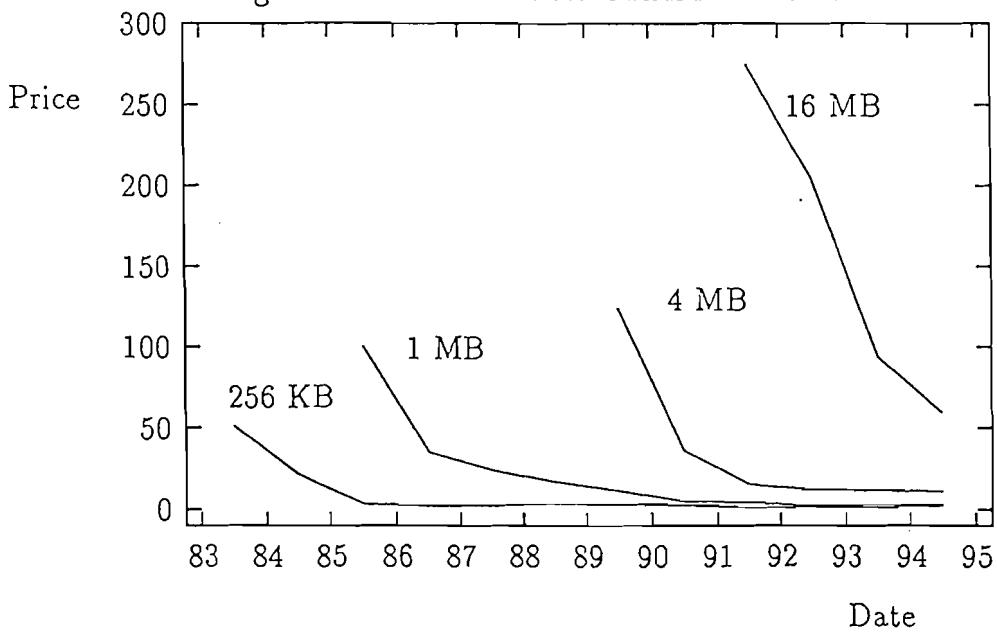

Figure 3: Price Trend and Start Dates for 4 MB DRAM Products

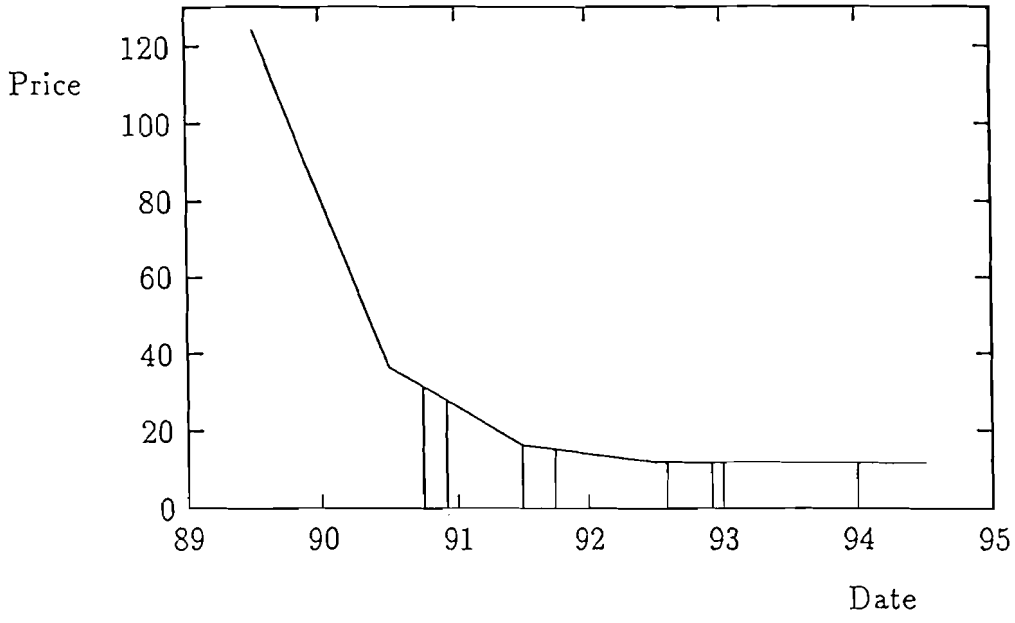

Figure 4: Simulated Penalties for Poor Starts Among 4 MB DRAM Processes

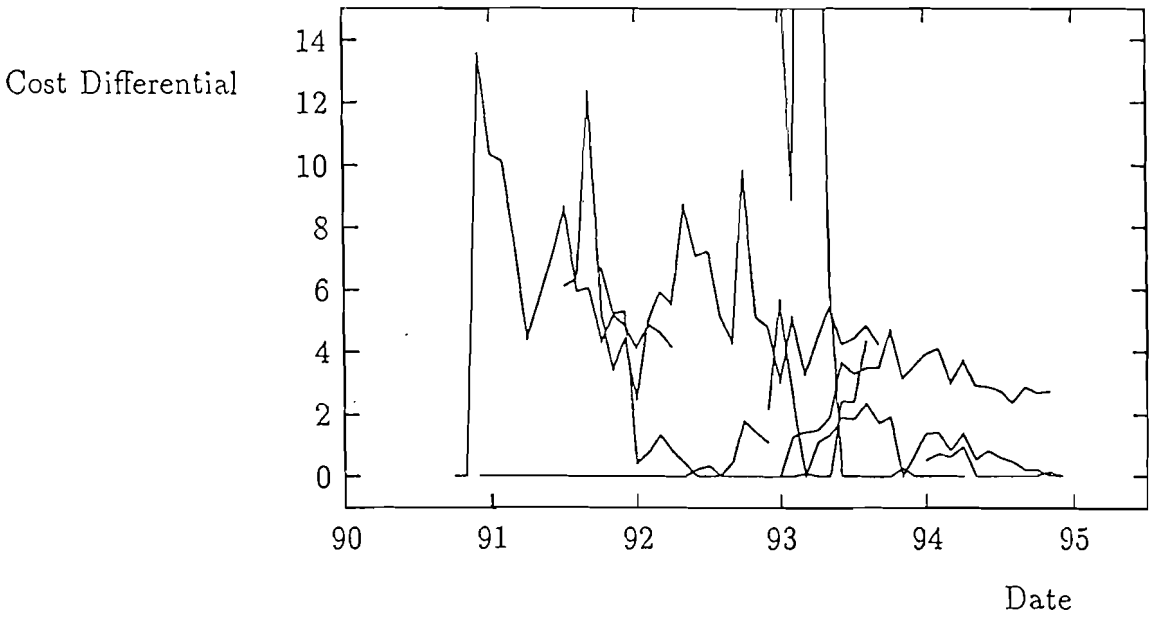

Figure 5: Defect Densities of Submicron Processes

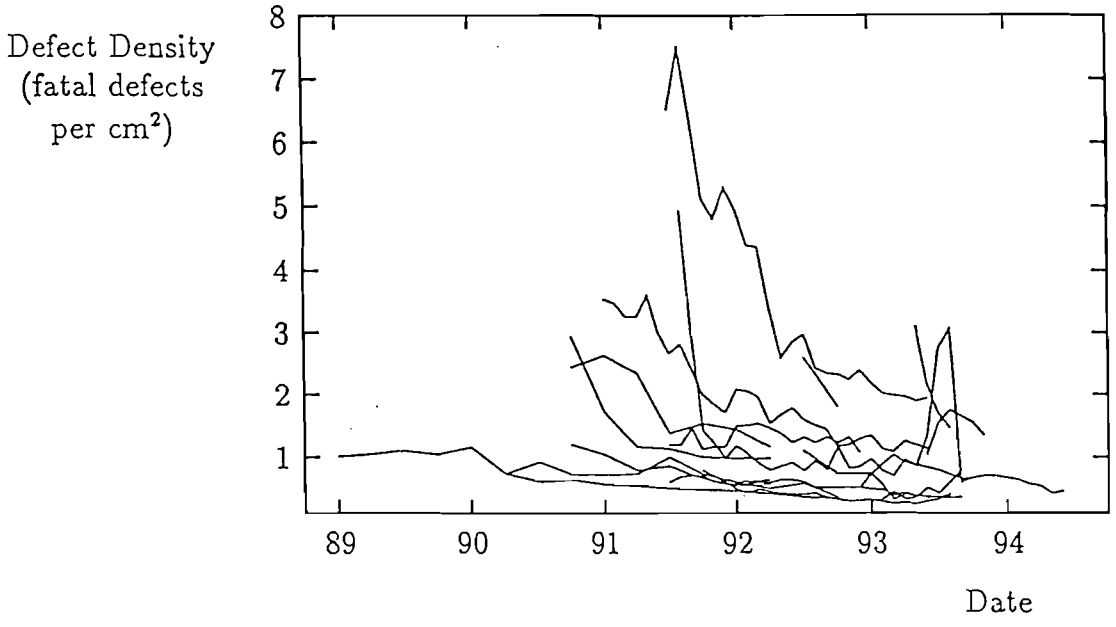

Figure 6: Defect Densities of 1.0 – 1.2 μm Processes

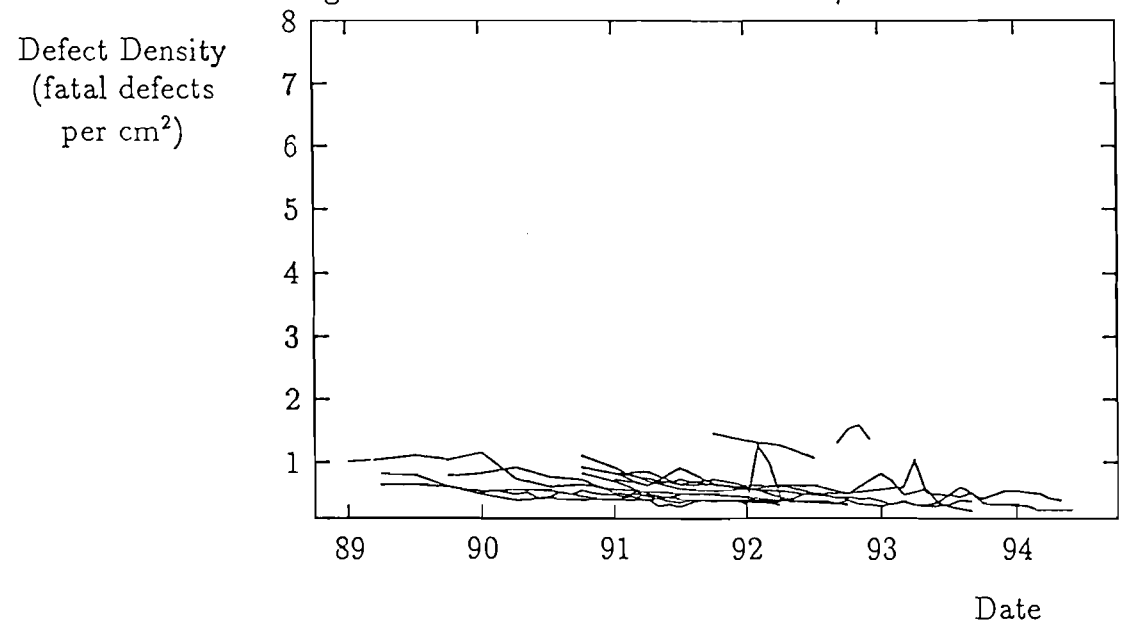

Table 1: Monthly Penalties per Unit Associated with a Late Start (Delay) and Poor Yields for a Sample of 4 MB DRAM Processes

Process 1		Process 2		Process 3		Process 4		Process 5		Process 6		Process 7		Process 8	
Delay	Yield	Delay	Yield	Delay	Yield	Delay	Yield	Delay	Yield	Delay	Yield	Delay	Yield	Delay	Yield
$92.59	$0.00	$95.94	$0.00	$107.65	$6.12	$108.71	$6.71	$111.89	$680.29	$111.93	$2.18	$111.94	$0.06	$112.16	$0.51
86.97	0.00	90.31	0.00	100.71	6.35	101.76	5.21	104.60	1465.63	104.64	5.59	104.65	1.31	104.89	0.74
81.34	13.56	84.69	0.00	93.76	12.34	94.82	5.30	97.31	478.34	97.35	2.63	97.36	1.40	97.62	0.64
75.72	10.33	79.06	0.00	86.82	5.16	87.87	0.41	90.02	94.46	90.06	0.00	90.07	1.47	90.35	0.98
70.09	10.11	73.44	0.00	79.87	3.43	80.93	0.78	82.74	46.14	82.77	1.10	82.78	1.92	83.08	0.00
64.47	7.52	67.82	0.00	72.93	4.42	73.98	1.35	75.45	18.60	75.48	1.32	75.49	3.70	75.81	0.00
58.85	4.46	62.19	0.00	65.98	2.48	67.04	0.82	68.16	8.91	68.20	1.90	68.21	3.29	68.54	0.00
53.22	5.78	56.57	0.00	59.03	5.01	60.09	0.43	60.87	27.76	60.91	1.88	60.93	3.51	61.26	0.00
47.60	7.07	49.62	0.00	52.09	5.95	53.15	0.00	53.58	50.81	53.64	2.37	53.66	3.48	53.99	0.00
41.97	8.61	42.68	0.00	45.15	5.53	46.20	0.00	46.29	6.61	46.37	1.70	46.40	4.67	46.73	0.00
35.03	5.95	35.73	0.00	38.20	8.72	38.91	0.00	39.01	0.00	39.10	1.92	39.13	3.15	39.46	0.12
28.08	6.07	28.79	0.00	31.26	7.09	31.63	0.00	31.72	0.00	31.83	0.00	31.86	3.55	32.19	0.03
21.14	4.31	21.84	0.00	24.31	7.23	24.34	0.00	24.45	0.00	24.56	0.65	24.59	3.92		
19.82	5.18	20.52	0.00	22.65	5.15	22.67	0.00	22.80	0.00	22.91	1.38	22.94	4.08		
18.50	4.85	19.20	0.00	20.98	4.32	21.01	0.00	21.16	0.00	21.27	1.40	21.29	2.97		
17.18	4.10	17.88	0.00	19.32	9.83	19.35	0.00	19.51	0.29	19.62	0.83	19.65	3.71		
15.85	4.87	16.56	0.00	17.65	5.14	17.68	0.00	17.86	0.00	17.97	1.39	18.00	2.90		
14.53	4.61	15.24	0.00	15.99	4.83	16.02	0.09	16.22	0.00	16.33	0.52	16.36	2.87		
13.21	4.16	13.92	0.25	14.33	3.05	14.35	0.00	14.57	0.00	14.68	0.82	14.71	2.72		
		12.60	0.36	12.66	5.09	12.69	0.00	12.93	0.00	13.04	0.60	13.06	2.34		
		10.93	0.02	11.00	3.27	11.02	2.43	11.28	0.00	11.39	0.48	11.42	2.85		
		9.27	0.44	9.33	4.43	9.36	2.40			9.74	0.20	9.77	2.69		
		7.60	1.81	7.67	5.43	7.71	4.37			8.10	0.19	8.13	2.71		
		5.94	1.40	6.00	4.27					6.45	0.00				
		4.28	1.09	4.34	4.44					4.81	0.00				
				4.01	4.85										
				3.69	4.27										

Table 2: Performance Measures for New Processes

Fab	Initial Defect Density (per cm^2)	Average Quarterly Rate of Reduction in Defect Density
Submicron Processes		
A	1.290	-3.8180%
B	0.769	14.1638%
C	0.572	10.5913%
D	1.191	9.7213%
D	0.746	-0.5490%
D	2.447	14.6494%
E	0.700	8.0261%
E	0.377	0.3196%
F	1.010	-1.3923%
G	4.918	30.0464%
G	8.412	53.8064%
H	2.919	25.5009%
I	0.520	18.5136%
I	0.800	16.1611%
I	3.090	39.6154%
J	0.668	2.1271%
K	6.519	18.8139%
K	3.525	17.0226%
L	0.395	-25.4615%
M	2.597	30.2656%
M	1.107	3.9566%
N	0.614	2.0910%
O	6.089	59.4945%
O	0.164	11.8935%
1.0 – 1.2 μm Processes		
C	1.116	19.3749%
D	0.559	-6.6940%
D	0.924	-3.8160%
D	0.739	3.6401%
H	0.645	5.1361%
M	0.823	2.9346%
M	1.470	9.5943%
M	0.828	8.2739%
N	0.504	3.2236%
P	2.076	2.5960%
Q	1.306	11.6606%
R	1.428	18.2075%