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Research Article

Stability Improvement of an Efficient Graphene Nanoribbon Field-Effect Transistor-Based SRAM Design

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The development of the nanoelectronics semiconductor devices leads to the shrinking of transistors channel into nanometer dimension. However, there are obstacles that appear with downscaling of the transistors primarily various short-channel effects. Graphene nanoribbon field-effect transistor (GNRFET) is an emerging technology that can potentially solve the issues of the conventional planar MOSFET imposed by quantum mechanical (QM) effects. GNRFET can also be used as static random-access memory (SRAM) circuit design due to its remarkable electronic properties. For high-speed operation, SRAM cells are more reliable and faster to be effectively utilized as memory cache. The transistor sizing constraint affects conventional 6T SRAM in a trade-off in access and write stability. This paper investigates on the stability performance in retention, access, and write mode of 15 nm GNRFET-based 6T and 8T SRAM cells with that of 16 nm FinFET and 16 nm MOSFET. The design and simulation of the SRAM model are simulated in synopsys HSPICE. GNRFET, FinFET, and MOSFET 8T SRAM cells give better performance in static noise margin (SNM) and power consumption than 6T SRAM cells. The simulation results reveal that the GNRFET, FinFET, and MOSFET-based 8T SRAM cells improved access static noise margin considerably by 58.1%, 28%, and 20.5%, respectively, as well as average power consumption significantly by 97.27%, 99.05%, and 83.3%, respectively, to the GNRFET, FinFET, and MOSFET-based 6T SRAM design.

1. Introduction

The impact of the future nanotechnology in electronic devices results in the scaling of the transistor size and the miniaturization of the transistor through scaling process. Presently, we have the 10th generation Intel Core i7 processor that contains over 600 million transistors in an integrated circuit. Hence, the performance of a nanotransistor is affected by scaling and miniaturization. The downscaling of the transistor size has become a challenge to sustain due to short-channel effects, namely, subthreshold leakage current. Therefore, innovations and novel nanostructures must be introduced in the More than Moore's Law regime for ultra high performances. These new approaches are new structure, design, and the introduction of an alternative material [1]. The larger number of transistors of SRAM cell occupies the larger surface area of system on chip (SOC). The number of the SRAM cells can be larger in the memory chip due to the decrease of the gate length of the FET. However, the conventional planar MOSFET faces the short-channel effect and threshold voltage problem when the technology scaled beyond 32 nm. 16 nm FinFET-based 6T SRAM cells can potentially be an alternative to conventional planar MOSFET. In addition to that, carbon-based materials, namely, carbon nanotube transistor field-effect transistor (CNTFET) and graphene nanoribbon field-effect transistor (GNRFET), can improve the performance of the devices in terms of not only the stability but also the lower power consumption. Their speed performance also rivals the properties of FinFET [2]. GaAs and high k-dielectric and strained silicon can augment the device performance that gives a remarkable gate control in addition to their abilities to reduce the short-channel

effects. In this work, the GNRFET structure is proposed to overcome the limitation of the conventional planar MOSFET and their performance as SRAM cells are explored [3].

2. Device Parameter of GNRFETs

Carbon-based FETs have risen over the years in view of their exceptional characteristics and compatibility to contemporary silicon-based fabrication processes [1]. Popular devices sought by researchers are CNTFETs and GNRFETs. The GNRFET does not face any alignment and transfer-related issues experienced by CNT-based devices [4], as it can be developed over an in situ process that is silicon compatible [5]. On the other hand, graphene-based circuits confront different sets of difficulties that include degraded mobility, unstable conductivity, and small band gap due to process variation [6]. Nevertheless, the small band gap issues can be overcome by band-gap engineering.

Figure 1 depicts the structure of the MOSFET-like GNRFET that has parallel ribbons that are connected from source, gate, and drain to increase the drive strength. The gate can be made to control the channel. The length of the channel is denoted as L_{ch}, the ribbon width as $W_{CH,}$ and space between the ribbons as $2W_{SP}$ [7–9]. The device parameter of GNRFET used in this work are shown in Table 1. The SPICE models used are from Predictive Technology Models (PTMs) for MOSFET and FinFET and Urbana-Champaign Model for GNRFET [10].

GNRFETs can overcome the short-channel effects that are prevalent in sub-100 nm Si MOSFET. A GNRFET provides reduced energy-delay-product (EDP) and power-delay-product (PDP) one order of magnitude that is lower than that of a MOSFET. Although the GNRFET is energy efficient, the circuit performance of the device is limited by the interconnect capacitances.

2.1. SRAM Cells. The structure of the elementary 6T-SRAM cell is illustrated in Figure 2. The access transistors are M5 and M6, which couple the output nodes of the two cross-coupled inverters with the bit line (BL) and the bit line bar (BL′). WL functions as the write line. Whenever the write line is high, the data present on BL and BL′ are sent to the nodes Q and Q', respectively. The pull-up transistors are M4 and M2. On the other hand, the transistors M3 and M1 work as the pull-down transistors [10]. The stability analysis of 6T-SRAM cells has been carried out in the work. In order to conduct the stability analysis, the sizing of transistors must be carefully selected [11, 12]. In 8T SRAM cells, two n-type FETs are added to the conventional 6T SRAM cells, which are controlled by the read word line (RWL) to isolate the access and write mode path for better access stability.

2.2. Transistor Sizing for 6T and 8T SRAM Cells. Table 2 tabulates the sizing of a structure used for various SRAM topologies, and Table 3 depicts device parameters of FinFETs. The aspect ratios used in 16 nm MOSFET are as follows: PMOS transistors, namely, M2 and M4, are used with W-48 nm and L-16 nm by considering W/L ratio of 3, whereas NMOS transistors such as M1, M3, M5, M6, M7,

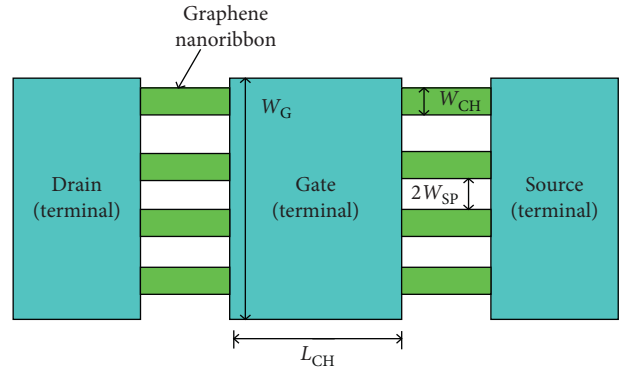

Figure 1: The structure of a MOSFET-like GNRFET.

Table 1: Device parameters of graphene nanoribbon field-effect transistor.

Device parameters	Values
Length of the channel	15 nm
Top gate dielectric material thickness	0.95 nm
Space between adjacent GNRs	2 nm
No. of GNRs	6
Substrate oxide thickness	20 nm
No. of dimer lines in GNR lattice	12

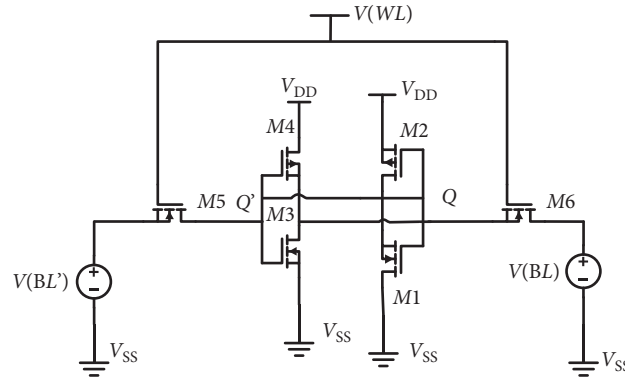

Figure 2: A schematic diagram of a 6T SRAM cell.

Table 2: Sizing of a structure used for various SRAM topologies.

Transistor	6T SRAM		8T SRAM	
	MOSFET W/L ratio	GNRFET W/L ratio	MOSFET W/L ratio	GNRFET W/L ratio
$M1$	16/16	0.86/15	16/16	0.86/15
$M2$	48/16	0.86/15	48/16	0.86/15
$M3$	16/16	0.86/15	16/16	0.86/15
$M4$	48/16	0.86/15	48/16	0.86/15
$M5$	16/16	0.86/15	16/16	0.86/15
$M6$	16/16	0.86/15	16/16	0.86/15
$M7$	—	—	16/16	0.86/15
$M8$	—	—	16/16	0.86/15

Table 3: Device parameters of fin field-effect transistors.

Device parameters	Values (nm)
Gate length, L_g	16
Top-fin width, W_{top}	8
Bottom-fin width, W_{bottom}	8
Fin height, H_f	32
Effective oxide thickness, EOT	1

and M8 are used with W-16 nm and L-16 nm. 8T SRAM cells are examined to enhance the efficiency of the SRAM cell, which contains a conventional 6T SRAM cell [13, 14]. NMOS has electrons as majority charge carriers, whereas PMOS has holes as majority charge carriers. Electrons have mobility ~2.7 times higher than the holes and thereby can be approximated by sizing the PMOS ~3 times to the NMOS sizing.

3. Device Performance of GNRFETs

This section focuses on electrical device performance of GNRFETs. Theoretical work has shown that GNRs have band gaps inversely proportional to their widths. Conductivity is also determined by the edge state. GNRs with predominantly armchair edges are observed to be semiconducting, while GNRs with predominantly zigzag edges demonstrate metallic properties. The width of a GNR (denoted W_{CH}) is commonly defined via the number of dimer lines N, where $W_{CH} = \sqrt{3}d_{cc}(N+1)/2$, in which d_{cc} is the carbon-carbon bond distance at 0.142 nm. As such, the width for both PGNR and NGNR models is 0.86 nm and length is 15 nm [15]. To isolate the cell core from the output, two extra n-type transistors with a control signal and additional bit line are incorporated. The write mode is performed through the access transistors. The access mode is conducted, and the data stored appears on the access bit. The cross-coupled inverters in the design is open circuited for the write mode as feedback loop is only needed in the access mode to store the data [16].

The device performance of GNRFETs can be evaluated by their I_d-V_d characteristics shown in Figure 3 for multiple gate voltages from 0 V to 1 V. Figure 4 illustrates the I_d-V_g transfer characteristic of symmetrical n-type and p-type GNRFET for $|V_d| = 0.1$ V and $|V_d| = 1$ V.

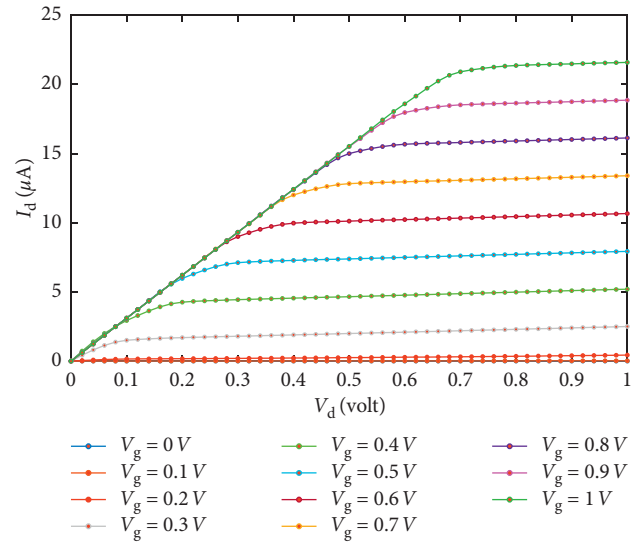

Figure 3: I_d–V_d characteristics of n-type GNRFETs for multiple gate voltages in 0.1 V decrement from $V_g = 1$ V at the top.

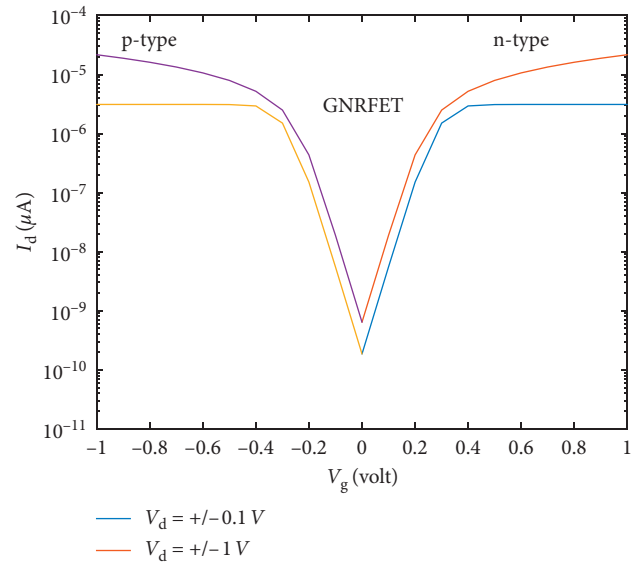

Figure 4: I_d-V_g transfer characteristics of symmetrical n-type and p-type GNRFETs for $|V_d| = 0.1$ V and $|V_d| = 1$ V.

4. SNM Extraction

To obtain the SNM graphically, a butterfly curve is plotted by depicting voltage transfer characteristics through the access mode and write mode schematic shown in Figures 5 and 6, respectively. The feedback of the cross-coupled inverter is separated according to the modes of operation. The voltage transfer characteristic (VTC) of SRAM cells is performed at node Q and Q'.

4.1. Stability Analysis of SRAM Cells. Figures 7, 8, and 9 show the butterfly curve of 6T SRAM cells in the retention mode, access mode, and write mode, respectively. SNM can be obtained from the butterfly curve plot. In previous work, the simulation of the SRAM model was carried out on 22 nm FinFET technology. The FinFET-based 8T SRAM cell gives better performance in static noise margin (SNM) and power consumption than 6T SRAM cells [17]. In this paper, MOSFET (16 nm), FinFET (16 nm), and GNRFET (15 nm) based SRAM designs are analyzed in order to improve efficiency based on power, delay, and PDP. Butterfly curve is obtained by toggling the x-axis and y-axis of one of the VTC curves and then merging these two separate VTC plots together. Figures 5 and 6 depict the schematic for butterfly curve measurement of SRAM cells in the retention mode and access mode, respectively. Figure 7 shows the VTC measurement of SRAM cells in the write operation. The write mode is a process of writing logic 0 to q and logic 1 to q,

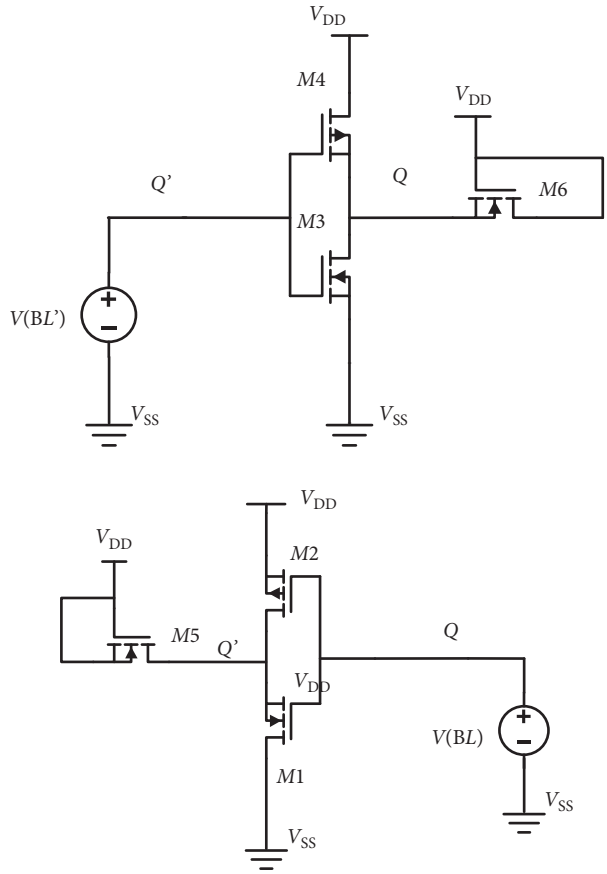

Figure 5: The schematic for butterfly curve measurement of SRAM cells in the access mode.

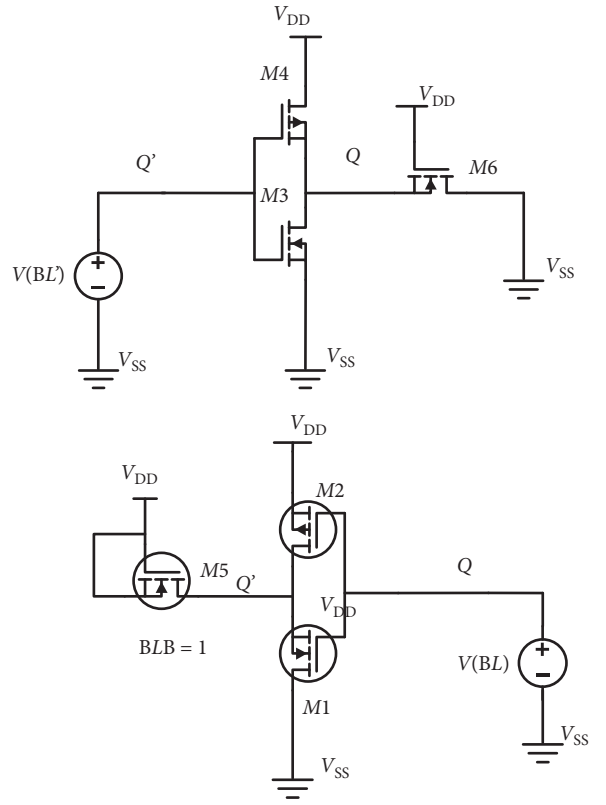

Figure 6: The schematic for butterfly curve measurement of SRAM cells in the write operation.

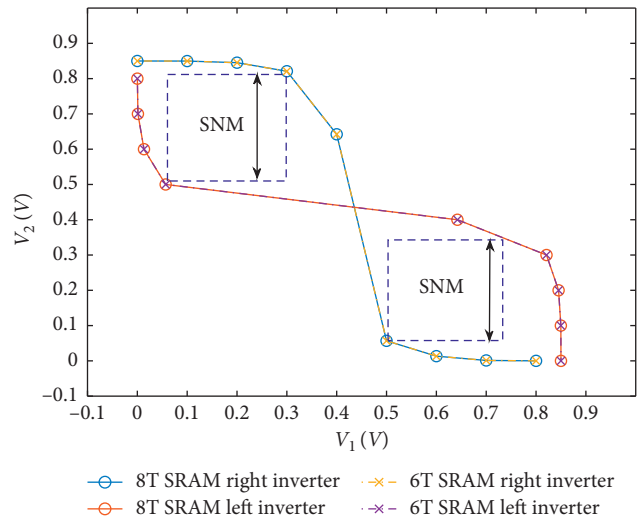

Figure 7: Butterfly curve of GNRFET-based 6T and 8T SRAM cells in the retention mode.

where BL is grounded and BLB is connected to V_{dd}. The static noise margin of 8T GNRFET SRAM cells in the retention mode and access mode is 300 mV and 340 mV, respectively. The SNM of a SRAM cell in the write mode is at 380 mV. Performance metrics such as average power, delay, and power delay product among MOSFET, FinFET, and GNRFET are then evaluated. The propagation delay is the difference in time when output switches after application of input. In this manuscript, delay has been calculated with reference signal as input and acquired signal as output using COSMOSCOPE tool. On average, the GNRFET-based SRAM designs dissipated around 10× less power than their MOSFET and FinFET counterparts, which demonstrates graphene-based devices to be a safer choice to reduce power dissipation with increased scaling. The different designs provide a varied performance over access times measurement. GNRFET-based SRAM design shows the least write delay amongst the three designs, whereas FinFET-based SRAM design performs marginally better while writing onto the bit line. On the whole, both GNRFET and FinFET-based SRAM designs outperform the MOSFET-based design.

Table 4 shows the noise margin of MOSFET-, FinFET-, and GNRFET-based 6T SRAM cells and 8T SRAM cells. It is observed that there is no change on the values of the SNM for both 6T and 8T SRAM cells. In addition, the 8T SRAM cells has improved access static noise margin (ASNM) but a comparable write static noise margin (WSNM) to 6T SRAM cells. For instance, GNRFET-based 8T SRAM cells have 58% enhancement of ASNM than the 6T SRAM cells. Discharging path from reading bit line to ground is zero, which leads to stability on 8T SRAM access mode [17, 18].

Tables 5, 6, and 7 shows the summary of the comparison of the 6T SRAM and 8T SRAM cells in terms of average

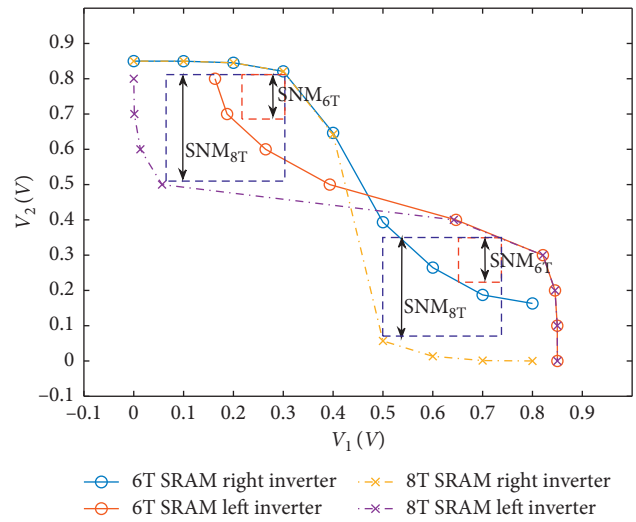

Figure 8: Butterfly curve of GNRFET-based 6T and 8T SRAM cells in the access mode.

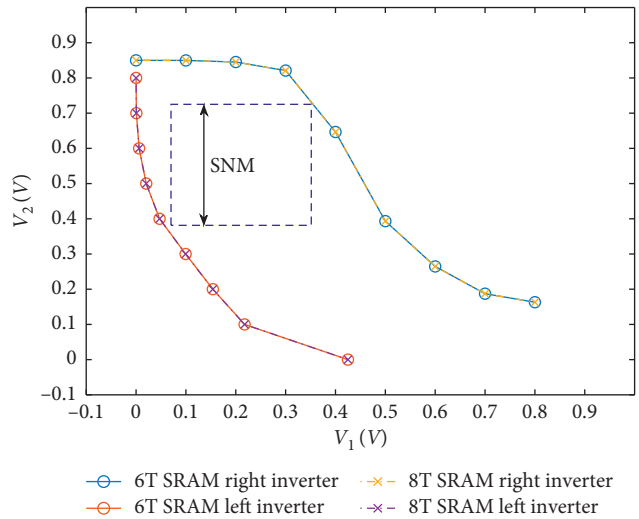

Figure 9: Butterfly curve of GNRFET-based 6T and 8T SRAM cells in the write mode.

Table 4: Analysis of noise margin of MOSFET-, FinFET-, and GNRFET-based technology.

SRAM characteristics	6T SRAM			8T SRAM		
	MOSFET	FinFET	GNRFET	MOSFET	FinFET	GNRFET
SNM (mV)	245	280	300	245	280	300
ASNM (mV)	170	200	215	205	256	340
WSNM (mV)	359	378	390	350	374	380

Table 5: Analysis of average power consumption of MOSFET-, FinFET-, and GNRFET-based technology.

SRAM characteristics	6T SRAM			8T SRAM		
	MOSFET	FinFET	GNRFET	MOSFET	FinFET	GNRFET
Retention mode (W)	3.0×10^{-7}	5.3×10^{-6}	1.8×10^{-6}	3.2×10^{-8}	2.2×10^{-8}	2.3×10^{-8}
Access mode (W)	3.0×10^{-7}	5.3×10^{-6}	1.8×10^{-6}	5.0×10^{-8}	5.0×10^{-8}	4.9×10^{-8}
Write mode (W)	4.5×10^{-7}	8.2×10^{-6}	2.1×10^{-6}	3.6×10^{-7}	3.5×10^{-7}	3.5×10^{-7}

Table 6: Analysis of delay of MOSFET-, FinFET-, and GNRFET-based technology.

SRAM characteristics	6T SRAM			8T SRAM		
	MOSFET	FinFET	GNRFET	MOSFET	FinFET	GNRFET
Retention mode (s)	1.9×10^{-13}	1.4×10^{-14}	1.3×10^{-13}	2.5×10^{-13}	1.6×10^{-13}	1.3×10^{-13}
Access mode (s)	2.5×10^{-13}	2.0×10^{-13}	1.6×10^{-13}	3.7×10^{-13}	3.6×10^{-13}	3.0×10^{-13}
Write mode (s)	1.3×10^{-13}	1.0×10^{-13}	9.3×10^{-12}	1.4×10^{-13}	1.3×10^{-13}	1.1×10^{-13}

Table 7: Analysis of power-delay-product of MOSFET-, FinFET-, and GNRFET-based technology.

SRAM characteristics	6T SRAM			8T SRAM		
	MOSFET	FinFET	GNRFET	MOSFET	FinFET	GNRFET
Retention mode (J)	5.5×10^{-18}	7.6×10^{-19}	2.2×10^{-19}	8.2×10^{-21}	3.5×10^{-21}	3.1×10^{-21}
Access mode (s)	7.5×10^{-18}	1.0×10^{-20}	2.9×10^{-19}	1.8×10^{-22}	1.8×10^{-22}	1.5×10^{-22}
Write mode (J)	5.7×10^{-18}	8.6×10^{-19}	2.0×10^{-19}	5.0×10^{-18}	4.6×10^{-20}	3.7×10^{-19}

power, delay, and power delay product for MOSFET-, FinFET-, and GNRFET-based technology.

The average power dissipation of the CMOS logic gate, driven by a periodic input voltage waveform with ideally zero rise- and fall-times, can be calculated from the energy required to charge up the output node to VDD and charge down the total output load capacitance to ground level. The propagation delay high to low (tpHL) is the delay when output switches from high to low, after input switches from low to high (tpLH). The delay is usually calculated at the point of input-output switching. Power and delay has been calculated using synopsys HSPICE and COSMOSCOPE, respectively, by analyzing transient analysis [19]. Similarly, SNM is calculated using COSMOSCOPE in DC analysis. The circuit inductance possibly causes spikes that are possible to be compensated by incorporating an on-chip decoupling capacitor at the output in parallel. The propagation delay is computed between 50% of the input rising and the 50% of the output rising. In addition to the average power consumption, the metric performance of designs in terms of power, delay, and PDP is obtained [20]. PDP parameter is the figure of merit and given by

$$\text{PDP} = P_{\text{avg}} \times t_p. \quad (1)$$

Our proposed 15 nm GNRFET-based 6T and 8T SRAM cells have less power consumption and enhanced stability. Our findings revealed that the static noise margin during the access mode is greatly improved in GNRFET-based 8T SRAM cells. In this work, all the designs were carried out for short gate length of 16 nm for MOSFET, 16 nm for FinFET, and 15 nm for GNRFET. Besides, the power consumption of the previous works has not been reported [19, 20]. As per the performance analysis in the retention mode, both 6T and 8T SRAM cells do not have significant discrepancy. Nevertheless, 8T SRAM cells generally improve the access stability with the support of access transistors that separate the access and write operation. Therefore, when it comes to the access mode, 8T SRAM cells perform considerably well. In the write mode, 6T SRAM cells perform well when compared to 8T SRAM cells. This is due to the switching activity of the transistors. However, in this work, the power consumption during access mode is presented and shows the least power is consumed with only 4.9×10^{-8} W to obtain the maximum access stability of 340 mV for GNRFET-based 8T SRAM cells.

5. Conclusion

GNRFET is another alternative solution to solve the obstacles and challenges that occur in the conventional planar MOSFET in the sub-100 nm technology node. Drain and transfer characteristics of 15 nm GNRFET have been explored. We have performed simulation and analysis of 6T SRAM cells and 8T SRAM cells in different modes of operation. SNM acquired from the maximum square of the VTC of the inverter. There are two types of the SNM that affect the stability of the SRAM cell, namely, the write static noise margin (WSNM) and access static noise margin (ASNM). The SNM of the 6T SRAM access mode is less than the static noise margin of the 6T SRAM during the retention mode. The 8T SRAM cell shows better ASNM than the conventional 6T SRAM cell. Due to the isolation of the access path from the storage node, GNRFET-based 8T SRAM configuration outperformed 6T SRAM cells by 58.1% in ASNM. The PDP of the access mode of 8T SRAM cells is significantly reduced when compared with 6T SRAM cells. This reduction in power consumption is due to the application of a single bit line for reading into the proposed GNRFET-based 8T SRAM model. It can be concluded that the GNRFET-based 8T SRAM cells show significant improvement in their performance with better stability and low-power consumption in the access mode.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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