An ‘Active’ Passive-Filter Topology for Low Power DC/AC Inverters

By

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Abstract

This thesis presents a new output passive filter for voltage source inverter applications which is based on a shunt connected single tuned filter topology. The proposed circuit has the advantage of tracing harmonic components wherever its location in the frequency spectrum. The change in the harmonic location might be as a result of a change in the inverter operating frequency. Also, the proposed filter achieves harmonic reduction close to the traditional single tuned passive filter. In order to show the superiority of the proposed model, a comparison is introduced with other self tuning harmonic filters showing merits and drawbacks of each technique. The proposed circuit (when integrated in square wave inverter) has also shown a tremendous reduction in the switching losses in comparison with high frequency Pulse Width Modulation inverter. Mathematical analyses showing the design of the proposed filter together with extensive simulation results to verify the design are also introduced. The practical implementation of the system is presented and the results show excellent agreement with the theory and simulation. In order to appreciate the proposed filter a new method for classifying passive power filters is introduced. The review includes a comparison of these configurations showing their merit and drawbacks.

To my Parents, Fayez, Khadijeh

& Sweet sisters, Mai, Mira, Mayar

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Table of Contents

	Page No.
Abstract	**IV**
Acknowledgements	**II**
List of Tables	**VIII**
List of Figures	**IX**
List of Symbols	**XIII**
List of Abbreviations	**XIV**
Chapter 1	**1**
Introduction	**1**
1.1 Preface	1
1.2 Description of Power Harmonics Phenomena	3
1.3 Sources and Effects of Power Harmonics	4
1.4 Thesis Aim and Outline	6
Chapter 2	**8**
Classification of Power Electronic Filters	**8**
2.1 Introduction	8
2.2 Classification of Passive Power Filters	8
2.2.1 Classification According Based on Connection and Compensated Harmonics	10
2.2.1.1 Series-Connected AC Reactor	10
2.2.1.2 Shunt-Connected Passive Filter	10
2.2.2 Classification According to Parameters in the Circuit	17
2.2.2.1 Fixed Passive Filter	18
2.2.2.2 Variable Passive Filter	18
2.2.3 Classification According to Point of Common Coupling	20
2.3 Overview of Active Power Filters	21
2.3.1 Configurations of Active Power Filters	22
2.3.1.1 Shunt Active Power Filters	23
2.3.1.2 Series Active Power Filters	25
2.3.1.3 Hybrid Active Power Filters	26
2.3.1.3.1 Series / Shunt Active Power Filters	26
2.3.1.3.2 Series Active / Shunt Passive Power Filters	27
2.3.1.3.3 Shunt Active / Shunt Passive Power Filters	27
2.4 General Comparison of Power Electronic Filters	28
2.5 Summary	31

Chapter 3 **32**

Investigation of Power Electronic Voltage Source H-bridge Inverters **32**

3.1 Introduction 32

3.2 Voltage Source H-bridge Inverters 32

3.2.1 Traditional H-bridge VSI 34

3.2.2 Common Modulation Methods for Traditional H-bridge VSI 37

3.2.2.1 Low Frequency Square Wave Modulation 37

3.2.2.2 High Frequency Sinusoidal PWM Modulation 37

3.2.3 Multilevel Cascaded H-bridge VSI 42

3.2.4 Common Modulation Methods for Multilevel Cascaded H-bridge VSI 45

3.2.4.1 Low Frequency Staircase Wave Modulation 46

3.2.4.2 High Frequency Multicarrier SPWM Modulation 47

3.2.4.3 Hybrid Frequency Modulation – HV-LV Stages 51

3.3 General Comparison of Voltage Source H-bridge Inverters 52

3.4 Summary 54

Chapter 4 **55**

The Switched Capacitor Circuit applied to the proposed Output Filter for Power Inverter **55**

4.1 Introduction 55

4.2 Switched Capacitor Circuit 55

4.2.1 Single Capacitor, Double Switch (SCDS) Circuit 56

4.2.1.1 Switching Function Analysis of SCDS Circuit 59

4.2.2 Double Capacitor, Double Switch (DCDS) Circuit 67

4.3 Other Topologies of Switched Capacitor Circuit 74

4.3.1 Single Capacitor, Single Switch (SCSS) Circuit 74

4.3.2 Triple Switch SCC configurations 75

4.4 Selection Criteria of SCC for the Proposed Output Filter 77

4.5 Summary 79

Chapter 5 **81**

Simulation Modelling and Implementation of the Proposed Single Capacitor Double Switch Filter **81**

5.1 Introduction 81

5.2 Computer Simulation Modelling of SCDS Tuned Output Passive Filter 82

5.2.1 Orcad PSPICE Software 82

5.2.2 Parameters and Components of the Simulated Model 84

5.2.3 Single Tuned Output Passive Filter for Traditional VSI 84

5.2.4 Single Capacitor Double Switch Tuned Output Passive Filter 86
5.2.4.1 Switching Strategy 87
5.2.4.2 Calculation of the Effective Capacitance 87
5.2.4.3 Calculation of the Duty Cycle 88
5.2.4.4 Determining the Value of the Fixed Capacitor 88
5.2.5 Simulation Results of the SCDS Filter Circuit 89
5.2.5.1 Tuned Effective Capacitance Traceability Performance 89
5.2.5.2 Harmonic Reduction using Traditional and Proposed Methods 91
5.2.5.3 Effect of SCDS Filter on Current Harmonics 93
5.2.5.4 Effect of SCDS Filter on Switching Losses 94
5.3 Implementation of the Single Capacitor Double Switch Circuit 97
5.4 Summary 109
Chapter 6 **111**
Conclusions and Future Work **111**
6.1Conclusions 111
6.2 Future Work 115
References **116**
Appendices
Appendix A: C-Language Program for Switching Pattern Generation **123**
A.1 Arduino Pins Initialisation 124
A.2 Setting Up the Switching Pattern Generation 125
A.3 Setting Up the Push Button Control for the Pulses Duty Cycle 127
Appendix B: List of Publications **130**

List of Tables

Page No.

Table 2-1 Comparison of Common Power Electronic Filters 29

Table 3-1 H-bridge VSI Switching States 36

Table 3-2 Multilevel Cascaded H-bridge VSI Switching States (5-Level CHB) 46

Table 3-3 Comparison of Voltage Source H-bridge Inverters 53

Table 4-1 Comparison between Switched Capacitor Circuits for the Selection Criteria 78

Table 5-1 Proposed Filter Parameters 84

List of Figures

Page No.

Figure 2.1 Classification of passive filter configuration based on connection type 9
Figure 2.2 Low Pass L-filter 11
Figure 2.3 Band Pass Tuned filter, Single and Double tuned Filter configuration 12
Figure 2.4 High Pass filter, 1st order and 2nd order HP filters 13
Figure 2.5 High Pass filter, 3rd order and C-Type HP filter 16
Figure 2.6 Composite passive filter 17
Figure 2.7 Classification of passive filter configuration based on element's parameters 18
Figure 2.8 Variable passive filter configurations 19
Figure 2.9 Passive Filter classification according to place of insertion 21
Figure 2.10 Classification of active power filters configurations 22
Figure 2.11 Generalized block diagram for Active Power Filters 22
Figure 2.12 Shunt active power filter configuration 24
Figure 2.13 Power circuit configurations of shunt APF VSI 24
Figure 2.14 Series active power filter configuration 26
Figure 2.15 Series / Shunt active power filter configuration 27
Figure 2.16 Series active / Shunt passive power filter configuration 28
Figure 2.17 Shunt active / Shunt passive power filter configuration 28
Figure 3.1 Classification of H-bridge voltage source inverters 33
Figure 3.2 Single Phase H-bridge voltage source inverters 34
Figure 3.3 H-bridge inverter switching states 35
Figure 3.4 Bipolar SPWM for H-bridge voltage source inverter 39
Figure 3.5 Unipolar SPWM for H-bridge voltage source inverter 41
Figure 3.6 Voltage Source Cascaded H-bridge Multilevel Inverter Topology 44
Figure 3.7 Output voltage of an 11-level multilevel cascaded H-bridgeVSI 44
Figure 3.8 Phase-shifted SPWM scheme for seven level CHB inverter 48
Figure 3.9 Level-shifted SPWM scheme for seven level CHB inverter 50
Figure 3.10 CHB inverter modulated by hybrid switching frequency scheme 52
Figure 4.1 Single Capacitor Double Switch Circuit 56
Figure 4.2 Single Capacitor Double Switch Circuit (SCDS) with inductor current limiter 57
Figure 4.3 The Switching Function 59
Figure 4.4 Relation between duty cycle, and effective capacitance of SCDS circuit 67
Figure 4.5 Double Capacitor Double Switch Circuit 68
Figure 4.6 Double Capacitor Double Switch Circuit 68
Figure 4.7 Relation between duty cycle, and effective capacitance of DCDS (S1) 72

Figure 4.8 Relation between duty cycle, and effective capacitance of DCDS (S2) 73
Figure 4.9 Single Capacitor Single Switch Circuit with inductor current limiter 75
Figure 4.10 Triple Switched Capacitor Circuits configurations, a: SCDS, and b: DCDS 76
Figure 5.1 Circuit Modeling using Orcad Pspice Software 83
Figure 5.2 A schematic overview of a: the Traditional and Proposed Single Tuned Filter 85
Figure 5.3 Proposed Single Tuned Filter utilizing Single Capacitor Double Switch 86
Figure 5.4 Tuned Effective Capacitance (Theoretical) 90
Figure 5.5 Tuned Effective Capacitance (Simulation) 90
Figure 5.6 Percentage of reduced 3rd harmonic (Simulation) 91
Figure 5.7 Percentage of reduced 5th harmonic (Simulation) 91
Figure 5.8 Percentage of reduced 7th harmonic (Simulation) 92
Figure 5.9 Percentage of reduced 9th harmonic (Simulation) 92
Figure 5.10 Total Harmonic Distortion for TCR and SCDS 94
Figure 5.11 Switching loss and Conduction loss in term of Switching frequency 95
Figure 5.12 Two voltage source inverter systems 95
Figure 5.13 Switching power losses in two power electronic H-bridge inverter systems 96
Figure 5.14 The proposed system showing traditional and new single tuned filter 98
Figure 5.15 Flowchart of the programmable generation of the switches' duty cycle 99
Figure 5.16 The experimental setup showing the proposed system 100
Figure 5.17 Voltage and Current wavefrom at K_o=0.1, (C=5 µF) 101
Figure 5.18 Voltage and Current wavefrom at K_o=0.2, (C=5 µF) 101
Figure 5.19 Voltage and Current wavefrom at K_o=0.3, (C=5 µF) 101
Figure 5.20 Voltage and Current wavefrom at K_o=0.4, (C=5 µF) 102
Figure 5.21 Voltage and Current wavefrom at K_o=0.5, (C=5 µF) 102
Figure 5.22 Voltage and Current wavefrom at K_o=0.6, (C=5 µF) 102
Figure 5.23 Voltage and Current wavefrom at K_o=0.7, (C=5 µF) 103
Figure 5.24 Voltage and Current wavefrom at K_o=0.8, (C=5 µF) 103
Figure 5.25 Voltage and Current wavefrom at K_o=0.9, (C=5 µF) 103
Figure 5.26 Voltage and Current wavefrom at K_o=0.1, (C=10 µF) 104
Figure 5.27 Voltage and Current wavefrom at K_o=0.2, (C=10 µF) 104
Figure 5.28 Voltage and Current wavefrom at K_o=0.3, (C=10 µF) 105
Figure 5.29 Voltage and Current wavefrom at K_o=0.4, (C=10 µF) 105
Figure 5.30 Voltage and Current wavefrom at K_o=0.5, (C=10 µF) 105
Figure 5.31 Voltage and Current wavefrom at K_o=0.6, (C=10 µF) 106
Figure 5.32 Voltage and Current wavefrom at K_o=0.7, (C=10 µF) 106
Figure 5.33 Voltage and Current wavefrom at K_o=0.8, (C=10 µF) 106

Figure 5.34 Voltage and Current wavefrom at K_o=0.9, (C=10 µF) 107
Figure 5.35 Anti-parallel switching pulses at K_o=0.5 107
Figure 5.36 Experimental results of SCDS (Fixed = 5 µF) 108
Figure 5.37 Experimental results of SCDS (Fixed = 10 µF) 108
Figure 5.38 Experimental results showing the percentage of reduced 5th harmonic 109

List of Symbols

θ, φ	Phase Angle
Ø	High Frequency Component of Switching Function
ω	Angular Frequency
ω_s	Switching Angular Frequency
γ	C_2/C_1
A_o, A_n, B_n	Fourier Coefficients
b	Number of DC Sources
C	Capacitance
C_{eff}	Effective Capacitance
$C_{eff\text{-}max}$	Maximum-Effective Capacitance
F(t)	Switching Function
f_r	Tuning or Resonance Frequency
f_s	Switching Frequency
I	Instantaneous Phase Current
$\hat{I}$	Peak Value of Current
i_1	Fundamental Component of Current
I_m	Maximum Current
i_t	Total Load Current
K_o	Duty Cycle
$K_{o\text{-}min}$	Minimum-Duty Cycle
L	Inductance
L_F	Tuned Filter Inductance
m	Voltage Level number
m_f	Frequency Modulation Index
n	Harmonic Number

Q	Quality Factor
R, r	Resistance
Rd	Damping Resistance
S	Switch
T	Time Period
t	Time
t_{off}	OFF Time
t_{on}	ON Time
$\hat{V}_{XY,}\ \hat{V}_{AB}$	Peak Value of Voltage
V_a	Instantaneous Voltage Level
V_{ab}	Output Voltage
V_{abn}	RMS voltage of nth order Harmonic
V_{an}	Voltage terminal across an
V_{bn}	Voltage terminal across bn
V_c	Capacitor Voltage
V_{cr}	Carrier Signal
V_{dc}	DC Voltage
V_g	Gate signal
V_L	Inductor Voltage
V_m	Modulating Signal
V_R	Resistor Voltage
V_s	Supply Voltage
X_c	Capacitive Reactance
X_{ceff}	Effective capacitive Reactance
X_L	Inductive Reactance

List of Abbreviations

1HP	First-Order High Pass Filter
2HP	Second-Order High Pass Filter
3HP	Third-Order High Pass Filter
APF	Active Power Filter
ASD	Adjustable Speed Drive
BJT	Bipolar Junction Transistor
CHB	Cascaded H-bridge
DCDS	Double Capacitor Double Switch
DSP	Digital Signal Processor
DT	Double Tuned Filter
FACTS	Flexible AC Transmission System
GTO	Gate Turn-off Thyristor
H	H-bridge Cell
HAPF	Hybrid Active Power Filter
HV-LV	High Voltage-Low Voltage Stage
IGBT	Insulated Gate Bipolar Transistor
LS-SPWM	Level Shifted-Sinusoidal Pulse Width Modulation
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PC	Personal Computer
PCC	Point of Common Coupling
PIC	Peripheral Interface Controller
PPF	Passive Power Filter
PS-SPWM	Phase Shifted-Sinusoidal Pulse Width Modulation
PWM	Pulse Width Modulation
RES	Renewable Energy Source

RMS	Root Mean Square
SCC	Switched Capacitor Circuit
SCSS	Single Capacitor Single Switch
SPICE	Simulation Program with Integrated Circuit Emphasis
SPWM	Sinusoidal Pulse Width Modulation
ST	Single Tuned Filter
T	Thyristor
TCR	Thyristor Controlled Reactor
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supply
VSI	Voltage Source Inverter
VS-MLI	Voltage Source-Multilevel Inverter

Chapter 1
Introduction

1.1 Preface

In more than a decade, the field of electric power quality has grown tremendously. This is due to a considerable increase in the occurrence of switching power electronic circuits in power systems. This fast growth in power electronic technology is associated with the use of various power semiconductors switching devices such as thyristors, GTOs as well as transistors (BJT, MOSFET, IGBT, etc.). This growth came with a price; such as current and voltage harmonics. Small distributed loads, such as computers and television (TV) sets with switched mode power supplies at their inputs are considered to be sources of harmonics in power distribution systems. In addition, switched power electronic converters used to drive ac motors, such as adjustable speed drives, are considered to be source of harmonics to the load. In general, harmonics can be injected towards the ac source or to a sensitive load (i.e. motor). These harmonics cause problems due to their harmful effects of increasing power losses in the system, resulting in oversized power devices due to the requirement of large heat sinks. Harmonics also contribute to transformer saturation, electromagnetic interference, incorrect operation of voltage sensitive devices, and shorter life of organic insulation. All the above mentioned harmful effects have led to an incremental concern about harmonic elimination or to reduce the effect of harmonic pollution [1-4].

Inconsequence, the idea of harmonic filtration methods started to emerge and critically studied in the research environment. A large number of filter topologies and filtering techniques are proposed in literature including passive, active and hybrid

filters. The first investigated type was the passive filter. The basic principle behind passive filtering techniques is to provide a low impedance path to ground for undesired harmonics [1]. Passive filter circuits, such as shunt LC passive filters, are used to draw harmonic currents to ground. Other series configurations provide high attenuation for current harmonics, hence decreasing their magnitudes. These filters are inserted in Shunt or Series at the source of harmonics. Passive filters can be described as tuned and high pass which are used to attenuate specific harmonics and to eliminate high-order harmonics, respectively [5]. Such filters are relatively easy to design, cheap and reliable. However, it implies increasing the number of components in order to eliminate several harmonics at a given site. Active filters were introduced after passive filters. They operate by injecting harmonic current into the line system with the same magnitudes as the harmonic generated by the nonlinear load, but at opposite phases. These filters generate the opposite phase harmonics by a switching power electronic circuits such as DC/AC inverters. They are preferred over the passive filters because of their better filtering characteristics and their capability of improving the system stability by avoiding possible resonance between the filter components and the mains impedance [6-12]. However, these filters suffer from complex control and high switching losses due to the presence of active power elements. Combining the merits of both passive and active filters, hybrid filter topologies have been introduced during the last decade. The main aim of developing this type of filters is to achieve the desired filtering performance with a significant reduction of kVA effort required by the power active filter [5]. They are cost-effective solutions to suppress harmonics compared to active filters [5].

Many researchers approach the problem from the point of view of diverting or eliminating most of the undesired harmonics from the system source. This is achieved

by designing and/or combining different filtering techniques (i.e. Passive, Active or Hybrid) in order to get the lowest undesired harmonic output. Most of the available filter topologies are used as an input filter (protecting system source) or as an output filter (protecting a sensitive load) for a power electronic converter. Such output filters must be flexible in order to reduce harmonics under different operating frequencies of the power electronic converter. In other words, these filters should be able to eliminate or reduce harmonics wherever its location in the frequency spectrum. In this case, other approaches are required to be investigated in this field of harmonic filtering and this is the main aim of the thesis.

1.2 Description of Power Harmonics Phenomena

Power systems apparatuses are designed to supply an alternating voltage and current which are purely sinusoidal. From terminological point of view, the purely sine waveform which the system is designed and is expected to operate is known as fundamental wave. The corresponding frequency is called fundamental frequency [13]. In some part of the world like United Kingdom fundamental frequency is 50 Hz and other existing value is 60 Hz [13]. In this work, fundamental frequency of 50 Hz is adopted.

Utilities endeavour to provide pure sinusoid supply to the consumers. In ideal situation, the supplied voltage and the current flowing to the end user load have waveforms of the same shape. Hypothetically, this situation is possible if the consumer is using a linear load. In practice, the current flowing through the system is a non linear function of the voltage and shows periodic distortions superimposed onto the fundamental sinusoidal current waveform [14].

These distortions can be decomposed into integer harmonics (n times 50/60), and other harmonics divided into inter harmonics and sub harmonics [14, 15]. Inter harmonics is composed of harmonics having frequencies which are greater than the fundamental frequency but not integer multiple of it. On the other hand, sub harmonics is composed of harmonics having frequencies which are smaller than the fundamental frequency and not an integer multiple of it [13]. Any current waveform, which is not linearly related to the supply voltage, is drawn from a non linear load. In general, when the current waveform contains harmonics not linearly related to those presented in the supply voltage, the non linear load is called a harmonic source [14]. Nowadays, the distortion level on the supply network is a serious concern due the proliferation of the non-linear loads in the industrial, commercial, and domestic environments [15]. Inconsequence, harmonic distortion can be considered as a sort of an electrical pollution in the power system which can cause problems if the accumulation of the harmonic currents exceeds certain limits [15].

1.3 Sources and Effects of Power Harmonics

The increasing use of power electronic devices has an enormous effect on the increasing attention about power quality issues such as harmonic distortion. Typical harmonic sources are adjustable speed drives (ASDs), personal computers (PCs), TVs, and many other devices that use power electronic conversion. Common harmonic sources can be categorized as follows [1,14,15]:

- Power electronic devices: the main purpose today for using switching power electronic devices the capability of drawing a current waveform and shape it in order to get the desired output (i.e. AC or DC). In other words, power electronic

converter can be viewed as a matrix of semiconductor switches that provides a flexible interconnection between input and output nodes of an electrical power system. These switches provide a good controllability on the converter output. Although this is beneficial, this has an immediate side effect which is the incremental levels of harmonics in the system. Power electronic converters include AC/DC rectifiers and DC/AC inverter and other power conversion circuits.

- Arcing devices: harmonics from these devices are generated as a result of the nonlinear relationship between the voltage and current. The main harmonic sources in this category are the electric arc furnace, and arc welders.
- Electromagnetic saturable devices: This phenomenon occurs mainly in equipments such as power transformers and electromagnetic devices with a steel core, including motors. Harmonics from these devices are generated due to the nonlinearity of the magnetic core caused by the electromagnetic saturation.

Each power system apparatus has a distinct sensitivity to harmonic distortion, and therefore harmonics flowing in power systems affect each type of apparatus differently. Harmonic distortion may have several effects such as the following:

- Transformer overheating: in transformers, the primary effect is the additional heat generated by the losses caused by the harmonic content of the load current. In this case, the designer must make different design choices for a transformer to accommodate higher frequencies [14,16,17].
- Telephone interference: it has also been observed that harmonics is a cause in the degradation of the communication system performance due to interference caused by harmonics with the communication system frequency [1,14].

- Malfunction of electronic loads: some power electronic loads are sensitive to AC supply voltage characteristics where they may malfunction [17].
- Metering errors: metering and instrumentation can be affected by harmonic components [17,18].

1.4 Aim and Objectives:

The aim of this research is to design a new topology of single tuned passive filter circuit which has the ability to perform the harmonic filtration process effectively. This new filter topology is designed as an output filter for DC/AC inverter. The new design leads to two significant results, first, to achieve the same performance in reducing a specific harmonic component as the traditional single tuned passive filter is capable of, secondly, is to trace any harmonic component regardless its location in the frequency spectrum. The new topology is a modification of the conventional single tuned passive filter topology. The modification is achieved by inserting a switched capacitor circuit in series with the tuned inductor. The switched capacitor circuit in this case acts as a variable capacitor which may be varied by changing the duty cycle of the semiconductor switches so that the value of the equivalent capacitance tracks the variation of the harmonic frequency profile which might be a result of a change of the operating frequency of an inverter. The novelty of introducing the switched capacitor circuit to the field of passive filtering is a main feature of this research. The main applications of the switched capacitor circuits in electrical power field are in active filtering and reactive power compensation, while no research has been conducted to introduce it to the field of passive filtering.

1.5 Thesis Outline:

The thesis consists of six chapters, broken down as follows: Chapter 1 is an introduction of the aim and the layout of the thesis. Chapter 2 elaborates different techniques and topologies for harmonic compensation using passive power filters with critical comparison between them. It also introduces a new method for classifying this type of filters. Also, a brief description of the other well-known methods of harmonic filtering, active and hybrid filters. Chapter 3 conducts an overview of voltage source H-bridge inverters where the proposed filter can be used as an output filter for this switching power converter. The author's contribution in chapter 2 and 3 are: critical review of different types of harmonic filters and H-bridge inverters (Traditional and Multilevel), and a comparative analysis of the reviewed topologies for the sake of determining the appropriate configuration in this research work. Chapter 4 presents the mathematical and analytical derivation of switched capacitor circuits in addition to an overview of other related topologies. A selection criterion is set in order to adopt the most accepted switched capacitor circuit configuration for the proposed filtering technique. Chapter 5 presents the modelling and the mathematical analysis of the proposed tuned passive filter using Orcad PSPICE software and simulation and practical results are presented and discussed in details. Finally the conclusions and future work are presented in chapter 6. Appendices A and B present the microcontroller program code and list of publications, respectively.

Chapter 2

Classification of Power Electronic Filters

2.1 Introduction

The survey of published papers on power electronic filtering techniques shows a great deal of interest in the past few years. Many references in the surveyed literature have discussed the evolution of filtering techniques over many years, including passive, active, and hybrid filters [19,20]. The interest in the subject focuses on circuit configurations with their ability to compensate specific or range of harmonics. Passive filters are given a special attention in this chapter due to the adoption of a new passive filter topology. This chapter classifies the available passive filtering techniques according to their configurations, location as well as type of connection. It also presents an overview of the other common filtering techniques (i.e. Active and Hybrid) surveyed in literature. A brief discussion is presented on the merits and drawbacks of each filtering method; leading to the provision of the main guidelines for the proposal of the adopted new passive filter in this thesis. This chapter highlights passive filter techniques in specific as it is necessary to appreciate the new proposed filter for inverter applications, which will be conducted in the following chapter.

2.2 Classification of Passive Power Filters

Passive filters (PPF) are constructed from passive elements (resistors, inductors, and capacitors) and thus the name [21]. Harmonic filters, passive filters in specific, come in many “shapes and sizes” and a large number of circuit configurations have

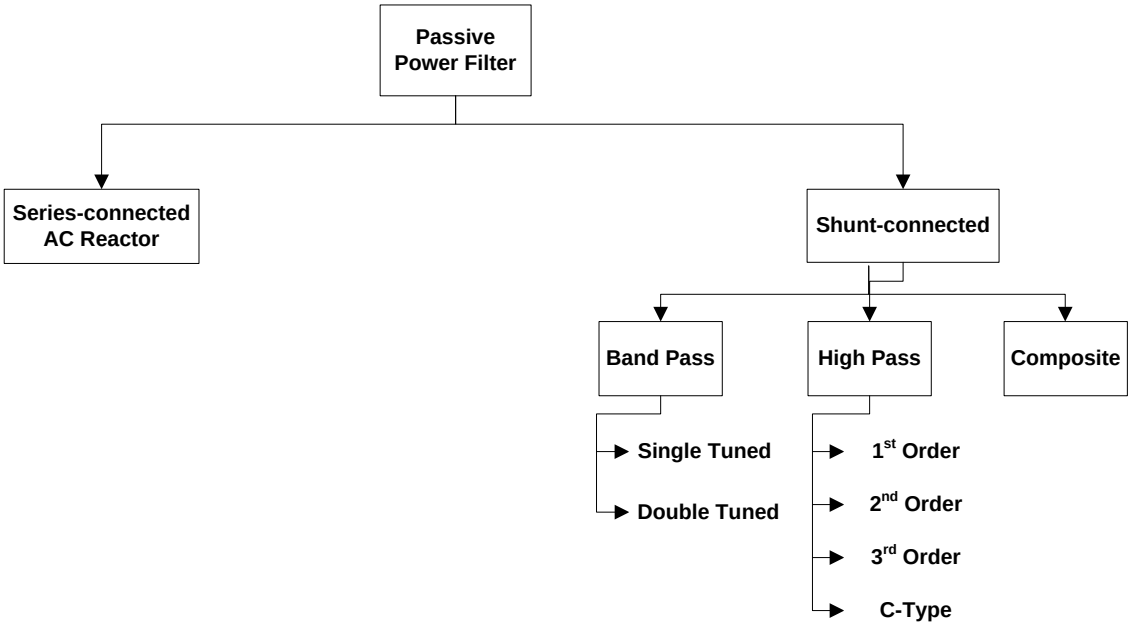


Figure 2.1 Classification of passive filter configuration based on connection type and harmonic to be compensated

been proposed in the literature to enable the compensation of harmonics in power systems. To classify these configurations for the purpose of clarifying the strengths and weaknesses of each topology, it is desirable first to distinguish and classify the overall passive filtering topologies and techniques. On the basis of the published work in the field of passive power filtering, this type of filers can be classified using the following criteria:

1. Topology and configuration based on connection type in the circuit (e.g. series connected or shunt connected) , and harmonics to be compensated (e.g. specific and/or range of harmonics);
2. Type of element's parameters in the circuit (e.g. Fixed or variable filters); and
3. Point of common coupling (e.g. Input or Output filters)

The following Sections classify the Passive Power Filter according to the above criteria. This will provide a better understanding in dealing with these filters, as it shows the merits and limitations of each type.

2.2.1 Classification According to Configurations Based on Connection Type in the Circuit and Compensated Harmonics

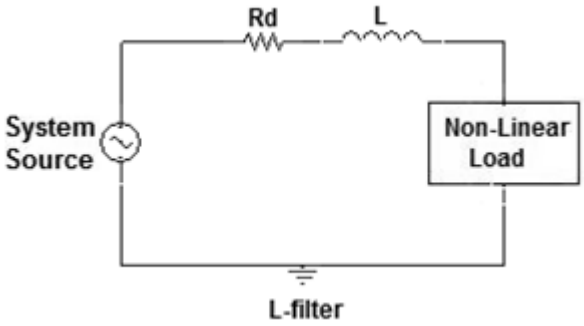
Passive filters are composed of a combination of capacitors, inductors, and damping resistors [5]. These filters can be categorized as series, and shunt connected filters as shown in Figure 2.1. Each type of connection and related topologies is presented in the following subsections showing differences and impedance-frequency relationship for harmonic compensation.

2.2.1.1 Series-Connected AC Reactor

Series AC Reactor is constituted of an inductor connected in series with the nonlinear loads. This type of configuration is considered as a low pass filter. Figure 2.2a illustrates the basic configuration of series-connected reactor in the power system. It has the ability to pass low frequency harmonics, the fundamental component, and provides high impedance to high frequency harmonic currents to limit their proliferation into the power system. Figure 2.2b shows filter impedance-harmonic frequency relationship at different damping resistor values (Rd). Rd controls the minimum impedance at a harmonic frequency which sometimes reflects the internal resistance of the series reactor. The merit of this filter is in its low cost, small size, and provides no system resonance condition. However, it suffers from handling the rated full load current, and it only improves harmonic distortion from 30% to 40% at best according to related studies [21].

2.2.1.2 Shunt-Connected Passive Filter

Shunt filters' passive components generally are rated for part of the system voltage (with respect to ground). Such design leads to smaller component sizes and costs.



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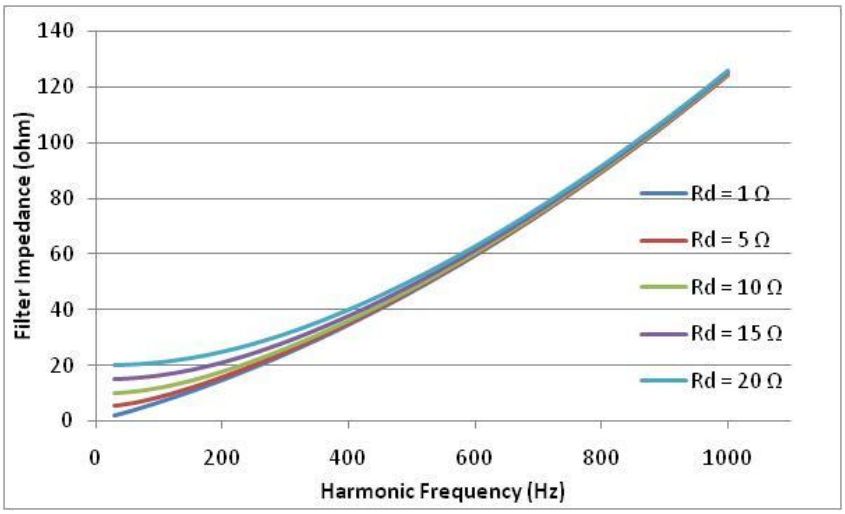


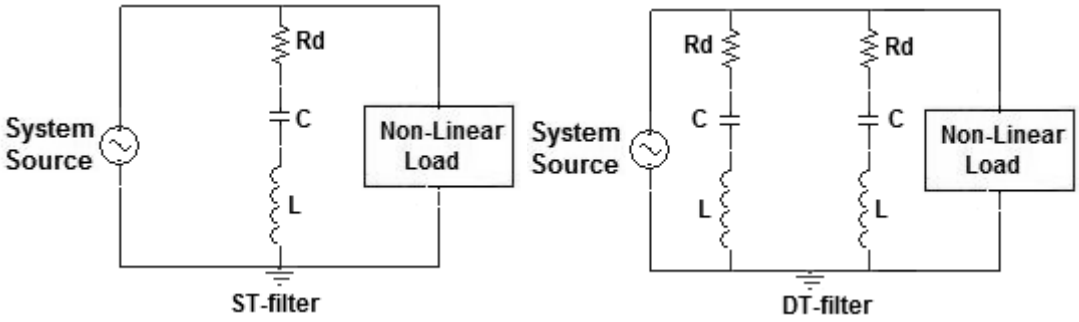
(b)

Figure 2.2 Low Pass L-filter, (a) Filter configuration in power system and (b) Filter impedance-harmonic frequency relationship at different damping resistors

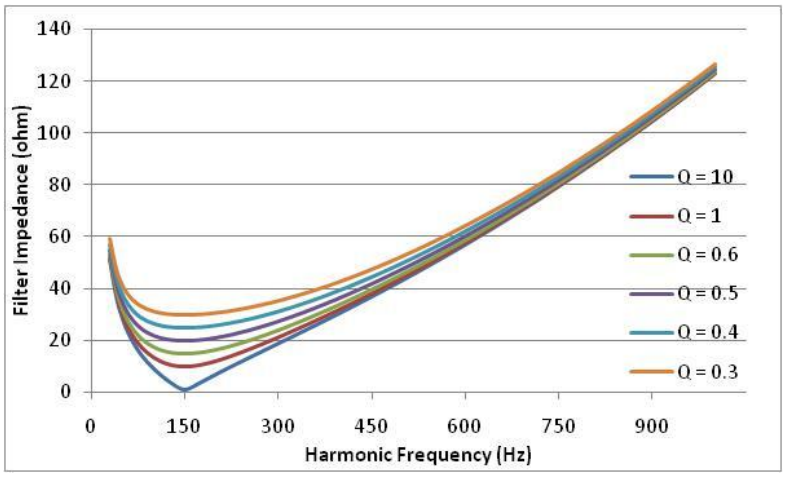
Shunt-connected passive filters can be classified into three basic categories as follows:

1. Band pass filters (of single or double tuned),
2. High pass filters (of first-, second-, or third- order, or c-type),
3. Composite filters.

Band pass filters, including single tuned (ST) and double tuned (DT), are usually used to compensate specific harmonic frequencies. The ST filter (Figure 2.3a) contains a capacitor (C) in series with an inductor (L).



(a)



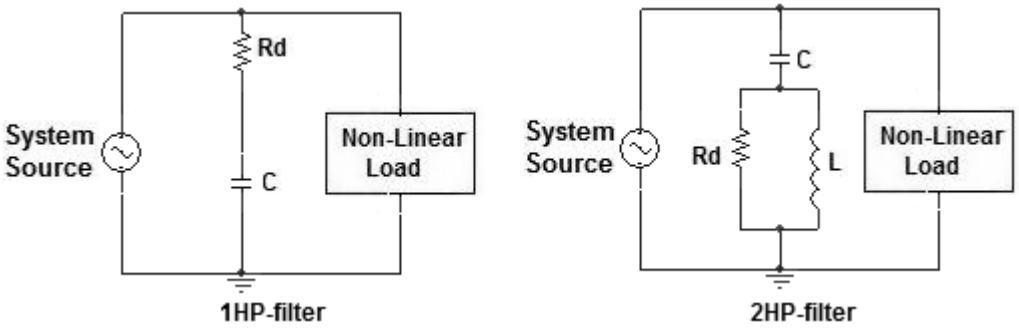
(b)

Figure 2.3 Band Pass Tuned filter, (a) Single and Double tuned Filter configuration in power system and (b) ST filter impedance-harmonic frequency relationship at different quality factors

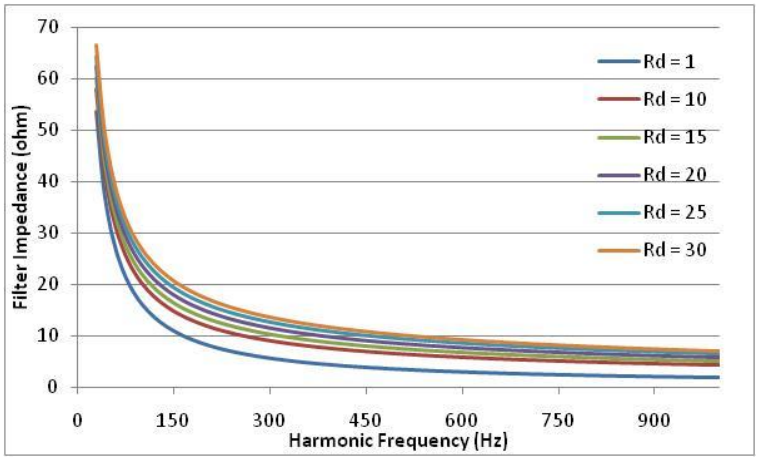
DT filter (Figure 2.3a) is composed of two ST filters connected in shunt with the non linear load in order to tune at two harmonic frequencies. Capacitor and inductor values, in both band pass filters, are determined so that the filter's impedance is near zero or at the harmonic frequency, which bypasses that harmonic. This harmonic frequency is called the tuning frequency which is given by:

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{2.1}$$

A damping resistor, Rd, can be inserted in series with the tuned components in order to adjust the tuning's sharpness [14].



(a)



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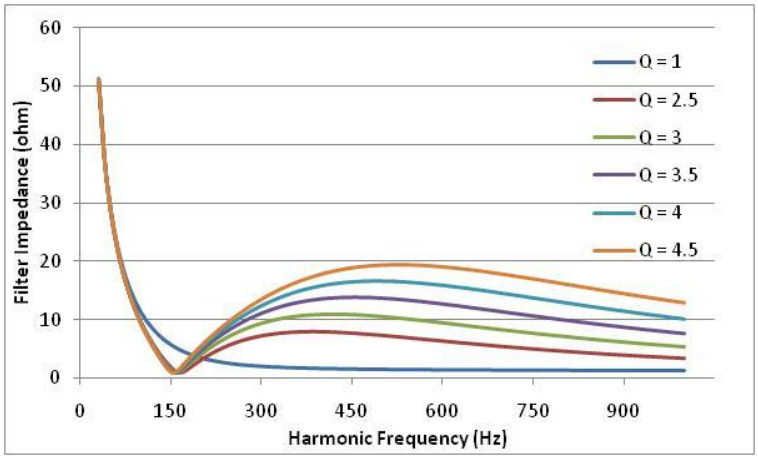


(c)

Figure 2.4 High Pass filter, (a) 1st order and 2nd order HP filters Filter configuration in power system, (b) 1st HP filter, and (c) 2nd HP filter impedance-harmonic frequency relationship at different quality factors

This adjustment is represented by a term called the quality factor (Q) which is given by:

$$Q = \frac{\sqrt{L/C}}{Rd} \tag{2.2}$$

Figure 2.3b illustrates ST filter impedance, tuned at 150 Hz, as a function of the harmonic frequency at different quality factor. It is noticed that the sharpness of the filter is controlled by varying this factor as in (2.2).

High pass filters are able to absorb a wide range of harmonic by providing a low impedance path at this range of high frequencies. The inserted damping resistor determines the sharpness of the tuning filter and its frequency response behaviour. For high pass filters, the quality factor is defined as follows [14]:

$$Q = \frac{Rd}{\sqrt{L/C}} \tag{2.3}$$

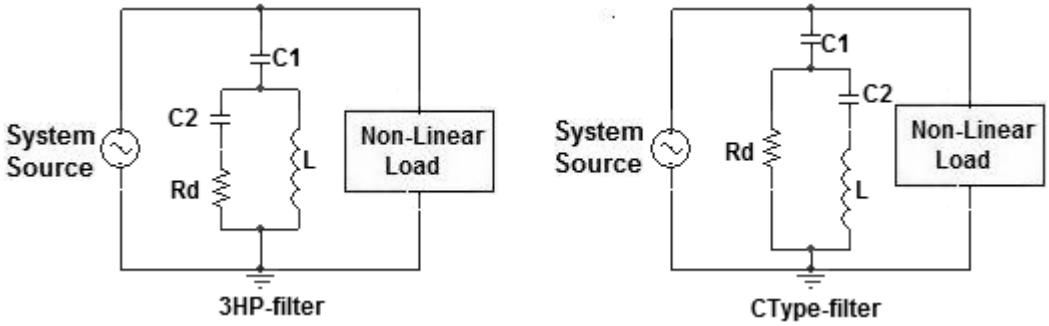
Figure 2.4a presents the first-order high-pass filter (1HP), which provides low impedance at high frequencies due to the capacitor characteristics. 1HP filter is basically composed of capacitor in series with a resistor. Due to the absence of an inductor, the quality factor does not apply, and the series resistance is chosen to limit the current that flows through the capacitor. Figure 2.4b shows 1HP impedance as a function of the harmonic frequency at various quality factors. In order to have low impedances at high frequencies, the capacitor size needs to be large. Inconsequence, this increases the cost and cause over reactive compensation of the system. For these reasons, this filter is not as much popularly used as are the other types of HP filters.

The second-order high pass filter (2HP), as shown in Figure 2.4a, consists of a capacitor in series with a parallel inductor and resistor. They are determined so that the filter acts like the ST filter at the tuning frequency and like the 1HP filter at high

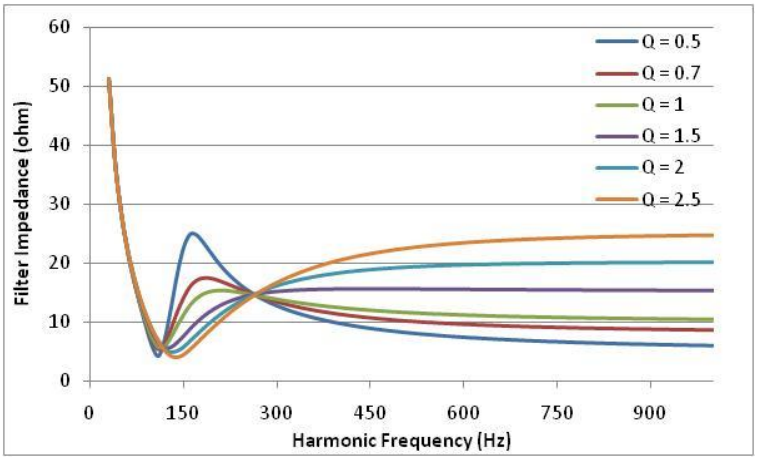
frequencies. This is due to the small value of the inductive reactance at low frequencies bypassing the resistor in the parallel branch, and large value at high frequencies, allowing the current to flow in the resistor branch. At the tuning frequency, a notch valley is observed (Figure 2.4c) which is a result of tuning the capacitor with the inductor at the desired harmonic frequency as in (equation 2.1). Figure 2.4c shows the effect of varying the quality factor where the higher Q is, the closer the filter acts like ST filter. The 2HP filter is considered as the most popular high pass filter adopted in industrial systems [14].

The third order high pass filter (3HP), as shown in Figure 2.5a, presents high impedance, mainly capacitive, at the fundamental frequency and low impedance, predominantly resistive, over high frequencies [14]. The behaviour of this filter matches ST and 1HP filter at tuning frequency, and at higher frequencies, respectively as shown in Figure 2.5b. This is due to the small inductive reactance at low frequencies, bypassing resistor-capacitor branch, and high impedance at higher frequencies, where the current will pass through resistor-capacitor branch. Capacitors C_1 and C_2 are tuned with the inductor to the desired frequency, (equation 2.1) [22,23]. 3HP filter yields less loss at the fundamental frequency compared to 2HP filter because of the insertion of C_2 in series with the resistor [24]. Figure 2.5b shows the impact of varying the quality factor over the filter's impedance characteristic. It is clearly shown that the filter exhibits a resonant valley at the tuning frequency and a resonant peak at higher frequency value [22]. This is also due to the effect of tuning both capacitors to the same frequency with the inductor.

The harmonic filtering performance of the C-type filter, shown in Figure 2.5a, lies in between that of the 2HP and 3HP filters. The series inductor-capacitor branch in



(a)



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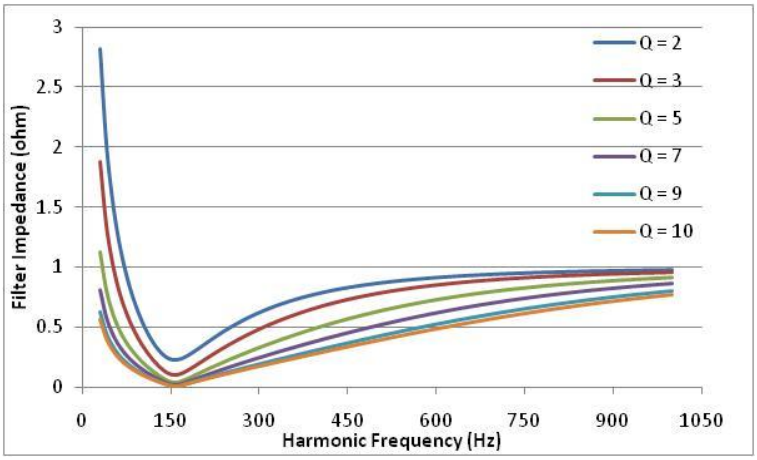


(c)

Figure 2.5 High Pass filter, (a) 3rd order and C-Type HP filters Filter configuration in power system, (b) 3rd HP filter, and (c) C-Type HP filter impedance-harmonic frequency relationship at different quality factors

parallel with the resistor is tuned at the desired frequency, (equation.2.1). At the tuning frequency, the resistor branch is bypassed by the low impedance branch exhibited by the tuned inductor and capacitor elements. Thus the filter acts as a capacitor branch at the fundamental frequency where a little current flowing through the resistor and loss is minimized. The tuning of C_1 and C_2 with the inductor makes the filter behaves like ST filter. At higher frequencies, the inductor reactance becomes large. Inconsequence, the current will flow through the resistor branch which makes the filter perform similar to the 1HP filter as shown in Figure 5.4c [25].

The third type of shunt connected filters is the composite passive filter, as shown in Figure 2.6. This type is composed of a number of passive filters, previously conducted, in shunt with the non-linear load. A common type of composite filter includes several band pass filters and a branch of a high pass filter. Band pass filters are tuned individually to selected low frequency harmonics. The high pass filter branch is inserted to attenuate high frequency harmonics [26].

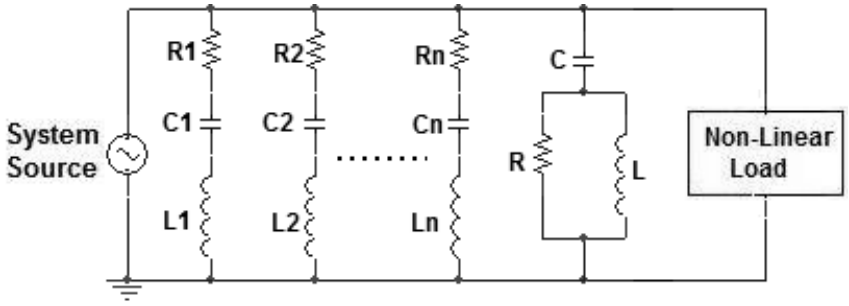


Figure 2.6 Composite passive filter : nth number of ST filter, and 2HP filter

2.2.2 Classification According to Parameters in the Circuit

Passive filters can be classified according to their element's parameters in the circuit. The operation of the filter is dependent on the parameters flexibility. In this section, passive filter is classified into fixed and variable filters. The latter type can be categorized as variable inductor, and variable capacitor as shown in Figure 2.7

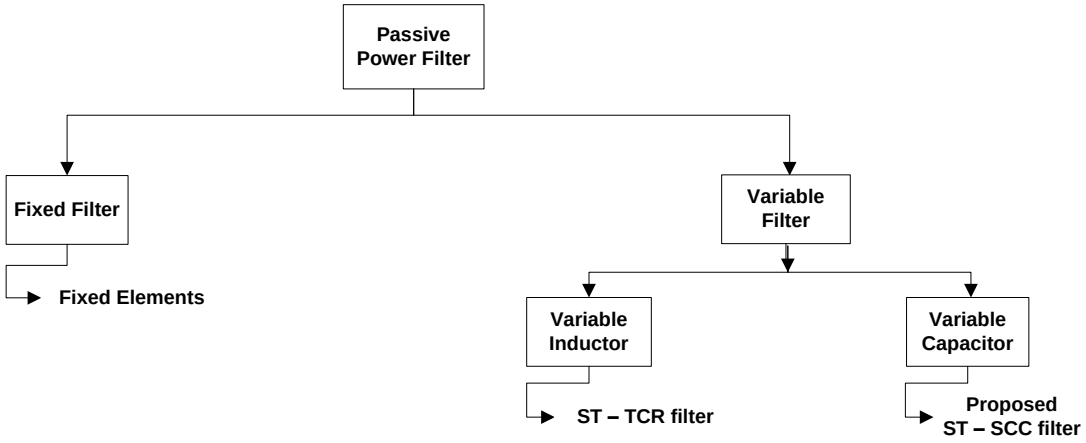


Figure 2.7 Classification of passive filter configuration based on element's parameters in the circuit

Each type of this classification and related topologies is presented in the following subsections.

2.2.2.1 Fixed Passive Filter

Passive power filters operate using fixed parameters (i.e. inductor, capacitor, and resistor), as presented in section 2.2.1, are classified as fixed filters. In this case, the filters do not respond to any change in the system. The filter performs the filtering action regardless any change in the frequency spectrum. All types of filters discussed earlier in this chapter are classified under this category.

2.2.2.2 Variable Passive Filter

Variable passive filters components are varied in order to get different values of inductors and/or capacitors. Such design can be implemented in various topologies of passive filter by replacing the fixed tuned element and insert the variable element circuit.

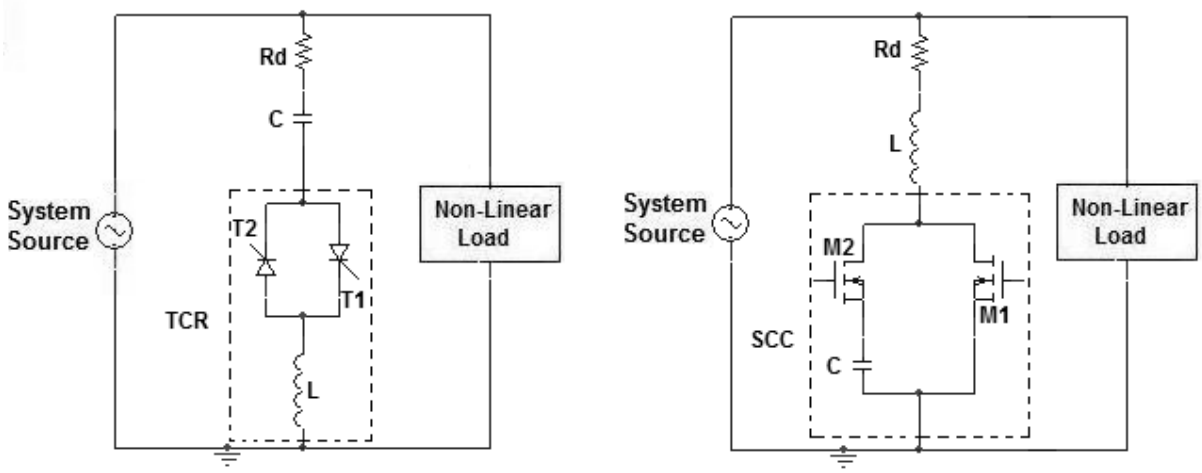


Figure 2.8 Variable passive filter configurations, a: ST filter using TCR, and b: Proposed ST filter using SCC

Variable passive filters can be classified into two basic categories as follows:

1. Variable inductor (of Thyristor-controlled reactor as presented in literature [27,28]),
2. Variable capacitor (of Switched capacitor circuit as proposed in this thesis),

Variable inductor based passive filter, include a tuned capacitor and thyristor-controlled reactor (TCR) which act as a variable inductor. Figure 2.8a illustrates this method adopted by ST filter topology. In this technique, the inductor is connected in series with two thyristors back to back (T1 and T2). The thyristors are either in zero or full conduction [5]. The equivalent inductor reactance in this circuit can be varied by controlling the triggering angle of the thyristors. Although such technique can be effective in varying the inductance value, however the triggering of the thyristors, in either zero or full conduction, can cause the generation of huge amount of current harmonics. This is due to the intrinsic capability of the thyristor to switch at low frequency. Therefore, although the inductor value is controlled, the harmonic distortion flowing into the system is increased. This requires insertion of additional passive filter

in order to compensate the harmonics injected by the TCR. Inconsequence, this will increase number of components, and the cost of the system.

Variable capacitor based passive filter, include a tuned inductor and variable capacitance circuit called Switched Capacitor Circuit (SCC). This circuit is the main contribution in this thesis. Figure 2.8b illustrates this method adopted by ST filter topology. In this technique, the capacitor is connected in series with a fast semiconductor switch (i.e MOSFET, M2) where the series configuration is connected in parallel with a second switch (M1). This type of SCC is called Single Capacitor Double Switch (SCDS) circuit. The equivalent capacitor reactance in this circuit can be varied by controlling the duty-cycles of the switches. The switches can operate at relatively high switching frequency (up to 10 kHz). High switching frequency is preferred to enhance the spectral performance of the SCCs output which shows superiority on TCR circuit in terms of harmonic injection. Inconsequence, no need for additional filters for the line current which will decrease number of components and the cost of the system compared to TCR. This proposed filter is covered in details in Chapter 4.

2.2.3 Classification According to Point of Common Coupling

Passive filters can be classified according to their point of common coupling in the system. Filters can be inserted before harmonic sources (i.e. power electronic converters) in order to protect the system source from harmonics; this type of filters is called Input Filters. On the other hand, filters inserted after power converters are called Output filters. The place where filter is inserted is called Point of common coupling (PCC). Figure 2.9a shows a schematic of shunt input filter which provides harmonic protection for the supply system. Shunt filter placement, as shown in Figure 2.9b, protects the consumer's load from harmonic injection into the main line.

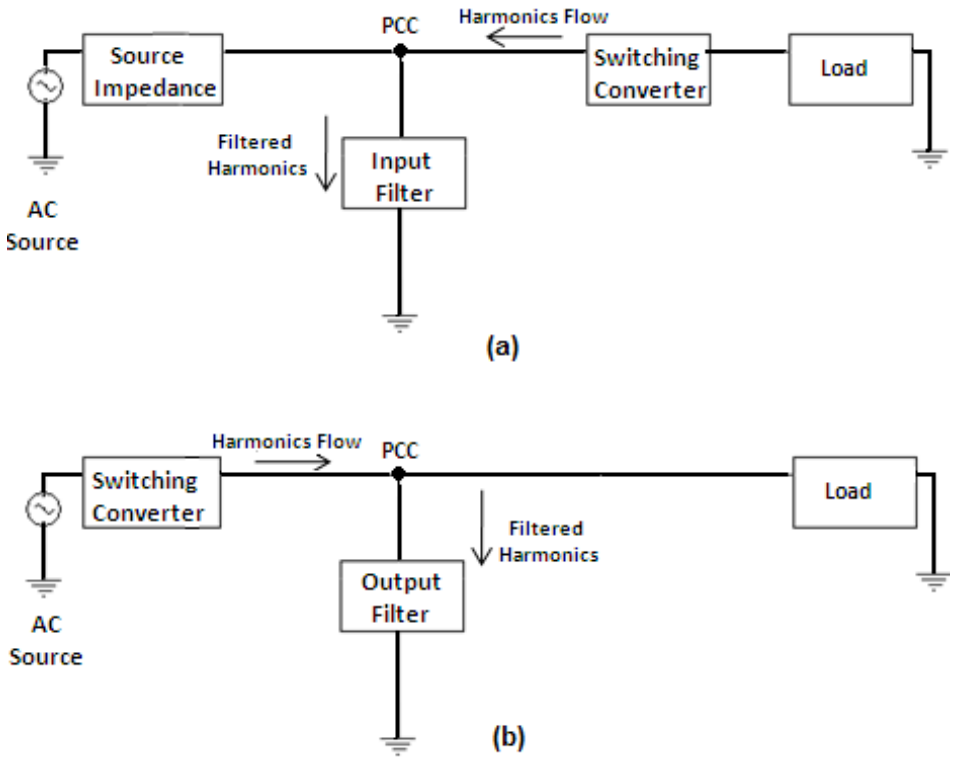


Figure 2.9 Passive Filter classification according to place of insertion, a: Shunt Input filter, and b: Shunt Output filter

All types of passive filter, previously conducted in this chapter, and other power electronic filters, active and hybrid filters conducted in the following sections, can be used as an input or output filters.

2.3 Overview of Active Power Filters

Active power filters were developed to provide better dynamic control of harmonic compensation. The developments in solid state switching devices and their control methods played a significant role in this area of harmonic filtering. Active power filters (APF) can be classified by types of converter used in their circuit and type of connection (i.e. Shunt or Series). APFs can be classified into shunt, series, and hybrid APFs as shown in the block diagram in Figure 2.10. Hybrid active power filters (HAPFs) are a combination of active and passive filters in order to combine the merit of each type as will be conducted in the following sections [5].

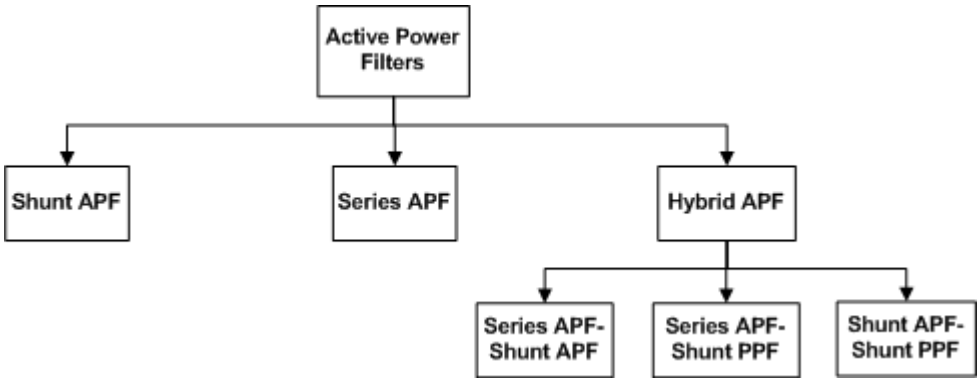


Figure 2.10 Classification of active power filters configurations

2.3.1 Configurations of Active Power Filters

A typical APF configuration, including components and their interconnections, can be represented by the generalised block diagram as shown in Figure 2.11. The transmitted harmonic current in the main line, which is generated by the nonlinear load, is sensed and supplied to the reference current estimator. The reference signal from the current estimator drives the overall system controller which generates the control strategy for the PWM switching pattern. This pattern controls the power circuit through a suitable interface. The power circuit in the generalized block diagram can be connected in series or shunt as will be discussed in APFs classification [19].

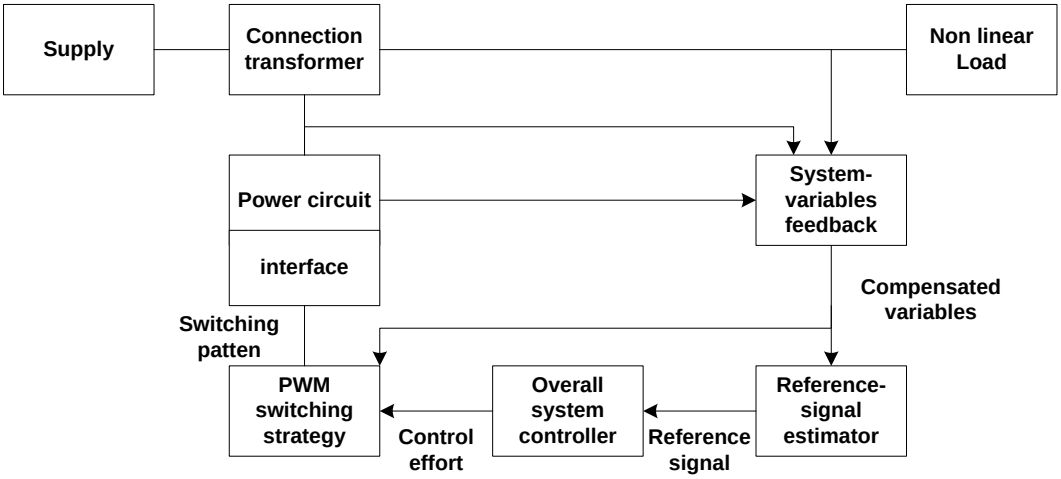


Figure 2.11 Generalized block diagram for Active Power Filters

2.3.1.1 Shunt Active Power Filters

Configurations of this type of APFs are considered as the most important and widely used type in industrial applications [19]. The main purpose of this type is to cancel out current harmonics generated by the non-linear load which are transmitted towards the supply. It is connected to the system as shown in the line diagram in Figure 2.12. Shunt configuration eliminate current harmonics by injecting equal but opposite harmonic current. This means that shunt APF operates as a current source injecting the harmonic components generated by the load but phase shifted by 180° [21]. Inconsequence, non-linear load harmonic currents flowing in the main line are cancelled by the effect of the APF, and the source current remains sinusoidal and free of undesired harmonics. The configuration of the shunt APF is shown in Figure 2.12 [19].

Shunt APFs are normally implemented with pulse width modulated-voltage source inverters (PWM-VSIs). This type of inverters operates as current controlled voltage source. Traditionally, two level PWM-VSI is aimed to compensate non-linear load harmonics rated in the medium power range (hundreds of kVA) due to semiconductors rated values limitations [21]. However, over the last years multilevel PWM-VSIs have been proposed for medium voltage and higher rated power applications. The use of multilevel VSI connected in cascade is considered as an alternative way to compensate high power non-linear loads harmonics.

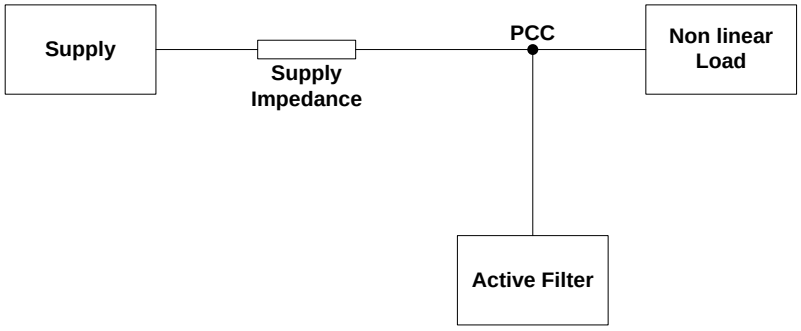


Figure 2.12 Shunt active power filter configuration

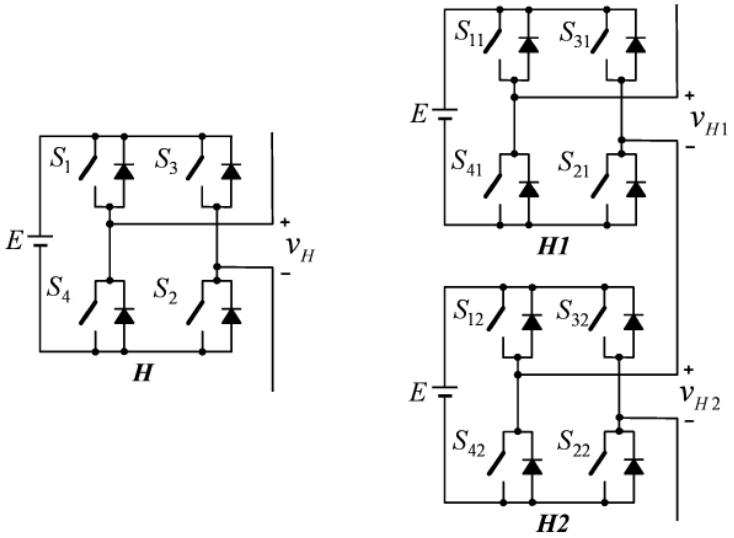


Figure 2.13 Power circuit configurations of shunt APF VSI, a:Two-level VSI, and b: Multilevel VSI

The power circuit configurations of traditional VSI, and multilevel VSI are shown in Figure 2.13. VSIs will be presented and overviewed in the following chapter where it is adopted for the application of the new proposed filter in this thesis. The two-level VSI circuit is common in most shunt APFs either for single-phase [19,29] or three-phase [30-36] configurations. Multilevel VSI based for APF circuits are found in [37]. The main advantages of VSIs in general are the relatively simple control strategy needed for PWM wave shaping and the standard availability for power ratings that can cover the low and medium, using two-level VSI, and high power application regions,

using multilevel VSIs. However, the switching frequency of this harmonic compensation system is considered to be relatively high.

2.3.1.2 Series Active Power Filters

Series APF produces a PWM voltage waveform, which is to be added/subtracted, on an instantaneous basis, to/from the supply voltage in order to apply a pure sinusoidal voltage waveform to the load [19]. Series APF is connected in series with the supply system. It prevents harmonic currents from flowing into the supply system or compensates the distortion in the load voltage as shown in Figure 2.14. This filter is controlled in a way so that it presents low and high impedance to fundamental and harmonic frequencies, respectively, at the PCC. This is applied in order to prevent harmonic currents from flowing into the system. It injects the needed voltage harmonic compensation at the PCC. The main aim of such type of active filters is not directly related to current harmonics compensation of the load, but to isolate these harmonics between the load and the supply source. A drawback to this type of APF is its full carriage of full load current which requires it to withstand high values of rated load current. Inconsequence, this increases the current rating, especially the secondary side of the coupling transformer (increase copper losses, and the physical size of the filter) [19]. In addition, this type is not able to directly eliminate current harmonics. Also, the load will lose the power supply if the filter's transformer experienced failure event [5]. Due to the abovementioned drawbacks, series APFs are less common industrially than shunt APFs.

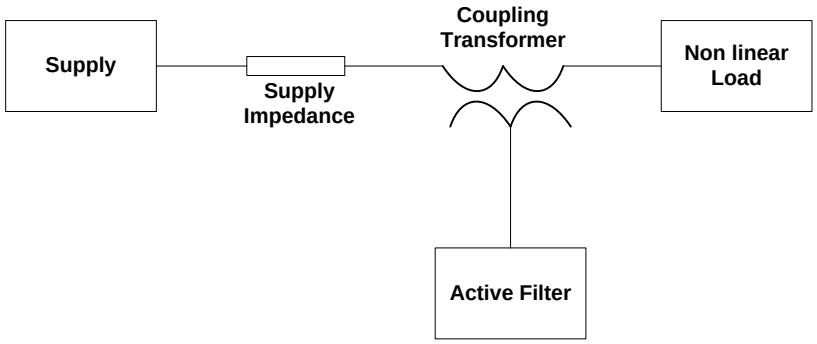


Figure 2.14 Series active power filter configuration

The main advantage of series filters over shunt ones is that they can be used easier for voltage harmonic compensation [19] which dedicates this type to the benefit of the loads. It supplies the load with a pure sinusoidal voltage waveform which is vital for voltage sensitive devices. Circuit configuration of the shunt active filters, in the previous section, can be reused for series APF where only two-level VSI is reported in the literature [19].

2.3.1.3 Hybrid Active Power Filters

Some combinations of the previous presented APFs and/or passive filters can achieve more benefits to the filtering operation, as shown in Figure 2.11. These can be classified as follows:

2.3.1.3.1 Series / Shunt Active Power Filters

This combination aims to gain the merits of series and shunt APFs configurations as shown in Figure 2.15. This can be achieved by controlling both filter topologies to get the desired performance of harmonic elimination. A special control algorithm must be developed for the control of both filters in order to get the maximum compensation performance of both filters.

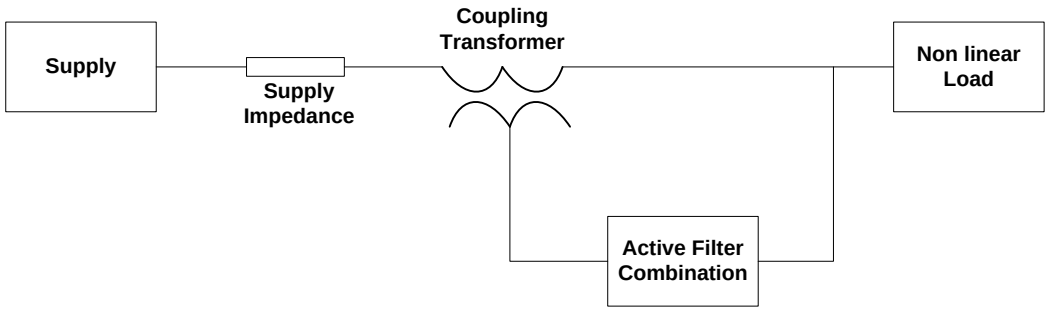


Figure 2.15 Series / Shunt active power filter configuration

This hybrid APF topology has received less attention compared to other APF configuration due to the control complexity, the dependency of the switching pattern of both filter circuits, and consequently higher cost [38-40]. According to literature [38], this topology is used in power system FACTs research studies.

2.3.1.3.2 Series Active / Shunt Passive Power Filters

This type does not suffer from complexity compared to the latter filter. It is composed of the series APF, which provides a high impedance for harmonic frequencies, and a shunt passive filter, which provides a low impedance path for the harmonic currents of the load [40,41]. This hybrid filter extend the capabilities of the traditional series APF to reduce current harmonics as well as voltage harmonics [40,41]. This topology has not been studied thoroughly in literature due to the lack of interest in series APF, and the huge concentration on shunt APFs topologies. Figure 2.16 illustrates the configuration of series active/ shunt passive power filter.

2.3.1.3.3 Shunt Active / Shunt Passive Power Filters

The integration of shunt active and shunt passive power filters represents a very important hybrid topology as shown in Figure 2.17. This combination shows a mixture of the most common configurations used in industrial applications, in both active and

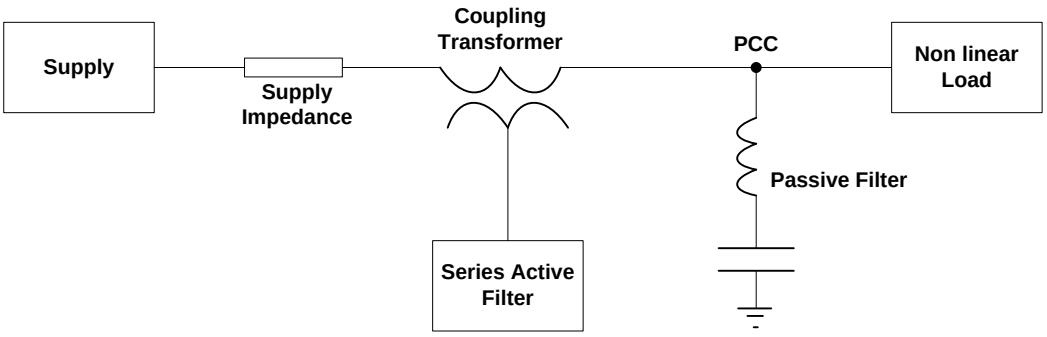


Figure 2.16 Series active / Shunt passive power filter configuration

passive filtering technologies. The active filter part is responsible of low order current harmonics while the passive part is designed for the rest load current harmonics [19,42]. The main drawback of this method and the latter hybrid topologies are high number of components due to the presence of two filters, passive and active circuits, from the point of view of size and cost.

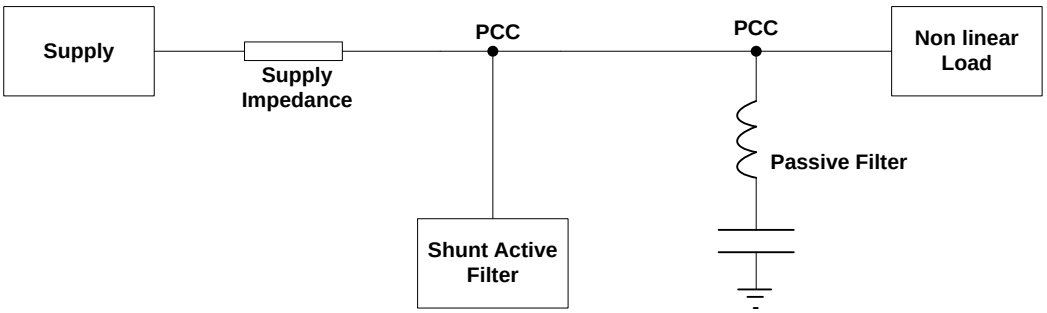


Figure 2.17 Shunt active / Shunt passive power filter configuration

2.4 General Comparison of Power Electronic Filters

It is noticed from the previous review of power electronic filters, the expansion of the use of power electronic circuits in order to eliminate harmonics which is generated mainly from switching converters. This can lead to the fact that the source of the harmonic problem can be solved using the power electronic circuit itself in the case of active filters. Although active filters, including hybrid configurations, have many

Table 2-1 Comparison of Common Power Electronic Filters

Power Filter	Type	Main Components	Merit	Drawback
Passive Filter	Series PPF	-Inductor -Resistor	-Low cost -Low component number	-Full load current carriage
	Shunt Tuned PPF	-Inductors -Capacitors -Resistors	-Low impedance path at tuned frequency -Harmonic load current carriage	-Filters one/two harmonics only -Require multiple filters for high harmonic number
	Shunt High Pass PPF		-Low impedance path for high range of frequencies -One filter is enough for the harmonic range	-Does not achieve as low as tuned filter impedance -High number of components some types in this category
Active Filter	Series APF	-Semiconductor Switches	-Dedicated to voltage sensitive loads (voltage harmonic elimination)	-Full load current carriage -Large physical size and cost -Disruption of supply when transformer failure occur
	Shunt APF		-Current harmonics compensation -Simple control -Standard availability of VSI	-High switching frequency -High component number in multilevel VSI based APF

Hybrid Active Filter	Series APF-Shunt APF	-Inductors -Capacitors -Resistors -Semiconductor Switches	-Voltage and Current harmonic elimination	-Complex control -High number of switches -High switching losses
	Series APF-Shunt PPF		-Extend the capabilities of APF to reduce current harmonics -Simpler control compared to Series APF-Shunt APF -Lower switching losses due to the presence of one APF	- The intrinsic drawbacks of Series APF
	Shunt APF-Shunt PPF		-Simple control due to the presence of shunt APF -Carriage of a portion of the load current	-High number of components

promising advantages, passive filters still have their unique features and merits as well. A comparison of the above discussed topologies, including passive and active filters, showing the merits and drawbacks together with its component level contents is presented in Table 2-1. However, the selection of the proper power electronic filter for a certain application which depends on many factors the designer has to compromise between them, such as; harmonics to be compensated (voltage and/or current) , size and volume, economic considerations, packaging requirements, switching frequency's range and whether the filter is used as an input or output filter. From the literature review and the above comparison between different topologies of power electronic filters, it has been shown that passive filters are superior in the point of view of ease in implementation, simple design, and low cost, especially single tuned filter which is the most common filter used in many applications. Therefore, this filter will be used after modification to implement the new passive filter topology aimed from this research. The proposed filter topology is an output filter for power inverters applications.

2.5 Summary

The subdivisions outlined in this chapter present a quick, yet a relevant review of power electronic filters technology presented in the surveyed published literature. It constitutes classification of passive and active filters used in electric power application. This subdivision is very useful from the point of view of recognising the merits and drawbacks of each type and configuration of power electronic filters. These points will lead to the definition of the new filter topology adopted in this research which is designed for power inverters applications. Therefore, it is important to introduce and discuss these inverters in the next chapter before presenting the new topology in chapter 4.

Chapter 3

Investigation of Power Electronic Voltage Source H-Bridge Inverters

3.1 Introduction

Power electronic converters which transform DC voltages to sinusoidal AC voltages are known as inverters. The main function of inverters is the generation of an AC output waveform with controllable amplitude, phase, and frequency for desired applications. The conversion is achieved by the suitable control of semiconductor switches, where this is called modulation. These switches interconnect the DC source to the AC load with different arrangements. The DC sources can be either energy storage components, such as batteries, or a rectifier (AC-DC converter). The main aim of using different types of modulation is to provide an output waveform with minimum undesired harmonics. In this thesis, inverters will be the main source of harmonics at which the proposed filter is tested. This chapter describes the most common H-bridge VSIs topologies and its modulation techniques found in industry. Special attention is given to low frequency, square wave, and high frequency, PWM, for both traditional and multilevel configurations.

3.2 Voltage Source H-bridge Inverters

VSIs are the most common power conversion systems in many power applications [5] such as uninterruptable power supplies (UPS), domestic appliances (washing machines, air conditioning, etc.), photovoltaic power conversion, adjustable speed drives, and active power filters. The inverter output current is defined by the load,

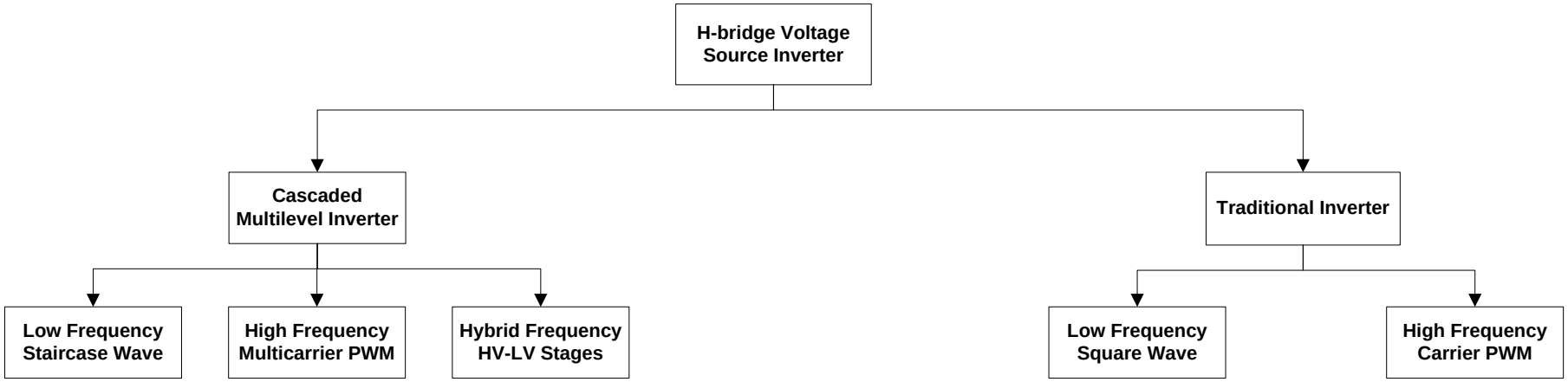


Figure 3.1 Classification of H-bridge voltage source inverters

which is required to have high spectral performance according to the need of the application [34]. This can be achieved by developing modulation schemes; otherwise output filters are used [5]. The following sections present the operating principles and concepts related to VSIs topologies and its corresponding control schemes. Figure 3.1 shows the classification of H-bridge VSI and its subdivision according to their modulation techniques.

3.2.1 Traditional H-bridge VSI

The popular H-bridge VSI is composed of four semiconductor switches, two switches for each leg. A single phase topology is illustrated in Figure 3.2. Each leg has its own switching control pattern, where 1 represents the switching during the conduction period (On-state), and 0 represents the disconnection period (Off-state) [5,43]. Four different switching states are defined by S_a and S_b as shown in Figure 3.3 illustrating the active parts of the circuits in each state [5]. For instance, the amplitude of output voltage v_{ab}, equals to the amplitude of V_{dc}.

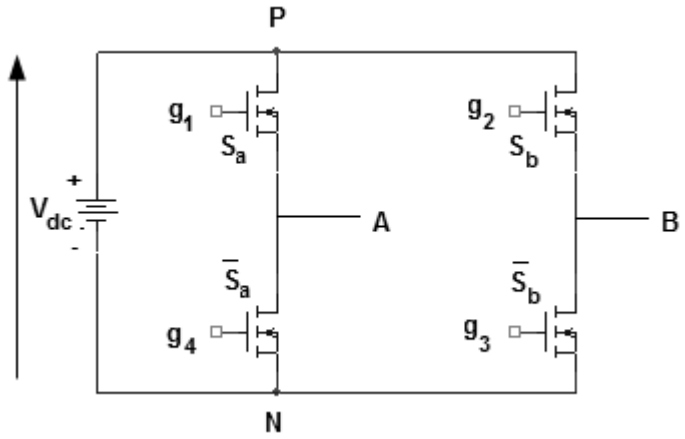


Figure 3.2 Single Phase H-bridge voltage source inverters

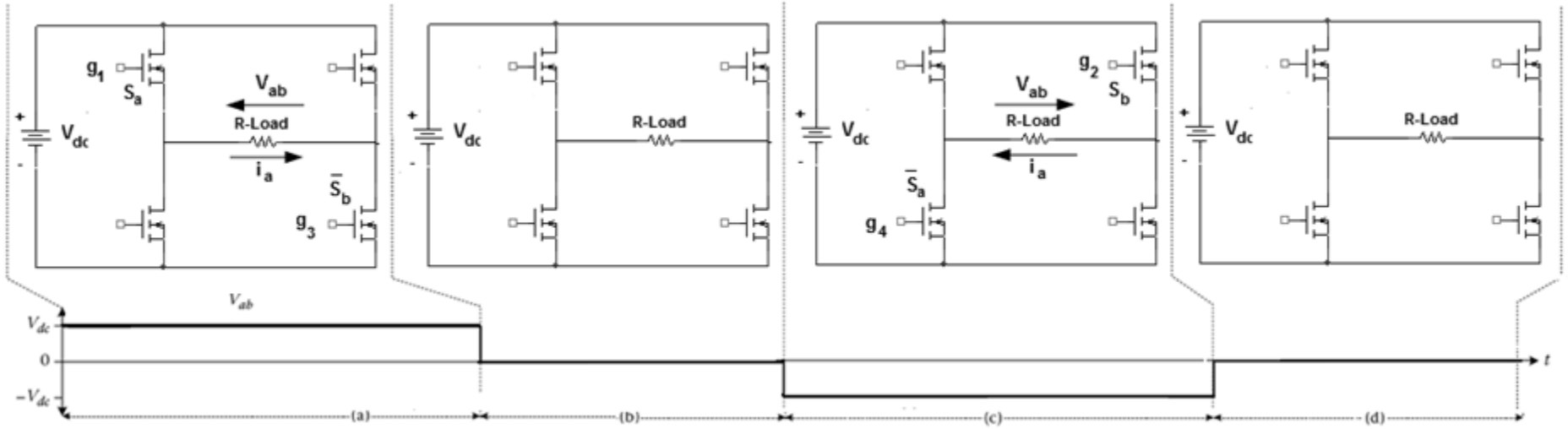


Figure 3.3 H-bridge inverter switching states: (a) vab = Vdc, (b) vab = 0, (c) vab = −Vdc, and (d) vab = 0.

Table 3-1 H-bridge VSI Switching States

Switching State	Gate Signal, S_a	Gate Signal, S_b	Output Voltage, v_{ab}
(a)	1	0	V_{dc}
(b)	0	0	0
(c)	0	1	$-V_{dc}$
(d)	0	0	0

The operation of generating different voltage levels can be expressed generally as follows [5]:

$$v_{ab} = (S_a - S_b)V_{dc} \tag{3.1}$$

where S_a and S_b equals to either 1 or 0. Gate signals switching states for each switch is shown in Table 3-1 [5]. Therefore, by replacing gate signals combination, different output voltage levels are obtained. Hence, three output voltage levels can be generated as $\{V_{dc}, 0, -V_{dc}\}$.

Transistor-based inverter topology is used for low voltage applications due to the limitation of the implemented semiconductor technology. Nevertheless, high voltage thyristor-based inverters can make this topology suitable for higher power applications. However, due to the limitation of using low switching frequency in thyristor-based inverters, filters are needed in order to control the output harmonics for many applications such as a.c. motors [5,44]. This problem can be solved using multilevel VSI, where H-bridge inverter topology is considered as its main building block as will be discussed later in this chapter. The multilevel topology produces more voltage levels hence reducing harmonics and therefore could be used in upgrading existing inverters to higher voltage applications [5].

3.2.2 Common Modulation Methods for Traditional H-bridge VSI

As conducted earlier, VSI inverters are required to provide sinusoidal output waveforms, free of undesired harmonics. This can be implemented by inserting an output filter in order to eliminate harmonics, from the square waveform which is rich in harmonics, or by modulating and controlling the semiconductor switches as will be presented in the following subsections. This process is called modulation; where there are various methods proposed and applied in industry [5,45]. Each method has its unique operating principles, implementation, and performance. This section presents the most common modulation methods for traditional VSI.

3.2.2.1 Low Frequency Square Wave Modulation

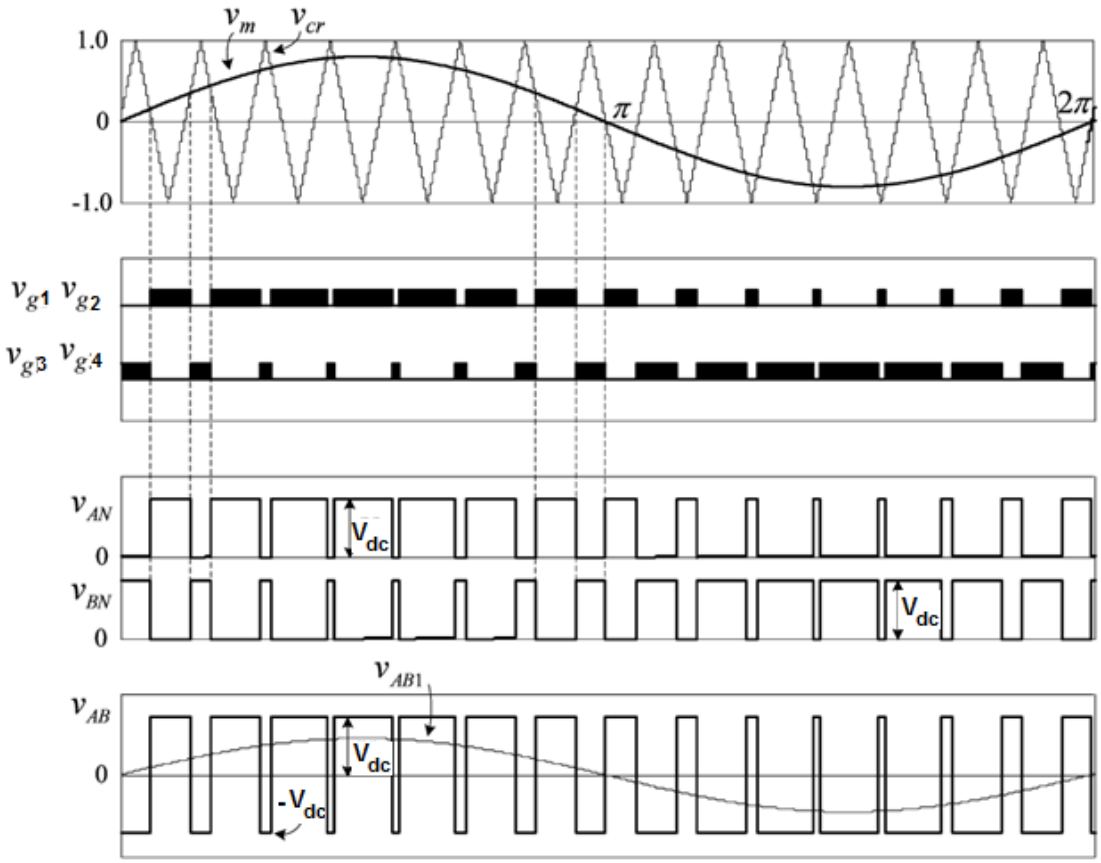
The square-wave modulation is the most basic and easy to implement for H-bridge VSIs [5,45]. This scheme generates a square output waveform with the desired frequency. Figure 3.3 illustrates the output voltage waveform using this modulation method. The operation of this modulation has been discussed in the previous section, showing switching states and the output voltage. This method suffers from low power quality output which is at the expense of the ease of implementation. Therefore, large size filters have to be inserted or another modulation technique can be used as will be conducted in the following section.

3.2.2.2 High Frequency Sinusoidal PWM Modulation

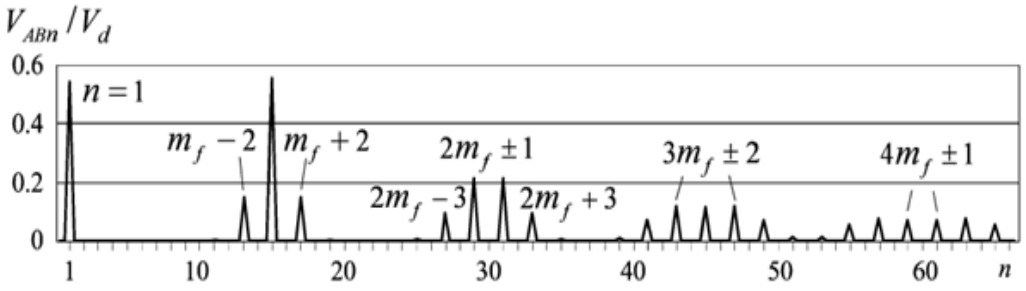
This type of modulation is classified under high frequency carrier based schemes where it is called Sinusoidal PWM (SPWM). It is considered as the most widely used technique in power inverters applications [5,45]. SPWM is well known in its good power quality output. However, it operates under high switching frequency which introduces high switching losses. On the other hand, if the switching frequency is low as

seen in square wave modulation, the size, volume, and economical cost of the output filters increase. In this case, a trade off between switching losses, and filter design cost has to be investigated. The basic idea behind SPWM is by generating a chopped square waveform. This can be achieved by controlling the width of the switching pulses which is also called the duty cycle [45]. The process is achievable by comparing a reference signal, sinusoidal wave, with a carrier signal, triangular wave, where the intersection between both signals produces the desired output waveform. Multicarrier SPWM strategies can be used for multilevel VSIs as will be discussed later in this chapter.

The most common SPWM modulation techniques can be classified as bipolar, and unipolar PWM methods [45]. Figure 3.4a illustrates a typical waveforms of H-bridge VSI modulated by bipolar scheme, where v_m is the sinusoidal modulating signal, v_{cr} is the triangular carrier signal, and v_{g1} and v_{g3} are the gate pulses for switches S_a and S_b, respectively as shown in Figure 3.2 [46]. The upper and lower in each inverter leg behaves in anti-parallel manor where one switch is on and the other is off. Therefore, two independent switch's gate signals are considered in the operating principle explanation, v_{g1} and v_{g3}. These gate signals are a result of the intersection between v_m and v_{cr}. According to Figure 3.4a, the inverter output voltage, v_{ab}, can be found from the inverter terminal output voltages v_{an} and v_{bn}. Since, the output voltage waveform v_{ab} switches between the positive and negative dc voltages, this scheme has derived its name as bipolar SPWM [46]. Figure 3.4b [46] shows the harmonic spectrum of the inverter output voltage using bipolar SPWM scheme, where v_{ab} is normalized to its dc voltage V_{dc}. v_{abn} is the rms value of the n^{th} order harmonic voltage. The spectral performance shows that harmonics appear as sidebands centred around the frequency modulation index m_f and its multiples such as $2m_f$ and $3m_f$, where this index is the relation between the modulating voltage frequency v_m, and the carrier frequency v_{cr}.



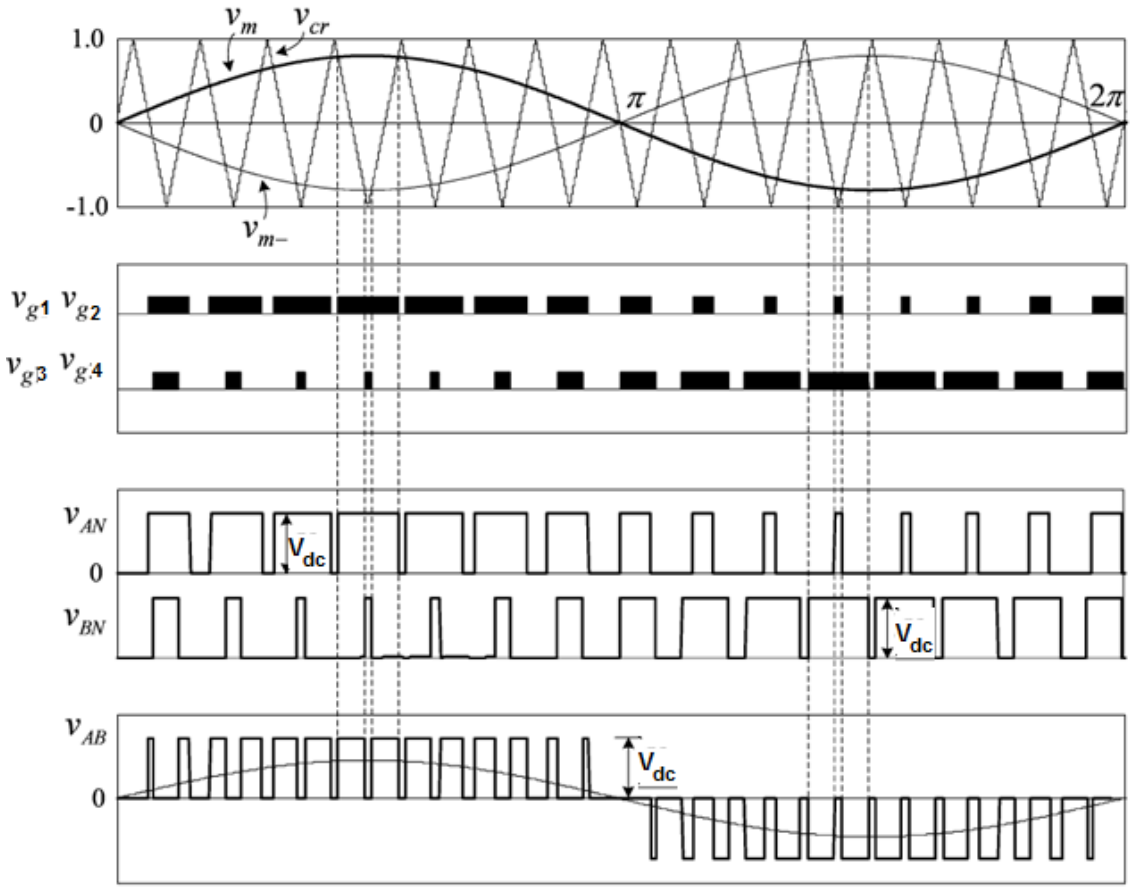
(a)



(b)

Figure 3.4 Bipolar SPWM for H-bridge voltage source inverter m_f = 15, (a) waveforms, (b) harmonic spectrum

The switching frequency of the semiconductor switches is equal to the carrier frequency. The second SPWM modulation technique is the unipolar scheme. This type normally requires two sinusoidal modulating signals, v_m and v_{m-}, where they have the same magnitude but opposite in phase as shown in Figure 3.5a. Both signals are compared with one triangular carrier signal v_{cr}, which generates two gate signals, v_{g1} and v_{g3}, for switches S_a and S_b, respectively. In this case, the inverter output voltage switches between zero and $+V_{dc}$ in the positive half cycle and between zero and $-V_{dc}$ in the negative half cycle of the fundamental frequency. Therefore, this method is known as unipolar SPWM [46]. Figure 3.5b illustrates the harmonic spectrum of the inverter output voltage v_{ab}, which shows the harmonics as sidebands centred around $2m_f$ and $4m_f$ [46]. The low order harmonics, seen around m_f in bipolar SPWM, are eliminated in this scheme. The dominant harmonics are seen around $2m_f$ and their sideband frequencies. This is actually the equivalent inverter switching frequency, which is also observed by the load [46]. Although, the switching frequency of the inverter in both modulation schemes, bipolar and unipolar, are the same, the dominant harmonics changed its location and are shifted higher in the spectrum in the unipolar case. This is due to the fact that switches S_a and S_b do not switch simultaneously, where they switch at different time instances, leading to doubling the inverter switching frequency. This phenomenon distinguishes the bipolar scheme from unipolar where all four switches are operating during each half cycle of the output waveform. An alternative way to implement unipolar SPWM is by using one modulating signal and two phase shifted carriers [46].



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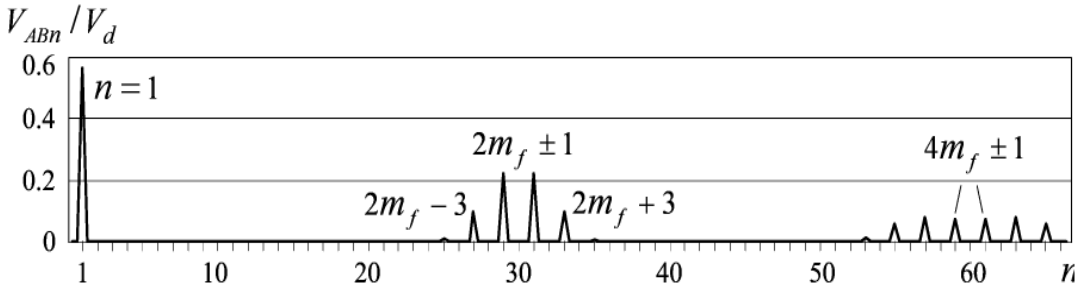


(b)

Figure 3.5 Unipolar SPWM for H-bridge voltage source inverter, (a) waveforms, (b) harmonic spectrum

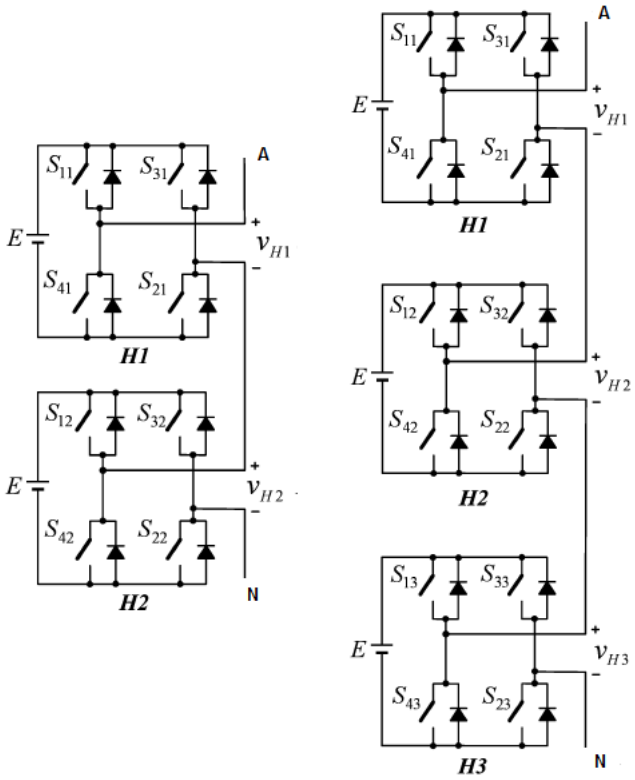
3.2.3 Multilevel Cascaded H-bridge VSI

Topologically, a general structure of voltage source-multilevel inverter (VS-MLI) can be considered as a large voltage synthesizer realized from a number of smaller discrete dc voltage sources [47]. The output is generated with a staircase AC output voltage. The previously presented traditional H-bridge inverter generates an output voltage with a square waveform with respect to the negative terminal of the voltage source, while the VS-MLI generates multiple voltages [48]. The results of a patent search show that VS-MLI circuits have been around for more than 30 years [48]. An early traceable patent appeared in 1975 [49], in which the cascaded H-bridge (CHB) inverter was first introduced with a format that connects H-bridge inverter cells in series where each cell is fed by separate DC source. CHB inverter was presented again by Marchesoni et al. in 1988 [48]. Although the CHB inverter was invented earlier, its applications did not prevail until the mid-1990s [49]. The advantages of CHB inverter compared to traditional inverters are [50]: lower output voltage harmonic distortion; lower switching losses; and higher output fundamental voltage. Ultimately, a zero harmonic distortion of the output wave can be obtained by an infinite number of levels. As mentioned earlier, VS-MLIs are believed to be promising in high power applications [51]. VS-MLIs applications include: Flexible AC Transmission Systems (FACTS) [52-62], active power filtering [63], drives [64], and renewable energy systems (RES) [65-70].

It is essential before conducting CHB inverter topology to introduce the following unique features which gives it a promising future in many applications. These features are [71-73]:

1. It is composed of a multiple units of single phase H-bridge power inverter cells (building block) which are connected in cascade to achieve low voltage harmonic distortion.
2. The number of power cells in a CHB inverter is mainly determined by its operating voltage, harmonic requirements, and manufacturing cost. The use of identical power cells leads to a modular structure, which is effective in packaging requirements.
3. CHB inverter is free from complicated connections where it is composed of several H-bridge inverters connected in series.
4. The modularity of CHB inverter allows ease of faulty cells replacement. When an internal fault is detected and the faulty cell is identified. It can be easily isolated through an external switch, and replaced by a new operative cell, without turning off the CHB inverter.

The previous facts of CHB inverter have drawn tremendous attention in the field of multilevel inverter. The general topology [71] of CHB inverter consists of a series of single phase H-bridge inverter units with equal dc sources, as shown in Figure 3.6a and 3.6b. The separate dc sources may be obtained from batteries, fuel cells or solar cells [71]. Each dc source is connected to a single phase H-bridge inverter cell and can generate three different voltage outputs. The ac outputs of the modular H-bridge inverter cells are connected in series so that the synthesized output voltage waveform is the sum of all of the individual inverter outputs. The number of output voltage levels in a CHB inverter is 2b + 1, where n is the number of dc sources. Figure 3.7 shows the output phase voltage of 11-level (b=5) CHB inverter [71]. The total output voltage is given by $V_o = v_{a1}+v_{a2}+ v_{a3}+v_{a4}+v_{a5}$. With enough levels and an appropriate switching



(a) (b)

Figure 3.6 Voltage Source Cascaded H-bridge Multilevel Inverter Topology, (a) Five-level, and (b) Seven-level Topology

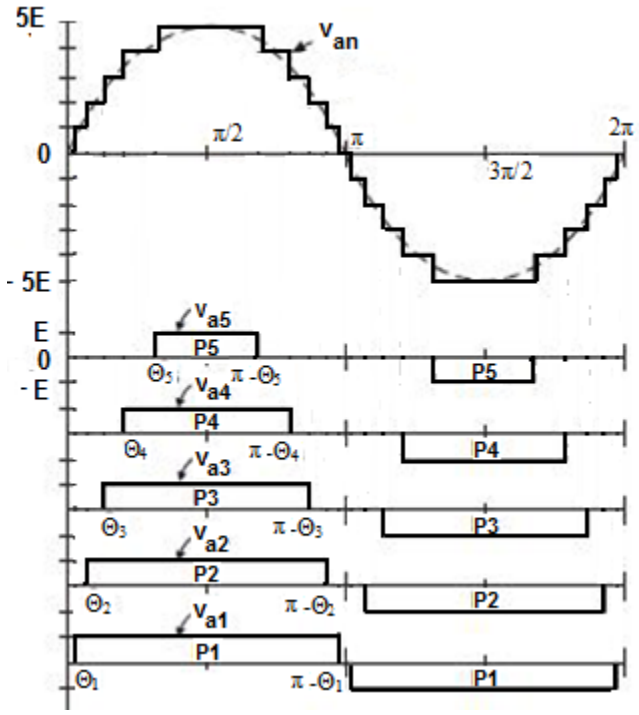


Figure 3.7 Output voltage of an 11-level multilevel cascaded H-bridgeVSI

angles, θ_1, θ_2, θ_3, θ_4 and θ_5, the CHB inverter results in an output voltage that is almost sinusoidal with low output harmonics. In addition, if all semiconductor devices of the H-bridge cells are switching at the fundamental frequency, the switching losses of the semiconductor devices are reduced, resulting in a better utilization and high overall efficiency [71].

3.2.4 Common Modulation Methods for Multilevel Cascaded H-bridge VSI

The different modulation strategies adopted in CHB inverters can be classified on the basis of the switching frequency as showed Figure 3.1. Low switching frequency modulation strategies perform a very low number of commutations of the switching devices during one period of the output voltage, where it generates a staircase waveform. High switching frequency modulation strategies lead to many commutations of the switches in a period of the output voltage. The most popular method is the multicarrier-based pulse width modulation (PWM) [74,75]. Low and high frequency modulation methods are extensions of traditional H-bridge inverter modulation strategies to several levels. Hybrid switching frequency modulation strategies includes a combination of low and high frequencies [76]. Hybrid switching frequency method is conducted due to its importance in multilevel conversion systems. It is noted that there is a trade-off between the inverter switching frequency and the harmonic output. Reducing the inverter switching frequency is one of the effective ways to reduce the switching losses. However, this approach contributes to increase the harmonic output and therefore decrease the output power quality [77].

3.2.4.1 Low Frequency Staircase Wave Modulation

The staircase-wave modulation is the most basic and easy to implement for CHB inverter. This scheme generates a staircase output waveform with desired frequency. Figure 3.7 illustrates the output voltage waveform using this modulation method.

Table 3-2 Multilevel Cascaded H-bridge VSI Switching States (5-Level CHB)

Output Voltage	Switching State				Cell Output	
	S_{11}	S_{31}	S_{12}	S_{32}	V_{H1}	V_{H2}
2E	1	0	1	0	E	E
E	1	0	1	1	E	0
	1	0	0	0	E	0
	1	1	1	0	0	E
	0	0	1	0	0	E
0	0	0	0	0	0	0
	0	0	1	1	0	0
	1	1	0	0	0	0
	1	1	1	1	0	0
	1	0	0	1	E	-E
	0	1	1	0	-E	E
-E	0	1	1	1	-E	0
	0	1	0	0	-E	0
	1	1	0	1	0	-E
	0	0	0	1	0	-E
-2E	0	1	0	1	-E	-E

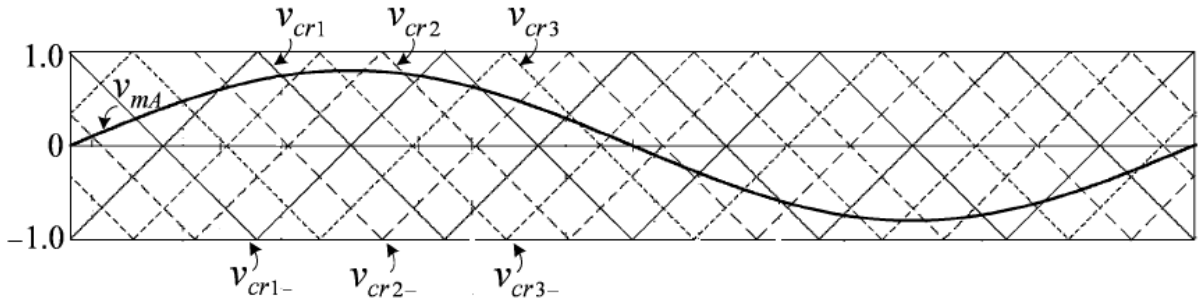
The operation of this modulation has been discussed earlier in the previous subsection. Table 3-2 shows the switching states of five levels CHB inverter, Figure 3.6a [46]. This method suffers from lower power quality output compared to other modulation schemes discussed later in this chapter. This method increases the chance of using more inverter cells in order to achieve a wave close to a sinusoidal waveform. Therefore, the system

suffers from high number of components and packaging constraints in some applications which is at the expense of the reduction in switching losses.

3.2.4.2 High Frequency Multicarrier SPWM Modulation

The most common high frequency strategy for CHB inverter is multicarrier SPWM. The same principle of SPWM carrier-based technique, conducted in traditional inverter modulation, is adopted in CHB inverter where it is the comparison of a reference sinusoidal waveform with a carrier waveform, which is usually a triangular waveform [50]. The carrier frequency defines the switching frequency of the inverter. For CHB inverter applications, multicarrier SPWM is used. The multicarrier techniques are divided into [46] level shifted, and phase shifted modulations.

In general, CHB inverter with m voltage levels requires m-1 triangular carrier signals. In phase-shifted modulation (PS-SPWM), all carrier signals share the same frequency and the same peak-to-peak amplitude. However, there is a phase shift difference between any two adjacent carrier signals. The gate signals are a result of the comparison between the modulating signal v_{mA}, sinusoidal, with the carrier signal. Figure 3.8a illustrates the basic principle of PS-SPWM scheme for seven-level CHB inverter (three H-bridge inverter cells) [46]. It is observed that six triangular carriers are used with 60^{o} phase difference between adjacent carriers. The carrier signals v_{cr1}, v_{cr2}, and v_{cr3} are used to generate gate signals switches S_{11}, S_{12}, and S_{13} in the left legs of the H-bridge cells H1, H2, and H3 in Figure 3.6b, respectively. The remaining carrier signals, v_{cr1-}, v_{cr2-} and v_{cr3-} are 180° out of phase with the first three carriers, v_{cr1}, v_{cr2} and v_{cr3}, respectively. These carriers are responsible of producing the gate signals of switches S_{31}, S_{32}, and S_{33} in the right legs of the H-bridge cells.



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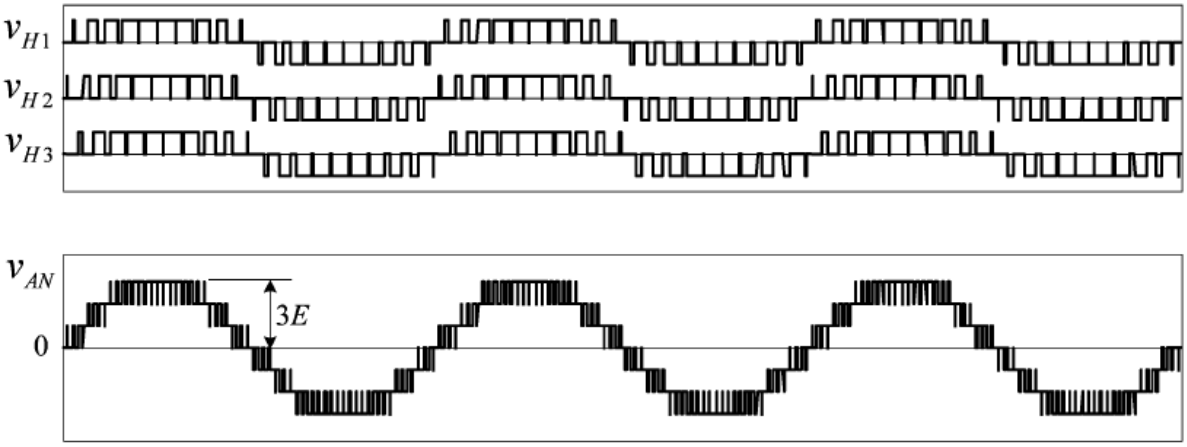

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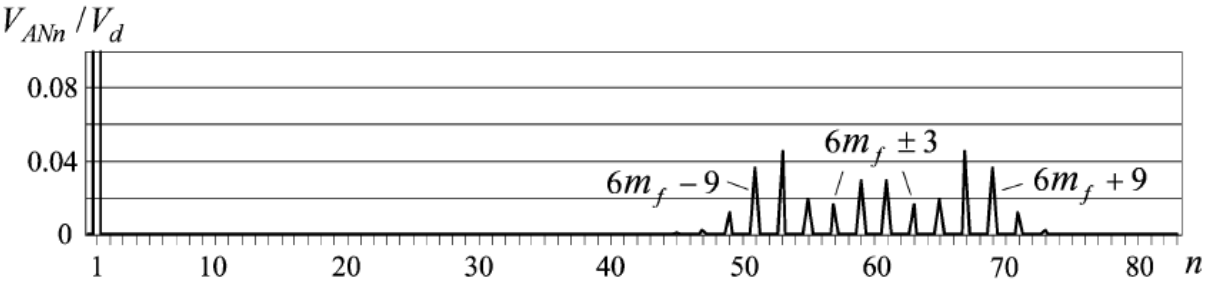
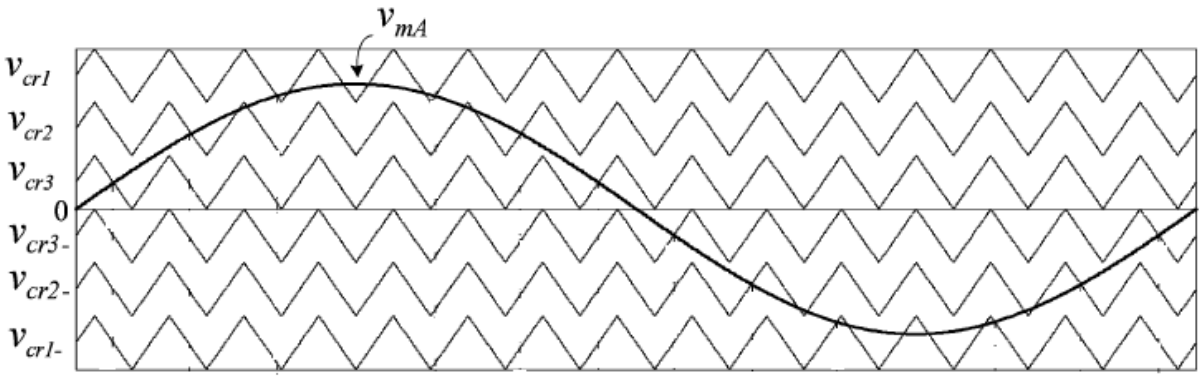


(c)

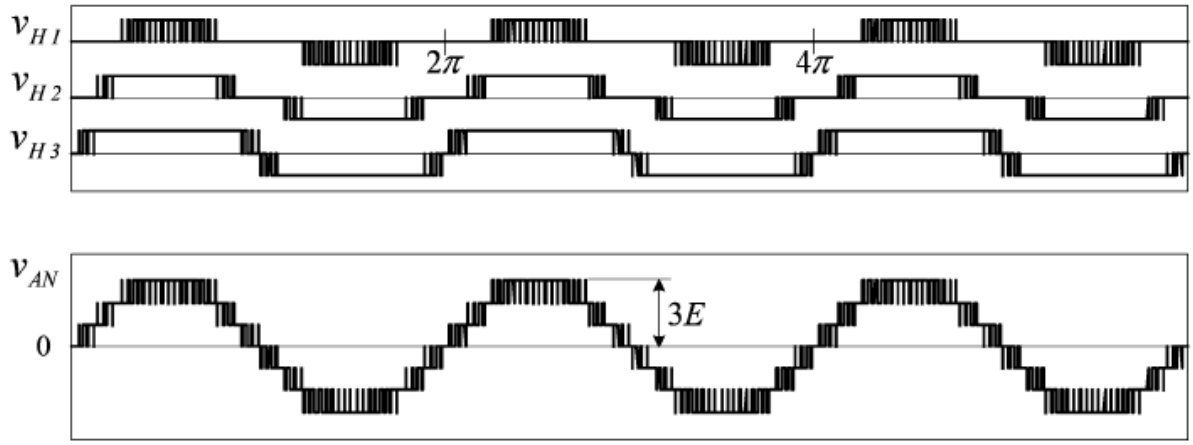
Figure 3.8 Phase-shifted SPWM scheme for seven level CHB inverter, (a)operating principle, (b) output voltage waveforms, and (c)output voltage harmonic spectrum

The gate signals for the remaining switches operate in anti-parallel manor with respect to their corresponding switches in each leg. In PS-SPWM scheme, the gate signals for switches S_{11} and S_{31} in H1 cell are generated by comparing v_{cr1} and v_{cr1-} with v_{mA}. The output voltage of v_{H1} is switched between zero and E in the positive half cycle or between zero and –E in the negative half cycle of the fundamental frequency. It is clear that the total output voltage, of seven-level CHB inverter, is formed by the voltage steps: +3E, +2E, +E, 0, -E, -2E, and -3E, which is the summation of the individual output voltages of cells H1, H2, and H3. Figure 3.8b [46] illustrates the output voltage waveform for individual inverters cells and seven-level CHB inverter with a peak value of 3E. It is observed that the waveforms of v_{H1}, v_{H2}, and v_{H3} are almost identical except a small phase difference caused by the phase shifted triangular carrier. The harmonic spectrum of the CHB inverter is shown in Figure 3.8c where it is shown that no side band harmonics is observed lower than n=60, which leads to a significant reduction in harmonics compared to traditional SPWM modulation conducted earlier in this chapter.

In level shifted modulation (LS-SPWM), an m level CHB inverter requires m–1 triangular carrier signals where all of them share the same frequency and amplitude. The carrier signals are vertically disposed so that these signals are adjacent. Figure 3.9a shows LS-SPWM scheme operating principle where all carriers are in phase and disposed vertically in seven levels CHB inverter. Referring to Figure 3.6b, the uppermost and lowermost triangular carrier signal pair, v_{cr1} and v_{cr1-}, produce gate signals for switches S_{11} and S_{31} in inverter cell H1 [46]. The inner most triangular carrier signal pair, v_{cr3} and v_{cr3-}, produce gate signals for S_{13} and S_{33} in H3. The remaining pair, v_{cr2} and v_{cr2-}, produce signals for switches S_{12} and S_{32} in H2. Figure 3.9b shows the output voltage waveforms for individual inverters cells, and CHB inverter.



(a)



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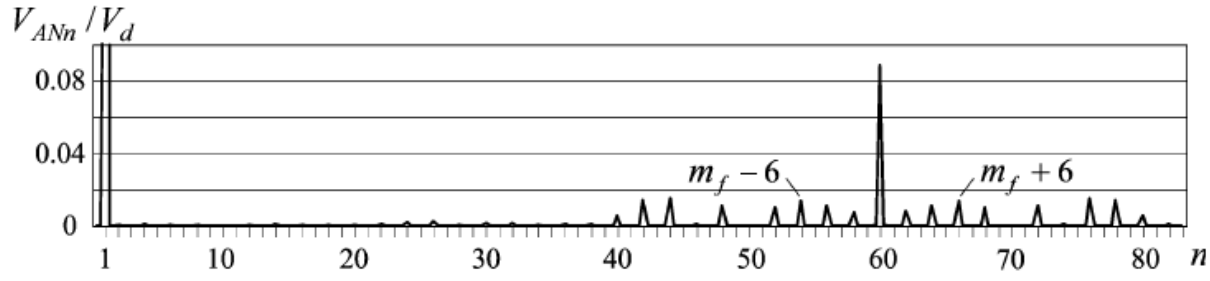


(c)

Figure 3.9 Level-shifted SPWM scheme for seven level CHB inverter, (a)operating principle, (b) output voltage waveforms, and (c)output voltage harmonic spectrum

Similar to PS-SPWM scheme, the dominant harmonics appear as sidebands centred around harmonic n=60, but with lower amplitudes. Inconsequence, better harmonic spectrum is achieved using this LS-SPWM scheme [46].

3.2.4.3 Hybrid Frequency Modulation – HV-LV Stages

Hybrid frequency modulation strategy made a breakthrough in CHB schemes and adopted by many researchers. This method is called high voltage-low voltages (HV-LV) stages method [76]. The main objective of this method is to achieve an output with high efficiency and low switching losses. HV-LV stages scheme has been applied on CHB inverters with unequal dc sources, which uses low frequency switches (i.e. Thyristors) at the HV stage cell to provide bulk power transfer, while it uses high frequency switches (i.e. MOSFETS) at the LV stage cell to enhance the spectral performance of the overall inverter [71].

The basic idea behind the application of this modulation method is to take the advantage of the different power rates among the cells to reduce switching losses, and improve the inverter efficiency [78]. Figure 3.10 shows the output waveform of individual inverter cells, and CHB inverter using this scheme. The input DC voltage used is $3V_{dc}$ for HV cell and V_{dc} for LV cell. It is shown in this figure that the HV cell turns on and off only one time during a half cycle. The un-modulated part left by the square shape of the HV stage cell output is then generated by the next power cell and so on, until the final un-modulated parts of the reference are modulated at high switching frequency by the smallest LV stage cell using traditional unipolar PWM [78]. This completes the generation of a hybrid CHB inverter waveform with a high frequency component but with the difference that fewer switching losses are produced to achieve it [78].

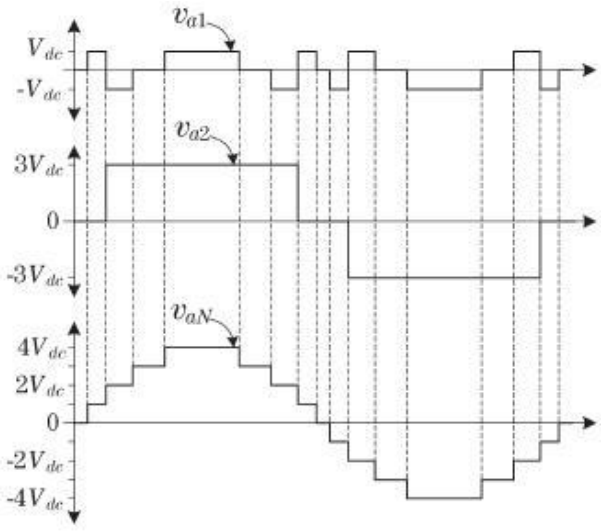


Figure 3.10 CHB inverter modulated by hybrid switching frequency scheme

3.3 General Comparison of Voltage Source H-bridge Inverters

A comparison between traditional H-bridge VSI and CHB inverter, in terms of the modulation scheme, showing merits and drawbacks for each topology is shown in Table 3-3. It is observed that the main distinct superiority of CHB inverter over traditional inverter is in terms of better spectral performance. However, this advantage is at the cost of higher component count, and complex control. This led to the fact that researchers started to develop modulation techniques to get a better harmonic profile. Modulation schemes for both topologies are classified to low and high switching frequency methods. High frequency scheme suffers from high switching losses compared to low frequency scheme. However, it has the superiority of a better harmonic performance which results in a small size output filter if needed. Complex control is a serious issue in implementing high frequency scheme. The invention of CHB inverter led the researchers to develop a promising modulation which is categorized under hybrid modulation scheme. This scheme aim to get low harmonic output with low switching losses compared to the high frequency scheme. However, this led to a

Table 3-3 Comparison of Voltage Source H-bridge Inverters

H-Bridge VSI Topology	Modulation Scheme	Merit	Drawback
Traditional Topology	Low Frequency	-Low Switching Losses -Easy implementation	-High Harmonic Output -Requires large output filters
	High Frequency	-Harmonics easier to filter -Small Filter size	-High Switching Losses -Complex control
Multilevel Topology	Low Frequency	-Low Switching Losses -Lower Harmonic Output compared to traditional VSI -Easy implementation -Modular Structure	-High Harmonic output compared to CHB high switching modulation -High component count -High isolated dc sources count
	High Frequency	-Harmonics easier to filter -Small filter size	-High Switching Losses -Complex Control
	Hybrid Frequency	-Lower switching losses compared to CHB high frequency modulation	-Complex control of two different switching frequencies

complex control of two different switching frequencies. A trade-off always appears between harmonic content and switching frequencies in all types of VSIs. From earlier and later discussions about all types of power electronic filters and VSIs, a new filter topology is proposed which can be integrated to traditional VSI as will be conducted in the following chapters. This combination can be used to drive a.c. motors where the speed of the motors depends on the operating frequency of the inverter. The new filter topology tracks the change in the harmonic components location due to the change in the inverter's operating frequency. This topology opens a new field of developing the integration of inverters and filters in one system in order to get the desired harmonic content.

3.4 Summary

The points presented in this chapter focuses on the topologies and modulation schemes for H-bridge VSIs. It is composed of the operating principle, modulation technique, and harmonic content for each topology. This overview is very helpful from the point of view of recognizing the strength and weakness points in each topology and the associated modulation scheme. The discussion in chapters 2 and 3 has led to the proposal of the new output filter topology which aim to be integrated with VSIs. The following chapter conducts the principles behind the new filter design.

Chapter 4

The Switched Capacitor Circuit Applied to the Proposed Output Filter for Power Inverter

4.1 Introduction

In chapter 3, different inverter topologies were critically reviewed. In this chapter, the proposed filter which is used in conjunction with an inverter is presented. The new output filter aims to trace harmonic components where they appear in the harmonic spectrum. The present work is carried out in an open loop manner. The change of the harmonic spectrum can be a result of a change in the operating frequency of the inverter. In the traditional passive filters, fixed values of the tuning elements must be set in order to filter out a specific harmonic; however, the proposed technique allows the filter to tune at any desired harmonic automatically. This can be achieved by introducing the switched capacitor circuit, where the value of the tuned capacitance can be varied by controlling the duty cycles of the associated switches. The following sections discuss the fundamental operating principle of the switched capacitor circuits.

4.2 Switched Capacitor Circuit

Switched capacitor circuits (SCC) family varies according to the number of the implemented capacitors and switches [79,83]. An investigation of the main two topologies in the field of SCCs is presented in addition to other topologies conducted in literature. Upon this investigation, the desired topology is adopted showing the justification of that selection. The main topologies are Single Capacitor Double Switch

(SCDS), and Double Capacitor Double Switch. Overview of other topologies is presented including Single Capacitor Single Switch, and Triple Switch configuration.

4.2.1 Single Capacitor, Double Switch (SCDS) Circuit

Single capacitor double switch configuration is shown in Figure 4.1. It is composed of one capacitor (C), and two bidirectional semiconductor switches (S_1) and (S_2). The semiconductor switch S_1 is connected in series with a fixed capacitor C, and another switch S_2 connected in parallel with S_1 and C.

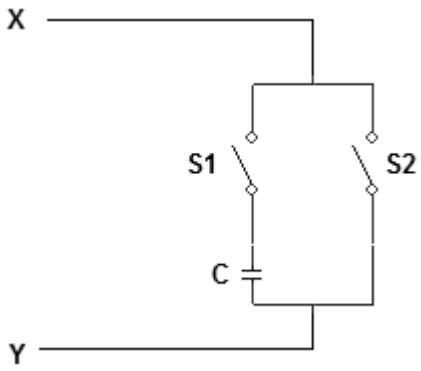


Figure 4.1 Single Capacitor Double Switch Circuit

The semiconductor switches can switch on or off at any time and allow the current to flow in any direction as well as it can operate at relatively high switching frequency (high enough to ensure smooth current but not so high in order to limit switching loss). This is discussed in more details in chapter 5. S_1 and S_2 operate in anti-parallel manor so that when S_1 is closed, S_2 is open and vice versa. The effective capacitance (C_{eff}) is the value of the capacitor measured across the terminals XY, as shown in Figure 4.1. The value of C_{eff} will be proven that it varies with varying the duty cycle of the semiconductor switches which introduces a variable capacitor. The capacitance value varies between the value of C at duty cycle (K_o)=1 and infinity at K_o=0. To derive the mathematical equations of SCDS operation, a current limiter is inserted to the circuit in

order to limit the transient current flowing through the semiconductor switches. The current limiter consists of an inductor in series with a small resistor which represents the internal resistance of the inductor as shown in Figure 4.2. When applying this circuit to the proposed output filter, a tuned inductor will be connected in series with the limiter inductor. In this case, one inductor is connected in the proposed filter which presents the summation of both inductors.

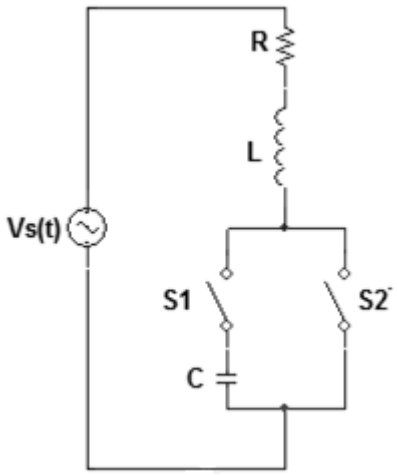


Figure 4.2 Single Capacitor Double Switch Circuit (SCDS) with inductor current limiter

In SCDS circuit both branches are connected alternately to the supply. One branch is composed of L, R, and C connected in series with S_1 during its conduction period (K_o=1). The other branch is composed of L and R connected in series with S_2 during its conduction period (K_o=0). The duty cycle "K_o" can have any value between 0 and 1. The voltage equations of these two branches are as follows, depending on the duty cycle, K_o of the switching element, S_1:

At K_o=0;

$$v_s(t) = i(t)R + L\,\frac{di}{dt} \tag{4.1}$$

At K_o=1;

$$v_s(t) = i(t)R + L\frac{di}{dt} + v_c(t) \tag{4.2}$$

and the instantaneous current, i(t) is given by:

$$i(t) = C\frac{dv_c}{dt} \tag{4.3}$$

If the supply voltage is given by:

$$v_s(t) = V_m \cos(\omega t + \emptyset) \tag{4.4}$$

The instantaneous value of the current, i_1 and i_2, for each case is found to be:

For K_o=0;

$$i_1 = I_{1m} \cos(\omega t - \varphi_1) \tag{4.5}$$

where

$$\varphi_1 = tan^{-1}\frac{\omega L}{R} \tag{4.6}$$

and

$$I_{1m} = \frac{V_m}{\sqrt{R^2 + \omega L^2}} \tag{4.7}$$

For K_o=1;

$$i_2(t) = I_{2m} \cos(\omega t - \varphi_2) \tag{4.8}$$

where

$$\varphi_2 = tan^{-1}\frac{(\omega L - \frac{1}{\omega c})}{R} \tag{4.9}$$

and

$$I_{2m} = \frac{V_m}{\sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}} \tag{4.10}$$

The steady state capacitor voltage, V_c is given by equation 4.11

$$V_c(t) = \frac{I_{2m}}{\omega c}\sin(\omega t - \varphi) \tag{4.11}$$

If R is adjusted so that $R \ll \omega L$ and $\ll {}^{1}/_{\omega C}$, the phase angles $\varphi_1$and φ_2 will be $\left(\frac{\pi}{2}\right)$

4.2.1.1 Switching Function Analysis of SCDS Circuit

The switching function theory [79] is defined as the process of the closing and opening state of the switches during an interval pattern. The switching state equals to 1 when the switch is turned on and zero when the switch is turned off. Figure 4.3 shows the switching function which takes the form of train of pulses.

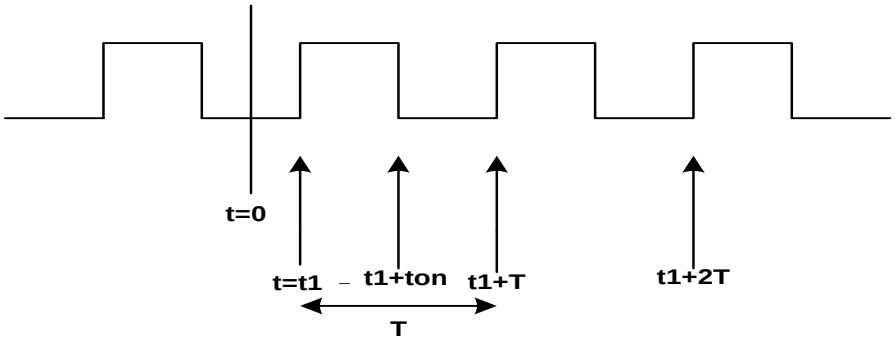


Figure 4.3 The Switching Function

The derivation of the effective capacitance is presented the following equation. If the switching frequency of S_1 and S_2 be f_s, where the period is T and the angular switching frequency ω_s, where;

$$T = \frac{1}{f_s} \tag{4.12}$$

and

$$\omega_s = 2\pi f_s \tag{4.13}$$

The angular duration of the unit value period is $2\pi K_o$ (radians), where K_o is the duty cycle, and the boundaries of the unit value period with respect to the time zero are 0 and $2\pi K_o$ (radians). From the definitions above, the switching function can be expressed as:

$$F(t) = \sum_{n=1}^{\infty} A_n \cos(n\omega_s t) + B_n \sin(n\omega_s t) \tag{4.14}$$

Calculating for the coefficients of Fourier expansion:

$$A_o = \frac{1}{T} \int_{t_1}^{t_1+t_{on}} F(t)\, dt = \frac{t_{on}}{T} = K_o \tag{4.15}$$

$$A_n = \frac{2}{T} \int_{t_1}^{t_1+t_{on}} F(t) \cos(n\omega_s t)\, dt = \frac{2}{nT\omega_s}\left[\sin\left(n\omega_s(t_1 + t_{on})\right)\right] - \sin[n\omega_s t_1] \tag{4.16}$$

$$B_n = \frac{2}{T}\int_{t_1}^{t_1+t_{on}} F(t)\sin(n\omega_s t)\,dt$$

$$= -\frac{2}{nT\omega_s}\left[\cos\left(n\omega_s(t_1+t_{on})\right)\right] - \cos[n\omega_s t_1] \quad (4.17)$$

By substituting equations 4.15, 4.16 and 4.17 in equation 4.14:

$$F(t) = K_o + \frac{2}{T\omega_s}\sum_{n=1}^{\infty}\frac{1}{n}\left[\sin\left(n\omega_s(t_1+t_{on})\right) - \sin(n\omega_s t_1)\cos(n\omega_s t)\right.$$
$$\left. - cos\left(n\omega_s(t_1+t_{on})\right) - \cos(n\omega_s t_1)\,sin(n\omega_s t)\right] \quad (4.18)$$

For the purpose of simplification, the switching instant is selected to be $t_1 = -(t_{on}/2)$ which will simplify and reduce equation 4.18 to:

$$F(t) = K_o + \sum_{n=1}^{\infty}\frac{4\sin\left(\frac{n\,t_{on}\,\omega_s}{2}\right)}{nT\omega_s}\cos(n\omega_s t) \quad (4.19)$$

Then by substituting the switching angular frequency ($\omega_s = 2\pi/T$) in equation 4.19:

$$F(t) = K_o + 2\sum_{n=1}^{\infty}K_n\cos(n\omega_s t) \quad (4.20)$$

For simplicity let:

$$\emptyset(t) = 2\sum_{n=1}^{\infty}K_n\cos(n\omega_s t) \quad (4.21)$$

Hence;

$$F(t) = K_o + \emptyset(t) \tag{4.22}$$

The later calculation of the switching function presents, F(t) of switch S_1. The switching function of switch S_2 will be the complementary function of S_1, F'(t), hence

$$F'(t) = 1 - (K_o + \emptyset(t)) \tag{4.23}$$

where n is an integer number, K_o is the duty cycle of the switch, $K_n = \sin(n \pi K_o/2)$, and ω_s is the angular switching frequency, ($\omega_s = 2\pi fs$).

The voltage across the inductor in Figure 4.2 is given by:

$$v_L(t) = L\frac{d}{dt}[F(t).i(t)] + L\frac{d}{dt}[F'(t).i(t)] = L\frac{d}{dt}[F(t).i(t) + F'(t).i(t)] \tag{4.24}$$

Substituting F(t)+F'(t)=1, then:

$$v_L = L\frac{d}{dt}i(t) \tag{4.25}$$

Similarly the voltage across the resistor is given by:

$$v_R(t) = R.i(t) \tag{4.26}$$

The voltage across points XY, as shown in Figure 4.1, is given by:

$$v_{XY} = F(t).v_c(t) \tag{4.27}$$

where;

$$v_c(t) = \frac{1}{c}\int_0^t F(t).i(t)dt \tag{4.28}$$

Expanding the proceeding equation into:

$$v_c = \frac{1}{C}\int_0^t [K_o + \emptyset(t)]\, i(t)d(\omega t)$$
$$= \frac{1}{C}\int_0^t K_o i(t)d(\omega t) + \frac{1}{C}\int_0^t \emptyset(t) i\,(t)d(\omega t) \tag{4.29}$$

The first term under the first integral, $K_o i(t)$, contains only the frequency components of the current i(t) through the SCDS filter branch. Hence, the current flowing through SCDS circuit is adequately presented by the fundamental frequency components as shown below:

$$i(t) = i_1 \sin(\omega t - \theta_1) \tag{4.30}$$

The second term in equation 4.29, Ø(t) i(t), leads to high frequency components of current since the switching frequency is relatively high (> 5kHz) according to:

$$\omega_s \pm \omega,\ \omega_s \pm 3\omega,\ \omega_s \pm 5\omega \tag{4.31}$$

High frequency components of current create low values of fixed capacitor voltage at these frequencies. Naturally, the frequency components of capacitor voltage can be approximated to the same order of components as the current. Hence the second part of equation 4.29 can be ignored as given by:

$$v_c(t) = \frac{1}{C}\int_0^t [K_o i(t) d(\omega t)] \tag{4.32}$$

Replacing equation 4.30 for i(t) as given by:

$$v_c(t) = \frac{1}{C}\int_0^t [K_o i(t) d(\omega t)]$$
$$= -K_o\left[\frac{i_1}{\omega C}\cos(\omega t - \theta_1)\right] \tag{4.33}$$

The voltage across the SCDS combination, $V_{XY}(t)$ as shown in Figure 4.1 is given by [79]:

$$v_{XY}(t) = \frac{F(t)}{C}\int_0^t [K_o\, i(t) d(\omega t)]$$

$$= [K_o + \emptyset(t)]\left[-K_o\left[\frac{i_1}{\omega C}\cos(\omega t - \theta_1)\right]\right]$$

$$= [-K_o^2]\left[\frac{i_1}{\omega C}\cos(\omega t - \theta_1)\right] \ldots . First\ term$$

$$[-\emptyset(t)K_o]\left[\frac{i_1}{\omega C}\cos(\omega t - \theta_1)\right] \ldots\ldots\ldots\ldots Second\ term \tag{4.34}$$

The first term in equation 4.37 contains the fundamental frequency components as the current flow through the SCDS circuit. The second term contains frequency components at much higher frequencies, determined by the switching frequency.

$$\omega_s \pm \omega,\ \omega_s \pm 3\omega,\ \omega_s \pm 5\omega \tag{4.35}$$

These terms are close to the switching frequency and are relatively of high order. They cannot give rise to high currents at these frequencies because of the presence of L. Hence due to the high switching frequency, ω_s, the first term is considered in the derivation of the voltage of filter which contains the fundamental frequency component.

Hence the voltage equation of the circuit can be rewritten as follows:

$$v_s(t) = R.i(t) + L\frac{d}{dt}\ i(t) + \frac{1}{C}\ F(t)\int_0^t F(t).\ i(t)dt \tag{4.36}$$

By assuming that $R << X_c$ and $R<<X_L$, then the resistive term in equation 4.36 can be neglected, therefore the voltage equation can be rewritten as:

$$v_s(t) = L\frac{d}{dt}\ i(t) + \frac{1}{C}\ F(t)\int_0^t F(t).i(t)\ dt \tag{4.37}$$

From the previous argument, equation 4.34, the switching frequency is chosen to be > 5 kHz. Equation 4.34 can be simplified for the fundamental components only as follows:

$$v_s(t) = [K_o X_c - X_L]\, i(t) \tag{4.38}$$

where X_c and X_L are the capacitance and inductance reactance calculated at the supply frequency. The assumption of f_s > 5 kHz is justified in the base that it should be high enough so that i(t) is smooth and free from low order harmonics. The peak value of the voltage across the circuit (V_{XY}) is given in terms of total branch reactance by:

$$\hat{V}_{XY} = K_o^2 X_c\, \hat{I} \tag{4.39}$$

Since the effective capacitive reactance is given by:

$$X_{Ceff} = \frac{\hat{V}_{XY}}{\hat{I}} \tag{4.40}$$

Substituting equation 4.40 in equation 4.39, the effective capacitance reactance can be calculated as follows:

$$X_{Ceff} = K_o^2\, X_c \tag{4.41}$$

Hence;

$$C_{eff} = \frac{C}{K_o^2} \tag{4.42}$$

From the preceding mathematical analysis of the SCDS, it is clear that this circuit can be used as a variable capacitor. At K_o=1, the capacitor branch is completely out of the circuit hence the circuit has zero capacitance. At K_o=0, the capacitor branch is fully in and the circuit has a fixed capacitor. The value of the fixed capacitor start to change from K_o=1, and increasing gradually with the reduction of K_o in an exponential manner, as shown in Figure 4.4.

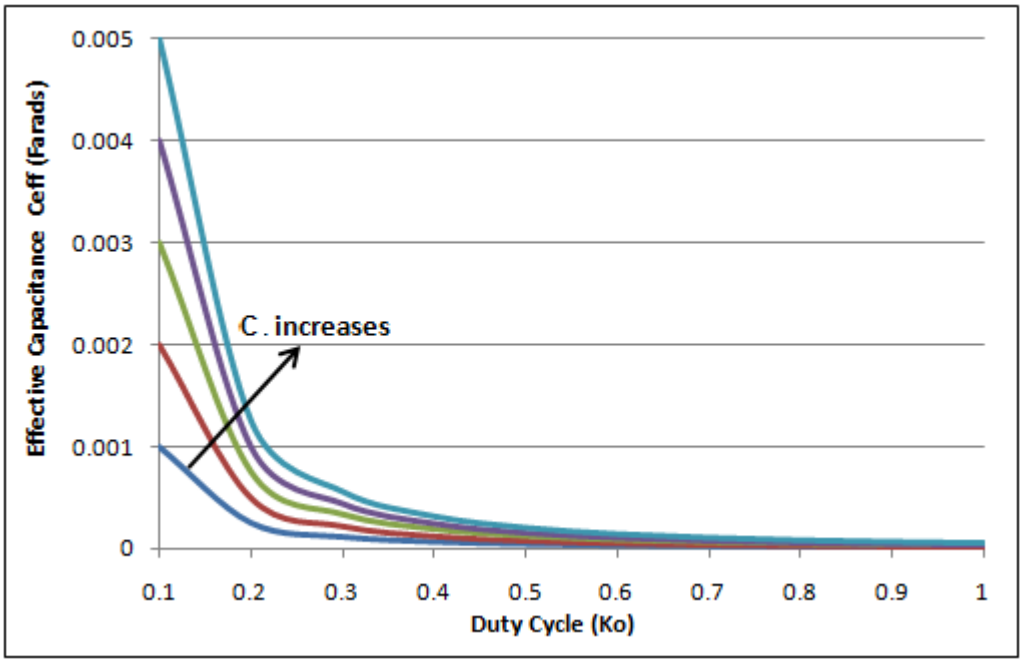


Figure 4.4 Relation between duty cycle, and effective capacitance of SCDS circuit

4.2.2 Double Capacitor, Double Switch (DCDS) Circuit

The second main topology of SCCs, is the Double capacitor Double Switch (DCDS) circuit as shown in Figure 4.5. In this configuration, two branches of fixed capacitors, C_1 and C_2, connected in series with two bidirectional semiconductor switches for each capacitor branch, S_1 and S_2, respectively.

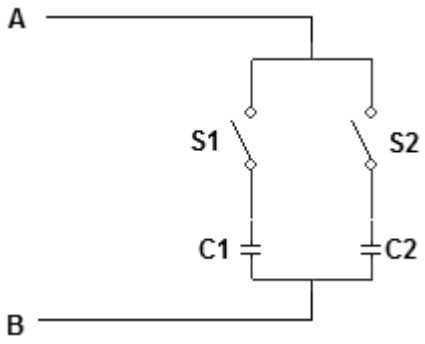


Figure 4.5 Double Capacitor Double Switch Circuit

The principle of operation of this circuit is the same as SCDS, where S_1 and S_2 operate in anti-parallel manor so that when S_1 is closed, S_2 is open and vice versa. Also, the effective capacitance is measured across the terminals AB, as shown in Figure 4.5. This circuit has the ability to operate as a variable capacitor by varying the duty cycle of the semiconductor switches. The limiting current inductor is inserted as in the case of SCDS circuit as shown in Figure 4.6. The derivation of the relation between the duty cycle and the effective capacitance across terminals A and B is similar to that in SCDS, the only difference is the introduction of two capacitors, C_1 and C_2, instead of one.

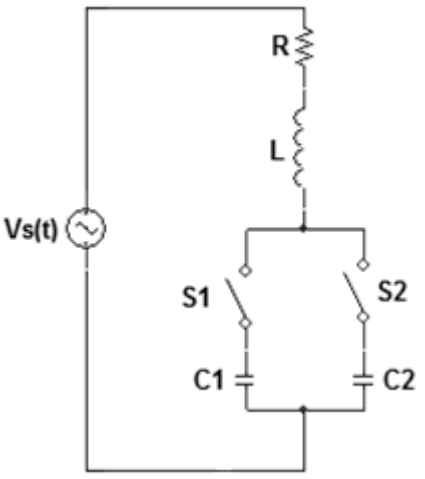


Figure 4.6 Double Capacitor Double Switch Circuit

This circuit replaces the fixed tuned capacitor in the proposed output filter. The derivation of C_{eff} with respect to duty cycle of S_1 which is in series with C_1 will be presented in the following mathematical analysis. By adopting the same approach used in SCDS analysis, the voltage equations for DCDS can be written according to Figure 4.6.

Referring to C_2 branch, and at K_o=0, the voltage equation for this branch as follows:

$$v_s(t) = i(t)R + L\,\frac{di}{dt} + v_{c1}(t) \tag{4.43}$$

While at K_o=1, the voltage equations is given as follows:

$$v_s(t) = i(t)R + L\,\frac{di}{dt} + v_{c2}(t) \tag{4.44}$$

The flowing currents through the circuit at K_o=0 and K_o=1, respectively are:

$$i(t) = c_1\frac{dv_{c1}}{dt} \tag{4.45}$$

$$i(t) = c_2\frac{dv_{c2}}{dt} \tag{4.46}$$

The voltage across DCDS circuit as shown in Figure 4.5, referring to branch C_1 and branch C_2, are given in equations 4.47 and 4.48, respectively :

$$\hat{V}_{AB} = [K_o^2\,X_{c1} + (1-K_o)^2\,X_{c2}]\;\hat{I} \tag{4.47}$$

$$\hat{V}_{AB} = [K_o^2\,X_{c2} + (1-K_o)^2\,X_{c1}]\;\hat{I} \tag{4.48}$$

Referring to equation 4.40 in branch C_1:

$$X_{Ceff} = \frac{\hat{V}_{AB}}{\hat{I}} = [K_o X_{c1} + (1 - K_o)^2 X_{c2}] \tag{4.49}$$

where, X_{ceff} is the effective capacitive reactance for DCDS circuit, as shown in Figure 4.6.

$$\frac{1}{\omega C_{eff}} = K_o^2 \frac{1}{\omega C_1} + (1 - K_o)^2 \frac{1}{\omega C_2} \tag{4.50}$$

From which;

$$\frac{1}{C_{eff}} = K_o^2 \frac{1}{C_1} + (1 - K_o)^2 \frac{1}{C_2} \tag{4.51}$$

$$\frac{1}{C_{eff}} = \frac{K_o^2 C_2 + (1 - K_o)^2 C_1}{C_1 C_2} \tag{4.52}$$

Equation 4.53 shows the effective capacitance C_{eff} in terms of both capacitors of the two branches and the duty cycle of C_1 by taking the reciprocal of equation 4.52:

$$C_{eff} = \frac{C_1 C_2}{K_o^2 C_2 + (1 - K_o)^2 C_1} \tag{4.53}$$

Dividing both the numerator and the denominator of equation 4.53 by C_1, the C_{eff} is given as follows:

$$C_{eff} = \frac{C_2}{K_o^2 \frac{C_2}{C_1} + (1 - K_o)^2} \tag{4.54}$$

For simplification, let;

$$\gamma = \frac{C_2}{C_1} \tag{4.55}$$

Substituting equation 4.55 in equation 4.54, the equation is given by:

$$C_{eff} = \frac{C_2}{\gamma K_o^2 + (1 - K_o)^2} \tag{4.56}$$

Dividing the numerator and denominator by γ, the final derived equation for calculating the effective capacitance, referring to branch C_1, as the duty cycle is given as follows:

$$C_{eff} = \frac{C_1}{K_o^2 + \frac{1}{\gamma} (1 - K_o)^2} \tag{4.57}$$

From the above derivation, the C_{eff} of the DCDS circuit can be calculated using equations 4.56 and 4.57, where the duty cycle is for the switch in series with C_1. Figure 4.7 illustrates the relation between the effective capacitance and the duty cycle of S_1 for different values of γ, using equation 4.56.

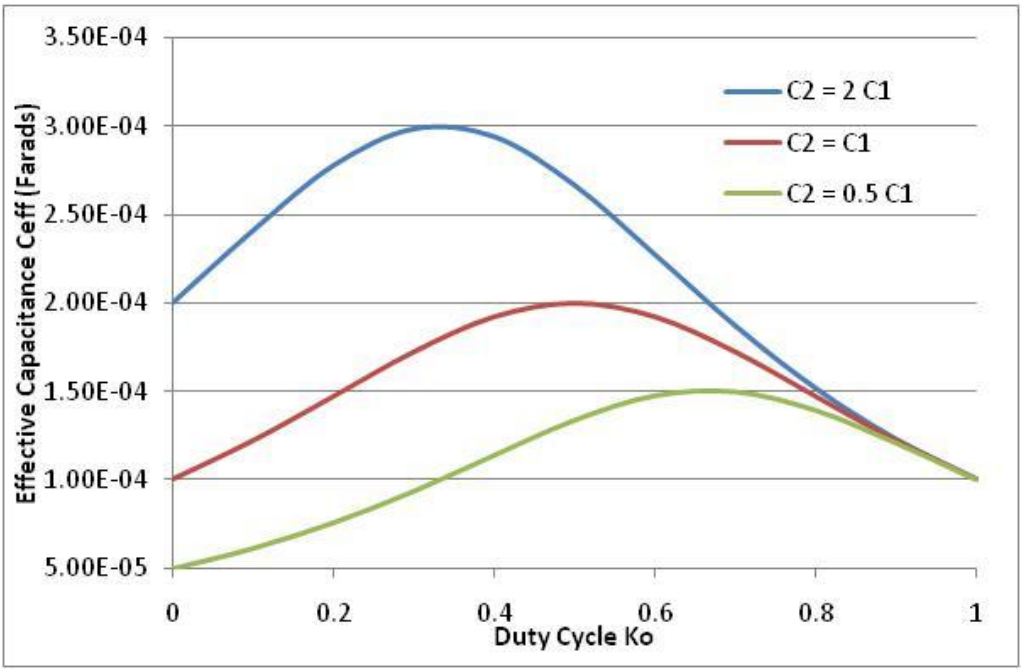


Figure 4.7 Relation between duty cycle, and effective capacitance of DCDS where the duty cycle is for S1

A second case can be approached in deriving C_{eff} with respect to the duty cycle of S_2 which is in series with C_2. Referring to equation 4.48, the derivation follows the same sequence implemented in the first case:

$$X_{Ceff} = \frac{\hat{\hat{V}}_{AB}}{\hat{I}} = [K_o^2 X_{c2} + (1 - K_o)^2 X_{c1}] \tag{4.58}$$

$$\frac{1}{\omega C_{eff}} = K_o^2 \frac{1}{\omega C_2} + (1 - K_o)^2 \frac{1}{\omega C_1} \tag{4.59}$$

$$\frac{1}{C_{eff}} = K_o^2 \frac{1}{C_2} + (1 - K_o)^2 \frac{1}{C_1} \tag{4.60}$$

$$\frac{1}{C_{eff}} = \frac{K_o^2 C_1 + (1 - K_o)^2 C_2}{C_1 C_2} \tag{4.61}$$

By taking the reciprocal of equation 4.59, it becomes:

$$C_{eff} = \frac{C_1 C_2}{K_o^2 C_1 + (1 - K_o)^2 C_2} \tag{4.62}$$

Dividing equation 4.62 by C_2:

$$C_{eff} = \frac{C_1}{\frac{1}{\gamma} K_o^2 + (1 - K_o)^2} \tag{4.63}$$

Then, Dividing by γ, the final equation becomes:

$$C_{eff} = \frac{C_2}{K_o^2 + \gamma(1 - K_o)^2} \tag{4.64}$$

The effective capacitance in the second case can be calculated using equations 4.63 and 4.64, where the duty cycle is for switch S_2 which is in series with C_2. Figure 4.8 illustrates the relation between C_{eff} and the duty cycle of S_2 for different γ.

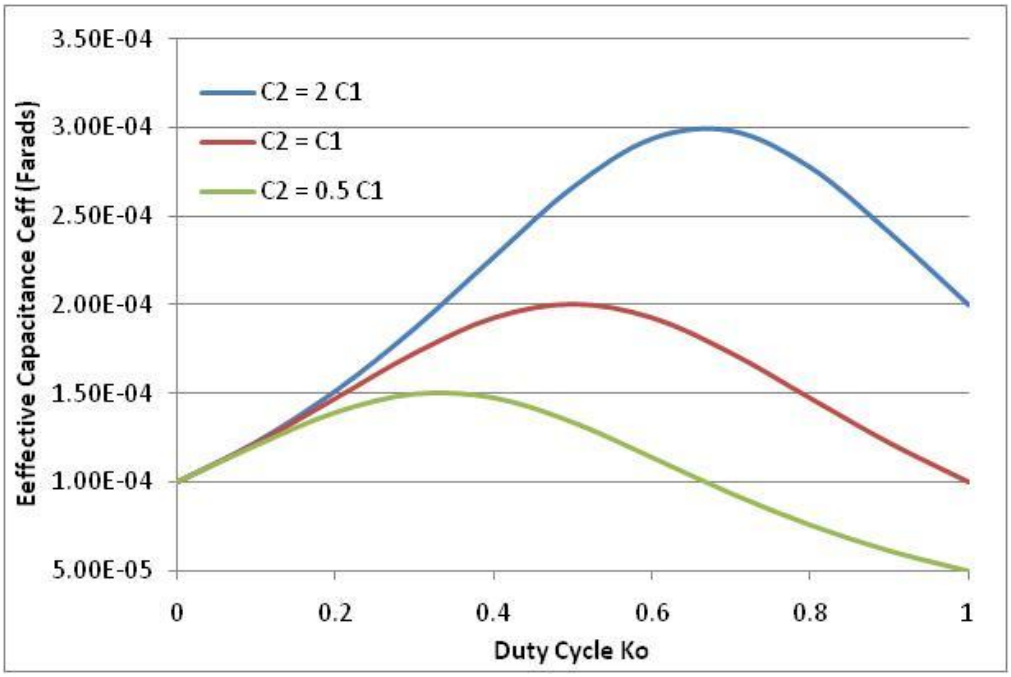


Figure 4.8 Relation between duty cycle, and effective capacitance of DCDS circuit where the duty cycle is for S2

According to the behavior of this topology as a variable capacitor, it has the ability to vary the value of the capacitor by controlling the duty cycle of either S_1 or (the complementary S_2). This has the capability of getting the desired C_{eff}. This feature can be at the expense of inserting an additional component, extra capacitor in the case of DCDS. The maximum achieved effective capacitance can reach the sum of both fixed capacitors.

4.3 Other Topologies of Switched Capacitor Circuit

In the following sections, other topologies of the switched capacitance circuit are conducted briefly which were presented in [79]. These topologies include Single Capacitor Single Switch (SCSS), and Triple SCC configurations. This presentation of these topologies in addition to the previous conducted configuration aims to justify the selection of the appropriate SCC circuit to be implemented in the proposed new output filter for power inverters.

4.3.1 Single Capacitor, Single Switch (SCSS) Circuit

The circuit consists of a bidirectional switch (S) connected in parallel with a fixed capacitor (C) as shown in Figure 4.9. The overall combination is connected in series with an inductor (L). This topology is considered as the simplest circuit in construction and operation amongst SCCs family, both in number of components and in control complexity.

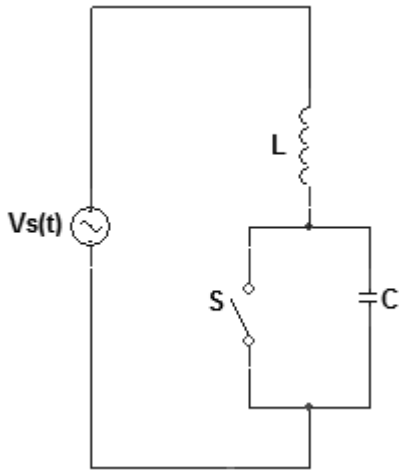


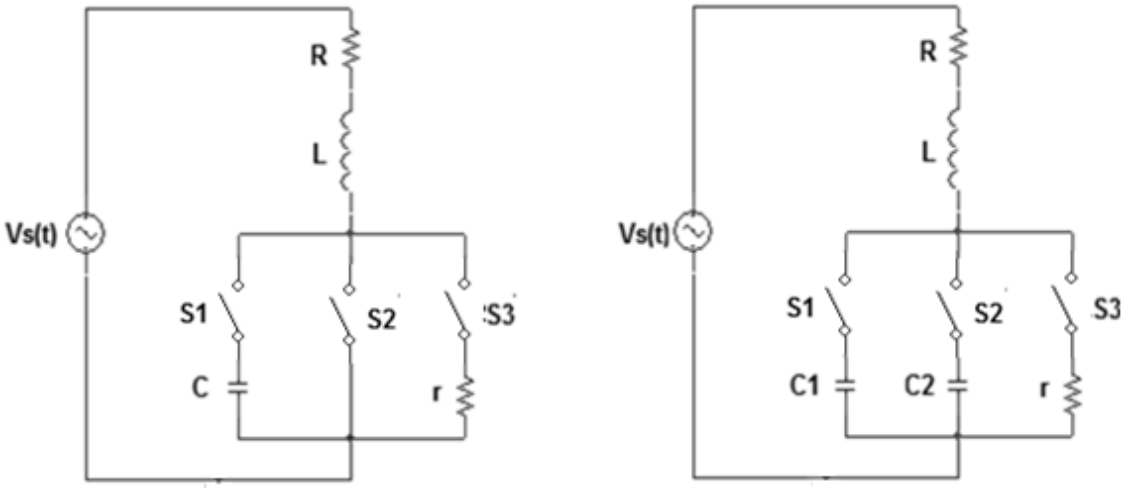
Figure 4.9 Single Capacitor Single Switch Circuit with inductor current limiter

In this circuit in order to avoid short circuiting the capacitor, the switch S can only be switched when the voltage across C is zero. Hence this circuit is limited at f_s. In practice, the switch must be closed when the voltage of the capacitor is very small or close to zero in order to let the capacitor to charge and discharge through the series inductor. The line current of this circuit is rich in harmonics due to the low switching frequency operation of the semiconductor switches compared to other SCCs which is considered as a serious drawback.

4.3.2 Triple Switch SCC Configurations

The introduction of triple configuration in the field of SCCs is due to the short circuit condition which is noticed during the transition between turning on and off the anti-parallel switches in the earlier conducted circuits, SCDS, and DCDS. This topology includes inserting a third branch consists of a switch in series with a resistor as shown in Figure 4.10 for SCDS, and DCDS circuits. In the previous SCDS and DCDS, its assumed that the two switches, S_1 and S_2, open and close instantaneously, however the switching devices take a finite time to change from one state to another. Therefore,

during the transition action between S_1 and S_2, there is a very short period where both switches are closed. During this small finite period the capacitor are short circuited and the switches are subjected to destructive surge currents.



(a) (b)

Figure 4.10 Triple Switched Capacitor Circuits configurations, a: SCDS, and b: DCDS

The third branch introduces a dead period when the two switches associated with the capacitors are open for a short circuit. The resistor (r) in the third branch provides smooth transfer of current from one branch to another. This topology has the advantage of operating the two switches SCCs configurations with protecting the semiconductor switches from dangerous surge currents during the transition instant of the switches. However, additional components are added to these circuits which introduce more switching losses due to their intrinsic characteristic of switching at high frequency.

4.4 Selection Criteria of SCC for the Proposed Output Filter

The SCC topologies were investigated fully and the required one should fulfill the following criteria:

1- Variable capacitor behavior

2- Harmonic output

3- Switching losses

4- Components count

The introduction of the new output filter for power inverters have to address the above criteria, which provide the filtering performance with minimum drawbacks compared to traditional passive output filters. The SCCs have to provide a variable capacitance by controlling the duty cycle of the associated switches. This feature discriminate the well-known bank of capacitor switch, which connects a capacitor to a circuit using mechanical switches, from the use of controlled semiconductor switches. The main aim of harmonic filters is to eliminate or reduce the unwanted distortion in the system. This shows clearly that the selected SCC must not inject harmonics to the system. If the SCC generates extra harmonics, its application in the filtering field will not be feasible. This means that the SCC should operate at high switching frequency, high enough so that it does not generate low order harmonics and low enough so that it does not consume high switching loss. In this case, a compromise between the harmonic output of the SCC and its switching losses must be taken into account. Also, the use of a minimum number of components, including switches, reduces the effect of switching losses and meets the size, cost and packaging requirements. The criteria set from one to four according to their importance for the author to design the new filter topology which is essential to apply any compromise between the circuits if needed.

Table 4-1 Comparison between Switched Capacitor Circuits for the Selection Criteria

SCC Topology	Selection Criteria	Suitability Comments
Single Capacitor, Single Switch (SCSS)	-Variable Capacitor -High Harmonic Output -Low Losses (f_s = 100 Hz) -Component Count (4)	-Not Suitable for filtering due to high harmonic distortion which is a major limit -Low switching losses -Low number of components
Single Capacitor, Double Switch (SCDS)	-Variable Capacitor in one setting -Low Harmonics -High Losses (f_s > 5 kHz) -Component Count (5)	-Suitable for filtering with low harmonic distortion is attractive -High switching losses is a drawback -Medium number of components - Not suitable for high power application
Double Capacitor, Double Switch (DCDS)	-Variable Capacitor in two settings -Low Harmonics -High Losses (f_s > 5 kHz) -Component Count (6)	-Suitable for filtering with low harmonics and flexibility in achieving variable capacitance -High switching losses is a drawback -Medium/High number of components
Triple Configurations for SCDS/DCDS	-Variable Capacitor in (one/two) setting -Low Harmonics -High Losses (f_s > 5 kHz) -Component Count (7/8)	-Same Suitability comments in SCDS and DCDS (Harmonics and Losses) -High number of components -Add control complexity -Essential for high power application

Table 4-1 illustrates a comparison between SCCs in term of the selection criteria and the suitability comments set in this thesis. It is clearly seen that a compromise is needed for appropriate selection of the suitable circuit for the new filtering technique. SCSS does not fulfill the most important feature where it suffers from poor spectral performance. On the other hand, SCDS and DCDS, shows a tremendous merits in terms of harmonic distortion. This is due to the switching frequency which causes high switching losses in the system. In terms of components count, the triple configuration suffers severely with eight components and complex control due to the introduction of the third switch branch as discussed earlier in this chapter, however it is essential for high power applications due to the absence of the overlap and dead zone switching problem. This led to the fact that the attractive topologies for harmonic filtering are SCDS and DCDS. This comparative study guided the author to select SCDS for the proposed filter design due to the close feature similarity of it with DCDS as well as the proposed filter will be implemented in low power applications. However, the selected one has the same performance in achieving the desired capabilities with less components count.

4.5 Summary

In this chapter four switched capacitor circuits were analysed for the aim of selecting the appropriate topology for the proposed output filter. A comprehensive mathematical analysis is implemented on SCDS, and DCDS showing their capability to act as a variable capacitor. The relation between the effective capacitance and the duty cycle is presented for both circuits. An overview of other topologies of SCCs is presented as well. A selection criterion is set by the author to provide an accurate guidance for adopting the appropriate SCC for the proposed filtering technique. This led

to a comparative analysis showing each topology and its ability to meet the criteria and the suitability comments assessed by the author. The result showed that SCDS circuit has a distinct superiority amongst other topologies. In the following chapter, the proposed output filter is discussed showing the simulation results, and the validation of this circuit is proved and compared with traditional output filter from several points of view.

Chapter 5

Simulation Modelling and Implementation of the Proposed Single Capacitor Double Switch Filter

5.1 Introduction

Review of harmonic filters was discussed in Chapter 2, focusing on passive power filters, where the characteristic of the available topologies is presented. Most of the configurations of passive filters have fixed parameters to filter out a specific and/or range of harmonic components. An exception has been shown in a variable inductor topology which is controlled using Thyristor Controlled Reactor (TCR) constructed from low frequency thryristor switches. The drawback associated with TCR is presented and discussed earlier in Chapter 2. This led the author to introduce a new topology of tuned passive output filter for power inverters by modifying the existing configuration of traditional tuned filter. Traditional square wave H-bridge VSI has been adopted for the application of the new filter as conducted in Chapter 3. The majority of the available tuned passive filter employs a fixed parameters configuration. The proposed topology includes the introduction of an appropriate switched capacitor circuit which is selected according to strict criteria was shown in the previous chapter. The first section of this chapter presents the simulation modelling and the choice of the appropriate software for this purpose. Simulation results of the circuit performance are also presented in the course of this chapter. The second section presents the implementation of SCDS circuit examining the effective capacitance-duty cycle relationship. Also, experimental results are shown for harmonic reduction in both the traditional and the proposed tuned passive filters.

5.2 Computer Simulation Modelling of SCDS Tuned Output Filter

Most studies concerning power electronic filters and its application with power electronic converters are simulated computationally using special purpose software. These simulation packages are very useful in studying circuit design; however, some of them have drawbacks. Several simulation studies have been done using circuit-based languages such as SPICE (i.e. Orcad PSPICE, PSim, Multisim, etc.) and Matlab (i.e. M-file and Simulink) in order to establish power electronic circuits model at the component level [80]. SPICE stands for Simulation Program with Integrated Circuit Emphasis which shows that this type of software is superior in accurate modelling of the electrical and the electronic components of power electronic circuits. Matlab-based power electronic models have the advantages of open environment which has the capability of interacting with many languages such as C language and it can act as an interface for digital electronic hardware such as PIC Microcontrollers and DSPs. However, SPICE package (Orcad PSPICE) is used in this research due its sole purpose and speciality in designing and simulating power electronic circuits. In addition, this software provides a comprehensive library of power components (i.e. Power switches) which are classified according to the manufacturer. Due to the aforementioned reasons, PSPICE package is adopted in simulating the proposed SCDS tuned output filter.

5.2.1 Orcad PSPICE Software

The modelling and simulation of the proposed filter has been carried out using PSPICE software , which provides a friendly environment to model the power inverter integrated with the new filter. Figure 5.1 shows the designed model using PSPICE package. The software includes a schematic circuit modeller which permits the user to construct the circuit using active (i.e. switches) and passive (resistors, capacitors, etc.)

power components. Moreover, a simulator manager is integrated with the schematic design environment in order to simulate voltage and currents at the desired terminals. It allows the selection of electronic devices according to the manufacturer's part number. No limitation is observed with respect to the research purpose, however, an interaction with Matlab is desirable in order to achieve the advantages of both SPICE model with respect to precise selection of electronic components and the Matlab with respect to control schemes.

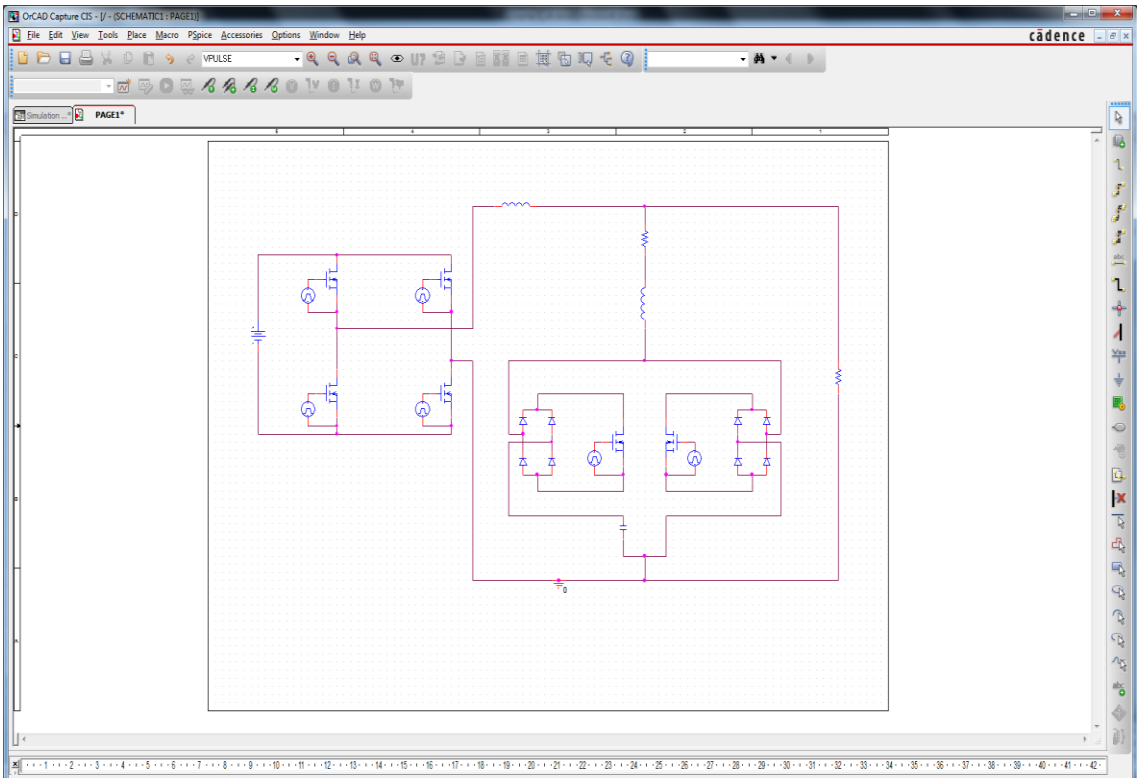


Figure 5.1 Circuit Modeling using Orcad Pspice Software

5.2.2 Parameters and Components of the Simulated Model

The components of the simulation model are taken from the internal library in PSPICE. MOSFET switches configured in bidirectional manner using diodes are implemented for the SCDS circuit. Each switch is connected across a diode rectifier in order to conduct in positive and negative half cycles. A battery is used as a DC source of the VSI.

Table 5-1 Proposed Filter Parameters

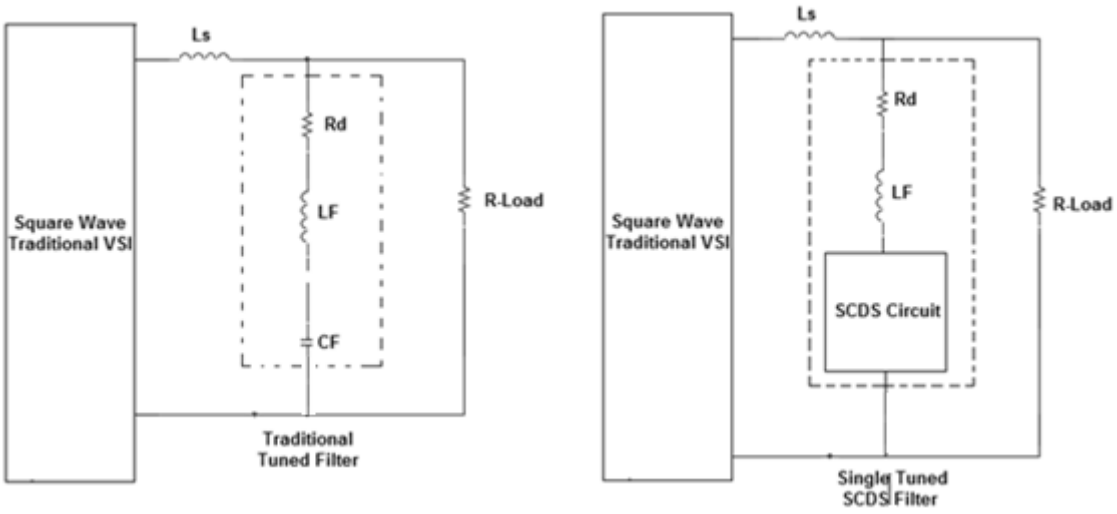
Parameter	Symbol	Value
Inverter Input Voltage	V_{dc}	12 volts
Tuned Inductor	L_F	0.3mH at f_o=150Hz
Inductor Resistance	r	1Ω
SCDS Fixed Capacitor	C	5μF
Resistive Load	R	10Ω

Also, the switching pattern of the associated switches is designed and fed the switches through a pulse generator for both the inverter and SCDS circuit. Passive components such as resistors, inductors and capacitors are inserted to the system from the software's library. Table 5-1 illustrates the parameters used for simulation work.

5.2.3 Single Tuned Output Passive Filter for Traditional VSI

The proposed single tuned filter circuit is based on the traditional single tuned passive filter (Figure 5.2a) with the introduction of the switched capacitor circuit inserted in series with the tuned inductor as shown in Figure 5.2b. Topologies of switched capacitor circuits, which were discussed and analyzed in chapter 4, led the author to adopt the single capacitor double switch configuration for the new proposed

filter. The new topology is simulated and the results of the simulation are presented in the following sections. Moreover, a comparison between the traditional and the proposed filter is presented based on the simulation results of both circuits. As mentioned earlier in chapter 4, for the selection criteria considerations, other topologies of switched capacitor circuits which do not meet the requirements are not considered.



(a) (b)

Figure 5.2 A schematic overview of (a) the Traditional Single Tuned and, (b) the Proposed Single Tuned SCDS filter

The main aim of this chapter is to study the effect of the proposed filter circuit on compensating current harmonics and its ability to trace specific harmonic components. It was stated before, in chapter 2, that single tuned passive filter operates either with fixed tuned elements or with variable tuned inductor. The proposal of new topology for variable tuned passive filter because of the drawbacks associated with the tuned inductor which was presented previously in chapter 2. As a matter of fact, changing the tuned capacitance value means that the filter can compensate a specific harmonic even if the location in the frequency spectrum is changed. This is useful in inverter applications under variable operating frequency environment. The proposed

filter has shown an achievement of the advantage of both current harmonic compensation and harmonic traceability enhancement compared to TCR filter. For this purpose, comparison is being held between the harmonic reduction performance from the traditional single tuned filter (Figure 5.2a) without inserting the switched capacitor circuit and after the insertion process (Figure 5.2b).

5.2.4 Single Capacitor Double Switch Tuned Output Passive Filter

The switched capacitance circuit is inserted in series with the tuned inductor; the circuit consists of a single capacitor connected in series with a semiconductor switch in order to form one branch. This branch is connected in parallel with a semiconductor switch as shown in Figure 5.3. The parallel resistor with the whole system represents the resistive load. The value of the fixed capacitor (C) is selected to be 5μF as will be explained in the following sections.

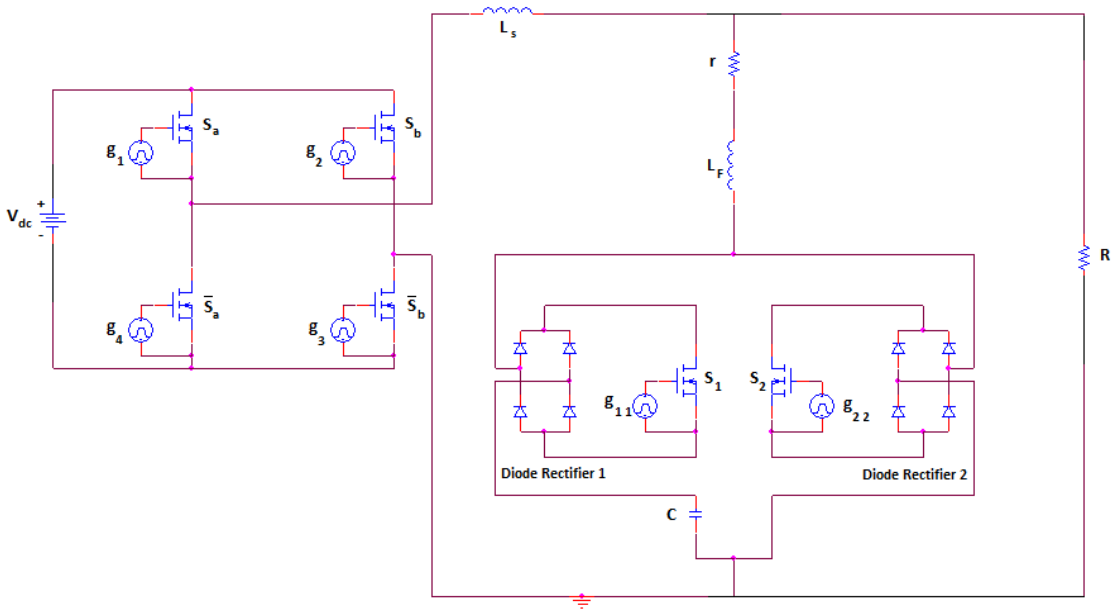


Figure 5.3 Proposed Single Tuned Filter utilizing Single Capacitor Double Switch circuit

5.2.4.1 Switching Strategy

In order to hold a valid comparison between the traditional single tuned filter and the proposed filter, the switching pattern of the SCC switches is designed so that the resulting effective capacitance of the circuit tuned with the inductor to track the variation of a specific harmonic component by controlling the duty cycles of the SCC switches (i.e. K_o=0.1, 0.2, etc..).

5.2.4.2 Calculation of the Effective Capacitance

From the above discussion, the tuned inductance value must satisfy the requirement of the resonation with the effective capacitance generated by the SCC. This led to the fact that the relation between the tuned inductor and the tuned effective capacitance, C_{eff}, can be calculated from equation 5.1 which represents the resonance frequency of an RLC series circuit:

$$f_r = \frac{1}{2\pi\sqrt{L_F C_{eff}}} \tag{5.1}$$

where; f_r is the resonance frequency at specific harmonic frequency, from which, C_{eff} can be found from the following equation:

$$C_{eff} = \frac{1}{2\pi L_F f_r^2} \tag{5.2}$$

5.2.4.3 Calculation of the Duty Cycle

For the single capacitor double switch circuit, the duty cycle is found from equation 4.42 as:

$$C_{eff} = \frac{C}{K_o^2} \tag{5.3}$$

In the proceeding equation, in order to calculate for the duty cycle, K_o, the value of the fixed capacitor, C, has to be set. The switching strategy is based on varying the fixed capacitance value in order to tune with the series inductor which means that the duty cycle is continuously changing to keep the resonation phenomena active for the sake of harmonic compensation.

5.2.4.4 Determining the Value of the Fixed Capacitor

The value of the fixed capacitor (C) is a major factor of determining the duty cycle and the effective capacitance. The duty cycle of the semiconductor switch controls the effective capacitance needed to resonate with the series tuned inductor. The fixed capacitor can be found as:

$$K_{o\,min} = \sqrt{\frac{C}{C_{eff\,max}}} \tag{5.4}$$

$$C = C_{eff\,max} \,.\, K_{o\,min}^2 \tag{5.5}$$

For example, if the required range of C_{eff} is 500µF. This should be associated to the minimum value of K_o=0.1 ($C_{eff\text{-}max}$ and $K_{o\text{-}min}$). As the duty cycle increases, the effective

capacitance value approaches the value of the fixed capacitor. In this case, putting C_{eff} = 500μF and K_o=0.1 in equation 5.5 will result in a fixed value of C equals to 5μF. The value of the fixed capacitor depends on the desired minimum and maximum effective capacitance in order to resonate with the series tuned inductor within the desired range of the effective capacitance values. The selection of the needed range depends on the harmonic frequency in the spectrum and its variation in the location. In this research work, the value of the fixed capacitor is set as 5 μF, which is able to track various harmonic components when the operating frequency of the inverter changes from 150 Hz to 950 Hz.

5.2.5 Simulation Results of the SCDS Filter Circuit

The proposed SCDS filter circuit is simulated using Orcad PSPICE software package. The associated results with this circuit focus on several aspects in this thesis. They can be divided as follows:

5.2.5.1 Tuned Effective Capacitance Traceability Performance

The proposed SCDS filter aim to trace specific harmonic components at different inverter output frequencies. Figures 5.4 and 5.5 show the desired tuned effective capacitance in terms of the variation of both inverter output frequency and the harmonic order components theoretically and computationally, respectively. It is shown that the tuned effective capacitance variation is controlled by the duty cycle of the associated switch in SCDS circuit. For instance, the 3^{rd} harmonic component (harmonic order = 3) is traced by the effective tuned capacitance in order to provide the resonation with the tuned inductor for the sake of allowing a low impedance path through the filter. Similarly, the same performance is applied to the 3^{rd}, 5^{th}, 7^{th},.....19^{th}.

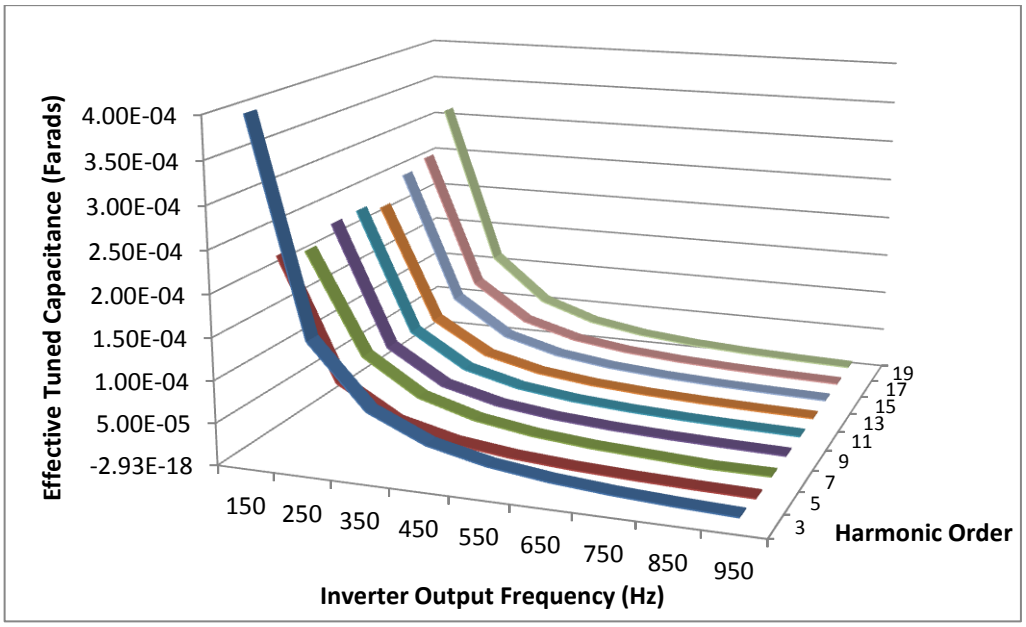


Figure 5.4 Tuned Effective Capacitance in term of inverter output frequency and harmonic component order (Theoretical)

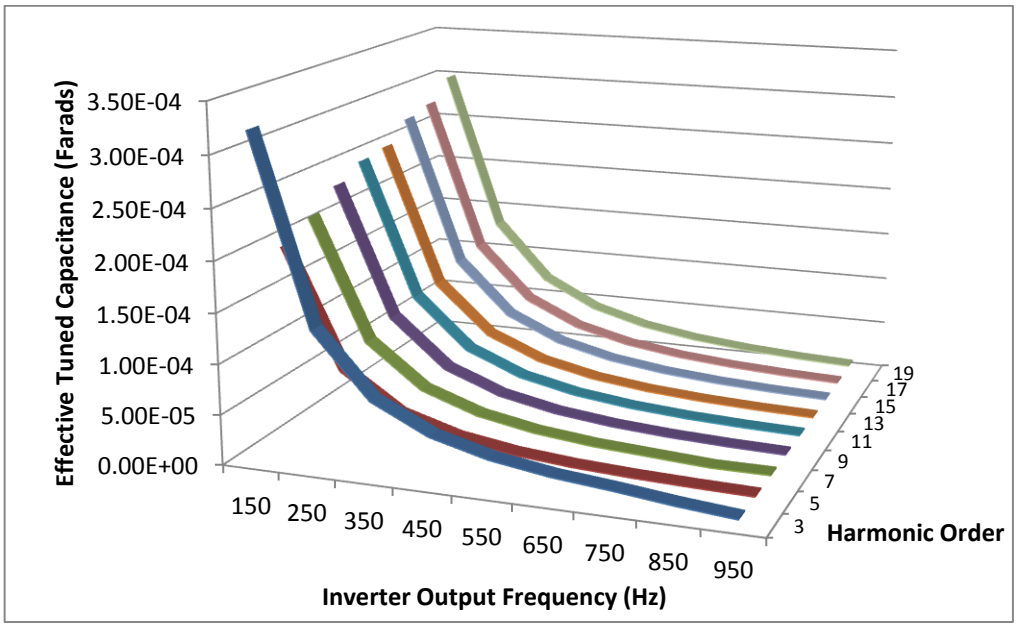


Figure 5.5 Tuned Effective Capacitance in term of inverter output frequency and harmonic component order (Simulation)

5.2.5.2 Harmonic Reduction using Traditional and Proposed Methods

Figure 5.6 illustrates the percentage of the reduced 3rd harmonics in the process of varying the inverter output frequency. Although traditional tuned LC filter reduces harmonics by less than 10% of the original harmonic component at all inverter output frequencies, it is observed that the SCDS filter can reduce harmonic components by 20% in the worst case as seen at f_o=150Hz.

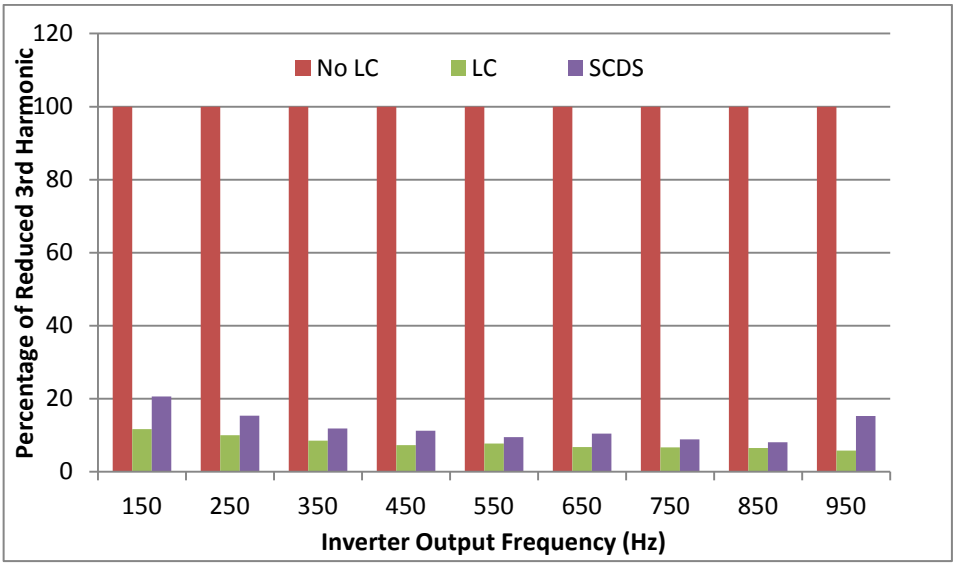


Figure 5.6 Percentage of reduced 3rd harmonic in terms of inverter output frequency using traditional LC filter and the proposed SCDS filter (Simulation)

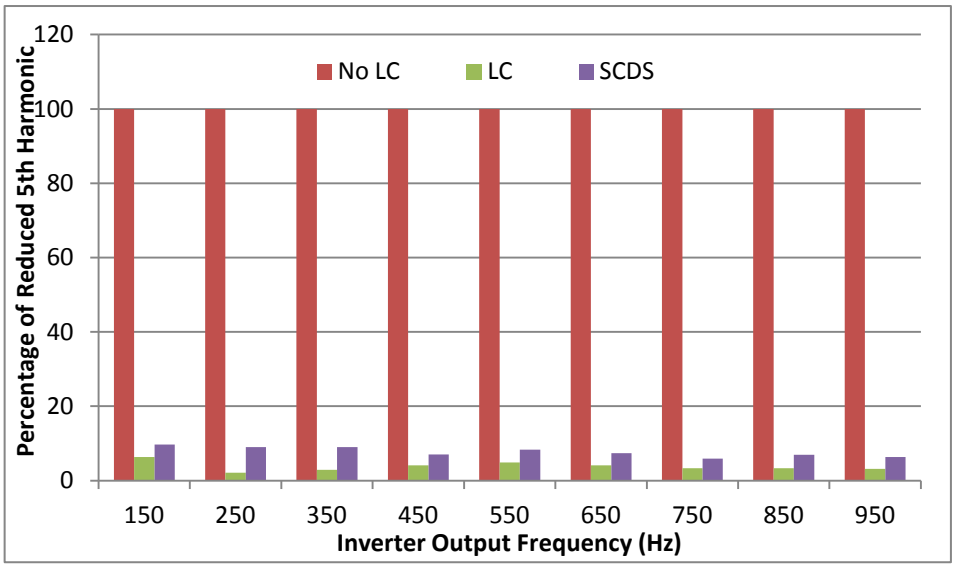


Figure 5.7 Percentage of reduced 5th harmonic in terms of inverter output frequency using traditional LC filter and the proposed SCDS filter (Simulation)

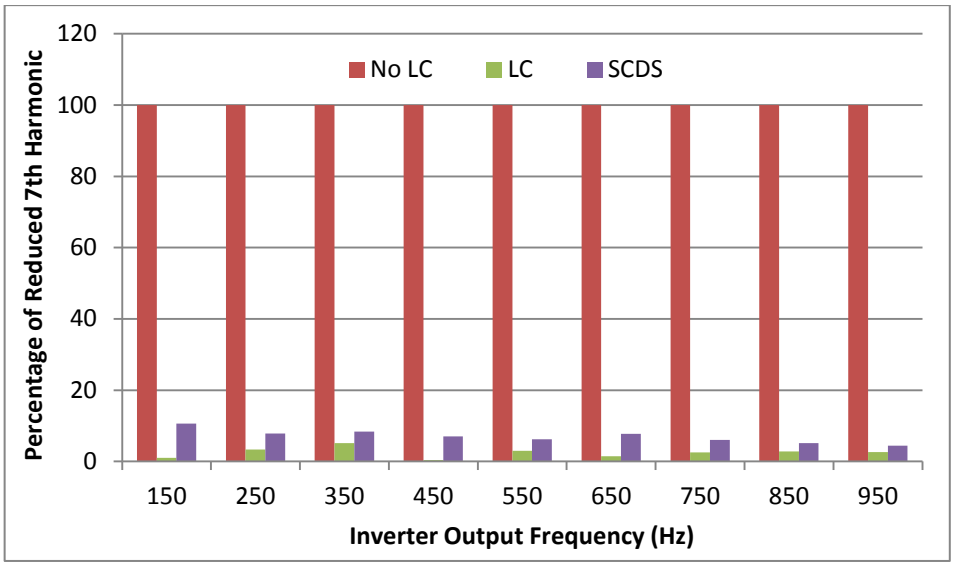


Figure 5.8 Percentage of reduced 7th harmonic in terms of inverter output frequency using traditional LC filter and the proposed SCDS filter (Simulation)

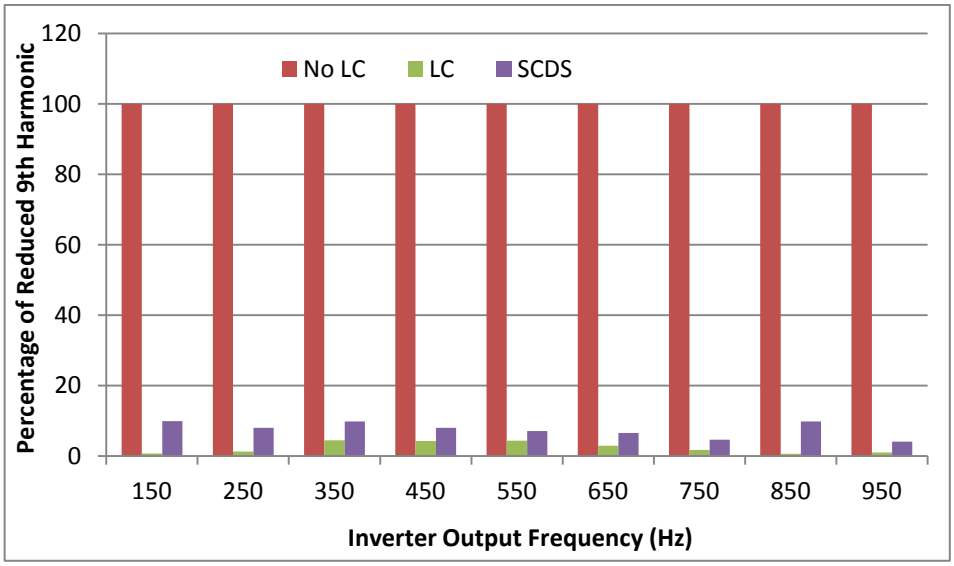


Figure 5.9 Percentage of reduced 9th harmonic in terms of inverter output frequency using traditional LC filter and the proposed SCDS filter (Simulation)

The rest harmonic components are reduced by less than 10% at other inverter's output frequencies. Regardless the difference between the performances of the proposed filter compared to the traditional one, it is shown that SCDS filter can reduce specific harmonics effectively (up to 80% to 90%). Figure 5.7 shows a better performance of SCDS in reducing the 5^{th} harmonic compared to 3^{rd} harmonic reduction. All 5^{th}

harmonics components at various inverter output frequencies are reduced by less than 10%. The same performance is observed in tracing 7th and 9th harmonic components as shown in Figure 5.8 and 5.9, respectively. Harmonics larger than 9^{th} with respect to the fundamental are too small to be considered for single tuning. It is observed that traditional LC filter is slightly better than the proposed system in harmonic reduction; however, the proposed method has the superiority of specific harmonic tracking.

5.2.5.3 Effect of SCDS Filter on Current Harmonics

The effect of using SCDS circuit in single tuned filters is studied in the previous sections showing the ability to trace different harmonic components at the variation of the inverter output frequency. In this section, a comparison is held in order to show the superiority of the proposed self tuning method compared to the existing methods represented by TCR circuit as conducted previously in chapter 2. It is stated before that TCR operates at low switching frequency due to the intrinsic characteristic of the thyristors. This led to high injection of low order harmonic in the system and in consequence elevating the Total Harmonic Distortion (THD). The THD can be defined as:

$$THD = \frac{\sqrt{i_t^2 - i_1^2}}{i_1} \tag{5.6}$$

Where i_t is the total load rms current flowing through the circuit, and i_1 is the fundamental components of the total RMS current. Figure 5.10 shows the THD of both self tuning methods, SCDS and TCR. It is observed that TCR suffer severely from high THD compared to the SCDS circuit. It is observed that THD for TCR circuit can reach 40% [81]. On the other hand, SCDS circuit shows THD which is less than 2%. This is due to the high switching frequency operation of SCDS circuit. However, the high

switching frequency causes high switching loss and this is dealt in the following section.

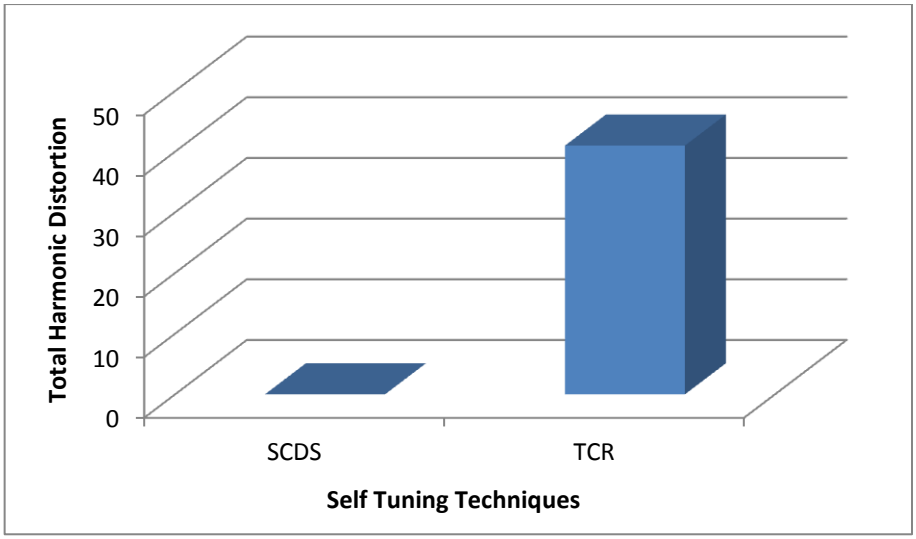


Figure 5.10 Total Harmonic Distortion for the existing self tuning methods (TCR) and the proposed method (SCDS)

5.2.5.4 Effect of SCDS filter on switching losses

The significant parameter where the switching frequency is decided is the switching losses. Higher switching frequency means an absence of low order harmonic in the frequency spectrum but at the expense of the overall efficiency of the system. The switches' conduction loss also affects the efficiency however it is independent on the switching frequency (Figure 5.11). Therefore, switching frequency is taken into account in this research. This will increase the size and cost of the heat sinks associated with the semiconductor power switches in order to overcome the problem of overheating. The proposed SCDS filter operates at relatively high switching frequency (f_s=10 kHz). However, in order to show the insignificant effect of this high frequency operation, a comparison is held with an existing high frequency PWM H-bridge inverter (Figure 5.12b). It is compared with a low frequency H-bridge inverter integrated with four

SCDS filter (Figure 5.12a) for the sake of tracing 3rd, 5th, 7th and 9th harmonic components at different inverter output frequencies. The high frequency operation of the PWM inverter gives the opportunity of installing a small size filter to compensate high order harmonics at the expense of high switching losses.

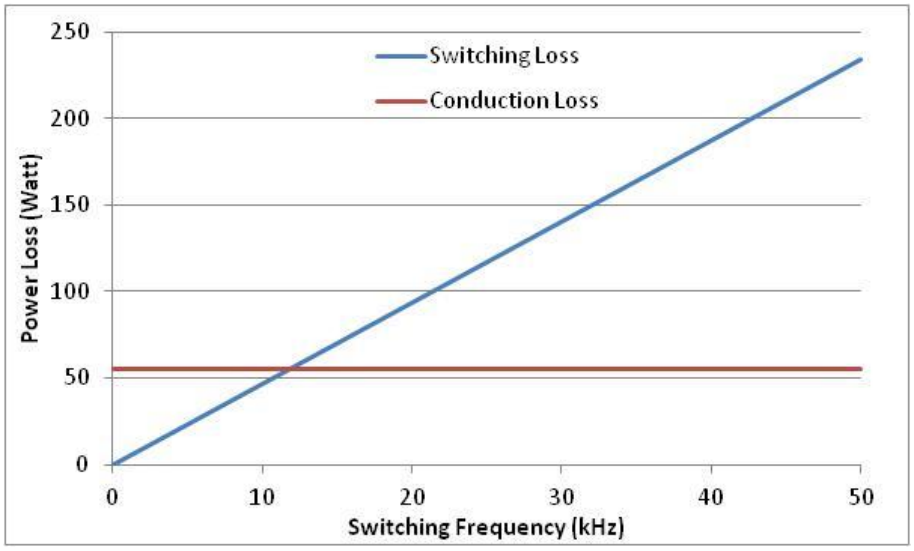
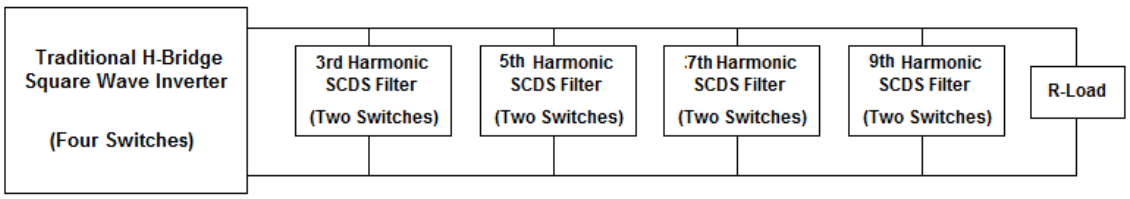
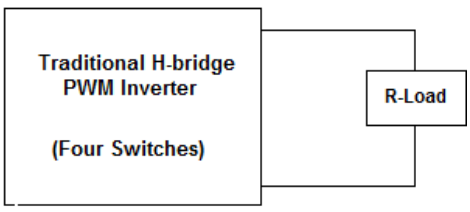


Figure 5.11 Switching loss and Conduction loss in terms of Switching frequency



(a)



(b)

Figure 5.12 Two voltage source inverter systems, a: Traditional H-bridge Square Inverter integrated with SCDS Filters, and b: PWM Inverter

Figure 5.13 shows the switching losses associated with the installed switches in both systems. It is observed that PWM inverter suffers from high switching losses of 35 watt which is the sum of the individual average switching losses associated with the four switches.

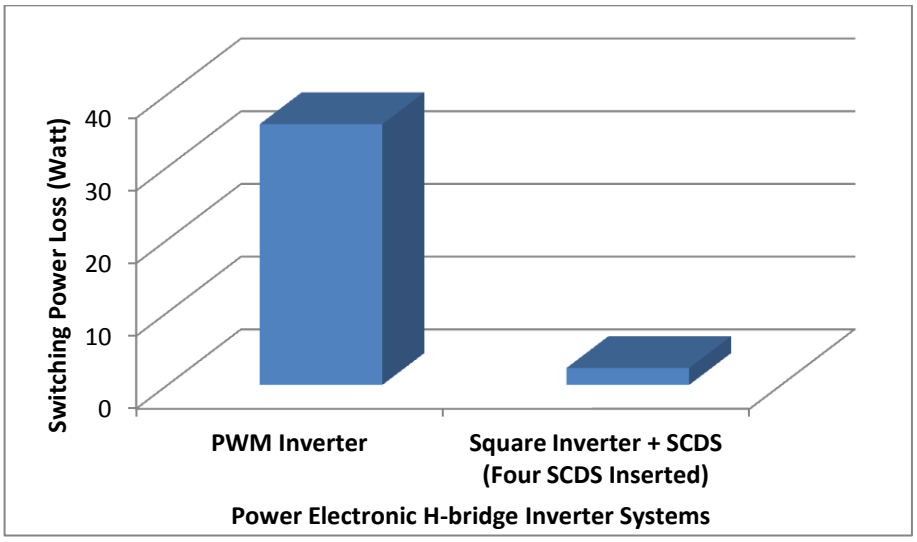


Figure 5.13 Switching power losses in two power electronic H-bridge inverter systems

On the other hand, the proposed SCDS filter (four filter branches) integrated with square wave inverter shows a tremendous reduction in the switching losses of 2.3 watt which is the sum of the average switching losses associated with the inverter (four switches), and SCDS four branches (8 switches). This is because the PWM inverter carries the full load current through its switches which led to consuming higher power. The other system is composed of a low frequency inverter and four high switching frequency SCDS filters each of each is carrying a portion of the load current which at its tuning frequency (i.e. 3^{rd} harmonic current only).

5.3 Implementation of the Single Capacitor Double Switch Circuit

Single capacitor Double switch circuit is built up experimentally using the required power components. Figure 5.14 shows the circuit used in the practical results. Two MOSFET switches, one capacitor, and an inductor are connected across the mains power supply. SCDS circuit has been implemented in the laboratory in order to verify the theoretical relations derived previously in this chapter showing the variable capacitance variations through controlling the duty cycle of the semiconductor switches. The detailed experimental setup of the SCDS circuit, shown in Figure 5.14, illustrating the powers MOSFET switches (IRF740) which are fed by the switching pattern signals through a driver circuits. The switching pattern is obtained from the output port of a microprocessor (Arduino Uno).

Push buttons have been constructed along side with the microprocessors using special purpose output ports in order to control the On and Off time instances of the power switches. A simple C++ program has been written to generate the desired train of pulses at 10 kHz operating frequency as shown in appendix A. Figure 5.15 shows a flowchart of the programmable generation of the switches' duty cycle. This program has the ability to provide a control method using the installed push button for the sake of adjusting the duty cycle between 0.1 and 0.9. An ultra fast power diode (16CTU04PbF) rectifier is constructed and connected across the MOSFET switches so that the MOSFET can operate in a bidirectional manner.

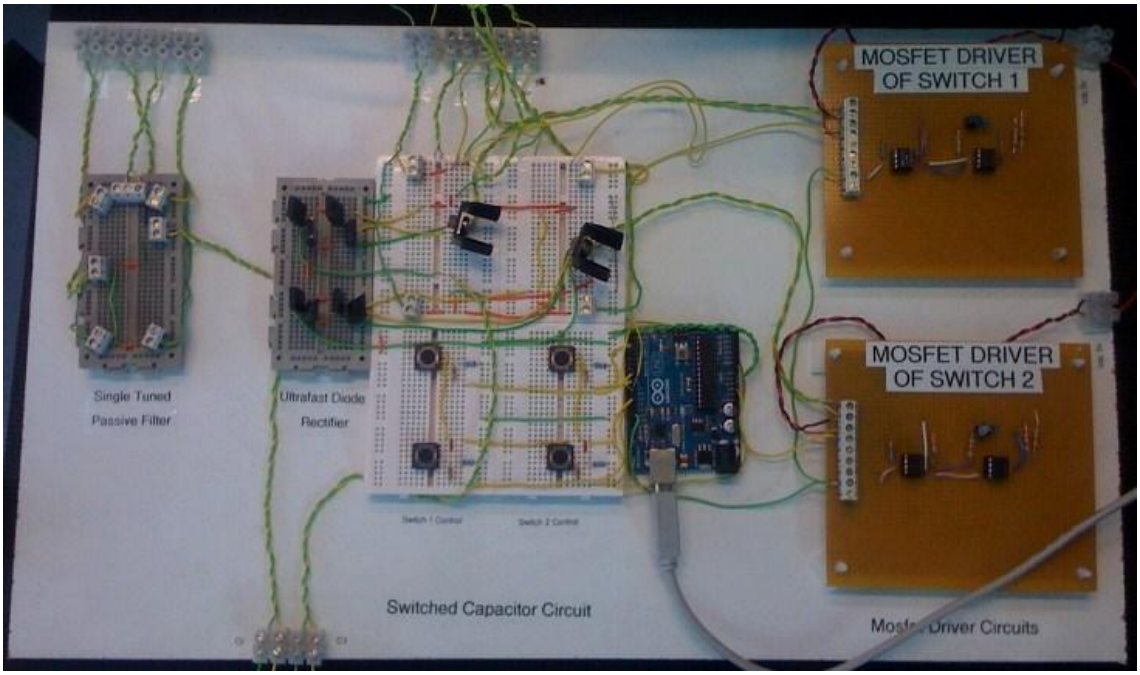


Figure 5.14 The proposed system showing traditional and new single tuned filter

The voltage and current flowing through the switches are measured using voltage, and current probes, respectively. The outputs waveforms are shown on digital oscilloscope (Tektronix) in order to calculate the capacitive impedance of the circuit and hence calculate the associated effective capacitance neglecting the ohmic resistance of the wires. The experimental setup of SCDS circuit is illustrated in Figure 5.16 which shows the overall system on the working bench, including the computer, square wave inverter, capacitor bank, and the inductor.

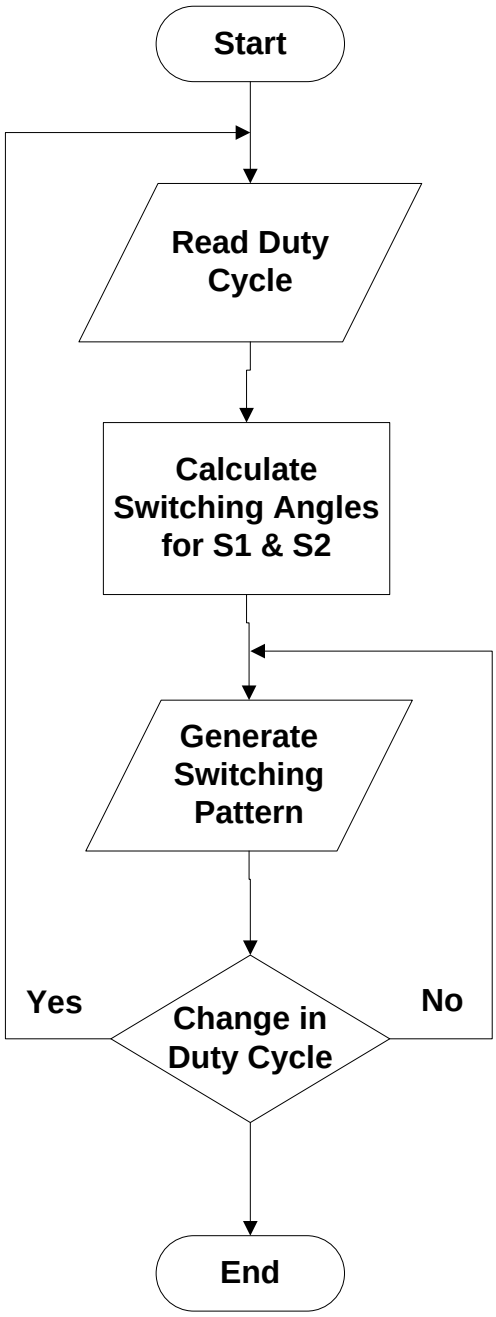


Figure 5.15 Flowchart of the programmable generation of the switches' duty cycle

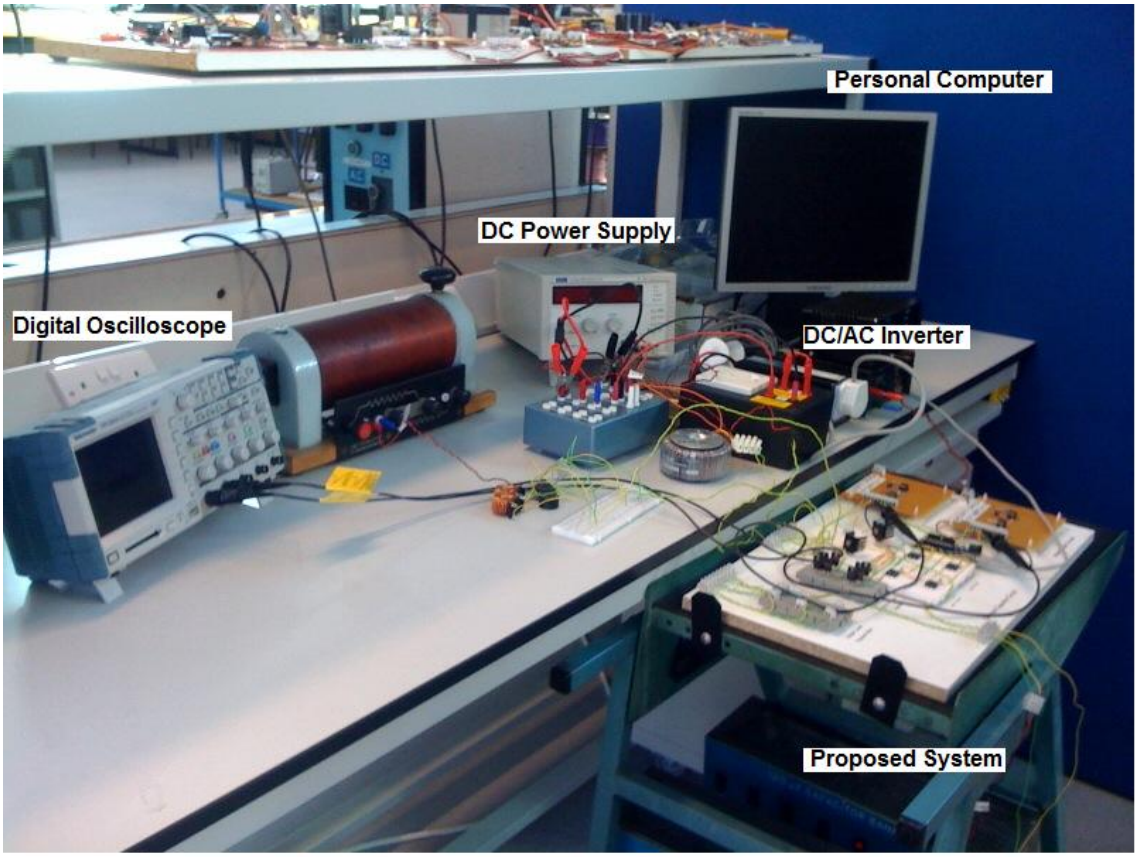


Figure 5.16 The experimental setup showing the proposed system and its associated components

The following figures shows screen shots of the experimental results of the voltage and current waveforms associated with single capacitor double switch circuit at different duty cycle of the semiconductor switches. Figures 5.17 to 5.25 illustrates the waveforms using a fixed capacitor, 5 μF at different duty cycles (0.1, 0.2, 0.3,.....0.9).

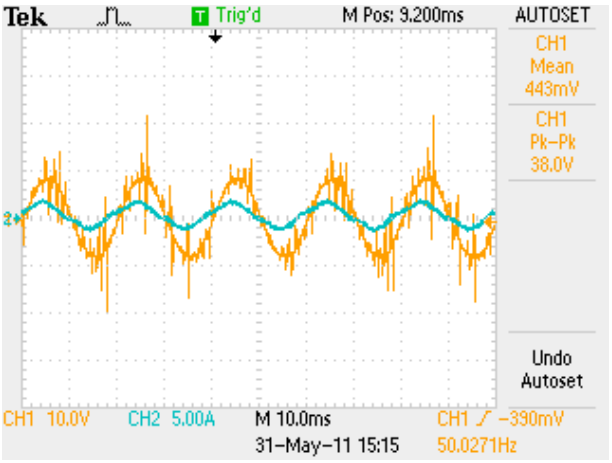


Figure 5.17 Voltage and Current waveform at K_o=0.1, (C=5 µF)

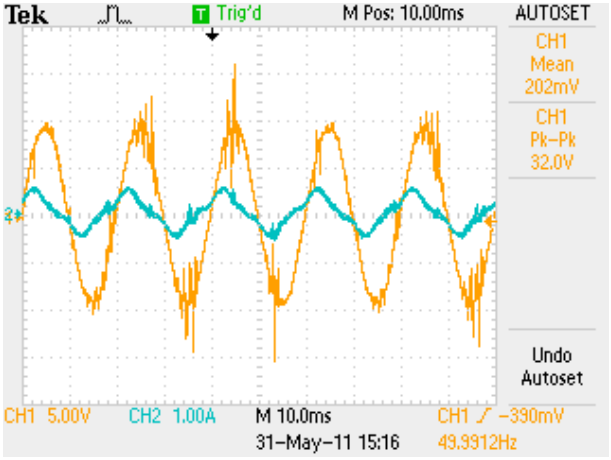


Figure 5.18 Voltage and Current waveform at K_o=0.2, (C=5 µF)

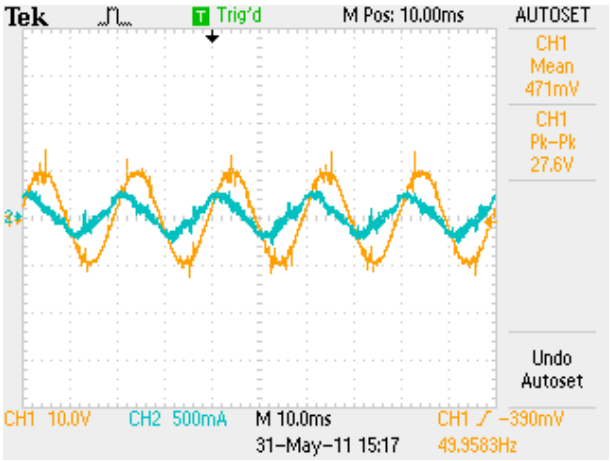


Figure 5.19 Voltage and Current waveform at K_o=0.3, (C=5 µF)

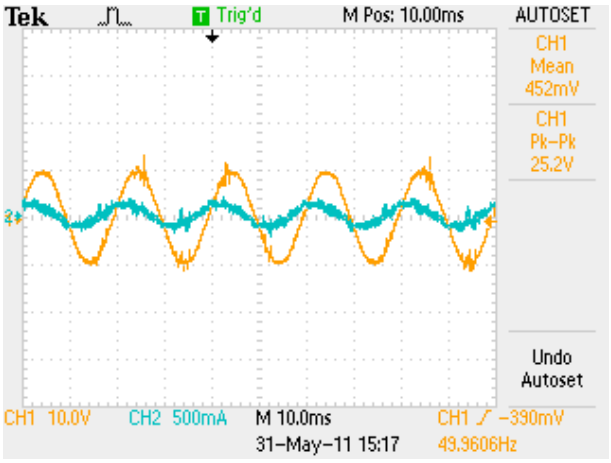


Figure 5.20 Voltage and Current waveform at K_o=0.4, (C=5 µF)

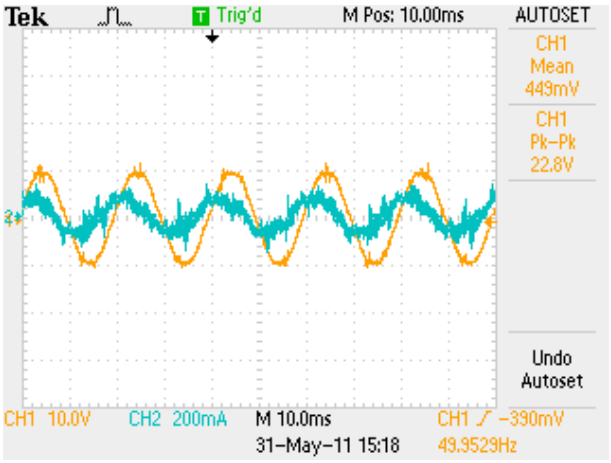


Figure 5.21Voltage and Current waveform at K_o=0.5, (C=5 µF)

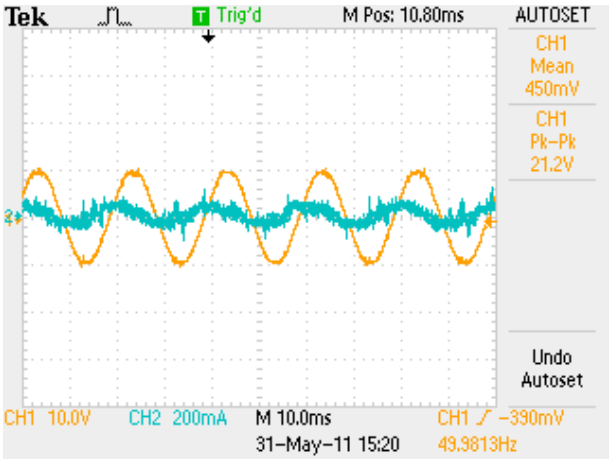


Figure 5.22 Voltage and Current waveform at K_o=0.6, (C=5 µF)

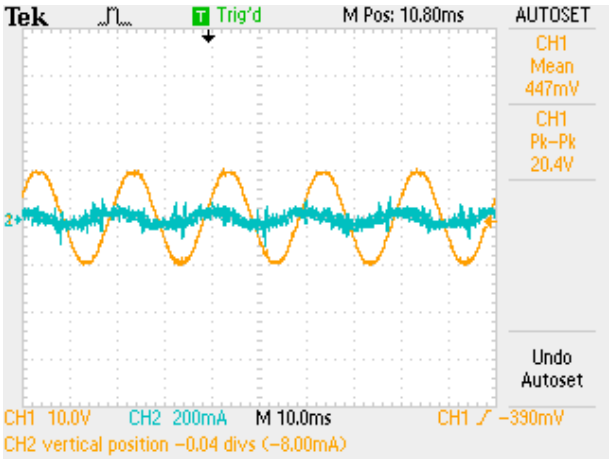


Figure 5.23 Voltage and Current waveform at K_o=0.7, (C=5 µF)

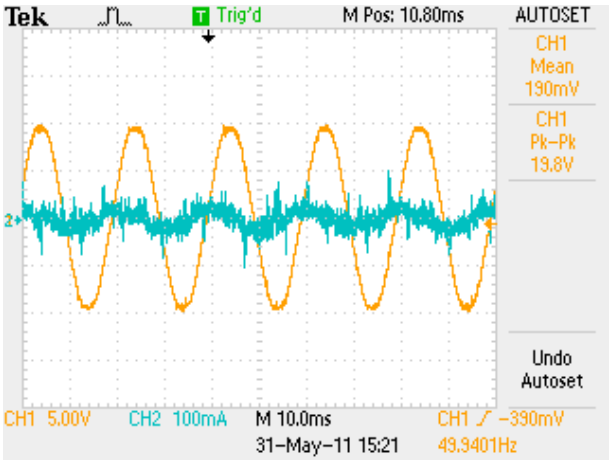


Figure 5.24 Voltage and Current waveform at K_o=0.8, (C=5 µF)

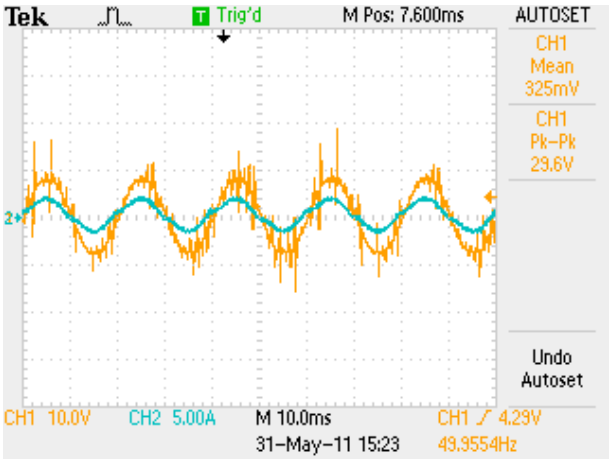


Figure 5.25 Voltage and Current waveform at K_o=0.9, (C=5 µF)

Figures 5.26 to 5.34 presents the waveforms using a fixed capacitor, 10 µF at different duty cycles (0.1, 0.2, 0.3,.....0.9). Figure 5.35 shows the anti-parallel train of pulses at K_o=0.5.

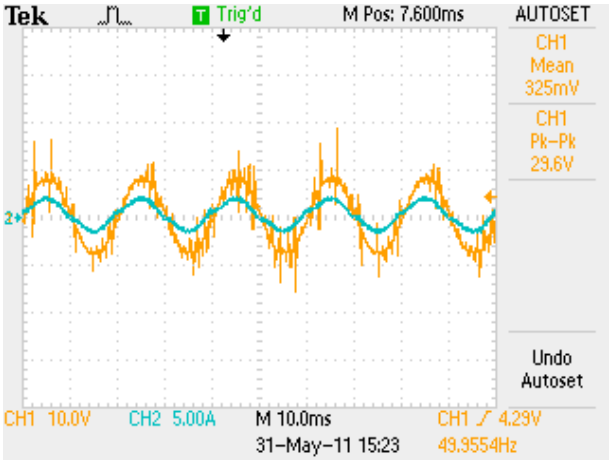


Figure 5.26 Voltage and Current waveform at K_o=0.1, (C=10 µF)

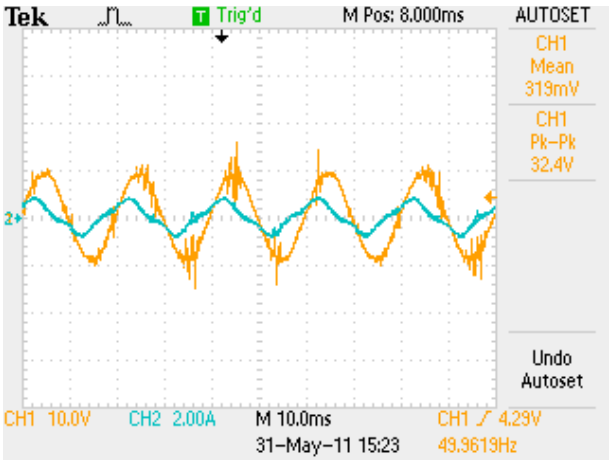


Figure 5.27 Voltage and Current waveform at K_o=0.2, (C=10 µF)

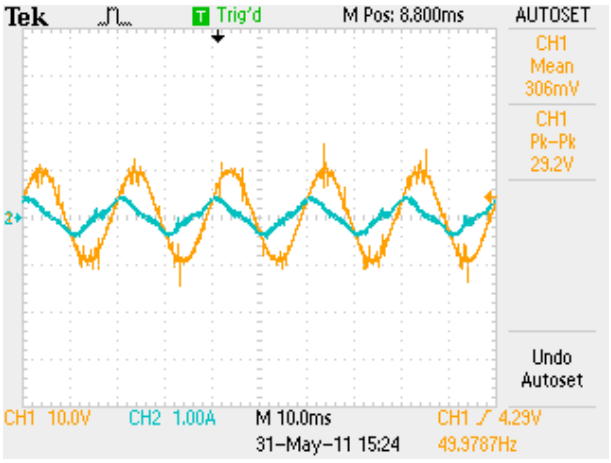


Figure 5.28 Voltage and Current waveform at K_o=0.3, (C=10 µF)

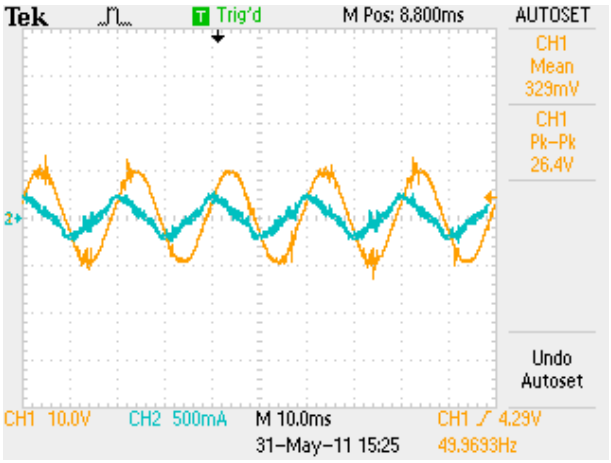


Figure 5.29 Voltage and Current waveform at K_o=0.4, (C=10 µF)

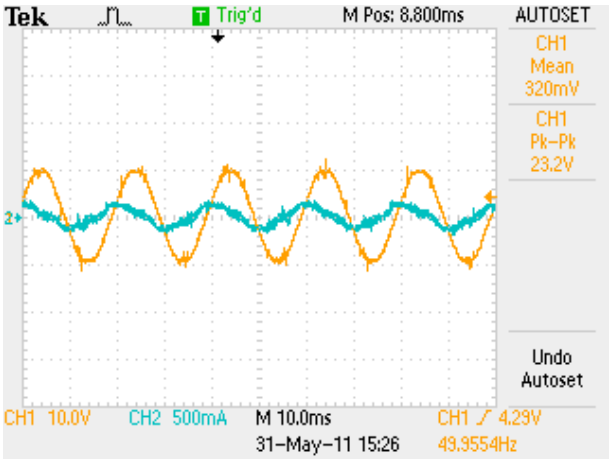


Figure 5.30 Voltage and Current waveform at K_o=0.5, (C=10 µF)

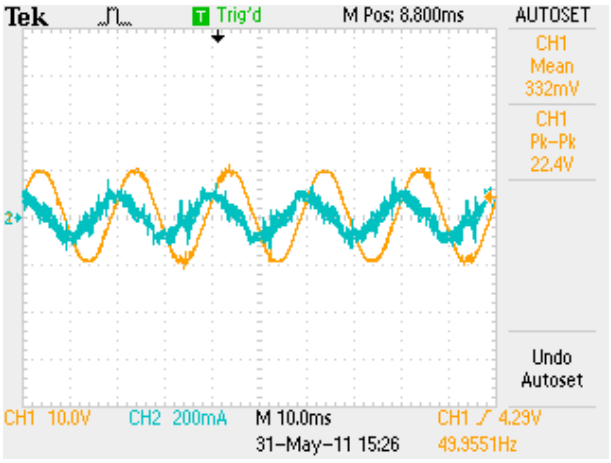


Figure 5.31 Voltage and Current waveform at K_o=0.6, (C=10 µF)

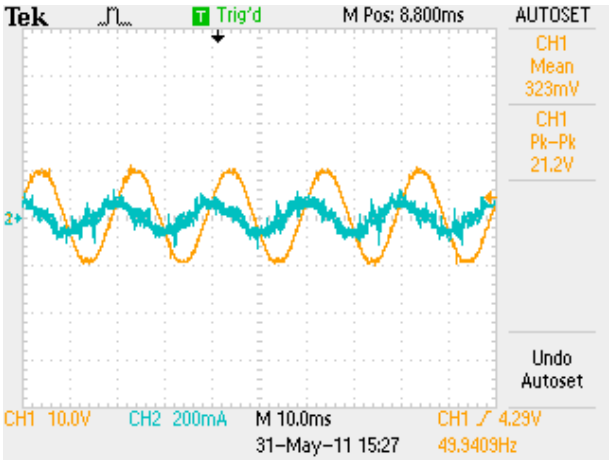


Figure 5.32 Voltage and Current waveform at K_o=0.7, (C=10 µF)

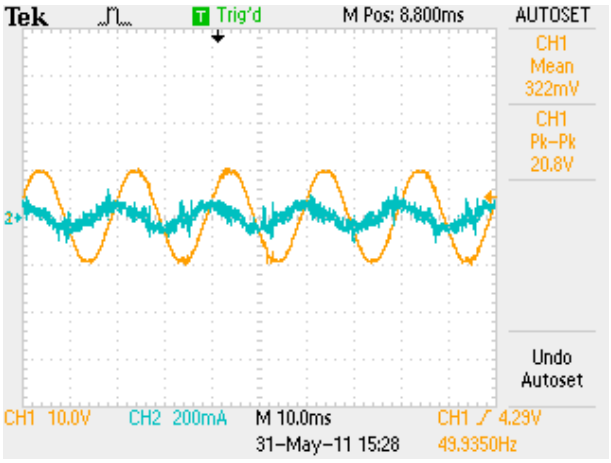


Figure 5.33 Voltage and Current waveform at K_o=0.8, (C=10 µF)

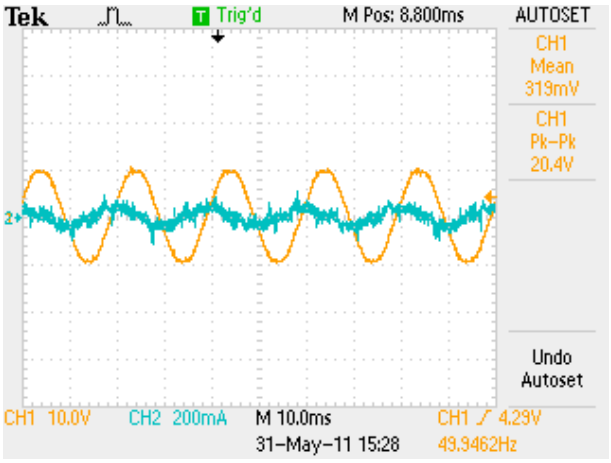


Figure 5.34 Voltage and Current waveform at K_o=0.9, (C=10 µF)

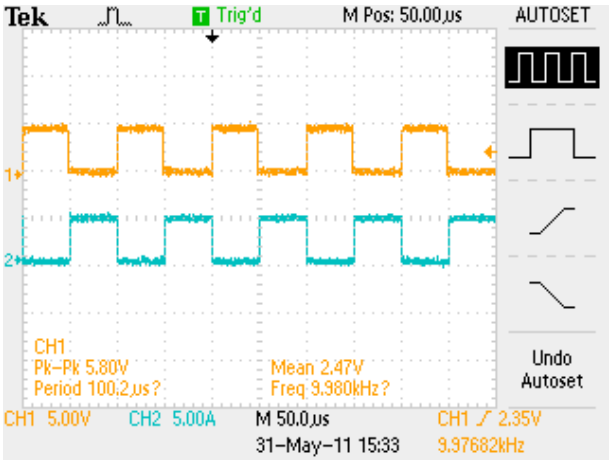


Figure 5.35 Anti-parallel switching pulses at K_o=0.5

Figure 5.36 and 5.37 shows the relation between the effective capacitance and the duty cycle for SCDS circuit for the value of a fixed capacitor, C=5 µF and C =10 µF, respectively. The slight deviation of the experimental characteristics from the theoretical characteristics is due to the approximation assumed by neglecting the Ohmic resistance of the circuit. However, the experimental results show a good verification in terms of the effective capacitance variation by controlling the duty cycle of the power switches. This shows that SCDS behaves as a variable capacitor across its terminals where the effective capacitance is measured and calculated.

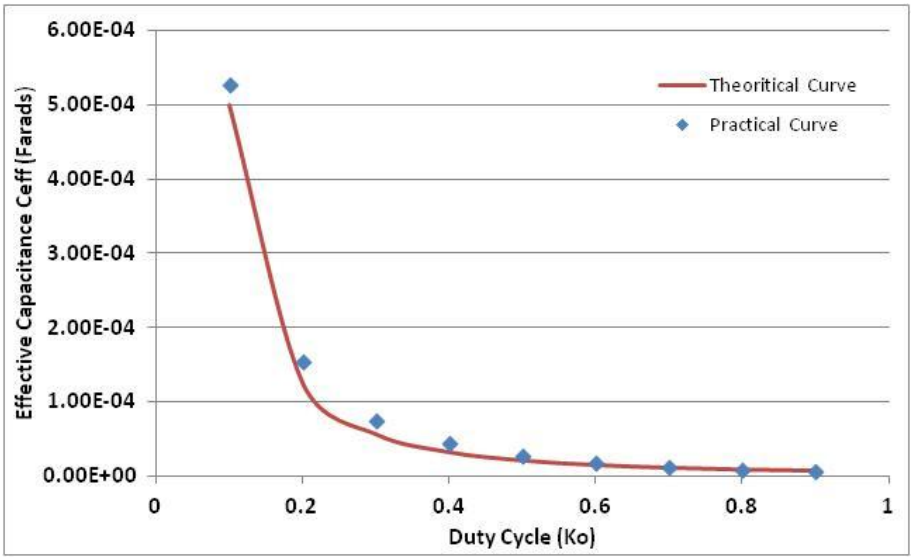


Figure 5.36 Experimental results showing the relation between Duty cycle and Effective Capacitance in SCDS circuit (Fixed C = 5 µF)

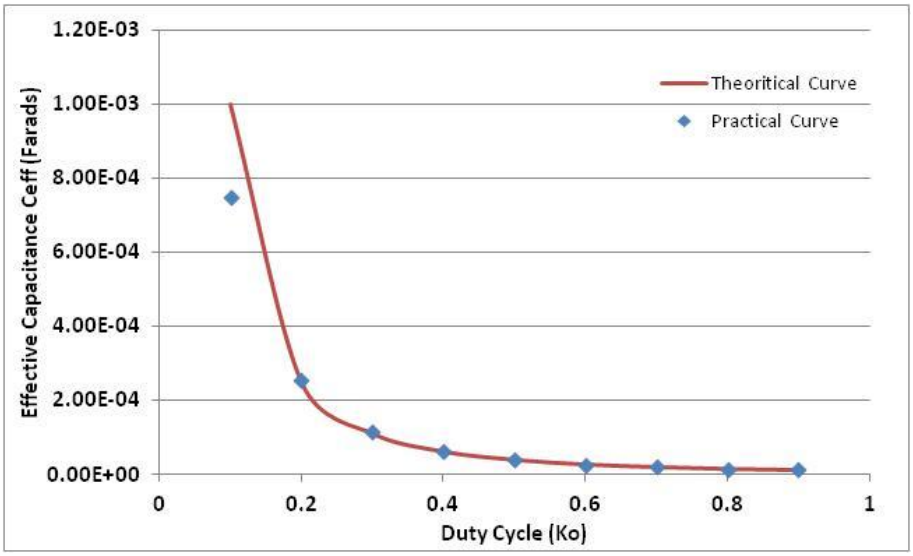


Figure 5.37 Experimental results showing the relation between Duty cycle and Effective Capacitance in SCDS circuit (Fixed C = 10 µF)

Figure 5.38 shows the experimental results of traditional LC filter and SCDS filter performance in reducing the 5th harmonic component at 50Hz square wave output frequency.

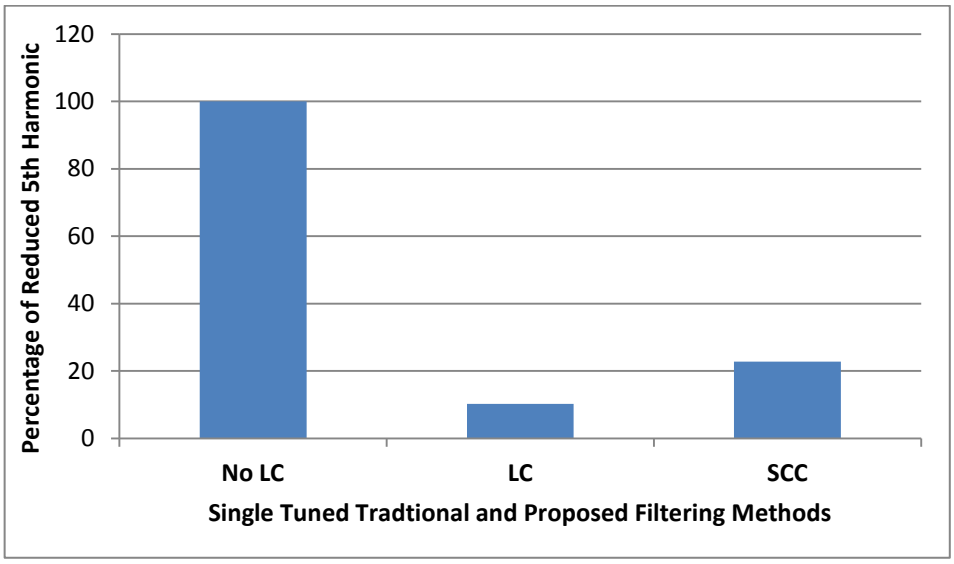


Figure 5.38 Experimental results showing the percentage of reduced 5th harmonic in square wave inverter output at fo=50Hz (Experimental).

This figure shows the 5th harmonic reduced to 10% and 22% of its original value in traditional LC, and SCDS tuned filter, respectively. The result shows a good agreement with the simulation results conducted earlier where the proposed filter has the ability to withdraw the tuned harmonic component.

5.4 Summary

This chapter presented the simulation and hardware implementation of the proposed single tuned passive output filter. The proposed model was designed using Orcad PSPICE software. The simulation results showed the ability of the SCDS filter to change its tuned effective capacitance at different inverter output frequency. It had also shown that it can reduce any tuned harmonic component, relatively in an effective way,

compared to traditional single tuned filter. In addition, a critical comparison was held between the proposed filter and two different techniques in dealing with harmonic in terms of total harmonic distortion and switching losses. The hardware implementation showed a good agreement with the theoretical results in term of effective capacitance-duty cycle relationship. Also, the proposed filter was implemented to reduce a specific harmonic which was able to do. The concluding remarks and future work follow in the next and the final chapter.

Chapter 6
Conclusions and Future Work

6.1Conclusions

The aim of this research work is to design a new output passive filter for inverter applications in order to trace and reduce harmonics wherever its location in the frequency spectrum. This has been accomplished by introducing the switched capacitor circuit as a new configuration of single tuned passive filter of traditional voltage source H-bridge inverter which has not been conducted in any publication until this research work was completed. To accomplish the aim of this research, the following objectives have been conducted where the contribution to knowledge in the field of passive filtering is also represented:

1. A comprehensive critical literature review of passive power filter in specific and active power filters were presented showing the merits and drawbacks of each technique. In addition, voltage source H-bridge inverter topologies where presented including their common modulation schemes in traditional and multilevel topologies which has been published as a journal article by the Author [82].

2. Upon completion of reviewing and presenting power filters and inverters configurations, decision was made to select single tuned filter as an output filter for square wave inverter applications. Single tuned filter provides a lower impedance path for harmonics compared to other passive filters. Also square wave inverter operates at low switching frequency which results in improvement of the overall efficiency of the system. This decision is made in order to modify the selected

filter by inserting switched capacitor circuit which acts as a variable tuned capacitor for the purpose of tracking harmonic frequencies in the current spectrum. It is considered as a new topology in harmonic filtering methods for inverter applications which has not been covered in any of the published literature in this topic.

3. Topologies of switched capacitor circuits have been analyzed, mathematically modelled, and overviewed showing their suitability for harmonic filtering applications. The mathematical analysis of the switched capacitor circuit as a variable capacitor has been developed for two circuits; single capacitor double switch and double capacitor double switch configurations. The relation between the effective capacitance and the duty cycle was derived for both circuits. It was concluded that single capacitor double switch circuit varies the capacitance value in a similar manner to the double capacitor double switch but with the obvious advantage of using one capacitor less.

4. Other two topologies of switched capacitor circuits have been presented briefly, single capacitor single switch, and triple switch configuration. These two topologies were not discussed in details due to their unsuitability for filtering action. Single capacitor single switch circuit suffer from low power quality performance which is essential in harmonic filtering. Triple switch configuration is useful in high power applications; however it suffers from high number of switching components, which is a major issue from the system's efficiency point of view. In order to decide the optimum switching frequency of high frequency operated switched capacitor circuits, a compromise between the switching losses which is elevated through the increase of the switching frequency and the

compensator current harmonics which requires the circuit to operate at high switching frequency.

5. For these reasons, the decision was made to consider single capacitor double switch in this research. The mathematical derivation of the characteristics of this topology proved the behaviour of acting as a variable capacitor by controlling the duty cycle of the power semiconductor switches. This relation contribute in tracking harmonic components wherever its location in the frequency spectrum.

6. An investigation has been conducted on power electronic software packages which are commonly used to design and simulate electronic circuits. This investigation showed two alternatives for power electronic circuit design and simulation: Orcad PSPICE, and Matlab. At the early stage of this research, several attempts were conducted in order to design the proposed model in both software packages. It was observed that Matlab does not have the flexibility of using real power components as in Orcad PSPICE. However, it has an attractive environment in control methods. Orcad PSPICE library includes a comprehensive number of components sorted by the manufacturer's part number. Also, it has the ability to measure any electrical physical quantity in a simple way. The above reasons led the author to adopt Orcad PSPICE for the design and simulation of the proposed filter.

7. The characteristics of the switched capacitor circuit were verified experimentally and it showed an excellent agreement with the theoretical results when the measuring instruments tolerance is taken into consideration. The proposed filter using switched capacitor circuit was simulated showing its performance in filtering action from different aspects. The simulation results proved that the switched capacitor circuit controls the amount of the current flowing through the circuit by

controlling the duty cycle of the switches. It showed an effective way of varying the tuned capacitance in order to resonate with the series tuned inductor at different harmonic frequencies. This was proved experimentally showing a significant reduction in a specific harmonic component compared to traditional single tuned filter.

8. The simulation results of the new filter was discussed from different aspects which is considered as a major part of the contribution to knowledge in this thesis as follows:

    - The contribution of tracing specific harmonics when the operating frequency of the inverter changes by controlling the duty cycle of the switched capacitor circuits. Also, the ability of reducing harmonic components close to traditional methods.
    - The contribution to present the new filter design showing its merits compared to existing self tuning methods in the field of harmonic injection to the system.
    - The contribution of showing the superiority of the proposed new filter integrated with square inverter over PWM inverter system in the field of switching losses which affects the efficiency of the system.

The simulation and experimental results were very promising and it opens the door for researchers to enhance the performance of the adopted topology and to introduce this concept by modifying other passive power filter topologies in the future.

6.2 Future Work

The following points are suggested for future work related to the implementation of the switched capacitor circuit in passive filtering field:

- More research on the triple switched capacitor configurations could be conducted to validate its performance in high power applications. The current single capacitor double switch configuration is suitable for low power application where the current rating is not high and can be tolerated by the internal impedances of the power components.
- Also, It is desired to undertake more research in finding the optimum value of switching frequency where it can minimize the injected current harmonics without extra unnecessary switching losses which affects the efficiency of the system.
- The single switch double capacitor circuit can be introduced to other passive filter topologies such as high pass filters and band pass filters in order to validate its performance in these types of harmonic filtering.
- More investigation to be done in improving the harmonic reduction performance of the proposed system compared to traditional methods.
- Accurate cost analysis of the proposed system should be carried out at the manufacturing stage. A comparison can be held between the traditional and the proposed single tuned filters.
- A closed loop system can be implemented on the proposed system in order to change the switches' duty cycle and in consequence the effective tuned capacitance.

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Appendix A

C-Language Program for Switching Pattern Generation

The following C-language program shows the generation of the switching pulses fed to two semiconductor switches in single capacitor double switch circuit. The switching pulses are generated in an anti-parallel manor (i.e. S1 is On, S2 is Off) at switching frequency equals to 10 kHz. The microcontroller used is Arduino Uno. The code is presented as follows:

A.1 Arduino Pins Initialisation

```
const int buttonPin2 = 2;      // the number of the pushbutton2 pin for S1

const int buttonPin7 = 7;      // the number of the pushbutton7 pin for S1

const int buttonPin8 = 8;      // the number of the pushbutton8 pin for S2

const int buttonPin11 = 11;    // the number of the pushbutton9 pin for S2

// variables will change:

int buttonState2 = 0;         // variable for reading the pushbutton status

int buttonState7 = 0;

int buttonState8 = 0;

int buttonState11 = 0;

int counter=1;

int counter2=4;
```

A.2 Setting Up the Switching Pattern Generation

```
void setup()

{

  // Turn off the timer while we make changes

  TCCR1B = TCCR1B & ~ ((1 << CS12) | (1 << CS11) | (1 << CS10));

  // Ensure the Timer 1 output pins are configured for output

  pinMode( 9, OUTPUT );

  pinMode( 10, OUTPUT );

    // Set Compare Output Mode and part of the Waveform Generation Mode (mode 14)

  TCCR1A =

     (1 << COM1A1) | (0 << COM1A0)  // Clear OC1A on Compare Match, set OC1A at BOTTOM (non-inverting mode)

     |

     (1 << COM1B1) | (1 << COM1B0)  // Set OC1B on Compare Match, clear OC1B at BOTTOM (inverting mode)

     |

     (1 << WGM11) | (0 << WGM10);  // Mode 14: Fast PWM, TOP = ICR1, Update of OCR1x at BOTTOM, TOV1 Flag Set on TOP
```

```
  // Set the other half of the Waveform Generation Mode (mode 14) and ensure a few things are disabled
  TCCR1B =
      (0 << ICNC1)  // Input Capture Noise Canceler disabled
      |
      (0 << ICES1)  // Input Capture Edge Select don't care
      |
      (1 << WGM13) | (1 << WGM12)  // Mode 14: Fast PWM, TOP = ICR1, Update of OCR1x at BOTTOM, TOV1 Flag Set on TOP
      |
      (0 << CS12) | (0 << CS11) | (0 << CS10);  // Clock continues to be disabled.  Not yet finished configuring.
  // Set the output frequency
  // fOCnxPWM = fclk_I/O / (N * (1 + TOP))
  // fOCnxPWM = 16000000 / (8 * (1 + 199))
  // fOCnxPWM = 10000 Hz
  ICR1 = 199;
    // Start with both outputs turned off
  OCR1A = counter;
  OCR1B = counter2;
```

```
  // Start the clock
 TCCR1B =
    TCCR1B
    |
    (0 << CS12) | (1 << CS11) | (0 << CS10);  // clkI/O/8 (From prescaler)
}
```

A.3 Setting Up the Push Button Control for the Pulses Duty Cycle

```
void loop()
{
  // read the state of the pushbutton value:
  buttonState2 = digitalRead(buttonPin2);
  buttonState7 = digitalRead(buttonPin7);
  buttonState8 = digitalRead(buttonPin8);
  buttonState11 = digitalRead(buttonPin11);
    Serial.println( digitalRead(buttonPin2));
    delay(10);
   if (buttonState2 == HIGH) {
    counter=counter+1;
    OCR1B = counter;  // set the PWM to 20% duty cycle
```

```
    Serial.println(counter);
    delay(50);
}
 if (buttonState7 == HIGH) {
   counter=counter-1;
   OCR1B = counter;  // set the PWM to 20% duty cycle
    Serial.println(counter);
    delay(50);
}
   Serial.println( digitalRead(buttonPin8));
   delay(800);
 if (buttonState8 == HIGH) {
   counter2=counter2+1;
   OCR1A = counter2;  // set the PWM to 20% duty cycle
    Serial.println(counter);
    delay(100);
}
 if (buttonState11 == HIGH) {
   counter2=counter2-1;
```

```
    OCR1A = counter2;  // set the PWM to 20% duty cycle

     Serial.println(counter);

     delay(100);

  }

}
```

Appendix B

List of Publications

List of Publications

[1] M. F. Arman, M. K. Darwish, "Critical Review of Cascaded H-Bridge Multilevel Inverter Topologies," *International Review of Electrical Engineering*, Vol. 4, pp. 730-743, 2009.

[2] M. A. Radi, M. F. Arman, M. K. Darwish, C. C. Marouchos, " PSPICE Modeling of a Build-in Feedback Automatic –Reactive Power Compensation", *International Review of Modelling and Simulation*, Submitted in Sep. 2011.