Analysis of Surface Charge Effects and Edge Fringing Capacitance in Planar GaAs and GaN Schottky Barrier Diodes

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***Abstract*— In this article, by means of a 2-D ensemble Monte Carlo simulator, the Schottky barrier diodes (SBDs) with realistic geometries based on GaAs and GaN are studied as promising devices for increasing the high-frequency performance- and power-handling capability of frequency mixers and multipliers. The nonlinearity of the capacitance–voltage (*C–V*) characteristic is the most important parameter for optimizing the performance of SBDs as frequency multipliers. The small size of the diodes used for ultrahigh-frequency applications makes the value of its intrinsic capacitance to deviate from the ideal one due to fringing effects. We have observed that the value of the edge capacitance well into reverse bias does not depend on the applied voltage. We define an edge-effect parameter β, which, interestingly, is affected by the presence or absence of surface charges at the semiconductor–dielectric interface σ. Two physical models have been considered: a fixed σ related to a surface potential V_S constant surface-charge model (CCM) and a self-consistent model in which the local value of σ is dynamically evaluated depending on the surrounding electron density self-consistent surface-charge model (SCCM). Using the CCM, we obtain that β depends on the depth of the depletion region W_S created by the surface charges, nearly irrespectively of the epilayer doping or semiconductor type. The more realistic SCCM indicates that, at low frequencies, when the surface charges are able to follow the variations of the applied voltage, the value of β approaches the one obtained without surface charges, while the high-frequency value (the significant one) is smaller.**

***Index Terms*— Edge effects (EEs), GaAs and GaN planar Schottky barrier diodes (SBDs), Monte Carlo (MC) simulation.**

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I. Introduction

TERAHERTZ technology has advanced considerably during the last 30 years; however, there are still important technological challenges for the broad commercial development of applications in the terahertz range, otherwise potentially attractive in several fields, such as security scanning, medical diagnosis, and ultrahigh-bandwidth wireless communications [1]. For example, there is a lack of compact solid-state devices capable of generating terahertz signals with enough power at room temperature. In contrast, in the terahertz detection field, there exist devices that have demonstrated very good performance, such as planar Schottky barrier diodes (SBDs) [2]. GaAs SBD technology is the most widespread used for the fabrication of both mixers and local oscillators based on frequency multipliers for heterodyne detection in the terahertz range [3]–[5]. However, the relatively low-power level that they can handle (given by the moderately low breakdown field and thermal conductivity of GaAs) can be strongly improved by the use of the promising GaN technology. The wide bandgap of GaN can help to reduce the size and complexity of frequency multipliers and mixers used in terahertz technology, extending its limits to applications that need higher power, such as terahertz wireless communications.

The most important parameter for optimizing the SBD performance as frequency multipliers is the nonlinearity of the capacitance–voltage (C–V) characteristic [6]. However, experimental C–V curves are very difficult to obtain and are not often available so that analytical models based on fitting equations are typically used. For this sake, SBDs based on GaAs and GaN have been widely studied by means of 1-D ensemble Monte Carlo (MC) simulations [7], [8]. However, for high-frequency applications, where the anode surface needs to be significantly reduced and the available power is low, the intrinsic capacitance C dramatically deviates from its ideal value due to fringing effects, and 2-D models are needed for a correct analysis of the diodes [9]. The scope of this article is too deep into the study of the influence on these edge effects (EEs) of the presence of surface charges σ at the semiconductor–dielectric interface and, thus, precisely compute the C–V curves of GaAs and GaN SBDs to be used as promising devices for the fabrication of terahertz-frequency multipliers. We will determine the value of the edge fringing capacitance by using a semiclassical ensemble MC simulator

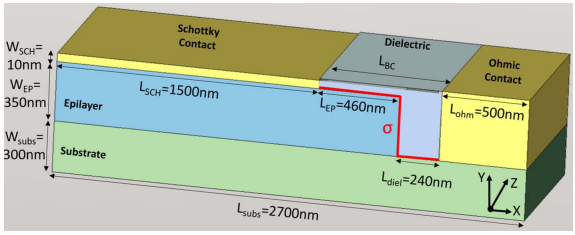

Fig. 1. Scheme of the 2-D MC simulated SBD.

of carrier transport self-consistently coupled with a 2-D Poisson solver [9]–[11]. Two physical models will be considered for the inclusion of σ in the simulations.

This article has been structured as follows. In Section II, details of the MC tool are given, including the surface-charge models, and the realistic topology of the simulated SBDs, based on fabricated devices, is described. In Section III, the MC results are presented, focusing on the EEs affecting the capacitance of the SBDs, linked with the influence of surface charges on the depletion region generated by the Schottky contact. The main conclusions are drawn in Section IV.

II. Model and Structure

For the analysis, we make use of a semiclassical ensemble MC simulator of carrier transport self-consistently coupled with a 2-D Poisson solver, which includes three nonparabolic spherical Γ, L, and X valleys to model the conduction band of GaAs, while valleys Γ_1, U, and Γ_3 are considered for GaN [9], [12], [13]. Ionized impurities, alloy, polar and nonpolar optical phonon, acoustic phonon, and intervalley scattering mechanisms are included in the simulator. Piezoelectric scattering is also considered for GaN. Fermi–Dirac statistics, using a self-consistent calculation of the Fermi level, are imposed for the occupancy of the energy states by means of a rejection technique after every scattering mechanism [11]. To ensure the accuracy of the simulations, the electric field is updated every time step $\Delta t = 0.2$ fs, the total simulation time is $t = 3{\cdot}10^{-11}$ s, and the cell size is in the range 2–5 nm, smaller than the Debye length in all the considered semiconductors.

The MC simulated structures are based in real planar GaAs SBDs fabricated using e-beam photolithography [4], [5], [9], [14]. The scheme of the 2-D simulated SBDs is shown in Fig. 1, with the values of the geometrical parameters and Z being the nonsimulated dimension. The GaAs or GaN layer structure consists of a highly doped n^+ substrate with doping $N_{\rm D} = 5 \cdot 10^{18}$ cm^{-3} and an n doped epilayer. Several values for the epilayer doping are considered: $N_{\rm E} = 10^{17}$, $3{\cdot}10^{17}$, and $6{\cdot}10^{17}$ cm^{-3}. The dielectric used in the simulations is silicon nitride (Si_3N_4), which has a permittivity of 7.5. In order to reduce the computational burden, the substrate thickness $W_{\rm Subs}$ has been decreased with respect to the fabricated device (as in [9], where $W_{\rm Subs} = 300$ nm), still large enough to ensure a flat potential profile at the bottom of the structure. The length of the lateral extension of the epilayer $L_{\rm EP}$ will be modified to study its influence on the fringing capacitance of the Schottky contact. The (reverse) applied voltage range has been chosen so that the epilayer thickness $W_{\rm EP}$ is always larger than the depletion region, thus avoiding its penetration into the substrate.

A thin Schottky contact ($W_{\rm LSCH} = 10$ nm) is placed on the top of the epilayer, while the ohmic contact is located directly on the substrate separated from the epilayer by the dielectric. The Schottky contact is modeled as a perfect absorbing boundary, that is, all the carriers reaching the electrode leave the structure while no carriers are injected [9], [11], [15]–[17]. The ohmic contact imposes charge neutrality in the proximity of the electrode by injecting carriers with the appropriate velocity distribution at the lattice temperature [18].

As we focus on the analysis of EEs on the junction capacitance as a function of the applied voltage in reverse bias (C–V characteristics), and such effects are associated with the bias-induced variations of the lateral extension (beyond the Schottky contact) of the depletion region created by the applied voltage, it is necessary to correctly model the surface effects at the semiconductor interfaces. We will, therefore, include in our simulations surface charges at the semiconductor–dielectric interfaces σ, in particular, at the free surfaces of the epilayer and the substrate in contact with the dielectric, as indicated in Fig. 1 with a red line.

Two models for the simulation of the surface effects are considered: 1) a simple constant surface-charge model (CCM) and 2) the so-called self-consistent surface-charge model (SCCM). Within the CCM, we manually fix a value for the negative surface-charge density, which does not depend on the position or the bias. The value of the surface charge σ considered in the MC simulator will be related to that of the corresponding surface potential $V_{\rm S}$ by

$$\sigma = -\sqrt{2qN_{\rm D}|V_{\rm S}|\epsilon_{\rm SC}} \tag{1}$$

where q is the electron charge, $N_{\rm D}$ is the doping, and $\epsilon_{\rm SC}$ is the permittivity of the semiconductor, which takes values of $\epsilon_{\rm GaAs} = 12.9$ in GaAs and $\epsilon_{\rm GaN} = 8.9$ in GaN.

On the other hand, the more realistic SCCM self-consistently updates the value of σ locally (without considering the details of electron trapping/detrapping dynamics), according to the number of carriers present near the semiconductor interfaces [19]. Thus, the local values of σ are consistent with the electron distribution for every bias condition, as well as adapted to the geometry of each structure. The validity of the SCCM has been previously confirmed by reproducing the experimental results in devices in which surface charge effects play a key role in their electrical behavior [19]–[22]. This model is also able to correctly account for the virtual gate effect [23] and to modulate the occupation of the surface states as experimentally observed in [24]. The price to pay in order to obtain more realistic results with the SCCM is that the time-domain updating process of σ involves a significant increase in the computation time with respect to the CCM.

The MC simulator allows us to evaluate the total charge inside the SBD at each bias point just by adding up the number of electrons in all the meshes. Thus, the bias-dependent capacitance is calculated as the variation of the total charge in the structure per unit voltage. In addition, this method allows us to locate the regions of the SBD contributing to the total capacitance, which corresponds to those where the depletion region is modified when changing the bias and, thus, identify the origin of the 2-D fringing capacitances and the influence

of surface charges. The ideal value of the charge (per unit length in the nonsimulated dimension, given in C/m) in the depletion region generated by the Schottky contact when EEs are not present Q_{Id} is given by

$$Q_{\mathrm{Id}}(V) = -L_{\mathrm{SCH}} q N_{\mathrm{E}} W(V) \tag{2}$$

where

$$W(V) = \sqrt{2\epsilon_{\mathrm{SC}}(V_{\mathrm{b}} - V)/qN_{\mathrm{E}}} \tag{3}$$

is the depth of the depletion region, with V_{b} being the built-in voltage of the Schottky contact and V being the voltage applied to the anode (Schottky contact) with the ohmic contact grounded.

It has been previously demonstrated [6], [25]–[27] that the additional charge originated by EEs can be modeled by a charge term associated with the 2-D geometry of the diode, i.e., to the lateral extension of the depletion region. If we include this term in (2), the total depleted charge $Q(V)$ is obtained

$$Q(V) = -L_{\mathrm{SCH}}\sqrt{2\epsilon_{\mathrm{SC}} q N_{\mathrm{E}}(V_{\mathrm{b}} - V)} + \beta \cdot \epsilon_{\mathrm{SC}}(V - V_{\mathrm{b}}) \tag{4}$$

where β is the dimensionless EE parameter. This term is, in principle, independent of the anode size and the epilayer doping. However, as observed in [9], it strongly depends on the presence or absence of surface charges at the epilayer.

With the results of the MC simulations, we compute the charge depleted below the Schottky contact Q_{MC} at a given applied voltage V as the difference between the total charge for that V and that in flat-band conditions ($V = V_{\mathrm{b}}$). Then, as in [9], β is calculated from the slope of the representation $(Q_{\mathrm{MC}} - Q_{\mathrm{Id}})$ versus $(V - V_{\mathrm{b}})$.

The value of the junction capacitance $C(V) = dQ(V)/dV$, including the 2-D EE correction, can be obtained from (4) as

$$C(V) = C_{\mathrm{Id}}(V) + C_{\mathrm{EE}} = L_{\mathrm{SCH}}\frac{\epsilon_{\mathrm{SC}}}{W(V)} + \beta \cdot \epsilon_{\mathrm{SC}} \tag{5}$$

where $C(V)$, $C_{\mathrm{Id}}(V)$, and C_{EE} are the total, ideal, and EE capacitances, respectively, per unit length in the nonsimulated dimension (given in F/m). Equation (5) indicates that the deviation from the ideal capacitance due to the 2-D geometry of the diode is a bias-independent contribution, $C_{\mathrm{EE}} = \beta \cdot \epsilon_{\mathrm{SC}}$, proportional to the permittivity of the semiconductor, and characterized by β, whose value and the parameters in which it depends will be analyzed in Section III.

Finally, it is necessary to remark that the correct analysis of the junction capacitance (and the depleted region) of the devices requires the precise calculation of the $n^+ - n$ diffusion voltage V_{n^+-n}. For that sake, we have performed exhaustive 1-D simulations of the $n^+ - n$ junction without the Schottky contact, with just a grounded ohmic contact placed at the boundary of the n^+ region. The value of V_{n^+-n} for each epilayer doping and semiconductor type was then calculated taking the (absolute) value of the (floating) electric potential at the boundary of the n region, which also accounts for a small potential drop of some mV at the ohmic contact, always present even if the contact is carefully modeled, as in [18]. In the simulations, $V_{n^+-n} + V_{\mathrm{b}}$ is the voltage to be considered as Dirichlet boundary condition at the ohmic contact, while the bias voltage V is applied at the Schottky contact.

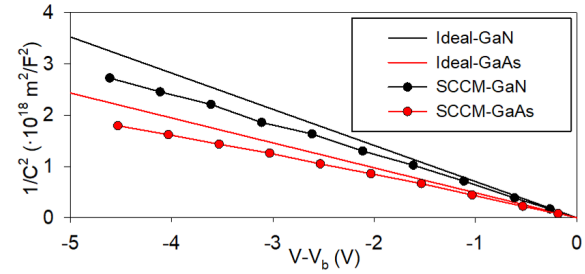

Fig. 2. Ideal and MC results of $1/C^2$ for both GaAs and GaN Schottky diodes with epilayer doping $N_{\mathrm{E}} = 10^{17}$ cm^{-3}.

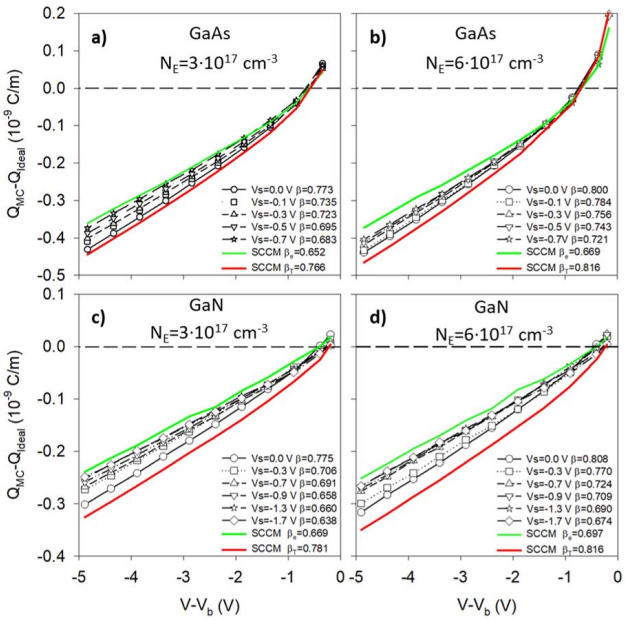

Fig. 3. EEs charge contribution due to the 2-D geometry of the Schottky diode for (a) and (b) GaAs and (c) and (d) GaN for a different N_{E}. The results of the CCM with different values of V_{s} are plotted with symbols, while those obtained with the SCCM are plotted with solid lines (green when just considering the electron charges and red when adding the contribution of the surface charges σ).

III. Results

In order to evidence the significant deviation from the ideal C–V characteristics of real GaN and GaAs SBDs, Fig. 2 shows the comparison between the ideal values of $1/C^2$ versus $V - V_{\mathrm{b}}$ (with a perfectly linear dependence) and those obtained by MC simulations for both diodes with $N_{\mathrm{E}} = 10^{17}$ cm^{-3}. As expected, due to its lower permittivity, the capacitance is smaller for the GaN SBD, and due to the presence of EEs, the MC capacitance is higher than the ideal one.

The EE parameter β is calculated from the slope of the excess charge per unit length $Q_{\mathrm{EE}} = Q_{\mathrm{MC}} - Q_{\mathrm{Id}}$ as a function of $V - V_{\mathrm{b}}$ since, according to (4), $Q_{\mathrm{EE}} = \beta \cdot \epsilon_{\mathrm{SC}}(V - V_{\mathrm{b}})$. Fig. 3 shows how these curves are perfectly linear when using both the CCM and SCCM, but only above a certain reverse bias, since current starts to flow when approaching flat band conditions, and the theory explained before does not hold anymore. Within the CCM, we have considered values of the surface potential V_{s} ranging from zero ($\sigma = 0$, no surface charge) to that corresponding to half of the bandgap of the semiconductor (-0.7 V in GaAs and -1.7 V in GaN) so

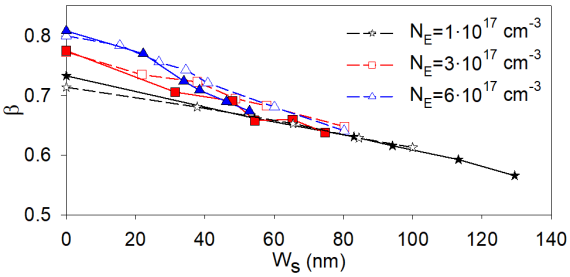

Fig. 4. Dependence of the EE parameter β on W_s, considering the CCM with different values of V_s for GaAs (dashed lines, open symbols) and GaN (solid lines, closed symbols).

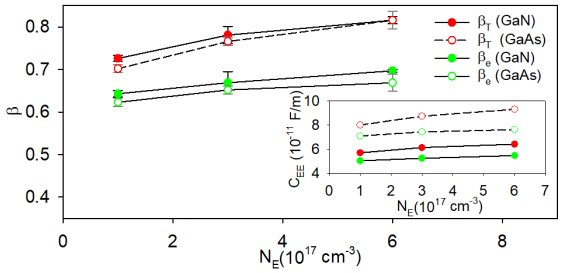

Fig. 5. EE parameters β_T and β_e versus N_E, considering or not, respectively, the contribution of the surface charge for GaN and GaAs, calculated with the SCCM. The inset shows the EE capacitance C_{EE}.

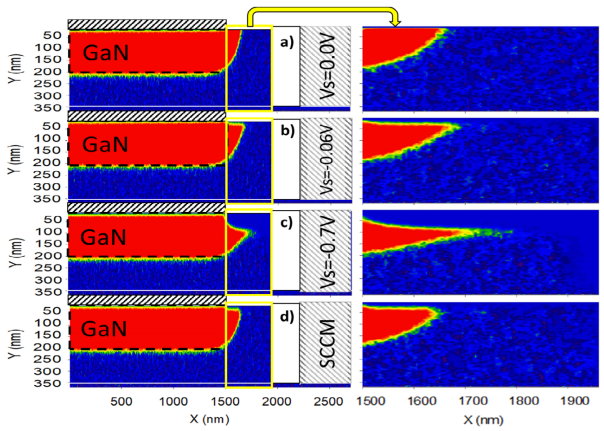

Fig. 6. Map of the local contribution to the total capacitance per unit length (calculated as the variation of the electron charge per unit length between flat-band conditions and the bias point V−V_b = −4.0 V, divided by the voltage difference, for the GaN SBD with N_E = 10^{17} cm^{-3}. Results are calculated with the CCM for (a) V_s = 0 V, (b) V_s = −0.06 V, (c) V_s = −0.7 V, and (d) with the SCCM. The red color represents the region where the electron charge is modified by the bias. The positions of the dielectric, the epilayer, and the Schottky and ohmic contacts are shown. The dashed rectangular zone indicates the depletion region expected for an ideal parallel plate capacitor so that the EEs can be visualized as the part of the depletion region outside this area. The figures on the right column show a zoomed-in view of the EEs region between the Schottky contact and the dielectric (solid rectangles in the left figures).

that the increasing depletion induced by the surface charges decreases the (absolute) value of Q_{EE}, as shown in Fig. 3.

The values of β, calculated from the results of Fig. 3, in the linear range (without increasing too much the reverse applied voltage since it would make the depletion region reach the substrate) are shown in Fig. 4 for both GaAs and GaN SBDs and for different values of N_E (10^{17}, $3{\cdot}10^{17}$, and $6{\cdot}10^{17}$ cm^{-3}). Notice that the dimensions of the diode, in particular $L_{EP} = 460$ nm, have been chosen to be large enough to have no influence on the depletion region generated around the edge of the Schottky contact, even for the highest bias.

According to our previous studies, performed in GaAs SBDs [9], the dependence of β on V_s could be considered as independent of the properties of the semiconductor beneath the contact. Nevertheless, when simulating GaN SBDs, we have noticed that the expression of $\beta(V_s)$ in [9] is no longer valid since the depletion region imposed by the surface charge depends on the dielectric constant of the epilayer ϵ_{SC} as well as of the doping level N_E. That is why, in Fig. 4, the values of β calculated for both SBDs with different values of V_s and N_E are plotted as a function of the depth of the depletion region imposed by the surface potential W_s given by $W_s = (2\epsilon_{SC}|V_s|/qN_E)^{1/2}$.

Significantly, β takes similar values for a different N_E in both GaAs and GaN SBDs for $W_s > 30$–40 nm and not much dependent on the epilayer doping. On the contrary, for low values of σ, β increases with the epilayer doping. This happens because of the coupling of the electric field between the Schottky contact and the semiconductor through the top dielectric, therefore adding an "extrinsic" contribution to the EE capacitance (in addition to the "intrinsic" one provided by the coupling through the semiconductor). Fig. 4 shows that this "extrinsic" coupling, which depends mainly on the permittivity of the dielectric and the thickness of the Schottky contact, is enhanced when N_E increases and, on the contrary, is screened when a high value of the surface charge is used.

When using the SCCM (see Fig 3), the variations with the bias of the total charge inside the device have two contributions: one given by the change in the number of electrons and a second one provided by the variation of the surface charge (not present with the CCM since surface charges are fixed). We separately compute those two contributions in order to extract the values of two EE parameters: β_e and β_T, corresponding to the variations of the free electron charge and of the total one (adding the change of the surface charges), respectively. Both values are plotted in Fig. 5 as a function of N_E. Due to the lack of precision in the calculation of the variations of the surface charges, we have made several simulations in order to extract the average value and error bars, also plotted.

The EE parameters β_T and β_e in Fig. 5 can be associated with the values of the capacitance expected when operating at low (LF) and high frequencies (HF), respectively. The variation of the surface charge is the result of the trapping/release of electrons in deep trap states, a very slow process compared with electron motion. Therefore, this contribution to the capacitance is only expected to be present when an LF ac excitation is applied, and the LF-EEs can be characterized by β_T. For HF (above some megahertz), the surface charges cannot follow the excitation so that the only expected contribution is that from the free electrons, and β_e is the significant value. Since SBDs are typically employed for HF applications, the practical value to be used is β_e. Fig. 5 shows that the values of both β_T and β_e are slightly higher for GaN than for GaAs due to its lower permittivity, which implies a stronger influence of the coupling through the top dielectric and, thus, a higher

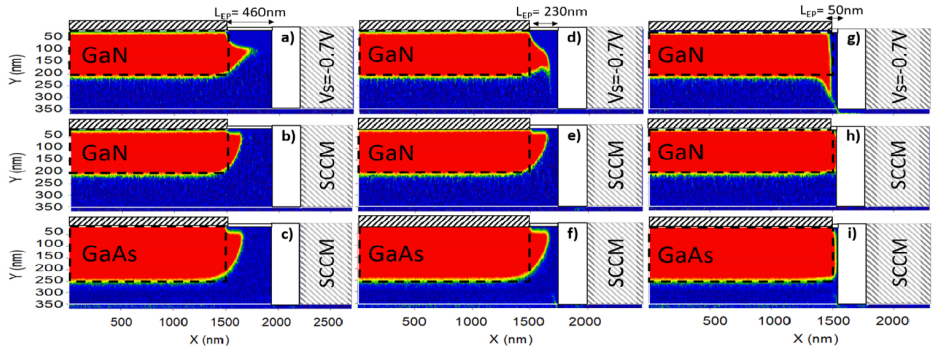

Fig. 7. Map of the local contribution to the total capacitance as in Fig. 6 for (a), (b), (d), (e), (g), and (h) GaN and (c), (f), and (i) GaAs diodes with $N_E = 10^{17}$ cm^{-3} and different values of L_{EP}: (a)–(c) $L_{EP} = 460$ nm, (d)–(f) 230 nm, and (g)–(i) 50 nm; calculated with (a), (d), and (g) CCM and $V_s = -0.7$ V and (b), (c), (e), (f), (h), and (i) SCCM.

"extrinsic" contribution to the EE capacitance. The smaller value of ϵ_{SC} makes that, in spite of the similar values of that the EE parameters take in both semiconductors, the EE capacitance is much lower for GaN since $C_{EE} = \beta \cdot \epsilon_{SC}$, as observed in the inset of Fig. 5.

The values of β_T obtained with the SCCM are very similar to those calculated by means of the CCM when $\sigma = 0$, Fig. 4. This can be explained by the fact that within the SCCM, σ disappears at the interfaces in contact with the depletion region, in contrast with a constant surface charge within the CCM. Focusing on β_e, which ignores the variations of σ, its value is much lower, in the range of those obtained with the CCM for surface depletion widths of 70–90 nm. However, this is not coherent with the smaller values of W_s resulting from the SCCM, approximately between 12 nm (for GaN with $N_E = 6 \cdot 10^{17}$ cm^{-3}) and 45 nm (for GaAs with $N_E = 10^{17}$ cm^{-3}), what indicates that the electric field distribution and the shape of the depletion region must be different in both cases.

In order to understand this effect, Fig. 6 shows maps with the local contribution of electrons in the different regions of the GaN SBD (with $N_E = 10^{17}$ cm^{-3}) to the total capacitance per unit length. The different estimation of the EEs associated with the electron concentration within the CCM and SCCM is evident when comparing Fig. 6(c), obtained with the CCM using $V_s = -0.7$ V (corresponding to a value of W_s of about 8 nm), and Fig. 6(d), obtained with the SCCM (resulting in a W_s of about 20 nm), both providing a similar value of β_e. The shape of the depletion region at the side of the Schottky contact is completely different: within the CCM, its lateral extension is longer so that covering the same surface (which corresponds to the electron charge and, therefore, to β_e in the SCCM), and σ must be higher than the value resulting from the SCCM. This different shape comes from the fact that within the SCCM, σ is null at the interfaces in contact with the depletion region, thus decreasing the lateral extension of the depletion layer and, thus, being similar to the CCM case with $\sigma = 0$, as shown in Fig. 6(a). Even when using the CCM with a value of σ providing a depletion width of about 20 nm, the same that of the SCCM [corresponding to $V_s = -0.06$ V, see Fig. 6(b)], there are still differences between the CCM and SCCM, and the lateral extension of the depletion region is wider for the CCM due to the presence of the surface charges so that β_e is slightly higher. The value of β_T obtained with the SCCM coincides with the one obtained with the CCM for $\sigma = 0$. Notice that β_T is calculated as the addition of β_e (integral of the values shown in Fig. 6(d), with the same shape as those in (a), but without the contribution of the region near the top interface) plus the variation of the values of σ, which coincides with the CCM contribution of the region at the top of the depletion region that was not depleted with $\sigma = 0$ but was already depleted in flat band conditions when using the SCCM.

The previous results are valid as long as the epilayer size L_{EP} is large enough so that its vertical interface has no influence on the depletion region generated around the edge of the Schottky contact. In order to analyze the influence of this parameter, in Fig. 7, the contribution to the local capacitance (as in Fig. 6) is shown for GaN and GaAs diodes with $L_{EP} = 460$, 230, and 50 nm (while L_{Diel} is kept as 240 nm). As observed, when decreasing the value of L_{EP}, the CCM provides nonphysical results, giving rise to a downward bending of the depletion region [see Fig. 7(d) and (g)] in clear evidence that more detailed methods, such as the SCCM, must be used in order to correctly take into account the surface effects in small devices. As expected, due to its higher permittivity, the depletion region is larger for GaAs (3) so that this effect appears for longer L_{EP} than in GaN. We remark that we have confirmed that β_e (and, therefore, C_{EE}) is independent of the bias as long as L_{EP} is large enough. However, this is not valid anymore if L_{EP} becomes too small since the influence of the vertical sidewall of the epilayer will be effective when increasing the applied voltage, thus decreasing β_e (and, therefore, C_{EE}).

When focusing on the results obtained with the SCCM for different values of L_{EP}, Fig. 7 shows that EEs are reduced when L_{EP} is decreased. In fact, when reaching the limit $L_{EP} = 0$, the EEs are completely suppressed [see Fig. 7(h) and (i)]. In order to better analyze the dependence of the EEs on L_{EP}, the values of β_e calculated within the SCCM are shown in Fig. 8 for both GaAs and GaN SBDs. For large values of L_{EP} (when the depletion region is not affected by the vertical interface of the epilayer), the value of β_e is almost independent on N_E for both GaAs and GaN diodes, taking values around 0.6 in both cases. For small values of L_{EP}, β_e dramatically decreases. This geometrical limit depends on N_E,

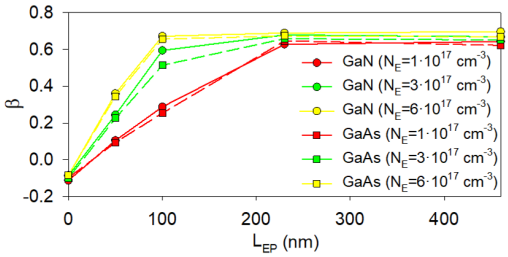

Fig. 8. β_e calculated considering the SCCM in both GaAs and GaN SBDs for a different N_E versus L_{EP}.

it is below 100 nm for $N_E = 6 \cdot 10^{17}$ cm^{-3} and around 200 nm for $N_E = 10^{17}$ cm^{-3}. Note that for $L_{EP} = 0$, the depletion region due to the surface charges at the vertical sidewall of the epilayer reduces the contribution to the capacitance of a narrow part of the region below the Schottky contact. In such a case, the depletion region becomes slightly smaller than the rectangular one associated with the ideal parallel plate capacitor, thus providing small negative values for β_e. This means that the EEs could be technologically suppressed or even inverted $\beta_e < 0$, by means of a self-aligned etching of the epilayer, aiming to produce devices with $L_{EP} = 0$.

IV. Conclusion

By means of 2-D MC simulations, we have analyzed surface-charge effects and the associated fringing capacitance in GaAs and GaN planar SBDs. Due to the EEs, the 2-D shape of the depletion region located under the Schottky contact differs from its ideal rectangular shape, this effect being at the origin of higher values of the capacitance. The EE contribution C_{EE} has been characterized by an EE parameter called β, which strongly depends on the surface-charge effects. Two surface-charge models have been used for the analysis. The CCM provides a value of β just depending on W_s, regardless of the epilayer doping and semiconductor type, as long as σ is high enough to screen the "extrinsic" contribution through the top dielectric. However, this simple CCM can only be employed if the depletion region is not affected by the lateral extension of the epilayer, this is, for $L_{EP} >$ 100–200 nm (depending on the value of N_E and the applied bias). The SCCM is able to discriminate the HF capacitance, coming from the variation of the electron charge and characterized by β_e, and an LF component, coming from the variation of the surface charges (traps involving long-time processes), which adds to the previous one to provide the total EEs characterized by β_T. Using this realistic model, we have demonstrated that by reducing the value of L_{EP}, EEs can be minimized so that for $L_{EP} = 0$ nm, β_e becomes even negative since the depletion region associated with the vertical sidewalls of the epilayer affects the region below the Schottky contact.

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