Implementation of 8-Point Slantlet Transform Based Polynomial Cancellation Coding-OFDM System Using FPGA

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ABSTRACT:

The objective of this paper is to implement a baseband OFDM transceiver on FPGA hardware. The design uses 8-point SLT/ISLT (Slantlet/Inverse Slantlet) for the processing module with processing block of 8 inputs data wide. All modules are designed and implemented using VHDL programming language. Software tools used in this work includes Altera Quartus II 7.2 and ModelSim Altera 6.1g, to assist the design process and downloading process into FPGA board while Cyclone III board EP3C120F780C7 is used to realize the designed module.

KEYWORDS: OFDM, PCC, FPGA and Slantlet Transform.

1. INTRODUCTION:

Orthogonal Frequency Division Multiplexing (OFDM) is a multi-carrier modulation technique which divides the available spectrum into many carriers, by spacing the channels much closer together and making all carriers orthogonal to one another to prevent interference between the closely spaced carriers. The main advantage of OFDM is their robustness to channel fading in wireless environment [1]. One of the main disadvantages of (OFDM) is its high peak-to-average power ratio (PAPR). OFDM transmitters therefore require very linear output amplifiers with wide dynamic range, these are expensive and inefficient [2].

The other limitation of OFDM in many applications is that it is very sensitive to frequency errors caused by frequency differences between the local oscillators in the transmitter and receiver. In the mobile radio environment relative movement between transmitter and receiver causes Doppler frequency shifts. These random frequency errors in OFDM system distort orthogonality between subcarriers and thus inter-carrier interference (ICI) occurs [1].

Polynomial cancellation coding (PCC) is a very efficient technique proposed recently, and provides several benefits for OFDM. An OFDM system with PCC is named polynomial cancellation coded OFDM (PCC-OFDM), which reduces intercarrier interference (ICI). Moreover, it reduces out-of-band power and ISI in OFDM system. Used in its simplest form, PCC achieved these advantages at the cost of bandwidth efficiency. The main idea of PCC is to map each complex number which is to be transmitted onto a group of subcarriers, with appropriate weightings, rather than to a single subcarrier [3].

Recently, I. W. Selesnick has constructed the new orthogonal discrete

wavelet transform called the Slantlet (SLT), with two zero moments and with improved time localization. This transform method has played an important role in signal and image processing applications; it has been successfully applied in compression and denoising [4].

In the next two sections, a brief description to PCC coding and Slantlet Transform used for OFDM system are presented. Then a detail description to FPGA implementation of Slantlet PCC-OFDM system is also presented.

2. POLINOMIAL CANCELLATION CODING (PCC):

PCC is a coding method for OFDM in which the information to be transmitted is modulated onto weighted groups of subcarriers rather than onto individual subcarriers [5]. Weighting are the coefficients of Binomial series [6]**:**

$$(1-x)^{m-1} = 1-(m-1)x+(m-1)(m-2)\frac{x^2}{2}+\cdots \qquad \ldots(1)$$

e.g.: groups of two weighted (pair) subcarriers, *m*=2;

$(1-x)^1 = 1-x$ weightings are **+1** , **-1**.

groups of three weighted subcarriers, *m*=3;

$(1-x)^2 = 1-2x+x^2$ weightings are **+1** , **-2** , **+1**.

Note that the sum of weightings is zero. The case study in this work is a group of pair subcarriers (i.e. M=2**n*, where M is the number of PCC outputs and *n* is the number of PCC inputs), for normal OFDM M=*n*. The way in which PCC and DePCC mapping is calculating, illustrated using the following Eqs. [5,7]:

For PCC mapping

$$\left.\begin{aligned} p_{2\times i-1} &= (-1)^{i+1}u_i \\ p_{2\times i} &= (-1)^i u_i \end{aligned}\right\} \; i = 1,2,\cdots,n \qquad \ldots(2)$$

For DePCC mapping

$$v_i = \frac{r_{2\times i-1} - r_{2\times i}}{2} \qquad i = 1,2,\cdots,n \qquad \ldots(3)$$

PCC-OFDM can be understood by considering the result of weighted pairs of subcarriers in the frequency domain and in the time domain. In OFDM, the spectrum of each subcarrier has a sin(x)/x form. Figure (1) shows how the weighting of a pair of subcarriers in PCC results in a canceling of the sidelobs and a very much faster overall spectral roll off. As a result, the overall power spectrum of a PCC-OFDM signal with mapping onto pairs of subcarriers falls off as $1/(N^3 f^4)$ compared with $1/(Nf^2)$ for standard OFDM [8].

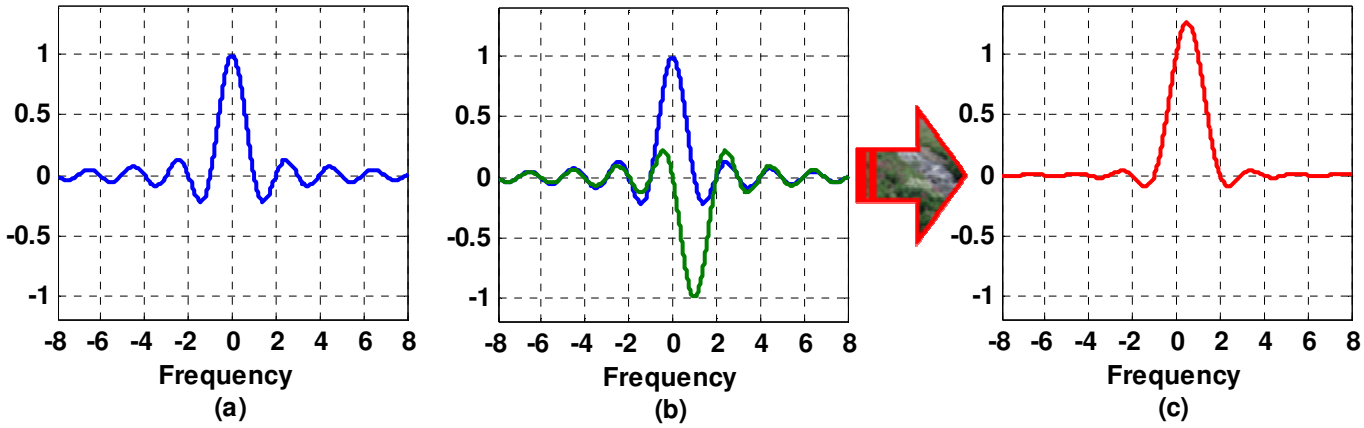


Figure 1: PCC-OFDM in the frequency domain (spectra of subcarriers) [8].
(a) One subcarrier.
(b) Two adjacent subcarriers, and
(c) Sum of weighted pair of subcarriers.

Figure (2) shows the combination of the real components of two adjacent subcarriers with opposite weighting, noting the sinusoidal envelope. This results in most of the energy of a PCC-OFDM symbol being concentrated in the center of the symbol period. This also means that PCC-OFDM is much less sensitive to ISI due to multipath transmission [8].

3. SLANTLET FILTERBANK:

The Slantlet Transform (SLT) is an orthogonal Discrete Wavelet Transform (DWT) with two zero moments, improved time localization, and is based on designing different filters that are not product for each scale instead of using filterbank iteration [4].

In general, the algorithm to obtain the l-scale Slantlet filterbanks is, as follows:

- The l -scale Slantlet has $2l$ filterbanks. The first filterbank is called the low pass filter (LPF), and its transfer function is $h_l(n)$. The adjacent to the LPF filterbank has transfer function $f_l(n)$. Both $h_l(n)$ and $f_l(n)$ are to be followed by down sampling of 2^l.
- The remaining $2l$ -2 filterbanks, there transfer functions are $g_i(n)$ and its shifted time reverse $g_i((2^{i+1}-1)-n)$ for $i= l$ -1, l -2,…,1. Each $g_i(n)$ and its shifted time reverse are to be followed by down sampling of 2^{i+1} for each value i.

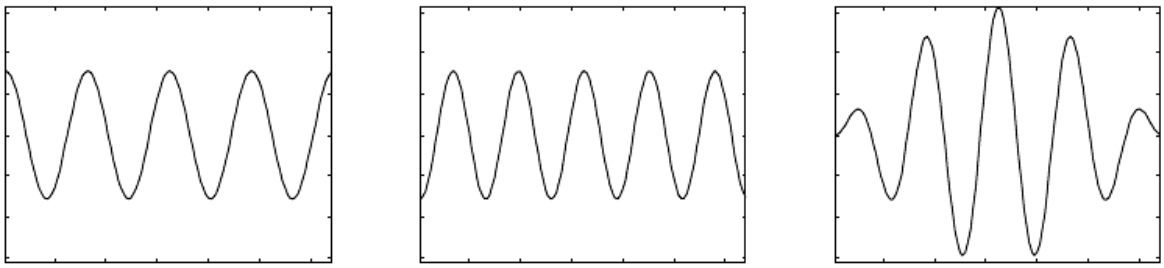
In the Slantlet filterbank, each $g_i(n)$ appears with its time reverse $g_i((2^{i+1}-1)-n)$, while $h_l(n)$ does not appear with its time reverse, instead it always appears paired with the filter $f_l(n)$. The transfer functions $h_l(n)$, $f_l(n)$ and $g_i(n)$ for l-scale Slantlet are calculated using the following expressions and the parameters in Tables (1) and (2) [4]:

$$h_l(n)=\begin{cases} b_{0,0}+b_{0,1}n, & for\ n=0,\cdots 2^l-1 \\ b_{1,0}+b_{1,1}(n-2^l), & for\ n=2^l,\cdots 2^{l+1}-1 \end{cases} \quad \ldots(4)$$

$$f_l(n)=\begin{cases} c_{0,0}+c_{0,1}n, & for\ n=0,\cdots 2^l-1 \\ c_{1,0}+c_{1,1}(n-2^l), & for\ n=2^l,\cdots 2^{l+1}-1 \end{cases} \quad \ldots(5)$$

$$g_i(n)=\begin{cases} a_{0,0}+a_{0,1}n, & for\ n=0,\cdots 2^i-1 \\ a_{1,0}+a_{1,1}(n-2^i), & for\ n=2^i,\cdots 2^{i+1}-1 \end{cases} \quad \ldots(6)$$

Figure (3) shows the third-scale Slantlet filterbanks and their transfer functions where l = 3 and i = 2,1. That is; third-scale Slantlet filterbanks has $h_3(n)$,



One symbol period **(a)**

One symbol period **(b)**

One symbol period **(c)**

Figure 2: PCC-OFDM in the time domain [8].

(a) One subcarrier.
(b) Next subcarriers with opposite polarity.
(c) Sum of pair of subcarriers.

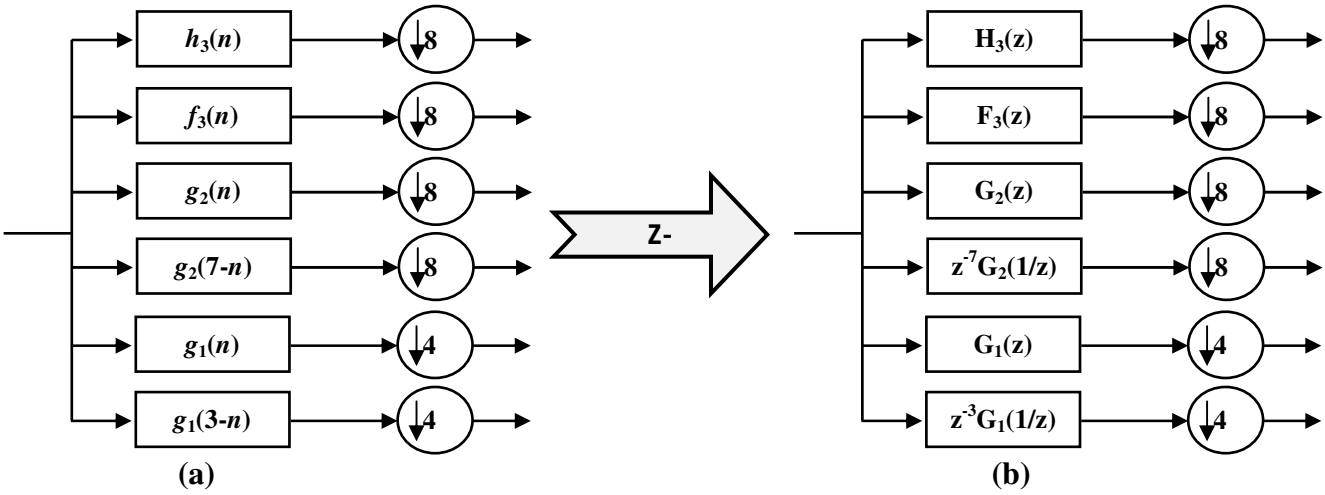


Figure 3: Three-scale Slantlet filterbank [4].
(a) Transfer functions of Slantlet filterbanks.
(b) Slantlet filterbanks after z-transform.

$f_3(n)$, $g_2(n)$ with its shifted time-reverse $g_2(7\text{-}n)$ each of these transfer functions followed by **8** down sampling, and $g_1(n)$ with its shifted time-reverse $g_1(3\text{-}n)$ each followed by **4** down sampling.

Using Eq. (4), (5), (6) and Tables (1), (2) to obtain the transfer functions $h_3(n)$, $f_3(n)$, $g_2(n)$ and $g_1(n)$, can be obtained as follows:

$$h_3(n) = 0.1670\,\delta(n) + 0.2112\,\delta(n-1) + 0.2554\,\delta(n-2) + 0.2996\,\delta(n-3) + 0.3438\,\delta(n-4) + 0.3880\,\delta(n-5) + 0.4322\,\delta(n-6) + 0.4764\,\delta(n-7) + 0.1866\,\delta(n-8) + 0.1424\,\delta(n-9) + 0.0982\,\delta(n-10) + 0.0540\,\delta(n-11) + 0.0098\,\delta(n-12) - 0.0344\,\delta(n-13) - 0.0786\,\delta(n-14) - 0.1228\,\delta(n-15) \quad \ldots(7)$$

$$f_3(n) = -0.0526\,\delta(n) - 0.0665\,\delta(n-1) - 0.0804\,\delta(n-2) - 0.0943\,\delta(n-3) - 0.1082\,\delta(n-4) - 0.1221\,\delta(n-5) - 0.1360\,\delta(n-6) - 0.1500\,\delta(n-7) + 0.5926\,\delta(n-8) + 0.4522\,\delta(n-9) + 0.3118\,\delta(n-10) + 0.1715\,\delta(n-11) + 0.0311\,\delta(n-12) - 0.1093\,\delta(n-13) - 0.24978(n-14) - 0.3901\,\delta(n-15) \quad \ldots(8)$$

$$g_2(n) = -0.5062\,\delta(n) - 0.0874\,\delta(n-1) + 0.3314\,\delta(n-2) + 0.7502\,\delta(n-3) - 0.0793\,\delta(n-4) - 0.1078\,\delta(n-5) - 0.1360\,\delta(n-6) - 0.1646\,\delta(n-7) \quad \ldots(9)$$

$$g_1(n) = -0.5062\,\delta(n) - 0.0874\,\delta(n-1) + 0.3314\,\delta(n-2) + 0.7502\,\delta(n-3) - 0.0793\,\delta(n-4) - 0.1078\,\delta(n-5) - 0.1360\,\delta(n-6) - 0.1646\,\delta(n-7) \quad \ldots(10)$$

4. SLANTLET BASED PCC-OFDM SYSTEM:

The SLT-based OFDM modulator and demodulator of the PCC-OFDM system are shown in Figure (4). PCC is to be added to the SLT-based OFDM system known as SLT based PCC-OFDM system and results in better performance to the system [9]. The block diagram of the Slantlet based PCC-OFDM system is depicted in Figure (5).

The processes of the S/P converter, the signal demapper and the insertion of training sequence are the same as in the FFT-OFDM system. Also, the zeros will be added as in the FFT based case and for the same reasons. Then, the PCC mapping and the inverse Slantlet transform (ISLT) will be applied to the signal. After that, the P/S converter will convert the OFDM symbol to its serial version and will be sent through the channel. At the receiver, also assuming synchronization conditions are satisfied, first S/P converts the OFDM symbol to parallel version. Then, the SLT will be performed. The zero pads will be removed and the other operations of the channel estimation, channel compensation, PCC demapper, signal demapper and P/S will be performed in a similar manner to that of the FFT-based OFDM.

5. FPGA IMPLEMENTATION OF SLT BASED-OFDM SYSTEM WITH SIMULATION RESULTS:

Table 1: $h_l(n)$ and $f_l(n)$ parameters [4].			
$m = 2^i$			
$u = 1/\sqrt{m}$	$v = \sqrt{(2m^2 + 1)/3}$	$q = \sqrt{3/(m\,(m^2 - 1))}/m$	
$b_{0,0} = u(v + 1)/(2m)$	$b_{1,0} = u - b_{0,0}$	$b_{0,1} = u/m$	$b_{1,1} = -b_{0,1}$
$c_{0,1} = q\,(v - m)$	$c_{1,1} = -q\,(v + m)$	$c_{1,0} = c_{1,1}\,(v + 1 - 2m)/2$	$c_{0,0} = c_{0,1}\,(v + 1)/2$

Table 2: $g_i(n)$ parameters [4].			
$m = 2^i$			
$s_1 = 6\sqrt{m/\left((m^2 - 1)(4m^2 - 1)\right)}$		$s_0 = -s_1.\,(m - 1)/2$	
$t_1 = 2\sqrt{3/\left(m\,(m^2 - 1)\right)}$		$t_0 = ((m + 1)\;s_1/3 - m\,t_1)(m - 1)/(2m)$	
$a_{0,0} = (s_0 + t_0)/2$	$a_{0,1} = (s_1 + t_1)/2$	$a_{1,0} = (s_0 - t_0)/2$	$a_{1,1} = (s_1 - t_1)/2$

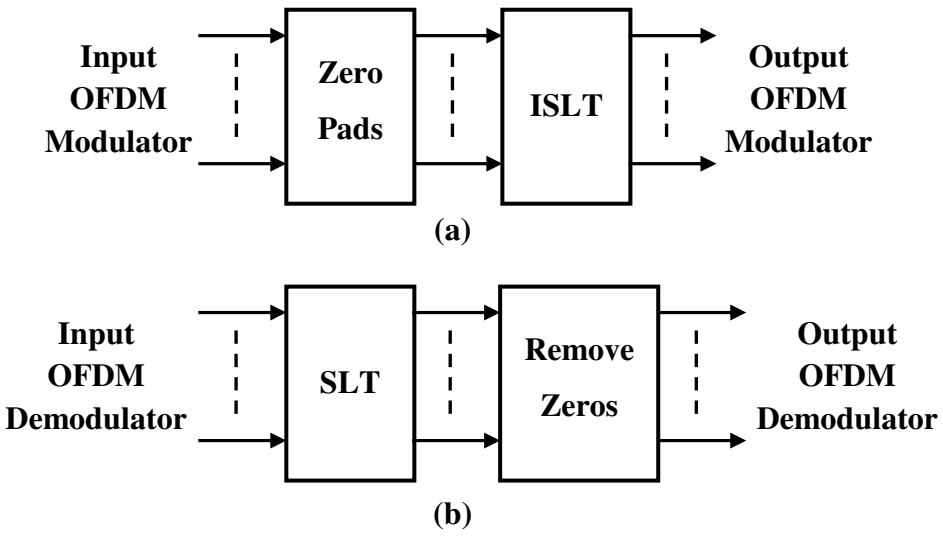


Figure 4: **(a)** SLT-based OFDM modulator.

(b) SLT-based OFDM demodulator [9].

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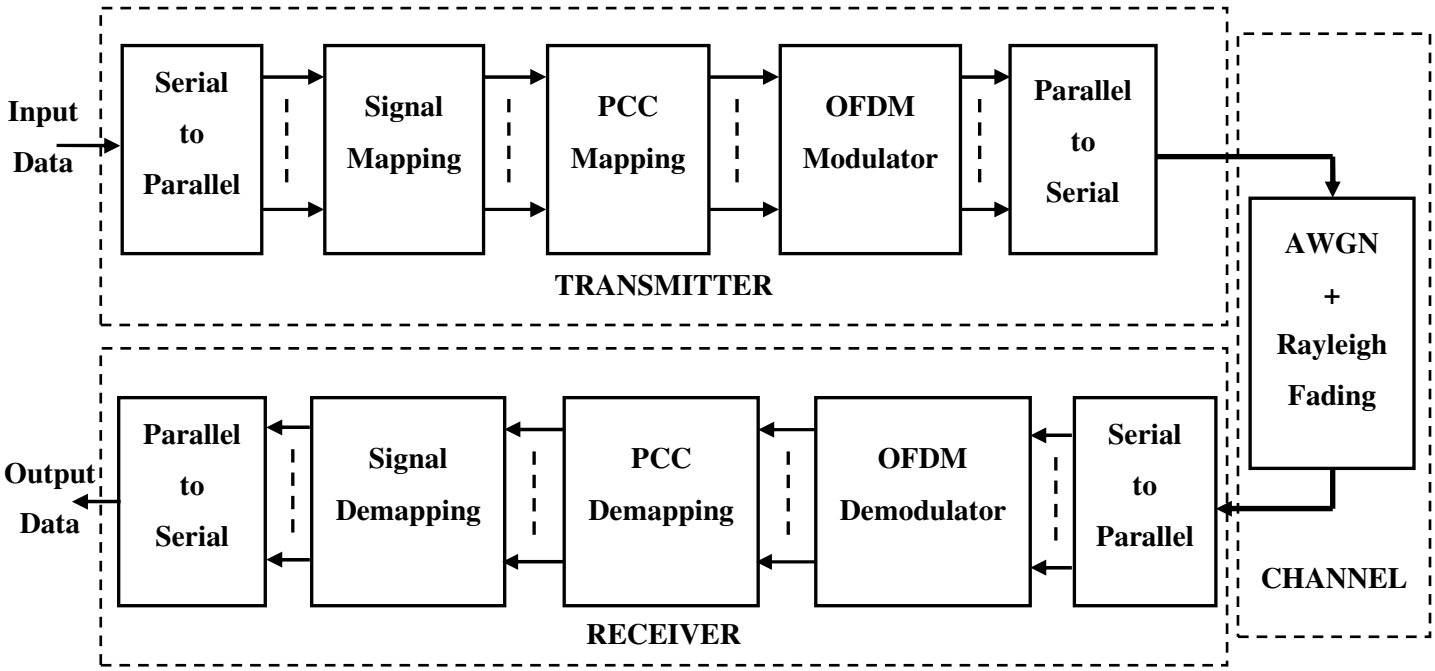

Figure 5: Slantlet based PCC-OFDM system [9].

The implementation of SLT based PCC-OFDM system consists of two parts; the transmitter and the receiver. Detailed descriptions of each part are presented in the next subsections:

- **The Transmitter Section:**

Seven main stages have been implemented in whole transmitter, named: S/P, SM, PCC, ZP, ISLT, P/S and LEDs display, are shown in Figure (6). In Quartus II, the transmitter structure has three main blocks labeled: ***SE2PA_T***, ***Transsaf*** and ***seven_segment***. Figure (7) shows the top-level design file for the implementation of the transmitter and pins location after successful compilation.

Using QUARTUS II software package provided by Altera, VHDL design modules are written for each of block entities. At the top level of design, a schematic file is created to assign input and output pins as it looks like in the chip.

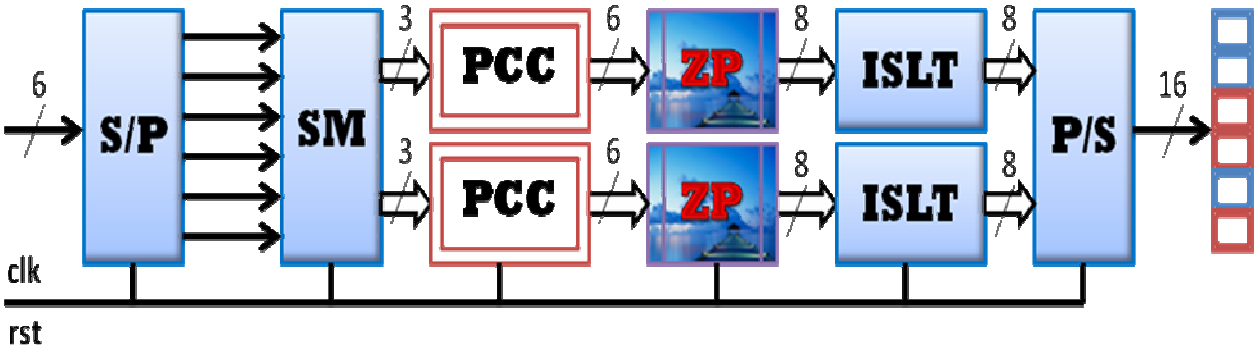

Figure 6: Transmitter design flow.

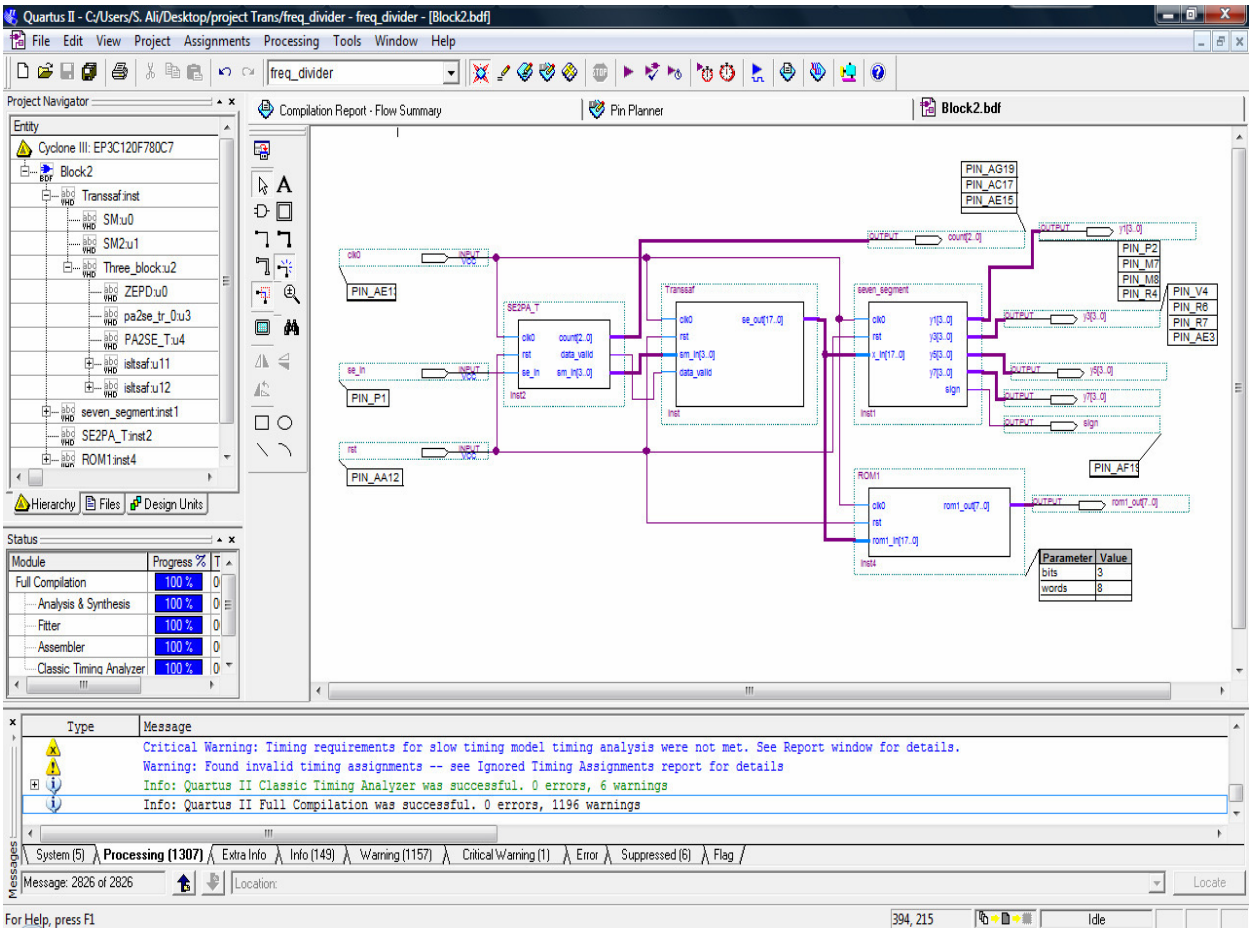

Figure 7: Top-level design of the FPGA implemented transmitter.

After the serial input data is converted to parallel ones, entered to the ***Transsaf*** Block that contains four components named: ***SM***, ***SM2***, ***PCC*** and ***Three_block***. The first two components are the signal mapping (***SM*** and ***SM2*** entities), ***SM*** entity converts each two adjacent bits into symbol ones (for 4QAM, symbol range will be 0, 1, 2 and 3), according to Table (3). The length of its output symbol is half than the length of the inputs bits. After applying ***SM*** entity, another process named ***SM2*** is applied where each symbol is mapped to real and imaginary, as shown in Figure (8), according to Table (4).

- **Simulation Results of the Transmitter Section:**

The simulation results using ModelSim Altera 6.1g of ***SM*** and ***SM2*** is shown in Figure (9). Notice that, the output signals become active only when ***rst*** (reset) signal is '**0**', this fact is true for each part of the whole system. *Getg* is a sub function called by the ISLT and SLT transformers. Its input is only *i* which is an integer number like 1, 2, 3… etc., and its return values are a0, a1, b0, b1, a0r, a1r, b0r and b1r for each transform. Each of these previous values is of real form.

Figure (10) presents the direction of input and output of *Getg* function with ISLT and SLT transform. The last task in the SLT-OFDM modulator is the ISLT (inverse Slantlet transform). Two inputs have been entered to ***isltsaf*** component which are real input and imaginary input, each of it is the output of the ***ZEPD***, in addition to clk0 and ***rst*** inputs. Each output is of real type; therefore, the ISLT coefficients are scaled by 10^4 to overcome the synthesis problem (since real type is not synthesis). A comparison is made

Table 3: 4QAM Symbol.		
Bit1	**Bit2**	**Symbol**
0	**0**	**0**
0	**1**	**1**
1	**0**	**2**
1	**1**	**3**

Table 4: Signal mapping values.		
Symbol	**Real**	**Imaginary**
0	**-1**	**1**
1	**-1**	**-1**
2	**1**	**1**
3	**1**	**-1**

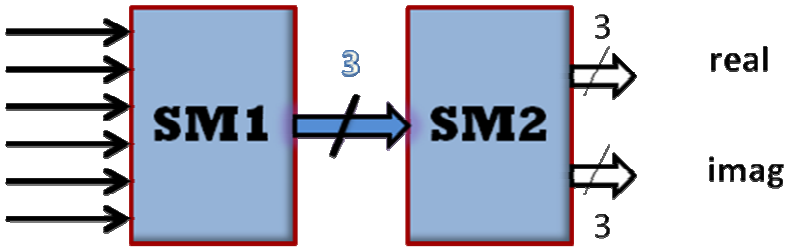

Figure 8: Signal mapping entities process.

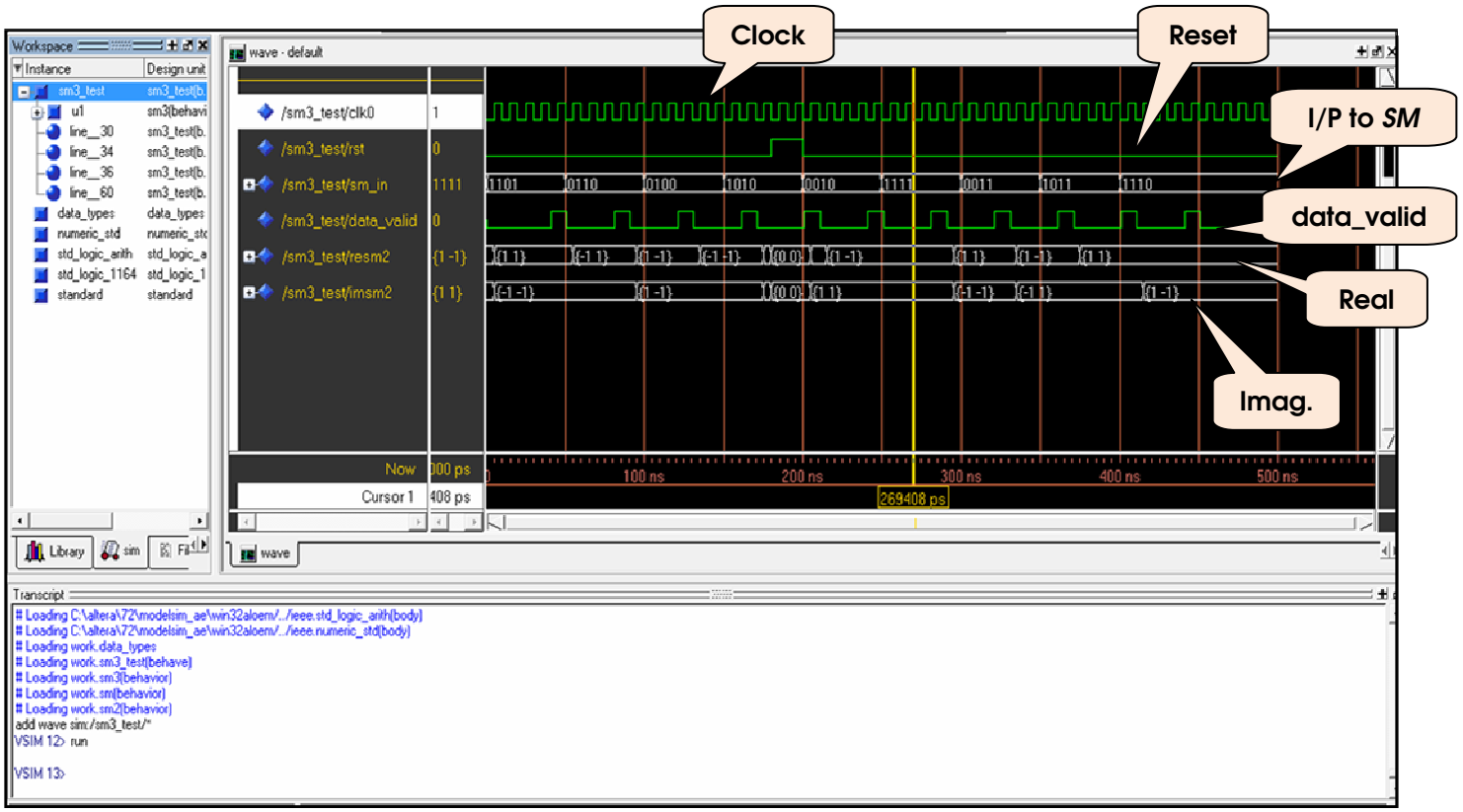

Figure 9: signal mapping entities input/output simulation waveforms.

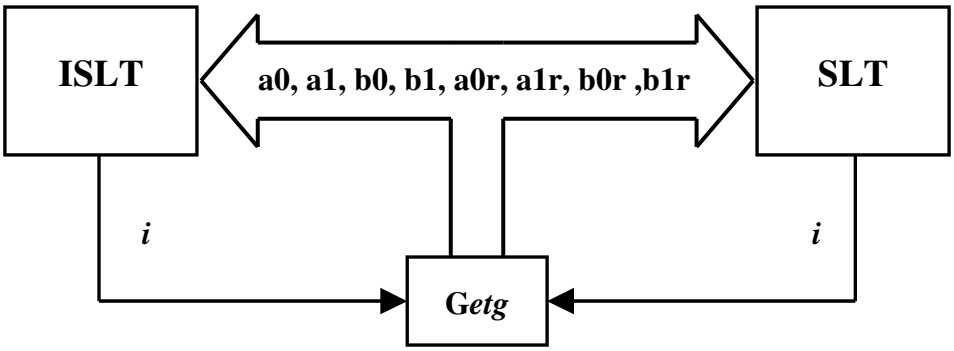

Figure 10: *Getg* function process.

Table 5: Matlab and VHDL codes for ISLT.

x_i	Input	Matlab o/p	VHDL o/p
x_1	0	0.1592	1592
x_2	1	1.0515	1051
x_3	1	-0.3444	-3444
x_4	0	-0.8663	-8663

between Matlab code and VHDL code as illustrated in Table (5). The input vector is {0,1,1,0}, the real values are rounded in VHDL to three digits while in Matlab is rounded to four digits after the decimal point. Notice that, the length of the ISLT input is of power 2. The simulation using ModelSim Altera 6.1g of ***isltsaf*** component is shown in Figure (11).

- **The Receiver Section:**

The same process done in the transmitter section has been done in the receiver section but in reverse order, as shown in Figure (12). The FPGA implementation of the receiver is carried out using three major blocks (entities) namely: ***S2PR1***, ***safrec*** and ***serial _converter***. Figure (13) shows the top-level design file and pins assignment after successful compilation for the receiver.

Pins assignments are made in the same approach of the transmitter. S2 switch push bottom is used as a (***rst)*** signal. The output is displayed using three LEDs from the FPGA. The speed of the design should be checked when it is implemented on Cyclone III device, the timing analysis report, the maximum register clock is 79.03 MHZ, then clk1 = 50 MHz is chosen to be used for the timing simulation.

The ***safrec*** block contains seven sub blocks namely: ***S2PR2***, ***S2PR3 Sltsaf, DZEPD, DePCC, DSM*** and ***DSM2***. The first two blocks belong to the serial to parallel converter. The third and fourth blocks belong to the OFDM demodulator while the last two blocks belong to signal demapping stage.

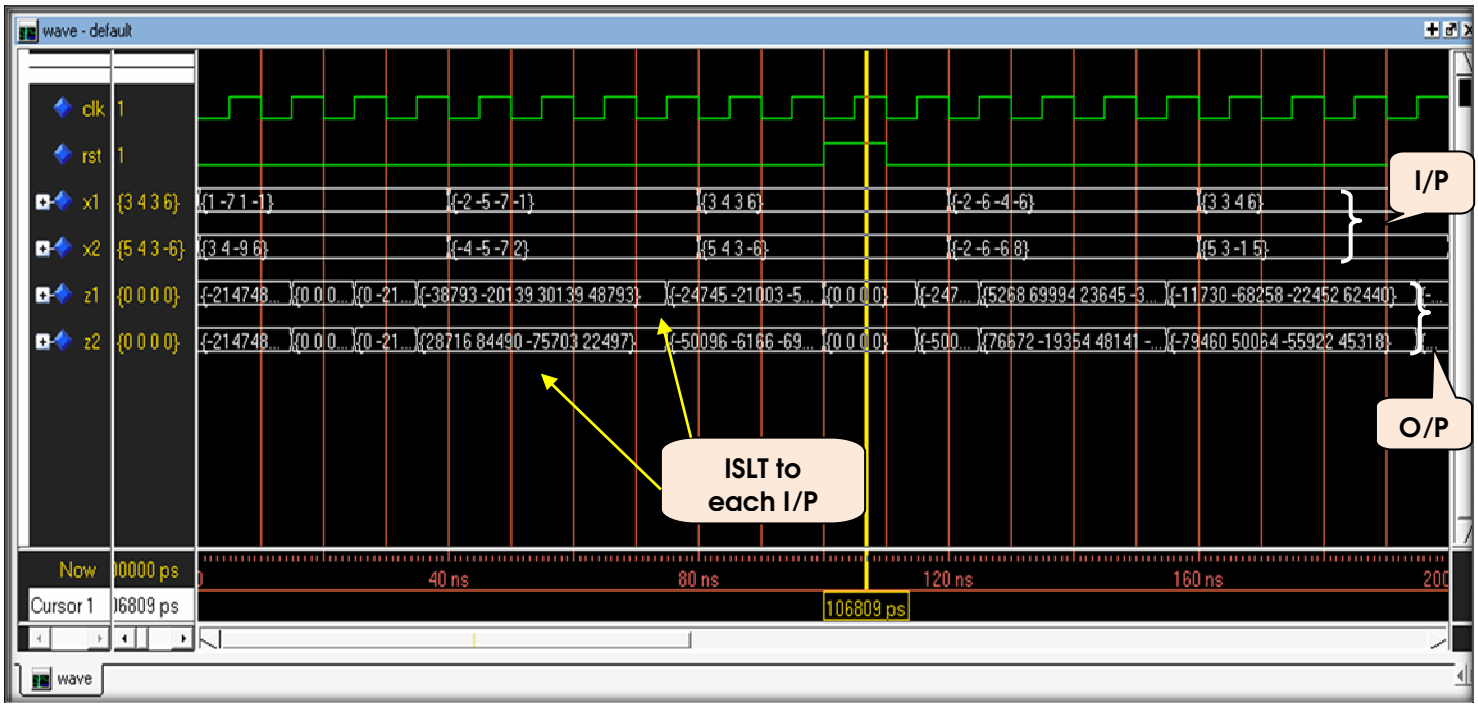

Figure 11: Simulation of ***isltsaf***

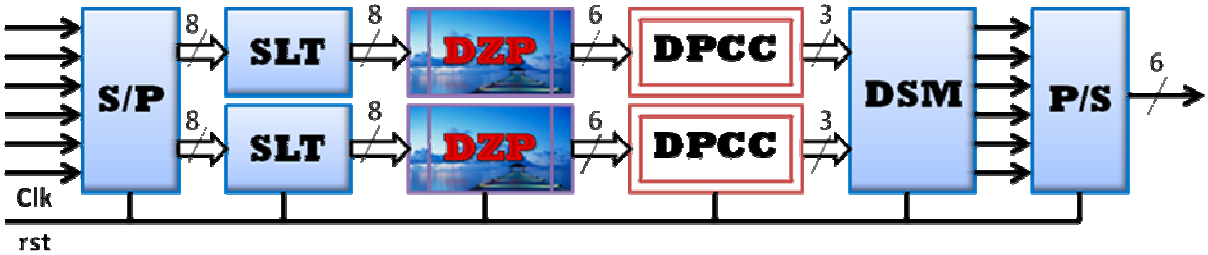

Figure 12: The receiver process.

The first task of the SLT-OFDM demodulator is the SLT (Slantlet transform), where two inputs sequence each of eight integers and the outputs are also of the same length and of integer type. Figure (14) show the schematic diagram of ***Sltsaf*** file and the simulation waveforms for *one* input vector. The next task has been done in ***DZEPD*** which removes the zero elements, as an example the input is of length 4, while the outputs are of length 2 elements for each sequence.

- **Simulation Results of the Receiver Section:**

Figure (15) illustrates the simulation waveforms of ***DZEPD*** using ModelSim Altera 6.1g. The output of the ***DePCC*** is half the input size. The simulation waveforms are illustrated in Figure (16). ***DSM*** and ***DSM2*** provide a specific outputs depending on whether both real or imaginary inputs are positive or negative, this done using ***DSM***, and then convert each symbol to binary in parallel form.

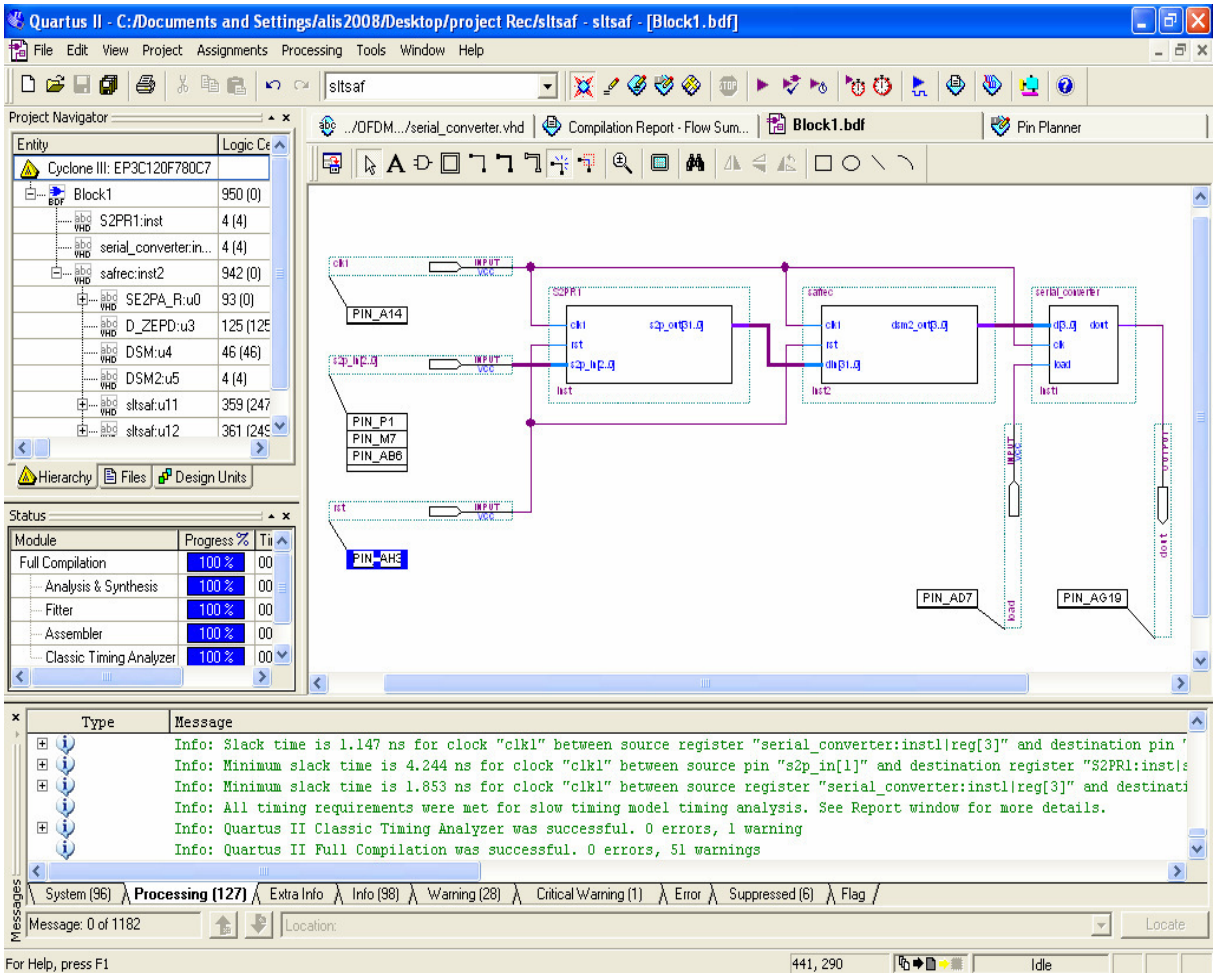

Figure 13: The receiver top-level design

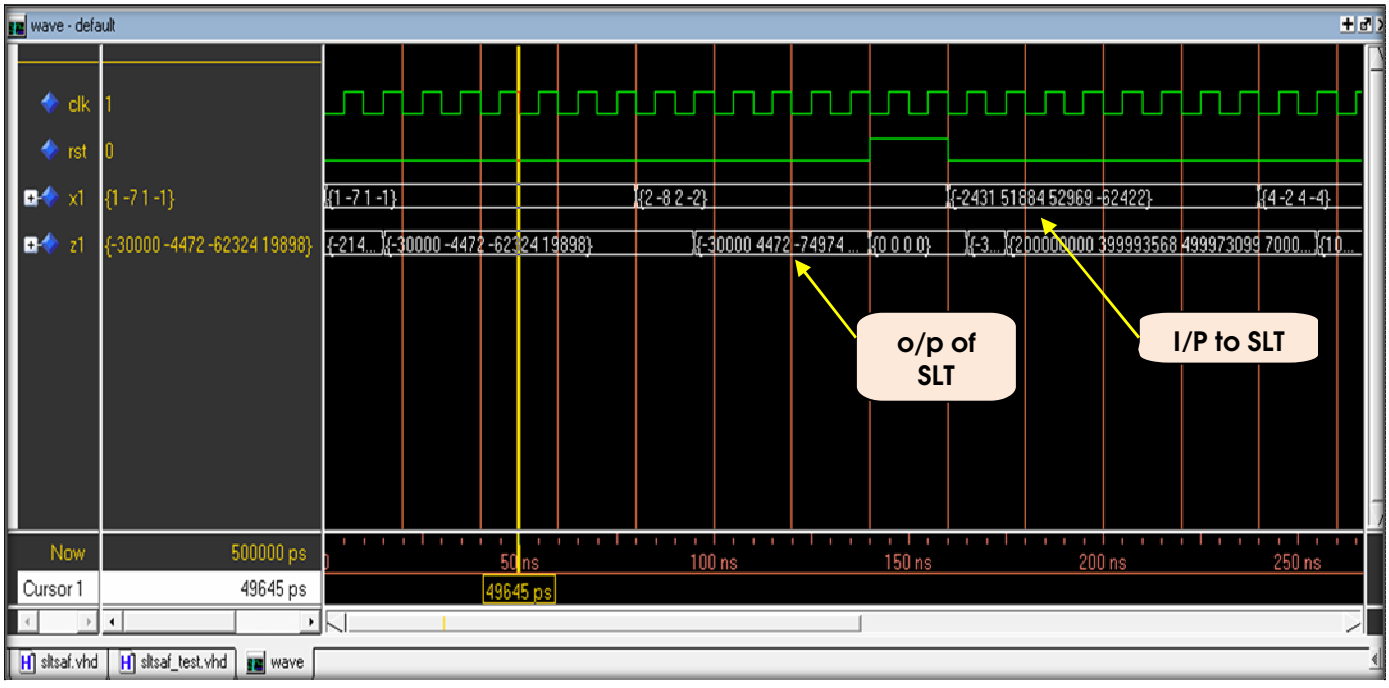

Figure 14: The simulation waveforms of ***Sltsaf***

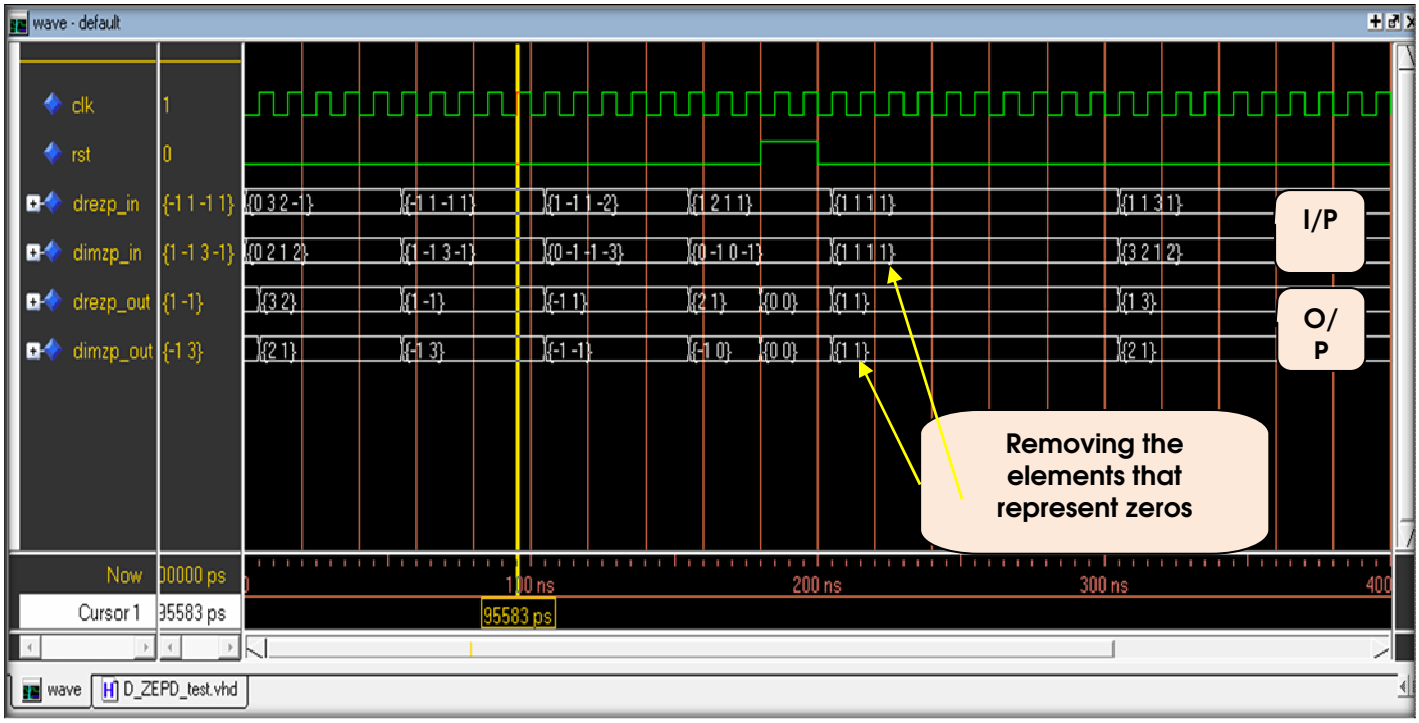

Figure 15: The simulation waveforms of ***Dzremoving***.

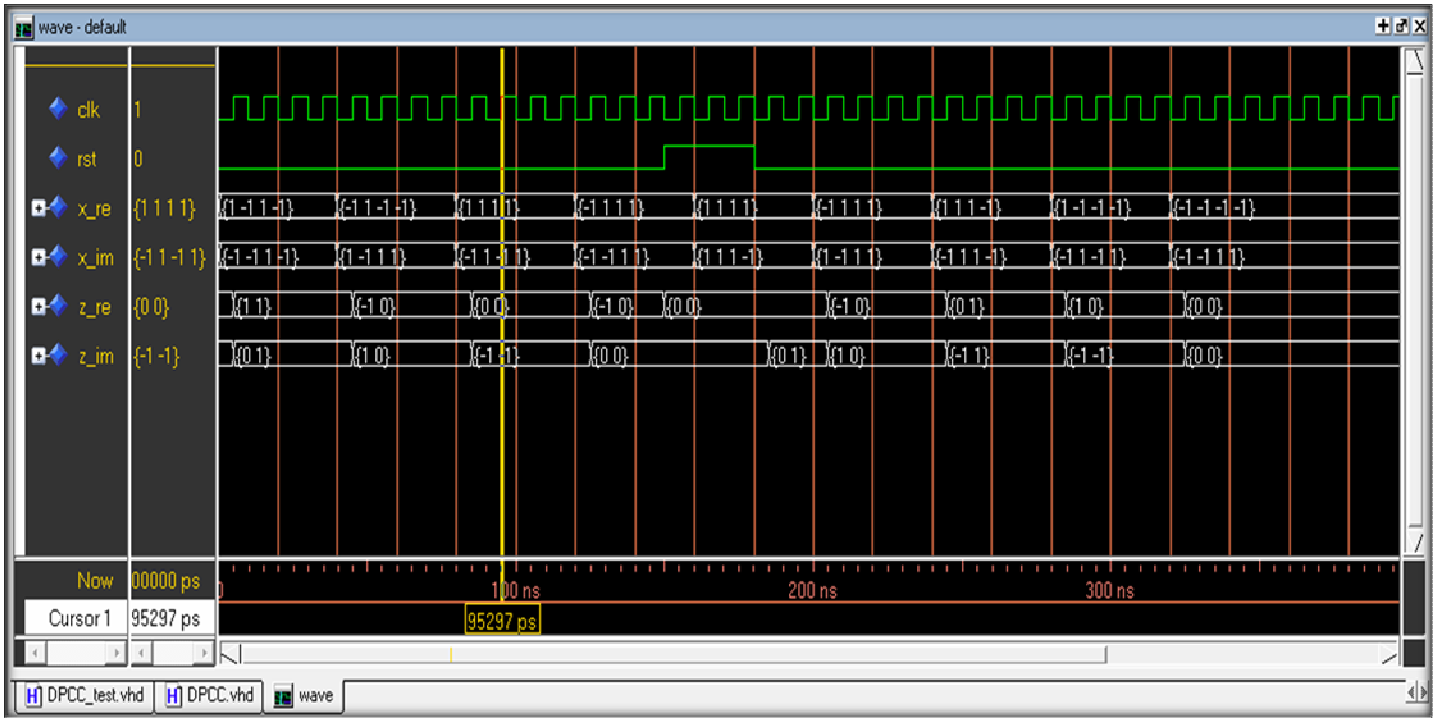

Figure 16: The simulation waveforms of ***DePCC***.

Figures (17) shows the simulation waveforms of ***DSM*** and ***DSM2*** blocks. Decimal values are converted to binary form to obtain the desired received information in ***DSM2***. Finally, ***serial_converter*** is applied to convert the parallel data obtained from ***DSM2*** to serial form which represents the transmitted data. Figure (18) shows the simulation waveforms of ***serial_converter***.

Finally, it is worth noted from synthesis process to the design system that the operating frequency, when it is implemented on Cyclon III device was 71.96 MHz, using input clock of 50 MHz for the timing simulation. The total logic elements (LEs) used were 772, the total registers were 485, while the total pins were 25.

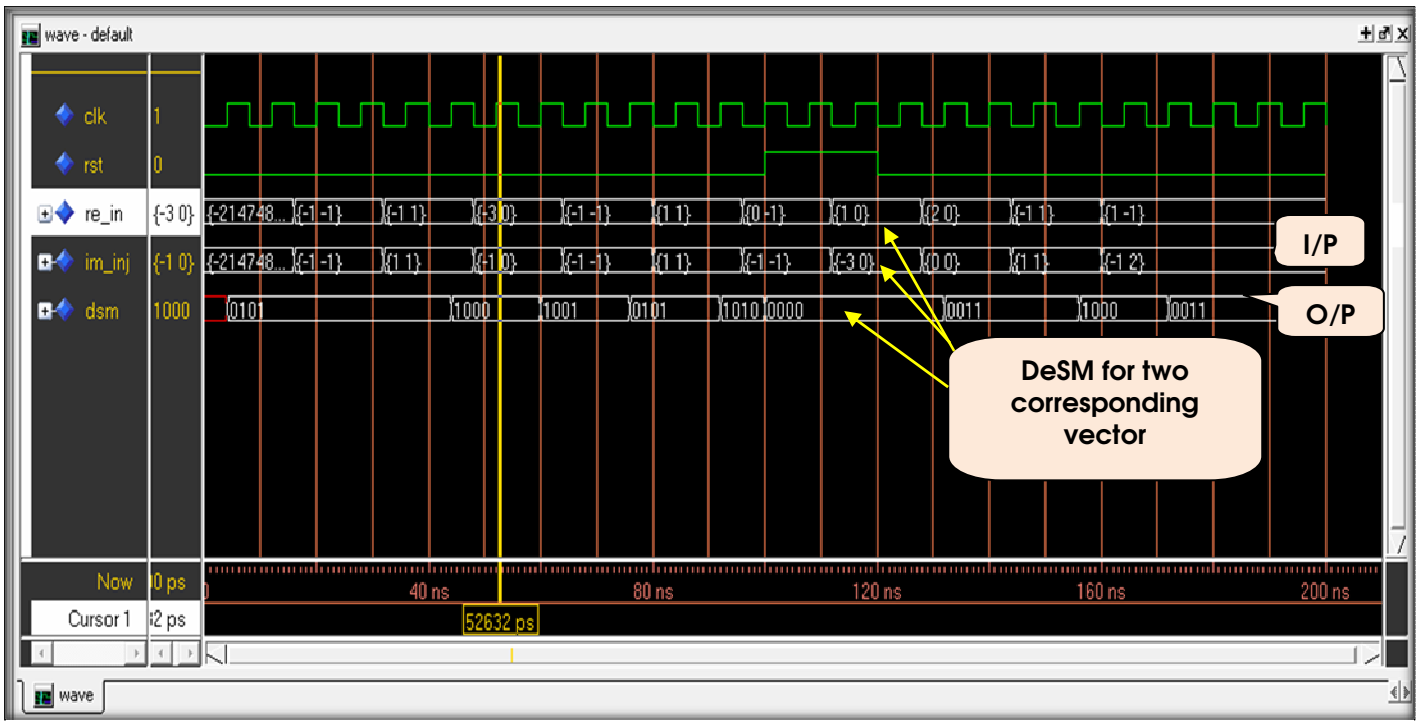

Figure 17: The simulation waveforms of ***DSM*** and ***DSM2***.

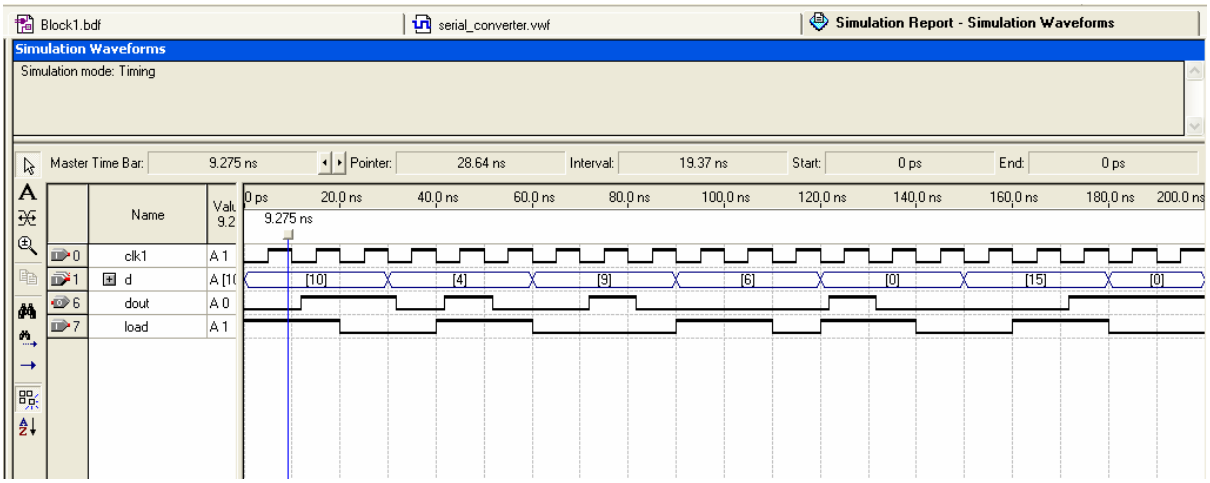

Figure 18: The simulation waveforms of ***serial_converter***.

CONCLUSIONS

A baseband OFDM was successfully developed using Altera Cyclone III EP3C120F780C7 FPGA development board. During the implementation stage, the operation of ISLT was tested using Matlab package. The hardware simulation results show that ISLT/SLT module is working correctly as obtained using Matlab simulations give slight difference from Matlab computation. The different was only that the result of the ISLT/SLT computation was in decimal notation while Matlab provided them in floating point notation. Matlab results were multiply by 10^4 such that it can be equally compared with the ISLT/SLT computations using VHDL. Synthesis results show that the implemented system could support the real time operation of OFDM system with on-chip basis.

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