Process Technology
for
High Speed InP Based Heterojunction Bipolar Transistors

Der Fakultät für Ingenieurwissenschaften der
Universität Duisburg-Essen
zur Erlangung des akademischen Grades eines

Doktor(s) Ingenieurs

genehmigte Dissertation

von

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Tag der Mündlichen Prüfung: 09.08.06

List of Symbols

A	degree of isotropy
A_C	collector area
A_E	emitter area
B	dc Current gain
B_{max}	maximum dc Current gain
BV_{CEo}	open-base Breakdown Voltage
C_{bc}	base-collector capacitance
C_{dep}	base-collector depletion capacitance per unit area
C_{fb}	feedback capacitance
C_{jc}	base-collector junction capacitance
C_{je}	base-emitter junction capacitance
χ_s	electron affinity of the semiconductor
D	high field diffusion constant
ΔE_C	conduction band discontinuity
ΔE_v	valence band discontinuity
D_{nB}	minority electron diffusion coefficient (in base)
D_{pE}	minority hole diffusion coefficient (in emitter)
ε	dielectric constant
e^*	highly energetic electrons
E_F	fermi energy (thermal equilibrium)
$E_{g,base}$	energy bandgap of base
$E_{g,emitter}$	energy bandgap of emitter
ϕ_B	energy barrier height
ϕ_{CB}	base-collector junction potential
ϕ_{Cl2}	$Cl_{2\ flow}$
ϕ_{Cl2+N2}	total gas flow
ϕ_M	work function of the metal
ϕ_M	work function of metal
f_{max}	maximum oscillation frequency

ϕ_{N2}	$N_{2\ flow}$
ϕ_S	work function of semiconductor
f_T	cut-off frequency
I_B	base current
I_B^*	back injection current
$I_{B,bulk}$	bulk recombination current
$I_{B,cont}$	interface recombination current
$I_{B,scr}$	space-charge recombination current
$I_{B,surf}$	surface recombination current
I_C	collector current
I_{SC}	collector saturation current
I_{SE}	emitter saturation current
J_B^*	back injection current density
$J_{B,bulk}$	bulk recombination current density
$J_{B,surf}$	surface recombination current density
$J_{C,max}$	maximum collector current density
J_{Kirk}	Kirk current density
k	Boltzmann's constant
$K_{B,surf}$	surface recombination current divided by perimeter
L_B	base length
L_D	amount of spreading
L_E	emitter length
L_{pad}	length of the TLM pad
L_T	transfer length
μ_n	electron mobility
μ_p	hole mobility
n_0	electron density in thermal equilibrium
N_B	base doping density
n_B	base ideality factor
n_C	collector ideality factor
N_c	effective density of states in the conduction band
N_C	collector doping density
N_E	emitter doping density
n_i	intrinsic carrier density
N_v	effective density of states in the valence band

p	pressure
p_0	hole density in thermal equilibrium
P_E	emitter Perimeter
P_{ICP}	ICP power
ρ	net charge density
$R_{b,cont}$	base contact resistance
$R_{b,spread}$	spreading resistance
R_{bb}	base resistance
$R_{bb}xC_{bc}$	general time constant
R_{cont}	contact resistance
R_E	emitter resistance
R_{gap}	base-emitter gap resistance
R_{jc}	collector junction resistance
R_{je}	emitter junction resistance
R_L	lateral etch rate
$R_{sh,base}$	base sheet resistance
R_{TOT}	Total resistance
R_v	vertical etch rate
S	selectivity
S_c	specific contact resistance
T	temperature in Kelvin
T_B	base thickness
τ_b	base transit time
T_C	collector thickness
T_{dep}	base-collector depletion region thickness
T_E	emitter thickness
τ_e	emitter charging time
τ_{sc}	space-charge transit time
V_2	base-collector bias depleting the collector layer
V_{BC}	base collector voltage
V_{BE}	base emitter voltage
V_{bi}	built-in potential
V_{CE}	collector emitter voltage
$V_{CE,offset}$	offset Voltage
v_{sat}	saturation velocity

$V_{trun\text{-}on}$	turn-on Voltage
W_B	base width
W_{dep}	depletion region width
W_E	emitter width
W_{EB}	base-emitter spacing
W_{pad}	width of the TLM pad

1 Introduction

In1904, Fleming invented vacuum tube diodes and this was the starting point of Electronics Engineering. By the beginning of 1907s, De Forest introduced a third electrode into the vacuum tube diode, and created a device called vacuum tube triode, which could generate oscillations and amplify radio signals. With this invention, live radio broadcasting became possible and radio industry was founded. Thus, Lee De Forest is known as the father of radio [1].

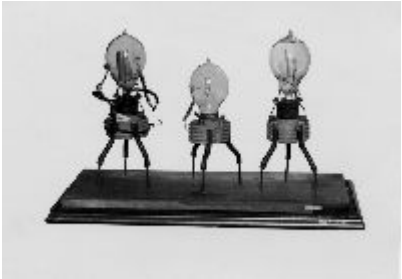


Figure 1.1 Fleming's first vacuum tube diodes [2]

Until 1950s, vacuum tube devices were used in electronic systems. In 1947, William Shockley, John Bardeen and Walter Brattain have invented the first solid-state transistor [3]. This invention was one of the most important milestones in electronics engineering [4].

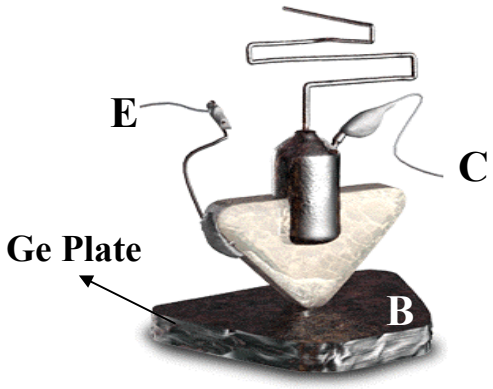


Figure 1.2 First Transistor invented at Bell Labs in 1947 [5]

Up to now, a rapid progress and lots of improvements have been done. The first transistor was realised on a germanium (Ge) plate. In comparison to the vacuum tube triodes, solid-state transistors were offering reliability, a longer lifetime, less power consumption and smaller device dimension, which was an important aspect for integrated circuits. Jack Kilby has used this integration aspect and has invented the first integrated circuit [6]. At the same time, by the beginning of 1950s, Shockley and Kroemer have introduced a concept, which was named as heterojunction concept, overcoming the constrains of homojunction transistors [7, 8, 9]. But it has taken nearly 20 years to realise these junctions. By the introduction of modern epitaxial crystal growth techniques, it became possible to produce high quality junctions produced with different materials [10].

These series of inventions have resulted in a rapid improvement of electronic circuits and systems.

By the advances in high frequency communication systems, and particularly Internet, wide bandwidth and high-speed transistors became key devices for the circuits. Especially, optical fibres can transport data at high rates. Therefore, high-speed electronics is necessary for all kind of data processing. One limitation is the ultra high frequency modulation of the light for data transport. This requires high frequency and high voltage of operation. Second, high linearity of amplification is necessary for analog-to-digital conversion (ADCs). A technology roadmap is shown in table 1.1 to present the high data rate potential of optoelectronic communication systems.

Table 1.1. Optoelectronic Communication Technology Roadmap [11]

Year	**1998**	**2000**	**2003**	**2005**	**2011**
Long Haul Bitrate (TDM)	10 Gbit/s	40 Gbit/s	80/ 160 Gbit/s		400 Gbit/s (?)

Indium Phosphide based Heterojunction Bipolar Transistors (InP HBTs) have the potential to provide high speed and high voltage for optoelectronic communication ICs. Moreover, since their energy band gap corresponds to the 1.3 and 1.55 μm wavelength, which are the wavelengths providing minimum optical loss in fibres, InP HBTs are the best choices for optical communication circuits [12].

The objective of this work is to demonstrate HBT to be used for "InP Electronics for +80 Gbit/s (InP-Elektronik für +80 Gbit/s)" project. This project is funded by German Federal Ministry of Education and Research (BMBF). Here, high speed, reproducible, reliable and high yield HBTs are required. Techniques have been investigated to decrease the parasitic capacitances and resistances leading to high speed HBTs. Wet chemical and dry etching methods have been optimised and compared to show that etching has an important influence on reproducibility and uniformity. An ICP-RIE (Inductively Coupled Plasma – Reactive Ion Etching) process with Cl_2/N_2 chemistry has been developed for the processing of submicron emitters and smaller device dimensions in a reliable way.

The present thesis is structured as follows:

Chapter 2 - Theory

The details about the basic device operation are given. The physical background and equations governing HBT operation are explained. The structure of a conventional InP HBT is given. The dc (direct current) and RF (radio frequency) properties of HBTs are discussed and equations are given to calculate the performance of HBTs. Simulations are performed for different material systems to show pros and cons, while discussing the possible "bandgap engineering". Details are given about the epitaxial growth and about the lateral design of HBTs. Different approaches are discussed to reduce the parasitic capacitances.

Chapter 3 - Fabrication of HBTs

Main steps and the evolution of the optimised HBT fabrication process are presented. The experiments and research, which have been performed to improve the performance and reliability, are presented.

Chapter 4 – HBT with the Optimised Layout and Processing

In this chapter, HBTs processed with the optimised processing procedure and the new designs are presented. GaAsSb DHBT measurement results are used for the comparison of the previous design and processing with the optimised ones. The Kirk effect is investigated experimentally. The influences of the emitter width and length on HBTs performance are elaborated.

Chapter 5 – Inductively Coupled Plasma- Reactive Ion Etching for HBT Applications

In this chapter, basics about the plasma processing are given. A hybrid etching process has been developed to be used for HBT applications. SHBTs processed with the optimised hybrid etching process have been investigated. The influence of emitter etching on HBT's uniformity is presented. The first results for submicron HBTs processed with ICP-RIE with Cl_2/N_2 chemistry are presented.

Chapter 6 – Conclusion and Outlook

This chapter summarises the improvements in processing and the results of the complete thesis. With the outlook, potentials for future applications are pointed out to guide for the upcoming work.

2 Theory

2.1 Heterojunction Bipolar Transistors

Especially, in the last two decades, by the advances in epitaxial growth techniques, heterojunction bipolar transistors (HBTs) became key devices for optoelectronics circuits. In comparison to their homojunction counter parts, the use of wide band gap heterojunction emitters allows the design of HBTs with very high base doping [13]. This provides a lower base resistance and base collector capacitance, and enables a better RF performance. In the following chapter, the structure of an InP-HBT and the details about device operation will be given.

2.1.1 Structure of an HBT

In comparison to the Bipolar Junction Transistors (BJTs), the HBTs contain a heterojunction, where two different materials with different band gaps are used. In figure 2.1, the conventional layer structure for a single heterojunction InP bipolar transistor (InP-SHBT) is shown.

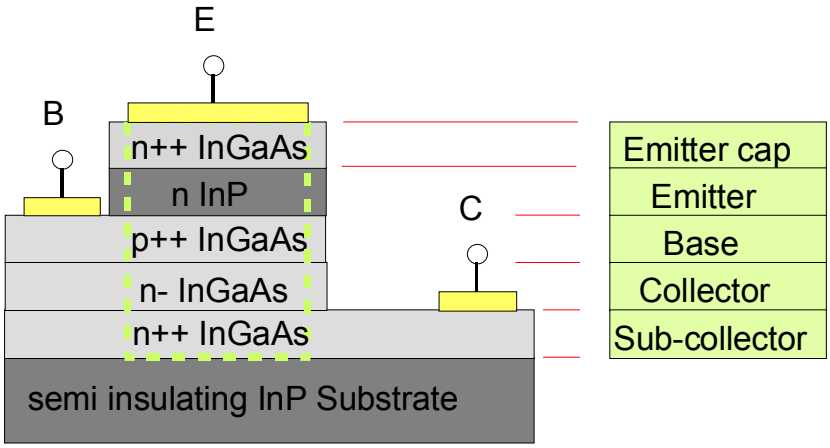


Figure 2.1 Layer structure of a conventional InP/InGaAs SHBT.

As depicted in figure 2.1, an HBT consists of three main layers, which are emitter, base and collector like in BJTs. These three layers form two pn junctions connected in a back-to-back configuration. In this example, the HBT is npn type, where emitter and collector are doped n-type, in contrary the base is placed between them,

with p type doping. There are also pnp transistors. As the electron mobility is higher than the hole mobility for all semiconductor materials, a given npn transistor tends to be faster than an equivalent pnp type. Therefore, npn transistors are preferred for circuit applications and will be considered here.

2.1.2 dc properties of HBTs

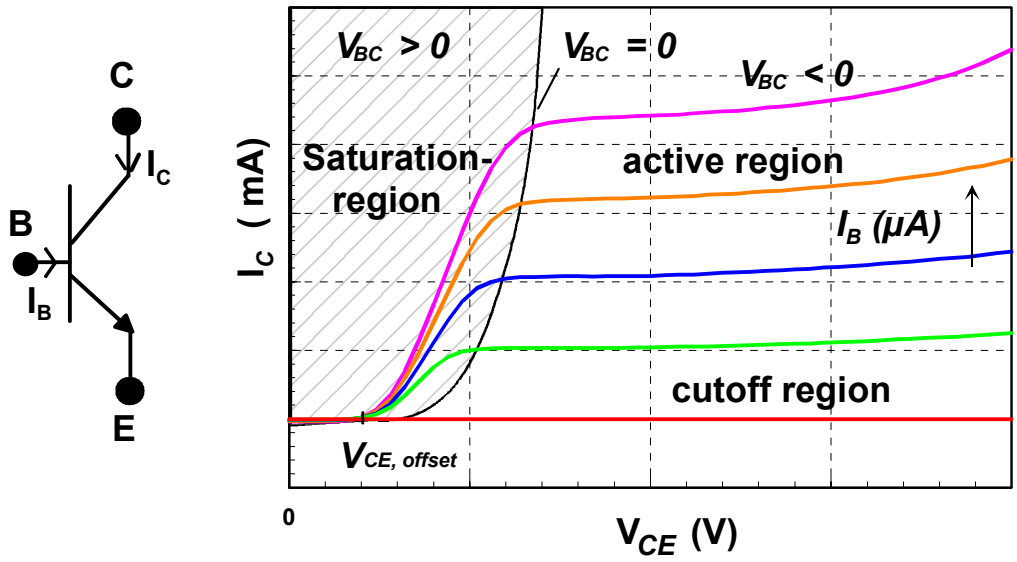


Figure 2.2 The common emitter output characteristic of a typical npn InP-HBT.

Under the normal operating conditions (active region), the base-emitter diode is forward biased, V_{BE}> 0 V, and the base-collector diode is reverse biased, V_{BC}< 0 V. In the saturation region both diodes are forward biased, V_{BC}, V_{BE}> 0 V. In the cut-off region, both diodes are reverse biased, V_{BC}, V_{BE}< 0 V. The base-emitter diode is reverse biased, V_{BE}< 0 V and the base-collector diode is forward biased, V_{BC}> 0 V, in the reverse region.

In the common emitter output characteristics shown in Figure 2.2, the output current I_C, is plotted as a function of V_{CE} for different input currents I_B. By dividing the output current I_C into the input current I_B at a certain bias point, dc current gain, B, can be identified. Here, one can also extract the offset voltage ($V_{CE,offset}$), the turn-on voltage ($V_{turn-on}$) and the breakdown voltage, BV_{CEo}.

The dc current gain of an HBT is given in equation 2.1 [14].

$$\frac{I_C}{I_B^*} = \frac{N_E T_E D_{nB}}{N_B T_B D_{pE}} \cdot \exp(\frac{\Delta E_v}{kT}) \qquad \text{equation 2.1}$$

Here, N_E and N_B are the emitter and base doping levels; T_E and T_B are the emitter and base thickness; D_{pE} and D_{nB} are the minority hole diffusion coefficient in the emitter and the minority electron diffusion coefficient in the base, respectively. ΔE_v is valence band discontinuity at base and emitter heterointerfaces [14]. The base current is denoted as I_B^* referring to the back-injection current. By the help of this valence band discontinuity, the diffusion of the holes from the base to emitter is reduced. This will keep the base current lower leading to higher dc current gain. In addition to the back-injection current, the base current is composed of 4 main components. These are: the surface recombination current $I_{B,surf}$, the interface recombination current $I_{B,cont}$, the bulk recombination current in the base region $I_{B,bulk}$, the space-charge recombination current in the base-emitter depletion region $I_{B,scr}$. $I_{B,surf}$ is defined as the recombination of the minority carriers injected from emitter with the base majority carriers at the surfaces. This is proportional to the emitter periphery. This component is much more important for GaAs surfaces where the surface recombination velocity is rather high. Especially for small devices having large perimeter area ratio, this component becomes dominant. This effect is also named as "emitter size effect". The dc current gain decreases with the decreasing emitter area. $I_{B,cont}$ becomes important when the base-emitter contact spacing is low. In this case, the minority carriers flow also laterally to the base contact and recombine with the majority carriers and increase the $I_{B,cont}$. If the base-emitter contact spacing is large, the minority carrier concentration reaching the base contact is nearly zero. The recombination of the carriers in the depletion region results in increase of $I_{B,scr}$ [14].

The offset voltage is caused by the different values for the turn-on voltages of base-emitter and base-collector diodes. The value of the offset voltage is determined by the ratio of base-emitter and base-collector junction areas, high-level injection effects and series resistances [15]. The offset voltage can be expressed as:

$$V_{CE,offset} = R_E I_B + \frac{nkT}{q}\ln(\frac{A_C}{A_E}) + \frac{nkT}{q}\ln(\frac{I_{SC}}{I_{SE}}) \qquad \text{equation 2.2}$$

Here, R_E is the emitter resistance, T is the temperature, n is ideality factor, A_C and A_E are the collector and emitter areas, respectively. I_{SC} and I_{SE} are collector and emitter saturation currents, respectively.

The turn-on voltage is defined as the base-emitter voltage required to achieve a certain collector current [16]. It is given as:

$$V_{BE,turn-on} = -\frac{kT}{q}\ln(R_{sh,base}) + \frac{E_{g,base}}{q} - \frac{kT}{q}\ln(q^2 \mu N_c N_v D_n / J_C) \qquad \text{equation 2.3}$$

The open base breakdown voltage, BV_{Ceo}, defines the maximum allowed collector-emitter voltage. When the collector-emitter voltage is higher than BV_{Ceo}, even though no current is applied to the input, there will be current flowing at the output. This breakdown effect is caused by the impact ionisation in the base-collector diode and the punch through effect [17].

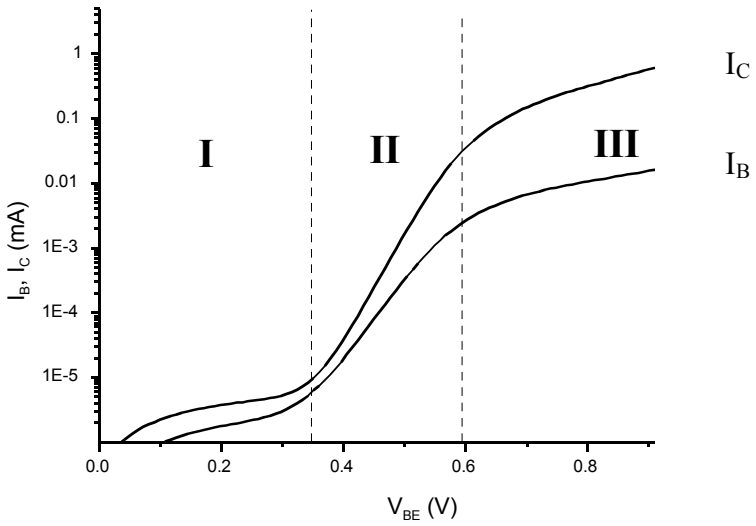


Figure 2.3 The typical Gummel Plot for an HBT (V_{CB}= 0V)

The Gummel Plot is the simultaneous plot of I_C and I_B as a function of V_{BE} when V_{CB}= 0 V as shown in Figure 2.3. The base and collector ideality factors (n_B and n_C) and leakage currents for both diodes can be extracted from this plot. Region I is the non-linear region, where leakage currents and low voltage effects dominate. Exponential behaviour can be observed in region II. In the ideal case, the dc current gain is constant

and ideality factors can be extracted in this region. High-current and series-resistance effects are dominant in region III.

For these measurements, the dc measurement set-up shown in figure 2.4 is used. The sample is placed on the Karl Süss PA 150 Prober. By the help of the controller, sample is aligned to contact the measurement needles. Via cables, measurement needles are connected to the semiconductor parameter analyser. Semiconductor parameter analyser is a stand-alone instrument capable of complete dc characterisation of semiconductor devices. It stimulates voltage and current sensitive devices, measures the resulting current and voltage response, and displays the results in a user selectable format on CRT display [18]. Here, the measurement PC collects the data from the analyser and saves them.

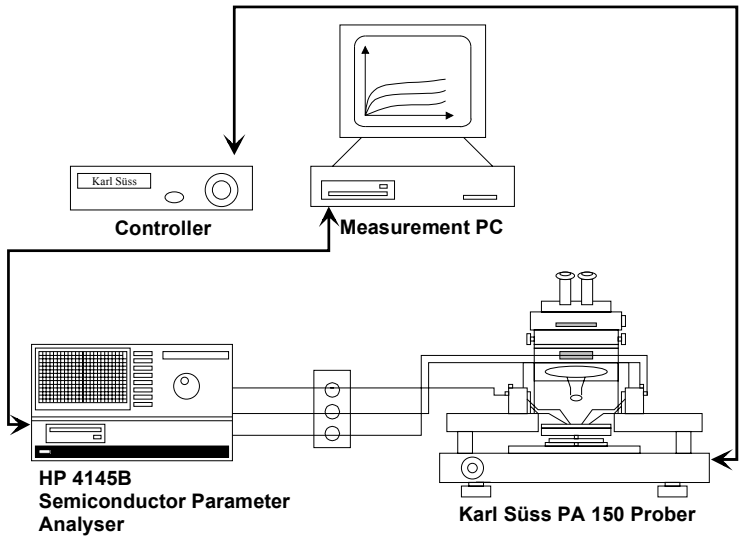


Figure 2.4 The dc measurement set-up used in this work

For the operation of an HBT, a key parameter is the thickness of the base. Here, one should consider two cases. Case 1, when the base thickness is relatively thick. Case 2, when the base thickness is less than the diffusion length (L_n).

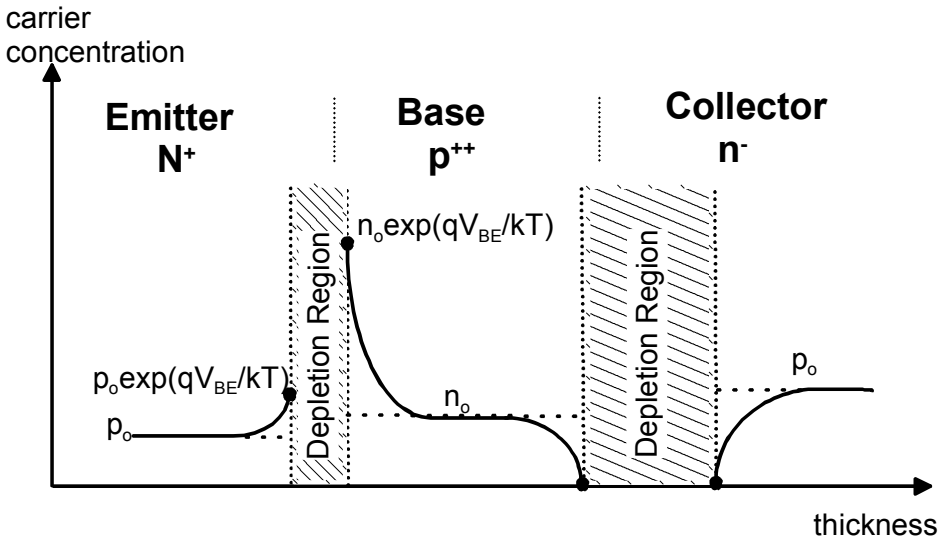


Figure 2.5 The minority carrier concentration for an npn transistor with relatively thick base layer

In case 1, since all the electrons emitted by emitter recombine with the holes in the base, there are no electrons reaching to the base-collector junction. As a result, the collector current is limited to the saturation current (I_{SC}). In figure 2.5, the distribution of the carrier concentration belonging to case 1 is shown. p_o and n_o are representing the equilibrium hole and electron concentration in emitter and in base, respectively. The first has small value equal n_i^2/N_B and the latter is n_i^2/N_E, where n_i is the intrinsic carrier concentration.

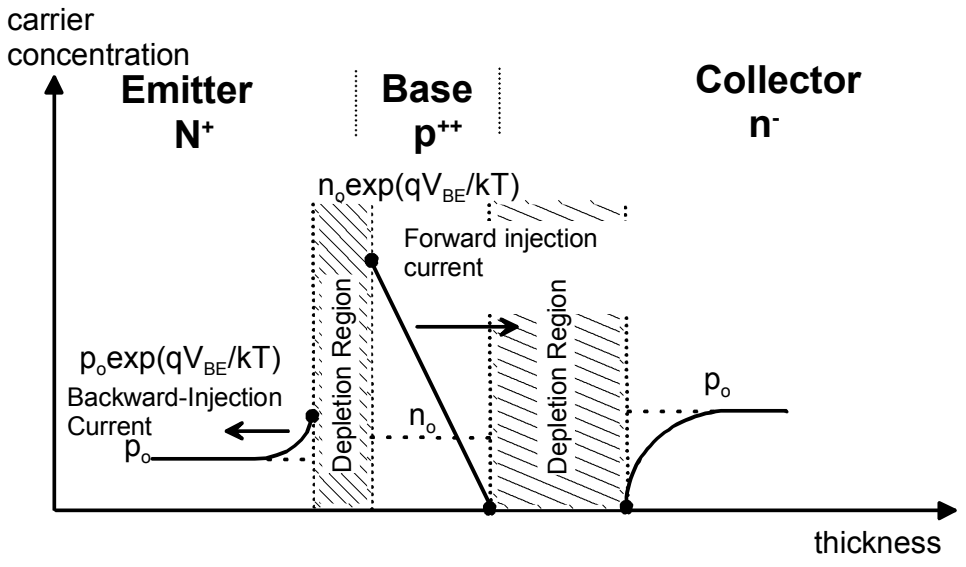


Figure 2.6 The minority carrier concentration for an npn transistor with proper base layer

In case 2, the thickness of the base is less than the diffusion length of the minority carriers, here electrons. The electrons emitted by the emitter, can reach the collector before they recombine with the holes in the base, because of the thinner base. Even though, the base-collector voltage is set to zero (V_{CB}= 0 V), by the help of the electric field in the base-collector depletion region these electrons can be swept into the collector. This leads to current flow in the collector. Here, the number of electrons is not the same as the number of electrons entering the base. This degradation occurs because of the unavoidable recombination in the base. In figure 2.6, the distribution of the carrier concentration belonging to case 2, is shown.

2.1.3 RF Properties of HBTs

There are two important figures of merit for the high frequency characterization of HBTs. These are the cut off frequency f_T, and the maximum oscillation frequency f_{max}.

The current gain cut off frequency is determined by the transit time of the electrons emitted by emitter. The current gain cut-off frequency is given as:

$$\frac{1}{2\pi f_T} = \tau_e + \tau_b + \tau_{sc} + \tau_c \qquad \text{equation 2.4}$$

Here, τ_e is defined as the emitter charging time.

$$\tau_e = \frac{kT}{qI_c}(C_{je} + C_{jc}) \qquad \text{equation 2.5}$$

C_{je} is defined as the base-emitter junction capacitance and C_{jc} is defined as the base-collector junction capacitance.

τ_b is the base transit time.

$$\tau_b = \frac{T_B^2}{2D_{nB}} \qquad \text{equation 2.6}$$

τ_{sc} stands for space-charge transit time and defined as the time for the carriers to drift through the depletion region of the base-collector junction.

$$\tau_{sc} = \frac{T_{dep}}{2v_{sat}} \qquad \text{equation 2.7}$$

T_{dep} is the base-collector depletion region thickness and v_{sat} is the saturation velocity. τ_c is the collector charging time given as:

$$\tau_c = (R_E + R_C) \cdot C_{jc} \qquad \text{equation 2.8}$$

This term is greatly influenced by the parasitic emitter resistance, R_E.

With the equations 2.5 – 2.8, the f_T can be written as:

$$\frac{1}{2\pi f_T} = \frac{kT}{qI_c}(C_{je} + C_{jc}) + \frac{T_B^2}{2D_{nB}} + \frac{T_{dep}}{2v_{sat}} + (R_E + R_C) \cdot C_{jc} \qquad \text{equation 2.9}$$

The equation 2.9 can be interpreted that the cut off frequency can be influenced mainly by the vertical design of HBTs, or in other words mostly with epitaxy.

Another important figure of merit for high frequency performance is the maximum oscillation frequency f_{max}. It is related with the charging and discharging time of the capacitances. It is defined as the frequency where the power gain drops to unity [19].

$$f_{\max} \approx \sqrt{\frac{f_T}{8\pi R_{bb} C_{bc}}} \qquad \text{equation 2.10}$$

The parameters are depicted in Figure 2.7 using the triple mesa design of a HBT.

The base resistance R_{bb}, consists of contact resistance $R_{b,cont}$, base-emitter gap resistance R_{gap} and spreading resistance underneath the emitter $R_{b,spread}$. The equation

2.11 depicts the components of base resistance R_{bb}. R_{sh} and S_C represents the specific sheet and contact resistances, respectively.

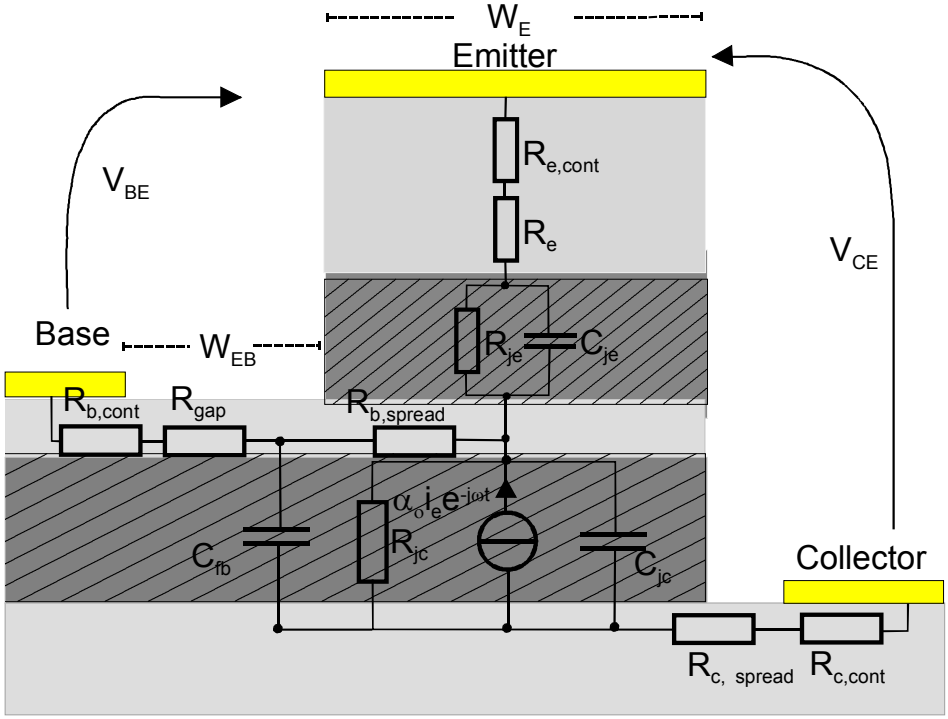


Figure 2.7. The triple mesa design HBT layout showing the small signal parameters and dimensions used in the equations. The shaded regions depict the space charge regions.

$$
\begin{aligned}
R_{bb} &= R_{b,cont} + R_{gap} + R_{b,spread} \\
R_{b,cont} &= \sqrt{R_{sh} S_C} / 2L_E \\
R_{gap} &= \rho_S W_{EB} / 2L_E \\
R_{b,spread} &= \rho_S W_E / 12L_E
\end{aligned}
\qquad \text{equation 2.11}
$$

C_{fb}, C_{jc} and C_{je} are the feedback, the intrinsic base-collector and the intrinsic base-emitter capacitances, respectively. C_{bc} is the total base-collector capacitance, and it is proportional to the base-collector junction area. The components of the base-collector capacitance can be represented as:

$$
\begin{aligned}
C_{jc} &= C_{dep} W_E L_B \\
C_{fb} &= C_{dep} (W_{EB} + W_B) L_B
\end{aligned}
\qquad \text{equation 2.12}
$$

Here, C_{dep} is the base-collector junction depletion capacitance per unit area and L_B is the length of the base contact.

There are several methods in the literature to improve the f_{max}, which are mostly related with technology and layout. The main idea for all of these methods is to find an optimum way to reduce the base-emitter gap and base-collector area. They will lead to a reduced base resistance and a reduced base-collector junction area will offer a lower base-collector capacitance and hence better RF performance [20, 21, 22, 23, 24, 25, 26] For the measurement of f_T and f_{max}, the RF measurement set-up shown in Figure 2.8 is used. This system is capable of performing dc and RF measurements. The sample, DUT (device under test), is placed on wafer prober from Alessi and contacts are realised with Picoprobe microwave needles with 150 μm pitch (GSG: ground signal ground). Before dc measurement, the system must be calibrated in order to eliminate the influence of the cables and measurement needles to the results. For the calibration, a calibration substrate is used. Up to 50 GHz RF measurement is possible with network analyser HP 8510C with serial synthesizer HP 83650. By the help of s-parameter test set HP 8517A, s-parameters are measured in the range of 45 MHz up to 50 GHz. HP 4142B parameter analyser is used to adjust the biasing point. High frequency calibration is performed by the SOLT (short, open, load, through) structures on the calibration substrate.

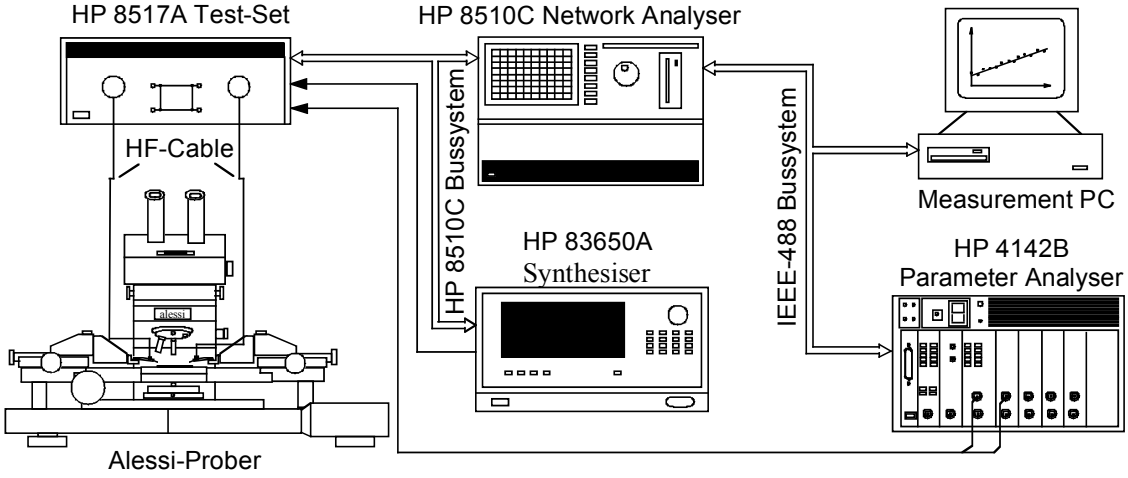


Figure 2.8 The RF Measurement Set-Up used in this work

Since they are easier to measure and work with at high frequencies than other kinds of parameters, scattering parameters are preferable. Scattering parameters are commonly referred to as s-parameters. They are the parameter set defined by travelling waves that

are scattered or reflected when an n-port network is inserted into the transmission line. Unlike other parameters set (like Z, h, y parameters), they are easier to measure, because they do not require successive opened or short circuited input and output of the device. This situation is much more critical for RF frequencies where lead capacitance and inductance make open and/or short circuits difficult to achieve. s-parameters are convertible to all other parameters set as shown in Appendix A [27].

The cut-off frequency is also defined as the frequency, where the current gain drops to unity. In other words, it is given as the frequency, where $|h_{21}|$ drops to unity. The h_{21} of an HBT is given as follows and can be extracted by the measured s-parameters [14]:

$$h_{21} = \left.\frac{i_2}{i_1}\right|_{v_2=0} = \left.\frac{i_c}{i_b}\right|_{v_{ce}=0} = \left|\frac{-2s_{21}}{(1-s_{11})(1+s_{22})+s_{12}s_{21}}\right| \qquad \text{equation 2.13}$$

2.1.4 Parameter extraction for HBTs

In addition to the dc and RF measurements, by using measured s-parameters, the extrinsic and intrinsic parameters of HBTs can be extracted. For this purpose, a T-model small signal equivalent circuit has been used as shown in Figure 2.9. The determinations start with identifying the extrinsic elements using evolutionary optimisation strategies [28, 29]. The optimisation procedure identifies the bias dependence of the extrinsic small-signal equivalent elements. And then, the intrinsic parameters are optimised by keeping the extrinsic parameters constant. All the procedure briefly described above is performed by a software called “evolHBT”, which is developed in the department [29].

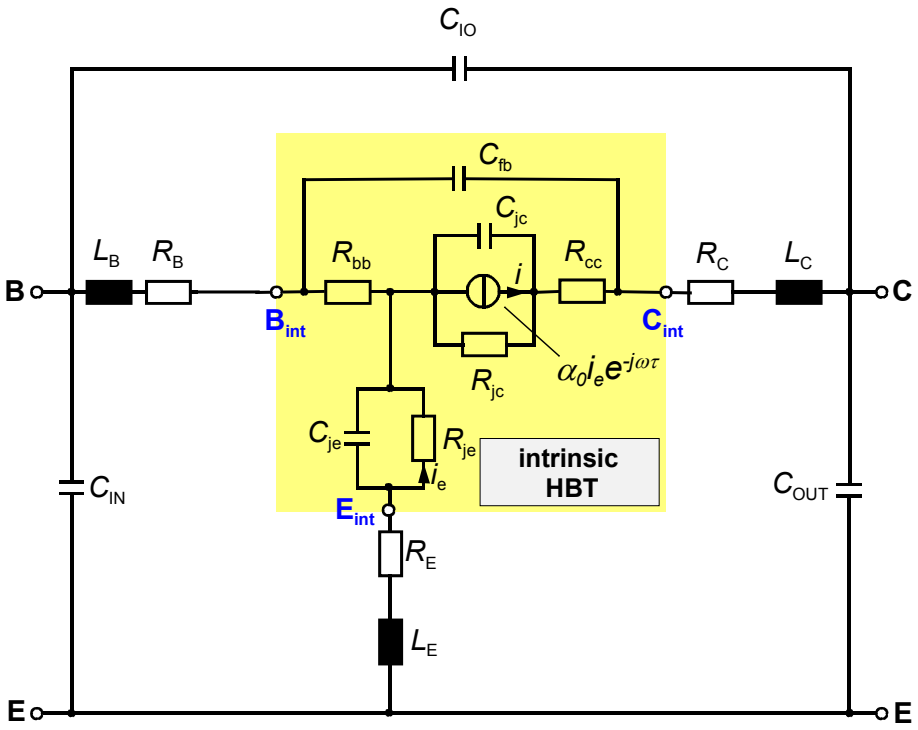


Figure 2.9 T-model small signal equivalent circuit for an HBT used for the parameter extraction

2.2 Different Material Systems used for InP based HBTs

The HBTs can be classified according to the substrate material used. In general, there are 3 main substrate materials used. These are; Gallium Arsenide (GaAs), Silicon (Si) and Indium Phopshide (InP). The most mature one is GaAs. As wide band gap emitter, AlGaAs was grown on GaAs [30, 31]. Later on, since it offers easier processing, indium gallium phosphide (InGaP) was used as emitter material [32]. In Table 2.1, possible material systems used for III-V HBTs are shown [33]. As depicted in table 2.1, if one of the junctions is a heterojunction, then it is named as Single Heterojunction Bipolar Transistor (SHBT). If both junctions are heterojunction, then it is called Double Heterojunction Bipolar Transistor (DHBT).

Table 2.1 HBT types with different material systems

Substrate	Emitter	Base	Collector	Type
GaAs	AlGaAs	GaAs	GaAs	SHBT
			AlGaAs	DHBT
	InGaP	GaAs	GaAs	SHBT
			InGaP	DHBT
InP	InP	InGaAs	InGaAs	SHBT
			InP	DHBT
	InAlAs	InGaAs	InGaAs	SHBT
			InP	DHBT
	InP	GaAsSb	InP	DHBT

InP substrate has several advantages over GaAs. First of all, the specific composition of InGaAs is lattice matched to the InP and InGaAs has about 1.5 times higher electron mobility than GaAs. Moreover, since the Γ-L and Γ-X valley's separations are greater for InP and InGaAs in comparison to GaAs. They offer higher velocity overshoot, which will result in higher electron velocity and higher $f_{T.}$

Table 2.2 Material parameter for different heterojunctions

Heterojunction (Emitter/Base)	$E_{g,emitter}$(eV)	$E_{g,base}$(eV)	ΔE_C(eV)	ΔE_V(eV)
InP/$In_{0.53}Ga_{0.47}As$	1.35	0.76	0.25	0.34
$In_{0.52}Al_{0.48}As$/$In_{0.53}Ga_{0.47}As$	1.48	0.76	0.48	0.24
$Al_{0.30}Ga_{0.70}As$/GaAs	1.86	1.42	0.28	0.15
$In_{0.49}Ga_{0.51}P$/GaAs	1.92	1.42	0.12	0.38

Smaller band gap InGaAs results in lower base–emitter turn-on voltage, which is an important aspect for low power applications. InGaAs has much lower surface recombination velocity (~1000 times lower) than GaAs. This leads to the lower base current due to the less recombination and therefore higher current gain. Especially for high power and high current applications, thermal conductivity should be considered. InP has thermal conductivity of 0.68 W/cm, where GaAs has 0.45 W/cm [14]. The most

important properties of InP substrate, which makes it attractive for optical communication circuits, is the compatibility with lasers working at 1.3 and 1.55 μm wavelength, where the fibre optic losses are minimum. On the other hand, InGaAs has lower mobility and lower doping capability degrading the base resistance. Moreover, InP substrate costs much more than GaAs substrate.

Now, different HBT types on InP substrate will be compared. There are two common heterojunctions for InP HBTs. These are InP/InGaAs and InAlAs/InGaAs. From Table 2.2, valence and conduction band discontinuities show that, InP/InGaAs heterojunction will offer a larger valence band step than InAlAs/InGaAs. This will reduce the hole back injection from base to emitter and therefore it will offer higher current gain. But on the other hand, since InAlAs does not contain Phosphor (P), this makes it easier to be grown in MBE (molecular beam epitaxy) systems [34]. In this work, we will concentrate on the InP/InGaAs single heterojunction bipolar transistors (SHBTs). To compare these structures, simulations have been performed using SimWin 1.50 [35].

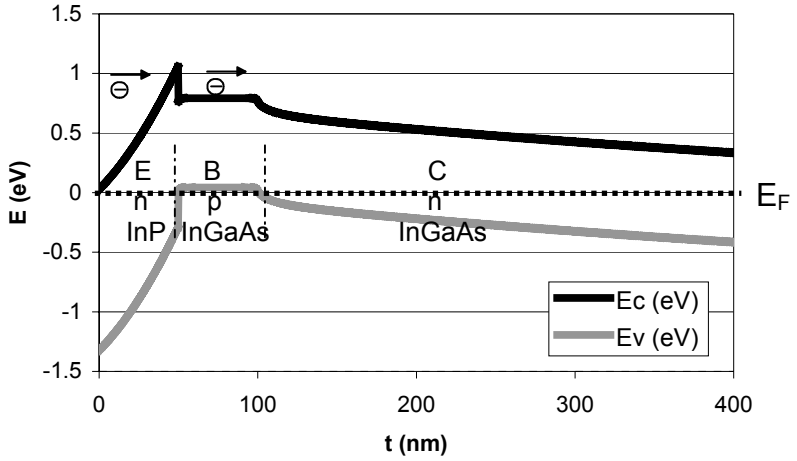


Figure 2.10 The band line-up of base, emitter and collector in InP/InGaAs SHBT (no voltage applied)

SHBTs do not suffer from the conduction band barrier in base-collector junction but since the collector material has low energy band gap, this results in lower breakdown voltages. Therefore, DHBTs are proposed having wider band gap material in the collector as shown in Figure 2.11.

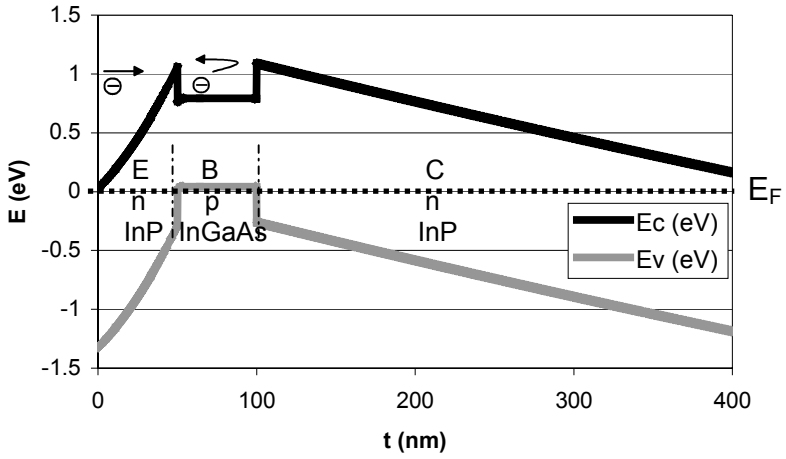


Figure 2.11 The band line-up of base, emitter and collector in InP/InGaAs DHBT (no voltage applied)

As it is depicted in Figure 2.11, there is blocking of the electron transport at the base-collector junction due to conduction band barrier. This will degrade the HBT performance [36]. The electrons emitted by emitter will tunnel through the base emitter junction. Since the collector is low doped, the depletion region is thick and this may result in electrons to be reflected from base-collector junction [37]. To overcome this problem, quaternary materials and spacer can be introduced between base and collector. This will minimise the conduction band barrier in BC junction and lead to better HBT performance. In Figure 2.12, a composite collector InP/InGaAs DHBT, with one InGaAs spacer and two InGaAsP quaternary layers, is shown.

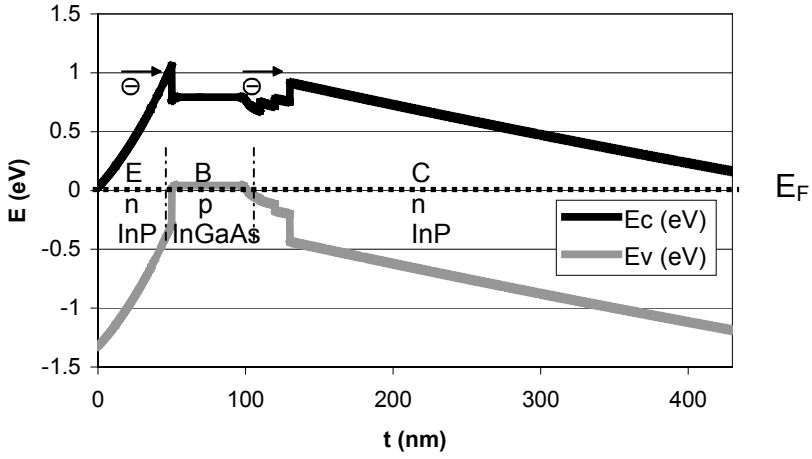


Figure 2.12 The band line-up of base, emitter and collector in InP/InGaAs DHBT with composite collector structure (no voltage applied)

Even though DHBTs offer higher breakdown voltages, there are some difficulties in growth and processing of InGaAsP layers.

Especially, in the last decade, there is a relatively new DHBT structure with GaAsSb base [38, 39, 40]. It has several advantages over the InP/InGaAs heterojunction. First of all, since they have no conduction barrier in the base-collector junction, they do not require any complicated composite collector structures. These make them easier to grow and process.

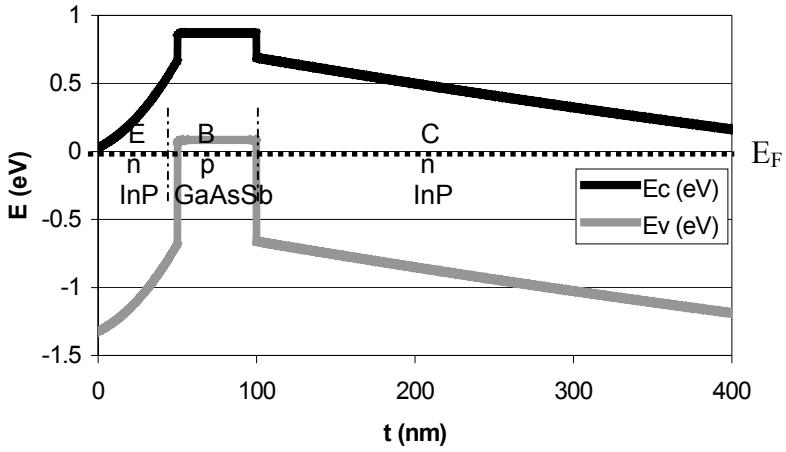


Figure 2.13 The band line-up of base, emitter and collector of InP/GaAsSb DHBT (no voltage applied)

Moreover, the valence band discontinuity of InP/GaAsSb DHBT is much higher than InP/InGaAs HBT, which makes the hole back injection almost negligible.

2.3 Vertical Design of HBTs

There are two well-known growth techniques for InP HBTs. These are Molecular Beam Epitaxy (MBE) and Metal Organic Vapour Phase Epitaxy (MOVPE). In MBE systems, elemental Group III and V sources are used. It is difficult to handle the elemental phosphorus (P). Because of this, gaseous sources like AsH_3 and PH_3 are introduced to these systems. These modified systems are called gas source MBE (GSMBE). In MOVPE, all Group III sources are metal organic sources [41, 42, 43, 44]. The HBTs used in this thesis were grown with an AIX200 RF 200 low pressure

MOVPE system with fully non-gaseous sources. Further details about the growth and doping are given in [41].

In Table 2.3, a typical SHBT layer structure is shown.

Table 2.3 Typical SHBT layer structure used in this thesis

Emitter-cap	n^{++} InGaAs	$1x10^{19}$ cm^{-3}	100nm
Emitter contact	n^{++} InP	$1x10^{19}$ cm^{-3}	50nm
Emitter	n^{+} InP	$2x10^{17}$ cm^{-3}	50nm
Base	p^{++} InGaAs	$2x10^{19}$ cm^{-3}	50nm
Collector	n^{-} InGaAs	nid	600nm
Stop Etch	n^{-} InP	$8x10^{17}$ cm^{-3}	10nm
Subcollector	n^{++} InGaAs	$1x10^{19}$ cm^{-3}	300nm
Buffer	InP	nid	50nm
SI. InP Substrate			

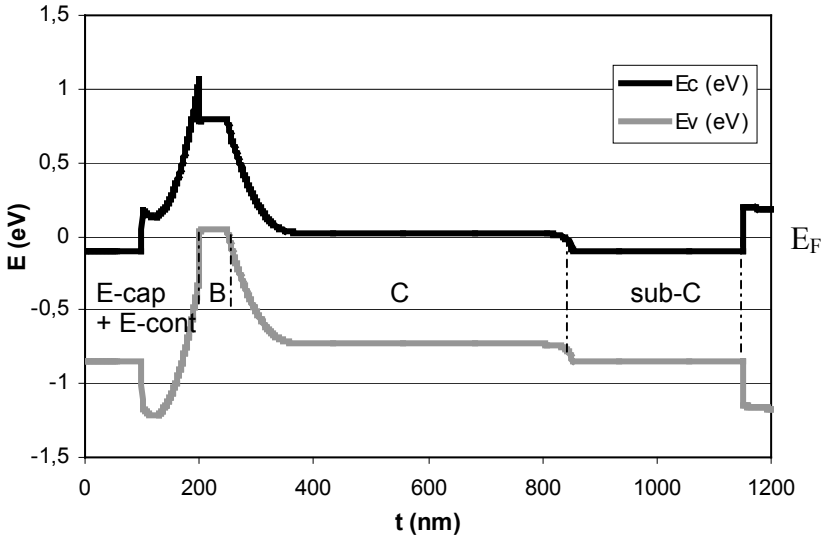


Figure 2.14 The band line-up of complete layer structure of an InP/InGaAs SHBT given in Table 2.3 (no voltage applied)

The InGaAs emitter cap serves as a contact layer for the emitter contact, to achieve low value ohmic emitter contact. The doping density of the emitter cap is in the

range of $1x10^{19}$ cm^{-3}. The thickness is chosen as 100 nm to have a lower emitter resistance and an optimum underetching. Since wet chemical etching is used intensively, thicker emitter will result in higher underetching leading to higher emitter and base resistances. On the other hand, since it may cause short circuit with base contact for self aligned HBTs, it is critical to have too thin emitter cap. Here, there is another layer used to reduce the contact resistance. 50 nm of highly doped ($1x10^{19}$ cm^{-3}) InP emitter contact layer is sandwiched between emitter cap and emitter layers.

Wide bandgap InP is chosen as emitter layer. The doping density is around $2x10^{17}$ cm^{-3}. The doping density is in this range to keep the base-emitter capacitance low. But, on the other hand, there is a lower limit for the doping, which should provide enough electrons for the current.

The base layer is one of the most critical layers in HBTs. As mentioned in chapter 2.1.2, this layer defines the current gain of the transistor. The thickness should be chosen as thin as possible to prevent excessive recombination and loss of electrons trying to reach the collector. Moreover, the thinner base results in shorter base transit time (equation 2.6) leading to higher cut off frequency. On the other hand, the sheet resistance is inversely proportional to the thickness. To overcome this problem, the base should be highly doped to provide lower sheet resistances. Here, in this work, for SHBTs, the base is 50 nm thick with $3x10^{19}$ cm^{-3} p-type doping.

The collector layer is mostly determining the maximum current density and the breakdown voltages of the HBTs. Here, for standard SHBTs, 600 nm thickness is preferred for two major reasons: One is to achieve sufficient breakdown voltages. The other is to have enough underetching for the collector to reduce the base-collector parasitic capacitance and to improve the RF performance. On the other hand, this thick collector will result in a lower cut-off frequency. Another important aspect for the collector is the doping influencing the maximum current density. This maximum current density is mainly specified by the Kirk Effect [17, 45, 46]. When no current is flowing through the HBT, I_C=0, the electric field profile and charge distribution in the base-collector junction will be as depicted in Figure 2.15 a. At this case, the holes in the base layer will diffuse towards the collector and the electrons in the collector will diffuse towards the base layer. These carriers will recombine and there will be positively ionised donors and negatively ionised acceptor on collector and base side, respectively. The electric field caused by these ions will prevent the further diffusion.

When the collector current increases and reaches to critical value ($I_C > qN_C v_{sat}$), where the electron density entering the base-collector depletion equals to the donor density, then the space charge region in the collector side is neutralized. The electric field is then caused by a dipole layer as shown in figure 2.15b. Further increase of current will cause base depletion layer move towards the collector. This will lead to an increase in the base width.

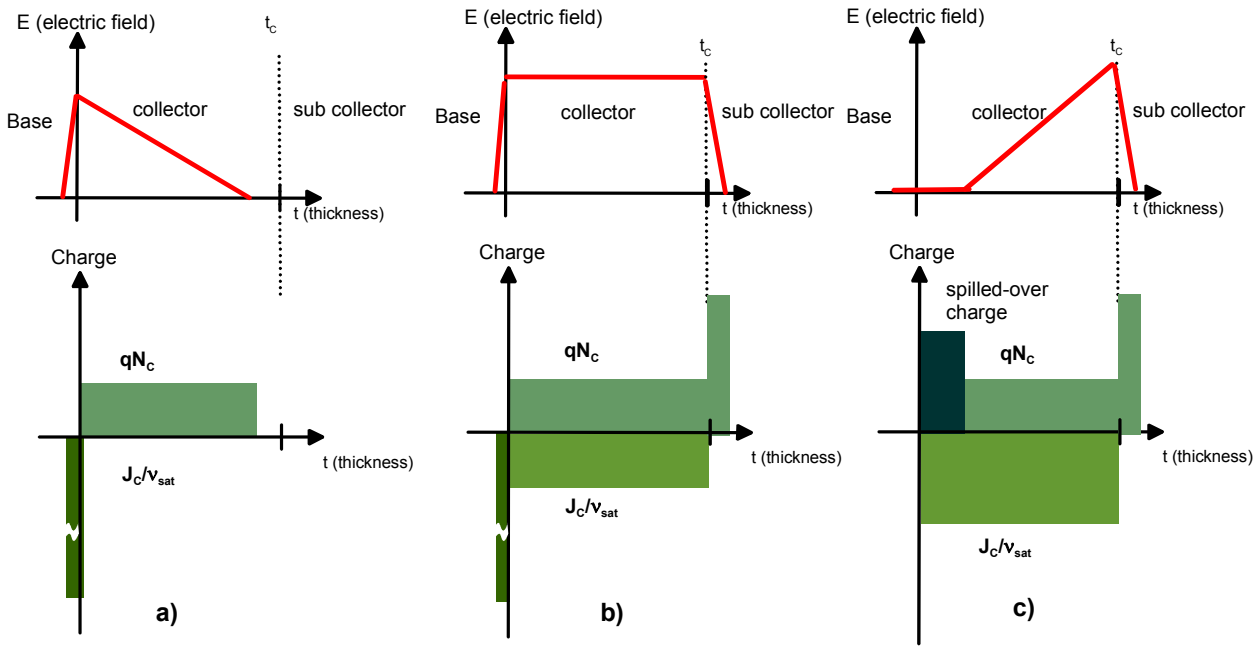


Figure 2.15 The charge distribution and the electric field profile in base-collector junction of HBT. a) low current case. b) I_C is high enough to make $n = N_C$. c) I_C is so high that $n > N_C$. As a result electric field profile changes and charges are spilled-over to the collector region

Since there is a larger distance for carriers to penetrate, this will degrade the current gain and also increase the base transit time and degrade RF performance. The current density, where this effect sets in is defined as J_{Kirk}. It is depicted as in Equation 2.14.

$$J_{Kirk} = (1 + \frac{V_{CB} + \phi_{CB}}{V_2 + \phi_{CB}}) q N_C v_{sat} \qquad \text{equation 2.14}$$

Here, ϕ_{CB} can be given as follows:

$$\phi_{CB} = \frac{E_g}{2} + \frac{kT}{q}\ln(\frac{N_C}{n_i}) \qquad \text{equation 2.15}$$

where;

ϕ_{CB} : Base-collector junction potential

V_2 : Applied base-collector bias that totally depletes collector layer when J_C=0

N_C : Collector doping

v_{sat} : Saturation velocity

n_i : intrinsic doping density

E_g : Energy band gap of the material

k : Boltzmann's constant (8.62×10^{-5} eV/K)

T : Temperature in Kelvin

By using equation 2.14 and 2.15, J_{Kirk} for the structure in Table 2.3, is calculated as 1 mA/μm^2. In this calculation, ϕ_{CB} is found to be 0.45 V. In the calculation of base-collector junction potential, $E_{g,InGaAs}$ is accepted as 0.76 eV. V_2 is calculated to be around 21 V and saturation velocity for InGaAs is taken as 7×10^6 cm/s [43, 14].

For small area devices there will be also delay of the Kirk Effect. At high injection levels, the carriers flow outwards when they enter the collector, because of a lateral concentration gradient existing in the depletion region. If the effect of lateral electric field is neglected, the amount of the spreading is approximately:

$$L_D = \sqrt{D.\tau} \qquad \text{equation 2.16}$$

where, L_D is the amount of spreading, D is the high field diffusion constant, τ is the collector transit time. The transit time is determined by the collector thickness (T_C) and the average drift velocity, υ_s. This means that L_D is determined by the layer structure and is independent from the lateral design of HBTs. For our SHBTs, L_D is calculated to be 0.4 μm. This value is much more important when the emitter width gets smaller. Especially for submicron HBTs, the shift in the maximum current density can be

explained in this manner [47]. This effect is elaborated in Chapter 5 with submicron emitters.

The 10 nm InP stop etch layer is used to stop directly on the InGaAs subcollector during etching. The etching rate of InP is much lower than in InGaAs with H_3PO_4 based etchant. In other words, InGaAs is selectively etched with this chemistry. This layer enhances the stability and reproducibility of the process technology.

The 300 nm subcollector serves as contact layer for the collector contacts. Like in emitter cap layer, it is highly doped to achieve ohmic contacts. Since this layer is n-type and highly doped with a sheet resistance of 8 Ω/sq, it is possible to realise low resistances about 2-3 Ohms, which is an important aspect for circuits. Since the epitaxial quality may degrade by higher doping levels for InGaAs, it is not preferable to dope the subcollector with doping densities higher than $1x10^{19}$ cm^{-3}

A thin InP buffer layer is used to have better starting conditions for the HBT layer growth.

2.4 Lateral Design of HBTs

As already explained in Chapter 2.1.3, two main parasitics affecting the RF performance are: base resistance and base-collector capacitance. Here, we will focus on techniques used to reduce the base resistance and/or the base-collector capacitance.

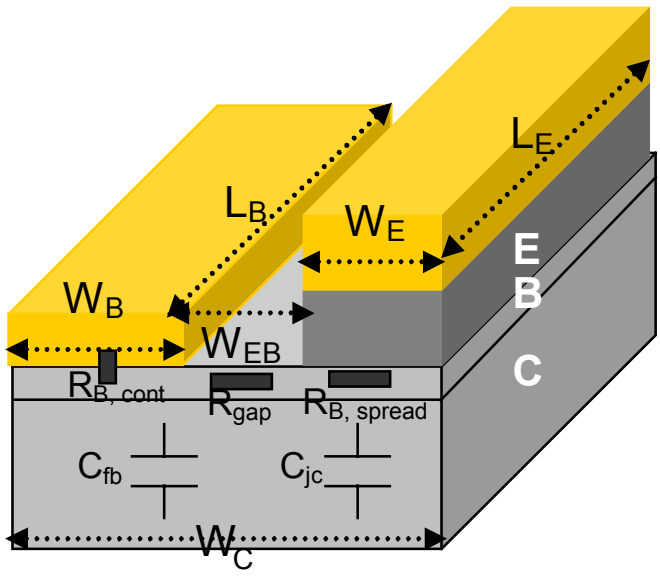


Figure 2.16 Schematic of HBT showing the dimension influencing the RF performance.

As depicted in equation 2.11, there are two major parameters influencing the base resistance. These are base-emitter contact spacing (W_{EB}) and the emitter width (W_E). The base-emitter contact spacing can be minimised by self-aligned base contacts, which will result in decrease in R_{gap}. For the reduction of the base-collector capacitance, one should reduce the base-collector junction area. One of the most common and mature techniques is to laterally etch the collector and, as a result, to reduce the respective area and capacitance [48, 49]. This method is effective especially for DHBTs. But, since in SHBTs, the base and collector material are same and this prevents selective etching, it is difficult to reduce the parasitic capacitance without affecting the base resistance. While the collector is laterally etched, the base will also be underetched. If this underetching is greater than the transfer length of the contact, this will lead to higher base resistances, which will degrade the RF performance. To prevent this problem, additional solutions have already been proposed, like shown in Figure 2.17 [50]. With this technique, the base layer is protected by SiN from all sides during the etching of collector layer. So, even in SHBTs, C_{bc} is reduced without degrading the base resistance.

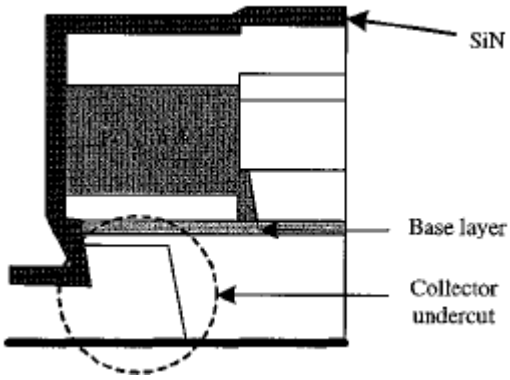


Figure 2.17 Schematic of the HBT's underetched collector protected by SiN by Lee [50]

Another old technique to reduce the C_{bc} is the ion implantation in the external base contact area [51].

There are also some growth related solutions to reduce the base-collector capacitance. These are regrown emitter and base. In regrown emitters [52], active base-emitter junction area is defined with an insulator and the emitter is grown after this step. The advantages of this procedure are: firstly emitter-base junction area can be reduced

regardless of the size of the contact holes. Secondly, emitter contact resistance can also be reduced by using larger metallization.

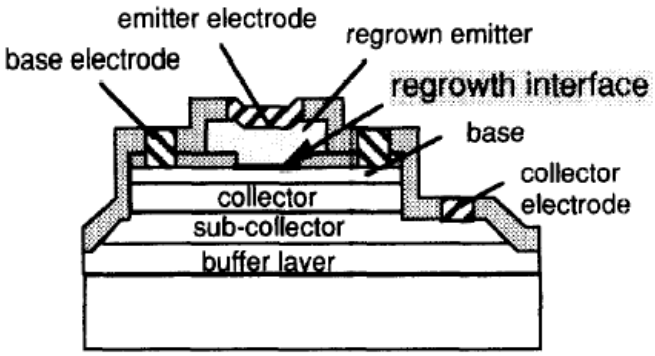


Figure 2.18 Schematic of the HBTs with regrown emitters proposed by Tanoue [52]

Another technique is to regrow the base [53]. With this technique, base layer underneath the base contact is regrown with highly doped material.

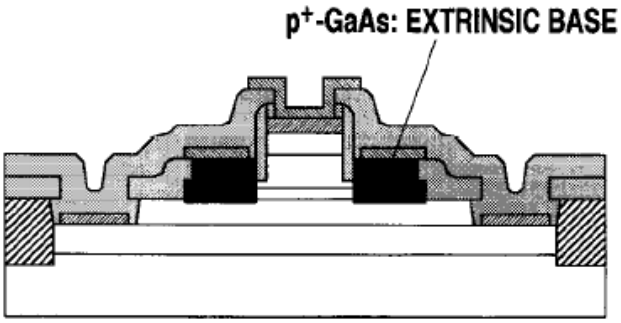


Figure 2.19 Schematic of the HBTs with regrown base contact proposed by Shimawaki [53]

The main advantage is, base can be thin without affecting the base contact resistance and current gain. Thinner base will lead to lower base transit time and higher cut off frequency. There are other similar regrown methods described in literature [54]. One of the latest growth techniques is using buried collector metal [55]. In this technique, prior to the HBT growth, tungsten metal wires are defined on the InP substrate. After that, layer structure is grown and these tungsten metal wires stay buried underneath the

emitter area and eliminating the extrinsic base-collector resistance. These techniques suffer from complicated epitaxial growth.

One popular method is the transferred substrate HBTs. Using this technique, maximum oscillation frequency, f_{max}, above 800 GHz is already presented [56]. The main idea is to process the collector contact from the backside and achieving reduced parasitic capacitance. Basically, emitter and base contacts are processed from the front side and then the wafer is transferred to a carrier substrate (mostly Si). After the transferring step, InP material is etched away till collector. The collector contact is realised from the backside of the wafer and this contact area defines the base-collector capacitance [57, 58, 59, 60, 61]. This technique is also realised during this work [62]. The details about the developed process and related results can be found in Appendix B.

3 Fabrication of HBTs

The fabrication of HBTs starts with the epitaxial growth of the desired HBT layer structure on semi insulating InP substrate. In this chapter, the processing details of the HBT process will be discussed. The critical steps of processing and the experiments performed to optimise the processing will be presented. Moreover, different layouts and their influence on the HBT performance will be discussed.

3.1 Main Steps of HBT Processing

The epitaxial growth and the processing of the HBTs are performed in clean room environment. The standard HBT is processed in a triple mesa design. During the processing of an HBT, 7 different mask layers are used. 3 etching steps are performed to form the mesa structures and 4 metallization steps for the contacts.

3.1.1 Lithography

This is one of the most critical steps for HBT processing. Basically, it is defined as the step replicating the patterns on the mask to the wafer. There are two main groups of lithography techniques. These are electron beam lithography (EBL) and optical lithography. During this work, for prototyping purposes EBL and for the processing of HBTs optical lithography are preferred. With EBL, it is possible to realise structures of 100 nm width with a tolerance close to 0. But on the other hand, especially for larger structures, in comparison to the optical lithography, EBL consumes much more time to write the patterns. Because of this, EBL is not preferred as main lithography technique, here. For the evaluation of the new layouts and new techniques, to save time and cost, EBL is used only for prototyping purposes.

For optical lithography, there are 3 main components. These are mask, photoresist and mask aligner. The optical masks are quartz masks with chromium (Cr) surface layer on. The structures to be replicated are transferred to the masks. The chromium layer (opaque layer) is used to block UV light (λ_1= 365 nm, λ_2= 405 nm), which is used to expose the structures. The quartz is transparent. Photoresists are photosensitive materials. They are liquids deposited using spin coaters, to form thin films. By changing the spinning time and speed of the spin coater, the thickness of the

film can be adjusted according to the demands. There are two main types of photoresists. These are negative and positive resists. The exposed negative photoresist is insoluble in the developer. In contrary, the positive photoresist is soluble in developer when it is exposed to UV light. Negative resists offer lower resolution but are much more sensitive than the positive ones.

In our standard process, we prefer using positive resists to form mesa and contact structures. We use AR-P 5350 and AR-P 3740 from Allresist GmbH [63] as standard photoresists for contacts and mesas, respectively. Especially, to provide good contact and adhesion of the photoresist, special efforts have to be given. Before applying any photoresist, an oxide dip should be done to remove any possible oxide film from the surface. In addition, the sample should be dried before applying the photoresist. For our processes, a Karl Süss MA6 mask aligner is used. With this system, it is possible to form structures with 0.7 μm width, with a tolerance of ± 0.1 μm. Here, the misalignment tolerance is about ± 0.25 μm. To achieve reliable and reproducible structures, 1 μm is chosen as minimum width. To obtain better resolution and real dimension close to nominal dimensions, vacuum contact is utilized, even though it degrades the durability of the mask.

3.1.2 Etching

Basically, etching can be described as the removal of material in the depth of the wafer. There are two main techniques: Wet chemical and dry etching. In wet chemical etching, mostly acids are used to remove the material from the surface. Basically, acid interacts with the material; forms new byproducts and these byproducts are removed from the surface. According to the application, there may be different demands for etching, like higher etch rates, uniformity, an/isotropy, selectivity, less damage to the surface. Especially for HBT applications, low etch rate, uniformity, selectivity, anisotropy and less damage to the surface are main demands.

Uniformity is defined as the etch rate deviation across the wafer. A high etch rate uniformity is necessary to have reliable devices with similar dc and RF properties.

Selectivity is defined as the ratio of the etch rate for different materials.

$$Selectivity = S = \frac{Etch\,rate\,of\ Material\,1}{Etch\,rate\,of\ Undesired\ Material\,2} \qquad \text{equation 3.1}$$

For example, to be able to stop etching on really thin base layer, emitter mesa etching should be selective to base etching.

An/isotropy is the etch rate difference for different crystallographic directions. The degree of isotropy "A", is depicted as:

$$A = 1 - \frac{R_L}{R_v} \qquad \text{equation 3.2}$$

where R_L is the lateral etch rate and R_v is the vertical etch rate. When $A = 0$ then the etching is perfectly isotropic and when $A = 1$ it is called as perfectly anisotropic.

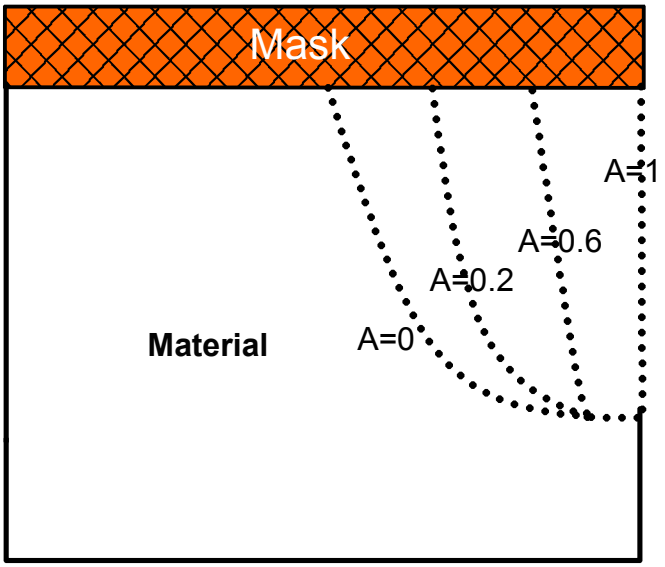


Figure 3.1 Schematic of underetching of the mask for wet chemical etching. The selectivity of material to the mask is assumed to be infinite. (S= ∞)

There are two types of etching processes. One is the diffusion controlled, where the diffusion of the active species to the surface and the removal of the soluble product occur. The other is: reaction limited, where chemical reaction at the semiconductor surface takes place. Both diffusion and reaction limited etching is temperature dependent. Diffusion limited etching is more sensitive in terms of agitation, where the reaction-limited etching is crystallographic orientation dependent. For III-V semiconductors, e.g. for InP, since the reaction will be different for In and P, this will lead to anisotropy [43]. Diluted phosphoric acid (H_3PO_4) based etchant is used for InGaAs material. Hydrochloric acid (HCl) is used to etch InP material. Here both etchants are highly selective for InGaAs and InP, respectively.

3.1.3 Formation of Contacts

Metallic thin films are required to form device contacts, passive elements, and conductive wires. For the formation of the contacts, a Leybold LH560 evaporator is used in this work. This is a high vacuum system used to deposit different contact materials on the sample. An electron beam (e-beam) evaporator exists in the system to deposit Nickel (Ni), Germanium (Ge), Platinum (Pt), Titanium (Ti). For the deposition of Gold (Au), thermal evaporator is chosen. The main requirements for a successful contact material are: high conductivity, high-resolution patterning, resistance to corrosion and mechanical stress. For different contacts and applications different material composition has been chosen offering better contact resistance and stability. The doping density of the layer underneath the contact and the diffusion properties of the contact material to the layer play important role for the determination of the contact resistance.

To achieve stable contact with proper profile, lithography parameters should be optimised. As already mentioned in chapter 3.1.1, AR-P 5350 photoresist is preferred for the contacts. The profile of the exposed photoresist is the key point. The profile of the resist with the optimised process is shown in figure 3.2.

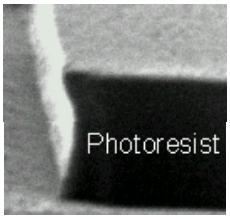


Figure 3.2 The photoresist profile for the AR-P 5350 after developing [64].

After achieving this profile, metal can be evaporated as shown in Figure 3.3.

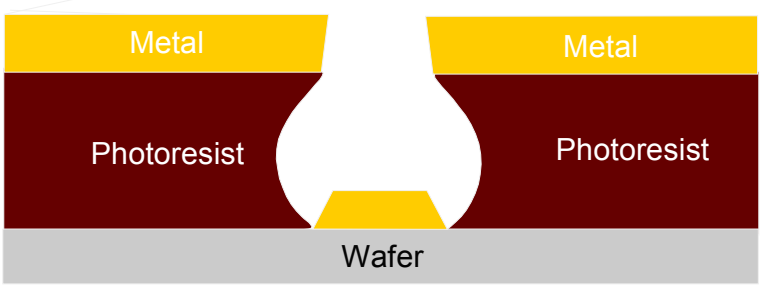


Figure 3.3 The photoresist and deposited metal just before lift off step.

After this point, lift off step starts for the contacts. Here, Acetone (Ac) is used, which dissolves the photoresist material and removes the metal deposited on the resist. By having the profile shown in figure 3.2 and 3.3, acetone may penetrate through the metal structures and dissolve the photoresist easily. In addition, with this profile, any possible short circuits between metals on the resist and material are prevented. In our processes, warm (60 °C) acetone process is used. But before heating the sample in acetone bath, the sample is left in cold acetone for 5 minutes, which will dissolve the resist lightly first. Later on, this step is followed with warm acetone step, to remove all the resist from the surface. With this cold acetone step, any polymerisation risk is prevented, which may occur with high temperature heating. This may cause difficulties in lift off and poor metal sidewall profile.

3.1.4 Processing Steps of an SHBT

The fabrication of an SHBT will be presented as an example. The details about the process and protocol are given in the Appendix C and G.

Processing of an HBT starts with the cleaning of the sample. Acetone is used to remove any organic materials, and it is followed by Isopropyl Alcohol (IPA) rinsing step to drive off any acetone residues from the sample. The next step is to remove any oxide layer from the sample surface. For this purposes, diluted HCl is used. After oxide removal, the sample is rinsed with water to stop the reaction and remove the residues from the surface.

The processing is going on by the formation of the emitter metal as shown in Figure 3.4a. As pointed out with the dotted circle in the figure, the emitters have triangular edges. This profile provides better underetching and is preventing any possible short circuit for the self-aligned base contacts. The next step is etching the InGaAs emitter cap, the InP emitter contact and emitter layers by using H_3PO_4 and HCl, respectively. Here, the emitter metal is used as etching mask. The base metal is deposited. There are 2 possible arrangements for base contacts. These are self aligned structure (sa), where the base contact metal is evaporated directly on the emitter metal as shown in Figure 3.4b and the other is the non self aligned structure (nsa), where the base contact metal is deposited 1 μm away from the emitter contact as shown in figure 3.4c. The spacing between base and emitter is realised by covering the emitter area with photoresist. Since the self aligned structures have lower base-emitter area and lower base emitter contact spacing, they will exhibit lower base-collector capacitance and base

resistance. The base contact metallization is followed by covering the base-emitter area with Durimide to protect the active area as shown in Figure 3.4d. Here, by using plasma ashing, Durimide is etched till the top of emitter contact metal is got free of Durimide. The Durimide film is used as mask for etching InGaAs base, collector and InP stop etch layers. Here, the most important thing is to have enough underetching for collector providing less parasitic base-collector capacitance. Meanwhile, the base contact should not be underetched. This may result in contact length less than transfer length and as a result higher base contact resistance.

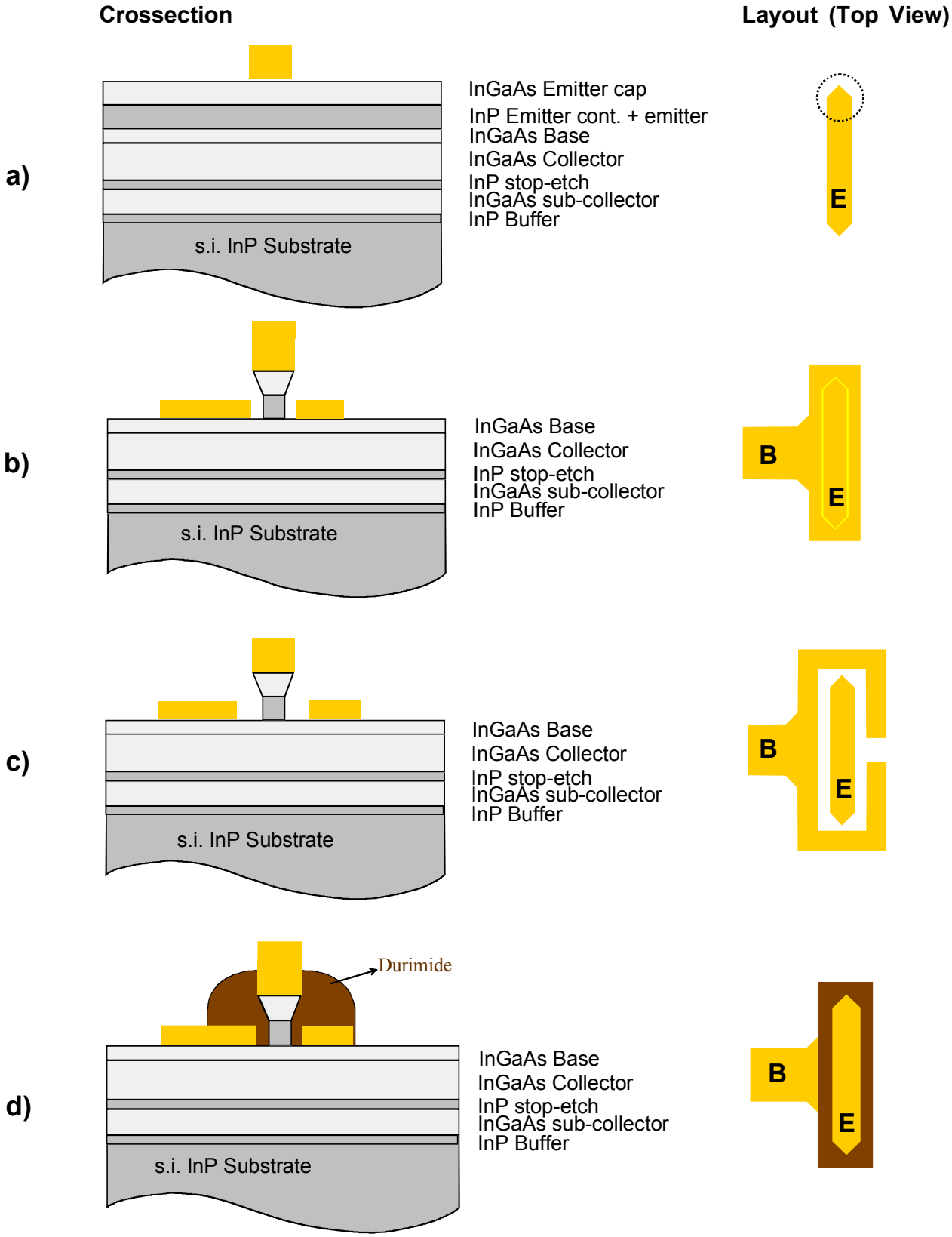


Figure 3.4a-d HBT processing steps

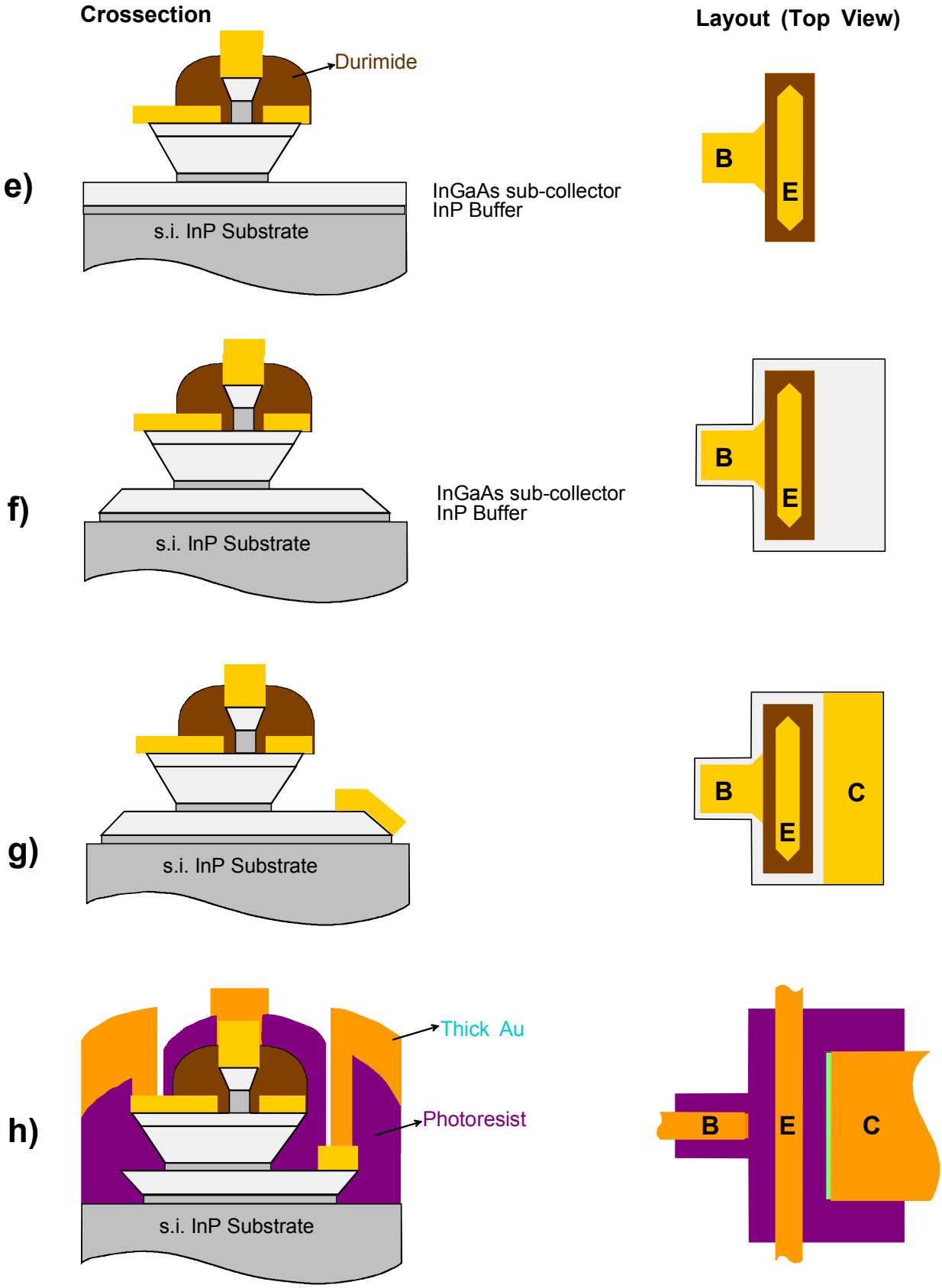


Figure 3.4e-h HBT processing steps

The area to be protected is covered with mesa resist (AR-P 3740). The InGaAs subcollector, the InP buffer layers, and the InP substrate are etched deep enough to isolate the devices on the semi insulating substrate. The profile after subcollector and substrate etching is shown in Figure 3.4f. As depicted in Figure 3.4g, the collector metal is deposited after collector mesa etching. Since it is not just collector metallization but also contact layer for circuits and passive elements, this step is named as imetal1 (Figure 3.4g). In addition to these contacts, which are really small, for measurement purposes, measurement pads are deposited. To connect these pads to the inner contacts, air bridge technique is optimised. This idea of realising connections with air bridges is to reduce parasitic effects. For this purpose, the whole device is covered with photoresist (AR-P 3740) and the areas where the connection metal will land are exposed and developed. This step is named as ISO standing for isolation layer. The last step is the thick Gold (Au) metallization step used for connection and pad metallization. Thick gold is preferred to achieve stable connection (figure 3.4h). This step is named as iMetal2, referring last metallization for pads and conductive lines for circuits.

In Figure 3.5, imetal1 and imetal2 layers separated with air bridges are presented [65].

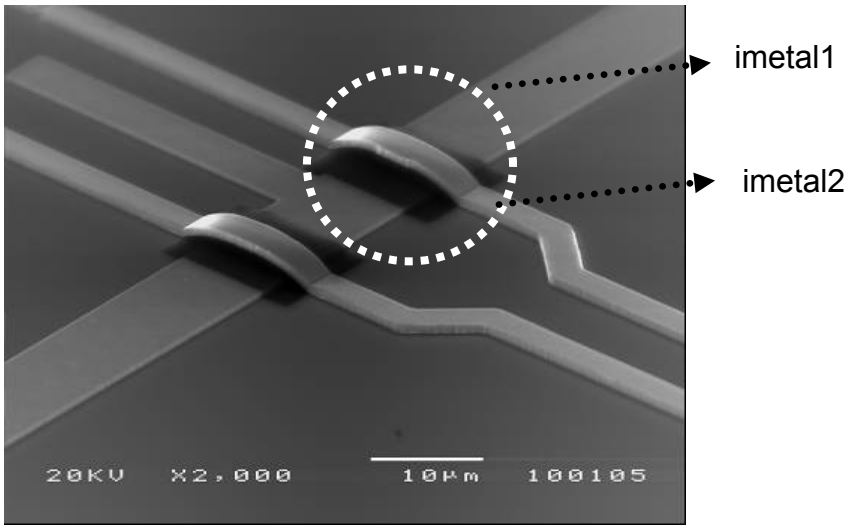


Figure 3.5 Another application for air bridge (circled with dotted line) used to separate imetal1 and imetal2, which is important especially for circuits

3.2 Improvements in HBT Processing

Here, the experiments and the ideas to improve the HBT performance will be discussed. Briefly, processing techniques prior to this work will be presented and new ideas developed during the work will be enlarged. To achieve faster HBTs, not only the layout but also the processing optimisation is an important issue.

3.2.1 Evolution of the HBT Design

Before starting the optimisation of the process, pros and cons of the previous processes are investigated. The samples processed with the previous mask set developed at 1997 and called HBT97 [41], are measured in detail. The layout of the HBT97 mask set is shown in Appendix D. According to these results, new ideas are collected for the new mask set, which is developed during this work. This new mask is called HBT03. The floorplan of the mask set is shown in Appendix E. In this sub chapter, main ideas for the HBT designs will be presented.

3.2.1.1 Orientation of the Emitters on the Wafer

On HBT97 mask set, the emitter contacts are oriented along the [001] crystal direction on a (100) si-InP substrate. In this design, since the emitter and base contact are quite small, dummy pads are used to contact the measurement pads and base, emitter contact. To minimise the additional parasitic effects due to larger dummy pads, microbridges are used. Since the etch rate is higher for [001] crystal direction, by choosing the μbridge width narrow enough, they are completely underetched. One of the 2x10 μm^2 self aligned HBT layout on this mask is shown in figure 3.6. Dotted circles designate the μbridges.

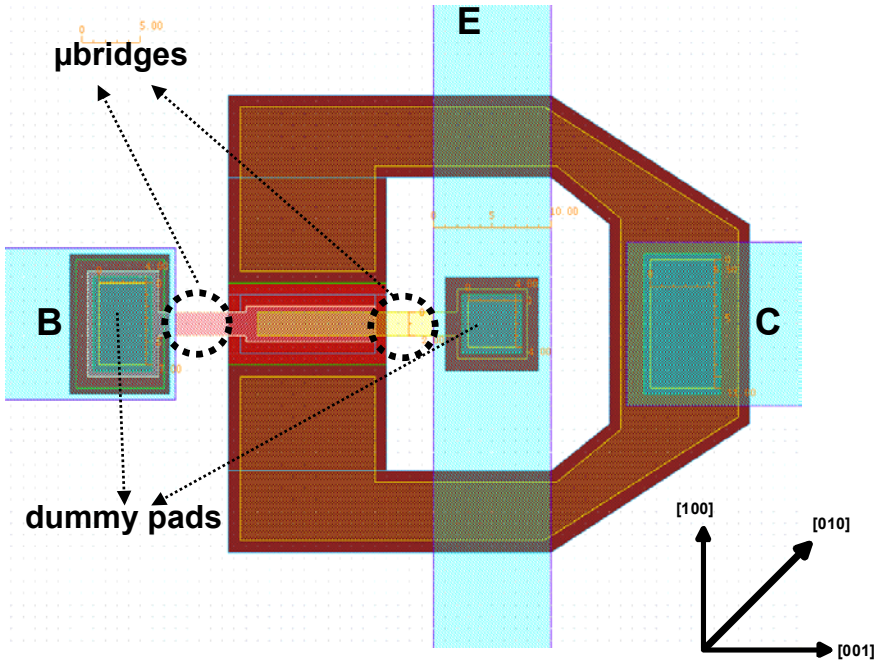


Figure 3.6 2x10 µm^2 HBT layout on HBT97 Mask

With this orientation, even though the microbridges are completely underetched and additional parasitic effects are reduced, the emitter and base resistances increase by excessively underetched emitters. This leads to degradation in RF performance. Moreover, even though, there are emitter widths varying between 1 and 3 µm with various lengths on this mask, only emitters of 3 µm width are reliable. These are really oversized HBTs to provide high-speed performance. This is due to the significant underetching for the emitter. Dependence of etching on crystallographic orientation is shown in figure 3.7 for InP based HBTs [66].

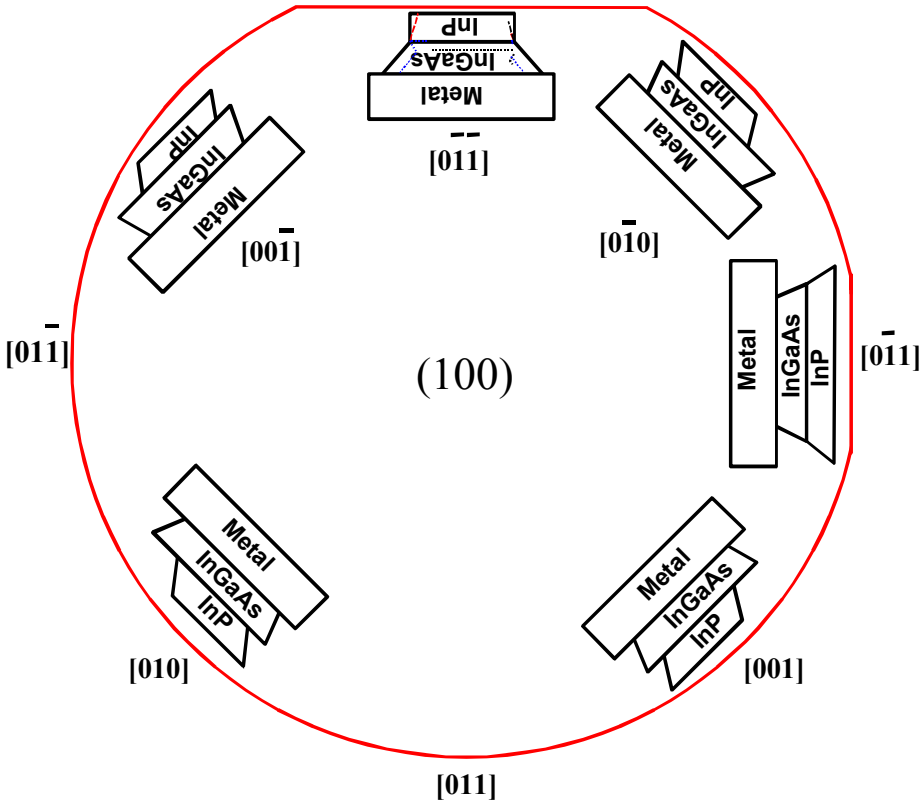


Figure 3.7 Etching Profile for Different crystal directions for InGaAs and InP [66]

Metal stripes are deposited along the [001] crystal direction and diluted phosphoric acid (H_3PO_4) and pure hydrochloric acid (pure HCl) at room temperature are used to etch InGaAs and InP layers, respectively.

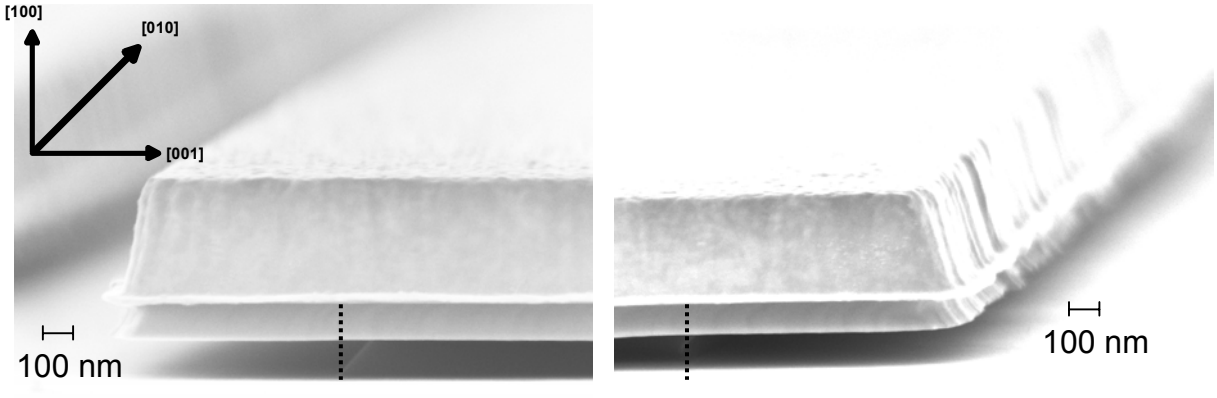


Figure 3.8 Etching Profile for different crystal directions for InGaAs and InP. Here metal stripes are deposited along the [001] crystal direction on a (100) si-InP substrate.

As shown in Figure 3.8, the underetching is nearly 750 nm for each side, which is critical to realise emitter widths less than 2 µm.

HBTs with this orientation and processing are realised and characterized. For this purpose the sample M2817 is used, for which the details about the processing details and the layer structure are given in Appendix C and Appendix F, respectively. The SEM and optical microscope micrographs for one of the processed HBTs is given in Figure 3.9.

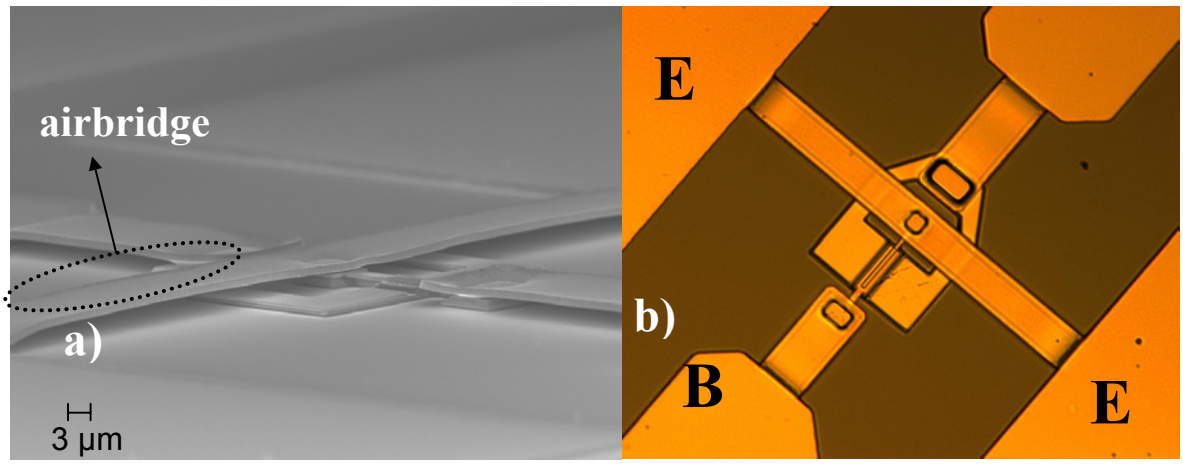


Figure 3.9 a) SEM micrograph b) Optical microscope micrograph of a 3x10 µm^2 device on sample M2821D processed with HBT97 mask

dc characterization has been performed for this device and the common emitter output characteristic in Figure 3.10 is observed.

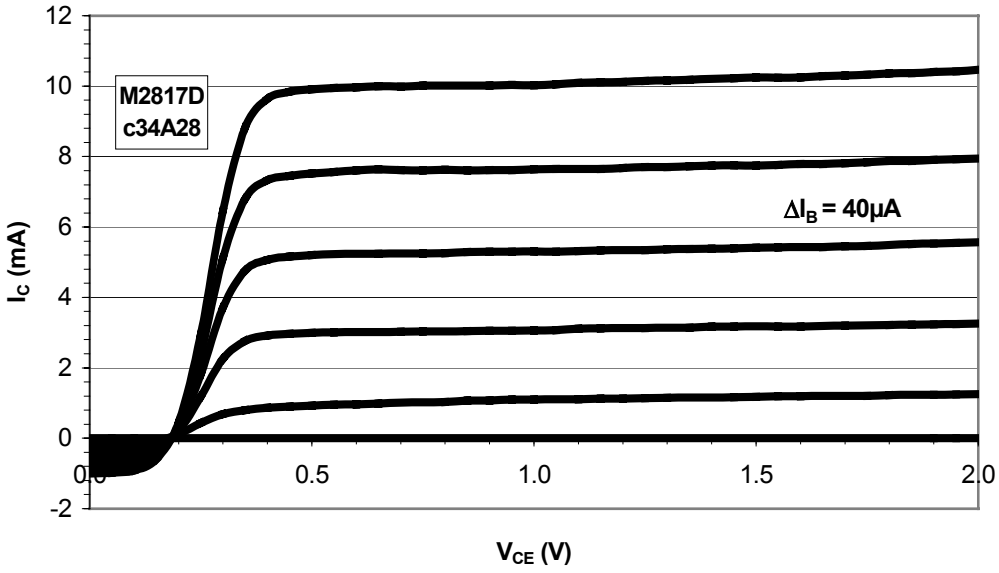


Figure 3.10 The common emitter outpiut characteristic for self-aligned 3x10 μm² device on sample M2817D

From figure 3.10, the dc current gain (B) is found to be about 50 at V_{CE}= 1.0 V and I_B= 200 μA. The breakdown voltage is measured as 3.5 V at I_C = 100 μA, when base contact is disconnected. The base and collector ideality factors are 1.29 and 1.12, respectively.

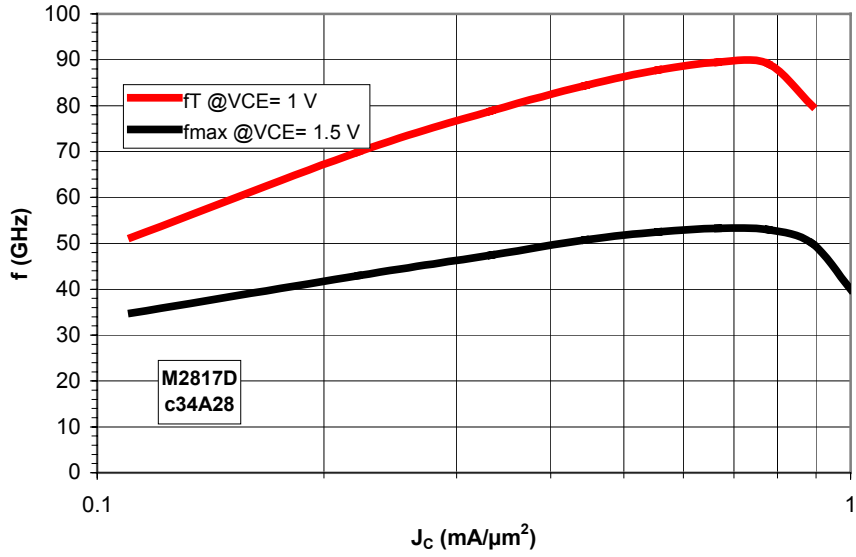


Figure 3.11 RF Performance vs. Current Density for self aligned 3x10 μm² device on sample M2817D

As shown in Figure 3.11, the maximum oscillation frequency is measured as 52 GHz and the cut-off frequency as 82 GHz at V_{CE}= 1.5 V and V_{CE}= 1V, respectively. When the nominal area is used, the maximum current density is found out to be 0.8 mA/μm^2. Even though, there were smaller devices like 1x10 μm^2, the reliable HBTs on this mask are 3x10 μm^2 HBTs. This is because of the orientation of emitter stripes (45° to Major flat) and the etchant used in this processing. These both result in total underetching of about 1.5 μm and it is not possible to realise 1 μm emitter width. The devices with 2 μm emitter width show poor RF performance mainly because of higher base resistance. On the other hand, since the device is large, the parasitic base-collector capacitance is high. Moreover, since the thickness of collector is 300 nm, it is difficult to control the underetching of the collector and reduce the C_{cb}.

To prevent excessive underetching for the emitters, they are patterned perpendicular to the major flat providing less underetching. The only problem is the etch profile for the side parallel to the major flat, which may result in short circuit for the self aligned HBTs. To prevent this, emitters are patterned as hexagonal structures [67, 68, 69]. With the conventional etchants, diluted phosphoric acid for InGaAs and pure hydrochloric acid for InP, the achieved underetching and profile are depicted in figure 3.12 and 3.13 for edges along [011] and [$0\bar{1}1$] crystal directions, respectively.

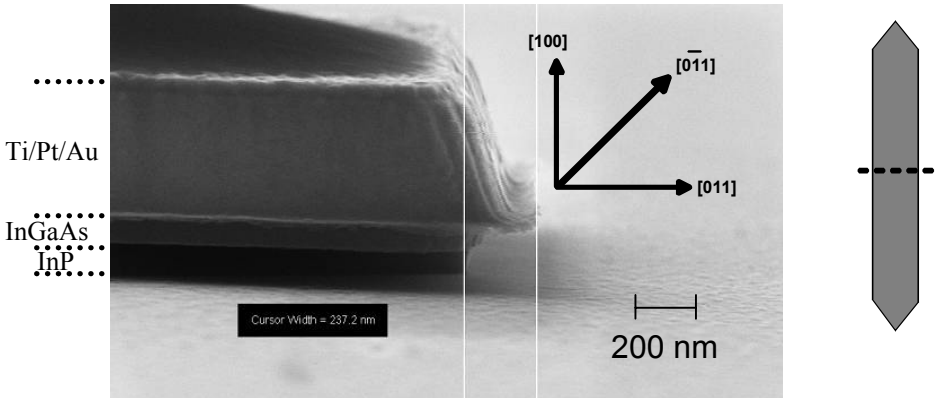


Figure 3.12 Underetching for the metal stripe in [011] crystal direction etched with pure HCl.

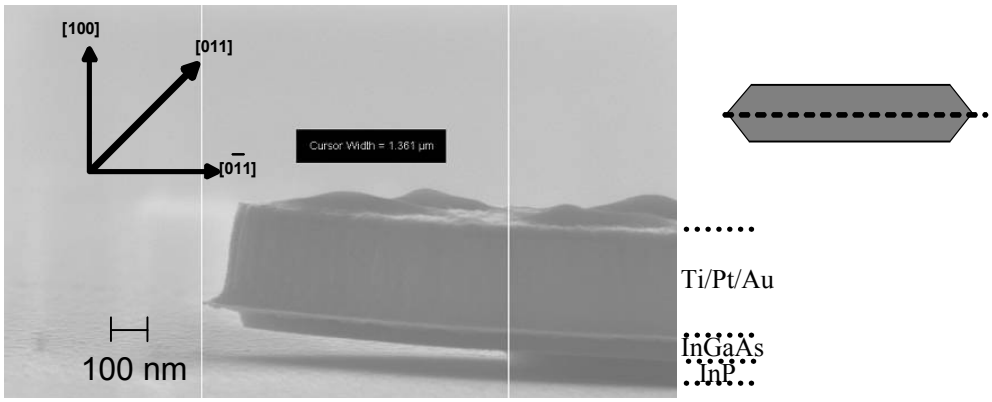


Figure 3.13 Underetching for the metal stripe in [0$\bar{1}$1] crystal direction etched with pure HCl.

Here, the underetching for each side is about 240 nm. The longer side is underetched about 1.3 µm. With this value, realization of 1 µm emitters is possible.

3.2.1.2 Optimisation of Underetching for Emitters

Even though the emitter metals are oriented along the [011] crystal direction, it has been observed that especially with pure hydrochloric acid (HCl), the underetching is still high. Since the etch rate of pure HCl is extremely high for InP (~200 nm/sec), the sample should be dipped in the etchant for a short time, less than 5 seconds, in order to etch the emitter of 100 nm thickness. This affects the reproducibility. Experiments are performed to achieve reliable and reproducible process without degrading the surface quality. There are two main parameters concerning the etch rate. One is the dilution of the etchant and the other is the temperature. In Figure 3.14 and 3.15, the effect of temperature on the etch rate of InP with pure and with 1:1 diluted HCl are depicted, respectively.

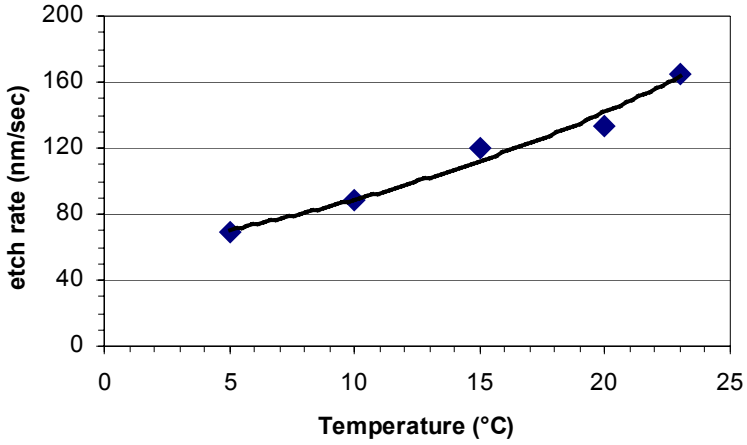


Figure 3.14 Etch Rate with respect to the etchant temperature using pure HCl for InP. The straight line shows the fitting for the measured values.

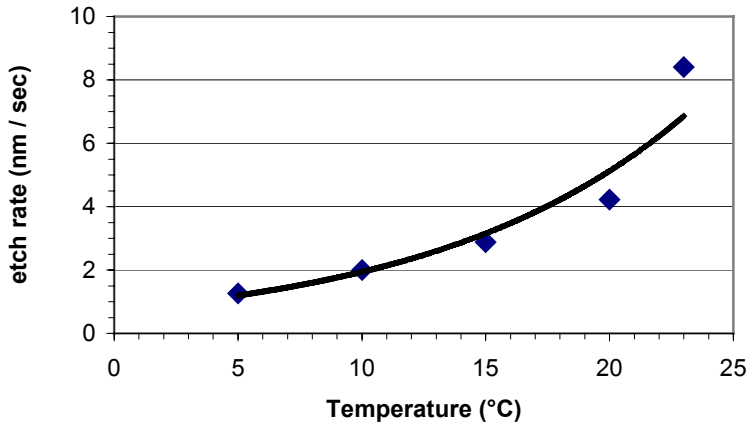


Figure 3.15 Etch Rate with respect to the etchant temperature using 1:1 H_2O:HCl for InP. The straight line shows the fitting for the measured values.

With these experiments, it is found out that using diluted HCl at room temperature will result in lower etch rates. This will improve reproducibility and reliability. The surface analysis has also shown that the roughness is comparable with the surfaces etched with pure HCl and for both etchants RMS surface roughness is about 3 nm. In Figure 3.16 and 3.17, the underetching of a metal stripe etched with diluted etchant (1:1 HCl:H_2O) are shown.

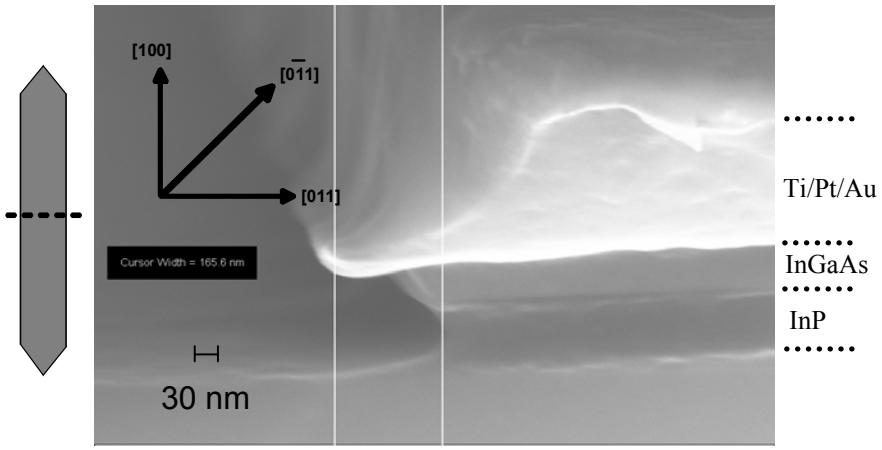


Figure 3.16 Underetching for the metal stripe along the [011] crystal direction etched with 1:1 HCl:H_2O at room temperature.

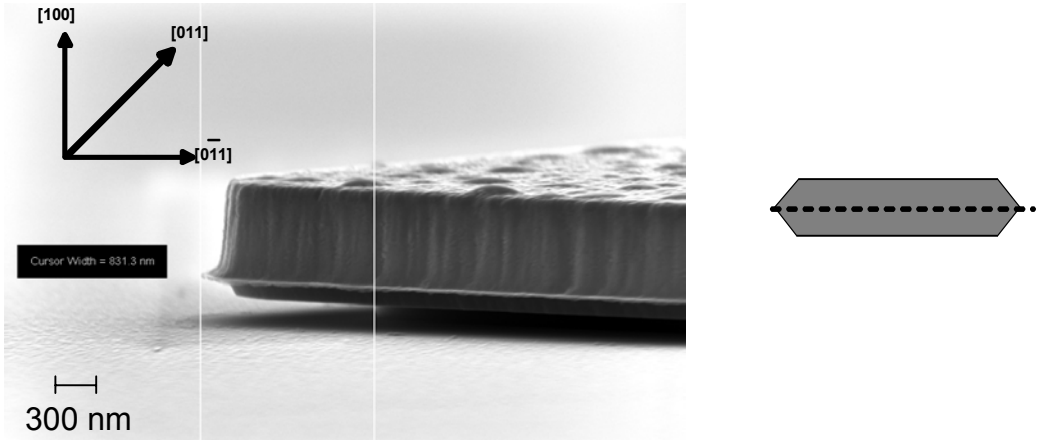


Figure 3.17 Underetching for the metal stripe along the [0$\bar{1}$1] crystal direction etched with 1:1 HCl: H_2O.

In comparison to the samples etched with pure HCl depicted in figure 3.12 and 3.13, figure 3.16 and 3.17 show less underetching. By the help of less underetching with the optimised etchant, one can realise smaller and reliable structures. Here, the underetching from one side is about 170 nm. For the longer side of the stripe underetching is about 835 nm. This is also important to reduce the base resistance of HBTs.

3.2.1.3 Directly Contacted Emitters

Regarding to the old design depicted in Figure 3.6, since there is only one microbridge connected to the emitter, the heat dissipation efficiency degrades. On the other hand, the dummy pad results in additional parasitic capacitance. Here, different techniques have been evaluated for the direct contacting of emitters.

The first method, during the ISO layer, the emitter area is also exposed and opened. The final air bridge metal is connected here, as shown in figure 3.18. Therefore it is named as exposing technique. Since the optical lithography has a tolerance of ± 0.25 μm, any misalignment causes the emitters to be short circuited with the base. Even though, this method provides functional devices, the reliability and yield are significantly low.

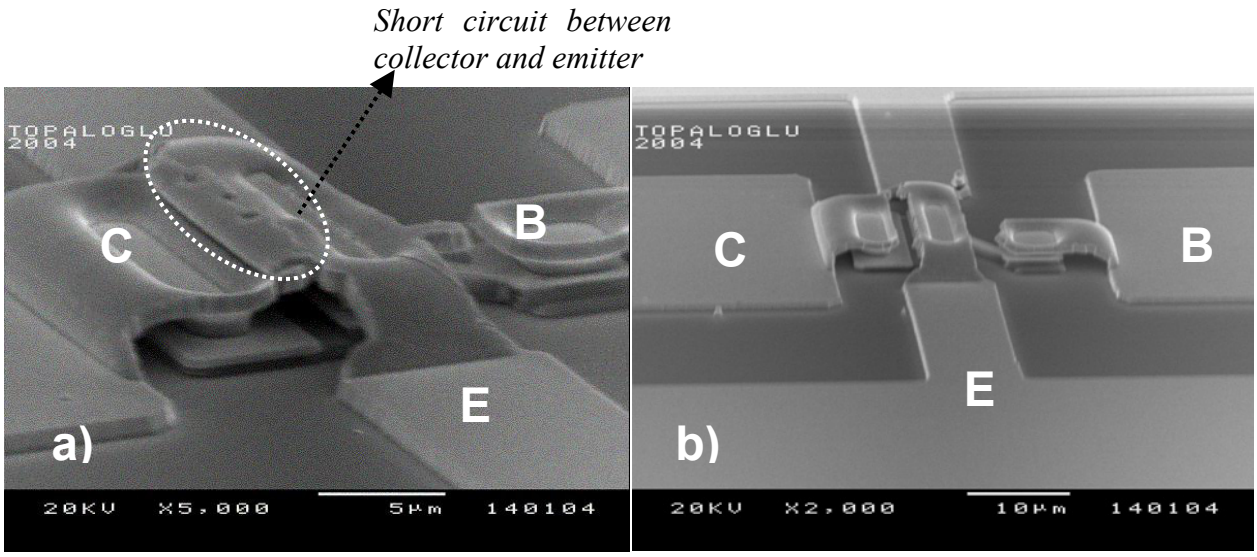


Figure 3.18 Directly contacted emitters using exposing technique

a) with failure

b) successful contact

The second technique is ashing the photoresist in the ISO step in a way that the emitter stripe is opened. Just before the last metallization step, areas covered with photoresist (ISO layer) for air bridge process, are ashed with O_2 plasma and then the metallization is performed.

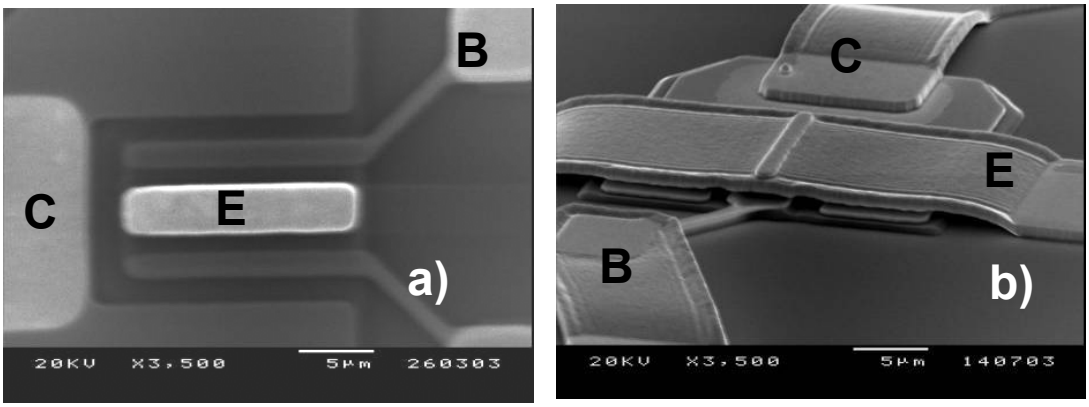


Figure 3.19 a) Opening of emitters by ashing the ISO photoresist layer
b) Final HBT with directly contacted emitters

Even though this technique is much more reliable than the previous one, any deviation in the HBT height and any fluctuation in the photoresist thickness may result in instabilities in process, which degrade the yield and reliability.

Finally, Durimide technique is investigated. Durimide is a trade name for a polyimide from Arch Chemicals, which does not require high curing temperatures [70, 71]. Regarding to this, base and emitter are covered with Durimide just after base metallization and Durimide is ashed with O_2 Plasma till the emitter stripe is opened, as explained in detail in Chapter 3.1.4. The main advantages are; a) resistant against any upcoming process like acetone proponal cleaning, etching and b) suppression of surface leakage current, both resulting in better dc performance. Here, since it is not stable and resistant against acids, photoresist is not preferred to cover the base-emitter area.

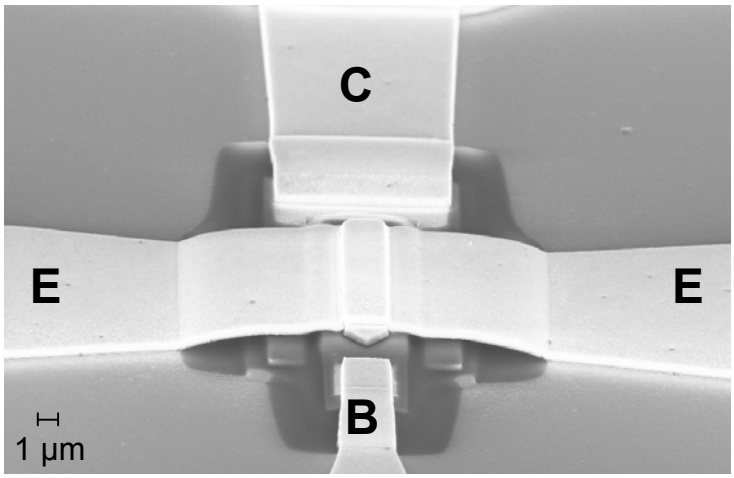


Figure 3.20 Directly contacted emitters realised with Durimide technique. The dark area is the charged photoresist.

By using directly contacted emitters, additional parasitic effects resulting from dummy pads are prevented. Moreover, heat can be dissipated by this wide emitter metal more efficiently.

3.2.1.4 Various Layouts

To achieve high speed HBTs, various layouts with different dimensions have been tested. All emitters are oriented perpendicular to the major flat i.e. [011] crystal direction and all of them are connected via direct contact technique with optimised Durimide process. Before testing these layouts, calculations have been performed. To simplify the calculations, an estimation program is written. For these estimations, the analytical equations have been utilized. The geometrical transistor design is based on the typical three-mesa design used for device fabrication. In this estimation program, a parameter file describing the complete transistor geometries and layer purposes are used as input. First of all, the effective lateral dimensions are calculated and then parameters related to the junctions i.e. junction voltages, capacitances, depletion region thickness, transit times at defined biasing points are determined. The details about the estimation algorithm can be found in [72]. According to these estimations, it has been observed that by decreasing emitter width and increasing emitter length, there is an improvement in the RF performance.

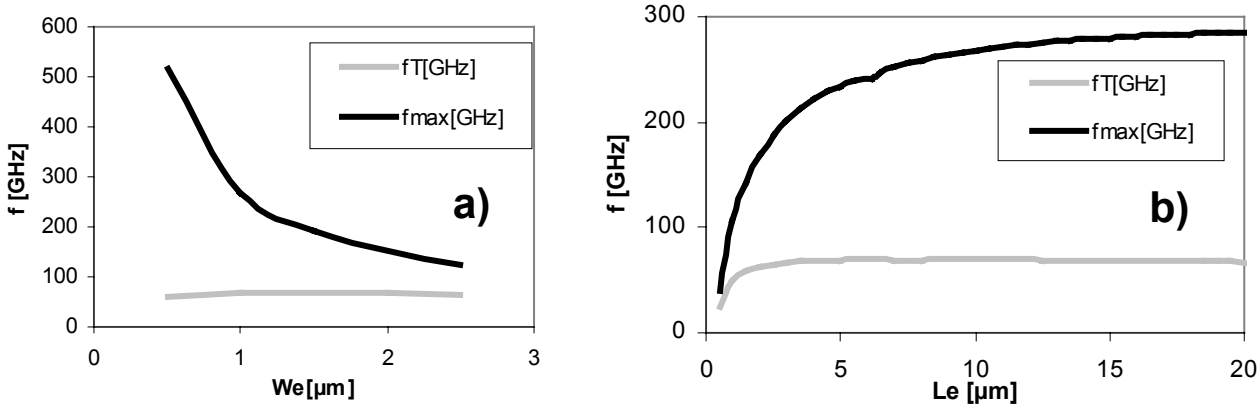


Figure 3.21 a) RF performance vs. Emitter Width (L_E= 10 µm)
b) RF performance vs. Emitter Length (W_E= 1 µm) [72]

The improvement in f_{max} by decreasing emitter width is attributed to the decrease in the base-collector area resulting in a lower base-collector parasitic capacitance. Therefore submicron emitters are required for ultra high speed HBTs. By these estimations, it is

also proven that lateral design has only weak influence on the cut-off frequency f_T. From Figure 3.21b, it can be observed that also by the increasing length of the emitter contact, the maximum oscillation frequency increases. This is attributed to the reduction of base resistance. But there is an upper limit for that, where base-collector parasitic capacitance increases proportional to the area and dominate. As a consequence, no more improvement is achieved. Briefly, the base resistance is inversely proportional to the emitter length, where the parasitic base-collector capacitance is proportional. From these estimations, 15 μm emitter length is found out to be the optimum length providing high speed HBTs for 1 μm emitter widths.

Following these estimations, a new mask set is developed in the work. It is named as HBT03. It contains different combinations of emitter widths, varying from 1 to 3 microns with emitter lengths from 5 to 15 microns. As depicted in Figure 3.22, mainly 4 different designs have been tested. In Figure 3.22a and b, there are two designs concerning base contact. In these types, dummy pads are used to contact the base. The objective was to minimise the base contact area also by underetching the microbridges like in former HBT mask set (HBT97). In Figure 3.22c, one can see the directly contacted emitters along the emitter metal. Here, the base contact should be replaced to the side of the emitter because of the air bridge metal location. In Figure 3.22d, different from 3.22c, direct emitter contacting is realised from the sides and base contact is replaced along the emitter metal. There are two main advantages with this design. First of all, heat dissipation will be much more efficient on the emitter over this wider metal. Secondly, the input signal fed to the base contact will be distributed homogenously.

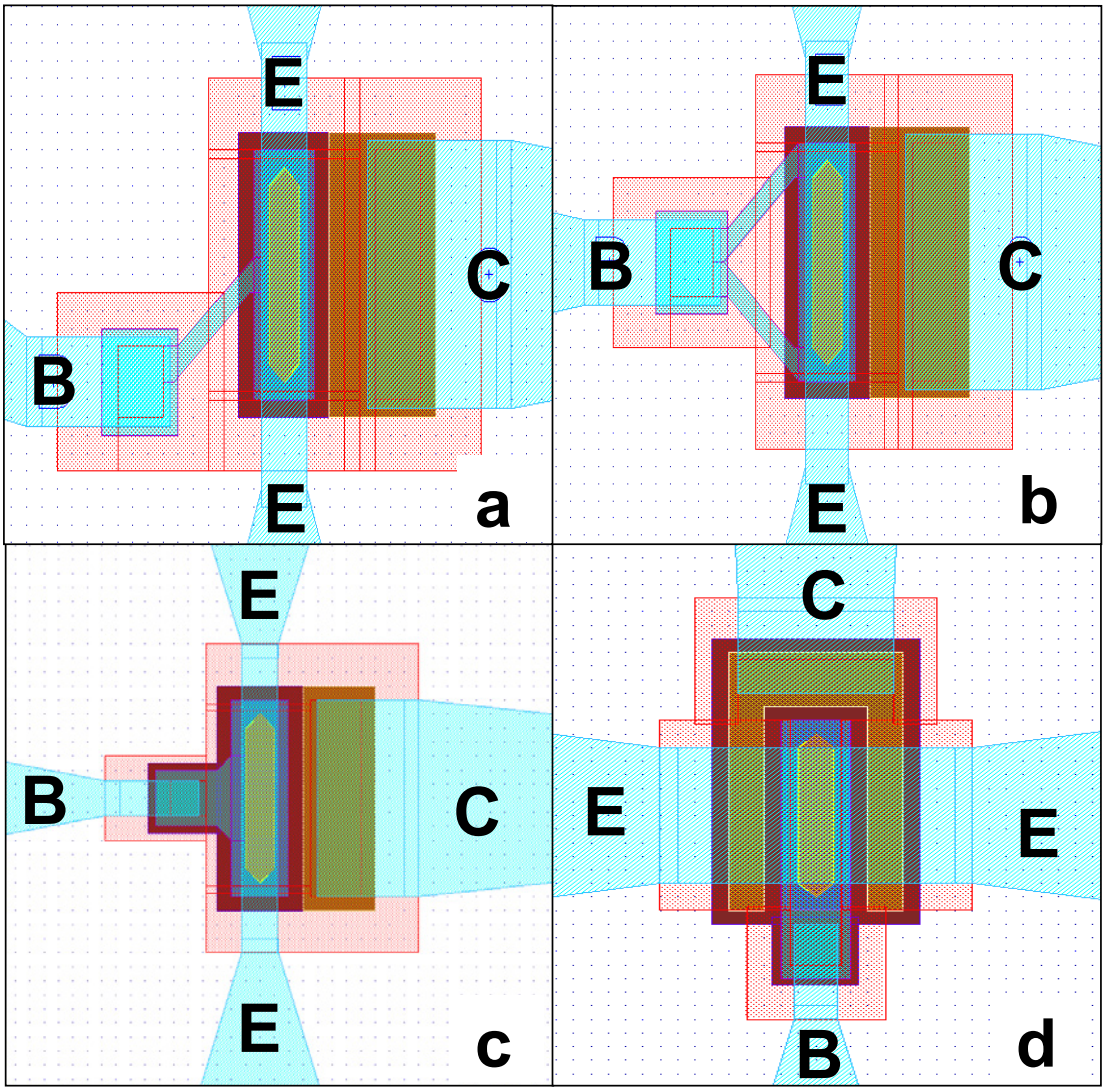


Figure 3.22 Various Layouts on the new mask set (HBT03) with different connection styles to the base and emitter contacts. a) The standard configuration with one µbridge to the base b) The standard configuration with two µbridges to the base c) The standard (std) configuration, where emitters are connected to the measurement pads along the emitter stripe d) The standard 90° (std90°) configuration where emitters are connected to the measurement pads from the emitter side

The Process Control Monitoring (PCM) structures are included in the design to achieve reproducible and reliable processes especially for optical lithography. The main aim of these structures is to minimize the possible misalignments and to obtain any valuable information during the process. A PCM structure cell of the new mask set, HBT03, is shown in Figure 3.23.

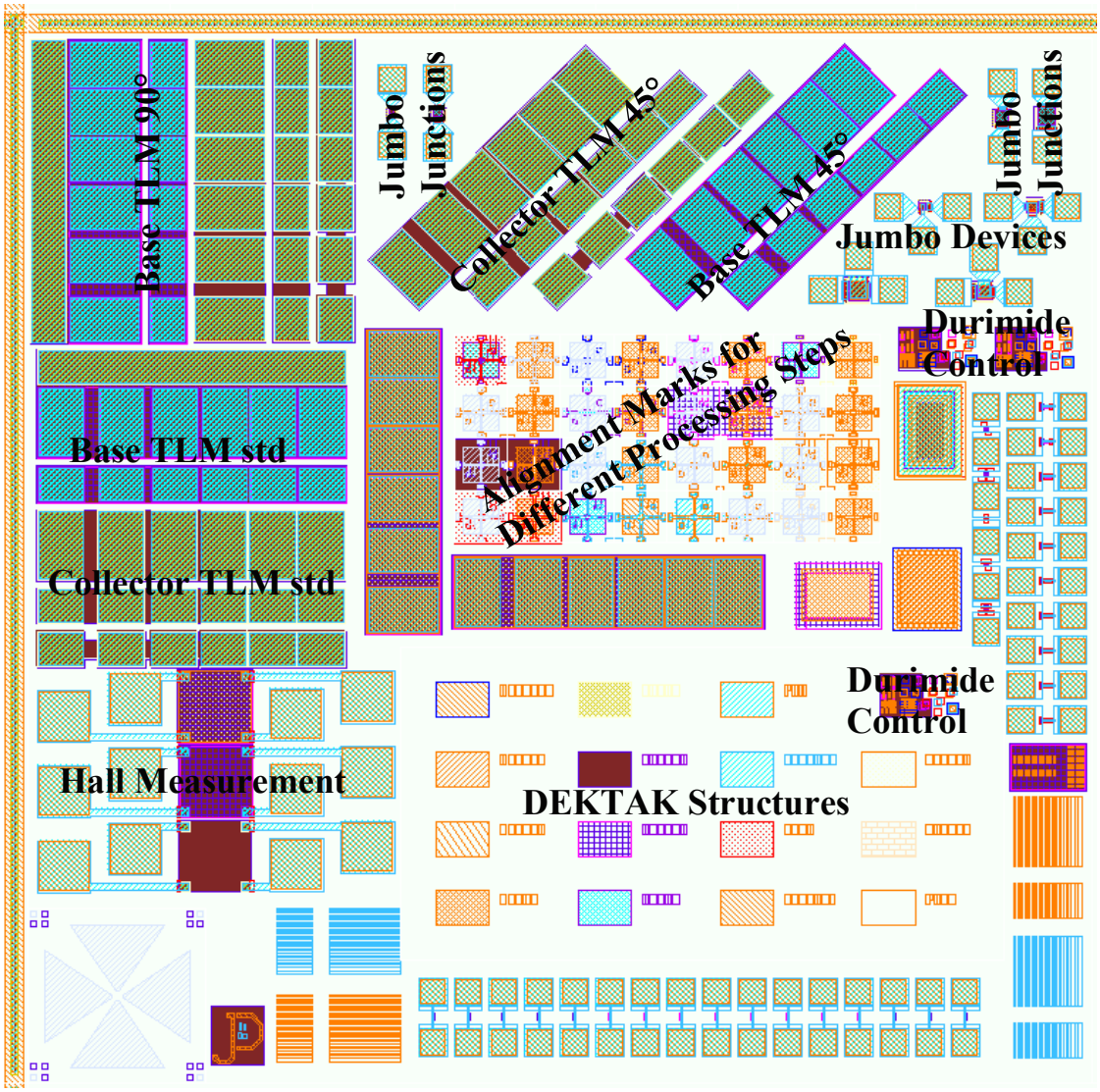


Figure 3.23 PCM (process control monitoring) cell from HBT03 used in all processing steps to control the process stability.

As it is depicted in the figure 3.23, there are different structures serving for different purposes. These structures are grouped in one cell and are repeated in different locations of the mask.

The Transmission Line Measurement (TLM) structures are used to measure the contact and the sheet resistances. There are 3 groups of TLM structures for emitter cap, base and subcollector. The TLM structures are realised with different orientations like horizontal, vertical and 45° to the major flat.

The Hall Measurement structures are used to measure the doping concentration for emitter cap, base and subcollector. Since the base is the key layer for the device, Hall measurements are performed for this layer.

There are also large HBT devices with an emitter area of 50 x 50 μm^2, which are named as jumbo devices. They are also called dc structures. The main aim is to identify the problems in processing or even in epitaxy. Therefore, these structures do not contain any air bridges. The jumbo junctions are BE and BC junctions for detailed failure identification.

"DEKTAK" structures are metal, Durimide and photoresist structures having 150 x 100 μm^2 area. DEKTAK is the model of the surface profiler from the company Veeco. It is used to measure the thickness of the thin films i.e. the deposited metal, the etched layer, the deposited photoresist layer and the Durimide during the process.

Alignment marks allow the alignment of patterns from different mask layers relative to each other and are designed for minimum misalignment in order to enhance the yield of the functional devices. A group of alignment marks are shown in Figure 3.24.

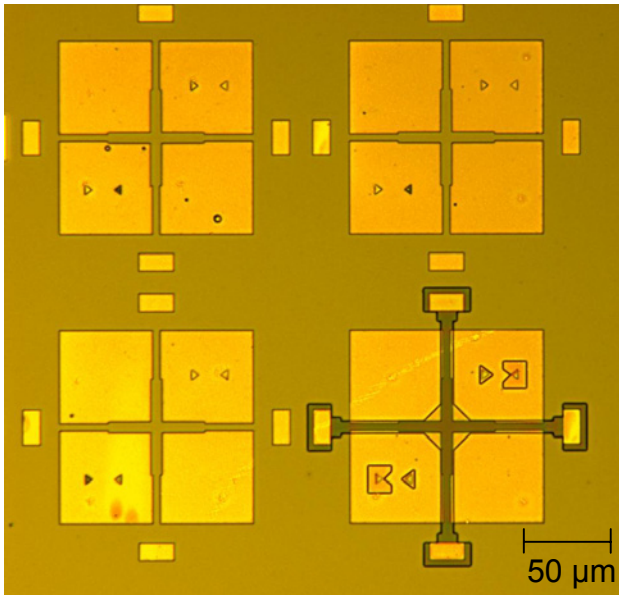


Figure 3.24 Optical micrograph of alignment marks taken during the process

As already discussed in Chapter 3.2.1.3, for the directly contacted emitters, Durimide technique is used. The key processing step in this technique is the ashing of the Durimide. Ashing is the removal of the organic materials like photoresist,

polyimide, etc. using O_2 plasma. Since Durimide is a transparent material, it is difficult to identify with optical microscopes, whether the ashing is sufficient to open the emitter contact.

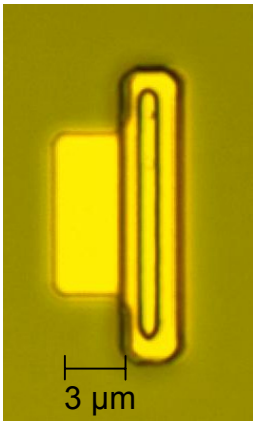


Figure 3.25 Optical micrograph of base-emitter metal covered with Durimide (before any ashing step).

In Figure 3.25, it is not possible to identify whether the emitter is covered or not with Durimide. Therefore, metal stripes, i.e. emitter metals, are deposited and half of the metal stripe is covered with Durimide as shown in figure 3.26.

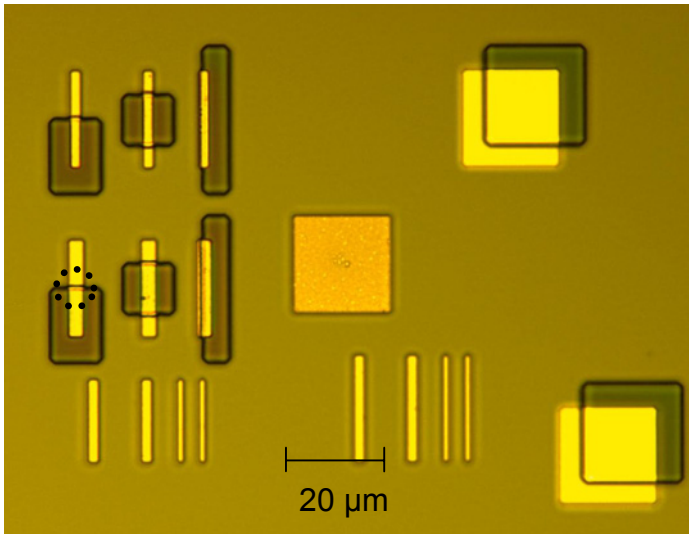


Figure 3.26 Optical micrograph of Durimide control structures taken during the process (before any ashing step)

Even though, Durimide is transparent, by the help of the contrast between metal and Durimide, one can identify that Durimide still covers the metal as shown with the dotted circle in Figure 3.26. By ashing the Durimide, one can easily check the structures with optical microscopy.

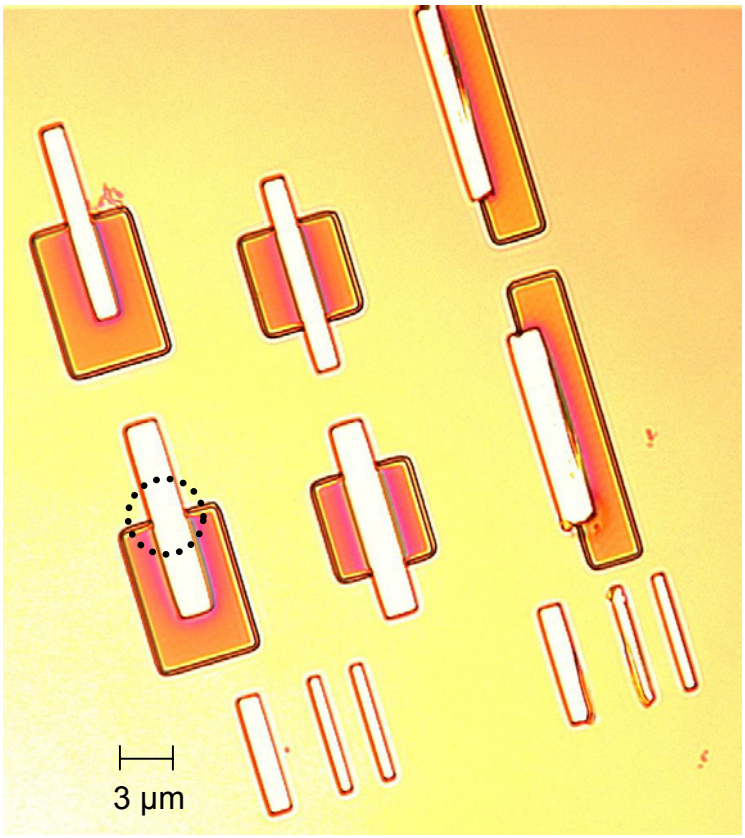


Figure 3.27 Optical Micrograph of Durimide control structures taken during the process (after successful ashing).

In figure 3.27, again with dotted circle, one can identify whether the ashing was sufficient to free the emitter metal from Durimide. By the helps of the structures mentioned above, the stability, reproducibility and reliability of the Durimide ashing process are improved.

3.3 Contact Optimisation

Since the maximum oscillation frequency is a function of the base resistance, the base contact plays an important role for high speed HBTs.

There are two types of contact. These are Ohmic contacts, which shows linear and symmetric current-voltage curve. The other one is Schottky contact, which shows non-linear and asymmetric behaviour.

For the metal semiconductor contacts, there are two mechanisms for the flow of carriers. If the doping level of the semiconductor is low, carriers can go over the barrier by thermal energy, therefore it is called "thermionic emission". For highly doped materials, since the depletion region for the barrier gets narrower, the carriers can penetrate through the barrier by quantum effects. This is called as "Tunnelling". By tunnelling, one can achieve better ohmic contacts. Beside these, there may also be combination of both for mid-doped semiconductors. For ohmic contacts, high doping is preferred, where depletion width can be minimised and as a consequence tunnelling can be achieved. Hence, doping of semiconductor is an important aspect for the contact.

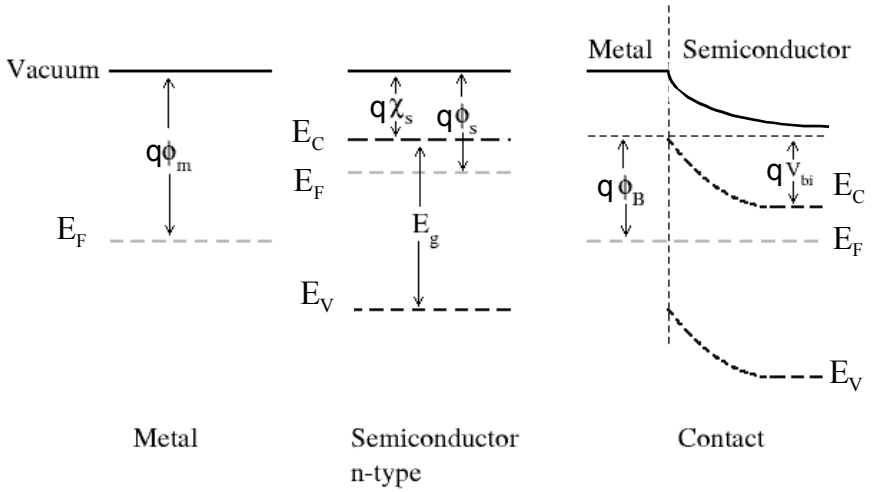


Figure 3.28 Metal n-type semiconductor contacts.

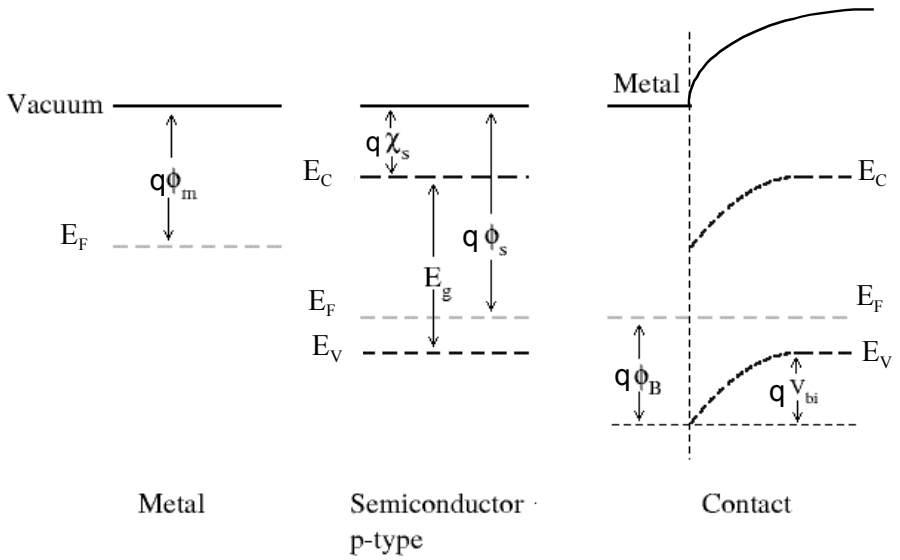


Figure 3.29 Metal p-type semiconductor contacts.

The depletion width can be determined by solving the Poisson's equation.

$$\nabla^2 V = \frac{\rho}{\varepsilon} \qquad \text{equation 3.3}$$

Here, ρ is the net charge density and ε is the dielectric constant. When the equation is integrated;

$$\frac{dV}{dx} = \frac{\rho}{\varepsilon} x + C_o \qquad \text{equation 3.4}$$

Here, considering the depletion region width, W_{dep}, the C_o constant can be written as $C_o = -\frac{\rho}{\varepsilon} W_{dep}$. Then;

$$V(x) = \frac{\rho}{2\varepsilon} x^2 - \frac{\rho W_{dep}}{\varepsilon} x + V_{bi} \qquad \text{equation 3.5}$$

By the help of boundary conditions; and $V(0) = V_{bi}$ and $V(W_{dep}) = 0$ then the depletion region width can be expressed as:

$$W_{dep} = \sqrt{\frac{2\varepsilon V_{bi}}{\rho}} \qquad \text{equation 3.6}$$

where $\rho = q.N_{dopant}$.

As it can be identified form equation 3.6, the depletion thickness is inversely proportional to the semiconductor doping. By doping the semiconductor, one can decrease the depletion width and increase the probability of tunnelling. As a consequence, ohmic contacts are achievable.

The metal system used will also have an important role for the contact behaviour. Alloyed and non-alloyed contacts are two main groups of contact that can be used for semiconductors. According to the application, these types may offer pros and cons.

For highly doped semiconductors where $E_F = E_C$ and $E_F = E_V$ for highly n-type and p-type doping, respectively, the barrier heights can be written as:

$$q\phi_{Bn} = q\phi_m - qX_s \qquad \text{(for n-type)} \qquad \text{equation 3.7}$$

$$q\phi_{Bp} = E_g - q(\phi_m - X_s) \qquad \text{(for p-type)} \qquad \text{equation 3.8}$$

For alloyed contacts, the contact material is deposited and heat treatment is applied. This treatment is performed a machine called Rapid Thermal Annealer (RTA), where the temperature can be increased precisely using high power halogen lamps. The annealing temperature is in the range of 300 – 450 °C. These values are defined by the eutectic formed. Eutectic is the compound having lower melting point than the individual melting point of the elements forming it [14]. By increasing temperature, metal will diffuse into the semiconductor.

On the other hand, considering HBTs, alloyed contacts are not preferable, especially for emitter and base. Even though the emitter is thick enough, any thermal process may result in emitter base to be short-circuited. This is much more critical for the base. Since the base layer is very thin, alloyed contacts can result in a short circuit with the collector. Because of these reasons, for HBT processing, non-alloyed contacts are preferable.

For the evaluation of the contacts transmission line measurements (TLM) are performed. TLM structures are patterned on the emitter cap, base and subcollector layers. These are series of 130x200 μm^2 (L_{pad}xW_{pad}) metal contacts on semiconductor mesa layer with increasing contact distances, d (3, 5, 10, 20, 40 μm).

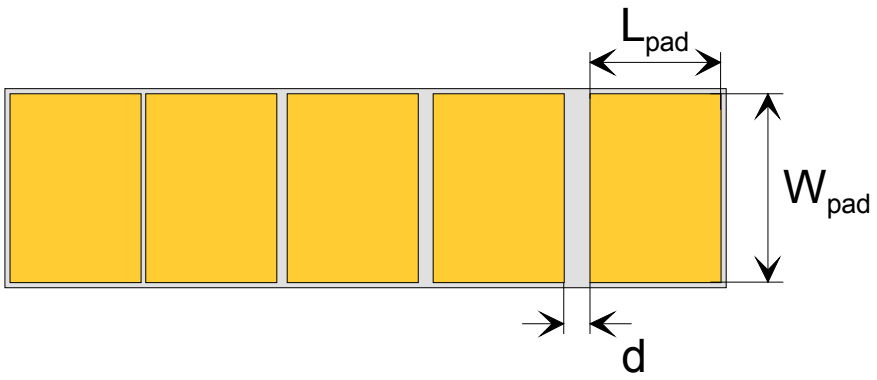


Figure 3.30 Layout for the TLM structures

For the TLM measurements, 4-probe Method is used. It was originally proposed by Wenner in 1916 and here, the probe and metal/probe contact resistance are eliminated [73].

The measurement data are plotted as depicted in Figure 3.31.

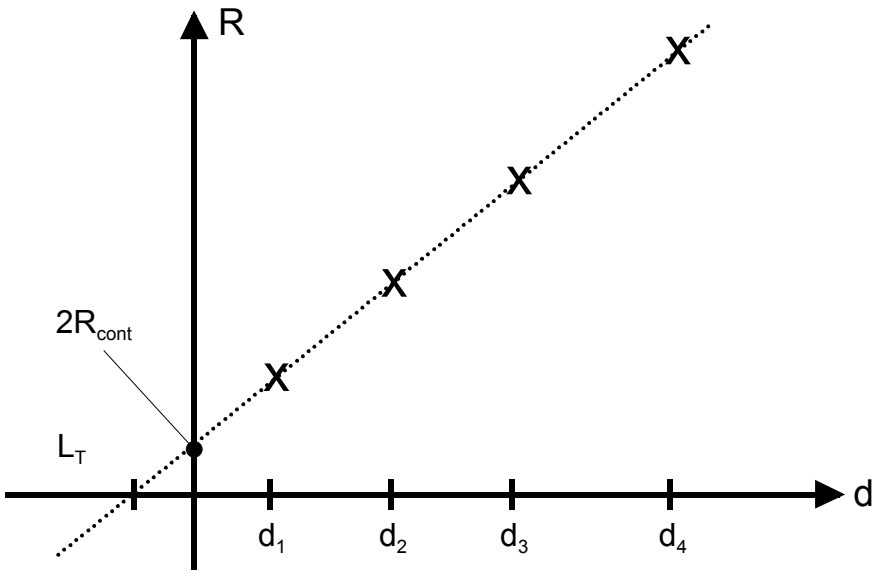


Figure 3.31 Total resistance as a function of contact spacing, d

The evaluation of Figure 3.28 yields to:

$$R_{TOT} = 2R_{cont} + R_{sh} \cdot (\frac{d_i}{W_{pad}}) \qquad \text{equation 3.9}$$

$$S_c = R_{cont} \cdot W_{pad} \cdot L_T \qquad \text{equation 3.10}$$

where R_{cont} is the contact, R_{sh} is the sheet, S_c is the specific contact resistances and d_i is the contact spacing, W_{pad} is the width of the contact and L_T is the transfer length of the contact. The transfer length is defined as the distance over which most of the current transfers from the semiconductor into the metal or from the metal to the semiconductor. It is given by

$$L_T = \sqrt{\frac{R_{cont}}{R_{sh}}} \qquad \text{equation 3.11}$$

By using the information above, tests have been performed to improve the base contact. Prior to this work, Ti/Pt/Au contacts have been preferred as base contact metal. Since holes have larger effective mass than electrons, it is difficult to achieve lower contact resistances on p-type materials. On the other hand, it is well known that in comparison to Ti, Pt offers better band line up on p-type material because of its higher metal work function [74, 75]. The work function of Titanium ($\phi_{M,\,Ti}$) is 4.33 V and for platinum, this value is 5.65 V. Since the energy barrier on p-type material is given as:

$$q\phi_B = E_g + q\phi_S - q\phi_M \qquad \text{equation 3.12}$$

where ϕ_B is the energy barrier, ϕ_S is work function for the semiconductor and ϕ_M is the work function of the contact metal. From the equation, it can be seen that higher metal work function leads to a lower barrier.

3.3.1 Contact optimisation for InGaAs-InP SHBT

Ti/Pt/Au (10/10/80 nm) and Pt/Ti/Pt/Au (2/10/10/80 nm) metal systems are deposited as base contacts on InGaAs base layer with p-type doping density of $3x10^{19}$ cm^{-3} of complete SHBTs, M3231D and M3231A, respectively. Transmission line measurements are performed for both samples. According to the measurements, sheet resistances have found to be 1350 Ohm/sq for both SHBTs. For M3231D, specific contact resistance is measured as $3.2x10^{-6}$ $Ohm{\cdot}cm^2$. For M3231A this value is $4x10^{-7}$

$Ohm \cdot cm^2$. With these results, nearly one order of magnitude improvement is achieved for the base contact resistance and therefore, Pt/Ti/Pt/Au contacts are chosen as standard base contact metal system [76, 77]. Here, the thickness of first Pt layer has been chosen as 2 nm. Increasing this thickness may result in spiking of Pt deep into the layer and result in base-collector to be short-circuited. To prevent short circuits between base and emitter, Au layer is chosen as 80 nm and complete metal system thickness is kept 100 nm, which is 100 nm less than emitter mesa thickness and which is also sufficient to prevent the risk of any short circuits.

On the other hand, for emitter and collector n-type contacts, Ti/Pt/Au metal system is preferred. Here, Titanium (Ti) provides good adhesion on the semiconductor, which improves the stability of the contact. Platinum (Pt) prevents the penetration of gold during any curing step.

3.3.2 Contact optimisation for GaAsSb layers

The same tests have been performed for highly p type doped GaAsSb single layers. The Ti/Pt/Au and Pt/Ti/Pt/Au contacts have been deposited on GaAsSb layers with $4x10^{19}\ cm^{-3}$ p-type doping density. The TLM measurements have shown contact resistances of $2.1x10^{-6}\ Ohm \cdot cm^2$ and $1.9x10^{-7}\ Ohm \cdot cm^2$ for Ti/Pt/Au and Pt/Ti/Pt/Au contacts, respectively [78].

During these tests, it has been observed optically that developer attacks the GaAsSb layer. To investigate the problem, detailed experiments have been performed. A single GaAsSb layer has been used and it is patterned with TLM structures. Atomic Force Microscope (AFM) measurements have been perfromed just after the metallization. Here, 145 nm metal is deposited.

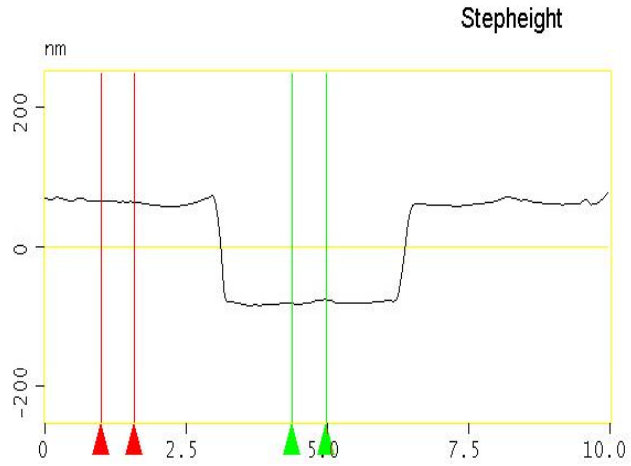


Figure 3.32 AFM for single GaAsSb single layer with TLM structures (just after the metallization).

To remove the oxide layer from the surface, the sample is dipped into the diluted HCl, and AFM measurement is performed again.

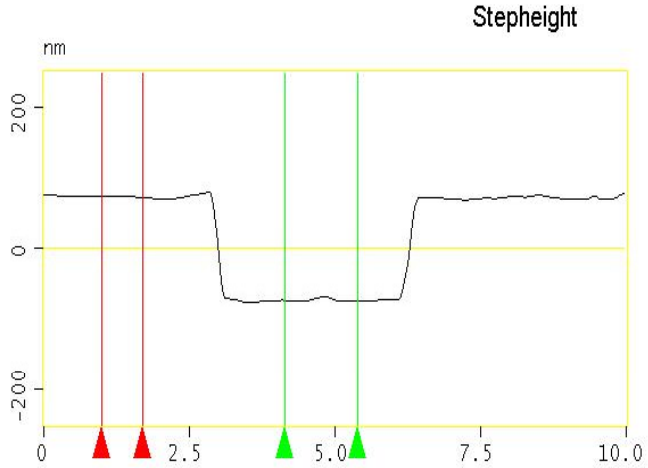


Figure 3.33 AFM measurement for single GaAsSb single layer with TLM structures (just after oxide dip).

Just after the oxide dip, the sample is dipped into the diluted developer (1:1, H_2O:Developer) for 90 seconds.

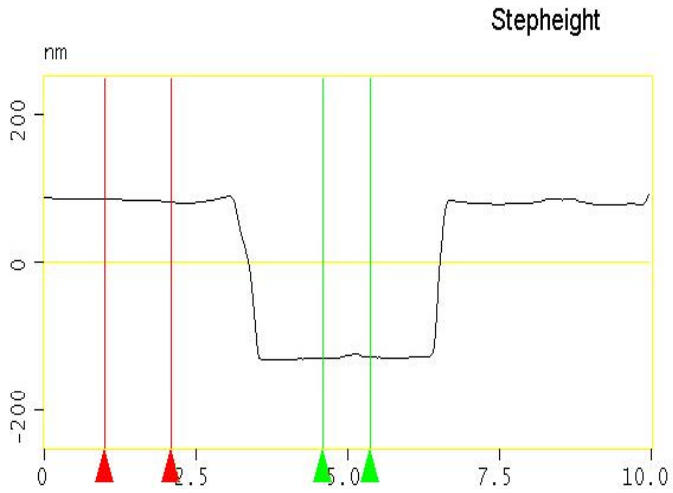


Figure 3.34 AFM measurement for single GaAsSb single layer with TLM structures (after 90 sec.s developer dip).

With this measurement, it is observed that developer etched 65 nm of GaAsSb material in 90 seconds, which corresponds to the etch rate of 0.72 nm/sec. The etching effect of developer seen in GaAsSb layers is not observed for InGaAs layers.

4 HBTs with the Optimised Layout and Processing

In this chapter, the measurement results for the optimised HBTs processed with HBT03 mask overcoming the constrains of HBT97 mask, will be presented. To present the improvement with the design and the processing parameters, GaAsSb DHBTs processed with HBT97 and HBT03 masks will be compared.

The Kirk effect will be also elaborated and experimentally investigated.

The size effects of HBTs, like the influence of width and length on HBT performance will be discussed and these results will be compared with the estimations performed in chapter 3.

4.1 Measurement Results for GaAsSb DHBTs

The GaAsSb/InP DHBTs are also optimised during this work. Before going into the detail about the measurement result, brief information will be given about the epitaxial growth. Especially, because of the instabilities in the growth and the difficulties in achieving reproducible GaAsSb/InP DHBTs, several efforts have been spent for optimising the epitaxial growth. In the early phase, the first successful GaAsSb-DHBT was processed with the HBT97 mask set and the previous processing procedure. The layer structure for this DHBT, M2748, is presented in Table 4.1.

Table 4.1 The layer structure for the GaAsSb DHBT (M2748)

Layer	**Material**	**Doping**	**Thickness**
Emitter cap	n++ InGaAs	$1x10^{19}$	100 nm
Emitter	n InP	$5x10^{17}$	60 nm
Base	p++ GaAsSb	$8x10^{19}$	20 nm
Collector	nid InP	nid	300 nm
subcollector	n++ InGaAs	$1x10^{19}$	300 nm
s.i. InP Substrate			

A 2x10 μm^2 device with HBT97 and previous processing procedure is shown in figure 4.1.

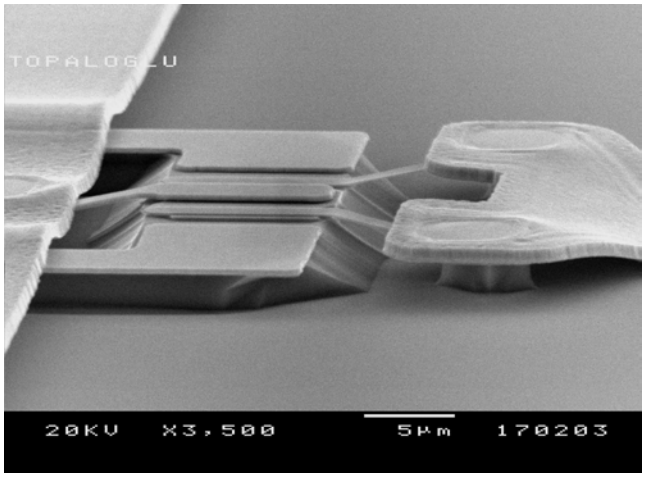


Figure 4.1 A 2x10 μm^2 device processed with previous design and processing (HBT97) on M2748A

The dc measurements for this device have shown a current gain of 40. Here, different from InGaAs/InP SHBTs, the offset voltage is around 0.1 V and the turn-on voltage is about 0.3 V, both very low in comparison to the InP/InGaAs HBTs. The Gummel Plot has shown ideality factors of 1.22 and 1.09 for n_b and n_c, respectively.

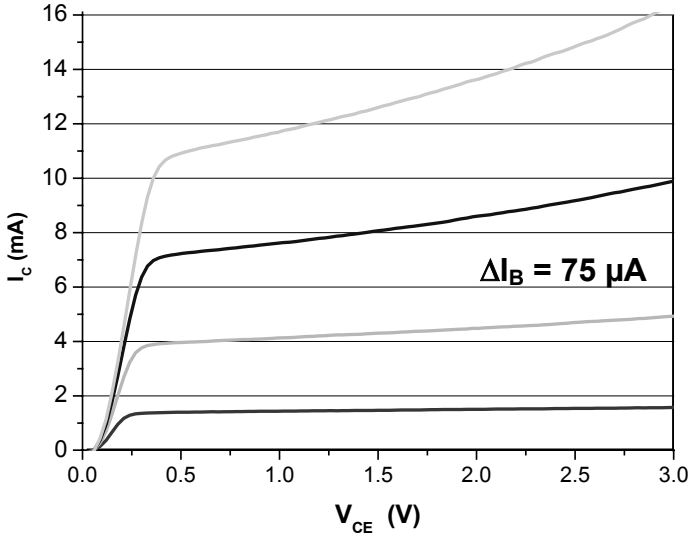


Figure 4.2 The common emitter output characteristic for 2x10 μm^2 device processed with early design and processing (HBT97) on M2748A

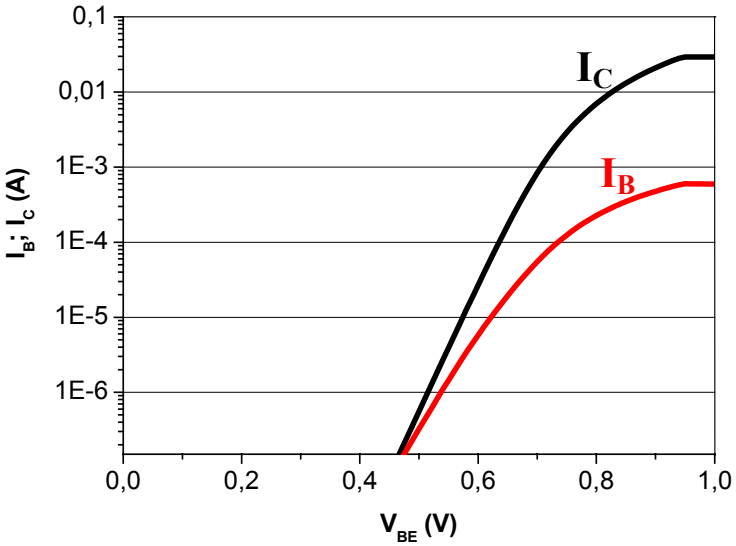


Figure 4.3 The Gummel Plot for 2x10 μm² device processed with early design and processing (HBT97) on M2748A

This device has shown maximum oscillation frequency of 55 GHz and the cut-off frequency of 90 GHz [79].

In addition to these results, regarding the dc properties the TLM structures for base layer have shown non-ohmic characteristic as shown in figure 4.4. This is attributed to an interlayer occurring during the base-emitter junction growth. Even though InP emitter can be selectively etched over GaAsSb layer, the base metal is deposited not on base layer but on this interlayer yielding non-ohmic behaviour. This was one difficulty in GaAsSb/InP DHBT growth. For further experiments, new growth runs have been performed but layers with poor crystalline quality were achieved, or even when they were crystalline layers, they suffered from offering only low dc current gain.

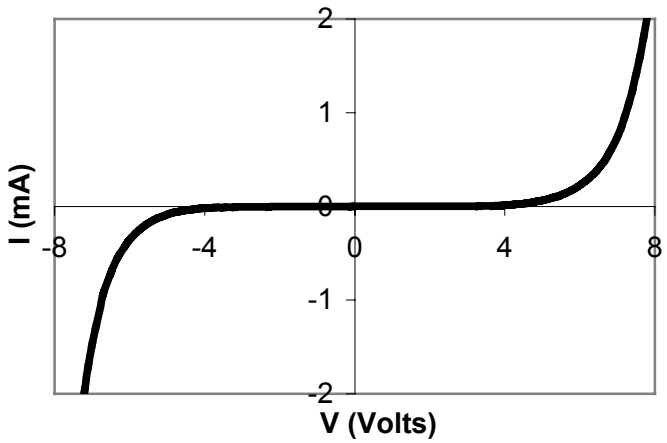


Figure 4.4 The IV measurements on Base TLM (M2748A)

There was evidence about the origin of the degradation. This was about the InGaAs subcollector layer underneath the base. To investigate the problem, test samples have been grown: Sample A is the test structure having InP as collector and InGaAs as subcollector underneath the GaAsSb base layer, while the InGaAs subcollector layers is missing in Sample B. The X-ray diffraction curves are depicted in Figure 4.5. Even though the base layers have the same doping density and thickness for both samples, one can see large difference in the intensity and shape of the curves.

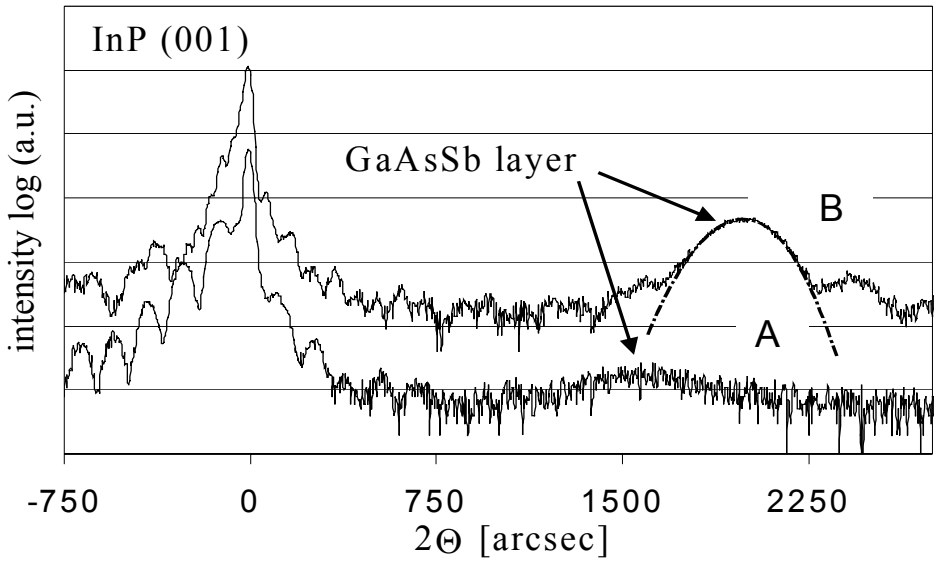


Figure 4.5 X-Ray diffraction curves for sample A and B

The intended thickness of the base layer was around 40 nm and this has been calculated from the curves for sample B. We assume that the degradation in the intensity is because of the Indium carry over into the GaAsSb layer degrading the crystal quality. Since InAs in the InGaAs material has weaker bond-strength compared to the InP, this is much more critical for Sample A.

As a result, the n^{++} InGaAs as subcollector is exchanged it with n^{++} InP. Two complete HBT layer structures have been grown with n^{++} InP subcollector. Here, the only difference for both samples is the doping of the base. The base layers have $8x10^{19}$ cm^{-3} and $6x10^{19}$ cm^{-3} doping density for M3273 and M3354, respectively. The X-Ray results as well as the mirror like surfaces of both samples indicate good crystal quality.

Both curves show clearly the presence of the GaAsSb layers beside the InP substrate peak. The layer thicknesses for GaAsSb base layers are calculated to be 40 nm. From the simulations, the Sb concentration of M3273 is determined as 42 %, while this value is 38 % for M3354. This shift is due to the different doping levels , affecting the III/V ratios because of the etching effect of Ga by CBr_4 [80].

M3354 is processed with the HBT03 and the optimised processing parameters. Different from M2748, base transmission lines have shown ohmic behaviour. 1260 Ohm/sq sheet resistance and $7x10^{-6}$ Ohm·cm^2 contact resistance have been measured.

The common emitter output characteristic and the Gummel Plot belonging to a 1x15 μm^2 device is shown in figure 4.6 and 4.7, respectively. As it is extracted from figure 4.6, the dc current gain is 35, the offset voltage is 0.25 V and the turn-on voltage is 0.5 V. The Gummel Plot measurements for this device has shown ideality factors of 1.38 and 1.04 for n_B and n_C, respectively.

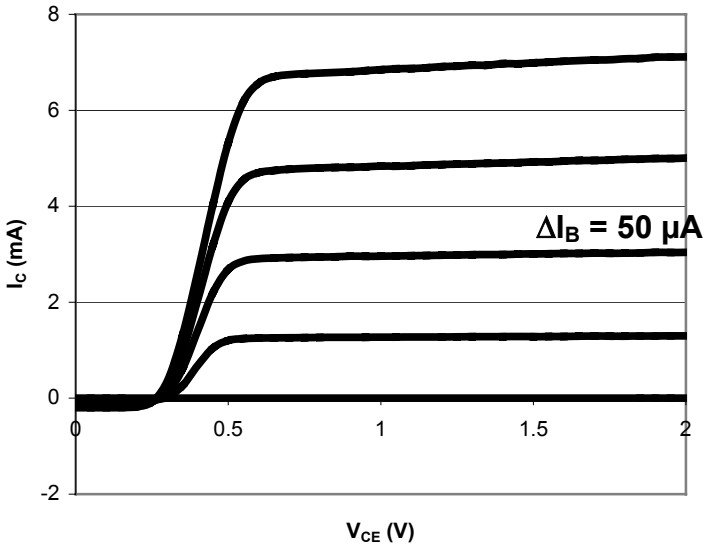


Figure 4.6 The common emitter output characteristic of 1x15 μm^2 std 90° device on M3354

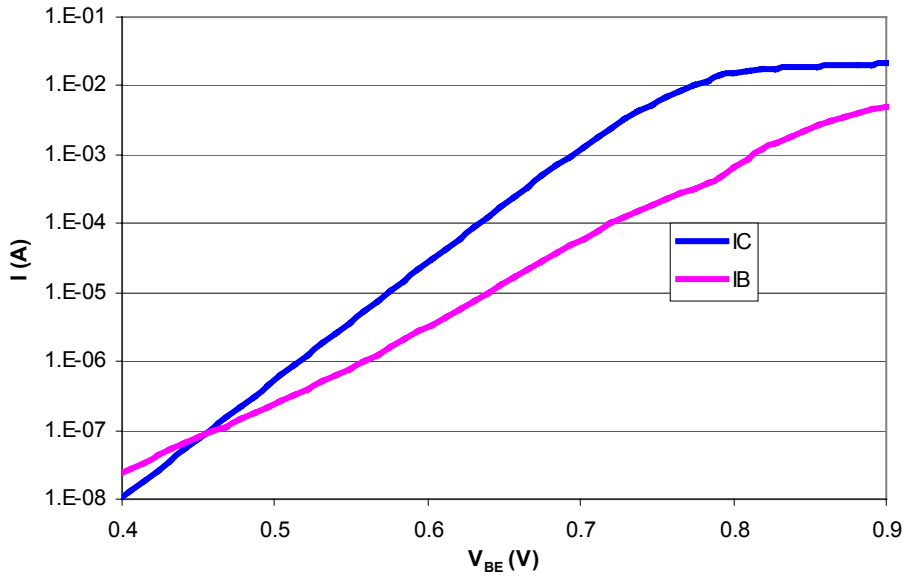


Figure 4.7 The Gummel Plot for 1x15 µm² std 90° device on M3354

RF measurements are also performed on this device. In addition to the 1x15 µm² device, in order to compare the results of new and old design for GaAsSb-DHBTs, a 2x10 µm² (which was the smallest reliable device on the early mask (HBT97)) device is also measured. The results for 1x15 µm² device on M3354A and the comparison of 2x10 µm² devices on M3354A and M2748A are shown in Figure 4.8 and Figure 4.9, respectively.

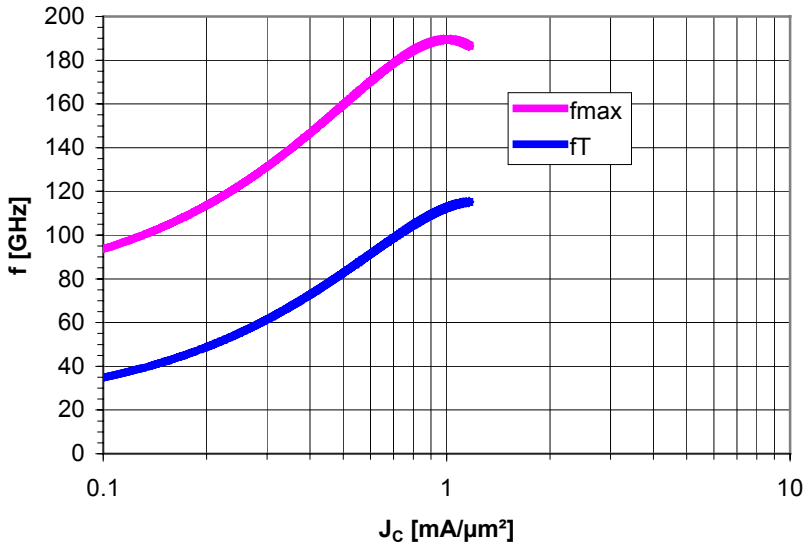


Figure 4.8 RF performance of a 1x15 µm² std 90° device on M3354A

For 1x15 µm^2 device on sample M3354A, 190 GHz of maximum oscillation frequency and 115 GHz of cut-off frequency are achieved at about 0.9 mA/µm^2.

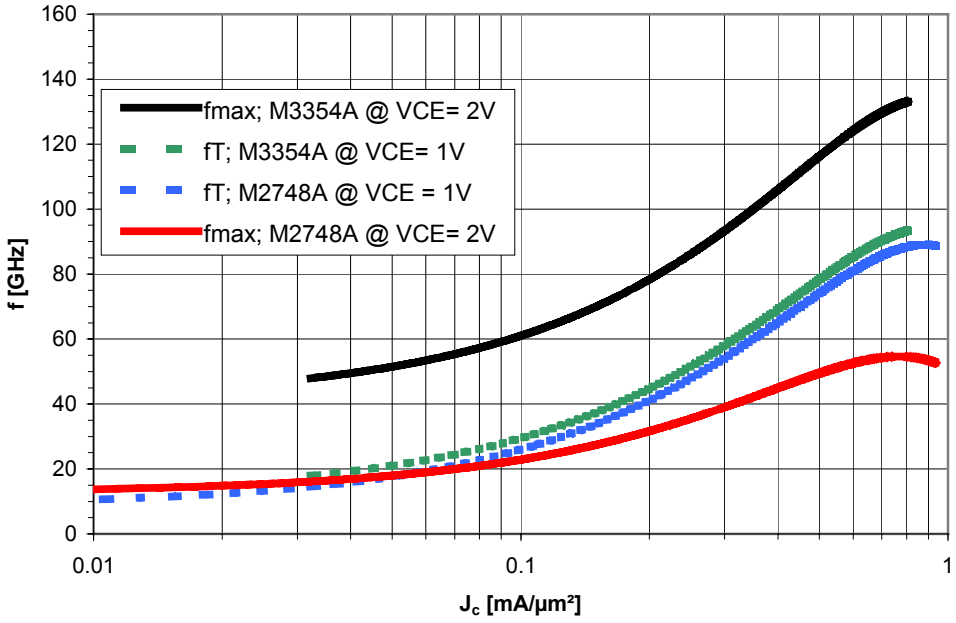


Figure 4.9 RF performance comparison of 2x10 µm^2 devices on M3354A and M2748A

The comparison of GaAsSb DHBT with HBT97 and the latter one with HBT03 have also proven that for the optimised design and processing, the maximum oscillation frequency is improved for GaAsSb DHBTs. Since with the early design and processing the smallest device is 2x10 µm^2, the same dimension has been chosen with the new design and processing. It has been observed that since the layer structure is similar, the cut-off frequency stays the same at 95 GHz and the maximum oscillation frequency has shown 80 GHz improvement and reached to 135 GHz at 0.8 mA/µm^2.

4.2 Improvement of Maximum Current Density

The Kirk effect is already elaborated in chapter 2.3. In this subchapter, this effect will be experimentally investigated for DHBTs and SHBTs.

4.2.1 Improvement of Current Density for DHBTs

HBTs have the potential to drive high currents which are also required in high speed circuit design. At high current levels, various effects may limit the performance

of the device. One of those effects, the Kirk Effect is already described in Chapter 2.3, results in degraded RF performance. This effect causes extension of base width when the current density exceeds the doping density in the collector. In order to study this effect experimentally, three DHBTs with the same layer structure but different collector doping densities are prepared. For this purpose, DHBTs, M3191, M3190 and M3181 with non-intentionally doped (nid), $5x10^{16}$ cm^{-3} and $5x10^{17}$ cm^{-3} collector doping densities, respectively, are grown. The complete layer structures are shown in Appendix F.

These samples are processed in parallel, to eliminate any deviation that may occur by environmental effects during processing. Like for SHBTs, device fabrication is carried out by conventional wet chemical etching based on phosphoric acid for InGaAs and InGaAsP layers, and hydrochloric acid for InP layers. The Ti/Pt/Au metal system is used for emitter and collector. The self-aligned base metallization is deposited as Pt/Ti/Pt/Au.

By using equation 2.14 and 2.15. the Kirk current densities of 0.8 $mA/\mu m^2$, 2 $mA/\mu m^2$ and 4 $mA/\mu m^2$ are calculated for M3191, M3190 and M3181, respectively. The doping density for non intentionally doped InP collector is taken as $1x10^{16}$ cm^{-3} for the calculations.

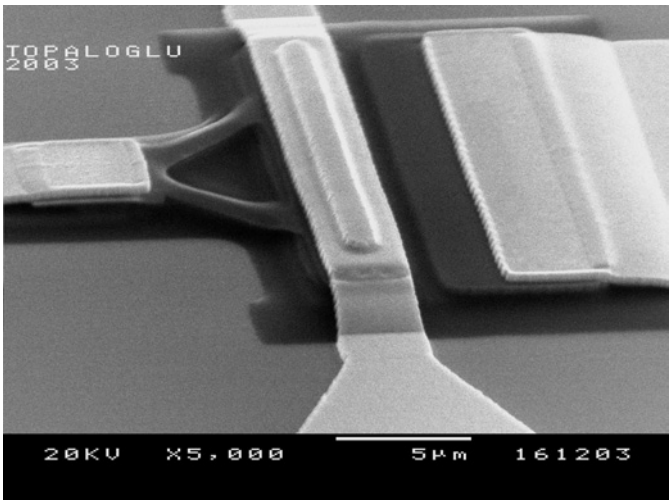


Figure 4.10 The SEM micrograph of a 2x10 μm^2 device used for the determination of the Kirk effect

The common emitter output characteristics are measured for the three samples, as shown in figure 4.11. As expected, the dc current gain is not affected by collector doping densities. For all samples, the dc current gain (B) is around 70 at V_{CE}= 1.5 V and I_B= 200 μA. It has been observed that, by increasing the collector doping density, the open-base breakdown voltage BV_{CEO} decreases, as expected.

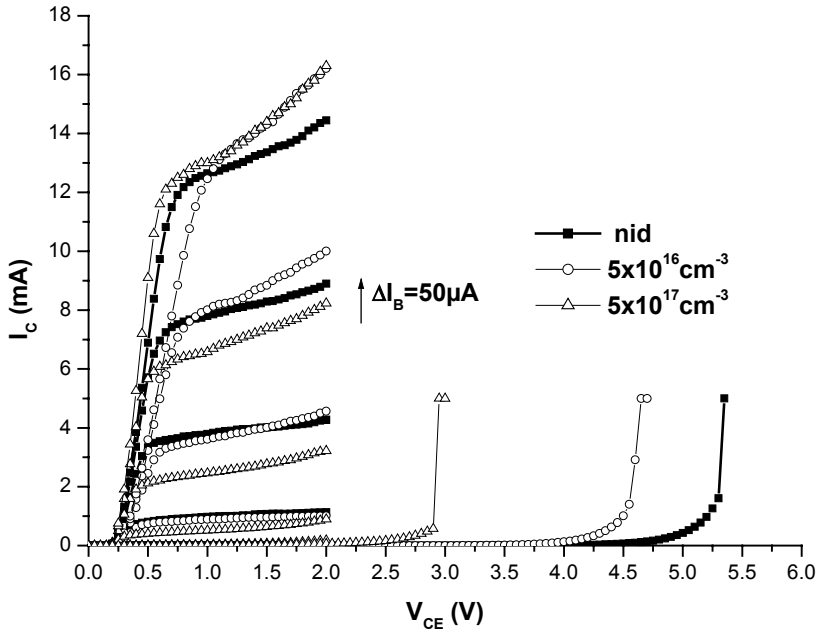


Figure 4.11 The common emitter output characteristics for different collector doping densities.

In addition to the dc measurements, RF measurements are also performed. As depicted in Figure 4.12, by increasing collector doping densities, the maximum oscillation frequency f_{max}, and the transition frequency f_T increases simultaneously.

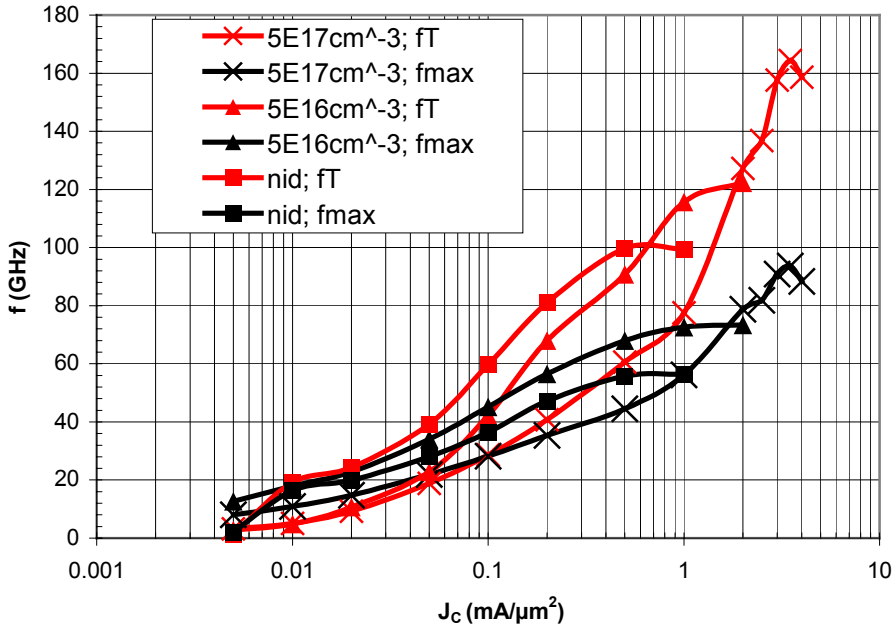


Figure 4.12 RF performance vs. current density for various collector doping densities.

Here, the maximum current densities for sample M3191, M3190 and M3181 are measured to be 0.5 mA/μm^2, 1.5 mA/μm^2 and 3.5 mA/μm^2, respectively. There is a good agreement between the calculated Kirk current densities and measured maximum current densities. The maximum current densities are defined as the current densities providing the highest RF performance.

Table 4.2 Influence of collector doping on HBT's RF performance and the breakdown voltage, BV_{CEO}.

Sample	**Collector Doping Density(n_c) (cm^{-3})**	**$J_{C,\,max,\,measured}$ (mA/μm^2)**	**$J_{Kirk,\,calculated}$ (mA/μm^2)**	**f_T (GHz)**	**f_{max} (GHz)**	**BV_{CEO} (V)**
M3191B1	nid	0.5	0.8	100	60	5.5
M3190A1	$5x10^{16}$	1.5	2	120	75	4.5
M3181C1	$5x10^{17}$	3.5	4	165	95	3.0

Finally, it has been proven that, by doping the collector, one can improve the maximum current density and as a result the RF performance. On the other hand, there is a trade off between the breakdown voltage and the RF performance. Especially for the SHBTs the degradation in the breakdown voltage may be much more critical.

4.2.2 Improvement of Current Density for SHBTs

As presented in chapter 4.2.1 in detail, doping the collector has improved the RF performance of DHBT. To investigate the influence of the Kirk Effect on SHBTs, two SHBT layer structures have been grown and processed in the same manner. The doping densities of M3312 and M3231 are nid and $1x10^{17}$ cm^{-3}, respectively.

The common emitter characteristic belonging to an 1x15 μm^2 emitter area device on M3312D is shown in Figure 4.13. The dc current gain (B) of 50 is achieved. From figure 4.13, an offset voltage of ($V_{CE,\ offset}$) 0.2 V and turn-on voltage of 0.4 V can be extracted. The breakdown voltage, BV_{Ceo}, is around 5.5 V.

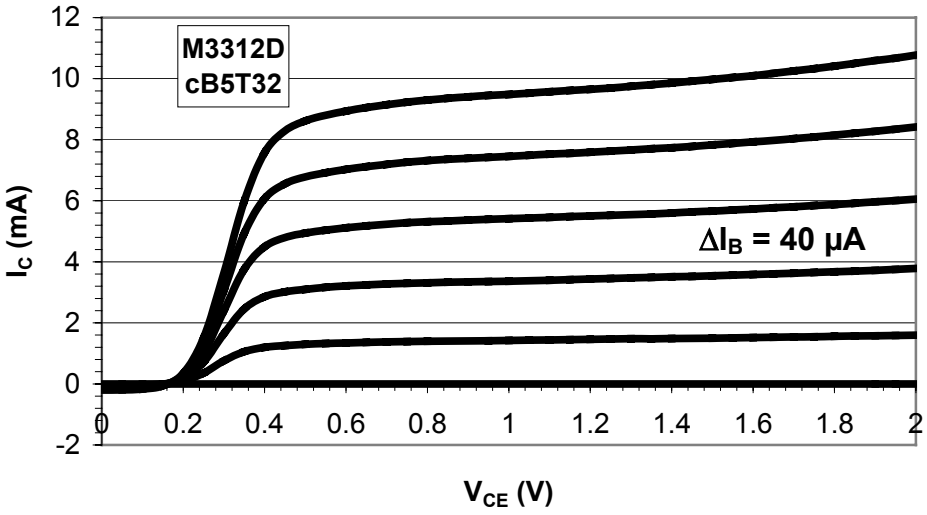


Figure 4.13 Common Emitter Output Characteristic of 1x15 μm^2 device (N_C = nid))

For this device, RF measurements are also performed as shown in Figure 4.14.

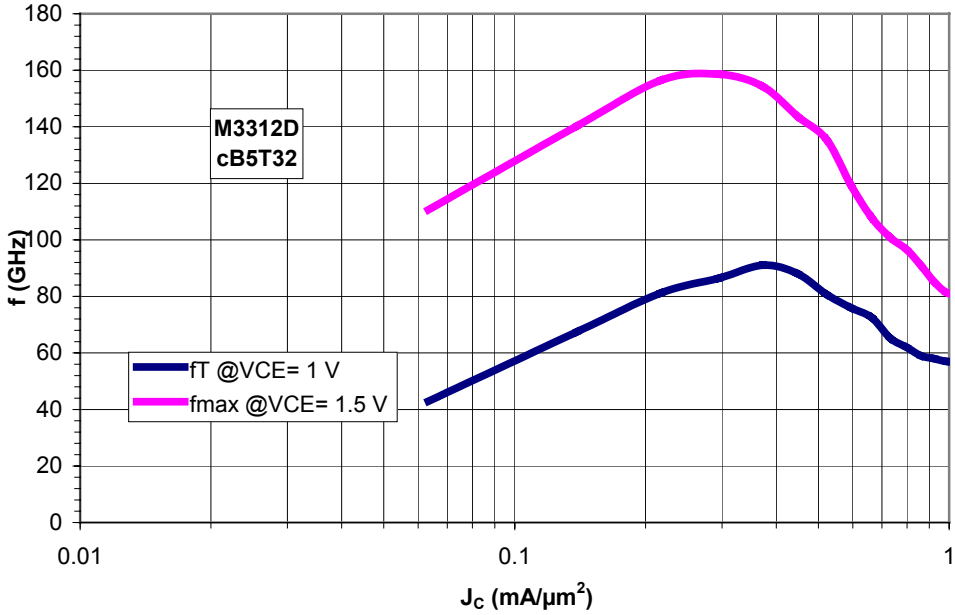


Figure 4.14 RF performance of self aligned 1x15 µm^2 device (N_C= nid)

As shown in Figure 4.14, a maximum oscillation frequency of 160 GHz and a cut-off frequency of 90 GHz are achieved at maximum current density of 0.4 mA/µm^2.

M3231 with 1x10^{17} cm^{-3} collector doping density is also processed. For the same device dimension (1x15 µm^2), the common emitter output characteristic in Figure 4.15 is achieved.

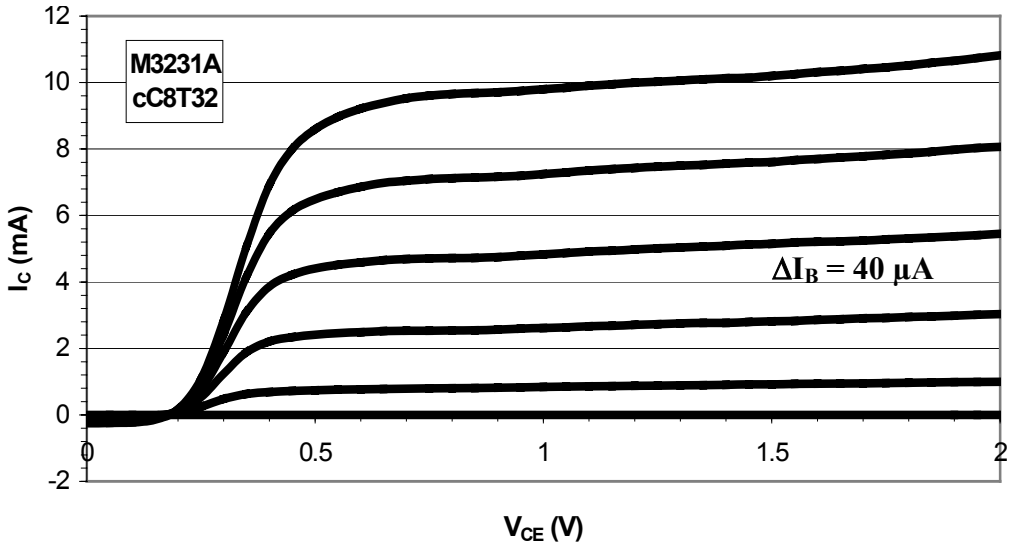


Figure 4.15. The common Output Characteristic of 1x15 µm^2 device (M3231A)

From figure 4.15, a dc current gain of 50, an offset voltage of 0.2 V and a turn-on voltage around 0.4 are observed. The breakdown voltage is found out to be 4.5 V.

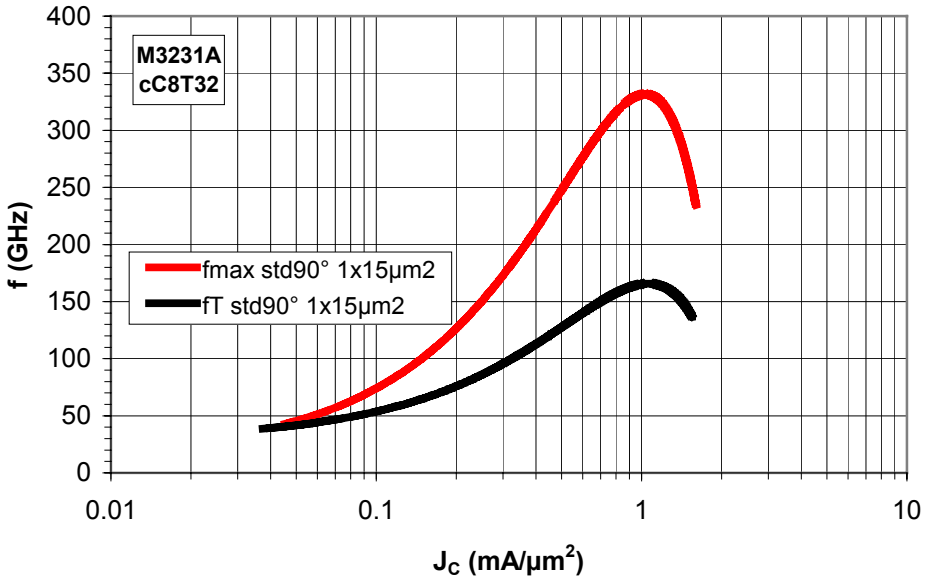


Figure 4.16. RF performance of self aligned 1x15 µm² device at V_{CE}= 1.5 V and J_C= 1.2 mA/µm².

As shown in figure 4.16, one of the best device on this sample has shown a maximum oscillation frequency of 330 GHz and a cut-off frequency of 170 GHz at 1.2 mA/µm². In comparison to M3312D, the maximum current density is tripled. Moreover the cut-off and the maximum oscillation frequencies are doubled.

4.3 Emitter Size Effects on HBT's Performance

On the mask set developed during this work (HBT03), there are different HBT layouts as discussed briefly in chapter 3.2.1.4. Here, the influence of the layouts and processing will be elaborated.

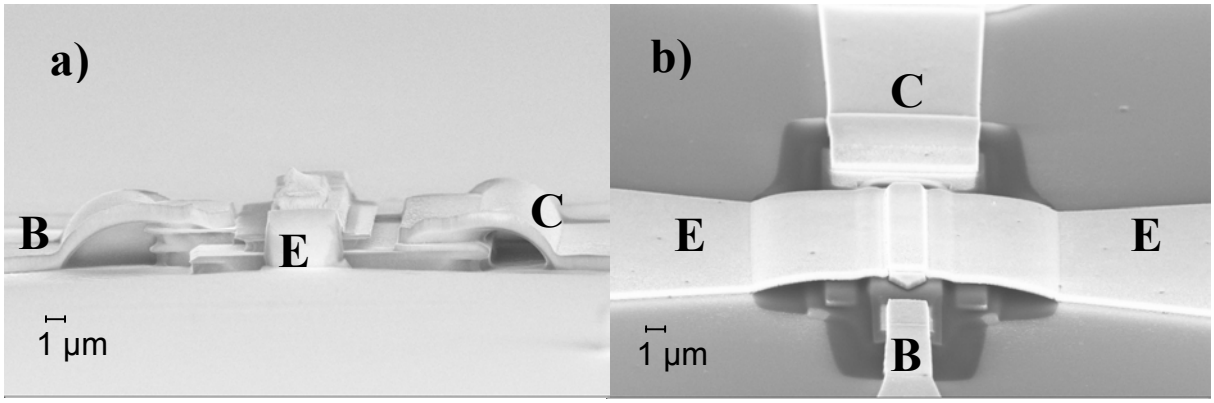


Figure 4.17 SEM micrographs of self-aligned a) standard (std) b) Standard 90° (std 90°) 2x10 µm^2 devices processed with HBT03 mask where emitters are oriented perpendicular to the major flat

For all of these layouts, the base is 1µm extending to both side of emitter.

Table 4.3 Different emitter areas on the new mask set (nsa: non self aligned; sa: self aligned)

T12	**T22**	**T32**	**T42**	**T52**	**T62**	**T72**
sa 1x5 µm^2	sa 1x10 µm^2	sa 1x15 µm^2	sa 2x5 µm^2	sa 2x10 µm^2	sa 2x15 µm^2	sa 3x10 µm^2
nsa 1x5 µm^2	nsa 1x10 µm^2	nsa 1x15 µm^2	nsa 2x5 µm^2	nsa 2x10 µm^2	nsa 2x15 µm^2	nsa 3x10 µm^2
T11	**T21**	**T31**	**T41**	**T51**	**T61**	**T71**

For the evaluation of the new layouts and processing, considering the collector underetching and Kirk effect, the new SHBT layer structure grown with 600 nm thick collector and collector doping density of 1x10^{17} cm^{-3} are used. The sample is called M3231. The detailed layer structure is placed in the appendix F. To check the quality of the crystal, X-Ray measurements have been performed. X-Ray result has shown that all layers are lattice matched to the InP substrate [41, 81].

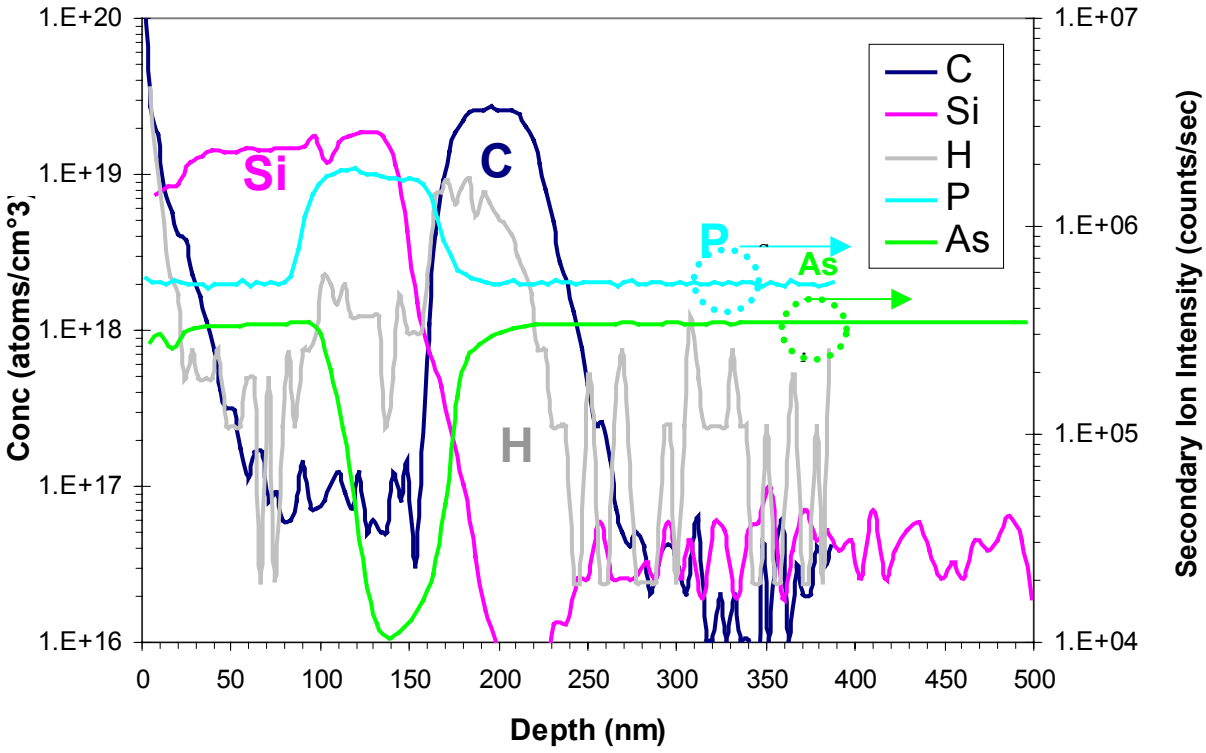


Figure 4.18 SIMS profile of M3231 SHBT

By the cooperation with Sony Corporation Semiconductor Development Technology Group, SIMS (Secondary Ion Mass Spectroscopy) measurements are performed. SIMS is technique for the analysis of impurities in solids. This technique relies on removal of material from a solid by sputtering and on analysis of the ionised species. Only the ionised atoms can be analysed by passing them through an energy filter and a mass spectrometer. Here, the doping density plot is achieved by monitoring the secondary ion signal of a given element as a function of time. The time axis can be converted to a depth axis by assuming constant sputtering rate, but here material composition is different for different layers and therefore sputtering rate is not constant [73]. In order to identify the depth, as shown in Figure 4.18, As and P content are also monitored. SIMS measurement has shown Carbon (C) concentration of $3x10^{19}cm^{-3}$. The Hall measurement performed for the base layer of this sample has shown $2.8x10^{19}$ cm^{-3} p-type doping density. There is more than 90 % of carbon activation for p-type doping. The details on carbon doping of InGaAs can be found in [82].

The TLM measurements are also performed for this sample and they have shown sheet resistance of 1350 Ohm/sq and specific contact resistance of $4.7x10^{-7}Ohm{\cdot}cm^2$.

M3231A is processed with the optimised optical mask set and processing parameters. The complete protocol is placed in the Appendix G. Solely wet chemical etching is used. In comparison to the M2817D (with HBT97 mask and previous processing procedure), here, emitters are oriented 90° to the major flat, and they have directly contacted emitters. Dummy pads and µbridges are eliminated. For the etching of emitter (InP), 1:1; $HCl:H_2O$ diluted etchant is used to minimize the underetching of the emitter. As base metal contact, the Pt/Ti/Pt/Au metal system is used.

The detailed investigations are performed for devices: the emitter width is kept constant (W_E= 1 µm) and the emitter length (L_E) has been varied as 5, 10 and 15 µm.

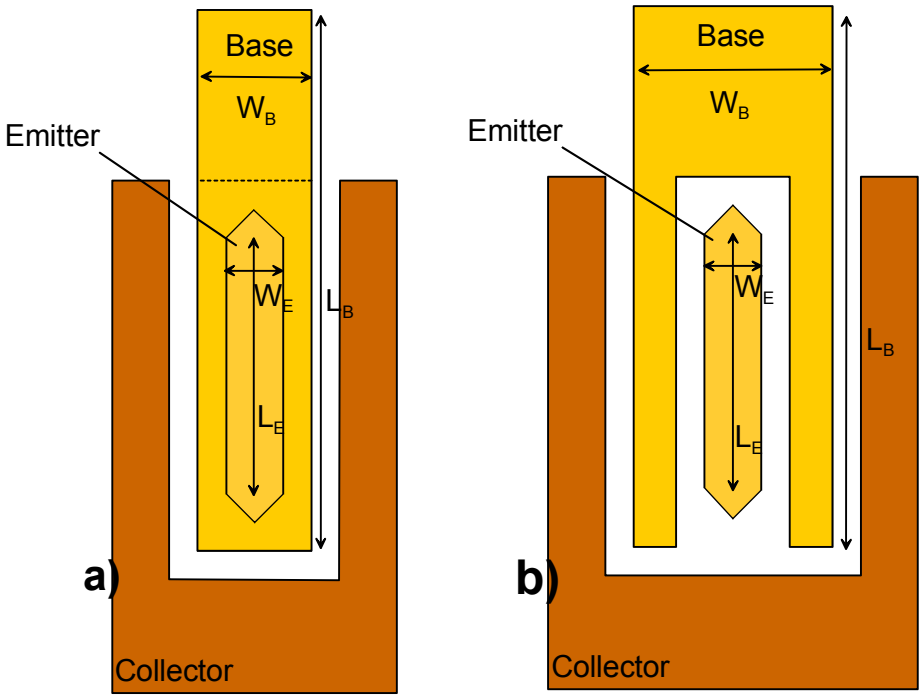


Figure 4.19. The HBT layout on HBT03 mask set with the emitter and base dimensions. a) HBT layout with self-aligned (sa) base contact providing less base resistance and better RF performance. b) HBT layout with nonself–aligned (nsa) base contact

As already discussed in chapter 2.1.3 and expressed in equations 2.11 and 2.12, not only the emitter dimensions but also the base dimensions are key parameters affecting the parasitic capacitances and resistances. With this manner, the influence of the length on transistor performance is tested and the extracted base-collector capacitance and base resistances are tabulated in table 4.4. Here, the parasitic

components are extracted for the maximum RF performance at V_{CE}= 1.5 V and J_C= 1.2 mA/μm^2. The $R_{bb}xC_{bc}$ product is defined as the general time constant [83] and is an important parameter for determining the maximum oscillation frequency as depicted in equation 2.10.

Table 4.4 Extracted intrinsic parameters for various emitter lengths when the emitter width is kept as 1 μm.

$A_{Emitter}$ (W_ExL_E)	A_{Base} (W_BxL_B)	R_{je}	Cjc	C_{fb}	C_{bc}	R_{bb}	$R_{bb}xC_{bc}$
1x5 μm^2	3x13 μm^2	11 Ohm	0.12 fF	8.10 fF	8.22 fF	95 Ohm	912.4 fs
1x10 μm^2	3x18 μm^2	4.5 Ohm	0.22 fF	10.80 fF	11.02 fF	45 Ohm	495.9 fs
1x15 μm^2	3x23 μm^2	3 Ohm	0.39 fF	12.65 fF	13.04 fF	31 Ohm	415.4 fs

From the results summarised in table 4.4, when the emitter length is doubled, the base collector area has increased by 35 % and this resulted in a 25 % increase in the base-collector capacitance. At the same time, again by doubling the emitter length, a 50 % decrease is achieved for base resistance R_{bb}. In total, the $R_{bb}xC_{bc}$ product is nearly halved, which results in a 35 % improvement in f_{max}. The calculated base resistance and its components are shown in table 4.5.

Table 4.5 The calculated base resistance and its components for HBTs with various emitter lengths when the width is kept 1 μm.

$A_{Emitter}$ (W_ExL_E)	$R_{b,\,cont}$	$R_{b,\,spread}$	R_{gap}	$R_{bb} = R_{b.\,cont} + R_{b,\,spread} + R_{gap}$
1x5 μm^2	24.90 Ohm	25.85 Ohm	38.75 Ohm	89.50 Ohm
1x10 μm^2	12.45 Ohm	12.95 Ohm	19.38 Ohm	44.80 Ohm
1x15 μm^2	8.30 Ohm	8.65 Ohm	12.95 Ohm	29.90 Ohm

The calculated base resistance values (R_{bb}) show a good agreement with the extracted parameters.

In addition to the extracted intrinsic components from s-parameter, the maximum oscillation frequency (f_{max}) and the cut-off frequency (f_T) are also determined and they are depicted in figure 4.20 and 4.21, respectively.

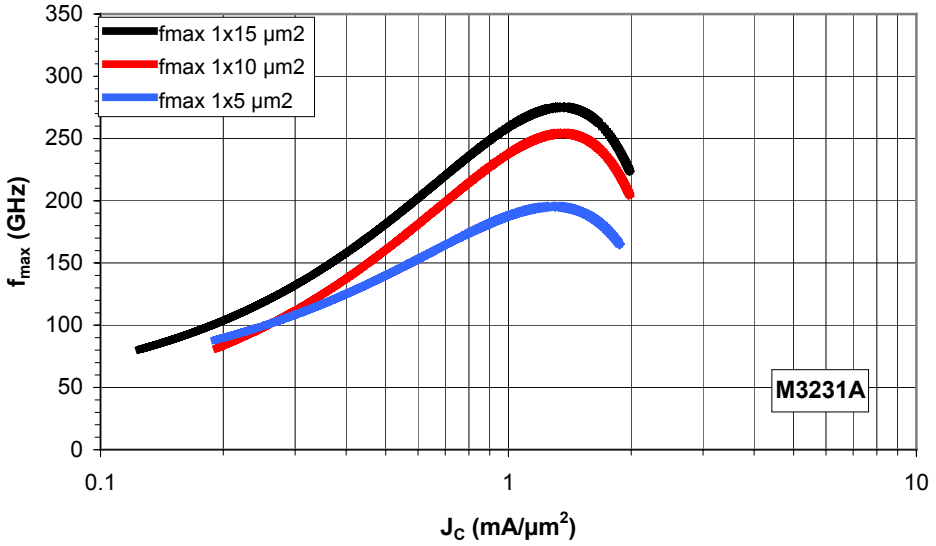


Figure 4.20 The measured maximum oscillation frequency of HBT's with various lengths at V_{CE}= 1.5 V (W_E= 1 µm)

From figure 4.20, maximum oscillation frequencies of 195 GHz and 255 GHz are achieved for 1x5 µm^2 and 1x10 µm^2 devices respectively. Here, by doubling the emitter length, a 30 % improvement in maximum oscillation frequency is observed. This result has good agreement with the extracted parameters. Not only from table 4.4 but also from figure 4.20, it is obvious that 1x15 µm^2 device has shown the highest maximum oscillation frequency with 280 GHz.

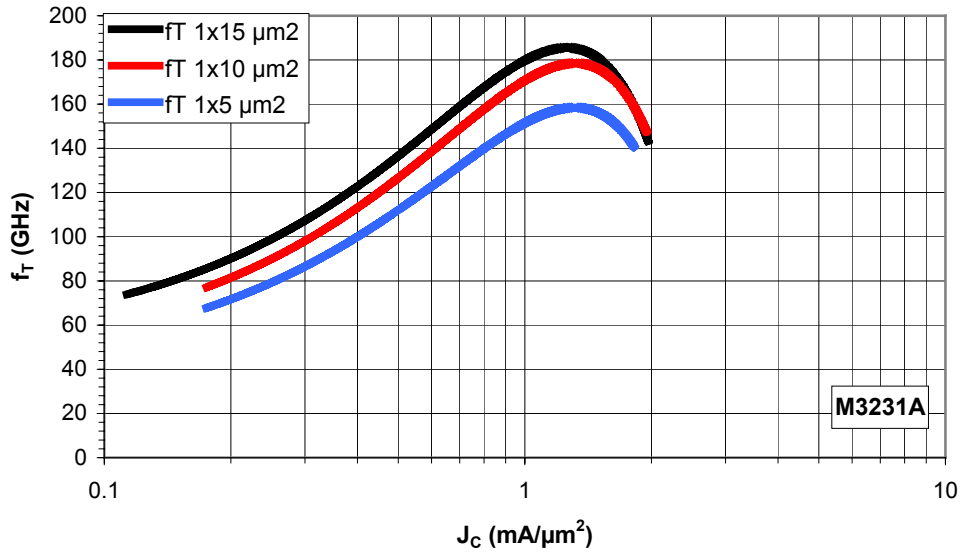


Figure 4.21 The measured cut-off frequencies of HBT's with various lengths at V_{CE} = 1 V (W_E= 1 µm)

The influence of the emitter length on the cut-off frequency is depicted in Figure 4.21. The slight deviation mainly comes from the deviation in the emitter junction resistance (R_{je}). The smaller emitter area will result in higher emitter junction resistance, and this will lead to lower cut-off frequency, as given with the equation 2.9. The emitter junction resistance is inversely proportional to the emitter area and is independent from the base contact dimensions

As a second group of experiment, emitter length (L_E) is kept constant at 10 µm. Even though 15 µm long layout shows the best performance, as depicted in table 5.3, there are more 10 µm long devices on the mask. Therefore 10 µm long layout has been chosen to test the influence of the emitter width. Like the experiments performed for the influence of the emitter length, the same procedure is applied for the emitter width influence tests on HBTs RF performance. The extracted intrinsic components from the s-parameters are depicted in table 4.6.

Table 4.6 Extracted intrinsic parameters for various emitter width when the emitter length is kept at 10 µm.

$A_{Emitter}$ (W_ExL_E)	A_{Base} (W_BxL_B)	R_{je}	Cjc	C_{fb}	C_{bc}	R_{bb}	R_{bb}xC_{bc}
1x10 µm^2	3x18 µm^2	4.5 Ohm	0.22 fF	10.80 fF	11.02 fF	45 Ohm	495.9 fs
2x10 µm^2	4x19 µm^2	2 Ohm	0.35 fF	14.34 fF	14.69 fF	52 Ohm	763.8 fs
3x10 µm^2	5x20 µm^2	1.5 Ohm	0.76 fF	19 fF	19.76 fF	62 Ohm	1225.1 fs

From the results summarised in table 4.6, when the emitter width is doubled, the base-collector area has increased by 40 % and this resulted in a 35 % increase in the base-collector capacitance. At the same time, again by doubling the emitter width, a 20 % increase is achieved for base resistance, R_{bb}. This increase in the base resistance is because of the increase in the spreading resistance underneath the emitter as depicted in equation 2.12. In total, R_{bb}xC_{bc} product has increased 50 %, which will result in approximately 25 % decrease in f_{max}.

Table 4.7 The calculated base resistances and its components for HBTs with various emitter widths when the length is kept at 10 µm.

$A_{Emitter}$ (W_ExL_E)	$R_{b,\,cont}$ (Ohm)	$R_{b,\,spread}$ (Ohm)	R_{gap} (Ohm)	R_{bb} (Ohm)
1x10 µm^2	12.45	12.95	19.38	44.80
2x10 µm^2	12.45	24.85	19.38	56.60
3x10 µm^2	12.45	36.75	19.38	68.50

By these calculations, it has been found out that spreading resistance is increasing linearly by wider emitters, while the $R_{B,\,cont}$ and R_{gap} stay constant.

In addition to the extracted intrinsic components from s-parameter, the maximum oscillation frequency (f_{max}) and the cut-off frequency (f_T) are also determined and they are depicted in figure 4.22 and 4.23, respectively.

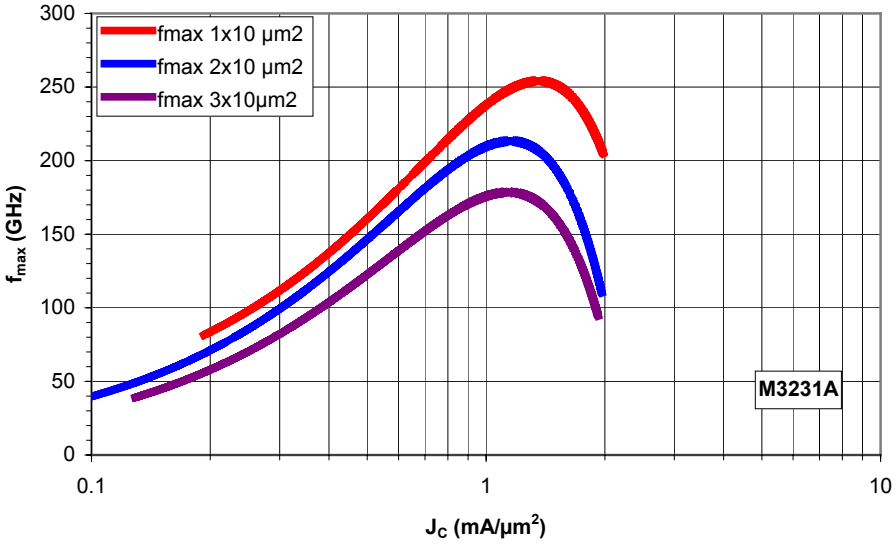


Figure 4.22 The measured maximum oscillation frequencies of HBT's with various widths at V_{CE} = 1.5 V (L_E= 10 µm)

Figure 4.22 shows that maximum oscillation frequencies of 255 GHz and 210 GHz are achieved for 1x10 µm^2 and 2x10 µm^2 devices respectively. Here, by doubling the emitter width, a 20 % decrease in maximum oscillation frequency is observed. This result has good agreement with the extracted parameters. The slight increase in the maximum current density by smaller the emitter width is attributed to the delay of Kirk effect due to the collector current spreading [47] as elaborated in chapter 2.3. This effect is much more dominant especially for smaller emitter widths.

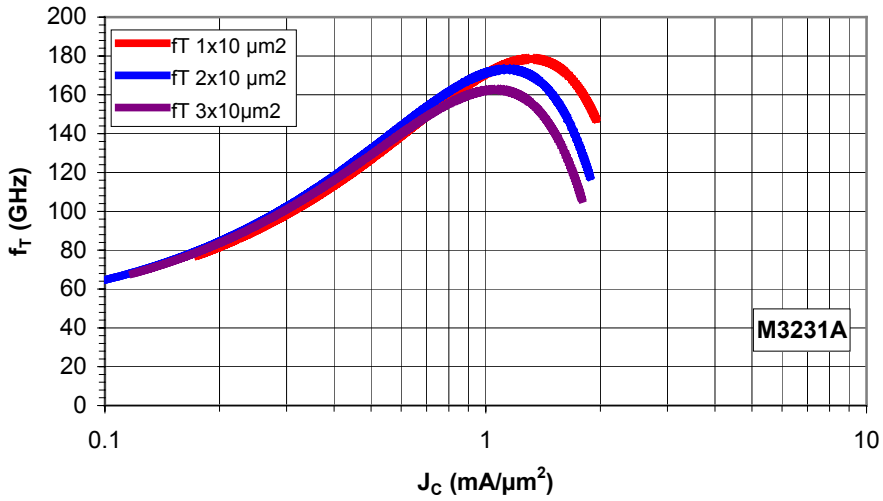


Figure 4.23 The measured cut-off frequencies of HBT's with various widths at V_{CE} = 1.0 V (L_E= 10 µm)

Comparable results are also observed in the work of Hattendorf [84] and Shen [85].

In addition to the influence of the emitter width and length on transistor RF performance, comparison of non-self aligned and self-aligned HBTs are also observed. For these purposes, 1x15 µm^2 devices, which present the best RF performance, have been chosen. The RF measurement results are depicted in figure 4.24.

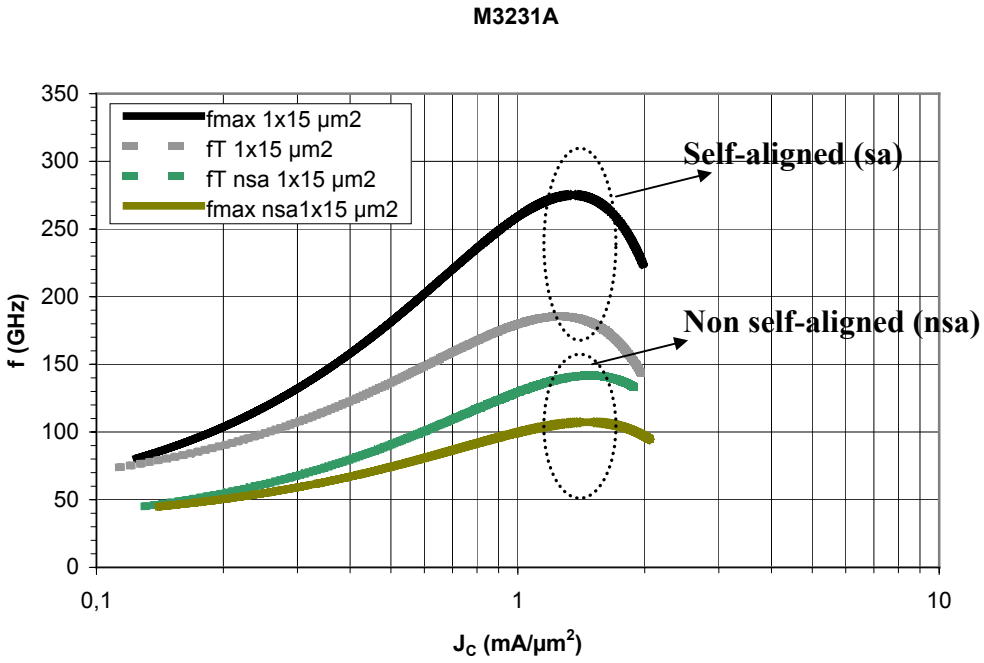


Figure 4.24 The comparison of self-aligned and non-self aligned 1x15 µm² SHBTs

As discussed in detail in Chapter 3.2.1.2, the underetching of emitters with the optimised wet chemical etching is for one side about 200 nm, thus the spacing between the base and emitter is also 200 nm for each side. In non-self aligned HBTs, since the base contact is patterned 1 µm beside the emitter contact, the total spacing between base and emitter here is about 1.2 µm for each side. This will result 50 % larger base-collector area, which will lead to higher base-collector parasitic capacitance. Moreover, since the spacing of base contact is large, this will increase the base resistance. These both will degrade the maximum oscillation frequency, as depicted in equation 2.10. From the s-parameters, base resistance (R_{bb}) of 31 and 51 Ohms are achieved for self-aligned and non-self aligned 1x15 µm² devices, respectively. The increase in the base resistance is because of the increase in the spacing between base emitter contact and therefore increase in the gap resistance as depicted in equation 2.11. The base-collector capacitance of non-self aligned device is nearly tripled.

In addition to the RF performance analysis for various emitter dimensions, the dc behaviour are also investigated to elaborate the influence of the perimeter – area ratio. From the Gummel Plot for an HBT of 1x15 µm² emitter area, base (n_B) and collector (n_C) ideality factors are extracted to be 1.26 and 1.14, respectively. These

results are comparable with SHBTs from Walid Hafez, in which the base and collector ideality factors are 1.35 and 1.18, respectively [86].

For the determination of the leakage currents and the surface effects on the manufactured transistors, devices with various perimeter area ratios are compared. From Figure 4.25, it has been observed that by increasing the emitter area the base current increases, too. On the other hand, the perimeter to area ratio plays an important role for the transistor's dc current gain. The dc current gain can be depicted in terms of base current components as in equation 4.1 [14].

$$\frac{1}{B} = \frac{J_{B,bulk} + J_{B,scr} + J_B^*}{J_C} + 2\frac{K_{B,surf}}{J_C}\left(\frac{1}{W_E} + \frac{1}{L_E}\right) \qquad \text{equation 4.1}$$

where $J_{B,bulk}$, $J_{B,scr}$ and J_{Bp} are the base bulk recombination current density, the base-emitter space-charge recombination current density, and the base-to-emitter back injected current density, respectively. $K_{B,surf}$ is the surface recombination current divided by emitter periphery and J_C is the collector current density. W_E and L_E are the emitter width and emitter length, respectively.

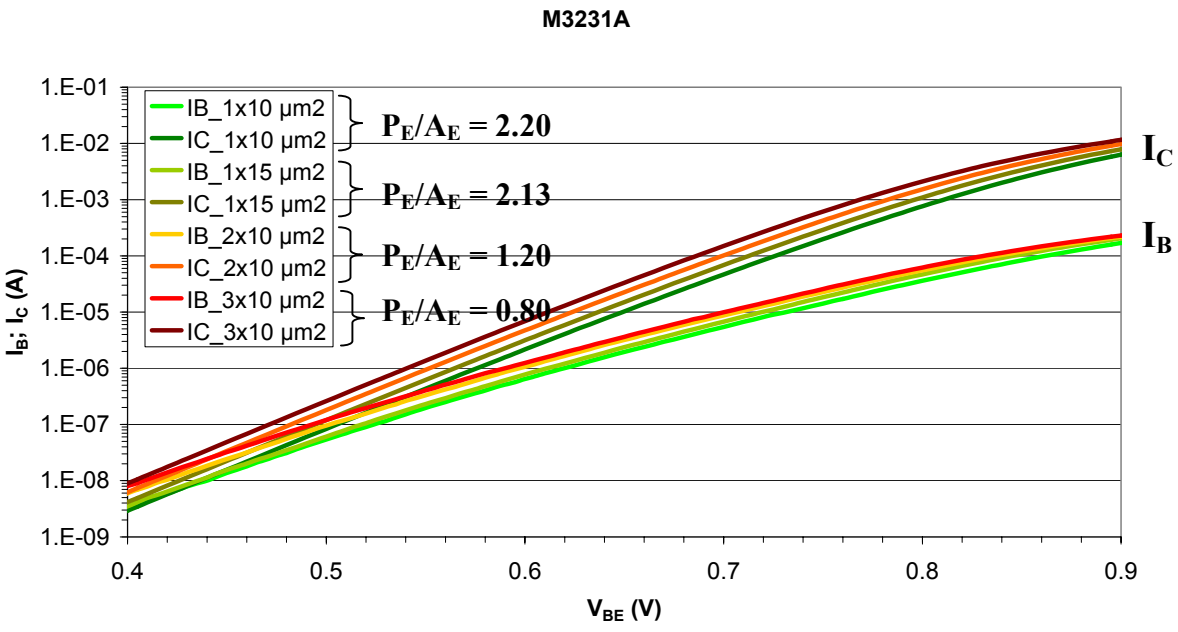


Figure 4.25. The Gummel Plot for various Perimeter Area ratio (P_E/A_E) at V_{CB}= 0V

The dc current gain for various emitter perimeter area ratios is depicted in figure 4.26.

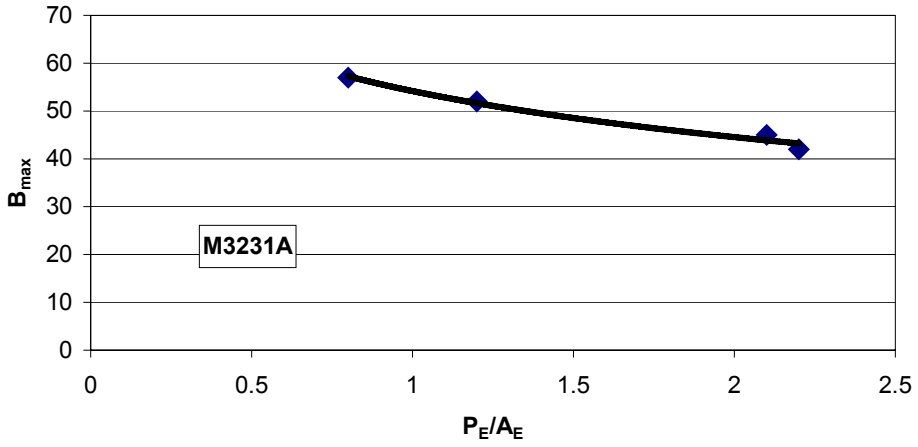


Figure 4.26 dc Current gain for various perimeter area ratio.

From figure 4.26, it is obvious that perimeter to area ratio (P/A) is inversely proportional to dc current gain. The dc current gain decreases by decreasing emitter area. These results show good agreement with the theoretical definition of emitter size effect and with the equation 4.1.

5 Inductively Coupled Plasma (ICP-RIE) Etching for HBT Applications

The plasma etching is firstly introduced in the 1970s and rapidly became a standard technique for semiconductor etching [87]. In the early phase, it was mostly used for resist stripping applications and then adopted to semiconductor etching. By the advances in circuit densities, smaller structures are required.

In comparison to wet chemical etching, plasma etching can provide anisotropic profile, therefore it became one of the best solutions for smaller dimensions. Moreover, adhesion of the mask on semiconductor is no more a severe problem for dry etching, and dangerous acids and/or solvents can be avoided [88]. It can also be carried out more easily with automated processes, which is an important aspect for industry.

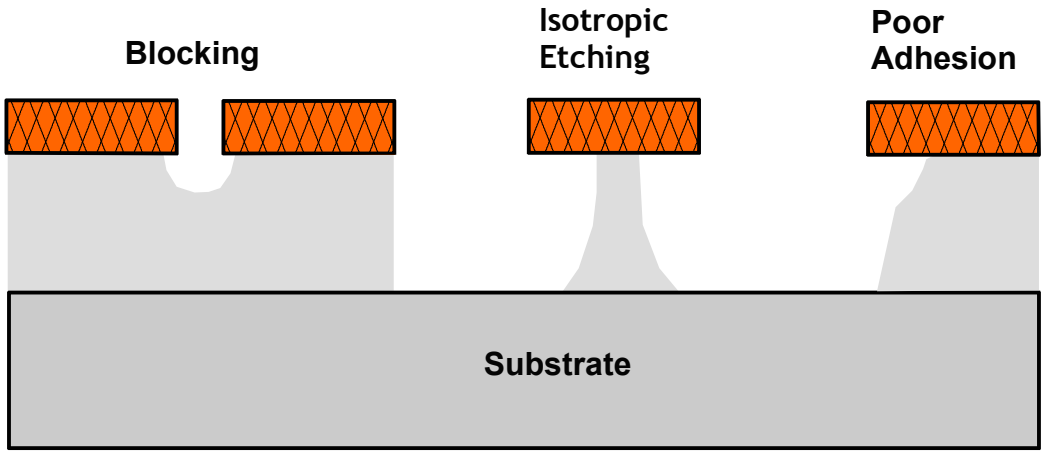


Figure 5.1 Problems with wet chemical

On the other hand, for plasma etching, there are challenges like surface defects caused by the ion bombardment in plasma and the loading effects because of the redeposition of the etched semiconductor and/or mask on the sample [89]. In this chapter, basics about the plasma etching and the optimised process with the new ICP-RIE (Inductively Coupled Plasma-Reactive Ion etching) with Cl_2/N_2 chemistry will be elaborated.

5.1 Basics of Plasma Etching

Before going into the details of the system and process optimisation, the basics about the plasma etching will be described.

Plasma can be considered as an ionised gas. By applying an electric field, free electrons collide with neutral molecules and form ionised gas molecules and more free electrons. Depending on the energy of the colliding electrons, there may happen various reactions. Highly energetic electrons (e*) may remove an electron from the molecules XY and ionise them. This is the most important reaction sustaining the plasma.

Ionisation: $e^* + XY \rightarrow XY^+ + e + e$ equation 5.1

They may also dissociate molecules XY into their atoms X, Y. Therefore; this reaction is named as “dissociation”.

Dissociation: $e^* + XY \rightarrow X + Y + e$ equation 5.2

When these high-energy electrons collide with molecules, they may excite one of the electrons to the higher state. This reaction is called excitation.

Excitation: $e^* + XY \rightarrow XY^* + e$ equaiton 5.3

When the excited electrons of the molecule XY^* shown in equation 5.3 return to their ground state XY, they will emit light, which is also known as glow discharge.

Relaxation: $XY^* \rightarrow XY + h\nu$ (optical emission) equation 5.4

With this knowledge, when considering RF plasmas, it is necessary to separate the plasma into two regions. These are bulk and sheath region. Since electrons are much lighter than ions, they may respond the alternating field applied to the electrode. They

will more frequently hit the electrodes and reactor walls. This will leave the plasma positively charged. During the positive cycle of the power supply, electrons in the plasma are attracted to the electrode and charge the capacitor negatively. As a consequence, a negative dc bias, which continuously attracts ions to the electrode for etching, is formed on the electrode. Close to the electrode, a sheath region (dark region) is observed. In this region, the density of free electrons is lower and therefore less collisions and less optical emissions occur.

Pressure is also important for the dc bias. At higher pressure levels, the mean free path of the electrons decrease. Therefore they gain less energy, which results in less formation of new electron and ions pair.

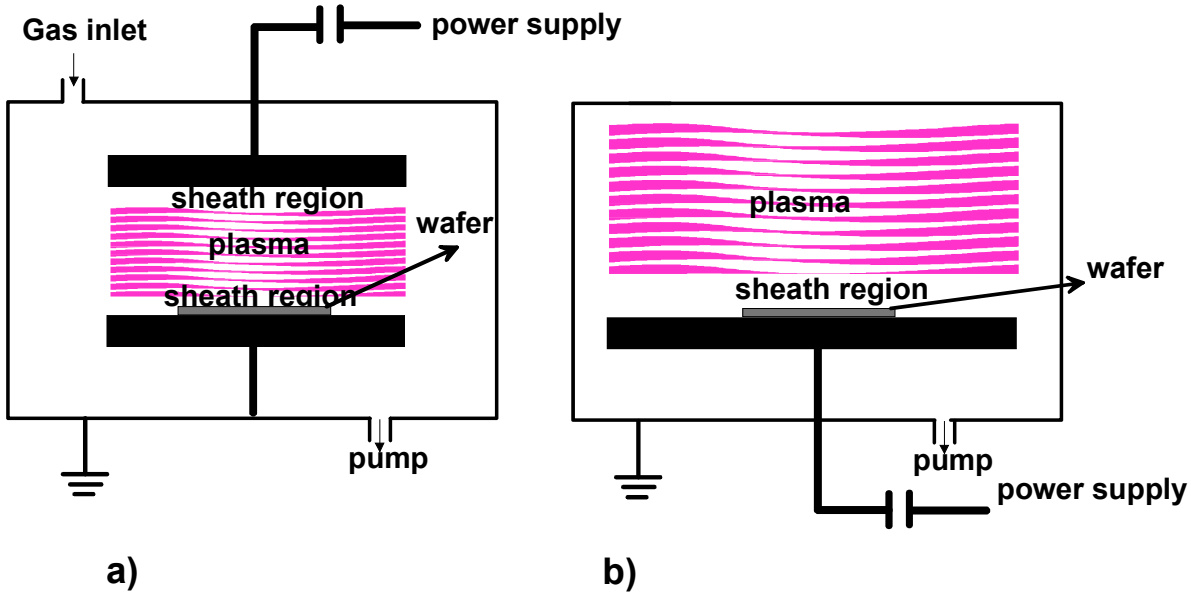


Figure 5.2 Typical plasma reactor showing the sheath and the plasma region. a) parallel plate plasma etch reactor b) Reactor in RIE configuration

Like in the wet chemical etching process, plasma etch can also be considered in terms of different steps. Six major steps are:

i. Generation of reactive (etchant) species
ii. Diffusion (transport) of these species to the surface
iii. Adsorption of etchant onto the surface
iv. Chemical reaction
v. Desorption of the byproducts from the surface
vi. Transport of byproducts away from the surface [90, 91]

There are different mechanisms in plasma etching. These are: chemical and physical etching.

The mature plasma system is one where the upper electrode is connected to the power supply, as shown in Figure 5.2a. It is used to generate the reactive species, which reacts with the surface and etches the material. The byproducts are desorbed from the surface and pumped away from the chamber. Basically, this type is named as chemical type. Therefore, the etching is isotropic.

There are also systems where the lower electrode is connected to the power supply and inert gas, e.g. Ar, is introduced to the system. The Ar ions are accelerated to the substrate with high kinetic energy. Ions hit the surface and knock atoms out of the surface. With this system, one can achieve an anisotropic profile but with a poor selectivity to the mask and damage to the sample.

One of the most commonly used plasma systems is reactive ion etching system (RIE), where ion bombardment and chemical reaction occur. This configuration is shown in figure 5.2 b. Here, chemically reactive gas i.e. Cl_2, CH_4, etc for the chemical reaction and inert gases for the bombardment are used as process gases. With the synergy of physical and chemical etching, it is possible to achieve higher etch rates with desired profiles and reasonably low damage. In RIE systems, the density of ions and the acceleration of the ions are realised by the same power supply connected to the lower electrode. To achieve higher etch rates, one may need higher ion densities. But, since the ion density and physical component of the etching are controlled by the same supply, higher power is necessary, which will also yield to higher physical etching. As a consequence, this will lead to critical substrate damage. To prevent this problem, systems are proposed where the ions are generated with an independent power supply. One of these systems is Inductively Coupled Plasma (ICP) system. Here, two power supplies are employed. One is connected to the lower electrode to mainly control the physical etching component and the other is inductively coupled through the walls to maintain the plasma and control the ion density. With these systems, one can optimise a process providing higher etch rates, and vertical profiles without degrading the surface quality.

5.2 ICP-RIE System

For InP HBT etching, anisotropic etching with vertical profile, lower etch rates and less surface damage are desired. Since the ion density and the dc bias can be controlled independently, an ICP-RIE system is preferred for this work [92]. The system that has been used during this thesis is Oxford Instruments Plasma Technology PlasmaLab System 100 ICP65 [93]. It is a modular system, on which the ICP head can be installed. ICP65 stands for chambers supporting up to 65 mm diameter wafers. The chamber and its parts are depicted shown in Figure 5.3. The 13.56 MHz, 300 W RF power sources are used for both ICP and substrate electrode. The ICP head is electrostatically shielded to ensure the inductive coupling. The wafers are loaded to the processing chamber via an automatic load-lock. With this load-lock system, the chamber stays clean and isolated from outside. This is an important aspect for the reproducibility of the process. The chuck supports up to +400 °C. To achieve temperature homogeneity, the sample is mechanically clamped to the chuck and helium pressure is applied to the back of the sample to provide good thermal conductivity. The system can be operated between 1 mTorr to 100 mTorr. The complete system is software (PC2000) controlled. All the processing parameters can be input via a PC and processes can be monitored. Different user levels can be programmed for different operators. For the safety, there are different alarm levels controlling the system and the process. The recipes can be written and saved. There is also the log option for the software, keeping all the information about the system and details about the process. Details of the system and the mimics of the software can be found in Appendix H.

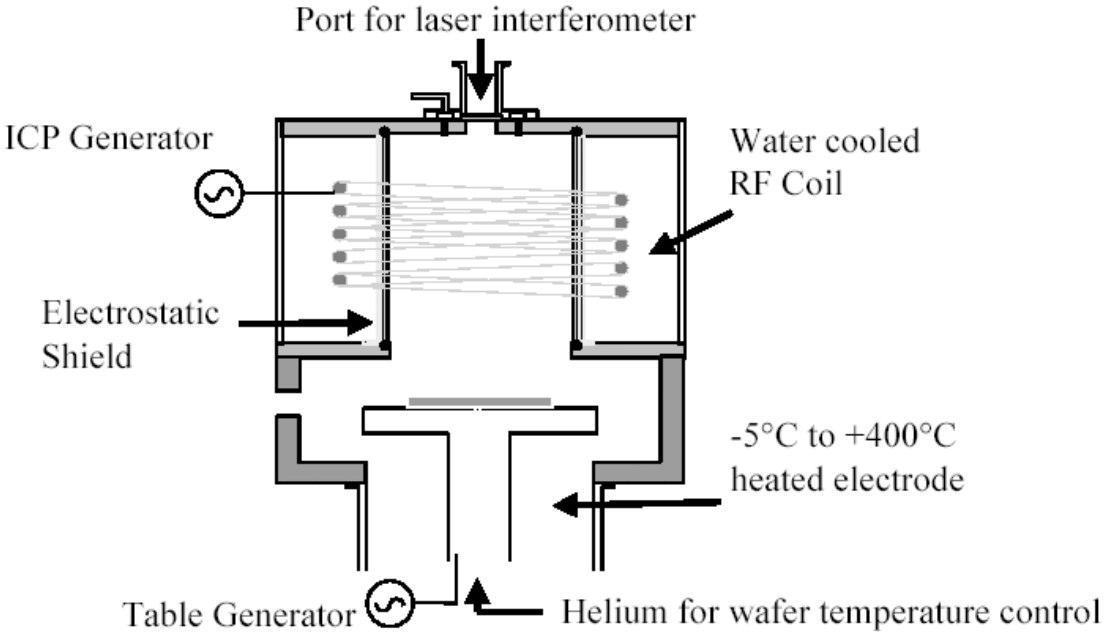


Figure 5.3 A typical schematic of the Plasmalab System 100 ICP-RIE Tool [94]

Traditionally, methane (CH_4) based chemistries have been preferred for InP and related material etching [95]. Even though, this chemistry offers low etch rates and easy desorption of the byproducts from the surface, they suffer from polymerisation and hydrogen passivation of the acceptors in the base layer [96]. If carbon (C) is used as p-type dopant in the InGaAs base layers, these acceptors are passivated by hydrogen radicals originating from the plasma and diffusing into the base layer. As a consequence, base resistance increases, which also degrades the RF performance [97, 98, 99, 100, 101]. Because of polymerisation, the chamber conditions are affected, which yields to problems in reproducibility of the process. Since they do not contain hydrogen based gases and offer higher etch rates, especially for photonics applications, Cl_2 containing chemistries are preferable [102, 103]. The commonly used ones are; Cl_2/Ar, pure Cl_2 and Cl_2/N_2 [104, 105, 106, 107]. There are also other chemistries containing iodine and bromine. Especially, due to the difficulties in gas handling, iodine chemistries are not preferred. On the other hand, since the $InBr_3$ byproducts can be removed at lower temperatures than $InCl_3$, the use is increasing recently, but there is still optimisation necessary for the sidewall profile as pointed out in [108, 109]. Since it offers cleaner processes and contains no hydrogen, Cl_2 based chemistries for our HBT applications have been chosen. It is well known that $InCl_x$ byproducts are not volatile at lower temperatures. The boiling point of $InCl_3$ is 600° C, where this value is 76 °C for

PCl_3 [110]. Since $InCl_x$ byproducts are resulting in rough surfaces and slow etch rates, N_2 is added to support the physical component, which can provide vertical sidewall profile and reduce the surface roughness. By the formation of NCl, the etch rate can be reduced for InP etching, which is an important aspect for the emitter etching having only 200 nm total thickness. Moreover, N_2 can also passivate the sidewalls and improve the sidewall profile [111, 112].

In addition to the Cl_2 and N_2 process gases, O_2 is connected to the system as process gas. With oxygen, one can clean the polymers deposited in the chamber.

5.3 Optimisation of the Process Parameters for ICP-RIE etching

In the ICP-RIE system, there are different parameters affecting the etching properties. These are mainly: temperature, power, pressure, gas flow ratio, mask materials. Before going into the details, the preparation phase will be addressed briefly.

The system supports 2" wafers. A carrier wafer is necessary if smaller pieces are in process. These pieces have to be glued on the carrier in order to achieve good thermal contact with the carrier and to distribute the heat over the sample homogenously. As glue material Dow Corning High Vacuum Grease has been selected, which is not toxic and stable even at higher temperatures [113]. Here, the grease should cover the whole backside of the sample. Special attention should be paid to prevent any grease exposing to the plasma, which may contaminate the chamber and/or deposit on the sample.

A special mask shown in figure 5.4 is used during the process optimisation. This mask contains patterns having 0.5, 1, 2, 3, 5, 10, 20 μm width with different orientations i.e. 45°, 90°, 180° to the major flat. With these orientations, one can identify the influence of crystal orientation on the etching.

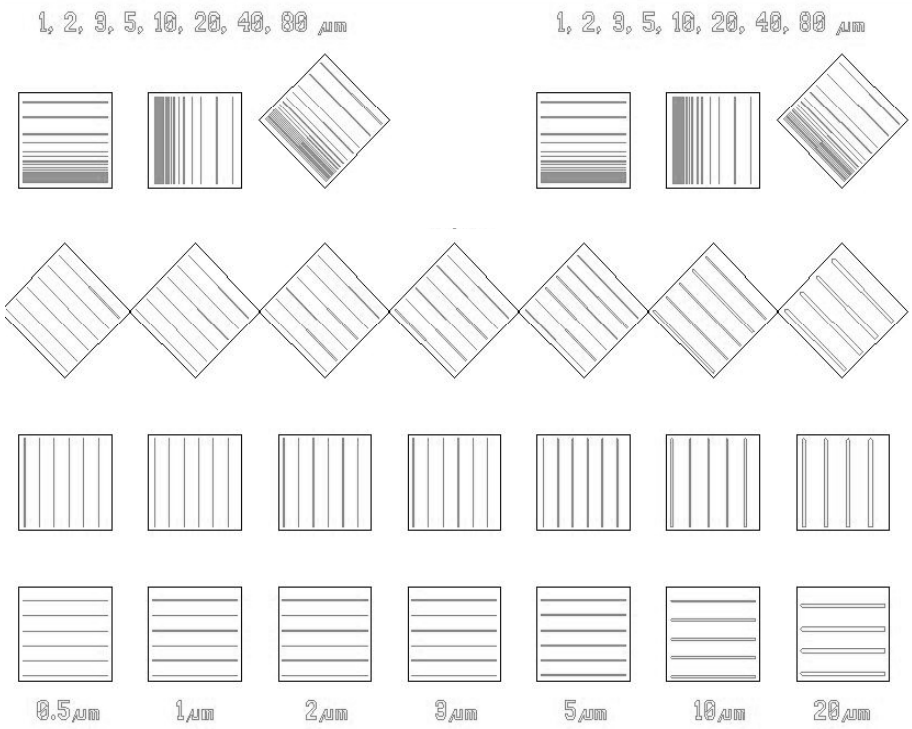


Figure 5.4 Etching mask with patterns in different orientations to be used for ICP-RIE process optimisation

Since the process is optimised mainly for the realization of HBTs with submicron emitters, a metal mask, which is resistant against Cl_2/N_2 chemistry, is necessary. For this purpose, Nickel (Ni) has been chosen [114, 115]. The Ni mask is deposited with e-beam evaporator on the standard emitter metal layer, 10 nm Ti, 10 nm Pt, 400 nm Au. Since the conductivity and resistance against corrosion are comparable to gold (Au), it is not necessary to remove nickel after the process. For our processes, 50 nm Ni is patterned and deposited using standard lift-off technique, as explained in chapter 3. In the early phase of the mask realization, some problems were experienced.

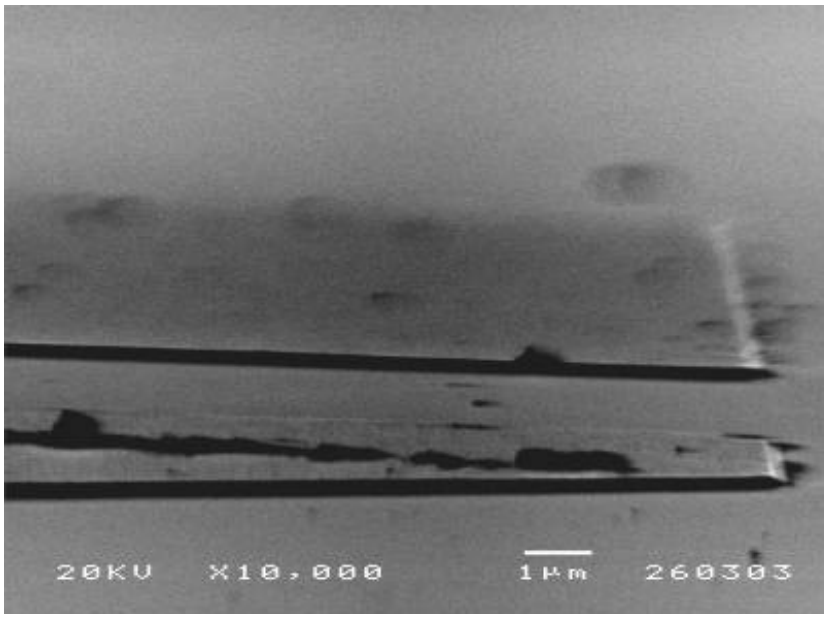


Figure 5.5 Ni mask lift-off problem with non-optimised deposition rate resulting in metal rests on the corner of the metal stripes.

As shown in Figure 5.5, there are metal rests on the corners of the metal stripes. This will lead to problems in the functionality of the devices and sidewall profile of the etched structure. This case is attributed to the deposition rate and time of the nickel. The evaporator deposits Nickel with deposition rate of 5 A°/sec. For the deposition of 100 nm thick Ni, 3.5 minutes of deposition time is necessary. This leads the lift-off photoresist to be exposed with high temperature for long time and degrades the lift-off profile of the resist. The deposition rate is reduced to 3 A°/sec and breaks have been given during the evaporation of the Nickel. With the optimised deposition rate and time, the spoil of the photoresist is avoided. Further, additional O_2 plasma ashing has been performed just before the evaporation. The final optimised Nickel mask is shown in figure 5.6.

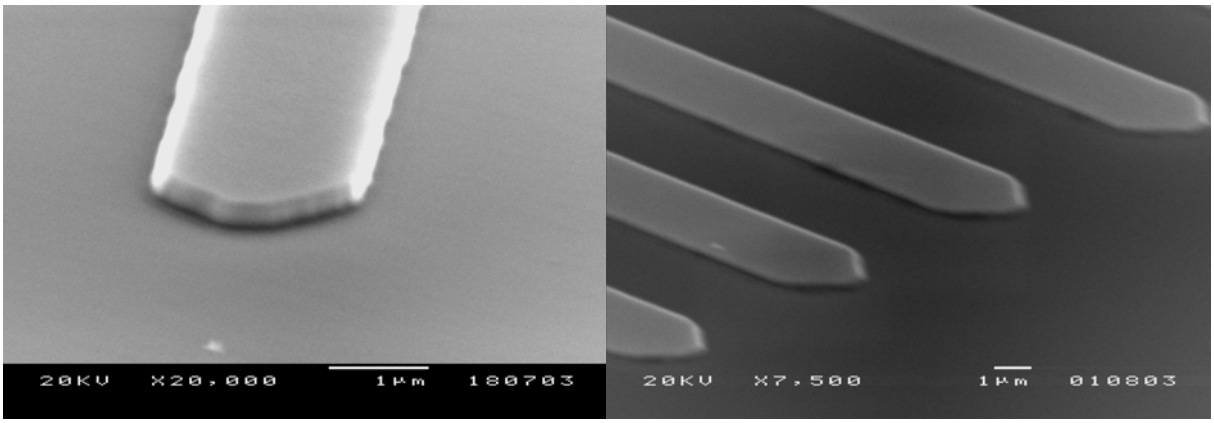


Figure 5.6 Optimised Ni mask on standard emitter metal (Ti/Pt/Au) with a smooth metal sidewall.

The objectives of the etching are: smooth surface and vertical sidewalls with low etch rates. To investigate the sidewall and surface profiles, scanning electron microscope (SEM) is used. To check the detailed surface morphology, Digital Instruments Dimension 3000 Atomic Force microscope (AFM) is used. For the determination of the etch rate, the surface profiler, Veeco DEKTAK ST, is utilized. Since HBTs have InP as emitter and InGaAs as emitter cap, InGaAs single layers on InP substrate are used as test samples. To maintain reliable results, for all of these tests, layer structures with same thickness and same size of samples are used. 2-minutes is chosen as process time.

5.3.1 Effect of Temperature

5 different temperature values 40, 100, 150, 170, 190 °C have been investigated to observe the influence of the temperature on the etching properties. Pressure is kept at 4 mTorr, ICP power at 300 W, and 50% ϕ_{Cl2} to total gas flow (ϕ_{Cl2+N2} flow). The mean free path is inversely proportional to the pressure, however at this low pressure level the probability of the electrons collision with molecules is low to sustain the plasma. To overcome this problem, the "strike pressure" option is used. Basically, the process is started with high pressure levels like 40 mTorr and plasma is sustained. Once it strikes the plasma, the pressure is reduced to the processing pressure. Pretest at 150 °C demonstrated that in spite of improving the thermal contact by Helium application from the backside, 5 minutes are necessary to establish the intended process temperature at

the sample surface. This may be due to a degraded thermal contact caused by the glue used.

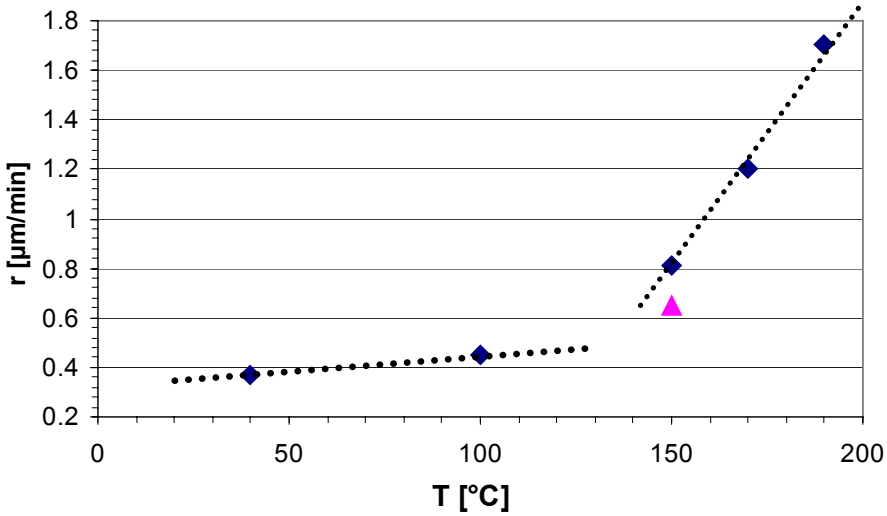


Figure 5.7 The etch rate for InGaAs/InP vs. temperature at p = 4 mTorr, P_{RF} =150 W, P_{ICP} = 300 W, $\phi_{Cl2} = \phi_{N2}$ = 10 sccm. The blue diamond points are the etch rates for 5 minutes of pre-bake and the purple triangle represents less etch rate for 2 minutes of pre-bake on the chuck.

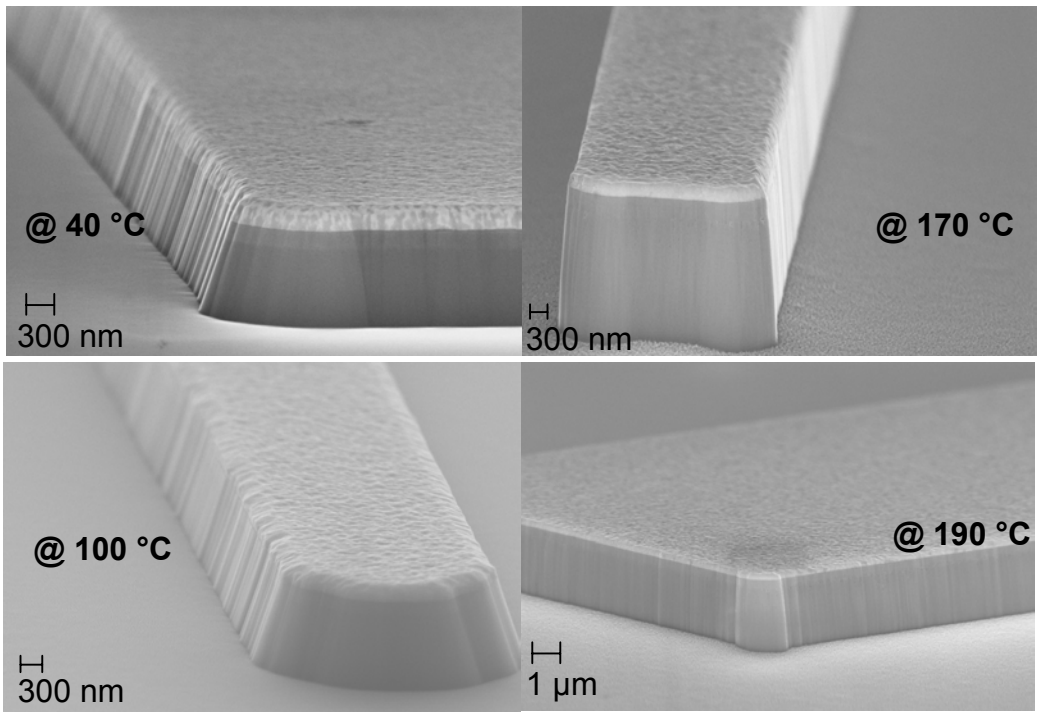


Figure 5.8 Sidewall profile for metal stripes etched with ICP-RIE at various temperatures, p = 4 mTorr, P_{RF} = 150 W, P_{ICP} = 300 W, $\phi_{Cl2} = \phi_{N2}$ = 10 sccm.

As shown in figure 5.7, there are two different regions depicted with the dotted lines with different slopes. For temperatures less than 150° C, the etch rate is lower. This is because of the low volatility of the $InCl_x$ [115]. Figure 5.8 shows that temperatures less than 150° C result into the tapered sidewall profile. But, at process temperatures higher than 150° C, the sidewall angle is nearly 90°. The difference in the slope is attributed to less desorption of $InCl_x$ from the surface and the sidewall at lower temperatures. On the other hand, AFM measurements have proven that at lower temperatures, the root mean square (RMS) surface roughness is around 0.3 nm. For the etched surface, this is an unusual case. Because, normally, before etching, RMS surface roughness of the substrate was already in 0.3 nm range. Rougher surface is expected after etching. It is supposed that the surface is damaged by the unbalanced etching of the substrate. For the unbalanced etching, the physical etching is more dominant. Moreover, since the temperature is lower, the desorption of the $InCl_x$ residues is no more effective. In other words, there occurs a thin In rich film, and the surface is no more crystalline. It is amorphous. On the other hand, for 170 °C, 5 nm RMS surface roughness is measured. The 3D AFM measurements for 40 °C and 170 ° C etching, are shown in figure 5.9.

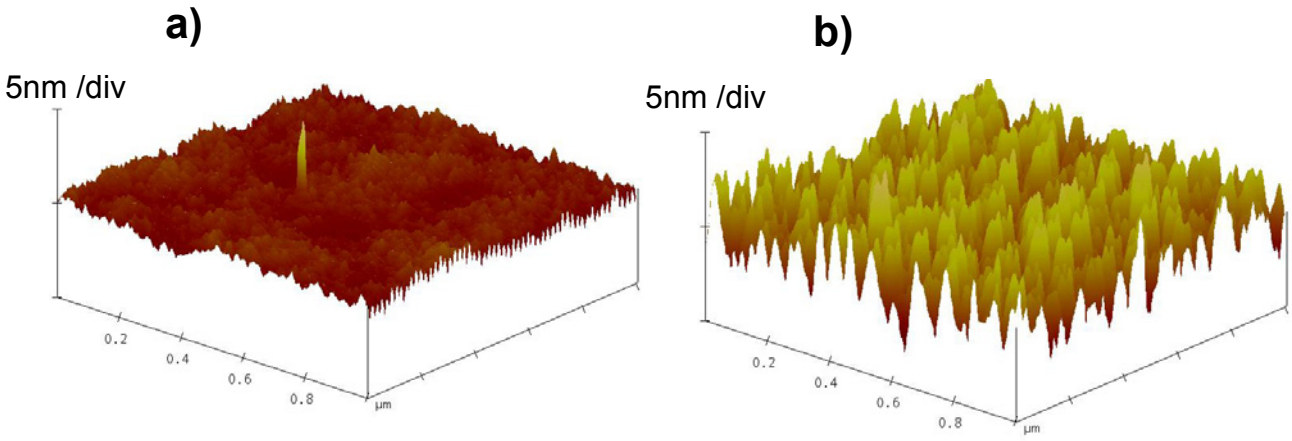


Figure 5.9 The AFM result for the etched surface a) at 40 °C; b) 170 °C, p = 4 mTorr, P_{RF} = 150 W, P_{ICP} = 300 W, $\phi_{Cl2} = \phi_{N2}$ = 10 sccm.

Since it offers proper properties with respect to less damages, lower etch rate, about 90° sidewall profile, 170 °C has been chosen as table temperature for the remaining optimisation process.

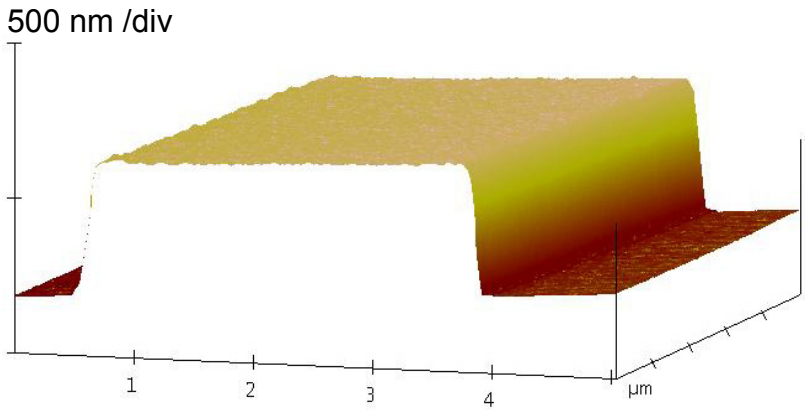


Figure 5.10 The AFM result for the etched sidewall and surface at 170 °C, p = 4 mTorr, P_{RF} = 150 W, P_{ICP} = 300 W, $\phi_{Cl2} = \phi_{N2}$ = 10 sccm.

5.3.2 Effect of Gas Mixture

As already discussed, Chlorine (Cl_2) is used for the chemical, Nitrogen (N_2) is used for the physical part of the etching. With different composition of gas mixture, one can influence the ratio of chemical and physical part of the etching. With our chemistry, since there may form NCl, the etch rate can be decreased by the gas ratio [112]. There are also additional effects of the gas mixture on the dc bias. When all other parameters are kept constant, the electronegativity properties of the gas will influence the dc bias voltage. The gases with lower electronegativity will provide higher absolute dc bias voltages. Chlorine is rather electronegative and prone to absorb free electrons and decrease the dc bias voltage [87].

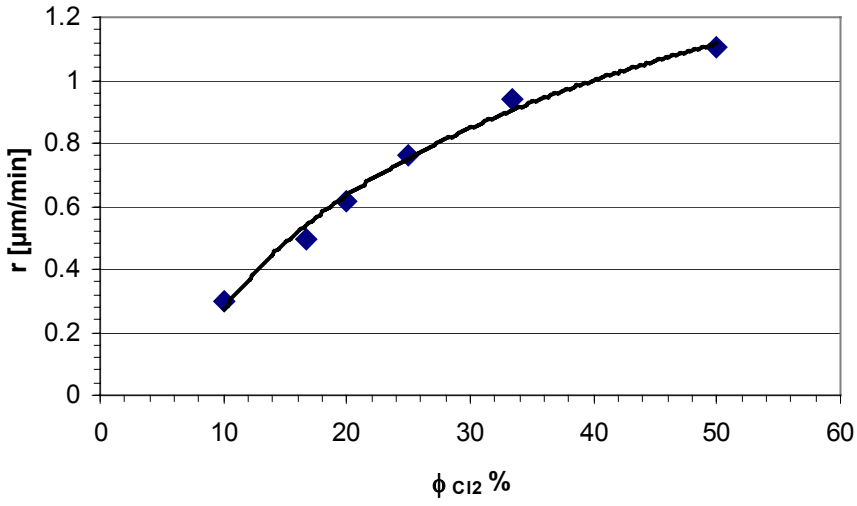


Figure 5.11 The etch rate for InGaAs/InP vs. Cl_2 content in total gas flow at p = 4 mTorr, P_{RF} = 150 W, P_{ICP} = 300 W, T = 170 °C.

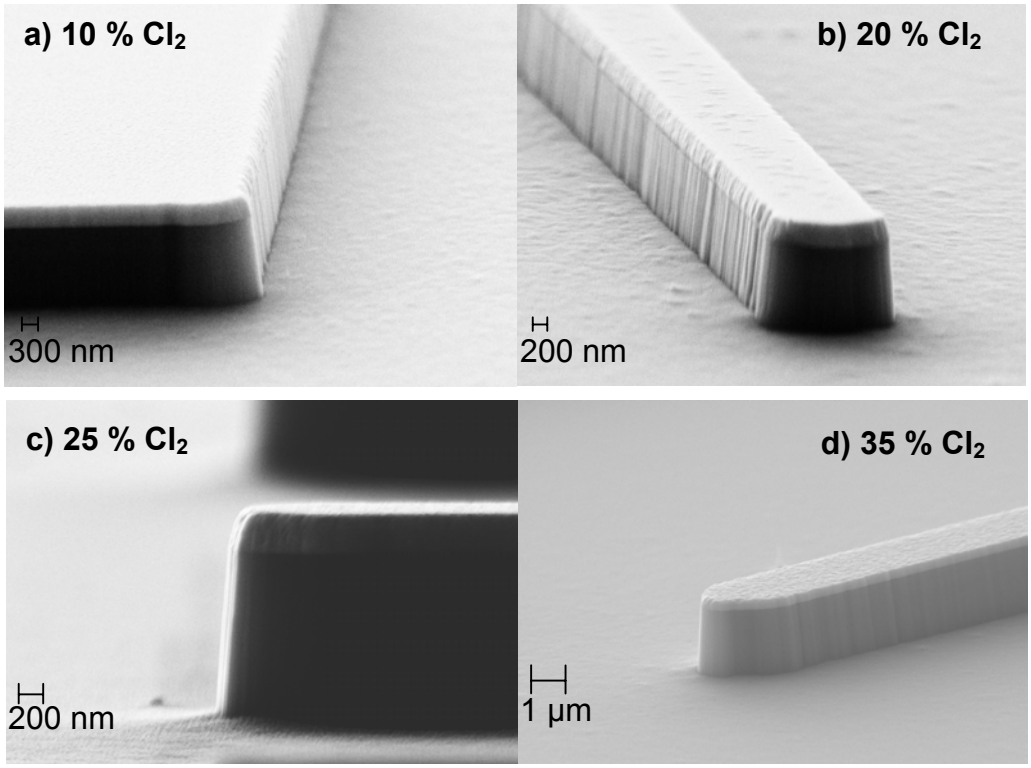


Figure 5.12 The SEM micrographs for various gas ratios showing vertical sidewall for different gas ratios and smooth surface at p = 4 mTorr, P_{RF} = 150 W, P_{ICP} = 300 W, T = 170 °C.

Figure 5.11 shows that by increasing chlorine ratio in the total gas flow, the etch rate increases, too. This is attributed to the enhancement of chemical etching by the chlorine. On the other hand, it is elaborated that for all gas ratios, the sidewall profile has approximately the same sidewall profile as shown in Figure 5.12. The AFM measurements have also been performed for these samples and all have shown RMS surface roughness less than 5 nm. The sidewall roughness in Figure 5.12 is due to the mask.

5.3.3 Effect of RF Power

The RF power is one of the main parameters influencing the dc bias. As mentioned already, ions are created by ICP power (coil power) and they are accelerated to the substrate by the dc-bias created by the RF power (table power). With this knowledge, it is obvious that by the increase of the RF power, the energy of the electrons and ions will increase, and this will result in higher dc bias voltage. By

keeping the temperature at 170 °C, the pressure at 4 mTorr, ϕ_{Cl2}/ϕ_{N2} ratio at 25 % and ICP power 300 W, experiments have been performed by varying the RF power.

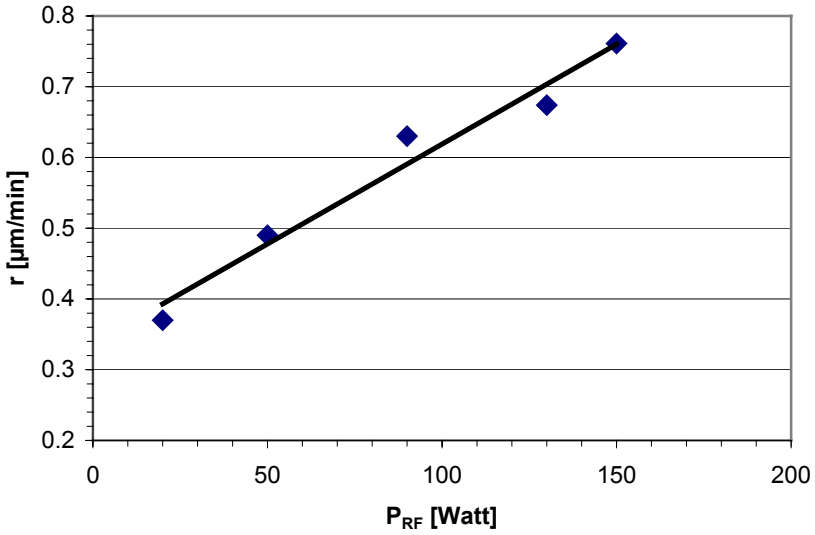


Figure 5.13 The etch rate for InGaAs/InP vs. RF power at p= 4 mTorr, $\phi_{Cl2}/(\phi_{Cl2+}\ \phi_{N2})$= 25 %, P_{ICP} = 300 W, T = 170 °C.

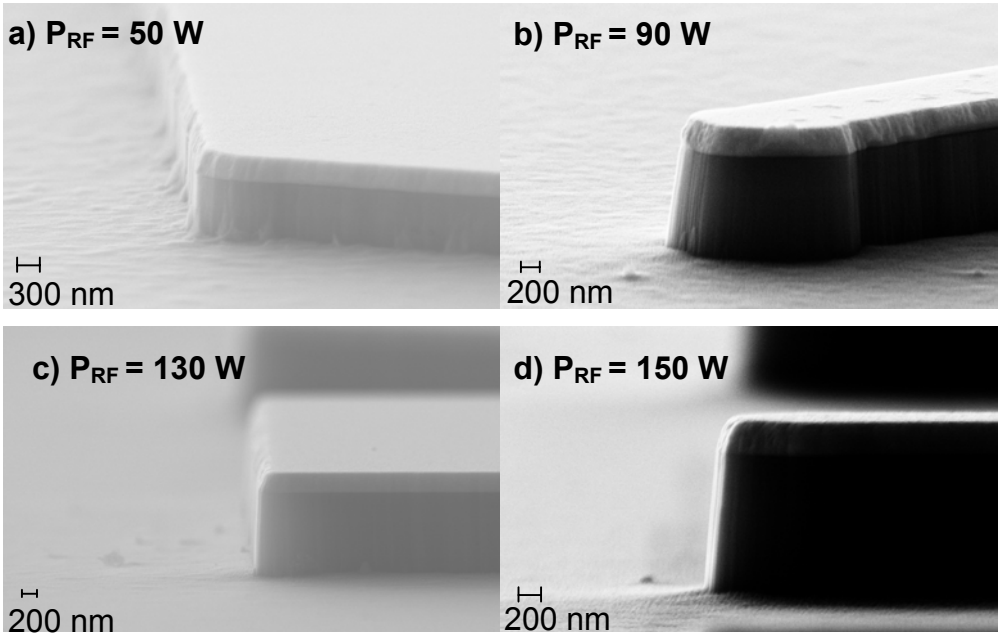


Figure 5.14 The SEM micrographs for various RF powers showing vertical sidewall profile at p = 4 mTorr, $\phi_{Cl2}/(\phi_{Cl2+}\ \phi_{N2})$= 25 %, P_{ICP} = 300 W, T = 170 °C.

For 20 W of RF power, an etch rate of 380 nm/min has been achieved at p = 4 mTorr, $\phi_{Cl2}/(\phi_{Cl2+}\ \phi_{N2})$= 25 %, P_{ICP} = 300 W, T = 170 °C . In the PlasmaLab system, the dc voltage is measured over the metal pin lift, where the sample is lifted up

during the transfer process. Since it is covered with the carrier substrate, here Si, the dc bias cannot be read successfully during the process. So, to measure the dc bias voltage, processes have been performed without transferring any sample into the chamber. For 20 W RF power about 140 V , for 150 W about 440 V dc bias voltages have been measured.

As it can be investigated from figure 5.14 a, since the physical etching part is lower with lower RF power, the sidewall of the structures became rougher due to $InCl_x$ residues. But still, when the surface is analysed with AFM, for all RF power, RMS surface roughness is measured as around 5nm.

During these tests, it has been observed that the etch rates for InGaAs and InP are approximately equal.

5.4 Optimised ICP-RIE Process Parameters for HBT Applications

After the series of experiments presented in detail in chapter 5.3, it has been found out that:

The temperature should be kept at 170 °C offering acceptable rough surface quality and vertical sidewall profile. Moreover, from these experiments, it is observed that one should decrease the chlorine ratio and the RF power to achieve lower etch rate, which is an important issue for emitter mesa etching having only 200 nm thickness. By combining these results, we have performed an ICP-RIE process at 170 °C, the pressure at 4 mTorr, the chlorine ratio to the total gas flow of 10 %, the RF power of 20 W and the ICP power of 300 W. With these parameters an etch rate of 120 nm/min has been achieved at 115 V dc bias voltage, which is sufficient to have a reproducible ICP-RIE etching process with desired profile and surface quality. The SEM micrograph of the test sample etched with optimised parameters is shown in figure 5.15.

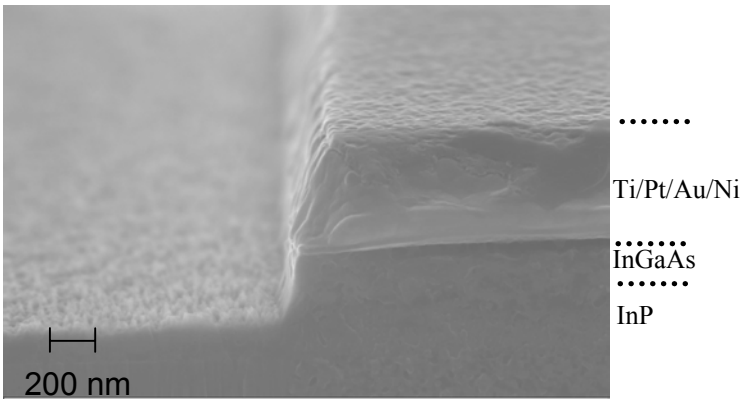


Figure 5.15 The SEM micrographs of a structure etched with optimised ICP-RIE process providing 120 nm/min etch rate at p = 4 mTorr, $\phi_{Cl2}/(\phi_{Cl2+}\ \phi_{N2})$= 10 %, P_{ICP} = 300 W, P_{RF} = 20 W, T = 170°C.

Here, the RMS surface roughness is measured to be 5 nm. The sidewalls are nearly vertical and no underetching present, which are desired especially for submicron HBTs.

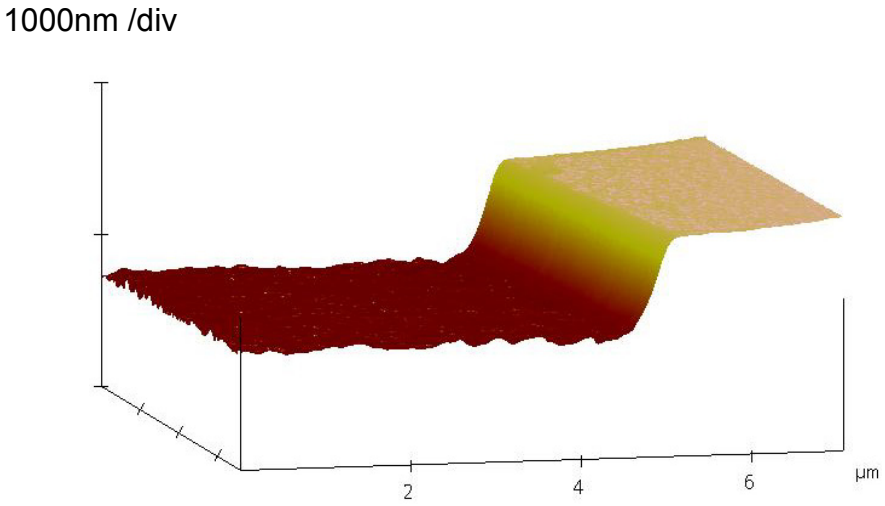


Figure 5.16 The AFM picture of the structure etched with optimised ICP-RIE process at p = 4 mTorr, $\phi_{Cl2}/(\phi_{Cl2+}\ \phi_{N2})$= 10 %, P_{ICP} = 300 W, P_{RF} = 20 W, T = 170°C.

Here, the selectivity of the etched material to the nickel mask is measured to be 20. The optimised process has been repeated and it has been observed that ± 5 % uniformity with respect to the etch rate over a quarter of a wafer is achieved. The run-to-run

repeatability for the etch rate is ± 5 % by keeping the surface roughness less than 5 nm and the sidewall profile vertical.

5.4.1 Removal of $NiCl_x$ residues from the surface

After the ICP-RIE processes, some residues have been observed on metal mask. This is attributed to the $NiCl_x$ residues occurring on material as shown in Figure 5.17.

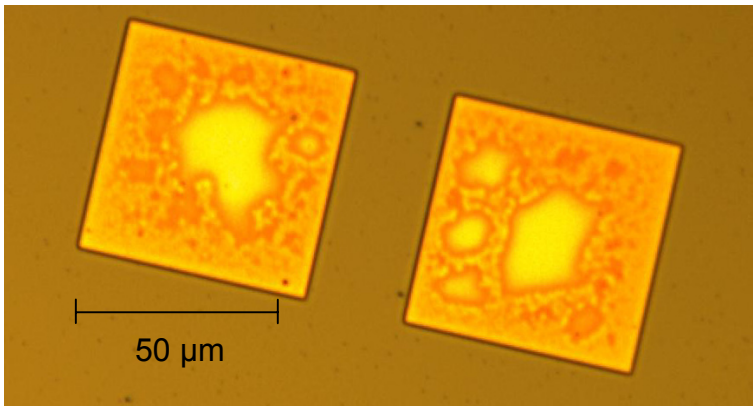


Figure 5.17 Optical micrograph of $NiCl_x$ residues on the metal structures after ICP-RIE etching

For the removal of these residues, water rinsing has been performed. It has been observed that optically clean metal surfaces have been achieved as shown in figure 5.18. After the electrical measurements, it is proven that these residues dissolve in water and do not spread and re-deposit on the wafer. So as standard process, just after the ICP-RIE process, 1 minute of water rinsing is performed for the sample.

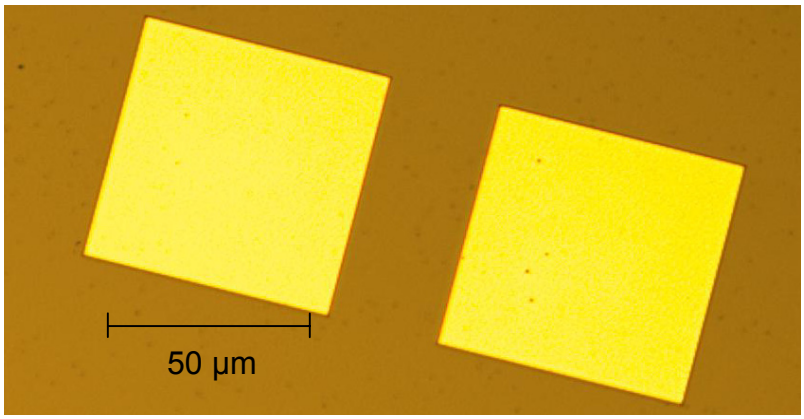


Figure 5.18 Optical micrograph of metal structures with clean and smooth surface after 1 minute of water rinsing

5.5 Optimisation of Hybrid Etching

In chapter 5.4, it has been presented that an etch rate of 120 nm/min providing good surface quality and vertical sidewalls can be achieved with ICP-RIE. But, as explained in detail in chapter 2 and 3, self-aligned HBTs are required for high-speed devices. With only ICP-RIE etching, it is difficult to realise self aligned HBTs. There are two main reasons for that. Firstly, with ICP-RIE, one cannot achieve selective etching between InGaAs and InP, which is required to stop on the thin base layer. Secondly, since ICP-RIE offers vertical sidewall with no underetching, there may happen short circuits between base and emitter. To prevent this, additional selective wet chemical etching is desired to achieve underetching. At the mean time, the high wet chemical etch selectivity ensure that the etching stops at the base layer. The combination of ICP-RIE first and then sequentially wet chemical etching, is named as "hybrid etching" [116].

By using HBT03 mask, emitters are patterned on the HBT layer stack as given in Table 2.3. Subsequently, the emitter mesa is etched with optimised ICP-RIE process for 75 seconds providing 150 nm etching. This means, vertically 100 nm of InGaAs emitter cap and 50 nm of InP emitter contact layers are etched. To achieve enough underetching necessary for the self-aligned base contacts, InGaAs layer is selectively etched. Here, 15 seconds H_3PO_4:H_2O_2:H_2O (1:1:25) etching is performed. This etchant has an etch rate of 2.5 nm/sec for InGaAs layer.

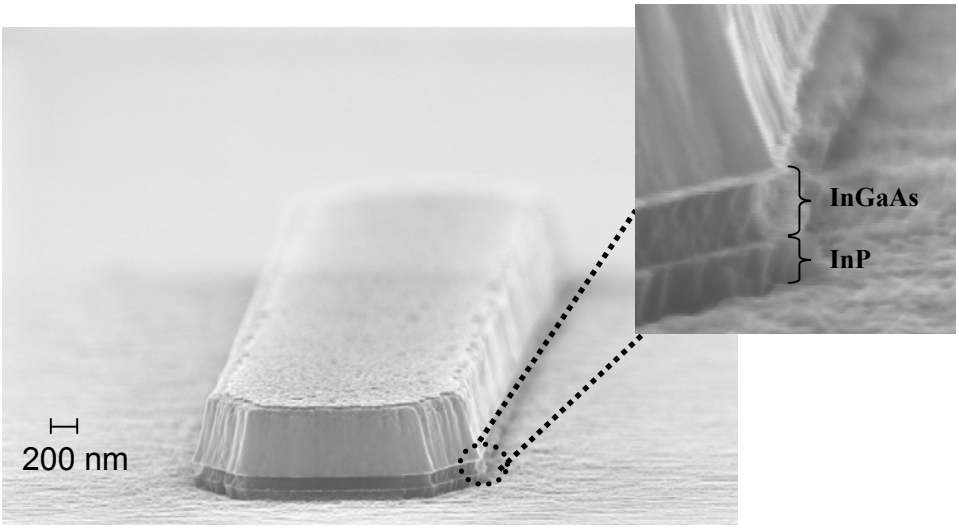


Figure 5.19 The SEM micrograph of the 2 µm emitter stripe after hybrid etching of InGaAs emitter cap

In figure 5.19, an emitter stripe having 2 µm width is shown after hybrid etching of InGaAs emitter cap. To reach the base layer properly, the InP layer is selectively etched for 20 seconds using 1:1 ($HCl:H_2O$). The achieved profile is shown in figure 5.20.

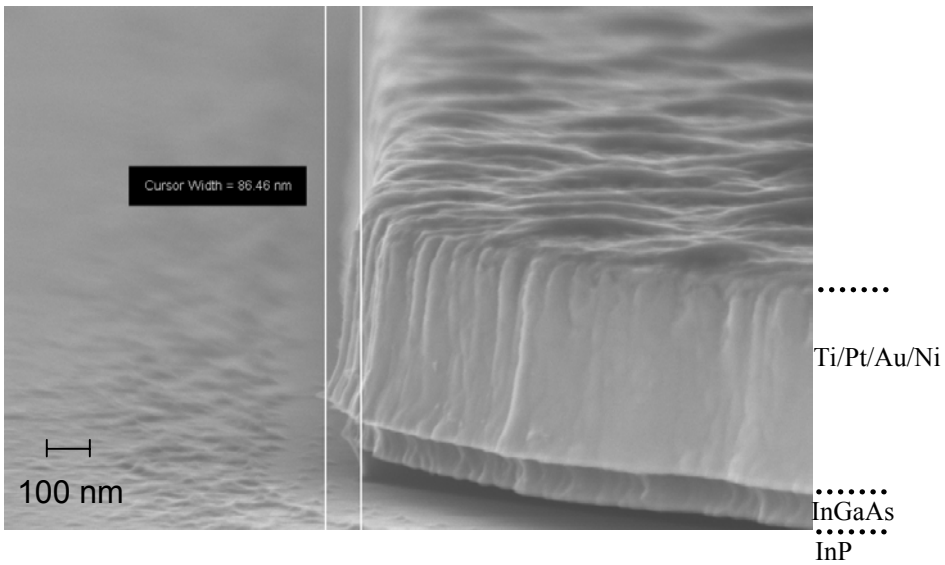


Figure 5.20 The SEM micrograph of 2 µm emitter stripe after complete hybrid etching with 85 nm underetching for InP layer

As measured with SEM, the lateral etching for emitter stripe is about 85 nm in total, which is pretty good value for the realisation of submicron HBTs.

The surface is analysed with AFM after hybrid etching. According to these measurements, RMS surface roughness of 2 nm is achieved.

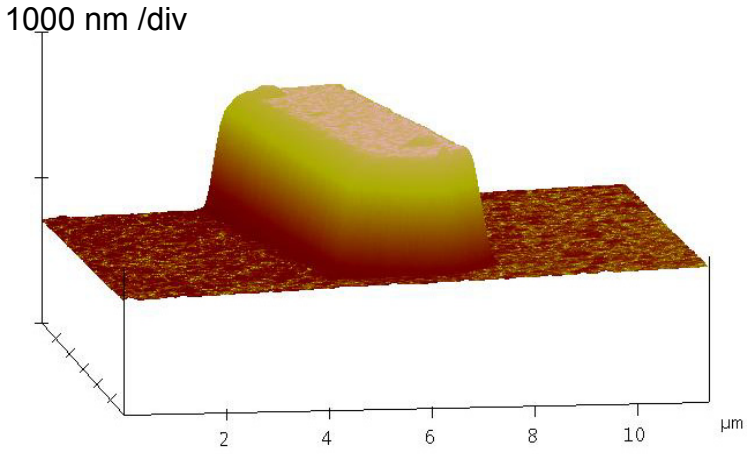


Figure 5.21 The AFM picture of the emitter stripe after complete hybrid etching. Vertical sidewall profile with smooth surface can be observed.

5.6 SHBTs processed with the optimised Hybrid etching process

5.6.1 Measurement Results for the Submicron HBTs

The emitter size dependent improvement of HBT performance is limited by the underetching problem by wet chemical etching. In order to investigate a possible further improvement with an emitter width smaller than 1 µm, dry etching is indispensable. In former section of chapter 5, a dry etching process has been developed for HBT processing. To elaborate the improvement with smaller dimensions, another quarter of M3231 sample has been processed. Since in standard processing optical lithography is used and it is not feasible to pattern submicron structures, here, the e-beam lithography has been preferred.

Different from M3231A, the emitter cap and emitter layers of M3231C have been etched with optimised ICP-RIE. In total, the emitter mesa thickness is 200 nm. Therefore the process time has been selected to 75 seconds for 150 nm etching. The remaining 50 nm have been etched with wet chemical etching as discussed in chapter 4.5. After accomplishing the hybrid-etching step, the further processing is performed in standard way.

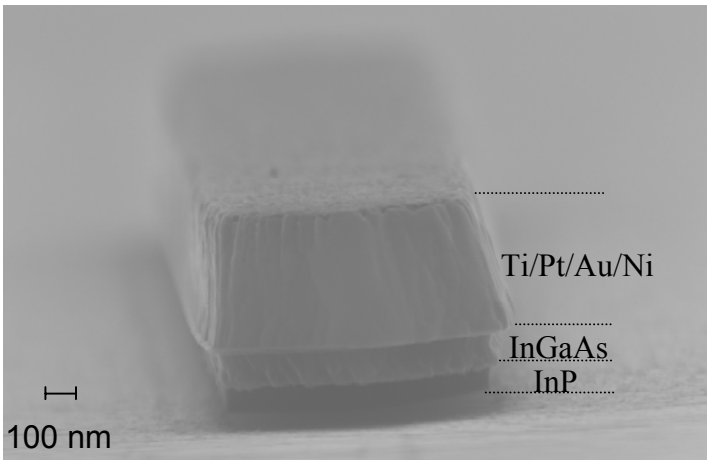


Figure 5.22 SEM micrograph of an emitter stripe on M3231C with 85 nm underetching and smooth surface after hybrid etching.

The SEM micrograph of the final HBT is shown in Figure 5.23.

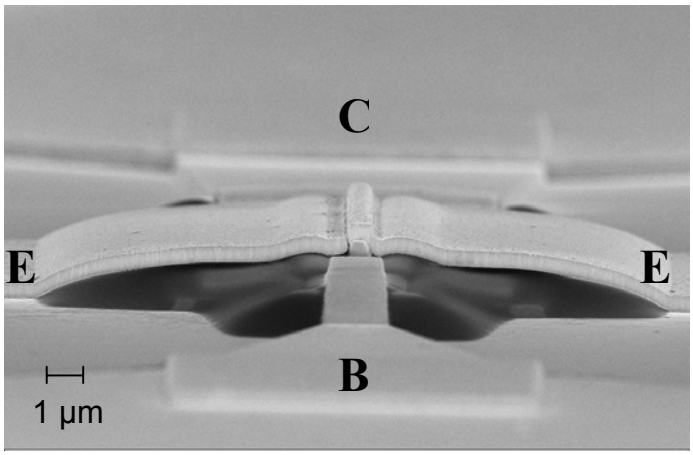


Figure 5.23 The SEM micrograph of 0.5x7.5 µm^2 HBT on M3231C

Dc measurements are performed on the 0.5x7.5 µm^2 devices and shown in Figure 5.24. The common emitter output characteristic has shown a dc current gain of 45, an offset-voltage of 0.25 V and turn-on voltage of 0.5 V.

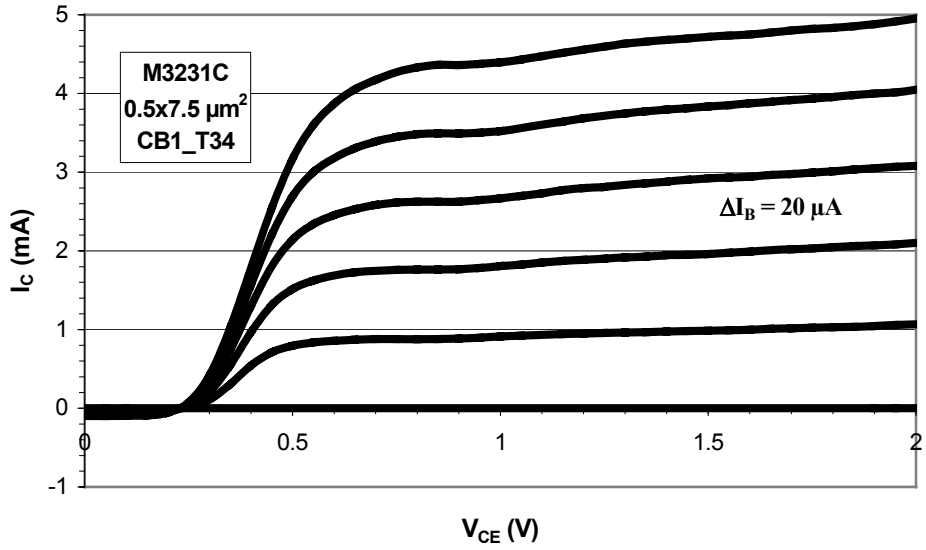


Figure 5.24 The common emitter output characteristic of 0.5x7.5 µm² device (M3231C)

For the same device, RF measurements are also performed. From the s-parameters, the intrinsic elements are extracted for this device. They are tabulated in Table 5.1

Table 5.1. Extracted intrinsic parameters for 0.5x7.5 µm² hybrid etched HBT

$A_{Emitter}$ (W_ExL_E)	Cjc	C_{fb}	C_{bc}	R_{bb}	R_{bb}xC_{bc}
0.5x7.5 µm²	0.06 fF	9.1 fF	9.16 fF	27 Ohm	274.4 fs

The calculated base resistance is 30.7 Ohm, which shows good agreement with the extracted one. In the work of Hafez [117], an SHBT with 0.35x12 µm² emitter area has shown a maximum oscillation frequency of 260 GHz and a cut-off frequency of 355 GHz. The extracted base collector capacitance is 16.5 fF and the extracted base resistance is 13 Ohm for this device.

As shown in Figure 5.25, the maximum oscillation frequency and the cut-off frequency are measured to be 370 GHz and 165 GHz, respectively.

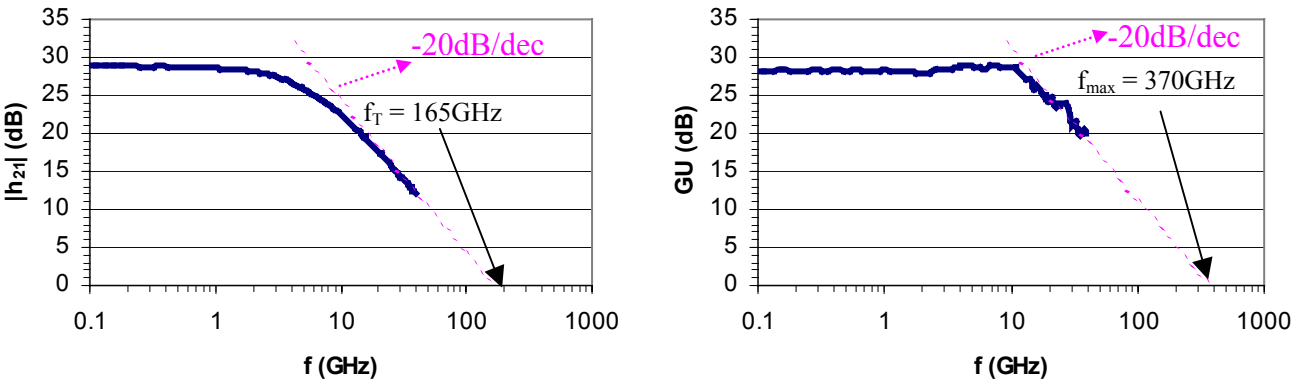


Figure 5.25. RF performance over $|h_{21}|$ and GU for self aligned 0.5x7.5 μm^2 device (M3231C) at 3mA/μm^2

It is observed that, the maximum current density has increased to 3 mA/μm^2, which was 1.2 mA/μm^2 for 1x15 μm^2 devices. This is attributed to the collector current spreading effect as briefly mentioned in chapter 2.3.

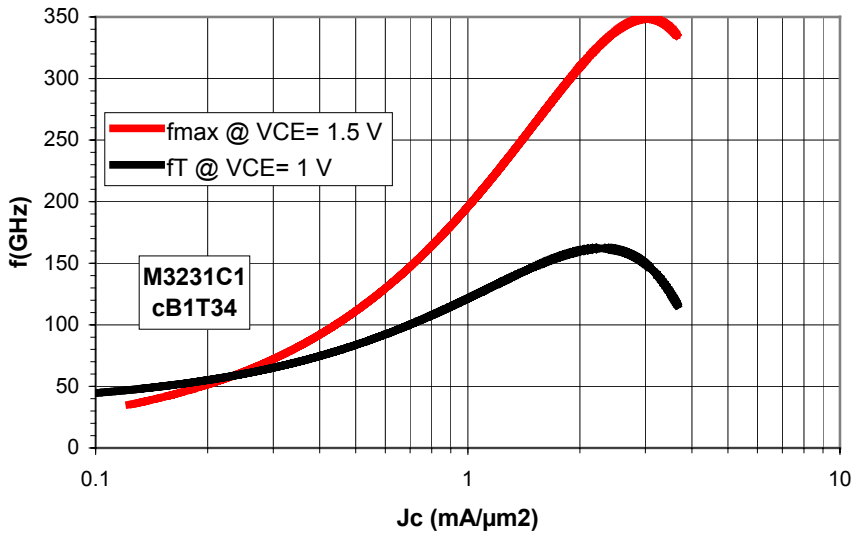


Figure 5.26 RF performance of self aligned 0.5x7.5 μm^2 device

5.6.2 Influence of the Emitter Etching on HBT's Uniformity

During the evaluation of solely wet chemically etched sample (M3231A), it has been observed that, on the different locations of the wafer, the dc and RF behaviour of the devices with same dimensions and layouts vary. To investigate this in detail, a

parallel process run has been performed. During this run, sample M3369, which is the reproduction of M3231, is used.

For the evaluation, 150 self aligned std 90°, 1x15 μm^2 devices have been patterned with e-beam lithography. The floorplan is given in Appendix I. Two parallel process runs have been performed. The emitter mesa etching of M3369d1a and M3369d1b have been realised with hybrid and solely wet chemical etching, respectively.

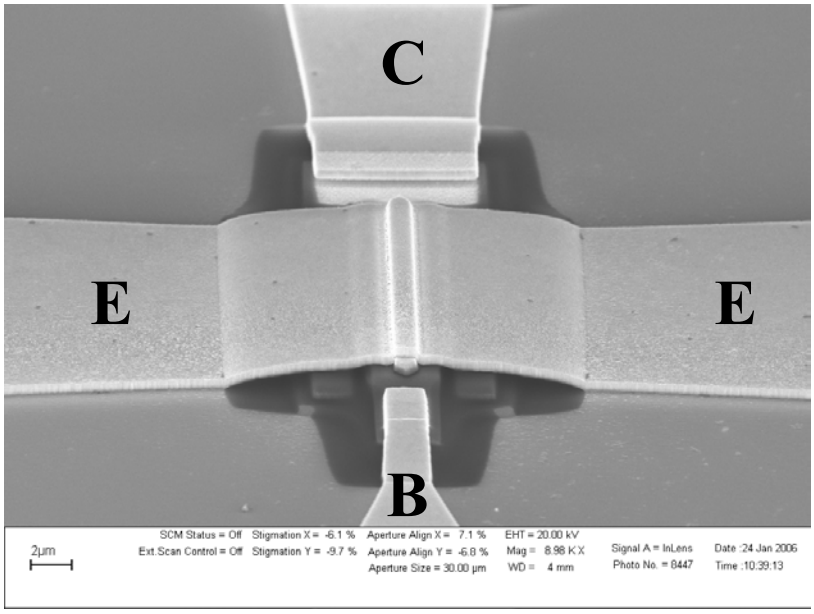


Figure 5.27 SEM micrograph of a self aligned 1x15µm² std 90° device (M3369d1a)

The further processing is identical and is realised in standard way, as applied for the other samples.

The dc characterizations have been performed for both samples. The typical yield is about 90 %. The sample M3369d1b has shown average dc current gain of 64 with a standard deviation of 5. On the other hand, the sample M3369d1a has presented average dc current gain of 41 with a standard deviation of 2. These values are comparable with literature [118]. For M3369d1a and M3369d1b, 20 HBTs are measured on the different part of the samples and the common emitter output characteristics are drawn by overlapping the results. The overlapped common emitter output characteristic for M3369d1b and M3369d1a are shown in Figure 5.28 and 5.29

respectively. The measurements for M3369d1a have shown similar curves in comparison to M3369d1b. This is because of the more uniform underetching of emitter with hybrid etching than solely wet chemical etching. Solely wet chemical etching results in different underetching on different part of the sample. From Figure 5.29, it has been investigated that, by hybrid etching, reliable devices can be achieved.

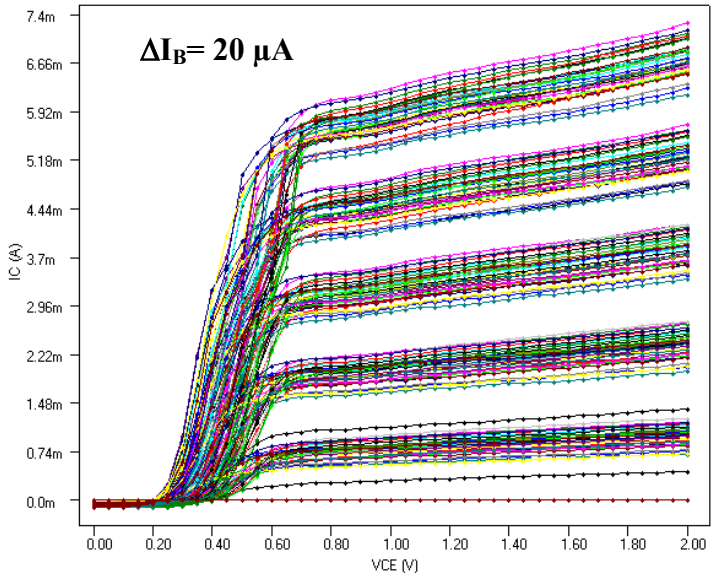


Figure 5.28 The common emitter output characteristics showing non-homogeneous behaviour for different devices on different parts of sample M3369d1b (solely wet chemically etched) (A_E = 1x15 µm^2)

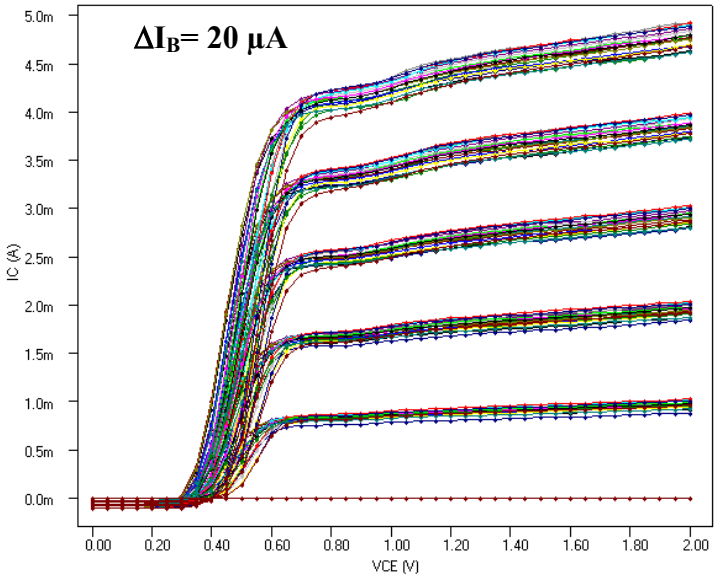


Figure 5.29 The common emitter output characteristics showing homogeneous behaviour for different devices on different parts of sample M3369d1a (hybrid etched) (A_E = 1x15 µm^2)

Even though, these samples have the same layer structure and device layout, significant difference with respect to the dc current gain is observed from for both samples. On the other hand, significant standard deviation in dc current gain is observed for solely wet chemically etched sample, M3369d1b. This is not the case for hybrid-etched sample, M3369d1a. The deviation over the whole M3369d1b is attributed to the different underetching for the different part of the sample. Since, during the wet chemical etching, the sample is dipped into the etchant, the etch rates for the bottom and the top of the sample become different. This is also proven by mapping. The devices close to the tweezers tip have shown lower dc current gain in comparison to the devices at the bottom. This is attributed to the bubbles occurring during the etching. These bubbles are moving up and blocking the etching towards to the top of the etchant. In figure 5.30 and 5.31, the histograms are presented for M3369d1b and M3369d1a, respectively.

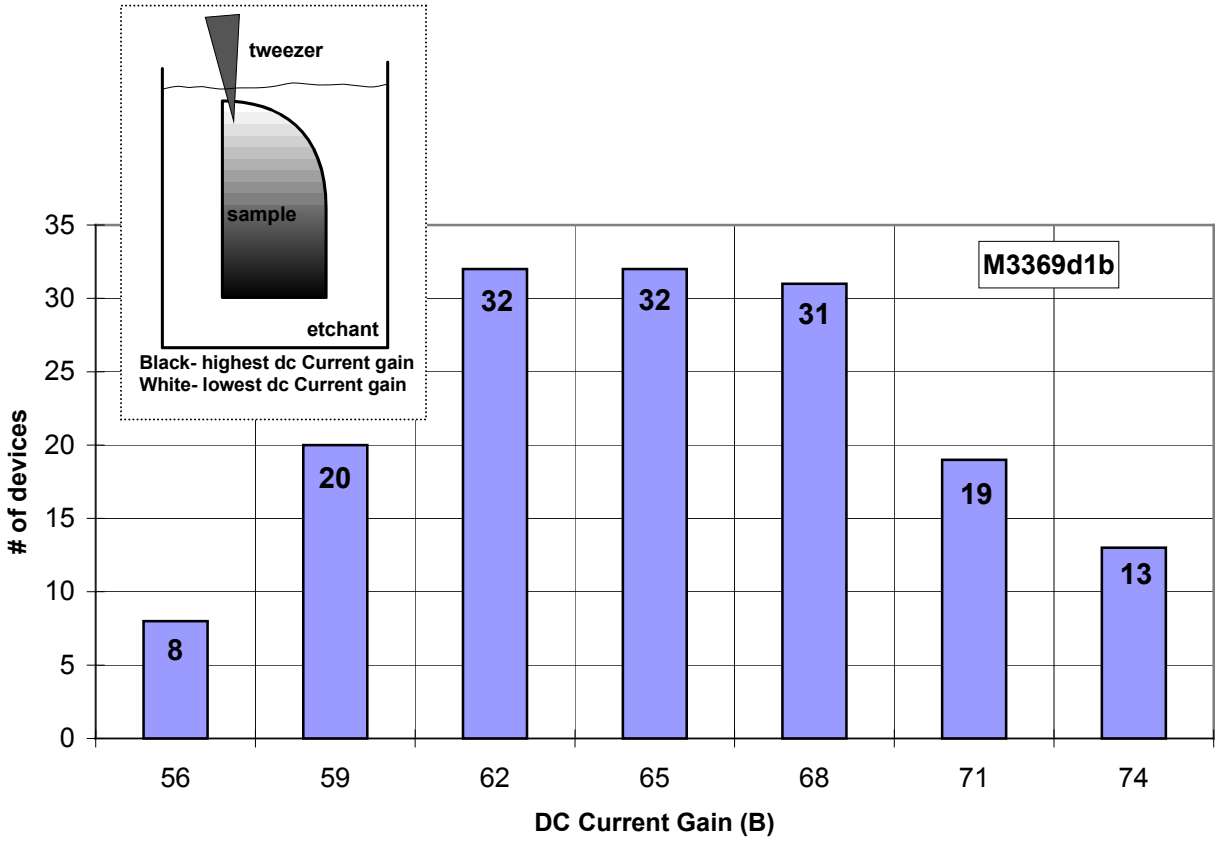


Figure 5.30 Histogram for dc current gain of devices on M3369d1b (solely wet chemically etched) showing significant deviation overall the wafer (A_E = 1x15 μm^2)

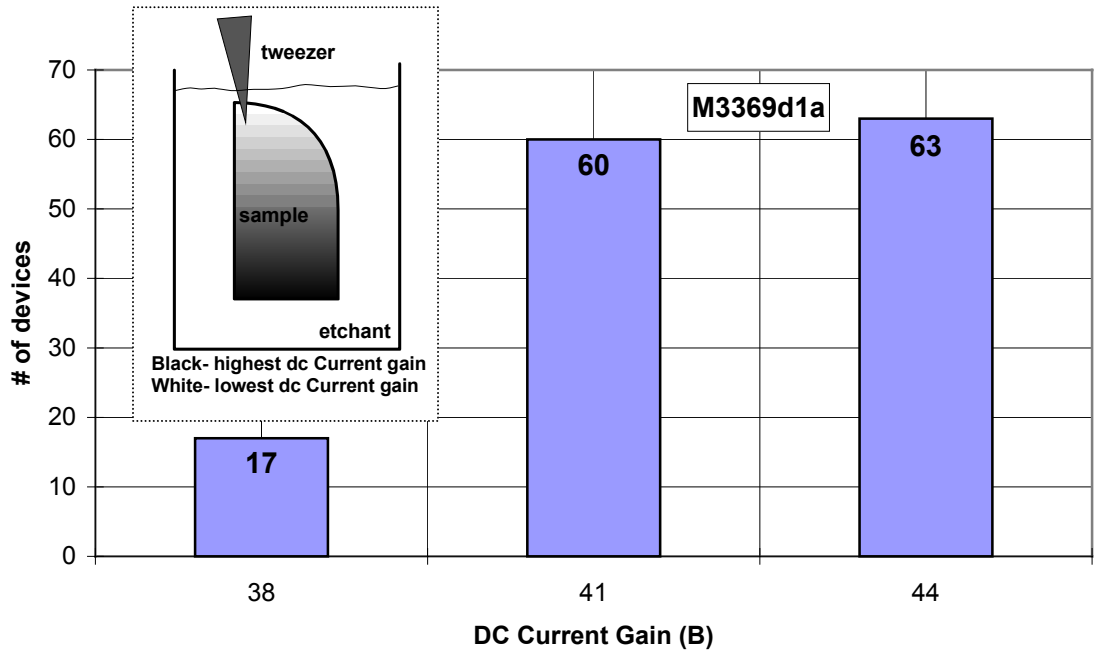


Figure 5.31 Histogram for dc current gain of devices on M3369d1a (hybrid etched) showing less deviation overall the wafer (A_E = 1x15 μm^2)

The difference in the dc current gain for hybrid etched and solely wet chemically etched samples is caused by the emitter–base contact spacing. When the spacing between the base and emitter contacts is less, the carriers injected from emitter flow laterally, too. When they flow laterally, they recombine underneath the base contact and this increases the interface recombination current $I_{B,cont}$. By increasing $I_{B,cont}$, the dc current gain degrades [119, 120, 121]. $I_{B,cont}$ is not only influenced by base-emitter spacing but also by the base doping level. The spacing of base and emitter are about 100 nm and 200 nm for M3369D1a and M3369D1b, respectively. Even though, the dc current gain degrades, since the base resistance is less for hybrid-etched samples, there is 20 GHz improvement in the maximum oscillation frequency.

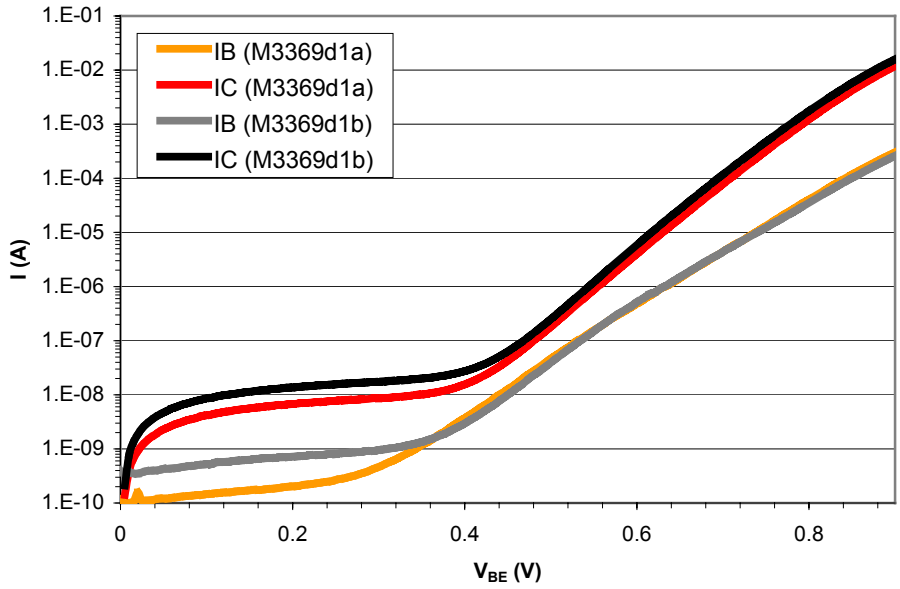


Figure 5.32 The Gummel Plot for M3369d1a and M3369d1b

With the Gummel Plot depicted in figure 5.32, the degradation in current gain is also investigated. For M3369d1a, n_b and n_c are calculated to be 1.56 and 1.23, respectively. For M3369d1b, these values are 1.44 and 1.21 for n_b and n_c, respectively. The slight degradation in the base ideality factor for hybrid etched sample, M3369d1a, is attributed to the increase in the interface recombination current, $I_{B,cont}$. Since there is no change on the base-collector junction, the collector ideality factor stays approximately the same.

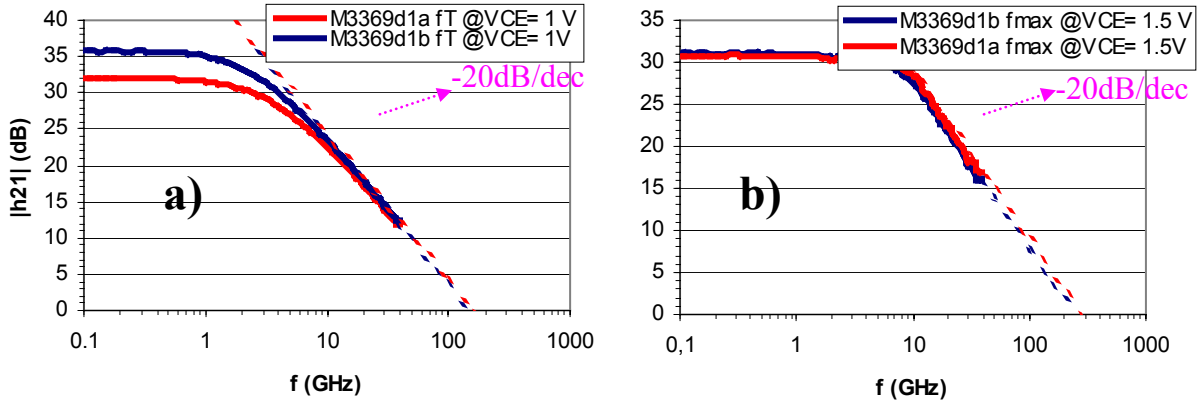


Figure 5.33 The comparison of RF performance for sample for M3369d1a and M3369d1b a) f_T b) f_{max} (A_E = 1x15 μm^2)

From the RF measurements of both samples, the cut off frequencies of 150 GHz and 160 GHz have been achieved as depicted in figure 5.33a, for M3369d1a and M3369d1b, respectively. Even though there is a slight degradation in f_T for hybrid-etched sample (M3369D1a) because of higher emitter area and higher base-emitter capacitance, there is an improvement in maximum oscillation frequency. The maximum oscillation frequency is measured to be 270 GHZ and 240 GHz for M3369d1b and M3369d1a as depicted in Figure 5.33b, respectively. About 10 % improvement in maximum oscillation frequency for hybrid-etched sample is attributed to the decrease in the emitter underetching resulting in reduction of the base resistance. As depicted in equation 2.11, base-emitter contact spacing is one of the key parameters affecting the total base resistance. The extracted parameters for M3369D1a and for M3369D1b have shown base resistances of 17.4 Ohm and 21.6 Ohm respectively. Calculation is performed to see the influence of underetching on the base resistance. They are summarised in table 5.2. These calculations are performed for device with $A_E = 1x15\ \mu m^2$.

Table 5.2. Calculated base resistance components for $A_E = 1x15\ \mu m^2$, with $R_{cont} = 4x10^{-7}$ Ohm·cm^2 and $R_{sh} = 1350$ Ohm/sq.

Type of Etching	**W_{EB} (nm)**	**$R_{b.\ cont}$ (Ohm)**	**$R_{b,\ spread}$ (Ohm)**	**R_{gap} (Ohm)**	**R_{bb} (Ohm)**
Solely Wet Chemical	170	7.90	7.70	7.85	23.45
Hybrid Etching	85	7.90	7.70	3.90	19.50

By halving the underetching of emitter, one can halve the base gap resistance R_{gap}. As a consequence, a 20 % decrease is achieved in the total base resistance R_{bb}. The calculated base resistances show a good agreement with the measured values.

6 Conclusion

By the advances in high frequency communication systems, and particularly Internet, wide bandwidth and high-speed transistors became key devices for the circuits. Indium Phosphide based Heterojunction Bipolar Transistors (InP HBTs) have the potential to provide high speed and high voltage for optoelectronic communication ICs. Moreover, since their energy band gap corresponds to the 1.3 and 1.55 μm wavelength, which are the wavelengths providing minimum optical loss in fibres, InP HBTs are the best choices for optical communication circuits. In this work, a process technology is developed for HBTs capable of 80 Gbit/s .

The first step of this work was a careful theoretical analysis showing that the main limitations for the device speed are the base-collector capacitances and base resistances. Various designs are elaborated to lower the according RC time constant. The influence of the emitter size is on RF performance is investigated. For optical lithography, it is found out that emitters with area of 1x15 μm^2 provides the best RF performance. Another important aspect is to lower any additional parasitic effects. Therefore directly contacted emitters are proposed to eliminate parasitic components caused by dummy pads and to dissipate the heat overall the emitter efficiently. Since the contact spacing between base and emitter plays an important role for base resistance, emitter contacts are patterned perpendicular to the major flat for low underetching. In addition to this, emitter mesa wet chemical etching process is optimised such that the underetching is reduced to 170 nm, which is sufficient to realize 1 μm width emitters. Finally, these results are used to design a mask set offering directly contacted emitters in a reliable process.

To reduce the base resistance, Pt/Ti/Pt/Au contact metal system providing $4x10^{-7}$ Ohm·cm^2 contact resistance, is used for the base layer.

Moreover, the current density is also an important aspect for the RF performance. The well-known Kirk Effect is analysed and the collector layer is doped to improve the maximum current density. $1x10^{17}$ cm^{-3} of collector doping density has doubled the maximum current density in comparison to the HBTs with non-intentionally doped collector layers. For HBTs with an emitter area of 1x15 μm^2 presented a maximum oscillation frequency (f_{max}) of 330 GHz and a cut-off frequency (f_T) of 170 GHz at 1.2 mA/μm^2.

The minimum width achievable by wet chemical etching is restricted to 1 μm. But on the other hand, for ultra high speed HBTs, submicron emitters are indispensable. Therefore, an ICP-RIE process with Cl_2/N_2 chemistry providing a submicron emitters due to less underetching is investigated. Dry etching processes offering etch rate in a wide range of 120 nm/min up to 1200 nm/min are developed. For HBTs, low etch rate, vertical sidewall profile, less damage to the surface are important aspects. An etch rate of 120 nm/min is sufficient for emitter mesa etching. Therefore, this process is elaborated in detail. A RMS surface roughness less than 5 nm, a ± 5 % uniformity over 2" wafer, and a ± 5 % run-to-run stability are achieved at this low etch rates.

Since the dry etching with this chemistry is not selective for InP and InGaAs, a hybrid etching process is sufficient to complete the emitter mesa etching. With this hybrid etching, the selectivity problem is solved with an emitter underetching of 85 nm, only. Submicron HBTs with emitter area of 0.5x7.5 μm^2 processed with hybrid etching, have shown a maximum oscillation frequency of 370 GHz and a cut-off frequency of 165 GHz.

Not only the RF performance but also the uniformity of the HBT properties is also an important aspect for circuit applications. Hybrid etching process offers better homogeneity in terms of etching in comparison to the solely wet chemical etching. The samples etched with wet chemical etching have shown dc current gain 42 with a

standard deviation of 2 where the solely etched ones have presented dc current gain of 64 with a standard deviation 5. The yield for both type of processing is more than 90 %.

As the final result of this work, layer structure and processing, InP HBTs with high speed, high yield and high uniformity are now ready for 80 Gbit/s communication circuits.

For further developments, The hybrid etching process may also be applied to the base-collector mesa etching. This will decrease the base collector area resulting into lower base-collector capacitance without degrading the base resistance. For a further improvement of the cut-off frequency, a thinner collector layers can be tried out lowering the space-charge transit time.

Appendix

APPENDIX A. Scattering Parameters relationships

s-parameters in terms of z-parameters	s-parameters in terms of z-parameters
$s_{11} = \frac{(z_{11}-1)(z_{22}+1)-z_{12}z_{21}}{(z_{11}+1)(z_{22}+1)-z_{12}z_{21}}$	$z_{11} = \frac{(1+s_{11})(1-s_{22})+s_{12}s_{21}}{(1-s_{11})(1-s_{22})-s_{12}s_{21}}$
$s_{12} = \frac{2z_{12}}{(z_{11}+1)(z_{22}+1)-z_{12}z_{21}}$	$z_{12} = \frac{2s_{12}}{(1-s_{11})(1-s_{22})-s_{12}s_{21}}$
$s_{21} = \frac{2z_{21}}{(z_{11}+1)(z_{22}+1)-z_{12}z_{21}}$	$z_{21} = \frac{2s_{21}}{(1-s_{11})(1-s_{22})-s_{12}s_{21}}$
$s_{22} = \frac{(z_{11}+1)(z_{22}-1)-z_{12}z_{21}}{(z_{11}+1)(z_{22}+1)-z_{12}z_{21}}$	$z_{22} = \frac{(1+s_{22})(1-s_{11})+s_{12}s_{21}}{(1-s_{11})(1-s_{22})-s_{12}s_{21}}$

s-parameters in terms of y-parameters	s-parameters in terms of y-parameters
$s_{11} = \frac{(1-y_{11})(1+y_{22})+y_{12}y_{21}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}}$	$y_{11} = \frac{(1+s_{22})(1-s_{11})+s_{12}s_{21}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}}$
$s_{12} = \frac{-2y_{12}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}}$	$y_{12} = \frac{-2s_{12}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}}$
$s_{21} = \frac{-2y_{21}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}}$	$y_{21} = \frac{-2s_{21}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}}$
$s_{22} = \frac{(1+y_{11})(1-y_{22})+y_{12}y_{21}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}}$	$y_{22} = \frac{(1+s_{11})(1-s_{22})+s_{12}s_{21}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}}$

s-parameters in terms of h-parameters	s-parameters in terms of h-parameters
$s_{11} = \frac{(h_{11}-1)(h_{22}+1)-h_{12}h_{21}}{(h_{11}+1)(h_{22}+1)-h_{12}h_{21}}$	$h_{11} = \frac{(1+s_{11})(1+s_{22})-s_{12}s_{21}}{(1-s_{11})(1+s_{22})+s_{12}s_{21}}$
$s_{12} = \frac{2h_{12}}{(h_{11}+1)(h_{22}+1)-h_{12}h_{21}}$	$h_{12} = \frac{2s_{12}}{(1-s_{11})(1+s_{22})+s_{12}s_{21}}$
$s_{21} = \frac{-2h_{21}}{(h_{11}+1)(h_{22}+1)-h_{12}h_{21}}$	$h_{21} = \frac{-2s_{21}}{(1-s_{11})(1+s_{22})+s_{12}s_{21}}$
$s_{22} = \frac{(1+h_{11})(1-h_{22})+h_{12}h_{21}}{(h_{11}+1)(h_{22}+1)-h_{12}h_{21}}$	$h_{22} = \frac{(1-s_{22})(1-s_{11})-s_{12}s_{21}}{(1-s_{11})(1+s_{22})+s_{12}s_{21}}$

APPENDIX B. The Transferred Substrate process

Focus of the work is to get a better understanding of the device performance with respect to parasitic and related consequences. With regard to literature, in most cases special bonding and soldering equipment is used to realise the transfer substrate process [20, 21, 22]. Also, applications have been demonstrated with Transferred substrate heterojunction Bipolar Transistors (TS-HBTs). Here, transferred-substrate process with regard to easy handling and simple process technology is developed. Therefore, only standard clean room equipment has been utilized to carry out the process.

With HBT03 mask set, it is possible to realise transferred substrate and standard (conventional) devices in parallel. This offers the opportunity to first measure standard devices from front and backside to evaluate the transfer process. After flipping the devices to the carrier, the backside collector metal for the special TS-HBT can be processed, and measurements can be performed at each etch step, before sub-collector, and before and after collector etching, to examine the influence of the fringing capacitances.

The proposed schematic of the process is depicted in Figure B1

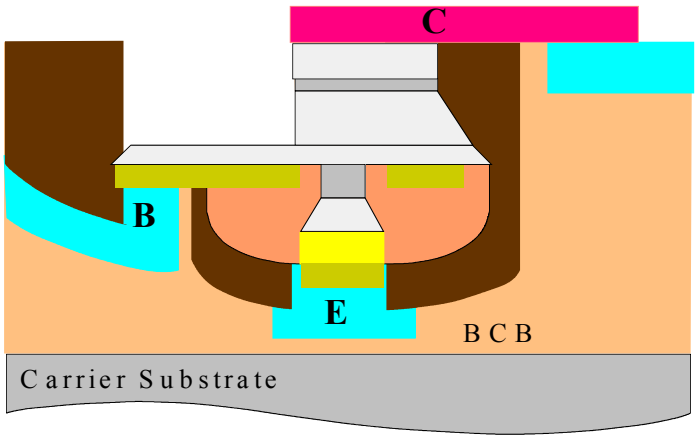


Figure B1. The schematic of the proposed TS-HBT structure

For this experiment, the layer structure depicted in table 2.3 is used.

Device fabrication is carried out like standard triple mesa HBT processing. The only difference is; the base mesa etching is carried out till the substrate and collector

metallization is omitted. Here on the substrate Pads metallization is performed and transfer process has started. Here, instead of using Ti/Au metal system for bonding pads, only Au is preferred. Because, Titanium (Ti) results in a contact problem with the RF probes. This is attributed to the oxidation of the Ti layer.

For the transfer process, mainly BCB (Benzo Cyclo Butene) [122] is used as glue material. BCB is resistant against acids (etching), cleaning steps (Acetone/IPA) and offers good mechanical properties. The only problem is; with BCB gas inclusions may occur. Several efforts are given to optimise the process without degrading the device performance and without having gas inclusions between carrier and the sample.

Figure B2. The optical microscope picture of the sample glued to the glass using BCB. Here, huge gas inclusions are observed

As it can be observed from Figure B2, with normal post bake and curing parameters, gas inclusions occur. These inclusions may be critical during backside substrate etching. To avoid these, post-bake time and temperature are adjusted in a way that the problem is minimized. Longer time (>24 hours) and lower temperature (<150°C) are used for the optimised post bake. The realised bonding with the optimised post-bake and curing parameters is shown in Figure B3. To be able to see the gas inclusions for these series of tests, glass is used as carrier instead of silicon wafer.

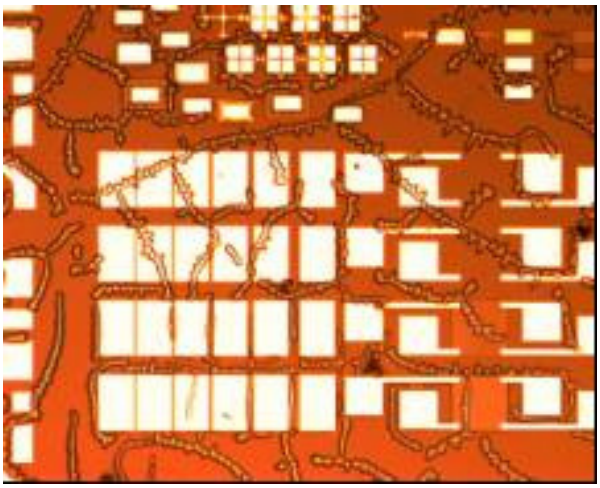


Figure B3. The optical microscope picture of the sample glued to the glass using BCB with optimised curing parameters. Here, less gas inclusions are observed.

After bonding the sample, the sticking property is also checked by applying force to the sample, and it is observed that with the optimised parameters, the sticking is sufficient for the TS process.

After transferring the substrate, the backside is lapped down approximately 300 µm to reduce the time of wet chemical etching and to achieve safer processing. The rest of the InP substrate is etched with pure HCl. During this etching, it has been observed that the position of the sample in the etchant affects the etching, and when it is kept vertically, the bottom side of the sample etched away faster than the top site. And this degrades the quality of the sample. To prevent this, the sample is kept in the etchant horizontally and it has been observed that etching is more homogeneous.

From the backside, the collector is defined solely with optical lithography. Directly after depositing the collector metal (Figure B4a), RF measurements have been performed to evaluate the effect of parasitic and fringing capacitances on device performance. Subcollector and collector layers are etched in two steps (Figure 4b). Therefore, after each etch step, further measurements are performed.

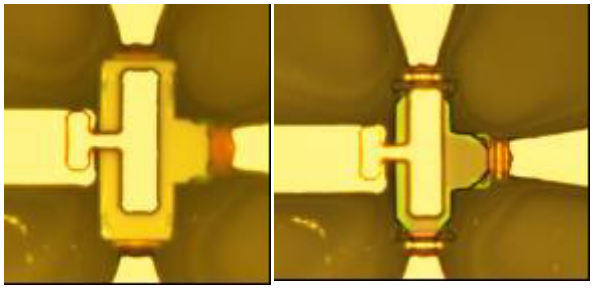


Figure B4. The optical microscope picture of the sample glued to the glass using BCB with optimised curing parameters. Here, less gas inclusions are observed.

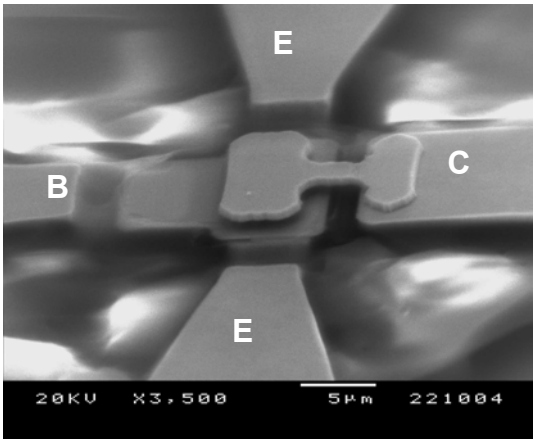
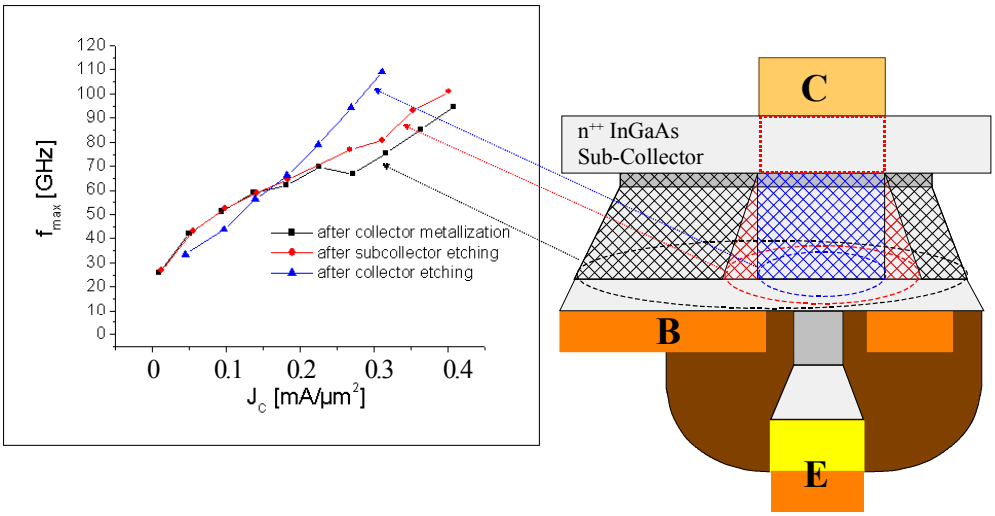


Figure B5. The optical microscope picture of the sample glued to the glass using BCB with optimised curing parameters. Here, less gas inclusions are observed.

The realised TS-HBT is measured in different steps after collector metal deposition aiming firstly at reducing the parasitic base collector capacitance C_{fb}, and secondly unavoidable fringing capacitances at the intrinsic C_{jc}.



A_E = 2x10 μm²; A_C = 3x12.5 μm²

Figure B6. The RF performance comparison of TS-HBT for different steps of etching

The best RF result achieved for A_E = 2x10 μm^2 and A_C = 3x12.5 μm^2 is f_{max} = 110 GHz and f_T = 70 GHz at J_C = 0.35 mA/μm^2. Normally for the mesa HBTs, the maximum values are achieved higher than 1 mA/μm^2. Here, the problem is the heat dissipation for the emitter contact. Normally for the mesa HBTs, the maximum values are achieved higher than 1 mA/μm^2. Here, the problem is the heat dissipation for the emitter contact.

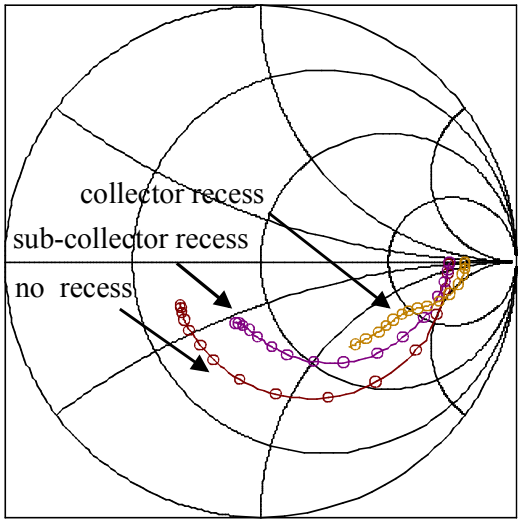


Figure B7. s_{22} for TS-HBT after different step of etching

From s-parameter results (Fig. B7), the reduction in the base-collector capacitance and increase in the collector resistance can be observed. By etching the sub-collector, the parasitic base collector capacitance (CCB) is reduced and slight deviation occurs after etching collector layer, which reduces the fringing capacitances.

A very simple and reliable method for transferring the substrate to a carrier has been developed in order to evaluate the intrinsic HBT performance potential. Up to now, the process is demonstrated on rather large devices with non-optimised layer structure. By realizing smaller emitter (even submicron emitters) and collector dimensions, high frequency performance can be improved. On the other hand, by optimising the epitaxial layer structures, like omitting the subcollector layer and realizing Schottky collector, better results can be achieved. Especially to improve the current density and therefore to achieve better RF performance, special methods can be applied to the emitter side for heat sinking as it is demonstrated in several publications.

APPENDIX C. The Early Process protocol

SAMPLE NAME

Cleaning	Ac-Pr H_2SO_4 1:1 20 sec
E-Ohm	AR-P 5350 5000/30/7000 15 min 95°C 5.5 sec exp. 1.5 min dev. 1:1
LH 560	100 Ti / 100 Pt / 3000 Au
Lift off	Ac-Pr
Annealing	30 sec 360 °C uni_du7
Etching	1 min 1:1:25 H_3PO_4 ; 5 sec HCl
B-Ohm	AR-P 5350 5000/30/7000 15 min 95°C 5.5 sec exp. 1.5 min dev. 1:1
LH 560	100 Ti / 100 Pt / 800 Au
Lift off	Ac-Pr
Annealing	30 sec 360 °C uni_du7
B-Mesa	H_2SO_4 1:1 20 sec AR-P 374 3000/30/3000 10 min 95°C 12 sec exp. B2 Mesa 60 sec dev. 45 min 120°C
Etching	120 sec 1:1:25 H_3PO_4
Lift off	Ac-Pr

C-Ohm	AR-P 5350 5000/30/7000 15 min 95°C 5.5 sec exp. 1.5 min dev. 1:1
LH 560	100 Ti / 100 Pt / 3000 Au
Lift off	Ac-Pr
C-Mesa 1	H_2SO_4 1:1 20 secs AR-P 3740 3000/30/3000 10 min 95°C 12 sec exp. 60 sec dev. 45 min 120°C
Ätzen	2 min 1:1:25 H_3PO_4
Lift off	Ac-Pr
C-Mesa 2	H_2SO_4 1:1 20 secs AR-P 3740 3000/30/3000 10 min 95°C 12 sec exp. 60 sec dev. 45 min 120°C
Ätzen	2 min 1:1:25 H_3PO_4 5 sec HCl conc.
Lift off	Ac-Pr
Brücken pure	AR-P 3740 3000/30/3000 10 min 120°C HP,15 sec.s exp. 1 1/2 min dev. 30 min 140°C HP AR-P 5350 3000/30/3000 10 min 95°C 10 sec exp. 2 min dev. 3:2 O_2-Plasma 2 min 25 W
LH 560	200 Ti / 4000 Au / 4000 Au
Lift off	DMF-Ac-Pr

APPENDIX D. The Early Mask Set (HBT97)

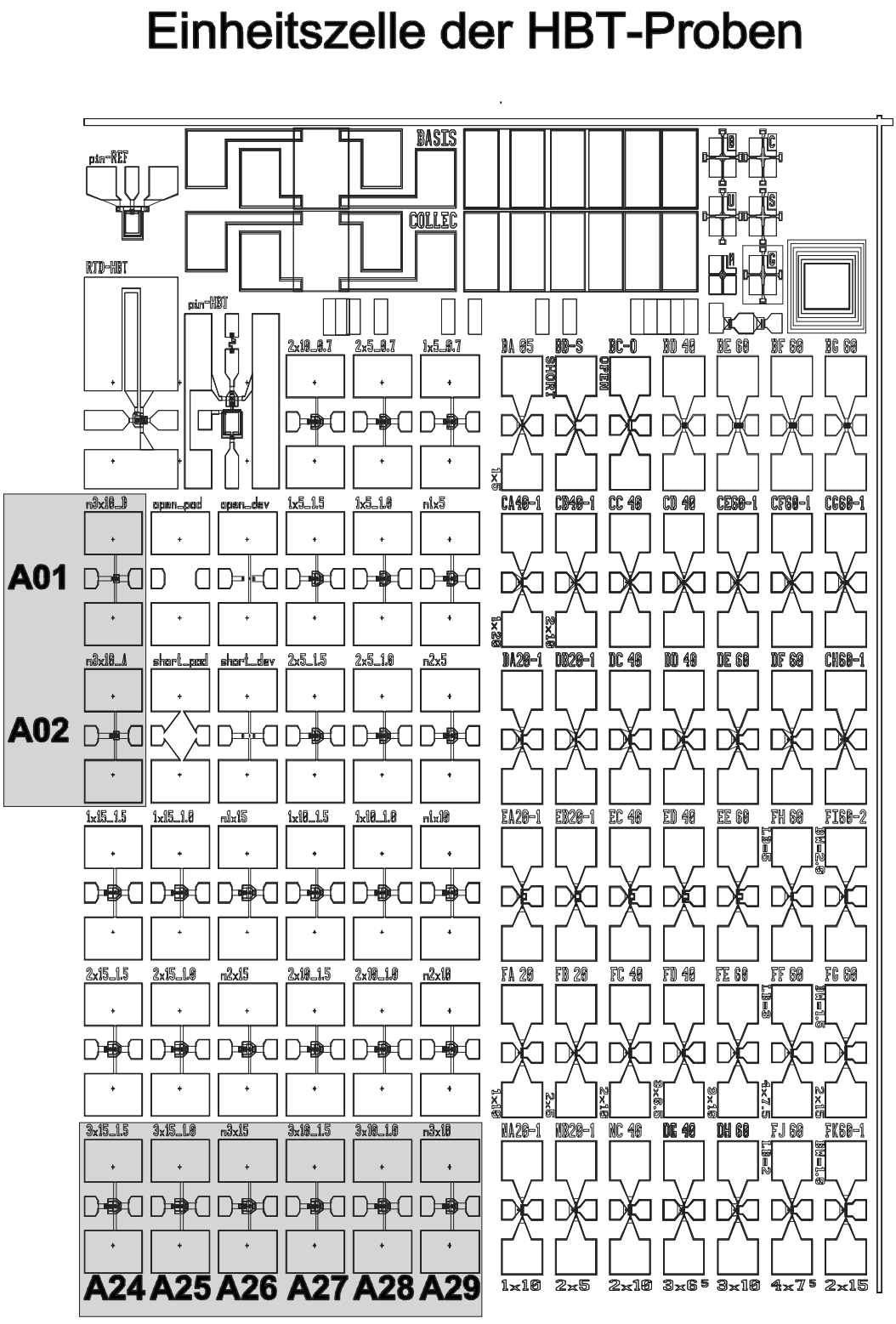


Figure D. The lay out for the mask set used in the early processing (HBT97-mask). On this mask there are 30 different standard HBT structures with different design and dimensions

APPENDIX E. The developed mask Set (HBT03)

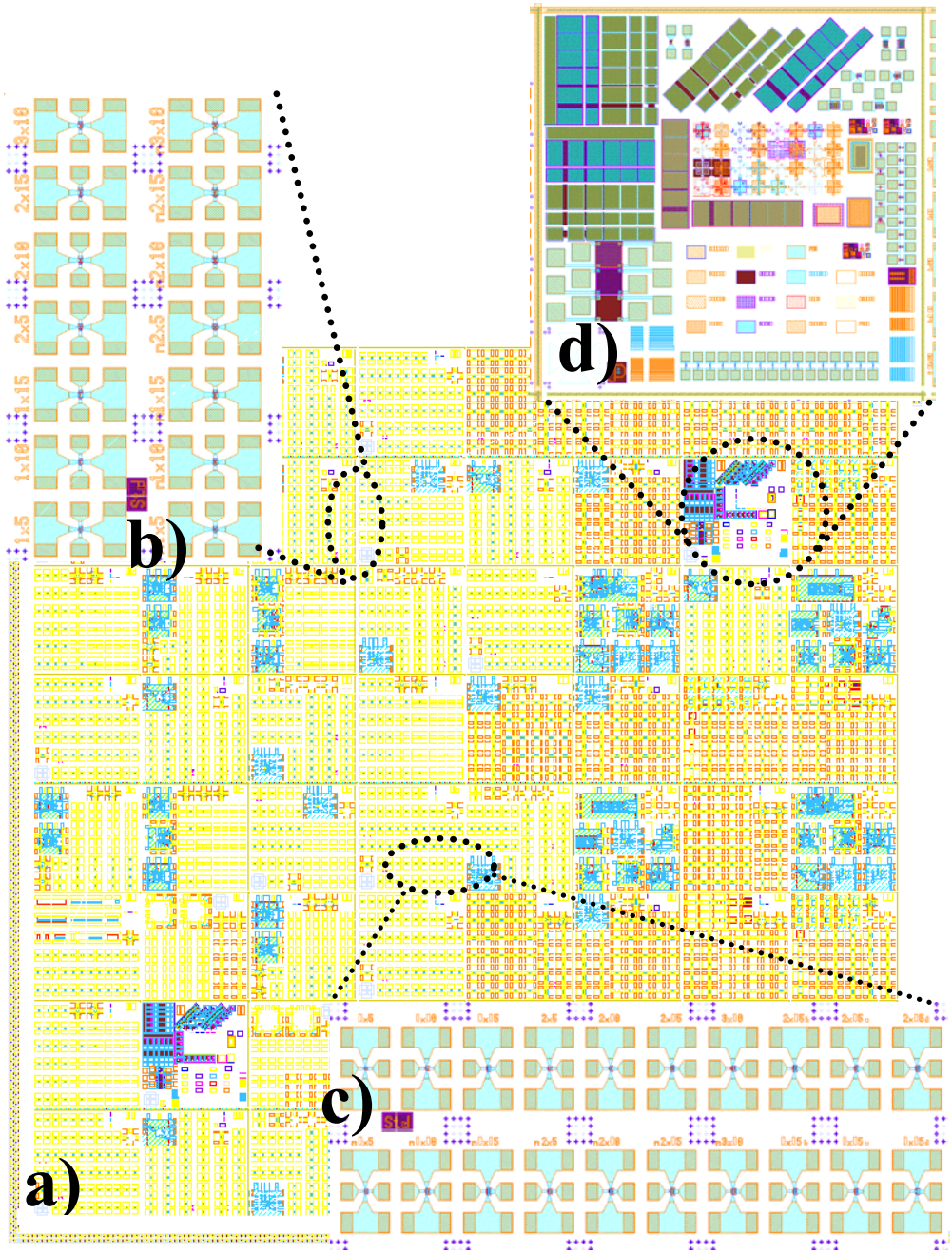


Figure E. The layout for the mask developed during this work

a) The complete floor plan for the mask set used in the optimised processing

b) The zoomed in std 90° HBT cell. There are 14 devices with different dimensions and base contacts

c) The zoomed in std HBT cell. There are 20 devices with different dimensions and base contacts

d) The zoomed in PCM cell

APPENDIX F. The layer structures of the HBTs

The HBTs in this work are named with their successive growth numbers starting with "M1234(ABCD)", where "M" denotes MOVPE growth and "1234" is the growth number. ABCD stands for the one quarter of a sample.

M2817

Emitter-cap	n++ InGaAs	1E19cm-3	100nm
Emitter	n+ InP	2E17cm-3	50nm
Base	p++ InGaAs	3E19cm-3	50nm
Collector	n- InGaAs	nid	300nm
Stop Etch	InP		10nm
Subcollector	n++ InGaAs	8E18cm-3	300nm
Buffer	InP		50nm
S.I InP Substrate			

M3231

Emitter-cap	n++ InGaAs	1E19cm-3	100nm
Emitter contact	n++ InP	1E19cm-3	50nm
Emitter	n+ InP	2E17cm-3	50nm
Base	p++ InGaAs	3E19cm-3	50nm
Collector	n- InGaAs	1E17cm-3	600nm
Stop Etch	InP		10nm
Subcollector	n++ InGaAs	8E18cm-3	300nm
Buffer	InP		50nm
S.I InP Substrate			

M3312

Emitter-cap	n++ InGaAs	1E19cm-3	100nm
Emitter contact	n++ InP	1E19cm-3	50nm
Emitter	n+ InP	2E17cm-3	50nm
Base	p++ InGaAs	3E19cm-3	50nm
Collector	n- InGaAs	nid	600nm
Stop Etch	InP		10nm
Subcollector	n++ InGaAs	8E18cm-3	300nm
Buffer	InP		50nm
S.I InP Substrate			

M3391

Emitter-cap	n++ InGaAs	1E19cm-3	100nm
Emitter contact	n++ InP	1E19cm-3	50nm
Emitter	n+ InP	2E17cm-3	50nm
Base	p++ InGaAs	3E19cm-3	50nm
Collector	n- InGaAs	1E17cm-3	300nm
Stop Etch	InP		10nm
Subcollector	n++ InGaAs	8E18cm-3	300nm
Buffer	InP		50nm
S.I InP Substrate			

M3181

Emitter-cap	n++ InGaAs	3E19cm-3	50nm
Emitter-cont	n++ InP	2E19cm-3	50nm
Emitter	n InP	5E17cm-3	50nm
Base	p++ InGaAs	3E19cm-3	50nm
Spacer	InGaAs		30nm
Quaternary	InGaAsP (0.81eV)		20nm
Quaternary	InGaAsP (0.95eV)		10nm
Collector	n- InP	5E17cm-3	100nm
Collector cont	n++ InP	1E19cm-3	100nm
Subcollector	n++ InGaAs	1E19cm-3	200nm
Buffer	InP		50nm
S.I InP Substrate			

M3190

Emitter-cap	n++ InGaAs	3E19cm-3	50nm
Emitter-cont	n++ InP	2E19cm-3	50nm
Emitter	n InP	5E17cm-3	50nm
Base	p++ InGaAs	3E19cm-3	50nm
Spacer	InGaAs		30nm
Quaternary	InGaAsP (0.81eV)		20nm
Quaternary	InGaAsP (0.95eV)		10nm
Collector	n- InP	5E16cm-3	100nm
collector cont	n++ InP	1E19cm-3	100nm
Subcollector	n++ InGaAs	1E19cm-3	200nm
Buffer	InP		50nm
S.I InP Substrate			

M3191

Emitter-cap	n++ InGaAs	3E19cm-3	50nm
Emitter-cont	n++ InP	2E19cm-3	50nm
Emitter	n InP	5E17cm-3	50nm
Base	p++ InGaAs	3E19cm-3	50nm
Spacer	InGaAs		30nm
Quaternary	InGaAsP (0.81eV)		20nm
Quaternary	InGaAsP (0.95eV)		10nm
Collector	n- InP	nid	100nm
Collector cont	n++ InP	1E19cm-3	100nm
Subcollector	n++ InGaAs	1E19cm-3	200nm
Buffer	InP		50nm
S.I InP Substrate			

M2747

Emitter-cap	n++ InGaAs	1E19cm-3	100nm
Emitter	n+ InP	2E17cm-3	60nm
Base	p++ GaAsSb	4/8E19cm-3	50nm
Collector	n- InP	nid	300nm
Subcollector	n++ InGaAs	8E18cm-3	300nm
Buffer	InP		50nm
S.I InP Substrate			

M3273

Emitter-cap	n++ InGaAs	1E19cm-3	100nm
Emitter	n+ InP	2E17cm-3	60nm
Base	p++ GaAsSb	8E19cm-3	40nm
Collector	n-InP	nid	300nm
Subcollector	n++ InP	1E19cm-3	150nm
Buffer	InP		50nm
S.I InP Substrate			

M3354

Emitter-cap	n++ InGaAs	1E19cm-3	100nm
Emitter	n+ InP	2E17cm-3	60nm
Base	p++ GaAsSb	6E19cm-3	40nm
Collector	n-InP	nid	300nm
Subcollector	n++ InP	1E19cm-3	150nm
Buffer	InP		50nm
S.I InP Substrate			

APPENDIX G. The Optimised Process Protocol

Date :

SHBT (std layer structure)

n+ InGaAs	**E-cap**	**100nm**
n InP	**E**	**100nm**
p InGaAs	**B**	**50nm**
InGaAs	**C**	**600nm**
InP	**Stop etch**	**10 nm**
n+ InGaAs	**Sub-C**	**300nm**
InP	**Buffer**	**41nm**
s.i. InP Substrate		

Objective :

Mask Set : HBT03

Processed by **:**

Cleaning Ac-Pr (hot)

Oxide Removal 20sec.s HCl 1:4
60sec.s DI, N_2 Drying

Control Optical; *Comments:*

<u>Emitter Metal</u>

Oxide Removal 20sec.s HCl 1:4
60sec.s DI, N_2 Drying

Control Optical; *Comments:*

E-Ohm Maske: emCon
ArP 5350 5000/30/7000 (Prog.5)
15 min 95°C HP, 6.5 sec bel, 1.5 min. ent. 1:1
DI Wasser, N_2 Drying

Control Optical; *Comments:*

O_2 Plasma 1min. 25W O_2 Plasma

Oxide Removal 20sec.s NH_3 1:10
N_2 Drying

Metallization Ti/Pt/Au 10/10/400 [nm]

Lift-off Ac-Pr

Control Optical; *Comments:*

Dektak …. ...../...../.....nm ➔……..nm should be:~420nm

<u>Emitter Mesa</u>

Etching 40sec.s H_3PO_4:H_2O_2:H_2O 1:1:25 (+15sec.s after colour change)
60sec.s DI Water, N_2 Drying

Dektak …. ...../...../.....nm ➔……..nm should be:~100nm

Etching 35sec.s 1:1 H_2O:HCl
60sec.s DI Water, N_2 Drying

Dektak …. ...../...../.....nm ➔……..nm should be:~100nm

Control Optical; *Comments:*

<u>Base Metal</u>

B-Ohm Maske: bsCon
ArP 5350 5000/30/7000 (Prog.5)
15 min 95°C HP, 6.5 sec bel, 1.5 min. ent. 1:1
DI Wasser, N_2 Drying

Control Optical; *Comments:*

O_2 Plasma 1min. 25W O_2 Plasma

Oxide Removal 20sec.s NH_3 1:10
N_2 Drying

Metallization Pt/Ti/Pt/Au 2/10/10/110 [nm]

Lift-off Ac-Pr

Control Optical; *Comments:*

<u>Base Mesa+Durimide Isolation</u>

Oxide removal 20sec.s HCl 1:4
60sec.s DI, N_2 Drying

Control Optical; *Comments:*

Base Mesa Maske bsMesa
Durimide 1:1 1000/150/5000 (Prog 8 E-Beam)
3min 95°C HP, 40sec. exp.

Conditioning 30mins room temp

Developing 30" HTRD2; 30" RER600
N2 Drying

Plasma Ashing 8mins 50W O2 Plasma
Control:
3mins 50W O2 Plasma
Control:

Curing >2h 200 C Dry Oven
5'250C, 5'300C RTA (IPAG_Iso1)

Control Optical; *Comments:*

Dektak …. **...../...../.....nm ➔…….nm** should be:~130nm

Etching 250 sec.s H_3PO_4:H_2O_2:H_2O 1:1:25
60sec.s DI Water, N_2 Drying

Dektak …. **...../...../.....nm ➔…….nm** should be:~645 nm

Etching 10sec.s 1:1 H_2O:HCl
60sec.s DI Water, N_2 Drying

Dektak …. **...../...../.....nm ➔…….nm** should be:~10nm

Control Optical; *Comments:*

<u>Collector Mesa</u>

Oxide Removal 20sec.s HCl 1:4
60sec.s DI, N_2 Drying

Control Optical; *Comments:*

C-Mesa Maske: coMesa
ArP 3740 3000/30/3000
10 min 95°C HP, 13sec bel, 1 min. pure
DI Wasser, N_2 Drying

O_2 Plasma 2min. 25W O_2 Plasma

Post Bake 45min.s 120C HP

Control Optical; *Comments:*

Etching 120 sec.s H_3PO_4:H_2O_2:H_2O 1:1:25
60sec.s DI Water, N_2 Drying

Dektak …. **...../...../.....nm ➔……..nm** should be:~300 nm

Etching 30sec.s 1:1 H2O: HCl
60 sec.s DI Water, N_2 Drying

Dektak …. **...../...../.....nm ➔……..nm** should be >70nm

Control Optical; *Comments:*

Lift-Off Ac-Pr

<u>Collector Metal</u>

C-Ohm Maske: coCon
ArP 5350 3000/30/3000 (Prog.1)
10 min 95°C HP, 9 sec bel, 60secs. dev. 1 :1
DI Wasser, N_2 Drying

Control Optical; *Comments:*

O_2 Plasma 1min. 25W O_2 Plasma

Oxide removal 20sec.s NH_3 1:10
N_2 Drying

Metallization Ti/Pt/Au 10/10/300 [nm]
Lift-off Ac-Pr

Control Optical; *Comments:*

<u>Airbridge ISO</u>

Oxide removal 20sec.s HCl 1:4
60sec.s DI, N_2 Drying

Control	Optical;	*Comments:*

ISO	Maske: iIso ArP 3740 3000/30/3000 10 min 120°C HP, 13sec bel, 1 min. pure dev. DI Wasser, N_2 Drying
Hard Bake	30min.140°C

Control	Optical;	*Comments:*

<u>Airbridge Metal</u>

AirBridge Metal	Maske: iMetal2+Pads ArP 5350 3000/30/3000 10 min 95°C HP, 9 sec bel, 60secs ent. 1:1 DI Wasser, N_2 Drying

Control	Optical;	*Comments:*

O_2 Plasma	2min. 25W O_2 Plasma
Oxide Removal	20sec.s NH_3 1:10 N_2 Drying
Metallization	Ti/Au/Au 10/400/400 [nm]
Lift-off	Ac-Pr

APPENDIX H. The ICP-RIE System

Figure H1. The front view of the Oxford PlasmaLab System 100 ICP65 System

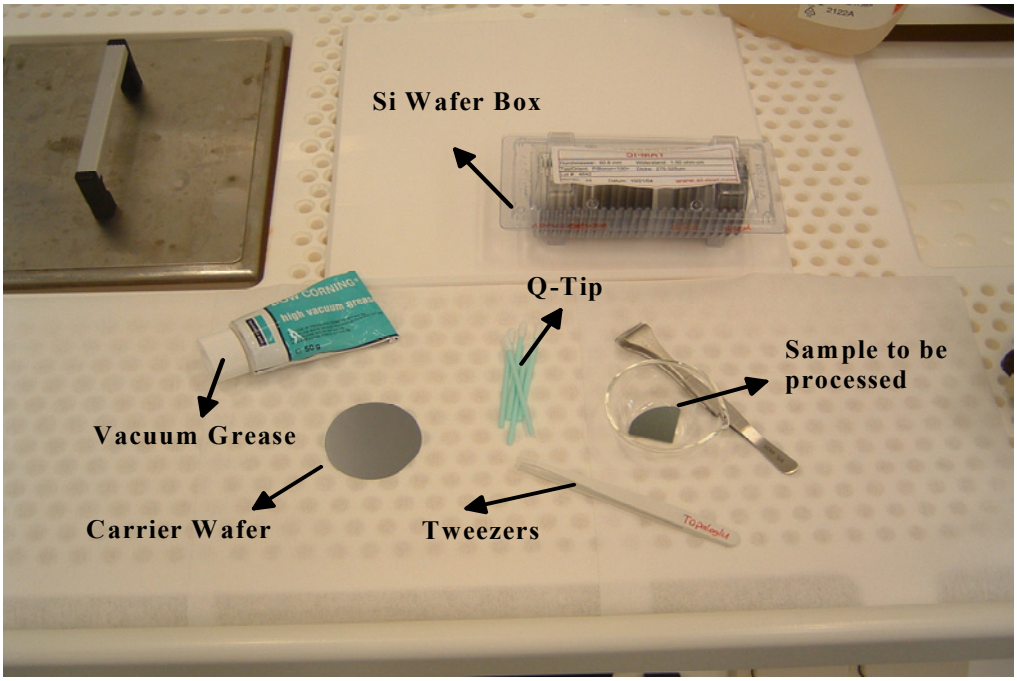


Figure H2. The materials used to fix (glue) the wafer on the carrier substrate. In this case Dow Corning High Vacuum grease is used as glue material and Silicon has been preferred as carrier

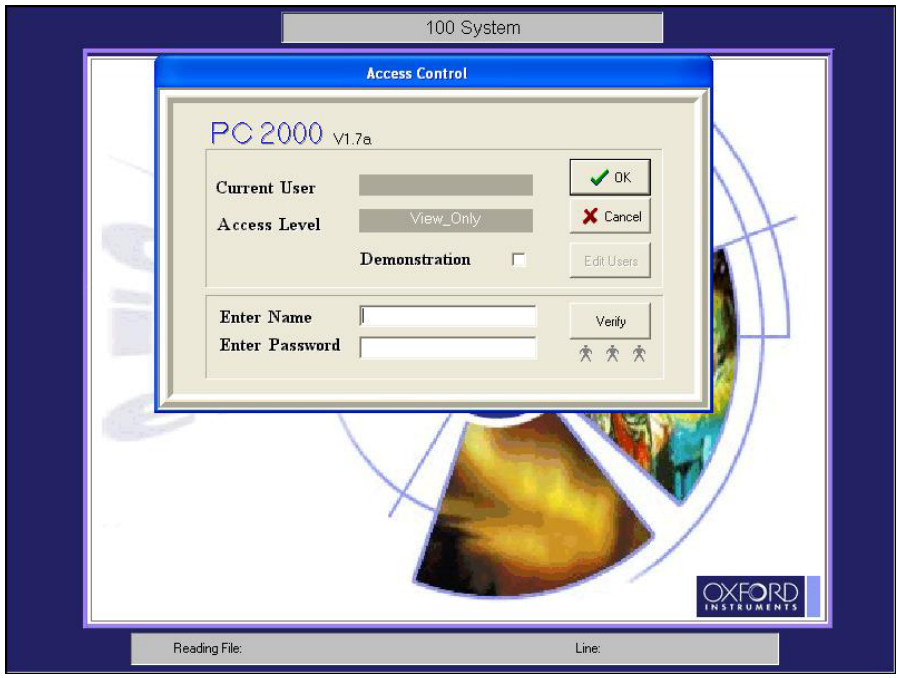


Figure H3. The Access control page view of the PC2000 software. This screen is asking for user names and related password. According to the defined user, access is possible with different levels

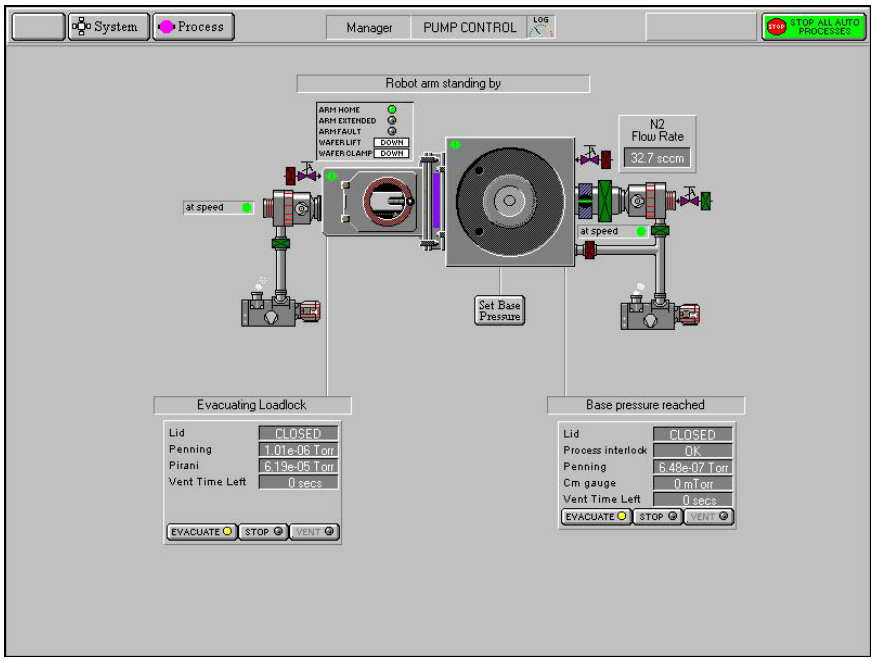


Figure H4. The pump control page view of the PC2000 software. This mimic shows the position of the valves and functionality of the pumps (pre-pumps and turbo pumps for both chambers). Here, load lock and chamber is also visible.

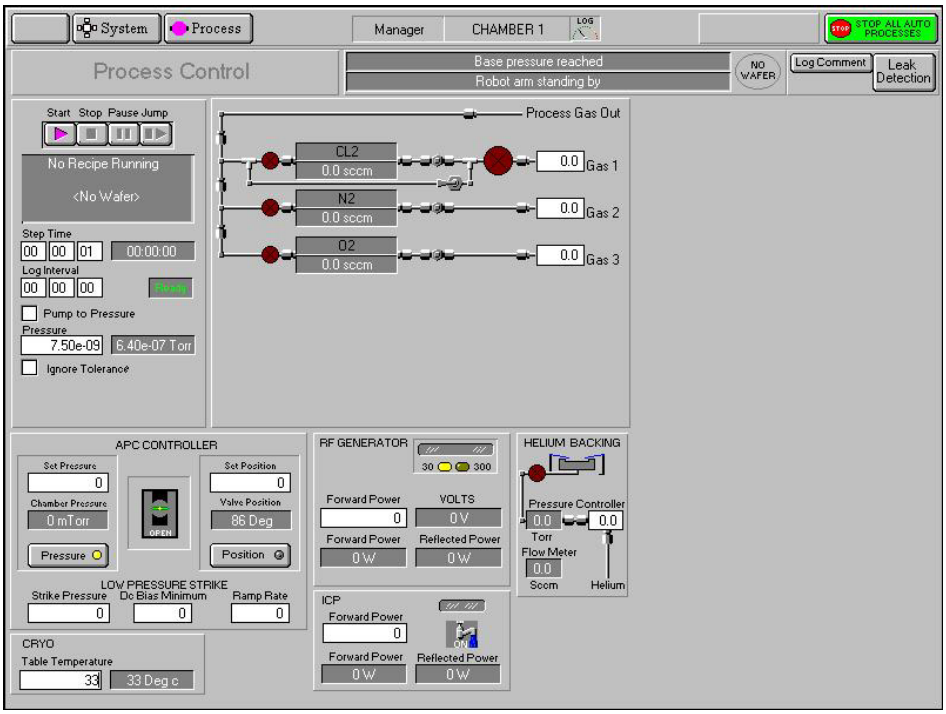


Figure H5. The process control page view of the PC2000 software. All process parameters like temperature, gas flow, pressure, power, process time can be controlled here. The He back cooling is also controlled here. During the process, these parameters are reflected to the screen real-time.

APPENDIX I. The E-Beam layout

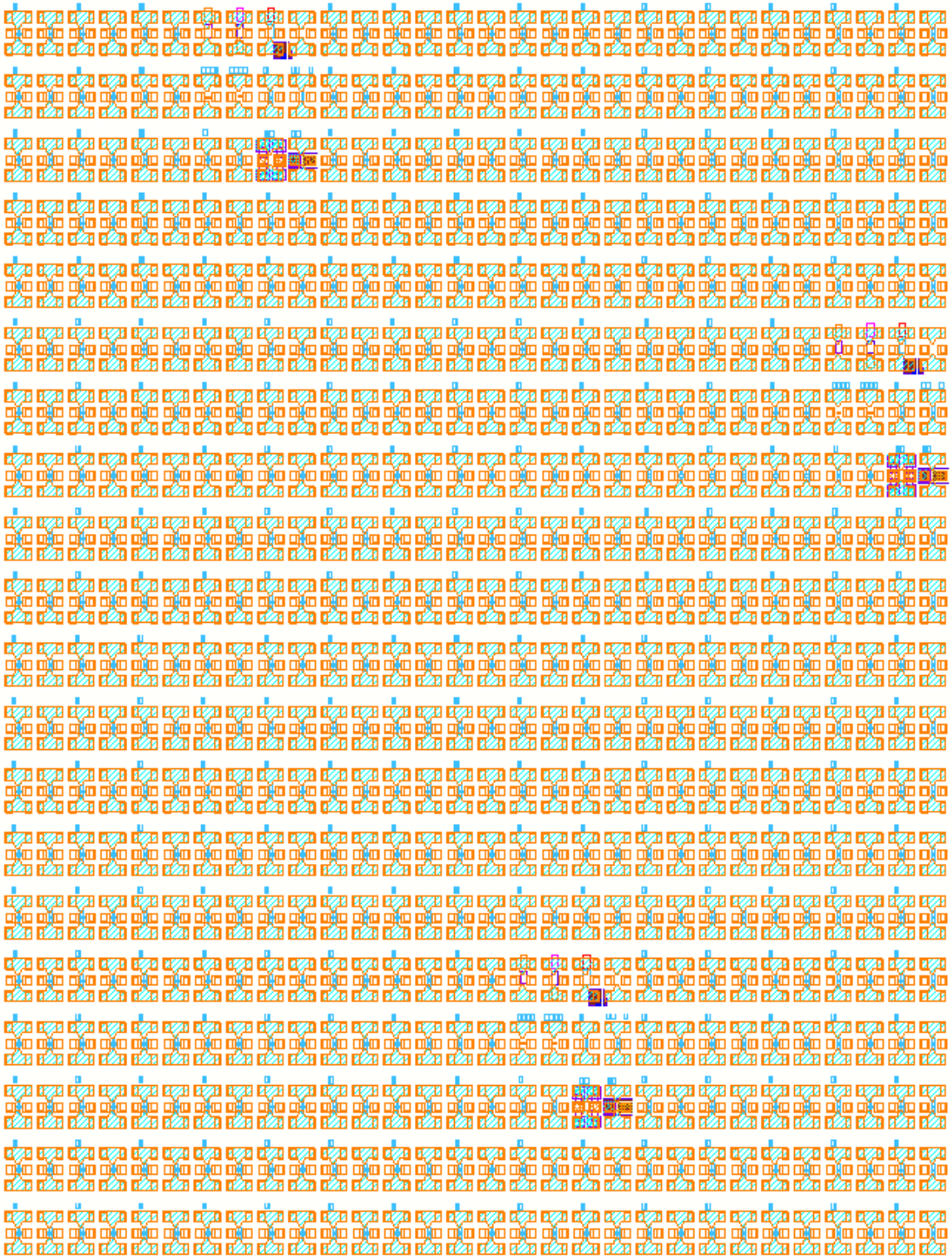


Figure I. The e-beam layout used to process M3369D1a and M3369D1b (hybrid etching and solely wet chemical etching, respectively). There are 12 cells containing 1x15 and 2x10 µm2.

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Acknowledgements

I am really grateful to many people. Last three and a half years at Solid State Electronics Department of University Duisburg Essen were unforgettable for me. Now, I have the chance to thank people, who has helped, guided and/or assisted me throughout the work.

First of all, I would like to thank my supervisor Prof. Dr. rer. nat. Franz Josef Tegude for giving me the chance to explore the world of solid-state electronics and guiding me during the development of this work. It was really pleasure for me to work with him. I am indebted to him for giving me freedom to realise my ideas.

I would like to thank Prof. Dr. rer. nat. Dieter Jäger for being co-referent of this work.

I would like to thank Dr. Werner Prost and the incredible cupboard in his room. He was always open to “two minutes” discussions. Moreover, I would like to thank him also for helping me especially during the correction phase of the work.

I am also thankful to Dr. Satoshi Taniguchi and Hideki Ono from Sony Corporation Semiconductor Development technology Group for the SIMS measurements.

I am also grateful to the all members of Oxford Instruments Plasma technology. Special thanks to Dr. Mark Dineen for supporting me about ICP-RIE etching and giving me some hints.

I am also grateful to Prof. Dr. Colombo Bolognesi and Prof Dr. Simon Watkins from Simon Fraser University and Dr. Emilio Gini from ETH Zurich, for the discussions especially about GaAsSb DHBTs. They were always open to the discussions.

I would like to express my sincere gratitude to all existing and former members of HLT for their constant help and support throughout my study. Here, we go:

Special thanks to Dr. Brockerhoff for encouraging me about my work and for organizing such fascinating social events. His ideas have always motivated me.

I would like to thank Jörn Driesen- *the CADENCE master*-, first of all for interpreting me the bills and contracts and for his co-operation during the project. The discussion on the white boards has always resulted in +20 GHz faster HBTs.
I would like to thank Ingo Regolin- Single layer and *Nanowhisker* expert - for his friendship and the samples he has grown for me.

The life in the constant temperature and humidity (Clean Room) would be really difficult without Heike Barbknecht- *with three star*-, Andrea Osinski- *the practical idea master*-, Thai Do- *Clean room DJ*-, Udo Doerk- *the octopus* - and Artur Poloczek- *TS expert*.
I would like to thank Reimund Tilders for providing us secure clean room environment and to Wolfgang Molls for supporting me especially during the installation of the ICP-RIE system. I am also grateful to Dr. Viktor Khorenkho for the technical discussion about plasma and plasma processes.

Here, I would like to thank Dr. Thorsten Reimann for introducing me the processing and to Stefan Neumann for providing me the HBTs.

I would like to thank to all the members of ARTEA GmbH.

I am thankful to the former members of IPAG (Innovative Processing AG). Here they are:

Special thanks to Andreas Brennemann for the discussions about the processing. His endless experience has shown me the proper way to go. I would like to thank Christoph van den Berg and Dr. Dietmar Keiper for their support about the evaluation of the ICP-RIE system vendors.

Even though he is former member of IPAG, I would like to make a new paragraph for Dr. Peter Velling. Family Velling (Peter and Silke- *the Doppelkopf partners*-) were always ready to support me and motivate me about the work. I really had good memories with them.

I would like to thank all the student assistants (HiWis) and trainees (Auszubildende) for their supports during this work.

Finally, I would like to thank all the scientists for contributing to the improvement of science and providing books, papers or other documents guided me during the work.

By the way, I would like to thank all the teachers and lecturers, and especially the scientist at Electronics and Communication Engineering Department of Istanbul Technical University, who have well equipped me with the background.

Last but not least, I would like to thank my wife Sema - *my all*- and my parents (Üren and Ahmet Topaloglu), my sister Ebru and my brother Orkun. Without their support, love and patience, I would never reach so far.

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