Solid-State Imaging in Standard CMOS Processes

Von der Fakultät für Ingenieurwissenschaften
der Universität Duisburg-Essen
zur Erlangung des akademischen Grades eines

Doktors der Ingenieurwissenschaften

genehmigte Dissertation

von

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Tag der mündlichen Prüfung: 03.02.2009

Acknowledgements

This thesis was written as a part of the activities developed at the chair *Microelectronic Systems* (MES) of the *University of Duisburg-Essen*, in collaboration with the *Photodetector Arrays* group, which forms part of the department *Signal Processing and System Development* (SYS) at the *Fraunhofer Institute of Microelectronic Circuits and Systems* (Fraunhofer IMS) in Duisburg, Germany. My almost four-year long stay in Germany, required to develop this investigation, was supported by the *German Academic Exchange Service* (DAAD), to whom I would never be able to thank enough for this marvellous and multifaceted experience.

My deepest gratitude goes to my research advisor, Prof. Bedrich J. Hosticka, Ph.D., for his enthusiastic support, invaluable discussions and continuous encouragement. The same goes to both group leaders I had the privilege to work with, Armin Kemna and Werner Brockherde.

I would also like to profoundly thank Prof. Dr. Holger Vogt and Prof. Dr. Anton Grabmaier for their support and the suggestions regarding different aspects of this work.

My gratitude goes also to Prof. Dr. Dieter Jäger for his readiness to become the second examiner of this work.

This investigation would have never been completed without the unique interest, hours of discussion, suggestions, and unforgettable brainstorming sessions of the entire SYS department, which proved to be an invaluable well of experience and help. I would like to thank all of them, and specially Christian Nitta, Wiebke Ulfig, Erol Özkan, Cornelia Metz, Frank Matheis, Salahedine Ibnouquassai, Omar Elkhalili, Andreas Spickermann, Olaf Schrey, Sascha Thoß, Stefan Bröcker, and Melanie Jung.

Many thanks also to Suzanne Linnenberg, Stefan Dreiner, Ralf Rudolph, Dirk Dietrich, Andrea Kahlen, Peter vom Stein, and Martin Figge for their help.

I would like to thank my family for their continuous, neverending love and support. Many things in my life would have never been possible without their presence.

Finally, I thank my wife Lizette for her unlimited patience and lovingly support in this incredible adventure. I could not wish for a better "accomplice". This work is dedicated to her.

Table of Contents

Table of Figures

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 6

Introduction

Charge-coupled devices (CCD) have been the dominant technology in the field of solid-state imaging for a couple of decades due to their capability to perform very efficiently and uniformly over large areas, the collection and transfer of photogenerated charge carriers and their measurement at low noise. But today, the maturity of *complementary metal-oxide-semiconductor* (CMOS) technology based photodetectors is established, and the advantages of their specific features which allow *x-y* pixel addressing, in-pixel amplification and signal processing, the "camera-on-a-chip" approach, and the use of deep sub-micron standard CMOS processes make them a perfect candidate for an increasing number of imaging applications.

Based on the constantly increasing market-potential regarding CMOS technology-based imaging applications, the research activity in this field has been increasing in the past years in many research institutes and companies interested in this area. In the foreground of these activities mainly stood the consumer-sector requiring low cost and high-resolution imaging systems for two-dimensional (2-D) imaging camera applications.

Nowadays, the frontiers are to be pushed further in what signal and spatial resolutions present in CMOS imagers are concerned. It is in this field where the consumer-sector is reactivating the huge semiconductor manufacturers who are, on the other hand, turning toward different research-facilities in the areas of CMOS imaging and photodetector arrays looking for special applications (e.g. in automotive or medicine oriented industries, as well as basic science, or telecommunications) with requirements every time more specific and more difficult to meet. So, being the *Fraunhofer Institute of Microelectronic Circuits and Systems* (Fraunhofer IMS) an institute which pursues industry oriented research and technology innovations, the need for further constant optimisation of both, photodetectors and readout circuits, has become for the *Photodetector Arrays* and *CMOS Imaging* groups at the *Fraunhofer IMS* evident with time.

Moreover, as the present thesis was developed as part of the research activities pursued by the *Photodetector Arrays* group at the *Fraunhofer IMS*, it shares the same goals and focuses on proper characterization and optimisation of standard CMOS processes available for in-house fabrication at the *Fraunhofer IMS* to be used in photodetection tasks. It pursues as well a proper design and characterization of imaging pixels (photodetectors and readout circuitry) fabricated in these processes. The latter implies acquisition and automation of proper measurement stations, design of adequate test-structures, and optimisation of diverse photodetector structures and imaging pixel configurations based on the experimental results obtained, which are used for their further modelling and simulation.

Fortunately, the existing technologies and procedures in fabrication and design of CMOS circuits still offer a vast range of possibilities where improvements can be expected, and as the CMOS processes addressed in this work are being developed at the same Fraunhofer IMS, it implies that a reduced number of alterations (as small as possible) of the processes can be undertaken without major difficulties if they do not significantly affect other applications. The key issues in this endeavour are always *signal-to-noise ratio* (SNR), spectral responsivity, and the response velocity of the fabricated devices.

Regarding the feature size, a new generation of CMOS devices is developed every couple of years, whose feature dimensions are less than 0.7 times those of the previous generation. In the year 2007, the industry available standard CMOS process minimum feature dimensions are oscillating between the 120nm and 90nm. The latter driven by the desire of smaller device area and lower power consumption, higher operation speed, and increased functionality. For Wong [Won96], while "standard" CMOS technologies were providing adequate imaging performance at the 2μm-0.8μm generations without any process change, some modifications to the fabrication process and innovations of the pixel architecture are needed to enable CMOS processes for good quality imaging at the 0.5μm technology generation and below. Regarding the pixel size, Wong suggested that CMOS imagers would benefit from further scaling after the 0.25μm generation only in terms of increased fill-factor and/or increased signal processing functionality within a pixel [Won96]. The latter proved true, and an increased number of imager manufacturers are introducing special imaging enhanced CMOS processes, departing from "standard" CMOS logic and memory technologies at the 0.35μm–0.25μm and below technology generations.

It can be concluded that in order to design a proper photodetector in a standard CMOS process, several compromises have to be held in mind. The quantum efficiency of the device should be high, as well as its bandwidth; its charge capacity should be also high, but the noise, which is directly related to the capacitance of the photodetector output node, its dark current and the number of additional transistors in the pixel, has to be as low as possible as it determines the sensitivity of the device. The solution of one issue affects all the others, and normally in the negative direction. In *CMOS imaging* industry, the huge advantages addressing camera-on-a-chip [Fos97] systems fabrication -where the detector devices and the related circuitry are on the same chip-, the random x-*y* pixel readout, the in-pixel signal processing, and the low prices (compared to special process designs), constantly deal with the CMOS technology progress "side-effects" affecting the optical sensitivity of the devices fabricated for this applications. Increased substrate doping, thinner gate-oxides, lower biasing voltages, etc., are all factors present in contemporary CMOS technology that normally reduce the photodetector sensitivity.

Thus, it is one of the main aims of this work to investigate the real CMOS imaging possibilities of standard (not CMOS imaging enhanced) 0.5μm and 0.35μm CMOS processes available for in-house fabrication at the Fraunhofer

IMS by performing an extensive study of standard available photodetector structures, mainly based on reverse biased *p-n* junctions and/or *metal-oxide-semiconductor* capacitors (MOS-C). Moreover, novel concepts of photodetector pixel structures and readout circuits are proposed, modelled, simulated, fabricated, and characterised, that should achieve an improvement in performance as well as new application developments in the area of CMOS imaging systems. The latter, undergoing as a small amount of changes (extra masks, thermal steps, ion implantations, etc.) as possible within the standard CMOS processes mentioned.

In this sense, in Chapter 1 a brief review of the fundamentals of silicon oriented photodetection and electronic devices physics is given, some of the basic postulates of which are directly applied to the case of the 0.5μm standard CMOS process available at the Fraunhofer IMS, whose photodetection possibilities are investigated in detail in Chapter 2. Chapter 3 deals with different pixel configuration possibilities to be fabricated in the 0.5μm process. As a potential solution to overcome some of the problems encountered in Chapter 3, in Chapter 4, the possibilities of using separated photoactive and readout regions in a mixed silicon-on-insulator (SOI) based high-voltage CMOS process developed for automotive industry applications are discussed. Moreover, the same *30V thin-film SOI* CMOS process is proposed for direct (not using a *scintillator* material) *X*-ray scientific CMOS imaging applications, as it is explained in Chapter 5. In Chapter 6, the photodetection possibilities of the recently developed 0.35μm standard CMOS process available at the Fraunhofer IMS are investigated, as well as different pixel configurations possible to be fabricated in this process. Finally, a discussion is carried out regarding the results obtained throughout the enlisted chapters, and new lines of investigation are attempted to be opened based on some of the results obtained in the present investigation.

1 Fundamentals of Silicon-Based Photodetection

Silicon-based photodetection relies on the physical principle of converting quanta of light energy (photons) into a measurable electrical quantity (voltage, electric current). The link between the photons at the input side of a phototransducer capable of this task, and the voltage or current signals that can be measured at its output are the charge carriers (electrons). Of great importance in this chain is the generation, capture, and transport of these carriers [The96]. If the phototransducer device is to be fabricated using the electro-magnetic properties of a semiconductor such as silicon (with all the advantages of a highly developed CMOS technology), then the principle of such a silicon-based solid-state phototransduction can be divided into three main parts: first, the absorption of photons in the silicon substrate; second, the separation and collection of charge carriers generated by electron *band-to-band* transitions inside the silicon bulk originated by photon to electron *scattering*; and third, the readout of these photogenerated carriers as a suitable current or voltage output signal.

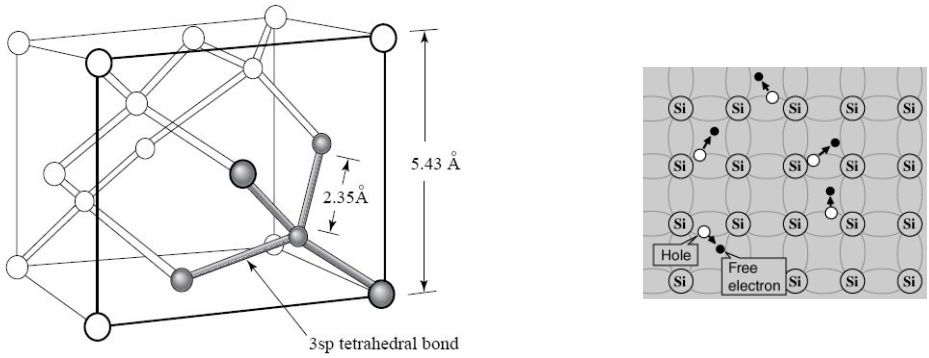
In this chapter, a brief review of fundamentals of silicon-based photodetection is presented which should explain the three processes just mentioned more in detail.

1.1 Energy Band Structure in Silicon

To understand how optical excitation is transduced into electronic information requires understanding the electronic properties of semiconductors; in this case, silicon. Silicon (Si^{14}) is a fourth group element of the periodic table with an electronic configuration: $[Ne]3s^1 3p^2$, that forms a diamond lattice crystal structure (in solid state), that belongs to the *face-centered-cubic* (*fcc*) crystal family and can be seen as two interpenetrating *fcc* sublattices with one sublattice displaced from the other by one-quarter of the distance along the body diagonal of the cube [Sze02], as shown in Figure 1. 1(a).

Each silicon atom in a diamond lattice is surrounded by four nearest neighbours with whom it forms covalent bounding, using its four valence electrons in this task (Figure 1. 1(b)). At the absolute zero temperature, the electrons are bound in their respective tetrahedron lattice, not being available for conduction. At higher temperatures, the originated thermal vibrations (*phonons*) may break the covalent bonds. When a bond is broken or partially broken, a quasi free electron results, that can participate in current conduction if exposed

to an external electric field, as shown in Figure 1. 1(b). Quasi-free electron definition is here used, as the electron finds himself outside the silicon atom in a complex electric field formed by the ions of the lattice and by the valence electrons of the neighbouring atoms, which retain him from leaving the crystal; being really "free" only in vacuum. At the same time, an electron deficiency is left in the covalent bond, which may be filled by one of the neighbouring electrons, which results in a shift of the deficiency location, giving reason for a fictitious particle to be considered - a *hole*.



(a) (b)

Figure 1. 1 – (a) Schematic of silicon diamond lattice based crystal structure [Onlin]; (b) schematic of the basic bond representation of intrinsic silicon showing broken bonds, resulting in conduction quasi-free electrons and *holes* [Onlin].

In 1926, Erwin Schrödinger developed a unified pattern for all mechanical behaviour, based on the Max Planck's quantum theory and using the De Broglie concepts that described the undulatory nature of a particle. This pattern is a partial differential equation that describes how the wave function of a physical system evolves over time. In Schrödinger's formulation of the quantum mechanics, a complex quantity Ψ, called the *wave function*, is related to a dynamical system. For a single particle system, for example, the wave function Ψ can be expressed as shown in Eq. (1. 1) [McK82], where $\hbar$ is the *reduced Planck constant* ($\hbar=h/2\pi$, for the *Planck constant h*), ω is the angular frequency of the wave ($2\pi f$, being f the wave frequency), m is the mass of the particle, and V(x,y,z) is its potential energy.

$$\left[-\frac{\hbar}{2m}\nabla^2 + V(x,y,z)\right]\Psi(x,y,z) = -\frac{\hbar}{i}\frac{\partial\Psi}{\partial t} \qquad (1.\ 1)$$

Following the second of the five basic postulates Schrödinger formulated concerning his wave function, the expression for the total energy E of the system expressed in Eq. (1. 2) [McK82], can be substituted by the classical *Hamiltonian* H of the system, formulating finally the Schrödinger equation as shown in Eq. (1. 3) [McK82], where $p = \frac{\hbar}{i}\nabla$ is the three-dimensional quantity of motion of the particle.

$$\mathrm{H} = E = -\frac{\hbar}{2m}\nabla^2 + V(x,y,z) = \frac{\left(\frac{\hbar}{i}\nabla\right)^2}{2m} + V(x,y,z) = \frac{p^2}{2m} + V(x,y,z) \tag{1. 2}$$

$$\mathrm{H}\Psi(x,y,z) = -\frac{\hbar}{i}\frac{\partial\Psi}{\partial t} \tag{1. 3}$$

The Schrödinger equation is normally solved using the usual mathematical techniques, one of which consists in separating the variables. Thus, solutions are considered following the form expressed in Eq. (1. 4) [McK82].

$$\Psi(x,y,z,t) = \Psi(x,y,z)\phi(t) \tag{1. 4}$$

If the Schrödinger equation (Eq. (1. 1)) is solved in terms of the time function $\phi(t)$ as shown in Eq. (1. 4), this last one can be expressed as $\phi(t) = e^{-\frac{iEt}{\hbar}}$, defining in this way the time dependent Schrödinger wave function as shown in Eq. (1. 5) [McK82].

$$\Psi(x,y,z,t) = \Psi(x,y,z)e^{-\frac{iE}{\hbar}} \tag{1. 5}$$

On the other hand, if the Schrödinger equation is solved for a stationary state, i.e. independently of time, then, it can be expressed as shown in Eq. (1. 6) [McK82].

$$\nabla^2\Psi + \frac{2m}{\hbar^2}(E - V(x,y,z))\Psi(x,y,z) = 0 \tag{1. 6}$$

Considering the wavefunction in stationary state, there exist no restriction for the system total energy E values, i.e. for each value of E there must exist the wave function $\Psi(x,y,z)$ that satisfies Eq. (1. 6). Nevertheless, the requirements of continuity, the finite aspect and the unique value of the solution of the Schrödinger wave function select from within the infinite continuum of possible solutions only those individual solutions that satisfy these conditions, which correspond to certain discrete values of the total energy E of the system, with a separation constant [McK82]. Thus, it can be found that only a certain group of solutions $\Psi(x,y,z)$ related to an associated set of energetic levels is acceptable as wave function for the system, as only these satisfy the wave function and, at the same time, the border conditions of the system. These are the so called *eigenfunctions* (real functions), and the corresponding energy levels they deliver are called the energy *eigenvalues* [McK82].

Up to this moment, the supposition was made that the total energy of the system, E, is negative within the range of $-V_0 < E < 0$, i.e. that the particle studied can only move within a region subject to a constant potential V_0 (e.g. an electron bound to a nucleus of a silicon atom). In case that E becomes positive, it is found that the Schrödinger wave function and all the border conditions can be

satisfied for any positive value of *E*. Thus, there exists a continuous range of allowed energy states and existing eigenfunctions that ascend starting with *E*=0. The eigenstates belonging to this continuum are called c*ontinuous states* [McK82].

Finally, if both cases are taken into account, it can be concluded that if the total energy of the system results in such a way that the classical particle remains limited by the potential *V*(*z*) to move in a finite region of space, there will exist a discrete group of eigenfunctions and energy levels (eigenvalues) that satisfy all the requirements of the wave function. On the other hand, for classical particles with energies big enough to be able to escape from any minimum of potential in the system into the infinity in at least one direction, there exists also a continuum of corresponding energy levels and eigenfunctions that describes the behaviour of this particle [McK82]. Now, if the latter is applied to the case of an isolated silicon atom, it can be concluded that electrons bound to its nucleus can only possess discrete energy levels separated by forbidden gaps where no energy level is allowed; but, if they acquire enough energy to escape the *Coulomb* and other forces that make them remain bound to the atom nucleus, their behaviour will be defined by a continuum of corresponding energy levels, i.e. they will become quasi-free (or free) electrons.

Until here, and in Eqs. (1. 1), (1. 2), and (1. 3), the Schrödinger equation was presented in three-dimensions: *x*, *y*, and *z*. Nevertheless, it is convenient to introduce wave functions that satisfy periodic boundary conditions, as those present within a crystalline grid, which requires wavefunctions to be periodic in *x*, *y*, and *z* with a certain period *L*, as shown in Eq. (1. 7) [Kit96] for the case of the x coordinate. Similar equations result for the *y* and *z* coordinates. Wavefunctions satisfying the free-particle Schrödinger equation and the periodicity condition are of the form of a travelling plane wave, expressed in Eq. (1. 8) [Kit96] for the spherical coordinate vector $\bar{r}$, provided that the components of the wavevector *k* satisfy k_x=0, $\pm\frac{2\pi}{L}$, $\pm\frac{4\pi}{L}$, ..., and similarly for k_y and k_z. Any component of *k* is of the form $2n\pi/L$, where *n* is a positive or negative integer. The components of *k* are the quantum numbers of the problem, along with the quantum number m_s for the spin direction [Kit96].

$$\Psi(x+L, y, z) = \Psi(x, y, z) \tag{1. 7}$$

$$\Psi_k(\bar{r}) = \exp(ik \cdot \bar{r}) \tag{1. 8}$$

According to Bloch's theorem, the eigenfunctions of the wave equation for a periodic potential are the product of a plane wave $e^{ik\cdot\bar{r}}$ times a function $U_k(\bar{r})$, known as the *Bloch function*, with the periodicity of the crystal lattice, as expressed in Eq. (1. 9) [Yad04].

$$\Psi_k(\bar{r}) = U_k(\bar{r})\exp(ik \cdot \bar{r}) \tag{1. 9}$$

The periodicity greatly reduces the complexity of solving the Schrödinger equation, now expressed as shown in Eq. (1. 10) [Kit96]. The wavevector k plays for a free-space electron the same role as does the wavevector Ψ in the wave function for any particle in the three dimensional space, and $\hbar k$ is known as the *crystal momentum* [Kit96] of an electron. For some ranges of momentum, the electron velocity is a linear function of its momentum, so the electron in the lattice can be considered as a classical particle: Newton's second law of motion and the law of conservation of momentum determine the trajectory of the electron in response to an external force or a collision [Yad04]. In other words, in quantum mechanics, within the first quantization, the electrons are particles in classical physics, while perturbations are considered waves (e.g. sound waves or electromagnetic waves). Nevertheless, in the *second quantization*, electrons behave as waves, while waves behave as particles with energy $\hbar\omega$. Thus, it is spoken of quanta of electromagnetic field – the *photons* [Sin96].

$$\left[-\frac{\hbar}{2m}\nabla^2 + V\left(\bar{r}\right)\right]\Psi_k\left(\bar{r}\right) = E_k\Psi_k\left(\bar{r}\right) \tag{1. 10}$$

According to the *Pauli exclusion principle*, no two identical *fermions* (particles that, as electrons, have a spin number m_s as multiple of s = ½, 3/2, 5/2,…) can occupy the same quantum states n, l, m, or m_s simultaneously, considering the opposite electron spins as different quantum numbers. In this sense, other particles, such as photons, with the spin number multiple of intrinsic whole numbers (s = 0, 1, 2, 3,…), do not follow this principle [McK82]. Thus, it can be understood why matter occupies space exclusively for itself and does not allow other material objects to pass through it, while at the same time allowing radiation to pass.

In a silicon crystal being formed by thousands of covalently bound silicon atoms, as the neighbouring atoms are brought together, identical electron energy levels accordingly split into similar but distinct energy levels to fulfil the *Pauli exclusion principle*. The previously discrete energy levels of the initially isolated atoms are spread into continuous bands of energy levels that are separated by gaps where no energy level is allowed [Yad04]. In this sense, the energy band structure of electrons in a crystalline silicon describes the relationship between the energy and momentum of allowed states, determined by solving the Schrödinger wave function, as it can be observed in Figure 1. 2.

For a one-dimensional lattice with a period of a, the region $-\pi/a \leq k \leq \pi/a$ in momentum space is called the first *Brillouin* zone. The energy band structure is periodic in k with period $2\pi/a$, so it is completely determined by the first unit cell, or the first *Brillouin* zone in the k space. At a temperature of absolute zero, the lowest energy band that is not fully occupied and all higher energy bands are called *conduction bands*; all lower bands are full of electrons and called valence bands. The separation between the minimum conduction band and the maximum valence band energies is called the bandgap energy E_g (1.1eV for silicon), as it can be observed in Figure 1. 2.

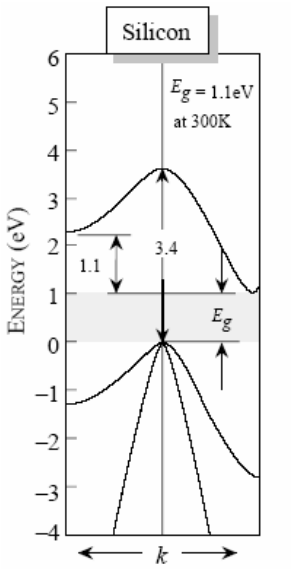


Figure 1. 2 - Electron crystal momentum dependent band structure diagram of silicon (Si), an indirect semiconductor [Sin03].

1.2 Carrier Concentration in Silicon in Thermal Equilibrium

A perfect semiconductor crystal without any impurities or defects is called an *intrinsic* semiconductor. In such material, thermal excitation generates electron-hole pairs (*ehp*) by providing the energy required for an electron to leave a state in the valence band and enter a state in the conduction band [Yad04]. The probability that such a quasi-free electron occupies an allowed electronic state (*eigenstate*) with energy E is given by the *Fermi-Dirac* distribution function, Eq. (1. 11), where E_F is the energy of the *Fermi* level: the energy at which the probability of occupation by an electron is exactly one-half [Sze02], k_B is the so called *Boltzmann constant* and T the absolute temperature expressed in Kelvin.

$$F(E) = \frac{1}{1 + e^{(E-E_F)/k_B T}} \tag{1. 11}$$

There is a large number of allowed states in the conduction band. However, for an intrinsic semiconductor there will not be many electrons there. Therefore, the probability of an electron occupying one of these states is low. There are also a large number of allowed states in the valence band. By contrast, most of these are occupied by electrons, giving the probability of an electron occupying one of these states in the valence band to be nearly unity. So, there will be only a few unoccupied electron states, that is holes, in the valence band. In consequence, the *Fermi* level is located near the middle of the bandgap [Sze04] in an energy band diagram. As for energies that are $3k_BT$ above or below the *Fermi* energy, Eq. (1. 11) can be simplified to $F(E)=\exp(-(E-E_F)/k_BT$, for $(E-E_F) > 3k_BT$, and, finally, the electron density in the conduction band, n, can be expressed as shown in Eq. (1. 12) [Sze02], where E_C is the effective density of states in the conduction band (at $T=300\text{K}$, $N_C = 2.86\times10^{19}\text{cm}^{-3}$ for silicon [Sze02]).

$$n = N_C e^{\frac{-(E_c - E_F)}{k_B T}} \tag{1. 12}$$

Similarly, Eq. (1. 13) expresses the hole density p in the valence band, where N_V is the effective density of states in the valence band (for silicon at room temperature, N_V= 2.66×10^{19}cm^{-3} [Sze02]).

$$p = N_V e^{\frac{-(E_V - E_F)}{k_B T}} \tag{1. 13}$$

For an intrinsic semiconductor, the number of electrons per unit volume in the conduction band is equal to the number of holes per unit volume in the valence band, that is $n = p = n_i$, where n_i is the *intrinsic carrier density* (n_i=9.65×10^{9}cm^{-3} [Sze02]), defined by the *mass-action law*, expressed in Eq. (1. 14), where $E_g \equiv E_C - E_V$ [Sze02].

$$n_i^2 = np = N_C N_V e^{-\frac{E_g}{k_B T}} \tag{1. 14}$$

The carrier concentrations in an intrinsic semiconductor can be dramatically altered by introducing special impurities, known as *dopants*. Introducing atoms belonging to the fifth group of the periodic table of elements, such as phosphorus (P) or arsenate (As) into the silicon crystalline grid, where they take the place of silicon atoms in the grid when exposed to high temperatures (>900°C), in order to form the covalent bounds with the four immediate neighbours of the silicon atom whose place they took, they will immediately be positively ionised, introducing an extra electron to the conduction band. These dopant atoms are normally known as *donors*. If, on the other hand, atoms from the third group of the periodic table of elements are introduced into the silicon grid, they will be negatively ionised, adopting a quasi free electron, and increasing the concentration of mobile holes. In doped semiconductors, the concentrations of mobile electrons and holes is no longer equal, and the material is called *extrinsic semiconductor*, of a *p*-type or an *n*-type, depending whether acceptors (increasing the concentration of positive (*p* for *positive*) mobile carriers – holes, within the silicon grid) were introduced into the silicon, or if it were the donors (increasing the concentration of negative (*n*) mobile carriers –electrons), respectively. The mass-action law still holds: if doping increases the concentration of electrons, the concentration of holes decreases and vice versa. Here, the predominant carrier is known as the *majority carrier*, and the other, as the *minority carrier*.

1.3 Fundamentals of Silicon-Based Phototransduction

As already explained in the sub-chapter 1.1, in quantum mechanical treatment of *scattering* from time dependent perturbation, in the so called *first quantization*, the electrons are particles in classical physics, while perturbations are considered to be waves. Nevertheless, in the *second quantization*, electrons

behave as waves, while waves behave as particles with energy $\hbar\omega$. To convert the wavelength λ of a time-dependent electromagnetic perturbation (radiation wave) to photon energy E_{ph} delivered by each quanta of radiation -observing the same phenomena in both quantizations- the expression shown in Eq. (1. 15) can be used in terms of the angular frequency $\omega=2\pi\nu$, where $\nu = \frac{c}{\lambda}$ is the light frequency and c the speed of light in vacuum.

$$E_{ph} = \hbar\omega = \frac{hc}{\lambda} \tag{1. 15}$$

In the case of light illuminating a semiconductor, light is described by a *photon occupation number*, i.e. how many photons are present in a particular frequency ω, and a polarization mode. This number is defined as *intensity of light*. In one of all scattering processes, the electron can absorb the photon which has an energy $\hbar\omega$. The final energy of the electron after absorption is given by $E_f = E_i + \hbar\omega$, where E_f is the final energy of the electron and E_i the initial one, i.e. the electron final energy is higher than the initial energy by one quanta [Sin96]. If this energy difference is higher than the semiconductor energy gap E_g, the most important optoelectronic interaction used by semiconductor devices occurs, namely the so called *band to band transition* (or *intrinsic transition* [Sze02]) of an electron. In other words, a photon scatters an electron in the valence band causing the electron to go into the conduction band. The latter leads then to the creation of quasi-free carriers: an electron-hole pair. The valence states occupied by electrons are considered to be empty of holes. When photon-electron scattering process that leads to band-to-band (or intrinsic) transitions is regarded, then this entire process is called the *intrinsic photoeffect*. If several *ehp* are being created due to the absorption of energy coming from several impinging photons, and they find themselves inside an electric field that will prevent them from immediate recombination, they will start moving along the electric field lines, causing a flux of carriers which, related to their origin, is normally referred to as a *photocurrent*.

Here, three actual events can happen. If the incoming photon energy $\hbar\omega$ is equal to the bandgap energy E_g, or is greater than E_g, an intrinsic transition takes place, with dissipation of the excess energy ($\hbar\omega$ - E_g) for the second case. On the other hand, for $\hbar\omega$ less than E_g, a photon will be absorbed only if there are available energy states in the forbidden bandgap due to chemical impurities or physical defects, i.e. if this process takes place within an extrinsic semiconductor. This third process is called *extrinsic transition* [Sze02], and it is the most important process on which the entire silicon-based solid-state imaging principle of operation relies and is made possible.

In addition to energy conservation present in the photoeffect, it is also needed that the momentum $\hbar k$ of the electron-photon system to be conserved. The photon k_{ph} (crystal momentum) value is essentially zero compared to the k-values for electrons. Thus, k-conservation ensures that the initial and final

electrons have the same *k*-value. Another way to say this is that only "vertical" k transitions are allowed in the band-structure picture (Figure 1. 2) [Sin96]. Nevertheless, in silicon, the minimum value of the conduction band and the maximum value of the valence band do not share the same electron *k*-value, which makes silicon an indirect semiconductor or a semiconductor in which only indirect electron transitions from the valence band to the conduction band are possible, as it can be observed in Figure 1. 2.

However, *phonons*, quantised unit of lattice vibration, have a momentum similar to that of electrons, with a significant $\hbar k$. Thus, in indirect transitions, electrons can only make this minimum energy transition (E_g) if a phonon is also involved. An indirect optical transition can occur if accompanied by the simultaneous absorption or emission of a phonon. The process can be described as occurring in two steps. First, the electron absorbs a photon and makes a transition to an intermediate state within the bandgap. Next, the electron absorbs or emits a phonon of large wave vector (depending of the energy of the photon absorbed in relation with the energy of the lowest energy state within the conduction band) and completes the transition into the conduction band. An electron can make a transition into a virtual state. Owing to the *uncertainty principle* for energy and time, an electron can occupy a virtual state, provided the duration for which it remains in it is relatively short. There are no *eigenstates* within the energy gap of a semiconductor, therefore being the intermediate states for the indirect transition virtual in intrinsic semiconductors. For the case of extrinsic semiconductors, the electron occupies an allowed energy state within the intrinsic energy gap, introduced by the dopant impurities.

Since the simultaneous absorption of a photon is a higher order process, an indirect transition is said to occur only to second or higher order. The probability of an indirect transition occurring depends then on the probability of two different processes to occur simultaneously, that is: the absorption of a photon and of a phonon. The combined probability is lower than the probability of either event occurring separately. This reduces the transition probability and, hence, the optical absorption. It adds, as well, temperature dependence. Nevertheless, because of the additional degree of freedom introduced by the phonon energy, $\hbar\omega_s$, transitions to many more states are possible [Wol89], which dramatically increases the probability of these events and allows silicon-based imaging. Also, the indirect band-to-band absorption begins at photon energies below the bandgap, such that $\hbar\omega \geq E_g - \hbar\omega_s$.

Assume that a semiconductor is illuminated by a light source exhibiting a photon flux Φ_{ph} (in units of photons per square centimetre per second), with photon energy $E_{ph}=\hbar\omega=h\nu$ higher than E_g. This flux travels through the semiconductor, being the fraction of photons absorbed (scattered) proportional to the intensity of the flux. Therefore, the number of photons absorbed within an incremental distance Δz will be given by $\alpha\Phi_{ph}(z)\Delta z$, where α is a proportionality constant defined as the *absorption coefficient*. After solving the relation between the impinging photon flux and the photon flux still existing at a certain depth *z* inside the semiconductor, for the boundary condition $\Phi_{ph}(z)$ =

Φ_{ph} at z = 0, the fraction of the photon flux that still exists at z is expressed in Eq. (1. 16) [Sze02]. Moreover, the impinging radiation can be also defined through the so called impinging radiant flux Φ(z) in units of watt. The absorption coefficient α is a function of E_{ph}, and the so called light absorption (extinction) depth is the depth inside a silicon substrate at which the incoming Φ reduces its value below (1/e) watts. If the absorbed irradiation energy generates *ehp*, the rate of carrier generation G_{ph} (rate per unit volume), is expressed as shown in Eq. (1. 17) [Sin96] for both, photon flux Φ_{ph} on one side, and radiant flux Φ in terms of the photoactive area A_{ph}, the area of the silicon surface actually being illuminated, on the other.

$$\Phi_{ph}(z) = \Phi_{ph} e^{-\alpha z} \tag{1. 16}$$

$$G_{ph} = \frac{\alpha \Phi(z)}{h\nu \cdot A_{ph}} = \alpha \Phi_{ph}(z) \tag{1. 17}$$

Both, measured wavelength dependent optical absorption coefficients and absorption (extinction) lengths for silicon, for the data obtained from [Gre95], can be observed in Figure 1. 3. For silicon, the wavelength value λ = 1127nm, at which $E_{ph} < E_g$, represents the so called *cut-off wavelength*, at which the *band-to-band* transitions and the material sensitivity drops drastically.

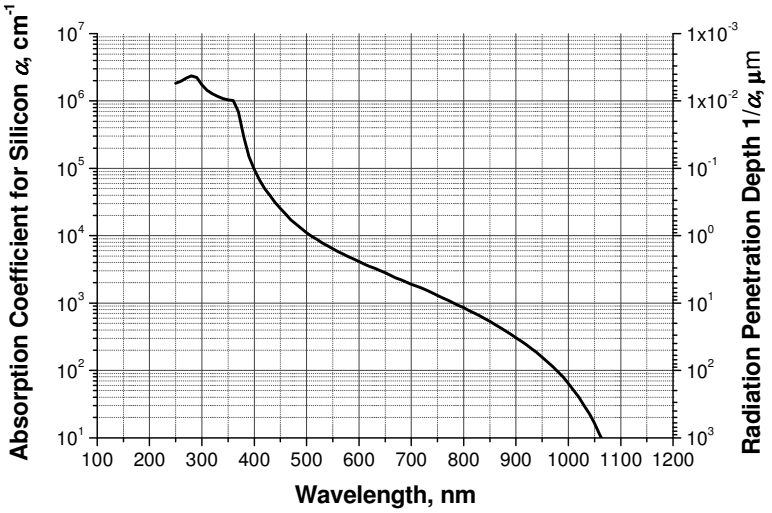


Figure 1. 3 - Wavelength (λ in nm) dependent optical absorption coefficient (in cm^{-1}) and radiation penetration depth (in μm) for silicon. Data used after [Gre95].

Nevertheless, taking in mind that as the number of *ehp* generated by the photons increases, so does the recombination rate, it is not possible to get a measurable signal simply by relying on optical generation. In order to collect a signal it is necessary to separate effectively the photo-generated *ehp* to minimize recombination and cause the carriers to reach some collection contacts. This can be managed by creating an electric field, which can be either a built-in field (e.g. *p-n* junction) or an externally applied field like in a MOS capacitor [Sin03]. These

configurations, if designed in such a way to be radiation sensitive, are then called *photodetectors*.

1.4 Silicon-Based Photodetectors

The most important optical properties of a silicon-based photodetector are its spectral response, its quantum efficiency, and its spatial resolution. The spectral response is a measure of the output voltage or current as a function of the incoming light energy. It is extremely wavelength dependent and directly proportional to the number of photons impinging on the device. For the case of a photodetector, (in this work) its spectral response is described by its *optical sensitivity S*, which gives the photocurrent generated by a given radiant flux Φ, in ampere per watt (A/W) units, as expressed in Eq. (1. 18). On the other hand, the spectral response of an entire pixel existing within a complete imager, will be defined as a pixel *spectral responsivity R*, in volt per joule per square centimetre (V/J/cm^2) units, and will be introduced in another chapter of this work.

$$S = \frac{I_{ph}}{\Phi} \tag{1. 18}$$

The photodetector quantum efficiency η, on the other side, is defined as the ratio of the number of photogenerated *ehp* for each incoming photon, or the probability of a single impinging photon to generate one *ehp*. It can be obtained as the ratio of the exact number of photogenerated electrons forming part of a photocurrent flowing in the photodetector during a certain integration time T_{int} to the exact number of photons forming part of the impinging radiant flux Φ in the same T_{int}, which in terms of the optical sensitivity *S* of the device can be expressed as shown in Eq. (1. 19), following Eq. (1. 15). Moreover, at high photon energies, more than one *ehp* can be obtained because there is enough energy to ionise more than one atom. For silicon at a room temperature (300K) this happens for energies higher than 3.65eV (soft *X*-rays).

$$\eta = \frac{I_{ph}(T_{\text{int}})/q}{\Phi(T_{\text{int}})/h\nu} = S\frac{hc}{\lambda q} \tag{1. 19}$$

The foremost issue in the detector design is to work with a material which has a good absorption coefficient for the frequencies to be detected. Nevertheless, image sensors are used not only to detect light-intensity variations in time, but also to detect light variations in the spatial domain. Here too, the devices have their limits: not all of them can detect the same high spatial frequency. This detection limit depends on the total number of pixels available within an imager. The area of the device also plays a crucial role in detecting spatial information. A parameter describing the detection capabilities of an imager in respect to spatial information is its *spatial resolution* [The96]. Resolution is a measure for the highest spatial frequency which can be resolved by the device taking a specific contrast into account. These spatial frequencies are stated in *line-pairs*/mm (lp/mm). The response of an image sensor to changing spatial frequencies is characterized by its *modulation transfer function*

(MTF). The MTF is defined as the response of the complete optical system to a sine-wave input signal exhibiting a certain spatial frequency, f_{sig}. Both values, the response of the imager and the input frequency f_{sig}, are normalized respectively to the response of the imager at zero spatial frequency and to the sampling frequency of the device, for example, a CCD [The96].

Moreover, it is known that at temperatures above the absolute zero, every semiconductor conducts electricity, i.e. the thermal energy (k_BT dependent) creates also band-to-band transitions: an electrical current, the so called *dark current*. This thermal generation of minority carriers obeys, of course, the usual generation-recombination laws valid for semiconductors. The problem is on one side, that these carriers form part of the output current of the photodetector reducing the storage capacity of the potential well created in the photodetector to collect the photogenerated charge, and on the other, that they introduce simultaneously additional amounts of noise (*dark noise*) in the output signal due to their generation mechanisms. Dark current is an important parameter to characterize the performance of an imager. Lowering the dark current improves the dynamic range and lowers the noise floor or the level of the minimal detection signal of the device, due to a reduction of the dark current shot noise. Dark currents are directly proportional to the space-charge-region (SCR) width and the number of mechanical defects (e.g. crystalline grid dislocations) or chemical impurities, both kinds of defects known as *Shockley-Read-Hall* (SRH) recombination-generation centres present in the silicon bulk, specially at the silicon surface. This particular issue will be addressed more thoroughly later on, in this text.

As already mentioned, once the *ehp* are generated due to the (normally used) *extrinsic photoeffect*, the two charge carrier types have to be separated in order to avoid their immediate recombination. This is accomplished by the presence of a *built-in* or an externally applied electrical field present, for example, in an reverse biased *p-n* junctions or a polysilicon-gate *metal-oxide-semiconductor* capacitor (MOS-C) based photodetectors, respectively. As in this investigation these two basic photodetectors will be presently addressed, a brief description of their basic physical relations is described below.

1.4.1 *p-n* Junction Based Photodetector Structures

In CMOS planar-technology, a *p-n* junction is normally fabricated by ion implantation of phosphorus (P) or arsenate (As) atoms into a *p*-type silicon substrate, or alternatively, by a ion implantation of boron (B) atoms into an *n*-type silicon. This is followed by a posterior high-temperature (~1100°C) impurity activation process by which the donor or acceptor impurities diffuse into the substrate in a certain volume of the silicon wafer (determined by proper photolithography processes). As they are diffusing, the impurity atoms also take place within the silicon crystalline grid, forming covalent bonds with the neighbouring silicon atoms. This process is called impurity activation. In this way, an *n*-well is being formed for the case of P or As atoms implanted and diffused within a *p*-type substrate, or a *p*-well for the case of boron atoms within an *n*-type substrate. The *p-n* junction is created at the limit where no further diffusion

of impurity atoms occurs during the CMOS process thermal steps. A schematic presentation of an *n*-well-*p*-substrate based *p*-*n* junction used as a photodiode can be observed in Figure 1. 4.

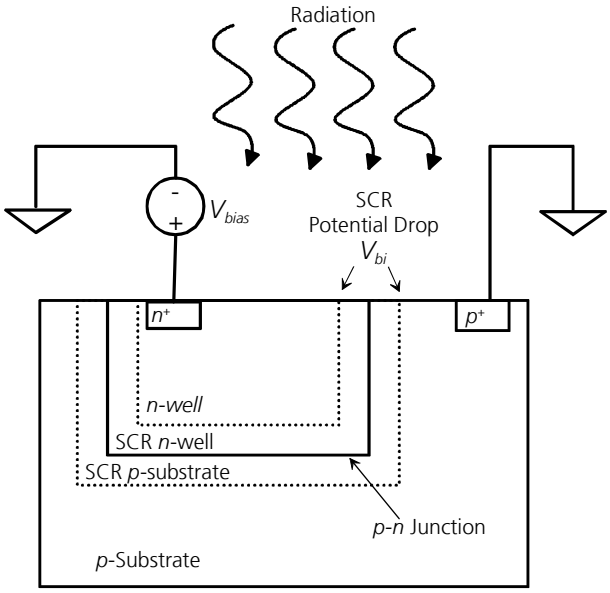


Figure 1. 4 – Schematic of an *n*-well- *p*-substrate based reverse biased *p*-*n* junction structure fabricated in CMOS planar technology and used as a photodiode in CMOS imaging applications.

When a semiconductor device such as a *p*-*n* junction is considered, in which such individual effects as the electron drift due to an electric field F, diffusion due to the concentration gradient, generation of carriers due to external excitation (thermal, irradiative, etc.), and recombination of carriers through intermediate-level recombination centres take place, it is highly convenient to be able to consider the overall effect when drift, diffusion, generation and recombination occur simultaneously in a semiconductor material. The governing equation is then the so called *continuity equation*. For the one-dimensional case under low-injection condition, the continuity equations for minority carriers, i.e. n_p in a *p*-type semiconductor, or p_n in an *n*-type one, are expressed in Eqs. (1. 20) and (1. 21) [Sze02], respectively. Here, μ_n is the electron mobility, i.e. the proportionality factor between the electron (or hole, for the case of hole mobility μ_p) drift velocity when moving inside an electric field and the value of this externally applied electric field, proportional to the mean free time (τ_c) that the electron (or hole) spends between collisions with the existing scattering centres within the crystalline grid, and the electron (or hole) effective mass (m^*) [Sze02]: $\mu_n \equiv \frac{q\tau_{c-n}}{m^*}$ or $\mu_p \equiv \frac{q\tau_{c-p}}{m^*}$. Also, q represents the elementary electron charge, and D_n in Eq. (1. 20) and D_p in Eq. (1. 21) are the electron and hole diffusion coefficients, respectively, related to the carrier mobility as shown in Eq. (1. 22), the so called *Einstein relation*. G_n and G_p are the electron and hole generation rates, respectively, n_{p0} and p_{n0} the electron and hole concentrations in equilibrium, respectively, and τ_n and τ_p are respectively the electron and hole recombination times.

$$\frac{\partial n_p}{\partial t} = n_p \mu_n \frac{\partial F}{\partial z} + \mu_n F \frac{\partial n_p}{\partial z} + D_n \frac{\partial^2 n_p}{\partial z^2} + G_n - \frac{n_p - n_{p0}}{\tau_n} \tag{1. 20}$$

$$\frac{\partial p_n}{\partial t} = -p_n \mu_p \frac{\partial F}{\partial z} - \mu_p F \frac{\partial p_n}{\partial z} + D_p \frac{\partial^2 p_n}{\partial z^2} + G_p - \frac{p_n - p_{n0}}{\tau_p} \tag{1. 21}$$

$$D_n = \left(\frac{k_B T}{q}\right)\mu_n \text{ or } D_p = \left(\frac{k_B T}{q}\right)\mu_p \tag{1. 22}$$

In addition to the continuity equations, *Poisson's equation* expressed by Eq. (1. 23) [Sze02], must be also satisfied at all times, where ε_0 is the dielectric permittivity in vacuum, ε_{Si} the silicon dielectric constant, and ρ_s is the space charge density given by the algebraic sum of the charge densities and the ionised impurity concentrations, $q(p\text{-}n+N_D^+\text{-}N_A^-)$, where *p* and *n* are the doping concentrations within the *p*-type and *n*-type semiconductor regions, respectively.

$$\frac{dF}{dz} = \frac{\rho_s}{\varepsilon_0 \varepsilon_{Si}} \tag{1. 23}$$

As the *p*-*n* junction is being formed, the large carrier concentration gradients at the junction cause carrier diffusion. Holes from the *p*-side diffuse into the *n*-side, and electrons from the *n*-side diffuse into the *p*-side. As holes continue to leave the *p*-side, some of the negative acceptor ions (N_A^-) near the junction are left uncompensated, since the acceptors are fixed in the semiconductor lattice, whereas the holes are mobile. Similarly, some of the positive donor ions (N_D^+) near the junction are left uncompensated as the electrons leave the *n*-side. Consequently, a negative space charge builds up at the *p*-side of the junction and a positive space charge builds up at the *n*-side. This *space charge region* (SCR) creates an electric field that is directed from the positive charge toward the negative charge [Sze02]. An electric current starts to flow in the direction opposite to the diffusion current for each type of charge carrier, i.e. the electrical field causes a drift current of each carrier type opposed to its diffusion current.

At thermal equilibrium, that is, in the steady-state condition at a given temperature without any external excitations at which the generation and recombination rates within a semiconductor are equal, the individual electron and hole currents flowing across the *p*-*n* junction are equal to zero. Thus, for each type of carrier, the drift current due to the electric field must exactly cancel the diffusion current due to the concentration gradient: the relation expressed as shown by Eq. (1. 24) [Sze02]. The same relation for the hole drift and diffusion current densities within a *p*-*n* junction also holds, as expressed in Eq. (1. 25) [Sze02].

$$J_n = J_n(drift) + J_n(diffusion) = q\mu_n nF + qD_n \frac{dn}{dz} = 0 \tag{1. 24}$$

$$J_p = J_p(drift) + J_p(diffusion) = q\mu_p pF - qD_p \frac{dp}{dz} = 0 \quad (1.\ 25)$$

For the condition of zero net electron and hole currents, the *Fermi level* must be constant throughout the sample. The constant Fermi level required at thermal equilibrium results in a unique space charge distribution at the junction, which together with the electrostatic potential ψ are given by the *Poisson*'s *equation* for this case, as expressed in Eq. (1. 26), if it is assumed that all donors and acceptors are ionised.

$$\frac{d^2\psi}{dz^2} = -\frac{dF}{dz} = -\frac{\rho_s}{\varepsilon_0 \varepsilon_{si}} = -\frac{q}{\varepsilon_0 \varepsilon_{si}}\left(N_D - N_A + p - n\right) \quad (1.\ 26)$$

In regions far away from the metallurgical junction, charge neutrality is maintained and the total charge density is zero, i.e. $\frac{d^2\psi}{dz^2} = 0$, and N_D - N_A + p –n = 0. So, the total electrostatic potential difference between the *p*-side and the *n*-side neutral regions at thermal equilibrium is called the *built-in potential* V_{bi}, defined by Eq. (1. 27) [Sze02].

$$V_{bi} = \frac{k_B T}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \quad (1.\ 27)$$

To solve the *Poisson's* equation and be able to determine the potential drop at the region occupied by the space charge and depleted of mobile carriers (the SCR or depletion region), the impurity distribution in both, *p*- and *n*- side of the *p*-*n* junction must be known. The free carriers are completely depleted from the SCR, so the *Poisson's* equation simplifies to Eq. (1. 28) [Sze02] in the region between the *p*-*n* junction and the beginning of both neutral regions (z_n and z_p, respectively). The total SCR width is given by $W_{SCR} = z_p + z_n$.

$$\frac{d^2\psi}{dz^2} = \frac{qN_A}{\varepsilon_0 \varepsilon_{si}}, \text{ for } -z_p \le z \le 0, \text{ and}$$
$$\frac{d^2\psi}{dz^2} = -\frac{qN_D}{\varepsilon_0 \varepsilon_{si}}, \text{ for } 0 \le z \le z_n \quad (1.\ 28)$$

The overall space charge neutrality of the semiconductor requires that the total negative space charge per unit area in the *p*-side must precisely equal the total positive space charge per unit area in the *n*-side. Moreover, integrating Eq. (1. 28), the electric field in a one-dimensional space can be obtained, as expressed in Eq. (1. 29) [Sze02], where F_{max} is the maximum electrical field that exists at z = 0 (the very *p*-*n* contact of the junction), given by Eq. (1. 30) [Sze02].

$$F(z) = -\frac{d\psi}{dz} = -\frac{qN_A\left(z + z_p\right)}{\varepsilon_0 \varepsilon_{si}}, \text{ for } -z_p \le z \le 0, \text{ and}$$

$$F(z) = -F_{\max} + \frac{qN_D z}{\varepsilon_0 \varepsilon_{Si}} = \frac{qN_D (z - z_n)}{\varepsilon_0 \varepsilon_{Si}}, \text{ for } 0 \le z \le z_n \tag{1. 29}$$

$$F_{\max} = \frac{qN_D z_n}{\varepsilon_0 \varepsilon_{Si}} = \frac{qN_A z_p}{\varepsilon_0 \varepsilon_{Si}} \tag{1. 30}$$

Integrating the expressions given by Eq. (1. 29) over the SCR gives the total potential variation, namely the *built-in potential* V_{bi}, as shown in Eq. (1. 31), where the SCR width W_{SCR} results as expressed in Eq. (1. 32) [Sze02].

$$V_{bi} = \frac{qN_D z_n^2}{2\varepsilon_0 \varepsilon_{Si}} + \frac{qN_A z_p^2}{2\varepsilon_0 \varepsilon_{Si}} = \frac{1}{2} F_{\max} W_{SCR} \tag{1. 31}$$

$$W_{SCR} = \sqrt{\frac{2\varepsilon_0 \varepsilon_{Si}}{q} \left(\frac{N_A + N_D}{N_A N_D} \right) V_{bi}} \tag{1. 32}$$

The junction depletion layer (or transition region) capacitance per unit area is defined as $C_j = \mathrm{d}Q/\mathrm{d}U$, where d$Q$ is the incremental change in depletion layer charge per unit area for an incremental change in the applied voltage dU. If U is increased by an amount dU, the charge and field distributions will expand outside $-\frac{W_{SCR}}{2} < z < \frac{W_{SCR}}{2}$ by a certain amount Δz. The incremental space charges on the *n*- and *p*- sides of the depletion region are equal but exhibiting opposite charge polarity, thus maintaining overall charge neutrality. From *Poisson's* equation, this incremental charge dQ causes an increase in the electric field by an amount of $\mathrm{d}F = \mathrm{d}Q/\varepsilon_0 \varepsilon_{Si}$. The corresponding change in the applied voltage $\mathrm{d}U$ is approximately $W_{SCR} \cdot \mathrm{d}F = W_{SCR} \cdot \mathrm{d}Q/\varepsilon_0 \varepsilon_{Si}$. Therefore, the depletion capacitance per unit area is given by Eq. (2.33) [Sze02] in farad per square centimetre (F/cm^2) units. Here, it was assumed that only the variation of the space charge in the SCR contributes to the capacitance, certainly a good assumption for the reverse-bias condition. For forward bias, however, a large current can flow across the junction corresponding to a large number of mobile carriers present within the neutral region. The incremental change of these mobile carriers with respect to the biasing voltage contributes an additional term, called the *diffusion capacitance* [Sze02], treatment of which, however, is beyond the scope of this work.

$$C_j = \frac{\varepsilon_0 \varepsilon_{Si}}{W_{SCR}} \tag{1. 33}$$

It becomes obvious that if an external voltage U is applied to a *p-n* junction, the precise balance between the diffusion current and drift current of electrons and holes is disturbed. Now, as the first approximation, the ideal current-voltage characteristics will be discussed which means that the following assumptions are made [Sze02]: (a) the SCR has abrupt boundaries and, outside

the boundaries, the semiconductor is assumed to be neutral; (b) the carrier densities at the boundaries are related by the electrostatic potential difference across the junction; (c) the low-injection condition, that is, the injected minority carrier densities, are low compared with the majority carrier densities; in other words, the changes in majority carrier densities are negligible at the boundaries of neutral regions by the applied bias; and, (d) neither generation nor recombination current exists in the depletion region, and the electron and hole currents are constant throughout the SCR.

When a forward bias is applied, the electrostatic potential difference at the *p*-*n* junction is reduced to V_{bi} - U; but when a reverse bias is applied, the electrostatic potential difference is increased to $V_{bi} + U$. Thus, the expression for the electron densities under bias is shown in Eq. (1. 34), where n_n and n_p are the non-equilibrium electron densities at the boundaries of the SCR in the *n*- and *p*-sides, respectively, with *U* positive for forward bias and negative for reverse bias.

$$n_n = n_p e^{q(V_{bi}-U)/k_B T} \tag{1. 34}$$

Figure 1. 5 shows band diagrams in a *p*-*n* junction under reverse-bias (shown left) and forward-bias (shown right) conditions, respectively. The minority carrier densities at the boundaries (-z_p and z_n) increase substantially above their equilibrium values under forward bias, whereas they decrease below their equilibrium values under reverse bias. The injected minority carriers recombine with the majority carriers as the minority carriers move away from the boundaries. The hole diffusion current will decay exponentially in the *n*-region with diffusion length $L_p = \sqrt{D_p \tau_p}$, and the electron diffusion current will decay exponentially in the *p*-region with diffusion length $L_n = \sqrt{D_n \tau_n}$, each related to hole and electron recombination times, respectively. The total (diffusion) current flowing, if the assumption is made that no current is generated within the SCR under idealized conditions, is expressed by Eq. (1. 35). This is the *ideal diode equation*, where J_{diff} is the *ideal diode saturation (diffusion) current density* defined by Eq. (1. 36) [Sze02], and p_{n0} and n_{p0} the concentration of holes in the *n*-region in equilibrium, and n_{p0} concentration of electrons in the *p*-region in equilibrium, respectively. This ideal current-voltage characteristic is shown in Figure 1. 5 (at the bottom). The rate of current increase is constant in the forward direction with positive bias on the *p*-side for $U \geq 3k_B T/q$,. At 300K for every decade change of current, the voltage change for an ideal diode is 60mV (2.3 $k_B T/q$) [Sze02]. In the reverse direction, the current density saturates at $-J_{diff}$.

$$J_{total} = J_{diff}\left(e^{\frac{qU}{k_B T}} - 1\right) \tag{1. 35}$$

$$J_{diff} \equiv \frac{qD_p p_{n_0}}{L_p} + \frac{qD_n n_{p_0}}{L_n} \tag{1. 36}$$

Leaving the idealized operation conditions, an important mode of operation of the *p-n* diode under illumination (when used as a photodetector) is when the diode is under reverse bias conditions. The reverse saturation (diffusion) current density considered in the ideal case as defined in Eq. (1. 36), is now driven by generation-recombination processes. Generation of excess carriers within the depletion region (by the extrinsic photoeffect) greatly enhances this reverse current. Therefore, if a reverse biased junction is illuminated with radiation of energy in excess of the bandgap, the reverse current is significantly increased because of the presence of photogenerated carriers. On the other hand, the photocurrent can be also understood as an additional current which normally exceeds the original reverse current. This approach results specially useful when the different carrier generation mechanisms are analysed in detail, as it will be explained in the following chapter.

Under reverse-bias, the height of the potential barrier between the two regions becomes equal to (U + V_{bi}), and the height of the energy barrier is respectively $q(V_{bi}+U)=\psi_{pn}+qU$. So, the total depletion layer width W_{SCR} is represented by Eq. (1. 37).

$$W_{SCR}=\left[\frac{2\varepsilon_{Si}\varepsilon_0(V_{bi}+U)}{q}\cdot\frac{(N_A+N_D)}{N_AN_D}\right]^{\frac{1}{2}} \tag{1. 37}$$

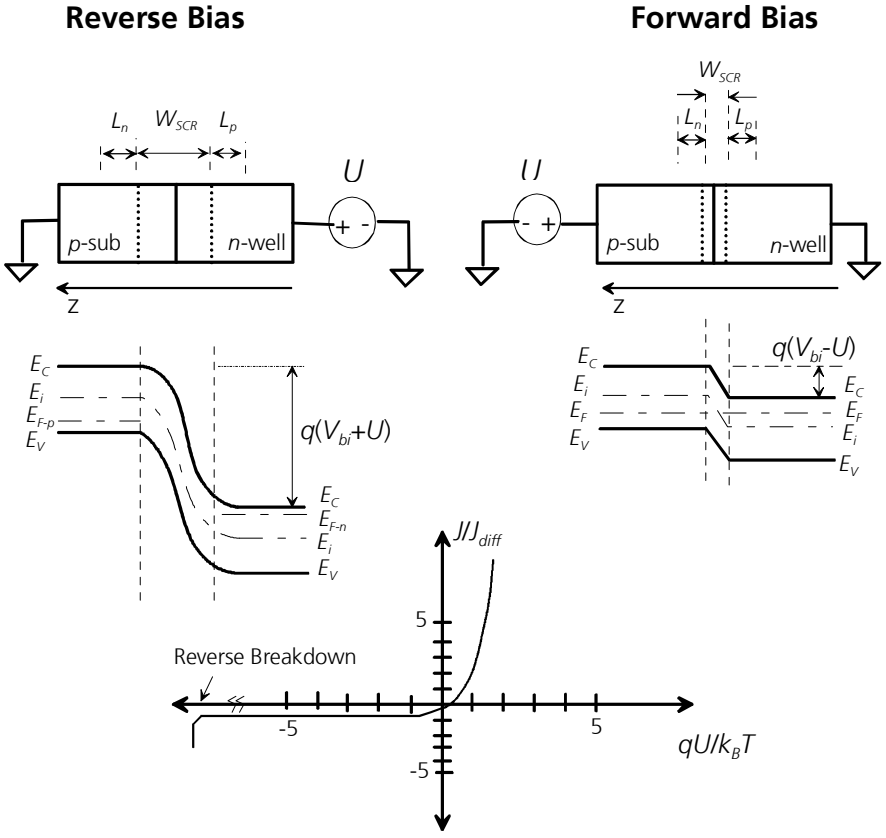


Figure 1. 5 – Schematic representation of the *p-n* junction shown in Figure 1. 4, under reverse (on the left) and forward (on the right) biasing conditions, with the corresponding simplified energy-band diagram for each case and the ideal current-voltage characteristic (on the bottom).

Here, the effective potential barrier is increased, leading to an exponential decrease in the number of carriers, energy of which is higher than the potential barrier. The current flowing across the *p-n* junction in this case depends on the number of carriers generated within the depletion region on one side, and on the number of carriers generated inside the silicon bulk within the diffusion length distance from the depletion region edges, on the other. The carriers generated in the silicon bulk firstly diffuse until they reach the SCR edges where they are immediately drifted in direction of the electrostatic potential maximum (normally, at the silicon surface for the reverse-biased *p-n* junction depicted in Figure 1. 4). Together with the carriers generated within the SCR, the carriers that managed to diffuse into the SCR form part of the photodiode total current consisting of thermally generated carriers in darkness, added to those generated due to photon absorption when illuminated.

The reverse bias aids the operation of the device in other ways. The depletion region in which the light is absorbed is enlarged by the action of the reverse bias, thereby enhancing the absorption. The photogenerated *ehp* are separated by the action of the drift field arose at the *p-n* junction. Photodiodes are attractive in detection applications because they provide high quantum efficiency and very high bandwidth.

This bandwidth, which is inversely proportional to the temporal response of the device, depends on three factors: the carrier diffusion to the depletion region edge, drift time within the depletion region, and the capacitance of the depletion region. Nevertheless, there is a compromise to be met here: in order to absorb the incident radiation fully, it is necessary to make SCR wide. However, as the SCR width increases, the transit time across the junction increases too, thereby reducing the bandwidth of the device. The speed of response also depends on the junction capacitance, which is associated with the reverse biased junction [Bre99].

Moreover, within the electrical field *F*(z), defined by Eq. (1. 29) for the ideal case, electrons and holes acquire enough energy to, when colliding with the atoms of the crystal lattice, generate new electrons and holes by the so called *impact ionisation*. This phenomenon restricts, of course, the value of the reverse maximum voltage which can be applied to a diode. The onset voltage for reverse bias breakdown is called *the breakdown voltage* V_{br}, expressed in Eq. (1. 38) [Bre99], and shown in Figure 2.5 (bottom). Further increase in reverse bias leads to a near exponential increase in the current. Eventually, the multiplication rate increases to the point at which the device becomes unstable, which is called the *avalanche breakdown condition*. Generally, avalanche breakdown occurs when the probability of a carrier's impact ionisation within the depletion region becomes 100% [Bre99]. Avalanche breakdown is fully reversible; when the reverse bias voltage is lowered, the diode behaves as before. However, if the *p-n* junction is reverse biased well beyond the avalanche breakdown point, an additional mechanism called secondary breakdown occurs. It is a no reversible process and leads to catastrophic failure of the junction.

$$V_{br} = \frac{\varepsilon_{Si}\varepsilon_0 F_{br}}{2qN_B} \tag{1. 38}$$

Under normal operating conditions, the photocurrent I_{ph} generated in an illuminated *p-n* junction contains the drift current originated from the photo induced carriers within the depletion region and the diffusion current due to the photo-induced minority carriers generated within their diffusion lengths from the edge of the depletion region, as shown in Eq. (1. 39). A more profound analysis of the photocurrent will be developed at the end of this chapter.

$$I_{ph} = I_{ph-drift} + I_{ph-diffusion}. \tag{1. 39}$$

Next, physics of MOS-C based photodetectors is addressed.

1.4.2 *Metal-Oxide-Semiconductor Capacitor* (MOS-C) based Photodetector Structures

This structure forms the basis of many important semiconductor devices. The most important difference between MOS-C structures and other junction types is that no *dc* current flows under bias in MOS-C structures, due to the presence of the insulator SiO_2 (gate-oxide) layer. Hence, all MOS-C structures are capacitive in nature. Such a structure, namely a *p*-type MOS-C fabricated on an *n*-well in CMOS planar technology and used as a photodetector, is shown in Figure 1. 6.

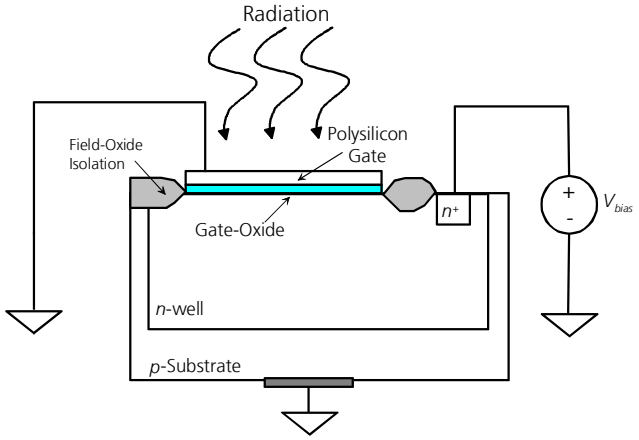


Figure 1. 6 - Cross section of a *p*-type MOS capacitor, fabricated on an *n*-well in CMOS planar technology, to be used as a photodetector in CMOS imaging applications.

An ideal system with the following properties is first considered [Bren99]: (a) the metal-semiconductor (in this case polysilicon-silicon) *work function* difference ϕ_{ms} (i.e. the difference between the Fermi level and the energy required for an electron to become free (vacuum level)) is zero at zero applied bias; (b) the gate-oxide is perfect, i.e. it has zero electrical conductivity (σ=0); (c) no interface states located at the oxide-silicon interface are assumed to exist; (d) the semiconductor is uniformly doped; (e) there is a field-free region between the silicon bulk and the back contact, i.e. there is no voltage drop within the

bulk semiconductor; (f) the structure is essentially one dimensional; and (g) the polysilicon gate can be treated as an equipotential surface.

As is always the case in equilibrium, the Fermi levels align throughout the entire structure, as shown in Figure 1. 7 [Bre99]. From assumption (a) above, the vacuum level is flat throughout the structure since the work functions are the same. Of course, this is in general not the case, but its validity is here assumed for simplicity. The work function difference ϕ_{ms} for a *p*-type MOS-C fabricated on an *n*-well can be determined from inspection of Figure 1. 7, as shown in Eq. (1. 40) [Bre99]. Here, ϕ_m is the metal (polysilicon) work function, χ is the electron affinity (the energy difference between the conduction band edge and the vacuum level in silicon), and ψ_B the barrier potential which is the energy difference between the Fermi level E_F and the intrinsic Fermi level E_i (the probability of 50% for an energy level to be occupied by an electron within an intrinsic semiconductor).

$$\phi_{ms} = 0 = \phi_m - \left[\chi + \frac{E_g}{2q} - \psi_b \right] \tag{1. 40}$$

In the above analysis, many simplifying assumptions have been made, which are invalid in most situations. In particular, it was assumed that the polysilicon-silicon work function difference ϕ_{ms} is zero at zero applied bias and that no interface states or impurities are present within the system [Bre99]. At first, a MOS-C system in which the metal-semiconductor work function difference is not zero is considered. It is important to realize that flat band (condition in which the conduction and the valence bands have zero slope) does not occur at zero bias applied to the polysilicon gate (typically referred to as zero bias). In other words, a voltage must be applied to the gate in order to attain the flat-band condition. This means then that in equilibrium, the energy bands within the semiconductor are bent.

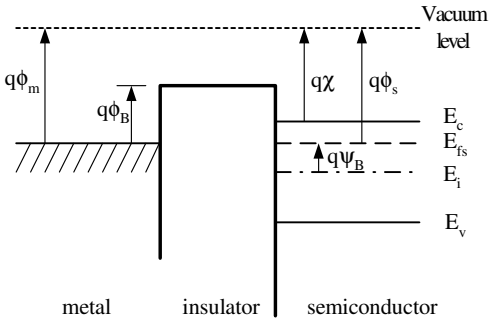


Figure 1. 7 – Energy band simplified diagram of an ideal MOS-C fabricated on an *n*-well, showing the energy bands and Fermi levels under equilibrium conditions; ϕ_m is the metal work function, ϕ_s is the silicon work function, χ is the electron affinity, and ψ_B is the barrier potential.

In equilibrium, the Fermi levels must align through the structure, once the MOS-C structure is formed. To accommodate the work function difference, the semiconductor bands bend up for the case of the MOS-C fabricated on an *n*-well, as the interface is approached from within the *n*-well structure, as shown in

Figure 1. 8. The presence of a net negative charge on the metal in equilibrium results in an electric field pointing from the semiconductor into the polysilicon gate.

In the example chosen, the effective negative potential on the gate repels the majority carrier electrons from the interface. As a consequence, a depletion layer forms in the semiconductor. Therefore, in order to achieve flat-band conditions, a positive gate voltage equal to the work-function difference must be applied. Here, the presence of charge, because of either surface states or impurities within the insulator layer, which can be either fixed or mobile, alters the equilibrium band diagram of the system.

In silicon/gate-oxide junctions, mobile charges due to sodium ion contamination are the most common source of impurities. Na^+ ions have a high mobility in SiO_2 at temperatures below 250˚C, at which the fabricated devices of this kind usually operate. Under application of a negative gate bias, the Na^+ ions migrate to the polysilicon-oxide interface, partially screening the gate bias with respect to the underlying semiconductor layer. In this way, the threshold voltage for strong inversion changes dramatically [Sze02].

In addition to mobile charge within the insulator, fixed charge can also arise at the interface, produced by dangling bonds between the underlying semiconductor and the covering insulator layer, or within the insulator itself. As a result of the band bending, the interface trap energy moves up or down depending on the nature of the applied bias. Clearly, the status of the interface changes with bias, affecting the behaviour of the underlying silicon.

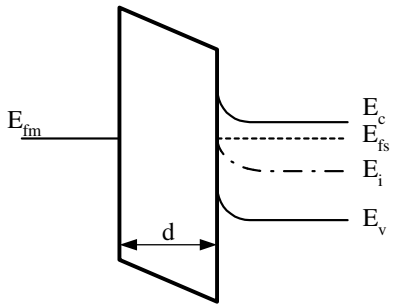


Figure 1. 8 – Band diagram of a MOS-C structure fabricated on an *n*-well, for a non ideal system where $\phi_m > \phi_s$, in equilibrium.

Up to this moment, a MOS-C structure in equilibrium has been analysed. Further on, the situation under non-equilibrium conditions will be revised for the same structure, i.e. the operation of a MOS-C under bias.

If a voltage more positive than U_{FB} with respect to the semiconductor layer is applied to the polysilicon gate, then the positive bias on the gate electrode attracts electrons within the semiconductor to the semiconductor-insulator interface. The potential at the semiconductor-oxide interface also moves in the positive direction, so that the energy bands bend downwards in the boundary region. As the Fermi level gets closer to the conduction band edge, the electron concentration increases in the vicinity of the interface. At each point

inside the semiconductor the thermal equilibrium condition represented in Eq. (1. 41) [Lut96] is fulfilled.

$$n = n_i e^{\frac{E_F - E_i}{k_B T}} \tag{1. 41}$$

Hence, an accumulation layer of electrons, the majority carriers in the *n*-type silicon (*n*-well), forms at the semiconductor-insulator interface. Because of the presence of the positive potential on the gate, the electron energies are lowered near the interface to balance the applied positive gate voltage. Subsequently, away from the interface, there is no net space charge, resulting in flat-band conditions, schematically shown in the band diagram in Figure 1. 9(a). The band diagrams shown in Figure 1. 9 represent a simplification of the *k*-dependent band diagram shown in Figure 1. 2, in which the crystal momentum dependence is being omitted, showing exclusively the energy dependences in different semiconductor structures.

Due to the exponential dependence of the electron concentration on the potential, the region of increased electron concentration is so thin that it can be approximated by a surface-charge density at the interface (remaining at bulk potential). This simplification is similar to the assumption of an abrupt change between a space-charge and a neutral region in the case of the diode. The surface charge density is then given by Eq. (1. 42) [Sze02], where C_{OX} is the oxide capacitance defined by Eq. (1. 43) in F/cm^2 units, ε_{OX} is the SiO_2 dielectric constant (ε_{OX}=3.9), d_{OX} is the gate-oxide thickness, A the area of the MOS-C, and U the bias applied at the polysilicon gate.

$$Q_{acc} = -\varepsilon_{OX}\varepsilon_0 \frac{U - U_{FB}}{d_{OX}} A = -C_{OX} A\left(U - U_{FB}\right) \tag{1. 42}$$

$$C_{OX} = \frac{\varepsilon_0 \varepsilon_{OX}}{d_{OX}} \tag{1. 43}$$

The Figure 1. 9(b) can be understood in another way [Dur03]. The positive bias applied to the gate effectively deposits positive charge onto the metal gate. Sufficient negative charge is induced at the insulator-semiconductor interface to maintain the space-charge neutrality due to the accumulation of free (mobile) electrons within the semiconductor. The finite conductivity of the semiconductor requires that the negative charge accumulates within a layer adjacent to the interface. The insulator (oxide) acts to separate the positive and the negative charges, producing an electric field across it, and leading to the band bending shown in the conduction band of the oxide. The semiconductor bands bend down toward the interface since the electron energies are lowered by the positive charge on the gate. This situation is called *accumulation*.

The situation becomes more complicated if a negative voltage is applied to the gate, as shown in Figure 1. 9(c). Then, the electrons are "pushed away" from the interface and a positive space-charge region is formed. This is a stable

situation if the voltage is low, and the process is called *depletion*. If the voltage is further increased, the depletion width also increases; however, this *over-depleted* situation is not stable. Thermally generated *ehp* are separated by the electric field in the space-charge region, the electrons moving towards the *n*-well and the holes accumulating at the semiconductor-insulator interface. The thin negative charge layer is named *inversion layer*, and the status of the system is called *inversion*, as it can be seen in Figure 1. 9(d).

If a voltage $U \leq U_{FB}$ appears across the MOS-C structure, the bands bend upwards and the electron concentration decreases (Figure 1. 9(c)). Due to the exponential dependence on the distance between Fermi level and conduction-band edge, the charge-carrier concentration drops off over a very short distance to a value that is negligible compared with the doping concentration, so that the assumption of an abrupt change from space-charge to undepleted semiconductor region can be made. With this approximation, it is easy to find the electric field configuration. Using basic relations, depletion-layer surface-charge density Q_B, silicon surface electric field F_s and the electrostatic potential ϕ_s can be expressed in terms of the SCR depth W_{SCR} formed beneath the gate, as shown in Eqs. (1. 44), (1. 45), and (1. 46), respectively [Sze02].

$$Q_B = qN_D W_{SCR} \tag{1. 44}$$

$$F_s = -\frac{qN_D W_{SCR}}{\varepsilon_{Si}\varepsilon_0} \tag{1. 45}$$

$$\psi_s = -\frac{qN_D W_{SCR}^2}{2\varepsilon_0\varepsilon_{Si}} \tag{1. 46}$$

Here, zero potential in the neutral silicon *n*-well region was assumed. The (constant) electric field in the insulator F_{OX} is scaled from F_s by the ratios of the silicon and oxide dielectric constants, as shown in Eq. (1. 47), and the relation between applied voltage *U* and depletion layer depth W_{SCR} is obtained as shown in Eq. (1. 48).

$$F_{OX} = \frac{\varepsilon_{Si}}{\varepsilon_{OX}} F_s = -\frac{qN_D W_{SCR}}{\varepsilon_{OX}\varepsilon_0} \tag{1. 47}$$

$$U - U_{FB} = \psi_s + d_{OX} F_{OX} = -\frac{qN_D}{\varepsilon_0} W_{SCR}\left(\frac{W_{SCR}}{2\varepsilon_{Si}} + \frac{d_{OX}}{\varepsilon_{OX}}\right) \tag{1. 48}$$

The depth of the SCR is thus given by Eq. (1. 49), and the electrostatic potential ψ_s SCR dependence representing bending of the bands at the interface, is defined by Eq. (1. 50).

$$W = \sqrt{\frac{\varepsilon_{Si}\varepsilon_0}{qN_D}\left(U_{FB} - U\right) + \left(\frac{\varepsilon_{Si}}{\varepsilon_{ins}} d_{ins}\right)^2} - \frac{\varepsilon_{Si}}{\varepsilon_{ins}} d_{ins} \tag{1. 49}$$

$$\psi_s = -\frac{qN_D W_{SCR}^2}{2\varepsilon_{Si}\varepsilon_0} \tag{1. 50}$$

If the voltage is further decreased, the intrinsic level at the interface reaches –and eventually crosses- the Fermi level ($\psi_s \leq \psi_B$). Then, the situation is that of a majority of holes at the interface, as shown in Figure 1. 9(d). This situation is called *weak inversion*. If, with further decrease of the voltage, the hole concentration reaches or surpasses the electron bulk concentration, the status of *strong inversion* is reached. This condition is accomplished when the surface potential has moved by approximately twice the distance of the Fermi level from the intrinsic level in the undepleted bulk, i.e. $\psi_s = -2\psi_B - 4\frac{kT}{q}$.

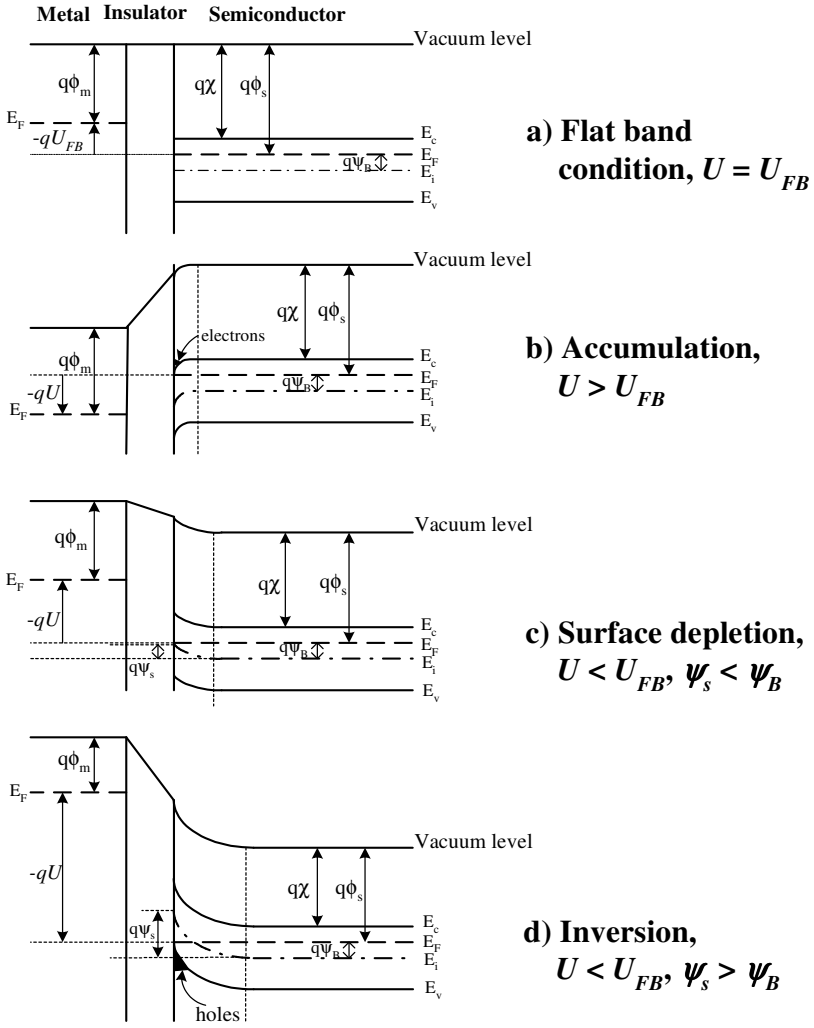


Figure 1. 9 - Simplified (not *k*-dependent) band diagrams for the different operation regions of a *p*-type MOS-C structure, where *U* is the potential applied at the gate, for [Dur03]: (a) flat-band condition; (b) accumulation; (c) surface depletion; (d) inversion. For simplification, it has been assumed that no oxide charges are present.

The hole density at the surface equals the electron density in the *n*-well, and the SCR depth is expressed in Eq. (1. 51). The electric field at the surface of the semiconductor is then given by Eq. (1. 52), and the threshold voltage can be calculated using Eq. (1. 53).

$$W_{inv} = \sqrt{\frac{4\varepsilon_{Si}\varepsilon_0\psi_s}{qN_D}} \tag{1. 51}$$

$$F_s = -\frac{qN_D}{\varepsilon_{Si}\varepsilon_0}W_{inv} \tag{1. 52}$$

$$U_{TH} = U_{FB} - 2\psi_B + F_{OX}d_{OX} = U_{FB} - 2\psi_B - \frac{d_{OX}}{\varepsilon_{OX}\varepsilon_0}\sqrt{4qN_D\varepsilon_{Si}\varepsilon_0\psi_B} \tag{1. 53}$$

Further increase above the corresponding threshold voltage in this approximation only increases the carrier concentration in the inversion layer, the depletion width remaining constant at W_{inv}. On the other hand, if *Debye* length is defined as the characteristic length for which the accumulation or depletion of charge carriers produces an exponential decay of the scattering potential [Bre99], $L_D \equiv \sqrt{\frac{kT\varepsilon_{Si}}{nq^2}}$, the expression for the electric field created beneath the gate-electrode can be expressed as Eq. (1. 54), where the + sign holds for $\psi > 0$, and the – sign applies to $\psi < 0$.

$$F_s = \pm\frac{\sqrt{2}k_BT}{qL_D}\sqrt{\left[\left(e^{-\frac{q\psi}{k_BT}} + \frac{q\psi}{k_BT} - 1\right) + \frac{n_{p0}}{p_{p0}}\left(e^{\frac{q\psi}{k_BT}} - \frac{q\psi}{k_BT} - 1\right)\right]} \tag{1. 54}$$

The surface charge Q_s can be readily determined from the surface electric field by use of *Gaussian law*, defined by Eq. (1. 55).

$$Q_s = -\varepsilon_0\varepsilon_{si}F_s \tag{1. 55}$$

The surface electric field F_s is determined from Eq. (1. 54) with the surface potential ψ_s instead of ψ. The result is plotted in Figure 1. 10.

It is interesting to analyse each of the four states of the MOS-C system in terms of Figure 1. 10 [Lut99]. In accumulation, the surface potential ψ_s is higher than zero and Q_s is positive. The expression for the field is dominated by the first term under the square root, $e^{-\frac{q\psi}{k_BT}}$. Hence, $Q_s \approx e^{\frac{q|\psi_s|}{2k_BT}}$. Flat band occurs when the surface potential is zero. In this case Q_s = 0, i.e. no excess surface charge is present. Depletion occurs when $\psi_B < \psi_s < 0$, and $Q_s \approx -\sqrt{\psi_s}$. When the surface potential is very much larger than ψ_B, the surface is in strong inversion. Under

these conditions, ψ_s is negative and the expression for the electric field is dominated by the fourth term under the square root: $Q_s \approx e^{\frac{q|\psi_s|}{2k_BT}}$.

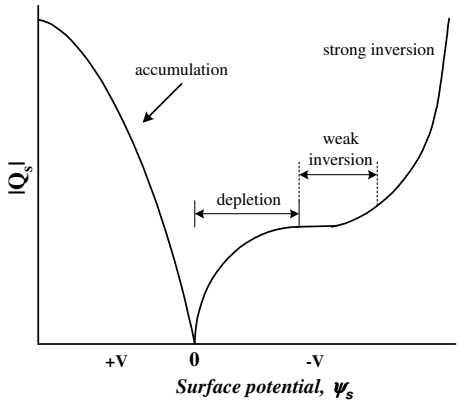


Figure 1. 10 - Plot of the space-charge density as a function of the surface potential to show the different regions of operation, that is: accumulation, depletion, weak inversion, and strong inversion [Sze02].

MOS-C structures have been successfully applied in photodetection, photometry and digital imaging ever since their early beginnings. Actually, the entire industry evolved around the concept of *Charge Coupled Devices* (CCD) and *Charge Injection Devices* (CID) is entirely based on the basic characteristics of this structure. With the evolution of the CMOS process, the idea of the so called *photogate* based detectors arouse - being the *photogates* nothing else but MOS capacitor structures used for radiation detection.

Each MOS-C based photodetector is typically biased initially into deep depletion. Minority carriers are photogenerated by incident photons that pass through the semi-transparent gate electrode (normally fabricated using polysilicon). The minority carriers are then collected within the potential well formed at the insulator-semiconductor interface. The amount of photogenerated minority carriers collected within an individual MOS-C is proportional to the input light intensity impinging onto the available (no metal covered) photoactive area of the MOS-C. Therefore, a two-dimensional grid of pixels can record a complete image. Depending on whether the MOS-C was fabricated on *n*- or *p*-type substrate, it is defined as the *p*-type or the *n*-type MOS-C, respectively.

1.5 Silicon-Based Standard Imaging Technologies

The standard used *charge-coupled devices* (CCD) and CMOS technology fabricated photodetectors are both usually organized as arrays of photodetectors that deliver an electrical signal related to the amount of photons that fall on the detector surface during a certain integration time. When light impinges upon a semiconductor and generates *ehp*, the detector performance depends upon collecting these carriers and thus changing the conductivity of the material or generating the voltage signal. The main difference between the two is the fact that the photoactive area present in CCD is normally fabricated on one chip, while the readout circuitry is fabricated on another chip, normally using any standard CMOS process; in CMOS imaging applications, the photoactive area

and the readout circuitry are fabricated on the same chip (using a single silicon substrate). Next, these two technologies will be explained in more detail.

1.5.1 Charge-Coupled Devices (CCD)

The basic principle of CCD is the dynamic charge storage and transfer in a polysilicon-gate based MOS capacitor array. When light is shining on CCD pixels, photons pass through the polysilicon gate and reach the externally induced SCR generated beneath (this is called front side illumination), or reach this SCR directly (called backside illumination). The photogenerated charge can be then temporarily stored in a MOS capacitor. After collecting the charge (usually designated as integration stage) in the externally created SCR (which corresponds to a potential well) beneath the first (photoactive) MOS-C, it is possible to transfer it from one potential well to the next adjacent one created beneath a neighbouring MOS-C.

Due to the gap (related to "feature size" of semiconductor fabrication) between adjacent polysilicon electrodes, the charges transfer process turns out to be a process that can suffer from charge transfer losses: then we speak about a low *charge transfer efficiency* (CTE). To solve this problem, Walden *et all* at *Bell Laboratories* designed *buried channel* CCD (BCCD) in 1972. The polysilicon electrodes are in this configuration buried by silicon oxide layers, and aluminium (Al) is used to fill the gap between polysilicon electrodes. These additional electrodes create extra potential wells, which combined with the potential wells due to polysilicon, form a potential well of stair shape. In this way, in the process of charge transfer, charges occupy one or more steps of well-stair so that they do not move without constraints, i.e. charges are always stored in potential wells. By clocking the voltage on electrodes, charges are transferred "smoothly" to the readout node. Nowadays, this additional aluminium electrodes are replaced by a second, overlapping, polysilicon layer.

In CCD operation, photoelectrons are transported in the charge domain through vertical (parallel) and horizontal (serial) buried channel CCD shift-registers to a single readout node where charge-to-voltage conversion is performed (commonly by "floating diffusion" technique, which will be discussed later in this text, more in detail). The key parameters that affect the CCD performance are: its quantum efficiency, its sensitivity, and gain and bandwidth of the source follower (SF) amplifier which serves as the output buffer of the integrated voltage signal readout at the floating diffusion. The SF is necessarily wideband in order to allow the *correlated double sampling* process (CDS), used for reduction of low-frequency noise, to occur in one pixel time frame with a complete settling of signals.

Any number of rows in a CCD chip can be added together and send to the serial output register; then any number of output register pixels can be added onto CCD output gate. Adding pixels together is called *binning*. Binning process increases the sensitivity of CCD. However, it decreases its spatial resolution as well.

1.5.2 Comparison of CCD and CMOS Imaging Technologies

Each CMOS pixel element normally contains a photodetector, a charge integrating readout diffusion (normally called *floating-diffusion* FD), a reset and a row (or column) select transistors, and an output amplifier (normally a *source-follower* SF configuration). On top of the whole sensor, there lays a grid of metal interconnects that carry *timing* and *readout* signals. The column lines of this grid connect to a set of decode and readout (multiplexing) electronics that are arranged outside the sensor array. This structure allows signals from the entire array, sub-array, or a single pixel to be read out by a simple *x-y* addressing technique.

The first part of the idea of using "standard" CMOS technology for imagers is to use a widespread, accessible process. The second part is that fully integrated camera systems can be built on a single chip [Fos97]. The low power consumption is easily accomplished for CMOS imagers: a) because only one row of pixels needs to be active during the readout, and b) because of low voltage operation. Integration of on-chip timing, control, signal processing, and analogue-to-digital converter electronics lowers sensor system cost. Analogue signal processing can include widening the dynamic range of the sensor, real-time object tracking, edge detection, motion detection, and image compression [Yad04]. On the other hand, CCD based imagers present optimised *signal-to-noise ratios* (SNR), very low dark currents, high fill-in factors, and other advantages that a mature technology such as this one can offer. Of course, there is a possibility of using separate substrates for phototransduction and readout, i.e. the silicon substrate choice (high resistivity, intrinsic bulk, etc.), as well as gate-oxide thickness, or applied biasing voltages used for the photodetectors does not interfere with the process parameters used for the readout circuitry. Nevertheless, such an approach would make this technology much more expensive if compared to the CMOS based one.

Anyway, as both technologies are based on silicon, the spectral response, the minimum pixel size, charge storage capacity per unit area, chip size and number of pixels within an imaging system, or the geometrical stability do not significantly differ from one technology to the other.

Moreover, *hybrid sensors* are attempts of combining technologies that can potentially deliver performance superior to CCD and CMOS bulk detectors. Nevertheless, a full-featured combination of both technologies would require almost all the stages from both processes, which means more than 30 masks, making this kind of solution to be highly impractical, although the feasibility of CMOS/CCD hybrids was demonstrated, for example by *Sun Imaging Microsystems* or *Eastman Kodak,* as analysed by Janesick in [Jan03].

Now, in order to get more specific in the next couple of chapters the two standard (not CMOS imaging enhanced) CMOS processes, namely the 0.5μm and the 0.35μm ones will be presented, available for imager systems in-house fabrication at the Fraunhofer IMS, and their photodetection possibilities will be profoundly studied.

2 The 0.5μm Standard CMOS Process and its Photodetection Possibilities

One major issue concerning CMOS imaging applications is the fact that a standard CMOS process intended for fabrication of imaging systems already exists in its final form, with all its fabrication steps and a determined number of photolithography masks, and was normally designed to meet specifications not related to imaging tasks, that is, it has been developed for other applications, such as fabrication of high-density digital circuits. This leaves almost no room for any posterior process changes that could affect the performance of other CMOS devices. So, the challenge consists in a proper optoelectronic characterization of the process and the creativity for obtaining the best photodetection performance by designing optimum photodetectors and imager systems using exclusively the fabrication steps and the photolithography masks available. Nevertheless, there is always some room for small changes that convert this standard CMOS process in an electrical imaging enhanced one. In this chapter, the standard 0.5μm CMOS process used for CMOS imaging application at the Fraunhofer IMS is profoundly studied and described to seize most of its imaging potential.

2.1 Meeting the 0.5μm Standard CMOS Process

The 0.5μm standard CMOS process studied uses the twin-well fabrication approach and features a single 280nm thick polysilicon layer as well as three metal layers, and it is LOCOS (*Local Oxidation of Silicon*) based. It uses 200mm diameter wafers, consisting of a highly doped (10-20 mΩ·cm) 750μm thick *p*-type silicon bulk, and a 5.5μm thick lowly doped (ρ=20-40 Ω·cm) epitaxial layer thermally grown on top of it. Due to the twin-well technology, the initial photosensitivity potential of a higher-resistivity epitaxial layer is immediately lost to highly doped ~1.5μm deep *n*-well and *p*-well structures (~10^{17}cm^{-3}) fabrication of which builds a modulated doping profile inside the epitaxial layer. Of course, although higher doping concentrations imply certain quantum efficiency loss in the NIR part of the spectra (as the SCR widths are certainly narrower), this fact also contributes to the response velocity of for example, a MOS-C based photodetector, as narrower SCRs are read out in shorter readout times.

The 12nm thermally grown gate oxides allow V_{DD}=3.3V maximum biasing, while the threshold voltages are V_{th}=0.65V for *n*-type *metal-oxide-semiconductor*

field-effect-transistors (NMOSFET), and V_{th}=-0.7V for *p*-type MOSFET (PMOSFET). Both threshold voltage values refer to transistors with 20μm channel widths (W) and 0.6μm channel lengths (L). The process was designed to suit the 0.6μm design rules, and its final cross-section diagram (not to scale) can be observed in Figure 2. 1 [IMS03].

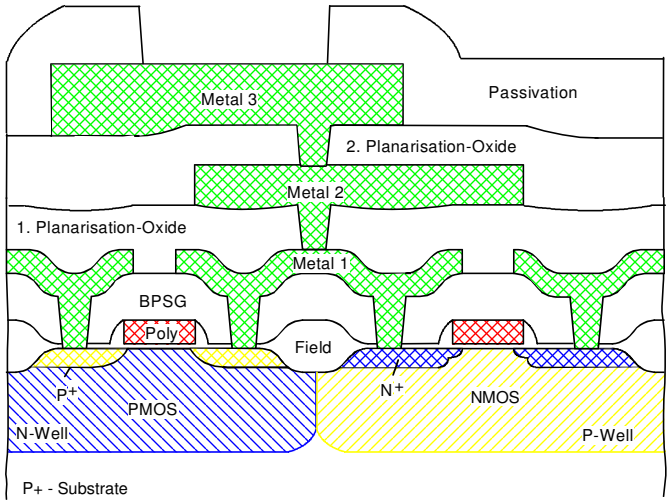


Figure 2. 1 – Final cross-section of the 0.5μm standard CMOS process (not to scale), showing the 1.5μm deep ~10^{17}cm^{-3} *n*-well and *p*-well structures, 0.3μm deep 2×10^{19}cm^{-3} highly doped n^+ and p^+ (*source* and *drain*) diffusions, the LOCOS ~620μm thick field-oxides used for isolation, borophosphosilicate glass (BPSG) layer used to isolate polysilicon from the first metal layer, the first and the second inter-metal oxides planarised through *chemical-mechanical planarisation* (CMP), the three metal layers, and finally the surface passivation layer [IMS03].

The basic building blocks observed in Figure 2. 1 as well as the fabrication steps and the lithography masks used to fabricate them are also the basic building blocks for any photodetector pixel array. In this work, a special attention is paid to reverse-biased *p*-*n* junctions fabricated using the *n*-well (on which the *p*-type MOSFET fabrication is based, as shown in Figure 2. 1), and the n^+ (*source and drain* diffusions used for the *n*-type MOSFET fabrication, Figure 2. 1) diode structures, from now on named *n*-well and n^+ photodiodes, respectively, as well as some other combinations of these basic blocks as it will be explained in the next sub-chapters. Moreover, a MOS-C based photodetector is also to be studied in detail, obtained using the polysilicon gate, the gate-oxide and the *p*-Epi substrate, for the case of an *n*-type MOS-C, from now on named *n*-type *photogate* (PG); or the same polysilicon layer, the same gate-oxide, and the *n*-well, for the case of a *p*-type MOS-C from now on *p*-type *photogate* (PG).

During each fabrication step present in the process, specially during those involving high temperatures (T > 600°C), the impurities from the highly doped silicon bulk, as well as those being implanted on the epitaxial (Epi) layer surface in order to create the different *p*- or *n*- wells, or p^+ or n^+ (*source-drain*) diffusions, diffuse into the epitaxial layer from both directions creating the modulated doping profile within. All these peculiarities of the potential photodetector structures imply depth related changing SCR widths within the epitaxial layer, a certain electrostatic potential arouse due to the concentration

gradient, as well as depth-related changing minority carriers lifetimes, absorption coefficients, and many other parameters. To be able to approach the real values describing all these figures of merit, simulations were carried out using the *TCAD* 8 software tool (provided by the former *ISE* company, nowadays *Synopsys, Inc.*), designed for microelectronic process and device simulations, considering all the fabrications steps forming part of the process under investigation. Figure 2. 2 shows both, the *n*-type MOSFET and the *p*-type MOSFET two dimensional doping concentration simulation performed. On the other hand, different test structures were fabricated and properly characterized, as it will be explained later in this text.

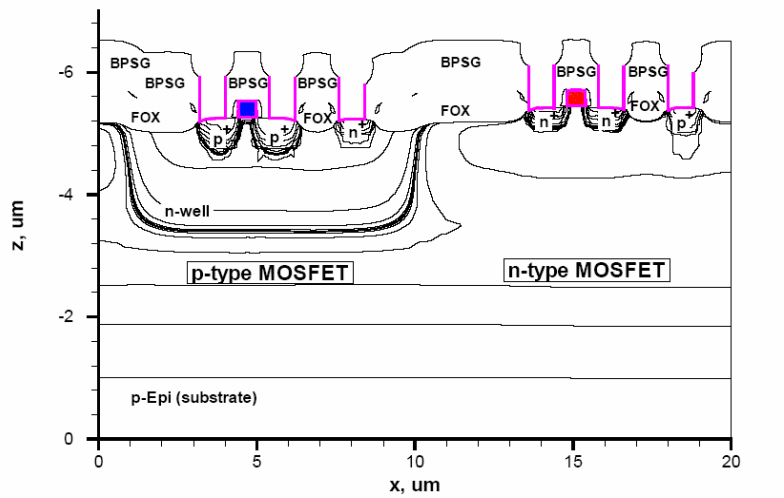


Figure 2. 2 – Two dimensional simulation performed using the TCAD software for the *n*-type and the *p*-type MOSFETs, respectively, fabricated in the 0.5μm CMOS process (*L*=0.6μm), where the modulation of the doping profiles within the epitaxial layer can be observed. Each line corresponds to a change in the doping concentration.

2.2 The Inter-Metal Isolation and Passivation Layer Influence on the Photodetectors Optical Sensitivity

The unavoidable (LOCOS) field-oxide structures used for wafer-surface isolation between semiconductor devices, as well as the *borophosphosilicate glass* (BPSG), the inter-metal oxides and the surface passivation layer existent on top of any integrated circuit (IC) fabricated in this process (observed in Figure 2. 1), deliver wavelength dependent variable transmittance in front-side illumination CMOS imaging tasks.

Namely, the varying transmission function of any material layer (in this case the just mentioned IC surface structure) is caused by interference between the multiple reflections of light caused by this material surface. Constructive interference occurs if the transmitted beams are in phase, and this corresponds to a high-transmission peak of the material. If the transmission beams are out of phase, destructive interference occurs and this corresponds to a transmission minimum. Whether the multiply-reflected beams are in-phase or not depends on the wavelength λ of the incoming light, the angle θ at which the light travels through the material layer, the thickness l of the material layer, and the

refractive index *n* between the air (assumed n_0=1) and the layer of interest, as it can be observed in Figure 2. 3 [Hec89].

The *radiant energy* E_W (measured in joules) refers to the total amount of energy emitted by a light source, penetrating a semiconductor surface, or being collected by a detector. The *radiant flux* Φ (measured in watts) is the radiant energy per second. The radiant flux incident on the unit detector area is called *irradiance* E_R (measured in watts per square centimetre). The irradiance of a *plane wave* -a constant-frequency wave, wave fronts of which are infinite parallel planes of constant amplitude normal to the phase velocity vector (a definition valid in optics for propagation in a homogeneous medium over length scales much longer than the wavelength, where the "rays" are locally plane waves)- defined by Eq. (2. 1) [Hec89], travelling in vacuum in the *z* direction, is given by Eq. (2. 2) [Dem96]. Here, I_0 is the complex amplitude of the wave, *i* the imaginary unit, ω the angular frequency, $\bar{k}$ the wave vector, *c* the velocity of light in vacuum, and ε_0 the dielectric permittivity constant. With the complex notation of the plane wave *u*(*z*, *t*) expressed in Eq. (2. 3) [Dem96], for $|A_0| = \frac{1}{2}|I_0|$, the irradiance E_R can be expressed as shown in Eq. (2. 4) [Dem96].

$$u(z,t) = I_0 e^{i(\omega t - \bar{k}z)} \tag{2. 1}$$

$$E_R = c\varepsilon_0 \left(u(z,t)\right)^2 = c\varepsilon_0 I_0^2 \cos^2\left(\omega t - \bar{k}z\right) \tag{2. 2}$$

$$u(z,t) = A_0 e^{i(\omega t - \bar{k}z)} + A_0^* e^{-i(\omega t - \bar{k}z)} \tag{2. 3}$$

$$E_R = c\varepsilon_0 \left(u(z,t)\right)^2 = 4c\varepsilon_0 A_0^2 \cos^2\left(\omega t - \bar{k}z\right) \tag{2. 4}$$

Most detectors, nevertheless, cannot follow the rapid oscillations of the light wave with the angular frequencies $\omega \sim 10^{13}$-10^{15} Hz in the visible (VIS) and near infra-red (NIR) part of the spectra. With a time constant $t >> 1/\omega$ they measure, at a fixed position *z*, the time-averaged irradiance $\overline{E_R}$, expressed in Eq. (2. 5) [Dem96].

$$\overline{E_R} = \frac{c\varepsilon_0 I_0^2}{t}\int_0^t \cos^2\left(\omega t - \bar{k}z\right)dt = \frac{1}{2}c\varepsilon_0 I_0^2 = 2c\varepsilon_0 A_0^2 \tag{2. 5}$$

Moreover, if it is assumed that the plane wave *u*(*z*, *t*) (Eq. (2. 1)) is incident at the angle θ_i on a plane transparent plate with two parallel, partially reflecting surfaces (the isolation layer surface and the silicon substrate one, Figure 2. 3), then at each surface the incident wave *u*(*z*, *t*) with amplitude I_0 is split into a reflected component $u_{R\text{-}1}$(*z*, *t*) with amplitude $I_{R1} = I_0\sqrt{R}$ (*R* being the reflectivity) and a refracted component $u_{T\text{-}1}$(*z*, *t*) with $I_{T1} = I_0\sqrt{(1-R)}$, if absorption is neglected. This entire system resembles then the so called *Fabry-*

Perot interferometer, where the isolation layer is the systems Fabry-Perot *etalon* (*etalon* coming from the french word *étalon*, meaning "measuring gauge" or "standard").

In this case, the reflectivity $R = \frac{u_{R1}(z,t)}{u(z,t)}$ depends on the angle of incidence θ_i and on the polarization of the incident wave. Provided the refractive index n is known, R can be calculated from *Fresnel's* formulas as follows. If the incident light beam is polarized with the electric field of the radiation perpendicular to the plane defined by the air - inter-metal oxide layer interface (upper left part of the diagram shown in Figure 2. 3), then the reflectivity R_0 can be defined as expressed in Eq. (2. 6) [Dem96], where the incidence angle θ_i can be obtained following the *Snell's law* ($n_0 \sin\theta_i = n_1 \sin\theta$). If the impinging beam is polarized with the plane defined by the inter-metal oxide layer in Figure 2. 3, then R_1 can be expressed as shown in Eq. (2. 7). If the incident radiation is not polarised, the reflection coefficient is $R = (R_0+R_1)/2$.

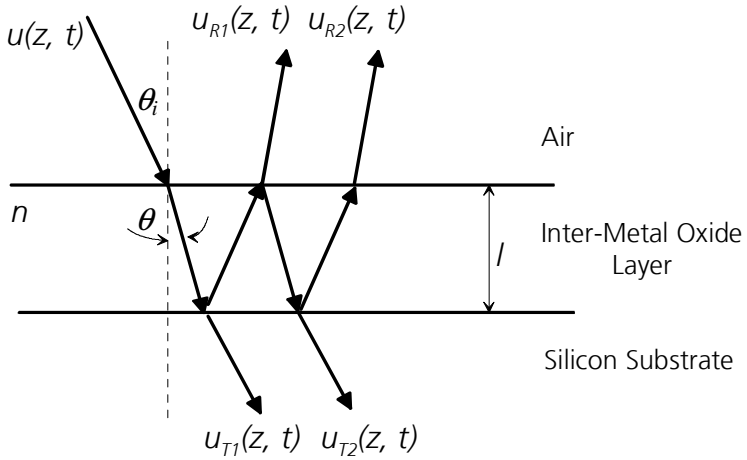


Figure 2. 3 – Diagram of the wafer surface structure resembling the plane Fabry-Perot interferometer, shows the incident light beam $u(z, t)$, the surface reflected light beams $u_{R1}(z, t)$ and $u_{R2}(z, t)$, the transmitted light beams that reach the silicon substrate $u_{T1}(z, t)$ and $u_{T2}(z, t)$, the thickness of the inter-metal oxide layer l, and the angle θ at which the light beam travels through the inter-metal oxide layer for the case of the radiation impinging on the photodetector.

$$R_0 = \left[\frac{\sin(\theta - \theta_i)}{\sin(\theta + \theta_i)}\right]^2 = \left[\frac{n_0 \cos(\theta_i) - n_1 \cos(\theta)}{n_0 \cos(\theta_i) + n_1 \cos(\theta)}\right]^2 \quad (2.\ 6)$$

$$R_1 = \left[\frac{\tan(\theta - \theta_i)}{\tan(\theta + \theta_i)}\right]^2 = \left[\frac{n_0 \cos(\theta) - n_1 \cos(\theta_i)}{n_0 \cos(\theta) + n_1 \cos(\theta_i)}\right]^2 \quad (2.\ 7)$$

For the case of near normal incidence of the light beam to the surface of the isolation layer, i.e. for $\theta_i = \theta = 0$, the reflection coefficient R is given by Eq. (2. 8).

$$R = \left(\frac{n_1 - n_0}{n_1 + n_0} \right)^2 \tag{2. 8}$$

Returning to Figure 2. 3, two successively reflected partial waves $u_{Ri}(z, t)$ and $u_{R(i+1)}(z, t)$ have the optical path difference defined by Δs as shown in Eq. (2. 9) [Dem96] if the refractive index within the plane-parallel plate is $n>1$ and outside the plate $n_0=1$ (air), as it is the case.

$$\Delta s = 2nl \cdot \cos\theta = 2nl\sqrt{1 - \sin^2\theta} \tag{2. 9}$$

This path difference causes a corresponding phase (ϕ) difference, where ϕ is defined as shown in Eq. (2. 10) [Dem96], and $\Delta\phi$ takes into account possible phase changes caused by the reflections.

$$\phi = \frac{2\pi\Delta s}{\lambda} + \Delta\phi = \frac{4\pi nl \cdot \cos\theta}{\lambda} + \Delta\phi \tag{2. 10}$$

For vertical incidence ($\theta_i = 0$), partially provided in this case by the optical breadboard system (Figure B. 4) explained later in this text, there exist an infinite number of reflections. Total amplitude I_R of the reflected wave $u_R(z, t)$ can be then expressed as shown in Eq. (2. 11) [Dem96] for the amplitude I_0 of the incident wave $u(z, t)$ as expressed in Eq. (2. 1) and the reflectivity R defined by Eq. (2. 8).

$$I_R = -\sqrt{R} I_0 \frac{1 - e^{i\phi}}{1 - \mathrm{Re}^{i\phi}} \tag{2. 11}$$

The irradiance $E_{R\text{-}R}$ of the reflected wave, defined for the case of interest as shown in Eq. (2. 5), can be expressed in terms of the incident irradiance $E_{R\text{-}0}$ as Eq. (2. 12) [Dem96].

$$E_{R-R} = E_{R-0} R \frac{4\sin^2\left(\frac{\phi}{2}\right)}{(1-R)^2 + 4R\sin^2\left(\frac{\phi}{2}\right)} \tag{2. 12}$$

In an analogous way, the total transmitted irradiance $E_{R\text{-}T}$ can be expressed as shown in Eq. (2. 13) [Dem96]. The Eqs. (2. 12) and (2. 13) are called the *Airy formulas*.

$$E_{R-T} = E_{R-0} \frac{(1-R)^2}{(1-R)^2 + 4R\sin^2\left(\frac{\phi}{2}\right)} \tag{2. 13}$$

Since the absorption has been neglected from the beginning, the condition $E_{R\text{-}0} = E_{R\text{-}R} + E_{R\text{-}T}$ can be easily verified from Eqs. (2. 12) and (2. 13).

Taking into account the absorption $A = (1\text{-}R\text{-}T)$ [Dem96] of each reflective surface, as well as the abbreviation $F = 4R/(1-R)^2$, Eq. (2. 13) has to be modified to Eq. (2. 14a) [Dem96], where $T^2 = T_1 T_2$ is the product of the transmittance of the two reflecting surfaces.

$$E_{R-T} = E_{R-0} \cdot \frac{T^2}{(A+T)^2} \cdot \frac{1}{\left[1 + F \sin^2\left(\frac{\phi}{2}\right)\right]} \tag{2. 14a}$$

On the other hand, if the absorption is considered, it causes three effects [Dem96]:

i. The maximum transmittance is decreased by the factor defined in Eq. (2. 14b) [Dem96], which means that already a small absorption of each reflecting surface results in a drastic reduction of the total transmittance.

$$\frac{E_{R-T}}{E_{R-0}} = \frac{T^2}{(A+T)^2} = \frac{T^2}{(1-R)^2} < 1 \tag{2. 14b}$$

ii. For a given transmission factor T, the reflectivity $R = 1\text{-}A\text{-}T$ decreases with increasing absorption. So, the quantity F decreases with increasing A, as shown in Eq. (2. 14c) [Dem96]. This makes the transmission peaks broader. The physical reason for this is the decreasing number of interfering partial waves. The *contrast* $E_{R-T}^{\max} / E_{R-T}^{\min} = 1 + F$, of the transmitted intensity also decreases.

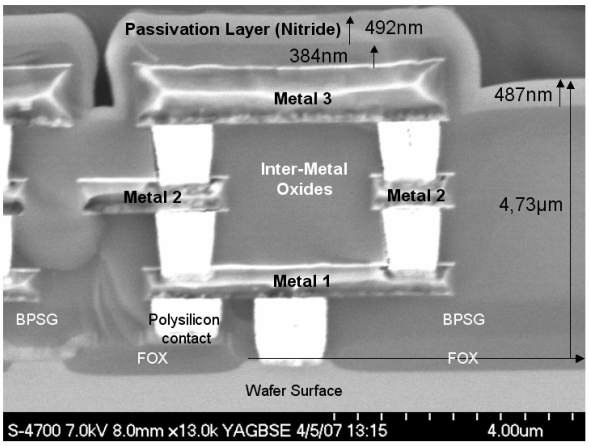
$$F = \frac{4R}{(1-R)^2} = \frac{4(1-T-A)}{(T+A)^2} \tag{2. 14c}$$

iii. The absorption causes a phase shift $\Delta\phi$ at each reflection, which depends on the wavelength λ, the polarization, and the angle of incidence θ_i. This effect causes a wavelength dependent shift of the maxima.

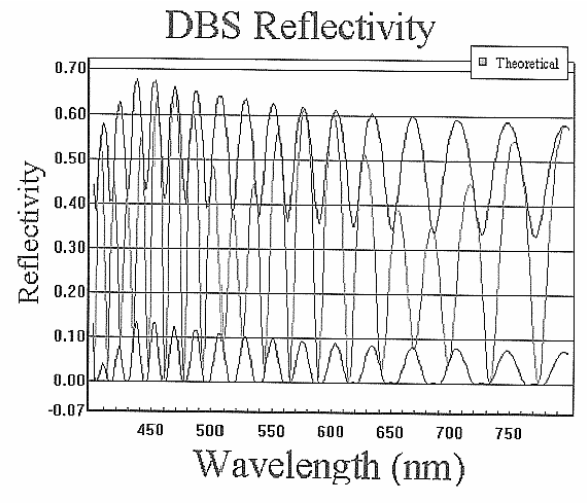
Figure 2. 4(a) shows a *scanning electron microscope* (SEM) image of the surface layers present in an IC fabricated in the 0.5μm standard CMOS process under investigation. In the image it is possible to observe the 4.73μm thick silicon dioxide layer, a combination of the BPSG and three inter-metal oxide layers, as well as the 487nm thick silicon nitride passivation layer laying on top of them.

Based on the data presented in Figure 2. 4(a), Figure 2. 4(b) shows the theoretically obtained wavelength dependent reflectivity graph, based on *dual beam spectrometry* (*DBS)* experimentally obtained refractive indexes (n_{SiO2} and

n_{Si3N4}) of the surface (SiO_2 and Si_3N_4 based) layers. This reflectivity variations shown in Figure 2. 4(b) (in the middle) are the sort of variations that could be expected to be present in the output signal of any photodetector fabricated in this technology; the maximum reflectivity values calculated corresponding to the minimum values of the generated photocurrent within the device, for obvious reasons.



(a)

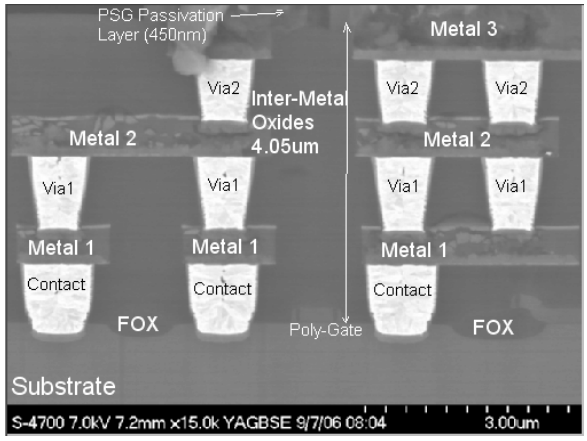


(b)

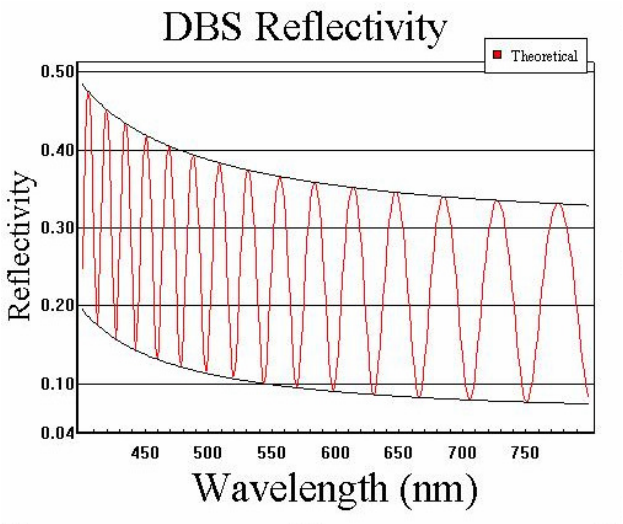
Figure 2. 4 – (a) SEM image of the surface of an integrated circuit fabricated in the 0.5μm CMOS process, where the FOX, BPSG, inter-metal oxides, and the passivation (Ni_3S_4) silicon-nitride layers, as well as the existing three metal layers, can be observed (Courtesy: Dr. S. Dreiner, Fraunhofer IMS); (b) theoretical wavelength dependent reflectivity curve for the structure shown in (a), obtained using the *dual beam spectrometry* (DBS) experimentally determined surface layer refractive indexes (Courtesy: Dr. J. Weidemann, *EL-MOS FEDU*).

As it was expected that the silicon-nitride passivation layer exhibits a heavy absorbance, an alternative passivation was proposed. This consists of a 450nm thick *phosphosilicate glass* (PSG) layer, with much lower absorbance coefficient for the entire spectra, when compared to silicon nitride. Figure 2. 5(a) shows an SEM image of the IC surface, using in this case the PSG passivation layer. Nevertheless, the wavelength-dependent changing reflectivity maxima effect of the surface isolation and passivation layers remained, as it can be observed in Figure 2. 5(b), where the theoretically obtained wavelength dependent reflectivity graph, based on *DBS* experimentally obtained refractive

index (n_{SiO2}) of the now only silicon dioxide based surface layer of interest is shown.



(a)



(b)

Figure 2. 5 - (a) SEM shot of the cross-section of the 4.05μm thick BPSG and the 3 intermetal oxide layers located on the wafer surface, together with the 450nm thick PSG passivation layer for the 0.5μm standard CMOS process under investigation (Courtesy: Dr. S. Dreiner, Fraunhofer IMS); (b) theoretical wavelength dependent reflectivity curve for the structure shown in (a), obtained using the DBS experimentally determined surface layer refractive indexes (Courtesy: Dr. J. Weidemann, EL-MOS FEDU).

To illustrate the impact of the passivation layer on the optical sensitivity and the quantum efficiency of different photodetectors, two identical (300x300)μm^2 *n*-well photodiodes were fabricated, one using the silicon-nitride based passivation shown in Figure 2. 4, and the second one using the PSG alternative shown in Figure 2. 5. Finally, both were characterized, with applied reverse bias at V_{DD}=3.3V and operated at room temperature, to obtain their optical sensitivity values (in A/W) and their quantum efficiencies for the impinging radiation with wavelengths in the range from 300nm (soft UV) to 1100nm (NIR). The compared results can be observed in Figure 2. 6.

For this kind of measurements, the *LOT-Oriel* ozone-free (OF) short-arc 1000W Hg(Xe) lamp was used as a light source for the wavelengths in the range

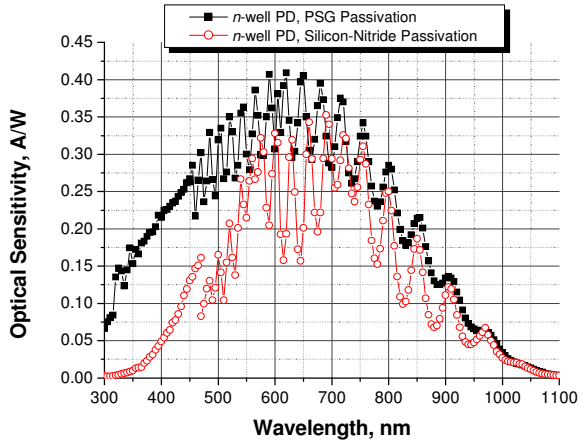
between the 300nm and 450nm. The lamp housing was connected to a monochromator with an optical grid presenting 1200l/mm and a 350nm blaze wavelength, whose output was opto-mechanically coupled to an optical system built on a breadboard, consisting of one bi-convex lens, one plane-convex lens, and three optical diaphragms (Figure A. 4). More details and a complete explanation of the measurement station, developed within the frame of this work, can be found in *Appendix A* at the end of this text.

For the case of impinging radiations with wavelengths between the 450nm and 1100nm, a slightly different approach was used. Here, the 250W *LOT-Oriel* tungsten-halogen lamp delivered a 10Hz electro-mechanical chopper modulated light to the *LOT-Oriel* MSH301 monochromator with two optical output ports and one optical grid presenting 1800l/mm and a 500nm blaze wavelength. More details and a more complete explanation of this measurement station can be found in *Appendix B*, at the end of this text.

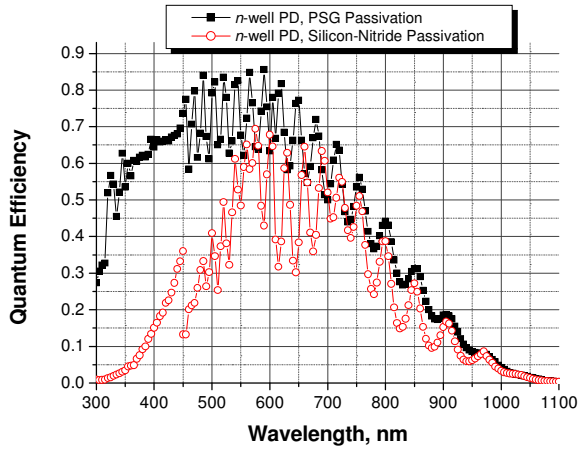
As in each measurement a different optical grid was used within a corresponding monochromator (the one for the wavelength range between the 300nm and 450nm presenting 1200l/mm, and the second one 1800l/mm), the wavelength irradiance distribution of the impinging radiation was different during each measurement. It was wider in the first case, delivering a higher range of different wavelengths to the photodetector surface. This means that, following Figures 2. 3(b) and 2. 4(b), the phase effects on the sum of radiation beams reflected from the surface of the photodetector were less noticeable for the case of the first measurement. This can be observed in Figure 2. 5(a), where the curve shows one behaviour in the range between the 300nm and the 450nm (where the 1200l/mm optical grid was used), and a different one, where the reflectivity maxima variations are easier to observe, in the range between the 450nm and 1100nm (where the 1800l/mm optical grid was used).

The data presented in Figure 2. 6(a) were used to calculate an approximated silicon-nitride passivation layer transmittance coefficient (in %) shown in Figure 2. 6(c) by calculating the ratio between the two graphs. It was assumed that the PSG has a similar absorbance coefficient as the rest of the silicon-oxides used, and that due to the thickness variations of the sum of these layers it could be considered that *S* would not change much when PSG is used, instead of just etching the silicon-nitride passivation layer, which would be more correct.

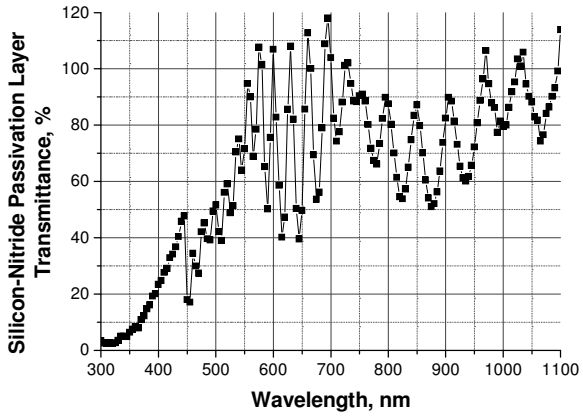
Proceeding in this way, in Figure 2. 6(c) it can be observed that the transmittance of the silicon-nitride passivation layer is around 5% at 300nm wavelengths and it starts growing until it reaches 100% at 580nm, decreasing again in the range between 720nm and 950nm wavelengths. The transmittance values above 100% are due to the reflectivity phase shifts between one test structure and the other caused by the difference in the inter-metal oxide and passivation layers thickness. Starting from 700nm wavelength, it could be assumed that the difference between the two structures is not significant any more as they reach the NIR part of the spectra, which can be clearly seen in Figures 2. 6 (a) and (b).



(a)



(b)



(c)

Figure 2. 6 – (a) Experimentally obtained wavelength dependent optical sensitivity (in A/W) for the two (300x300)μm^2 identical *n*-well photodiodes, fabricated using silicon-nitride as a passivation layer in the first case, and PSG in the second; (b) wavelength dependent quantum efficiency curves obtained for (a); (c) wavelength dependent silicon-nitride passivation layer transmittance curve (in %).

As it was already explained, and according to Eq. (2. 10), the wavelength dependent reflectivity curve maximas and minimas (caused by the phase shifting of the reflected radiation) are strongly related to the layer thickness. For different inter-metal oxide layers the wavelength dependent reflectivity maxima variation frequency will change and eventually diminish. Shown in Figure 2. 7 is the comparison between the theoretically obtained reflectivity curves for oxide layer thickness of 3500nm, 3753nm, and 4000nm, respectively, where the frequency and phase changes between the different curves are easy to observe. Nevertheless, thinning the surface inter-metal isolation layers until a specific thickness is reached at which this effect diminishes is quite an elaborate process which requires a very high thickness accuracy, not reachable within the available standard CMOS process under investigation.

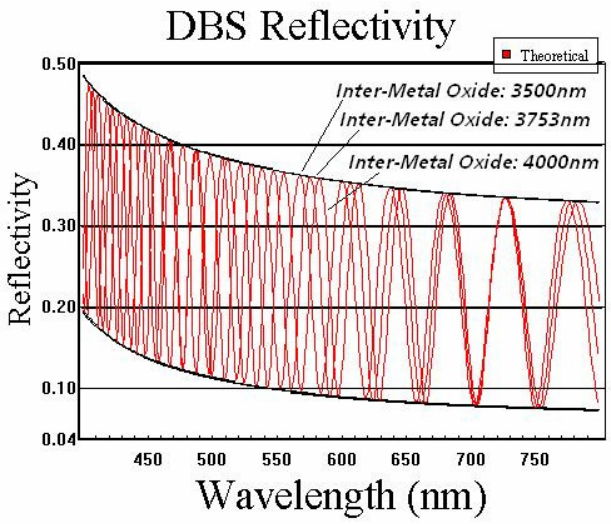


Figure 2. 7 - Comparison of the theoretical wavelength dependent reflectivity curves obtained for the structure shown in Figure 3. 5(a) and inter-metal oxide layers thickness of 3500nm, 3753nm, and 4000nm, obtained using the DBS experimentally determined surface layer refractive indexes (Courtesy: Dr. J. Weidemann, EL-MOS FEDU).

To avoid this wavelength and isolation thickness dependent reflectivity maxima phase shifts as well as the surface layer irradiation absorbance, both of the effects which directly affect the photodetectors quantum efficiency, the solution is to etch the inter-metal oxide layers existing on top of the photoactive area of any photodetector fabricated in this process. This could be done by introducing an extra mask (and turning this process in an imaging enhanced one) and an extra thin silicon nitride layer deposition, as well as the corresponding nitride layer etching step.

The silicon nitride layer just mentioned and deposited on top of the photoactive area should work as an etch stop. The 60nm thick etch-stop nitride layer should be deposited just after the polysilicon oxidation fabrication step, i.e. before the source/drain implantations, as well as before the BPSG reflow. If the LOCOS based field-oxide layer is avoided on top of the photoactive area (using the same extra mask used for etch-stop nitride layer or the special *gate-oxide* mask in the case of the *n*-well PD), then at the end there will exist only the

passivation 450nm PSG layer on top of the photoactive area. A schematic diagram of this last structure can be observed in Figure 2. 8.

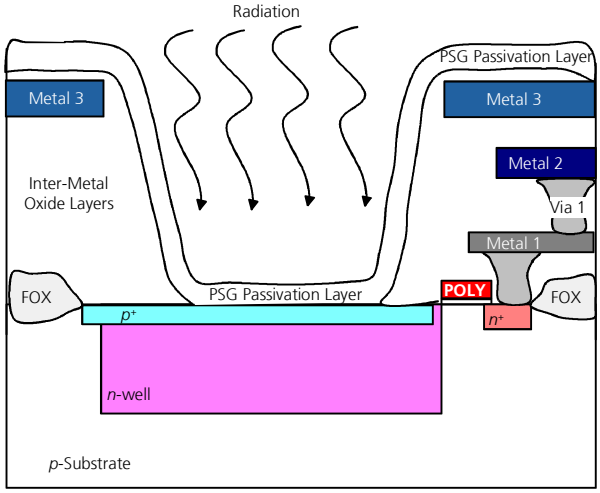


Figure 2. 8 – Schematic diagram of the photodetector surface layer structure proposed to reduce the surface layer radiation absorption and reflection maxima phase shifts.

Nevertheless, this solution still exhibits the reflection maxima interference, as it can be observed in Figure 2.9, where the theoretically obtained reflectivity curve for the 450nm PSG passivation layer is shown, varying between the 80% and 90%. Moreover, etching of around 3μm thick oxide layers is also not an easy task, which would require a fair amount of investigation on its own.

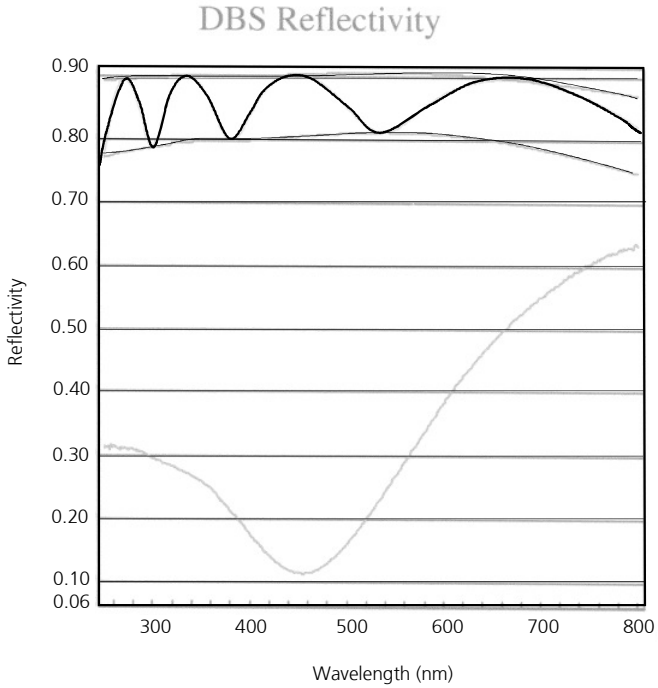


Figure 2. 9 - Theoretical wavelength dependent reflectivity curve for the PSG passivation layer (upper curve), obtained using the DBS experimentally determined surface layer refractive indexes (Courtesy: Dr. J. Weidemann, EL-MOS FEDU).

At the Fraunhofer IMS, there exist previous works dedicated to this issue. For example, in [Bus03] the problem present in this same process was addressed

in 2003. In this work, two additional possible solutions were suggested: 1) the deposition of the so called $\frac{\lambda}{4}$ layer [Eic93], i.e. a layer deposited between those with different refractive indexes (here, the SiO_2 inter-metal layers with the refractive index n_1=~1.46 (at λ=555nm) and the silicon bulk with n_2 = 3.8-5.4 [Bus03]), that should exhibit the refractive index $n_3 = \sqrt{n_1 n_2}$ (for example, Si_3N_4 layer could be considered, as it presents n_{Si3N4}=~2.02, close enough to n_3, unfortunately with all the drawbacks of the irradiation absorption) and thickness of $d_{\lambda/4} = \frac{\lambda_{R,0}}{4n_3}$. This layer would use the reflection phase shift effects in such a way that for a specific wavelength $\lambda_{R,0}$ in vacuum and under perpendicular illumination, the multi-layer system would present a zero reflection factor; and 2) the so called "moth eye effect" application explained by Bernhard in 1967 [Ber67], a wideband effect used in the eyes of a moth which, if illuminated by flash light, present no reflected light what so ever. This effect is due to quasi-continuous refractive index junctions, i.e. an interface consistent of very fine pyramid-like structures whose height and the distance between them is around one half of the minimal wavelength of the incoming radiation [Gom02], a layer of which is used instead of a planar border between the two media.

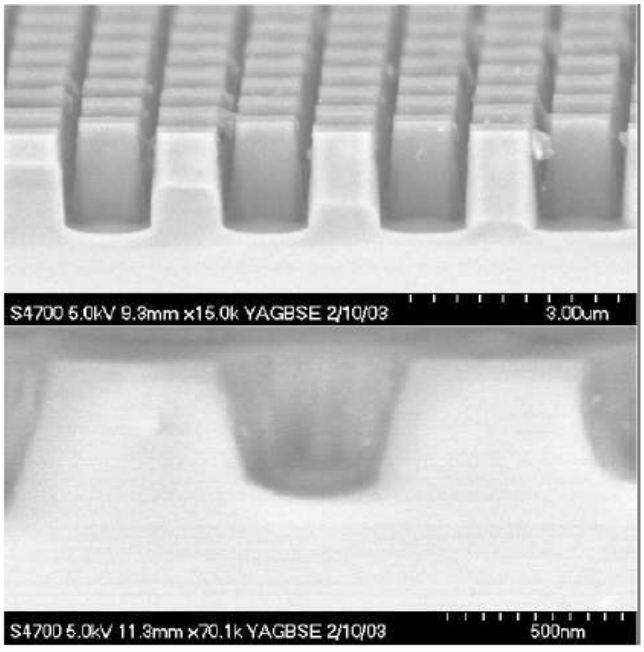


Figure 2. 10 – SEM microphotograph of the cross-section of the perforated passivation layers of *n*-well photodiodes fabricated in the 0.5μm standard CMOS process, for 1.0μm deep structure holes (above), and the 0.5μm deep structure holes (below) [Bus03].

As normally wide-band impinging radiation applications are pursued instead of single wavelength ones, and moreover, as no additional mask or fabrication step has to be integrated in the standard CMOS process under study in order to apply it, the second solution was tested as follows.

The idea was to use the last CMOS process fabrication step, namely the passivation oxide etching step for contact generation, to perform passivation

(PSG) layer perforations as shown in Figure 2. 10 [Bus03] with 0.5μm, 1.0μm, and 2.0μm structure heights and distance between the neighbouring structures. Of course, if the desire is to be working in the VIS-NIR part of the spectra, the structures height and distance should be at the most 200nm, or even better 100nm for the 200nm-1127nm wavelength silicon absorption limits. Nevertheless, at that time, so small structures were not yet possible to fabricate [Bus03] and further attempts stay beyond the scope of this work. Moreover, there were problems of uneven perforation depths oscillating between the 0.5μm and 2.4μm for the same structure layer [Bus03], as well as sub- and over-etching problems, specially on the structure borders where in most cases no oxide perforations were anywhere to see [Bus03].

Figure 2. 11 [Bus03] shows the normalized optical sensitivity of two identical (300×300)μm^2 *n*-well PD structures, with and without the "anti-reflective coating (ARC)" layer. Although the measurement results present a huge amount of noise and no absolute values, it can be observed that for the wavelengths in the range between the 600nm and 750nm of impinging radiation, the amplitude of reflected minima and maxima has actually been diminished.

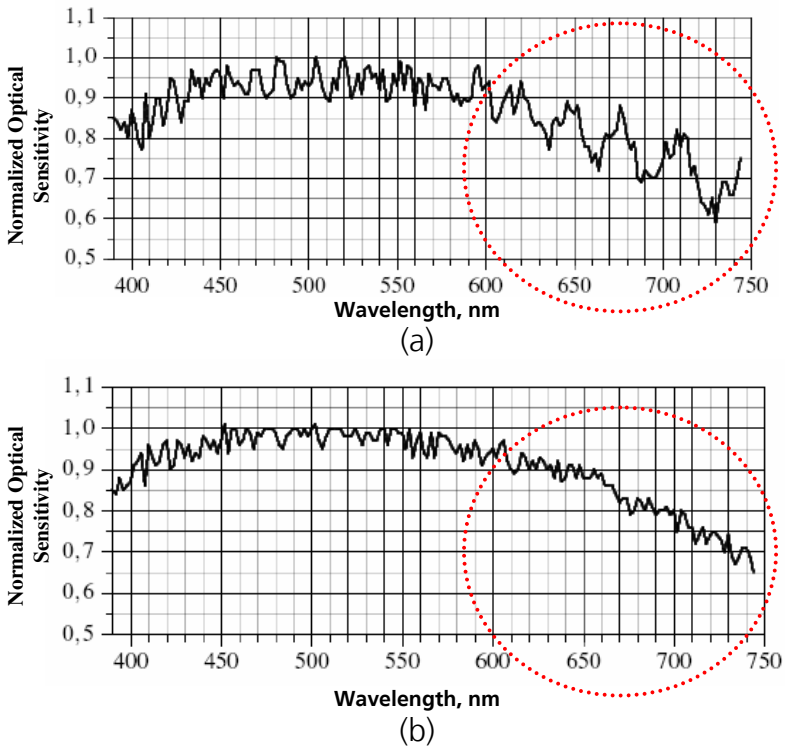


Figure 2. 11 – Normalized optical sensitivity curves (originally in A/W) for the 400nm to 750nm wavelength impinging radiation obtained from two identical (300×300)μm^2 *n*-well PDs: (a) fabricated using the standard PSG based passivation layer in the 0.5μm CMOS process under investigation [Bus03]; and (b) fabricated using the passivation layer 0.5μm perforations, i.e. the anti-reflective coating layer in the same CMOS process [Bus03]. Circles point out the region of the spectra for which the difference can be clearly observed.

Of course, the ultimate solution to this quantum efficiency and photodetector response problem is to perform this kind of anti-reflective coating oxide etching to the passivation layer during the last CMOS process fabrication

step, shaping 100nm deep structures, applied to the structure shown in Figure 2. 8. Nevertheless, a quite acceptable solution for photodetectors fabricated in the process under investigation to be used in VIS-NIR irradiation applications, would be to conserve the inter-metal oxide multi-layer structure and apply the ARC PSG passivation layer on top of it.

2.3 Minority Carrier Lifetimes

As it was already explained in *Chapter 1* of this work, when talking about silicon based phototransduction, one of the main issues addressed are the generation-recombination mechanisms present in the semiconductor. There exist in general three basic *ehp* generation-recombination processes. These are: *Auger*, a radiative, and a thermal one. An *Auger* process is defined as an *ehp* recombination followed by a transfer of energy from the recombined *ehp* to a free carrier, which is then excited to a high energy level within the conduction band. The inverse *Auger* effect, in which an *ehp* is produced, is called *impact ionisation* [Bre99]. On the other hand, in a radiative recombination event, an *ehp* recombines with the emission of a photon. The electron recombines from the conduction band with a hole in the valence band. The energy lost by the electron is equal to the sum of its excess kinetic energy and the energy gap of the material. A photon exhibiting precisely this amount of energy is produced. Radiative generation events of an *ehp* occur (*extrinsic photoeffect*) from the absorption of a photon of energy greater than or equal to the bandgap energy. Thermal recombination and generation events arise from phonon emission or absorption, respectively [Bre99], when operating at any temperature above the absolute zero.

When speaking about generation and recombination mechanisms in a semiconductor, it is unavoidable to introduce the concept of carrier lifetimes. For Schroder [Sch98], lifetimes fall into two primary categories: *recombination lifetimes* and *generation lifetimes*. The concept of recombination lifetime τ_r, holds when excess carriers decay as a result of recombination [Sch98]. In other words, it is the time during which a minority carrier can survive surrounded by majority carriers, before it recombines. Generation lifetime τ_g, applies when there is a paucity of carriers, as in the SCR of a reverse-biased photodiode or a photogate, and the device tries to attain equilibrium, i.e. the generation time is the time it takes on average to generate an *ehp*.

At high carrier densities, the lifetime in silicon is controlled by *Auger* recombination and at low densities by multiphonon (thermally originated) recombination. *Auger* recombination has the $1/n^2$ or $1/p^2$ dependence [Sch98], for n and p being the n-type substrate and p-type substrate doping concentrations, respectively. The high carrier densities may be due to high doping densities or high excess carrier densities. Whereas multiphonon (thermal) recombination is controlled by the cleanliness of the material, *Auger* recombination is an intrinsic property of the semiconductor [Sch98].

When these generation and recombination events occur in the bulk, they are characterized by τ_r and τ_g. When they occur at the surface, they are

characterized by the *surface recombination velocity* s_r and the *surface generation velocity* s_g [Sch98]. Since devices consist of bulk regions and surfaces, both bulk and surface recombination or generation occur simultaneously, so the measured lifetimes are always effective lifetimes consisting of bulk and surface components [Sch98].

There are two types of states from which a carrier can be generated or into which a carrier can be recombined, namely either band or bound states. Band states are defined simply as states in either the conduction or the valence band of the host semiconductor. Bound states, on the other hand, are defined as states arising from the presence of impurities or imperfections in the host semiconductor crystal. Unintentionally introduced impurities typically form levels nearer the middle of the bandgap. As a result, unlike donor or acceptor states, these impurity states do not readily ionise. They behave more like traps, capturing and later reemitting electrons and holes [Bre99]. The rate at which a carrier moves into the energy level in the forbidden gap (introduced by these "traps") depends on the distance of the introduced energy level from either of the band edges. Therefore, if energy is introduced close to either band edge, recombination is less likely as the electron is likely to be re-emitted to the conduction band edge rather than recombine with a hole which moves into the same energy state from the valence band. For this reason, energy levels near mid-gap are very effective for recombination. Whenever there are impurities or defects in the semiconductor, and their energetic level is approaching the half of the band gap, they are referred as *deep-level impurities* or *Shockley-Read-Hall* (SRH) generation-recombination centres. Since semiconductors always contain some impurities, this mechanism is always active. It is particularly important for indirect band semiconductors as it is, for example, silicon [Sch98].

Three main recombination mechanisms determine the recombination lifetime: 1) SRH or *multiphonon* (thermal) recombination, characterized by the lifetime τ_{SRH}; 2) *radiative* recombination, characterized by τ_{rad}, and 3) *Auger* recombination, characterized by τ_{Auger}. The recombination lifetime τ_r is determined by the three mechanisms according to Eq. (2. 15) [Sch97].

$$\tau_r = \frac{1}{\tau_{SRH}^{-1} + \tau_{rad}^{-1} + \tau_{Auger}^{-1}} \tag{2. 15}$$

During SRH recombinations, *ehp* recombine through deep-level impurities, characterized by the impurity density N_T, energy level E_T in the band gap, and capture cross sections σ_n and σ_p for electrons and holes, respectively [Sch97]. The energy liberated during the recombination event is dissipated by lattice vibrations or *phonons*.

The standard SRH equation for the recombination lifetime $\tau_{SRH}=\tau_{r\text{-}n}=\tau_{r\text{-}p}$, for $\tau_{r\text{-}n}$ being the electron recombination lifetime in a *p*-type substrate and $\tau_{r\text{-}p}$ a hole recombination time in an *n*-type substrate, both defined by Eq. (2. 16) [Sch98], is expressed in Eq. (2. 17) [Sch98], where p_o and n_o are the equilibrium hole and electron concentrations, respectively, Δn and Δp are the excess carrier

densities, v_{th} is the thermal velocity of each minority carrier, and n_1 and p_1 are respectively defined by Eq. (2. 18) [Sch98].

$$\tau_{r-n} = \frac{1}{\sigma_n v_{th} N_T} \text{ and } \tau_{r-p} = \frac{1}{\sigma_p v_{th} N_T} \tag{2. 16}$$

$$\tau_{SRH} = \frac{\tau_{r-n}\left(p_O + p_1 + \Delta p\right) + \tau_{r-p}\left(n_O + n_1 + \Delta n\right)}{n_O + p_O + \Delta n} \tag{2. 17}$$

$$n_1 = n_i \exp\left(\frac{E_T - E_i}{k_B T}\right) \text{ and } p_1 = n_i \exp\left(\frac{-\left(E_T - E_i\right)}{k_B T}\right) \tag{2. 18}$$

Besides SRH bulk recombination there is also SRH surface recombination at bare surfaces or interface recombination at oxide/silicon interfaces. Analogous to the SRH recombination lifetime defined in Eq. (2. 17), the SRH surface recombination velocity s_r is given by Eq. (2. 19) [Sch97]. Here, subscript refers to the appropriate quantity at the surface, and s_{r-n} and s_{r-p} are defined by Eq. (2. 20), for the interface trap density N_{it}, in units of cm^{-2}, assumed constant [Sch97].

$$s_r = \frac{s_{r-n} s_{r-p}\left(p_{0-s} + n_{0-s} + \Delta n_s\right)}{s_{r-n}\left(n_{0-s} + n_{1-s} + \Delta n_s\right) + s_{r-p}\left(p_{0-s} + p_{1-s} + \Delta p_s\right)} \tag{2. 19}$$

$$s_{r-n} = \sigma_{n-s} v_{th} N_{it} \text{ and } s_{r-p} = \sigma_{p-s} v_{th} N_{it} \tag{2. 20}$$

Each of the recombination processes discussed so far has a generation counterpart. Optical *ehp* generation is the counterpart of radiative recombination and impact ionisation is that of *Auger* recombination. The inverse of the SRH recombination mechanism or *multiphonon* recombination is the thermal *ehp* generation, characterized by the generation lifetime τ_g. It is determined by the *Shockley-Read-Hall* (SRH) mechanisms and is the only generation lifetime usually considered, provided optical and impact ionisation generations are negligible. The τ_g is defined by Eq. (2. 21) [Sch98].

$$\tau_g = \tau_{g-p} e^{\frac{(E_T - E_i)}{k_B T}} + \tau_{g-n} e^{\frac{-(E_T - E_i)}{k_B T}} \tag{2. 21}$$

The generation lifetime can be quite long if the impurity energy level E_T does not coincide with E_i. Moreover, τ_g is sometimes written as Eq. (2. 22) [Sch97], in terms of the SHR recombination time τ_r.

$$\tau_g \approx \tau_r e^{\frac{|E_T - E_i|}{k_B T}} \tag{2. 22}$$

As it was already mentioned in *Chapter 1* of this work, dark current is an important parameter to characterize the performance of a photodetector, just as the diffusion length of minority carriers is. As the dark current is nothing else but the flux of thermally generated minority carriers which inevitably takes place at any temperature value above absolute zero and is characterized by the minority carriers generation time, and the diffusion length is square root proportional to the minority carriers recombination times, a proper measurement of these minority carrier lifetimes is essential.

Two measurement techniques were applied to obtain the generation lifetime τ_g and the recombination lifetime τ_r, respectively; namely, the *pulsed MOS-C measuring method* proposed by M. Zerbst in [Zer66] for τ_g and surface generation velocities s_g, and the *steady-state short circuit current method* applied to a grounded *p-n* junction for τ_r experimental determination [Sch97]. Both methods and the experimental results obtained for the 0.5μm standard CMOS process will be now presented.

2.3.1 The *Pulsed MOS-C Measuring Method* Used to Experimentally Determine the Generation Lifetimes and Generation Surface Velocities Present in the 0.5μm Standard CMOS Process

This method is based on the measurement of the relaxation time of a MOS-C when pulsed into deep depletion using a capacitance time variation during this process (a *C-t* plot). Here, the majority carriers are repelled across the depth of the depleted SCR by the depleting voltage pulse. This occurs in a time much shorter than typical *C-t* responses, which last on the order of the capacitance measurement instrument that is the time-limiting element during the capacitance decrease [Sch98].

A MOS-C is originally biased in inversion. If a reverse biasing pulse is afterwards applied between the metal and the semiconductor very rapidly so that neither the charge state of the interface states can change nor an inversion layer can form, then a *deep depletion* situation occurs. In other words, at first no voltage is applied and the capacitance of the device is given by the oxide capacitance C_{ox} (Eq. (1. 43)). Then, the voltage step is applied to the polysilicon gate and a SCR is created. In the absence of an external stimulus such as light, a net generation of *ehp* takes place in the SCR as well as in the quasi-neutral bulk. Both of these effects result in the reduction of W_{SCR} as a function of time and the width of the depletion region relaxes as the inversion layer forms until equilibrium is reached. Namely, a MOS-C pulsed into a deep depletion state returns to the quasi-equilibrium inversion condition (*Chapter 1*) as a result of thermal carrier generation in the bulk and at the surface of the device. Five generation components contribute to its return to equilibrium: 1) *ehp* generation within the bulk SCR (away from the insulator/semiconductor interface) characterized by the generation lifetime τ_g; 2) the SCR "lateral" carrier generation on the surface of the SCR exceeding the area beneath the gate, characterized by the surface generation velocity $s_{g\text{-}S}$; 3) the *ehp* generation in the SCR located under the gate, characterized by the surface generation velocity s_g; 4) quasi-neutral bulk carrier generation, characterized by the minority carrier

diffusion length L_n or L_p; and 5) the back surface carrier generation, characterized by the generation velocity $s_{g\text{-}B}$ [Sch98]. Throughout this time, the device is represented by a series connection of the oxide capacitance C_{OX} and the space-charge capacitance C_s. C_s has a minimum value immediately after the voltage pulse has been applied, i.e. where the SCR is widest and then starts to continually narrow. When equilibrium is reached at t_{final}, the SCR has reached its minimum width and the capacitance assumes its maximum value C_{final}. The MOS-C SCR width W_{SCR} dependence on the MOS-C output capacitance C (containing both capacitances mentioned) can be thus expressed as Eq. (2. 23) [Sch98].

$$W_{SCR} = \varepsilon_O \varepsilon_{Si} \left(\frac{1}{C} - \frac{1}{C_{ox}} \right) \tag{2. 23}$$

If it is assumed that at room temperature the diffusion current can be neglected and the wafer thickness is greater than the minority carrier diffusion length, then the minority carrier generation rate within the SCR can be expressed as Eq. (2. 24) [Sch98], where A_{Gate} is the MOS-C gate area, $A_{SCR\_lateral}$ is the area of the lateral portion of the SCR (assuming the lateral SCR width to be identical to the vertical SCR width W_{SCR}), $W_{SCR} - W_{inv}$ stands for the effective generation region width being W_{SCR} the width of the SCR and W_{inv} the width of the inversion region formed under the MOS-C at t_{final}, s_g the lateral surface SCR generation velocity, and the term $qn_i s_{g\_\text{eff}}$ accounts for the SCR width independent generation rates (surface generation under the gate and in the quasi-neutral region), defined by Eq. (2. 25) [Sch98], for s_g' being the surface SCR under the gate generation velocity, $D_{n/p}$ the electron (n) or hole (p) diffusion coefficient, N_B the bulk doping concentration and $L_{n/p}'$ the electron or hole effective diffusion length.

$$\frac{dQ_n}{dt} = -\frac{qn_i}{\tau_g}\left(W_{SCR} - W_{inv}\right) - qn_i s_g \frac{A_{SCR\_lateral}}{A_{Gate}} - qn_i s_{g\_eff} \tag{2. 24}$$

$$s_{g\_eff} = s_g' + \frac{n_i D_{n/p}}{N_B L_{n/p}'} \tag{2. 25}$$

The effective SCR width (W_{SCR}-W_{inv}) approximates the actual generation width and ensures that at the end of the C-t transient the SCR generation becomes zero [Sch98]. The major uncertainty in estimating the true generation width arises from a lack of knowledge of the quasi-Fermi levels during the transient. If only the SCR generation rates considered in Eq. (2. 24) are taken into account, the effective generation time can be defined using Eq. (2. 26) [Sch98].

$$\frac{dQ_{n\_SCR}}{dt} = -\frac{qn_i\left(W_{SCR} - W_{inv}\right)}{\tau_{g\_eff}} \tag{2. 26}$$

Moreover, from the MOS-C theory it is known that the *ehp* generation rate can be expressed in terms of the output measured capacitance as expressed in Eq. (2. 27) [Sch98].

$$\frac{dQ_n}{dt} = -\frac{q\varepsilon_{Si}\varepsilon_0 C_{OX} N_B}{C^3} \cdot \frac{dC}{dt} \tag{2. 27}$$

Finally, combining Eqs. (2. 23), (2. 24), and (2. 27), the Eq. (2. 28) [Zer66] is yielded which is the basis of the well-known *Zerbst plot*.

$$-\frac{d}{dt}\left(\frac{C_{ox}}{C}\right)^2 = \frac{2C^2}{q\varepsilon_O\varepsilon_{Si}N_B}\left[\frac{q\varepsilon_O\varepsilon_{Si}n_i}{C_{final}C_{ox}\tau_g'}\left(\frac{C_{final}}{C}-1\right)+\frac{qn_i s_{g\_eff}}{C_{ox}}\right] \tag{2. 28}$$

The slope of the *Zerbst plot*, where $\frac{d}{dt}\left(\frac{C_{OX}}{C}\right)^2$ is plotted versus $\left(\frac{C_{final}}{C}-1\right)$, gives τ_g, while its intercept with the *y*-axis gives s_{g_eff}. Here, s_{g_eff} is the effective surface generation velocity which has a maximum value equal to s_g at the beginning of the transient process and then starts decreasing with time due to the screening of SRH generation-recombination centres at the surface with the creation of the inversion layer.

The most useful part of this plot is the linear portion. The curved portion near the origin is when the device approaches equilibrium and the curvature at the other end of the straight line has been attributed to field-enhanced emission from interface and/or bulk traps [Sch98]. The Zerbst plot vertical axis is proportional to the total *ehp* carrier generation rate or to the generation (dark) current, and the horizontal axis is proportional to the SCR generation width.

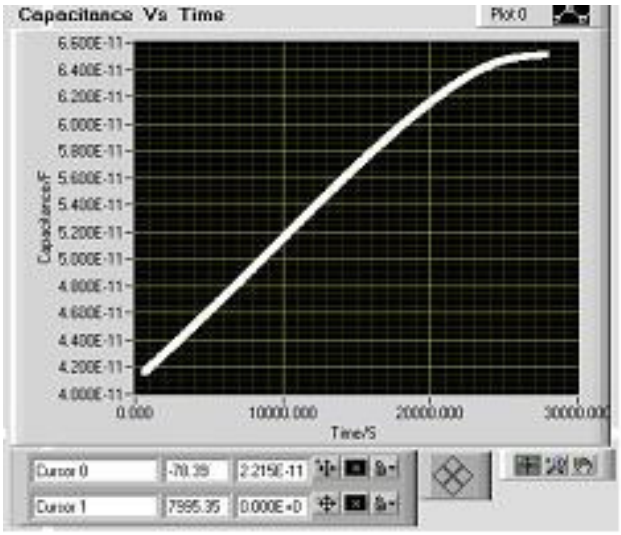
After the proper *Zerbst plot* has been created, based on an experimentally obtained *C-t* graph of a MOS-C, the effective minority carrier generation lifetime τ_{g_eff} can be calculated from Eq. (2. 29) [Mba06, Tch07] for the slope m_{Zerbst} of the linear part of the *Zerbst curve*. On the other hand, the effective surface generation velocity s_{g_eff} can be calculated as shown in Eq. (2. 30) [Mba06, Tch07], for the *y*-axis intercept y_{Zerbst}.

$$\tau_{g\_eff} = \frac{2n_i C_{ox}}{C_s N_B \cdot m_{Zerbst}} \tag{2. 29}$$

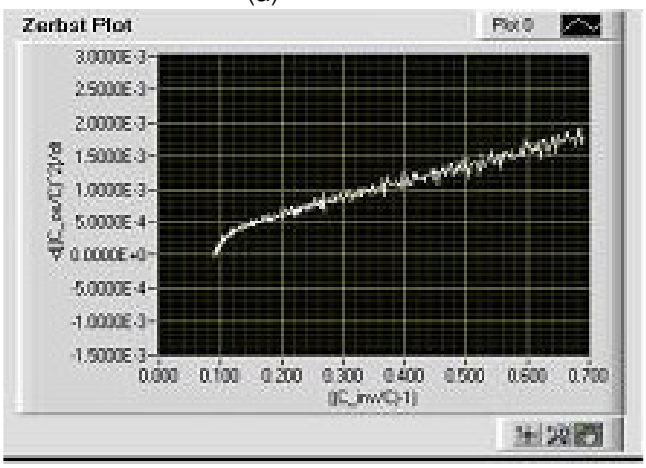
$$s_{g\_eff} = \frac{\varepsilon_{Si} d_{ox} N_B \cdot y_{Zerbst}}{2\varepsilon_{OX} n_i} \tag{2. 30}$$

2.3.1.1 Experimental Results Obtained for the *n*-Type MOS-C Fabricated on *p*-Epi (substrate) in the 0.5μm CMOS Process

Four (300×300)μm^2 square MOS-C based test structures were fabricated in the 0.5μm standard CMOS process under investigation, forming part of the same wafer, located within different dies. At first, capacitance measurements under changing applied bias (*C-V* measurements)[1] were performed on them, delivering the inversion capacitance mean value C_{inv}=70.97pF, gate-oxide capacitance mean value C_{OX}=257.6pF, and substrate doping concentration N_A=1.34×10^{17}cm^{-3} (obtained using the capacitance values mentioned). The measurements were performed using the *Keithley 590* semiconductor analyser in darkness, at room temperature.



(a)



(b)

Figure 2. 12 – (a) The *C-t* graph obtained for one of the *n*-type MOS-C test structures used for the *p*-substrate minority carriers effective generation lifetime and surface velocity characterization, fabricated in the 0.5μm CMOS process [Mba06]; (b) a modified (showing only the filtered linear part) *Zerbst plot* [Mba06] obtained from the *C-t* graph showed in (a).

[1] For a detailed description of the *C-V* and the *C-t* measurements performed in this case, as well as of the measuring station and the software developed for it, consult [Mba06], the bachelor thesis developed within the frame of this work.

Once these values were known, the *C-t* measurements were performed using the same *Keithley 590* device, a standard on-wafer measuring station, and a PC with GPIB data acquisition card available together with a *LabView 6i* based specially developed "*C-t* Measurement" software described in detail in [Mba06]. The *Keithley 590* device was programmed to perform *C-t* measurements applying a 100kHz AC signal superimposed on the applied voltage step with a default 0V bias applied before t=0, and a 3.3V bias applied during the entire measurement until C_{final} is reached. A reading rate of 10 readings per second was initially set and then varied depending on the time-extension of each measurement. All measurements were once again performed in darkness at room temperature.

Figure 2. 12(a) shows a screen shot of the *C-t* graph obtained for one of the four test structures characterised in this way within the special *LabView* based software tool already mentioned. On the other hand, Figure 2. 12(b) shows the modified (presenting only the filtered linear part of it) *Zerbst plot* obtained from the *C-t* graph shown in Figure 2. 10(a).

The results obtained are enlisted in Table 2. 1, presenting the mean effective *p*-Epi (substrate) electron generation lifetime τ_{g_n} = 2.249 ± 0.49 ms, and the mean effective electron surface generation velocity s_{g_n} = 4.75 ± 1.03 μm/s. The capacitance curve reached final saturation C_{final} (Chip 1) = 64.6pF during the first test structure measurement in t_{final} (Chip 1) = 28200s, for the second test structure, C_{final} (Chip 2) = 64.8pF in t_{final} (Chip 2) = 26000s, for the third one, C_{final} (Chip 3) = 64.2pF in t_{final} (Chip 3) = 27000s, and finally, for the fourth one, C_{final} (Chip 4) = 64.7pF in t_{final} (Chip 4) = 27500s.

The internal capacitance of the *Keithley 590* device, as well as the parasitic capacitance effects of about ±2pF originated within the connecting cables between the PC and the devices measured provided a source of error in the *C-t* measurements. Moreover, the mathematical filtering and the generation of the nearly linear curve, from which the sweep and *y*-axis interception values could be extracted, added an additional source of probable uncertainty. Actually, it is because of this step that the results presented here result so different from those presented in [Mba06], although the *Zerbst plots* were based on the same *C-t* measurement results. Taking into account these considerations, an approximate error of 10% to 15% in the final results must be considered.

Table 2. 1

Parameter	*Chip 1*	*Chip 2*	*Chip 3*	*Chip 4*	*Mean Value*
τ_{g_n} (*p*-Epi), s	2.943×10^{-3}	1.913×10^{-3}	1.871×10^{-3}	2.269×10^{-3}	2.249×10^{-3}
s_{g_n} (*p*-Epi), cms^{-1}	5.985×10^{-4}	3.881×10^{-4}	3.907×10^{-4}	5.209×10^{-4}	4.75×10^{-4}

2.3.1.2 Experimental Results Obtained for the *p*-Type MOS-C Fabricated on *n*-well in the 0.5μm CMOS Process

Four additional (300×300)μm^2 square *p*-type MOS-C based test structures were fabricated in the 0.5μm standard CMOS process under investigation. The same measurement station, devices and procedures described in the previous sub-chapter were used for their *C-V* and *C-t* characterizations, respectively[2]. From the *C-V* measurement, the following mean-value parameters were extracted: inversion capacitance C_{inv}=34pF, gate-oxide capacitance C_{OX}=240pF, and the *n*-well substrate doping concentration N_D=1.95×10^{16}cm^{-3}.

The *Keithley 590* device was once again programmed (using the measuring software described before) to perform *C-t* measurements applying a 100kHz AC signal superimposed on the applied voltage step with a default 0V bias applied before *t*=0, and a 3.3V bias applied during the entire measurement, until C_{final} was reached. The *n*-well substrate was biased at 3.3V, while the *p*-type substrate was at all times grounded during the measurement. A reading rate of 10 readings per second was initially set and then varied depending on the time-extension of each measurement. All measurements were once again performed in darkness at room temperature.

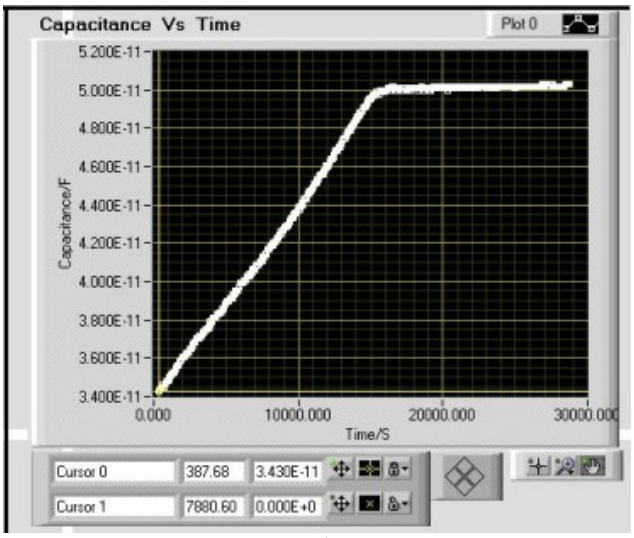
Figure 2. 13(a) shows a screen shot of the *C-t* graph obtained for one of the five test structures characterised in this way within the special *LabView* based software tool. On the other hand, Figure 2. 13(b) shows the modified (presenting only the filtered linear part of it) *Zerbst plot* obtained from the *C-t* graph shown in Figure 2. 13(a) using *Origin*® software tool.

The results obtained from all four test structures are enlisted in Table 2. 2, presenting the mean effective *n*-well electron generation lifetime τ_{g_p} = 639.2 ± 229.6 μs, and the mean effective electron surface generation velocity s_{g_p} = 203.3 ± 59.1 μm/s. Here, it must be stressed that the *p*-type MOS-C structures fabricated on the *n*-well possess a 0.1μm deep p^+ diffusion layer at the surface, aroused through channel implantation used to control the threshold voltage of the PMOSFETs in the process under investigation. This p^+ diffusion layer creates then a *p-n* junction which screens the channel surface avoiding the carriers thermally generated on the surface to reach the SCR created under the gate, i.e. a structure similar to buried CCD photogate is fabricated. So, the surface velocity values obtained in these measurements do not describe the reality unless applied to similar *p*-type MOS-C structures.

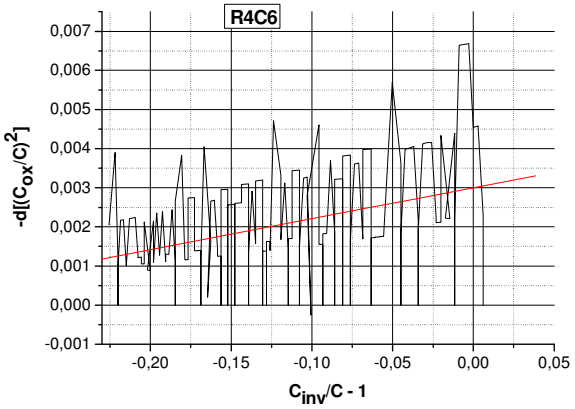
The capacitance curve reached final saturation value C_{final} (Chip 1)=49.2pF during the first test structure measurement in t_{final} (Chip 1)=6500s, for the second test structure, C_{final} (Chip 2)=49.6pF in t_{final} (Chip 2)=8000s, for the third one C_{final} (Chip 3)=49.7pF in t_{final} (Chip 3)=8500s, and finally, for the fourth one C_{final} (Chip 4)=50pF in t_{final} (Chip 4)=16000s. The temperature proved to be a huge factor (as it was expected) determining the results of the present

[2] For a detailed description of the *C-V* and the *C-t* measurements performed in this second case, consult [Kab07], another bachelor thesis developed within the frame of this work.

characterization. Nevertheless, generation lifetime and surface generation velocity values are expected to vary on the same wafer depending on the position of the test structure of interest on it.



(a)



(b)

Figure 2. 13 - (a) The *C-t* graph obtained for one of the *p*-type MOS-C test structures used for the *n*-well minority carriers effective generation lifetime and surface velocity characterization, fabricated in the 0.5μm CMOS process [Kab07]; (b) a not modified *Zerbst plot* [Kab07] obtained from the *C-t* graph showed in (a).

Once again, taking into consideration the measurement and mathematical approximation errors described in the last sub-chapter, an approximate error of 10% to 15% in the final results must be considered.

Table 2. 2

Parameter	*Chip 1*	*Chip 2*	*Chip 3*	*Chip 4*	*Mean Value*
τ_{g_P} (*n*-well), s	474.4×10^{-6}	786.1×10^{-6}	414.5×10^{-6}	882×10^{-6}	639.2×10^{-6}
s_{g_p} (*n*-well), cms^{-1}	23.4×10^{-3}	20.55×10^{-3}	25.4×10^{-3}	11.98×10^{-3}	20.33×10^{-3}

2.3.2 Minority Carriers Recombination Lifetime and Diffusion Length Measurements Based on the *Steady-State Short-Circuit* Optical Method

According to Schroder [Sch98], in the *surface photovoltage* (SPV) steady-state technique for determining the minority carrier diffusion length using optical excitation, the wafer surface with induced SCR is uniformly illuminated by chopped monochromatic light of energy higher than the band gap, with the back surface kept in dark. The light is chopped to enhance the *signal-to-noise ratio* (SNR) using lock-in techniques (already explained in the sub-chapter 2.2 and the *Appendix B* of this work). The wavelength is varied during the measurement.

Here, a *p*-type semiconductor wafer is considered, exhibiting thickness d_W, reflectivity R, minority carriers (electrons) recombination lifetime τ_{r_n}, minority carriers diffusion coefficient D_n, minority carriers diffusion length L_n, and surface recombination velocities s_{r_n1} and s_{r_n2} at the two surfaces. Monochromatic light of photon flux density Φ_{ph}, wavelength λ, and absorption coefficient α (Figure 1. 3), is incident on one side of this wafer. It is assumed that the photogenerated carriers diffuse in the z direction (sub-chapter 1.3) and that the wafer has an infinite extent in the x-y plane. This allows to neglect the edge effects [Sch98]. The steady-state, small-signal excess (photogenerated) minority carrier density $\Delta n_{ph}(z)$ is obtained from a solution to the one-dimensional continuity equation, Eq. (2. 31) [Sch98], subject to boundary conditions expressed in Eq. (2. 32) [Sch98].

$$D_n \frac{d^2 \Delta n_{ph}(z)}{dz^2} - \frac{\Delta n_{ph}(z)}{\tau_{r\_n}} + G(z) = 0 \tag{2. 31}$$

$$\left.\frac{d\Delta n_{ph}(z)}{dz}\right|_{z=0} = s_{r\_n1} \frac{\Delta n_{ph}(0)}{D_n}, \text{ and } \left.\frac{d\Delta n_{ph}(z)}{dz}\right|_{z=d_W} = -s_{r\_n2} \frac{\Delta n_{ph}(d_W)}{D_n} \tag{2. 32}$$

The generation rate is in this case given by Eq. (2. 33), for the quantum efficiency η.

$$G(z,\lambda) = \eta \Phi_{ph}(z) \alpha(z) [1 - R(\lambda)] e^{-\alpha(\lambda) z} \tag{2. 33}$$

The solution to Eq. (2. 31) using the boundary condition from Eq. (2. 32), as well as Eq. (2. 33) is presented in detail in the *Appendix C* of this work together with the detailed analysis of the case when instead of the wafer piece, a *p*-*n* junction is considered.

In the *steady-state short-circuit* method, which is related to the SPV method, the sample must contain an n^+-p junction and the short-circuit current flowing within the grounded junction is measured as a function of wavelength. The current density for the short-circuited structure of Figure 1. 4 is obtained by considering only the diffusion current of electrons J_n in the *p*-Epi and the

diffusion current of holes J_p in the *n*-well. An implicit assumption is that there are no voltage drops across the *n*-well and *p*-Epi regions and that the drift currents are negligible there. This is not quite the case within the epitaxial layer under investigation, although the drift currents are still considered negligible. In the SCR the electric field is dominant, and recombination is negligible as it is explained in *Appendix C* of this work.

For this task, n^+ photodiode test structures were used. Here, the short-circuit current density is given by Eq. (2. 34) [Sch98], according to Eq. (C. 7), assuming that the undepleted wafer (~750μm of the silicon bulk wafer and 5.4μm of the undepleted Epi-layer) is much thicker than the diffusion length (normally around 30μm), that the SCR (W_{SCR}≈0.05μm) is small when compared to L_n, that the absorption coefficient α is sufficiently low for $\alpha W_{SCR} << 1$, but sufficiently high for $\alpha(d_W - W_{SCR}) >> 1$ (which is ensured by using VIS to NIR radiations in the way described in *Appendix B* of this work), that the measured diameter is large compared to the sample thickness allowing a one-dimensional analysis, and finally that low-injection prevails.

The diffusion length is generally low for heavily doped layers, allowing the second term to be neglected for the n^+-*p* junction used, converting Eq. (2. 34) into Eq. (2. 35).

$$J_{sc} \approx q\eta(1-R)\Phi_{ph}\left(\frac{L_n}{L_n+1/\alpha}+\frac{L_p}{L_p+1/\alpha}\right) \tag{2. 34}$$

$$J_{sc} \approx q\eta(1-R)\Phi_{ph}\left(\frac{L_n}{L_n+1/\alpha}\right) \tag{2. 35}$$

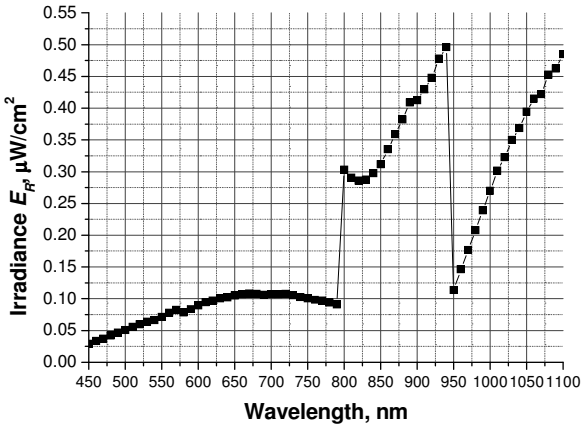
Eq. (2. 35) can be also written as Eq. (2. 36) if X is defined as $X = q\eta(1-R)\Phi_{ph} / J_{sc}$ and $1/\alpha$ (Figure 1. 3) is plotted against $(X\text{-}1)$. The diffusion length is in this case given by the slope of the plot obtained. Moreover, as the measuring station used in this characterization, described in *Appendix B*, delivers wavelength dependent irradiance $E_R(\lambda)$ and not Φ_{ph}, the new X is defined as Eq. (2. 37). Here, A_{n+_PD} = (300×300)μm^2 is the photoactive area of the n^+ photodiode used, I_{ph} is the photocurrent, *h* the Planck constant and *c* the speed of light in vacuum (photon energy $E_{ph}=hc/\lambda$, Eq. (1. 15))[3]. For the reflectivity value *R*, the middle value (R = 0.3) was taken from the theoretically calculated wavelength dependent reflectivity curve based on experimentally determined refractive indexes of the IC surface layer shown in Figure 2. 5(b).

$$\frac{1}{\alpha(\lambda)} = (X(\lambda)-1)L_n \tag{2. 36}$$

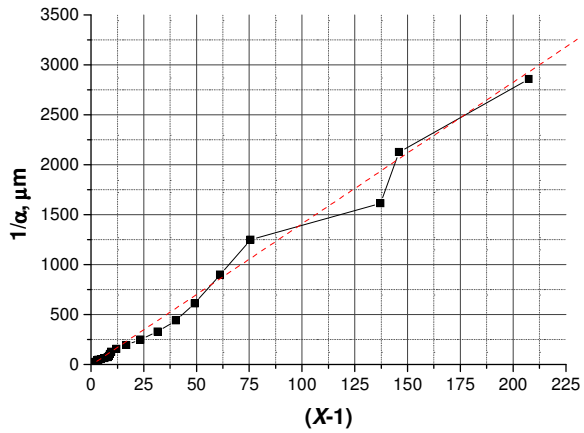
[3] For a detailed description of measurements performed in this case, consult [Kab07], a bachelor thesis developed within the frame of this work.

$$X(\lambda) = \frac{q\eta(1-R)A_{n^+\_PD}\lambda E_R(\lambda)}{I_{ph}(\lambda)hc} \tag{2. 37}$$

Four (300×300)μm^2 n^+ PD test structures were characterized, all belonging to the same wafer but distributed along it within different dies. In all cases, the substrate cathode, as well as the n^+ PD anode were grounded, while the structures were being illuminated by a 10Hz chopper-modulated monochromatic light (*Appendix B*) with wavelengths ranging from 450nm (VIS) to 1100nm (NIR). The photocurrents were measured with a lock-in technique. Figure 2. 14 shows one of the *steady-state short-circuit* graphs obtained, also including the impinging irradiance values.



(a)



(b)

Figure 2. 14 – (a) Impinging radiation irradiance values, in μW/cm^2, for the case of n^+ PD test structure diffusion length L_n characterization using the *steady-state short-circuit* optical measuring method; (b) radiation penetration depth $1/\alpha$ vs. (X-1) graph obtained for the conditions shown in (a), from which sweep L_n value is calculated.

Table 2. 3 summarizes the data obtained for all four test structures of interest. The electron effective lifetime τ_{r_n} obeys $\tau_{r\_n} = L_n^2/D_n$.

Table 2. 3

Parameter	*Chip 1*	*Chip 2*	*Chip 3*	*Chip 4*	*Mean Value*
L_n, μm	28.33	24.17	58.08	16.5	31.77
τ_{r_n}, s	2.13×10^{-7}	1.55×10^{-7}	8.95×10^{-7}	7.22×10^{-7}	4.96×10^{-7}

From the data presented in Table 2. 3, it can be easily calculated that the minority carriers (electrons) diffusion length in the *p*-Epi (substrate) is $\overline{L_n} = 31.77\,\mu m$ (± 18.21μm), and its lifetime $\overline{\tau_{r\_n}}$ = 496.2ns (± 368.2ns). If it is considered that the diffusion length holds also for holes within a supposed *n*-well, then the holes recombination lifetime can be expressed as shown in Table 2. 4, following $\tau_{r\_p} = L_p^2/D_p$.

Table 2. 4

Parameter	*Chip 1*	*Chip 2*	*Chip 3*	*Chip 4*	*Mean Value*
L_p, μm	28.33	24.17	58.08	16.5	31.77
τ_{r_p}, s	6.11×10^{-7}	4.45×10^{-7}	2.57×10^{-6}	2.07×10^{-7}	9.58×10^{-7}

2.4 Reverse Biased p-n Junction Based Photodetectors Fabricated in the 0.5μm Standard CMOS Process Under Investigation

In this sub-chapter, the *n*-well photodiode, the n^+ photodiode, and the *n*-well photodiode with an additional p^+ implantation on the surface called the *buried photodiode* will be analysed in detail. All the photodetectors have been fabricated in the 0.5μm standard CMOS process under investigation.

2.4.1 Reverse Biased *p-n* Junction Based Photodetector Dark Current Considerations

A full discussion of the behaviour of a *p-n* photodiode is normally highly impractical, as it would require solving the *Poisson's* equation, the time dependent continuity equation and the generation-recombination process equation, simultaneously. This discussion is rather involved, as a set of partial differential equations has to be solved. On the contrary, a simpler formulation for the current flow, namely the *Shockley equation*, is to be taken here instead; where the formulation of the current flow is derived under the assumptions that the depletion region width W_{SCR} is abrupt (ends in a "stepwise" manner) and the non-degenerate conditions hold throughout the structure, i.e. the *Boltzmann* distribution approximation to the carrier densities holds on both, the *p* and the *n* sides, respectively [Bre99]. In this case, the minority carrier sources are to be considered independently in order to obtain the expressions for the dark current flow in the reversed biased *p-n* junction, i.e. the *n*-well photodiode.

Sources of dark current of an *n*-well photodiode normally considered [Bre99] are:

1. *Thermal generation of minority carriers in the quasi-neutral areas within a diffusion length of the SCR boundary*, characterized in terms of a

diffusion current. Here, the existence of the *n*-region and the *p*-region must be taken into account with holes and electrons as minority carriers, respectively, in each case. It is assumed that at the edge of the SCR, the minority carrier concentration is zero and that it increases exponentially to the thermal equilibrium value. For the *p*-Epi substrate, such profile of the minority carriers can be written as $n = \frac{n_i^2}{N_A}\left(1 - e^{-\frac{z}{L_n}}\right)$; the expression $p = \frac{n_i^2}{N_D}\left(1 - e^{-\frac{z}{L_p}}\right)$ being valid for the *n*-well. A rough three-dimensional view of an *n*-well PD can be seen in Figure 2. 15. The electron current I_{diff_n} flowing into the SCR from the *p*-Epi substrate due to diffusion of electrons is then expressed by Eq. (2. 38). Here, $A_{n\text{-}diff}$ is the area through which the electron diffusion current flows into the SCR generated on the junction, i.e. the *n*-well PD area A_n for the portion of the diffusion current flowing along the *z* axis (Figure 2. 15), and the area formed by the *n*-well perimeter P_n and the *n*-well depth $d_{n\text{-}well}$ for the portion of the diffusion current flowing along the *x* and *y* axis into the lateral SCR of the *n*-well, valid only if the lateral *n*-well borders are considered to be rectangular and perpendicular to the wafer surface. The total minority carriers diffusion current flowing in the reverse biased *n*-well PD is expressed in terms of the minority carriers recombination lifetime and equilibrium concentrations as expressed by Eq. (2. 38).

$$I_{diff\_n} = -qD_n A_{n-diff}\frac{dn}{dz} = -qD_n A_{n-diff}\frac{n_i^2}{N_A}\frac{1}{L_n}e^{-\frac{z}{L_n}}\Big|_{z=0} = -\frac{qA_{n-diff}D_n n_i^2}{L_n N_A} \qquad (2.\ 38)$$

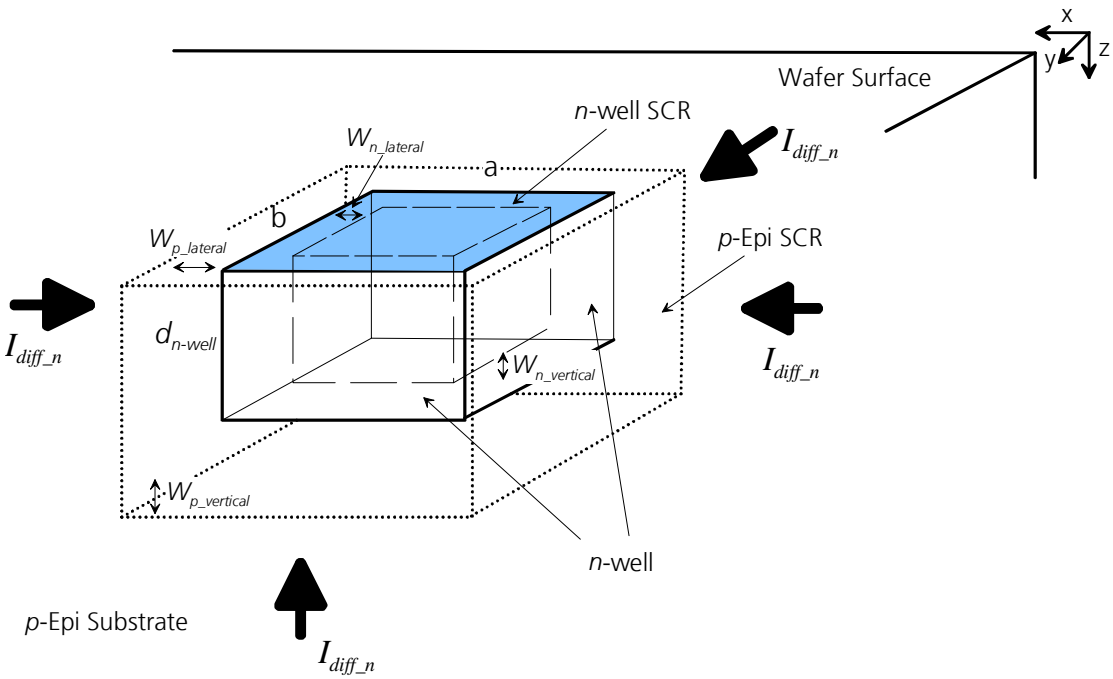


Figure 2. 15 – Three dimensional view of an *n*-well photodiode.

2. *Minority carrier generation within the depletion region*, where carriers generated within the depletion region are swept out by the electric field and thus constitute a depletion or drift current. The dark drift current considers the minority electrons generated within the *p*-Epi SCR and is expressed in terms of Eq. (2. 39). Here, the electron drift current area A_{depl_n} consists again of the area of the *n*-well A_n for the portion of the electron drift current generated within the SCR located at the "bottom" side of the *n*-well, added to the area formed by the *n*-well perimeter P_n and the depth $d_{n\text{-}well}$ of the lateral walls of the *n*-well, for the *n*-well "lateral" SCR.

$$I_{drift\_n} = -\frac{qn_i A_{depl\_n}}{\tau_{g\_n}} \tag{2. 39}$$

3. *Generation of minority carriers out of fast surface states*, which depends highly on the silicon surface crystalline defects. It is characterized for the purposes of this work as the length-dependent dark current arising from the *p-n* junction at the area where the SCR reaches the wafer surface. It is defined as shown in Eq. (2. 40) [Sch98], assuming the low-level injection, for the electron surface generation velocity s_{g_n} within the *p*-Epi substrate SCR at the wafer surface.

$$\left|I_{surface\_dark}\right| = qn_i P_n W_{p\_lateral} s_{g\_n} \tag{2. 40}$$

4. *Background flux generation*, the current generated by the incident background flux, expressed in Eq. (2. 41), for the quantum efficiency η, and the background photon flux Φ_B. Due to the 5.5μm thick epitaxial layer existence on top of the 750μm thick silicon bulk, this term is here negligible and will not be taken into account for further calculations.

$$\left|I_{background-flux}\right| = Aq\eta\Phi_B \tag{2. 41}$$

5. *Dark current term due to tunnelling and impact ionization*. It becomes important in highly doped junctions, which have a narrow depletion layer with relatively short tunnelling distances [Lou03]. At higher applied voltages, tunnelling is overtaken by the impact ionization followed by avalanche breakdown. Both tunnelling (band-to-band and trap assisted) and impact ionization mechanisms depend strongly on the electric field inside the structure. Tunnelling is also most important in narrow-bandgap materials. For the case of interest, it also results negligible.

Finally, the expression for the total amount of dark current flowing in a reverse biased *n*-well photodiode results as shown in Eq. (2. 42).

$$\left|I_{dark}\right| = qn_i\left[\begin{array}{l} A_n\left(\frac{n_i}{N_A}\sqrt{\frac{D_n}{\tau_{r\_n}}}+\frac{W_{p\_vertical}}{\tau_{g\_n}}\right)+P_n d_{n-well}\left(\frac{n_i}{N_A}\sqrt{\frac{D_n}{\tau_{r\_n}}}+\frac{W_{p\_lateral}}{\tau_{g\_n}}\right)+ \\ +P_n W_{p\_lateral} s_{g\_n} \end{array}\right] \quad (2.\ 42)$$

Based on Eq. (2. 42), it can be concluded that the amount of dark current flowing within a reverse biased *n-well* photodiode increases with the increased amount of impurities present in the silicon bulk that decrease the minority carrier lifetimes. Also, the dark current increases its value with the increase of the SCR width, i.e. the increase of the area of the *n*-well or its perimeter on one side, and the biasing voltage on the other which holds square root dependence to the drift current (Eq. (1. 37)). Moreover, the amount of dark current is also very temperature dependent. This can be concluded from the n_i temperature dependence expressed in Eq. (2. 43) [Sze02], where m^* is the effective mass (around 0.25 of the electron mass m_0), and N_C and N_V the effective carrier concentration in the conduction and valence bands, respectively. Additionally, there exist also the D_p and D_n temperature dependence (Eq. (1. 22)), the carrier mobility as well as E_g temperature dependence [Sze02], and finally, the minority carrier lifetime temperature dependences (Eq. (2. 21) and the thermal velocity v_{th} in Eq. (2. 16)) already explained in the previous sub-chapter. If it is considered that an electron can make a transition from any state in the valence band to any state in the conduction band, being the most likely transitions from states near the top of the valence band to states near the bottom of the conduction band, then the last part belonging to Eq. (2. 43) [Sze02] represents a good approximation, where m^* is the effective mass (around 0.25 of the electron mass m_0), and $c_{CV} \approx 5\times10^{19}\text{cm}^{-3}$ is the concentration prefactor.

$$n_i = \sqrt{N_C N_V}\, e^{-\frac{E_g}{2k_B T}} = 2\left(\frac{m^* k_B T}{2\pi\hbar^2}\right)^{\frac{3}{2}} e^{-\frac{E_g}{2k_B T}} \approx c_{CV}\left(\frac{m^*}{m_0}\right)^{\frac{3}{2}}\left(\frac{T}{300K}\right)^{\frac{3}{2}} e^{-\frac{E_g}{2k_B T}} \quad (2.\ 43)$$

As the doping concentrations and the concentration of impurities, i.e. the carrier lifetime values, are normally fixed in standard CMOS processes, the dark current can be controlled to a certain level through proper geometric design of the photodetector, i.e. its area and perimeter extensions, as well as through the biasing voltage and the operation temperature. Another measure that helps reducing the amount of dark current in a photodetector is the so called "screening" of the silicon surface or the elimination of the term expressed by Eq. (2. 40) from the dark current, i.e. the introduction of a grounded p^+ diffusion (*source/drain* diffusion present in the PMOSFET, shown in Figure 2. 1) on top of the *n*-well, that "pushes" the peak of the electrostatic potential present within the SCR away from the surface in the *z*-axis direction (Figure 2. 15), as explained more in detail later on in this chapter.

2.4.2 *n*-well Photodiode (*n*-well PD)

As it was already explained throughout this text, the *n*-well photodiode consists of an ~1.5μm deep *n*-well, fabricated within the *p*-Epi substrate and

surrounded by *p*-well diffusions due to the twin-well fabrication technology of this process. It presents a modulated doping profile with an average concentration of around N_D=1×10^{17}cm^{-3} in the middle.

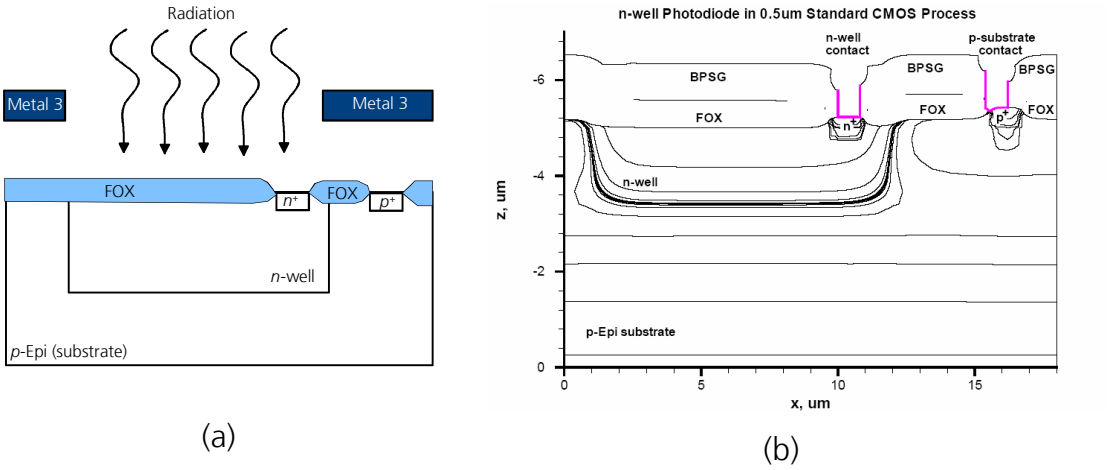


Figure 2. 16 – (a) Schematic of an *n*-well photodiode; (b) two-dimensional doping profile simulation results for the *n*-well photodiode fabricated in the 0.5μm CMOS process under investigation obtained using TCAD process and device simulation software.

The schematic of this photodetector structure, as well as the two-dimensional doping concentration graph, obtained after the structure was simulated considering all the fabrication steps present in the 0.5μm CMOS process using TCAD software, can be observed in Figure 2. 16. In Figure 2. 16(a), the *Metal 3* layer is used to define the photoactive area.

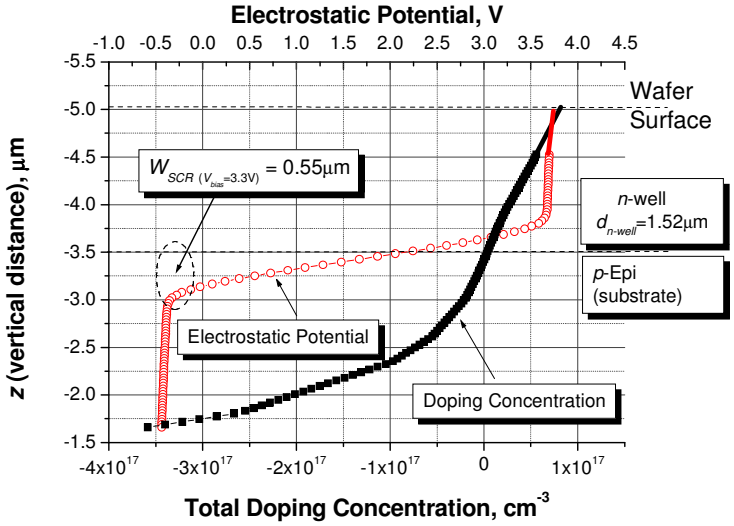


Figure 2. 17 – Total doping concentration graph together with the electrostatic potential one obtained form a vertical cut done to the two-dimensional simulation result shown in Figure 2. 13(b) when the *n*-well PD is reverse biased at V_{DD}=3.3V.

For a better understanding of the doping profile and the behaviour of the photodetector under different reverse biasing conditions, the total doping concentration and electrostatic potential data were extracted along a vertical cut

line (parallel to the *z*-axis) performed to the two-dimensional simulation data display shown in Figure 2. 16(b) at x = 7μm, for the structure reverse biased at V_{DD}=3.3V. The total doping concentration graph together with the one describing the electrostatic potential at the cut can be observed in Figure 2. 17. The 1.51μm deep *n*-well structure can be recognized in Figure 2. 17, as well as the 0.55μm wide SCR within the *p*-Epi substrate. The SCR width inside the *n*-well is in this case 0.48μm.

Moreover, Figure 2. 18 shows the *p*-Epi substrate SCR width bias dependence extracted from the TCAD simulation results for both, the case of the vertical cut (shown in Figure 2. 17) and for the data extraction cut perpendicular to the *z*-axis, performed at z = 4.5μm, for the case shown in Figure 2. 16(b), respectively. Also, Figure 2. 18 shows *n*-well SCR width bias dependence, again for both cases.

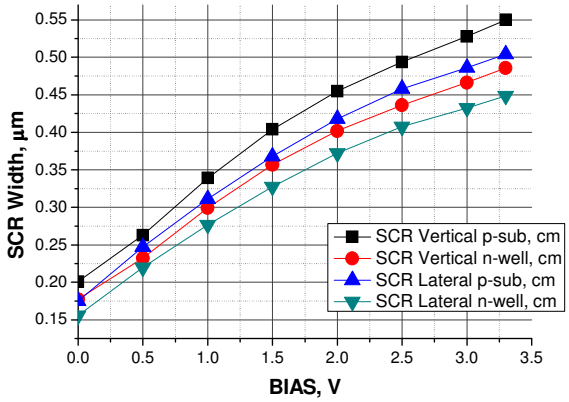


Figure 2. 18 – *p*-Epi substrate SCR width bias dependence extracted from the TCAD simulation results for both, the case of the vertical cut (shown in Figure 2. 14) and for an extraction cut perpendicular to the *z*-axis at z = 4.5μm for the case shown in Figure 2. 13(b); *n*-well SCR width bias dependence is also shown.

2.4.3 *Buried* Photodiode (BPD)

The *buried* photodiode structure consists of the same ~1.5μm deep *n*-well already described, on top of which the ~0.2μm deep p^+ diffusion (PMOSFET *source/drain*) is fabricated, exceeding the *n*-well borders in about 0.6μm in the *x*-*y* direction (Figure 2. 15) to screen the SCR (W_{SCR}=0.55μm under V_{DD}=3.3V biasing) formed within the *n*-well on one side and within the *p*-Epi substrate on the other, from the silicon surface. The measure eliminates the part of the dark current originated out of fast surface states and expressed by Eq. (2. 44), and thus significantly reduces the overall dark current. If the complete depletion of the *n*-well could be reached by the overlapping SCRs created at the *n*-well – *p*-Epi substrate junction on one side and at the p^+ - *n*-well junction on the other, it should also increase the quantum efficiency of the photodetector for impinging radiation with wavelengths between 400nm (soft UV-blue part of the spectra) and 550nm (green light), with absorption lengths of $1/\alpha$=0.1μm-1.5μm (Figure 1. 3) due to the elimination of the diffusion process losses within the *n*-well. A buried photodiode with a fully depleted well, in which case the electrostatic

potential within the *n*-well becomes "pinned", is often called a *pinned photodiode* (PPD).

The schematic of this photodetector structure, as well as the two-dimensional doping concentration graph, obtained after the structure was simulated, considering all the fabrication steps present in the 0.5μm CMOS process, using TCAD software, can be observed in Figure 2. 19. The depth of the surface p^+ diffusion in Figure 2. 19(b) exceeds 0.2μm (value obtained from spread-resistance measurements performed) due to the fact that the TCAD software, lacking the diffusion parameter values for BF_3 molecules (much bigger and with smaller diffusivity than B_2) implanted and diffused during the fabrication, used the models proper of boron atoms.

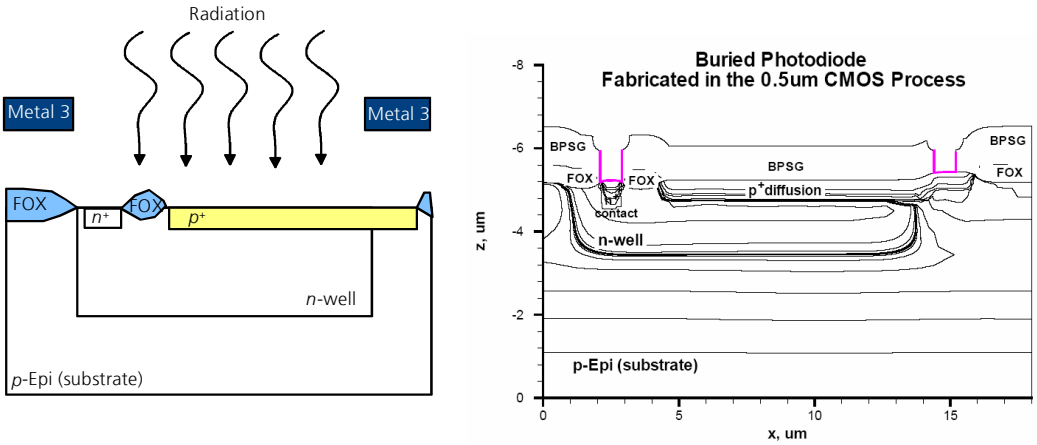


Figure 2. 19 - a) Schematic of a *buried* photodiode; (b) two-dimensional doping profile simulation results for the *buried* photodiode fabricated in the 0.5μm CMOS process under investigation obtained using TCAD process and device simulation software.

Figure 2. 20 shows the total doping concentration (in cm^{-3}) and the electrostatic potential profile within the BPD structure when biased at V_{DD}=3.3V. The total doping concentration and electrostatic potential data shown in Figure 2. 20 were extracted along a vertical cut line (parallel to the *z*-axis) performed to the two-dimensional simulation data display shown in Figure 2. 19(b) at x = 10μm. Here, the electrostatic potential peak can be observed as being "pushed" away from the surface by the grounded p^+ diffusion. If compared to the *n*-well PD, this structure also presents a diminished well capacity, as the new *n*-well depth is now 1.3μm (in comparison to the original 1.5μm).

However, Figure 2.20 shows that for this particular CMOS process the two SCR do not overlap in the *n*-well, so that the *n*-well cannot be fully depleted. Hence, this yields a diminished quantum efficiency in the UV part of the spectra due to the reduced absorption length (of around of tens of nanometres) of the impinging radiation, i.e. the photogeneration of carriers within the grounded p^+ layer where they finally stay. Moreover, as instead of creating a device exhibiting a single capacitance due to the fully depleted *n*-well, i.e. generating the *pinned* photodiode structure, here, a parallel connection of two capacitors (the p^+-*n*-well junction and the *n*-well-*p*-substrate one) exists. So,

the overall output capacitance of the photodiode should be expected to be higher than the one presented by the *n*-well photodiode. Finally, the SCR width bias dependences follow the values presented in Figure 2. 18.

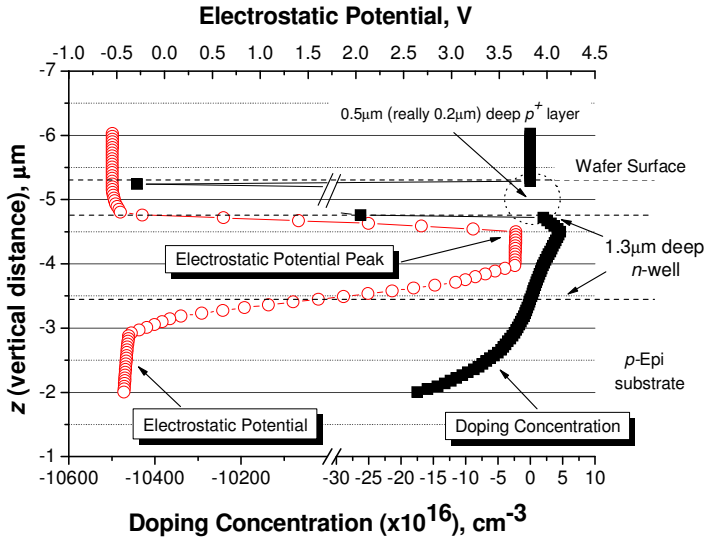


Figure 2. 20 - Total doping concentration graph together with the electrostatic potential one obtained form a vertical cut done to the two-dimensional simulation result shown in Figure 2. 16(b) for the *buried* PD reverse biased at V_{DD}=3.3V.

2.4.4 n^+ Photodiode (n^+ PD)

The n^+ photodiode consists of one 0.3μm deep n^+ diffusion (NMOSFET *source/drain*) with a peak donor concentration of N_D=1.5×10^{20}cm^{-3}, fabricated on top of the *p*-well diffusion. The schematic of this photodetector structure as well as the two-dimensional doping concentration graph, obtained after the structure was simulated considering all the fabrication steps present in the 0.5μm CMOS process, using TCAD software, can be observed in Figure 2. 21.

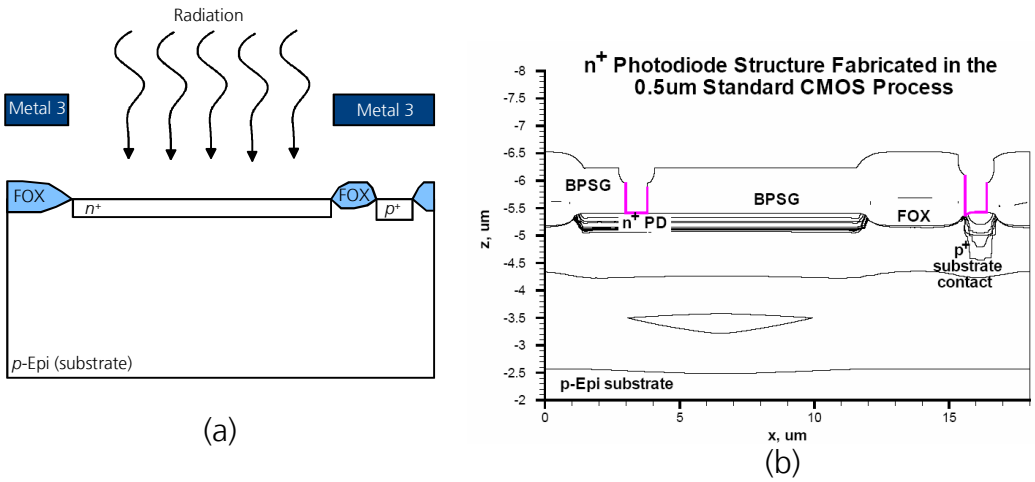


Figure 2. 21 - a) Schematic of an n^+ photodiode; (b) two-dimensional doping profile simulation results for the n^+ photodiode fabricated in the 0.5μm CMOS process under investigation obtained using TCAD process and device simulation software.

An important characteristic of this kind of photodetectors is the fact that the generated photocurrent depends on its drift part only for wavelengths of impinging radiation until the 465nm ($1/\alpha$=0.55μm). For radiations above this wavelength value, almost the entire photocurrent depends then on its diffusion part, although impact ionisation mechanisms start playing a significant role, as shown in [Lou03].

Figure 2. 22 shows the total doping concentration (in cm^{-3}) and the electrostatic potential profile (in volts) within the n^+ PD structure when reverse biased at V_{DD}=3.3V. The total doping concentration and electrostatic potential data were extracted along a vertical cut line performed to the two-dimensional simulation data display shown in Figure 2. 21(b) at x = 8μm.

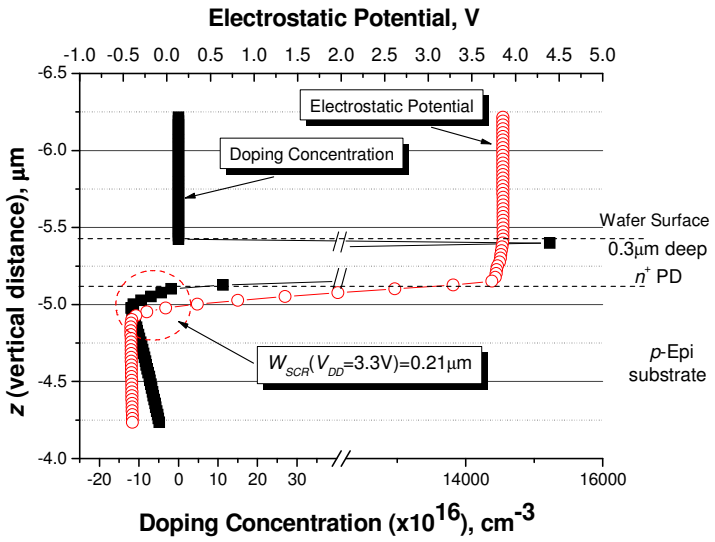
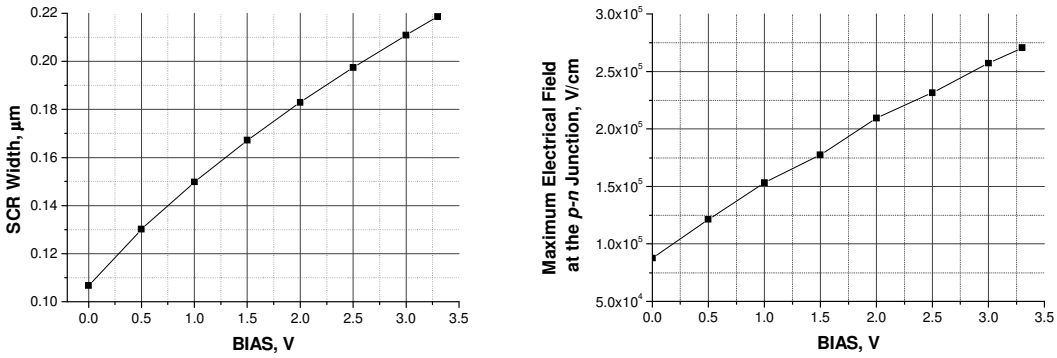


Figure 2. 22 - Total doping concentration graph together with the electrostatic potential one obtained form a vertical cut done to the two-dimensional simulation result shown in Figure 2. 21(b) for the n^+ PD reverse biased at V_{DD}=3.3V.

Extracted from two dimensional simulations performed using the TCAD software at different biasing voltages, and in almost perfect correspondence with Eq. (1. 37), the SCR width biasing dependence can be observed in Figure 2. 23(a), varying between the 0.107μm under 0V and the 0.21μm under V_{DD}=3.3V. Moreover, in Figure 2. 23(b), the maximum electrical field F_{max} at the *p-n* junction for different biasing conditions just described can also be observed.



(a) (b)

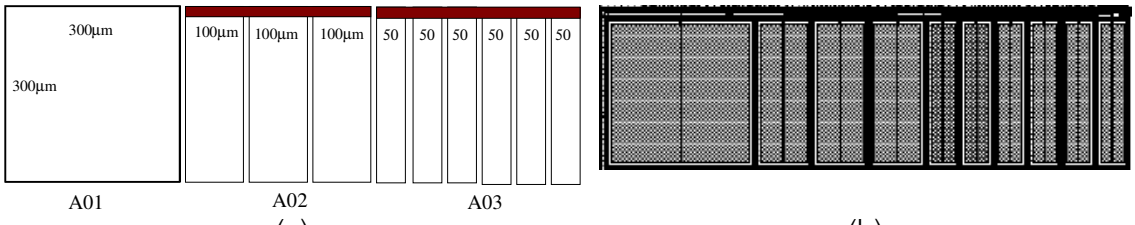
Figure 2. 23 – (a) *p*-Epi substrate SCR width bias dependence extracted from the TCAD simulation results of n^+ PD structures fabricated in the 0.5μm CMOS process under investigation; (b) maximum electrical field at the *p*-*n* junction for the same case.

2.4.5 Reverse Biased *p*-*n* Junction Based Photodetectors Electrical and Optical Characterization

All three reverse biased *p*-*n* junction based photodetector structures were fabricated in the 0.5μm standard CMOS process under investigation and then characterized, as it will be explained in this sub-chapter.

2.4.5.1 Dark Current (*I*-*V*) Measurements

Three different kinds of *n*-well PD, BPD and n^+ PD based test structures were fabricated in the 0.5μm standard CMOS process. They all present the same area: (300×300)μm^2, but different perimeter values, namely: P_1=1200mm, P_2=2400μm, and P_3=4200μm. The schematics of all the three test structure types, namely A01, A02, and A03, as well as the layout developed with *Cadence*® design tool for their fabrication, can be observed in Figure 2. 24.



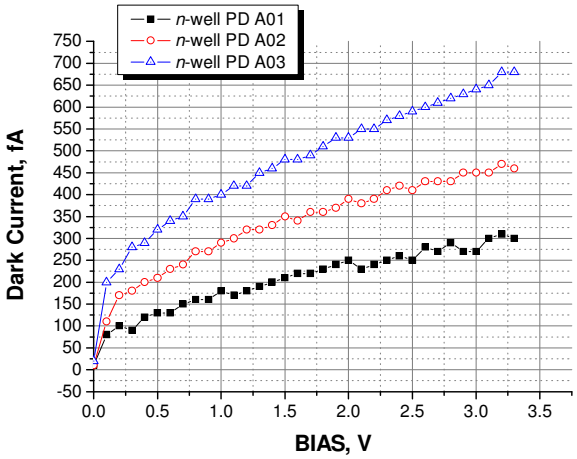
(a) (b)

Figure 2. 24 – (a) Schematic diagram of the A01, A02, and A03 *n*-well PD, BPD, and n^+ PD based test structures; (b) *Cadence*® developed layout for the fabrication of the test structures shown in (a).

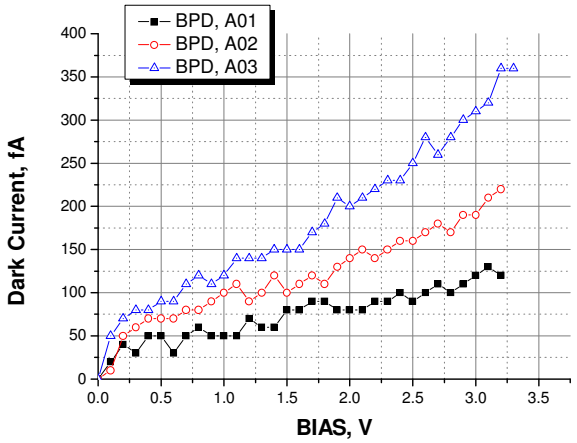
The dark current measurement averaged results for all three test structure types are to be found in Figure 2. 25. The measurements were performed using the *Hewlett Packard HP4155B Semiconductor Analyser* device, at room temperature, long integration times, and voltage steps of 100mV.

It is crucial for a proper photodetector design to be able to predict the amount of its dark current. Just as well, it is important to understand in detail all the mechanisms of the dark current generation to be able to optimise the

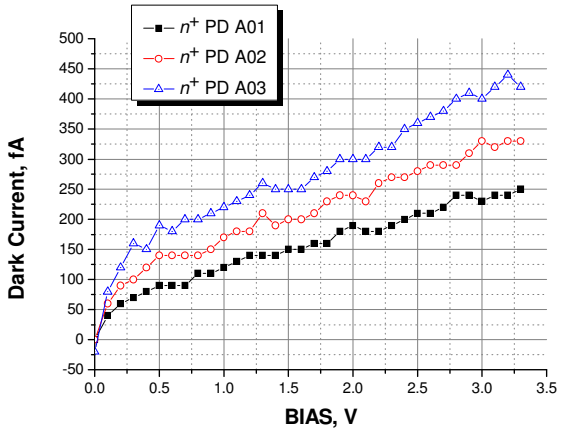
photodetector in this sense. So, the first attempt here was to try to theoretically reproduce the experimental results shown in Figure 2. 25, using Eq. (2. 42), and the minority carrier lifetimes measured for the 0.5μm CMOS process under investigation.



(a)



(b)



(c)

Figure 2. 25 – Dark current (*I-V*) averaged measured bias dependence for A01, A02, and A03 test structure types shown in Figure 2. 21, for: (a) *n*-well PD, (b) BPD, and (c) n^+ PD.

Although the modulated doping profile within the photodiode requires a proper mathematical model, here instead, the average impurity concentrations were considered present at different depths inside the silicon epitaxial layer. Based on spread resistance measurements for the case of the *n*-well PD and the BPD, these were N_D=1×10^{17}cm^{-3} and N_A=2×10^{17}cm^{-3} considered for the vertical diffusion part of the dark current, whilst N_D=5×10^{16}cm^{-3} and N_A=8×10^{16}cm^{-3} for the lateral diffusion. For the n^+ PD structures, the impurity concentrations were N_D=2×10^{19}cm^{-3} and N_A=2×10^{16}cm^{-3} for both directions.

Moreover, for the calculations considered, besides n_i=9.65×10^{9}cm^{-3} [Sze02], D_n=37.7 cm^2/*V*·s, and D_p=13.13 cm^2/*V*·s, proper for all test structures, A_n(A01)=(300×300)μm^2, P_n(A01)=0.12cm, $d_{n\text{-}well}$=1.5μm, τ_{r_n}=4.96×10^{-7}s, τ_{r_p}=9.58×10^{-7}s, the W_{SCR} values shown in Figure 2. 18, τ_{g_p}=767.1×10^{-6}s, and s_{g_n}=4.75×10^{-4}cms^{-1} were considered for the case of the *n*-well PD. As it was already explained, the s_{g_p} value lacks meaning if applied to the case of an *n*-well PD, so the s_{g_p} value was taken here instead, for both SCR regions, namely the *n*-well and the *p*-Epi substrate ones. On the other hand, the same theoretical approximation was performed for the case of the BPD test structures, eliminating the surface dark current term (Eq. (2. 40)) from the mathematical model presented in Eq. (2. 42), and considering A_n(A01)=(296×296)μm^2, P_n(A01)=0.1184cm, and $d_{n\text{-}well}$=1.3μm, valid for the fabricated BPD A01 test structures. All the other parameters remained identical in both cases. For the n^+ PD structures, again Eq. (2. 42) was used for theoretical calculations of the dark current. The results obtained for all three A01 test structures can be observed in Figure 2. 26.

If the plots shown in Figure 2. 26(a) and (c) are compared, namely the theoretical and measured curves for the case of the *n*-well PD A01 and BPD A01 (Figure 2. 26(c)), respectively, the curves obtained for the BPD A01 structure are in much more acceptable agreement than those belonging to the *n*-well PD.

Keeping in mind that the only difference between the *n*-well PD and the BPD curves consists in the elimination of the dark current part originated from the fast surface states in the second case, it can be concluded that if a higher surface velocities s_{g_p} and s_{g_n} are considered, a better approximation between the theoretical and measured curves could be reached for the case presented in Figure 2. 26(a). So, if instead of $s_{g\_p} = s_{g\_n}$ = 4.75×10^{-4} cm/s, the value of 4.5cm/s is taken, the new theoretical curve fits almost perfectly the measured one for the case of the *n*-well PD, as it can be observed in Figure 2. 26(b).

For the case of the n^+ PD shown in Figure 2. 26(d), the situation is slightly more complicated. The exponential behaviour of the measured curve in Figure 2. 26(d) can be explained only through the consideration of *tunnelling* and *impact ionisation* mechanisms [Hur92] neglected in Eq. (2. 42). Tunnelling becomes important in highly doped junctions, which have a narrow depletion layer with relatively short tunnelling distances [Hur92]. Not only *band-to-band tunnelling* but also *tunnelling via traps* can be important. The band-to-band tunnelling

describes transitions of electrons which tunnel directly from valence band to the conduction band [Huk92], dominating the reverse characteristics of heavily doped diodes (here, N_D=2×10^{19}cm^{-3}) with breakdown voltage below approximately 6V [Huk92]. The contribution of the band-to-band tunnelling to the dark current can be expressed as shown in Eq. (2. 44) [Huk92]. Here, F_{max} is once again the maximum electric field (the electric field at the *p-n* junction) under different biasing conditions, F_0 is a constant which depends on the temperature through the temperature dependence of the bandgap E_g (F_0 ~ $E_g^{3/2}$=1.9×10^{7}V/cm at room temperature), U is the bias voltage, and c_{bbt} is the temperature independent prefactor [Hur92].

$$J_{btb} = c_{bbt} U \left(\frac{F_{\max}}{F_0} \right)^{\frac{3}{2}} e^{-\frac{F_0}{F_{\max}}} \tag{2. 44}$$

On the other hand, *tunnelling via traps* influences the conventional SRH mechanisms (Eq. (2. 42)) through the function $\Gamma = 2\sqrt{3\pi}\frac{|F|}{F_\Gamma} e^{\left(\frac{F}{F_\Gamma}\right)^2}$ [Huk92] which accounts for the effects of tunnelling on both, the density of captured carriers by a trap and the emission of carriers from a trap, with F_Γ defined by Eq. (2. 45), where F is the local electric field and m^* (m^*=0.25m_0 [Huk92]) is the effective mass of carriers. Eq. (2. 46) [Huk92] accounts for the dark current density contribution due to tunnelling via traps mechanism, for W_{SCR_0} being the SCR of the n^+ PD at zero bias. The SRH recombination rate is under reverse bias approximately constant in the SCR, except within a distance of W_{SCR}/2 from the SCR boundaries [Huk92], behaviour approximated by $c_{SRH} = \frac{n_i}{2\tau_g \cosh\left[(E_T - E_i)/k_B T\right]}$, being E_T the energy level of the traps inside silicon.

$$F_\Gamma = \frac{\sqrt{24 m^* (k_B T)^3}}{q\hbar} \tag{2. 45}$$

$$|J_{tat}| = q\sqrt{3\pi} c_{SRH} W_{p\_vertical} \frac{f_\Gamma}{|F_{\max}|} \left[e^{\left(\frac{F_{\max}}{F_\Gamma}\right)^2} - e^{\left(\frac{F_{\max} W_{SCR\_0}}{F_\Gamma W_{p\_vertical}}\right)^2} \right] \tag{2. 46}$$

Finally, the total dark current flowing within an n^+ PD can be expressed as shown in Eq. (2. 47), considering the SRH generation, band-to-band tunnelling and tunnelling via traps mechanisms. At higher applied voltages, tunnelling is usually overtaken by the impact ionisation followed by avalanche breakdown, which for maximum bias of V_{DD}=3.3V is not the case.

$$\left|I_{dark}\right| = qn_i\left[A_n\left(\frac{n_i}{N_A}\sqrt{\frac{D_n}{\tau_{r\_n}}} + \frac{W_{p\_vertical}}{\tau_{g\_n}} + \left|J_{btb}\right| + \left|J_{tat}\right|\right) + P_n\left(W_{p\_lateral}s_{g\_n}\right)\right] \qquad (2.\ 47)$$

Figure 2. 26(d) shows the comparison between the experimentally obtained and the theoretically calculated (according to Eq. (2. 47)) bias dependent dark current curves for the case of the n^+ PD A01 test structure. Here, A_n(A01)=(300×300)μm^2, P_n(A01)=0.12cm, d_{n+PD}=0.2μm, $\tau_{r\_n}=\tau_{r\_p}$=4.96×10^{-7}s, the W_{SCR} values shown in Figure 2. 23(a), τ_{g_p}=767.1×10^{-6}s, s_{g_n}=4.75×10^{-4}cms^{-1}, F_{max} values shown in Figure 2. 23(b), c_{bbt}=8.33A/V, and c_{SRH}=38.16×10^{14}cm^{-1}s^{-1} were the corresponding quantities used for the calculations.

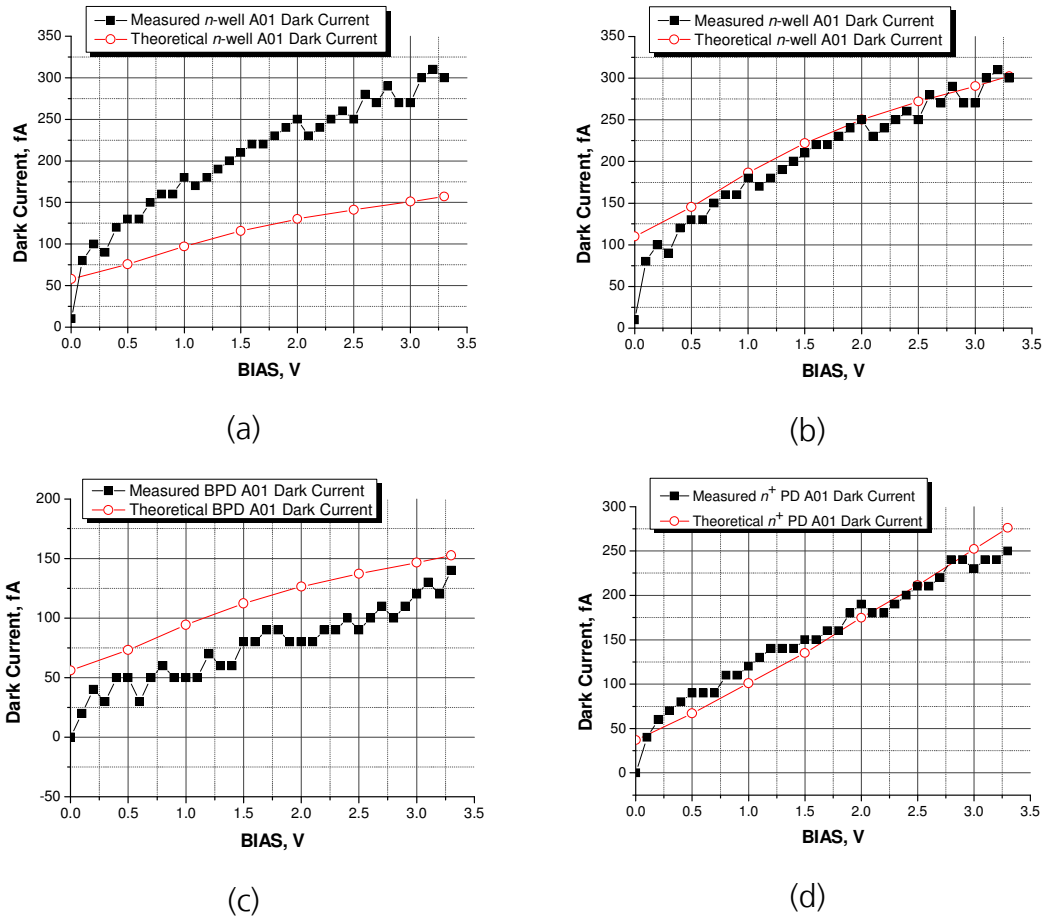


Figure 2. 26 – Comparison of theoretically obtained and measured dark currents for the A01 test structures: (a) *n*-well PD using the experimentally obtained minority carriers lifetimes and surface velocities; (b) corresponds to a case of the *n*-well PD, where the theoretical dark currents were obtained using fitted surface velocities; (c) BPD; and (d) n^+ PD.

On the other hand, although it can be concluded from Figures 2. 16(a) and 2. 26(c) that the problem of non-ideal matching between the theoretical calculations and the actually measured dark current within the *n*-well PD A01 structures might be hidden in the thermal generation of minority carriers out of surface states, taking in mind that the theoretically obtained curve for the case of the BPD A01 structure approximates much better the measured one. If the same procedure is applied to structures A02 and A03, the theoretical curves fail,

specially for the case of the *n*-well PD, although remaining in an acceptable current range (of hundreds of fempto amperes). The reason for this can be found in so many approximations made to develop the mathematical model, as well as in the measuring errors made during each experiment, ranging from minority carrier lifetimes measurements on one extreme to the *I-V* measurements on the other. For example, the generation lifetimes obtained using the pulsed MOS-C method, even if we neglect all the possible measurement errors, are valid only for the region of 0.16μm (SCR width below the MOS-C gate, as it will be explained in on of the following sub-chapters) below the wafer surface and is reasonable to expect them to change at the 1.5μm depth, where the *n*-well PD SCR is originated, mostly due to the modulated doping profile. Here, the temperature should be thoroughly monitored during each measurement, introducing the pertinent changes in the mathematical model, following Eq. (2. 43). Moreover, the reflection factor considered to be 0.3 (average value taken from the graph shown in Figure 2. 5(b)) does not represent the reality, as the wavelength dependent reflectivity should be constantly monitored and considered during the diffusion length measurements in the *steady state short-circuit optical method*. Also, the surface velocity values were difficult to obtain, as the sweep and the *y*-axis intersection of the *Zerbst plot* depend mostly on the curve filtering and its linear approximation. Finally, the "edges" of the *n*-well and the n^+ diffusion considered to form a right angle between them, which is not the case, and other geometry factors were also neglected. So, proper geometry factors [The96, Yad04] should be also introduced to obtain acceptable matching, specially in A02 and A03 test structures.

The list of probable errors is long. Some of them, as the reflectivity factor and temperature monitoring, can be avoided through a better planning of the measurement process (not possible for the moment at the Fraunhofer IMS where the measurements took place), being on the other hand, those similar to the change in the minority carrier generation time, if considered at the *p-n* junction depth in the silicon bulk, impossible to avoid, at least with the methods followed.

Taking all of this into account, it was decided to adopt a different approach, considering exclusively the measured dark currents at identical photodetector structure types, but with different areas and perimeters.

Considering the different areas (although it is not the case here) and the different perimeters of each set of test structures, namely A01, A02, and A03, the equation system following Eq. (2. 48) can be deduced introducing the concepts of the *specific area dependent dark current density* $J'_{dark}(A)$ measured in A/cm^2, and the *specific perimeter dependent dark current density* $J'_{dark}(P)$, measured in A/cm. Eq. (2. 49) shows the analytical solution to the common specific area dependent dark current density $J'_{dark}(A)$, if only two test structures are considered, obtained from Eq. (2. 48), where $I_{darkA01}$ and $I_{darkA03}$ are the measured dark currents of for example, A01 and A03 structures, respectively, A_1 and A_2 their areas, and P_1 and P_2 their respective perimeters. Eq. (2. 50) shows the analytical solution of the Eq. (2. 48) for the specific perimeter dependent

dark current density $J'_{dark}(P)$. Of course, the higher the number of different structures with notoriously different areas and perimeters considered, the more accurate become the results regarding $J'_{dark}(A)$ and $J'_{dark}(P)$.

$$I_{dark} = J'_{dark}(A) \cdot A_n + J'_{dark}(P) \cdot P_n \tag{2. 48}$$

$$J'_{dark}(A) = \frac{I_{dark2} P_1 - I_{dark1} P_2}{P_1 A_2 - P_2 A_1} \tag{2. 49}$$

$$J'_{dark}(P) = \frac{I_{dark1} A_2 - I_{dark2} A_1}{P_1 A_2 - P_2 A_1} \tag{2. 50}$$

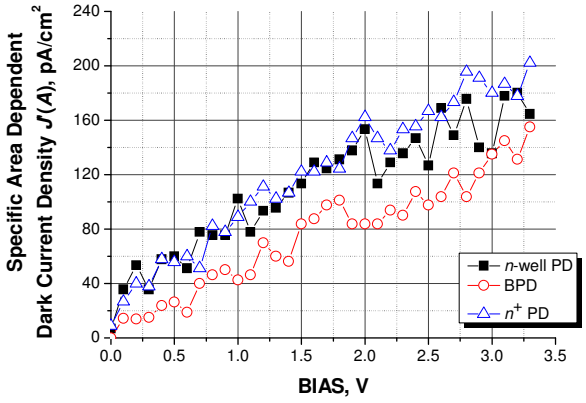
Finally, the plots showing the specific area dependent dark current density $J'_{dark}(A)$ versus reverse bias voltage for all *n*-well PD, BPD, and n^+ PD structures fabricated in this process can be found in Figure 2. 27. In the same figure, we can find the specific perimeter dependent dark current density $J'_{dark}(P)$ voltage dependence.

Figures 2. 25 and 2. 27 proved most of the theory developed in this chapter to be valid. If the dark currents measured for the A01 (Figure 2. 25) are considered, then it can be concluded that the BPD dark current was much lower than the one of the *n*-well PD (almost 41.66% lower) due to the screening of the surface fast states via the p^+ diffusion.

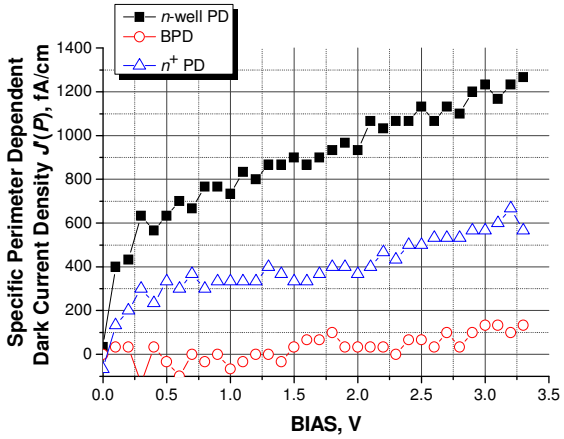
From Figure 2. 27 on the other hand, it can be concluded that for the case of the *n*-well PD A01, the area contribution to the total dark current was of 49.5%, whilst the perimeter contributed with the remaining 50.5%. For the case of the BPD, the area was responsible of 87.4% of the total dark current, whilst the perimeter of the remaining 12.56%, being the area dependence of the n^+ PD responsible of the 68.8% of the dark current, whilst its perimeter dependence of the remaining 31.82%.

Also, Figure 2. 27 shows an almost negligible perimeter dependence of the dark currents flowing in BPD structures, pointing out the importance of the contribution to the dark current from the thermally generated carriers out of surface states in the region where the *n*-well-*p*-Epi substrate junction SCR reaches the silicon surface, which is in the case of the BPD structures screened. Because of this reason, although the n^+ PD presents a less important perimeter dependence of its dark current than the *n*-well PD, mainly because of the difference between the n^+ diffusion (0.2μm) and the *n*-well (1.5μm) respective depths, it is still much higher than the one of the BPD structures, precisely because of the silicon surface thermal generation of carriers.

When applied to different pixel photodiode structures, with different areas and perimeters, the data shown in Figure 2.27 proved highly useful and accurate to a 95%.



(a)



(b)

Figure 2. 27 – (a) Specific area dependent dark current density $J'_{dark}(A)$ reverse biasing voltage dependence for *n*-well PD, BPD, and n^+ PD test structures fabricated in the 0.5μm CMOS process under investigation; (b) specific perimeter dependent dark current density $J'_{dark}(P)$ voltage dependence for the same photodetector structures.

2.4.5.2 Capacitance (*C-V*) Characterization

Due to parasitic capacitance structures created by SCR formed at the *p-n* junction together with those created between the lateral walls (parallel to the *z*-axis in Figure 2. 15) of the SCR and the *p*-Epi substrate in the photodiode, the overall capacitance of the A01, A02, and A03 structures changes depending on the area, but also on its perimeter values. In order to learn the experimental relation between the bias dependent capacitance, and the perimeter and area values, respectively, *specific area dependent capacitance density* C_A', measured in F/cm^2, and *specific perimeter dependent capacitance density* C_P', measured in F/cm, concepts were introduced here and determined for each of the test structures fabricated. Following the same procedure proposed for the case of the dark current, the expressions for both characteristics can be found as given by Eqs. (2. 51) and (2. 52), respectively, if only two structures are considered in the solution of the equation system shown in Eq. (2. 53). Here, C_1 is the measured capacitance of the first test structure (of area A_1 and perimeter P_1), and C_2 is the measured capacitance of the second test structure (of area A_2 and perimeter P_2).

$$C_A^{'} = \frac{C_2 P_1 - C_1 P_2}{P_1 A_2 - P_2 A_1} \tag{2. 51}$$

$$C_P^{'} = \frac{C_1 A_2 - C_2 A_1}{P_1 A_2 - P_2 A_1} \tag{2. 52}$$

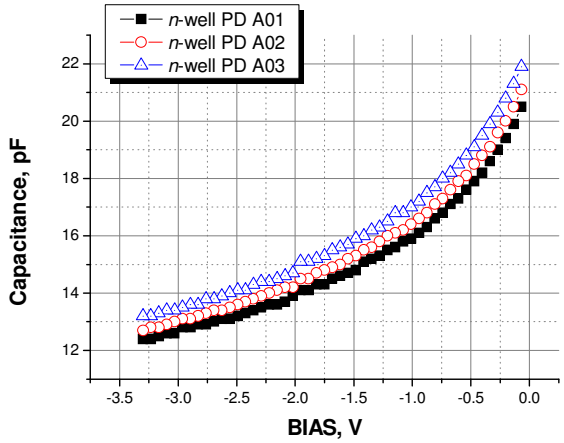
$$C = C_A^{'} \cdot A_n + C_P^{'} \cdot P_n \tag{2. 53}$$

C-V measurements were then performed on the A01, A02, and A03 test structures depicted in Figure 2. 24, using the *Hewlett-Packard HP4275A semiconductor analyser* device, at room temperature (*T*=300K), connecting the short-circuited *chuck* (the wafer bottom electrode) and the surface substrate contact to the H (high) output of the device, and grounding the *n*-well or n^+ contact (the cathode); applying sweep voltage, starting at V_{start}=0V and ending at V_{stop}=-3.3V, together with the superimposed AC signal with the frequency *f*=100kHz, and AC voltage amplitude V_{AC}=100mV, having a delay-time between each sample measurement of 1 second, and taking 50 sample points; choosing the parallel device connection model of the measuring device and performing calibrations using the *open-model* possibility. The averaged results of all the test structures measured are to be seen in Figure 2. 28.

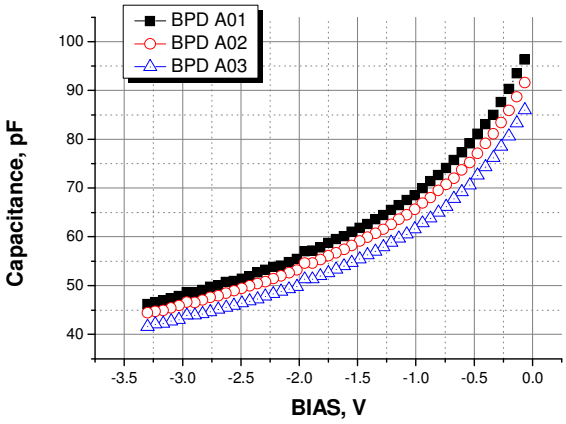
As it can be observed from the experimentally obtained results, only for the case of the *n*-well PD and the BPD structures, it is possible to observe a difference, although not quite clear enough, in the capacitance curves obtained from test structures with different areas and perimeters. The problem of reduced difference between the curves resulted specially dramatic for the case of the n^+ PD, where all three curves obtained were almost identical. Nevertheless, comparing the results, it can be observed that the capacitance characteristic for the BPD structures was much higher than the one related to *n*-well photodiodes. This was expected, as in the not fully depleted BPD structure two parallel capacitances exist, namely the one originated by the *n*-well-*p*-Epi substrate junction on one side, and the other one due to the p^+-*n*-well junction on the other, as it was already explained before in this text. Moreover, as it was already mentioned, being able to completely deplete the *n*-well in the BPD structures would lead to reduced capacitance values. Regarding the *n*-well PD, a second set of test structures was fabricated, consisting of the C_{Area} test structure, presenting A_{Area}=(300×300)μm^2, and a perimeter of P_{Area}=0.12cm, and the C_{Peri} test structure, divided in 60 stripes in parallel connection, with the joint area A_{Peri}=60×(5×240)μm^2 and joint perimeter P_{peri}=29400μm. Much better results were obtained for this second set of *n*-well PD based test structures, so a bigger difference in area and perimeter proved valuable.

Following the same philosophy, a third set of test structures was fabricated, regarding this time n^+ PD structures. It consisted of 10 stripes of n^+ photodiode structures in parallel connection, 1mm long and 5μm thick each, with the common area of A_1=5×10^{-4}cm^2 and perimeter P_1=2.01cm on one side,

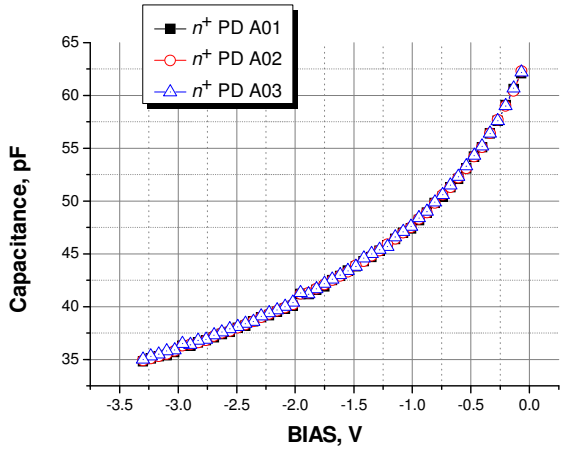
and 8 n^+ PD stripes in parallel connection, 1mm long and 0.6μm thick each, connected in parallel with another 10 identical structures, giving the common area of A_2=4.8×10^{-4}cm^2 and perimeter of P_2=16.01cm, on the other.



(a)



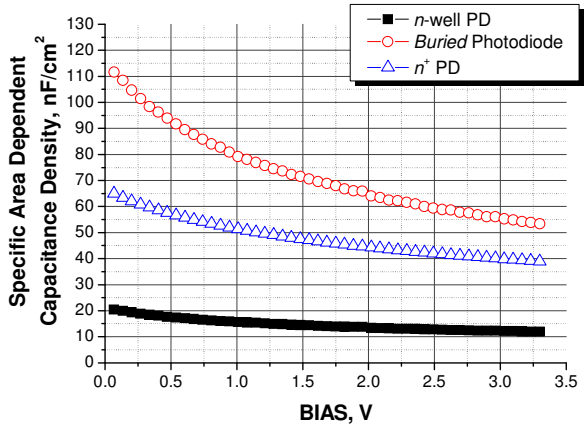
(b)



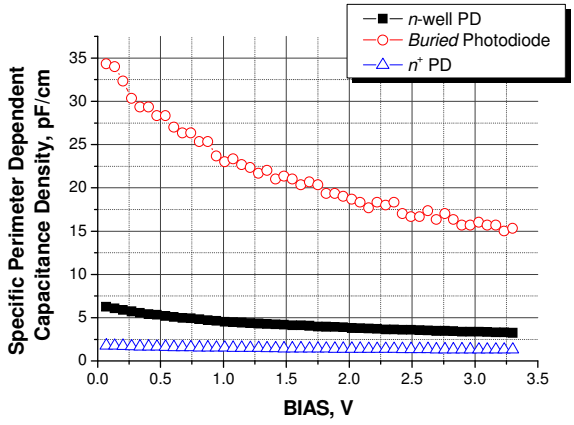
(c)

Figure 2. 28 – *C-V* measurement results obtained for the A01, A02, and A03 test structures fabricated for the case of: (a) *n*-well PD, (b) BPD, and (c) n^+ PD.

Following Eqs. (2. 51) and (2. 52) and the experimental results obtained from all three sets of test structures, the specific area dependent capacitance density C'_A and the specific perimeter dependent capacitance density C'_P were obtained for different biasing conditions and for all three reverse biased *p-n* junction based photodetector structures of interest. The compared results can be observed in Figure 2. 29.



(a)



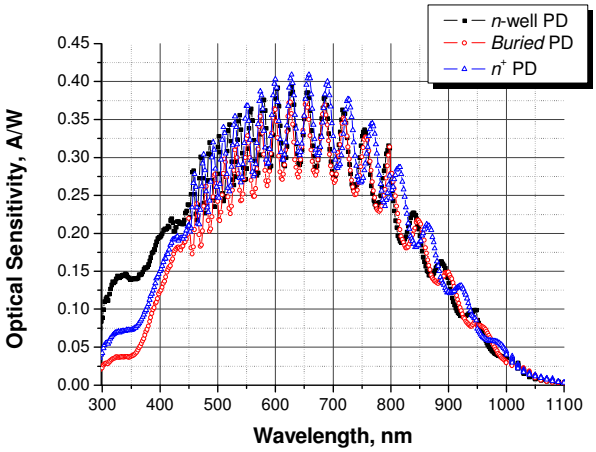
(b)

Figure 2. 29 – (a) *Specific area dependent capacitance density*, in nF/cm^2, for *n*-well PD, BPD, and n^+ PD photodetector structures fabricated in the 0.5μm CMOS process under investigation; (b) *specific perimeter dependent capacitance density*, in pF/cm, for the same three structures of interest.

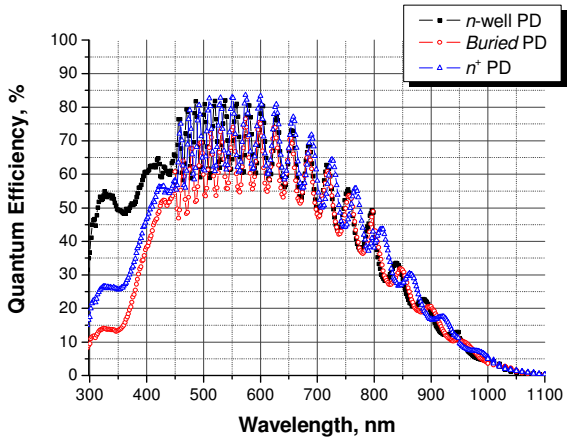
2.4.5.3 Optical Sensitivity and Quantum Efficiency Measurements

Using the optical sensitivity and quantum efficiency measuring stations described in *Appendix A* and *Appendix B* of this work, the results shown in Figure 2. 30 were obtained for each of the reverse biased (at V_{DD}=3.3V) *p-n* junction based photodetector types. The differences between the wavelength dependent optical sensitivity curves of all three test structure types, namely the A01, A02, and A03 when biased at V_{DD}=3.3V at room temperature resulted almost negligible.

In the graphs presented in Figure 2. 30, the wafer surface isolation layer reflection maxima and minima effects can be observed, discussed in the sub-chapter 2.2. The maximum quantum efficiency of almost 82.8% (S=0.275A/W) was reached by the n-well PD and n^+ PD at λ=530nm (green light) which decreased in both directions, namely towards NIR and towards UV radiation wavelengths. For the same wavelength, the BPD structures reached 72.6% of quantum efficiency, or 0.31A/W of optical sensitivity. On the other hand, the maximum optical sensitivity value reached by the n-well PD and n^+ PD, at λ=626nm, was S=0.404A/W (η=80%). The smaller optical sensitivity and, consequently, quantum efficiency values obtained for the BPD structures for wavelengths smaller than 650nm can be explained through existence of two SCRs within the n-well, which suggests that the thermally generated carriers outside the SCRs diffuse either in one direction (to finally reach the n-well - p-Epi substrate SCR and be drifted by the electrical field present there) or the other (to reach the p^+ - n-well SCR).



(a)



(b)

Figure 2. 30 – (a) Measured wavelength dependent optical sensitivity (in A/W) graph for the n-well PD A01, A02, and A03 test structure types for the soft UV to NIR part of the spectra; (b) wavelength dependent quantum efficiency graph obtained from (a).

At λ=300nm (soft UV), the quantum efficiency of 42% reached by the *n*-well PD, with *S*=0.116A/W, proved to be much higher than the 17.45% obtained from n^+ PD structures, or the 10.9% delivered by the BPDs. Moreover, regarding the soft UV part of the spectra, *n*-well PD reached the maximum value of 54.9% of quantum efficiency (*S*=0.14A/W) at λ=326nm, in contrast to the 26.5% quantum efficiency (*S*=0.07A/W) delivered by the n^+ PD, and η=14% (*S*=0.037A/W) measured at the BPD structures, which makes the *n*-well PD definitively the best photodetector structures for this part of the spectra. All the values have a precision error of around 10% as explained in *Appendix B*.

2.4.5.4 UV-Enhanced Quantum Efficiency Photodiode Stripes

For several spectroscopy and similar applications, one of the main requirements is a sufficient optical sensitivity (quantum efficiency) in the UV part of the spectra (λ=200nm-400nm), where the main goal is not to create a digital image but to be able to detect the impinging radiation and its exact optical power (photon flux). Bearing this in mind, and considering the results reported in [Pau99], although not pursuing a UV-blue light selective PD, but a PD with UV-enhanced quantum efficiency and with acceptable values of η for the entire spectra, n^+ PD and *n*-well PD based strip photodetectors were proposed.

The main problem in this task is the radiation absorption length, in the range between the 5.4nm (for λ=250nm) and 105nm (λ=400nm) depth, as shown in Figure 1. 3. The idea was to use photodiode stripes to be able to collect the carriers photogenerated within and below each PD stripe, but also at the silicon surface between the stripes, specially if the SCR of the neighbouring PD stripes could overlap, so no loss in the collected charge could appear due to recombination.

The four test structures fabricated for this tasks were: 1) 10 interconnected 1mm long and 5μm wide *n*-well PD stripes, with a 5μm distance between the neighbouring stripes and the common photoactive area of $1.05\times10^{-4}cm^2$; 2) and 3) the same photodetector stripes (5μm wide and with a distance of 5μm between the neighbouring stripes) fabricated using n^+ PD structures with- and without- field-oxide (bird's peak) isolation between the neighbouring stripes, respectively; and 4) 8×10 n^+ PD based photodetector stripes connected in series, 1mm long, 0.6μm wide, with a distance of 0.6μm between the neighbouring stripes and the common area of $1.035\times10^{-4}cm^2$. The layouts generated using the Cadence® software, together with the 2-D electric field results obtained after the first (*n*-well PD based) and the last (0.6μm wide n^+ PD based) test structures were simulated using the TCAD software are shown in Figure 2. 31.

The simulation shown in Figure 2. 31(b) suggests that the 5μm distance between the neighbouring *n*-well PD based stripes is insufficient since their SCR reverse biased at V_{DD}=3.3V inverse biasing originated SCR (lateral W_{SCR}=0.5μm, as shown in Figure 2. 18) do not overlap. On the other hand, from Figure 2. 31(c) it can be concluded that the 0.6μm wide n^+ PD based stripes generate

slightly overlapping SCRs when reverse biased at 3.3V (lateral W_{SCR}≈0.22μm, as shown in Figure 2. 23).

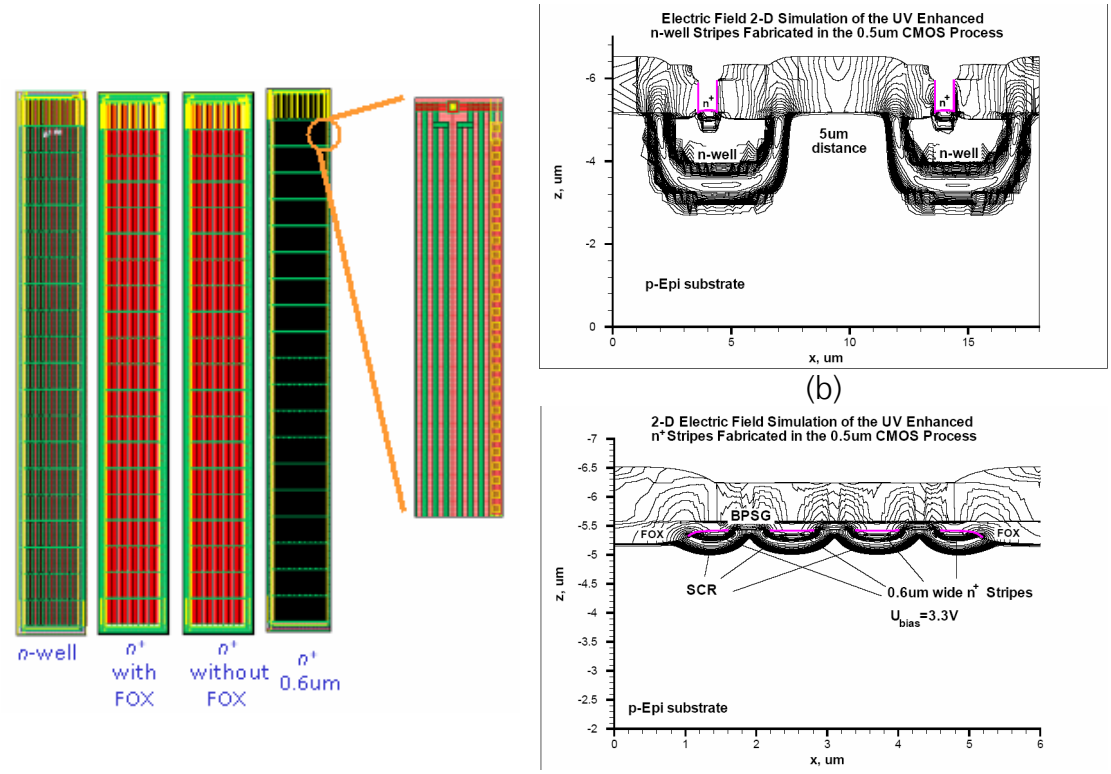


Figure 2. 31 – (a) Layout of the four test structure sets fabricated in the 0.5μm CMOS process for UV-enhanced quantum efficiency investigation; (b) the 2-D electric field simulation of the *n*-well based stripe photodetector under V_{DD}=3.3V reverse biasing; (c) 2-D electric field simulation of the 0.6μm bright n^+ PD based stripe photodetector under V_{DD}=3.3V reverse biasing.

All the four test structure sets were then properly characterized, electrically and finally, optically. The *C-V* and *I-V* curves, obtained from measurements performed at room temperature and using the *Hewlett-Packard HP4275A semiconductor analyser* and *HP4155B* devices respectively, can be observed in Figure 2. 32(a) and (b). On the other hand, the optical sensitivity and quantum efficiency measurements performed on the same test structures using the measurement station described in Appendix A of this text, can be observed in Figure 2. 32(c) and (d), respectively.

From Figure 2. 32, it can be concluded that although the 0.6μm wide n^+ PD based stripe photodetector generates slightly overlapping SCRs between the neighbouring stripes, its optical sensitivity and quantum efficiency performance are poorer than those of the 5μm wide n^+ PD based stripes. Also, as expected, the n^+ PD based stripes without the field-oxide isolation yielded a better performance than those with the bird's peak oxide structures between the stripes, as the bird's peak oxides penetrate the n^+ diffusion and diminish its effective depth and SCR on its perimeter, as it can be observed in Figure 2. 31(c) for the two n^+ diffusions on the extremes. Moreover, the best performance of all the four test structure sets had the *n*-well PD based stripe photodetector with 55% quantum efficiency under λ=330nm of impinging radiation.

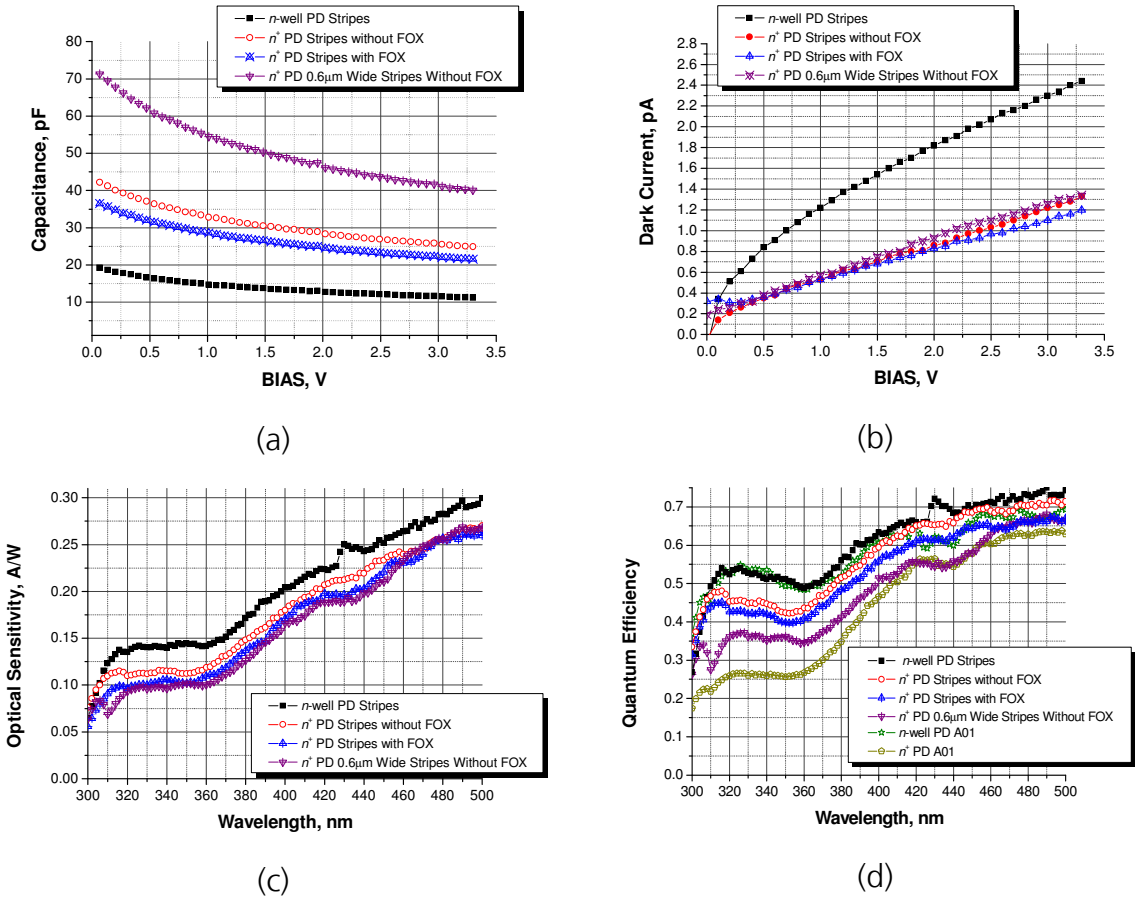


Figure 2. 32 – (a) *C-V* curves measured on all 4 UV-enhanced quantum efficiency test structure sets; (b) dark current voltage dependence for (a); (c) wavelength dependent optical sensitivity for the 4 test structure sets; and (d) wavelength dependent quantum efficiency curves for the four UV-enhanced stripe PD test structure sets compared to the quantum efficiency curves obtained from the *n*-well PD A01 and n^+ PD A01 test structures (Figure 2. 30).

From these results can be concluded that the amount of photogenerated carriers lost by recombination processes is much less within the *n*-well or the n^+ diffusion than it is on the surface of the *p*-Epi substrate between the PD stripes. That also explains why 5μm wide n^+ PD based stripes had better quantum efficiency performance than the 0.6μm wide ones. Nevertheless, the amount of photogenerated carriers existent within the *p*-Epi substrate between the stripes results in a significant increase of quantum efficiency of this kind of stripe photodetectors when compared to normal n^+ PD structures, e.g. the n^+ PD A01 test structure, as it can be observed in Figure 2. 32(d). For the case of the *n*-well PD, there was no difference in the quantum efficiency measured between the stripe photodetector and the *n*-well PD A01 test structure.

Finally, although generating the highest amount of dark current (2.5pA under 3.3V), the *n*-well PD based stripe photodetector resulted the best candidate for this kind of applications, presenting also the smallest capacitance (11pF).

2.5 MOS-C Based Photodetector Structures Fabricated in the 0.5μm Standard CMOS Process Under Investigation

In this sub chapter, the photodetectors based on the MOS capacitor structure, consisting of the silicon bulk, the 12nm gate-oxide layer and the 280nm thick highly doped polysilicon, fabricated on the *p*-Epi substrate (*n*-type PG) on one side, and on an *n*-well (*p*-type PG) on the other, will be analysed in detail.

2.5.1 MOS-C Based Photodetector Dark Current Considerations

In *Chapter 1* a of this work, it was explained that the charge integration process taking place within a photogate (MOS-C) structure is a non-equilibrium process. This due to the SCR width dependence on the amount of stored charge, under constant bias voltage, which decreases eventually reaching the steady-state, when the SCR can no longer be considered giving place to the inversion layer, with its W_{inv} width smaller than the original W_{SCR}. In order to gain some insight into the charge integration operation, a mathematical model that describes the non-equilibrium PG processes was developed as a first approximation to these phenomena.

For modelling purposes, the *n*-type PG was considered in this analysis as a series connection of the oxide capacitance C_{OX}, SCR region capacitance C_{SCR}, and the undepleted silicon resistance R_s. This last component can be neglected here due to high impurity concentration existent in the silicon epitaxial layer at the end of the 0.5μm CMOS process fabrication (N_A=2×10^{17}cm^{-3}). The boundary of the SCR within silicon was approximated by a step function.

According to the *Kirchhoff's Voltage Law* (KVL), the relation shown in Eq. (2. 54) was obtained for steady state conditions. Here, U_{PG} stands for the voltage applied to the PG; $U_{SCR} = \frac{qN_A W_{SCR}^2}{2\varepsilon_0 \varepsilon_{Si}}$ is the voltage drop at the SCR [Dur04], and U_{OX} is the voltage drop at the oxide layer of the PG.

$$U_{PG} - U_{OX} - U_{SCR} = 0 \tag{2. 54}$$

From the capacitor basic theory it follows that $U_{OX} = \frac{Q}{C_{OX}}$, where Q is the charge stored under the gate. On the other hand, it is a reasonable conclusion that the total amount of charge in the semiconductor required to neutralize the charge induced in the oxide through the applied voltage is the sum of the minority electrons and the acceptor impurities existing in the substrate, so, for the PG photoactive area A_{PG}, Eq. (2. 55) holds.

$$Q = Q_e + qN_A W_{SCR} A_{PG} \tag{2. 55}$$

Taking into account the formula for the oxide capacitance (Eq. (1.43)), and the PG area A_{PG}, the final expression for the voltage drop at the gate-oxide layer was expressed as shown in Eq. (2. 56).

$$U_{OX} = \frac{Q_e + qN_A W_{SCR} A_{PG}}{C_{OX}} \tag{2. 56}$$

So, considering Eq. (2. 56) and the expression for the voltage drop at the SCR, Eq. (2. 54) was rewritten as Eq. (2. 57).

$$U_{PG} = \frac{qN_A W_{SCR}^2}{2\varepsilon_0 \varepsilon_{Si}} + \frac{Q_e + qN_A W_{SCR} A_{PG}}{C_{OX}} \tag{2. 57}$$

Solving Eq. (2. 57) for the complete inversion charge, $Q=Q_e+qN_A W_{SCR} A_{PG}$, and considering the absolute value for U_{PG}, the expression Eq. (2. 58) is obtained.

$$\left(U_{PG} - \frac{qN_A W_{SCR}^2}{2\varepsilon_0 \varepsilon_{Si}} \right) C_{OX} = Q_e + qN_A W_{SCR} A_{PG} \tag{2. 58}$$

If a *non-steady state* is now considered, in which the total charge concentration and, consequently, the SCR width are changing in time, Eq. (2. 58) can be solved for Q_e and derived in time to obtain Eq. (2. 59) in terms of the charge flow (dark current) in the circuit.

$$\frac{dQ_e}{dt} = qN_A \frac{dW_{SCR}(t)}{dt} A_{PG} \left(\frac{W_{SCR}(t)\varepsilon_{OX}}{d_{OX}\varepsilon_{Si}} + 1 \right) \tag{2. 59}$$

On the other hand, and as it was already explained for the case of photodiodes in one of the previous sub chapters, a detailed analysis of a PG in the transient state should be carried out by solving the *Poisson*'s equation and the time dependent continuity equation simultaneously, including the generation-recombination rate. Again, this process results rather involved, so a simpler approach was taken here, where the three minority carrier sources were considered independently, pointing out the important physical parameters to control the storage time [Bre03].

Sources of dark current considered here, and mostly explained for the case of reverse biased *p-n* junction based photodetectors, are: 1) thermal generation of minority carriers within the bulk, diffusing into the depletion region from which they are collected into the potential well generated beneath the gate, forming the component of the PG dark current defined by Eq. (2. 60) [Bre03]; 2) minority carrier generation within the depletion region, given by the generalization of the generation-recombination term within the *Shockley equation* for the reverse current in a *p-n* junction, modified to suit the case of a MOS capacitor in deep depletion, expressed by Eq. (2. 61) [Bre03]; 3) generation of minority carriers out of fast surface (interface) states, characterized by the

surface generation velocity s_g; 4) the here not considered term, that arises from the background flux generation, given by the product of the electronic charge q, the background quantum efficiency η_B, and the background photon flux density Φ_B, as $I_{BF} = q\eta\phi_B$; and, finally, an additional 5) dark current term due to tunnelling, most important in narrow-bandgap materials. Resuming, the dark current flowing in a PG can be expressed as Eq. (2. 62).

$$I_{diff\_n} = -A_{PG} q \frac{n_i^2}{N_A} \sqrt{\frac{D_n}{\tau_{r\_n}}} \tag{2. 60}$$

$$I_{drift\_n} = -\frac{q n_i A_{PG} W_{SCR}}{\tau_{g\_n}} \tag{2. 61}$$

$$\left| I_{dark\_PG} \right| = q n_i A_{PG} \left[\frac{n_i}{N_A} \sqrt{\frac{D_n}{\tau_{r\_n}}} + \frac{W_{SCR}}{\tau_{g\_n}} + s_{g\_n} \right] \tag{2. 62}$$

Considering once again Eq. (2. 59), and substituting the charge flow defined by Eq. (2. 62), Eq. (2. 63) was easily formulated.

$$\frac{dW_{SCR}(t)}{dt} = \frac{q \frac{n_i^2}{N_A} \sqrt{\frac{D_n}{\tau_{r\_n}}} - \frac{q n_i W_{SCR}(t)}{\tau_{g\_n}}}{q N_A \left(\frac{W_{SCR}(t) \varepsilon_{OX}}{d_{OX} \varepsilon_{Si}} + 1 \right)} \tag{2. 63}$$

After a proper integration, the expression for the maximum depletion region width reached in the process of creating the potential well at the silicon - gate-oxide interface was formulated as Eq. (2. 64).

$$W_{\max} = \sqrt{\frac{2\varepsilon_0 \varepsilon_{Si}}{q N_A} U_{PG}} \tag{2. 64}$$

Eq. (2. 64) represents the initial condition for the second, the charge integration, stage. Here, the expression $W_{SCR}(t) \cdot \varepsilon_{OX} / d_{OX} \cdot \varepsilon_{Si} >> 1$ holds, due to the fact that the maximum depletion region width is being reached. The process of charge collection initiates and consequently, the depletion region width will start to decrement its value. Equation (2. 65) is obtained simplifying equation (2. 63).

$$\frac{dW_{SCR}}{dt} \left(\frac{\varepsilon_{OX} W_{SCR}(t)}{\varepsilon_{Si} d_{OX}} \right) = -\frac{n_i W_{SCR}(t)}{N_A \tau_{g\_n}} - \frac{n_i^2}{N_A} \sqrt{\frac{D_n}{\tau_{r\_n}}} \tag{2. 65}$$

Solving the differential equation (2. 65) for $W_{SCR}(t)$ [Dur04], the SCR width time dependence for the charge storing mode is finally obtained and expressed in Eq. (2. 66) [Dur03], for $M_1 = \frac{n_i \varepsilon_{Si} d_{OX}}{N_A \varepsilon_{OX}}$ and $M_2 = \frac{n_i}{N_A}\sqrt{\frac{D_n}{\tau_n}}$.

$$t = -\frac{\tau_{g\_n}}{M_1}\left\{W_{SCR}(t) - W_{\max} - M_2\tau_{g\_n}\ln\left[\frac{W_{SCR}(t) + M_2\tau_{g\_n}}{W_{\max} + M_2\tau_{g\_n}}\right]\right\} \tag{2. 66}$$

Due to the fact that it is quite difficult to solve Eq. (2. 66) for $W_{SCR}(t)$, for further calculations the equation was solved for time t, in seconds, in terms of $W_{SCR}(t)$, starting at $W_{SCR}(t) = W_{inv}$ (Eq. (1. 51)), the inversion layer width for the case of strong inversion.

Afterwards, having obtained the depletion region width behaviour in time for the thermally generated charge, the changes in charge concentrations for the same cycle were determined. Namely, considering Eqs. (1. 43) and (2. 58), the expression for the thermally- generated charge concentration time dependence, directly influenced by the SCR width behaviour in time, was obtained as Eq. (2. 67).

$$Q(t) = \left(|U_{PG}| - \frac{qN_A W_{SCR}(t)^2}{2\varepsilon_0\varepsilon_{Si}}\right)\left(\frac{\varepsilon_0\varepsilon_{OX} A_{PG}}{d_{OX}}\right) \tag{2. 67}$$

Finally, the behaviour in time for the total amount of current in this charge storing mode was examined. From the expression for the dark current obtained in Eq. (2. 62), and for all the assumptions already mentioned, the final expression for the charge storing process current behaviour in time, directly proportional to the SCR width time dependence, was defined by Eq. (2. 68).

$$\left|I_{dark\_PG}(t)\right| = qn_i A_{PG}\left(\frac{n_i}{N_A}\sqrt{\frac{D_n}{\tau_{r\_n}}} + \frac{W_{SCR}(t)}{\tau_{g\_n}} + s_{g\_n} + \frac{N_A}{n_i}\frac{dW_{SCR}}{dt}\right) \tag{2. 68}$$

In Eq. (2. 68), the first term on the right represents the dark current (diffusion) component generated in the *p*-Epi substrate (or the *n*-well, for the case of the *p*-type PG, in which case, N_A should be changed for N_D, τ_{r_n} for τ_{r_p}, τ_{g_n} for τ_{g_p}, and s_{g_n} for s_{g_p} in the entire equation), the second term is the dark current component generated within the SCR, the third one expresses the dark current aroused due to fast surface states, and the last one is the expression for the displacement current due to the SCR width changing in time.

2.5.2 *n*-type Photogate (*n*-type PG)

As it was already explained, the *n*-type PG consists of a MOS-C, formed on the *p*-Epi substrate, the 12nm dick gate-oxide thermally grown on of it, and the heavily doped 280nm thick polysilicon gate deposited on top of the gate-oxide. The schematic of this PG, as well as the results of the two-dimensional

electrostatic potential simulations performed considering all the fabrication steps of the 0.5μm standard CMOS process under study, using TCAD software tools, are to be found in Figure 2. 33.

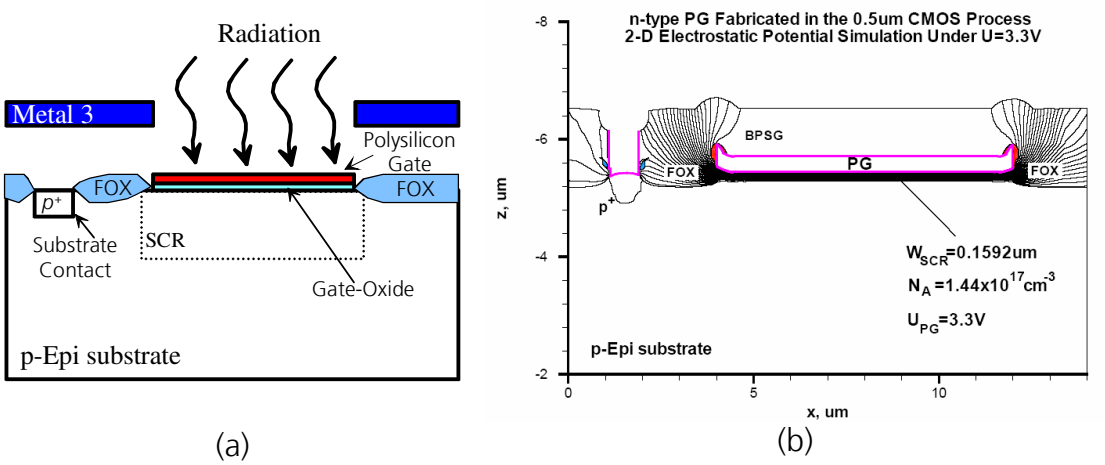


Figure 2. 33 - (a) Schematic of an *n*-type photogate; (b) two-dimensional electrostatic potential simulation results for the *n*-type PG fabricated in the 0.5μm CMOS process under investigation, obtained using TCAD process and device simulation software.

For a better understanding of the doping profile and the behaviour of the photodetector under different reverse biasing conditions, the total doping concentration and electrostatic potential data were extracted along a vertical cut line (parallel to the *z*-axis) performed show the two-dimensional simulation data display in Figure 2. 33(b) at x = 8μm, for the structure reverse biased at V_{DD}=3.3V. The total doping concentration graph together with the one describing the electrostatic potential at the cut, can both be observed in Figure 2. 34. Beneath the gate-oxide, the modulated doping concentration of the *p*-Epi substrate can be observed (with mean value N_A=1.44×10^{17}cm^{-3}), as well as the SCR width of 0.16μm.

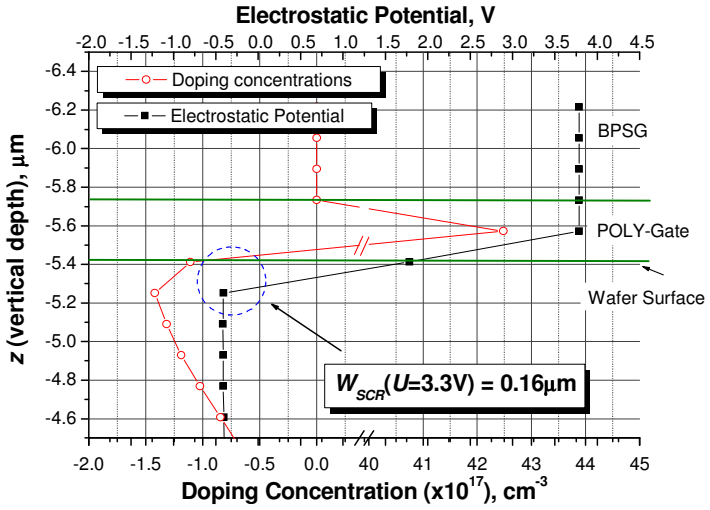


Figure 2. 34 - Total doping concentration graph together with the electrostatic potential one, obtained form a vertical cut done to the two-dimensional simulation result shown in Figure 2. 31(b) for the *n*-type PG reverse biased at V_{DD}=3.3V.

Following Eq. (2. 64), and in quite good agreement with the data extracted from the TCAD 2-D simulations, the SCR width under different biasing voltages is plotted in Figure 2. 35.

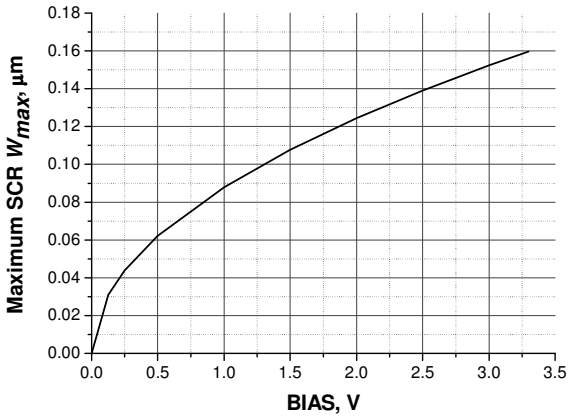
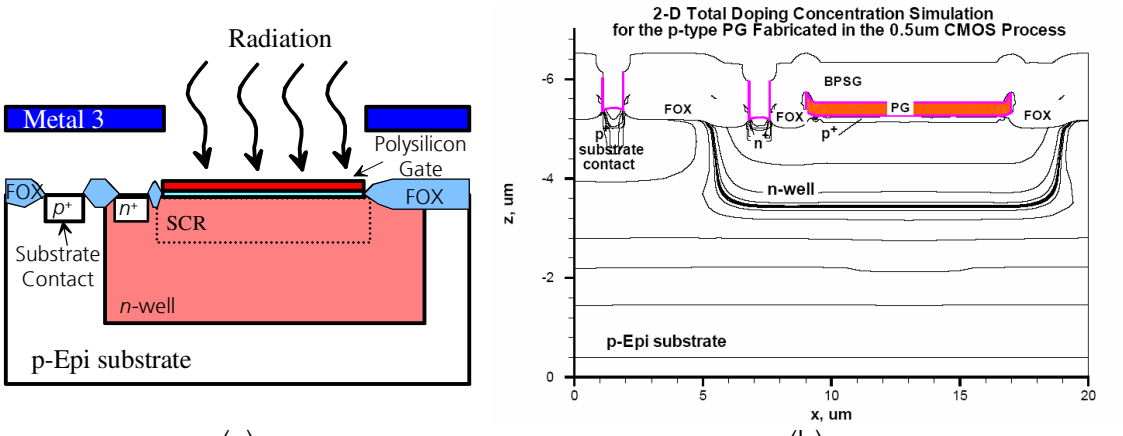


Figure 2. 35 – Maximum SCR width of the *n*-type PG fabricated in the 0.5μm CMOS process under investigation for different inverse biasing conditions.

2.5.3 *p*-type Photogate (*p*-type PG)

The *p*-type PG is a MOS-C structure fabricated on top of the *n*-well in the 0.5μm CMOS process under investigation, consisting of the 1.5μm deep *n*-well (*n*-type substrate) presenting a modulated doping profile within with an average donor concentration in the middle of N_D=1×10^{17}cm^{-3}, the 12nm thick gate-oxide thermally grown on top of it, and finally covered by the 280nm thick highly doped polysilicon gate. The schematic diagram of this PG structure, as well as the results of the two-dimensional total doping concentration simulations performed considering all the fabrication steps of the 0.5μm standard CMOS process under investigation, using TCAD software tools, can be observed in Figure 2. 36.



(a) (b)

Figure 2. 36 - (a) Schematic of a *p*-type photogate; (b) two-dimensional total doping concentration simulation results for the *p*-type PG fabricated in the 0.5μm CMOS process under investigation, obtained using TCAD process and device simulation software.

For a better understanding of the doping profile and the behaviour of the photodetector under different reverse biasing conditions, the total doping concentration and electrostatic potential data were extracted along a vertical cut line (parallel to the *z*-axis) performed to the two-dimensional simulation data display shown in Figure 2. 36(b) at x = 12μm, for the structure inversely biased at V_{DD}=3.3V. The total doping concentration graph together with the one describing the electrostatic potential at the cut, can both be observed in Figure 2. 37. Beneath the gate-oxide, the modulated doping concentration of the *n*-well can be observed (with mean value at the PG SCR: N_D=1×10^{17}cm^{-3}), as well as the SCR width of 0.14μm. As it can be seen in Figure 2. 37, due to the so called pMOSFET channel implantation step (implantation of BF_2), used to control the value of the threshold voltage of the pMOSFET, a 0.06μm deep p^+ (N_A=7×10^{16}cm^{-3}) arises, screening the wafer surface from the SCR generated beneath the gate. This quite beneficial feature resembles the "buried CCDs" and decreases the amount of dark current in this kind of photodetectors.

On the other hand, special attention has to be paid here to the SCR generated by the *n*-well – *p*-Epi substrate junction. It is proposed here to ground the *n*-well to keep it as small as possible, applying negative voltage to the PG, as all the carriers photogenerated outside the *p*-type PG SCR have the possibility to diffuse into *n*-well SCR instead of the PG's one, decreasing the quantum efficiency in a significant manner. Moreover, for impinging radiation wavelengths approaching the NIR part of the spectra (λ>550nm) the absorption length lays beneath the *n*-well depth. Thus, all the photogenerated carriers inside the *p*-Epi substrate will also be irremediably lost to the photo signal of the PG.

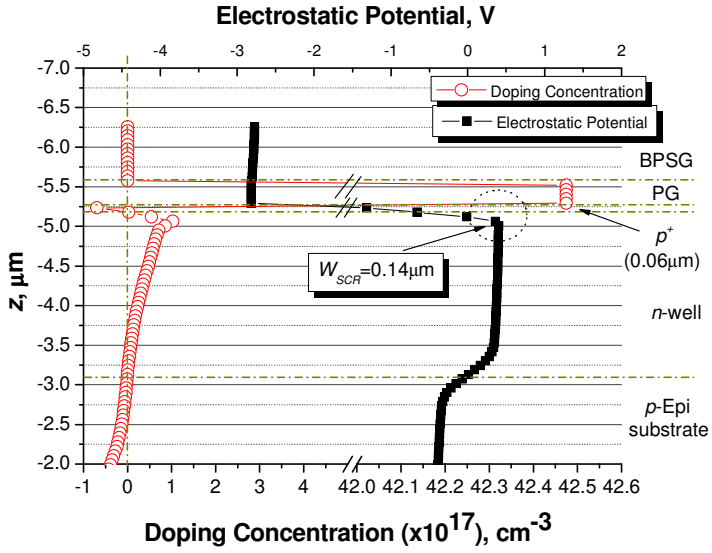


Figure 2. 37 - Total doping concentration graph together with the electrostatic potential one, obtained form a vertical cut done to the two-dimensional simulation result shown in Figure 2. 36(b) for the *p*-type PG biased at V_{DD}=-3.3V, and *n*-well at $U_{n\text{-}well}$=0V.

Based on Eq. (2. 64), and again in quite good concordance with the data extracted from the TCAD 2-D simulations, the SCR width of the *p*-type PG, under different biasing voltages, is shown in Figure 2. 38.

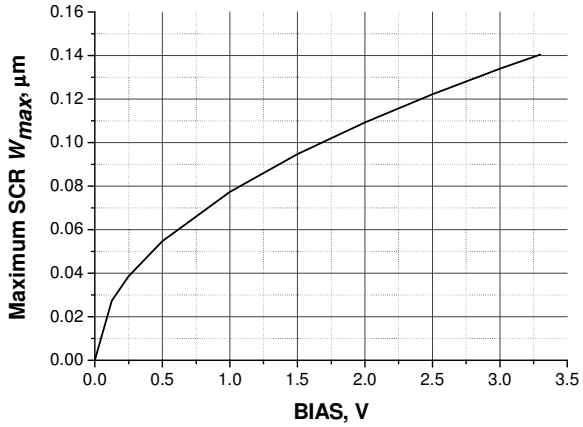


Figure 2. 38 - Maximum SCR width of the *p*-type PG fabricated in the 0.5μm CMOS process under investigation for different reverse biasing conditions.

2.5.4 Electrical and Optical characterization of MOS-C Based Photogate Detectors

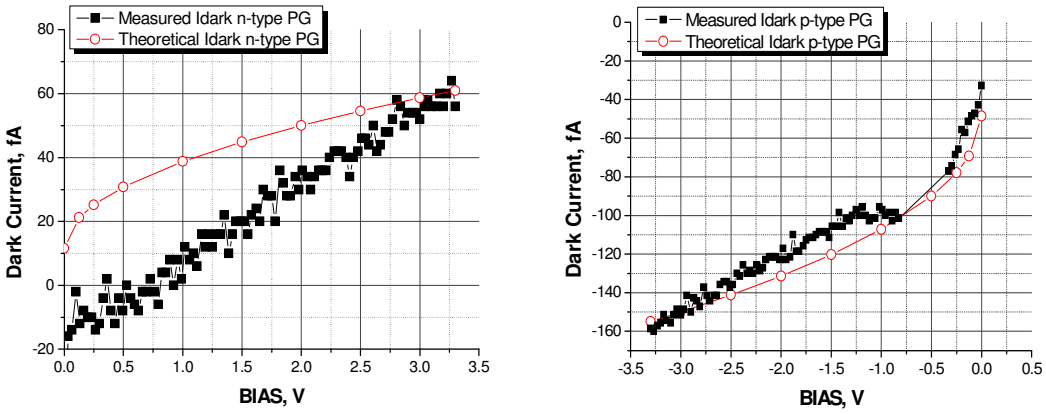
Next, dark current (*I-V*) measurement and optical sensitivity (and quantum efficiency) optical characterization results, obtained from MOS-C based PG test structures fabricated in the 0.5μm CMOS process under investigation will be presented.

2.5.4.1 Dark current (*I-V*) Measurements

The dark current (*I-V*) measurements were performed on two sets of 5 test structures, namely the (300×300)μm^2 *n*-type PG and *p*-type PG, respectively. The measurements were performed "on the wafer", at room temperature, using the *Hewlett-Packard* HP 4155B device, grounding the *p*-type substrate and the *n*-well electrodes, and performing a voltage sweep on the polysilicon (gate) electrode used as the anode, starting at 0V and ending at –3.3V, while sampling in 0.33V intervals, for the case of the *p*-type PG; and grounding the *p*-type substrate while performing a voltage sweep on the polysilicon (gate) used as an anode, starting at 0V and ending at 3.3V, for the case of the *n*-type PG. The results, after proper averaging, can be found in Figure 2. 39, together with the theoretical curves, obtained using Eq. (2. 68) for t=0s and the W_{max} values shown in Figures 2. 33 and 2. 36, respectively.

Considering the uncertainties already discussed affecting the minority carrier lifetime values, to obtain theoretical curves that acceptably fit the curves measured on test structures, generation time of τ_{g_p}=450μs and the surface velocity of s_{g_p}=8×10^{-3}cms^{-1} were used for the case of the *n*-type PG, whilst for the *p*-type PG, the values used were τ_{g_n}=182.2μs and s_{g_n}=3.5×10^{-2}cms^{-1}. The main idea here is once again, not to attempt using the theoretically calculated values for anything else than for understanding the processes of generation of

dark current in *n*-type and *p*-type PG structures. The mathematical relations of the theoretically obtained curves hold when compared to the experimentally obtained ones, which proves the validity of the theory presented so far.



(a) (b)

Figure 2. 39 – Measured and theoretically determined dark current reverse bias dependence for the *n*-type and *p*-type PG structures fabricated in the 0.5μm CMOS process under investigation.

The absolute values of specific area dependent dark current densities, in pA/cm^2, for both, the *n*-type and the *p*-type PG structures, can be observed in Figure 2. 40.

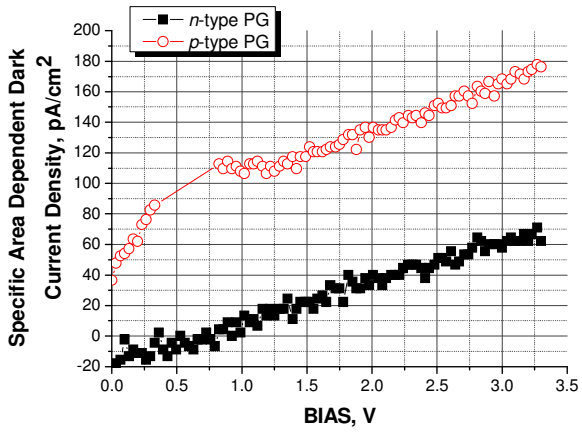


Figure 2. 40 – Measured specific area dependent dark current densities for the *n*-type and *p*-type PG structures fabricated in the 0.5μm CMOS process under investigation.

2.5.4.2 Optical Sensitivity and Quantum Efficiency Measurements

As it was already explained before, one of the main drawbacks of using MOS-C based PG photodetectors is the strong absorbance of the 280nm thick polysilicon gate, specially in the soft-UV and blue-green part of the spectra. To obtain its exact radiation transmittance, the quantum efficiency obtained from a (300×300)μm^2 *n*-well PD and an identical structure covered by a grounded polysilicon layer were compared.

The quantum efficiencies obtained in both cases, as well as the polysilicon layer wavelength dependent transmittance obtained as the ratio of the two quantum efficiency graphs can be observed in Figure 2. 41, together with the *Cadence*® software generated layout for the test structures. The variation in the inter-metal isolation oxide layers thickness, different for the *n*-well PD and the polysilicon layer covered *n*-well PD test structures is the cause of values of polysilicon transmittance reaching more than 100%. The measuring station used for this characterizations is described in Appendix B of this work.

As Figure 2. 41(c) suggests, the polysilicon transmittance is quite reduced for impinging radiations at wavelengths shorter than 450nm, the value at which the polysilicon layer has a transmittance of only 20%. At 550nm, there is a first maximum of 95% in the transmittance curve, which decreases down to 60% at 610nm wavelengths, to finally reach the 100% for wavelengths longer than 720nm. Another limiting factor for the quantum efficiency and the optical sensitivity is the depth of the SCR created beneath the PG, namely 0.16μm for the case of the *n*-type PG and 0.14μm for the *p*-type PG. This causes the diffusion component of the generated photocurrent to dominate, specially for wavelengths longer than 470nm.

The two sets of test structures already described, used for electrical measurements of the PG structures, were used here for their optical characterization. The test structures were reverse biased at V_{DD}=3.3V in all the cases, and the measurements were performed using the measuring station described in the Appendix B of this work. In Figure 2. 42 the optical sensitivity and quantum efficiency graphs for impinging radiation with wavelengths between the 450nm and 1100nm can be observed for both, the *n*-type and the *p*-type PG structures fabricated in the 0.5μm CMOS process under investigation, together with the optical sensitivity and quantum efficiency curves obtained from the reverse biased *p*-*n* junction based photodetectors already analysed in this text, used here as a reference.

As expected, in Figure 2. 42 a lower optical sensitivity and quantum efficiency values are obtained for both types of PGs when compared to the reverse biased *p*-*n* junction based photodetectors. Nevertheless, the situation is much more dramatic for the case of the *p*-type PG. This issue was already discussed, and is due to an additional quantum efficiency, or better defined charge collection efficiency, limiting factor: the existence of the SCR generated at the *n*-well – *p*-Epi substrate junction, even if the *n*-well remains grounded maintaining its width at a minimum. The problem arises when the minority carriers are photogenerated outside the SCR created beneath the PG, and have to diffuse to reach electrostatic potential minima created within the volume defined by their diffusion length; this electrostatic potentials or electrical fields exist beneath the PG and also, at the border of the *n*-well. The probability that a carrier diffuses into the *n*-well – *p*-Epi substrate SCR, where it is lost for the PG output signal, is very high, and becomes specially influential for the charge generated outside the 1.5μm deep *n*-well, i.e. mostly for wavelengths longer than 550nm (green light) with absorption length of $1/\alpha$=1.5μm (Figure 1. 3).

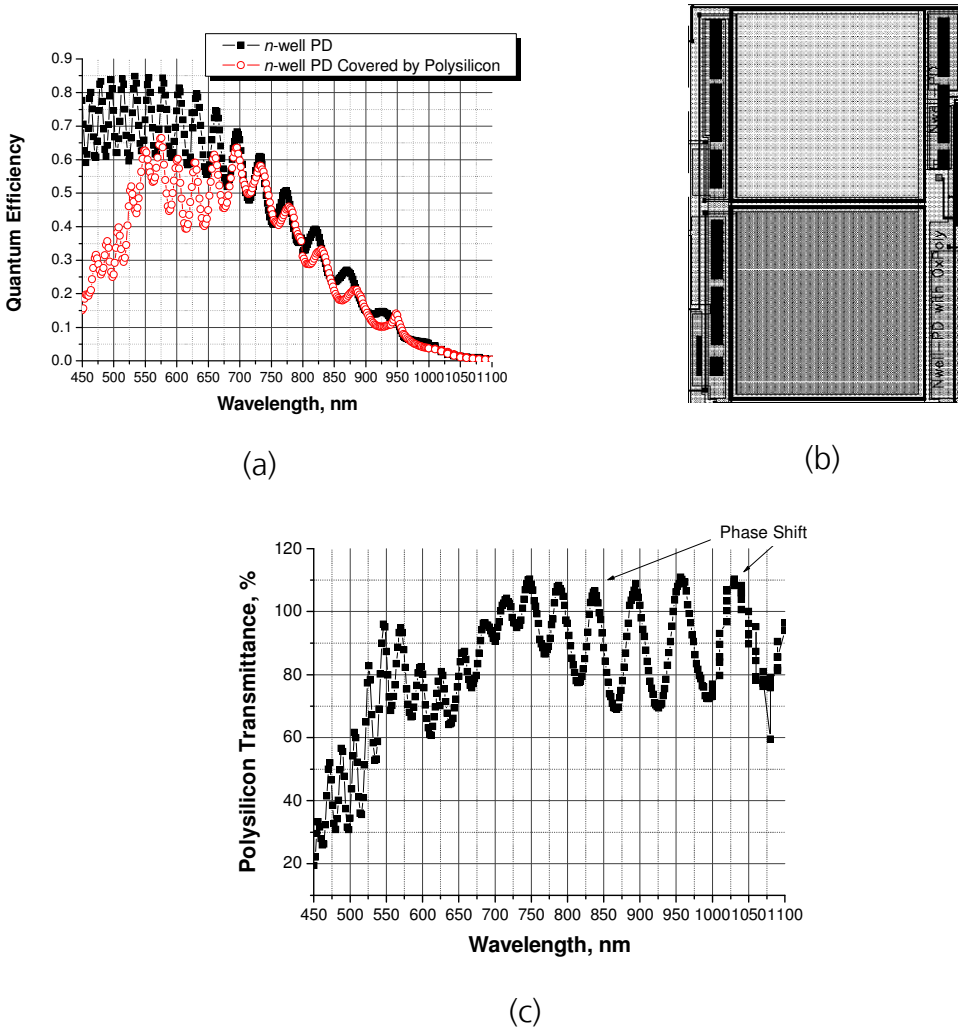
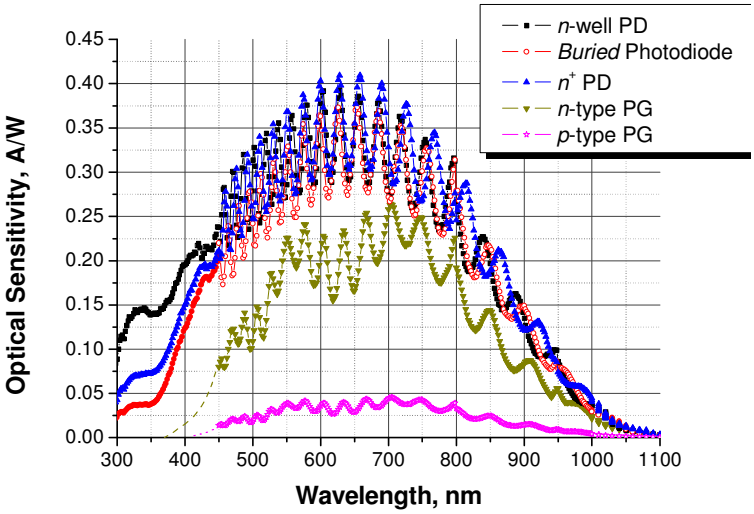


Figure 2. 41 – (a) Quantum efficiency graphs obtained from the (300×300)μm^2 *n*-well PD and the similar (300×300)μm^2 *n*-well PD covered by the 280nm thick polysilicon layer; (b) Cadence® software generated layouts for the test structures; (c) radiation transmittance wavelength dependence for the polysilicon layer present in the 0.5μm CMOS process under investigation.

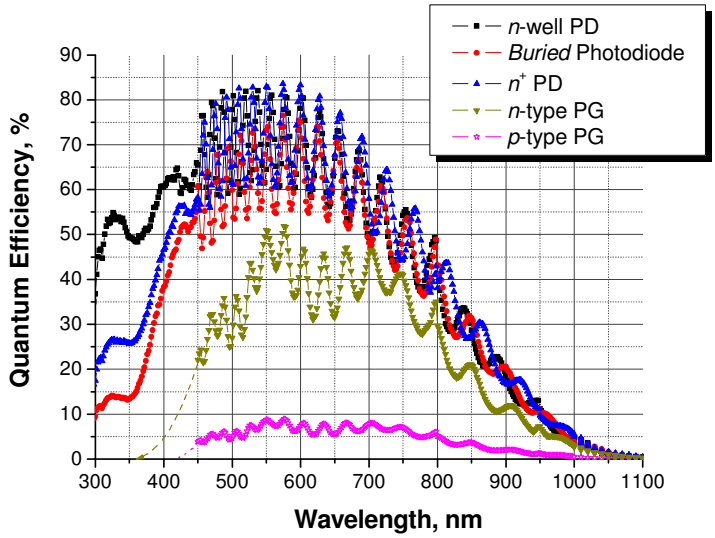
The maximum quantum efficiency of 52% is reached by the *n*-type PG at λ=576nm, with an optical sensitivity of S=0.241A/W for the same wavelength. The *p*-type PG, on the other hand, reaches only 9% of quantum efficiency, with S=0.04A/W, for the same λ=576nm, only 17% of the values reached by the *n*-type PG. Moreover, both PG structures are practically insensitive for wavelengths in the UV part of the spectra.

For the case of the *p*-type PG quantum efficiency and optical sensitivity performance, there is not much that can be done, specially as the most influential factor is the *n*-well on which these structures are fabricated. On the other hand, for the case of *n*-type PG structures, the optical sensitivity and quantum efficiency limiting factor is the polysilicon radiation absorption, specially in the UV-VIS part of the spectra (Figure 2. 41). So, the improvement of these figures of merit can be expected if some kind of a photogate is fabricated with higher transmittance in this part of the spectra. Following the experiences gathered mainly by the *Eastman Kodak Company* in the late 1990s, we have tried to incorporate an Indium-Tin-Oxide (ITO) semi transparent layer to the

0.5μm CMOS process, to be used as a photogate. Our experiences are described in the next sub-chapter.



(a)



(b)

Figure 2. 42 - (a) Measured wavelength dependent optical sensitivity (in A/W) graph for the *n*-type PG and the *p*-type PG fabricated in the 0.5μm CMOS process under investigation (the lower two curves) compared to the *n*-well PD, n^+ PD, and BPD optical sensitivity curves used here as a reference, for the soft UV to NIR part of the spectra; (b) wavelength dependent quantum efficiency graph obtained from (a).

2.6 Indium-Tin-Oxide (ITO) Layer Used for Fabrication of Semi Transparent Photogates in the 0.5μm Standard CMOS Process Under Investigation

Interest in transparent conductors, the so called *Transparent Conductive Oxides* (TCO), can be traced back to 1907 when reports of transparent and conductive cadmium oxide (CdO) films first appeared [Bas98]. Due to large

interests in their proper characterization, it is now known that non-stoichiometric and doped films of oxides of tin, indium, cadmium, zinc and their various alloys exhibit high transmittance and nearly metallic conductivity [Cho83]. Nevertheless, *indium tin oxide* (ITO), with reported transmittance and conductivity as high as 95% and $10^4\Omega^{-1}cm^{-1}$ [Bas98] respectively, is among the most popular of these films used in electronic, optoelectronic, and mechanical applications.

Although partial transparency -with acceptable reduction in conductivity- can be obtained for very thin (d_{ITO}<150nm [Tor03]) metallic films, high transparency and simultaneously high conductivity cannot be attained in intrinsic stoichiometric materials. The only way this can be achieved is by creating electron degeneracy in a wide bandgap (E_g>3eV for VIS part of the spectra) material by controlled introduction of non-stoichiometry and/or appropriate dopants. These conditions can be conveniently met for ITO [Bas98]. *Indium tin oxide* is essentially formed by substitutional doping of In_2O_3 with tin (Sn) which replaces the In^{3+} atoms from the cubic bixbyte structure of indium oxide [Fan77]. Sn thus forms an interstitial bond with oxygen and exists either as SnO or SnO_2 – accordingly, it has a valency of +2 or +4, respectively. This valency state has a direct bearing on the ultimate conductivity of ITO. The lower valence state results in a net reduction in carrier concentration since a hole is created which acts as a trap and reduces conductivity [Bas98]. On the other hand, predominance of the SnO_2 states means Sn^{4+} acts as an *n*-type donor releasing electrons to the conduction band. However, in ITO, both substitutional tin and oxygen vacancies contribute to the high conductivity and the material can be represented as $In_{2-x}Sn_xO_{3-2x}$ [Bas98]. ITO films have a lattice parameter close to that of In_2O_3 and lie in the range of 10.12Å to 10.31Å [Bas98].

However, ITO films grown at room temperature have large stacking faults and represent an amorphous structure [Bas98]. Increasing this temperature to 200°C leads to a polycrystalline structure and final annealing results in near single crystallinity with uniform grain size which leads to increased conductivity. On the other hand, the direct optical bandgap of ITO films is generally greater than 3.75eV although a range of values from 3.5eV to 4.06eV have also been reported in literature [Fan77, Bas98]. The high optical transmittance of these films is a direct consequence of their being a wide bandgap semiconductor. The fundamental absorption edge generally lies in the UV part of the spectra and shifts to shorter wavelengths with increasing carrier concentration. The reported value for the refractive index of ITO is 1.96 [Szc83]. The transmittance of ITO films is also influenced by a number of minor effects which include surface roughness and optical inhomogeneity in the direction normal to the film surface. Inadvertently grown dark brown (effectively translucent) metallic films of ITO have also been reported [Bas98]. This opaqueness has been attributed to unoxidised Sn metal grains on the ITO surface as a result of instability due to absence of sufficient oxygen during deposition [Fan77].

The enlisted properties of the ITO films made them quite attractive for the imaging industry. In an effort to boost the sensitivity of front-side illuminated CCD in the blue/green region of the spectrum, the *Eastman Kodak Company*

proposed in the late 1990's a new gate structure based on ITO [Rop99]. Moreover, when compared to other solutions, such as back-side illumination or using mechanical lens on a chip for front-side illuminated CCD, the quantum efficiency of ITO imagers in the blue/green region exceeded the QE performance generally seen in lens-on chip and open-electrode designs, and was less complicated to implement than the back-side illuminated CCD that involved rather complicated silicon substrate thinning. The quantum efficiency behaviour for different kinds of CCD based imagers can be observed in Figure 2. 43, as presented by [Rop99]. Furthermore, ITO devices have no inherent reduction of dynamic range and carry a fairly comparable price tag [Rop99].

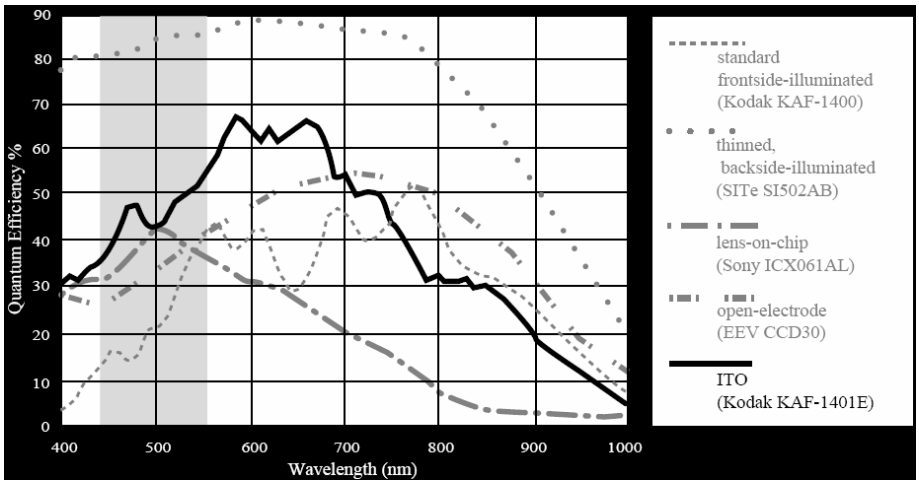


Figure 2. 43 - Quantum efficiency behaviour for different approaches followed to resolve the blue/green sensitivity issue. ITO technology presents a better performance compared to a front-side illuminated CCD, lens-on-chip or open-electrode imagers [Rop99].

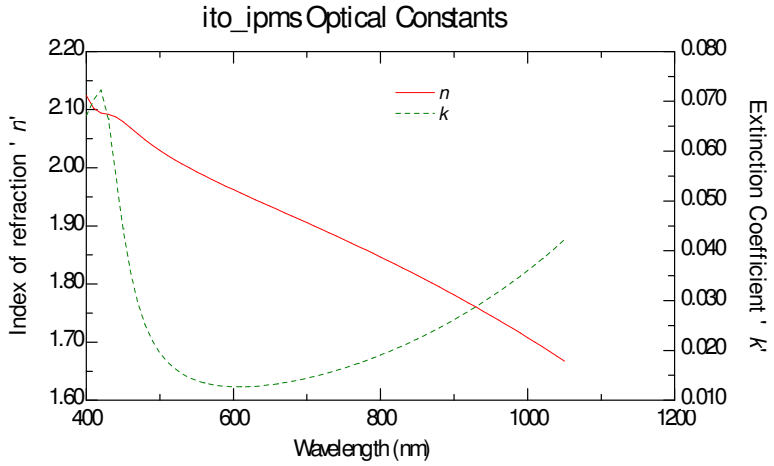
The *Eastman Kodak* alternative approach consisted in replacing the second level of polysilicon gate electrodes with more optically transparent ITO gates. Originally implemented only in CCD technology, the *KAF-3200E Kodak-Eastman* sensor devices were built using heavily doped *p*-type substrates with a more lightly doped *p*-type epitaxial layer on top [Mei01]. *n*-channel transistors and shift-registers (for use in CCD) were built using a single level of doped polysilicon and a single level of ITO gate electrodes. A single level of aluminium connected the gates to bonding pads [Mei01]. The dark current generation rates between the polysilicon and ITO processes were essentially the same within the tolerance of lot to lot variations in CCD [Mei01].

Within this work, it was intended to analyse the possibility of introducing a layer of semi transparent highly conductive ITO films in the process flow of the 0.5μm CMOS process under investigation, as follows.

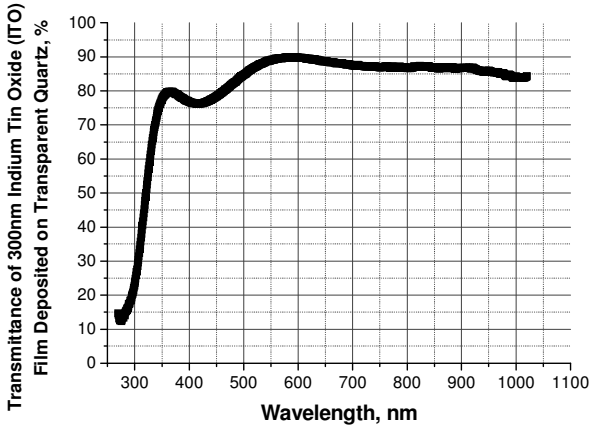
2.6.1 Integration of the ITO Layer Deposition in the 0.5μm CMOS Process Under Investigation

The ITO film deposition used in this work was carried out at the *Fraunhofer Institute for Photonic Microsystems* (Fraunhofer IPMS) in Dresden, using the thin film deposition facility VES400/13 of the *Applied Materials* department. This facility is normally used for deposition of layers used for

organic light-emitting diodes (OLED), carried out through thermal evaporation, on (300×400)mm^2 silicon substrates. Additionally, two magnetic sputtering cathodes, of type *PK500*, were also installed in the facility. So, with one of the cathodes, using an ITO target and a DC process with a superimposed RF radiation used for sputtering, ITO films can be deposited on radiation heated silicon substrates (heating temperature can reach the 750°C). Moreover, to reduce the sputtering damage on the silicon substrate, a "facing target" or "mirror shape target sputtering" [ITOF07] technique was used, in which a plasma environment is created between two ITO targets installed facing each other within the facility, whilst the silicon wafer is placed outside of this region. By applying a strong magnetic field, acceptable deposition rates can be achieved. At the Fraunhofer IPMS, this kind of OLED-cluster deposition facility was installed, made in Korea by *Sunic System*.



(a)



(b)

Figure 2. 44 – (a) Wavelength dependent refraction and extinction coefficients measured for the 300nm thick ITO films deposited on transparent quartz [ITOF07]; (b) wavelength dependent transmittance curve for the condition enlisted in (a).

The first modification of the film deposition facility was the construction of the 200mm diameter wafer (used in the standard 0.5μm CMOS process under investigation) recipients that would enable the wafers to be used within the facility. Once it was done, the first 300nm thick ITO films were deposited on

the 200mm diameter rotating silicon wafers, with a specific resistance of $5.6\times10^{-4}\ \Omega\cdot cm$, the carrier concentration of $5.45\times10^{-4}cm^{-3}$, and the electron mobility of $\mu_n=22.3cm^2/V\cdot s$ (obtained through *four-probe* and *Hall-effect* based measurements respectively, performed on ITO films).

The optical characterization of ITO films deposited on transparent quartz-glass was performed using ellipsometry based measuring techniques, for impinging radiation with wavelengths in the range between the 400nm and 1000nm. The obtained wavelength dependent refraction and extinction coefficients, respectively, as well as the transmittance of the ITO layer for the same wavelength range, are shown in Figure 2. 44 [ITOF07].

To incorporate the ITO layer deposition as part of the standard 0.5μm CMOS process under investigation, involves several changes to be seen in Figure 2. 45 [ITOF07]. Due to contamination risks, the cleaning steps (SC1, CARO) normally undertaken in the standard process flow, after the source/drain implantation, are to be replaced by the back-end EKC cleaning. In this way, the second polysilicon oxidation step grows thermally the 15nm thick ITO-gate oxide together with the 50nm field oxide isolation between the polysilicon and ITO layers. This oxide thickness difference arises due to higher impurity concentration within the polysilicon layers. Afterwards, as the contamination risks are too high for the wafers on which the ITO layer was deposited at the Fraunhofer IPMS in Dresden, to re-enter the front-end fabrication clean room, the source-drain impurity activation and all other high-temperature steps are to be performed within a specially dedicated furnace (CTA4) for these tasks. So, the source/drain impurity activation will no longer be realised through rapid-thermal-annealing (RTA) step in 20 seconds at 1000°C, but through slower heating (30 min.) within a horizontal furnace (at 900°C).

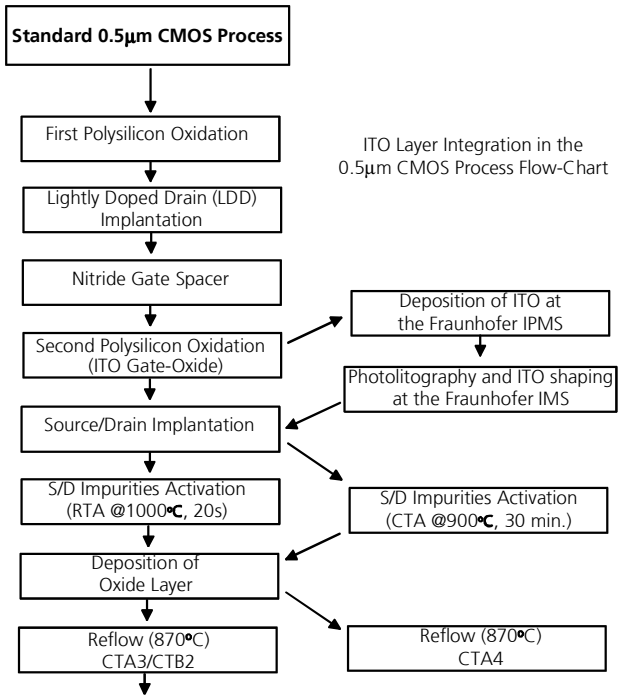


Figure 2. 45 – Excerpt of the 0.5μm CMOS process flow-chart, with and without the ITO layer deposition possibility [ITOF07].

Following the restriction that the electrical parameters of the microelectronic devices fabricated in the original 0.5μm CMOS process must not be changed, this impurity activation step must be chosen correctly, monitoring at the same time the changes it could imply for the ITO layer electrical and optical characteristics. For this purpose, different temperatures to be used for the impurity activation were tested, enlisting the activation levels (sheet resistivity in Ω/sq) at the source/drain surfaces in Table 2. 5 [ITOF07], at the same time measuring the sheet resistivity of the 300nm thick ITO films, also enlisted in Table 2. 5 [ITOF07], together with the refraction and extinction coefficients of the ITO layers deposited on transparent quartz-glass undergoing the same thermal steps shown in Figure 2. 46 [ITOF07].

Table 2. 5

Impurity Activation Step	*n-type MOSFET Source/Drain Sheet Resistivity, in Ω/sq*	*ITO Layer Sheet Resistivity on the Entire Wafer, in Ω/sq (range)*
as deposited		4.3 – 4.5
@ 700°C, 30 min.	101.3	11.5 – 12.6
@ 800°C, 30 min.	98.6	10.6 – 10.8
@ 900°C, 30 min.	78.1	9.9 – 10.3
RTA @ 1000°C, 20s	73.3	

From the results shown in Table 2. 5 [ITOF07] and Figure 2. 46 [ITOF07], the best compromise between the electrical and optical parameters of the ITO films and the standard 0.5μm CMOS process devices electrical characteristics is achieved when the impurity activation step is undertaken at 900°C during 30 minutes, in nitrogen (inert) atmosphere.

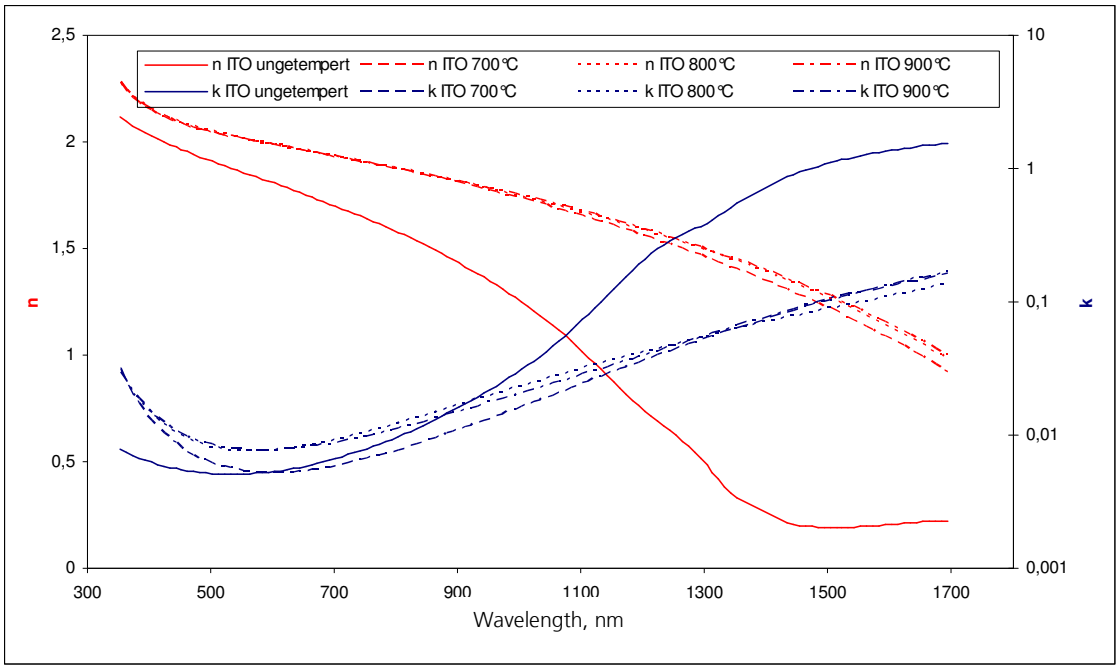
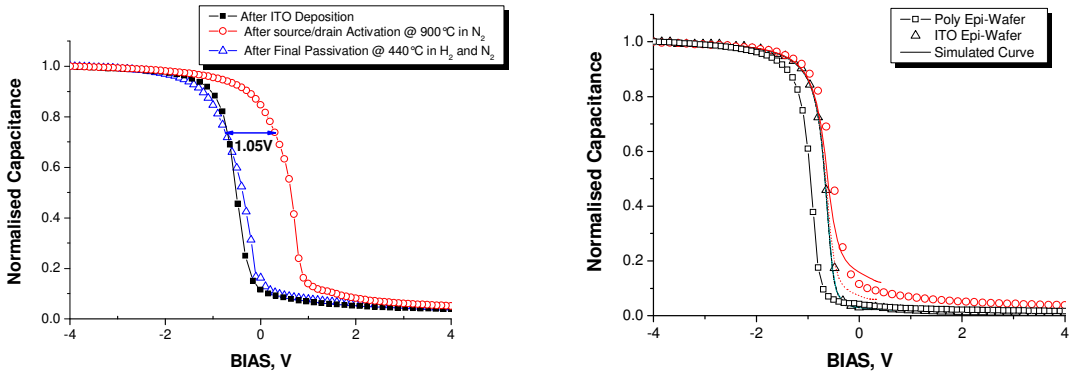


Figure 2. 46 – Changes occurred in the optical characteristics (refraction and extinction coefficients) of the ITO deposited layers due to impurity activation high temperature process steps performed at 700°C, 800°C, and 900°C.

The ITO layer etching was done using HCl in a wet environment. The problem occurred regarding the reduced selectivity of this etching technique between the ITO and oxide structures (1:1.7), which was partially solved leaving the last 30nm-50nm of the ITO layer on the oxide, which were then removed during the CARO-cleaning process together with the remaining photoresist. On the other hand, after the photolithography step, small quantities of photoresist were found on top of the ITO layers belonging to different test structures. These remaining photoresist was finally eliminated using a combination of acetone in the spin-coater and photoresist plasma incineration. All of this left, nevertheless, thinner ITO layers (around 280nm thick) with rather high ITO surface roughness.

Another problem detected in the process flow-chart presented in Figure 2. 45 is the fact that the 300nm thick ITO layer is deposited over the ITO-gate oxide only after a transportation to Fraunhofer IPMS in Dresden and the ITO-gate oxide exposure to contamination during this period. To quantify the contamination of the ITO-gate oxide during the wafer transportation, the ITO-gate MOS-C *C-V* curves were obtained for the MOS-C based test structures after different process fabrication steps, namely immediately after the ITO photolithography step, after the source/drain impurity activation step, and finally after the final passivation annealing step, performed at the end of the 0.5μm CMOS process, at 440°C during 30 minutes, respectively, all of which can be observed in Figure 2. 47(a). On the other hand, *C-V* measurements were performed on both, the ITO-gate and the polysilicon-gate MOS-C test structures immediately after the ITO photolithography step and are presented in Figure 2. 47(b), compared to the *C-V* curves simulated using the TCAD software for the structures of interest.



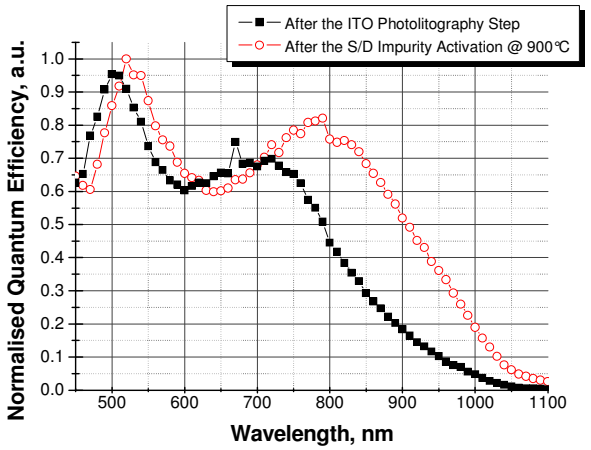
(a) (b)

Figure 2. 47 – (a) ITO-gate MOS-C C-V curves obtained after different high-temperature fabrication steps [ITOF07]; and (b) comparison between the ITO-gate MOS-C and polysilicon-gate MOS-C C-V curves, additionally compared to the C-V curves simulated using the TCAD software for the same structures [ITOF07].

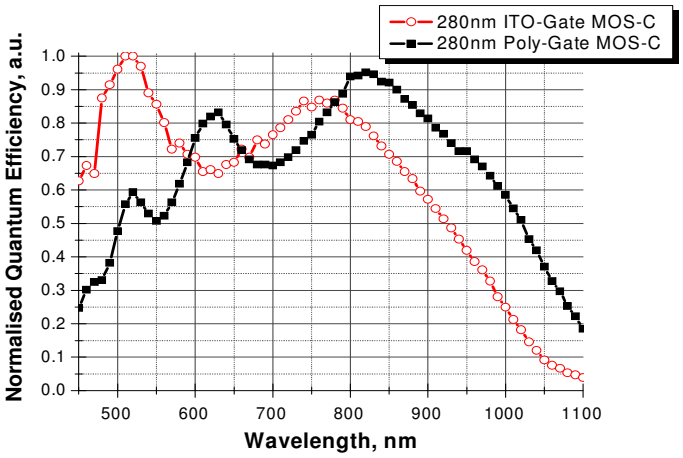
From Figure 2. 47(a) can be observed that the source/drain impurity activation step leads to the flat-band voltage shift of +1.05V, i.e. to the diffusion of the ITO-gate oxide contamination impurities acquired during the wafer transportation to Dresden. Fortunately, as it can also be observed in Figure 2. 47(a), the final passivation step present in the 0.5μm CMOS process flow-chart,

carried out at 440°c during 30minutes, reduces the number of oxide fast- and mobile- traps and shifts the *C-V* curve back again to the original value of the flat-band voltage.

On the other hand, from Figure 2. 47(b), the flat-band voltage obtained for the ITO-gate MOS-C structure was of –0.53V, while for the polysilicon-gate MOS-C it was of –0.82V, giving a difference of around 0.3V, which should also reflect the difference between the both threshold voltages. To obtain identical flat-band voltages in both cases, the threshold voltage control channel implantation should be optimised for the case of ITO-gate capacitors and eventual MOSFETs.



(a)



(b)

Figure 2. 48 – (a) The wavelength dependent normalised quantum efficiency graph obtained from the 4mm^2 ITO-gate MOS-C based test structures at different stages of fabrication, namely immediately after the ITO photolithography step, and after the 30 minute source/drain impurity activation step at 900°C, respectively [ITOF07]; (b) comparison between the wavelength dependent normalised quantum efficiency graphs obtained from the ITO-gate and polysilicon-gate MOS-C based test structures, respectively, immediately after the source/drain impurity activation high-temperature fabrication step [ITOF07].

The MOS-C based test structures, with ITO-gates, were then characterized at different stages of fabrication, using the measurement station described in Appendix B of this work. The results can be observed in Figure 2. 48(a) [ITOF07]. The first quantum efficiency curve (here presented in arbitrary units, a.u.) was obtained right after the ITO photolithography step. The second was measured after the 900°C source/drain impurity activation high-temperature step. From Figure 2. 48(a), it can be concluded that the quantum efficiency increased after the high-temperature step in the region of wavelengths higher than 750nm, and also in the region between the 520nm and 600nm, although decreasing for the soft UV-green (450nm-520nm) and the 620nm-700nm (red light) parts of the spectra.

On the other hand, together with the ITO-gate MOS-C based 4mm^2 test structures, similar polysilicon-gate MOS-C test structure were fabricated on the same p^+ doped wafer. Both sets of test structures were characterized using the measurement station described in Appendix B of this work, although without the optical bread-board part, and illuminating the structures "on-the-wafer", right after the source/drain impurity activation step. Figure 2. 48(b) shows the normalised quantum efficiency graphs obtained from both sets of test structures for impinging radiation with wavelengths in the range between the 450nm and 1100nm.

Observing Figure 2. 48(b), it can be concluded that ITO based PG structures present clear advantages (2 times higher quantum efficiency) over polysilicon-gate based PGs in the soft-UV to VIS part of the spectra (450nm – 580nm), although have a poorer performance for the NIR wavelengths (λ>780nm). Nevertheless, it must be taken into account that the two sets of test structures characterised, are still missing the BPSG and the inter-metal oxide layers normally present at the surface of the wafer at the end of the process flow, that introduce the wavelength dependent reflection maxima phase shifts and will probably change the quantum efficiency curves. Moreover, the sheet resistivity of the ITO layer (10Ω/sq) is still much lower than the resistivity of the polysilicon (40Ω/sq), which suggests that the ITO layer thickness should be reduced in order to meet an acceptable compromise between its transmittance and the conductivity, both figures of merit that should improve in this way, also enabling further optimisations in regard to the reflection maxima shifts, dependent on the layer thickness.

3 Pixel Configurations in the 0.5μm CMOS Process

Each CMOS pixel element, basic part of any CMOS image sensor built nowadays, normally contains a photodetector, a charge integrating amplifier (CIA), a reset and a select transistors, and an output amplifier. Pixels are arranged to form a pixel matrix. On top of the whole sensor, there lays a grid of metal interconnects that carry *timing* and *readout* signals. The column lines of this grid connect to a set of decode and readout multiplexed electronics that are arranged outside the pixel array. This structure allows signals from the entire array, a sub-array, or a single pixel to be readout by a simple *x-y* addressing technique.

From a contemporary point of view, CMOS pixels can be categorized in two basic groups, each with a huge number of variations as it will be seen later in this text: the *passive pixel sensors* (PPS), with one transistor per pixel, schematic of which (if using an *n*-well PD) is shown in Figure 3. 1(a), and *active pixel sensors* (APS), with 3 to 4 or even more transistors per pixel, a three transistor (3T) example of which is shown in Figure 3. 1(b).

In a PPS pixel, the photodiode is connected to a vertical column bus of the pixel array if the only existent transistor that serves as a pixel select switch becomes activated (Figure 3. 1(a)). Charge integrating amplifier readout circuit at the bottom of the column bus keeps the PD voltage on the bus constant, thus reducing the *reset* noise, defined below. The photodiode is then reset to this column bus voltage and the corresponding charge is converted to voltage by the charge integrating amplifier. Only if a second transistor is added, PPS can perform *x-y* addressing [Wer04]. Nevertheless, PPS suffer from many other limitations such as slow readout and lack of scalability, although, for a given pixel size, these pixel configurations also have the highest *fill factor* (the ratio of the photoactive area to the entire pixel area). The addition of an amplifier to each pixel alleviates these problems, and resulted in the creation of the *active pixel sensor* (Figure 3. 1(b)).

In an *n*-well PD based APS, the electrical charge generated by the photodiode is buffered using a *source-follower* amplifier. Therefore, the reading of the signal is non-destructive and much faster than in PPS. This buffer amplifier is the major difference between PPS and APS [Mey03, Ack96, Fos97]. In this chapter, all the possibilities of fabricating APS in the 0.5μm standard CMOS process under investigation will be profoundly analysed and various issues will be addressed ranging from *signal-to-noise ratio* (SNR), charge-coupling, power

consumption and response speed, to fill-factors regarding the various pixel configurations proposed.

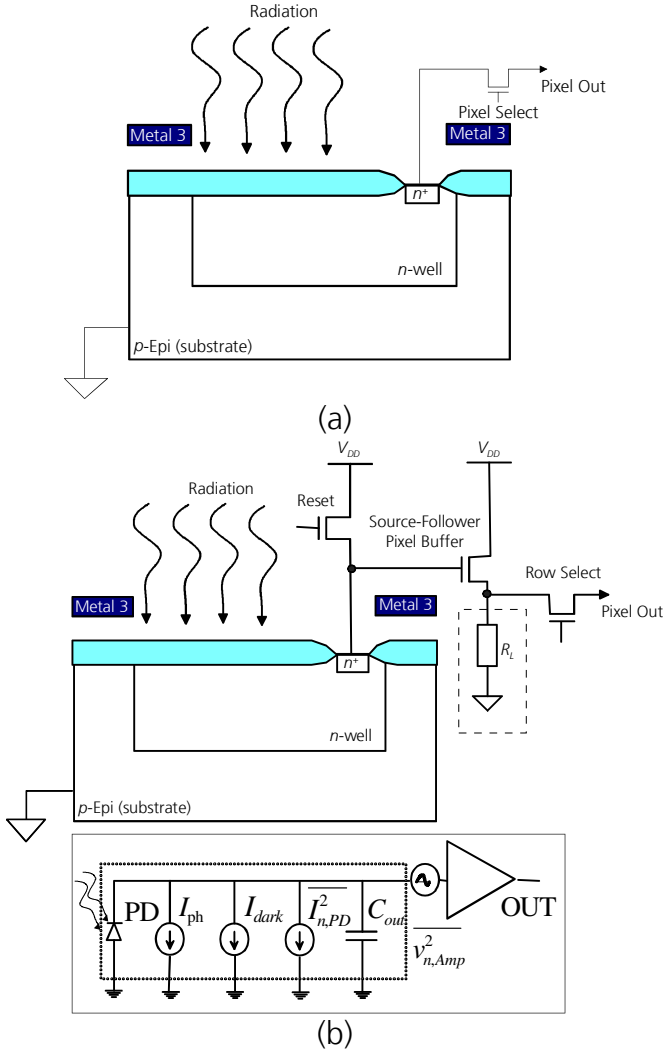


Figure 3. 1 – (a) Schematic of a one transistor (1T) *n*-well PD based *passive pixel sensor* (PPS); (b) schematic of a three transistor (3T) *n*-well PD based *active pixel sensor* (APS) and its electrical model showing the sources of noise (lower part).

3.1 Signal-to-Noise Ratio (SNR) Issues in Active Pixel Sensors

To be able to discuss *signal-to-noise ratio* (SNR) issues regarding the active pixel sensors, at first a fair deal of attention should be put on *noise*: the unwanted signals that appear as a result of random processes and interfere with the APS output signal. Noise signals cannot be described by closed-form time domain expressions, i.e. they are stochastic. So, as noise cannot be represented by a mathematical function, it must be characterized by probability and statistics [Lea94].

In this sense, an acceptable way to represent any noise signal is by using its *probability density function* $p(x)$. It is a function that describes the probability density in terms of the input variable x, if $p(x) \geq 0$ for any value of x, where the probability of the x values of interest to lie in the range from certain x_1 to x_2 is defined as the area under the curve of $p(x)$ between these values, as shown in

Eq. (3. 1) [Lea94]. This is valid if $p(x)$ satisfies Eq. (3. 2) [Lea94], i.e. if it is certain with 100% of probability that x falls in the range $-\infty < x < \infty$.

$$\Pr obability(x_1 < x < x_2) = \int_{x_1}^{x_2} p(x)dx \tag{3. 1}$$

$$\int_{-\infty}^{\infty} p(x)dx = 1 \tag{3. 2}$$

Moreover, the *integrated probability density function*, $P(x)$ is defined by Eq. (3. 3) [Lea94]. This function gives the probability that a single observed value lies in the range from $-\infty$ to x, being $P(-\infty)=0$, $P(\infty)=1$, and $p(x)$ as expressed by Eq. (3. 4) [Lea94].

$$P(x) = \int_{-\infty}^{x} p(\xi)d\xi \tag{3. 3}$$

$$p(x) = \frac{d}{dx}P(x) \tag{3. 4}$$

On the other hand, the *variance* σ^2 of a random variable x is defined as the average value of $(x-\bar{x})^2$ [Lea94]. Namely, for N sources of x, assumed identical in that each is governed by the same process, where the output of each source is described by the same probability density function, it can be assumed that the sources are independent in the sense that the value of the output of one does not depend on the value of the output of any other. If the outputs of all sources are observed at the same time t_1, and if $x_i(t_1)$ is the output of the ith source, the *ensemble average* of $x(t_1)$ is defined by Eq. (3. 5) [Lea94].

$$\overline{x(t_1)} = \frac{1}{N}\sum_{i=1}^{N} x_i(t_1) \tag{3. 5}$$

If N is assumed sufficiently large so that the result does not significantly change if N is increased, and if x is independent of time over the time interval of interest, the random process is said to be stationary, and the *ensemble average of* x ($\bar{x}$) is defined by Eq. (3. 6) [Lea94]. This equation can be generalized to obtain the ensemble average of any function $f(x)$ of a random variable x, as defined by Eq. (3. 7) [Lea94].

$$\bar{x} = \frac{1}{N}\left[\int_{-\infty}^{\infty} N \cdot x \cdot p(x)dx\right] = \int_{-\infty}^{\infty} x \cdot p(x)dx \tag{3. 6}$$

$$\overline{f(x)} = \int_{-\infty}^{\infty} f(x)\,p(x)dx \tag{3. 7}$$

For x being a voltage or a current, the variance is the mean-square value of its AC component, defined by Eq. (3. 8) [Lea94].

$$\sigma^2 = \overline{\left(x - \bar{x}\right)^2} = \int_{-\infty}^{\infty} \left(x - \bar{x}\right)^2 p(x) dx \tag{3. 8}$$

The square-root of the variance, i.e. σ, is called the *standard deviation*. If x is a voltage or a current, its standard deviation is simply the rms value (root of the mean of the square, or the square root of the mean-squared voltages) of its AC component. Because noise signals do not have a DC component, the variance is equal to the rms value [Lea94]. By the way, the rms definition is based on the equivalent heating effect. The true rms voltmeters measure the applied time-dependent voltage $v(t)$ according to Eq. (3. 9) [Mot93], where T is the period of the voltage.

$$V_{rms} = \sqrt{\overline{v^2}} = \sqrt{\frac{1}{T}\int_0^T \overline{v^2}(t) dt} \tag{3. 9}$$

Following [Lea94], the notation from here on (also shown in Eq. (3. 9)) considers noise to be a small-signal variable which is defined as the rms value calculated from the instantaneous noise voltages and currents, i.e. $v_n(t)$ and $i_n(t)$, respectively. The mean square values are the square of the rms values and are written $\overline{v_n^2}$ and $\overline{i_n^2}$.

Much noise has a *Gaussian* or *normal* distribution of instantaneous amplitudes with time [Mot93]. The *Gaussian* curve is limiting case produced by overlying an imaginary coordinate grid structure on the noise waveform. If one could sample a large collection of data points and tally the number of occurrences when the noise voltage level is equal to or greater than a particular level $\bar{x}$, the *Gaussian* curve would result, mathematically described as Eq. (3. 10) [Mot93]. Eq. (3. 10) is in this case the *probability density function* of noise following the *Gaussian* distribution. On the other hand, lots of phenomena observed in nature follow the so called *Poisson* distribution, just as several mechanisms giving rise to noise do. The *Poisson* probability distribution, as well as different noise mechanism relevant to the current study will be explained later in the text.

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left[\frac{-\left(x - \bar{x}\right)^2}{2\sigma^2}\right] \tag{3. 10}$$

The spectral density of a random variable is defined as its mean-square value per unit bandwidth. For a noise-voltage, it is denoted by the symbol $S_v(f)$ and has the units V^2/Hz. For a noise current, it is denoted by the symbol $S_i(f)$ and has the units A^2/Hz [Lea94]. Let $v_n(t)$ be a zero-mean random voltage that is defined over the time interval $-T/2 \le t \le T/2$. It is assumed that $v_n(t) = 0$ outside

this interval and that it can be defined by Eq. (3. 6), i.e. that the process is *ergodic*. The mean-square value of $v_n(t)$ can be written as the time average, expressed by Eq. (3. 11).

$$\overline{v_n^2} = \frac{1}{T}\int_{-T/2}^{T/2} v_n^2(t)dt \tag{3. 11}$$

If a function of frequency $S_v(f)$ is defined such that $\overline{v_n^2}$ can be also defined by Eq. (3. 12), then $S_v(f)\Delta f$ is interpreted as being the amount of $\overline{v_n^2}$ that is contained in the frequency band from f to $f+\Delta f$, where Δf is small [Lea94]. In this case, $S_v(f)$ is called the *spectral density* of $v_n(t)$ and it has the units of V^2/Hz.

$$\overline{v_n^2} = \int_0^{\infty} S_v(f)df \tag{3. 12}$$

Three main types of fundamental noise mechanisms taking place in any electronic circuit are the so called *thermal* noise, *shot* noise, and low-frequency (1/*f*) or *flicker* noise [Mot93].

Thermal noise is caused by the random thermally excited vibration of the charge carriers in a conductor. It was first observed by J. B. Johnson of *Bell Telephone Laboratories* in 1927, and a theoretical analysis was provided by H. Nyquist in 1928 [Mot93]. Because of their work, thermal noise is called *Johnson noise* or *Nyquist noise*. Nyquist namely showed that the mean-square open-circuit thermal noise voltage across a resistor ($\overline{v_{n\_t}^2}$) is given by Eq. (3. 13) [Lea94]. The corresponding mean-square short-circuit thermal noise current ($\overline{i_{n\_t}^2}$) is given by Eq. (3. 14) [Lea94].

$$\overline{v_{n\_t}^2} = 4k_B TR\Delta f \tag{3. 13}$$

$$\overline{i_{n\_t}^2} = \frac{\overline{v_{n\_t}^2}}{R^2} = \frac{4k_B T\Delta f}{R} \tag{3. 14}$$

Regarding a more general case, for Z the complex impedance of a two terminal network, the mean-square thermal noise voltage generated by this impedance in the band Δf is given by Eq. (3. 15) [Lea94], a *Nyquist formula* for a complex impedance. Because Z is a function of frequency, Δf must be small enough so that Re(Z) is approximately a constant over the band. Otherwise, the noise must be expressed by an integral. Following, the mean-square, short-circuit thermal noise current in the frequency band Δf is given by Eq. (3. 16) [Lea94].

$$\overline{v_{n\_t}^2} = 4k_B T\,\mathrm{Re}(Z)\Delta f \tag{3. 15}$$

$$\overline{i_{n\_t}^2} = \frac{4k_B T\,\mathrm{Re}(Z)\Delta f}{|Z|^2} = \frac{4k_B T\Delta f}{\mathrm{Re}(Z)} \tag{3. 16}$$

The spectral density of a noise source is the mean-square value of the source per unit band-width. In general, the spectral density is a function of frequency. The voltage and current spectral densities, respectively, for the thermal noise generated by a complex impedance *Z* are given by Eqs. (3. 17) and (3. 18) [Mot93]. The spectral density of the thermal noise generated by a resistor is independent of frequency, i.e. it is said to be uniform or flat. It is also called *white noise* by analogy to white light which also has a flat spectral density in the optical band.

$$S_v(f) = \frac{\overline{v_{n\_t}^2}}{\Delta f} = 4k_B T\,\mathrm{Re}(Z) \tag{3. 17}$$

$$S_i(f) = \frac{\overline{i_{n\_t}^2}}{\Delta f} = \frac{4k_B T}{\mathrm{Re}(Z)} \tag{3. 18}$$

The available noise power in a conductor, N_t, is found to be proportional to the absolute temperature and to the bandwidth of the measuring system, as shown in Eq. (3. 19) [Mot93]. Thermal noise ultimately limits the resolution of any measurement system. Even if an amplifier could be built perfectly noise-free, the resistance of the signal source would still contribute noise [Mot93].

$$N_t = k_B T\Delta f \tag{3. 19}$$

On the other hand, *shot* noise is generated by the random emission of electrons or by the random passage of electrons and holes across a potential barrier. The shot noise generated in a device is modelled by a parallel noise current source (Figure 3. 1(b)). The mean-square shot noise current $\overline{i_{n\_sh}^2}$ in the frequency band Δf is given by Eq. (3. 20) [Lea94], where I_{DC} is the DC current flowing through the device. This equation is known as the *Schottky formula*. The spectral density of shot noise is given by Eq. (3. 21) [Lea94]. This is constant with frequency, thus shot noise is also a *white noise*.

$$\overline{i_{n\_sh}^2} = 2qI_{DC}\Delta f \tag{3. 20}$$

$$S_i(f) = \frac{\overline{i_{n\_sh}^2}}{\Delta f} = 2qI_{DC} \tag{3. 21}$$

Flicker noise is, nevertheless, a noise that has a spectral density that is proportional to $1/f^n$, where $n \cong 1$. It is also called "one-over-*f*-noise". This type of noise seems to be a systematic effect inherent in electrical conduction. Various explanations of its origin have been made, but it remains an ill-

understood phenomenon [Lea94]. In resistive materials, its origin seems to be caused by a fluctuation of the mobility of the free charge carriers. In semiconductors, it is generated by tunnelling effects in the surface oxide layer of the material. It can be also generated by the imperfect contact between two conducting materials, in which case it is called *contact* noise. The 1/*f* spectral density of flicker noise has been shown to hold down to extremely low frequencies, and is modelled also as a noise current in parallel with a device (Figure 3. 1(b)). In general, the mean-square *flicker* noise current in the frequency band Δf is given by Eq. (3. 22) [Lea94], where $n \cong 1$, K_f is the flicker noise coefficient, and *m* is the flicker noise exponent. The spectral density is given by Eq. (3. 23) [Lea94]. Actually, if carrier trapping and detrapping mechanisms are modelled, then a *Lorentzian* spectrum (i.e. $\propto \frac{1}{f^2}$) is obtained. If different trapping times are involved, then we obtain an evelope exhibiting 1/*f* behaviour. Nevertheless, since in short-channel MOSFETs the gate area is smaller, a tendency towards $\frac{1}{f^2}$-behaviour is to be observed in this case instead of the expected $\frac{1}{f}$-behaviour.

$$\overline{i_{n\_f}^2} = \frac{K_f I_{DC}^m \Delta f}{f^n} \tag{3. 22}$$

$$S_i(f) = \frac{\overline{i_{n\_f}^2}}{\Delta f} = \frac{K_f I_{DC}^m}{f^n} \tag{3. 23}$$

The possible solution normally applied for reduction of the low-frequency noise is the correlated double sampling (CDS) that acts in the baseband both, as a high-pass filter for DC offsets and the 1/*f* noise. The CDS transfer function can be defined as $|H(f)|^2 = 4\sin^2(\pi \Delta f T_D)$, where T_D is the sample-to-sample time, as it will be explained more in detail later in this text. Nevertheless, CDS doubles the noise power of the *white noise*. Additional measures are needed then to suppress this side effect [The96]. Here, attention must be paid to noise of individual devices.

Finally, and keeping all the definitions formulated so far in mind, the *signal-to-noise ratio* (SNR), usually measured at the output of a circuit where the signal and noise voltages are larger (if an amplifier forms part of it) and easier to measure, is given by Eq. (3. 24) [Lea94], specified in dB, where v_{so}^2 is the output signal voltage power and $\overline{v_{no}^2}$ is the mean-square noise output voltage. When the calculation of the SNR is made at the circuit input, and the source is modelled by a *Thévenin* source (in series connection with the impedance), it is given by $SNR = v_s^2 \Big/ \overline{v_{ni}^2}$, where v_s^2 is the input signal voltage power and $\overline{v_{ni}^2}$ is the mean-square equivalent input noise voltage. When it is modelled by a *Norton* source

(in parallel with the impedance), it is given by $SNR = i_s^2 \Big/ \overline{i_{ni}^2}$, where i_s^2 is the input signal current power and $\overline{i_{ni}^2}$ is the mean-square equivalent input noise current, the case depicted in the lower part of Figure 3. 1(b).

$$SNR = 10\log\left(\frac{v_{so}^2}{\overline{v_{no}^2}}\right) \tag{3. 24}$$

To be able to discuss the SNR of the *n*-well PD based APS depicted in Figure 3. 1(b), its operation principle should be examined more in detail. Here, when the *reset* NMOS transistor is turned "on", the *n*-well PD is effectively connected to the power supply V_{DD}, charging the SCR capacitance to the voltage V_{DD}, but –due to the noise of the reset transistor- with an uncertainty called "reset noise". This charging operation constitutes the so called photodiode *reset* phase. Since the reset transistor in Figure 3. 1(b) is of *n*-type, the pixel operates in the so called "soft" reset mode. Soft reset advantageously results in low reset-noise and a high *power supply rejection ratio* (PSRR) [Pai00]. However, disadvantageously, soft reset results also in high image lag, and yields a markedly non linear response under low illumination. Nevertheless, the NMOS transistor, used in this case to reset the PD, acts also as an anti-blooming measure, as it prevents the *p-n* based PD to become forward-biased. On the other hand, the so called "hard" reset mode, normally achieved by using a PMOS transistor for this task, advantageously eliminates image lag but increases the reset noise and dark current, and reduces PSRR [Pai00] and fill-factor -specially for small pixel sizes-.

Addressing the mentioned noise problems, this reset mechanisms give rise to two spurious noise components, the so called *reset* and *partition* noises, respectively. This kind of noises, closely related to the *thermal* noise, are important at all locations at which capacitors are charged and discharged through a circuit and appear due to the thermodynamical uncertainty of the charge on a capacitor. Considering the electrical model of the noise sources present in an *n*-well PD based APS, depicted in the lower part of Figure 3. 1(b), the complex impedance Z –consisting of the *n*-well PD capacitance C_{PD} connected in parallel to the undepleted silicon resistance R_B added to the resistance of the joint metal connecting layers, jointly expressed through R_M- is defined using Eq. (2. 25) [Lea93]. On the other hand, considering Eqs. (3. 11) and (3. 15), the total open-circuit mean-square reset noise voltage $\overline{v_n^2}$, measured at the pixel output, with $\omega=2\pi f$, is expressed using Eq. (3. 26). Here, ξ is the so called *reset constant* that takes the value of 0.5 for the case of *soft* reset and 1 for *hard* reset operations [Pai00]. Eq. (3. 26) results nevertheless valid for $t\rightarrow\infty$. The precise expression in time domain should incorporate the term $\left(1-e^{-\frac{t}{R_B C_{PD}}}\right)$ multiplying the result of Eq. (3. 26).

$$Z = R_M \left\| \left(\frac{1}{j\omega C_{PD}} \right) = \frac{R_M}{1 + j\omega C_{PD} R_M} = \frac{R_M}{1 + (\omega R_M C_{PD})^2} - j \frac{\omega R_M^2 C_{PD}}{1 + (\omega R_M C_{PD})^2} \right. \quad (3.\ 25)$$

$$\overline{v_n^2} = \xi \int_0^\infty 4k_B T \,\mathrm{Re}(Z) df = \xi \int_0^\infty \frac{4k_B T R_M}{1 + (2\pi f R_M C_{PD})^2} df = \xi \frac{2k_B T}{\pi C_{PD}} \int_0^\infty \frac{dx}{1 + x^2} = \xi \cdot \frac{k_B T}{C_{PD}} \quad (3.\ 26)$$

$\overline{v_n^2}$ is independent of R_M, and this noise is often referred as "k_BT/C (kT over C) noise". In CMOS imaging it is used to express the amount of noise using the so called *equivalent noise charge* (ENC). If the k_BT/C noise was expressed in Eq. (3. 26) as the mean-square noise voltage $\overline{v_n^2} = Q_n^2 / C_{PD}^2$, then the ENC due to k_BT/C can be expressed as Eq. (3. 27).

$$ENC_{k_BT/C} = \frac{\sqrt{\xi \cdot k_B T C_{PD}}}{q} \quad (3.\ 27)$$

Moreover, it was found that there exists an additional noise source, the so called *partition* noise, closely related to the reset noise, which used to be embedded in the reset noise model with a scaling factor α_{part} applied to the conventional thermal noise source [Lai05]. α_{part} is found to be inversely related to the fall time of applied gate pulse (in this case, the pulse applied to the *reset* transistor depicted in Figure 3. 1(b)). It is believed that a fast fall time will trap residual charge in the channel after the transistor pinches off. The leftover charge is the primary source of partition noise [Lai05]. For standard used clocking signals provided normally by *Flip-Flop* devices, rise and fall times present in the signal are of around 2ns, for which value α_{part}=1..3, and the mean-square partition noise voltage can be expressed as Eq. (3. 28), where C_{G_RST} is the gate capacitance of the reset transistor shown in Figure 3. 1(b). Following the same development pursued to obtain Eq. (3. 27), the *partition* ENC is defined by Eq. (3. 29).

$$\overline{v_{n\_par}^2} = \alpha_{part} \cdot \frac{2(k_B T C_{G\_RST})}{\pi^2 C_{PD}^2} \quad (3.\ 28)$$

$$ENC_{part} = \frac{\sqrt{2\alpha_{part} \cdot k_B T C_{G\_RST}}}{q\pi} \quad (3.\ 29)$$

On the other hand, the so called *dark current* noise is the statistical variation of the number of collected thermally generated charge carriers. This noise is closely related to the *shot* noise and originates due to physical mechanisms involved in the dark current generation within the PD, explained in detail in Chapter 2 of this text, during a certain integration time T_{int}. The dark current noise follows the so called *Poisson* probability distribution function, discovered by Simeón-Denis Poisson, expressed by Eq. (3. 30), for k=(0,1,2,...). The *Poisson* distribution describes discrete occurrences (thermal generations) that

take place during T_{int}. Here, $\overline{n_{dark}}$ is not only the mean number of thermally generated carriers, but also its variance σ^2_{dark}. Thus, the number of thermally generated electrons fluctuates about $\overline{n_{dark}}$ with a standard deviation $\sigma_{dark} = \sqrt{\overline{n_{dark}}}$. The dark current noise cannot be suppressed using CDS methods [Yon00]. This is because the dark current noise is *white* in general and CDS can suppress only correlated noise. In consequence, minimizing dark current minimizes this noise. Finally, following the definitions enlisted so far, the *dark* ENC, represented by the variance of thermally generated carriers occurring during T_{int}, i.e. its mean value, is given by Eq. (3. 31).

$$f(x,t) = \frac{e^{-\overline{xt}}\overline{x}^{k}}{k!} \tag{3. 30}$$

$$\sigma^2_{dark} = \overline{n_{dark}} = \frac{I_{dark} \cdot T_{\text{int}}}{q} \tag{3. 31}$$

Continuing with the noise mechanisms involved in *n*-well PD photodetection, another noise component of importance is the *photon shot* noise, which originates from the nature of the impinging radiation itself: a photon striking on an object that also follows the *Poisson* probability distribution function. Just as in the case of dark current noise, the variance of the mean value of carriers generated by impinging photon flux equals its mean value, i.e. $\sigma^2_{ph} = \overline{n_{ph}}$. This is a fundamental problem, so the aim for 100% fill factor and quantum efficiency is at the same time, the aim for reduced photon shot noise. The ENC due to photon noise, represented by the variance of the number of carriers generated by impinging photon flux occurring during T_{int}, σ^2_{ph}, is defined by Eq. (3. 32).

$$\sigma^2_{ph} = \overline{n_{ph}} = \frac{I_{ph} \cdot T_{\text{int}}}{q} \tag{3. 32}$$

Continuing with the noise analysis of the *n*-well PD based APS depicted in Figure 3. 1(b), the second (SF) transistor shown in the electrical diagram forms part, together with the load resistor R_L (normally substituted by a *current-mirror*), of the already mentioned *source-follower* pixel buffer amplifier. This allows the *n*-well PD output voltage V_{PD}, related through a proportionality factor C_{PD} to the amount of integrated charge Q_{PD} collected in the *n*-well during T_{int}, to be observed without removing Q_{PD}, i.e. in a non-destructive manner. Following Eq. (3. 8), the variance of the pixel output signal caused by the SF buffer amplifier, defined here as the *SF* noise, is defined by Eq. (3. 33), as the variance σ^2_{SF} of the *SF*, $ENC_{SF} = C_{PD} \cdot \frac{\sqrt{\overline{v^2_{n\_SF}}}}{q}$, where $\overline{v^2_{n\_SF}}$ is the input-referred mean-square noise voltage.

$$\sigma_{SF}^2 = \frac{C_{PD}^2 \cdot \overline{v_{n\_SF}^2}}{q^2} \tag{3. 33}$$

Finally, the *row-select* transistor allows a single row of the pixel array to be read out by the readout electronics, and the pixel SNR can be expressed as shown in Eq. (3. 34).

$$\begin{aligned} SNR &= 10 \cdot \log\left(\frac{\overline{n_{ph}}^2}{\sigma_{dark}^2 + \sigma_{ph}^2 + \sigma_{k_BT/C}^2 + \sigma_{part}^2 + \sigma_{SF}^2} \right) = \\ &= 10 \cdot \log\left(\frac{\overline{n_{ph}}^2}{\overline{n_{dark}} + \overline{n_{ph}} + \frac{k_B T C_{PD}}{q^2} + \frac{2\alpha_{part} \cdot k_B T C_{G\_RST}}{\pi^2 q^2} + \frac{C_{PD}^2}{q^2} \cdot \overline{v_{n\_SF}^2}} \right) \end{aligned} \tag{3. 34}$$

Two extreme cases can be defined for the SNR. On one hand, the maximum SNR (SNR_{max}) of a pixel to be used in a specific application is obtained by considering the maximum number of photogenerated carriers $\overline{n_{ph,\max}}$ instead of $\overline{n_{ph}}$ in Eq. (3. 34). This $\overline{n_{ph,\max}}$ is defined by Eq. (3. 32), only considering the maximum photocurrent $I_{ph,max}$ produced for the highest impinging irradiance and the maximum collection efficiency of photogenerated carriers in the specific application. On the other hand, the minimum SNR (SNR_{min}) describes the pixel operation in darkness, i.e. where $\overline{n_{ph}} = 0$. The amount of thermally generated carriers in darkness $\overline{n_{dark}}$ depends on the amount of dark current flowing in the pixel, explained in detail in Chapter 2, as defined by Eq. (3. 31).

Regarding Eq. (3. 34), the *n*-well PD APS *equivalent noise charge* can be obtained as shown in Eq. (3. 35). From Eq. (3. 35) it can be concluded that in order to diminish the amount of noise carriers, and considering the *photon* shot noise, an unavoidable effect independent of the photodetector pixel structure, the only two parameters which can be optimised (i.e., minimized) are the dark current flowing in the photodetector, the RST transistor gate capacitance C_{G_RST}, and the photodetector capacitance C_{PD}. The partition noise, directly proportional to C_{G_RST} has, nevertheless, a minor contribution to the pixel ENC, as it will be shown later in this text.

$$ENC = \sqrt{\overline{n_{dark}} + \overline{n_{ph}} + \frac{k_B T C_{PD}}{q^2} + \frac{2\alpha_{part} \cdot k_B T C_{G\_RST}}{\pi^2 q^2} + \frac{C_{PD}^2}{q^2} \cdot \overline{v_{n\_SF}^2}} \tag{3. 35}$$

Moreover, as it was explained above, the commonly used low-frequency noise reduction method in discrete-time circuits is CDS. The reduction of the white noise is, however, much more involved. There are several techniques which can be followed for low-noise analog circuit design. For example, in amplifiers the gain and bandwidth management is absolutely essential. The front

gain stages should provide enough gain so that the noise contribution of the following stages is negligible. On the other hand, the transconductances of active loads and current sources should be sufficiently low so their noise is not greatly amplified [Hos07]. In addition, the bandwidth limitation, particularly important in the case of white noise must be also carefully controlled [Hos07].

To illustrate the pertinence of the analysis developed so far in what the pixel and the entire imager designs are concerned, the sensor requirements to be used in 3-D imaging based on the *time-of-flight* (TOF) measuring method will be examined as an example, and several issues ranging from charge-coupling possibilities to noise, spectral responsivity and fill-factor of several pixels proposed for this task, to be fabricated in the 0.5μm standard CMOS process under investigation, will be discussed in the next section.

3.2 Time-of-Flight 3-D Imaging in the 0.5μm Standard CMOS Process

For three-dimensional (3-D) imaging applications, essential for highly reliable object recognition and indispensable for measurement of object distance, shape, and volume (mainly for machine-vision applications [Elk04]), two approaches are normally used. On one side, there exist the triangulation approach, either based on passive [Bes88] or active (e.g., projected fringe methods [Dor94]) measurement methods, both of which rely on stereoscopic vision properties. This approach, nevertheless, presents numerous problems. Not only it requires scenes featuring high contrast, and for the case of active triangulation, the method also requires high speed mechanical scanning for 3-D imaging, which calls for expensive and bulky moving high-precision mechanical parts [Lan01]. On the other side, *time-of-flight* (TOF) approach, based on measuring the time required for an emitted light beam to reach an object, be reflected by it, and for the reflected beam to reach an imager localized in the vicinity of the light source. Although the TOF method also employs mechanical scanning in so called laser scanners, here we consider new "scannerless" approaches. Such an approach is depicted in Figure 3. 2, where the laser beam is spread out using a diffuser to cover an entire scene [Elk04]. This method is well competing with the triangulation measurement methods mainly due to its simplicity.

The TOF method is available in two main versions: based on light pulse modulation [Elk04, Nic05, Saw07], and on continuous wave modulation [Lan01]. In the first TOF method mentioned, total flight time of a light pulse is measured instead of the phase difference between emitted and received signals, as used in continuous wave modulation. The main advantage of the pulse- over continuous wave modulation-based methods is that due to its nonambiguity the operation range of a few meters to several kilometres can be achieved avoiding the use of different modulation frequencies [Nic05]. Nevertheless, to achieve milimetric accuracies, the TOF systems based on pulse-modulation must have pico second time discrimination capability, high detection speed, low noise, and high SNR. The problem of so short time scales are the short integration times of photogenerated current, i.e. the reduced amount of integrated charge and

problems regarding its proper readout, specially if the background- to pulse-originated illumination discrimination is taken into account. So, to achieve an acceptable SNR, a special effort should be invested into reduction of the amount of noise present in the pixel, or increase of the amount of signal carriers collected during the integration phase. The SNR could be improved by using high-power light sources, but this is implying high power dissipation, high cost, and possible violation of eye safety regulations. Single photon avalanche photodiodes [Nic05] are in this sense a good alternative, although they cannot be fabricated in standard CMOS processes without extra fabrication masks and additional implantations. On the other hand, regarding the noise reduction, offset and 1/*f* noise voltages present in the output signal of each pixel, as well as the background illumination effects, can be cancelled by applying correlated-double-sampling operation, which can be readily implemented in the readout electronics.

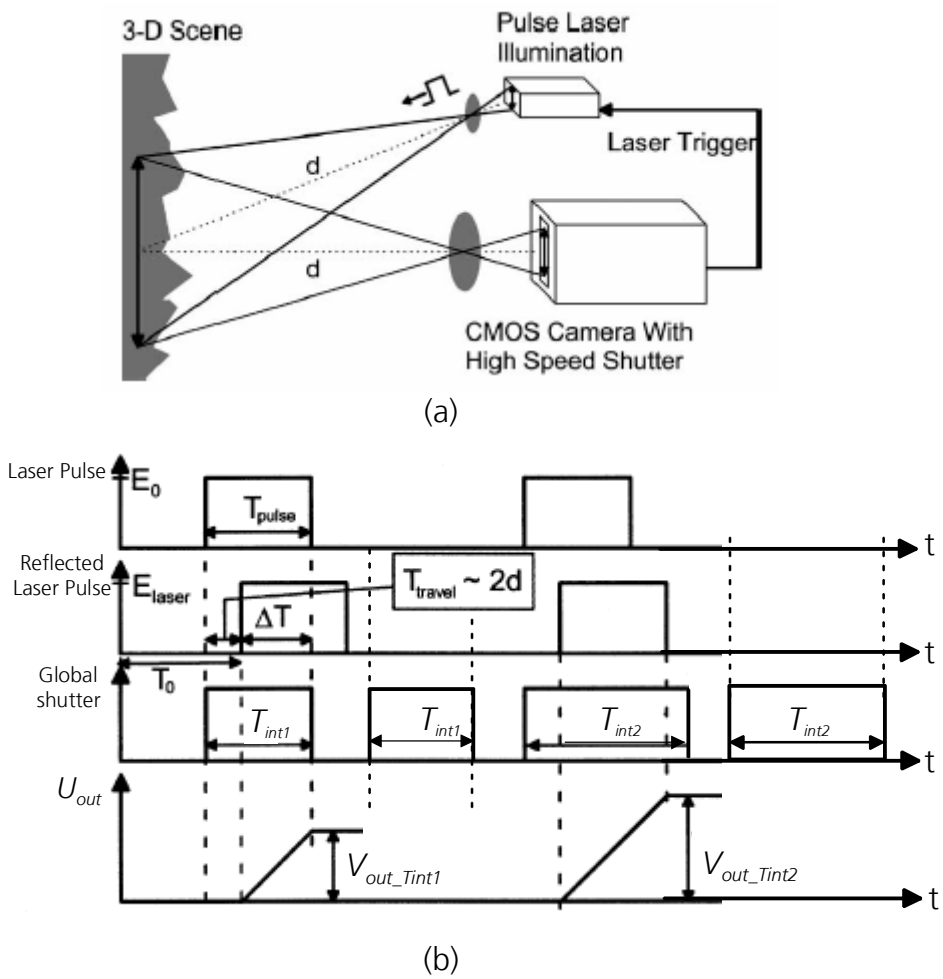


Figure 3. 2 – (a) TOF based 3-D measurement principle [Elk04]; (b) time diagram [1] for (a).

For 3-D range sensing purposes, we apply the *time-of-flight* (TOF) method depicted in Figure 3. 10. Here, the laser diode operating in the near-infrared (NIR) part of the spectra (λ=910nm) emits at first a 30ns to 200ns long radiation pulse (implying measurement range between the 4.5m [Elk04] and 18m, respectively), widespread through a simple optical diffuser to illuminate an entire scene area. The laser pulse emission is synchronized with the start of the

(previously discharged) photodetector array employing a global electronic shutter. The pulse is then reflected from an object and travels back to the photodetector array where it starts to generate a photocurrent. The resulting charge is defined by the photocurrent and the integration time. This integration time is then given by the shutter time window minus pulse travel time. This time is here designated as T_{int1}. However, if there is a variable delay between the firing of the laser pulse and the start of T_{int1}, the initial point of the measurement can be fixed at will, remaining the maximum range determined by the $c{\cdot}T_{pulse}$ multiple, where c is the speed of light in vacuum and T_{pulse} the laser emitted pulse width. The charge collected within the photodetector array corresponds at this time to the impinging radiation coming from the background illumination, added to the radiation due to the pulse reflected from the target scene.

Following the process just described, a second photocurrent integration is performed, this time without a laser pulse to be fired, i.e. the photocharge is generated by background illumination only, using T_{int1} again. The CDS stages, one per array column, are also used as a row-wise multiplexed analog memories, adding an extra C_{Fx} capacitor per pixel to each CDS circuit, as it can be observed in Figure 3. 3 [Elk06]. At the end of T_{int1}, according to the selected row of the pixel matrix, the sampling capacitance C_{c1} is charged to the selected pixel output voltage U_1. Following this, a second photocurrent integration is performed, this time without a laser pulse to be fired, i.e. the photocharge is generated by background illumination only, using T_{int1} again. The second pixel output voltage U_2 is then substracted from the already stored U_1, and the resulting voltage difference U_{out_Tint1}, amplified by the CDS amplification factor (e.g., $A_{CDS} = 4$), is stored at the chosen C_{Fx} capacitor by closing the correspondent A_{ccx} switch (Figure 3. 3). The entire pixel array is then read out in a rolling manner.

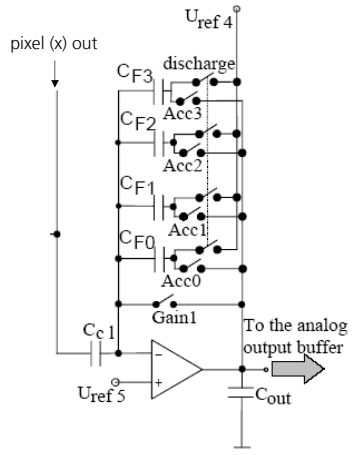


Figure 3. 3 - CDS and multiplexed analog memory circuit [Elk06].

The amount of reflected radiation reaching the TOF sensor depends on the laser power, the reflectance properties of the targeted objects in the scene, and their particular distance d from the sensor, that obeys an inverse square-law relation to it. So, a reference amount of impinging radiation coming from the entire laser pulse is required, obtained in an integration time T_{int2} chosen so large that the irradiance corresponding to the entire reflected pulse can be integrated

for the same operating conditions (Figure 3. 2(b)). As the integration time T_{int1} of the photodetector array is synchronized (even if a fixed time delay is used for the start of the shutter, as described above) with the laser pulse emission, the corresponding part of the reflected pulse impinging on the array in this integration time, related to the complete reflected pulse radiation integrated in T_{int2}, is used to determine the distance of the targeted object as shown in Eq. (3. 36) [Elk04], for U_{out_Tint1} the pixel output voltage after T_{int1}, and U_{out_Tint2} after T_{int2}. The time diagram corresponding to the range measurement described so far can be observed in Figure 3. 2(b). This measuring method is called multiple double short integration time (MDSI) [Men01].

$$d = \frac{c}{2} \cdot T_{pulse} \left(1 - \frac{U_{out\_T_{\text{int}1}}}{U_{out\_T_{\text{int}2}}} \right) \tag{3. 36}$$

Each of the measurements is then performed using n laser pulses during T_{int1} and T_{int2}, respectively. The resulting U_{out_Tint1} and U_{out_Tint2} are respectively accumulated at the C_{Fx} memory n times, increasing the pixel final output voltage U_{out_final} as shown in Eq. (3. 37) for T_{int1}, for example.

$$U_{out\_final\_T\,\text{int}1}(x) = U_{ref\,4} - n \cdot \frac{C_{C1}}{C_{F_x}} U_{out\_T\,\text{int}1}(x) \tag{3. 37}$$

Since all the high-frequency noise is uncorrelated, the SNR increases here with $\sqrt{n}$ (see Eq. (3. 34)), and extends the sensor range resolution by a factor of $n/\sqrt{n} = \sqrt{n}$. Finally, the $U_{out\_final\_Tint1}$ and $U_{out\_final\_Tint2}$ are to respectively substitute U_{out_Tint1} and U_{out_Tint2} in Eq. (3. 36). Once again, x designates here the determined pixel whose signal is being read out at the moment of interest.

Normally, for range measurements up to 4.5m, 4 laser pulses (n=4) are sufficient to accomplish an acceptable range resolution. For measurements reaching the 20m, 64 laser pulses (n=64) should be used. In this sense, the system (containing the sensor and the laser module) response time $t_{response}$ can be defined as shown in Eq. (3. 38).

$$t_{response}(n, n_{row}, N_{pixel}) = 2 \cdot [t_{set-up} + t_{acq}(n) + (t_{readout} \cdot N_{pixel})] \tag{3. 38}$$

In Eq. (3. 38), $t_{readout}$ (~330ns) is a single pixel readout time and N_{pixel} is the number of pixels of the entire sensor. The system acquisition time t_{acq} is defined as shown in Eq. (3. 39), where t_{CDS} (~2μs) is the time between single integration periods, n_{row} the number of pixel rows in the entire sensor, and t_{wait} the additional time required to achieve the condition $t_{acq}(n) \geq \frac{n}{f_{laser,\max}}$, where $f_{laser,max}$≈10kHz is the maximum laser repetition rate (number of laser pulses per second). From Eqs. (3. 38) and (3. 39), it can be concluded that the limiting factor of the system response time is actually $f_{laser,max}$.

$$t_{acq}(n) = n \cdot [t_{CDS} \cdot (1 + n_{row}) + t_{wait}] \quad (3.\ 39)$$

Going back to the range measurement issues (Eq. (3. 36)), the range resolution Δd involved in TOF measurements described so far presents a linear relation to the ENC, as it can be concluded from Eq. (3. 40), where $S(\lambda)$ stands for wavelength dependent optical sensitivity (in A/W), A_{PD} is the detector photoactive area and E_R the impinging irradiance (in W/cm^2).

$$\Delta d = \frac{q \cdot ENC \cdot c}{2 \cdot S(\lambda) \cdot A_{PD} \cdot E_R} \quad (3.\ 40)$$

To improve the range resolution of the sensor, the first attempt made was to decrease the ENC by separating the highly capacitive photoactive areas (i.e. areas generating and collecting the photogenerated charge) of the BPD, n^+ PD, and *n*-type PG photodetectors from the readout nodes, designing active pixel configurations that will be described in the next couple of sections in this text.

3.3 Possibilities of Charge-Coupling the Separated Photoactive and Readout Node Regions in Different Active Pixel Configurations Fabricated in the 0.5μm CMOS Process

As it can be observed from dark current (*I-V*) and capacitance (*C-V*) measurements performed on all photodetector structures to be fabricated in the CMOS process under investigation and presented in Chapter 2 of this work, although the BPD presents the lowest dark current of all reverse biased *p-n* junction based photodetectors (mainly due to the screening of the *Shockley-Read-Hall* (SRH) generation/recombination centres at the wafer surface), the *n*-well of this structure is not completely depleted under 3.3V. It thus consists of two parallel-connected capacitors: the one formed by the p^+-*n*-well junction and the second one by the *n*-well-*p*-substrate junction, delivering much higher total output capacitance. On the other hand, the *n*-type PG yields the lowest amount of dark current of all photodetectors tested, mainly due to reduced SCR generated under its gate and longer minority carriers lifetimes within the *p*-substrate if compared to those located in the *n*-well, which define the *p*-type PG performance. Due to all these characteristics, the BPD and the *n*-type PG were thus proposed as ideal candidates for active pixel configurations to be fabricated in the 0.5μm standard CMOS process under investigation.

As already explained, an attempt was made to decrease the ENC defined by Eq. (3. 35) by separating the highly capacitive photoactive regions, consisting of BPD, n^+ PD, or *n*-type PG photodetectors, from an additionally fabricated low-capacitance readout node, as described below for different active pixel configurations. The complete transfer of the charge collected in the photoactive region into the readout node, as standard used in PG and BPD APS [Jan03], would here be carried out by employing a MOS-C based *transfer gate* TG (e.g., 0.7μm long). The readout node would then be an n^+ *floating diffusion* (FD) - source terminal of the reset (RST) transistor depicted in Figure 3. 1(b). This yields

a simplified electric diagram of such an APS that can now be observed in Figure 3. 4. Here, it must be stressed that the idea works only if complete charge transfer (i.e., charge transfer efficiency (CTE) of 100%) from the photodetector into the readout region is accomplished. If instead of complete charge transfer, charge "sharing" between C_{PD} and C_{FD} (i.e., incomplete charge transfer) takes place, then SNR and the spectral responsivity ($\Re$) of the pixel decrease instead of increasing their values.

Considering the case where the charge transfer efficiency of 100% is accomplished, the FD, besides exhibiting much smaller capacitance than C_{PD}, would enable the use of the so called "true" CDS (unlike conventional CDS operation, the "true" CDS also cancels effects of the reset noise), and help avoiding the image lag problem present in most pixel configurations similar to the one shown in Figure 3. 1(b). Smaller C_{FD} (if compared to C_{PD}) increases, as well, the charge to voltage conversion factor.

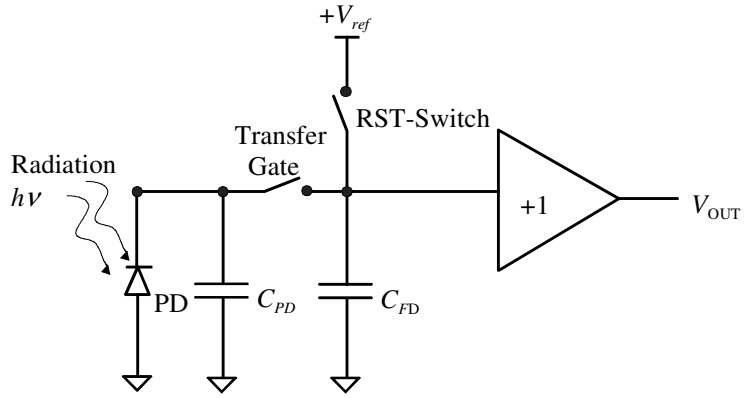


Figure 3. 4 – A simplified electric diagram of a PD based active pixel using a MOS-C based transfer gate and an n^+ floating diffusion (FD) based readout node.

Next, different active pixel configurations with charge-coupled separated photodetector and readout regions proposed will be studied in detail and the possibilities of their fabrication in the CMOS process of interest will be examined.

3.3.1 Reverse-Biased *p-n* Junction Based Active Pixels with Separated Charge-Coupled Photoactive and Readout Regions

For light sensing operation of any PD based active pixel with separated charge-coupled photoactive and readout regions, the PD structure is initially reverse biased at a certain V_{PD}. During the integration phase, photogenerated majority carriers are stored at the wafer surface of the PD, decreasing its potential below V_{PD}. For readout, the n^+ floating diffusion is first reset to V_{DD} (Figure 3. 4). Next, the transfer gate (TG) switch is closed and the complete charge collected at the PD is transferred to FD [Lul00].

The secret hidden behind a 100% charge transfer efficiency between a photodetector and a separated FD is achieving a proper electrostatic potential profile created beneath the PD, the TG, and the FD in an active pixel configuration, when all these three devices are biased to perform the readout operation. In other words, when ready for readout (i.e., the charge transfer from

the photoactive region to the FD), the electrostatic potential maximum formed within the *n*-well PD has to be weaker than the electrostatic potential maximum formed beneath the TG, which on the other hand should exhibit a mid-value between the PD maximum electrostatic potential value and the maximum electrostatic potential formed at the FD. This principle can be observed in Figure 3. 5(a) for the case of an *n*-well PD used as a photodetector.

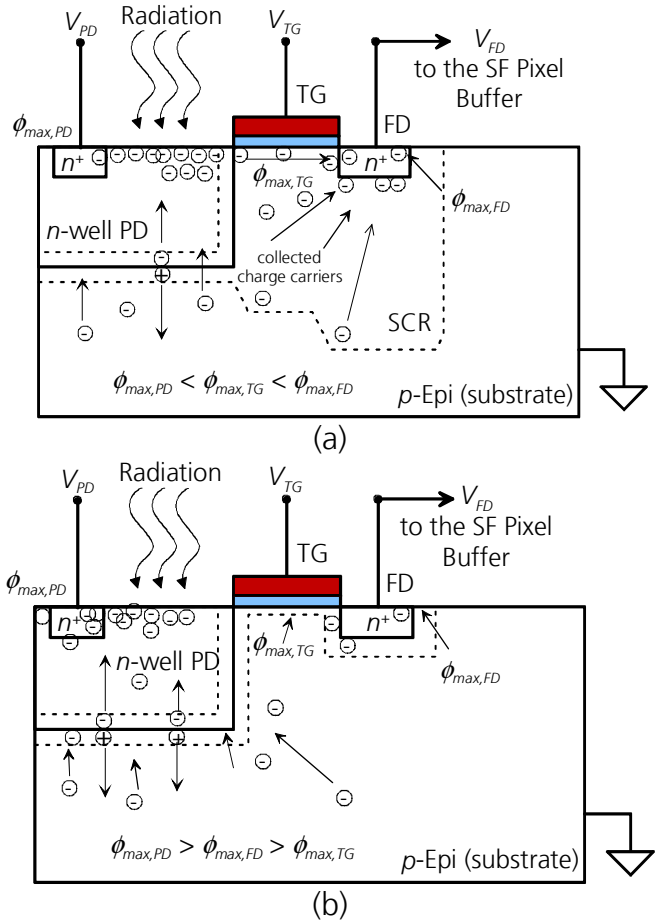


Figure 3. 5 – (a) Schematic representation of an *n*-well PD based active pixel configuration using TG enabled charge-coupled separated *n*-well PD and FD regions during readout; (b) the same pixel configuration during charge collection.

If this is the case, and the electrostatic potential maximum (ϕ_{max}) of the entire photodetection system is located at the FD, then all the charge carriers collected at the *n*-well PD will be immediately drifted via the TG toward the FD, modifying C_{FD} and consequently V_{FD}, which is then used as the photodetector system output signal. Moreover, as long as the "stair-wise" electrostatic potential profile depicted in Figure 3. 5(a) can be formed in the readout phase, any photodetector can be used to create and integrate the photocurrent in such an active pixel configuration, with all the advantages of this approach already explained above. Of course, at the same time, proper biasing conditions should be met to create sufficiently high potential barriers between the PD and the FG during the charge collection phase, so that a proper charge collection can be carried out at the PD during T_{int} without any charge losses, similarly to the case sketched in Figure 3. 5(b).

Nevertheless, in the example depicted in Figure 3. 5 the presence of an n^+ diffusion within the *n*-well PD, used to contact the *n*-well PD, introduces an extra electrostatic potential maximum to the system due to the sum of the concentration gradient which appears within the *n*-well and the bias voltage applied to this n^+ diffusion, which prevents a significant part of the collected carriers to be drifted toward the FD in the charge transfer process (Figure 3. 5(a)), i.e. it causes image lag. On the other hand, in this configuration, the reset of the *n*-well PD and that of the FD must be performed separately, which introduces a large amount of k_BT/C_{PD} noise to the output signal of the photodetector caused mainly by the *n*-well PD proportionally "high" capacitance on the one hand, and the proportionally smaller amount of k_BT/C_{FD} noise caused by resetting the FD on the other. The sum of both effects causes the k_BT/C noise at the photodetector output of this solution (which should reduce the noise) to be even higher than the noise caused by resetting a normal *n*-well PD. Finally, in this configuration, the photo- and thermally- generated carriers are being stored at the silicon surface (ϕ_{max}), full of SRH generation/recombination centres, which makes the output signal to be even more noisy (and the photodetector to deliver a considerable amount of dark current and its accompanying dark noise).

One of the favourite solutions to many of the problems just described is for most scientists [Jan03] the use of a *pinned* photodiode (PPD) as a photodetection device in this kind of active pixel configurations. The principle of operation of a PPD is as follows. A shallow *n*-well (normally ~1μm deep) is here to be properly chosen which creates, if sandwiched between a grounded p^+ diffusion on the wafer surface and a grounded *p*-type substrate and due to the concentration gradient and the intrinsic properties of a *p*-*n* junction such as this, a certain electrostatic potential maximum, also called the *pinned voltage* V_{pinned}, which *pins* the potential, meaning that the entire *n*-well becomes depleted and no more majority carriers can be extracted from the device [Fox98]. The potential than remains fixed inside the device and cannot be increased any further. The reset process of such a device can be then preformed through the FD, extracting all the remaining minority carriers from both, the "buried" shallow *n*-well and the FD without any need for an additional *n*-well contact. On the other hand, the electrostatic potential maximum within this *pinned* shallow *n*-well is being pushed away from the silicon surface in a manner already described for the BPD. The increased concentration of the p^+ diffusion provides for higher recombination rates of the thermally generated minority carriers (reduces the amount of dark current), which together with the fact that here the collected carriers are being held away from the same silicon surface, means that the amount of noise at the signal output is importantly reduced if compared to *n*-well PD solutions similar to the one depicted in Figure 3. 1.

Nevertheless, regarding the image lag problems in potential PPD active pixel configuration, Ramaswami *et al.* [Ram01] group explains that one reason for possible residual charge in a *pinned* photodiode is the very high resistance of a fully depleted *n*-region. For them, the pinned photodiode can be modelled as a lumped element non-linear RC delay network, with the resistance of each element being a heavy function of the voltage, as it can be observed in Figure 3.

6. In large photodiodes, the series resistance of the stages closer to the output can increase the time required to deplete the stages farther away from the output. If the resulting delay is longer than the width of the pulse applied to the transfer gate TG, then charge is left behind in the photodiode [Ram01]. The same applies to the reset pulse, when both TG and RST are turned on.

Even for relatively small pixels, charge can be left behind if the voltage required to deplete the first RC stage is less than that required for the subsequent sections. In such a case the voltage dependent resistance from the first RC stage rises more rapidly than the voltage dependent resistance from the next one, delaying the extraction of charge from this subsequent second RC stage. If the difference in depletion voltages is large enough, then a certain amount of charge is always left behind in this second subsequent RC stage, constituting a "fat zero" [Ram01]. Nevertheless, some charge does get extracted from the "fat zero" through thermionic emission over the energy barrier created between the PPD and TG. The rate of emission, therefore, decays exponentially with time; and the charge extracted is thus greater for a larger "fat zero" [Ram01].

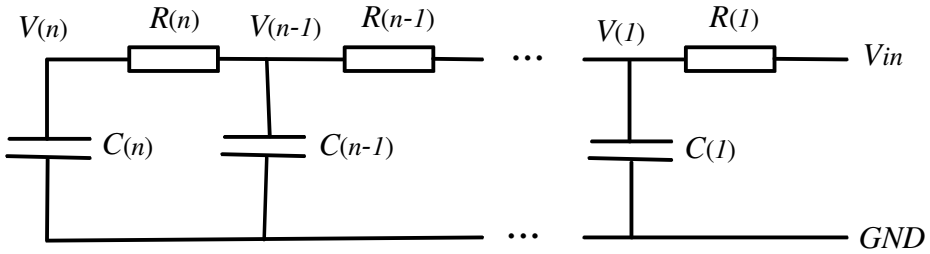


Figure 3. 6 - Equivalent representation of a *pinned* photodiode (PPD) [Ram01].

Unfortunately, as analysed in Chapter 2 of this text, the BPD photodetector structure fabricated in the standard CMOS process under investigation cannot be used as *pinned* photodiode due to the fact that the *n*-well does not get completely depleted (not even under V_{DD}=3.3V reverse biasing, neglecting all the drawbacks this solution implies). Nevertheless, the reduced dark current delivered by this structure still makes it an attractive solution for some applications, if no charge coupling is to be implemented. Also, completely depleting the *n*-well in this photodetector could be possible if a higher biasing voltage is to be used, e.g. V_{bias}≈5.4V. In that special case, an improved quantum efficiency in the blue region of the spectrum could be expected [Jan03], as well as a reduced capacitance if compared to the BPD.

Taking all this in mind, a two dimensional (2-D) (*ISE-Synopsys*) TCAD electrostatic potential simulation was performed for the BPD based active pixel configuration to be fabricated in the 0.5μm standard CMOS process under investigation, for its readout phase -after the photogenerated charge was collected in the photodetector during a certain integration time T_{int}-. Of course, for simulation purposes, the results obtained are also valid for the *n*-well PD, as both photodetectors are based on the same *n*-well structure. The transfer gate length chosen was of 0.7μm, and the floating diffusion was 2μm wide. Moreover, in order to allow the *n*-well to laterally diffuse until it reaches the first

edge of the TG, it was drawn 0.3μm longer (in direction of the x axis in Figure 3. 7) than it should be, a design rule that should be followed also for layout generation. On the other hand, for the surface p^+ diffusion (Figure 2. 19) to stop at least 0.1μm [Ino99] before the TG edge (and the outer edge of the *n*-well), it had to be drawn 0.2μm shorter, also in the direction of the x axis in Figure 3. 7.

For the TCAD simulation performed, V_{PD}=0.6V was applied to the BPD (or the *n*-well PD), creating a vertical SCR of 0.26μm in the *p*-Epi substrate, which together with the 1.5μm barrier depth X_j (*p*-*n* junction depth) indicates that in order to transport the entire signal charge from the *n*-well (or BPD) to the floating diffusion, the electrostatic potential under the TG also at 1.76μm depth inside the *p*-Epi substrate should be higher than the one at the edge of the *n*-well SCR, the same depth at which the electrostatic potential under the FD should be higher than the one under the TG. The same electrostatic potential relation should be valid for the *p*-*n* junction depth (1.5μm) and, of course, the wafer surface. On the other hand, the transfer gate was biased with V_{TG}=3.3V, creating a SCR of 0.16μm on the very surface of the wafer. The floating diffusion was assumed, immediately after the reset operation through the RST NMOS transistor, to be biased with V_{DD}-V_{th} of the RST transistor (although for simulation purposes, V_{FD}=3.3V was considered). That causes the generation of a floating SCR initial depth of 0.22μm, which together with the n^+ diffusion depth of 0.3μm indicates the existence of an electrostatic potential only until the 0.52μm below the n^+ FD. The *p*-Epi substrate was considered to be grounded.

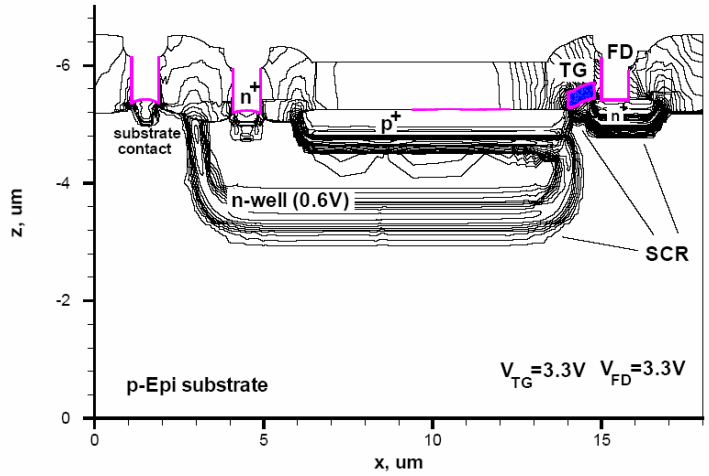


Figure 3. 7 – Result of the 2-D electrostatic potential simulation performed using TCAD software tools for the readout stage in a BPD based APS fabricated in the 0.5μm standard CMOS process under investigation, where only exist charge "sharing" between the PD and the FD [Dur07P].

As expected from the previous analysis, fabrication of active pixel sensors with charge-coupled BPD and FD structures, where in the readout phase the entire signal charge is transported via the TG from the BPD to the FD is impossible in the 0.5μm standard CMOS process under investigation. As it can be observed in Figure 3. 7, the complete charge transfer does not work for PD based pixels: only charge sharing is here obtained, where a huge part of the charge is left at the PD.

A second attempt was then made, this time for an active pixel configuration based on the n^+ PD. The principle of operation of this pixel structure is identical to the one described above, only that instead of a BPD, a PPD, or an *n*-well PD, the n^+ PD is used as the photodetector. Again, a 2-D electrostatic potential simulation of the active pixel is performed using TCAD software tools, the result of which can be observed in Figure 3. 8. Here, the n^+ PD was biased again at 0.6V, V_{TG}=3.3V, and V_{FD}=3.3V was considered for simulation purposes.

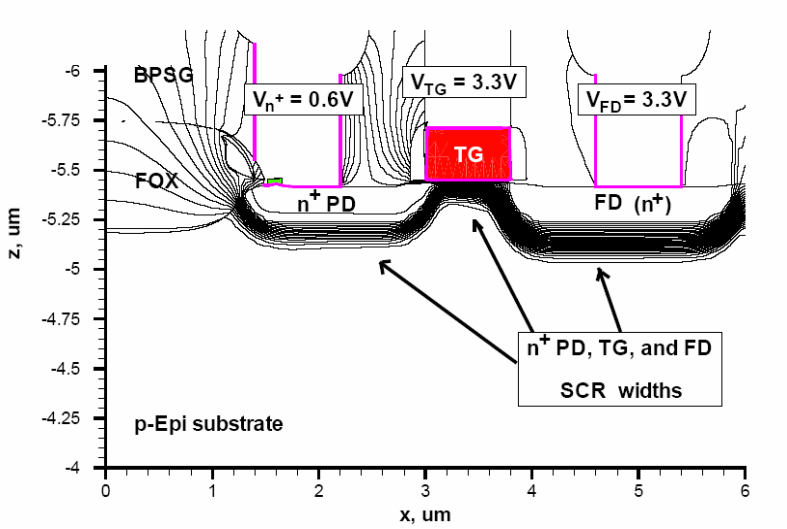


Figure 3. 8 – Result of the 2-D electrostatic potential simulation performed using TCAD software tools for the readout stage in an n^+ PD APS fabricated in the 0.5μm standard CMOS process under investigation, where the charge coupling is also not possible [Dur07P].

As in the previous case, the charge coupling between the n^+ PD and the FD does not work for the photogenerated charge readout. Instead, only charge sharing between the photoactive region (n^+ PD) an the readout node (FD) is obtained, where still a huge amount of signal charge remains on the PD.

Next, APS structures based on reverse-biased *n*-type PG photodetector are studied in detail.

3.3.2 Reverse-Biased *n-type* PG Based Active Pixel Sensor

Photogate Active Pixel Sensors were developed by workers at the *Jet Propulsion Laboratory* (JPL), based on the same principle normally used for CCD. The basic structure of such a sensor is identical to the APS structures discussed so far, just considering an *n*-type PG instead of the PD, for the case of the electric diagram shown in Figure 3. 2.

As it was already explained in Chapter 2 of this work for the reverse-biased *n*-type PG photodetectors, during integration, the photogenerated charge is accumulated in the potential well generated under the photogate (i.e., its SCR). For readout, the complete charge is transferred via the transfer gate onto the floating diffusion after that had been reset. So, most of the photosensitive area does not contribute to the charge-to-voltage conversion capacitance.

The photogate is at first biased at a positive voltage V_{PG} higher than the threshold voltage V_{th} (e.g., V_{DD}=3.3V) thereby creating a potential well in the depleted *p*-Epi substrate. At this moment, the photo- and the unavoidable thermally- generated charge is stored under the PG gate electrode. The transfer gate is also positively biased at V_{TG}, a lower voltage than V_{PG}, although higher than V_{th}, to provide for some lateral anti-blooming control. It acts as a surface channel CCD in the charge integration task. The FD acts as the charge-voltage conversion node, and the signal is finally readout using the conventional *source-follower* based buffer circuit, in the rolling readout mode.

A typical operating sequence for the PG is shown in Figure 3. 9. At the first moment, PG is biased into deep-depletion non-equilibrium mode, while TG and RST are biased into depletion, but at a voltage V_{TG}, as it can be observed in Figure 3. 9(a). When exposed to irradiation, this represents the signal charge integration step. Here, the deep depletion case refers to rapid ramping of the DC bias gate voltage, where the minority carrier charge does not have enough time to develop, although $V_{PG}>V_{th}$. To satisfy the whole charge neutrality, the depletion region width expands beyond W_{inv} (SCR depth under V_{th}), because repulsion of the majority carriers only takes a time scale of the dielectric relaxation time constant. If the bias applied is kept constant or the ramping rate is slowing down, the charge distribution reverts back to the equilibrium situation with the equilibrium inversion charge value and W_{SCR} will snap back to W_{inv}.

At the reset stage, or the first step toward the signal readout, the RST transistor is biased at V_{DD}, in order to reset the FD to a voltage $V_{FD}=V_{DD}-V_{th}$, immediately before the signal readout. This can be observed in Figure 3. 9(b).

Finally, the readout step is being performed, where the voltage applied to the PG is lowered to ground potential in order to collapse the potential well under the gate electrode. The charge is then transferred to the potential well created under TG at V_{TG}, and finally added to any charge remaining after the reset operation in the FD. This can be observed in Figure 3. 9(c). The charge is then finally being read out [Hor00].

One of the principal issues in the operation of a photogate APS is the *charge transfer efficiency* (CTE) between the PG and the TG, where some amount of photogenerated charge can get lost. Thus, a 2-D electrostatic potential simulation of the PG APS structure to be fabricated in the 0.5μm standard CMOS process under investigation was performed, using TCAD software tools. Lacking an overlapping polysilicon layer, the PG active pixel was designed placing the PG and the TG at a minimum distance of 0.5μm from each other, as it can be observed in Figure 3. 10. Once again, a 0.7μm long TG was considered, with V_{TG}=3.3V for the readout phase, as well as a 2μm wide n^+ PD based FD which immediately after reset was considered to be reverse-biased at RST NMOS transistor's $V_{DD}-V_{th}$ (although for simulation purposes the value considered was equal to 3.3V).

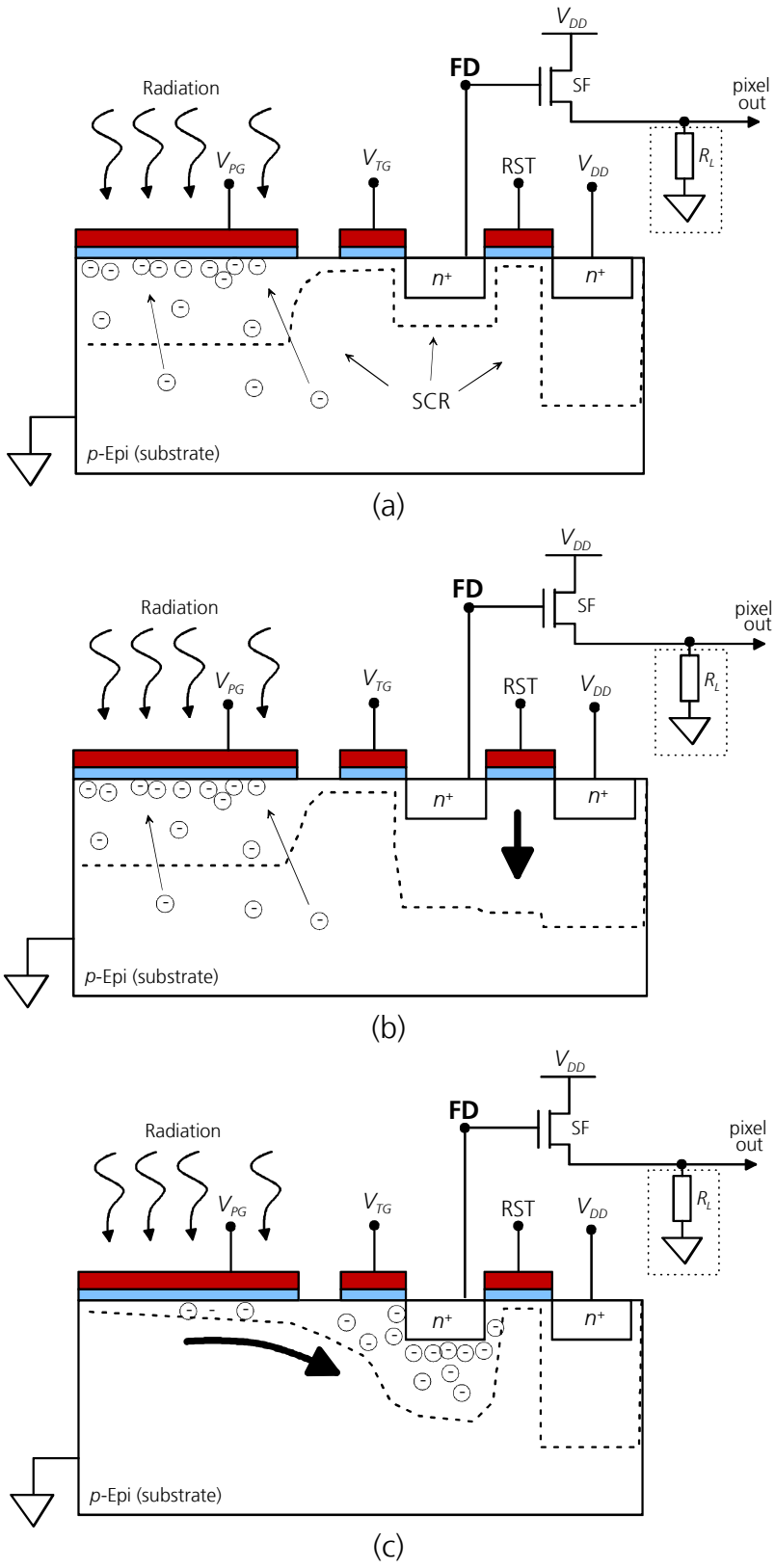


Figure 3. 9 – (a) Schematic representation of the PG APS structure under irradiation, during the charge integration process; (b) schematic representation of the PG APS during the FD reset phase; and (c) schematic representation of the PG APS during signal readout.

It can be seen in Figure 3. 10, that the lateral SCR of the TG, reverse-biased at V_{TG}=3.3V, is much narrower than the 0.5μm distance between the PG and the TG. This leads to the disruption of the electrical field in the charge transfer path between the PG and the TG. In other words, a potential barrier appears in the charge transfer path that dramatically reduces the CTE, as it can be observed in the electrostatic potential plot obtained at the very wafer surface, i.e. just below the PG silicon-oxide interface, shown in the lower left corner in Figure 3. 10. An extra n^+ diffusion between the PG and TG structures [Jan03] is also not a solution, as it can be inferred from Figure 3. 8. This means that the use of a charge-coupled separated readout node in PG active pixel configuration is also not possible in the standard CMOS process employed here.

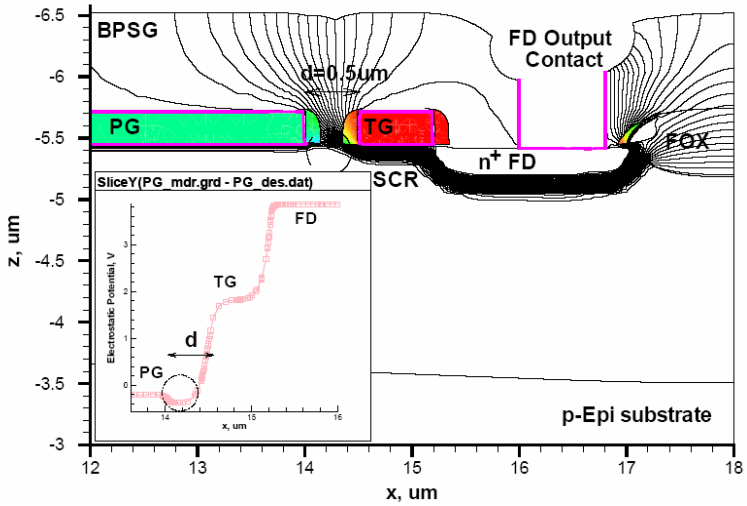


Figure 3. 10 - 2-D electrostatic potential simulation performed using TCAD software tools for the readout stage in the *n*-type PG based APS where the potential barrier can be observed between the PG and TG placed at a minimum distance of 0.5μm from each other; here V_{PG}=0V, V_{TG}=3.3V, and V_{FD}=3.3V [Dur07P].

3.3.2.1 ITO Based PG Active Pixel Proposal

Dealing with the discussed problem of reduced CTE in PG active pixel structures, that makes this kind of pixels inoperable in the 0.5μm CMOS process under investigation, and following the discussion developed in sub-chapter 2.6.1 of this text, a novel ITO based PG APS is here proposed. As it was already explained, the physical mask normally used for *Metal 3* is used in this proposal as the mask for the ITO layer, eliminating the metal 3 layer from the entire layout. The latter brings the possibility of using an overlapping ITO based PG, which improves the CTE of the ITO based PG APS and should make the pixel structure operable. A schematic diagram of the ITO based PG, the TG, the FD, and the RST transistor, operating in the way identical to the one described for normal PG APS, can be observed in Figure 3. 11(a). Figure 3. 11(b) shows the ITO-PG APS layout prepared using *Cadence*® software tools for the 0.5μm standard CMOS process under investigation.

The problems occurring during the fabrication of ITO-PG active pixel structures were already discussed in detail in Chapter 2 of this text. Nevertheless, the problem detected regarding the reduced selectivity of the HCl wet etching

technique between the ITO and oxide structures, which was partially solved leaving the last 30nm-50nm of the ITO layer on the oxide, which were then removed during the CARO-cleaning process together with the remaining photoresist, can be better understood if observing Figure 3. 12 [ITOFhG]. Namely, after the photolithography step, small quantities of photoresist were found on top of the ITO layers belonging to different test structures. These remaining photoresist was finally eliminated using a combination of acetone in the spin-coater and photoresist plasma incineration. All of this left, nevertheless, thinner ITO layers (around 280nm thick) with rather high ITO surface roughness.

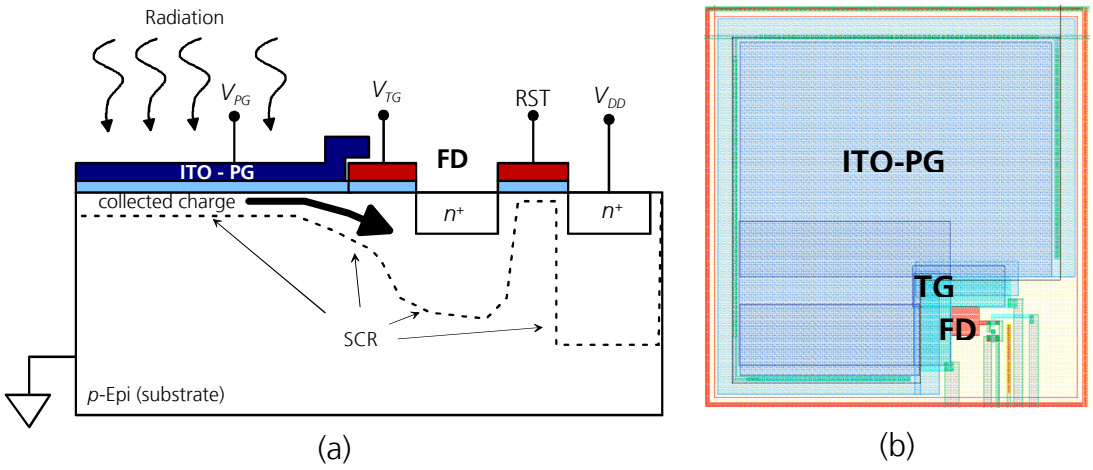


Figure 3. 11 – (a) Schematic diagram of the ITO-PG active pixel proposal, where overlapping ITO-PG and polysilicon TG can be observed in the readout phase; (b) layout prepared for the ITO-PG active pixel using *Cadence*® software tools.

In Figure 3. 12(a) [ITOFhg], a detail of the fabricated ITO-PG APS structure, the layout of which is shown in Figure 3. 11(b), can be observed, where the photoresist rests were eliminated applying acetone. In Figure 3. 12(b) [ITOFhG], the ITO surface belonging to the same test structures can be observed where the higher ITO roughness can be seen, provoked by the photolithography step just described, taking place after the *source/drain* implantation.

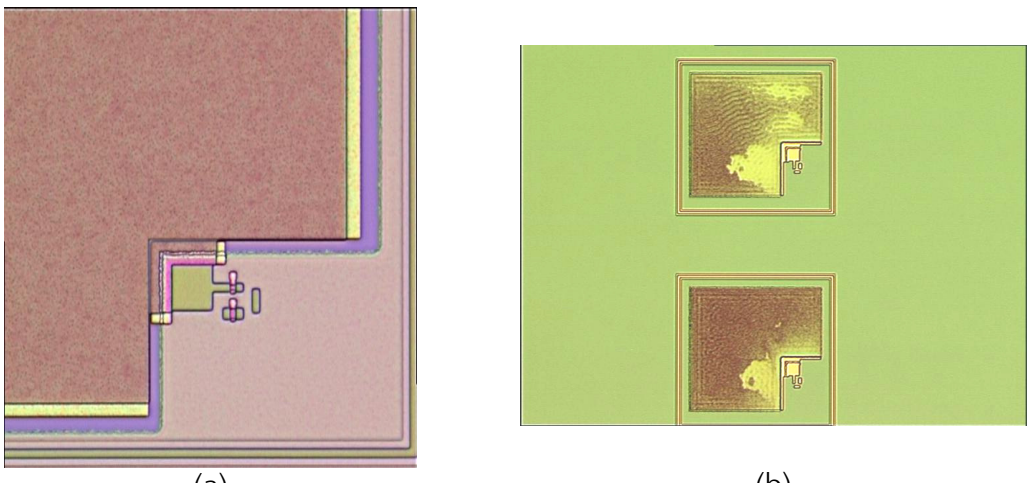


Figure 3. 12 – (a) A detail of the fabricated ITO-PG APS structure, where the photoresist rests were successfully eliminated applying acetone [ITOFhG]; (b) the same test structures where the higher ITO roughness can be seen [ITOFhG].

Due to issues already discussed in Chapter 2, the processing of the chips stopped before the first metal layer was deposited, so the ITO-PG APS were never properly tested.

The limitations of the 0.5μm standard CMOS process under investigation enlisted so far, reduced the amount of possibilities to be applied in pixel and entire CMOS imager designs. Obviously, it is not possible to employ the idea of charge-coupling the separated photoactive and readout nodes in this process. This severely restricts the applications of this standard CMOS process for imaging purposes. Nevertheless, the still available imaging principles were applied in different pixel configurations based on both, the reverse-biased *p-n* junction based photodetectors, as well as on reverse-biased MOS-C based ones, and will be discussed in detail in the next section, where they are to be used in high-speed NIR three dimensional TOF imaging applications.

3.4 n-well PD Based Active Pixels for 3-D TOF Imaging

At first, three pixel configurations based on reverse biased *n*-well PD are investigated. Although the laser pulses are fast (their width is in nanosecond range) they exhibit a rather low repetition rate. While the acquisition of the reflected pulse must be also fast, the readout can be in comparison slower (in microsecond range). Hence, the readout requires a lower bandwidth and this reduces the noise bandwidth. For this purpose, in all three cases, the *n*-well PD requires an additional pixel storage capacitor C_s where a voltage proportional to the charge photogenerated during the integration phase can be stored with minimum time dependent losses (through dark or parasitic currents), enabling synchronous photocharge integration and rolling readout of the entire pixel array.

The voltage-independent capacitor, consisting of a special *CAPA* n^+ diffusion and a MOS-C fabricated on top of it, available in the 0.5μm standard CMOS process under investigation, was chosen for this task (see Figure 3. 13).

During the initial reset phase, the *n*-well PD and C_s are charged to the reference voltage $U_{ref\,PD}$ via the reset (RST) PMOS transistor switch (used here to achieve "hard" reset operation) and the shutter transistor M1 (see Figures 3. 13, 3. 16, and 3. 18), before each integration period. After the RST switch is turned OFF, the discharge of the PD and the C_s begins due to photo- and thermally generated currents flowing in the *n*-well PD. Deactivating the shutter switch M1 stops the current flow from the PD to the C_s and thus enables the integration time control. Through the activation of the row-select transmission-gate switch, consisting of an NMOS and PMOS transistor pair, the voltage stored at the C_s is readout to the CDS and multiplexed analog memory circuit (see Figure 3. 3).

3.4.1 TOF Pixel Configuration with an *n*-well PD and Two Source-Follower Based Buffers

The first solution, depicted in Figure 3. 13, includes two *source-follower* based buffer stages. Due to *n*-well PD low output current and high pixel response speed requirements, the idea is to electrically decouple the *n*-well PD

and the C_s using the SF1 stage, as desired above. The CDS stage has much more relaxed bandwidth requirements since the duty cycle of the pulses is usually very low (~2μs). This enables the addition of C_{Hx}, a pixel output noise bandwidth limiting capacitor, used to decrease the *kT/C* noise of the SF2 output buffer. With a slew-rate of 1.6×10^7V/s, i.e. the maximum rate at which C_s can be charged by the SF1 buffer defined by Eq. (3. 41) [Bak05], obtained for an example irradiance of 1420W/m^2 (background illumination (solar constant at the Earth surface) added to the reflected laser pulse (λ=910nm)), and a 3dB-frequency of 80MHz, the SF1 stage enables an acceptable response speed of the pixel.

$$slew\_rate = \frac{dV_{SF1\_drain}}{dt} = \frac{I_{SF1}}{C_s} \tag{3. 41}$$

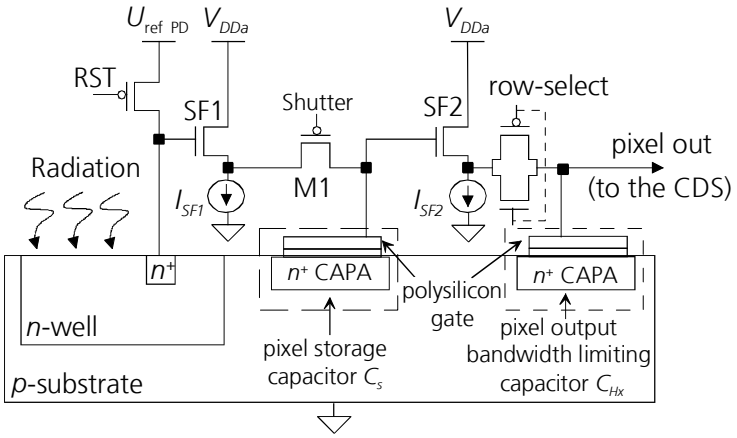


Figure 3. 13 - TOF pixel configuration with an *n*-well PD and two *source-follower* based buffers [Elk04].

Noise bandwidth is, by the way, not the same as the commonly used 3dB bandwidth. There is one definition of bandwidth for signals and another for noise. The bandwidth of an amplifier or a tuned circuit is classically defined as the frequency span between half-power points, the points on the frequency axis where the signal transmission has been reduced by 3dB from the central or midrange reference value [Mot93]. A 3dB reduction represents a loss of 50% in the power level and corresponds to a voltage level equal to 0.707 of the voltage at the centre frequency reference [Mot93]. Considering a parallel RC connection in a circuit, its 3dB frequency can be defined as shown in Eq. (3. 42) [Elk05].

$$f_{3dB} = \frac{1}{2\pi RC} \tag{3. 42}$$

The noise bandwidth, Δf, is on the other hand, the cut-off frequency of a "brick-wall" filter exhibiting the same noise power as the original filter. Thus, this corresponds to the frequency span of a rectangularly shaped power gain curve equal in area of the actual power gain versus frequency curve. Noise bandwidth is the area under the power curve, the integral of power gain versus frequency, divided by the peak amplitude of the curve [Mot93]. Following Eq. (3. 42), it can be defined as Eq. (3. 43) [Elk05].

$$\Delta f = \frac{\pi}{2} \cdot f_{3dB} = \frac{1}{4RC} \tag{3. 43}$$

The peak power consumption for the pixel structure depicted in Figure 3. 13 is of 660μW, where each SF consumes 100μA. If multiplied by the number of pixels in an imager, this peak power consumption could reach beyond the acceptable. The spectral responsivity obtained in this case for T_{int}=30ns integration time and λ=910nm of impinging reflected laser pulse radiation (once the background illumination has been eliminated) is $\Re$=25.83V·cm^2/μJ. The *noise-equivalent power* (NEP) reaches in this pixel structure 303.12μW/cm^2.

The NEP is here defined, expressed by Eq. (3. 44), as the ratio between the pixel output noise voltage $\overline{v_{n\_out}^2}$, measured at the at the end of the readout chain (consisting of the pixel, the CDS circuit, and usually the imager output buffer), and the specific wavelength dependent *spectral responsivity* of the pixel ($\Re(\lambda)$) defined for a certain T_{int}. The spectral responsivity of a pixel is the figure of merit defined as the pixel output voltage V_{out} (in volts), measured at the end of the same readout chain mentioned, per unit of impinging irradiance E_R (normally, in watt per square centimetre) multiplied by T_{int} (in seconds). The spectral responsivity is normally expressed in V·cm^2/μJ units.

$$NEP = \frac{\sqrt{\overline{v_{n\_out}^2}}}{\Re \cdot T_{\text{int}}} \tag{3. 44}$$

Moreover, if Eqs. (1. 18) and (1. 19) are taken into consideration, the voltage produced at the *n*-well PD can be defined by Eq. (3. 45), if the RST transistor source-drain potential difference V_{SD}(RST) is neglected, as well as the sign reverse in the KLV analysis of the circuit shown in Figure 3. 13.

$$V_{PD} = \frac{I_{ph} \cdot T_{\text{int}}}{C_{PD}} = \frac{S(\lambda) \cdot A_{PD} \cdot E_R \cdot T_{\text{int}}}{C_{PD}} \tag{3. 45}$$

On the other hand, the V_{out} (pixel output voltage measured at the end of the readout chain) can be defined in terms of $\Re$ as shown by Eq. (3. 46), where $\Re$ can be calculated in terms of the wavelength dependent optical sensitivity $S(\lambda)$ as defined by Eq. (3. 47).

$$V_{out} = \Re(\lambda) \cdot E_R \cdot T_{\text{int}} \tag{3. 46}$$

$$\Re(\lambda) = \frac{S(\lambda) \cdot A_{PD}}{C_{PD}} \cdot \left(\frac{C_{c1}}{C_{Fx}} \right) \tag{3. 47}$$

Solving Eq. (3. 44) for $\sqrt{\overline{v_{n\_out}^2}}$ and considering the spectral responsivity definition expressed by Eq. (3. 47), the NEP linear dependence on C_{PD} can be

stressed again for the case of the active pixel configuration shown in Figure 3. 13, as shown by Eq. (3. 48).

$$NEP = \frac{C_{PD}}{S(\lambda)\cdot A_{PD}} \cdot \left(\frac{C_{Fx}}{C_{c1}}\right) \cdot \sqrt{\overline{v_{n\_out}^2}} \cdot \frac{1}{T_{\text{int}}} \tag{3. 48}$$

There are two ways in which the imager containing the kind of pixels shown in Figure 3. 13 can be conceptualised, namely on one side merging the photoactive area and the pixel circuit structure, in which case the fill-factor (the ratio of the photoactive area to the entire pixel area) is 52.3% for a (130×300)μm^2 pixel size, or keeping the pixel circuitry on the periphery of the joint photoactive area of the entire imager, in which case there is no need to define the fill-factor.

Next, a detailed noise analysis will be performed of the pixel shown in Figure 3. 13. All the mean square noise voltages determined are referred to the output node of the pixel structure at the end of the readout chain. In this sense, each should consider the gain factor of both SF based buffer stages (A_{SF1}=A_{SF2}=0.85), as well as the charge-to-voltage conversion factor ratio between the C_s capacitor (Figure 3. 13) and the C_{c1} capacitor of the CDS circuit (Figure 3. 3).

In this sense, based on Eq. (3. 26), the k_BT/C part of the *n*-well PD reset noise is obtained following Eq. (3. 49), where the input capacitance of the first SF buffer is considered to be the sum of the *n*-well PD (C_{PD}) and the SF1 transistor gate (C_{GD_SF1}) capacitances. The reset constant ξ=1 is here taken, due to the "hard" reset operation enabled by the RST PMOS transistor.

$$\overline{v_{n\_C_{PD}}^2} = \xi \cdot \frac{k_B T}{\left(C_{PD} + C_{GD\_SF1}\right)} \cdot \left(\frac{C_{c1}}{C_{Fx}}\right)^2 \cdot A_{SF1}^2 \cdot A_{SF2}^2 \tag{3. 49}$$

Following the same idea, the partition noise, based on Eq. (3. 28), is obtained using Eq. (3. 50).

$$\overline{v_{n\_PD\_part}^2} = \alpha_{part} \cdot \frac{2\left(k_B T C_{G\_RST}\right)}{\pi^2\left(C_{PD} + C_{GD\_SF1}\right)^2} \cdot \left(\frac{C_{c1}}{C_{Fx}}\right)^2 \cdot A_{SF1}^2 \cdot A_{SF2}^2 \tag{3. 50}$$

The first *source-follower* based buffer, consisting of the SF1 NMOS transistor and another NMOS transistor M_{CM1} which forms part of the current mirror based active load, represented in Figure 3. 13 by the ideal current source I_{SF1}, is considered next. Both transistors introduce channel thermal noise to the pixel output voltage signal, which arises due to thermal noise fluctuations in the MOSFET channel. The spectral density of this channel thermal noise is expressed in the form shown in Eq. (3. 51) [Ren06], for the case of long channel devices (L>1.7μm). The mean square current noise for the same case is defined as Eq. (3.

52). Here, g_{d0} is the drain conductance at zero *drain-to-source* voltage, and γ_c is the long-channel bias-dependent noise parameter.

$$S_{I_d}(f) = 4k_B T \gamma_{lc} g_{d0} \tag{3. 51}$$

$$\overline{i_d^2} = \frac{2}{3} \cdot 4k_B T g_{d0} \Delta f \tag{3. 52}$$

According to this model [Ren06], the noise parameter approaches unity when the drain-to-source voltage V_{DS} approaches zero and decreases to 2/3 as the device enters the saturation regime and remains at that value when V_{DS} exceeds the saturation value. Here, the noise manifested at the device terminals must correspond to noise generated by a resistance of value $1/g_{d0}$.

Nevertheless, the saturation value of γ_c=2/3 is valid for long channel MOSFETs built on lightly doped substrates. For higher substrate dopings, and for shorter channel lengths, the noise increases. Actually, for this new conditions, the parameter γ, which starts at unity at V_{DS}=0V, increases instead of decreasing (as predicted in long-channel MOSFET theory) steadily with increasing V_{DS} [Ren06]. There has been a great argument about the real causes of this excess noise measured in short-channel MOSFET devices fabricated on highly doped substrates. Nevertheless, experimentally obtained, the values of this *excess noise factor* γ, reported in literature for the 0.5μm channel lengths, oscillate between 1.5 and 3 for the case of strong inversion [Ren06].

For the process under investigation, the value of γ considered for the transistors SF1 and M_{CM1} depends on their operation points and is assumed that γ=1.1 for the weak inversion, γ=1.25 for the moderate inversion, and γ=2 for strong inversion. *Cadence*® software based simulation results showed that for the case of interest, both transistors remain in strong inversion during readout.

Since its first practical demonstration in 1960 [Ren06], the *flicker* noise has been the most widely studied and debated phenomena in the history of noise. The source of the 1/*f* fluctuations in MOSFETs was believed to be due to carrier trapping and detrapping at the oxide-semiconductor interface. Therefore, 1/*f* noise was believed to be a surface effect, until the concept of *correlated mobility fluctuations* due to coulombic scattering of inversion layer carriers by the fluctuating trapped charge was incorporated. Unification of compact 1/*f* noise models for *n*- and *p*- channel devices has been attempted, introducing correlated mobility fluctuations, as shown in Eq. (3. 53) [Ren06], where K is a constant dependent on the device type and processing, g_m is the device transconductances, and C_{OX} is the gate capacitance per unit area.

$$\overline{i_{n\_1/f}^2} = \frac{K}{f} \cdot \frac{g_m^2}{WLC_{OX}^2} \Delta f \tag{3. 53}$$

Considering the noise equivalent small-signal circuit diagram for the case of the first *source-follower* buffer, depicted in Figure 3. 14, the equation based on *Kirchhoff's current law* (KCL) considering the currents flowing between the SF1 and M_{CM1} transistors, as well as C_s, expressed by Eq. (3. 54) [Elk05] can be deduced, where $v_{gs\_SF1}=v_{G\_SF1\_1}-v_{out}$ and $v_{gs\_MCM1}=v_{G\_MCM1\_1}$. Considering these definitions and Eq. (3. 54), finally the expression for v_{out} can be deduced as Eq. (3 55) [Elk05].

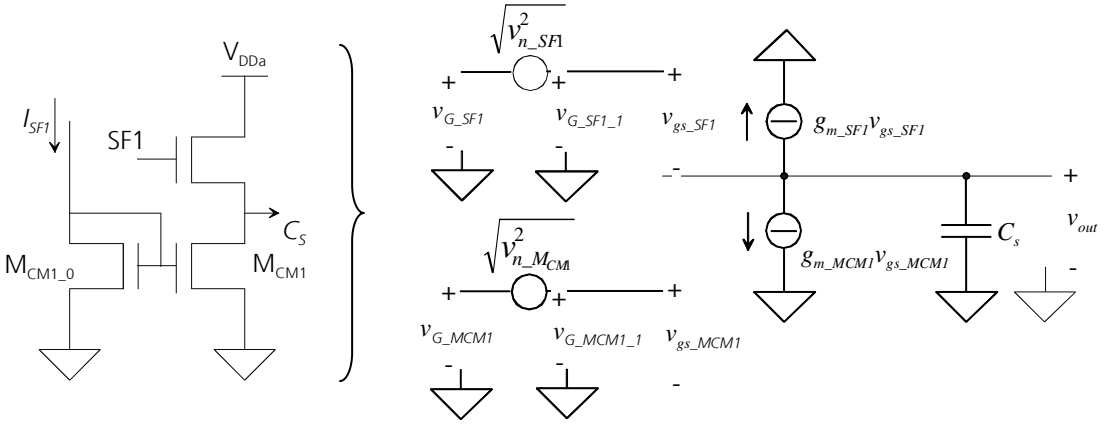


Figure 3. 14 – Noise equivalent small-signal circuit diagram (right) for the *source-follower* based SF1 buffer (left) (see Figure 3. 13).

$$g_{m\_SF1}v_{GS\_SF1} = -g_{m\_M_{CM1}}v_{GS\_M_{CM1}} + sC_s v_{out} \tag{3. 54}$$

$$v_{out} = \frac{1}{1+s\dfrac{C_s}{g_{m\_SF1}}}\left(v_{G\_SF1\_1} + \frac{g_{m\_MCM1}}{g_{m\_SF1}}v_{G\_MCM1\_1}\right) \tag{3. 55}$$

The first term in Eq. (3. 55) defines low-pass condition of the *source-follower* buffer, where the term g_{m_SF1}/C_s defines the bandwidth of the entire circuit response, with a 3dB frequency defined as Eq. (3. 56) [Elk05].

$$f_{3dB} = \frac{g_{m\_SF1}}{2\pi C_s} \tag{3. 56}$$

On the other hand, and following Eq. (3. 56) the noise bandwidth is defined in this case as Eq. (3. 57).

$$\Delta f = \frac{\pi}{2}\cdot f_{3dB} = \frac{g_{m\_SF1}}{4C_s} \tag{3. 57}$$

From Eq. (3. 55), it follows that the mean square noise voltage $\overline{v^2_{n\_M_{CM1}}}$ (Figure 3. 14), is sensed on the output with an amplification factor of g_{m_MCM1}/g_{m_SF1}. Considering this result, the final mean square noise

contribution of the SF1 stage is defined by Eq. (3. 58), while neglecting the noise of I_{SF1} and M_{CM1_0}.

$$v_{n\_SF1}^2 = \frac{k_B T}{C_s} \cdot \left(\gamma_{SF1} + \gamma_{M_{CM1}} \left(\frac{g_{m\_MCM1}}{g_{m\_SF1}} \right) \right) \cdot \left(\frac{C_{cl}}{C_s} \right)^2 \cdot A_{SF1}^2 \cdot A_{SF2}^2 \tag{3. 58}$$

Considering the shutter transistor M1, it also introduces k_BT/C noise to the pixel output signal, which can be defined as shown in Eq. (3. 59), where amplification factor of the SF1 buffer is not considered any more.

$$\overline{v_{n\_shutter}^2} = \frac{k_B T}{C_s} \cdot \left(\frac{C_{c1}}{C_s} \right)^2 \cdot A_{SF2}^2 \tag{3. 59}$$

For the case of the second buffer stage, SF2, consisting of the NMOS transistor SF2 and another NMOS transistor M_{CM2} which forms part of the current mirror based active load, represented in Figure 3. 13 by the ideal current source I_{SF2}, its capacitive load considered consists of C_{Hx} (Figure 3. 13) and C_{c1} (Figure 3. 3) capacitors. Following an analogue analysis to the one performed for the case of the SF1 stage, it can be concluded that its mean-square noise voltage can be defined as shown in Eq. (3. 60). In this case, according to circuit simulation results, the SF2 transistor is operating in moderate inversion, whilst the M_{CM2} transistor operates in strong inversion.

$$\overline{v_{n\_SF2}^2} = \frac{k_B T}{C_{Hx} + C_{c1}} \cdot \left(\gamma_{SF2} + \gamma_{M_{CM2}} \left(\frac{g_{m\_MCM2}}{g_{m\_SF2}} \right) \right) \cdot \left(\frac{C_{c1}}{C_{Fx}} \right)^2 \cdot A_{SF2}^2 \tag{3. 60}$$

Finally, the case of the CDS circuit noise contribution is considered. Figure 3. 15 shows a small-signal noise equivalent circuit of the CDS stage shown in Figure 3. 3 and on the left side of Figure 3. 15. From the small-signal noise equivalent circuit, and following the KCL, for the output node the equation shown in Eq. (3. 61) can be formulated.

$$g_{m\_OTA} v_d = sC_{out} \cdot v_{out} + s\left(\frac{C_{c1} C_{Fx}}{C_{c1} + C_{Fx}} \right) \left(v_{out} - v_{pixel\_out} \right) \tag{3. 61}$$

Solving the net for v_d, following the *Kirchhoff's voltage law* (KVL), where $v_d = -\left(v_{out} - v_{CDS\_input}\right) \frac{1}{\left(1 + \frac{C_{c1}}{C_{Fx}}\right)} - v_{CDS\_input}$, the transfer function of the CDS circuit can be defined as shown in Eq. (3. 62) [Elk05].

$$\frac{v_{out}}{v_{CDS\_input}} = \frac{\dfrac{sC_{c1}}{g_{m\_OTA}} - \dfrac{C_{c1}}{C_{Fx}}}{1 + \dfrac{s}{g_{m\_OTA}}\left[\left(1 + \dfrac{C_{c1}}{C_{Fx}}\right)C_{out} + C_{c1}\right]} \tag{3. 62}$$

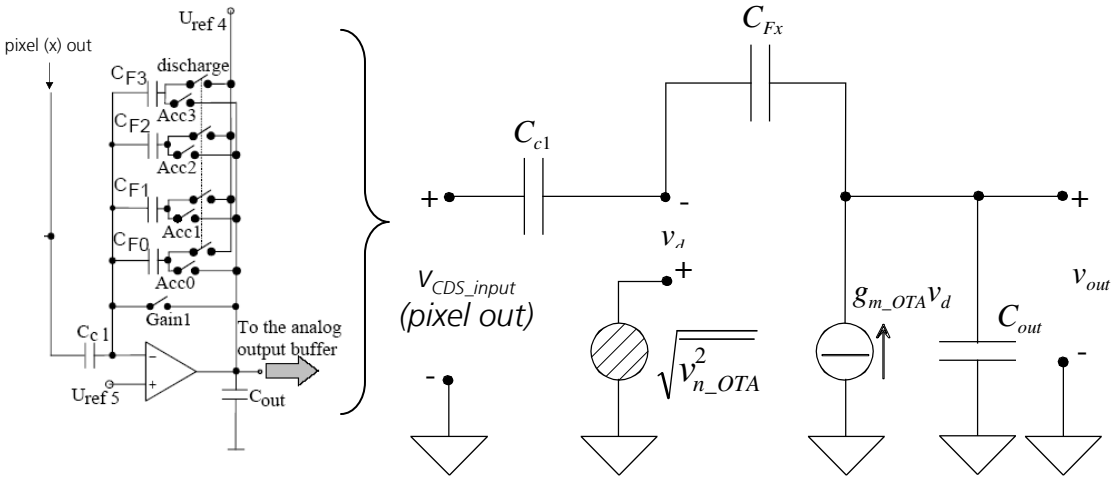


Figure 3. 15 – A simplified small-signal noise equivalent circuit of the CDS circuit (left), forming part of the pixel output readout chain [Elk05].

From Eq. (3. 62), the 3dB frequency of the CDS circuit is defined as Eq. (3. 63), and the noise bandwidth is consequently Eq. (3. 64).

$$f_{3dB} = \frac{g_{m\_OTA}}{2\pi}\left(\frac{1}{\left(1 + \dfrac{C_{c1}}{C_{Fx}}\right)C_{out} + C_{c1}}\right) \tag{3. 63}$$

$$\Delta f = \frac{g_{m\_OTA}}{4}\left(\frac{1}{\left(1 + \dfrac{C_{c1}}{C_{Fx}}\right)C_{out} + C_{c1}}\right) \tag{3. 64}$$

As in any operational amplifier (Op-Amp) circuit (left part in the Figure 3. 15), the main part of the k_BT/C noise is generated by the input transistor pair in the CDS stage. In this case, the noise contribution of the remaining (load) transistors forming part of the Op-Amp will be considered by introducing a noise constant K_a, as shown in Eq. (3. 65). Of course, and as it was already explained in this text, the CDS reduces to low frequency noise. Hence, the flicker or 1/*f* noise is thus neglected in this analysis, although one of the main problems in this kind of solutions remains the doubling of the remaining white noise components. The mean square noise voltage contribution of the CDS circuit itself is multiplied by 2 in Eq. (3. 65). The circuit simulation results showed that the input transistor pair is operating during the readout stage in moderate inversion (γ_{OTA}=1.25).

$$\overline{v_{n\_CDS}^2} = 2 \cdot \gamma_{OTA} \cdot \frac{K_a \cdot k_B T}{C_{c1} + C_{out}\left(1 + \frac{C_{c1}}{C_{Fx}}\right)} \cdot \left(1 + \frac{C_{c1}}{C_{Fx}}\right)^2 + \frac{k_B T}{C_{cl}}\left(\frac{C_{c1}}{C_{Fx}}\right)^2 + \frac{k_B T}{C_{Fx}} \qquad (3.\ 65)$$

On the other hand, during the readout stage, U_1 voltage is at first saved at the C_{Fx} capacitors by turning the correspondent A_{ccx} switch transistor ON (see Figure 3. 15 left). The A_{ccx} also has a noise contribution quantified as $\overline{v_{n\_Acc_x}^2} = k_B T / C_{Fx}$, incorporated to Eq. (3. 65) as the end term. Moreover, the U_1-U_2 voltage substraction, required to obtain U_{out_Tint1} or U_{out_Tint2}, is enabled through activation of the *row-select* transistor switch (Figure 3. 13) of the pixel of interest. The k_BT/C noise of this procedure is then incorporated to the signal charge contained at the C_{c1}, multiplied by the charge-to-voltage conversion ratio (C_{c1}/C_{Fx}), incorporated as the second term in Eq. (3. 65), which is now complete and shows the noise contribution of the CDS to each pixel output signal mean square noise voltage.

Based on the noise analysis performed so far for the pixel output signal measured at the CDS stage, Eq. (3. 66) is formulated to obtain the pixel joint output mean square noise voltage $\overline{v_{n\_out}^2}$. Of course, once again the doubling of white noise components when using correlated double sampling has to be taken into account, multiplying the mean square noise contributions of each stage by 2.

$$\overline{v_{n\_out}^2} = 2 \cdot \left(\overline{v_{n\_C_{PD}}^2} + \overline{v_{n\_PD\_part}^2} + \overline{v_{n\_shutter}^2} + \overline{v_{n\_SF1}^2} + \overline{v_{n\_SF2}^2} + \overline{v_{n\_CDS}^2}\right) \qquad (3.\ 66)$$

The pixel depicted in Figure 3. 13, fabricated in the 0.5μm standard CMOS process under investigation yields a pixel joint noise voltage $\sqrt{\overline{v_{n\_out}^2}}$ of 234.8μV [Elk04]. On the other hand, and following Eq. (3. 44), the NEP calculated for the operating conditions, already explained in detail, is of 303.12μW/cm^2. The quantification of Eq. (3. 66) showed that for the case of this pixel configuration, the SF1 stage delivers 35.9% of the total noise, whilst the *n*-well PD reset operation delivers 5.84% with 0.07% originated by the RST transistor partition noise, the shutter transistor delivers 16.9%, the SF2 stage 11.37%, and the CDS circuit the rest 29.9%. The dark and photon noises are not considered here, as for comparison purposes they remain constant under identical operating conditions and identical *n*-well PD areas for all three *n*-well PD based TOF pixel configurations which we examine in detail in this chapter.

A second pixel configuration is then proposed, targeting the reduction of NEP of the pixel structure, as it is described in the following section.

3.4.2 TOF Pixel Configuration with an *n*-well PD and a Single Source-Follower Based Buffer

The second pixel, shown in Figure 3. 16, is then investigated. It lacks the SF1 stage, aiming at NEP decrease and lower power consumption. Here, the *n*-

well PD and the C_s are electrically coupled through M1, giving rise to charge-sharing during the integration stage, i.e. the charge integrated at the *n*-well PD is not completely transferred to C_s during the integration process. This effect reduces the spectral responsivity of the pixel by 3.4% (to a measured value of $\Re$=24.95V·cm^2/μJ). On the other hand, the power consumption of this second pixel configuration is of around 330μW (one half of the previous case), and $\sqrt{\overline{v_{n\_out}^2}}$ decreases by 29.8% to 164.67μV. For the output noise analysis, once again Eq. (3. 66) can be followed, eliminating $\overline{v_{n\_SF1}^2}$ and merging $\overline{v_{n\_C_{PD}}^2}$ and $\overline{v_{n\_shutter}^2}$. Also, the amplification factor of the first buffer stage in the previous structure, A_{SF1}, is not applicable any more to the individual mean square voltage analysis.

Considering $\overline{v_{n\_C_{PD}}^2}$ and $\overline{v_{n\_shutter}^2}$, it should be recalled that the *n*-well PD reset node and the capacitor C_s are disconnected when the shutter switch M1 is thrown OFF, which means that the capacitance noise contribution during the readout process is due exclusively to C_s. On the other hand, during the integration phase, they remain connected, which means that they both should have an influence on the amount of noise forming part of the signal charge collected in the *n*-well PD SCR, as well as on C_s. The noise equivalent small-signal circuit for the case of the system formed by the reset transistor RST, the shutter transistor M1, the *n*-well PD and C_s can be observed in Figure 3. 17.

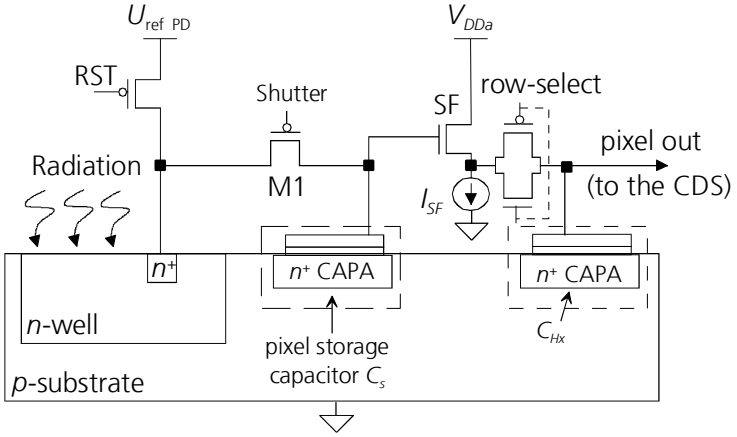


Figure 3. 16 – TOF pixel configuration with an *n*-well PD and a single *source-follower* based buffer.

In Figure 3. 17, the mean square noise voltage contribution of the joint reset operation, where participate both, the RST and the M1 transistors, referenced to the common analog ground and measured immediately after the *n*-well PD capacitance, can be defined as $\overline{v_{n\_C_{PD}}^2} = \overline{v_{PD\_RST}^2} + \overline{v_{PD\_M1}^2}$, where the first term stands for the noise contribution of the RST transistor and the second for M1. Moreover, the mean square noise voltage contribution of the shutter transistor M1 and the RST transistor, measured as $\overline{v_{n\_J}^2}$ in Figure 3. 17, can be defined as $\overline{v_{n\_J}^2} = \overline{v_{C_s\_RST}^2} + \overline{v_{C_s\_M1}^2}$.

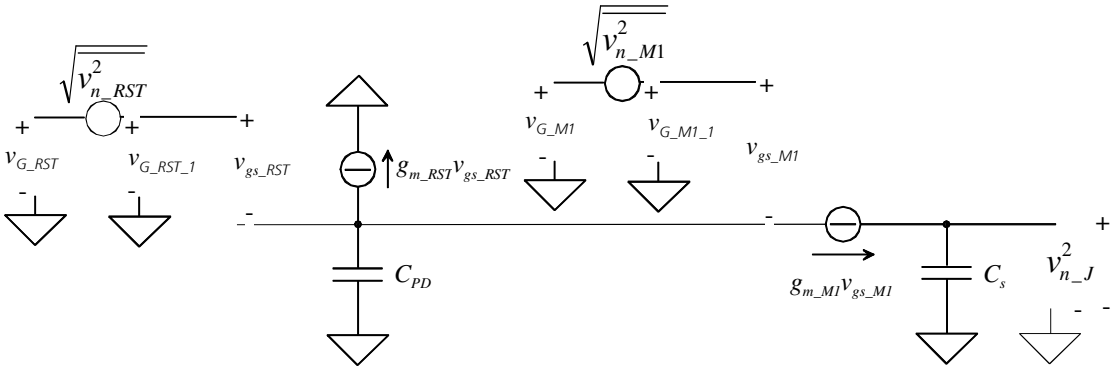


Figure 3. 17 - Noise equivalent small-signal circuit diagram for the calculation of the mean square noise voltage $\overline{v_{n\_J}^2}$ input of the SF buffer stage (see Figure 3. 16).

Following the analysis performed in [Bus03] for a very similar case, $\overline{v_{n\_C_{PD}}^2}$ can be defined as shown in Eq. (3. 67) [Bus03], and $\overline{v_{n\_C_s}^2}$ as Eq. (3. 68) [Bus03], both based on small-signal noise equivalent circuit diagram shown in Figure 3. 17.

$$\overline{v_{C_{PD}}^2} = \frac{k_B T}{C_{PD}} \left(\frac{\left(\frac{1}{g_{m\_RST}}\right)C_{PD} + \left(\frac{1}{g_{m\_M1}}\right)C_s + \left(\frac{1}{g_{m\_RST}}\right)C_s}{\left(\frac{1}{g_{m\_RST}}\right)C_{PD} + \left(\left(\frac{g_{m\_RST} + g_{m\_M1}}{g_{m\_RST}\, g_{m\_M1}}\right)\right)C_s} \right) = \frac{k_B T}{C_{PD}} \tag{3. 67}$$

$$\overline{v_{C_s}^2} = \frac{k_B T}{C_s} \left(\frac{\left(\frac{1}{g_{m\_RST}}\right)C_s + \left(\frac{1}{g_{m\_RST}}\right)C_{PD} + \left(\frac{1}{g_{m\_M1}}\right)C_s}{\left(\frac{1}{g_{m\_RST}}\right)C_{PD} + \left(\left(\frac{g_{m\_RST} + g_{m\_M1}}{g_{m\_RST}\, g_{m\_M1}}\right)\right)C_s} \right) = \frac{k_B T}{C_s} \tag{3. 68}$$

According to Eqs. (3. 67) and (3. 68), the conclusion is that $\overline{v_{n\_J}^2}$ depends exclusively on the capacitance C_S and not on the joint capacitance (C_{PD}+C_s), increasing the noise contribution of the reset stage, responsible for the 41.2% of the output noise. The partition noise, obtained using Eq. (3. 50), only eliminating the A_{SF1} amplification factor, equals the 1.84% of the output noise. The SF buffer mean square noise voltage, obtained using Eq. (3. 53), adds 15.7%, and the CDS circuit, the contribution of which was calculated in the same way as in the previous case, the last 41.26%. The NEP for this pixel is of 220μW/cm^2 (for the same operating conditions already described), and the fill-factor, for the case of (130×300)μm^2 pixel, is again of 52.3% (although space optimisation is possible).

3.4.3 TOF Pixel Configuration with an *n*-well PD, one *Common-Source* Amplifier and one *Source-Follower* Based Buffer

The third pixel structure, diagram of which can be observed in Figure 3 18, pursues an increase in the SNR by an additional amplification of the *n*-well PD output signal using a *common-source* (CS) amplifier formed by transistors M2 and M3 (with a desired amplification factor A_{CS}=4). Here, the CS amplifies the PD output signal together with the reset and the partition noises, all components that will be additionally amplified at the CDS stage in A_{CDS}=4. Nevertheless, the additional noise generated by the shutter transistor M1, the SF stage, and the CDS circuit is only amplified by the A_{CDS} factor, i.e. four times less.

The measured NEP of this kind of pixel configurations decreases its value to 191μW/cm^2 [Fon06]. The spectral responsivity on the other hand, measured under identical operating conditions as in the previous two cases, increases its value almost 5 times (reaching $\Re$=127.3V·cm^2/μJ) when compared to the pixel shown in Figure 3. 13 under the same operating conditions. Unfortunately, the peak power consumption of the pixel increases to the unacceptable 2.64mW, where only the CS amplifier consumes 700μA and introduces electrical cross-talk through parasitic effects related to the electrical connections on-chip.

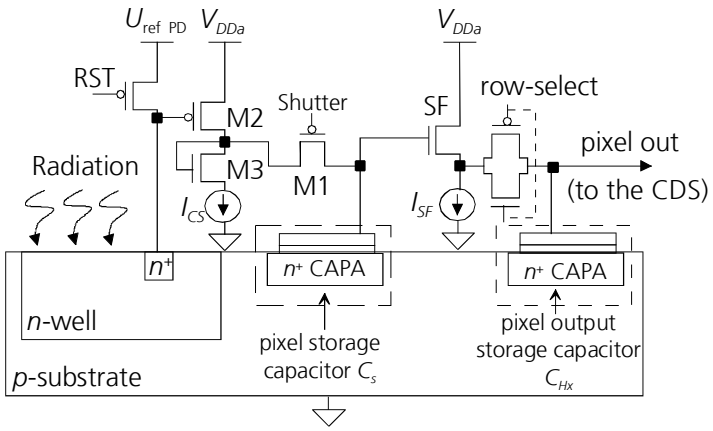


Figure 3. 18 – TOF pixel configuration with an *n*-well PD, one *common-source* amplifier, and one *source-follower* based buffer stage.

Additionally, the CS amplifier yields an inverse output voltage, which means that the SF stage input finds itself normally in the range of voltages below the 1.6V: the SF threshold voltage required to achieve the desired buffer amplification. So, the $U_{ref\,1}$ has to be reduced to 2.2V, which leads to an increase in the *n*-well PD capacitance, and consequently causes a 10% loss in the pixel spectral responsivity due to the charge-to-voltage conversion factor (reaching $\Re$=114.2V·cm^2/μJ) [Fon06]. Also, the response speed of the CS amplifier remains below the desired value[4]. The fill-factor in case of a (130×300)μm^2 pixel depicted in Figure 3. 18 is of 40%.

[4] For more details, consult [Fon06].

Regarding a detailed noise analysis of the common-source amplifier stage, its noise equivalent small-signal circuit diagram can be observed in Figure 3. 19.

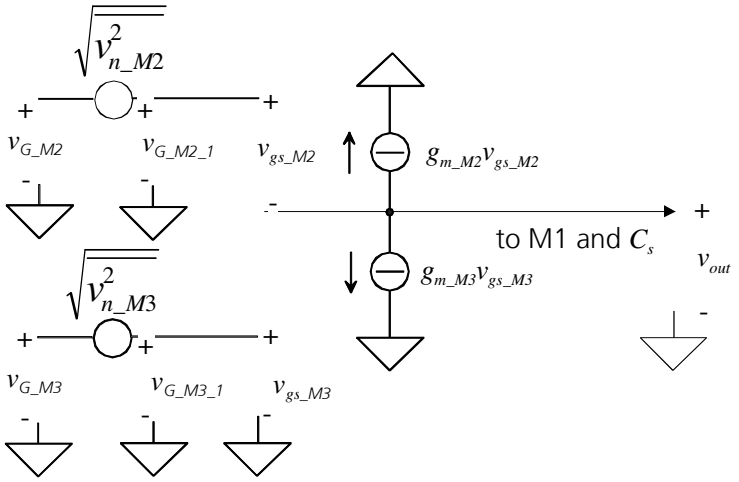


Figure 3. 19 - Noise equivalent small-signal circuit diagram of the *common-source* amplifier stage in the TOF pixel configuration shown in Figure 3. 18.

Following the KVL applied to the node existent between the two current sources, $g_{m\_M2}v_{gs\_M2}$ and $g_{m\_M3}v_{gs\_M3}$, shown in Figure 3. 19, the output noise voltage of the *common-source* amplifier stage in the pixel, v_{out}, can be defined as shown in Eq. (3. 69).

$$v_{out} = \frac{1}{1 + s\dfrac{C_s}{g_{m\_M2}}}\left(v_{G\_M2\_1} + g_{m\_M3}\frac{v_{G\_M3\_1}}{g_{m\_M2}}\right) \tag{3. 69}$$

Following Eq. (3. 69), the 3dB frequency results in Eq. (3. 70), while the noise bandwidth can be defined as shown in Eq. (3. 72).

$$f_{3dB} = \frac{g_{m\_M2}}{2\pi C_s} \tag{3. 70}$$

$$\Delta f = \frac{g_{m\_M2}}{4C_s} \tag{3. 71}$$

Based on the same analysis performed for the SF1 buffer stage present in the pixel configuration depicted in Figure 3. 13, performed to obtain Eq. (3. 58), the CS amplifier stage mean square noise voltage is here defined as shown in Eq. (3. 65), where A_{CS} is the CS amplifier amplification factor. Circuit simulations performed using *Cadence*® software tools showed that both transistors, M2 and M3, remain during the readout phase in strong inversion, i.e. $\gamma_{M2}=\gamma_{M3}=2$.

$$\overline{v_{n\_CS}^2} = \frac{k_B T}{C_s}\cdot\left(\gamma_{M2} + \gamma_{M3}\left(\frac{g_{m\_M3}}{g_{m\_M2}}\right)\right)\cdot\left(\frac{C_{c1}}{C_{Fx}}\right)^2 \cdot A_{CS}^2 \cdot A_{SF}^2 \tag{3. 72}$$

Performing a similar analysis as for the previous two cases and calculating the amount of mean square noise voltage in each stage, referred to the output of the CDS circuit, and considering always the C_{c1}/C_{Fx} ratio, as well as the CS amplifier (A_{CS}=4), the SF (A_{SF}=0.85), and the CDS (A_{CDS}=4) amplification factors, the following results were obtained. Namely, for the pixel configuration shown in Figure 3. 18, the PD reset delivers 15.8% of the final noise voltage $\sqrt{\overline{v_{n\_out}^2}} = 654.37\,\mu V$, the CS amplifier the 75.6% (as expected), the SF buffer 1.92%, and the CDS circuit the remaining 5.8%.

Table 3. 1 offers a general overview of the three pixel configurations analysed so far, based on identical *n*-well PD photodetectors, fabricated in the 0.5μm standard CMOS process under study, and aimed for 3-D time-of-flight imaging application. In all cases, as it was thoroughly explained, the values enlisted in Table 3. 1 are obtained for T_{int}=30ns, and λ=910nm of reflected laser pulse impinging radiation. Additionally to all the figures of merit already mentioned, the maximum SNR was added to Table 3. 1, obtained in decibels for the ratio between the PD output voltage span V_{PD}, and the respective amount of $\sqrt{\overline{v_{n\_out}^2}}$, as $SNR_{\max} = 20\log\frac{V_{PD}}{\sqrt{\overline{v_{n\_out}^2}}}$. In all three cases, an output voltage span of 2.2V was measured at the end of the readout chain (V_{out_max}=2.2V). Following, V_{PD} was obtained by respectively dividing V_{out_max} by all the amplification factors present in the pixel readout chain for each of the pixel configurations under investigation, namely A_{SF1}=A_{SF2}=0.85, A_{CDS}=4, and A_{CS}=4.

Table 3. 1

Pixel Configuration	Responsivity $\Re$, V·cm²/μJ	Peak Power Consumption, μW	Contribution to $\overline{v_{noise\_out}^2}$	NEP, μW/cm²	Fill-factor for (130×300)μm² pixel area	Max. SNR, dB
***n*-well PD and 2 SF buffers**	25.83	660	PD reset: 5.84% partition: 0.07% SF1 stage: 35.9% shutter: 16.9% SF2 stage: 11.37% CDS: 29.9%	303.1	52.3%	70.2
***n*-well PD and a single SF buffer**	24.95	330	(C_{PD}+C_s) reset: 41.2% partition: 1.84% SF buffer: 15.7% CDS: 41.26%	220	52.3%	72.19
***n*-well PD, one CS amplifier and one SF buffer**	114.2	2640	PD reset: 15.8% CS amplifier: 75.6% SF buffer: 1.97% CDS: 5.8%	191	40%	47.76

Table 3. 1 shows how the circuit design affects the pixel performance, because all three pixel configurations use the same PD type. From the results enlisted, it can be concluded that, depending on the application, the right choice for a pixel configuration to be fabricated in the 0.5μm standard CMOS process

under investigation should fall between the first and the second options. The third option was a nice try, but it proved completely unsuitable because of its tremendously high power consumption and quite low SNR_{max} if compared to the other two options. Also, the noise generation was not significantly lower in this configuration if compared to other two ones. The criteria to be followed when choosing between the two first options should be based on power consumption and NEP, as $\Re$ and maximal SNR are quite similar in both cases.

Following the experience gained from the pixel comparison just described, a test 4×4 pixel CMOS imager was then designed which could contain different pixel configurations to be compared, using the same readout circuitry. This test imager was then simulated using *Cadence*® software tools, and its layout was drawn. The idea was to generate a general imager frame, containing the CDS stages (one per column), the multiplexed connections to each of the 16 (100×100)μm^2 pixel structures, as well as the imager output buffer amplifier circuit, to be able in the future to compare the different pixel configurations without the need of generating a completely new imager design each time. This should save time and allow direct comparison between the different pixels integrated on identical imager systems. Unfortunately, as the test imager was designed for the 0.5μm standard CMOS process under investigation so far, and in the mean time, all the efforts were started to focus on the newly developed 0.35μm CMOS process at the Fraunhofer IMS, whose possibilities will be shortly described in the final chapter of this text, the test imager has not been fabricated. Thus, only the theoretical considerations and the simulation results obtained for the test imager designed will be briefly presented in the next section. Based on the results enlisted in Table 3. 1, the BPD photodetector, together with a single SF buffer pixel configuration was chosen, taken here as an example to show how a complete (although quite small) imager is designed.

3.5 4×4 Pixel CMOS Test Imager Designed in the 0.5μm Standard CMOS Process

The 4×4 pixel CMOS test imager to be fabricated in the 0.5μm standard CMOS process under investigation is presented in Figure 3. 20. Namely, it consists of 16 pixel structures, 4 CDS circuits (one per pixel column), one *source-follower* based buffer SF2 incorporated to drive the CDS output signal on its path to the imager output buffer, and the output buffer of the entire CMOS imager. As the idea is to be able to fabricate and compare different pixel configuration within the same imager, five global signals were considered which should serve as input signals to any pixel (or most of them). In Figure 3. 20 these global pixel signals were named *row control signals*.

The idea is to use global integration and rolling readout approach for designing the CMOS imager. This means that all the 16 pixels will collect photo-thermally- generated carriers during a certain T_{int} simultaneously, but their signals will be delivered to the CDS circuits row-per-row, 4 pixels at a time in parallel. To achieve this, four additional signals are generated to select the desired row to be read out, one at a time. In Figure 3. 20, these signals were named *row select signals* and the combination of those with the *row control* signals enable the

readout of each selected row in a multiplexed manner. Once each of the four CDS circuits is ready to deliver an output signal belonging to one of the four selected pixels, these CDS output signals will be delivered to the imager output buffer, once the signals have been driven by the SF2 intermediate buffer, in a serial manner, controlled by the 4 column select signals additionally implemented in the circuit. In Figure 3. 20 they are called *col select signals*. In this way, the CMOS imager output voltage V_{out} will consist of a series of output signals belonging for example, to the *Pixel 0*, followed by the one belonging to the *Pixel 1*, then *Pixel 2*, and finally *Pixel 3*, all the four pixels forming the first pixel row of the 4×4 pixel imager. The same readout sequence is then repeated for the second row, and continues in this way until all the 16 pixel output signals have been read out.

As mentioned before, it was decided to design the 4×4 pixel CMOS test imager using at first the basic pixel configuration consisting of the BPD photodetector structure and a single SF based buffer. The simplified schematic diagram of such a pixel can be observed in Figure 3. 21, and its operation was already described in the previous section in this text. Note that an additional NMOS transistor is incorporated here for the anti-blooming function. Normally, this function is performed by the NMOS RST transistor in soft-reset operation modus. Here, both benefits are pursued, namely the hard-reset operation together with the anti-blooming alternative.

Moreover, referring to Figure 3. 21, not all of the five global pixel signals (*row control signals* (0..4)) are used in this pixel configuration. Actually, only 3 of them will be applied, named in the following manner: instead of the *row control signal 0*, the *reset* (RST) signal (Figure 3. 21) are used from now on, instead of *row control signal 1*, the *shutter* signal (Figure 3. 21), and instead of the *row control signal 2*, the *select* signal (Figure 3. 21). The remaining two row control signals are referred from now on as *not in use* (nu).

Considering the C_s value of 1.94pF, as well as the *shutter* and *select* transmission-gate based MOSFET switches (transmission-gate configuration is here used to expand the pixel output voltage span), the layout generated using *Cadence*® software tools for each of the (100×100)μm^2 pixels to be fabricated in the 0.5μm standard CMOS process under investigation can be observed in Figure 3. 22.

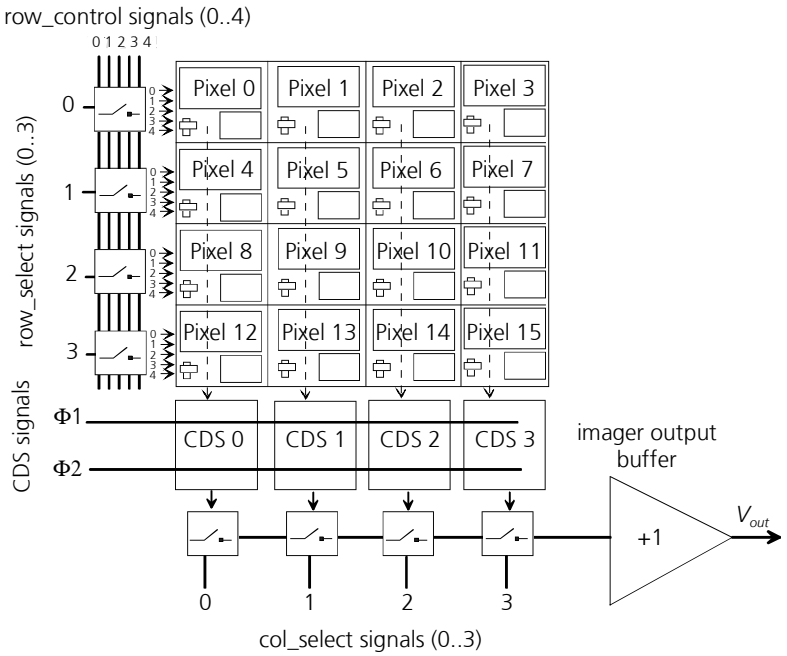


Figure 3. 20 – Schematic diagram of the 4×4 pixel test CMOS imager to be fabricated in the 0.5μm CMOS process showing the 16 pixel structures, the 4 CDS circuits (one per column), the imager output buffer, and the applied signals: 5 global pixel signals (*row control signals* (0..4)), 4 row selecting signals (*row select* (0..3)), and the 2 CDS circuits input signals (Φ1 and Φ2).

From the layout shown in Figure 3. 22, it can be concluded that for a pixel size of (100×100)μm^2 and the pixel circuit configuration shown in Figure 3. 21, the photoactive area occupies (90×53.8)μm^2, i.e. the pixel has a fill-factor of 48.4%.

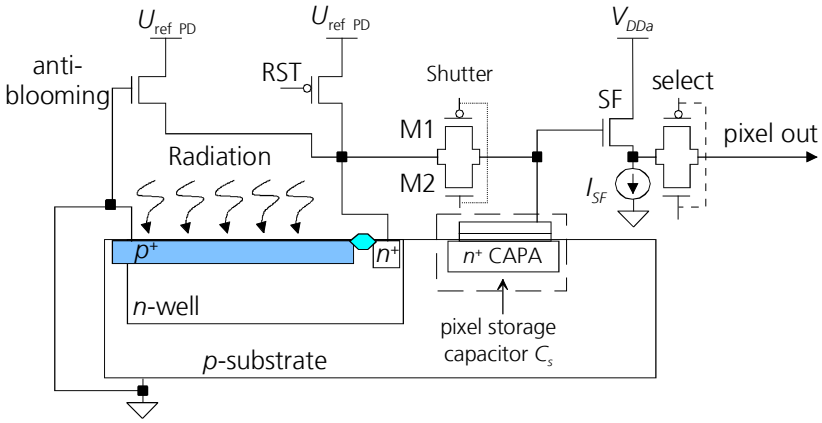


Figure 3. 21 – Basic BPD based pixel configuration, containing a single SF buffer stage, used in the design of a 4×4 pixel CMOS test imager to be fabricated in the 0.5μm standard CMOS process.

For the BPD area mentioned, the photodetector generates a dark current I_{dark}=11.33fA, as it can be extracted from Figure 2. 27. On the other hand, observing the optical sensitivity results obtained for the BPD and shown in Figure 2. 30, it can be concluded that the maximum current response of the device is obtained for the impinging radiation with λ=626nm wavelength, where its optical sensitivity is S=0.373A/W. So, in order to estimate an average photocurrent delivered by the BPD, it is considered here that 10^2 lux (room-

lighting or average out-doors illumination [Bre99]) of red light are impinging on the pixel photoactive area. Converted into irradiance, it is E_R=1.47×10^{-5}W/cm^2, and the delivered photocurrent is in this case I_{ph}=265.6pA. Finally, the BPD capacitance reaches C_{BPD}=3.02pF, as it can be calculated from the results presented in Figure 2. 29.

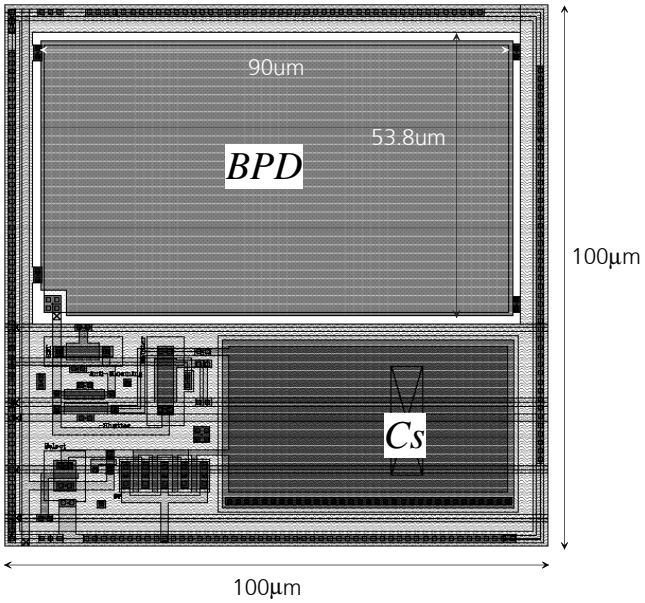


Figure 3. 22 – Layout of the (100×100)μm^2 *BPD and a single SF based buffer stage* pixel forming part of the 4×4 pixel CMOS test imager to be fabricated in the 0.5μm standard CMOS process.

According to Eqs. (3. 67) and (3. 68) the pixel reset noise depends exclusively on the value of C_s, so the difference of using a BPD instead of the already discussed *n*-well PD as photodetector in this kind of pixel configurations can be observed exclusively in the dark current reduction.

The entire readout chain, following each of the 16 pixels in this CMOS imager, can be observed in Figure 3. 23. As already explained, the CMOS imager designed works respectively in a global shutter integration, and rolling readout manners. This means that after the BPD and C_s global reset, performed during 1ms in all the pixels, enabled by the *reset* signal applied to the RST PMOS transistors (Figure 3. 21), the global integration phase begins with T_{int}=19ms. Once the integration time T_{int} is up (i.e., the *shutter* and *reset* switches are turned off), the first row (*row* 0) of pixels is enabled by turning the select transistors of each of the 4 pixels belonging to it ON, as well as the *row select signal 0*, shown in Figure 3. 20.

As it can be observed also in Figure 3. 24, where the time-diagram of the signals applied to the 4×4 pixel CMOS imager is shown, as soon as the integration time is over, and the first row of the imager has been enabled, the 4 pixel output voltages, containing the photo and dark current information, as well as all the mean square noise voltages generated during the reset and integration operations, are saved at the C_{cl} capacitor of each of the four CDS circuits, previously reseted to the U_{ref5} voltage (Figure 3. 23), by turning the Φ1 switches on, and leaving the Φ2 switches deactivated.

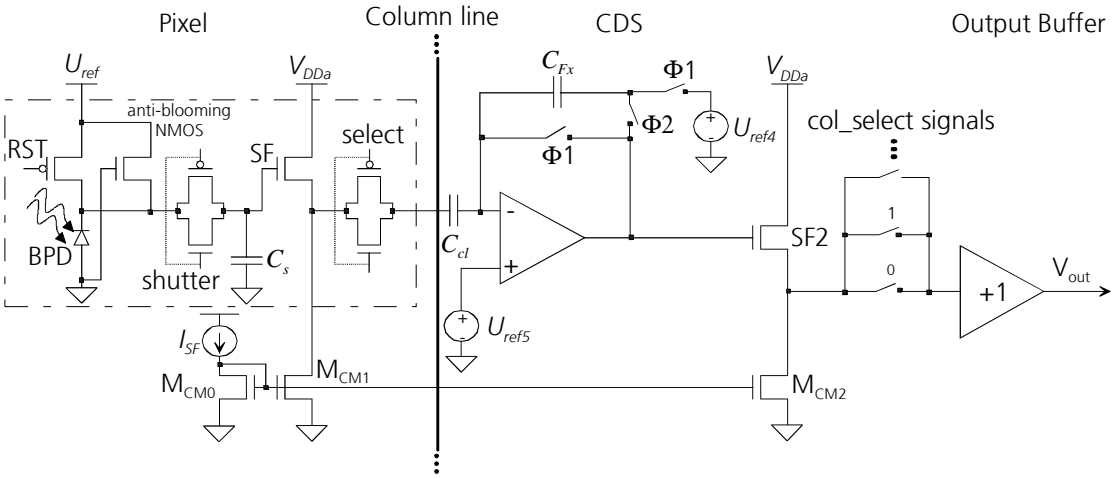


Figure 3. 23 - A simplified schematic diagram of the pixel readout chain, showing each pixel electric diagram (there are 16 of them), the CDS circuit (one per each of the 4 columns), the *source-follower* based buffer SF2 (one per column), and the 4×4 pixel CMOS imager output buffer.

As soon as the process of charging the C_{cl} capacitors to the pixel output voltages is over (8μs in this case), the Φ1 switches turn off, while the *reset* and *shutter* switches of each of the 4 pixels belonging to the selected pixel row, as well as the Φ2 switches of the CDS circuits turn on. This enables the pixel output reset voltage to be substracted from the original pixel output value already saved at each of the designated C_{cl} capacitors, and their difference to be stored at each of the C_{Fx} capacitors (Figure 3. 23) forming part of the CDS stage. The voltage value stored at each C_{Fx} capacitor is then considered to be the output signal of a determined pixel, free of low-frequency noise components and offsets generated mainly during the BPD reset operation.

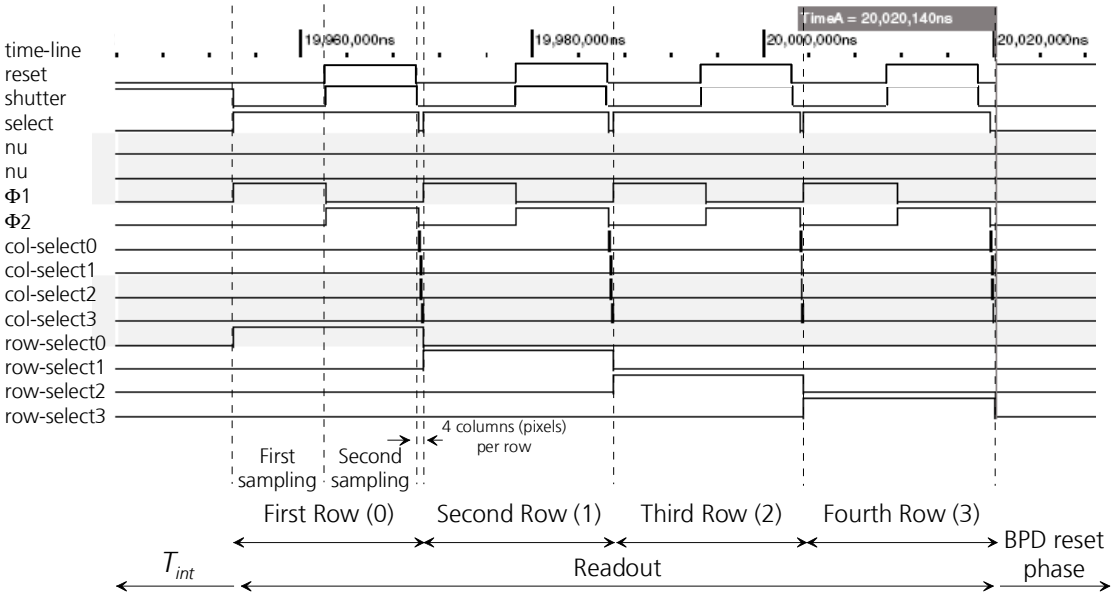


Figure 3. 24 – Time-diagram used for the 4x4 pixel CMOS imager, showing the imager readout stage, with *reset*, *shutter*, and *select* signals applied to each of the 16 pixels, the two available *row control signals not in use* (nu), Φ1 and Φ2 signals used by each of the 4 CDS circuits, and the column and row select signals.

Normally, in order to eliminate the exact amount of noise and offset voltages from the pixel output signal, the pixel output reset voltage generated during the first BPD reset operation (before the beginning of the integration phase) should be saved at an analog memory cell and this value should substracted from the pixel output voltage obtained during the pixel readout phase. This operation is then called *"true" correlated double sampling*. In this case, only an approximated amount of noise is eliminated from the pixel output voltage (but still close enough), so we speak here about approximated correlated double sampling or *delta differential sampling* (DDS).

Considering the amounts of dark- and photo- currents expected to be delivered by the BPD photodetector under normal operating conditions, a parametric electrical simulation of the entire readout chain was performed using *Cadence*® software tools. The results obtained can be observed in Figure 2. 25, where the voltage signals delivered respectively by the BPD (*diode out*), each pixel (*pixel out*), the CDS circuit (*cds out*), and finally the imager output buffer (*chip out*) were plotted against the expected amount of signal current delivered by the BPD.

From Figure 3. 25 can be concluded that, although the BPD based pixel configuration was optimised to deliver an output voltage span ranging respectively from –0.3V to almost 3.3V for the BPD generated signal currents in the range between 0A and 385pA, after each stage belonging to the readout chain, this voltage span has been reduced, resulting at the end in the range between the 0.35V and 2.54V, respectively.

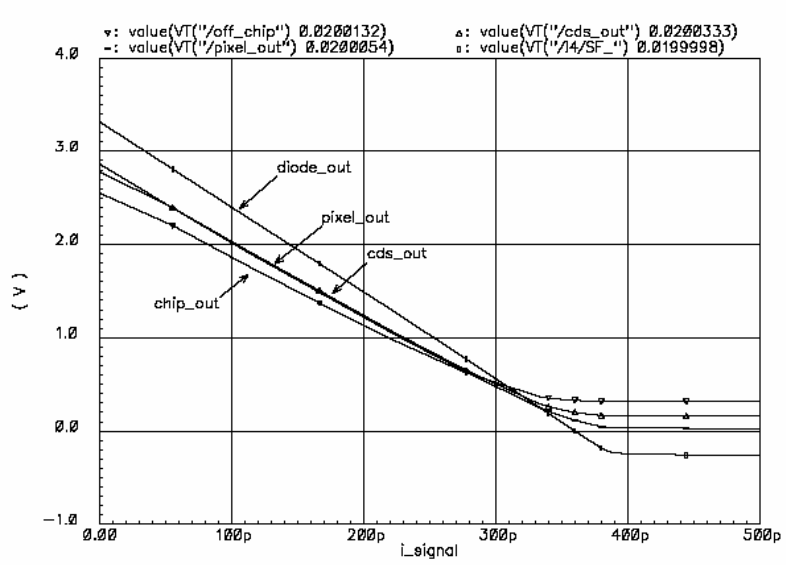


Figure 3. 25 – Results of the electrical parametric simulation performed for the 4x4 pixel CMOS test imager to be fabricated in the 0.5μm standard CMOS process showing the output voltage signals delivered by each of the readout chain stages, dependent on the amount of signal current generated by the BPD photodetector.

The layout of the entire 4x4 pixel CMOS test imager, generating using *Cadence*® software tools, can be finally observed in Figure 3. 26. In Figure 3. 26, the matrix conformed by the 16 BPD based pixels, as well as the 4 CDS circuits,

the imager output buffer, as well all the necessary pad structures can be observed. The entire imager circuit occupies (1540x1820)μm^2.

So far, pixel configurations, and even an entire 4x4 pixel CMOS test imager, based exclusively on reverse-biased *p-n* junction photodetector structures were analysed in detail. Nevertheless, these photodetectors are not the only alternative left. In the next section, a PG based pixel configuration will be proposed, which instead of charge coupling between the PG and a separated FD, uses charge injection into the substrate as a readout principle.

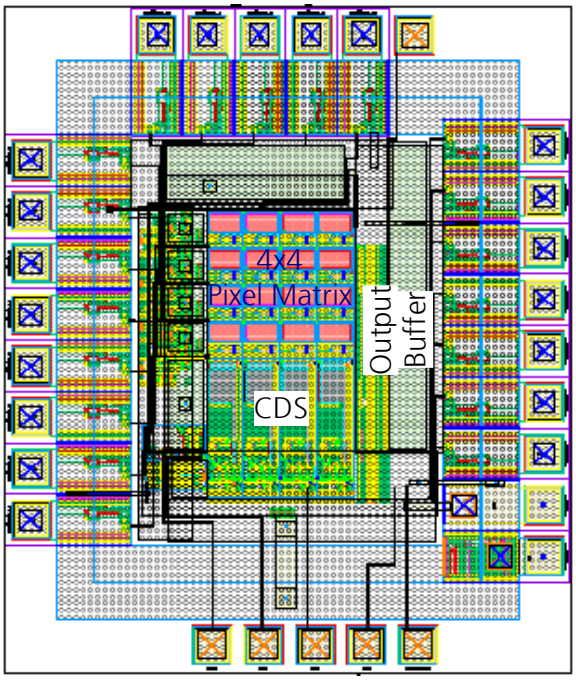


Figure 3. 26 – Layout generated using *Cadence*® of the entire 4x4 pixel CMOS test imager to be fabricated in the 0.5μm standard CMOS process.

3.6 CMOS Charge-Injection Photogate Active Pixel Sensor (CI-PG APS)

Another principle of operation is used in the proposed *charge-injection photogate* (CI-PG) pixel, schematic of which can be found in Figure 3. 27(a). It relies on injection of the photogenerated charge, collected during T_{int} in the *p*-type PG SCR, into an electrically floating *n*-well substrate. It represents an alternative readout principle of a PG based pixel configuration, aiming to replace the charge-coupled PG and FD regions required for standard PG APS readout. Of course, all the considerations made during the discussion in reference to the collection of photo- and thermally- generated minority carriers during the integration phase for the case of standard PG based pixels, remain valid here.

Once the integration phase is over, during which U_{PG} remained reverse biased at V_{DD}=3.3V, as it can be observed in the time diagram showed in Figure 3. 27(b), rapidly rising at t=T_{int} the PG bias voltage during a certain $T_{readout}$ time from U_{PG}=-3.3V towards V_{GND}=0V, the SCR gradually collapses and the majority carriers generate an injection current in the *n*-well. This injection current is

sensed at the *n*-well substrate ring-electrode fabricated around the PG in form of a voltage drop measured across the high-resistivity polysilicon based load resistance R_L (Figure 3. 27(a)).

During T_{int}, the *n*-well remains grounded, time during which M_{S0} is closed (Figure 3. 27(b)). Short before the PG transition, M_{S0} stops conducting and leaves the *n*-well floating during $T_{readout}$, as shown in the time diagram in Figure 3. 27(b). This enables the injection current to be sensed for readout. The process of charge injection will be analysed more in detail in the next section.

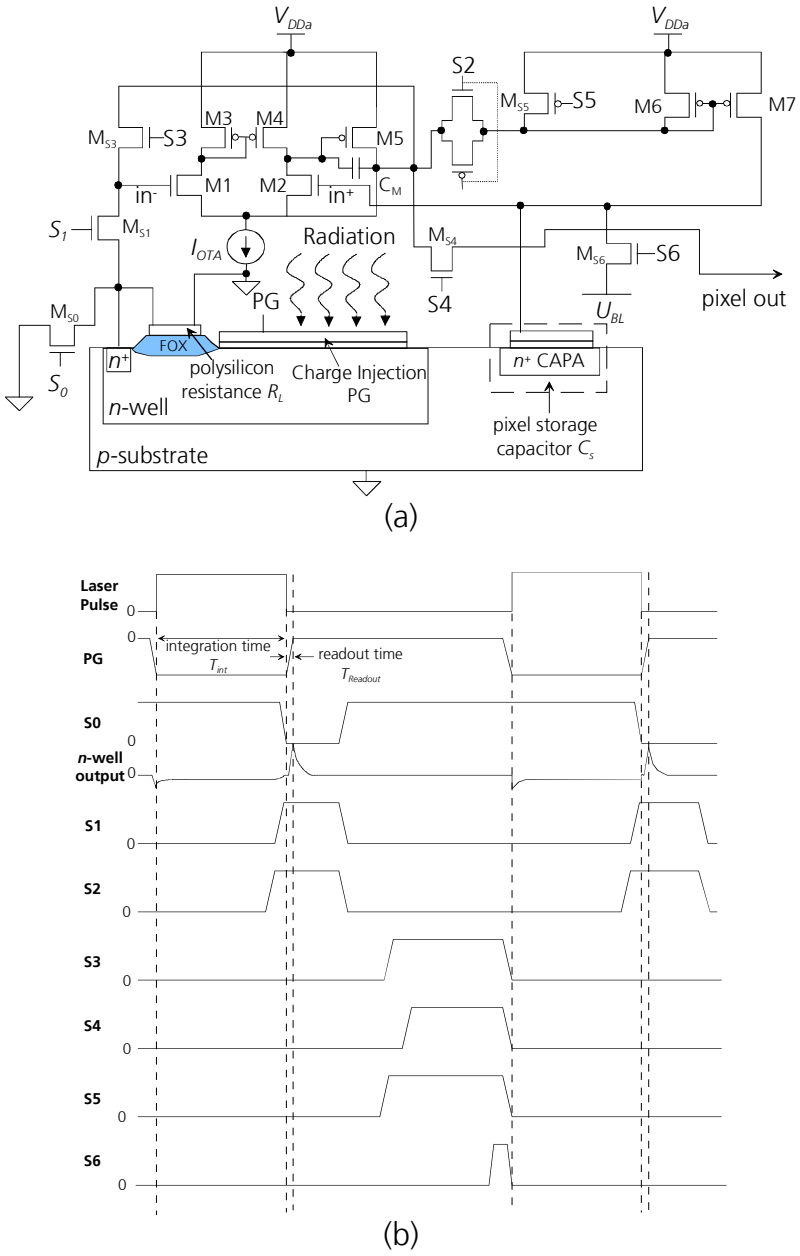


Figure 3. 27 – (a) Schematic of the *charge-injection photogate* (CI-PG) pixel configuration; (b) time-diagram used for the circuit diagram presented in (a).

3.6.1 Physical Principles of the Charge Injection Process in the CI-PG APS

At first, it is important to stress that because of the very short duration of the charge injection stage, it is possible to neglect any photo- or thermal-generation during this charge injection process. So, the charge injected into the *n*-well is assumed to represent the exact amount of charge collected during the integration process of the *p*-type PG under study.

The time dependence of the applied PG bias voltage is defined by Eq. (3. 73) [Dur03].

$$U_{PG}(t) = \begin{cases} V_{GND} - \dfrac{V_{GND} - |V_{DD}|}{T_{readout}} \cdot t, & T_{\text{int}} < t < T_{readout} \\ V_{GND}, & t \geq T_{readout} \end{cases} \tag{3. 73}$$

At the moment $t=T_{int}$, where the U_{PG} starts to rise from –3.3V toward 0V, the SCR (i.e. the potential well generated beneath the PG) starts to collapse, as the external voltage applied to the gate begins to decrease. This generates at first the so called SCR *displacement current* at the *n*-well contact, defined as Eq. (3. 74) [Mal04], where A_{PG} is the photoactive area of the *p*-type PG. The SCR displacement current, integrated by the majority carriers flowing into the volume previously occupied by the space-charge, continues to flow until the SCR width reaches the value W_{crit} at $t=T_{inj}$.

Namely, W_{crit} defines the *p*-type PG SCR width at which the minority carriers collected during T_{int} are to be found, drifted during charge collection to the silicon-oxide interface where there exists a maximum electric field. The case considered here is the one at which $W_{SCR}>W_{crit}$, i.e. the potential well is not full of collected minority carriers and the entire system operates out of thermal equilibrium. The new equilibrium condition will be reached at the moment when the inversion layer is formed, and $W_{SCR}=W_{inv}$, as it was explained in detail in Chapter 2 of this text.

$$I_{displ} = -qA_{PG}N_D \frac{dW_{SCR}}{dt} \tag{3. 74}$$

Following the SCR displacement current, as U_{PG} continues to decrease, an injection of holes into the substrate appears. Taking into account that the charge stored in the potential well can be defined as the product of the insulator capacitance C_{OX} and a certain gate voltage applied to the PG, for purposes of the present calculus, an auxiliary voltage V_{charge} is introduced such that $V_{GND} < |V_{charge}| < |V_{DD}|$ and the charge stored within the potential well is defined as $Q_{\text{int}} = C_{OX}\left|V_{ch\,\text{arg}\,e}\right|$. The absolute values of the bias voltages were considered here for mathematical simplicity, but will be omitted during the following analysis, considering always the positive values of the voltages, although not forgetting that the PG remains at all times under reverse-biasing.

Recalling the mathematical analysis of the charge storing process developed in Chapter 2 of this text for the *n*-type PG, if Eq. (2. 62) is applied to the case of the *p*-type PG that describes the system based on the KVL, and if the displacement current just described through Eq. (3. 74) is considered, the equation expressed by Eq. (3. 75) [Mal04] can be formulated. Here, $R_{n\text{-}well}$ stands for the resistance generated due to the undepleted *n*-well region.

$$U_{PG} = \frac{Q_{\text{int}} + qN_D A_{PG}}{C_{OX}} W_{SCR} + \frac{qN_D W_{SCR}^2}{2\varepsilon_0 \varepsilon_{Si}} + qA_{PG} N_D \frac{dW_{SCR}}{dt}\left(R_L + R_{n-well}\right) \tag{3. 75}$$

For $R_L >> R_{n\text{-}well}$, $R_{n\text{-}well}$ can be neglected. Considering $V_{charge} = \frac{Q_{\text{int}}}{C_{OX}}$, Eq. (3. 75) can be transformed into Eq. (3. 76) [Dur03] for non-steady conditions in which the charge flow and SCR width time dependence are taken into account for the bias transition from $-V_{DD}$ towards V_{GND}, introducing also the definition of C_{OX}.

$$U_{PG}(t) - V_{charge} = qA_{PG} N_D R_L \frac{dW_{SCR}}{dt} + \frac{qN_D W_{SCR}(t)^2}{2\varepsilon_0 \varepsilon_{Si}}\left(1 + \frac{2d_{OX}\varepsilon_{Si}}{\varepsilon_{OX} W_{SCR}(t)}\right) \tag{3. 76}$$

If it is assumed that $d_{OX}/W_{SCR}(t) << 1$ and Eq. (3. 76) is solved for dW_{SCR}/dt, the differential equation Eq. (3. 77) [Dur03] can be formulated to define the SCR width time dependence for the readout process.

$$\frac{dW_{SCR}}{dt} = \frac{1}{qA_{PG} N_D R_L}\left[U_{PG}(t) - V_{charge} - \frac{qN_D W_{SCR}(t)^2}{2\varepsilon_0 \varepsilon_{Si}}\right] \tag{3. 77}$$

At $t=T_{int}$, the value of the depletion region width is determined by the charge accumulated in the potential well during the charge storing process, as shown in Eq. (3. 78) [Dur03].

$$W_{crit} = \sqrt{\frac{2\varepsilon_0 \varepsilon_{Si}}{qN_D}\left(U_{PG} - V_{charge}\right)} \tag{3. 78}$$

As already explained, until $t = T_{inj}$, the only current flowing in the circuit is the displacement current due to SCR width time dependence. For $t \geq T_{inj}$, an injection current arises which is sensed in the outer circuit and can be defined as shown in Eq. (3. 79) [Mal04].

$$I_{inj} = -\frac{dQ_{\text{int}}}{dt} \tag{3. 79}$$

If the expression of the KVL applied to the circuit shown in Figure 3. 20(a) is taken into account, and as it was just mentioned, after $t = T_{inj}$ there exist no

SCR and consequently no voltage drop at the SCR either, Eq. (3. 80) [Dur03] can be formulated for the case of the *p*-type PG shown in Figure 3. 20(a).

$$U_{PG}(t) = \frac{Q_{\text{int}}}{C_{OX}} + R_L \frac{dQ_{\text{int}}}{dt} \tag{3. 80}$$

Solving the differential equation Eq. (3. 80) yields the injected charge time dependence for the readout process of the CI-PG as expressed in Eq. (3. 81) [Dur03], for the different stages already mentioned.

$$Q_{int}(t)= \begin{cases} V_{charge} C_{OX}\,, & \text{for } T_{int} < t < T_{inj} \\ Q_{\text{int}} e^{-\frac{t-T_{readout}}{R_L C_{OX}}} + C_{OX}\left[\begin{array}{l}\left(V_{DD} - \dfrac{(V_{DD}-V_{GND})t}{T_{readout}}\right) - V_{DD} e^{-\frac{t}{R_L C_{OX}}} + \\ + (V_{DD}-V_{GND})\left(1 - e^{-\frac{t}{R_L C_{OX}}}\right)\dfrac{R_L C_{OX}}{T_{readout}}\end{array}\right], & T_{inj}<t<T_{readout} \\ Q_{\text{int}} e^{-\frac{t}{R_L C_{OX}}} + C_{OX}\left[\begin{array}{l} V_{GND} e^{\frac{T_{readout}}{R_L C_{OX}}} - V_{DD} + \\ + V_{GND} C_{OX}\left[1 - e^{-\frac{t-T_{readout}}{R_L C_{OX}}}\right] + \\ + \dfrac{R_L C_{OX}(V_{DD}-V_{GND})}{T_{readout}}\left(e^{\frac{T_{readout}}{R_L C_{OX}}} - 1\right) e^{-\frac{t}{R_L C_{OX}}}\end{array}\right], & t > T_{readout} \end{cases} \tag{3. 81}$$

Next, it is possible to obtain the current dependence on time for the CI-PG readout process. As it was already discussed, depending on the percentage of the potential well (the PG SCR) that the collected charge occupies, the readout current will consist of two parts: first, the displacement current due to the depletion region width changing in time until $W_{SCR}=W_{crit}$, and second, the injection current due to the potential well stored charge injection into the substrate. This will induce the majority carriers (electrons) to generate an injection current in order to recombine with the injected holes, measurable in the outer circuit as the potential drop across R_L. Solving Eq. (3. 81) for dQ_{int}/dt, i.e. the injection current, Eq. (3. 82) [Dur03] is obtained. Of course, as the injection (readout) current of the CI-PG is measured as the voltage drop at R_L, $V_{readout}=I_{inj}(t)R_L$.

$$I_{inj}(t) = \begin{cases} -qA_{PG}N_D \dfrac{dW_{SCR}}{dt} = -\dfrac{1}{R_L}\left((V_{DD} - V_{charge}) - \dfrac{qN_D W_{SCR}(t)^2}{2\varepsilon_0 \varepsilon_{Si}}\right), & 0 < t < T_{inj} \\ \dfrac{Q_{\text{int}}(t)}{R_L C_{OX}} - \dfrac{U_{PG}(t)}{R_L}, & \text{for } t > T_{inj} \end{cases} \tag{3. 82}$$

3.6.2 Experimental Results Obtained for the CI-PG Photodetectors Fabricated in the 0.5μm Standard CMOS Process

At first, using the 0.5μm standard CMOS process under investigation, we fabricated and characterized CI-PG (300×300)μm^2 photodetector structures, i.e. *p*-type PGs, the simplified schematic diagram and the two dimensional electrostatic potential simulation results, obtained using the TCAD software tools, of which can be observed in Figure 3. 28 [Dur07P, Dur07E].

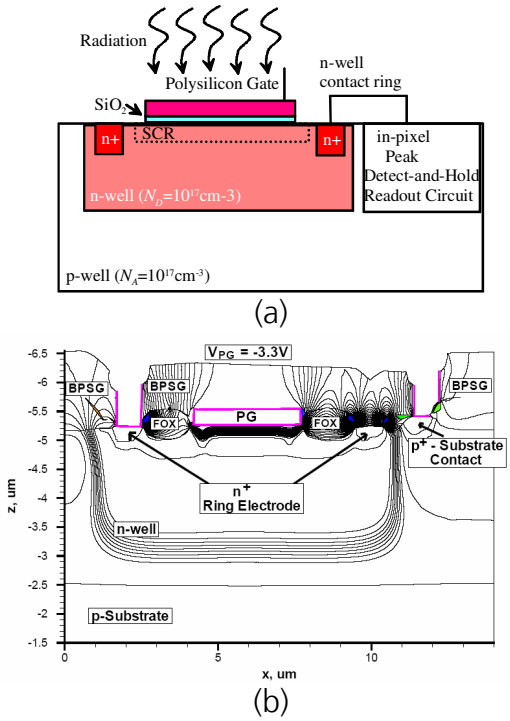
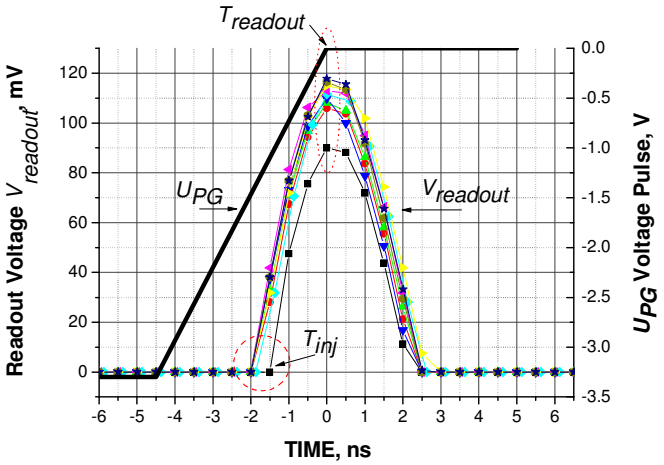


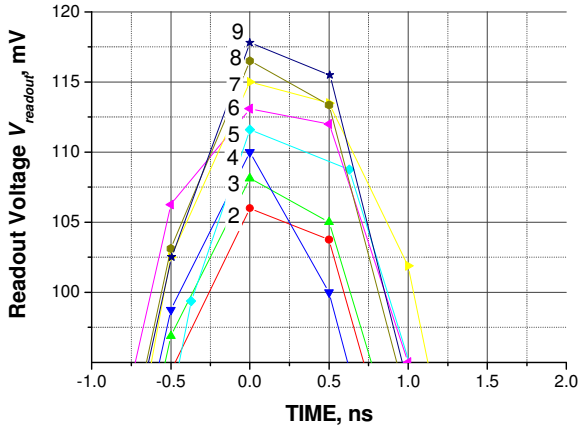
Figure 3. 28 - (a) simplified schematic of the CI-PG pixel [Dur07P]; (b) TCAD 2-D electrostatic potential simulation of the structure schematically shown in (a), fabricated in the 0.5μm CMOS process [Dur07E].

The test photodetector structures were illuminated first with visible red light (λ=625nm), at different irradiance values (between 20 and 160 μW/cm^2) during T_{int}=20ms (a standard rate used in most of video applications), using a transition time $T_{readout}$=4.5ns. The results obtained are shown in Figure 3. 29 [Dur07E], where a linear relation can be observed between the incoming photon flux impinging on the PG photoactive area and the readout current peaks measured as potential drop across the R_L=1kΩ.

On the other hand, in these measurements a high "time-compression" amplification [Mal03] arises, dependent on the amount of injected charge, due to the significantly longer T_{int}=20ms when compared to $T_{readout}$=4.5ns, as it is schematically shown in Figure 3. 30 [Dur03]. This parametric amplification is defined as the ratio of the readout current peak value (118μA) to the induced photocurrent in the charge integration phase (4.46nA), using R_L=1kΩ, and reaches, e.g. 2.73×10^4 for the case of 160μW/cm^2. The photodetector requires in this case 6.5ns for complete readout.



(a)



(b)

Figure 3. 29 – (a) Readout voltage peaks, obtained as a voltage drop at the load resistor R_L=1kΩ under U_{PG}, delivered by the (300×300)μm² CI-PG pixel photodetectors, with $T_{readout}$=4.5ns, when illuminated by visible red radiation (λ=625nm), at: 1) 0μW/cm², 2) 20μW/cm², 3) 40μW/cm², 4) 60μW/cm², 5) 80 μW/cm², 6) 100μW/cm², 7) 120μW/cm², 8) 140μW/cm², and 9) 160μW/cm²; (b) detail of the readout voltage peaks shown in (a) [Dur07E].

Considering the amount of injected charge into the *n*-well as the integral of the current readout peak in time, and calculating the areas below each of the readout curves shown in Figure 3. 29, the amount of injected (readout) charge can be obtained for each of the irradiance values of interest. Also, and based on the results obtained for the optical sensitivity of *p*-type PG photodetectors, shown in Figure 2. 42, which for the impinging radiation with wavelength λ=625nm is S=0.031A/W, the amount of collected charge in the PG SCR during T_{int}=20ms can be also calculated, for the area A_{PG}=(300×300)μm² and the dark current of I_{dark}=180pA/cm² obtained for the same structures (Figure 2. 40). If both values are compared, it can be concluded that during the charge injection process, and due to the influence of the thermal noise mainly generated by R_L, the readout amount of charge is in average 28.1%-52.8% smaller than the amount of collected charge during T_{int}. This is a discouraging number, which will be discussed later in this text.

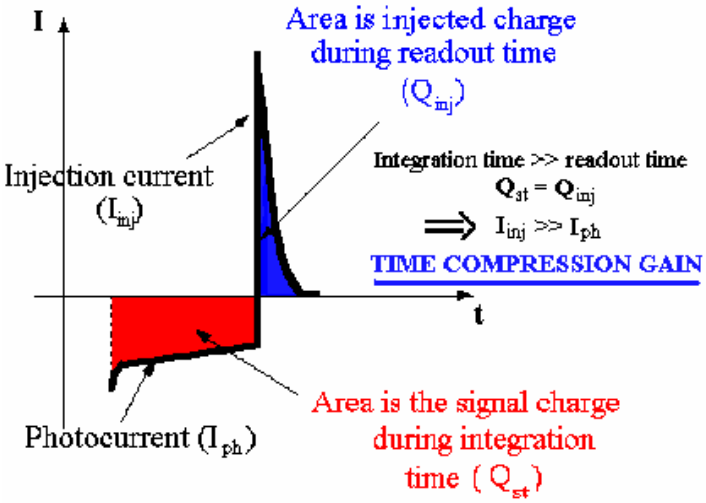


Figure 3. 30 – Diagram which explains the appearance of a huge "time-compression" amplification in charge-injection photogate detectors [Dur03].

Next, the same measurements performed on the CI-PG photodetector test structures were repeated, only this time using $T_{readout}$=1.4μs. The results obtained for the different irradiance values, ranging again between 20μW/cm^2 and 160μW/cm^2 of impinging radiation with λ=625nm can be observed in Figure 3. 30. The first problem aroused, which can be seen in Figure 3. 31, was the reduced discrimination possibility (i.e. decreased resolution) between the different curves, influenced by the decreased "time-compression" amplification factor, in this case 1.16×10^4 for the case of 160μW/cm^2, and the reduced amount of collected charge during the integration time. The expected reduction of the readout voltage peaks can be also observed in Figure 3. 31.

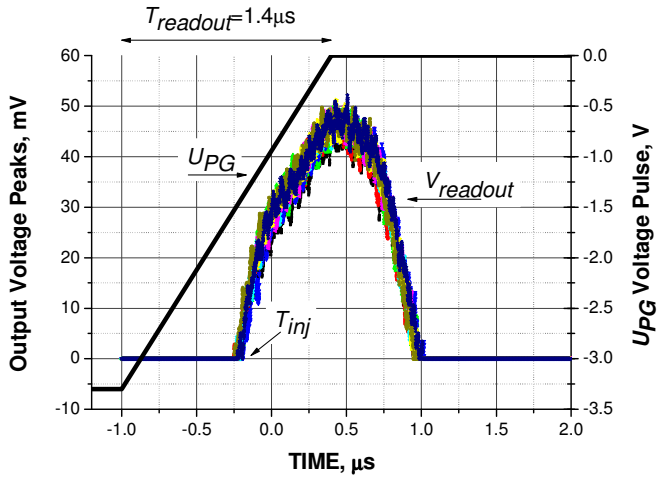
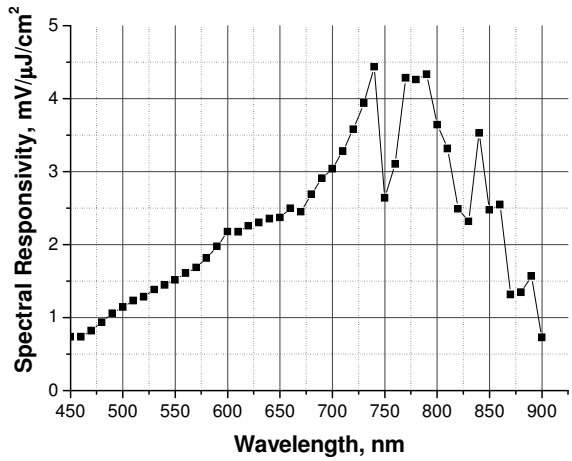


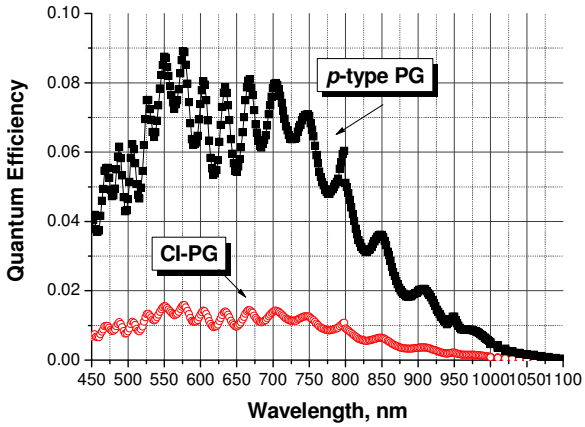
Figure 3. 31 - Readout voltage peaks, obtained as a voltage drop at the load resistor R_L=1kΩ, under U_{PG}, delivered by the (300×300)μm^2 CI-PG pixel photodetectors, with $T_{readout}$=1.4μs, when illuminated by visible red radiation (λ=625nm), at: 1) 0μW/cm^2, 2) 20μW/cm^2, 3) 40μW/cm^2, 4) 60μW/cm^2, 5) 80 μW/cm^2, 6) 100μW/cm^2, 7) 120μW/cm^2, 8) 140μW/cm^2, and 9) 160μW/cm^2.

As a following characterization step, the output voltage peaks of the CI-PG photodetector test structures were measured for impinging radiation in the range between λ=400nm and λ=900nm, while illuminating them by a 1000W

Xe/Hg lamp, followed by a monochromator, a measurement station described in Appendix A of this text. Once again, U_{PG}=-3.3V, V_{GND}=0V, T_{int}=20ms, $T_{readout}$=1.4μs, and R_L=1kΩ were used. The wavelength dependent spectral responsivity curve (in mV/μJ/cm^2) obtained is shown in Figure 3. 32(a). The "time-compression" amplification factors, strongly dependent on the irradiance values of the impinging radiation, i.e. the amount of the charge collected during T_{int}, in this case oscillate in this case between 2×10^3 and 1×10^4 [Dur07E].



(a)



(b)

Figure 3. 32 – (a) Spectral responsivity curve obtained for CI-PG photodetector test structures for impinging radiation with wavelengths in range from λ=450nm to λ=900nm, using U_{PG}=-3.3V, V_{GND}=0V, T_{int}=20ms, $T_{readout}$=1.4μs, and R_L=1kΩ; (b) quantum efficiency curves measured for the *p*-type PG on one side, and the CI-PG, obtained from the curve shown in (a), on the other.

The quantum efficiency values were then calculated, basing the calculations on the amount of injected charge contained in the readout voltage peaks from which the spectral responsivity $\Re$ curve showed in Figure 3. 31 was obtained. The results revealed that, specially when using $T_{readout}$=1.4μs, η drops to less than 20% of the original quantum efficiency measured for *p*-type PG, much more than for the measurements in which $T_{readout}$=4.5ns was used. Nevertheless, this could be also originated due to the difficulties encountered to

properly quantify the amount of injected charge from the results obtained for $T_{readout}$=1.4μs.

At the end, the external quantum efficiency of such a pixel, fabricated in the 0.5μm standard CMOS process under investigation, delivers quantum efficiency values shown in Figure 3. 32(b) ($\bar{\eta} \approx 1.1\%$), which result absolutely unacceptable for most applications. The latter is thought to be related to the reduced amount of collected charge, as well as with the high doping profile of the *n*-well in the 0.5μm CMOS process under investigation, both factors which drastically reduce the amount of injected charge effectively sensed at the load resistor, and increment the losses due to recombination and other quantum effects that participate in the charge injection process. This conclusion follows from the experimental results obtained for CI-PG pixel photodetectors fabricated on higher-resistivity substrates and the possibility of using up to 30V for U_{PG}, as it will be explained in Chapter 4 of this text.

3.6.3 Two-Phase Peak Detect-And-Hold (PDH) Circuit

Based on the results presented so far, the next step was to design a proper peak detector. For this task, a two-phase *peak detect-and-hold* (PDH) circuit which re-uses the same peak-sensing structure as an output buffer in order to cancel the otherwise additional buffer offset voltage was chosen [DeG02, Dur06] and is shown in Figure 3. 27 as a constitutional part of the CI-PG pixel presented. Here, as it can be observed in the time-diagram shown in Figure 3. 27(b), during the peak detection phase, the switches S1 and S2 remain closed, while the switches S3, S4, and S5 are open. This situation is then reversed during the peak maximum voltage (stored at C_s) "read" phase. S6 is used at the end of each period to reset shortly the pixel storage capacitor C_s. No additional signal amplification is in this case required.

The PDH circuit consists of a differential input stage (transistors M1 and M2), which together with the ideal current source I_{OTA}, the current mirror (M3 and M4), and the second stage of this OTA (transistors M1, M2, M3, M4, and M5 in Figure 3. 27(a)), constituted by M5 and coupled through a *Miller capacitor* C_M, work both, as the input peak sensing structure and the output buffer, respectively. As in the previous pixel configurations presented, the pixel storage capacitor C_s serves as an analog memory where the peak information is being stored. An additional PMOS transistor, M7, in a current mirror configuration with M6, acts as a C_s charging element in the peak detection phase and, also as a switch which allows the signal readout from the electrically isolated C_s. The OTA circuit is used as a simple comparator in the first, peak detection phase. When a detector output voltage peak arrives, enabled by switching S1 to ON (Figure 3. 27(b)), to the negative input (in^-) of the OTA (gate of the M1), and is higher than the held voltage of C_s connected to the positive input (in^+) of the OTA comparator (gate of M2) -close to zero after C_s was properly reset via S6-, it generates a sharp negative peak at the gate of M7, at least V_{th} (threshold voltage) below V_{DD} that switches M7 on and provides an I_d current to charge the storage capacitor C_s [DeG02]. When the incoming peak has reached its maximum value, and the voltage at in^+ results lower than the one at in^-, a sharp positive transition at the gate of M7 switches the transistor off. Since there is no

discharge path available for C_s, it retains the peak value of the incoming signal [DeG02].

Two factors appear to define the over-all circuit function: the OTA response speed and the precision of the voltage peak detection. At first, the response speed of the OTA and the current limitation, accomplished by the current mirror consisting of the transistors M6 and M7 was optimised. Actually, the addition of the M6 transistor enabled better precision of the peak detector, limiting the current that normally flows towards C_s in the peak detection phase, and represents, together with the addition of the second stage to the original OTA, the major difference when compared to the pixel configuration published in [Dur06, Dur07C, and Dur07S] as the first solution for a CI-PG pixel, and shown in Figure 3. 33.

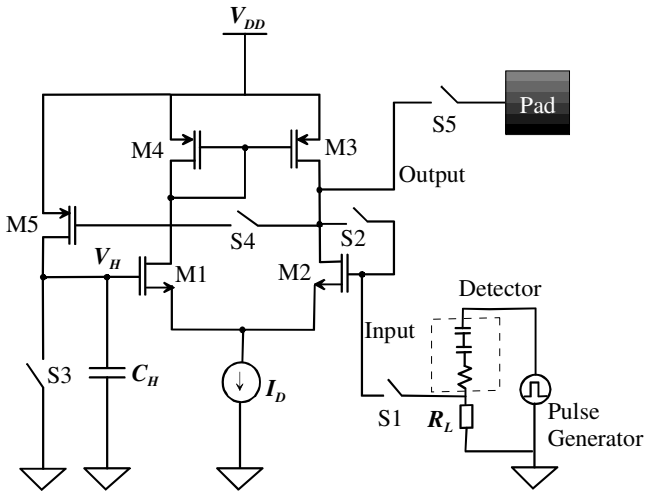


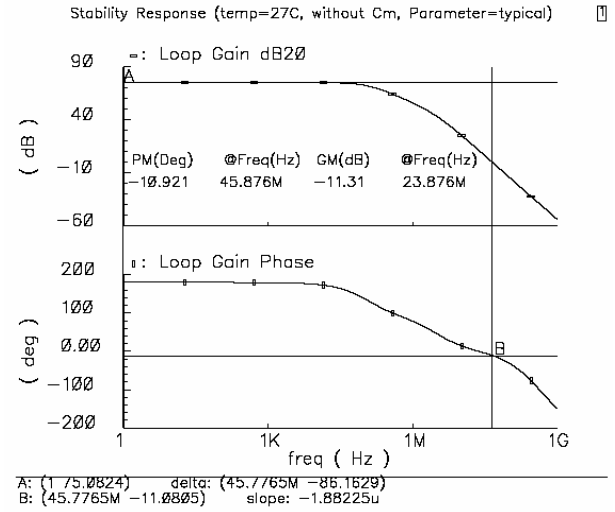
Figure 3. 33 – A simplified pixel configuration for the CI-PG pixel, which presented much higher precision in the peak detect-and-hold applications [Dur06, Dur07C, and Dur07S].

Incorporating an additional switch to disconnect the *Miller capacitance* C_M showed in Figure 3. 27(a) during the peak detection phase (phase margin: -10.9° as shown in Figure 3. 34), and connect it during the "read" phase (phase margin: 60.09°) brings speed improvement. The OTA circuit remains in this way unstable during the peak detection phase, and acquires stability in the peak "read" phase. The entire CI-PG pixel consumes 346.5μW of power.

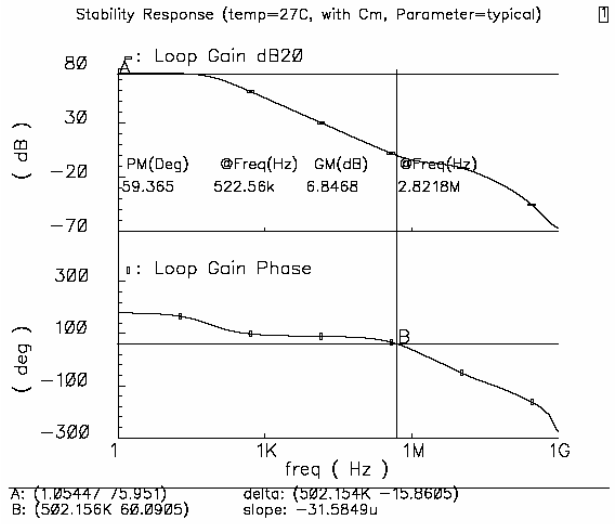
The CI-PG PDH circuit shown in Figure 3. 27(a) provides an error of 0.7% in its peak detection and hold tasks for readout voltage peaks generated using $T_{readout}$=1.4μs and a peak maximum of V_{max}=120mV, as it can be observed in Figure 3. 35 in the middle, where the *Cadence*® simulation results of the circuit are shown also for incoming peaks with V_{peak}=50mV (with an error of 1.5%), and finally V_{peak}=500mV (with an error of 6.06%). The upper transient response is obtained at the gate of M7 for each case, which shows the disruption of the C_s charging current after the peak has reached its maximum, while the lower curve shows the signal at the in^+ input of the OTA (Figure 3. 27(a)).

Following the experimental results obtained for the CI-PG pixel photodetectors shown in Figures 3. 29, and 3. 31, $T_{readout}$ of the incoming

readout voltage peaks was changed and new transient simulations of the PDH circuit were performed for each of the new values. Unfortunately, while for $T_{readout}$=200ns the error is 18%, and is getting worse as the $T_{readout}$ decreases, for $T_{readout}$=4.5ns it reaches 86%. The conclusion is that $T_{readout}$ should be around 2μs for acceptable output results. On the other hand, V_{peak} can also be increased by incrementing the voltage level via R_L.



(a)



(b)

Figure 3. 34 – (a) Frequency response of the OTA circuit used in the CI-PG shown in Figure 3. 26(c), without the Miller capacitance C_M. The phase margin (PM) of –10.9° shows that the two-stage OTA is not stable in the peak detection phase; (b) frequency response obtained for the CI-PG pixel OTA circuit with the Miller capacitance C_M. The phase margin (PM) of 60.09° indicates stability of the OTA operation in the peak "read" phase.

3.6.4 CI-PG Pixel for TOF 3-D CMOS Imaging

The TOF measurement process used in the reverse-biased *p-n* junction based pixels is repeated here, and the difference between the *n*-well output peaks is stored at the C_{Fx} capacitor, from which the distance to the target scene can be obtained as shown in Eq. (3. 36), incorporating an additional calibration constant $\boldsymbol{C}$.

As the photodetector requires in the best of cases 6.5ns for complete readout (see Figure 3. 29), it appears to be useful for TOF imaging. In order to be able to compare the CI-PG pixel with the three *n*-well PD based pixels, shown respectively in Figures 3. 13, 3. 16, and 3. 18, a (130×300)μm^2 CI-PG pixel is examined, layout of which can be found in Figure 3. 35, generated using *Cadence*® software. We incorporated in the pixel the circuit shown in Figure 3. 27, and have chosen R_L=2kΩ and C_s=5pF. The fill-factor obtained is of 61%, delivering a PG area of (191.2×125)μm^2.

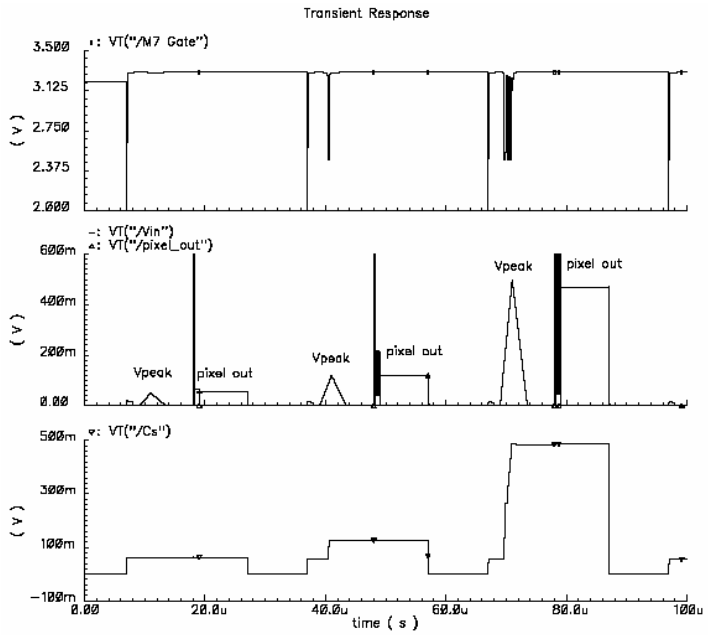


Figure 3. 35 – Simulated transient responses for the CI-PG pixel PDH circuit for the incoming readout voltage peaks generated with $T_{readout}$=1.4μs, and V_{peak} of respectively 50mV, 120mV, and 500mV.

For considered 1420W/m^2 of incoming irradiance (the excepted value for joint background illumination (solar constant) and the reflected laser pulse with λ=910nm) and T_{int}=120ns, the 0.3pC of collected charge would generate a voltage peak of 1.48mV, if $T_{readout}$=4ns and R_L=2kΩ are considered (Figure 3. 27). This makes the system inoperable, which leads to a conclusion that such a pixel configuration is unsuitable for TOF imaging as it was conceived in this text, although it remains an attractive alternative for 2-D low level radiation imaging (T_{int}≈20ms).

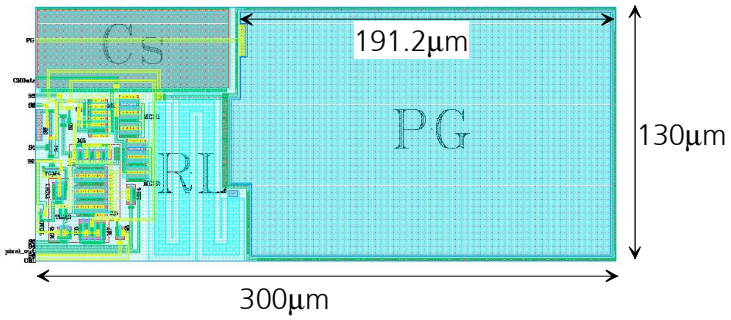


Figure 3. 36 - Layout developed using Cadence® software for a (130×300)μm^2 CI-PG pixel to be fabricated in the 0.5μm CMOS process.

Another possibility is to immediately integrate the entire output current peak at the C_s, using a similar system to the one depicted in Figure 3. 16. This would mean incorporating the CI-PG photodetector (left part in Figure 3. 27(a)) instead of the *n*-well PD and the RST transistor, to the circuit shown in Figure 3. 16, together with a suitable correction factor in Eq. (3. 36) that would consider the part of the signal defined by the $\sim 5 \cdot e^{-t/R_L C_{OX}}$ discharge time.

Of course, a higher substrate resistivity on which the entire CI-PG pixel could be fabricated, or even using a high-resistivity substrate on which the photodetector could be placed, and achieving an electrical connection between this photodetector (with huge SCR and extremely enhanced quantum efficiencies specially in the NIR) and a separated readout region where a standard CMOS process could be developed, would bring immense advantages and turn the whole concept of CI-PG pixels into a quite desirable imaging solution, as it will be explained and analysed in the next chapter.

4 CMOS Silicon-On-Insulator Technology: An Alternative for NIR Quantum Efficiency Enhanced CMOS Imaging

The camera-on-a-chip approach, *x-y* random pixel addressing, and photodetector output signal in-pixel processing possibilities are valuable CMOS imaging advantages over all other imaging technologies. Nevertheless, as it was discussed throughout the last two chapters, adapting the pixel and radiation detector designs to an already existing standard CMOS process is normally not an easy task. Highly doped substrates, low operation voltages, and fixed doping profiles in a CMOS process drastically reduce the possibilities of designing an optimal CMOS imager. The SOI technology offers an interesting solution for solving some of these problems, as it will be explained in the following pages.

4.2 Conception and Theoretical Analysis of the SOI Based CI-PG Pixel Detector with NIR Enhanced Quantum Efficiency

As it was just explained, a limited sensitivity of the photodetector structures analysed in the previous chapter, and specially PG, calls for photodetectors fabricated on higher resistivity substrates. Actually, when near-infra-red radiation impinges on the photodetector, it delivers weak photocurrents due to huge absorption lengths and the recombination processes inside the silicon bulk. Also because of its readout principle, for high-speed NIR imaging applications, such as for example TOF based 3-D imaging, a PG based pixels with internal signal amplification are highly desirable. Thus, a novel PG based pixel configuration is here proposed: the *SOI Charge-Injection Photogate*, that features separated detection and readout regions, fabricated using a CMOS *silicon-on-insulator* (SOI) based process.

The basic requirements for increased quantum efficiency -an advantage when it comes to low-level or near infrared radiation sources- are the increased capacity for charge storing and deeper potential wells created. The latter is achieved here by using the so called "local SOI" option of the *30V thin-film 1.0μm SOI* process available at the Fraunhofer IMS. The photodetector is in this solution placed on the higher resistivity (ρ=40Ω·cm) handle-wafer, while the readout circuitry is fabricated on the low-resistivity (ρ≈28mΩ·cm) 200nm thick silicon film, separated of the handle-wafer by a 600nm thick buried oxide layer as depicted in Figure 4. 1. The capacity and the depth of the SCR created at the

silicon-oxide interface, when low voltages are applied to a polysilicon gate electrode, are in this way increased. Moreover, this process was originally designed to meet extreme operation conditions and use voltages as high as 30V which definitely favours NIR enhanced quantum efficiency of any photodetector. Actually, the same concept can be applied to all the pixel configurations examined in Chapter 3, as all the four of them depend exclusively on an electrical connection (no charge-coupling principle can be applied) between the photoactive area and the pixel storage capacitor C_s, which enables the physical separation of the photoactive and readout regions.

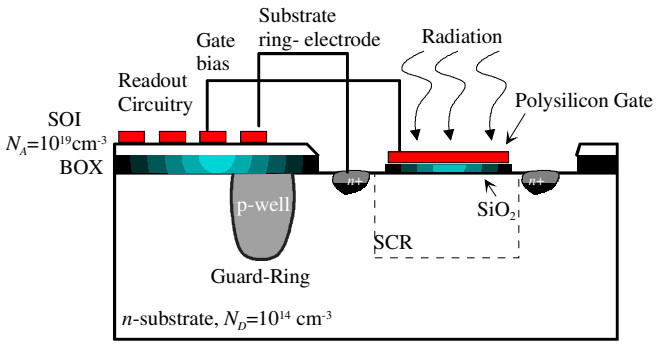


Figure 4. 1 - Schematic of the SOI CI-PG integrated pixel configuration, fabricated in the *30V thin-film SOI* process [Dur07C].

The *SOI CI-PG* pixel array proposed here consists of a large area (500x500µm^2) active pixels connected in an array, with separated photodetection and readout regions and fabricated using a local SOI based process available at the Fraunhofer IMS. The schematic representation of such an array is shown in Figure 4. 2. The basic readout scheme proposed in Chapter 3 for the CI-PG pixel configuration to be fabricated in the 0.5µm standard CMOS process is to be followed also in this application. Moreover, although the SOI CI-PG pixels require the existence of an extremely deep low-doped *p*-well for their integration in the photodetector array, here the first test structures were fabricated using directly the handle-wafer *n*-type silicon substrate, as for single photodetector applications. The idea is to show the basic functionality of this novel approach.

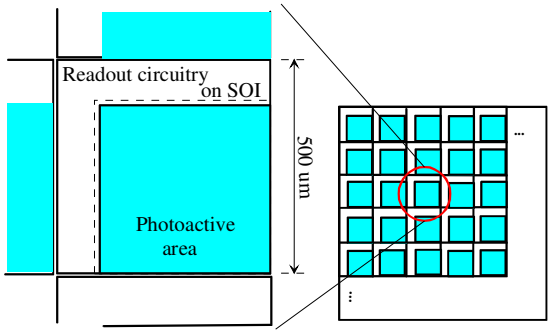


Figure 4. 2 - Schematic of the SOI CI-PG pixel array and single pixel distribution [Dur06].

As proposed and theoretically modelled in Chapter 3, the principle of "time-compression" parametric amplification, which also applies here, relies on the operation of a PG out of equilibrium. For the case of the SOI CI-PG, the PG is

at first driven into initial inversion to minimize the semiconductor-insulator interface effects applying a constant voltage offset, in the SOI proposal V_{GND}=-3V. Although this could generate image-lag effects, this concept of external generation of a "fat zero", borrowed from the CCD technology, is followed here as proposed in [Mal03]. The SOI CI-PG pixel photodetector was simulated using TCAD software tools, and the results obtained in form of a 2-D electrostatic-potential profile can be observed in Figure 4. 3, for the PG reverse-biased at V_{GND}=-3V, where W_{SCR}=4.2μm.

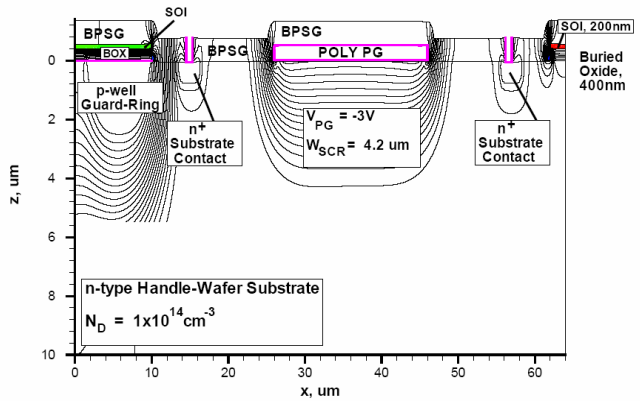


Figure 4. 3 - TCAD software electrostatic potential simulation of the photodetector, the PG and the *p*-well GR are biased at V_{inv}=-3V [Dur07C].

Starting from this equilibrium condition, a reverse-bias voltage pulse, U_{PG}=20V, is applied to the gate electrode exhibiting a rise time $T_{readout}$=10μs. The latter generates deep-depletion and creates a potential well (with SCR depth, W_{SCR}=12.57μm), where photogenerated charge is being stored during the pulse duration or T_{int}=20ms, as used in typical video applications (f=50Hz), under exposure to incoming radiation. The voltage pulse returns back to its original value in $T_{readout}$=10μs. During the voltage transition, no current can be sensed until T_{inj} is reached, as the partially filled potential well is retrieving, and only the SCR displacement current is being generated. At T_{inj}, the integrated charge is no longer attracted by the voltage applied to the gate electrode, and it is injected into the silicon substrate, as explained in detail in Chapter 3. The injection current can be sensed in the outer circuit through the substrate ring-electrode fabricated around the gate in a distance larger than the lateral SCR width from the detector (in Figure 4. 2, it is 20μm). The current peak, which reaches its maximum value at $T_{readout}$=10μs, decays exponentially depending on the oxide capacitance (here, C_{OX}=86.3nF/cm^2 for the oxide thickness d_{OX}=40nm) and the load resistor (R_L=1kΩ) used for signal sensing relaxation time T_{relax}≈700μs, as defined by Eq. (3. 75). After a certain reset period, the device is ready to receive the next signal peak.

The currents generated in the (500×500)μm^2 PGs, theoretically obtained using Eq. (2. 73) and incorporating the radiant flux dependent photocurrent element to it, for the charge integration period T_{int}=20ms under different radiant flux values of green light (λ=555nm) impinging radiation, as well as for the current flowing in dark conditions, are shown in Figure 4. 4 [Dur06]. Not measured directly, realistic values were chosen for the minority carrier lifetimes in

the SOI handle-wafer substrate; namely, generation time τ_g=500μs, and recombination time τ_p=10μs.

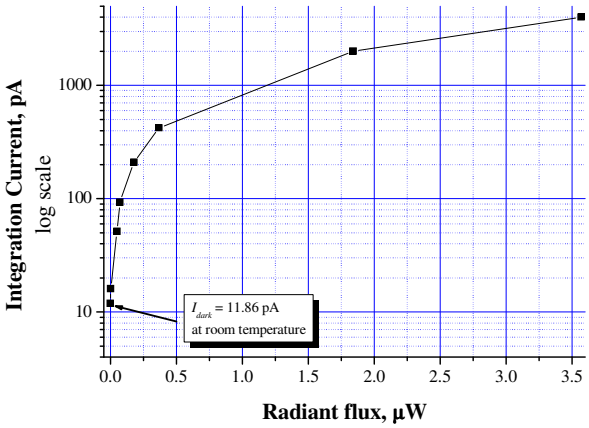


Figure 4. 4 – Charge storage current taking place during the 20ms integration time, considering τ_g=0.5ms, τ_p=10μs, N_D=1x10^{4}cm^{-3}, V_{GND}=-3V, U_{PG}=-20V, R_L=1kΩ, and different impinging green light (λ=555nm and absorption coefficient α=2x10^{4}cm^{-1}) radiation radiant fluxes, ranging from dark condition, 3.56nW (10lux or candle light [Bre99]), over 73.14nW (200lux or room-lighting [Bre99]), until 3.57μW (1x10^{4}lux or partially cloudy outdoors lighting conditions [Bre99]) [Dur06].

Moreover, and as it was explained in Chapter 2, the charge storing process is a dynamical one in which the SCR of a PG decreases its value with time causing the integration current also to decrease until the potential well generated at the oxide-silicon interface disappears completely, turning into an inversion layer. At this moment, the system is said to have reached equilibrium. The time required for the potential well to disappear was simulated using Eq. (2. 73), considering the operating conditions explained. The theoretically obtained curves for the photocurrents flowing in the PG in darkness, and under different radiant flux values of impinging green light radiation, until the second equilibrium condition is met, can be observed in Figure 4. 5.

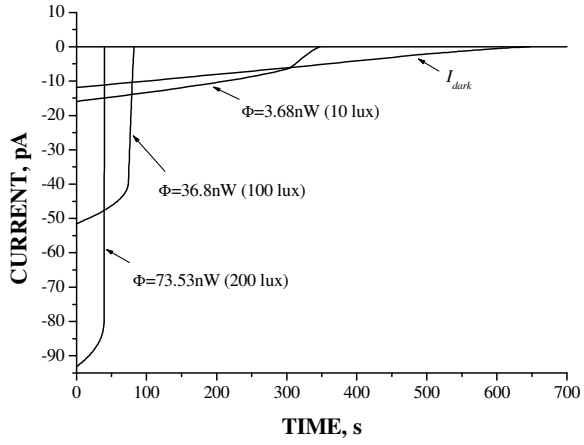


Figure 4. 5 – Currents flowing in the SOI CI-PG photodetector until the potential well created at the silicon-oxide interface disappears, in darkness and under 10lux, 100lux, and 200lux of impinging radiant flux (λ=555nm).

On the other hand, the detector output current peaks are mathematically obtained using Eq. (3. 75) for the same conditions already given here. They are created during the transition time, i.e. the fall time of the voltage pulse in transition from U_{pulse}=-20V towards U_{offset}=-3V, namely t_{tran}=10μs. The amount of charge accumulated in the potential well during the integration phase is obtained by integrating the current flowing from t=0 till t=T_{int}. The same value is then introduced into the mathematical model of the detector output current peak, Eq. (3. 75), considered for the case of the partially filled potential well.

Figure 4. 5 shows respectively both, the current integration and the photodetector output stages, for 0.18μW (500 lux) of green light (555nm) incoming radiant flux, as well as the results of the device operation in dark conditions. The time-compression parametric amplification factor, defined as the ratio of the detector output current peak and the average value of the current flowing during T_{int}=20ms, in this case reaches 2.27x10^6 or 127.13dB, and can be improved by reducing $T_{readout}$ to, as shown sufficient for the PDH circuit correct functioning in Chapter 3, for example, 1.4μs. This will be shown later on in this text.

The "time-compression" amplification factor exhibits a direct linear dependence on the T_{int} / $T_{readout}$ ratio [Mal03], and an inverse exponential dependence of the $R_L C_{OX}$ factor [Dur03]. It exhibits an inverse exponential dependence on the amount of charge accumulated in the potential well at the beginning of the photodetector output phase, i.e. the impinging radiant flux value for a fixed T_{int}/$T_{readout}$ ratio, as well. This dependence can be seen in Figure 4. 6 [Dur06].

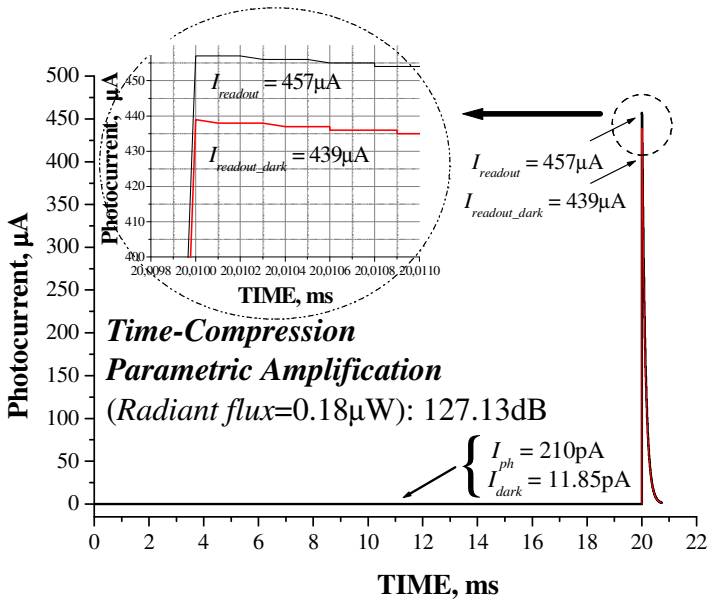


Figure 4. 6 - The charge integration (T_{int}=20ms) and the SOI CI-PG output ($T_{readout}$=10μs) phases, simulated together for both, the device operation under impinging 0.18μW radiant flux green light (λ=555nm) radiation, and under dark conditions. The amplification factor under irradiation is of 127.13dB [Dur06].

From Figure 4. 6, it can be concluded that the amplification is high for low amounts of stored charge (low levels of illumination) and is reduced exponentially as the values of the radiant flux (the amount of charge stored during T_{int}) increase. This particular characteristic opens a wide range of possibilities in what intra-scene dynamic range requirements are concerned. The CMOS imaging active pixel sensor working principle which allows independent *x-y* pixel addressing in a matrix, delivers -when combined with the latter characteristic- high dynamic range values.

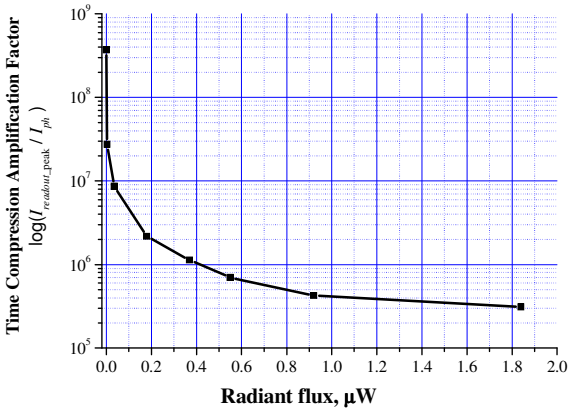


Figure 4. 7 - The inverse exponential dependence of the "time-compression" parametric amplification on the value of incoming radiant flux, for fixed $T_{int}/T_{readout}$ ratio (2000) and the $R_L C_{OX}$ factor (2.16x10^{-7}) [Dur06].

As it was already explained, the PG output current peak is measured as a voltage drop across the load resistor R_L=1kΩ, shown in Figure 4. 1. Using Eq. (3. 75), and all the operating conditions enlisted so far, namely N_D=1×10^{14}cm^{-3}, τ_g=500μs, τ_p=10μs, V_{GND}=-3V, U_{PG}=-20V, R_L=1kΩ, A_{PG}=(500×500)μm^2, and T=300K, the voltage signals generated under different impinging radiant fluxes are transferred to the low-noise peak detect and hold (PDH) stage, and shown in Figure 4. 7 [Dur06].

4.2 Experimental Results Obtained From SOI CI-PG Pixel Photodetectors

As already explained, the standard CMOS SOI based process available at the Fraunhofer IMS offers a higher-resistivity (ρ=40Ω·cm) handle-wafer, coupled to a 120nm (after processing) thick low-resistivity (ρ≈28mΩ·cm) SOI film, separated by a 400nm thick buried oxide (BOX). It offers 40nm thick gate oxides covered by a 520nm thick polysilicon gates, and a possibility of using up to 30V voltage biasing.

The SOI CI-PG photodetector structures were fabricated in the *30V thin-film CMOS SOI* process, consisting of (653.2×625.5)μm^2 big PG photoactive areas, surrounded by a 4μm thick substrate n^+ (N_D=8×10^{19}cm^{-3}) ring-electrode located at a distance of 20μm from each edge of the square PG, a distance aimed to maintain the substrate electrodes at all times outside the PG SCR, which when biased at V_{int}=-15V reaches 12.57μm, and at V_{inv}=-3V it reaches

4.2μm. The final layout generated using *Cadence*® software can be observed In Figure 4. 9 [Dur07C].

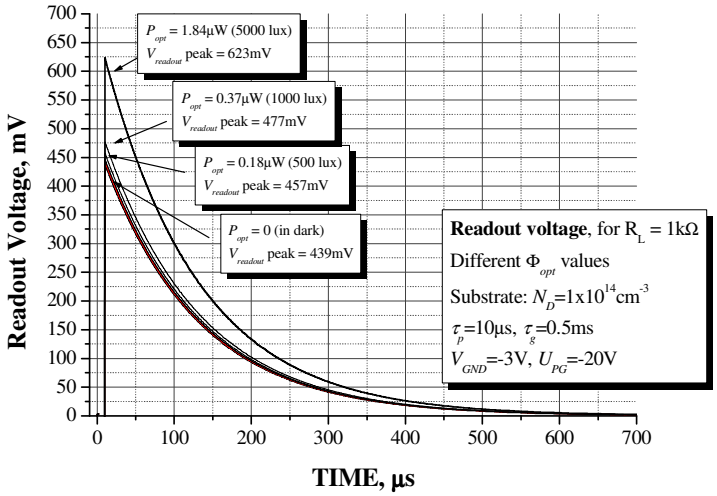


Figure 4. 8 - Different detector output voltage signals to be delivered to the pixel readout stage, for R_L=1kΩ, N_D=1x10^{14}cm^{-3}, τ_p=10μs, τ_g=0.5ms, V_{GND}=-3V, U_{PG}=-20V, and different values of the impinging radiant flux, for incoming radiation wavelength λ=555nm and absorption coefficient in silicon, α=2x10^{4}cm^{-1} [Dur06].

Figure 4. 10 [Dur07S] shows the wavelength dependent optical sensitivity (in A/W) and quantum efficiency curves obtained for the 4 PG structures fabricated on the handle-wafer substrate, for λ=450nm-1100nm, using the measurement station described in Appendix B of this work. Their quantum efficiency values were compared to those obtained from a PG structure fabricated in the 0.5μm standard CMOS process, shown originally in Figure 2. 42. Here, *lock-in* amplifier based output voltage measurements were performed, while illuminating the photodetectors by a 10Hz modulated 250W light source followed by a monochromator.

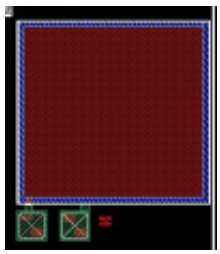
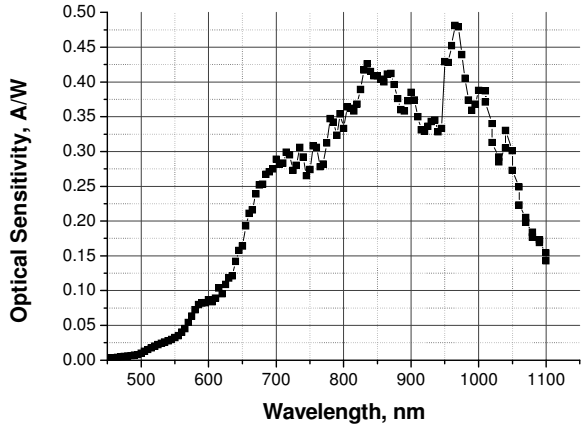
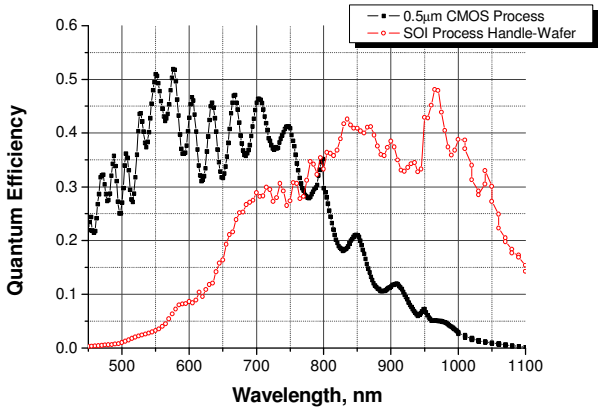


Figure 4. 9 – The layout generated using *Cadence*® software tools for the (653.2×625.5)μm^2 big *p*-type PG photoactive area to be used in SOI CI-PG pixels [Dur07C].

Both structures were reverse biased at 3.3V. As expected, the much lower resistivity of the handle-wafer, i.e. much deeper SCR, produces a highly enhanced quantum efficiency (QE) of the SOI based photodetector in the NIR part of the spectra, when compared to its similar fabricated in 0.5μm CMOS process. The loss of QE in the ultra-violet and visible parts of the spectra for the SOI based PGs is due to the reduced transmittance of the polysilicon gate, and the use of a silicon nitride protection layer in the SOI process.



(a)



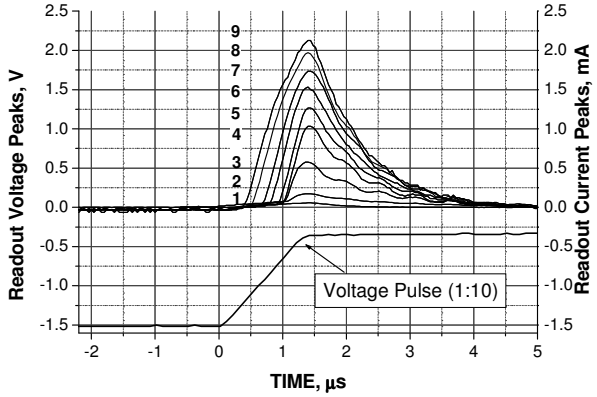
(b)

Figure 4. 10 – (a) Optical sensitivity in A/W for the SOI based PG structures; (b) comparison of the experimentally obtained quantum efficiencies for the PG photodetector structures fabricated in the *30V thin-film CMOS SOI* and the 0.5µm standard CMOS processes, respectively [Dur07S].

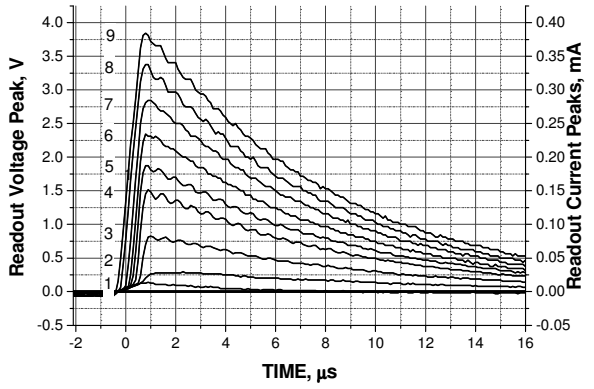
On the other hand, to test the charge-injection readout principle, the SOI CI-PG detectors were illuminated using the *idLUX Color Illuminator*, with visible red light (λ=625nm, and light penetration depth: 1/α=~2µm) irradiation, at different irradiance values (between 20 and 160 µW/cm^2). A voltage step was simultaneously applied at the PG, starting at V_{GND}=-3V and creating a deep-depletion SCR with U_{PG}=-15V during the T_{int}=20ms integration time, then switching back to V_{GND} in a transition time $T_{readout}$=1.4µs.

Knowing that the amplification coefficient is inversely proportional to the value of R_L, and also to that of $T_{readout}$, two different load resistors were used for the signal readout, namely R_L=1kΩ and R_L=10kΩ, although maintaining $T_{readout}$ constant. The experimental results obtained can be found in Figure 4. 11 [Dur07C]. The amplification factors obtained as ratios between the induced photocurrents and the readout current peaks, for the conditions described in Figure 4. 11, can be observed in Figure 4. 12 [Dur07C].

As expected, a higher current amplification factor (3.9×10^4) was obtained for R_L=1kΩ, at impinging radiation of 60μW/cm^2, 6.9 times higher than the one obtained for the same conditions using R_L=10kΩ. Nevertheless, following the *Ohm's law*, when considering the output voltage signal, the voltage readout peak measured at R_L=1kΩ was 2.1V for 160μW/cm^2 irradiance, while at R_L=10kΩ, it was 3.8V.



(a)



(b)

Figure 4. 11 - (a) Readout voltage peaks (left), obtained as a voltage drop at the load resistor R_L=1kΩ, and the readout current peaks (right) for the same case, delivered by the SOI CI-PG pixel detector when illuminated by visible red radiation (λ=625nm), at: 1) 0μW/cm^2, 2) 20μW/cm^2, 3) 40μW/cm^2, 4) 60μW/cm^2, 5) 80 μW/cm^2, 6) 100μW/cm^2, 7) 120μW/cm^2, 8) 140μW/cm^2, and 9) 160μW/cm^2. The voltage pulse applied (V_{inv}=-3V, V_{int}=-15V), for $T_{readout}$=1.4μs and T_{int}=20ms, can be observed below in a 1:10 scale [Dur07C]; (b) the results obtained for the conditions identical to those shown in (a), just using R_L=10kΩ, instead of R_L=1kΩ [Dur07C].

Moreover, the $R_L C_{OX}$ factor, for C_{OX} the oxide capacitance of the PG, affecting the readout relaxation time is of course, directly proportional to the R_L value, which affects the pixel response velocity, being the configuration using R_L=10kΩ, more than 5 times slower.

Finally, measuring the output voltage peaks of the SOI CI-PG photodetectors (for R_L=1kΩ), while illuminating them by a 1000W Xe/Hg lamp, followed by a monochromator (part of the measuring station described in

Appendix A), the wavelength dependent spectral responsivity curve (in V/μJ/cm^2) is obtained, shown in Figure 4. 13, for impinging irradiations in the range between from 450nm to 1100nm wavelengths.

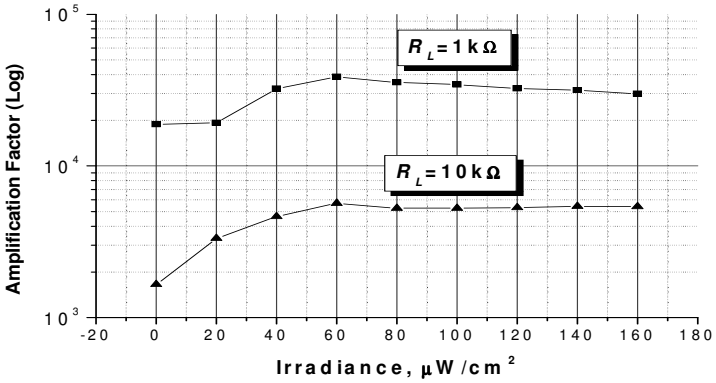


Figure 4. 12 - Internal time-compression amplification factors obtained measuring the SOI CI-PG pixel detector output current peaks and the induced photocurrents, for the conditions shown in Figure 4. 11 [Dur07C].

Considering the readout current peaks obtained and shown in Figure 4. 11, if the part of the curve between the beginning of the transition time in which the PG bias is changing from U_{PG} towards V_{GND} (0 seconds in Figure 4. 11(a)) until it reaches $T_{readout}$=1.4μs is integrated for $T_{readout}$, the amount of charge flowing in the readout stage can be obtained. Then, with this value, it is easy to obtain the amount of induced photocurrent that should be flowing in the charge integration stage (during T_{int}=20ms) if there would not exist any losses in the charge injection process. Finally, knowing the amount of photon flux impinging on the photoactive area, the experimental quantum efficiency can be obtained for the charge injection process.

In this case, if the experimental charge-injection quantum efficiency is compared to the quantum efficiency obtained for the PG photodetector alone, shown in Figure 4. 10, it appears to be strongly related the amount of photon flux impinging on the PG. Here, the quantum efficiency obtained from the SOI CI-PG detector, if illuminated with 20μW/cm^2 of red light irradiation (λ=625nm), represent the 44.6% of the quantum efficiency obtained for the PG alone for the same impinging radiation. On the other hand, for 160μW/cm^2 of photon flux, the final quantum efficiency represents the 88.05% of the PG original one. Following this procedure, the time-compression charge injection quantum efficiency is obtained for the impinging radiation in the range from 450nm to 1100nm, and compared to the quantum efficiency obtained for the PG alone, before the charge injection process. The results can be observed in Figure 4. 13 [Dur07C].

It has to be stressed here that the $R_L C_{OX}$ relaxation time obtained in Figure 4. 11 can be drastically reduced if a smaller photoactive area APG is chosen (here A_{PG}=(653.2×625.5)μm^2). For example, for the case of A_{PG}=2.4×10^{-4} cm^2 (Figure 3. 28), the SOI CI-PG relaxation time is of only 103.1ns.

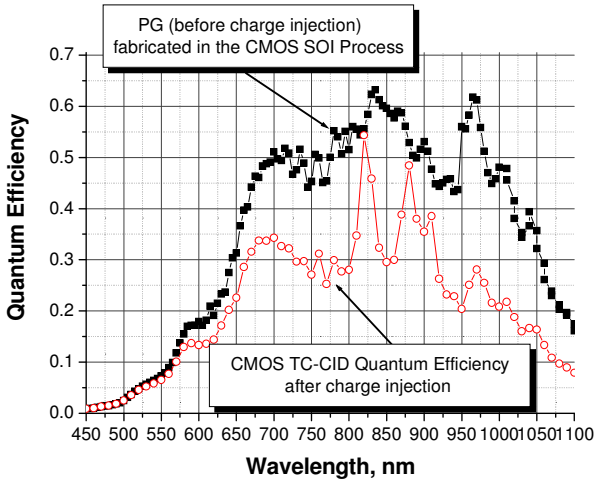


Figure 4. 13 - Comparison of quantum efficiencies before and after the charge injection process in a SOI CI-PG fabricated in *30V thin-film CMOS SOI* process. The charge injection efficiency is strongly dependent on the photon flux of the impinging radiation and oscilates between 45% and 90%.

As shown so far, the silicon-on-insulator technology offers a vast range of possibilities for different CMOS imaging applications in both, 2-D and 3-D. On the other hand, it also offers several solutions for direct soft *X*-ray detection, if no scintillation material is to be used, as it is described in the following chapter.

5 SOI Technology Used in *X*-Ray Imaging Tasks

By the end of 2005, the Fraunhofer IMS was contacted by a group of scientists working on a technical design for a TESLA *X*-ray *free-electron laser* (XFEL) laboratory, at the *German Electronic Synchrotron* (DESY) in Hamburg, to propose a solution for a set of imaging detectors which could be used together with the XFEL facility in different user experiments. The TESLA XFEL laboratory comprises an injector, a superconducting 20GeV electron linear accelerator, an electron beam distribution switchyard, five undulators for FEL and synchrotron radiation, and an experimental hall with ten experiments. XFEL radiation of unprecedented peak brilliance and full transverse coherence is provided in the wavelength range of 0.1nm to 6.4nm (corresponding to a photon energy range of 0.2 to 12.4 keV) with the option to reach a wavelength of 0.086nm. The pulse duration is of the order of 100fs. The laser-like FEL radiation is supposed to provide unique research possibilities for condensed matter physics, chemistry, material science, and structural biology.

A theoretical solution was proposed, which will be analysed briefly in this chapter. One of the main difficulties, beside proving the immunity of the system to *X*-ray hard radiation, was the high frequency the imager should achieve, namely 5MHz for 1 million (1k×1k) pixels connected in an array. This goal was never achieved, but an alternative solution finally accepted, based on JFET silicon drift detectors [Gat83, Gat84, Gat89, Cas98, Cas06], was close enough. On the other hand, as the solution proposed could be applied to *X*-ray medical or dental radiography applications (radiation photon energy between 15keV and 30keV), it was decided here to explain the photodetector proposed and to investigate its performance under impinging hard-radiation.

5.1 XFEL Project Description and Detector Specifications

The unique properties of X-ray radiation to be generated by *Free Electron Lasers* such as the XFEL in Hamburg and the LCLS in Stanford impose an unprecedented combination of requirements on *X*-ray detection systems such as multi-element detection, high spatial resolution, high framing rates, high quantum efficiency, high dynamic range and low noise. Such detectors do not exist today but are of central importance for experiments employing free electron laser sources. An appropriate detector development program is, therefore, mandatory.

A subset of the most relevant XFEL source parameters is listed in Table 5. 1. A sketch of the required timing is given in Figure 5. 1. The length of a macro-bunch (MB) is 650 microseconds containing a maximum number of 3250

bunches, yielding a minimum bunch spacing of 200ns. The default macro-bunch repetition rate is 10Hz. An increase to 20-30Hz seems technically feasible while maintaining the same number of bunches per second. The LCLS repetition rate is 120Hz with one bunch per macro-bunch. Longer term upgrades could involve a dc-like bunch-structure with ≥10000 equally separated bunches/s. For further information we refer to [XFEL].

Table 5. 1

Parameter	*Data*
Photon energy	3 up to 15 keV (0.826 Å <λ< 4.13Å)
Photon per bunch	10^{12}
Divergence	< 1 up to few 10 μrad
Source appearance	~ 100 μm (diffraction limited)
Bandwidth	~ 0.1 %
Pulse duration	100 – 300 fs (probably decreasing)
Repetition rate	Macro-Bunch (MB): 10 (up to 120) Hz single bunches within MB: < 5 MHz

Three prominent classes of experiments that require 2-D detection schemes have been identified:

i) (Time resolved) Pump-Probe Experiments
ii) Imaging Experiments
iii) Photon Correlation Spectroscopy Experiments.

(i) A sample is promoted to a "pumped" state by a pump pulse (e.g. a visible laser, magnetic or electric field, XFEL or other pulse) and analysed after time Δt with an XFEL bunch. Samples might comprise single crystals, powders, liquids and geometries might span from small (SAXS) to large Q scattering. The detection of the scattered signal might need very high spatial resolution (*Bragg* peaks in a single crystal) and a very high dynamic range (e.g. SAXS). It is conceivable that experiments require records of as much as 3250 pump-probe events per macro-bunch.

ii) The sample is illuminated by the coherent XFEL beam and images are recorded in either the near-field (phase-contrast) or the far-field (speckle-imaging/lensless imaging). The so-called "single molecule diffraction" involves the recording of speckle patterns in the far field whereby phase retrieval by "oversampling" requires very fine detector resolution while the achievable resolution is determined by the maximum accessible momentum transfer (requiring a large detector). A combination of 2 detectors for the simultaneous recording of large and small Q images has been discussed.

(iii) Photon correlation spectroscopy analyses the temporal changes in a speckle pattern that are related to the sample's equilibrium or non-equilibrium dynamics. The method operates in the far-field and takes advantage of the coherence properties of the beam. Data are taken in either sequential mode (with the accessible time windows determined by the time structure of the machine), in "split-pulse" mode giving access to fast (ps-ns) dynamics (and requiring a

delay-line device) or in "pump-probe" mode requiring a pump pulse. Experiments want to take advantage of as many bunches as possible.

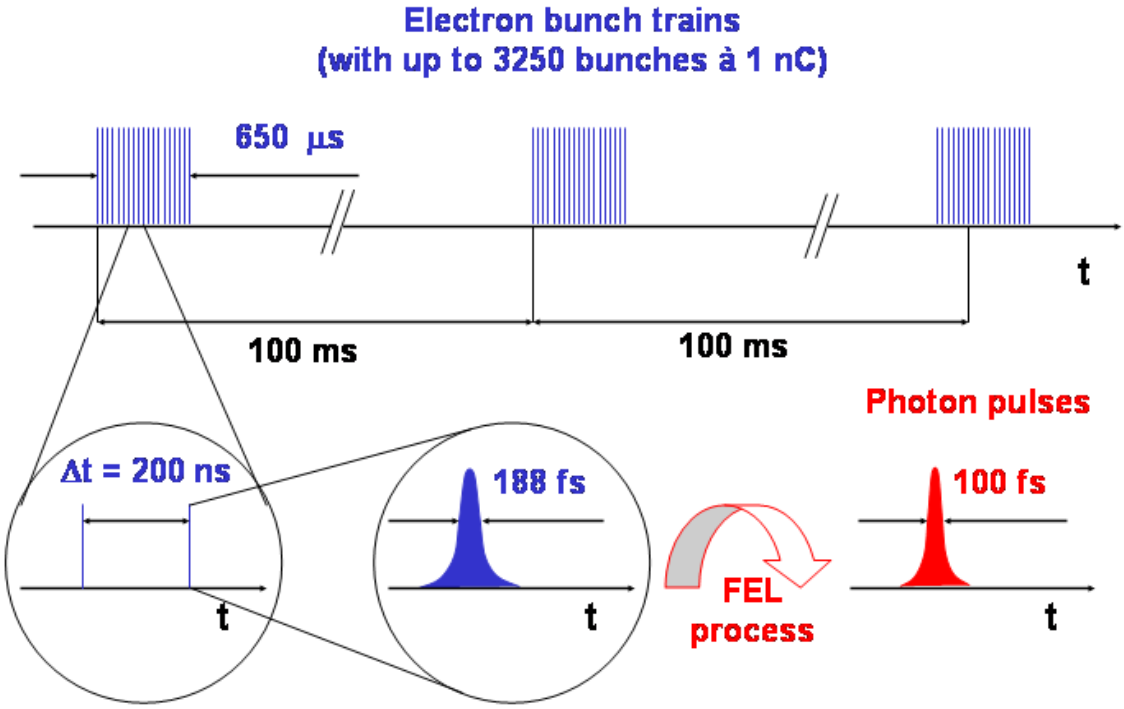


Figure 5. 1 - Schematic representation of the XFEL timing.

Detector Specifications

Requirements are distinguished between "Must" and "Nice to have" features. It was assumed that the systems should be capable of operating also at LCLS, thus requiring 120Hz timing. The ≥10kHz "Nice to have" request refers to an eventual longer term dc upgrade of the XFEL machine.

COMMON:	MUST	NICE TO HAVE
Single photon resolution	yes	-
Photon energy range [keV] [1)]	8-12	3 - 15
Quantum efficiency	>0.8	1
Radiation Hardness	yes	-
Harmonics Discrimination	no	yes
Number of Pixels	1k x 1k	2k x 2k
Need for tiling	yes	-
Preprocessing (hit finding algorithm, autocorrelator,..)	no	yes
[1)] operation at the XFEL fundamental		
DETECTOR I (pump-probe)		
Pixel Size [µm]	≤ 100	50
Vacuum Compatibility	no	yes
Signal rate/pixel/bunch	up to 10e4	up to 10e5

Timing	10 Hz (bunch train)	30Hz (bunch train)
	5 MHZ during 0.65 ms	-
	120 Hz (single bunch)	≤10 kHz
DETECTOR II (imaging)		
Pixel Size [μm]	30	< 30
Vacuum Compatibility	yes	-
Signal rate/pixel/bunch	up to 10e4	up to 10e5
Timing	10Hz (bunch train)	30Hz (bunch train)
	-	5MHz during 0.65ms
	120 Hz (single bunch)	≤10 kHz
DETECTOR III (XPCS)		
Pixel Size [μm]	50-75	≤50
Vacuum Compatibility	no	yes
Signal rate/pixel/bunch	few up to 100	up to 1000
Timing	10 Hz (bunch train)	30Hz (bunch train)
	5 MHZ during 0.65 ms	-
	120 Hz (single bunch)	≤10 kHz

Problem Analysis and Proposed Solution

In order to meet the specifications required at the XFEL facility, we propose a 2-D *X*-ray detector fabricated in SOI technology (with the possibility of local SOI, to be able to reach the handle-wafer substrate) as illustrated in Figure 5. 2. This will enable us to process on-chip CMOS integrated detector and readout circuitry parts, and will provide radiation-hard readout circuitry fabricated on the thin SOI layer. The only modification to the standard *30V thin-film SOI* process available at the Fraunhofer IMS required, is the use of a high-resistivity handle-wafer instead of the normally used one with N_D=3×10^{14}cm^{-3}.

As offered by SOITEC [SOI], the *high-resistivity UNIBOND 200mm* standard wafer (obtained using the *Czochralski* (Cz) growing method) which is to be used in this solution presents the specifications enlisted in Table 5. 2.

Table 5. 2

- Handle-wafer growing method: *Cz*-Si;
- Wafer diameter, *d*=200mm;
- Handle-wafer thickness d_{HW}=725μm, with the possibility of thinning to d_{HW}=500μm;
- the SOI layer thickness is d_{SOI}=200nm (final thickness 120nm), compatible with in-house SOI-CMOS process fabrication;
- Buried oxide (BOX) layer thickness d_{BOX}=400nm;
- Handle-wafer concentration (not doped): n^-=N_D=4.3×10^{12}cm^{-3} (ρ_{HW}>1kΩ·cm);
- SOI *n*-type layer concentration: n_{SOI}=1.96×10^{14}cm^{-3} (compatible with in-house SOI process fabrication n_{SOI}=1×10^{14}cm^{-3});
- Photodiode p^+ diffusion concentration: p^+=N_A= ~2×10^{16}cm^{-3}, and depth d_{p+}=0.5μm.

The existing *30V thin-film SOI* process available at the Fraunhofer IMS is absolutely compatible with the wafer specifications above mentioned. It possesses the possibility of local SOI, and voltages so high as 600V can be used with it (using special design criteria).

The detector part consists in this case of the fully depleted [Nie05], high-resistivity (ρ>1kΩ·cm), Cz-Si handle-wafer, which for energies E_{ph}≈15keV should not show deterioration effects, as reported in [Tuo03] for proton energies (E_{ph}>10MeV), with wafer thickness d_{HW}=500μm. The cross-section of the proposed 2-D imaging detector can be observed in Figure 5. 2.

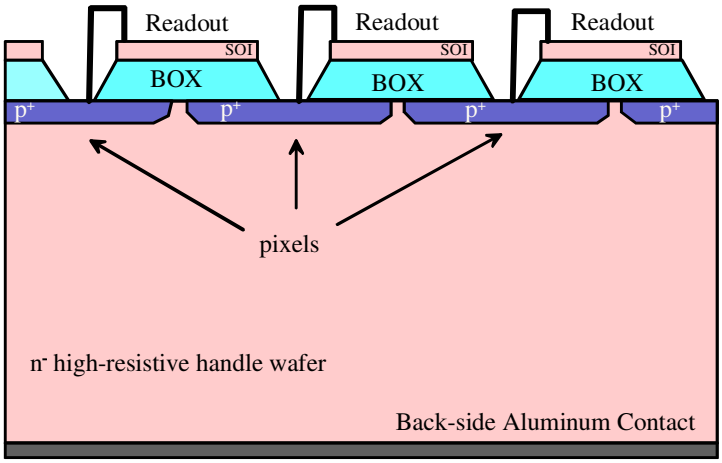


Figure 5. 2 - *Wafer-Bonding* SOI technology based, fully-depleted handle-wafer *X*-ray detector.

For the case of the proposed photodetector array shown in Figure 5. 2, a positive bias-voltage V_{bias} is applied to the back-side contact, while the *p*+ PD contacts remain grounded during T_{int}. The value of V_{bias} required to completely deplete the handle-wafer, d_{HW}=500μm, can be obtained through Eq. (5. 1).

$$V_{bias} = \left\{ \left[\frac{d_{HW}\left(N_D + N_A\right)}{N_A} \right]^2 \frac{qN_D N_A}{2\varepsilon_0 \varepsilon_{Si}\left(N_D + N_A\right)} \right\} - V_{bi} \qquad (5.\ 1)$$

Nevertheless, as the fabrication of the proposed photodetector should follow the *30V thin-film SOI* process flow-chart, the process simulation was first performed, using TCAD software tools, in order to obtain the exact value of the p^+ PD doping concentrations after the standard process PMOS *source-drain* implantation step is performed on the high-resistivity handle-wafer and partially through the joint SOI thin film and BOX layers. The results of this simulation can be observed in Figure 5. 2, according to which the concentration of acceptors in the p^+ pixel regions is in average N_A=1×10^{19}cm^{-3}.

For the fully-depleted handle-wafer photodetector proposed and depicted in Figure 5. 2, where the concentration of donors within the handle-wafer is N_D=4.3×10^{12}cm^{-3}, concentration of acceptors in the p^+ layer is N_A=1×10^{19}cm^{-3}, and the built-in voltage $V_{bi} = \frac{k_B T}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right) = 0.698V$, the bias voltage required

to completely deplete the handle-wafer is $V_{bias}(d_{HW}=500\mu m) \geq$ 815.9V. Further thinning reduces this value to below 600V.

The specific capacitance delivered by each pixel of such a detector, based on an reverse-biased *p-n* junction, can be calculated using Eq. (5. 2), and is C_j=2.1×10^{-11}F/cm^2. Depending on the respective photodetector (pixel) area enlisted in XFEL detector specifications, the capacitance values for each of the three detector applications can be respectively observed in Table 5. 3.

$$C_j = \sqrt{\frac{q\varepsilon_0\varepsilon_{Si}N_D}{2(V_{bi}+V_{bias})}} \qquad (5.\ 2)$$

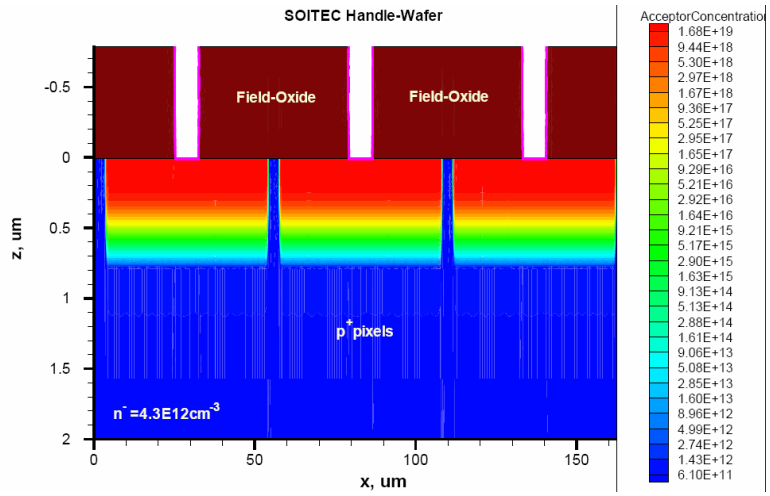


Figure 5. 3 - Results of TCAD software based simulation for the SOITEC high-resistivity wafer used in the *30V Thin-Film SOI* process, for the PMOS transistor *drain/source* standard process implantation step applied to the handle-wafer.

Table 5. 3

Detectors	Pixel area, cm^2	Specific Capacitance, F/cm^2	Pixel Capacitance, fF
Detector 1, Pump-probe Experiments	1×10^{-4}	2.1×10^{-11}	2.1
Detector 2, Imaging	9×10^{-6}	2.1×10^{-11}	0.189
Detector 3, Photon Correlation Spectroscopy	25×10^{-6}	2.1×10^{-11}	0.525

5.3 Quantum Efficiency Considerations

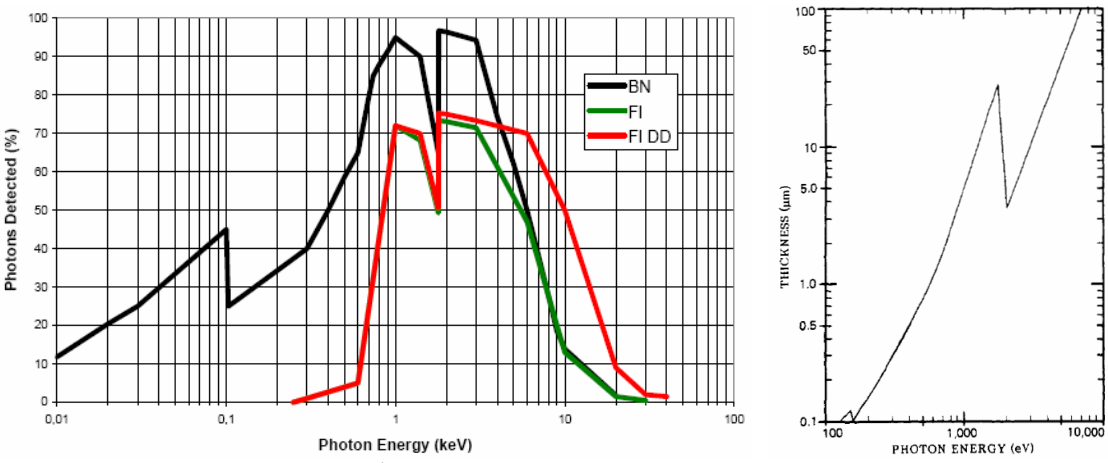
Silicon (Z=14, ρ_{ch}=2.33g/cm^3) is highly effective as an absorber of *X*-rays in the energy range E_{ph}=(3.5-20)keV. For these energies, neither *Compton* scattering (generation of a secondary *X*-ray inside the target material with lower energy, i.e. longer wavelength than the original incident *X*-ray) nor electron/positron pair generation are significant effects in silicon detectors, and

radiation is absorbed predominantly by photoelectric capture (Einstein, 1905) in bulk silicon [Wes99]. *X*-ray photons interacting with the silicon lattice generate secondary electron clouds, with the number of electrons in the cloud being proportional to the photon energy [Pri03]. Spatial resolution (related to the accuracy with which an *X*-ray event position can be measured) and the spectral one (which pertains to the accuracy with which the energy of an *X*-ray event can be determined) are both, interrelated critical parameters when considering *X*-ray imagers.

The absorption of *X*-rays in silicon occurs with the release of an electron-hole pair for each (in average) E_{ehp}=3.62eV [Reh04] at room temperature, or E_{ehp}=3.72eV at T=80K, of incoming photon energy E_{ph}. The latter is defined by Eq. (5. 3), where $\overline{Q}$ is the average amount of charge.

$$\overline{Q} = q\left(\frac{E_{ph}}{E_{ehp}}\right) \tag{5. 3}$$

The probability that an *X*-ray photon will be absorbed in a detector is directly related to the energy of the incident photon, as it can be observed in Figure 5. 4(a), for the case of CCD: the *quantum efficiency graph* provided by *Andor Technology* in [And02] for back-illuminated (BN), front-illuminated (FI), and front-illuminated deep-depletion (FI DD) CCDs. High energy X-rays (E_{ph}>10keV) have a low absorption cross-section in silicon, so that most photons will pass through the silicon lattice undetected [Wad84]. According to Figure 5. 4(b) [Wad84], in order to assure more than 90% of probability of absorption of an impinging *X*-ray, e.g. for energies in between E_{ph}=3keV and E_{ph}=15 keV, the depth of the photo-active region (SCR depth or W_{SCR}) should be 10μm to more than 12mm, respectively. The abrupt features occurring near 0.17keV and 1.8keV, observed in figure 5. 4(b), are produced by silicon absorption edges [Wad84].



(a) (b)

Figure 5. 4 - (a) Quantum efficiency curves for back-illuminated (BN), front-illuminated (FI), and front-illuminated deep-depletion (FI DD) CCDs [And02]; (b) Thickness of silicon required for 90% probability of photon absorption as a function of photon energy [Wad84].

Based on the so called *Absorption (Beer's) law* (the number of photons interacting with the material decays exponentially with the depth in the silicon, $I(z)=I_0e^{-\alpha z}=I_0e^{-\alpha' \rho z}$, where α is the absorption coefficient (cm^{-1}), α' is the mass absorption coefficient (cm^2g^{-1}), ρ_{ch} is the material density ($g\text{-}cm^{-1}$), and z is the axis of propagation or distance travelled by the radiation through the material (cm), it is possible to determine the characteristic absorption length L_{abs}, for different amounts of the impinging photon energies. The mass absorption coefficient α' is proportional to λ^3 (the cube of the incoming *X*-ray wavelength λ) [Wes99]. The wavelength is related to energy according to Eq. (5. 4), for λ in Å and E_{ph} in keV.

$$\lambda = \frac{E_{ph}}{12.398} \tag{5. 4}$$

According to the data experimentally obtained and published in [Hen93], the characteristic absorption length in silicon for an *X*-ray (if it is absorbed) with E_{ph}=3keV is L_{abs}=4.38μm, for E_{ph}=8keV it is L_{abs}=69.62μm, for E_{ph}=12keV it is L_{abs}=228.7μm and, finally, for E_{ph}=15keV it is L_{abs}=442.6μm. In conclusion, if high detection efficiency is desired for *X*-rays with energies in the range from E_{ph}=3keV to E_{ph}=15keV (XFEL), then an at least 500μm thick silicon wafer should be used to assure that all the *X*-rays which present absorption are to be completely absorbed.

The problem is that not every *X*-ray generates exactly the same average number of ehp. For every event, a *Gaussian* can be fit to the measured distribution of charge. The *full width at half maximum* (FWHM) of such a *Gaussian* gives the energy resolution (variance) σ_E of the device, for impinging photons of energy E_{ph}, expressed as Eq. (5. 5), where N_r is the amount of readout noise in silicon, and F is the so called *Fano factor*.

$$\sigma_E = 2.355E_{ehp}\sqrt{\frac{FE_{ph}}{E_{ehp}} + N_r^2} \tag{5. 5}$$

This energy resolution σ_E is determined by the *Fano noise*, the fundamental statistical fluctuation in the photoelectron count [Bur97], and is the best that can be done with the so called room-temperature detectors. The fundamentally possible X-ray energy resolution to be achieved, is plotted in Figure 5. 5 [Sel04] for different impinging *X*-ray energy values. The limit at 10keV of incoming radiation is 143eV FWHM, for example. Drift detectors [Gat89] have achieved good resolution down to 500eV and below.

For further understanding, not all the energy of the incoming radiation is spent in breaking the covalent bonds inside the silicon crystalline grid (the average energy for creating an ehp in silicon is E_{ehp}=3.65eV at room temperature, although the forbidden bandgap value is E_g=1.115eV). Some of it is ultimately released to the lattice in form of phonons. But, the amount of the energy released for each of these mechanisms changes. U. Fano discovered in

1946 that the generation of ehp by an *X*-ray is not a series of independent events, and cannot be calculated by simple *Poisson* statistics (approximated by *Gaussian statistics* for reasonably large counts) [Lun95]. Thus, a factor called *Fano factor*, *F*, has to be introduced to modify the expression for obtaining both, the energy resolution for determining the energy of each impinging *X*-ray, and the variance in the number of photogenerated ehp σ_Q, which can be calculated following Eq. (5. 6). This variance follows a *Gaussian* distribution with root mean square (rms). It would be otherwise most misfortunate, as the *Fano factor* increases the resolution limited by intrinsic quantum statistics [Lun95] represented as a perfect *Poisson* relation. In other words, the fluctuations of the produced charge, expressed by Eq. (5. 6), are smaller (for silicon, $\sqrt{0.12}$ =0.35 times smaller) than the fluctuations corresponding to the production of E_{ph}/E_{ehp} independent charges [Che02]. The true value of *F* for silicon is still unknown, but the value of *F*=0.12 has been used, obtaining a satisfactory agreement with the measured results.

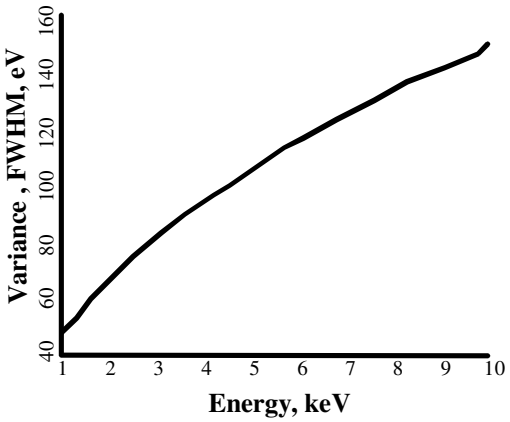


Figure 5. 5 - Fundamental *X*-ray energy resolution possible, expressed in FWHM eV, for different energies of the impinging *X*-ray in keV [Sel04].

$$\sigma_Q = q\sqrt{F\left(\frac{E_{ph}}{E_{ehp}}\right)} \tag{5. 6}$$

The method proposed in [Che02], for determining the variance in the total amount of charge produced by *N* converted *X*-rays, consists firstly of a summation of the charge released by each individual *X*-ray for obtaining the total amount of charge released in a single event, as is the arrival of one bunch in the case of the XFEL, i.e. $Q_{tot} = \sum_1^N Q_{bunch}$. In this summation, each Q_{bunch} fluctuates according to Eq. (5. 6), and the number of converted *X*-rays fluctuates according to *Poisson* statistics with the mean number $\overline{N}$ [Che02]. Equations (5. 7) and (5. 8) express the mean value of generated charge $\overline{Q}_{tot}$ and its variance σ_{Qtot}.

$$\overline{Q}_{tot} = \overline{N} \cdot \overline{Q} \tag{5. 7}$$

$$\sigma_{Q_{tot}} = \overline{Q}^2 \times \sigma_N + \overline{N} \times \sigma_Q \quad (5.\ 8)$$

Finally, substituting in Eq. (5. 8) the results from Eqs.(5. 3) and (5. 6), Eq. (5. 9) is readily obtained.

$$\sigma_{Q_{tot}} = \left(q \frac{E_{ph}}{E_{ehp}} \right)^2 \cdot \overline{N} \left(1 + F \frac{E_{ehp}}{E_{ph}} \right) + \overline{N} \sigma_Q \quad (5.\ 9)$$

In the case of the XFEL, the incoming photon energies are 3keV<E_{ph}<15keV, E_{ehp}=3.65eV at room temperature, and F=0.12. The charge created by the interaction of *X*-ray photons in the sensor is very small and has to be amplified in a low-noise circuit before any further signal processing [Edl04].

From the analysis performed so far, it can be concluded that, for the case of E_{ph}=3keV *X*-rays generated at the XFEL, according to Eq. (5. 3) the amount of charge generated by each photon is $\overline{Q}_{E_{ph}=3keV} = 1.3 \times 10^{-16}$C, or 822 photogenerated holes, with a fluctuation of σ_Q=1.6×10^{-18}C, or approximately 10 holes, according to Eq. (5. 6). For E_{ph}=15keV, $\overline{Q}_{E_{ph}=15keV} = 6.57 \times 10^{-16}$C, or approximately 4110 photogenerated holes, with σ_Q=3.55×10^{-18}C, or approximately 22 holes according to Eq. (5. 6).

In order to achieve single-photon counting, as required at the XFEL, the read-noise present in the device should not exceed ideally ENC of 10 electrons (the variance in the amount of charge produced by a single *X*-ray photon with 3keV, the E_{ph} defined as "nice to have"), or minimally an ENC of 16 electrons, which is the variance for 8keV impinging *X*-ray photons.

According to [Fow04], the minimal RMS read noise achievable nowadays could be around 14 to 20 electrons, using the fastest ROI readout mode, for a standard CMOS active pixel sensors. In practice, this noise can be as large as 20 electrons or more. To improve the read noise of the detector devices, which strongly degrades the device performance, as it can be concluded from Eq. (5. 5), the parasitic capacitances must be reduced at the charge sensing mode. Splitting the readout of the detector into 100 pixels reduces the thermal and flicker noises by 100. Here, as the dark current is reduced 100 times, the dark current noise is reduced by a factor of 10. This is the rationale for a pixellated detector. An added advantage is that the overall rate capability goes up, too [Sel04].

The major cause of degradation of the spatial and the spectral resolutions of an *X*-ray silicon detector (for example, CCD) is charge diffusion from the active area beneath the depletion region [Wad84], if the entire silicon bulk is not fully depleted. This would be the case if the handle-wafer of the SOI structure would not be completely depleted. When a photon is absorbed beneath the depletion region, the resulting electron cloud moves through the silicon lattice and into the depletion region influenced only by diffusion. Diffusion increases the diameter of the charge cloud in a manner that is proportional to the distance

that the cloud has travelled. Charge splitting occurs if the charge cloud overlaps two or more pixels prior to entry into the depletion layer. When this occurs, portions of the original charge cloud are split among several pixels. The splitting manifests itself as image smearing and a decrease in the apparent energy of the *X*-ray event [Wad84]. In X-ray spectroscopic measurements, these events are discarded during subsequent data analysis, since the incomplete charge collection and spread of the signal over many pixels causes the total noise of such events to be unacceptably high [Pri03].

Events from the undepleted bulk occupy a disproportionately large fraction of the surface area of the device. As a result, a probability of having a second photon to arrive at the pixel which has already accumulated some signal charge from a previous photon (the so called "pile-up") is many times higher for the events from undepleted bulk [Pri03]. In order to partially solve this problem, the depletion layer width should be at least as wide as the absorption length of the highest energy *X*-ray in the incident beam [Wad84]. A second cause of spatial and spectral resolution degradation is event splitting and charge loss, when *X*-ray photons are absorbed at the boundary of two or more pixels, but within the depletion layer.

5.4 Radiation Hardness Considerations

For silicon based radiation detectors working in hard radiation conditions (>10MeV), the defects induced due to radiation degrade the performance of the silicon devices in two principal ways. First, these defects create generation-recombination centres that decrease the minority carrier diffusion length and increase the leakage current with relation to the irradiation dose [Tay96]. Second, lattice defects change the effective resistivity of the silicon. Consequently, the operating voltage needed for the full depletion of the detector changes, and gradually may exceed the breakdown voltage of the device. Additionally, as the irradiation dose increases, the defects eventually change the type of conductivity of the silicon [Tuo03].

A widely studied approach to improve the radiation hardness (>10MeV) of silicon detectors is to introduce oxygen into the silicon material. The model used to explain the behaviour of the oxygen enriched silicon identifies the V_2O (vanadium oxide) defect as the main responsible for the radiation induced negative space charge [Cas03]. The formation of V_2O is suppressed in oxygen rich materials, through the reaction of interstitial oxygen with vacancies [Cas03]. The reaction that leads to formation of V_2O is: $V + O_i \rightarrow VO$, $VO + O \rightarrow V_2O$. Increasing the concentration of interstitial oxygen enhances the ratio of the first of the two reactions, reducing the formation of V_2O [Cas03].

Normally, the *float zone* (Fz) silicon is preferred in the radiation detectors manufacturing, as higher bulk resistivities, and consequently full depletion detectors at reasonable voltages, can be achieved in this way. However, Fz-Si has a low oxygen concentration. On the other hand, silicon wafers made using the *Czochralski* (Cz) method, intrinsically contain high concentrations of oxygen, and nowadays, the production of Cz wafers with sufficient resistivity and well

controlled, high concentration of oxygen, are available [Tuo03]. Moreover, Cz-Si wafers exist up to a diameter of 300mm, while the Fz-Si wafers typically exhibit diameters of about 100mm or 150mm. The oxygen concentration of the material in a Cz-Si, *n*-type <100> wafer, with a resistivity of ~1kΩ·cm, is around 15ppma (parts per million atomaric) [Tuo03], or around $8\times10^{17}cm^{-3}$ [Cas03]. At the Fraunhofer IMS clean-room facility, the standard processes employ 200mm diameter wafers, which than strongly indicates Cz-Si high-resistivity wafers must be used.

On the other hand, in the presently used CMOS technologies the transistors have a very thin, high-quality gate-oxide that can withstand sufficiently high total doses of irradiation [Bog00]. In contrast, in LOCOS based processes, the less quality 400-1000nm dick oxides are used to isolate different devices. Due to the trapping of positive charges in the oxide during the irradiation, the threshold voltages of the NMOS structures decrease, as the LOCOS field oxides lose their isolating function after a few tens of Grays [Bog00]. The devices get statically biased during the irradiation, as there is a large effect of the electric field on the initial yield of unrecombined holes (a parasitic field transistor appears parallel with the designed transistor) [Bog00]. Two solutions are proposed by Bogaerts and Dierickx [Bog00] to circumvent the observed degradation mechanisms. Pixels based on PMOS transistors are a straightforward way to tackle the total ionising dose problems. Another solution is the use of enclosed (gate-all-around) NMOS transistors for readout. The disadvantage here would be the area required for such circuits.

In the case of the XFEL, each bunch would originate ~10^4 *X*-ray photons to be impinging on a pixel detector, for the case of detectors I (D1) and II (D2), and ~10^3 photons (nice to have) for the case of the detector III (D3). If the single pixel photoactive area should be $A_{pixel}=(100\times100)\mu m^2$ for the case of D1, it gives 10^8 photons/cm^2/bunch. For the case of D2, $A_{pixel}=(30\times30)\mu m^2$, which gives 1.11×10^9 photons/cm^2/bunch. In the case of the last detector structure, $A_{pixel}=(50\times50)\mu m^2$, which for ~$10^3$ photons/bunch gives 4×10^7photons/cm^2/bunch.

There are 4000 bunches for every 100ms, or (10^8 photons/cm^2/bunch×4000bunches×10(ms/s))=4×10^{12}photons/s·cm^2, for the case of D1, or 4.44×10^{13} photons/s·cm^2 for D2, or 1.6×10^{12} photons/s·cm^2 in the case of D3. If the device should be performing one second exposures, it means that each silicon detector pixel should tolerate, in average, the photon flux Φ_0 of 4×10^{12}, 4.44×10^{13}, or 1.6×10^{12} *X*-ray photons/s·cm^2 respectively for detectors I, II, and III.

Multiplying the value of the photon fluxes obtained in photons/s·cm^2 for each energy, dividing the result by the characteristic absorption length of an *X*-ray with this energy in silicon, namely L_{abs}(3keV)=4.38μm, L_{abs}(8keV)=69.62μm, L_{abs}(12keV)=228.7μm, and L_{abs}(15keV)=442.6μm [Hen93], also shown in Figure 5. 6(a), and the silicon material density ρ_{ch}(Si)=2.328g/cm^3, the total dose-per-exposure (total-dose-per-second) to be received at the surface of each pixel can

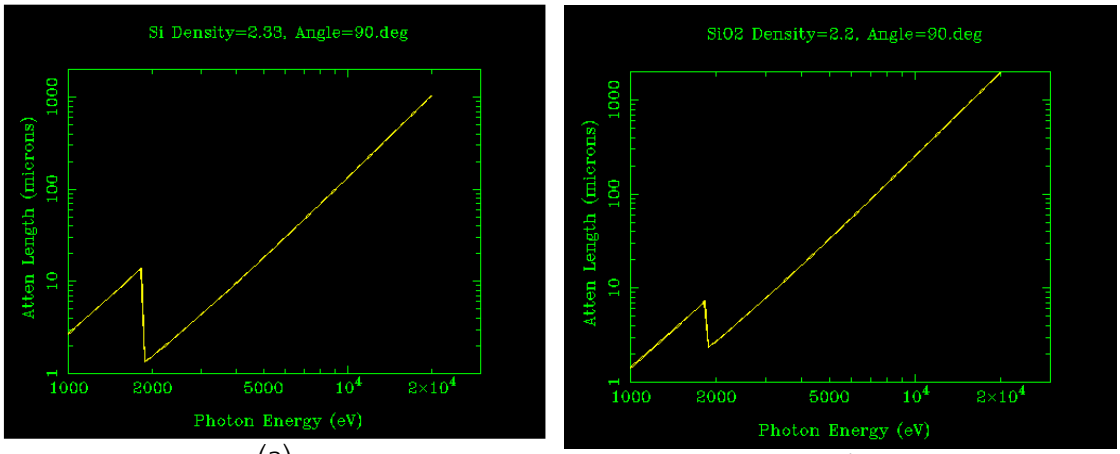
be calculated using Eq. (5. 10), together with the conversion factor 1Rad=6.25×10^{13}eV/g.

$$RadDose = \frac{\Phi_0 E_{ph}}{L_{abs} \cdot \rho_{ch}} \cdot \frac{1Rad}{6.25\times10^{13}\,\frac{eV}{g}}, Rad \qquad (5.\ 10)$$

The results of the total-dose impinging on the surface of the handle-wafer substrates of each of the detectors, for different *X*-ray energies can be observed in Table 5. 4.

Table 5. 4

Detectors	***ρ_{ch}(Si), g/cm^3***	***Φ_0, $\frac{photons}{s\cdot cm^2}$***	***Total-Dose*** E_{ph}=3keV L_{abs}=4.38μm	***Total-Dose*** E_{ph}=8keV L_{abs}=69.62μm	***Total-Dose*** E_{ph}=12keV L_{abs}=228.7μm	***Total-Dose*** E_{ph}=15keV L_{abs}=442.6μm
D1	2.328	4×10^{12}	188.3 kRad	31.6 kRad	14.42 kRad	9.32 kRad
D2	2.328	4.44×10^{13}	2.09 MRad	350.65 kRad	160.12 kRad	103.42 kRad
D3	2.328	1.6×10^{12}	52.69 kRad	12.64 kRad	5.77 kRad	3.73 kRad



(a) (b)

Figure 5. 6 - (a) Absorption length for *X*-rays in silicon [CXRO]; (b) Absorption length for *X*-rays in SiO_2 [CXRO].

Extensive studies involving high-energy particle physics experiments, developed over many years, have shown silicon itself to be highly tolerant (>100MRad) to *X*-rays and electrons below 100keV [Wes99]. Therefore, the Cz-Si based *X*-ray detectors, working under the conditions described, should not be damaged by the radiation present at the XFEL facility, according to the results presented in Table 5. 5.

Table 5. 5

Detectors	**Number of exposures, E_{ph}=3keV**	**Number of exposures, E_{ph}=8keV**	**Number of exposures, E_{ph}=12keV**	**Number of exposures, E_{ph}=15keV**
D1	~531	~3164	~6935	~10730
D2	~48	~285	~625	~967
D3	~1898	~7911	~17543	~26810

In order to calculate the amount of the photon flux Φ_1 that exits the 500μm thick handle-wafer, the relation $\Phi_1 = \Phi_0 e^{-\alpha d_{HW}}$ [Sze02] is being used.

By definition, the absorption length is the distance a photon should travel within a certain material in order to decrease the value of its incidental photon flux to the 1/e part of it. From the latter, it can be easily calculated that α=1/L_{abs}. Finally, using Eq. (5. 10) and the absorption coefficients α for each *X*-ray photon energy of interest, the amount of photon flux exiting the 500μm handle-wafer layer and striking the BOX layer can be easily calculated, for the *X*-rays actually being absorbed, i.e. 90% of Φ_0. Nevertheless, the thickness of the handle-wafer (500μm) was chosen to assure the almost total absorption of each impinging *X*-ray, i.e. Φ_1 values will be in all cases almost zero, and the BOX layer should receive around 10% of Φ_0 which did not undergo the absorption process to strike the BOX structure and the SOI based CMOS readout circuitry.

The calculations of the irradiation dose impinging on the BOX layer are performed using Eq. (5. 9), and considering $\rho_{ch}(SiO_2)$=2.2g/cm^3 and the absorption length values for the *X*-rays impinging on the silicon oxide taken from the experimental data available in [CXRO], Figure 5. 6(b). The results can be observed in Table 5. 6.

Table 5. 6

Detectors	***$\rho_{ch}(SiO_2)$ g/cm^3***	***Φ_1, $\frac{photons}{s \cdot cm^2}$***	***Total-Dose*** E_{ph}=3keV L_{abs}=7.9μm	***Total-Dose*** E_{ph}=8keV L_{abs}=128.2μm	***Total-Dose*** E_{ph}=12keV L_{abs}=433.2μm	***Total-Dose*** E_{ph}=15keV L_{abs}=839.8μm
D1	2.2	4×10^{11}	0	0	0.81 kRad	0.52 kRad
D2	2.2	4.4×10^{12}	0	0	8.95 kRad	5.77 kRad
D3	2.2	1.6×10^{11}	0	0	0.32 kRad	0.21 kRad

Finally, the total-dose-per-pixel-per-1s-exposure of *X*-rays to be received by the readout circuitry fabricated on the thin (200nm) SOI layer is calculated using the absorption lengths for the *X*-rays in silicon and the silicon density values, to be substituted in Eq. (5. 10) on one hand, and the gate and field oxides, on the other.

The results of the total-dose irradiation impinging on the surface of the SOI based readout circuitry, for back-illuminated detector structures and different *X*-ray energies, can be observed in Table 5. 7 for the case of the SOI thin silicon layer, and Table 5. 8 for the case of the gate and field oxides present in the readout circuitry.

Table 5. 7

Detectors	***$\rho_{ch}(Si)$, g/cm^3***	***Φ_2, $\frac{photons}{s \cdot cm^2}$***	***Total-Dose*** E_{ph}=3keV L_{abs}=4.38μm	***Total-Dose*** E_{ph}=8keV L_{abs}=69.62μm	***Total-Dose*** E_{ph}=12keV L_{abs}=228.7μm	***Total-Dose*** E_{ph}=15keV L_{abs}=442.6μm
D1	2.328	3.8×10^{11}	0	0	1.37 kRad	0.88 kRad
D2	2.328	4.43×10^{12}	0	0	15.97 kRad	10.32 kRad
D3	2.328	1.6×10^{11}	0	0	0.58 kRad	0.37 kRad

The irradiation values finally reaching the readout circuitry fabricated on the thin SOI film and enlisted in Tables 5. 7 and 5. 8 should not represent any problem at all for the silicon CMOS circuits, even more so if thin gate-oxides are used, as well as PMOS transistors (not irreplaceable by NMOS ones). Readout chips designed for LHC experiments for example, made in standard 0.25μm CMOS technology, tolerate over 30Mrads of 10keV *X*-rays [Wes99].

Table 5. 8

Detectors	$\rho_{ch}(SiO_2)$ ***g/cm³***	Φ_1, $\frac{photons}{s \cdot cm^2}$	***Total-Dose*** E_{ph}=3keV L_{abs}=7.9μm	***Total-Dose*** E_{ph}=8keV L_{abs}=128.2μm	***Total-Dose*** E_{ph}=12keV L_{abs}=433.2μm	***Total-Dose*** E_{ph}=15keV L_{abs}=839.8μm
D1	2.2	3.8×10^{11}	0	0	0.81 kRad	0.52 kRad
D2	2.2	4.43×10^{12}	0	0	8.92 kRad	5.75 kRad
D3	2.2	1.6×10^{11}	0	0	0.32 kRad	0.21 kRad

According to the conclusions drawn so far, it results viable to produce SOI based photodetector arrays with completely depleted handle-wafer high-resistivity silicon substrates, to be used in *X*-ray detection and imaging task for energies between 3keV and at least 15keV, although the results indicate that a possibility exists to extend this range even to 30keV, where different applications as for example, in dental radiography, could be found.

In the next chapter, the new 0.35μm standard CMOS process available at the Fraunhofer IMS will be described, which offers a combination of high-voltage and low-voltage (or digital) on the same chip, and five different substrates on which photodetectors can be fabricated.

6 The Standard 0.35μm CMOS Process and its Photodetection Possibilities

Throughout the previous chapters several issues were discussed, which affect the quantum efficiency, optical sensitivity, noise, dissipated power, geometry and spectral response of different photodetectors and pixel configurations that contain them, fabricated in a standard twin-well CMOS process, such as for example the 0.5μm process available at the Fraunhofer IMS. It was shown that high doping profiles, thin gate-oxides and low bias voltages (as the used V_{DD}=3.3V) affect adversely the performance of CMOS imagers, and can still cause problems if standard solutions to some of these issues are to be applied. This includes using separated photoactive (e.g., *n*-well PD, BPD, or PG) and readout node areas (e.g., FD), where charge-coupling between the two regions is not always possible. On the other hand, as reduced SCR widths (of around 0.16μm to 0.55μm) degrade the photodetector quantum efficiencies, especially in the NIR part of the spectra, it was proposed to use mixed CMOS processes, in which there exist low-voltage and high-voltage operation microelectronic devices. One example of such a process is the *30V thin-film SOI* process. In the proposed solution, the photodetector structure is to be placed on the higher-resistivity handle-wafer, while the readout circuitry is fabricated on the 200nm thick low-resistivity SOI film. This approach proved useful (especially if voltages as high as 30V can be applied to the device), although the photoactive and readout regions can be only electrically connected, which implies that the signal charge collected in the photodetector during the integration time must be integrated (i.e., converted into an electrical signal) already at the photodetector, where its capacitance still implies several noise and driving problems.

The standard 0.35μm *n*-well double polysilicon and 4 metal layers standard CMOS process which combines low-voltage and high-voltage MOSFETs proved to be an excellent solution, as it comprises all the advantages discussed for the SOI and standard CMOS processes, only integrated on the same silicon substrate, plus offering the possibility of a second polysilicon layer, crucial for the PG APS design. Moreover, the 0.35μm process developed for operating conditions present in the automotive industry applications, offers 5 different substrate concentrations and opens a wide range of photodetection possibilities, as it will be shown and discussed in the following sections.

6.1 Meeting the 0.35μm Standard CMOS Process

As introduced above, the process available at the Fraunhofer IMS for fabrication of CMOS imagers is the new 0.35μm *n*-well, double polysilicon and 4 metal layers standard CMOS process which combines low-voltage (DG) and high-voltage (HV, up to 80V) MOSFETs. It presents approx. 10nm thick DG and approx. 50nm thick HV gate-oxides, two polysilicon work-functions (n^+ doped, in case of NMOS transistor gates, or p^+ doped, in case of PMOS transistor gates), a second polysilicon layer, as well as five available substrate concentrations.

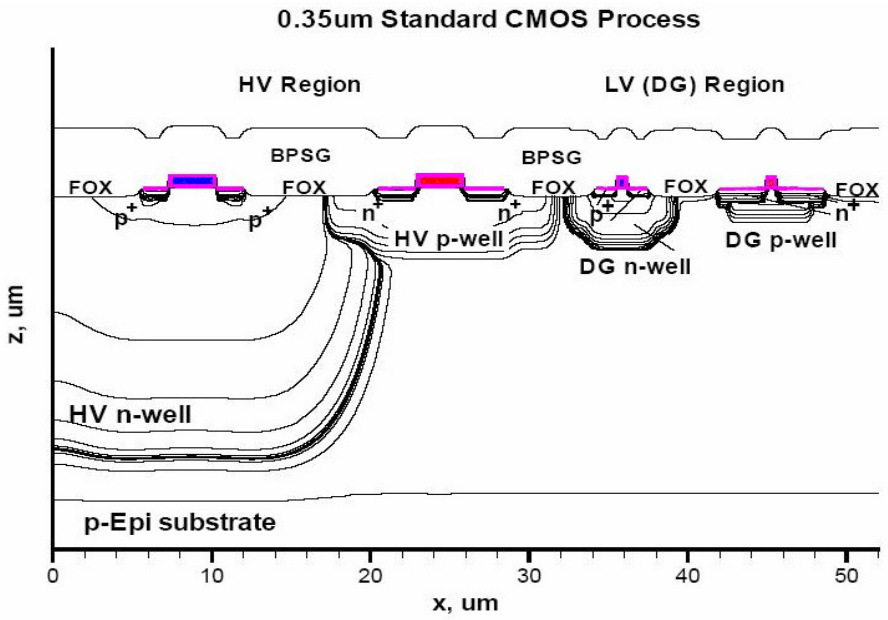
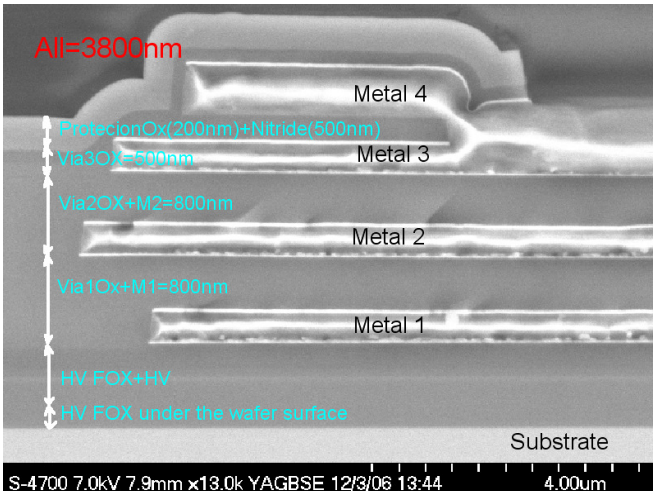


Figure 6. 1 – Two dimensional simulation performed using TCAD software tools for the HV and DG regions CMOS MOSFET pairs, fabricated in the 0.35μm standard CMOS process under investigation.

The substrate concentrations mentioned are: 1) the deep HV *n*-well, 2) the HV *p*-well, 3) the DG *n*-well, 4) the DG *p*-well, originally developed as the HV *p*-type MOSFET channel implantation performed to control its threshold voltage V_{th}, and finally 5) the 15μm deep *p*-type epitaxial layer grown on top of the highly doped silicon bulk (N_A=1×10^{19}cm^{-3}), with an average concentration of N_A=3×10^{14}cm^{-3}. It is spoken here about average concentrations because of the modulated doping profile present in all the structures, built due to space-charge diffusion from the highly-doped silicon bulk on one side, and the epitaxial layer surface where the different dopants are implanted during the entire CMOS process flow on the other, taking place during each high-temperature step. The data presented here were extracted form 2-D simulations performed using (*Synopsys*) TCAD software tools, following all the fabrication steps forming part of the flow-chart of the 0.35μm standard CMOS process under investigation.

In Figure 6. 1, the results of the two dimensional simulation of the 0.35μm CMOS process under investigation are shown, where the total doping concentrations are indicated for both, the HV and the DG MOSFET pair (*p*-type and *n*-type MOSFETs). The modulated doping profile is identified by the different lines which indicate the change in the doping concentration.



(a)

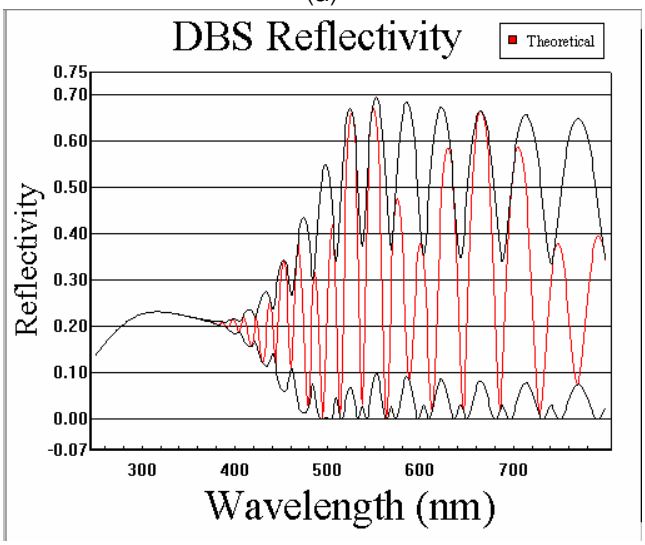


Figure 6. 2 – (a) SEM image of the surface of an integrated circuit fabricated in the 0.35μm CMOS process under investigation, where silicon substrate, as well as the FOX, BPSG, inter-metal oxides, and the passivation (Ni_3S_4) silicon-nitride layers, as well as all the 4 metal layers can be observed [ELMOS]; (b) theoretical wavelength dependent reflectivity curve for the structure shown in (a), obtained using the DBS experimentally obtained surface layer refractive indexes (courtesy: Dr. J. Weidemann, EL-MOS FEDU).

Unfortunately, as already explained in Chapter 2 of this text for the case of the 0.5μm CMOS process, the unavoidable field-oxide (FOX) structures used for wafer-surface isolation between neighbouring semiconductor devices, as well as the BPSG, the inter-metal oxides, and the silicon-nitride based passivation layer existent on top of any integrated circuit fabricated in this process deliver wavelength dependent variable transmittance if used for front-side illumination CMOS imaging. The SEM image of the surface of an integrated circuit fabricated in this process can be observed in Figure 6. 2(a) [ELMOS]. Figure 6. 2(b), shows the theoretical wavelength dependent reflectivity curve for the same structure, obtained again using the surface layer refractive indexes experimentally obtained through *dual beam spectrometry* (DBS) measurements.

Once again, the major concern aroused regarding the silicon-nitride passivation layer, formerly used also in the 0.5μm standard CMOS process

analysed in Chapter 2, the heavy absorption of which in the UV, blue and green part of the spectra (up to 550nm wavelengths of impinging radiation) can be observed in Figure 2. 6. Nevertheless, due to extreme operating conditions under which the ICs fabricated in this technology should operate, it is impossible to eliminate the silicon nitride or use a PSG layer instead, as it was done for the case of the 0.5μm process. So, the solution proposed in Chapter 2, and depicted in Figure 2. 8 also applies for this case. Nevertheless, avoiding the use of Metal 3 and Metal 4 layers in the photoactive area of any pixel configuration would simplify here the BPSG and inter-metal oxides etching. The theoretically obtained reflectivity curve of the silicon-nitride passivation layer, which would be alone covering the silicon wafer surface according to the solution proposed and depicted in Figure 2. 8 can be observed in Figure 6. 3. The additional solution of generating perforated passivation layers, applying the so called "moth eye effect" as shown in Figure 2. 10 would certainly help to generate an anti-reflective coating of the existent passivation layer.

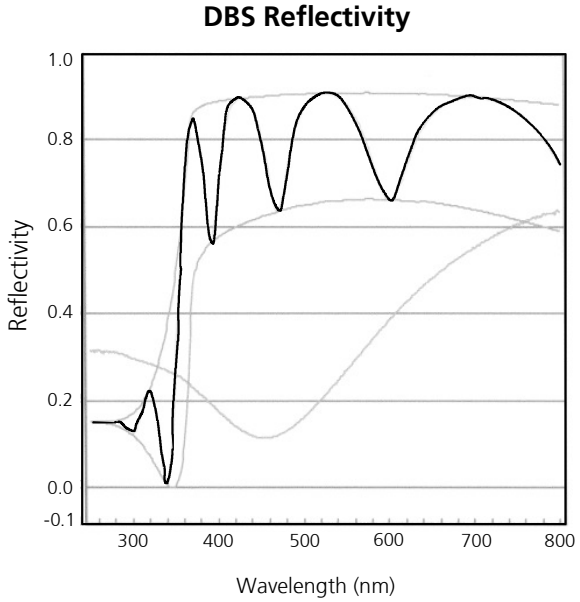


Figure 6. 3 – Theoretical wavelength dependent reflectivity curve for the approximately 500nm thick silicon-nitride passivation layer, obtained using its DBS experimentally determined wavelength dependent refractive indexes (courtesy: Dr. J. Weidemann, EL-MOS FEDU).

Nevertheless, for the time being it is the silicon-nitride absorbance in the UV-to-green part of the spectra which gives rise to more concern, so experiments are being carried out aiming to use UV transparent passivation layers, as it is normally done in EPROM memories, where their programming is done through UV irradiation. This kind of solution results the most viable one, but its detailed analysis remains beyond the scope of this work.

Next, the photodetector structures available in the 0.35μm standard CMOS process under investigation will be enlisted.

6.2 Photodetector Structures Available in the 0.35μm Standard CMOS Process

The process offers the possibility of fabricating eight different reverse-biased *p-n* junction based photodetectors: 1) HV *n*-well photodiode (PD); 2) LV *n*-well PD; 3) LV BPD, which features a p^+ (source/drain) diffusion on top of the LV *n*-well, used to push the electrostatic potential maximum from the silicon surface and thus improve the dark current and detector noise characteristics; 4) n^+ (*source/drain* implantation) PD on HV *p*-well, X_j=0.3μm; 5) n^+ PD on LV *p*-well; 6) n^+ PD on the *p*-type epitaxial layer; 7) p^+ PD on HV *n*-well; and 8) p^+ PD on LV *n*-well.

Additionally to the reverse-biased *p-n* junction based photodetectors presented so far, the different *metal-oxide-semiconductor* capacitor (MOS-C or *photogate* (PG)) based photodetectors which can be fabricated in the 0.35μm CMOS process under investigation are: 1) LV *p*-type PG, consisting of a LV gate-oxide grown thermally on top of a LV *n*-well and covered by a first polysilicon layer (POLY1); 2) LV *n*-type PG located on top of the LV *p*-well diffusion; 3) LV *n*-type Poly2 PG, consisting of a second polysilicon layer deposited on top of an oxide-nitride-oxide (ONO) dielectric; one of the advantages of this structure is the possibility of overlapping the first polysilicon layer, which in case of a PG active pixel configuration improves drastically the *charge-transfer efficiency* (CTE); 4) Epi *n*-type PG, identical to the LV *n*-type PG, only fabricated on top of the lower-doped *p*-Epi substrate; 5) Epi *n*-type Poly2 PG, identical to the LV *n*-type Poly2 PG only fabricated on top of the *p*-Epi substrate; 6) HV *n*-type PG, consisting of a HV gate-oxide thermally grown on top of a HV *p*-well, covered by a polysilicon (POLY1) gate; and, finally 7) a HV *n*-type Poly2 PG, fabricated by depositing a second polysilicon layer on top of a HV ONO structure, using a HV *p*-well diffusion as silicon substrate.

6.3 Experimental Results

Following the same procedures already described in Chapter 2, dark current (*I-V*), capacitance (*C-V*), and optical sensitivity and quantum efficiency measurements were performed on some of the photodetector structures described above. It is important to mention here that the 0.35μm standard CMOS process was, at the time period the first test structures were fabricated in it, still in its development phase. So, some problems appeared during the fabrication of the DG BPD, the DG (Epi) *n*-well, DG n^+ PD and n^+ (Epi) PD photodiodes. On the other hand, some of the values obtained could consequently change together with the process fabrication steps. Nevertheless, this first characterization offers a quite valuable insight into the properties of photodetectors fabricated in this process.

Two sets of test structures were designed and fabricated in the 0.35μm process, regarding the reverse-biased *p-n* junction based photodetectors enlisted above. In case of the DG *n*-well PD, the first test structure consists of a (243.4×243.2)μm^2 rectangle, while the second (DG *n*-well PD *stripes*) is a series connection of 40 DG *n*-well stripes, which share a common area of $7.1\times10^{-5}cm^2$,

and a perimeter of 0.356cm. On the other hand, the DG n^+ PD first test structure is a (243.4×243.2)μm^2 rectangle identical to the one described for the DG *n*-well PD, while the second DG n^+ PD test structure consists of 40 interconnected stripes with a common area of 10.4×10^{-5}cm^2, and a 4.32cm perimeter. Furthermore, two additional test structures were designed and fabricated in order to characterize the HV *n*-well PD. The first test structure was a (236.7×243.4)μm^2 square, while the second one consisted of 4 interconnected stripes, presenting an area of (8×236)μm^2 each, and a common test-structure area of 9×10^{-5}cm^2. All three sets of test structures were fabricated on the same multi-project chip (MPC) and 5 dice belonging to the same wafer, containing all these test structures, were characterized in order to obtain average experimental results which are presented below.

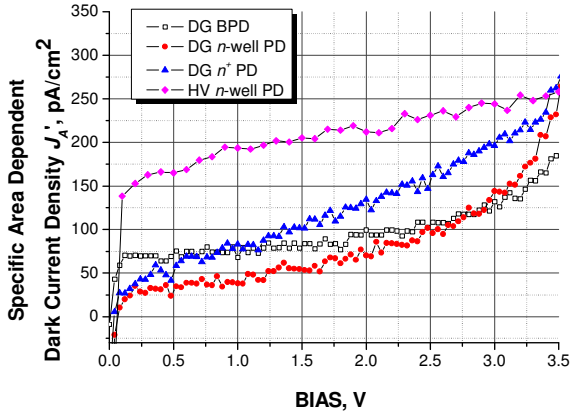
Regarding the PG test structures, three sets were additionally fabricated and incorporated into the same MPC. Namely, for the case of a DG *n*-type PG, it was a (250×250)μm^2 square. For the case of the DG (Epi) *n*-type PG, it had (250.2×250)μm^2, while for the DG *p*-type PG, a (231.2×226.6)μm^2 square was fabricated on top of a DG *n*-well.

6.3.1 Dark Current (*I-V*) Measurements

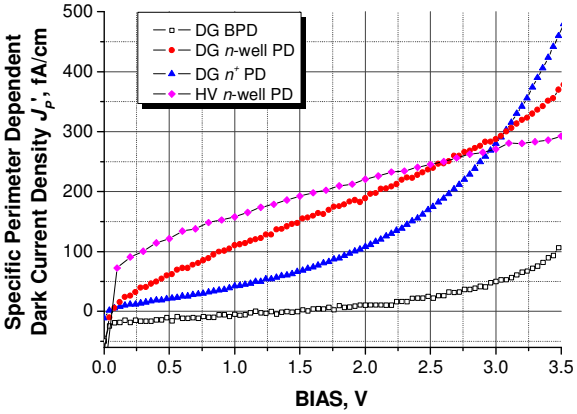
As explained in Chapter 2, I-V measurements were performed on all the test structures described, in darkness and at room-temperature, using the *Hewlett Packard HP1455B semiconductor analyser* device. The dark current measurements were performed on all the five fabricated dice, and using the equation system consisting of Eqs. (2. 48), (2. 49), and (2. 50), the reverse-bias averaged *specific area dependent dark current density* $J'(A)$ measured in pA/cm^2, as well as the reverse-bias averaged *specific perimeter dependent dark current density* $J'(P)$ measured in fA/cm, obtained for the case of all three photodiode test structure sets, can be observed in Figure 6. 4.

From Figure 6. 4, the effect of much deeper HV *n*-well, when compared to the DG *n*-well, can be observed, especially if the specific perimeter dependent dark current densities of these two structures are taken into account. On the other hand, if the results presented in Figure 6. 4 are compared to the results obtained for similar structures fabricated in the 0.5μm CMOS process to be observed in Figure 2. 27, they result almost identical, at least for the DG *n*-well PD area dependence. Moreover, the structures fabricated in the 0.35μm process deliver less perimeter dependent dark current (approx. 300fA/cm under V_{DD}=3.3V reverse biasing) then their counter-parts fabricated in the 0.5μm process (approx. 1.3pA/cm for same biasing conditions). The area dependent dark current densities of the DG and HV PDs fabricated in the 0.35μm process result quite similar. On the other hand, although the amount of the specific area dependent dark current density delivered by the DG BPD is very similar to that of the DG *n*-well PD, and under certain bias-voltages even higher, the specific perimeter dependent dark current density of the DG BPD is much smaller than the perimeter dependent contribution of all the other photodiodes, which yields smaller amount of dark current flowing in this structure when compared to the

others, namely due to the increased concentration within the surface p^+ implantation and the electrostatic potential peak "pushed" away from the silicon surface.



(a)



(b)

Figure 6. 4 – (a) Specific area dependent dark current density $J'_{dark}(A)$ reverse biasing voltage dependence obtained for the DG *n*-well PD and HV *n*-well PD fabricated in the 0.35μm standard CMOS process under investigation; (b) specific perimeter dependent dark current density $J'_{dark}(P)$ voltage dependence for the same photodetector structures.

The dark current measurement results obtained in form of specific area dependent dark current density for all three PG based photodetector structure can be observed in Figure 6. 5. As it was expected due to the SCR dark current dependence (Eq. (2. 63)), the DG (Epi) *n*-type PG delivers the highest amount of dark current per cm^2 of all three PG structures, almost $400fA/cm^2$ when reverse-biased at V_{DD}=3.3V.

On the other hand, and opposite to the situation examined for the 0.5μm process (Figure 2. 40), here the DG *p*-type PG delivers almost a half of the dark current density delivered for the same biasing conditions by the DG *n*-type PG, although its SCR is wider (0.21μm in contrast to the 0.14μm in case of the DG *n*-type PG). The latter probably due to the minority carriers lifetime differences in the DG *p*-well and the DG *n*-well diffusions.

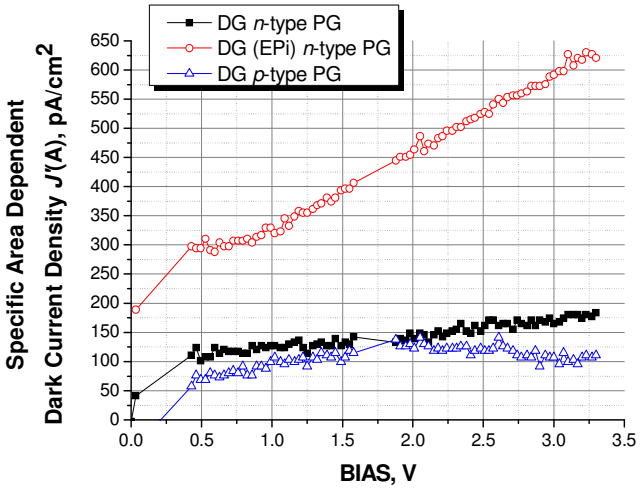


Figure 6. 5 - Specific area dependent dark current density $J'_{dark}(A)$ reverse biasing voltage dependence obtained for the DG (Epi) *n*-type PG, DG *n*-type PG, and DG *p*-type PG, fabricated in the 0.35μm standard CMOS process.

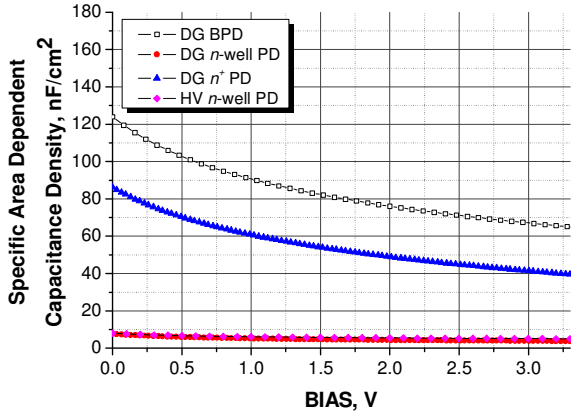
In the following section, capacitance (*C-V*) measurement results obtained for the same test structures already described will be discussed and compared.

6.3.2 Capacitance (*C-V*) Measurements

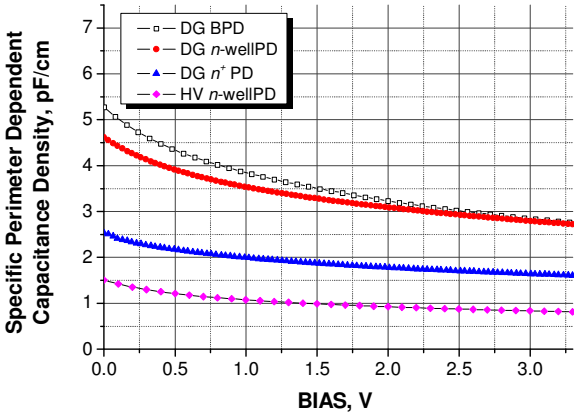
C-V measurements were performed on all the reverse-biased *p-n* junction based photodetector test structures described, using the *Keithley 590 semiconductor analyser*, at room temperature. To perform the measurements, the measurement station *chuck* (which connects the metallic plate on which the MPC wafer is located during the measurement) was short-circuited to the surface substrate contact of each die, using it as a new test structure anode, while the *n*-well or n^+ electrodes were grounded, converted into test structure cathodes. A reverse-biasing sweep voltage was then applied to the wafer surface, starting at -3.3V and ending at 0V, together with a superimposed ac signal with a 100kHz frequency. Each measurement was performed using long integration times.

The *C-V* characterization results can be observed in Figure 6. 6, expressed through the specific area dependent capacitance density in nF/cm^2 (Figure 6. 6(a)), and the specific perimeter dependent capacitance density in pF/cm (Figure 6. 6(b)). The much higher area dependent capacitance density of the HV *n*-well PD when compared to the DG *n*-well PD can be explained by the notorious difference in the doping concentration-dependent *p-n* junction SCR widths generated by the same bias voltage in the two photodetectors. On the other hand, the much more expanded lateral area of the HV *n*-well PD, i.e. higher lateral capacitance, causes its specific perimeter dependent capacitance density to be around 24% higher than the one of the DG *n*-well PD. Once again, the not fully-depleted *n*-well causes an increased capacitance of the DG BPD, although deeper SCR on both sides yield smaller capacitance of this structure fabricated in the 0.35μm than the one fabricated in the 0.5μm.

If compared to the *n*-well PD fabricated in the 0.5μm CMOS process, the DG n-well PD presents 50% less capacitance area dependence, although the perimeter dependences of the both structure remains very similar.



(a)



(b)

Figure 6. 6 – Specific area dependent capacitance density, in nF/cm^2, for the DG *n*-well PD and HV *n*-well PD photodetector structures fabricated in the 0.35μm standard CMOS process under investigation; (b) specific perimeter dependent capacitance density, in pF/cm, for the same test structures of interest.

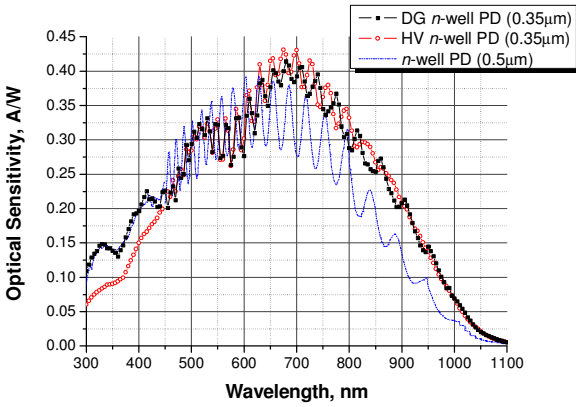
For the case of PG test structures, the oxide capacitance of DG PGs is 36.7μF/cm^2, while for the HV PGs it is 7.58μF/cm^2.

6.3.3 Optical Sensitivity and Quantum Efficiency Measurements

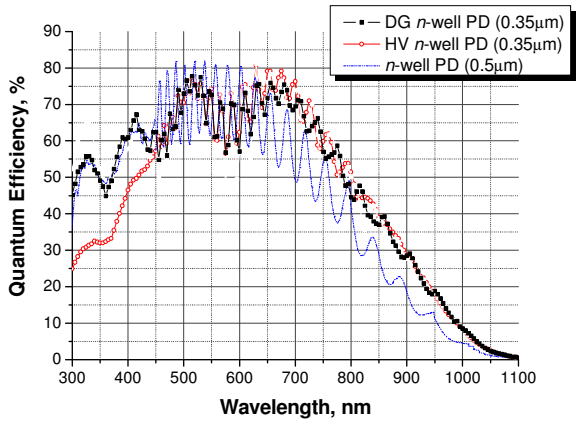
Using the optical sensitivity and quantum efficiency measuring stations described in *Appendix A* and *Appendix B* of this work, the results shown in Figure 6. 7 were obtained for the reverse-biased (at V_{DD}=3.3V) *p-n* junction based DG *n*-well PD and HV *n*-well PD photodetector structures fabricated in the 0.35μm CMOS process, compared to the *S* and η curves previously obtained for the *n*-well PD fabricated in the 0.5μm process.

In Figure 6. 7, the wafer surface isolation layer reflection maxima and minima effects caused by can be observed, as predicted by the theoretical

wavelength dependent reflectivity curve shown in Figure 6. 2. From the curves obtained it can be concluded that the maximum optical sensitivity (S=0.414A/W) of the DG n-well PD fabricated in the 0.35μm process is reached for λ=680nm of impinging radiation, at which wavelength its quantum efficiency is of 75.24%. On the other hand, the same photodetector structure presents the highest quantum efficiency (η=81.2%) for impinging red light with λ=630nm. The HV n-well PD reaches maximum optical sensitivity of 0.43A/W (η=76.26%) for impinging radiation with λ=700nm, and maximum quantum efficiency of 79.2% for irradiation at 675nm wavelength.



(a)



(b)

Figure 6. 7 – Measured wavelength dependent optical sensitivity graph (in A/W) for the DG n-well PD and HV n-well PD photodetector structures fabricated in the 0.35μm standard CMOS process under investigation, compared to the optical sensitivity graph obtained for the n-well PD fabricated in the 0.5μm CMOS process; (b) wavelength dependent quantum efficiency graph obtained for (a).

Nevertheless, the most interesting discovery was made for the soft-UV part of the spectra, where for λ=305nm of impinging radiation the DG n-well PD presents 0.118A/W reaching 55% of quantum efficiency, even higher or at least in the same range (considering the 10% of possible measurement error) as the n-well PD fabricated in the 0.5μm process (also shown in Figure 6. 7 for

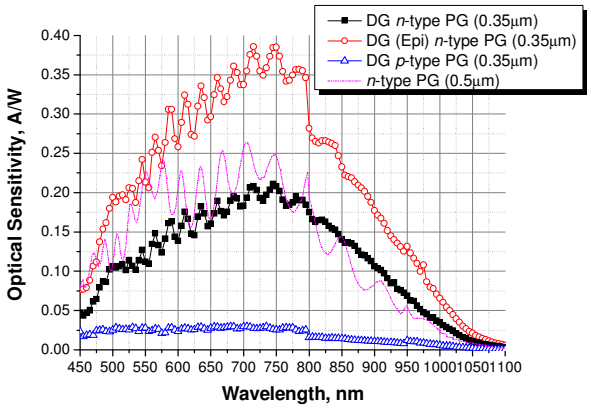
comparison). This contravenes the previous speculations made about the magnitude of quantum efficiency decrease in the UV part of the spectra due to the silicon-nitride based passivation layer, based on the results presented in Figure 2. 6 for the 0.5μm CMOS process. Of course, due to the distance between the silicon surface (where most of *ehp* are generated when illuminated by UV radiation) and the SCR generated at the *p*-*n* junction parallel to the wafer surface in the HV *n*-well PD (of around 5μm or more than 3 times longer than in case of the DG *n*-well PD) the loss of minority carriers due to recombination processes within the HV *n*-well is much higher here, and the HV *n*-well PD exhibits a quantum efficiency of only 26.7% (S=0.07A/W) for impinging radiation at λ=305nm.

It was already explained above that the existence of the epitaxial layer avoids the photo- and thermally carriers generated in the highly-doped silicon bulk from reaching the SCRs of any photodetector fabricated in the epitaxial layer, due to the existence of the epitaxial-bulk junction. As this could take more time than T_{int}, this is an excellent measure combating image-lag. Nevertheless, in the 0.5μm CMOS process, the epitaxial layer thickness was of 5.5μm, i.e. almost 3 times thinner than the one existent in the 0.35μm process (of 15μm). The latter implies that in the 0.35μm process a larger number of minority carriers is able to diffuse to the photodetector's SCR where it gets drifted. Of course, the probability of *ehp* photogeneration to take place deeper in the substrate rises with the wavelength dependent silicon absorption length. So, it is no surprise that both *n*-well PD structures have much higher quantum efficiency in the NIR part of the spectra than their counter-part fabricated in the 0.5μm process.

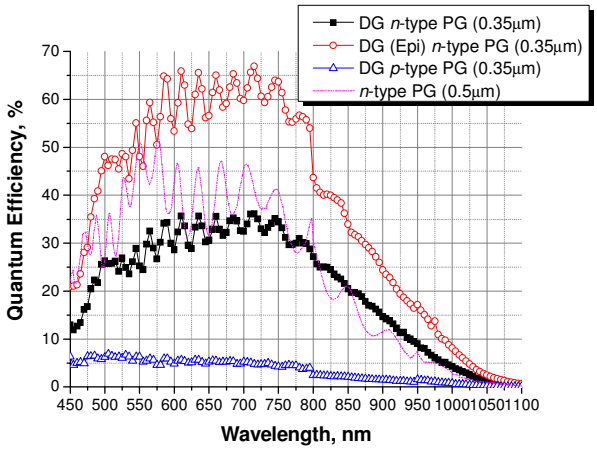
Considering now the PG based photodetector structures fabricated in the 0.35μm CMOS process, and using the test structures already described above, the same optical sensitivity and quantum efficiency measurements were performed on them, using a 10Hz modulated illumination and the measurement station described in *Appendix B* of this text. The results obtained for the DG *n*-type PG, DG (Epi) *n*-type PG, and the DG *p*-type PG can be seen in Figure 6. 8, compared to the wavelength dependent curves obtained for the *n*-type PG fabricated in the 0.5μm process.

As it was expected, and due to the higher-resistivity epitaxial substrate, the DG (Epi) *n*-type PG presented much higher optical sensitivity and quantum efficiency values than any other PG based photodetector. Its highest optical sensitivity of 0.385A/W (η=63.66%) stands for impinging radiation at λ=750nm, much higher than the 0.21A/W presented by the DG *n*-type PG at 745nm wavelengths. On the other hand, the DG (Epi) *n*-type PG reaches its maximum quantum efficiency of 66.7% for impinging 715nm wavelengths, while the DG *n*-type PG reaches its maximum 35.7% of quantum efficiency for λ=610nm. When compared to the results obtained from the *n*-type PG fabricated in the 0.5μm process, it can be concluded that the DG *n*-type PG has worse performance than its 0.5μm process fabricated equivalent in the UV-VIS part of the spectra, but is better for NIR applications. For 910nm of impinging

wavelengths, the DG (Epi) *n*-type PG delivers 0.17A/W (η=22.8%), while the DG *n*-type PG has only 0.101A/W (η=13.81%). The worst of all due to reasons already explained in Chapter 2 referring to the case of the 0.5μm CMOS process, is the DG *p*-type PG which delivers 0.01A/W (η=1.4%) for the same impinging radiation. The *n*-type PG fabricated in the 0.5μm process delivers 0.09A/W (η=11.7%) under same conditions.



(a)



(b)

Figure 6. 8 - Measured wavelength dependent optical sensitivity graph (in A/W) for the DG *n*-type PG, DG (Epi) *n*-type PG, and DG *p*-type PG photodetector structures fabricated in the 0.35μm standard CMOS process under investigation, compared to the optical sensitivity graph obtained for the *n*-type PG fabricated in the 0.5μm CMOS process; (b) wavelength dependent quantum efficiency graph obtained for (a).

Taking into account all the considerations made so far, a couple of pixel configuration possibilities in the 0.35μm standard CMOS process under study will be discussed in the following section.

6.4 Possible Pixel Configurations in the 0.35μm Standard CMOS Process

Following the discussion carried out in Chapter 3, once again the standard solutions regarding noise, response speed, and spectral response issues

of different pixel configurations were attempted. Namely, in case of reverse-biased *p-n* junction based photodetectors, the standard BPD APS with separated photoactive and readout areas was designed and properly simulated using TCAD software tools for the case of the standard 0.35μm CMOS process under study.

For the case of interest, a (10×10)μm^2 BPD photodetectors were designed to be charge-coupled to a separated FD consisting of a (2×2)μm^2 n^+ NMOS *source/drain* diffusion fabricated on top of the epitaxial layer (blocking the DG *p*-well and *n*-well implantations in this area). The charge coupling is to be realised through a DG (Epi) *n*-type PG based transfer gate. The basic working function of such an active pixel sensor was already described in detail in Chapter 3 of this work.

Figure 6. 9(a) shows the two-dimensional doping concentration profile of such a structure, obtained as a result of a 0.35μm process and device simulation performed using TCAD software tools. On the other hand, Figure 6. 9(b) shows the electrostatic potential profile of the structure obtained at a horizontal cut (parallel to the wafer surface) at the DG *n*-well barrier height, i.e. at the lower edge of the SCR generated when the BPD is reverse-biased at 0.6V, for the two operation phases: the photocharge collection (integration phase) in which case the TG remains grounded, just as hypothetically (controlled by a RST transistor) does the FD; and the readout phase during which the BPD remains biased at 0.6V, but the TG and the FD are biased at 3.3V (for simulation purposes) immediately after the FD is reset to V_{DD}=3.3V.

Considering the results depicted in Figure 6. 9 it can be concluded that the combination of DG BPD and the TG and FD structures fabricated on the epitaxial layer proved useful, and it can be concluded that such a fully-operational pixel configuration can be fabricated in the 0.35μm CMOS process under investigation. This opens a wide range of possibilities in what CMOS imaging is concerned. Nevertheless, the proper pixel design, fabrication, and characterization, containing this kind of structures remains beyond the scope of this work.

Turning to the PG based pixel configurations, in Chapter 3 we already discussed most of the issues regarding the charge transfer efficiency from the PG photoactive area to the FD readout node, when using a TG in a single polysilicon process. Nevertheless, in the investigated 0.35μm CMOS, there exist a possibility of using a second polysilicon layer, which should turn these kind of PG APS configurations into a viable solution to introduce low-capacitance FD and "true" CDS realisation issues.

As in the case of the BPD APS, a 2-D doping and electrostatic potential simulation was performed for a pixel structure containing a (10×10)μm^2 DG *n*-type PG photodetector, charge-coupled through a 0.7μm long DG *n*-type PG based TG to a separated FD consisting of a (2×2)μm^2 n^+ NMOS *source/drain* diffusion fabricated on a DG *p*-well diffusion. The results of the TCAD software tools based simulation performed for the DG PG APS are shown in Figure 6. 10.

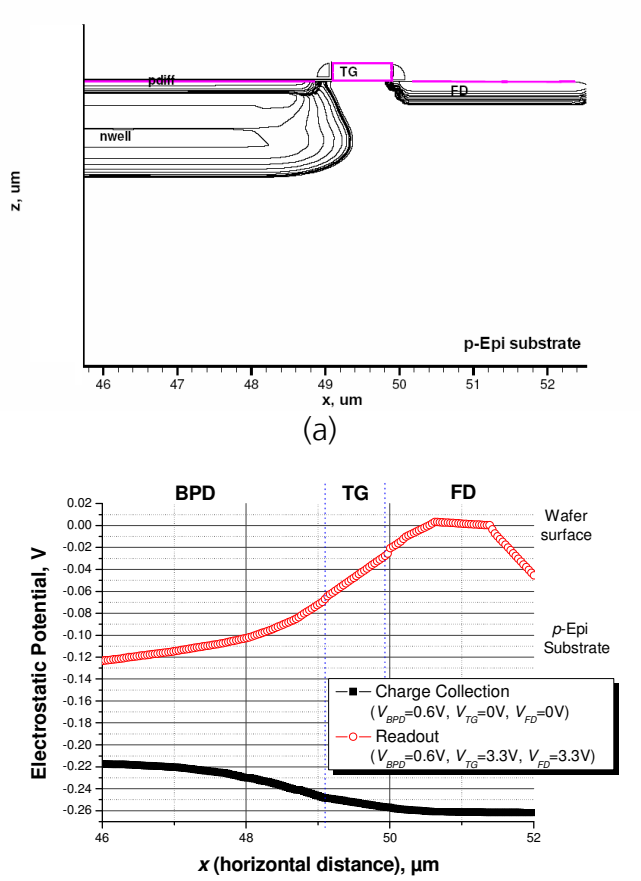


Figure 6. 9 – (a) 2-D total doping concentration simulated using TCAD software for the BPD APS, fabricated in the 0.35μm CMOS process; (b) the simulated electrostatic potential horizontal profile for both, the charge integration and the readout stages, obtained for (a) at the *n*-well SCR border (BPD barrier height).

Figure 6. 10(a) shows the 2-D electrostatic potential simulation for the case of the readout phase. Here, the PG remains grounded, while the TG and the FD are both, reverse-biased at V_{DD}=3.3V. The electrostatic potential profile obtained at the silicon-oxide interface beneath the DG *n*-type PG, parallel to the wafer surface for both, the photocharge collection (integration) and readout operation modes of this pixel configuration can be observed in Figure 6. 10(b). Here, during charge collection, the PG remains reverse-biased at V_{DD}=3.3V, turning grounded during the readout phase, while the TG remains biased at V_{TG}=1.6V all the time, and the FD is in the worst case always reverse-biased at 3.3V. For the case where during the charge collection phase the PG is biased at 3.3V, and the TG at 0V, the complete isolation of the photoactive area is even more pronounced, as it can be observed in Figure 6. 10(c). So, from these simulation results, here again could be concluded that a proper fabrication and operation of DG PG APS structures is possible and viable in the investigated 0.35μm CMOS process. Once again, the process of pixel design, layout, fabrication, and characterization remains beyond the scope of this work.

Moreover, and based on the analysis and the experimental characterization of different PG based photodetector structures performed, a

higher quantum efficiency is to be expected from DG (Epi) *n*-type PG APS, especially beneficial in 3-D TOF based CMOS imaging tasks. So, another TCAD software based set of electrostatic potential and total doping simulations was performed regarding this kind of pixel structures, which can be observed in Figure 6. 11.

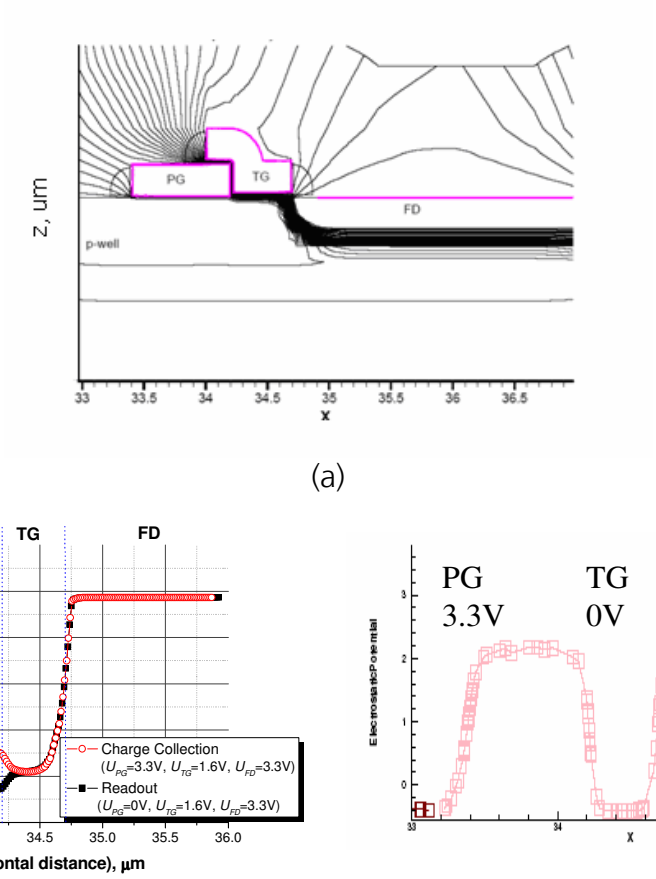


Figure 6. 10 – (a) 2-D electrostatic potential simulation performed using TCAD software for a DG *n*-type PG APS in the readout stage, fabricated in the 0.35μm CMOS process; (b) electrostatic potential profile obtained from a horizontal cut performed to the 2-D simulation shown in (a) at the silicon-oxide interface for the charge collection and readout operation modes of the DG *n*-type PG APS; (c) the charge collection phase, during which the PG and the FD remain even more isolated, as the PG is reverse biased at 3.3V, the TG at 0V, and the FD at a certain voltage between 0V and 3V.

Figure 6. 11(a) shows the results of a 2-D electrostatic potential simulation of the DG (Epi) *n*-type PG APS during the charge collection phase. Here, the DG (Epi) *n*-type PG remains during T_{int} reverse biased at 3.3V, the DG (Epi) *n*-type PG based TG remains grounded to achieve a proper electric isolation between the PG photoactive and the FD readout regions, while the FD is considered to be reverse-biased at 1.6V.

On the other hand, Figure 6. 11(b) shows the same pixel configuration fabricated on top of the epitaxial layer, blocking the DG *n*-well and *p*-well implantation steps, in the readout modus. Here, as before, the PG is grounded, while the TG and the FD are assumed to be reverse-biased at 3.3V. As it can be

observed form the graph, the electrostatic potential profile enables correct and complete transfer of all the carriers collected in the integration phase from the photoactive (PG) area to the FD.

For a better understanding of both operation modes, Figure 6. 11(c) shows one dimensional cuts of the electrostatic potential profiles shown in Figures 6. 11(a) and 6. 11(b), performed at the silicon-oxide interface.

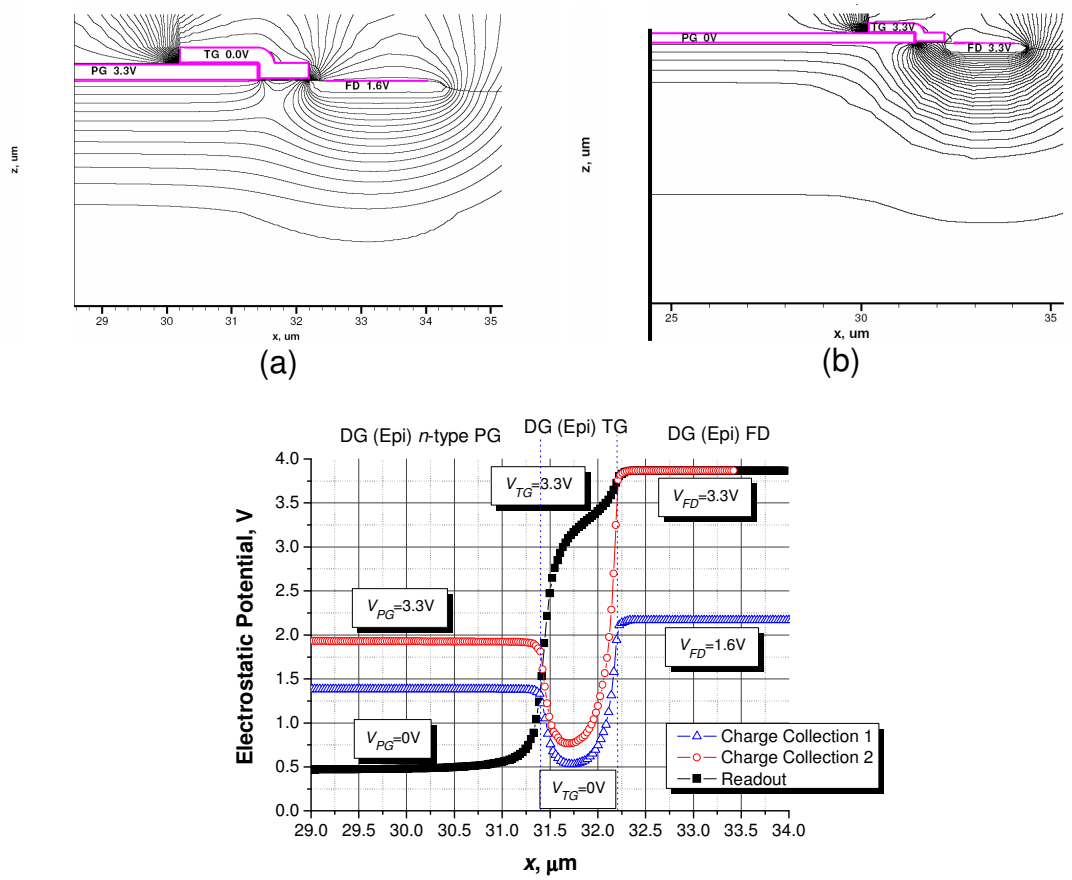


Figure 6. 11 – (a) 2-D electrostatic potential simulation result, performed using TCAD software tools, for DG (Epi) *n*-type PG APS configuration during the charge collection phase; (b) the same pixel configuration in the readout modus; and (c) electrostatic potential profiles obtained from (a) and (b) as one-dimensional cuts performed at the silicon-oxide interface.

Finally, and based on the experimental results and theoretically simulated results enlisted so far, it can be concluded that the 0.35μm standard CMOS process available at the Fraunhofer IMS for CMOS imager fabrication offers a vast range of novel possibilities, if compared to the previously examined 0.5μm and the SOI processes.

There is a lot of work to be done following this investigation, which remains beyond the scope of this work.

Conclusions

Photodetection possibilities of the three CMOS processes available for CMOS imagers fabrication at the Fraunhofer IMS, namely the 0.5μm, the 0.35μm, and the *30V thin-film SOI* CMOS processes, were examined in detail in this work. It was shown that in order to design and fabricate optimal CMOS imagers, at first proper photodetector structure characterization is to be performed, results of which are to be used in further design optimisation and in the electrical simulation of potential pixel configurations.

The first problem encountered, when using standard (not imaging enhanced) CMOS processes, was related to the inter-metal isolation and passivation layer influence on the photodetectors optical sensitivity. Namely, the dielectric structure covering the surface of any electronic circuit fabricated in any of the three standard CMOS processes under investigation, delivers wavelength dependent variable transmittance in front-illumination imaging applications. A theoretical analysis of the effect explained the reflected radiation wavelength dependent maxima shifts observed in experimentally obtained optical sensitivity curves of various photodetectors fabricated in these processes. A solution is proposed here, consisting of a combination of measures. On one hand, it consists of the complete elimination of the inter-metal oxides normally deposited on top of the photoactive area, followed on the other hand, by a perforation of the passivation layer, applying the so called "moth eye effect", which should diminish the amount of radiation reflected from the wafer surface and turn the passivation layer into an anti-reflecting coating.

Following the concept of dark current, present as an unavoidable physical effect at any temperature above 0K, minority carrier lifetimes were measured for the case of the 0.5μm standard CMOS process. Using the "pulsed MOS-C" measuring method, minority carrier generation times of 2.25ms with a surface velocity of 4.75μms^{-1} were obtained for the *p*-well diffusion, while for the *n*-well the generation time was of 639.2μs with a surface velocity of 203.3μms^{-1}. Moreover, using the so called "steady-state short-circuit" optical measuring methods, recombination lifetimes of 496ns were obtained for electrons in *p*-well diffusions, which implies diffusion lengths of 31.8μm. For the case of holes in *n*-well diffusions, their recombination times resulted in average to be of 958ns for similar diffusion lengths (of around 30μm) as in the previous case. Once these experimental values were obtained, mathematical models of the dark current flowing in different reverse biased *p-n* junction or MOS-C based photodetectors fabricated in the 0.5μm process were developed and compared to the experimentally obtained dark current curves. Although an acceptable correspondence between theory and the measured results was achieved, especially in what the tendencies and mechanisms of thermal generation in each case are concerned, several possible sources of measurement error were discovered that could have taken place during the experimental determination of

the minority carrier lifetimes. Taking this into account, it was decided that the amounts of dark current flowing in any photodetector structure fabricated in this process could be better modelled if a different approach is to be followed. Namely, the specific area dependent dark current densities in A/cm^2 were then measured for each type of potential photodetectors, together with the specific perimeter dependent dark current densities in A/cm. The second model for the dark current, which considers the geometry (area and perimeter) of any device fabricated in a certain CMOS process proved more useful, as it presents a smaller amount of possible sources of measurement error (as a smaller number of different measurements is performed).

The same concept was followed for the biasing voltage dependent capacitance characterization, also very dependent on the specific geometrical features of a particular photodetector. The capacitance value of a photodetector in a specific pixel configuration results of great importance for the pixel SNR.

Based on the need of proper electrical and optical characterization of the potential photodetector structures to be fabricated in any CMOS process of interest, dark current (*I-V*), capacitance (*C-V*), as well as wavelength dependent optical sensitivity and quantum efficiency measurements were performed on each of the photodetector structures examined in the 0.5μm and the 0.35μm standard CMOS processes under investigation. A review of the obtained results is enlisted in tables C. 1 to C. 3, divided by process.

Regarding the PG based photodetector structures, it was found that the *n*-type PG quantum efficiency limiting factor is on one side, the depth of the epitaxial layer on which they are fabricated, and on the other the absorbance of the polysilicon gate. For the case of *p*-type PG structures, the quantum efficiency limiting factor is the depth of the *n*-well on which they are fabricated, i.e. the distance of the upper border of the SCR generated at the *n*-well – *p*-Epi (substrate) to the silicon-oxide interface where the SCR is generated under the PG where the photogenerated charge is to be collected. Regarding the first case of interest, the gate absorbance was attempted to decrease by using semi transparent ITO gates instead of polysilicon. Moreover, the use of ITO gates was also to improve the CTE between the PG and the FD in PG APS configurations. Unfortunately, the latter was not completely accomplished due to ITO etching and other problems. Two sets of MOS-C based test structures were nevertheless compared, showing that the ITO gate based PG structures present 2 times higher quantum efficiencies than their counter-parts fabricated using standard polysilicon gates, at least in the soft-UV – VIS part of the spectra (450nm-580nm). After this wavelength and further in direction of NIR or UV part of the spectra, the standard polysilicon gate based PG structures showed much better performance than the ITO based ones. Based on these results, the aim of incorporating ITO layers in the standard 0.5μm CMOS process was abandoned.

As far as pixel configurations are concerned, the standard *n*-well PD based APS proved not to be the optimum pixel configuration. It yields a high noise equivalent power (NEP) dependence on the photodetector capacitance, and proved unsuitable for "true" CDS. Standard applied solution in which the

photoactive area is separated from the readout node, i.e. where a MOS-C based transfer gate is incorporated to enable charge-coupling between the photodetector (PD or PG) and a small area, small capacitance n^+ floating diffusion, proved impossible to realize in the 0.5μm process, although highly desirable. In the 0.35μm process it resulted viable, thanks to the possibility of fabricating TG and n^+ FD structures directly on the higher-resistivity epitaxial layer (blocking the DG *n*-well and *p*-well implantations).

Photodetector	*Specific Area Dependent Dark Current Density (V_{DD}=3.3V),* pA/cm^2	*Specific Perimeter Dependent Dark Current Density (V_{DD}=3.3V),* pA/cm	*Specific Area Dependent Capacitance Density (V_{DD}=3.3V),* nF/cm^2	*Specific Perimeter Dependent Capacitance Density (V_{DD}=3.3V),* pF/cm
n-well PD	180	1.3	11.9	3.24
BPD	160	0.15	53.4	15.33
n^+ PD	200	0.7	35.5	1.25
p-type PG	176.2	-	C_{OX}=287.6	-
n-type PG	71.1	-	C_{OX}=287.6	-

Table C. 1 – Electrical parameters for the photodetectors fabricated in the 0.5μm CMOS process.

Photodetector	Specific Area Dependent Dark Current Density (V_{DD}=3.3V), pA/cm^2	Specific Perimeter Dependent Dark Current Density (V_{DD}=3.3V), pA/cm	Specific Area Dependent Capacitance Density (V_{DD}=3.3V), nF/cm^2	Specific Perimeter Dependent Capacitance Density (V_{DD}=3.3V), pF/cm
DG *n*-well PD	181.17	0.283	3.79	2.72
DG BPD	156.14	0.076	65.14	2.77
DG n^+ PD	223.13	0.389	39.56	1.61
HV *n*-well PD	248	0.337	5.04	0.816
DG *n*-type PG	183.4	-	36.7×10^3	-
DG *p*-type PG	110.7	-	36.7×10^3	-
DG (Epi) *n*-type PG	629.9	-	36.7×10^3	-

Table C. 2 – Electrical parameters for the photodetectors fabricated in the 0.35μm CMOS process.

As no better solution was found for CMOS imaging applications in the 0.5μm CMOS process, pixel configurations were fabricated incorporating an additional charge storage capacitance. For 3-D time-of-flight based CMOS imaging, where high response speed and specially high SNR are required, three basic pixel configurations were examined pursuing an increase of the SNR, but maintaining the consumption power within reasonable limits. It was discovered that if a pixel configuration based on the *n*-well PD and two source-follower buffers is fabricated, the response speed of the pixel is optimal, although the consumed power reaches the acceptable upper limit, and the NEP is higher than it could be desired. As the 35.9% of the mean square noise voltage is being delivered in this pixel configuration by the first buffer stage, a second configuration was examined where this first buffer stage was eliminated. This measure brought a charge-sharing effect between the *n*-well PD and the storage

capacitance, which decreased the spectral responsivity of the pixel in 3.4%. Nevertheless, the power consumption was reduced in one half, and the NEP was reduced in 27%. Trying to decrease even more the NEP (and to increase the SNR), a third configuration was tested, where the signal is already amplified at the photodetector. This reduced the NEP in additional 9%, but increased the power consumption, due to the addition of a common-source based amplifier to the pixel, 4 times if compared to the first pixel configuration studied.

Photodetector	*Optical Sensitivity*, A/W (λ=300nm)	*Quantum Efficiency* (λ=300nm)	*Optical Sensitivity*, A/W max.	*Quantum Efficiency* max.	*Optical Sensitivity*, A/W (λ=910nm)	*Quantum Efficiency* (λ=910nm)
n-well PD	0.116	42%	0.392 (λ=624nm)	82% (λ=538nm)	0.106	14.4%
BPD	0.03	11.77%	0.373 (λ=626nm)	76.5% (λ=574nm)	0.13	17.8%
n^+ PD	0.053	21.56%	0.409 (λ=658nm)	83.6% (λ=574nm)	0.124	16.9%
p-type PG	0	0	0.045 (λ=704nm)	8.91% (λ=576nm)	0.015	2.04%
n-type PG	0	0	0.263 (λ=706nm)	51.9% (λ=576nm)	0.0873	11.9%

Table C. 3 – Optical sensitivity and quantum efficiency properties measured for the photodetector structures fabricated in the 0.5μm standard CMOS process.

Photodetector	*Optical Sensitivity*, A/W (λ=300nm)	*Quantum Efficiency* (λ=300nm)	*Optical Sensitivity*, A/W max.	*Quantum Efficiency* Max.	*Optical Sensitivity*, A/W (λ=910nm)	*Quantum Efficiency* (λ=910nm)
DG *n*-well PD	0.119	48.26%	0.4143 (λ=680nm)	77.8% (λ=515nm)	0.205	27.9%
HV *n*-well PD	0.066	26.7%	0.4306 (λ=700nm)	78.4% (λ=655nm)	0.198	24.47%
DG *n*-type PG	0	0	0.21 (λ=745nm)	36.11% (λ=715nm)	0.1	13.81%
DG *p*-type PG	0	0	0.003 (λ=735nm)	4.77% (λ=715nm)	0.01	1.4%
DG (Epi) *n*-type PG	0	0	0.386 (λ=715nm)	66.9% (λ=715nm)	0.17	22.8%

Table C. 4– Optical sensitivity and quantum efficiency properties measured for the photodetector structures fabricated in the 0.35μm standard CMOS process.

Additionally, two novel pixels were proposed in this work, based on *p*-type PG structures, in which the readout principle relies on charge injection into a floating substrate. Moreover, if the charge is injected into the substrate in a time much shorter than the integration time, then a huge parametric "time-compression" amplification appears of the photodetector current. This amplification is understood as the ratio of the induced photocurrent and the maximum readout injection current peak. This injection current readout principle was mathematically modelled and experimentally investigated for the case of the 0.5μm process, where it showed viable for 2-D imaging applications, presenting an amplification factor of around 10^4, if a readout time of 4.5ns is used together with an integration time of 20ms, and the injection current is measured as a

voltage drop at a 1kΩ load resistor. Nevertheless, the quantum efficiency reached at the end of the readout process showed huge losses in the collected charge due to charge-injection and readout mechanisms. Moreover, a two-phase peak detect-and-hold circuit was designed which presents an acceptable detection error of less than 1% for readout times of approximately 2μs, increasing to the 86% for the case of 4.5ns readout times, which turned the entire pixel concept even less attractive.

A second proposal was then made, in which separated readout and photoactive regions are presented, using local SOI features of the *30V thin-film SOI CMOS* process available at the Fraunhofer IMS. To show the NIR quantum efficiency enhanced properties of a photodetector fabricated on the higher-resistivity handle-wafer, while its readout circuitry is fabricated on the high-doped 200nm thick SOI film, the SOI charge-injection photogate (SOI CI-PG) pixel configuration was proposed. A considerable increase of the quantum efficiency in the NIR part of the spectra was measured at the *p*-type PG fabricated on the handle-wafer, if compared to its counter-part fabricated in the 0.5μm process. Moreover, using a readout time of 1.4μs, an integration time of 20ms, and a load resistor of 1kΩ, quite acceptable results were obtained. The SOI CI-PG presented a "time-compression" amplification of 4×10^4 and the charge injection efficiency proved to oscillate in this case between the 45% and the 90%, depending on the amount of collected (injected) charge.

Moreover, the same 30V thin-film SOI CMOS process was proposed to be used in *X*-ray direct scientific imaging. The idea is to generate p^+ diffusions on the 500μm thick handle wafer surface and to deplete it completely (in this process, applying certain special designs, up to 600V can be used), and use it as a back-illumination hard-radiation detector. Theoretical investigations proved this kind of pixel arrays to be radiation hard, up to energies of 15keV of impinging radiation, with an acceptable quantum efficiency, and suitable for medical and dental radiography applications.

The pixel design, fabrication, and characterization for imager arrays to be fabricated in the 0.35μm CMOS process under study remained beyond the scope of this work, and constitute of course the main part of the future work to be done in this area.

References

[Ack96] B. **Ackland** and A. **Dickinson**, "Camera on a Chip", in *ISSCC Dig.*, Feb. 1996, pp. 22-25.

[And02] *Andor Technology*-LOT Oriel Group Europe, *X-Ray CCD Detectors – Course Notes*, September 2002.

[Ane00] G. M. **Anelli**, *Conception et caracterisation de circuits integres resistants aux radiations pour les detecteurs de particules du LHC en technologies CMOS submicroniques profondes*, Ph.D. thesis, *Institut National Polytechnique de Grenoble*, Dec. 2000

[Bak05] R. J. **Baker**, *CMOS Circuit Design, Layout, and Simulation*, 2nd Ed., IEEE Press, Wiley-Interscience, USA, 2005

[Bar97] S. L. **Barna** *et al.*, "Characterization of a prototype Pixel Array Detector (PAD) for use in microsecond framing time-resolved X-ray diffraction studies", *IEEE Trans. Nucl. Sci.*, vol. 44, No. 3, June 1997, pp. 950-956

[Bas98] S. A. **Bashar**, *Study of Indium Tin Oxide (ITO) for Novel Electronic Devices*, Ph.D. thesis, King's College of the University of London, 1998

[Bau81] W. A. **Baum**, B. **Thomsen**, and T. J. **Kreidl**, "Subtleties in the Flat-Fielding of Charge Coupled Device /CCD/ Images", *Solid State Imagers for Astronomy: SPIE No. 290*, 1981

[Ber67] C. G. **Bernhard**, „Strukturelle und funktionelle Adaptation in einem visuellen System", *Endeavour XXVI*, vol. 98, 1967, pp. 79-84

[Bes88] P. **Besl**, "Active optical range imaging sensors", *Machine Vis. and Applications*, vol. 1, 1988, pp. 127-152

[Bla03] L. **Blanquart** *et al.*, "FE12 : A front-end readout chip designed in a commercial 0.25 □m process for the ATLAS pixel detector at LHC", *Proc. IEEE Nuclear Science Symposium Portland 2003*.

[Bog00] J. **Bogaerts**, B. **Dierickx**, "Total dose effects on CMOS Active Pixel Sensors", (http://citeseer.csail.mit.edu/301532.html)

[Bre99] K. F. **Brennan**, *The physics of semiconductors with applications to optoelectronic devices*, Cambridge University Press, UK, 1999.

[Bur97] B. E. **Burke**, J. A. **Gregory**, M. W. **Bautz**, G. Y. **Prigozhin**, S. E. **Kissel**, B. B. **Kosicki**, A. H. Loomis, D. J. Young, "Soft X-ray CCD imagers for AXAF", *IEEE Trans. Electron Dev.*, vol. 44, No. 10, Oct. 1997, pp. 1633-1642

[Bus03] A. **Bußmann**, *Charakterisierung und Optimierung elektrooptischer Bauelemente in Standard CMOS Prozessen*, Ph.D. Thesis, adviser Prof. B. Hosticka, Ph.D., University of Duisburg-Essen, 2003

[Büt03] B. **Büttgen**, T. **Oggier**, R. **Kaufmann**, P. **Seitz**, N. **Blanc**, "Demonstration of a novel drift-field pixel structure for the demodulation of modulated light waves with application in three-dimensional image capture", SPIE, Proc. Vol 5302, 2004, pp. 9-20

[Büt04] B. **Büttgen**, T. **Oggier**, R. **Kaufmann**, N. **Blanc**, P. **Seitz**, "Advanced simulations of semiconductor optoelectronic devices: the Drift-Field Pixel structure", *CSEM Scientific Report 2003*, p. 47

[Cas03] G. **Casse**, "Development of semiconductor detectors for very harsh radiation environments in high energy physics applications", *Proceedings ERICE 2003*, 2003.

[Cas97] A. **Castoldi**, C. **Guazzoni**, A. **Longoni**, E. **Gatti**, P. **Rehak**, L. **Strüder**, "Conception and design criteria of a novel silicon device for the measurement of position and energy of X-rays", *IEEE Trans. On Nuclear Science*, Vol. 44, No. 5, Oct. 1997, pp. 1724-1732.

[Cas98] A. **Castoldi**, E. **Gatti**, C. **Guazzoni**, A. **Longoni**, P. **Rehak**, L. **Strüder**, "A new high resolution X-ray imaging detector with fast read-out", *Nuclear Instruments & Methods in Physics Research, A 409*, 1998, pp. 379-381

[Cas06] A. **Castoldi**, A. **Galimberti**, C. **Guazzoni**, P. **Rehak**, R. **Hartmann**, L. **Strüder**, "Multi-linear silicon drift detectors for X-ray and Compton imaging", *Nucl. Instr. And Meth. In Phys. Res.*, Section A, No. 568, 2006, pp. 89-95

[Cel03] G. K. **Celler**, S. **Cristoloveanu**, "Frontiers of silicon-on-insulator", *Journal of Applied Physics*, vol. 93, No. 9, May 2003, pp. 4955-4978.

[Che02] W. **Chen**, G. **De Geronimo**, Z. **Li**, P. **O'Conno**r, V. **Radeva**, P. **Rehak**, G. C. **Smith**, B. **Yu**, "Active Pixel Sensors on High-Resistivity Silicon and their Readout", *IEEE Trans. Nucl. Sci.*, vol. 49, No. 3, June 2002, pp. 1006-1011

[Cho83] K. L. **Chopra**, S. **Major** and D. K. **Pandya**, "Transparent Conductors – A Status Review", *Thin Solid Films*, vol. 102, 1983, pp. 1-46

[CMS98] "CMS, The Tracker System Project", *Technical Design Report, CERN/LHCC/98-006*, 1998.

[CXRO] http://www.cxro.lbl.gov/optical_constants

[Dam95] C. J. S. **Damerell**, "Vertex detectors: The state of the art and future prospects", *RAL-P-95-008*, 1995.

[Dam98] C. J. S. **Damerell**, "Charge coupled devices as particle tracking detectors", *Rev. Sci. Instr., vol. 69*, 1998, pp. 1549-1573.

[Dem96] W. **Demtröder**, *Laser Spectroscopy: Basic Concepts and Instrumentation*, 2nd Edition, Springer-Verlag Berlin Heidelberg, Germany, 1996

[Dep04] G. **Deptuch**, "Direct Detection of Electrons in Backside Illuminated CMOS Imagers", *Proc. BNL, 30. Oct. 2004*.

[DeG01] G. **De Geronimo**, P. **O'Connor**, A. **Kandasamy**, "Analog CMOS Peak Detect and Hold Circuits. Part 1. Analysis of the Classical Configuration", *Nucl. Instr. and Meth. in Phys. Res.,* A 484, *Elsevier*, 2002, pp. 533-543

[DeG02] G. **De Geronimo**, P. **O'Connor**, A. **Kandasamy**, "Analog CMOS Peak Detect and Hold Circuits. Part 2. The Two-Phase Offset-Free and derandomizing Configuration", *Nucl. Instr. and Meth. in Phys. Res.,* A 484, *Elsevier*, 2002, pp. 544-556

[Die00] B. **Dierickx** – Fill Factory Image Sensors, "CMOS Image Sensors, Limits of Performance", *Photonics West 2000 Short Course*, 2000

[Dor94] R. G. **Dorsch**, G. **Hausler**, J. M. **Herrmann**, "Laser Triangulation: Fundamental Uncertainty in Distance Measurements", *Appl. Opt.*, vol. 33, 1994, pp. 1306-1314

[Dos89] J. **Dostál**, *Operationsverstärker*, VEB Verlag Technik, Berlin, 1989

[Dur03] D. **Durini**, *Research on Novel Metal-Insulator-Silicon Sensors*, M.Sc. thesis, sup. Dr. O. Malik, National Institute of Astrophysics, Optics and Electronics (INAOE), Mexico, Nov. 2003

[Dur05] D. **Durini**, A. **Kemna**, W. **Brockherde**, B. **Hosticka**, "CMOS integrated pixel array for low-level radiation detection using 'time compression' parametric amplification", *Proc. 10th European Symposium on Semiconductor Detectors (SDS)*, Wildbad Kreuth, Germany, June 2005

[Dur06] D. **Durini**, A. **Kemna**, W. **Brockherde**, B. **Hosticka**, "CMOS integrated pixel array for low-level radiation detection using 'time compression' parametric amplification", *Nucl. Instr. Meth. Phy. Res.*, A568, 2006, pp. 112-117

[Dur07E] D. **Durini**, W. **Brockherde**, B. J. **Hosticka**, "MOS-Capacitor Based CMOS Time-Compression Photogate Pixel for Time-of-Flight Imaging", Proc. *33rd European Solid state Circuit Conference (ESSCIRC) & 37th European Solid-State Device Research conference (ESSDERC), Munich, Germany*, Sept. 2007, pp. 340-343

[Dur07C] D. **Durini**, W. **Brockherde**, B. J. **Hosticka**, "SOI Pixel Detector Based on CMOS Time-Compression Charge-Injection", *Proc. European Conference on Circuit Theory and Design ECCTD 2007, Seville, Spain*, August 2007, pp. 946-949

[Dur07P] D. **Durini**, B. J. **Hosticka**, "Photodetector Structures for Standard CMOS Imaging Applications", *Proc. IEEE PRIME 2007, Bordeaux, France,* July 2007, pp. 193-196

[Dur07S] D. **Durini**, K. E. **Enowbi**, W. **Brockherde**, B. J. **Hosticka**, "CMOS Silicon-On-Insulator technology: An Alternative for NIR Quantum Efficiency Enhanced CMOS Imaging Pixel Detectors", *Proc. EOS Conference on Frontiers in Electronic Imaging, World of Photonics Congress 2007, Munich, Germany*, June 2007, pp. 26-27

[Edl04] F. **Edling**, *DIXI – a Hybrid Pixel Detector for X-ray Imaging*, Dissertation, Uppsala University, Faculty of Science and Technology, Comprehensive Summary 1018, 2004

[Eic93] H. J. **Eichler**, A. **Fleischer**, J. **Kross**, M. **Krystek**, H. **Lang**, H. **Niedrig**, H. **Rauch**, G. **Schmahl**, H. **Schoenebeck**, E. **Sedlmayer**, H. **Weber**, K. **Weber**, *Optik*, Vol. 3: *Bergmann, Schaefer: Lehrbuch der Experimentalphysik*, de Gruyter, Berlin, 1993

[ElG02] A. **El Gamal**, "Trends in CMOS Image Sensor Technology and Design", *Proc. Digest. Intern. Electron Devices Meeting, IEDM '02*, 2002, pp. 805-808

[Elk04] O. **Elkhalili**, O. M. **Schrey**, P. **Mengel**, M. **Petermann**, W. **Brockherde**, B. J. **Hosticka**, "A 4x64 Pixel CMOS Image Sensor for 3-D Measurement Applications", *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 7, July 2004, pp. 1208-1212

[Elk05] O. **Elkhalili**, *Entwicklung von optischen 3D CMOS-Bildsensoren auf der Basis der Pulslaufzeitmessung*, Ph.D. thesis, adv. Prof. B. J. Hosticka, Ph.D., University of Duisburg-Essen, April 2005

[Elk06] O. **Elkhalili**, O. M. **Schrey**, W. **Ulfig**, W. **Brockherde**, B. J. **Hosticka**, "A 64x8 3-D CMOS Time of Flight Image Sensor for Car Safety Applications", *Proc. 32nd European Solid state Circuit Conference (ESSCIRC), Montreaux, Switzerland*, Sept. 2006, pp. 568-571

[Fan77] J. C. C. **Fan**, J. B. **Goodenough**, "X-Ray Photoemission Spectroscopy Studies of Sn-doped Indium Oxide Films", *Journal of Applied Physics*, vol. 48 (8), 1977, pp. 3524-3531

[Fis96] P. **Fischer**, "An area efficient 128 channel counter chip", *Nucl. Inst. Meth. A378*, 1996, pp. 297-300

[Fon06] B. A. **Fontem**, *Characterization and Improvement of a New Photodiode Readout Circuit for CMOS Time-Of-Flight Range Sensors with Reduced NEP*, Bachelor Thesis, University of Duisburg-Essen, adv. Prof. B. J. Hosticka, Ph.D. (supervisor W. Ulfig), Duisburg, August 2006

[Fos97] E. **Fossum**, "CMOS Image Sensors: Electronic Camera-On-A-Chip", *IEEE Transactions on Electronic Devices* 44, Oct. 1997, pp. 1689-1698

[Fos84] E. **Fossum** and R. **Baker**, "Measurement of hole leakage and impact ionisation currents in bistable metal-tunnel oxide-semiconductor junctions", *IEEE Trans. Electron Devices*, vol. ED-31, No. 9, 1984, p. 1168

[Fow04] B. **Fowler** *et al.*, "An ultra low noise high speed CMOS linescan sensor for scientific and industrial applications", *Proc. SPIE*, 2004.

[Fox98] E. C. **Fox** *et al.*, "A high speed linear CCD sensor with pinned photo-diode photosite for low lag and low noise imaging", *Proc. SPIE*, vol. 3301, 1998, p. 17.

[Fuj00] I. L. **Fujimori**, C. C. **Wang**, C. G. **Sodini**, "A 256×256 CMOS Differential Passive Pixel Imager with FPN Reduction Techniques", *IEEE J. Solid-State Circuits*, vol. 35, No. 12, Dec. 2000, pp. 2031-2037.

[Gat83] E. **Gatti**, P. **Rehak**, "Semiconductor Drift Chamber – an application of a novel charge transport scheme", *Proc. 2nd Pisa Meeting on Advanced detectors, Grosseto, Italy, June 3-7, 1983*.

[Gat84] E. **Gatti**, P. **Rehak**, "Semiconductor Drift Chamber – an application of a novel charge transport scheme", *Nuclear Instruments and Methods in Physics, Research Section A*, Vol. 225, No. 3, Sep. 1984, pp. 608-614.

[Gat89] E. **Gatti**, P. **Rehak**, M. **Sampietro**, "Double particle resolution in semiconductor drift detectors", *Nuclear Instruments and Methods in Physics, Research Section A*, Vol. 295, No. 3, Nov. 1990, pp. 489-491

[Gom02] A. **Gombert**, "Mikrooptik im großen Stil", *Physik Journal* 1, Nr. 9, 2002, pp. 37-42

[Gre95] M.A. **Green** *et* M. **Keevers**, "Optical properties of intrinsic silicon at 300 K", *Progress in Photovoltaics*, Vol. 3, No. 3, 1995, pp.189-92

[Gre00] J. **Gregory**, B. **Burke**, B. B. **Kosicki**, and R. K. **Reich**, "Developments in X-Ray and Astronomical CCD Imagers", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and associated Equipment* 436, January 2000, pp. 1-8.

[Gys01] T. **Gys**, "The pixel hybrid photon detectors for the LHCb-RICH project", *Nucl. Inst. Meth. A465*, pp. 240-246, 2001.

[Hat00] K. **Hatano**, M. **Furumiya**, I. **Murakami**, T. **Kawasaki**, C. **Ogawa**, and Y. **Nakashiba**, "A 1/3-inch 1.3-M pixel single-layer electrode CCD with a high-frame-rate skip mode", in *ISSCC Dig*., Feb. 2000, pp. 112-113

[Hec89] E. **Hecht**, *Optik*, transl. F. Siemsen (original title: *Optics*), Addison-Wesley, Germany, 1989

[Hel03] H. **Helmers** and M. **Schellenberg**, "CMOS vs. CCD Sensors in Speckle Interferometry", *Optics & Laser Technology* 35, April 2003, pp. 587-595.

[Hen93] B.L. **Henke**, E.M. **Gullikson**, and J.C. **Davis**, "X-ray interactions: photoabsorption, scattering, transmission, and reflection at E=50-30000 eV, Z=1-92", *Atomic Data and Nuclear Data Tables*, vol. 54, No.2, July, 1993, pp. 181-342.

[Hol03] P. **Holl**, P. **Fischer**, R. **Hartmann**, G. **Hasinger**, J. **Kollmer**, N. **Krause**, P. **Lechner**, G. **Lutz**, N. **Meidinger**, I. **Peric**, R. **Richter**, H. **Soltau**, L. **Strüder**, J. **Treis**, J. **Trümper**, N. **Wermes**, "Active pixel sensors for imaging X-ray Spectrometers", *Proc. SPIE, vol. 4851*, 2003, pp. 770-778

[Hos07] B. J. **Hosticka**, "Analog Circuits for Sensors", *Proc. ESSCIRC/ESSDERC 2007 Munich, Germany* (invited talk), Sept. 2007, pp. 97-102

[Hur92] G. A. M. **Hurkx**, H. C. **de Graaff**, W. J. **Kloosterman**, and M. P. G. **Knuvers**, "A New Analytical Diode Model Including Tunneling and Avalanche Breakdown", *IEEE Trans. On Electron Devices, Vol. 39, No. 9*, Sept. 1992, pp. 2090-2098

[Hor00] R. I. **Hornsey**, *Design and Fabrication of Integrated Image Sensors*, Course Notes, Electrical and Computer engineering, University of Waterloo, Canada.

[IMS03] *Design Manual C0512M+*, Revision 4.0, Author: S. Linnenberg, Fraunhofer IMS, Duisburg, 2003

[ITOFhG] *Hochleitfähige transparente Schichten aus Indium-Zinn-Oxid (ITO) für Verdrahtung und MOS-Gates in CMOS Kameras*, Abschlussbericht zum Mittelstandsorientiertes Eigenforschungsprojekt (MEF), Verfasser: S. Dreiner (IMS), C. May (IPMS), Fraunhofer Gesellschaft, 2007

[Ino99] I. **Inoue**, H. **Ihara**, H. **Yamashita**, T. **Yamaguchi**, H. **Nozaki**, R. **Miyagawa**, "Low dark current pinned photo-diode for CMOS image sensor", Mitsubishi Corporation, 1999

[Jan04] Jim **Janesick**, *Scientific CMOS Pixels*, *Sarnoff Corporation*, lecture given on July 1st, 2004.

[Jan03] Jim **Janesick**, "Charge coupled CMOS and hybrid detector arrays", *SPIE, Focal Plane Arrays for Space Telescope*, paper No. 5167-1, San Diego, Aug. 2003

[Jin06] R. P. **Jindal**, "Compact Noise Models for MOSFETs", *IEEE Trans. On Electron. Dev.*, vol. 53, No. 9, Sept. 2006, pp. 2051-2061

[Kab07] S. T. **Kabadjeu**, *Measurement of minority carriers recombination and generation lifetimes to be used for mathematical modeling of dark currents present in photosensitive test structures fabricated in a 0.5µm standard CMOS process*, Bachelor Thesis, adv. Prof. B. Hosticka, Ph.D (supervisor: D. Durini), University of Duisburg-Essen, April 2007

[Ken99] C. **Kenney**, S. **Parker**, J. **Segal**, C. **Storment**, "Silicon detectors with §-D electrode arrays: fabrication and initial test results", *IEEE Trans. Nucl. Sci. vol.46(4)*, 1999, pp. 1224-1236.

[Ken03] C. **Kenney**, E. **Westbrook**, J. D. **Segal**, S. I. **Parker**, J. **Morse**, J. **Hasi**, C. **Da Via**, "First results from active-edge, planar radiation sensors", *Proc. IEEE Nuclear Science Symposium Portland 2003*.

[Kle02] S. **Kleinfelder**, H. **Bichsel**, F. **Bieser**, H. S. **Matis**, G. **Rai**, F. **Retiere**, H. **Wieman**, E. **Yamamoto**, „Integrated X-ray and charged particle active pixel CMOS sensor arrays using an epitaxial silicon sensitive region", *Proc. SPIE Hard X-Ray and Gamma Ray Detector Physics IV, Seattle, WA, July 2002*

[Kod94] **Eastman Kodak Company** – Microelectronics Technology Division, *"Solid State Image Sensors Terminology", Application Note*, Rochester, NY, December 8th, 1994

[Kit96] C. **Kittel**, *Introduction to Solid State Physics*, 7th Edition, John Wiley & Sons Inc., USA, 1996

[Kwo03] H. **In Kwon**, "Dark current characterization of the CMOS APS Imagers fabricated using a 0.18 µm CMOS technology", *SMDL Annual Report 2003*, Seoul, 2003

[Lai05] J. **Lai**, A. **Nathan**, "Reset and Partition Noise in Active Pixel Image Sensors", *IEEE Trans. On Electron Dev.*, pp. 1-4, 2005

[Lal97] P. **Lalanne**, J. C. **Rodier**, "CMOS photodiodes based on vertical p-n-p junctions", *Second Workshop on Optics and Computer Science (WOCS)*, Geneva, Switz., July, 1997

[Lan01] R. **Lange**, P. **Seitz**, "Solid-State Time-of-Flight range Camera", *IEEE Journal of Quantum Electronics*, vol. 37, No. 3, March 2001, pp. 390-397

[Lea94] W. M. **Leach**, Jr., "Fundamentals of Low-Noise Analog Design", *Proceedings of the IEEE*, Vol. 82, No. 10, Oct. 1994, pp. 1514-1538

[Lee99] T. H. **Lee**, R. M. **Guidash**, P. P. **Lee**, "Partially pinned photodiode for solid state image sensors", U.S. Patent 5 903 021, 1999.

[Lin03] G. **Lindström**, "Radiation damage in silicon detectors", *Nucl. Inst. Meth. A512*, 2003, p. 92

[Lor07] http://www.lot-oriel.com

[Lou03] N. V. **Loukianova**, H. O. **Folkerts**, J. P. V. **Maas**, D. W. E. **Verbugt**, A. J. **Mierop**, W. **Hoekstra**, E. **Roks**, A. J. P. **Theuwissen**, "Leakage Current Modelling of Test Structures for Characterization of Dark current in CMOS Image Sensors", *IEEE Trans. On Electron Devices*, vol. 50, No.1, Jan. 2003, pp. 77-83.

[Lul00] T. **Lulé**, S. **Benthien**, H. **Keller**, F. **Mütze**, P. **Rieve**, K. **Seibel**, M. **Sommer**, M. **Böhm**, "Sensitivity of CMOS Based Imagers and Scaling Perspectives", *IEEE Trans. Electron Devices*, Vol. 47., No. 11, Nov. 2000, pp. 2110-2122.

[Lum88] D. H. **Lumb**, A. D. **Holland**, "Background rejection techniques in CCD X-ray detectors for Astronomy", *IEEE Trans. Nucl. Scienc.*, vol. 35, No. 1, Feb. 1988, pp. 534-538.

[Lun95] M. W. **Lund**, *More than one ever wanted to know about X-ray*, MOXTEC, Inc. Publications, 1995.

[Ma03] J. **Ma**, *Snapshot on Solid-Sate Image Sensors*, Term Paper prepared for Physics687 (Physics of Materials), advisor: Prof. N. M. Ravindra, New Jersey Institute of Technology, 2003.

[Mag03] P. **Magnan**, "Detection of visible photons in CCD and CMOS: A comparative view", *Nuclear Instruments and Methods in Physics Research A 504*, *Elsevier*, 2003, pp. 199-212.

[Mal03] A. **Malik**, "Conception of Optical Sensors Based on Transient Processes in MIS Structures", *Proc. 16th Int. Conf. on Solid-State Transducers, EUROSENSORS XVI*, Prague, 15-18 Sept. 2003, pp. 731-734

[Mal04] A. **Malik**, V. **Grimalsky**, A. **Torres Jácome**, D. **Durini**, "Theoretical modeling and experimental investigation of MIS radiation sensor with giant internal signal amplification", *Sensors&Actuators A114, Elsevier*, 2004, pp. 319-336

[Mar04] J. **Marczewski** *et al*., "SOI Active Pixel Detectors of ionizing radiation – technology & design development", *Proceedings IEEE Vertex 2004*, 2004, pp. 365-367

[Mat03] H. S. **Matis**, F. **Bieser**, S. **Kleinfelder**, G. **Rai**, F. **Retiere**, H. G. **Ritter**, K. **Singh**, S. E. **Wurzel**, H. **Wieman**, E. **Yamamoto**, "Charged particle detection using a CMOS active pixel sensor", *IEEE Trans. Nucl. Sci. vol. 50, No. 4*, pp. 1020-1025, Aug. 2003

[Mba06] E. M. **Mbanya**, *Development of a minority carriers generation lifetime and surface velocity measuring system for CMOS processes to determine the minority carrier generation lifetimes and surface generation velocities of a 0.6µm CMOS standard process*, Bachelor Thesis, University of Duisburg-Essen, adv. Prof. B. Hosticka, Ph.D. (supervisor D. Durini), August 2006

[McK82] J. P. **McKelvey**, *Solid State and Semiconductor Physics*, Krieger Pub Co., USA, 1982

[Mea85] C. **Mead**, "A sensitive electronic photoreceptor", *1985 Chapel Hill Conference on VLSI*, H. Fuchs ed., Computer Science Press, Rockville, 1985, pp. 463-471.

[Mei01] E. J. **Meisenzahl**, W. C. **Chang**, W. **DesJardin**, H. Q. **Doan**, J. P. **Shepherd**, E. G. **Stevens**, "A 3.2 million pixel full-frame true 2ϕ CCD image sensor incorporating transparent gate technology", *Proceedings of SPIE Volume 3965*, 2001, pp. 92-100

[Men01] P. **Mengel**, G. **Doemens**, L. **Listl**, "Fast range imaging by CMOS sensor array through multiple double short time integration (MDSI)", *Proc. IEEE Int. Conf. In Image Processing (ICIP2001), Thessaloniki (Greece)*, 2001, pp. 169-172

[Men88] R. **Menozzi**, L. **Selmi**, E. **Sangiorgi**, G. **Crisenza**, T. **Cavioni**, B. **Riccó**, "Layout Dependence of CMOS Latch-up", *IEEE Transactions on Electron Devices,* vol. ED-35, Nov. 1988, pp. 1892-1901

[Mey03] G. **Meynants**, B. **Dierickx**, A. **Alaerts**, D. **Uwaerts**, S. **Cos**, D. **Scheffer**, S. **Noble**, "A 35mm 13.89 Million Pixel CMOS Active Pixel Image Sensor", *IEEE Workshop on CCD & AIS, May 15-17, 2003, Elmau, Germany*.

[Miy95] R. **Miyagawa** and T. **Kanade**, "Integration time based computational image sensor", *1995 IEEE Workshop on CCDs and Advanced Image Sensors*, Dana Point, Ca., April 20-22, 1995

[Mot93] C. D. **Motchenbacher**, J. A. **Connelly**, *Low-Noise Electronic System Design*, John Wiley & Sons, USA, 1993

[Mot98] *Motorola*, "MCM20008, 1/3" Colour VGA image sensor", Tech. Datasheet, 1998

[Nic05] C. **Niclass**, A. **Rochas**, P. A. **Besse**, E. **Charbon**, "Design and Characterization of a CMOS 3-D Image Sensor Based on Single Photon Avalanche Diodes", *IEEE Journal of Solid-State Circuits*, vol. 40, No. 9, September 2005, pp. 1847-1854

[Nie05] H. **Niemiec** *et al*., "Monolithic active pixel sensor realized in SOI technology – concept and verification", *Elsevier Microelectronics Reliability 45*, 2005, pp. 1202-1207

[Onlin] http://onlineheavytheory.net/silicon.html

[Pai00] B. **Pain**, G. **Yang**, T. **Cunningham**, B. **Hancock**, "Photodiode-based CMOS APSs with zero-lag, low-noise, high-linearity design", *NASA Tech. Briefs*, ABP, Nov. 2000

[Pau99] A. **Pauchard**, P. A. **Besse**, R. S. **Popovic**, "A Silicon Blue/UV Selective Stripe-Shaped Photodiode", *Sensors and Actuators A, Physical*, vol. 76, 1999, pp. 172-177

[Pri03] G. **Prigozhin**, N. R. **Butler**, S. E. **Kissel**, G. R. **Ricker**, "An experimental study of charge diffusion in the undepleted silicon of X-ray CCDs", *IEEE Trans. Electr. Devices*, vol. 50, No. 1, Jan. 2003, pp. 246-253

[Ram01] S. **Ramaswami**, S. Agwani, L. Loh, N. Bossemeyer "Characterization of Pixel Response Time and Image Lag in CMOS Sensors", *Image Capture Operation, Motorola Inc.*, Chandler, AZ.

[Reh04] P. **Rehak**, "Silicon radiation Detectors", *IEEE Trans. Nucl. Sci.*, vol. 51, No. 5, Oct. 2004, pp. 2492-2497.

[Rop99] **Roper Scientific, Inc.** "What should you know about ITO?", *Technical Notes*, 1999

[Saw07] T. **Sawada**, S. **Kawahito**, M. **Nakayama**, K. **Ito**, I.A. **Halin**, M. **Homma**, T. **Ushinaga**, and Y. **Maeda**, "A TOF range image sensor with an ambient light charge drain and small duty-cycle light pulse," *Proc. Int. Image Sensor Workshop*, Maine, June 2007, pp.254–257

[Sch97] D. K. **Schroder**, "Carrier Lifetimes in Silicon", *IEEE Transactions on Electron Devices*, Vol. 44, No. 1, January 1997, pp. 160-170

[Sch98] D. K. **Schroder**, *Semiconductor Material and Device Characterization*, 2nd Edition, John Wiley & Sons, Inc., USA, 1998

[Sel04] P. **Seller**, "Investigation of a Low-Energy X-ray Spectrometer based on Pixellated Hybrid Silicon Detectors", *Rutherford Appleton Laboratory,* Technical Report, RAL-TR-2004-014, 2004.

[Sin96] J. **Singh**, *Optoelectronics. An Introduction to Materials and Devices*. McGraw Hill Companies, Inc., Singapore, 1996

[Sin03] J. **Singh**, *Electronic and Optoelectronic Properties of Semiconductor Structures*, Cambridge University Press, UK, 2003

[Sno92] W. **Snoeys**, J. **Plummer**, S. **Parker**, C. **Kenney**, "A new integrated pixel detector for high energy physics", *IEEE Trans. Nucl. Sci. vol. 39*, 1992, pp. 1263-1269

[SOI] www.soitec.com

[Sze02] S. M. **Sze**, *Semiconductor devices. Physics and technology*, 2nd Edition, John Wiley & Sons, USA, 2002

[Szc83] J. **Szczyrbowski**, A. **Dietrich**, H. **Hoffmann**, "Optical and Electrical Properties of r.f. Sputtered indium-Tin Oxide Films", *Phys. Stat. Sol.* (a), vol. 78, 1983, pp. 243-252

[Tay96] G. N. **Taylor** *et al.*, "Radiation induced bulk damage in silicon detectors – RD2 Collaboration", *Nucl. Instr. & Meth.*, vol. A383, 1996, pp. 144-154.

[The96] A. J. P. **Theuwissen**, *Solid-State Imaging with Charge-Coupled-Devices*, Kluwer Academic Publishers, 1996

[Tor03] M. Y. **Torres Padilla**, *Fabricación y caracterización de películas de óxido de indio-estaño para aplicaciones optoelectrónicas*, M.Sc. thesis, National Institute of Astrophysics, Optics and Electronics (INAOE), Mexico, 2003

[Tuo03] E. **Tuominen**, *Development of Radiation Hard Radiation Detectors – Differences between Czocralski Silicon and Float Zone Silicon*, Dissertation, Helsinki Institute of Physics, Finland, Oct. 2003.

[Tur04] R. **Turcheta**, "CMOS Monolithic Active Pixel Sensors (MAPS): new "eyes" for science?", CCLRC, *Proc. Vertex 2004, Como (Italy), 13th-18th Sept. 2004*

[VdW76] F. **Van de Wiele**, "Photodiode Quantum Efficiency" in "Solid State Imaging", *NATO Advanced Study Institute on Solid State Imaging*, Ed. P. Jespers, F. Van de Wiele, M. White, Noordhoff, Leyden, 1976, pp. 47-90

[Wad84] M. **Wadsworth**, R. D. **McGrath**, "Charge Coupled Devices for X-ray Imaging", *IEDM Proceedings*, 1984, pp. 20-24.

[War93] V. **Ward**, M. **Syrzycki** and G. **Chapman**, "CMOS Photodetector with built-in light adaptation mechanism", *Microelectonics J.*, vol. 24(5), August 1993, pp. 547-553.

[Wer02] N. **Wermes**, "Design and prototype performance of the ATLAS pixel detector", *Nuclear Inst. Meth. A447*, pp. 121-128, 2002.

[Wer04] N. **Wermes**, "Trends in pixel Detectors: Tracking and Imaging", *IEEE Trans. Nucl. Sci.*, Vol. 51, No. 3, 2004, pp. 1006-1015.

[Wes99] E. M. **Westbrook**, "Performance characteristics needed for protein crystal diffraction x-ray detectors", *Proc. SPIE **3774***, 1999, pp. 2-16.

[Whi70] M. H. **White**, D. R. **Lampe**, *et al*., *IEEE Trans. Solid State Circuits SC-9*, 1970, p. 1

[Won96] H. S. **Wong**, „Technology and Device Scaling Considerations for CMOS Imagers", *IEEE Trans. Electron Devices*, Vol. 43, No. 12, Dec. 1996, pp. 2131-2142.

[Wol89] C. **Wolfe**, N. Jr. **Holonyak** and G. **Stillman**, *Physical Properties of Semiconductors*, Prentice-Hall Inc., NJ, 1989, p. 214-219

[XFEL] http://xfel.desy.de

[Yad04] O. **Yadid-Pecht** *et* R. **Etienne-Cummings**, *CMOS Imagers. From Phototransduction to Image Processing*, Kluwer A. P., NL, 2004

[Yad92] O. **Yadid-Pecht**, "Widening the dynamic range of pictures", in *Proc. SPIE/IS&T Symp. On Electronic Imaging: Science and Technology, San Jose, Ca., Feb. 9-14*, *SPIE vol. 1656*, 1992, pp. 374-382

[Yan94] W. **Yang**, "A wide-dynamic-range, low power photosensor array", *IEEE ISSCC vol. 37*, 1994, pp. 230-231

[Yon00] K. **Yonemoto**, H. **Sumi**, "A CMOS Image Sensor with a Simple Fixed-Pattern-Noise-Reduction Technology and a Hole Accumulation Diode", *IEEE Journal of Solid-State Circuits*, vol. 35, No.12, Dec. 2000, pp. 2038-2043

[Zer66] M. **Zerbst**, "Relaxation Effects at Semiconductor-Insulator Interfaces", *Z. Angew. Phys. **22***, May 1966, pp. 30-33

APPENDIXES

A Optical Sensitivity Measuring Station for the Soft-UV (300nm-450nm) Part of the Spectra

A.1 Apparatus

The optical sensitivity measuring station for the soft-UV (λ = 350nm-450nm) part of the spectra consists of:

- A PC containing *National Instruments LabView 7.1* software, *general purpose interface bus* (GPIB) connection facility and the *National Instruments* data acquisition card;
- *LOT-Oriel* 1000W Hg(Xe) ozone-free (OF) short-arc lamp, original model-Nr.: 6271H, current model-Nr.: LSB751, working at 28.5A, 32-38V, with an approx. 40.000lm flux;
- *Lamp-adapter* original model-Nr: 6162, current model-Nr.: LSA555 for the lamp housing;
- *Lamp housing LOT-ORIEL*, original model-Nr: 66921, current model-Nr.: LSH501, with condensing optics;
- Light intensity controller: *ORIEL Instruments*, Model: 68850;
- Arc lamp power supply: *ORIEL Instruments*, Model: 68920;
- Cooler *HAAKE*, class D;
- Monochromator*: ORIEL Instruments Corner Stone 1/8m*, Model: 74000;
- Semiconductor parameter analyser*, Hewlett-Packard HP4145B;*
- Measurement black-box;
- Opto-mechanical adapter which couples the monochromator radiation output to the black-box and the optical system built on an optical breadboard;
- *Optical breadboard system*: 1 bi-convex lens, 1 plane-convex lens, and 3 optical diaphragms.

A.2 Radiation Related Specifications

The light source used for this measurement station is a 1000W Hg(Xe) ozone-free (OF) short-arc lamp, original *Oriel Instruments* model-Nr.: 6271H, current *LOT-Oriel* model-Nr.: LSB751, working at 28.5A, 32-38V, with an approx. 40.000lm flux [Lor07].

Short arc lamps are the brightest manufactured sources, discounting lasers. Light is generated by a discharge arc burning in gas between two electrodes. This lamp type has two remarkable features: high output in the UV-VIS, and small radiating arc region. The anode and cathode, made of tungsten, are sealed in a clear quartz envelope (Figure A. 1). Quartz is used for mechanical and thermal durability. The tungsten used in the cathode is doped with materials such as thorium to enhance electron emission. The anode is more massive than the cathode to withstand the electron bombardment and efficiently dissipate the heat produced. When the lamps run, the internal pressure increases to some tens of bars.

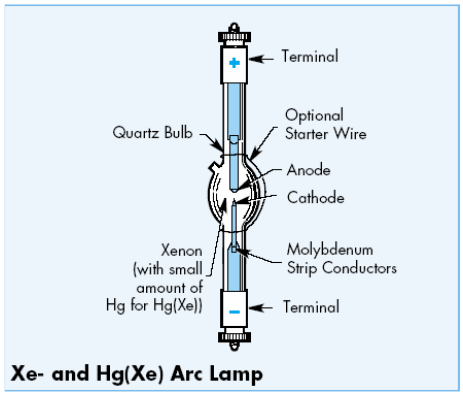


Figure A. 1 - *LOT-Oriel* 1000W Hg(Xe) ozone-free (OF) short-arc lamp schematic diagram [Lor07].

The high pressures demand special care in the handling and operation of these lamps. Xenon lamps are filled with purified xenon at some bars. Xenon and Hg(Xe) lamps have supra atmospheric pressure even when cold (up to 8 bar). The pressure triples during operation. Xenon lamps operate with the anode at the top. The small intense arcs radiate like 5500 – 6000 K full radiators with some xenon lines superimposed. The xenon lines dominate between 750 and 1000 nm, but the spectrum is almost featureless through the ultraviolet and visible. Ozone free lamps have bulbs that absorb below 300nm and have a cut-off around 250nm. The physical exact measures (left) and the wavelength dependent spectral irradiance (right) of the *LOT-Oriel* 1000W Hg(Xe) ozone-free (OF) short-arc lamp can be observed in Figure A. 2 [Lor07].

The lamp housing *LOT-ORIEL*, original model-Nr: 66921, current model-Nr.: LSH501, with condensing optics holds the ignitor, collecting and collimating optics, rear reflector, cooling fan, external lamp and reflector adjusters as well as all the necessary electronics, as shown in Figure A. 3. A spherical reflector collects the output from the rear of the lamp and focuses it on or near the arc for collection by the condenser, as observed in Figure A. 3(a). Output is increased by as much as 60%. The lamp is held by an adapter which places the arc on the condenser axis, current adapter model-Nr.: LSA555. The UV quartz condenser with F/1.0 and 50mm aperture, current model *LOT-Oriel* LSC510, is intended for collimated beams, but can also be positioned for compensating focal length change due to dispersion and to produce a diverging or converging beam. The glass condensers do not transmit below 350 nm, reason because of which a quartz one was chosen.

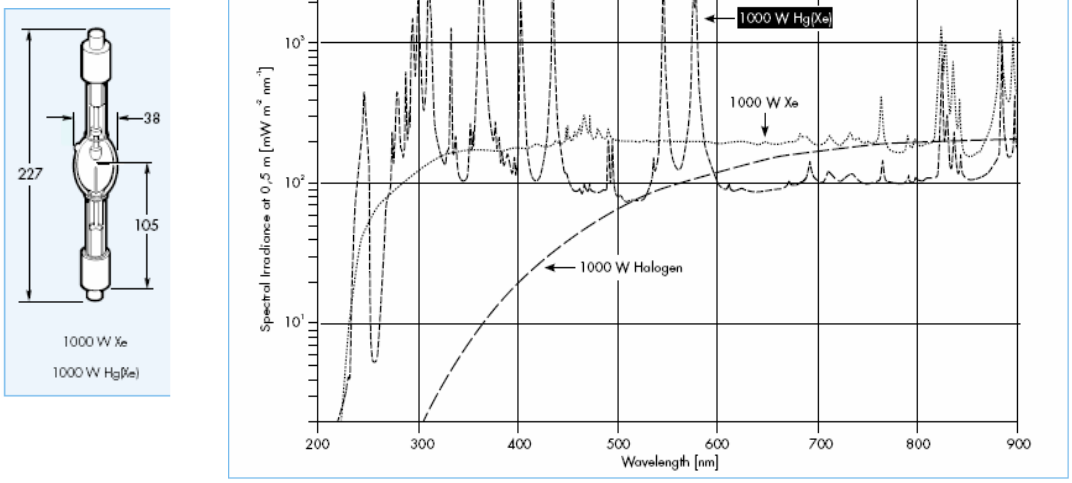
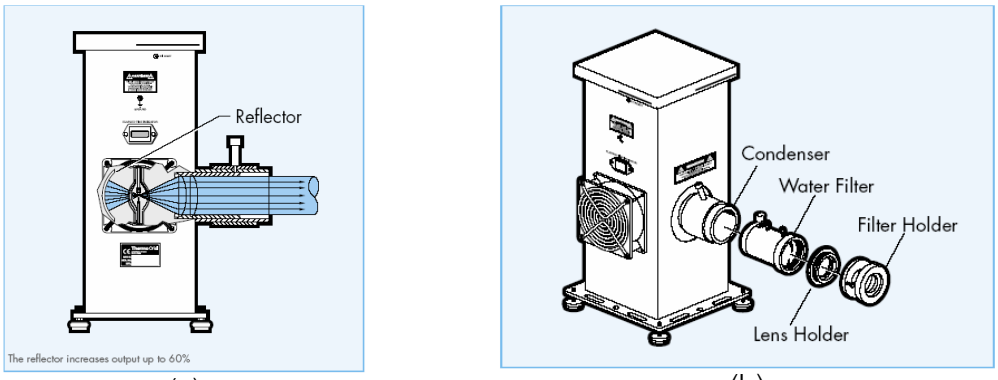


Figure A. 2 - Physical measures (left) and the wavelength dependent spectral irradiance (right) of the *LOT-Oriel* 1000W Hg(Xe) ozone-free (OF) short-arc lamp [Lor07].

For best quality images, the condenser as a collimator together with a secondary focussing lens is being used, namely the plane-convex *Suprasil* lens with a 50.8mm diameter, focus distance of 200mm (589nm), and an average thickness of 6.4mm, model-Nr.: 3-41790. The refractive index of quartz increases dramatically as wavelength drops below 300nm. The focal length of a quartz lens therefore decreases significantly with decreasing wavelength. In the case of interest, the 38mm in diameter of the lamp bulb allows to create a collimated beam for wavelengths even below 300 nm.



(a) (b)

Figure A. 3 - (a) Spherical reflector mechanism [Lor07], and (b) additional optic used together with the *LOT-ORIEL* lamp housing [Lor07].

The bulb temperature of arc lamps should not exceed 600–900°C, because the bulb then is not able to withstand the high gas pressure due to temperature related change of quartz structure (recrystallisation). Because of potential current conductor oxidation, the socket temperature must not exceed 230°C. The lamp used require bulb cooling provided by baffled air flow.

Liquid filters are useful for applications where the infrared is not required, and its heating effect is a problem, as it is the case. The filter consists of a cell that holds the liquid and two fused silica windows transmitting down to 250nm.

The cell has an external chamber for cooling water circulation and a pressure relief valve. External cooling is needed to remove the energy absorbed by the liquid when filtering continuous high power (>200W) sources, as it is the case. The cooling in this case is provided through the *HAAKE*, Class D aluminium cooler which uses distilled water.

The monochromator *ORIEL Instruments Corner Stone 1/8m*, model: 74000, currently *LOT-ORIEL* model-Nr.: MSH101, is a 130mm, f/3.7 dual grating motorized monochromator. It offers 0.5nm resolution with a 1200l/mm grating. The MSH101 is a compact device, it can be fully remote controlled (IEEE-488 and RS232 interface) and comes with an integrated electronic shutter. It supports two gratings simultaneously. The gratings are individually replaceable. The MSH101 is ideal for both emission and detection. It presents a modified *Ebert* design, an operating range between 185nm and 23mm wavelengths (with interchangeable gratings), a grating dependent dispersion of 6,5 nm/mm for 1200 l/mm grating at blaze wavelength, an accuracy at 546nm of ±0,5nm, repeatability of ±0,11nm, and a drive step size of 0,1nm. The grating size is 30x30 mm^2, and presents 1200 l/mm, a 350nm blaze wavelength, and is indicated for optimum wavelengths between 200nm and 1600nm. The original grating's model-Nr. was *ORIEL Instruments* 74024, currently renamed into *LOT-Oriel* model-Nr.: MSGx15, presenting a 350nm blaze wavelength.

The normally available liquid light guides are dedicated to operations in the visible range spectra and cannot support temperatures of the input window above 40°C. Thus, the IR-radiance above 680nm must be filtered out completely. A similar effect takes place for radiations bellow 340nm (VIS models). So, in order to transmit radiations at wavelengths between the 300nm and 450nm, the liquid light guide had to be omitted. Instead, an opto-mechanical adapter was used, which couples the monochromator radiation output to the black-box and the optical breadboard system.

In order to further align and homogenise the radiation impinging on the test structures of interest, an additional optical system was built on a breadboard and allocated between the output of the monochromator and the test structure. It consists of a bi-convex lens, a plane-convex one, and three optical diaphragms, as shown in Figure A. 4. As the glass lenses do not transmit below 350nm, quartz ones were chosen for this optical system.

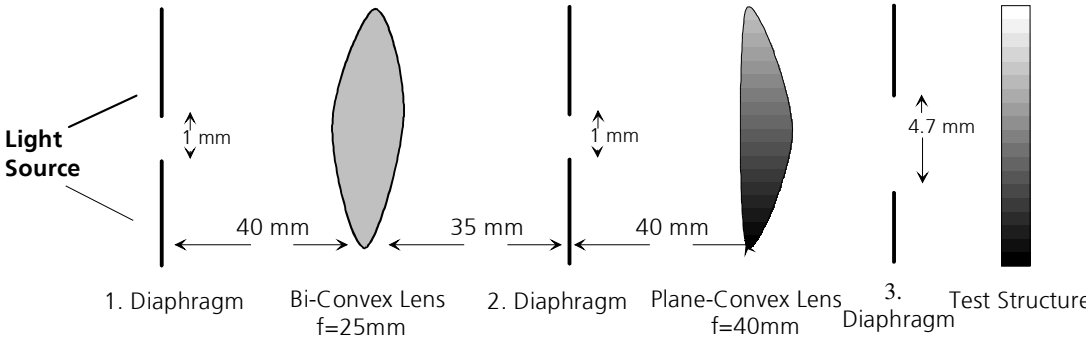


Figure A. 4 - Optical breadboard system diagram.

The irradiance values (in μW/cm^2) of the radiation impinging on the DUT (after the optical breadboard system) in this measuring station can be observed in Figure A. 5.

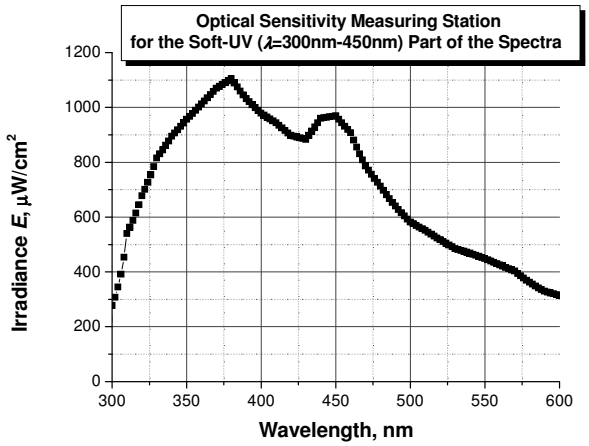


Figure A. 5 - Irradiance values (in μW/cm^2) of radiation impinging on the DUT (after the optical breadboard system) in the *optical sensitivity measuring station for the soft-UV (λ=300nm-400nm) part of the spectra.*

A.4 Measurement System Connections Scheme

The optical sensitivity soft-UV measuring station connections scheme diagram is shown in Figure A. 6.

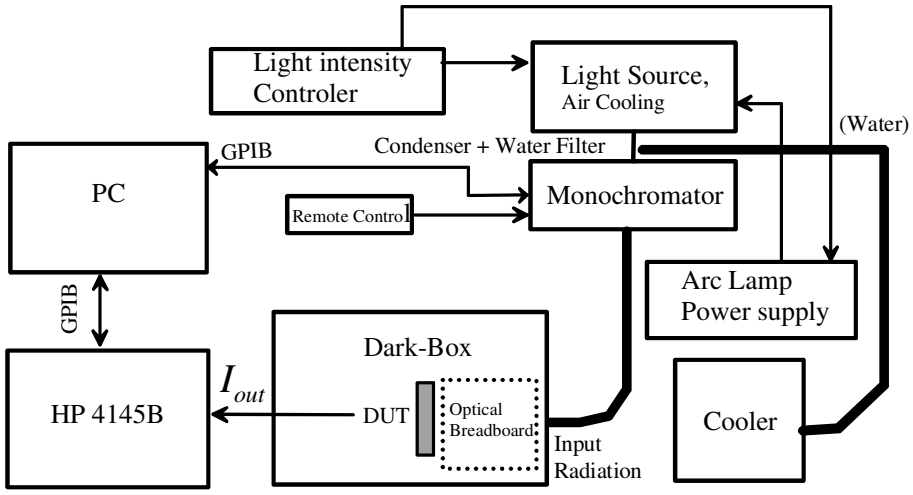


Figure A. 6 - *Optical sensitivity soft-UV measuring station* connections scheme diagram.

A.5 Measurement Procedure

A.5.1 Monochromator Calibration

After the connections of the entire system have been revised, and the GPIB communication tested using the *Measurement and Automation* software provided by *National Instruments*, the proper monochromator calibration takes

place. If the *Oriel Instruments Cornerstone 130™ Motorized 1/8m Monochromator Model 74000* datasheet are consulted, on page 28, under Chapter VIII-1 entitled "Memory Loss (Large wavelength calibration errors)", it is written that if "there are large errors in wavelength positioning of all gratings (maybe 10nm), or the instrument lists all gratings as 1200 l/mm", it means that "the instrument memory has been cleared, which may be the result of a power failure or a spike on the mains, or from electro-static discharge or other high-filed radiation in contact with, or very nearby, the instrument". The solution is to reload the instrument parameters, which are:

	Grate 1	Grate 2
Lines/mm	1200	
Label	350	
Factor	0.99913	
Offset	-0.000658	
Grate1Zero	0.0878480	

This must be done using through the *Oriel Cornerstone 130™ Utility Program* or the *LabView* based driver. Next step is to verify the calibration or realise further calibration if required (consult the Datasheet), using the spectrometer *Ocean Optics, Inc. USB 2000* device, which forms part of the *Aspect Systems Optoelektronische Messplatz*, and the software which belongs to it. In order to manually set a certain wavelength value in the monochromator device, the *Oriel Instruments* remote control is used, at first establishing communication through the *Units/Local* button, and then indicating the value of the out-coming wavelength through the *Go Wave* button and finally, pushing *Enter*. It is important to disable the remote control communication pushing again the *Units/Local* button, in order to facilitate the GPIB communication.

A.5.2 Calculus

In order to obtain the proper value for the irradiance (measured in W/cm^2) impinging on the test structure, a *Hamamatsu* fabricated reference photodiode is used. As its *optical sensitivity* $S_{ref\text{-}PD}$ (in A/W) is known and was certified by a competent laboratory, by measuring its output current with the *HP4145B* device, the optical power values can easily be calculated for each wavelength of interest. The reference photodiode should be placed exactly on the same place where the test structure comes later on, taking the impinging radiation coming out of the optical collimator structure as a reference.

At first, the reference photodiode (ref-PD) will undergo the "re-calibration" procedure, or the first measurement process, through which the linear dependence factor is to be calculated between the irradiance and the output photocurrent ($I_{ph\text{-}ref\text{-}PD}$) for each wavelength of interest, i.e. the factor which has to multiply the test structure's I_{ph} in order to obtain its *optical sensitivity* in A/W: the multiplication factor β, as shown in Eq. (A. 1). Here, $A_{ref\text{-}PD}$ is the area of the *Hamamatsu* reference photodiode.

$$\beta = \frac{S_{ref-PD} A_{ref-PD}}{I_{ph-ref-PD}} \quad \text{(A. 1)}$$

Moreover, as the output signal of the ref-PD contains both, the dark current $I_{dark\text{-}ref\text{-}PD}$, originated through the thermal generation of minority carriers, and the photo current $I_{ph\text{-}ref\text{-}PD}$, originated by the impinging radiation, an initial step to measure the output current of the ref-PD in absolute darkness ($I_{dark\text{-}ref\text{-}PD}$) has to be performed. Afterwards, the first measurement process should take place, delivering the wavelength dependent output signal, as expressed in Eq.(A. 2).

$$I_{out}(\lambda) = I_{ph}(\lambda) + I_{dark} \quad \text{(A. 2)}$$

Finally, in order to obtain $I_{ph\text{-}ref\text{-}PD}(\lambda)$, a simple subtraction has to be performed, following Eq. (A. 2).

Once the first measurement (recalibration) process is finished, the test structure is placed on the exact position previously occupied by the ref-PD. As before, at first an initial step has to be performed in order to obtain the test structure dark current $I_{dark\text{-}TS}$, and afterwards the test structure (TS) wavelength dependent photocurrent $I_{ph\text{-}TS}$, as described above. Once done, the optical sensitivity of the test structure can easily be calculated using Eq. (A. 3), where A_{TS} is the photoactive area of the test structure.

$$S_{TS} = \frac{I_{ph-TS}\beta}{A_{TS}} \quad \text{(A. 3)}$$

Finally, the quantum efficiency (η) of the test structure (TS) can be obtained following Eq. (A. 4), where h is the Planck constant (6.62607×10^{-34}J·s), c the speed of light in vacuum (2.99792×10^{10}cm/s), q the fundamental charge (1.60218×10^{-19}C), and λ the wavelength of interest (in cm), as shown in Eq. (2.19) in chapter 2 of this text.

$$\eta_{TS} = S_{TS} \frac{hc}{q\lambda} \quad \text{(A. 4)}$$

A.5.3 Measurement Procedure

The first step required to perform a measurement using the *Soft-UV Optical Sensitivity Measurement Station* is to turn on the HAAKE class D cooler and wait until the temperature indicated at the cooler's display reaches the 15°C. Once the desired temperature has been reached, the short-arc lamp power supply, the light intensity controller, the monochromator, and the HP4145B semiconductor analyser should be turned on. After a few moments, the lamp should be also turned on, using the white button on the lamp power supply housing (it could take some seconds until the lamp turns on, so the button should remain pushed until is happens). Once the lamp has been turned on, it is recommended to wait

half an hour until the lamp irradiance stabilizes. Then, the first measurement can be carried out.

At first, the proper PC with its *general purpose interface bus* (GPIB) input connected to the monochromator and the HP4145B device, should be turned on, and then the *Soft-UV Optical Sensitivity* software should be launched. The first image to be seen on the monitor is the one shown in Figure A. 7, namely the *General Settings* screen.

Here, the heading of the future results data file is to be designed by introducing the name of the place where the measurements are being done (e.g. Fraunhofer IMS), the name of the operator, the device, wafer, and lot identification numbers, respectively, for the test structures of interest, as well as any desired comments. Next, the path to the desired results data file (.txt) is to be typed or browsed using the proper option on the right.

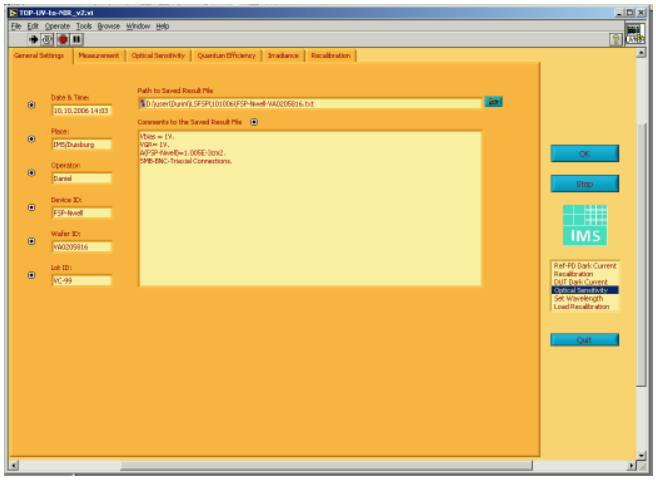


Figure A. 7 – *General Settings* screen of the *Soft-UV Optical Sensitivity* software developed using the *National Instruments LabView* tool at the Fraunhofer IMS.

Next, from the upper part of the screen, the option *Recalibration* is to be chosen. The first measurement can be now carried out, the so called recalibration one, using the already described *Hamamatsu* reference photodiode as a *device under test* (DUT). After the Ref-PD was properly connected and prepared for the measurement, the path and name of the future β data file (.txt) is to be introduced in the field where "Path to Saved Recalibration Data" is written (Figure A. 8). Afterwards, the path to the data file (.txt) where there are the laboratory certified optical sensitivity (in A/W) data of the Ref-PD to be found should be introduced in the field entitled "Path to Ref-PD Recalibration (Optical Sensitivity) Data", as it can be observed in Figure A. 8.

Now, the first recalibration measurement can start. On the right side of the screen, under the Fraunhofer IMS logo, a menu can be observed. From this menu, at first, the option "Ref-PD Dark Current" should be chosen. Afterwards, click the OK button. A menu will pop-up on the screen, asking if the monochromator output shutter should remain open or closed during this

measurement. Of course, it should be closed as no light should enter the black box where the DUT is to be found, so this option should be chosen. After the HP4145B starts programming its inputs and outputs, the OK button should be deactivated. The Ref-PD output should always be connected to the SMU1 input of the HP4145B. Once the measurement of the Ref-PD is performed, the same monochromator menu will again pop-up on the screen asking if the monochromator shutter should be opened or should remain closed. This time, the option "Open the shutter" should be chosen, so that the optical measurement could begin. On the left upper corner of the recalibration graph, the new value of the Ref-PD appears, indicating that this step was completed.

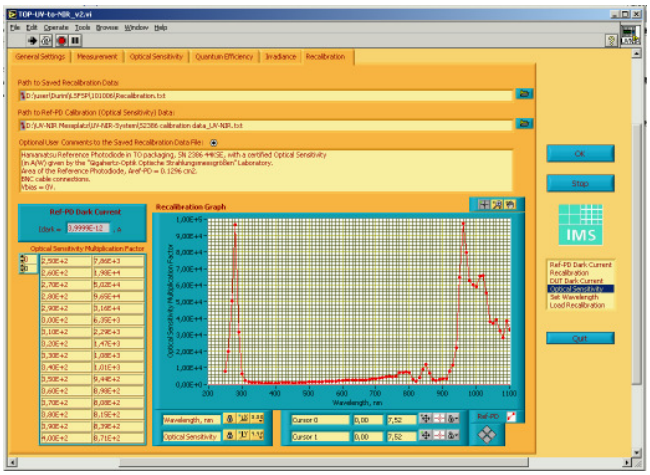


Figure A. 8 – *Recalibration* sheet of the *Soft-UV Optical Sensitivity* software developed using the *National Instruments LabView* tool at the Fraunhofer IMS.

Going back to the menu list on the right side of the screen, the option "Recalibration" is now to be chosen. Afterwards, back to the upper part of the screen, the "Measurement" sheet is to be opened, which can be observed in Figure A. 9.

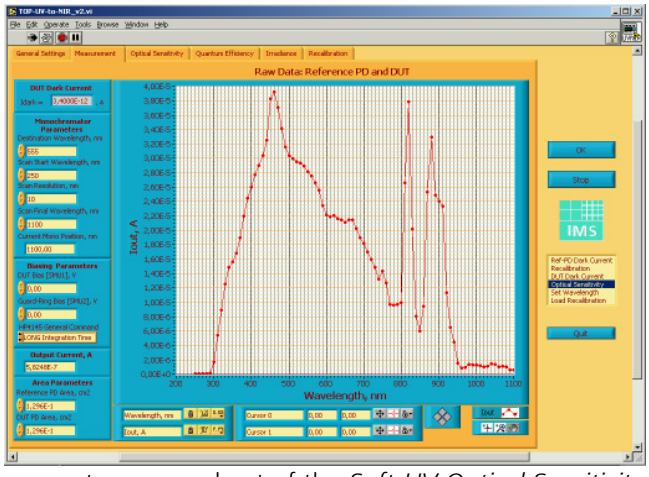


Figure A. 9 - *Measurement* program sheet of the *Soft-UV Optical Sensitivity* software developed using the *National Instruments LabView* tool at the Fraunhofer IMS.

On the left part of the screen, under "Monochromator Parameters", the "Destination wavelength, nm" value, together with the option "Set Wavelength" of the menu on the right side of the screen will bring the

monochromator output to the desired wavelength, if you click the OK button afterwards. The new output light beam wavelength will be indicated on the left side of the screen in the "Current Mono Position, nm" field. Now, in order to start the Ref-PD recalibration measurement, the initial wavelength is to be introduced in the "Scan Start Wavelength, nm" field, in nanometres. Following, the distance between every two measured wavelengths is to be introduced in the field "Scan resolution, nm" also in nanometres. For the recalibration measurement, this resolution should be 10nm. Finally, the final wavelength is to be introduced in the field "Scan Final Wavelength, nm".

Following, in the menu "Biasing Parameters", the biasing voltage values for the DUT and its guard-ring (explained later in this text) should be introduced. For the case of the recalibration measurement, they should be both 0V. Next, the integration time of the HP4145B is to be determined. Suggested is to use "long integration times". In "Area Parameters" menu, the areas (in cm^2) of the DUT and the Ref-PD ($A_{ref\text{-}PD}$=1.296×$10^{-1}cm^2$) are to be, respectively, written.

Once all the required fields have been filled in, the OK button should be pressed so that the recalibration could start. Once the measurement starts, deactivate the OK button. The Ref-PD output current values (in amperes) referred to each wavelength of interest can be monitored on the "Raw Data: Reference PD and DUT" graph (Figure A. 9) on one side, and the multiplication factor β in the "Recalibration Graph" (Figure A. 8), on the other.

After the recalibration measurement ends, the Ref-PD should be replaced by the test structure of interest: the new DUT. Normally, the photodiodes possess a certain guard-ring, i.e. an *n*-well based ring fabricated around the photodiode to avoid any cross-talk from surrounding structures. This guard ring is biased through the SMU2 connection of the HP4145B. When the new DUT is properly connected and situated at the exact spot where its Ref-PD predecessor was, then the second measurement can start.

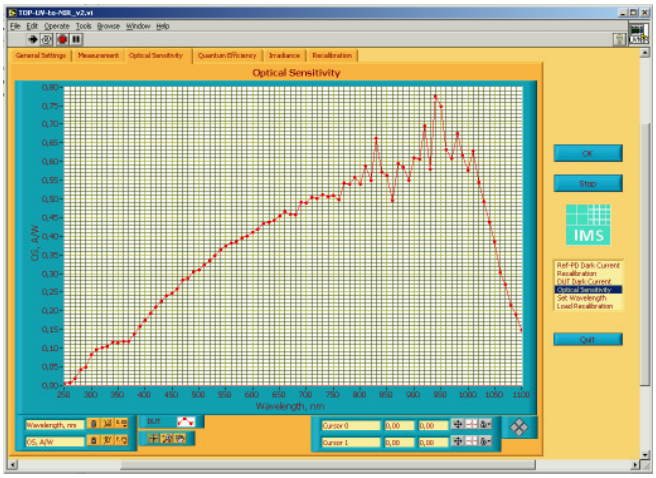


Figure A. 10 – *Optical Sensitivity* screen of the *Soft-UV Optical Sensitivity* software developed using the *National Instruments LabView* tool at the Fraunhofer IMS.

On the *Measurement* screen of the *Soft-UV Optical Sensitivity* software at first the option "DUT Dark Current" has to be elected on the menu located on

the right side of the screen. As before, after the OK button has been clicked on, a pop-up screen will appear asking if the monochromator shutter should be closed. After an affirmative answer, the OK button should be deactivated. The measurement will be carried out and on the left upper corner, in the field labelled "DUT Dark Current" (Figure A. 9), the new value of the test structure dark current will appear which will be substracted from each output current value measured during the future DUT optical sensitivity measurement.

Following, on the menu on the right side of the screen, the option "Optical Sensitivity" should be chosen, at the same as the initial, the final, and the resolution wavelength (any value can here be chosen starting with 1nm) should be respectively filled in the properly labelled fields on the left side of the screen. Finally, the OK button activation will start the optical sensitivity measurement of the test structure of interest.

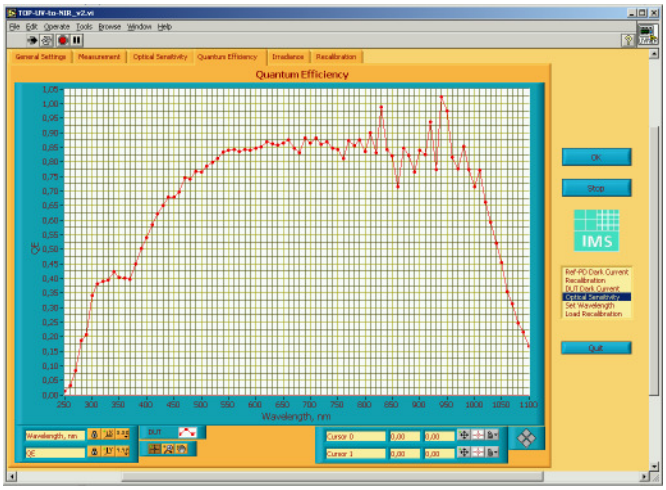


Figure A. 11 – *Quantum Efficiency* screen of the *Soft-UV Optical Sensitivity* software developed using the *National Instruments LabView* tool at the Fraunhofer IMS.

During the measurement, the values can be monitored by selecting the proper program sheet on the upper part of the screen. On the *Measurement* screen, the output current is monitored in "real time". Simultaneously, on the *Optical Sensitivity* screen, shown in Figure A. 10, the wavelength dependent optical sensitivity data are being followed. The same happens with the quantum efficiency data on the *Quantum Efficiency* screen, Figure A. 11, and the irradiance on the *Irradiance* screen, shown in Figure A. 12. The output data file will contain the dark current value, as well as the measured photocurrent, the optical sensitivity, the quantum efficiency, and the irradiance for each wavelength of interest.

A.6 Soft-UV Optical Sensitivity Software Precision Evaluation

Two different test structures, namely the *n*-well and n^+ photodiodes, respectively, fabricated on the same chip, were characterized using the *Soft-UV Optical Sensitivity* measuring station on eight different days. They were each time reverse biased at V_{DD}=3.3V and the measurements were carried out at room temperature. The results referred to the 600nm wavelength impinging radiation

obtained are enlisted in Table A. 1, while those referred to the 300nm wavelength impinging radiation are enlisted in Table A. 2.

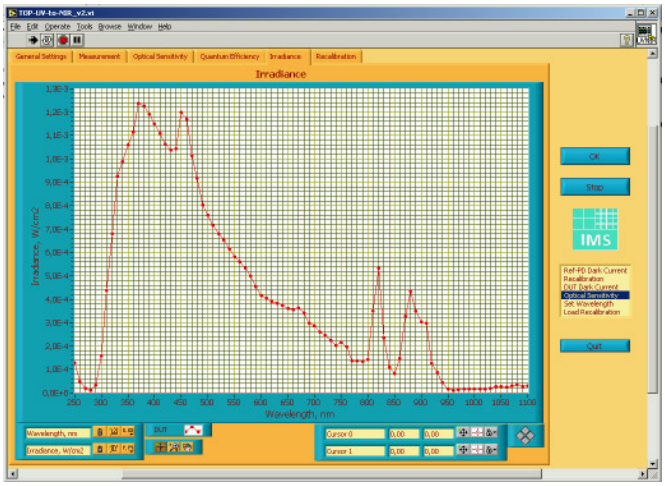


Figure A. 12 - *Irradiance* program sheet of the *Soft-UV Optical Sensitivity* software developed using the *National Instruments LabView* tool at the Fraunhofer IMS.

From the values enlisted in Table A. 1, the optical sensitivity ($\overline{S}$) and quantum efficiency ($\overline{\eta}$) mean values can be respectively calculated for each of the columns, being for the *n*-well PD: $\overline{S}_{n\text{-well}}$ = 0.3425 ± 0.0061 A/W (standard deviation: $S_x = \left[\frac{1}{n-1}\sum_{i=1}^{n}\left(\overline{x}-x_i\right)^2\right]^{1/2}$, for any variable *x*) and $\overline{\eta}_{n\text{-well}}$ = 0.708 ± 0.0091; and for the n^+ PD: $\overline{S}_{n+}$ = 0.2996 ± 0.0042 A/W and $\overline{\eta}_{n+}$ = 0.619 ± 0.02. The precision error can than be calculated as $\%EP = \frac{\left|\overline{S} - S_{\max}\right|}{\overline{S}} \times 100$, being for the *n*-well PD: $\%EP_{n\text{-well}}(S)$ = 18.1%, and for the n^+ PD: $\%EP_{n+}(S)$ = 17.86%. Considering the system precision as %*P* = (100-%*EP*), and calculating the average value of all the precision percents obtained, it can be concluded that the *Soft-UV Optical Sensitivity* measuring station posses a precision of around 82.02%, or a precision error of around 17.98% at 600nm wavelength impinging radiations.

Date of Measurement	*n*-well PD		n^+-PD	
	***S*, A/W (λ=600nm)**	**η (λ=600nm)**	***S*, A/W (λ=600nm)**	**η (λ=600nm)**
18.10.06	0.3007	0.6219	0.2790	0.5764
20.10.06	0.2678	0.5538	0.2507	0.5180
23.10.06	0.3594	0.7426	0.3459	0.7148
24.10.06	0.3995	0.8256	0.3398	0.7021
25.10.06	0.3348	0.6918	0.3273	0.6763
30.10.06	0.3310	0.6840	0.3084	0.6373
31.10.06	0.4045	0.8359	0.2461	0.5086

Table A. 1 – Results of the optical sensitivity (*S*) and quantum efficiency (η) measurements obtained from reverse biased (V_{DD}=3.3V) *n*-well and n^+ PD test structures, for the 600nm wavelength impinging radiation.

From the values enlisted in Table A. 2, for the *n*-well PD: $\overline{S}_{n\text{-well}}$ = 0.0969 ± 0.0048 A/W and $\overline{\eta}_{n\text{-well}}$ = 0.4006 ± 0.002; and for the n^+ PD: $\overline{S}_{n+}$ = 0.0472 ± 0.004 A/W and $\overline{\eta}_{n+}$ = 0.1953 ± 0.017. The precision error is for the *n*-well PD: $\%EP_{n\text{-well}}(S)$ = 7.95%, and for the n^+ PD: $\%EP_{n+}(S)$ = 15.68%. Considering the system precision as $\%P = (100-\%EP)$, and calculating the average value of all the precision percents obtained, it can be concluded that the *Soft-UV Optical Sensitivity* measuring station posses a precision of around 88.19%, or a precision error of around 11.81%, for the 300nm wavelength impinging radiation.

Date of Measurement	***n*-well PD**		***n*$^+$-PD**	
	***S*, A/W (λ=300nm)**	**η (λ=300nm)**	***S*, A/W (λ=300nm)**	**η (λ=300nm)**
18.10.06	0.0891	0.3680	0.0422	0.1745
20.10.06	0.0952	0.3936	0.0473	0.1957
23.10.06	0.0959	0.3966	0.0448	0.1850
24.10.06	0.0996	0.4115	0.0453	0.1873
25.10.06	0.1046	0.4324	0.0546	0.2255
30.10.06	0.0984	0.4066	0.0465	0.1921
31.10.06	0.0957	0.3956	0.0501	0.2071

Table A. 2 - Results of the optical sensitivity (*S*) and quantum efficiency (η) measurements obtained from reverse biased (V_{DD}=3.3V) *n*-well and n^+ PD test structures, for the 300nm wavelength impinging radiation.

B Optical Sensitivity Measurement Station for the VIS-NIR (450nm-1100nm) Part of the Spectra

B.1 Apparatus

The optical sensitivity measuring station for the VIS-NIR (λ = 450nm-1100nm) part of the spectra consists of:

- A PC containing *National Instruments LabView 7.1* Software, GPIB connection facility and the *National Instruments* data acquisition card;
- 250W halogen lamp, original model: *Oriel Instruments* model Nr.: 66055, currently *LOT-Oriel* model Nr.: LSB123 / 5, working at 10.5A, 24V, with an approx. 10.000lm flux;
- *LOT-Oriel* lamp-adapter, current model Nr.: LSA131 for the lamp housing;
- *Oriel Instruments* open chopper system, model Nr.: 75159;
- Monochromator*:* original model *ORIEL Instruments Corner Stone 1/4m*, Model: 74100, currently *LOT-Oriel* model Nr.: MSH301 monochromator;
- 2 FEMTO Variable-Gain Low-Noise Current Amplifiers DLPCA-200;
- 2 *Perkin Elmer Instruments* Lock-In amplifiers, Model Nr.: 5210;
- Measurement black-box;
- *LOT-Oriel* VIS-NIR 1m long liquid light guide, model Nr. : LLG314;
- Optical system built on an optical breadboard: 1 bi-convex lens, 1 plane-convex lens, and 3 optical diaphragms.

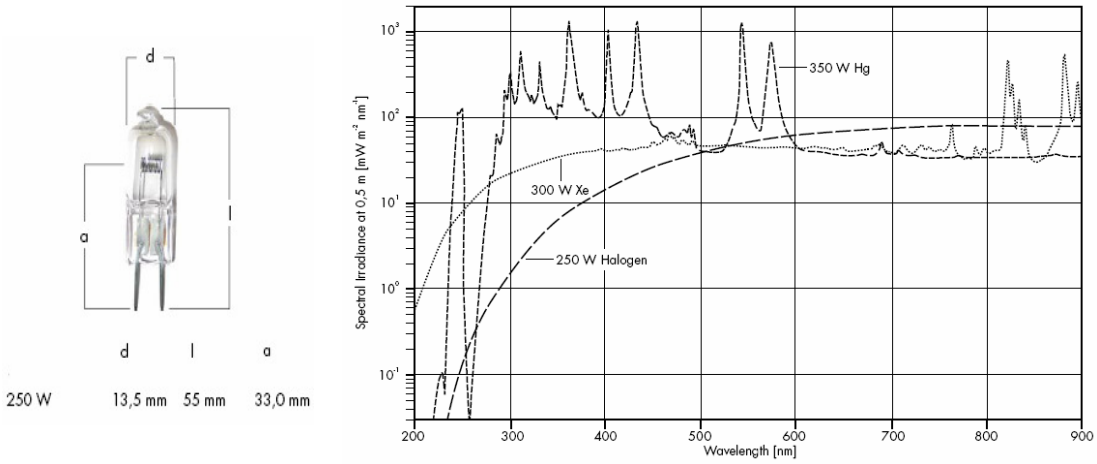
B.2 Radiation Related Specifications

The light source used for this measurement station is a 250W halogen lamp, original model: *Oriel Instruments* model Nr.: 66055, currently *LOT-Oriel* model Nr.: LSB123 / 5, working at 10.5A, 24V, with an approx. 10.000lm flux.

Tungsten halogen incandescent lamps are thermal radiators. This means that the light is generated by heating a solid body to a high temperature. The higher its temperature, the "brighter" the light. In halogen lamps the required temperature is produced by passing a current through an electrical conductor of greater or lesser conductivity. The incandescent material must have a high melting point and slow rate of vaporization in order to reach as high a temperature as possible and be capable of maintaining this over a long period of time. Although tungsten is limited with its melting point of 3383°C and its low

rate of vaporization, no better incandescent material with better properties has been found yet despite intensive research.

In conventional incandescent lamps the vaporized tungsten is deposited on the glass bulb. This blackens the bulb wall and gradually reduces the light output. To keep the light loss as low as possible the bulb surface is large, keeping the absorbing layer thin. With tungsten halogen lamps the bulb is filled with an inert gas (Krypton or Xenon) mixed with a low amount of a halogen element (bromine or iodine). The vaporized tungsten from the filament then can be intercepted before reaching the bulb wall and returned to the filament. This thermo-chemical process is called *halogen cycle*. As a result the glass bulb stays clean, the output remains equally bright till the end of lamp life. Converting electrical current to light also is more efficient. As the bulb does not blacken, it can be relatively small compared to conventional tungsten lamps which allows to use them in spectroscopy applications. The bulb material for tungsten halogen lamps is quartz, which allows bulb temperatures of up to 900 °C and operating pressures of up to 20 bar. The halogen lamp (used in this measuring station) physical measures and its wavelength dependent spectral irradiance characteristic can be observed in Figure B. 1.



(a) (b)

Figure B. 1 - Physical measures (left) and the wavelength dependent spectral irradiance (right) of the *LOT-Oriel* 250W halogen lamp, model. Nr.: LSB123 / 5 [Lor07].

The outgoing light beam is modulated using the *Oriel Instruments* open chopper system model Nr.: 75159 with a 10Hz frequency. Afterwards, the so modulated light enters the current *LOT-Oriel* model Nr.: MSH301 monochromator, with an output optical grid (*LOT-Oriel* model Nr.: MSGx13) that presents 1800l/mm grating groove density, 500nm blaze wavelength, and an optimum output radiation wavelength range between the 300nm and 1100nm. The monochromator has two optical outputs. On one side, the *Hamamatsu* reference photodiode (described in *Appendix A* of this work) is illuminated using the *LOT-Oriel* VIS-NIR 1m long liquid light guide, model Nr. : LLG314. This liquid light guide can be used with temperatures from -5° to 35° C. Nevertheless, it should not be exposed to radiation smaller than 420 nm. To avoid this, UV filters were incorporated on both ends of the light guide. Afterwards, the light beam is introduced into the optical collimator shown in Figure A. 4, to finally impinge the

surface of the *device under test* (DUT). On the other hand, a monitoring photodiode similar to the reference one is illuminated through the second optical output port of the monochromator (Figure B. 3). The output photocurrents coming from both photodiodes are then converted into voltage signals and amplified by a couple of really sensitive pre-amplifiers (FEMTO *Variable-Gain Low-Noise Current Amplifiers DLPCA-200*), and then delivered to a couple of *Perkin Elmer Instruments* lock-In amplifiers, Model No. 5210. The irradiance values are then extracted from the reference photodiode output signal, and then used during the test structure characterization as explained in Appendix A. The entire system is controlled, and the lock-in amplifier outputs are captured by a *National Instruments LabView* software based *IdSpectral* program developed by *AspectSystems GmbH*. The phase lock-in principle used here eliminates the dark current and most of the noise contributions to the output signal.

The irradiance values (in μW/cm^2) of the radiation impinging on the DUT (after the optical breadboard system) in this measuring stations can be observed in Figure B. 2.

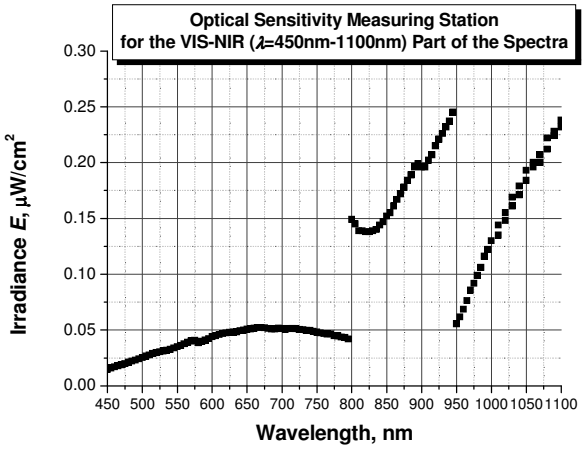


Figure B. 2 - Irradiance values (in μW/cm^2) of radiation impinging on the DUT (after the optical breadboard system) in the *optical sensitivity measuring station for the VIS-NIR (λ=450nm-1100nm) part of the spectra*.

B.4 Measurement System Connections Scheme

The optical sensitivity measurement station for the VIS-NIR (*λ*=450nm–1100nm) part of the spectra connections scheme diagram is shown in Figure B. 3.

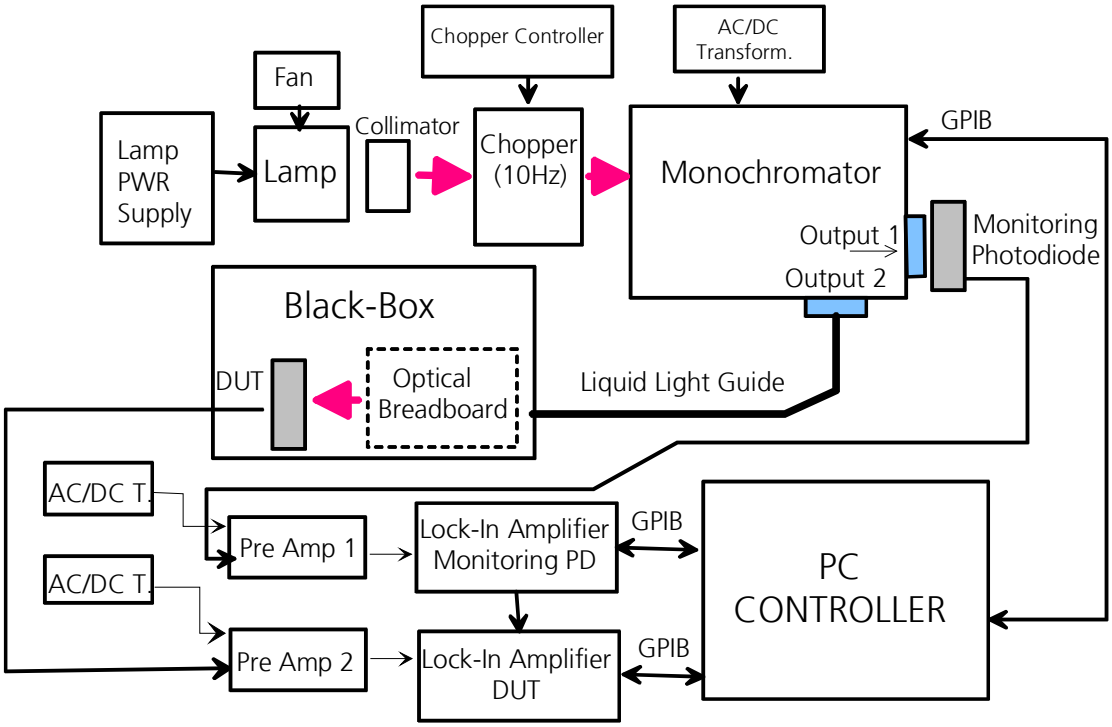


Figure B. 3 - Connections scheme diagram of the optical sensitivity measurement station for the VIS-NIR (λ=450nm–1100nm) part of the spectra.

C A Detailed Mathematical Analysis of the ehp Photogeneration Process Within a Wafer and a p-n Junction

Continuing the discussion initiated in the sub-chapter 2.3.2, the solution to the steady-state, small-signal excess (photogenerated) minority carrier density $\Delta n_{ph}(z)$, expressed in Eq. (2. 31) [Sch98], subject to boundary conditions expressed in Eq. (2. 32) [Sch98] and using Eq. (2. 33), results in Eq. (C. 1), where the terms A_1, B_1, and D_1 are defined according to Eq. (C. 2) [Sch98].

$$\Delta n_{ph}(z) = \frac{(1-R)\eta\Phi_{ph}\alpha\tau_{r\_n}}{(\alpha^2 L_n^2 - 1)}\left[\frac{A_1 + e^{-\alpha d_W} B_1}{D_1} - e^{-\alpha z}\right] \tag{C. 1}$$

$$\begin{aligned} A_1 &= \left(\frac{s_{r\_n1}s_{r\_n2}L_n}{D_n} + s_{r\_n2}\alpha L_n\right)\sinh\left(\frac{d_W - z}{L_n}\right) + \left(s_{r\_n1} + \alpha D_n\right)\cosh\left(\frac{d_W - z}{L_n}\right) \\ B_1 &= \left(\frac{s_{r\_n1}s_{r\_n2}L_n}{D_n} - s_{r\_n1}\alpha L_n\right)\sinh\left(\frac{z}{L_n}\right) + \left(s_{r\_n2} - \alpha D_n\right)\cosh\left(\frac{z}{L_n}\right) \\ D_1 &= \left(\frac{s_{r\_n1}s_{r\_n2}L_n}{D_n} + \frac{D_n}{L_n}\right)\sinh\left(\frac{d_W}{L_n}\right) + \left(s_{r\_n1} + s_{r\_n2}\right)\cosh\left(\frac{d_W}{L_n}\right) \end{aligned} \tag{C. 2}$$

Now, if instead of a wafer of thickness d_W, a *p-n* junction is considered (Figure 1. 4), taking into account now the *n*-well thickness $d_{n\text{-}well}$ and the hole recombination lifetime τ_{r_p}, and also that under short-circuit current conditions the excess carrier density is zero at the edge of the SCR ($z = d_{n\text{-}well}$), which from a surface recombination velocity point of view means $s_{r\_n2} = \infty$, from Eq. (C. 1), Eq. (C. 3) can be derived for A_2, B_2, and D_2 defined by Eq. (C. 4) [Sch98].

$$\Delta p_{ph}(z) = \frac{(1-R)\eta\Phi_{ph}\alpha\tau_{r\_p}}{(\alpha^2 L_p^2 - 1)}\left[\frac{A_2 + e^{-\alpha d_{n-well}} B_2}{D_2} - e^{-\alpha z}\right] \tag{C. 3}$$

$$A_2 = \left(\frac{s_{r\_p} L_p}{D_p} + \alpha L_p\right)\sinh\left(\frac{d_{n-well} - z}{L_p}\right)$$
$$B_2 = \left(\frac{s_{r\_p} L_p}{D_p}\right)\sinh\left(\frac{z}{L_p}\right) + \cosh\left(\frac{z}{L_p}\right) \quad \text{(C. 4)}$$
$$D_2 = \left(\frac{s_{r\_p} L_p}{D_p}\right)\sinh\left(\frac{d_{n-well}}{L_p}\right) + \cosh\left(\frac{d_{n-well}}{L_p}\right)$$

Similar arguments are valid for the *p*-type substrate, using $z' = (z - d_{n\text{-well}} - W_{SCR})$, $d_{p\text{-Epi}} = (d_W - d_{n\text{-well}} - W_{SCR})$, and $s_{r\_n1} = \infty$, so Eq. (C. 5) can be defined with A_3, B_3, and D_3 definitions in Eq. (C. 6) [Sch98].

$$\Delta n_{ph}(z') = \frac{(1-R)\eta\Phi_{ph}\alpha\tau_{r\_n}}{(\alpha^2 L_n^2 - 1)}\left[\frac{A_3 + e^{-\alpha d_{p-Epi}} B_3}{D_3} - e^{-\alpha z'}\right] e^{-\alpha\left(d_{p-Epi} + W_{SCR}\right)} \quad \text{(C. 5)}$$

$$A_3 = \left(\frac{s_{r\_n} L_n}{D_n}\right)\sinh\left(\frac{d_{p-Epi} - z}{L_n}\right) + \cosh\left(\frac{d_{p-Epi} - z}{L_n}\right)$$
$$B_3 = \left(\frac{s_{r\_n} L_n}{D_n} - \alpha L_n\right)\sinh\left(\frac{z'}{L_n}\right) \quad \text{(C. 6)}$$
$$D_3 = \left(\frac{s_{r\_n} L_n}{D_n}\right)\sinh\left(\frac{d_{p-Epi}}{L_n}\right) + \cosh\left(\frac{d_{p-Epi}}{L_n}\right)$$

The additional term $\exp[-\alpha(d_{p\text{-Epi}}+W_{SCR})]$ in Eq. (C. 5) accounts for the carrier generation beyond $z = d_{p\text{-Epi}} + W_{SCR}$ [Sch98]. The absorbed photon flux density has already diminished by this factor when the photons enter the *p*-Epi (substrate). The excess carrier density in the SCR is considered to be zero, as the *ehp* are considered to be swept out of that region as soon as they are generated.

The current density for the short-circuited structure of Figure 1. 4 is obtained by considering only the diffusion current of electrons J_n in the *p*-Epi and the diffusion current of holes J_p in the *n*-well. An implicit assumption is that there are no voltage drops across the *n*-well and *p*-Epi regions and that the drift currents are negligible there. In the SCR the electric field is dominant, and recombination is negligible. With these assumptions, the short-circuit current density J_{sc} can be expressed as shown in Eq. (C. 7) [Sch98].

$$J_{sc} = J_p + J_n + J_{SCR} \quad \text{(C. 7)}$$

The hole current density is then in this context defined by Eq. (C. 8) with A_4, B_4, and D_4 as shown in Eq. (C. 9) [Sch98].

$$J_p = \frac{q\eta(1-R)\Phi_{ph}\alpha L_p}{\alpha^2 L_p^2 - 1}\left[\frac{A_4 - e^{-\alpha d_{n-well}}B_4}{D_4} - \alpha L_p e^{-\alpha d_{n-well}}\right] \quad \text{(C. 8)}$$

$$A_4 = \frac{s_{r\_p}L_p}{D_p} + \alpha L_p$$

$$B_4 = \left(\frac{s_{r\_p}L_p}{D_p}\right)\cosh\left(\frac{d_{n-well}}{L_p}\right) + \sinh\left(\frac{d_{n-well}}{L_p}\right) \quad \text{(C. 9)}$$

$$D_4 = \left(\frac{s_{r\_p}L_p}{D_p}\right)\sinh\left(\frac{d_{n-well}}{L_p}\right) + \cosh\left(\frac{d_{n-well}}{L_p}\right)$$

The electron current density is defined by Eq. (C. 10) for A_5, B_5, and D_5 as shown in Eq. (C. 11) [Sch98].

$$J_n = \frac{q\eta(1-R)\Phi_{ph}\alpha L_n}{\alpha^2 L_n^2 - 1}\left[\frac{-A_5 - e^{-\alpha d_{p-Epi}}B_5}{D_5} + \alpha L_n\right]e^{-\alpha(d_{n-well}+W_{SCR})} \quad \text{(C. 10)}$$

$$A_5 = \left(\frac{s_{r\_n}L_n}{D_n}\right)\cosh\left(\frac{d_{p-Epi}}{L_n}\right) + \cosh\left(\frac{d_{p-Epi}}{L_n}\right)$$

$$B_5 = \frac{s_{r\_n}L_n}{D_n} - \alpha L_n \quad \text{(C. 11)}$$

$$D_5 = \left(\frac{s_{r\_n}L_n}{D_n}\right)\sinh\left(\frac{d_{p-Epi}}{L_n}\right) + \cosh\left(\frac{d_{p-Epi}}{L_n}\right)$$

Finally, the SCR photocurrent density is defined by Eq. (C. 12) [Sch98].

$$J_{ph\_SCR} = q\eta(1-R)\Phi_{ph}e^{-\alpha d_W}\left(1 - e^{-\alpha W_{SCR}}\right) \quad \text{(C. 12)}$$

On the other hand, the photocurrent flowing within an *n*-well PD can be divided, just as it is the case with the dark current into its diffusion part formed by the photogenerated minority carriers in the silicon bulk within a diffusion length distance of the edges of the SCR, and the drift component arouse through the photogenerated carriers inside the SCR which are immediately drifted due to the electrical fields existent. For photogenerated carriers in both, the depletion region and in the bulk, it is necessary to consider the quantum efficiency. For the depletion region, it is possible to assume η_{SCR} = 1. Nevertheless, in the region of undepleted silicon substrate (d_s) there are considerable recombination losses, because during the diffusion process the charge carriers are lost by recombination, effects considered within the bulk quantum efficiency value η_{bulk}. The total efficiency of the carrier collection process η can be described by Eq. (C. 13) [VdW76].

$$\eta = \eta_{SCR} + \eta_{bulk} \quad \text{(C. 13)}$$

The bulk quantum efficiency component can be written as shown in (C. 14) [VdW76].

$$\eta_{bulk} = \frac{\alpha L_p^{\,2}}{\alpha^2 L_p^{\,2} - 1}\left(\alpha e^{-\alpha W_{SCR}} + \frac{e^{-\alpha d_s} - e^{-\alpha W_{SCR}} \cosh\left[\frac{(d_s - W_{SCR})}{L_p}\right]}{L_p - \sinh\left[\frac{(d_s - W_{SCR})}{L_p}\right]} \right) \qquad \text{(C. 14)}$$

D List of Published Papers and Thesis Produced in Frame of this Work

Papers:

- D. **Durini**, A. **Kemna**, W. **Brockherde**, B. **Hosticka**, "CMOS integrated pixel array for low-level radiation detection using 'time compression' parametric amplification", *Proc. 10th European Symposium on Semiconductor Detectors (SDS)*, Wildbad Kreuth, Germany, June 2005
- D. **Durini**, A. **Kemna**, W. **Brockherde**, B. **Hosticka**, "CMOS integrated pixel array for low-level radiation detection using 'time compression' parametric amplification", *Nucl. Instr. Meth. Phy. Res.*, A568, 2006, pp. 112-117
- D. **Durini**, "Characterization of Optoelectronic Devices*", Fraunhofer Institut Mikroelektronische Schaltungen und Systeme Annual Report 2006*, pp. 31-34
- D. **Durini**, K. E. **Enowbi**, W. **Brockherde**, B. J. **Hosticka**, "CMOS Silicon-On-Insulator technology: An Alternative for NIR Quantum Efficiency Enhanced CMOS Imaging Pixel Detectors", *Proc. EOS Conference on Frontiers in Electronic Imaging, World of Photonics Congress 2007, Munich, Germany*, June 2007, pp. 26-27
- D. **Durini**, B. J. **Hosticka**, "Photodetector Structures for Standard CMOS Imaging Applications", *Proc. IEEE PRIME 2007, Bordeaux, France,* July 2007, pp. 193-196
- D. **Durini**, W. **Brockherde**, B. J. **Hosticka**, "SOI Pixel Detector Based on CMOS Time-Compression Charge-Injection", *Proc. European Conference on Circuit Theory and Design ECCTD 2007, Seville, Spain*, August 2007, pp. 946-949 (**Best Paper Award**)
- D. **Durini**, W. **Brockherde**, B. J. **Hosticka**, "MOS-Capacitor Based CMOS Time-Compression Photogate Pixel for Time-of-Flight Imaging", Proc. *33rd European Solid State Circuit Conference (ESSCIRC) & 37th European Solid-State Device Research Conference (ESSDERC), Munich, Germany*, Sept. 2007, pp. 340-343
- D. **Durini**, W. **Brockherde**, W. **Ulfig**, B. J. **Hosticka**, "Time-of-Flight Imaging Pixel Structures in Standard CMOS Processes", paper revised and accepted to be published in *IEEE Journals of Solid-State Circuits*, July 2008

Thesis:

- E. C. **Nguh**, *Experimental Characterization and Determination of Minority Carrier Lifetimes in the C0512 Process*, Bachelor Thesis, University of Duisburg-Essen, adv. Prof. B. Hosticka, Ph.D. (supervisor D. Durini), September 2005
- E. M. **Mbanya**, *Development of a minority carriers generation lifetime and surface velocity measuring system for CMOS processes to determine the minority carrier generation lifetimes and surface generation velocities of a 0.5µm CMOS standard process*, Bachelor Thesis, University of Duisburg-Essen, adv. Prof. B. Hosticka, Ph.D. (supervisor D. Durini), August 2006
- K. E. **Enowbi**, *Development of a Time-Compression Photogate Pixel for CMOS 2-D Imaging in the 0.5µm Standard CMOS Process*, Bachelor Thesis, adv. Prof. B. Hosticka, Ph.D (supervisor: D. Durini), University of Duisburg-Essen, June 2007
- S. T. **Kabadjeu**, *Measurement of minority carriers recombination and generation lifetimes to be used for mathematical modelling of dark currents present in photosensitive test structures fabricated in a 0.5µm standard CMOS process*, Bachelor Thesis, adv. Prof. B. Hosticka, Ph.D (supervisor: D. Durini), University of Duisburg-Essen, April 2007
- M. **Jung**, *Entwicklung zweier CMOS Imaging-Pixel in einem 0,35µm Standard CMOS Prozess*, Diplomarbeit (M. thesis), adv. Prof. Dr.-Ing. Werner Bonath (supervisor: D. Durini), Fachhochschule Gießen-Friedberg, Fachbereich Elektro- und Informationstechnik, July 2007

E List of Symbols

Symbol	Description	Unit
A_{ph}	Photoactive area	cm^2
C	Capacitance	F
C_j	*p-n* junction diffusion capacitance	F
c	Velocity of light in vacuum (2.99792×10^{10})	cm/s
D_n	Diffusion coefficient of electrons	cm^2/s
D_p	Diffusion coefficient of holes	cm^2/s
d_{OX}	Silicon-oxide thickness in a MOS-C	cm
E_C	Bottom of the conduction band in the energy band diagram	eV
E_F	Energy of the Fermi level	eV
E_g	Energy gap in an energy-band diagram (for Si: 1.1)	eV
E_R	Irradiance	W/cm^2
E_V	Top of the valence band in the energy band diagram	eV
$F(E)$	*Fermi-Dirac* distribution function	
F	Electric Field	V/cm
F_{max}	Maximum electric field	V/cm
f	Frequency	Hz
G_n	Electron generation rate	$cm^{-1}s^{-1}$
G_p	Hole generation rate	$cm^{-1}s^{-1}$
G_{ph}	Carrier photogeneration rate per unit volume	$cm^{-1}s^{-1}$
g_m	MOSFET transconductance	A/V
H	Hamiltonian operator	
h	Planck constant (6.62607×10^{-34})	J·s
I	Current	A
I_{dark}	Dark Current	A
I_{inj}	Injection current	A
I_{ph}	Photocurrent	A
J	Current density	A/cm^2
J_{diff}	Ideal diode saturation (diffusion) current density	A/cm^2
J_{tat}	Trap assisted tunnelling current density	A/cm^2
k_B	Boltzmann constant (1.38066×10^{-23})	J/K
k	Crystal momentum	
L_n	Electron diffusion length	cm
L_p	Hole diffusion length	cm
N_A	Concentration of acceptor impurities	cm^{-3}
N_B	Concentration of doping impurities in silicon	cm^{-3}
N_C	Effective density of states in the conduction band	cm^{-3}
N_D	Concentration of donor impurities	cm^{-3}
N_V	Effective density of states in the valence band	cm^{-3}
m_0	Electron mass	kg
m^*	Effective electron mass	kg

n	Electron density in the conduction band (density of free electrons)	cm^{-3}
$\bar{n}$	Refractive index	
n_i	Carrier concentration in intrinsic silicon (9.65×10^{9} [Sze02])	cm^{-3}
P	Integrated probability density function	
p	Hole density in the valence band (density of free holes)	cm^{-3}
Q	Charge	C
q	Magnitude of elementary charge (1.60218×10^{-19})	C
R	Reflectivity	
$\bar{r}$	Spherical coordinate vector	
S	Optical sensitivity	A/W
s_r	Minority carriers surface generation velocity in silicon	cm/s
s_g	Minority carriers surface recombination velocity in silicon	cm/s
T	Absolute temperature	K
T_{int}	Charge collection (integration) time in a CMOS imager	s
$T_{readout}$	Readout time (U_{PG} pulse rise-time) in CI-PG	s
t	Time	s
U	Bias voltage	V
$U_k(\bar{r})$	Bloch function	
$u(z, t)$	Plane wave	
V_{bi}	Built-in potential	V
V_{br}	*p-n* junction breakdown voltage	V
W_{SCR}	Space-charge (depletion) region width	cm
z	Propagation direction	cm
$\hbar$	Reduced Planck constant ($h/2\pi$) (1.05457×10^{-34})	J·s
α	Absorption coefficient of the medium	1/cm
Γ	Tunnelling via traps dark current generation function	
χ	Electron affinity	eV
ε_0	Permittivity in vacuum (8.85418×10^{-14})	F/cm
ε_{OX}	Oxide (SiO_2) dielectric constant (3.9)	F/cm
ε_{Si}	Silicon dielectric constant (11.9)	F/cm
Φ	Radiant flux	W
Φ_{ph}	Photon flux	1/s
$q\phi_m$	Metal (polysilicon) work function	eV
γ	Bias-dependent excess noise parameter	
η	Quantum efficiency	
λ	Wavelength	cm
μ_n	Electron mobility	$cm^2/V\cdot s$
μ_p	Hole mobility	$cm^2/V\cdot s$
ν	Frequency of light	Hz
σ	Standard deviation	
σ^2	Variance	
τ_c	Carrier mean free time between collisions	s
τ_{r_n}	Electron recombination time in silicon	s
τ_g	Minority carriers generation time in silicon	s
τ_{r_p}	Hole recombination time in silicon	s
ω	Angular frequency of the wave ($2\pi f$ or $2\pi\nu$)	Hz

ω_s	Phonon angular frequency	Hz
Ψ	Wave function	
ψ_B	Barrier potential	V