Advanced Converter Control Techniques for Improving the Performances of DFIG based Wind Turbines

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Abstract

Among the renewable energy alternatives, wind energy has made the biggest impact on the total energy production in the last decade. Maintaining or improving the reliability of the wind turbine system in power generation sector with optimal performances is one of the important tasks. Especially the wind turbines connected to the grid are subjected to certain electricity grid connection regulations specified in grid codes. A detailed study of the performance of wind turbine systems in various case scenarios is necessary, so that appropriate solutions can be recommended, especially in the converter controls which play the major role in the overall system.

In this thesis, the doubly fed induction generator (DFIG) which is still the most widely used wind turbine type is selected for detailed investigation. Its performances during steady state operation in two alternative scenarios, namely, using different pulse width modulation (PWM) types and using different converter topologies, are investigated. The performance criteria include generated common mode voltage at machine side converter (MSC), current total harmonic distortion in the low voltage network, converter power losses and reactive power capability. Additionally, the component counts in the converter and its estimate cost are compared.

Regarding the first scenario, the influence of different PWM types on the converter power losses, the reactive power capability and the total harmonic distortion has been investigated in detail, and the most suitable PWM type depending on the optimal performance criteria as well as operational speed range is proposed.

In the second scenario, two different converter topologies, namely back-to-back two-level converter and back-to-back three-level neutral point clamped (NPC) converter were implemented in the simulation model, and on the basis of the simulation results their performances in terms of cost against the accruing operational advantages are compared.

Finally, a new protection scheme for fault ride-through in back-to-back three-level NPC converter is proposed as an alternative to conventional protection scheme using DC-link chopper. The proposed scheme shows a very similar dynamic behaviors with the conventional scheme when the inner IGBTs of the MSC are designed for about two times higher current rating than the over-current protection limit. Furthermore, it implements simpler operation without higher component count. The need for the inner IGBTs with higher current rating significantly increases the cost of the MSC. However, the total cost of the DFIG system is slightly reduced about 15% by the elimination of the DC-link chopper circuit.

Abstrakt

Unter den alternativen erneuerbaren Energiequellen hat Windenergie in den letzten zehn Jahren den größten Stellenwert im Energieerzeugungssystem erlangt. Die Erhaltung bzw. die Verbesserung der Zuverlässigkeit des Stromversorgungsnetzes mit zunehmenden Windenergieanlagen und deren optimale Nutzung ist eine der wichtigsten Aufgaben. Die Windenergieanlagen sind im Netzbetrieb bestimmten in Netzanschlussrichtlinien angegebenen Anschlussregeln unterworfen. Dies erfordert eine detaillierte Untersuchung von Windenergieanlagen in verschiedenen operativen Szenarien, so dass geeignete Lösungen empfohlen werden können, insbesondere bezüglich Umrichter-Regelung, die die Hauptrolle im Gesamtsystem spielen.

In dieser Forschung wurde der doppelt-gespeiste Asynchrongenerator, der immer noch am häufigsten verwendeter Windturbinentyp ist, für eine detaillierte Untersuchung ausgewählt. Sowohl das Betriebsverhalten im stationären Betrieb allgemein als auch unter Berücksichtigung von zwei alternativen Pulsweiten-Modulation (PWM)-Typen und verschiedenen Umrichter-Topologie, untersucht. Vergleichskriterien sind die erzeugte maschinenseitige „common mode“ Spannung, Gesamtverzerrung der Stromwelle im Niederspannungsnetz, Umrichter-Leistungsverluste und Blindleistung-Einspeisefähigkeit. Zusätzlich werden die Anzahl der Komponenten im kompletten Umrichter-System und die geschätzten Kosten als Vergleichskriterien herangezogen.

Bezüglich des ersten Szenarios, der Einfluss unterschiedlicher PWM-Typen auf Umrichter Verlustleistung, die Blindleistung-Einspeisefähigkeit und die gesamte harmonische Verzerrung wurden im Detail untersucht, und der am besten geeignete PWM-Typ bezüglich optimaler Leistungskriterien sowie Drehzahlbereiche vorgeschlagen.

Im zweiten Szenario wurden zwei verschiedene Umrichter-Topologie, nämlich zweistufiger „Back-to-Back“ Umrichter und dreistufiger „Neutral-Point-Clamped (NPC)“ „Back-to-Back“ Umrichter wurden im Simulationsmodell implementiert, und auf der Grundlage der Simulation Ergebnisse ihre Eignung in Bezug auf Kosten gegen die anfallenden Betriebsvorteile verglichen.

Schließlich wurde ein neues Schutzschema für „Fault-Ride-Through“ im dreistufigen „Back-to-Back“ NPC-Umrichter als Alternative zum konventionellen Schutzschema mit Chopper im Gleichspannung-Zwischenkreis vorgeschlagen. Das vorgeschlagene Schema zeigt ein sehr ähnliches dynamisches Verhalten wie das konventionelle Schema, wenn die inneren IGBTs des maschinenseitigen Wechselrichters (MWR) für etwa zweifachen Nennstrom der Überstromschutzgrenze ausgelegt werden. Außerdem ermöglicht eine einfachere Bedienung

ohne höhere Anzahl von Komponenten. Die Verwendung von inneren IGBTs mit höherem Nennstrom erhöht die Kosten der MWR. Jedoch werden die Gesamt Kosten um etwa 15% weniger, da der Chopper im Gleichspannung-Zwischenkreis dadurch überflüssig gemacht wird.

Acknowledgement

First of all and always I thank almighty ‘Allah’ for giving me the strength and health to carry out the work in this thesis.

This dissertation is not the result of a few weeks or months of work, but rather of years of work. It would not have been possible without the help and support of many people. Therefore, I thank all those who have directly or indirectly supported me in this endeavor. Of these generous people, I take this opportunity to thank a few by name.

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List of Symbols

p	Active power in [p.u.]
q	Reactive power in [p.u.]
ω	Angular frequency in [p.u.]
r	Length of rotor in [m]
v	Speed in [m/s]
ρ	Air density in [kg/m^3]
A	Area in [m^2]
c_p	Power coefficient in [p.u.]
λ	Tip speed ratio in [p.u.]
β	Pitch angle in [°]
t	Time in [p.u.]
α	Angle of attack in [°]
t	Torque in [p.u.]
J	Inertia constant in [p.u.]
k_Sh	Shaft stiffness constant in [p.u./rad]
d_Sh	Shaft damping constant in [p.u.]
θ	Mechanical angle in [p.u.]
u	Instantaneous voltage in [p.u.]
i	Instantaneous current in [p.u.]
ψ	Instantaneous flux in [p.u.]
r	Resistance in [p.u.]
l	Inductance in [p.u.]
σ	Leakage coefficient in [p.u.]
x	Reactance in [p.u.]
z	Impedance in [p.u.]
C	Capacitor in [F]
R	Resistor in [Ω]
L	Inductor in [H]
s_gen	Generator slip
$\mathrm{T_x}$	IGBT component
$\mathrm{D_x}$	Freewheeling diode component
$\mathrm{P_x}$	NPC diode component

s	Complex frequency in [p.u.]
δ	Damping coefficient in [p.u.]
τ	Time constant in [p.u.]
k	Gain factor in [p.u.]
T_S	Fundamental pulse period in [s]
φ	Power factor angle in [°]
M	Modulation index
a, b, c	Three phase quantities
E	Switching energy losses in [mJ]
U	Voltage in [V]
I	Current in [A]
P	Power losses in [W]
Z	Thermal impedance in [K/W]
T_j	Junction temperature in [°C]
D	Duty cycle in [s]
h	Harmonic order

List of Abbreviations

AC	Alternating current
APOD	Alternative phase opposition disposition
CMV	Common mode voltage
CPWM	Continuous pulse width modulation
D	Drag
DC	Direct current
DFIG	Doubly fed induction generator
DPWM	Discontinuous pulse width modulation
DPWM0	Discontinuous PWM with 0 modulation phase angle
DPWM1	Discontinuous PWM with $\pi/6$ modulation phase angle
DPWM2	Discontinuous PWM with $\pi/3$ modulation phase angle
DPWM3	Discontinuous PWM with $\pi/4$ modulation phase angle
FC	Flying capacitor
FOM	Full order model
FRT	Fault ride-through
GTO	Gate turn-off thyristor
H	Hybrid
HDF	Harmonic distortion factor
HVDC	High voltage direct current
IGBT	Insulated gate bipolar transistor
IGCT	Integrated gate commutated thyristor
L	Lift
LSC	Line side converter
LV	Low voltage
MOSFET	Metal oxide semiconductor field effect transistor
MSC	Machine side converter
NPC	Neutral point clamped
OCP	Over-current protection
OP	Operating point
PD	Phase disposition
PMSG	Permanent magnet synchronous generator
POD	Phase opposition disposition

PS	Phase shifted
PWM	Pulse width modulation
SCIG	Squirrel cage induction generator
SIC	Super imposed carrier
SLF	Switching loss function
SPWM	Sinusoidal pulse width modulation
STHIPWM4	1/4 peak value of sinusoidal third harmonic injection PWM
STHIPWM6	1/6 peak value of sinusoidal third harmonic injection PWM
SVPWM	Space vector PWM
THD	Total harmonic distortion
TTHIPWM	1/4 peak value of triangular third harmonic injection PWM
WRIG	Wound rotor induction generator
WT	Wind turbine

1 Introduction

In recent years, renewable energy resources such as wind, solar, geothermal, biomass, etc. have become important resources for present and future electrical energy demand all over the world. This is due to growing environmental, economical, and political concerns on the electrical energy production using fossil fuels such as coal, petroleum, and natural gas. Among the renewable energy alternatives, wind energy has made the biggest impact on the total energy production in the last decade.

This chapter provides an overview of the wind energy status around the world. A brief historical development in wind turbine generating systems is presented. Subsequently, the aims of the thesis are stated and finally the structure of the report is outlined.

1.1 Background

The power of the wind has been utilized for at least 3000 years. Until the early twentieth century wind power was used to provide mechanical power to pump water or to grind grain. At the beginning of modern industrialization, the use of the fluctuating wind energy resource was substituted by fossil fuel fired engines or the electrical grid, which provided a more consistent power source.

In the early 1970s, interest in the power of the wind re-emerged after the oil crisis. This time, the main focus was on wind power providing electrical energy instead of mechanical energy. From this time, the technology was improved step by step. By the end of the 1990s, wind energy has re-emerged as one of the most important sustainable energy resources. It has increased dramatically and several international forecasts expect the growth to continue. Figure 1-1 shows the global cumulative installed wind capacity from 1996 to 2012, while Figure 1-2 shows the wind capacity forecast from 2013 to 2017 [1]. It is forecasted that the cumulative capacity growth rate will be between 12% - 19% and the cumulative installed wind capacity will reach about 536 GW in the 2017 [1]. This growth is being enabled by advanced wind turbine production technologies based on the aerodynamic, civil, mechanical, and electrical engineering fields; hence, wind energy is converted to electrical energy economically and marketed at competitive prices with the electricity produced by the conventional power plants such as thermal, hydro, and nuclear power plants.

Maintaining or improving the reliability of the wind turbine system in power generation sector with optimal performances is one of the important tasks. Especially the wind turbines connected to the grid are subjected to certain electricity grid connection regulations specified

in grid codes. This task can be contributed by the power electronic converters which play the major role for improving the electrical performances in the overall system.

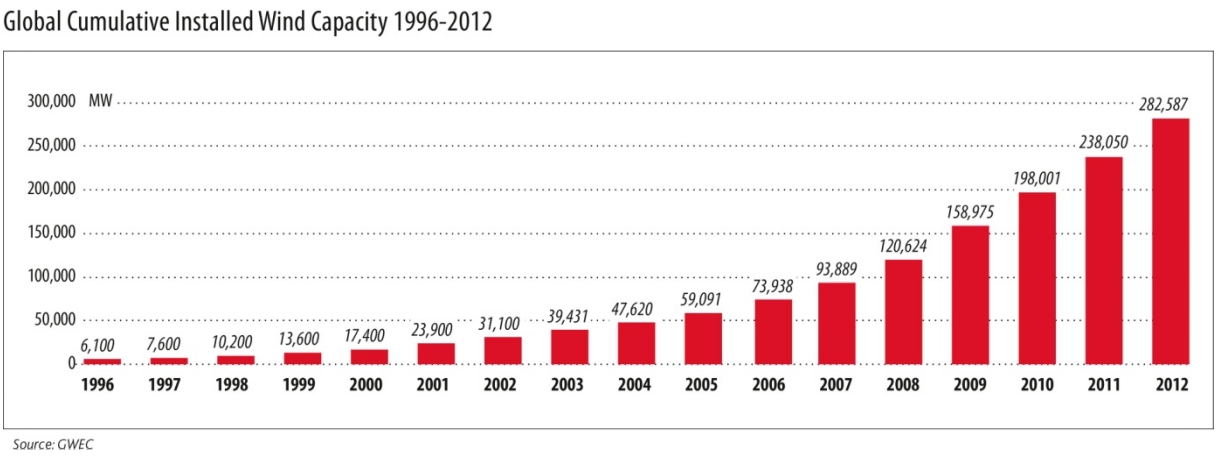


Figure 1-1: Global cumulative installed wind capacity [1]

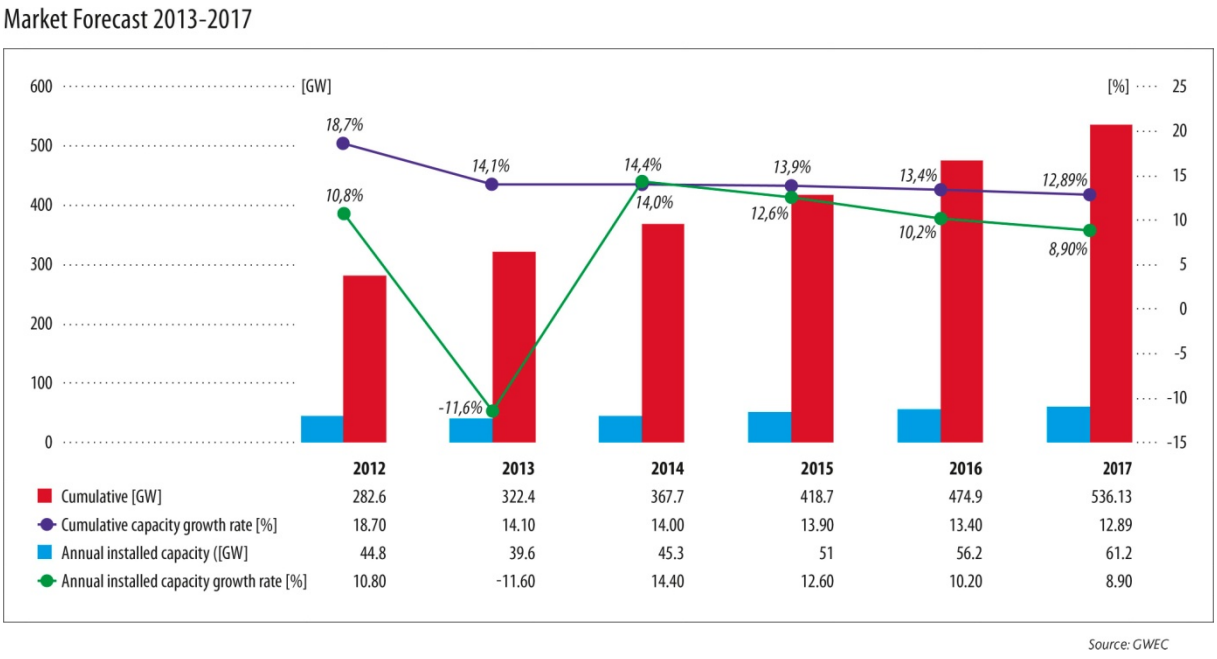


Figure 1-2: Market forecast installed wind capacity [1]

1.2 Objectives of the thesis

As described in the previous section, the wind turbines contribute an important role in the renewable power generation system. Among them, doubly fed induction generators (DFIGs) are the most widely used wind turbine generation system. Thus, this thesis focuses only on the DFIG based wind turbine (WT). A detailed study of the performance of the DFIG systems in various case scenarios is necessary, so that appropriate solutions can be recommended to

improve the system with optimal performances. Therefore, the thesis is written with objectives as follows:

- Development of the dynamic model of DFIG based WT connected to the grid which enable operating with two different converter topologies namely two-level converter and three-level neutral point clamped (NPC) converter including their control structure.
- Overview and analysis of existing switching methods of the insulated gate bipolar transistors (IGBTs) to have an idea of choosing appropriate switching technique for optimal performances in switching losses and harmonic distortion level.
- Development and analysis of the converter power losses model and thermal model which to be implemented in the simulation model.
- Evaluation the performance of DFIG based WT in terms of generated common mode voltage at machine side converter (MSC), converter power losses, harmonic distortion level in the low voltage network and reactive power capability during steady state operation in two alternative scenarios, namely using different pulse width modulation (PWM) types and using different converter topologies.
- Analysis of the results obtained from the simulation of the two scenarios and recommend solution for optimal performances.
- Development of a new protection scheme using zero state switching for improved fault ride-through of the DFIG during grid faults. Then, analysis of their dynamic behavior and comparison with conventional protection scheme using DC-link chopper.
- Analysis of the components count and their cost for different converter topologies (two-level and three-level NPC converter). Also the cost comparison when using the new protection scheme in the three-level NPC converter.

1.3 Outline of the thesis

The thesis starts with general introduction in chapter 1 discusses wind energy background, objectives and contents of the thesis. Historical development and current status of wind power is summarized at the beginning.

Chapter 2 provides an overview of the most common WT concepts. Basic configurations and characteristics of different wind generator systems are described. The thesis focuses on the variable speed system with partial-scale power converter which is also known as the DFIG system. Thus, it has been explained in detail including its advantages and disadvantages.

Chapter 3 describes the modeling of DFIG based WT that is implemented in Matlab/Simulink environment. Detailed model is approached for dynamic simulation. The model system is generally separated into mechanical part and electrical part. The main focus is the power converter model where two different topologies are proposed, namely two-level converter and three-level NPC converter.

Chapter 4 discussed the derivation and analysis of the control system of the DFIG based WT. This includes the control of rotor blade, speed control and converter control. The standard controller for controlling the back-to-back converter is defined which is applicable for both two-level and three-level converter topologies.

This is followed in chapter 5 by the overview and analysis of basic concepts of converter switching. The well known switching schemes and the standard pulse width modulation (PWM) types are describes. From the literature analysis, the PWM switching scheme is selected for further investigation. Among the standard PWM types, four types are selected and proposed to be applied for the switching of the IGBTs. The performance comparison in terms of switching losses and harmonics distortion level among the PWM types is analyzed. Then, the switching generation method for both two-level and three-level NPC converter is defined.

In chapter 6, power losses model and thermal model for both converters are developed. Power losses model is first developed since their outputs are required for the thermal model. This includes the derivation of conduction losses, switching losses and total power losses of the IGBT/diode. The calculation of power losses model are based on the manufacturer parameters that can be obtained from the semiconductor datasheets. To develop the power losses model for two-level and three-level NPC converter, analysis of IGBT switching state, its commutation and suitable IGBT technology are first performed. From the obtained data of power losses, the thermal model is developed which is also defined the junction temperature of IGBTs. The analysis in this chapter correlates to the evaluation of the performances in power losses and reactive power capability.

Chapter 7 investigates the performances of DFIG based WT in two different cases, namely using different PWM types in two-level converter and using different converter topologies. In the beginning, the performance indexes are described. This includes the generated common mode voltage at MSC, the current total harmonic distortion in the low voltage network, the converter power losses and the reactive power capability of the DFIG system. In each case, the performance indexes are analyzed, and then appropriate solution for optimal performances is recommended. A verification of the power losses and thermal model described in the

chapter 6 is also included in this chapter. The results are compared with the standard manufacturer simulator, namely SEMISEL from Semikron which available online.

Chapter 8 focuses of the protection schemes for three-level NPC converter of the DFIG based WT. It starts with the introduction of the current grid code requirements concerning fault ride-through (FRT). The existing protection schemes for FRT including crowbar and DC-link chopper are reviewed. Then, a new protection scheme which using the control of zero state switching is proposed and described. This protection scheme allows safe FRT without the need for additional protection hardware. Detailed time domain simulation studies are presented in this chapter to illustrate the effect of the protection schemes during symmetrical and unsymmetrical grid faults. Simulation studies prove the similar dynamic performance of the proposed scheme with the conventional scheme. In the end, component count and cost comparison of the back-to-back three-level NPC converter between the two protection schemes are evaluated.

Chapter 9 summarizes the main results and conclusions within the scope of the research work performed and reported in this thesis. Possible further research topics are also highlighted.

2 Wind Turbine Concepts

Based on the rotation speed, wind turbine (WT) concepts can be grouped into fixed speed, limited variable speed and variable speed. For variable speed WT, based on the rating of power converter related to the generator capacity, they can be further grouped into wind generator systems with a partial-scale and a full-scale power electronic converter. The most common in operation of the variable speed partial-scale power converter WT is doubly fed induction generator (DFIG), while in the variable speed full-scale power converter WT is permanent magnet synchronous generator or squirrel cage induction generator in combination with a frequency converter, which is designed for the full WT electrical power. It can be summarized as below:

- Fixed speed system
- Limited variable speed system
- Variable speed system
    - Full-scale power converter: Permanent magnet synchronous generator or squirrel cage induction generator in combination with a frequency converter.
    - Partial-scale power converter: Doubly fed induction generator.

In this chapter, according to contemporary WT concepts, the basic configurations and characteristics of different wind generator systems are explained.

2.1 Fixed speed system

The fixed speed system consists of a gearbox and a squirrel cage induction generator (SCIG) which is directly connected to the grid through a transformer. Figure 2-1shows a typical configuration of that type. The generator offers no option for electrical control and it always consumes reactive power from the grid. Due to that reason, this type was extended with a capacitor bank for reactive power compensation. Smoother grid connection was also achieved by incorporating a soft-starter.

The well-known advantages of this system are it is robust, easy and relatively cheap for mass production. In addition, it enables stall-regulated machines to operate at a constant speed when it is connected to a large grid, which provides a stable control frequency. The power control of fixed speed system can be implemented as stall or active stall control. While the first only roughly limits the output power through the stall characteristic of the rotor blades, the latter results in a constant power output above nominal wind speed. The disadvantages of the fixed speed system are mainly on its speed controllability and its cost. The speed is not

controllable and variable only over a very narrow range, in which only speeds higher than the synchronous speed are possible for generator operation. The installation of capacitor bank and the large mass of gearboxes invest a very expensive cost [2]-[9].

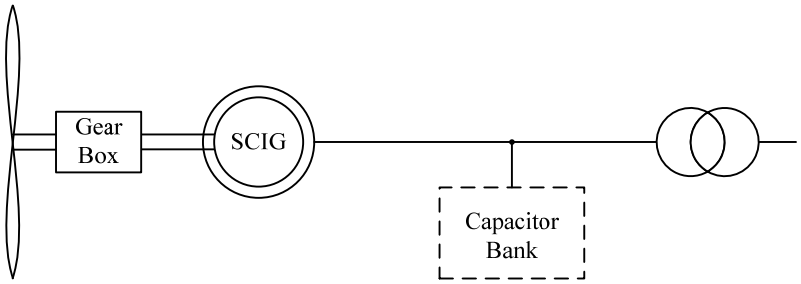


Figure 2-1: Fixed speed wind turbine system

2.2 Limited variable speed system

The limited variable speed system consists of a gearbox and a wound rotor induction generator (WRIG) with variable rotor resistance by means of a power electronic converter, as shown in Figure 2-2.

The stator of WRIG is directly connected to the grid, whereas the rotor winding is connected in series with a controlled resistor. The main limiting factors of this approach are the rotor losses, which increase with the speed range. The dynamic speed control range depends on the size of the variable rotor resistance, and the energy extracted from the external resistor is also dumped as heat loss in the controllable rotor resistance. A typical limited variable speed range is less than 10% above the synchronous speed [2]-[4], [6]. Like the fixed speed system, the limited variable speed system is a reactive power consumer and requires compensation devices. A soft-starter is also required for this type.

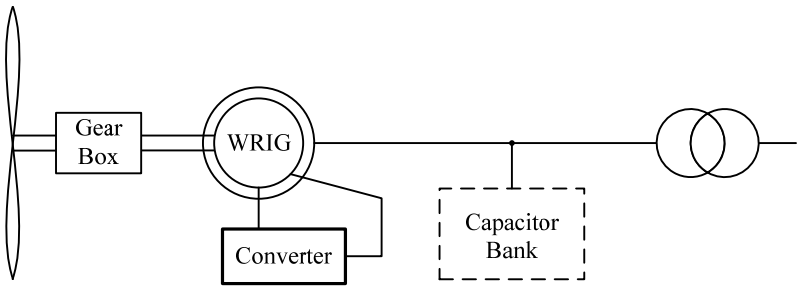


Figure 2-2: Limited variable speed wind turbine system

2.3 Variable speed system

Variable speed systems are generally grouped into the full-scale power converter and the partial-scale power converter. When compared between both types, the full-scale power converter can perform smooth grid connection over the entire speed range. However, it has a

higher cost and a higher power loss in the power converter, since all the generated power has to pass through the power converter.

Commonly, the variable speed systems are equipped with pitch controlled rotor blades for power limitation above nominal wind speed. A braking chopper in the DC circuit is used to dissipate the generated power during grid faults. A line inductor and an output filter are used at the line side converter for enhanced power quality.

2.3.1 Variable speed system with full-scale power converter

Basically, a type of variable speed system with full-scale power converter used in the market is permanent magnet synchronous generator (PMSG) or SCIG in combination with a frequency converter. The scheme of a grid-connected WT with PMSG or SCIG is shown in Figure 2-3.

In recent years, the use of PMSG is more attractive than before, because the performance of PMSG is improving and the cost is decreasing. PMSG is not standard off-the-shelf machines and they allow a great deal of flexibility in their geometry, so that various topologies may be used. PMSG can be classified into the following types: the radial flux, the axial flux and the transversal flux, based on the direction of flux penetration.

PMSG does not require energy supply for excitation, as it is supplied by the permanent magnets. The stator of a PMSG is wound and the rotor has a permanent magnet pole system. The salient pole of PMSG operates at low speeds, and thus the gearbox can be removed. The advantages of PMSG over electrically excited machines can be summarized as follows according to literatures [2], [10]-[17]:

- Higher efficiency and energy yield due to lower generated power losses in the machine.
- No additional power supply for the magnet field excitation.
- Improvement in the thermal characteristics due to the absence of field losses.
- Higher reliability due to the absence of mechanical components such as slip rings.
- Lighter and therefore higher power to weight ratio.

However, PMSG has some disadvantages, which can be summarized as follows:

- High cost of PM material.
- Difficulties to handle in manufacture.
- Demagnetization of PM at high temperature.

The SCIG has also the same scheme with the PMSG as shown in Figure 2-3. However, the SCIG is not very popular compared to the PMSG due to their main disadvantage where

having problem with obtaining excitation current from the stator terminal. A higher maintenance of the gearbox also make not attractive for this scheme.

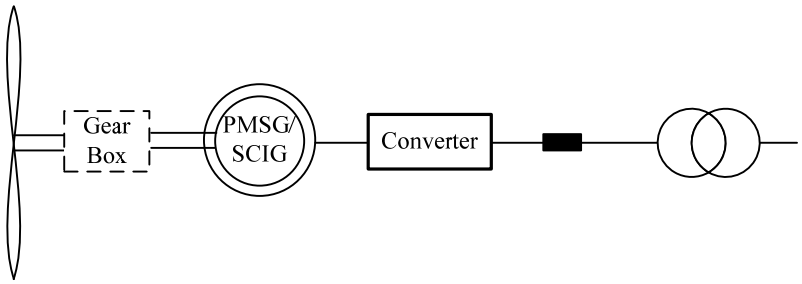


Figure 2-3: PMSG or SCIG wind turbine system with full-scale power converter

Compared with the fixed speed system, the variable speed system with full-scale power converter type has advantages of the flexible control with a full-scale power, such as variable speed operation, better performances of reactive power compensation and smooth grid connection. However, their disadvantage is the higher cost and losses of the full-scale converter, and the efficiency of the total system (gearbox induction generator and converter) may be low.

2.3.2 Variable speed system with partial-scale power converter

This configuration is known as the DFIG based WT, which corresponds to a variable speed system with a WRIG and a partial-scale power converter on the rotor circuit, as illustrated in Figure 2-4. The stator is directly connected to the grid, whereas the rotor is connected through a power electronic converter. The power converter controls the rotor frequency and thus the rotor speed. This concept supports a wide speed range operation, depending on the size of the frequency converter. Typically, the variable speed range is ±30% around the synchronous speed [2]-[6]. The rating of the power electronic converter is only 25-30% of the generator capacity, which makes this concept attractive and popular from an economic point of view.

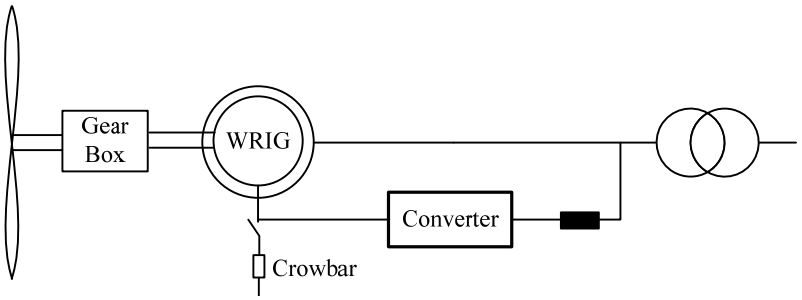


Figure 2-4: DFIG based wind turbine system

A rotor crowbar is used to protect the rotor side converter against over-currents and the DC capacitors against over-voltages during grid faults. But a crowbar ignition means the loss of the generator controllability through the machine side converter (MSC), since the machine rotor is short-circuited through the crowbar resistors and the MSC is blocked. During this time slot the generator acts as a common induction generator and consumes reactive power, which is not desirable from grid point of view. In order to avoid a crowbar ignition for most fault scenarios, a DC chopper is used to limit the DC voltage by short-circuiting the DC circuit through the chopper resistor.

The DFIG system has advantages where the rotor energy, instead of being dissipated, can be fed into the grid by the power electronic converter. Moreover, the power converter system can perform reactive power compensation and smooth grid connection, for example, the line side converter (LSC) can control its reactive power, independently of the generator operation; this allows the performance of voltage support towards the grid. However, the DFIG system has the following disadvantages [2]-[4], [6], [10].

- A gearbox is still necessary in the drive train because the speed range for DFIG is far from a common turbine speed of 10-25 rpm. A gearbox is inevitable to have some drawbacks, such as heat dissipation from friction, regular maintenance and audible noise.
- The slip ring is used to transfer the rotor power by means of a partial-scale converter, which requires a regular maintenance, and maybe result in machine failures and electrical losses.
- Under grid fault conditions, large stator currents result in large rotor currents and could cause damages to the power electronic switches, rotor windings and DC-link capacitor. Thus, protection circuit in rotor circuit or DC-link is necessary.
- According to grid connection requirements for wind turbines, in case of grid disturbances, a ride-through capability of DFIG is also required, so that the corresponding control strategies may be complicated.

3 Modeling of DFIG based Wind Turbines

The main goal of this study is to develop enhanced converter control strategies for DFIG based wind turbines (WTs) and to investigate their performances in term of harmonics distortion level, power losses, reactive power capability and generated common mode voltage. For this purpose it is essential to develop appropriate realistic models for the electrical system as well as for the mechanical part of the WT. The mechanical part of the WT includes aerodynamic model and drive train model, while the electrical system includes generator, power electronics converter, DC circuit and transformer. An overview over the modeling scheme is illustrated in Figure 3-1.

In this chapter, the model of the mechanical system and the electrical system are presented. DFIG based WT of 2 MW power will be investigated. Parameters of the machine and the control system are based on manufacturer data, and the simulation results are intended to reflect the existing reality as accurately as possible. The DFIG based WT model are developed using Matlab/Simulink environment.

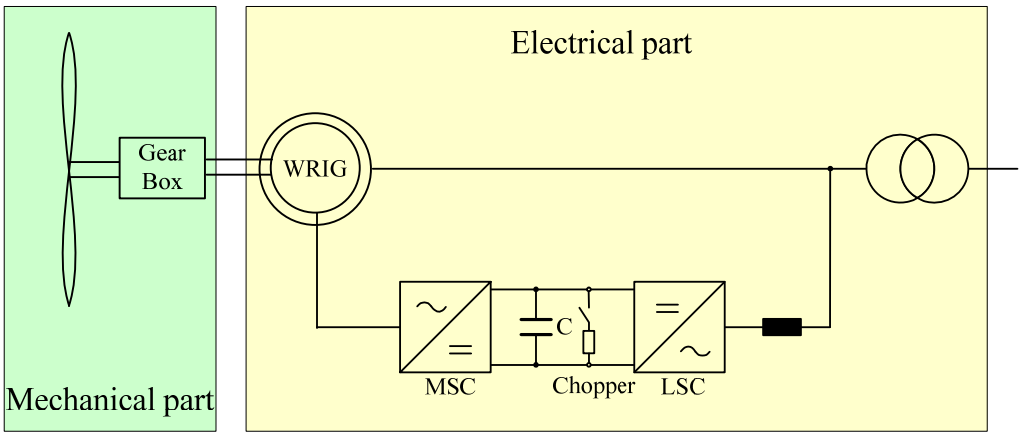


Figure 3-1: Modeling scheme of mechanical and electrical system of DFIG based WT

3.1 Aerodynamic model

Figure 3-2 illustrates the cross section of WT blade. The kinetic energy obtained by the blades from the wind is transformed to mechanical torque on the rotor shaft of the WT. The blades are attached to the rotor shaft and rotate with the tip speed $\omega_{rot} \times r$, where r is the length of the blade. The blade profile experiences a relative wind velocity generated by the superposition of the tip speed and the wind velocity v_w. While wind is passing the profile it introduces lift (L)

and drag (D) forces on the blade, which results in movement of the blade. From these forces the power obtained from the wind can be calculated as:

$$P_{\mathrm{W}} = \frac{1}{2}\rho A_{\mathrm{rot}} c_{\mathrm{p}}(\lambda,\beta) v_{\mathrm{w}}^{3} \tag{3.1}$$

With the power coefficient:

$$c_{\mathrm{p}}(\lambda,\beta) = \frac{P_{\mathrm{W}}(\lambda,\beta)}{P_{\mathrm{wind}}} \tag{3.2}$$

And the tip speed ratio:

$$\lambda = \frac{\omega_{\mathrm{rot}} \cdot r}{v_{\mathrm{w}}} \tag{3.3}$$

Thereby ρ is the air density, v_{w} is the free wind speed experienced by the rotor and A_{rot} is the swept rotor area. The power coefficient depends upon the pitch angle β.

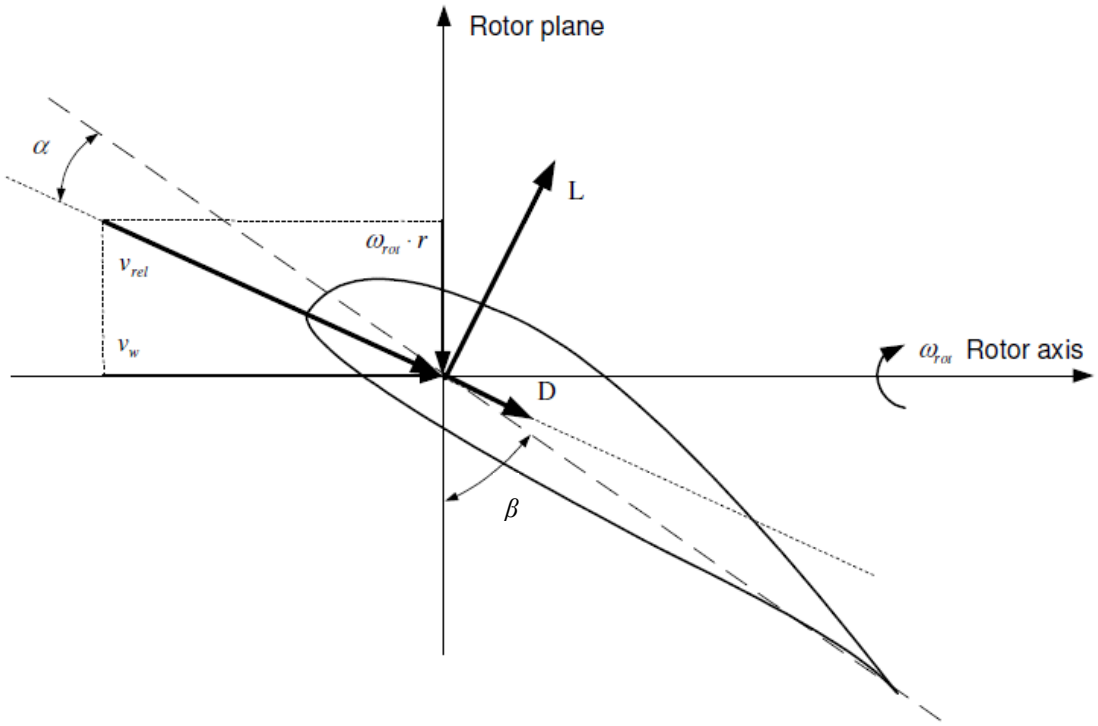


Figure 3-2: Cross section of wind turbine blade (α is the angle of attack) [18]

Usually, the power coefficient curves are provided by the manufacturers of the rotor blades in form of data tables. Figure 3-3 shows the power coefficient curves of a multi-MW pitch controlled wind turbine.

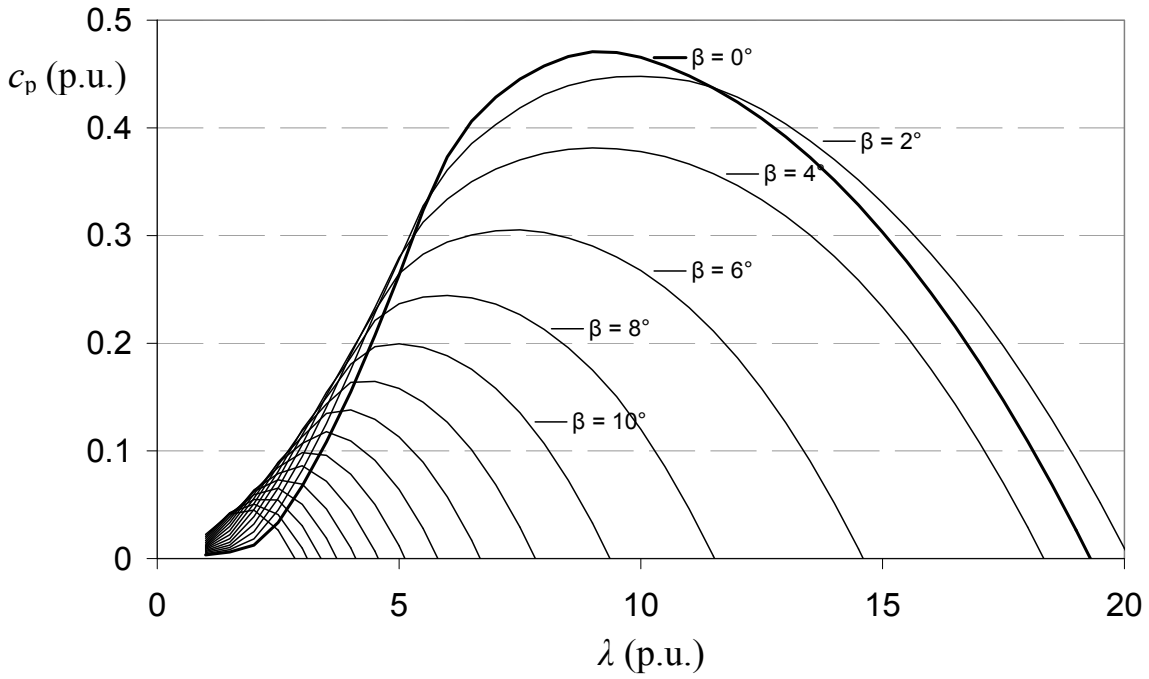


Figure 3-3: c_p-curves of a multi-MW pitch controlled wind turbine [19]

3.2 Drive train model

In this section the simplified drive train model of the wind turbine will be described. This dynamical model has been explained in many literatures [20]-[30] and is widely accepted as expressing the dynamical behavior of the drive train for the area of research.

The wind turbine drive train can be modeled as a two-mass system coupled through a gear train as shown in Figure 3-4. The quantities on the wind turbine rotor side of the gearbox can be reflected to the generator side. This eliminates the gear ratio and results in a two-mass representation of the wind turbine. Neglecting the effects of the gearbox moment of inertia, damping, and stiffness is justifiable since the moment of inertia of the wind turbine rotor is comparatively very high.

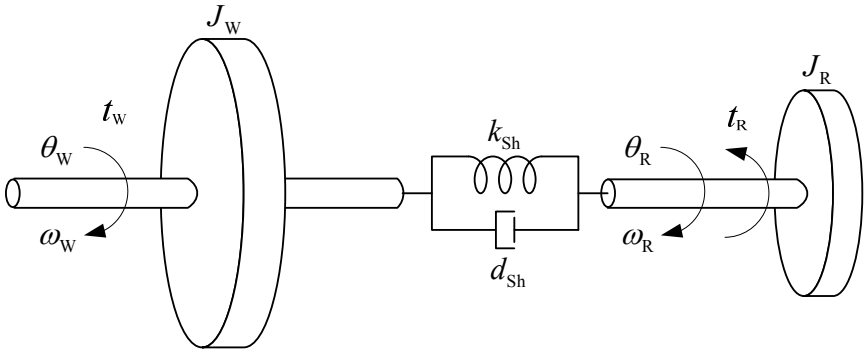


Figure 3-4: Two-mass model of the wind turbine drive train

Torque equations representing the mechanical behavior of the wind turbine are derived based on the two-mass model. The aerodynamic torque from the wind turbine rotor and the electromechanical torque from the direct-connect induction generator act in opposition to each other.

According to the momentum theorem [31], the two-mass model can be described by the following equations where all quantities referred to the generator side.

$$\frac{\mathrm{d}\omega_{\mathrm{W}}}{\mathrm{d}t} = \frac{1}{J_{\mathrm{W}}}\left(t_{\mathrm{W}} - k_{\mathrm{Sh}}\Delta\theta - d_{\mathrm{Sh}}\Delta\omega\right) \tag{3.4}$$

$$\frac{\mathrm{d}\omega_{\mathrm{R}}}{\mathrm{d}t} = \frac{1}{J_{\mathrm{R}}}\left(-t_{\mathrm{R}} + k_{\mathrm{Sh}}\Delta\theta + d_{\mathrm{Sh}}\Delta\omega\right) \tag{3.5}$$

The mechanical speed and angle difference are given as:

$$\frac{\mathrm{d}\Delta\theta}{\mathrm{d}t} = \frac{\mathrm{d}\left(\theta_{\mathrm{W}} - \theta_{\mathrm{R}}\right)}{\mathrm{d}t} = \Delta\omega = \omega_{\mathrm{W}} - \omega_{\mathrm{R}} \tag{3.6}$$

where,

$J_{\mathrm{W}}, J_{\mathrm{R}}$ = moments of inertia of the wind turbine rotor and the generator [p.u.]

$t_{\mathrm{W}}, t_{\mathrm{R}}$ = wind turbine aerodynamic and generator electromagnetic torque [p.u.]

$\omega_{\mathrm{W}}, \omega_{\mathrm{R}}$ = wind turbine rotor and the generator speed [p.u.]

$\theta_{\mathrm{W}}, \theta_{\mathrm{R}}$ = angular position of the rotor and the generator [p.u.]

$k_{\mathrm{Sh}}, d_{\mathrm{Sh}}$ = equivalent stiffness and damping [p.u/rad], [p.u.]

3.3 Generator model

The generator of the DFIG based WT system is an induction machine with a wound rotor, which is connected via a power converter, while the stator is directly connected to the grid. The converter supplies an additional rotor voltage with slip frequency to the rotor terminals. The variable rotor voltage assures variable speed operation of the generator and allows independent control of the generator's active and reactive power. Depending on the rotor voltage's amplitude and phase, the generator operates in sub-synchronous or super-synchronous operation. In sub-synchronous operation the converter feeds power into the rotor, while in super-synchronous operation the rotor power is fed via the converter back to the grid. The power flow in the converter is thus bi-directional, as can be shown in Figure 3-5. The converter must therefore consist of self-commutated semiconductors, allowing power flow in both directions. The selection of power semiconductor will be described in section 3.4.1.

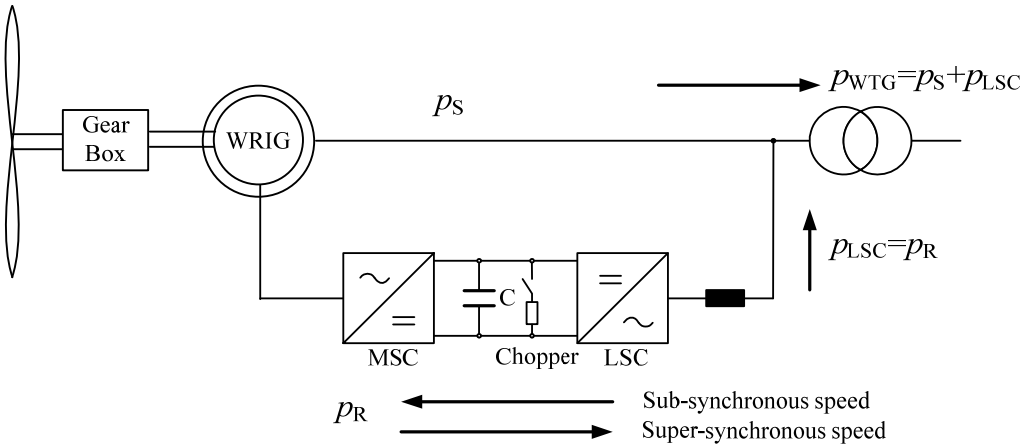


Figure 3-5: Power flow in the DFIG based WT

3.3.1 Full-order model

The full-order model (FOM) of the DFIG is based on the dynamic equations of stator and rotor voltage given in Eq. (3.7)-(3.10), which considers the physical three-phase quantities with the generator reference arrow system shown in Figure 3-6.

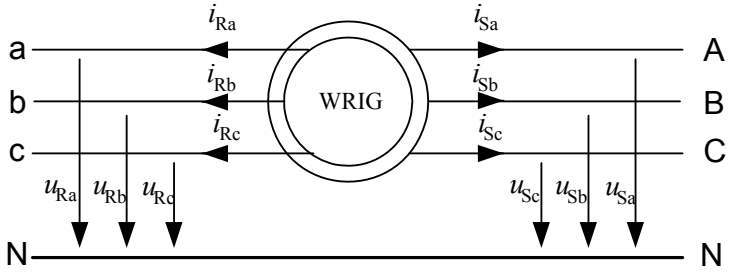


Figure 3-6: Slip–ring induction generator with measured quantities

Voltage equations:

$$\begin{pmatrix} u_{Sa} \\ u_{Sb} \\ u_{Sc} \end{pmatrix} = -r_S \begin{pmatrix} i_{Sa} \\ i_{Sb} \\ i_{Sc} \end{pmatrix} - \frac{d}{dt} \begin{pmatrix} \psi_{Sa} \\ \psi_{Sb} \\ \psi_{Sc} \end{pmatrix} \tag{3.7}$$

$$\begin{pmatrix} u_{Ra} \\ u_{Rb} \\ u_{Rc} \end{pmatrix} = -r_R \begin{pmatrix} i_{Ra} \\ i_{Rb} \\ i_{Rc} \end{pmatrix} - \frac{d}{dt} \begin{pmatrix} \psi_{Ra} \\ \psi_{Rb} \\ \psi_{Rc} \end{pmatrix} \tag{3.8}$$

Flux equations:

$$\begin{pmatrix} \psi_{Sa} \\ \psi_{Sb} \\ \psi_{Sc} \end{pmatrix} = l_S \begin{pmatrix} i_{Sa} \\ i_{Sb} \\ i_{Sc} \end{pmatrix} + l_M \begin{pmatrix} i_{Ra} \\ i_{Rb} \\ i_{Rc} \end{pmatrix} \tag{3.9}$$

$$\begin{pmatrix}\psi_{\mathrm{Ra}}\\ \psi_{\mathrm{Rb}}\\ \psi_{\mathrm{Rc}}\end{pmatrix}=l_{\mathrm{M}}\begin{pmatrix}i_{\mathrm{Sa}}\\ i_{\mathrm{Sb}}\\ i_{\mathrm{Sc}}\end{pmatrix}+l_{\mathrm{R}}\begin{pmatrix}i_{\mathrm{Ra}}\\ i_{\mathrm{Rb}}\\ i_{\mathrm{Rc}}\end{pmatrix} \tag{3.10}$$

With the stator and rotor inductance:

$$l_{\mathrm{S}}=l_{\sigma\mathrm{S}}+l_{\mathrm{M}} \tag{3.11}$$

$$l_{\mathrm{R}}=l_{\sigma\mathrm{R}}+l_{\mathrm{M}} \tag{3.12}$$

The three-phase equations can be described by a space vector, which consists of two orthogonal components, without zero sequence components since the neutral point of the DFIG is usually not connected and consequently no zero system occurs.

Using Clarke transformation, the three-phase equations, Eq. (3.7) – (3.10) are transformed into space vectors in an arbitrary reference system (denoted by superscript $\angle$) and the following system of equations are obtained.

Voltage equations:

$$\underline{u}_{\mathrm{S}}^{\angle}=-r_{\mathrm{S}}\underline{i}_{\mathrm{S}}^{\angle}-\mathrm{j}\omega_{\angle}\underline{\psi}_{\mathrm{S}}^{\angle}-\frac{\mathrm{d}\underline{\psi}_{\mathrm{S}}^{\angle}}{\mathrm{d}t} \tag{3.13}$$

$$\underline{u}_{\mathrm{R}}^{\angle}=-r_{\mathrm{R}}\underline{i}_{\mathrm{R}}^{\angle}-\mathrm{j}\left(\omega_{\angle}-\omega_{\mathrm{R}}\right)\underline{\psi}_{\mathrm{R}}^{\angle}-\frac{\mathrm{d}\underline{\psi}_{\mathrm{R}}^{\angle}}{\mathrm{d}t} \tag{3.14}$$

Flux equations:

$$\underline{\psi}_{\mathrm{S}}^{\angle}=l_{\mathrm{S}}\underline{i}_{\mathrm{S}}^{\angle}+l_{\mathrm{M}}\underline{i}_{\mathrm{R}}^{\angle} \tag{3.15}$$

$$\underline{\psi}_{\mathrm{R}}^{\angle}=l_{\mathrm{M}}\underline{i}_{\mathrm{S}}^{\angle}+l_{\mathrm{R}}\underline{i}_{\mathrm{R}}^{\angle} \tag{3.16}$$

After some algebraic manipulation, the complex state equation for the stator and rotor circuits can be expressed as:

$$\frac{\mathrm{d}\underline{\psi}_{\mathrm{S}}^{\angle}}{\mathrm{d}t}=\left(-\frac{r_{\mathrm{S}}}{\sigma l_{\mathrm{S}}}-\mathrm{j}\omega_{\angle}\right)\underline{\psi}_{\mathrm{S}}^{\angle}+\frac{l_{\mathrm{M}}r_{\mathrm{S}}}{\sigma l_{\mathrm{S}}l_{\mathrm{R}}}\underline{\psi}_{\mathrm{R}}^{\angle}-\underline{u}_{\mathrm{S}}^{\angle} \tag{3.17}$$

$$\frac{\mathrm{d}\underline{\psi}_{\mathrm{R}}^{\angle}}{\mathrm{d}t}=\left(-\frac{r_{\mathrm{R}}}{\sigma l_{\mathrm{R}}}-\mathrm{j}\left(\omega_{\angle}-\omega_{\mathrm{R}}\right)\right)\underline{\psi}_{\mathrm{R}}^{\angle}+\frac{l_{\mathrm{M}}r_{\mathrm{R}}}{\sigma l_{\mathrm{S}}l_{\mathrm{R}}}\underline{\psi}_{\mathrm{S}}^{\angle}-\underline{u}_{\mathrm{R}}^{\angle} \tag{3.18}$$

Where the leakage factor is given as:

$$\sigma=1-\frac{l_{\mathrm{M}}^{2}}{l_{\mathrm{S}}l_{\mathrm{R}}} \tag{3.19}$$

The stator and rotor currents can be expressed as:

$$\underline{i}_{\mathrm{S}}^{\angle} = \frac{l_{\mathrm{R}}\underline{\psi}_{\mathrm{S}}^{\angle} - l_{\mathrm{M}}\underline{\psi}_{\mathrm{R}}^{\angle}}{\sigma l_{\mathrm{S}} l_{\mathrm{R}}} \tag{3.20}$$

$$\underline{i}_{\mathrm{R}}^{\angle} = \frac{l_{\mathrm{S}}\underline{\psi}_{\mathrm{R}}^{\angle} - l_{\mathrm{M}}\underline{\psi}_{\mathrm{S}}^{\angle}}{\sigma l_{\mathrm{S}} l_{\mathrm{R}}} \tag{3.21}$$

The electromagnetic torque is given as:

$$t_{\mathrm{el}} = \mathrm{Im}\left\{\underline{\psi}_{\mathrm{S}} \cdot \underline{i}_{\mathrm{S}}^{*}\right\} = \mathrm{Im}\left\{\underline{\psi}_{\mathrm{R}} \cdot \underline{i}_{\mathrm{R}}^{*}\right\} \tag{3.22}$$

All these equations form the FOM that can be used for instantaneous value based dynamic time domain simulations. State variables are the stator and rotor flux components as well as the rotor speed. The stator voltage is assumed to be constant or interpreted as an independent input variable. This allows using the FOM for single machine infinite bus investigations.

3.3.2 Steady state model

The steady-state model of the DFIG is mainly required for the calculation of the initial conditions for the initialization of the state variables in the dynamic models. Additionally, it is the foundation of the derivation of the standard rotor current control structure, which will be described in chapter 4. Based on this model, the steady-state performance of the machine will be reviewed briefly with the objective of identifying the range of control options and the operational capabilities of the machine.

Neglecting the derivative terms in Eq. (3.13) and Eq. (3.14), and regarding the equations in synchronously rotating grid coordinates:

$$\underline{u}_{\mathrm{S}} = -r_{\mathrm{S}}\underline{i}_{\mathrm{S}} - \mathrm{j}\omega_{\mathrm{S}}\underline{\psi}_{\mathrm{S}} \tag{3.23}$$

$$\underline{u}_{\mathrm{R}} = -r_{\mathrm{R}}\underline{i}_{\mathrm{R}} - \mathrm{j}\left(\omega_{\mathrm{S}} - \omega_{\mathrm{R}}\right)\underline{\psi}_{\mathrm{R}} \tag{3.24}$$

Eliminating the flux linkages using Eq. (3.15) and Eq. (3.16), the following equations are obtained:

$$\underline{u}_{\mathrm{S}} = -r_{\mathrm{S}}\underline{i}_{\mathrm{S}} - \mathrm{j}\omega_{\mathrm{S}}\left(l_{\mathrm{S}}\underline{i}_{\mathrm{S}} + l_{\mathrm{M}}\underline{i}_{\mathrm{R}}\right) = -r_{\mathrm{S}}\underline{i}_{\mathrm{S}} - \mathrm{j}x_{\mathrm{S}}\underline{i}_{\mathrm{S}} - \mathrm{j}x_{\mathrm{M}}\underline{i}_{\mathrm{R}} \tag{3.25}$$

$$\frac{\underline{u}_{\mathrm{R}}}{s_{\mathrm{gen}}} = -\frac{r_{\mathrm{R}}}{s_{\mathrm{gen}}}\underline{i}_{\mathrm{R}} - \mathrm{j}\omega_{\mathrm{S}}\left(l_{\mathrm{M}}\underline{i}_{\mathrm{S}} + l_{\mathrm{R}}\underline{i}_{\mathrm{R}}\right) = -\frac{r_{\mathrm{R}}}{s_{\mathrm{gen}}}\underline{i}_{\mathrm{R}} - \mathrm{j}x_{\mathrm{M}}\underline{i}_{\mathrm{S}} - \mathrm{j}x_{\mathrm{R}}\underline{i}_{\mathrm{R}} \tag{3.26}$$

where the slip, $s_{\mathrm{gen}} = \dfrac{\omega_{\mathrm{S}} - \omega_{\mathrm{R}}}{\omega_{\mathrm{S}}}$.

Eq. (3.25) and Eq. (3.26) can also be illustrated using the equivalent circuit given in Figure 3-7.

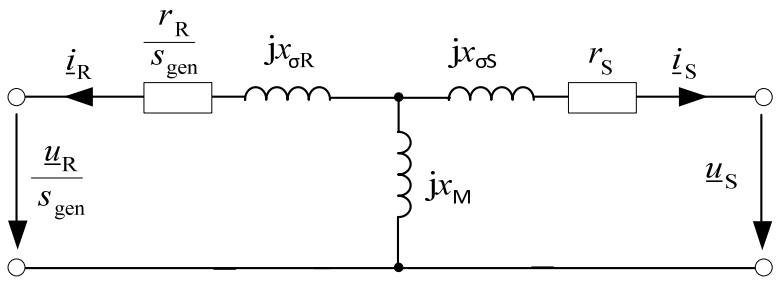


Figure 3-7: Equivalent circuit of doubly fed induction machine in steady-state

3.4 Power converter

The power converter of DFIG based WT can be designed as different structure such as:

- The static Kramer drive (Figure 3-8a) [32], [33]
- The VCRS system (Figure 3-8b) [32], [34]
- The back-to-back system (Figure 3-8c)

The static Kramer drive and the VCRS system are uni-directional type with regard to power flow and only able to generate power when operating above synchronous speed or below synchronous speed. The back-to-back system is a bi-directional power converter consisting of two voltage source converters coupled in a back-to-back fashion. It is able to generate power both above and below synchronous speed which allows this system to track the optimum tip speed in a larger speed range than the static Kramer drive and the VCRS system. Further, the back-to-back system is able to provide reactive power control [35], [36] and harmonic compensation [37] both by the line side converter (LSC) and by the machine side converter (MSC). Thus, it is more preferable than the other two systems and implemented in this study.

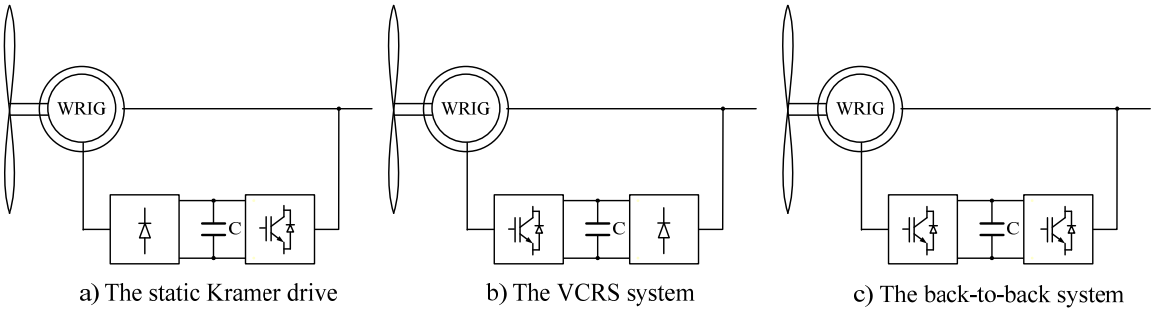


Figure 3-8: Different structure of power converter in a DFIG based WT

In wind turbines applications, voltage level of the back-to-back converter can be distinguished between low voltage (400-690 V) and medium voltage converters (3.0-6.6 kV). In medium voltage converters, the three-level NPC converter is the most common topology and practical in full-scale converter systems. In the DFIG based WT, the low voltage converters which is

normally using two-level converter is widely been used since many years. In this study, performance comparison between both two-level and three-level converters used in the DFIG system will be investigated. In order to have a good comparison, thus the DFIG system is designed with the same power rating (2 MW) and having the same voltage level (690 V) for both converter topologies. In this section, both converter topologies and their switching devices that will be used in the DFIG model are explained.

3.4.1 Switching devices

There is a large variety of power semiconductors that function as switching devices in a converter such as metal oxide semiconductor field effect transistors (MOSFETs), insulated gate bipolar transistors (IGBTs), gate turn-off thyristors (GTOs), and integrated gate commutated thyristors (IGCTs). Figure 3-9 shows maximum current and voltage values for controllable power semiconductors on the market today [38], [39]. While Figure 3-10 shows common switching frequency ranges for various power semiconductors [39].

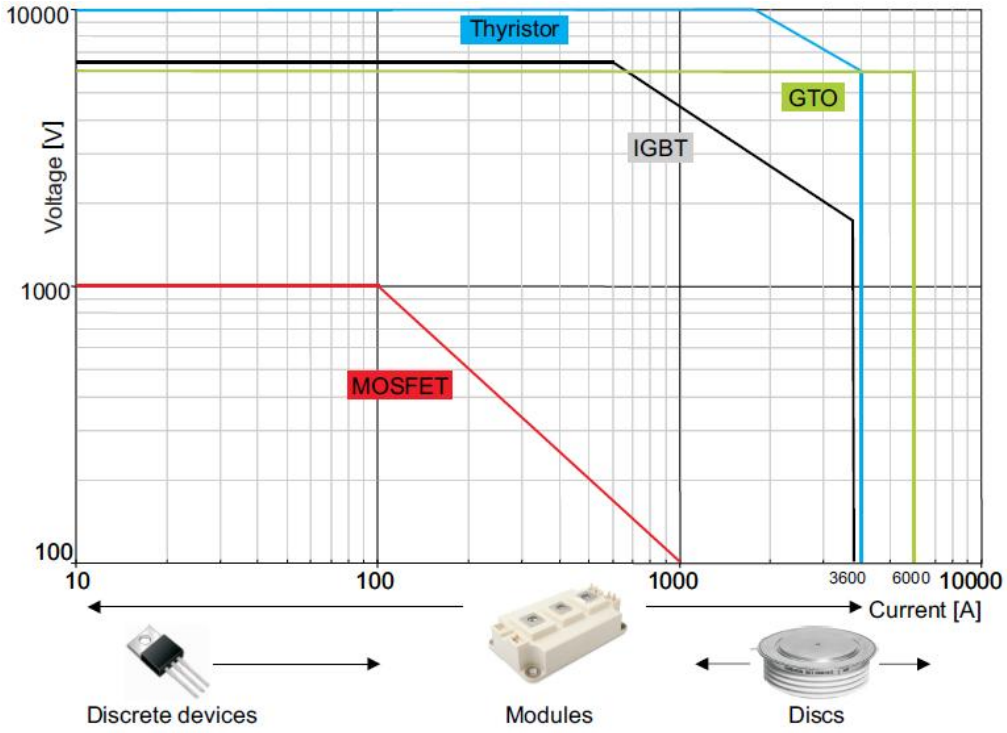


Figure 3-9: Maximum current and voltage values for controllable power semiconductors on the market [39]

IGBTs were introduced on the market in 1988. Nowadays, they have become especially important for the “mass markets” of mains powered systems and equipment with a medium or

high switching performance. With recent advances in semiconductor technology, IGBTs of a rating up till 6.5 kV with DC current ratings up to 3.6 kA are commercially available today.
The selection of semiconductor devices is always a compromise between controllability and dynamic requirements of the generator system on the one hand, and moderate losses on the other hand. In the DFIG based WT, the IGBTs are clearly the dominating semiconductor devices used in various converter topologies. They offer switch-on and switch-off capability and thus provide full controllability at a wide range of switching frequencies. As shown in Figure 3-10, the upper limit of the frequency range is determined by the semiconductor switching losses and is approx. at 5 kHz for power applications. The lower limit is due to the increased harmonic generation at low switching frequencies and the corresponding increased filter size and is at approx. 500 Hz. Other switching devices like GTOs or IGCTs also offer switch-off capability, but work at lower switching frequencies. Therefore, in this study, the IGBTs are selected as the switching devices.

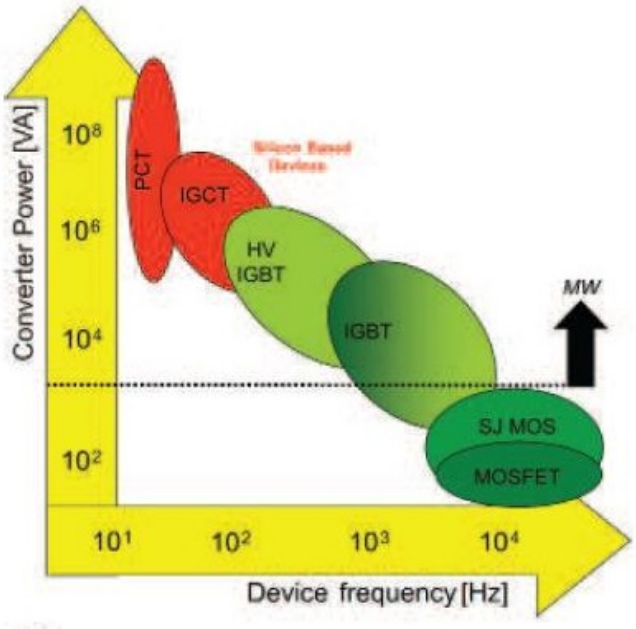


Figure 3-10: Common switching frequency ranges for various power semiconductors [39]

A typical module comprising of an IGBT with an anti-parallel diode is shown in Figure 3-11. In DFIG applications, since the valves experience the entire DC voltage, the rating of the components required is high. The diodes in the module must have a rating comparable to that of the IGBT, as in case of short circuit faults or during overload faults they will experience a large inrush current.
In order to avoid such large inrush current which could cause a negative impact on the aging, lifetime, and reliability of the IGBT, the IGBT must be blocked when the current reach its

limit. This limit is called over-current protection (OCP). Normally, in real applications the IGBT must be blocked at about 2.5 of rated current to prevent over-voltage during switching.

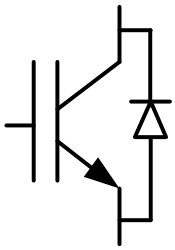


Figure 3-11: Module comprising of an IGBT and its freewheeling diode

3.4.2 Two-level converter topology

Since the appearance of power semiconductors with intrinsic gate-turn-off capability, the two-level voltage source converter has been the most widely used power converter for three phase motor drive applications. Probably, due to the maturity obtained in the drives industry during more than a decade, the two-level voltage source converter was widely adopted by the wind turbine industry for use in large scale wind turbines in the late nineties.

Since the back-to-back two-level voltage source converter seems to be the preferred converter topology in wind turbine applications, the purpose of this chapter is to establish a foundation to compare and evaluate the back-to-back two-level voltage source converter against other converter topologies applicable for the DFIG based WT system.

The two-level converter topology is shown in Figure 3-12. It consists of three legs, one for each phase. Each converter leg consists of two IGBTs and two freewheeling diodes in parallel with each IGBT. The output of each leg of the converter depends only on the DC-link voltage u_{DC} and the switch state. The output voltage is independent of the output load current since one of the two IGBTs or freewheeling diodes in a leg is always on at any instant. Therefore, the converter output voltage is independent of the direction of the load current. It is capable of producing two output voltage levels namely $+u_{DC}$ and $-u_{DC}$. The crude AC waveform obtained has a high harmonic content.

Some advantages of a two-level converter include:

- Simple circuitry.
- Low cost and less component count compared to multi/level converter.

Although the two-level converter topology offers some advantages there are certain limitations that also need to be considered, such as:

- The valves experience a very high voltage and hence they need to be rated with high blocking voltage capabilities.

- The crude AC waveform obtained contains a lot of unwanted harmonics. The switching frequency can be increased to push the harmonics to higher frequencies using PWM, but this leads to higher switching losses in the converter.

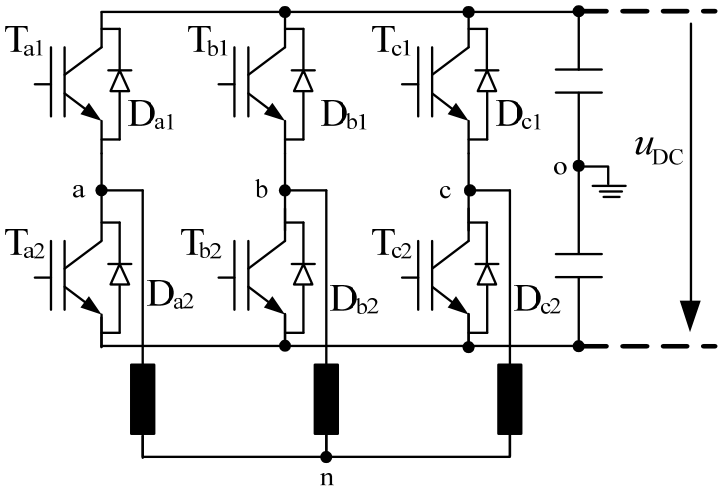


Figure 3-12: Two-level converter topology

3.4.3 Three-level NPC converter topology

With increase in power ratings, more number of switching devices needs to be added in series. Simultaneous switching of a series chain of IGBT's becomes complex, as there may occur a delayed switching owing to heating of the devices. Hence, the concept of multi-level converters was introduced. It gave flexibility in switching the devices independently and at lower frequencies. Different topologies have been developed and a lot of research is being done in improving the overall performance of the converter to provide an output of high quality.

The most common multi-level converter topologies are [40]:

- Three-level Neutral Point Clamped (NPC)
- Three-level Flying Capacitor (FC)
- Three-level active NPC
- Cascade H-Bridge
- Modular Multi-level

In wind turbine generation systems, the three-level NPC converter is the most common topology. It is mostly used in medium voltage converter for full-scale wind turbine system. However, with improved performances as well as reduced cost of the converter, the usage of

this topology could be broadening for other wind turbine application such as the DFIG based WT.

The topology of the three-level NPC (diode-clamped) converter is presented in Figure 3-13. It contains 12 IGBTs having anti-parallel diodes and 6 neutral point clamp (NPC) diodes. The IGBTs T_{x1} and T_{x4} are named 'outer IGBTs' and the remaining IGBTs T_{x2} and T_{x3} are designated 'inner IGBTs'. The group of NPC diodes is referred to as P_{x1} and P_{x2}. This converter has a zero DC voltage centre point '0', which is switchable to the phase outputs, thereby creating the possibility of switching each converter phase leg to one of three voltage levels. This provides another level in the modulation of the output voltage and allows the reduction of the switching frequency or the filter size. Consequently, this leads to a reduction of converter losses. Other benefit of this configuration is that, while there are twice as many switches as in the two-level converter, each of the switches must block only one-half of the DC- link voltage '$u_{DC}/2$' [41]. However, apart from that fact, the behavior of this converter is very similar to that of the two-level topology.

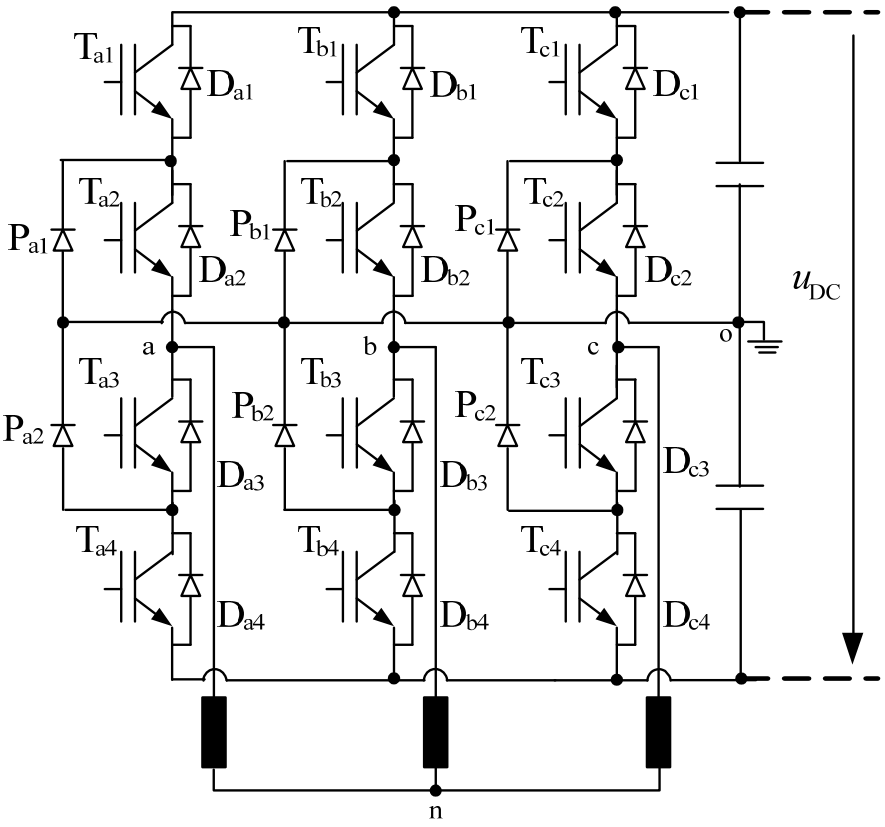


Figure 3-13: Three-level NPC converter topology

Some additional features include:

- High voltage rating of blocking diodes is required.

- Unequal device rating leading to different current ratings of devices.
- The more level in the modulation of output voltage produce better waveform quality. Thus, the output waveform has a lower harmonics distortion level compared to the two-level converter.
- Suffers from capacitor voltage unbalance problem.

3.5 Transformer

The nominal output voltages of wind turbine generators are in the range of 400 V-6.6 kV. For the purpose of grid connection at a common voltage level a machine transformer is required to step-up the voltage to the grid level (typically 10 kV or 20 kV onshore, 30 kV offshore). The wind turbines with a stator voltage of 400 V or 690 V use a two-winding transformer with a vector group of Dyn5 or Dyn11. DFIG based WTs with higher stator voltages have different voltage levels at the generator and the line side converter and require a three-winding transformer. In the most cases, it is connected with a vector group of Dyn5yn5.

3.6 DC circuit

The DC circuit consists of DC capacitor and DC-link chopper with its braking resistor. Figure 3-14 shows the electrical configuration of the DC circuit.

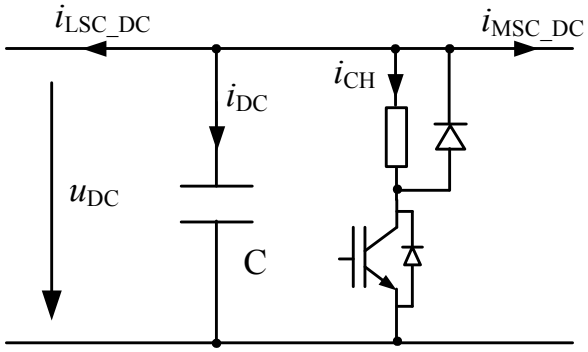


Figure 3-14: Model of DC circuit

If the converter losses are neglected, the differential equation for the DC voltage is given as:

$$\frac{\mathrm{d}u_{\mathrm{DC}}}{\mathrm{d}t} = \frac{1}{C}\cdot i_{\mathrm{DC}} = \frac{1}{C}\left(-i_{\mathrm{LSC\_DC}} - i_{\mathrm{MSC\_DC}} - i_{\mathrm{CH}}\right) = \frac{1}{C\cdot u_{\mathrm{DC}}}\left(-p_{\mathrm{LSC}} - p_{\mathrm{MSC}} - p_{\mathrm{CH}}\right) \quad (3.27)$$

Where the chopper active power is given as:

$$p_{\mathrm{CH}} = \begin{cases} 0 & \text{, if chopper off} \\ \dfrac{u_{\mathrm{DC}}^2}{r_{\mathrm{CH}}} & \text{, if chopper on} \end{cases} \quad (3.28)$$

4 Control of DFIG based Wind Turbines

In this chapter, mechanical control and converter control of the DFIG based WT will be presented. The mechanical control is including generator speed control and rotor blade pitch control which have their different control tasks. In general, the variable speed WTs may have two different control goals, depending on the wind speed. In low to moderate wind speeds, the control goal is to maintain a constant optimum tip speed ratio for maximum energy conversion. In high wind speeds, the control goal is to keep the rated output power.

The converter control consists of machine side converter (MSC) control and line side converter (LSC) control. The MSC and LSC are controlled in a d-q reference frame. The LSC maintains the DC voltage and provides reactive current support for optimization of reactive power sharing between MSC and LSC during steady state and grid faults. The MSC controls active and reactive power of the WT and follows a tracking characteristic to adjust the generator speed for optimal power generation depending on wind speed. Figure 4-1 shows the block diagram of the overall control schemes of the DFIG based WT.

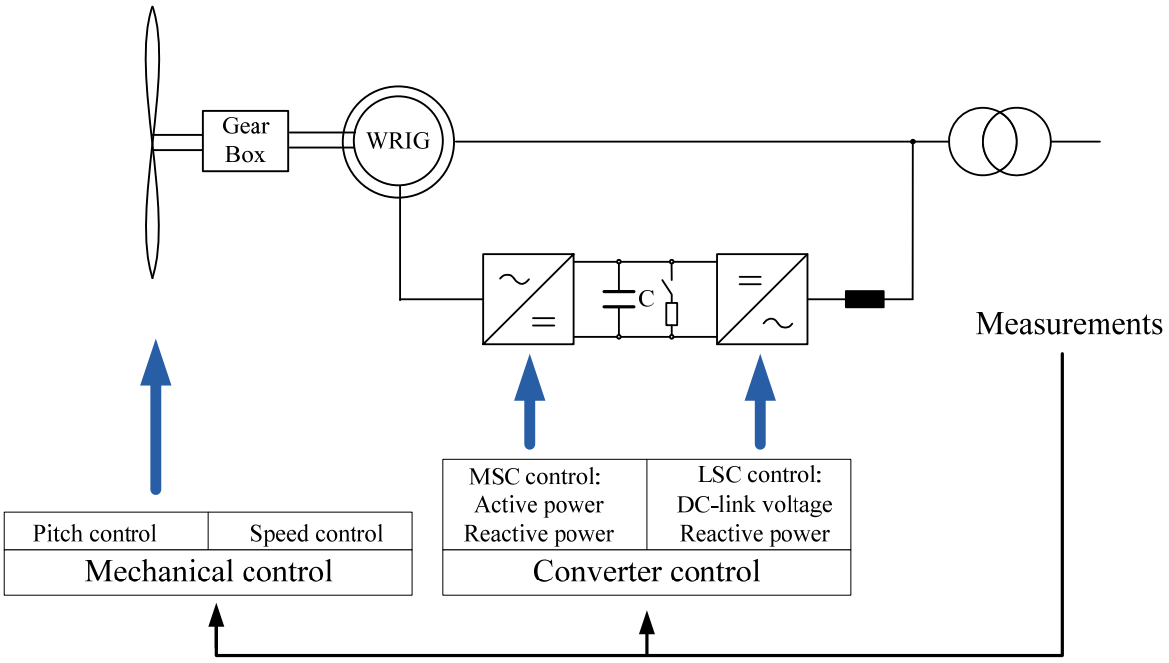


Figure 4-1: Overall control schemes of DFIG based wind turbine

4.1 Mechanical control

At high wind speeds or above nominal wind speed, it is necessary to limit the input power to the turbine, or aerodynamic power control. There are three major methods of aerodynamic

power control: stall, pitch and active stall control [42]. The three methods are described as follows:

- Stall control implies that the blades are designed to stall above nominal wind speeds and no pitch mechanism is thus required.
- Pitch control is the most common method of controlling the aerodynamic power generated by a turbine rotor for newer larger wind turbines. Almost all variable speed wind turbines use pitch control. Below nominal wind speed the turbine should produce as much power as possible, using a pitch angle that maximizes the energy capture. Above nominal wind speed the pitch angle is controlled in such a way that the aerodynamic power is kept at its nominal value. In order to limit the aerodynamic power, at above nominal wind speeds, the pitch angle is controlled to decrease the angle of attack.
- Active stall is also working with the stall effect to increase angle of attack towards stall in order to limit the aerodynamic power. This method can be used to fine-tune the power level at high wind speeds for fixed speed turbines.

In modern multi-MW WT system, the aerodynamic pitch control is normally combined with the speed control to achieve their control goals. Both control schemes are presented in the next section.

4.1.1 Pitch control

As mentioned previously, the main task of the aerodynamic control is to limit WT mechanical power (torque) at high wind speeds to the nominal value of the WT by moving the rotor blades out of the wind.

In order to turn the rotor blades (pitch angle) out of the wind, pitch actuators are used, so that the turbine output power which is modeled based on the cp-curves of the WT and the basic equation of wind power conversion (Eq. 3.1) can be limited. The reference pitch angle is determined by a PI controller which provides the quasi-stationary limitation of the rotor speed to the given set-point. This controller is only active if the generator speed exceeds its nominal value. Figure 4-2 shows the structure of a simple pitch controller.

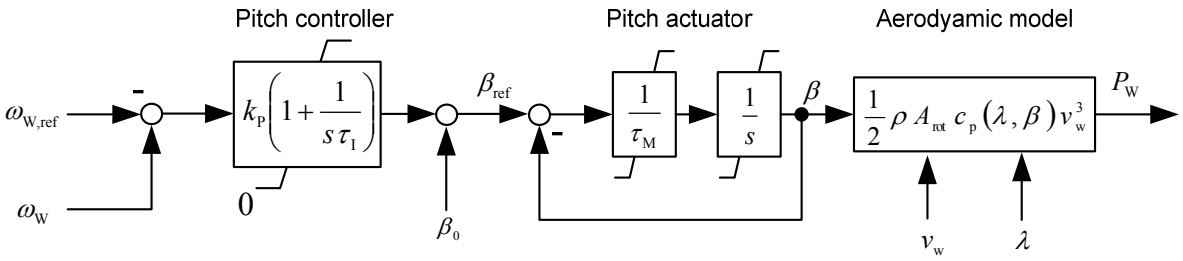


Figure 4-2: Structure of pitch control and aerodynamic model of a DFIG based WT

4.1.2 Speed control

The speed control is working to maximize the power output of the wind turbine across a wide range of wind speeds by adjusting the turbine rotational speed according to the optimal tracking characteristic, which considers the rotor blade characteristics. Figure 4-3 shows the typical power tracking curve of a DFIG based WT as a function of speed range.

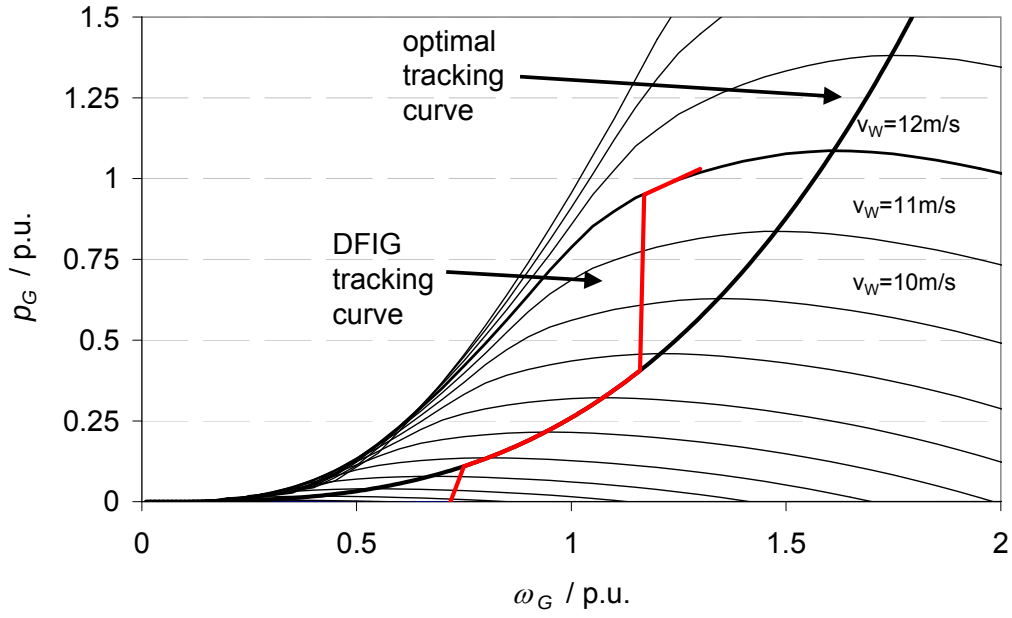


Figure 4-3: Typical power tracking curve of a DFIG based WT

The speed control used in this simulation is based on PI controller. The PI controller adjusts the generator speed by following the reference speed which is determined by a lookup table. This lookup table stores a fixed relationship between measured electrical power and reference speed. Figure 4-4 shows the structure of a simple speed controller.

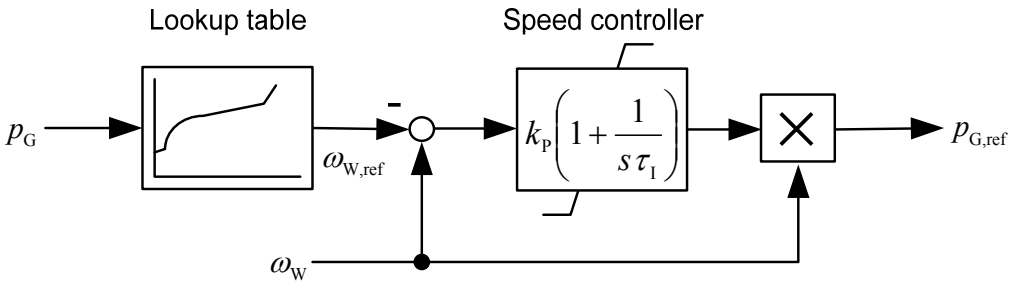


Figure 4-4: Structure of speed control of a DFIG based WT

4.2 Power converter control

The converter control is the most important feature in controlling the DFIG based WT. Different control methods for the converter control has been published in the literature. Vector control technique, which has been well developed for DFIG using back-to-back converters [43]-[46], is applied in this study. The vector control scheme is based on Park's transformation provides two orthogonal channels d and q to each converter thereby allowing decoupled control of active and reactive power.

The objective of the vector control scheme for the LSC is to keep the DC-link voltage constant regardless of the magnitude and direction of the rotor power. It also is responsible for controlling reactive power flow into the grid by adjusting reactive power reference during steady state and grid faults. The vector control scheme for the MSC ensures decoupling control of stator-side active and reactive power drawn from the grid. The reference value of the stator-side active power is obtained from the output of speed controller. It also provides a generator with a wide speed range operation.

4.2.1 Line side converter control

A vector control approach is used with a reference frame oriented along the grid voltage vector position, enabling independent control of the active and reactive power flowing between the grid and the LSC. Figure 4-5 shows the circuit diagram of the LSC in a two-level topology.

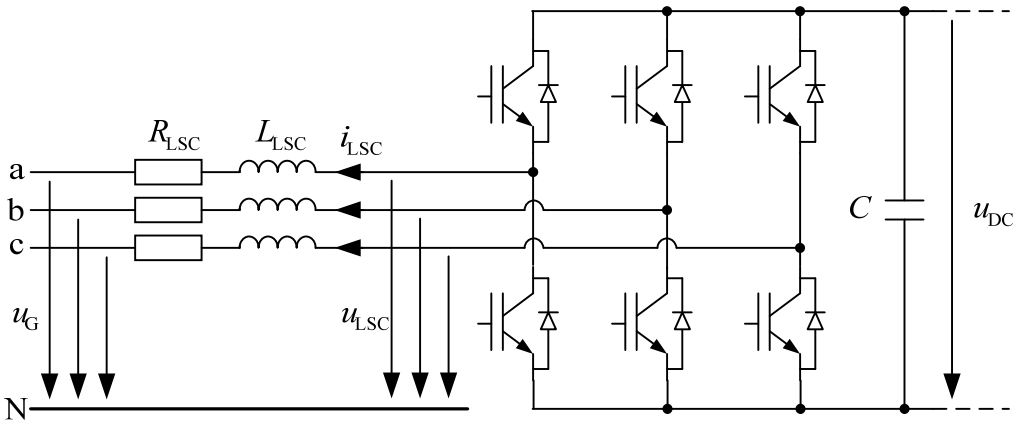


Figure 4-5: LSC circuit diagram

From the LSC circuit, with the voltage drop across the grid reactor considered, the resulting three-phase equations are [47]:

$$\begin{pmatrix} u_{\mathrm{G,a}} \\ u_{\mathrm{G,b}} \\ u_{\mathrm{G,c}} \end{pmatrix} = \begin{pmatrix} u_{\mathrm{LSC,a}} \\ u_{\mathrm{LSC,b}} \\ u_{\mathrm{LSC,c}} \end{pmatrix} - R_{LSC} \cdot \begin{pmatrix} i_{\mathrm{LSC,a}} \\ i_{\mathrm{LSC,b}} \\ i_{\mathrm{LSC,c}} \end{pmatrix} - L_{LSC} \cdot \frac{\mathrm{d}}{\mathrm{d}t} \begin{pmatrix} i_{\mathrm{LSC,a}} \\ i_{\mathrm{LSC,b}} \\ i_{\mathrm{LSC,c}} \end{pmatrix} \tag{4.1}$$

Using the Park's transformation matrix, the corresponding equations in the d-q reference frame rotating, which aligned to the positive sequence terminal voltage (denoted by $\angle u_{\mathrm{G}}$) are expressed as:

$$u_{\mathrm{LSC,d}}^{\angle \mathrm{u_G}} = u_{\mathrm{G,d}}^{\angle \mathrm{u_G}} + r_{\mathrm{LSC}} \cdot i_{\mathrm{LSC,d}}^{\angle \mathrm{u_G}} + l_{\mathrm{LSC}} \frac{\mathrm{d}i_{\mathrm{LSC,d}}^{\angle \mathrm{u_G}}}{\mathrm{d}t} - \omega_0 l_{\mathrm{LSC}} \cdot i_{\mathrm{LSC,q}}^{\angle \mathrm{u_G}} \tag{4.2}$$

$$u_{\mathrm{LSC,q}}^{\angle \mathrm{u_G}} = u_{\mathrm{G,q}}^{\angle \mathrm{u_G}} + r_{\mathrm{LSC}} \cdot i_{\mathrm{LSC,q}}^{\angle \mathrm{u_G}} + l_{\mathrm{LSC}} \frac{\mathrm{d}i_{\mathrm{LSC,q}}^{\angle \mathrm{u_G}}}{\mathrm{d}t} + \omega_0 l_{\mathrm{LSC}} \cdot i_{\mathrm{LSC,d}}^{\angle \mathrm{u_G}} \tag{4.3}$$

It has to take note that in this rotating voltage reference frame, $u_{\mathrm{G,q}}^{\angle \mathrm{u_G}} = 0$ and $u_{\mathrm{G,d}}^{\angle \mathrm{u_G}} = \left| u_{\mathrm{G,d}}^{\angle \mathrm{u_G}} \right|$.

The equations for feed-forward current control can be derived considering steady-state operation and neglecting the derivative terms.

In order to account for uncertainty parameters, PI controllers for the d-axis and q-axis are included with the outputs:

$$u_{\mathrm{LSC,d\_PI}}^{\angle \mathrm{u_G}} = k_{\mathrm{P}} \left(1 + \frac{1}{s\tau_{\mathrm{I}}} \right) \left(i_{\mathrm{LSC,d\_ref}}^{\angle \mathrm{u_G}} - i_{\mathrm{LSC,d}}^{\angle \mathrm{u_G}} \right) \tag{4.4}$$

$$u_{\mathrm{LSC,q\_PI}}^{\angle \mathrm{u_G}} = k_{\mathrm{P}} \left(1 + \frac{1}{s\tau_{\mathrm{I}}} \right) \left(i_{\mathrm{LSC,q\_ref}}^{\angle \mathrm{u_G}} - i_{\mathrm{LSC,q}}^{\angle \mathrm{u_G}} \right) \tag{4.5}$$

The resulting controller equations are:

$$u_{\mathrm{LSC,d\_ref}}^{\angle u_G} = u_{\mathrm{LSC,d\_PI}}^{\angle u_G} + u_{\mathrm{G,d}}^{\angle u_G} + r_{\mathrm{LSC}} \cdot i_{\mathrm{LSC,d\_ref}}^{\angle u_G} - \omega_0 l_{\mathrm{LSC}} \cdot i_{\mathrm{LSC,q\_ref}}^{\angle u_G} \tag{4.6}$$

$$u_{\mathrm{LSC,q\_ref}}^{\angle u_G} = u_{\mathrm{LSC,q\_PI}}^{\angle u_G} + u_{\mathrm{G,q}}^{\angle u_G} + r_{\mathrm{LSC}} \cdot i_{\mathrm{LSC,q\_ref}}^{\angle u_G} + \omega_0 l_{\mathrm{LSC}} \cdot i_{\mathrm{LSC,d\_ref}}^{\angle u_G} \tag{4.7}$$

From Eq. (4.6) and (4.7), the inner current control loops for the LSC can be depicted as in Figure 4-6. The cross-coupling terms of the voltage across the grid reactor and the grid voltage are fed forward so that the PI controllers only have to provide a fast transition of the current to the respective set-values. The output of the inner current control will be transformed into three-phase voltages using inverse Park's transformation, then passing to the converter driver to generate pulse width modulation (PWM) switching instants for the IGBTs in the LSC.

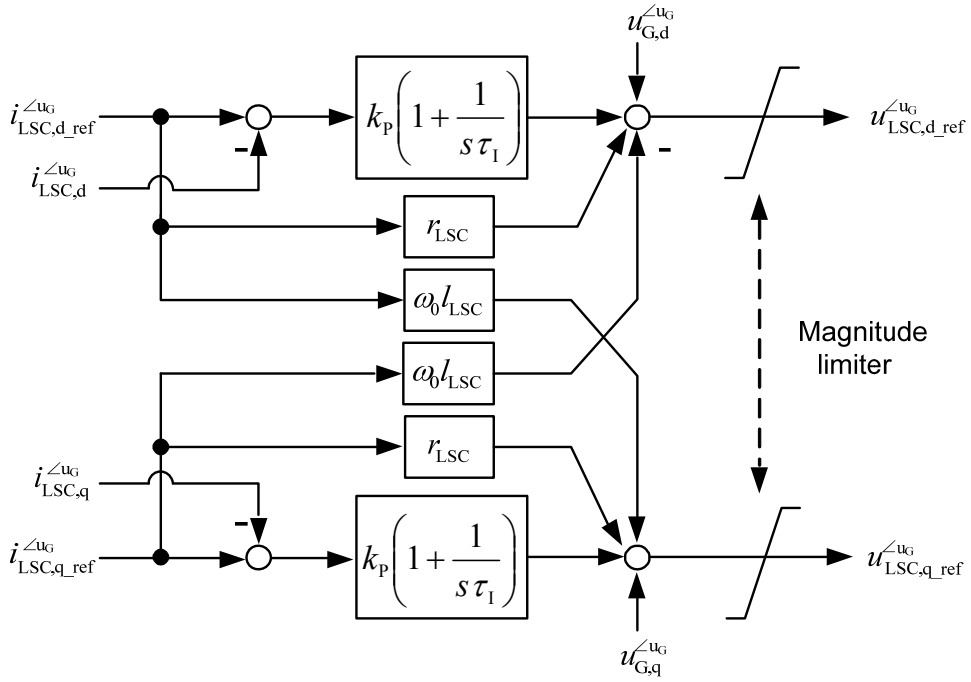


Figure 4-6: Inner current control for LSC with feed-forward terms

The input reference values of the inner current control, $i_{\mathrm{LSC,d\_ref}}^{\angle u_G}$ and $i_{\mathrm{LSC,q\_ref}}^{\angle u_G}$ are calculated from outer control loop which is including DC-link voltage control in the d-component and reactive power control in the q-component, as shown in Figure 4-7. The DC-link voltage control uses a PI controller for adjusting the measured DC-link voltage following the nominal value. The performance of the DC voltage controller is enhanced by the feed-forward control of the active current of the MSC, which is calculated via the MSC active power and the line voltage. The magnitude of the current set value is limited according to the converter rating with a priority for the active current to ensure correct DC-link voltage control.

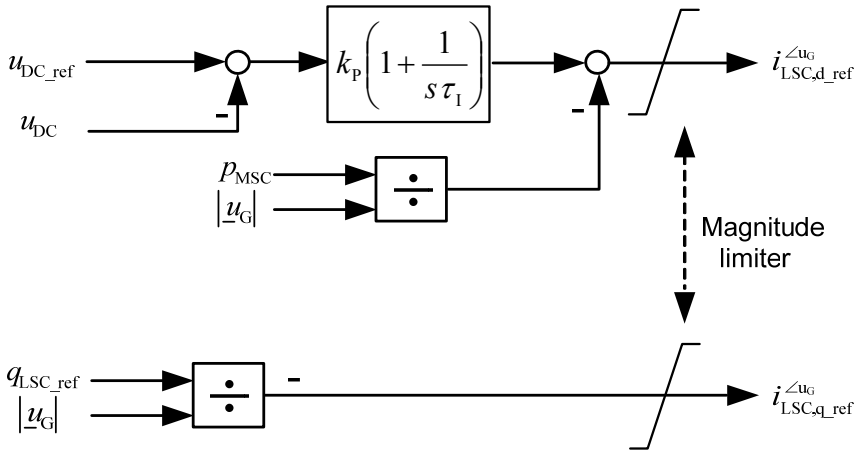


Figure 4-7: Outer LSC control loop with DC-link voltage and reactive power control

4.2.2 Machine side converter control

The vector control approach is also used in the MSC control with a reference frame oriented along the stator voltage vector position. This control approach can be realized with PI controllers for both d-axis and q-axis with the use of feed-forward decoupling terms to improve the dynamic controller behavior.

The fundamental system of equations for the DFIG in the synchronous reference frame linked to the stator voltage that has been presented in chapter 3 as Eq. (3.13) and Eq. (3.14). Considering steady-state operation and neglecting the derivative terms and stator resistance, the resulting equations, which aligned to the positive sequence stator voltage vector (denoted by $\angle u_S$) are expressed as [47]:

$$\underline{u}_S^{\angle u_S} = -\mathrm{j}x_S \underline{i}_S^{\angle u_S} - \mathrm{j}x_M \underline{i}_R^{\angle u_S} \tag{4.8}$$

$$\underline{u}_R^{\angle u_S} = -r_R \underline{i}_R^{\angle u_S} - s_{gen}(\mathrm{j}x_M \underline{i}_S^{\angle u_S} - \mathrm{j}x_R \underline{i}_R^{\angle u_S}) \tag{4.9}$$

From Eq. (4.8),

$$\underline{i}_S^{\angle u_S} = \frac{\underline{u}_S^{\angle u_S} + \mathrm{j}x_M \underline{i}_R^{\angle u_S}}{-\mathrm{j}x_S} \tag{4.10}$$

Inserting Eq. (4.10) into Eq. (4.9) results the feed-forward current control as:

$$\underline{u}_R^{\angle u_S} = s_{gen}\frac{x_M}{x_S}\cdot\underline{u}_S - r_R \underline{i}_R^{\angle u_S} - \mathrm{j}s_{gen}x_R \underline{i}_R^{\angle u_S}\sigma \tag{4.11}$$

In order to account for uncertainty parameters, PI controllers for the d-axis and q-axis are included with the outputs:

$$u_{\mathrm{R,d\_PI}}^{\angle u_\mathrm{S}} = k_\mathrm{P}\left(1+\frac{1}{s\tau_\mathrm{I}}\right)\left(i_{\mathrm{R,d\_ref}}^{\angle u_\mathrm{S}} - i_{\mathrm{R,d}}^{\angle u_\mathrm{S}}\right) \tag{4.12}$$

$$u_{\mathrm{R,q\_PI}}^{\angle u_\mathrm{S}} = k_\mathrm{P}\left(1+\frac{1}{s\tau_\mathrm{I}}\right)\left(i_{\mathrm{R,q\_ref}}^{\angle u_\mathrm{S}} - i_{\mathrm{R,q}}^{\angle u_\mathrm{S}}\right) \tag{4.13}$$

Considering the stator voltage orientation ($u_{\mathrm{S,d}}^{\angle u_\mathrm{S}} = u_\mathrm{S}, u_{\mathrm{S,q}}^{\angle u_\mathrm{S}} = 0$), the resulting controller equations are:

$$u_{\mathrm{R,d\_ref}}^{\angle u_\mathrm{S}} = u_{\mathrm{R,d\_PI}}^{\angle u_\mathrm{S}} + s_\mathrm{gen}\frac{x_\mathrm{M}}{x_\mathrm{S}}\cdot u_\mathrm{S} - r_\mathrm{R}\cdot i_{\mathrm{R,d\_ref}}^{\angle u_\mathrm{S}} + \sigma s_\mathrm{gen} x_\mathrm{R} i_{\mathrm{R,q\_ref}}^{\angle u_\mathrm{S}} \tag{4.14}$$

$$u_{\mathrm{R,q\_ref}}^{\angle u_\mathrm{S}} = u_{\mathrm{R,q\_PI}}^{\angle u_\mathrm{S}} - r_\mathrm{R} i_{\mathrm{R,q\_ref}}^{\angle u_\mathrm{S}} - \sigma s_\mathrm{gen} x_\mathrm{R} i_{\mathrm{R,d\_ref}}^{\angle u_\mathrm{S}} \tag{4.15}$$

From Eq. (4.14) and (4.15), the inner current control loops for the MSC can be depicted as in Figure 4-8. By forwarding this voltage the parallel PI current controllers only have to put into effect the transition of the rotor currents to the set values. The output of the inner current control will be transformed into three-phase voltages using inverse Park's transformation, then passing to the converter driver to generate PWM switching instants for the IGBTs in the MSC.

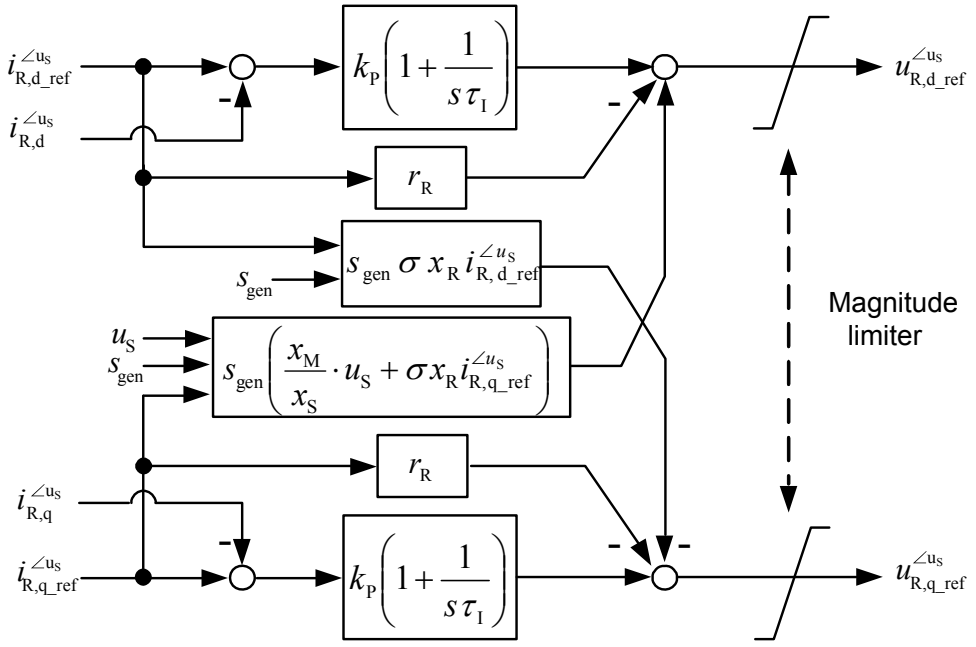


Figure 4-8: Inner current control for MSC with feed-forward terms

The rotor current set-points $i_{\mathrm{R,d\_ref}}^{\angle u_\mathrm{S}}$ and $i_{\mathrm{R,q\_ref}}^{\angle u_\mathrm{S}}$ can be calculated from the steady-state system equations of total power of a DFIG system. The equations for the power are given as:

$$p_{\mathrm{WTG}} = p_{\mathrm{S}} + p_{\mathrm{LSC}} \tag{4.16}$$

$$q_{\mathrm{WTG}} = q_{\mathrm{S}} + q_{\mathrm{LSC}} \tag{4.17}$$

$$p_{\mathrm{S}} = \mathrm{Re}\left\{\underline{u}_{\mathrm{S}}\underline{i}_{\mathrm{S}}^{*}\right\} \tag{4.18}$$

$$q_{\mathrm{S}} = \mathrm{Im}\left\{\underline{u}_{\mathrm{S}}\underline{i}_{\mathrm{S}}^{*}\right\} \tag{4.19}$$

Taking into account Eq. (4.8), the following equations can be obtained:

$$p_{\mathrm{S}} = -\frac{x_{\mathrm{M}}}{x_{\mathrm{S}}} \cdot \left|\underline{u}_{\mathrm{S}}\right| \cdot i_{\mathrm{R,d}}^{\angle u_\mathrm{S}} \tag{4.20}$$

$$q_{\mathrm{S}} = \frac{1}{x_{\mathrm{S}}} \cdot \left|\underline{u}_{\mathrm{S}}\right|^2 + \frac{x_{\mathrm{M}}}{x_{\mathrm{S}}} \cdot \left|\underline{u}_{\mathrm{S}}\right| \cdot i_{\mathrm{R,q}}^{\angle u_\mathrm{S}} \tag{4.21}$$

From Eq. (4.20) and (4.21), the feed-forward terms of the outer power control loop can be shown in Figure 4-9.

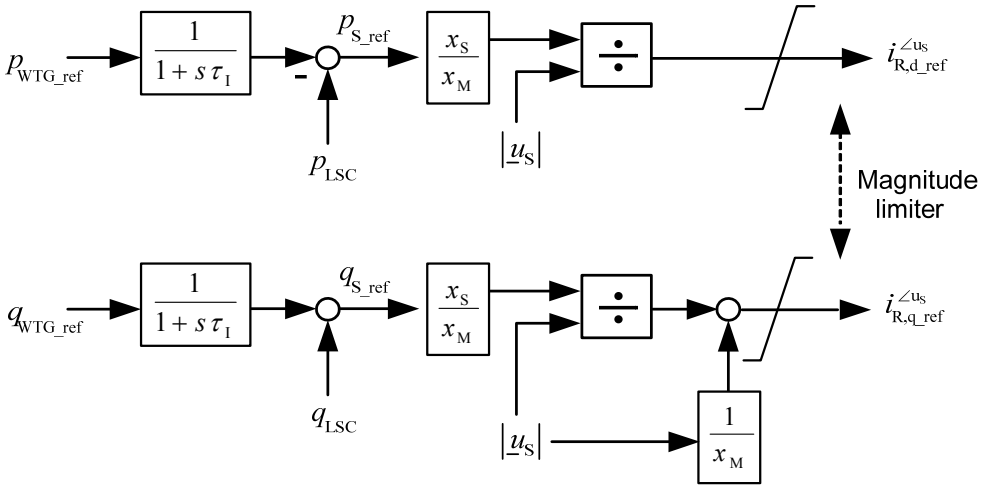


Figure 4-9: Outer MSC control loop

5 Basic Concepts of Converter Switching

The converter switching concepts are an important part of the control structure. It should provide features like [48]:

- Wide range of linear operation.
- Increase DC voltage utilization (higher output voltage).
- Low content of higher harmonics in voltage and current.
- Low frequency harmonics.
- Operation in over-modulation.
- Reduction of generated common mode voltage.
- Minimal number of switching to decrease switching losses.

Figure 5-1 shows the block diagram of switching flow for semiconductor devices in a converter, which gives a general overview. Various modulating reference signals define the types of pulse width modulation (PWM).

This chapter will describe the basic concepts of converter switching which review the switching schemes, the modulation strategies and the PWM types. Selected modulation strategies and PWM types will be implemented for the converter of the DFIG system, and the simulated results will be compared and analyzed.

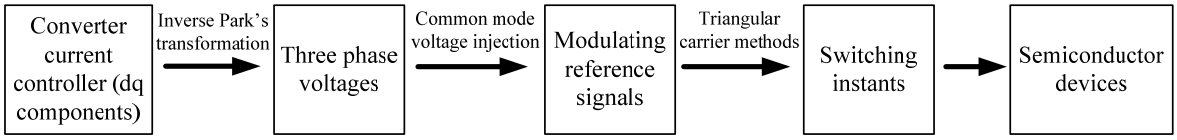


Figure 5-1: Block diagram of switching flow for semiconductor devices

5.1 Switching schemes

Almost all power electronic converters are operated in the "switched mode". This means the semiconductor switches within the converter are always in either one of two states; turn-off (no current flows), or saturated (turn-on completely, with only a small voltage drop across the switch). These turn-on and turn-off states are occurred by triggering switching instants (signals) to the gate of the semiconductor switches. The switching instants are generated which dependent on switching schemes such as square-wave and pulse width modulation (PWM) [49].

5.1.1 Square-wave

In the square-wave switching scheme, each switch of the converter leg is turned-on for one half-cycle (180°) of the desired output frequency as shown in Figure 5-2. One of the advantages of the square-wave scheme is that each semiconductor switch changes its state only twice per cycle, or less switching frequency. Thus, it generates low switching losses. A small number of switching is important for high-power semiconductor switch e.g. thyristor which generally have slower turn-on and turn-off speeds. This scheme also runs in a simple operation [50].

Besides, one of the serious disadvantages of the square-wave scheme is that the converter is not capable of regulating the output voltage magnitude. Therefore, the output voltage contains large harmonic distortion which can become unacceptable [50].

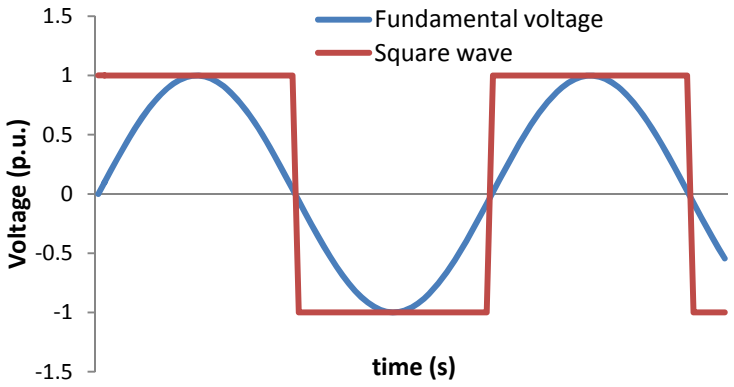


Figure 5-2: Square-wave switching scheme

5.1.2 Pulse width modulation (PWM)

In order to control the flow of power in a converter, the semiconductor switches alternate between turn-on and turn-off states. This happens rapidly enough that the inductors and capacitors at the input and output nodes of the converter average or filter the switched signal. The switched component is attenuated and the desired DC or low frequency AC component is retained. This process is called pulse width modulation (PWM), since the desired average value is controlled by modulating the width of the pulses.

PWM switching scheme is used to obtain variable voltage and frequency supply. This scheme is the most widely used switching scheme in most drive system including in the DFIG based WT application. The advantages and disadvantages possessed by PWM switching scheme are as below [50]:

- The output voltage control with this method can be obtained without any additional components.
- Lower order harmonics can be eliminated or minimized along with its output voltage control. As higher order harmonics can be filtered easily, the filtering requirements are minimized.
- The main disadvantage of this method when compared to the square-wave switching scheme is that this scheme generate higher switching losses since it has higher switching frequency.

5.2 PWM types

Several PWM types have been developed and these can be generally classified into continuous PWM (CPWM) and discontinuous PWM (DPWM) [51], [52]. The classification is based on the waveform of modulating reference signal, where in DPWM the modulating reference signal is clamped to the DC-link for one third of fundamental period.

The variety of modulating reference signals (except for sinusoidal PWM) is produced by adding different waveform shape of common mode voltage (CMV) to the fundamental voltages. This CMV is a zero sequence signal which normally the third harmonic whose frequency is three times that of the fundamental voltage. It can be obtained by comparing the magnitude of the three fundamental voltages with some analytical expressions.

In converter applications, the main reason of injection CMV for PWM is to increase the DC voltage utilization, so that the converter will have more generated output voltage with about 1.155 p.u. Apart from that, the injection CMV for PWM could also influence the generated voltage and current harmonics distortion level, and switching losses of the converter. Generally, adding CMV is necessary for CPWM types to have lower harmonics distortion level while for DPWM types to have lower switching losses. These two performances are the main focus in this thesis and will be investigated further.

The difference between CPWM and DPWM also can be seen in the generated switching instants which reduced one third for DPWM as shown in Figure 5-3. The PWM types and their characteristics can be summarized as in Table 5-1.

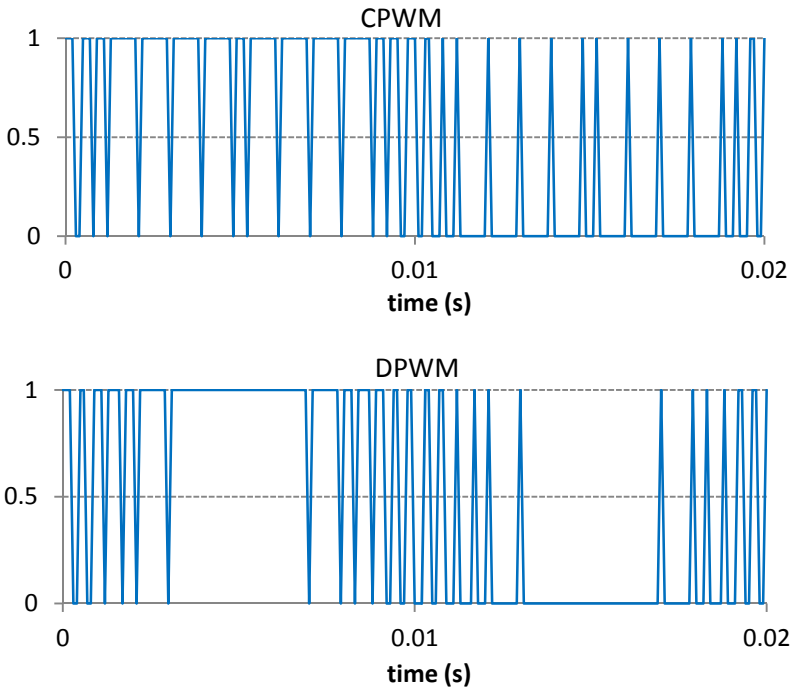


Figure 5-3: Switching instants of CPWM and DPWM (pulse peak at 1.0)

Table 5-1: General overview of PWM types and their characteristics

PWM types		**Injection CMV**	**Characteristics**
CPWM	SPWM	Without CMV	Basic type with 1.0 p.u. output voltage
	TTHIPWM	With CMV	Have lower harmonics distortion level, and more output voltage of 1.155 p.u.
	STHIPWM4		
	STHIPWM6		
DPWM	DPWM0		Have lower switching losses, and more output voltage of 1.155 p.u.
	DPWM1		
	DPWM2		
	DPWM3		
	DPWMMIN		
	DPWMMAX		

5.2.1 Continuous PWM

Continuous PWM (CPWM) types such as sinusoidal PWM (SPWM), 1/4 peak value of sinusoidal third harmonic injection PWM (STHIPWM4), 1/6 peak value of sinusoidal third harmonic injection PWM (STHIPWM6), 1/4 peak value of triangular third harmonic injection PWM (TTHIPWM) which also called space vector PWM have been studied extensively [53]-

[70]. In CPWM, the modulating signal is a continuous time varying signal. The modulating reference signals are always within the triangle peak boundaries and within every carrier cycle triangle and modulation waves intersect, and, therefore, on and off switching occur.

Among the CPWM types, TTHIPWM is selected for further investigation and will be implemented for the DFIG based WT. Figure 5-4 shows the three fundamental voltages (u_a, u_b, u_c), the modulating reference signal of "phase a" (u_a^*) and the injection CMV (u_{no_PWM}) for TTHIPWM. The injection CMV is obtained using the following analytical expressions:

$$\begin{aligned}
&\text{if } |u_a| \le |u_b| \text{ and } |u_a| \le |u_c| \quad \Rightarrow \quad u_{no_PWM,1} = 0.5 \times u_a \\
&\text{if } |u_b| \le |u_a| \text{ and } |u_b| \le |u_c| \quad \Rightarrow \quad u_{no_PWM,2} = 0.5 \times u_c \\
&\text{if } |u_c| \le |u_a| \text{ and } |u_c| \le |u_b| \quad \Rightarrow \quad u_{no_PWM,3} = 0.5 \times u_b \\
&\textit{else} \quad u_{no_PWM,1}, u_{no_PWM,2}, u_{no_PWM,3} = 0 \\
&u_{no_PWM} = u_{no_PWM,1} + u_{no_PWM,2} + u_{no_PWM,3}
\end{aligned} \tag{5.1}$$

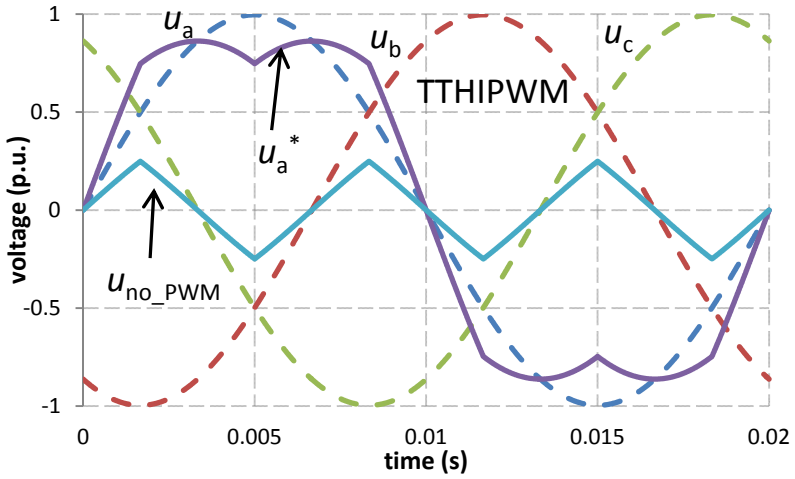


Figure 5-4: Modulating reference signal of "phase a" with injection CMV for TTHIPWM

5.2.2 Discontinuous PWM

Discontinuous PWM (DPWM) types are including DPWM0, DPWM1, DPWM2, DPWM3, DPWMMAX and DPWMMIN [58]. In DPWM, the modulating reference signal of a phase has at least one segment which is clamped to the positive or negative DC-link for at most a total of 120°, therefore, within such intervals the corresponding converter leg discontinues modulation.

Among the DPWM types, DPWM0, DPWM1 and DPWM2 are selected for further investigation and will be implemented for the DFIG based WT. Figure 5-5 shows the three fundamental voltages (u_a, u_b, u_c), the modulating reference signal of "phase a" (u_a^*) and the

injection CMV ($u_{\text{no\_PWM}}$) for DPWM0, DPWM1 and DPWM2. The injection CMV for each type is obtained using the following analytical expressions:

DPWM0:

$$\begin{aligned}
&\text{if } |u_c| \le |u_a| \text{ and } |u_c| \le |u_b| \quad \Rightarrow \quad u_{\text{no_PWM},1} = \text{sign}(u_a) - u_a \\
&\text{if } |u_b| \le |u_c| \text{ and } |u_b| \le |u_a| \quad \Rightarrow \quad u_{\text{no_PWM},2} = \text{sign}(u_b) - u_b \\
&\text{if } |u_a| \le |u_b| \text{ and } |u_a| \le |u_c| \quad \Rightarrow \quad u_{\text{no_PWM},3} = \text{sign}(u_c) - u_c \\
&\textit{else} \quad u_{\text{no_PWM},1}, u_{\text{no_PWM},2}, u_{\text{no_PWM},3} = 0 \\
&u_{\text{no_PWM}} = u_{\text{no_PWM},1} + u_{\text{no_PWM},2} + u_{\text{no_PWM},3}
\end{aligned} \tag{5.2}$$

DPWM1:

$$\begin{aligned}
&\text{if } |u_b| \le |u_a| \text{ and } |u_c| \le |u_a| \quad \Rightarrow \quad u_{\text{no_PWM},1} = \text{sign}(u_a) - u_a \\
&\text{if } |u_a| \le |u_b| \text{ and } |u_c| \le |u_b| \quad \Rightarrow \quad u_{\text{no_PWM},2} = \text{sign}(u_b) - u_b \\
&\text{if } |u_a| \le |u_c| \text{ and } |u_b| \le |u_c| \quad \Rightarrow \quad u_{\text{no_PWM},3} = \text{sign}(u_c) - u_c \\
&\textit{else} \quad u_{\text{no_PWM},1}, u_{\text{no_PWM},2}, u_{\text{no_PWM},3} = 0 \\
&u_{\text{no_PWM}} = u_{\text{no_PWM},1} + u_{\text{no_PWM},2} + u_{\text{no_PWM},3}
\end{aligned} \tag{5.3}$$

DPWM2:

$$\begin{aligned}
&\text{if } |u_b| \le |u_a| \text{ and } |u_b| \le |u_c| \quad \Rightarrow \quad u_{\text{no_PWM},1} = \text{sign}(u_a) - u_a \\
&\text{if } |u_c| \le |u_b| \text{ and } |u_c| \le |u_a| \quad \Rightarrow \quad u_{\text{no_PWM},2} = \text{sign}(u_b) - u_b \\
&\text{if } |u_a| \le |u_c| \text{ and } |u_a| \le |u_b| \quad \Rightarrow \quad u_{\text{no_PWM},3} = \text{sign}(u_c) - u_c \\
&\textit{else} \quad u_{\text{no_PWM},1}, u_{\text{no_PWM},2}, u_{\text{no_PWM},3} = 0 \\
&u_{\text{no_PWM}} = u_{\text{no_PWM},1} + u_{\text{no_PWM},2} + u_{\text{no_PWM},3}
\end{aligned} \tag{5.4}$$

As shown in the figure, the modulating reference signal (u_a^*) is clamped to the upper and lower terminals of the DC-link (±1.0 p.u.) with total period of clamping corresponding to one third of the fundamental period. Adjusting modulation phase angle ψ from the intersection point of the two fundamental signals (as shown in Figure 5-5) changing CMV and modulating reference signal which is given as ψ=0 for DPWM0, ψ=π/6 for DPWM1 and ψ =π/3 for DPWM2.

Since modulation reference signal implies switching losses, the switching loss characteristics of CPWM and DPWM types are different. Detailed studies indicated the waveform quality and switching losses will be presented in the next section.

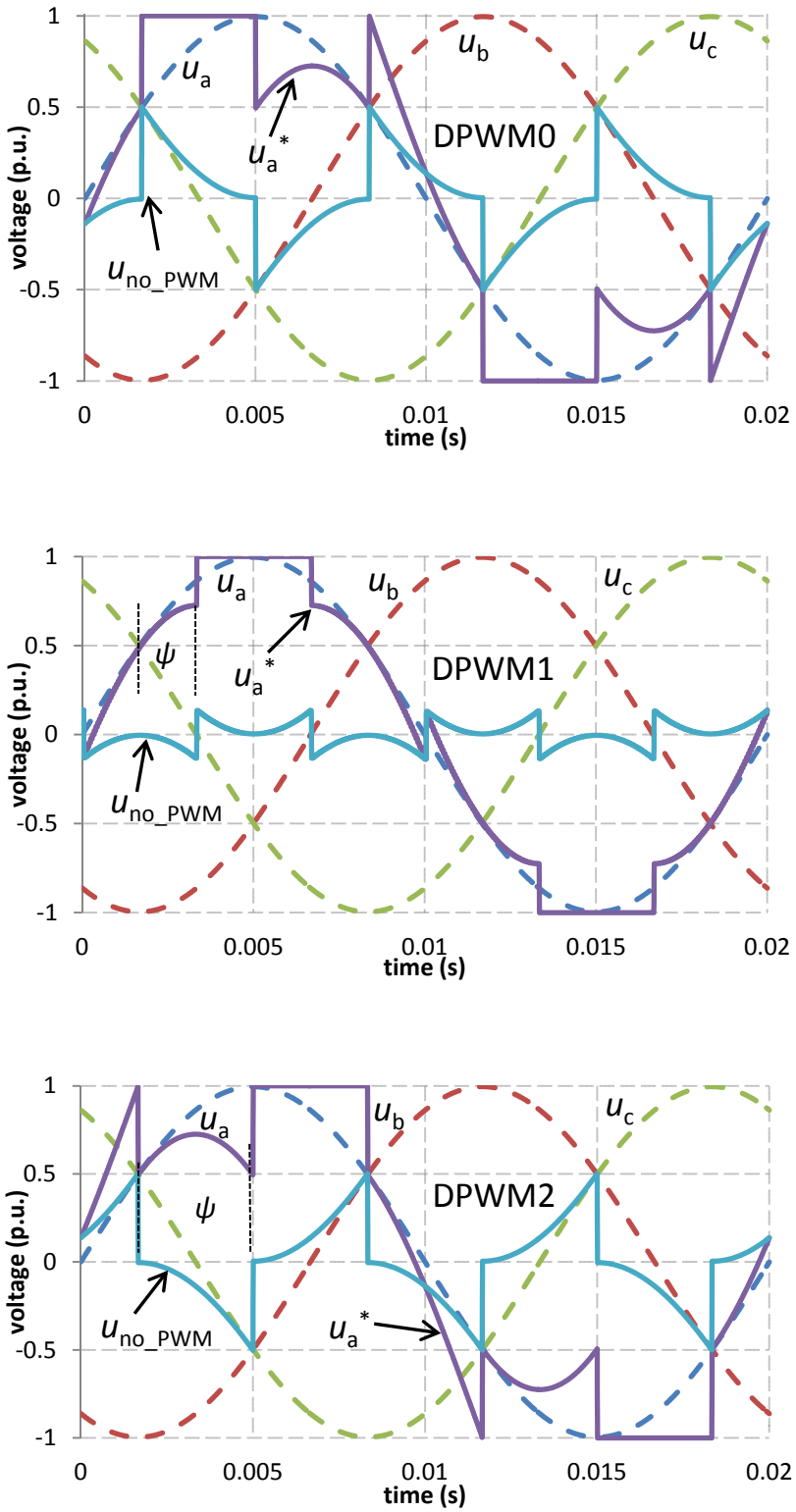


Figure 5-5: Modulating reference signal of "phase a" with injection CMV for DPWM0, DPWM1 and DPWM2

5.2.3 Analysis of switching losses

In CPWM types, all three phase currents are commutated within each carrier cycle of a full fundamental cycle. Therefore, for all CPWM methods, the switching losses are the same and independent of power factor.

In DPWM types, however, the switching losses are significantly influenced by the waveform of modulating reference signal and load power factor angle. DPWM types cease to switch each switch for a total of 120° per fundamental cycle and the location of each DC-link clamped segment with respect to the modulation wave fundamental component phase is modulator type dependent. Therefore, the load power factor and the modulating reference signal together determine the time interval that the load current is not commutated.

The switching losses of a PWM are also load current dependent and increase with the current magnitude. Switching device manufacturers' manual (for example IGBT datasheet) indicates this relation is approximately linear, where the switching losses are proportional to the current magnitude.

Assuming the converter switching devices have linear current turn-on and turn-off characteristics with respect to time and accounting only for the fundamental component of the load current, the average value of the switching losses over the fundamental cycle can be derived as:

$$p_{\mathrm{SWloss}} = \frac{1}{2\pi} \cdot \frac{u_{\mathrm{DC}} \cdot \left(t_{\mathrm{on}} + t_{\mathrm{off}}\right)}{2T_{\mathrm{S}}} \cdot \int_0^{2\pi} \left| i \right| \, \mathrm{d}\omega t \tag{5.5}$$

where i is the load current, t_{on} is the turn-on time, t_{off} is the turn-off time and u_{DC} is the DC voltage.

Assuming steady state operation where the currents are practically sinusoidal, the Eq. (5.5) is the function of the load power factor angle and the current magnitude. Thus, the power factor angle φ enters the formula as the integral boundary term. For CPWM types which are φ independent, the switching losses value can be derived as:

$$p_{\mathrm{SWloss\_CPWM}} = \frac{u_{\mathrm{DC}} \cdot \left(t_{\mathrm{on}} + t_{\mathrm{off}}\right)}{\pi T_{\mathrm{S}}} \cdot i_{\max} \tag{5.6}$$

where $i_{\max}$ is the load current maximum value. Normalizing p_{SWloss} to $p_{\mathrm{SWloss\_CPWM}}$, the switching loss function (*SLF*) of the DPWM types can be expressed as:

$$SLF = \frac{p_{\mathrm{SWloss}}}{p_{\mathrm{SWloss\_CPWM}}} \tag{5.7}$$

By the definition of Eq. (5.7), the *SLF* of CPWM types is unity. The *SLF* of the DPWM types can be easily calculated from the current switching function as:

$$SLF_{\mathrm{DPWM}} = \begin{cases} \frac{\sqrt{3}}{2}\cos\left(\frac{4\pi}{3}+\psi-\varphi\right), & -\frac{\pi}{2} \le \varphi \le -\frac{\pi}{2}+\psi \\ 1-\frac{1}{2}\sin\left(\frac{\pi}{3}+\psi-\varphi\right), & -\frac{\pi}{2}+\psi \le \varphi \le -\frac{\pi}{6}+\psi \\ \frac{\sqrt{3}}{2}\cos\left(\frac{\pi}{3}+\psi-\varphi\right), & \frac{\pi}{6}+\psi \le \varphi \le \frac{\pi}{2} \end{cases} \tag{5.8}$$

The *SLF* function of the DPWM0, DPWM1 and DPWM2 can be easily evaluated from Eq. (5.8) by substituting ψ=0, ψ=π/6 and ψ=π/3 respectively.

Figure 5-6 shows the switching loss function of DPWM0, DPWM1 and DPWM2 in relation to power factor angle under fixed carrier frequency constraint with *SLF* of TTHIPWM as a reference. In other words, the *SLF* of TTHIPWM is always 1.0 p.u. by definition.

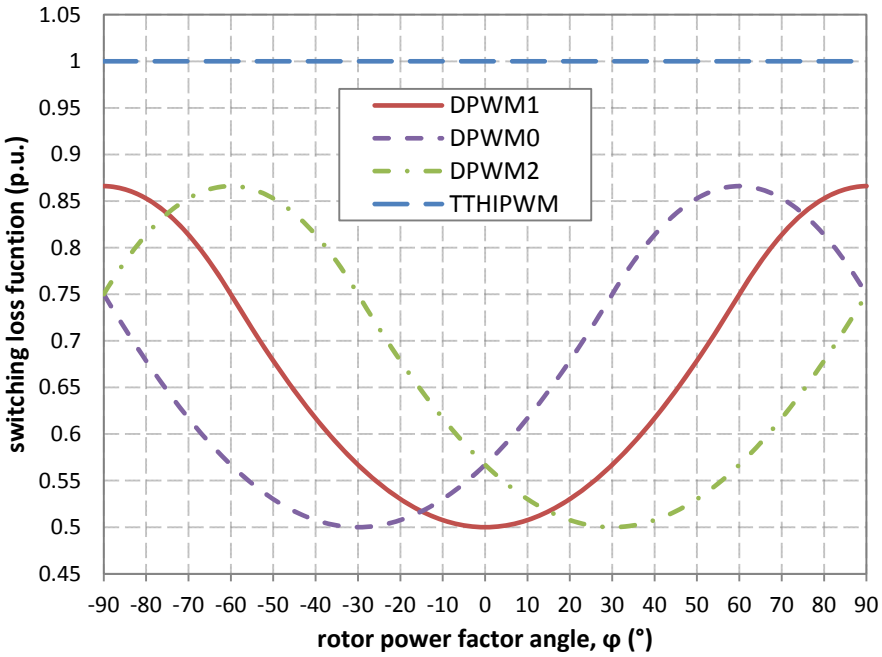


Figure 5-6: Switching loss function of TTHIPWM, DPWM0, DPWM1 and DPWM2 at constant carrier frequency

From the figure, at different power factor angles, the switching losses of PWM types show different values. For example, at φ=0° the DPWM1 has the lowest switching losses while having the worst at φ=90° and φ=-90°. Between φ=15° and φ=90°, the DPWM2 has the lowest switching losses while between φ=-15° and φ=-90°the DPWM0 has the lowest switching losses.

5.2.4 Analysis of harmonics

Harmonics of a converter concentrated at the carrier frequency, its sidebands, its multiples, and the sideband of its multiples. A converter's waveform quality is determined by the rms value (per fundamental cycle) of these harmonics. With the assumption that the carrier frequency is higher than the fundamental frequency by at least an order of magnitude and the load high frequency model can be approximated with an inductance, the harmonic current rms value can be closed-form calculated as a function of the modulation index [71], [72]. To obtain a load inductance and carrier frequency independent formula, the rms harmonic current can be normalized to a base value.

Harmonic distortion factor (*HDF*) function is a polynomial which only depends on the modulation index. The *HDF* of TTHIPWM, DPWM1, DPWM0 and DPWM2 are given as [71]:

$$HDF_{\text{TTHIPWM}} = \frac{3}{2}\left(\frac{\pi}{4}M\right)^2 - \frac{4\sqrt{3}}{\pi}\left(\frac{\pi}{4}M\right)^3 + \left(\frac{27}{16} - \frac{81\sqrt{3}}{64\pi}\right)\left(\frac{\pi}{4}M\right)^4 \tag{5.9}$$

$$HDF_{\text{DPWM1}} = 6\left(\frac{\pi}{4}M\right)^2 - \left(\frac{8\sqrt{3}+45}{2\pi}\right)\left(\frac{\pi}{4}M\right)^3 + \left(\frac{27}{8} + \frac{27\sqrt{3}}{32\pi}\right)\left(\frac{\pi}{4}M\right)^4 \tag{5.10}$$

$$HDF_{\text{DPWM0, DPWM2}} = 6\left(\frac{\pi}{4}M\right)^2 - \frac{35\sqrt{3}}{2\pi}\left(\frac{\pi}{4}M\right)^3 + \left(\frac{27}{8} + \frac{81\sqrt{3}}{64\pi}\right)\left(\frac{\pi}{4}M\right)^4 \tag{5.11}$$

where m is the modulation index, defined as the ratio of the fundamental component magnitude of the line to neutral converter output voltage u_{m} to the fundamental component magnitude of the six-step mode voltage $u_{\text{m6step}}=2u_{\text{DC}}/\pi$, given as:

$$m = \frac{u_{\text{m}}}{u_{\text{m6step}}} \tag{5.12}$$

Figure 5-7 shows the harmonic distortion factor curves in the linear modulation range assuming equal carrier frequency for each PWM types. The figure clearly shows that all DPWM types have higher *HDF* compared to the TTHIPWM at the entire modulation range.

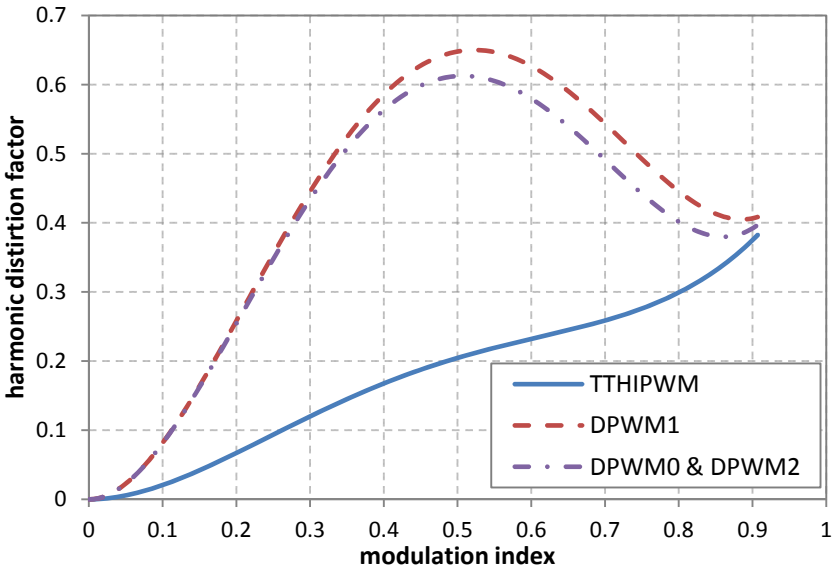


Figure 5-7: Harmonic distortion factor of TTHIPWM, DPWM0, DPWM1 and DPWM2 at constant carrier frequency in the linear modulation range

When carrier frequency is taken into account, the performances of CPWM and DPWM in terms of switching losses and harmonic distortion factor can be characterized by the following three practical cases [71].

A. Constant carrier frequency:

   DPWM has an average switching frequency that is two thirds of the carrier frequency. For all DPWM types, the switching losses are lower than that of CPWM. The highest reduction in switching losses is 50% when a phase is clamped around the peak phase current. However, the *HDF* is higher than that of CPWM over the entire modulation range.

B. Constant average switching frequency:

   The carrier frequency of DPWM is selected as 1.5 of CPWM carrier frequency. In general, the *HDF* of DPWM is lower than CPWM at modulation indexes above approximately 0.65. However, the switching losses of DPWM are reduced by half with maximum 25%.

C. Constant switching losses (at $-30° \leq \varphi \leq 30°$):

   The carrier frequency of DPWM is selected as 2.0 of CPWM carrier frequency. The *HDF* of DPWM and CPWM are at almost the same level for modulation index below approximately 0.25. The *HDF* of DPWM becomes lower than that of CPWM above approximately 0.25.

In this study, the first case with a constant carrier frequency of 2250 Hz is selected for both CPWM and DPWM to have the converter with the maximum switching losses performance.

5.3 Switching instants generation method: Triangle intersection

Switching instants of both CPWM and DPWM types can be produced either by triangle intersection (also called carrier based) technique or direct digital (also called space vector modulation) technique. Both techniques are different in their operation but generate the same switching instants. In this study, the triangle intersection technique is selected and presented in detail.

In triangle intersection technique, three-phase modulating reference signals are compared with a common triangular carrier signal. In this way, the logical signals are generated, which define the switching instants of power converter. Figure 5-8 shows the block diagram of the triangle intersection technique with common mode voltage injection.

The purpose of PWM three-phase converters is to shape and to control the three-phase output voltages in magnitude and frequency with an essentially constant input voltage u_{DC}. To obtain balanced three-phase output voltages in a three-phase PWM, the same triangular voltage waveform u_{tri} is compared with three modulating reference signals u_a^*, u_b^*, u_c^* that are 120° out of phase.

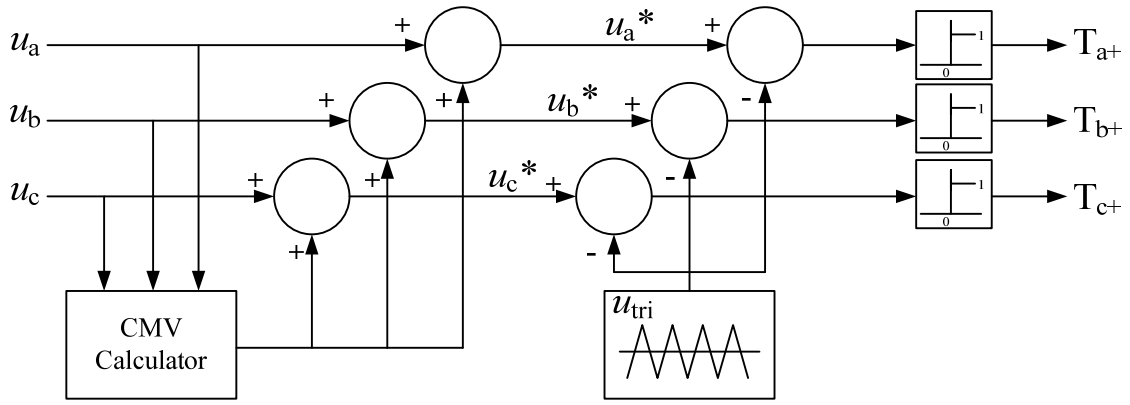
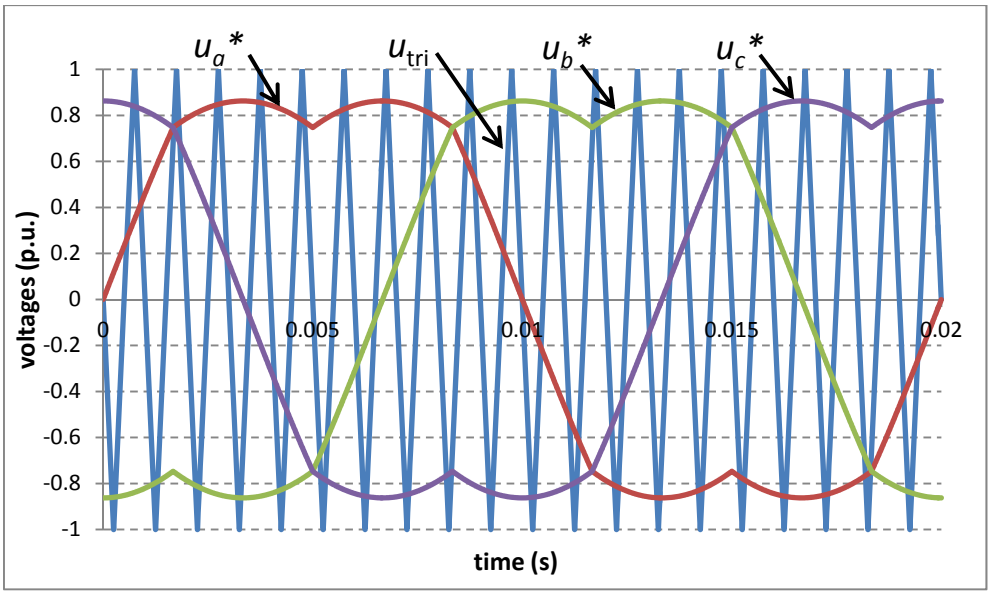


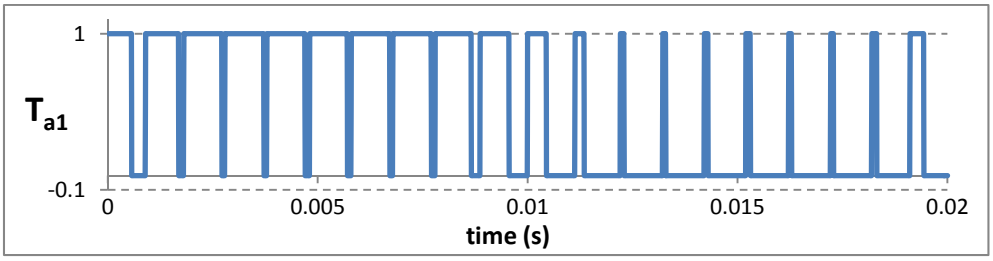
Figure 5-8: Triangle intersection technique based PWM with common mode voltage injection

5.3.1 Switching instants generation in two-level converter

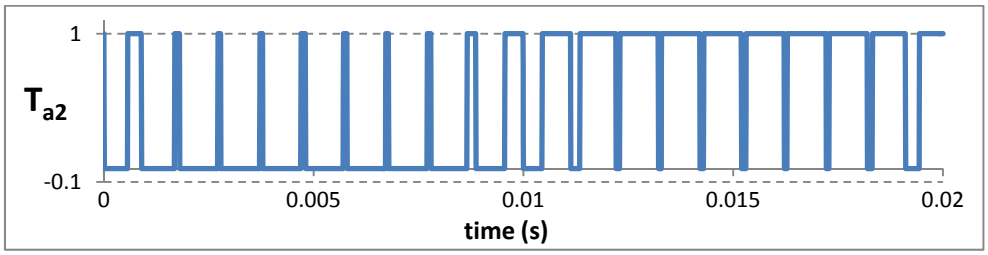
In two-level converter, in order to generate the switching instants, three modulating reference signals are compared with a single triangular carrier waveform u_{tri} as shown in Figure 5-9(a). Figure 5-9(b),(c) shows the resulting switching instants for “phase a”.



(a) Modulating reference signals with single triangular carrier



(b) Switching instants for upper IGBT in "phase a" leg T_{a+}



(c) Switching instants for lower IGBT in "phase a" leg T_{a-}

Figure 5-9: Switching instants generation in two-level converter

In order to trigger the IGBTs, the following algorithm can be used:

$$u_x^* > u_{\text{tri}} \quad \Rightarrow \quad \text{T}_{x1} = \text{on} \quad (\text{T}_{x2} = \text{off}) \quad \Rightarrow \quad u_{xo} = \frac{u_{\text{DC}}}{2} \quad (x = \text{a,b,c}) \tag{5.13}$$

$$u_x^* < u_{\text{tri}} \quad \Rightarrow \quad \text{T}_{x1} = \text{off} \quad (\text{T}_{x2} = \text{on}) \quad \Rightarrow \quad u_{xo} = -\frac{u_{\text{DC}}}{2} \quad (x = \text{a,b,c}) \tag{5.14}$$

Two possible switching states for each phase leg are given in Table 5-2, where 1 and 0 denote the on state and off state of the IGBT, respectively. For the three-phase two-level converter, eight combinations of switching states which also called voltage vectors are possible as shown in Table 5-3. For example, [+ - -] means that T_{a1}, T_{b2}, T_{c2} are turned-on and T_{a2}, T_{b1},

T_{c1} are turned-off. Table 5-3 also shows the output voltage of the converter at each phase leg and the generated common mode voltage, u_{no_conv} which expressed as:

$$u_{no\_conv} = \frac{u_{ao} + u_{bo} + u_{co}}{3} \tag{5.15}$$

This generated common mode voltage will be discussed further in chapter 7.

Table 5-2: Switching states for each phase of two-level converter

Switching states	T_{x1}	T_{x2}
Positive "+"	1	0
Negative "-"	0	1

Table 5-3: Switching states, output phase voltage and generated common mode voltage of three-phase two-level converter

Vector	Leg a	Leg b	Leg c	u_{ao}	u_{bo}	u_{co}	u_{no_conv}
u_1	+	-	-	$u_{DC}/2$	$-u_{DC}/2$	$-u_{DC}/2$	$-u_{DC}/6$
u_2	+	+	-	$u_{DC}/2$	$u_{DC}/2$	$-u_{DC}/2$	$u_{DC}/6$
u_3	-	+	-	$-u_{DC}/2$	$u_{DC}/2$	$-u_{DC}/2$	$-u_{DC}/6$
u_4	-	+	+	$-u_{DC}/2$	$u_{DC}/2$	$u_{DC}/2$	$u_{DC}/6$
u_5	-	-	+	$-u_{DC}/2$	$-u_{DC}/2$	$u_{DC}/2$	$-u_{DC}/6$
u_6	+	-	+	$u_{DC}/2$	$-u_{DC}/2$	$u_{DC}/2$	$u_{DC}/6$
u_7	+	+	+	$u_{DC}/2$	$u_{DC}/2$	$u_{DC}/2$	$u_{DC}/2$
u_0	-	-	-	$-u_{DC}/2$	$-u_{DC}/2$	$-u_{DC}/2$	$-u_{DC}/2$

5.3.2 Switching instants generation in three-level NPC converter

In three-level NPC converter, in order to generate the switching instants, two triangular carrier waveforms, upper carrier u_{tri_up} and lower carrier u_{tri_low} are compared with three modulating reference signals that are 120° out of phase, as shown in Figure 5-12.

Different methods of the triangular carrier signals can be implemented for the three-level NPC converter which including [73], [74],

- Alternative phase opposition disposition (APOD)
- Phase disposition (PD)
- Phase opposition disposition (POD)
- Hybrid (H)
- Phase shifted (PS)

- Super imposed carrier (SIC)

Different triangular carrier method generates different level of generated common mode voltage (CMV), which will be described in chapter 7. In this study, the commonly used method, namely PD and POD are selected and will be presented in detail.

Phase dispositions (PD): The upper and lower carrier waveforms are all in phase as shown in Figure 5-10.

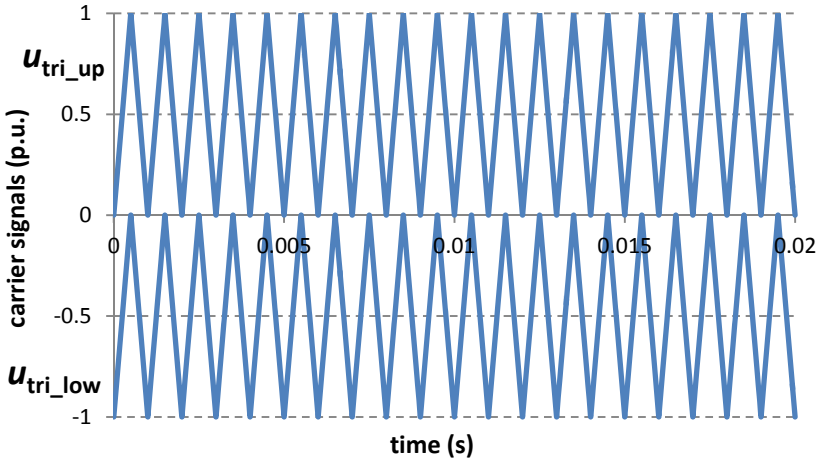


Figure 5-10: Phase disposition (PD)

Phase opposition dispositions (POD): The upper and lower carrier waveforms are in phase shift of 180° as shown in Figure 5-11.

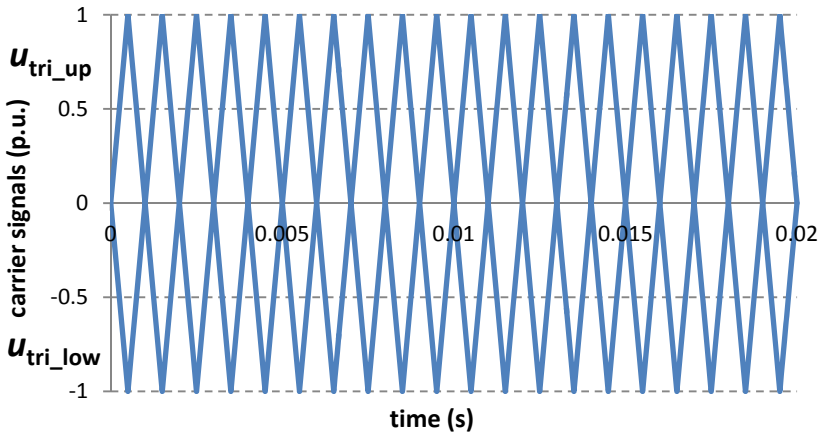


Figure 5-11: Phase opposition disposition (POD)

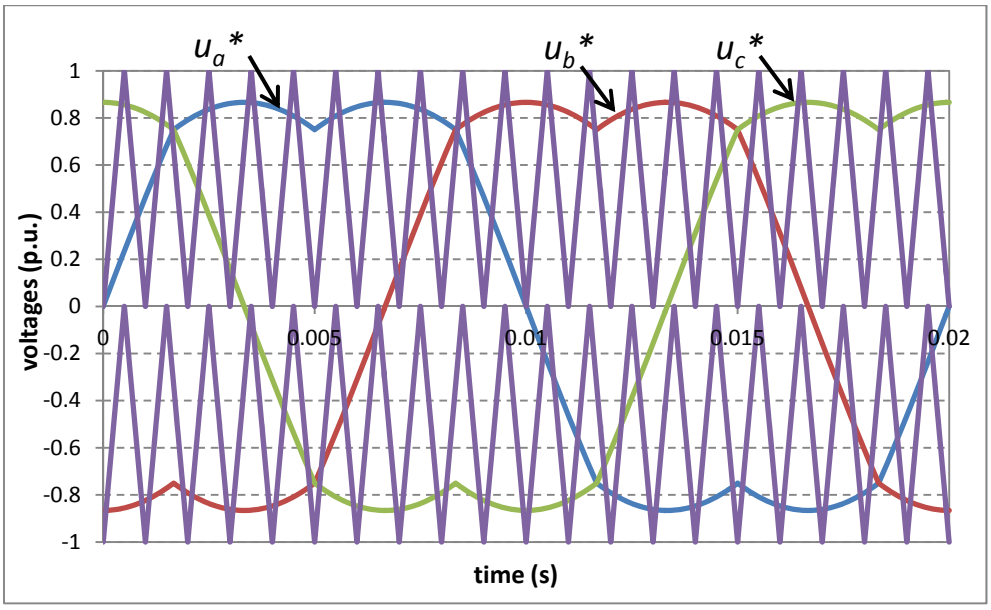
In order to trigger the IGBTs, the following algorithm can be used:

$$u_x^* > u_{\text{tri\_up}} \quad \Rightarrow \quad (\mathrm{T}_{x1} = \text{on} \,,\, \mathrm{T}_{x2} = \text{on}) \quad \Rightarrow \quad u_{xo} = \frac{u_{\mathrm{DC}}}{2} \quad (x = \mathrm{a}, \mathrm{b}, \mathrm{c}) \tag{5.16}$$

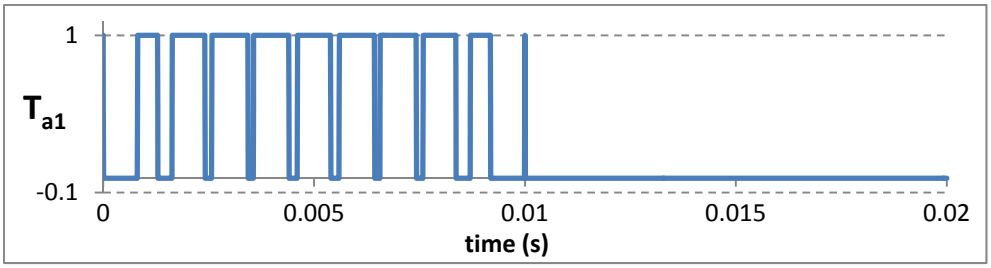
$$u_x^* < u_{\text{tri\_low}} \quad \Rightarrow \quad (\mathrm{T}_{x3} = \text{on} \,,\, \mathrm{T}_{x4} = \text{on}) \quad \Rightarrow \quad u_{xo} = -\frac{u_{\mathrm{DC}}}{2} \quad (x = \mathrm{a}, \mathrm{b}, \mathrm{c}) \tag{5.17}$$

$$\text{else} \quad \Rightarrow \quad u_{xo} = 0 \quad (x = \mathrm{a}, \mathrm{b}, \mathrm{c}) \tag{5.18}$$

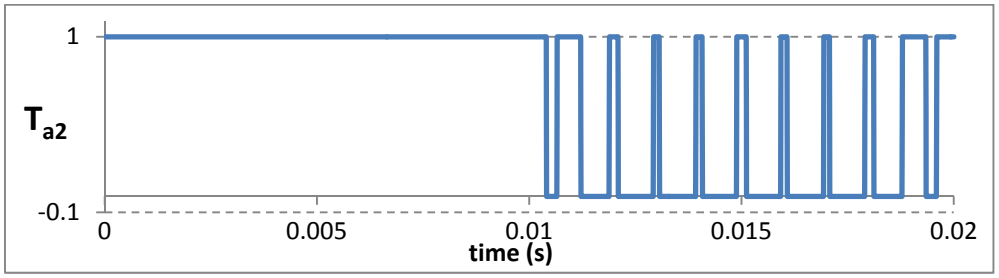
The switching instants for “phase a” are depicted in Figure 5-12(b),(c).



(a) Modulating reference signals with upper and lower triangular carrier



(b) Switching instants for upper IGBT in “phase a” leg T_{a1}



(c) Switching instants for upper IGBT in “phase a” leg T_{a2}

Figure 5-12: Switching instants generation in three-level NPC converter

Three possible switching states for each phase leg are given in Table 5-4, where 1 and 0 denote the on state and off state of the IGBT, respectively [75]. The positive half wave of the desired sinusoid is generated by switching the respective phase leg between the positive "+" and zero "0" states, and the negative half wave is generated by switching between the zero "0" and negative "-" states. The average switching frequency per device equals half the carrier frequency visible at the output.

Table 5-4: Switching states for each phase of three-level NPC converter

Switching states	T_{x1}	T_{x2}	T_{x3}	T_{x4}
Positive "+"	1	1	0	0
Negative "-"	0	0	1	1
Zero "0"	0	1	1	0

For the three-phase three-level NPC converter, 27 combinations of switching states are possible as shown in Table 5-5. For example, [+ - 0] means that T_{a1}, T_{a2}, T_{b3}, T_{b4}, T_{c2}, T_{c3} are turned-on and T_{a3}, T_{a4}, T_{b1}, T_{b2}, T_{c1}, T_{c4} are turned-off. Table 5-5 also shows the output voltage of the converter at each phase leg and the generated common mode voltage, $u_{\text{no\_conv}}$ which is also expressed in Eq. (5.15).

Table 5-5: Switching states, output phase voltage and generated common mode voltage of three-phase three-level NPC converter

Vector	Leg a	Leg b	Leg c	u_{ao}	u_{bo}	u_{co}	u_{no_conv}
u_0	-	-	-	$-u_{DC}/2$	$-u_{DC}/2$	$-u_{DC}/2$	$-u_{DC}/2$
u_1	0	-	-	0	$-u_{DC}/2$	$-u_{DC}/2$	$-u_{DC}/3$
u_2	+	-	-	$u_{DC}/2$	$-u_{DC}/2$	$-u_{DC}/2$	$-u_{DC}/6$
u_3	-	0	-	$-u_{DC}/2$	0	$-u_{DC}/2$	$-u_{DC}/3$
u_4	0	0	-	0	0	$-u_{DC}/2$	$-u_{DC}/6$
u_5	+	0	-	$u_{DC}/2$	0	$-u_{DC}/2$	0
u_6	-	+	-	$-u_{DC}/2$	$u_{DC}/2$	$-u_{DC}/2$	$-u_{DC}/26$
u_7	0	+	-	0	$u_{DC}/2$	$-u_{DC}/2$	0
u_8	+	+	-	$u_{DC}/2$	$u_{DC}/2$	$-u_{DC}/2$	$u_{DC}/6$
u_9	-	-	0	$-u_{DC}/2$	$-u_{DC}/2$	0	$-u_{DC}/3$
u_{10}	0	-	0	0	$-u_{DC}/2$	0	$-u_{DC}/6$
u_{11}	+	-	0	$u_{DC}/2$	$-u_{DC}/2$	0	0
u_{12}	-	0	0	$-u_{DC}/2$	0	0	$-u_{DC}/6$
u_{13}	0	0	0	0	0	0	0
u_{14}	+	0	0	$u_{DC}/2$	0	0	$u_{DC}/6$
u_{15}	-	+	0	$-u_{DC}/2$	$u_{DC}/2$	0	0
u_{16}	0	+	0	0	$u_{DC}/2$	0	$u_{DC}/6$
u_{17}	+	+	0	$u_{DC}/2$	$u_{DC}/2$	0	$u_{DC}/3$
u_{18}	-	-	+	$-u_{DC}/2$	$-u_{DC}/2$	$u_{DC}/2$	$-u_{DC}/6$
u_{19}	0	-	+	0	$-u_{DC}/2$	$u_{DC}/2$	0
u_{20}	+	-	+	$u_{DC}/2$	$-u_{DC}/2$	$u_{DC}/2$	$u_{DC}/6$
u_{21}	-	0	+	$-u_{DC}/2$	0	$u_{DC}/2$	0
u_{22}	0	0	+	0	0	$u_{DC}/2$	$u_{DC}/6$
u_{23}	+	0	+	$u_{DC}/2$	0	$u_{DC}/2$	$u_{DC}/3$
u_{24}	-	+	+	$-u_{DC}/2$	$u_{DC}/2$	$u_{DC}/2$	$u_{DC}/6$
u_{25}	0	+	+	0	$u_{DC}/2$	$u_{DC}/2$	$u_{DC}/3$
u_{26}	+	+	+	$u_{DC}/2$	$u_{DC}/2$	$u_{DC}/2$	$u_{DC}/2$

6 Converter Power Losses Model and Thermal Analysis

Modeling power losses of DFIG converter is one of important objective in this study since their outputs are required for thermal model. Developing a valid thermal model could predict junction temperature of the IGBT module in a voltage source converter which provides the following benefits [76]:

- Characterize the output power capability of a converter.
- Reduce the cost of design and production.
- Increase reliability.
- Quantify the accuracy of the estimated thermal impedance of an IGBT module.
- Predict the maximum switching frequency without violating thermal limits.
- Quantify the characteristics of the heat sink needed to dissipate the heat under worst case conditions.

This study will develop the power losses model and investigate the thermal analysis of DFIG converter specifically to characterize the output power capability of the converter. Generally, the output power of the DFIG converter is limited by mechanical power, stator current and rotor current. Among these limiting factors, the rotor current is limited by the junction temperature of the IGBT module of the machine side converter (MSC) especially during low frequencies (namely around synchronous operating points).

The power losses inside an IGBT module can restrict its use and therefore is becomes an important issue that cannot be ignored in the design stage. The power losses work as a heat source inside the IGBT and this heat will elevate the junction temperature and change the temperature profile inside the device. This is called self-heating effect.

The junction temperature should not exceed its limit that specified by the semiconductor manufacturer (normally 150°C). It could affect overheating in the converter and lead to IGBT failure. When the limit is exceeded, a current de-rating is necessary to reduce the junction temperature below its limit. Consequently, it could lead to a reduction in the output power capability of the converter. The performance of the power losses and the power capability of the DFIG converter will be discussed and presented in the next chapter with a comparison study on the two-level converter and the three-level NPC converter, and between continuous PWM and discontinuous PWM.

6.1 Power losses of IGBT and diode

The first step in performing the thermal analysis in an IGBT module is to calculate the power losses in the module. The power losses analysis in the two-level and three-level NPC converters has been reported extensively in a lot of literatures [77]-[80].

The power losses of semiconductor devices are divided into the static power losses and the non-static power losses based on manufacturer application notes. The static power losses are the on-state losses (conduction losses) and the blocking losses.

The non-static losses are divided into the switching losses (turn-on and turn-off) and driving losses. The driving losses and blocking losses are neglected since they accounted for a small portion of the overall power losses.

For an ideal switch, the power losses are zero. For a real switch, however there will be conduction and switching losses which are shown in Figure 6-1.

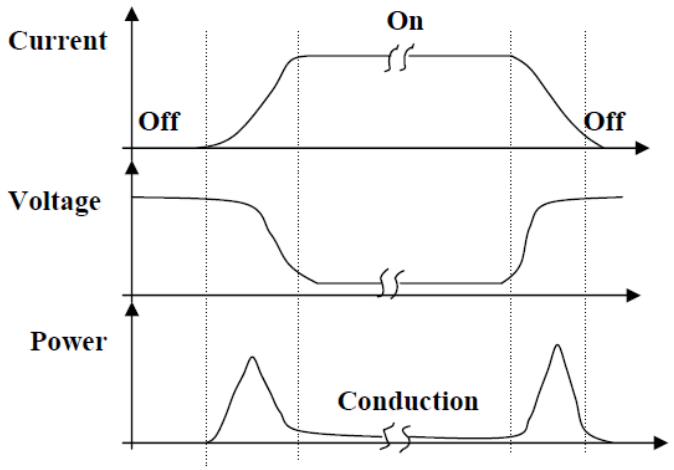


Figure 6-1: Current waveform, voltage waveform and instantaneous power losses for an IGBT over one switching cycle

When turn-on or turn-off the switch, the transient process takes time (several microseconds for IGBT) and the device consumes power while both the voltage and current are non-zero. When the switch is conducting, because there is voltage falling on the switch (several volts for IGBT), the conduction also has power dissipation.

There are different ways to calculate power losses of IGBT module. However, some complex models require many IGBT and diode parameters to perform the calculations. This study shows a way of modeling converter power losses making use of only information provided in the IGBT datasheets [81]-[83]. The proposed algorithm provides not only relatively accurate information, but it shows power losses for the entire operating conditions of the converter.

6.1.1 Conduction losses equations

IGBT is a not an ideal switch. Therefore, there will be a voltage drop across the IGBT and its free-wheeling diode while it conducts current. The calculation for conduction losses of IGBT and diode are derived in [82], [83] and given as:

$$P_{\mathrm{C1oss\_T}} = \int_0^T i(t)\cdot\left(U_{\mathrm{CE}}(t) + R_{\mathrm{CE}}\cdot i(t)\right)\mathrm{d}t \tag{6.1}$$

$$P_{\mathrm{C1oss\_D}} = \int_0^T i(t)\cdot\left(U_{\mathrm{F}}(t) + R_{\mathrm{F}}\cdot i(t)\right)\mathrm{d}t \tag{6.2}$$

Where U_{CE}, U_{F} are the threshold voltages and R_{CE} and R_{F} are the on-state resistances of the IGBT and diode, respectively. These variable parameters are obtained from the manufacturer datasheet [83] using the $\mathrm{I_C}$ vs. $\mathrm{U_{CE}}$ and $\mathrm{I_C}$ vs. $\mathrm{U_F}$ curves.

6.1.2 Switching losses equations

Switching losses occur when there is a turn-on and turn-off signal at IGBT's gate. The switching losses of IGBT and diode are dependent on load current, DC-link voltage and switching frequency.

The switching losses are calculated from the energy versus current curves obtained from manufacturer datasheet [83]. These curves represent the turn-on and turn-off losses of IGBT and diode which can be expressed as:

$$P_{\mathrm{SW1oss\_T}} = E_{\mathrm{on}} + E_{\mathrm{off}} \tag{6.3}$$

$$P_{\mathrm{SW1oss\_D}} = E_{\mathrm{rr}} \tag{6.4}$$

Where E_{on}, E_{off} are, respectively, the turn-on, turn-off losses on the IGBT and E_{rr} stands for the turn-off losses due to the reverse recovery in the diode.

In this study, these curves are approximated by a second order polynomial using the Polyfit function of Matlab/Simulink.

6.1.3 Total power losses equations

Combining Eq. (6.1)-(6.4), the average total power losses, P_{totavg} for a single IGBT and diode can be calculated by averaging the total power losses over the whole pulse or switching period, T_{s}. While the maximum total power losses, P_{totmax} can be calculated by averaging the total power losses over the total on-state time, t_{on} of IGBT or diode, respectively, within the pulse period, T_{s}.

$$P_{\text{totavg\_T}} = \frac{1}{T_S} \cdot \left(P_{\text{Closs\_T}} + P_{\text{SWloss\_T}} \right) \tag{6.5}$$

$$P_{\text{totavg\_D}} = \frac{1}{T_S} \cdot \left(P_{\text{Closs\_D}} + P_{\text{SWloss\_D}} \right) \tag{6.6}$$

$$P_{\text{totmax\_T}} = \frac{1}{t_{\text{on}}} \cdot \left(P_{\text{Closs\_T}} + P_{\text{SWloss\_T}} \right) \tag{6.7}$$

$$P_{\text{totmax\_D}} = \frac{1}{t_{\text{on}}} \cdot \left(P_{\text{Closs\_D}} + P_{\text{SWloss\_D}} \right) \tag{6.8}$$

Eq. (6.5)-(6.8) are modeled in Matlab/Simulink environment and implemented in the DFIG system.

6.2 Power losses in two-level converter

In order to calculate the power losses of a two-level converter, it is important to understand the operating principles of the converter. The operating principles show conduction paths and commutations of the converter that determine which IGBT and diode generate the conduction losses and the switching losses.

6.2.1 Conduction paths and commutations

The two-level converter produces the output voltage at the levels of $+u_{\text{DC}}$, $-u_{\text{DC}}$, which are produced by the specific conduction paths depending on the output current direction and the output voltage polarity. The current paths for positive and negative phase currents are depicted in Figure 6-2. In any switching state, one semiconductor lies within the current path. It should be noted that all IGBTs and diodes of the two-level converter are stressed by u_{DC}. Assuming a sinusoidal phase current, the maximum IGBT/diode current is the maximum phase current. These parameters determine the rating of the main semiconductors.

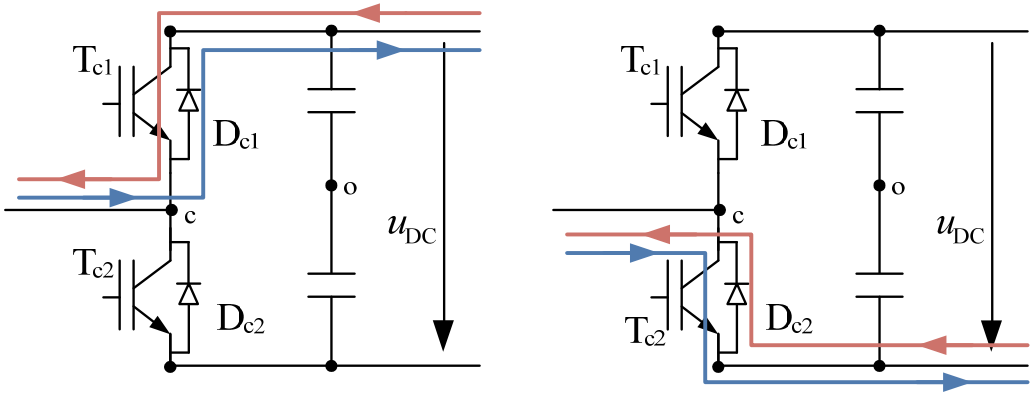


Figure 6-2: Conduction paths showing positive and negative current direction

Switching losses are created by the commutation processes between the different switching states. Only turn-on and turn-off losses of active IGBTs and recovery losses of diodes are considered. Turn-on losses of diodes are usually small so that they can be neglected [77]. The distribution of the switching losses and the conduction losses are summarized in Table 6-1 and Table 6-2 respectively.

Table 6-1: Devices that generate conduction losses in two-level converter

Switching states	T_{x1}	T_{x2}	D_{x1}	D_{x2}
Positive phase current				
"+"	x			
"–"				x
Negative phase current				
"+"			x	
"–"		x		

Table 6-2: Devices that generate switching losses in two-level converter

Commutations	T_{x1}	T_{x2}	D_{x1}	D_{x2}
Positive phase current				
+ ↔ –	x			x
Negative phase current				
+ ↔ –		x	x	

For a positive phase current, the commutation (+ → –) is initiated by the turn-off of T_{x1} and the current forced from T_{x1} to D_{x2} (x = a, b, c). The situation is visualized in Figure 6-3, where the current path of the switching active device is marked bold and the current path of the switching passive device is marked with a dashed line. The loss devices are encircled. In contrast, the commutation (– → +) is initiated by the turn-off of D_{x2} and the current forced from D_{x2} to T_{x1}.

For a negative phase current, the commutation (+ → –) is initiated by the turn-off of D_{x1} and the current forced from D_{x1} to T_{x2}. In contrast, the commutation (– → +) is initiated by the turn-off of T_{x2} and the current forced from T_{x2} to D_{x1}, as shown in Figure 6-3.

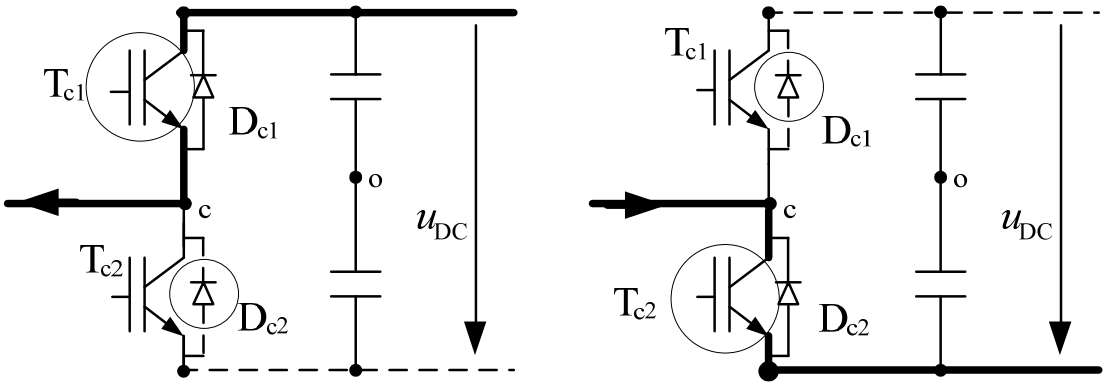


Figure 6-3: Commutations and switching losses of two-level converter

In each phase leg of the two-level converter, the conduction losses and switching losses of the upper and lower IGBTs/diodes are distributed equally (as shown in Table 6-1 and Table 6-2). Assuming that the three-phase AC currents are sinusoidal and symmetrical, thus the distribution of power losses in each IGBT/diode in the two-level converter is the same in one fundamental pulse period. Therefore, the total power losses calculation for the two-level converter is obtained by multiplying single IGBT/diode power losses (Eq. (6.5)-(6.8)) with the total number of IGBT/diode, which are 6.

6.2.2 IGBT module selection

As mentioned in section 6.1, the calculation of power losses in an IGBT module is based on the information provided in the IGBT datasheets from the semiconductor manufacturer. Thus, it is necessary to select appropriate IGBT module for the simulation. The IGBT module selection for two-level converter of 2 MW DFIG systems is based on the availability in the market and the commutation voltage.

The commutation voltage is the voltage across the IGBT during off-state. For the two-level converter, it is equal to the DC voltage. According to parameters of the DFIG system (Appendix A.1), the DC voltage is 1100 V which also the same value for the commutation voltage of the two-level converter. Considering some voltage reserves for transient overload or over-speed, 1700 V IGBT class with 2400 A of nominal current is proposed. Having the required ratings, SKiiP2414GB17E4-4DUW [84] from Semikron manufacturer is selected for this study.

6.2.3 Power losses model

For the conduction losses calculation, the U_{CE} versus I_C curves and the U_F versus I_F curves of the SKiiP2414GB17E4-4DUW as shown in Figure 6-4 and Figure 6-5 are referred (Appendix

A.2). The worst case junction temperature of 150°C is considered and the gate voltage is selected as 15 V. The necessary values extracted from the curves are given in Table 6-3. Using Eq. (6.1) and Eq. (6.2) and the obtained values from Table 6-3, the conduction losses of an IGBT and a diode are calculated.

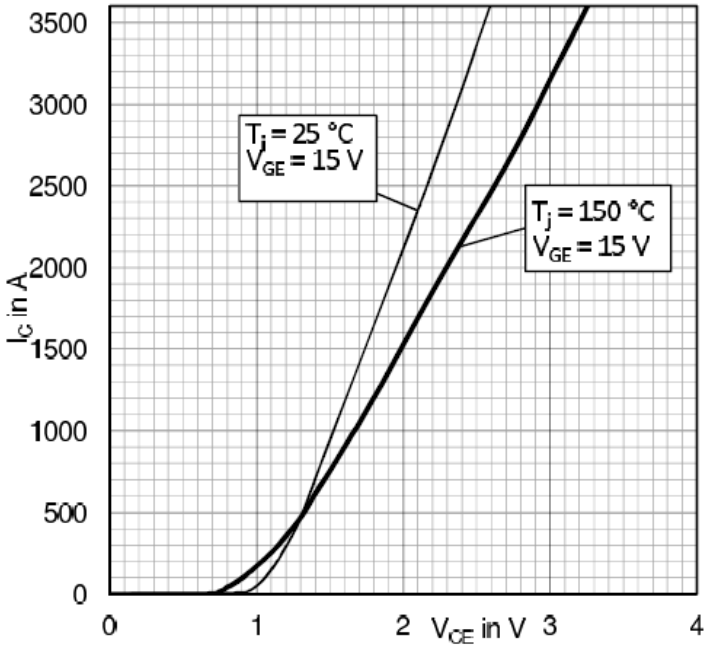


Figure 6-4: U_{CE} versus I_C curves of SKiiP2414GB17E4-4DUW [84]

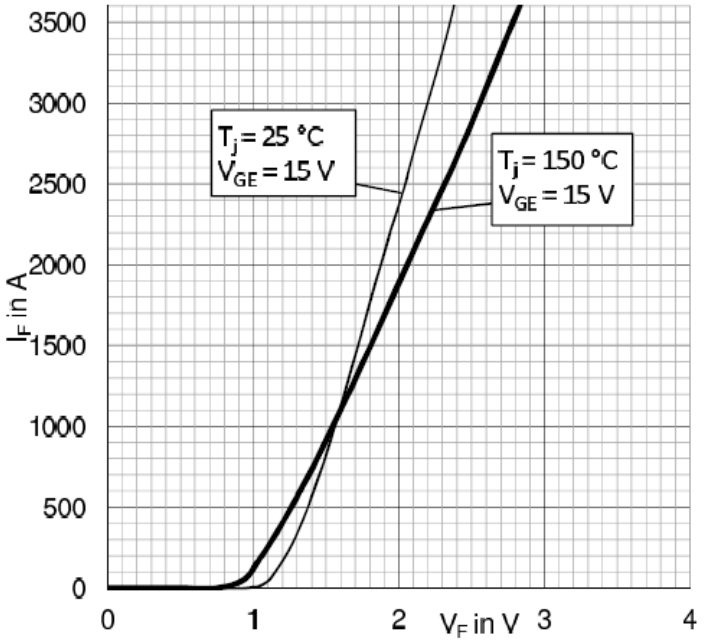


Figure 6-5: U_F versus I_F curves of SKiiP2414GB17E4-4DUW [84]

Table 6-3: Parameters of conduction losses

Parameter	Value
U_{CE}	1.05 V
R_{CE}	0.65875 mΩ
U_F	1.05 V
R_F	0.533 mΩ

For the switching losses calculation, the energy losses versus current curves of the SKiiP2414GB17E4-4DUW as shown in Figure 6-6 are referred. Three points are extracted from each curve (E_{on}+E_{off} curve and E_{rr} curve) and applied in the Polyfit function, which then generate the switching losses approximation expressed as:

$$E_{off} + E_{on} = \int_0^T \frac{U_{DC}}{1300}\left(0.119\, i^2(t) + 916.7\, i(t) - 35710\right)\cdot 10^{-6}\ \mathrm{d}t \tag{6.9}$$

$$E_{rr} = \int_0^T \frac{U_{DC}}{1300}\left(-0.005952\, i^2(t) + 158.3\, i(t) + 107100\right)\cdot 10^{-6}\ \mathrm{d}t \tag{6.10}$$

where U_{DC} is the DC voltage that the IGBT has to withstand when it is in the off-state. Eq. (6.9) is valid for the output current below 2500 A. As the curves are given for a specific voltage value (U_{cc}=1300 V), it is necessary to consider the real DC bus voltage of the converter. In order to remain conservative, the parameters of junction temperature at 150°C are used.

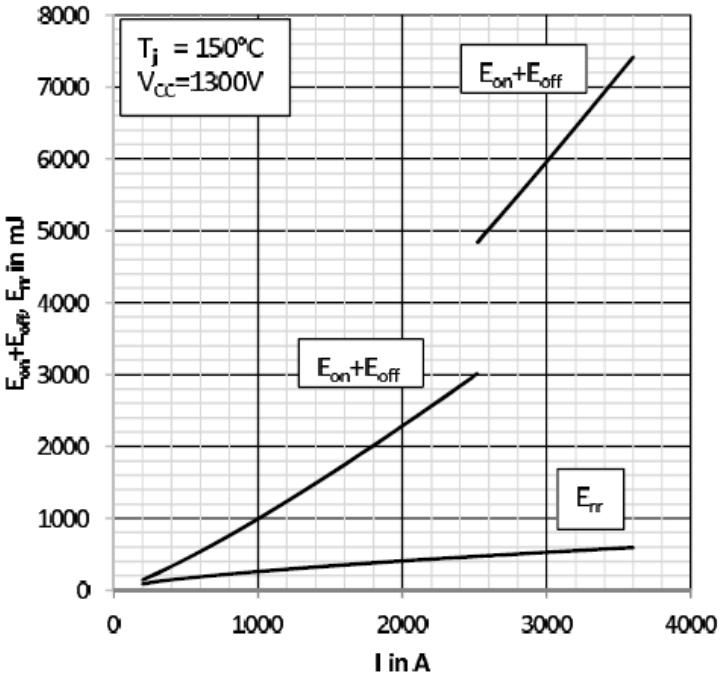


Figure 6-6: Turn-on and turn-off energy losses curves of SKiiP2414GB17E4-4DUW [84]

The switching losses fitting curves should be checked with the original curves to ensure they are accurate approximations. This checking is performed by placing the approximated curves obtained by Polyfit on the same graph of the manufacturer datasheet.

Using Eq. (6.3), (6.4) and Eq. (6.9), (6.10), the switching losses of an IGBT and a diode are calculated.

From the calculated conduction losses and switching losses of a single IGBT and diode, the total power losses of the two-level converter can be calculated. Since the power losses of the IGBT and the diode are distributed equally, the total power losses for the two-level converter can be expressed as:

$$P_{\text{totavg\_2L}} = \left(P_{\text{totavg\_T}} + P_{\text{totavg\_D}}\right) \cdot 6 \tag{6.11}$$

$$P_{\text{totmax\_2L}} = \left(P_{\text{totmax\_T}} + P_{\text{totmax\_D}}\right) \cdot 6 \tag{6.12}$$

6.3 Power losses in three-level NPC converter

In order to calculate the power losses of a three-level NPC converter, same as in the two-level converter, their operating principles including conduction paths and commutations are firstly explained. The different if compared to the two-level converter is that the power losses distribution in each IGBT and diode in the three-level NPC converter is unequal.

6.3.1 Conduction paths and commutations

The current paths for positive and negative phase currents are depicted in Figure 6-7. In zero switching state, the direction of phase current determines whether the upper or lower path of the neutral tap is utilized. Therefore, both T_{x2} and T_{x3} have to be turned-on in zero switching state "0" to provide an open path in case the phase current reverses. In any switching state, two semiconductors in series lie within the current path, either two IGBTs or two diodes for the positive "+" and negative "-" switching states. It should be noted that each of the switches must block only one-half of the DC-link voltage $u_{DC}/2$ assuming sinusoidal currents. The maximum IGBT/diode current is the maximum phase current. These parameters condition the rating of the main semiconductors. The distribution of the conduction losses is summarized in Table 6-4.

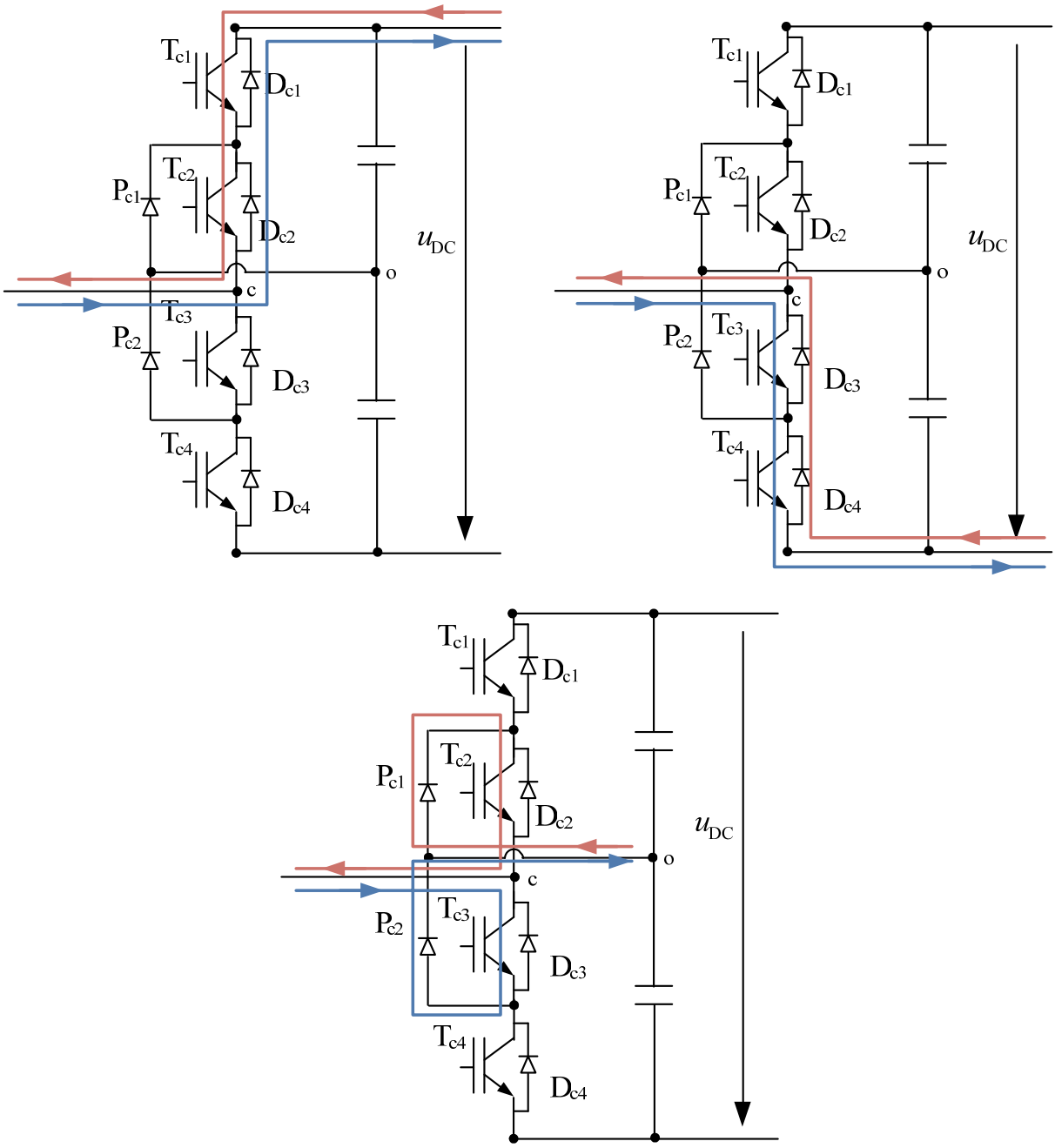


Figure 6-7: Conduction paths showing positive and negative current direction

Table 6-4: Devices that generate conduction losses in three-level NPC converter

Switching states	T_{x1}	D_{x1}	T_{x2}	D_{x2}	T_{x3}	D_{x3}	T_{x4}	D_{x4}	P_{x1}	P_{x2}
Positive phase current										
"+"	x		x							
"0"			x						x	
"–"						x		x		
Negative phase current										
"+"		x		x						
"0"					x					x
"–"					x		x			

Switching losses are generated by the commutation processes between the different switching states. For a positive phase current, the commutation from "+" towards "–" (+ → 0 → –) is named "forced commutation". The contrary natural commutation (– → 0 → +) realizes a positive output power gradient. They are initiated by an active turn-on transient.

For the following discussion of commutations, a positive phase current is assumed. Only turn-on and turn-off losses of IGBTs and recovery losses of diodes are considered. For a positive phase current, the commutation (+ → 0) is initiated by the turn-off of T_{x1} and the current is forced from T_{x1} to P_{x1}. After a dead time (to ensure that T_{x1} has completely turned-off), T_{x3} is turned-on. The switches T_{x2} and T_{x4} stay on and off, respectively.

Only one IGBT and diode are involved in this commutation, that is T_{x1} and P_{x1}. Essential turn-off losses occur in T_{x1}. Though the switch T_{x3} is turned-on, it does not experience losses since it does not take over any current after the commutation.

For the reverse commutation (0 → +), all switching transitions take place in the reverse order. T_{x3} is turned-off first, followed by turning on T_{x1} after the dead time. Turning off T_{x1} does not affect the phase current. It only returns to the positive rail after the turn-on of T_{x1}. Recovery losses occur in P_{x1}, and T_{x1} experiences turn-on losses. The situation for this pair of commutations is visualized in Figure 6-8a, where the current path of the switching active device is marked bold and the current path of the switching passive device is marked with a dashed line. The loss devices are encircled.

Four devices are involved in the commutation (0 → –) (Figure 6-8b). It is started by the active turn-off of the T_{x2}, forcing the current from its path through P_{x1} and T_{x2} to D_{x4} and D_{x3}. T_{x3} has already been in the on-state before; T_{x4} is turned-on after a dead time. T_{x2} faces turn-off losses.

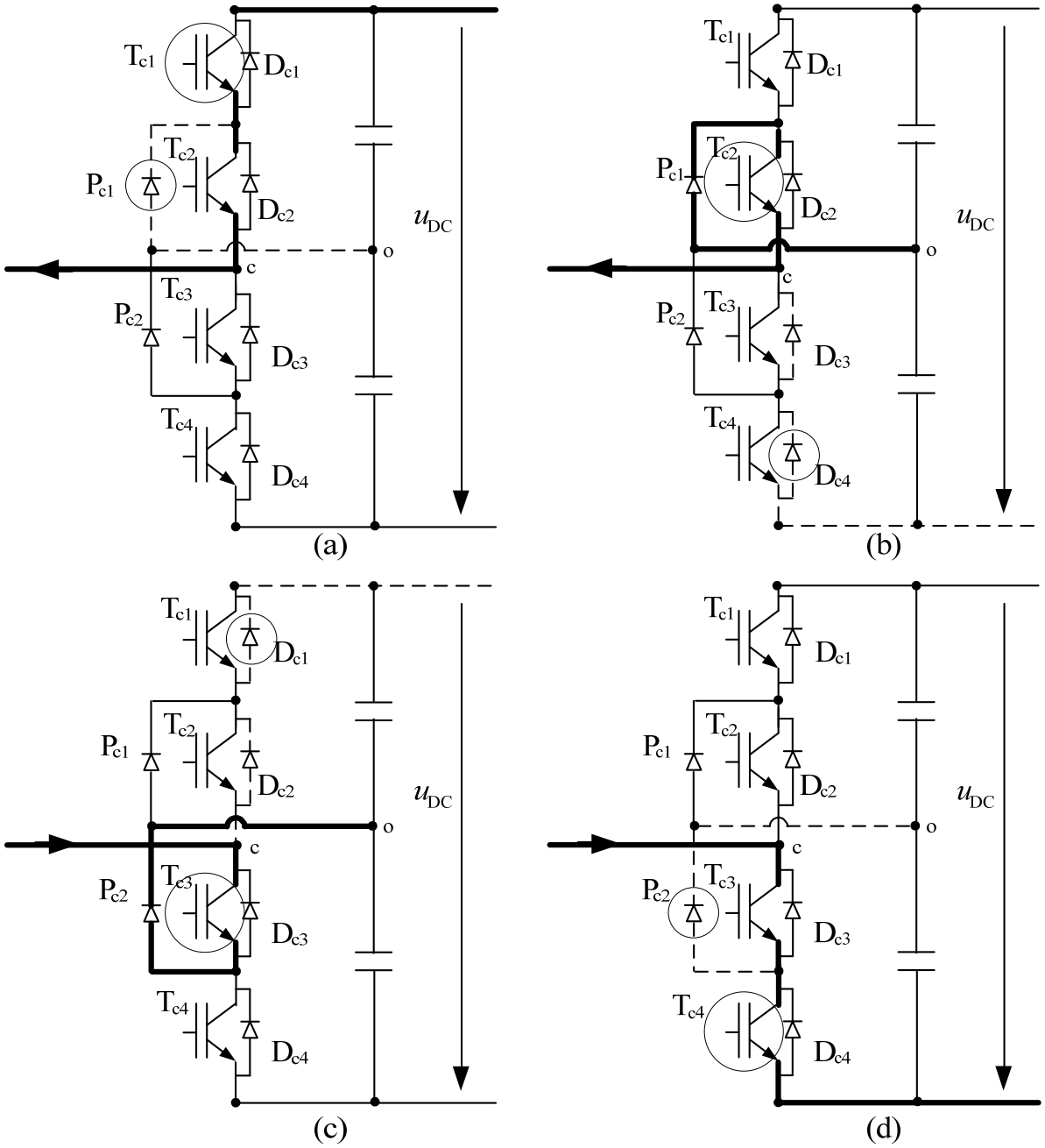


Figure 6-8: Commutations and switching losses of three-level NPC converter. (a) and (b) for positive load current, (c) and (d) for negative load current

Although the diode P_{x1} in series with T_{x2} is turned-off too, it does not experience notable recovery losses since it does not take over voltage after the commutation. Again, for the reverse commutation ($- \rightarrow 0$), all switching transitions take place in the reverse order. T_{x4} is turned-off, and T_{x2} is turned-on after a dead time. After triggering T_{x2}, the phase current commutates from D_{x4} and D_{x3} back to P_{x1} and T_{x2}. Both diodes in series D_{x4} and D_{x3} are turned-off, but only D_{x4} takes over blocking voltage.

Thus, only D_{x4} experiences recovery losses. T_{x2} faces turn-on losses. This situation is depicted in Figure 6-8b. The commutations at negative phase current are illustrated in Figure 6-8c and Figure 6-8d. The distribution of the switching losses is summarized in Table 6-5.

Table 6-5: Devices that generate switching losses in three-level NPC converter

Commutations	T_{x1}	D_{x1}	T_{x2}	D_{x2}	T_{x3}	D_{x3}	T_{x4}	D_{x4}	P_{x1}	P_{x2}
Positive phase current										
+ ↔ 0	x								x	
0 ↔ –			x					x		
Negative phase current										
+ ↔ 0		x			x					
0 ↔ –							x			x

The power losses of each semiconductor device in the three-level NPC converter are unequally distributed (as shown in Table 6-4 and Table 6-5). In half cycle of a fundamental pulse period, the power losses are contributed by five semiconductor devices, that is T_{x1}, D_{x1}, T_{x2}, D_{x2}, P_{x1} which also according to T_{x3}, D_{x3}, T_{x4}, D_{x4}, P_{x2}. Thus, conduction losses and switching losses of these five semiconductor devices have to be calculated separately.

6.3.2 IGBT module selection

The commutation voltage for the three-level NPC converter is half of the DC voltage. Thus, for the DFIG system used in this study, the commutation voltage becomes 550 V. As presented in the previous section, for the two-level converter, the 1700 V IGBT class has been considered. Theoretically, for the three-level NPC converter, 850 V IGBT class, that is half value of the IGBT in the two-level converter should be considered. However, this IGBT class is not commercially available. Thus, a higher IGBT class, 1200 V technology with 2400 A is proposed. Having the required ratings and regardless of the module structure, SKiiP2414GB12E4-4DUW [85] from Semikron manufacturer is selected for this study. The parameters for NPC diodes P_{x1}, P_{x2} are considered the same as the parameters of IGBT free-wheeling diodes. For the converter cost calculation, the price of SKiiP2414GB12E4-4DUW has to multiply by approx. two.

6.3.3 Power losses model

For the conduction losses calculation, the U_{CE} versus I_C curves and the U_F versus I_F curves of the SKiiP2414GB12E4-4DUW as shown in Figure 6-9 and Figure 6-10 are referred

(Appendix A.3). The worst case junction temperature of 150°C is considered and the gate voltage is selected as 15 V. The necessary values extracted from the curves are given in Table 6-6. Using Eq. (6.1) and Eq. (6.2) and the obtained values from Table 6-6, the conduction losses of IGBTs (T_{x1}, T_{x2}) and diodes (D_{x1}, D_{x2}, P_{x1}) are calculated.

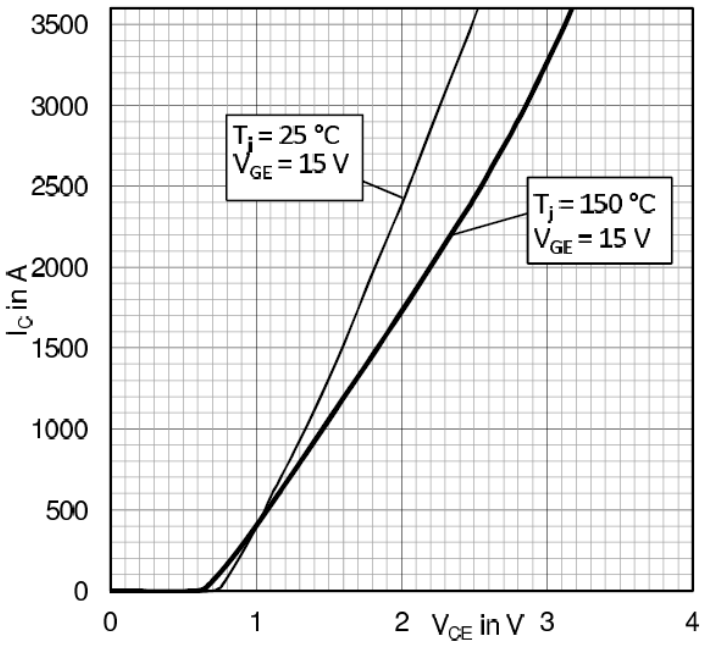


Figure 6-9: U_{CE} versus I_C curves of SKiiP2414GB12E4-4DUW [85]

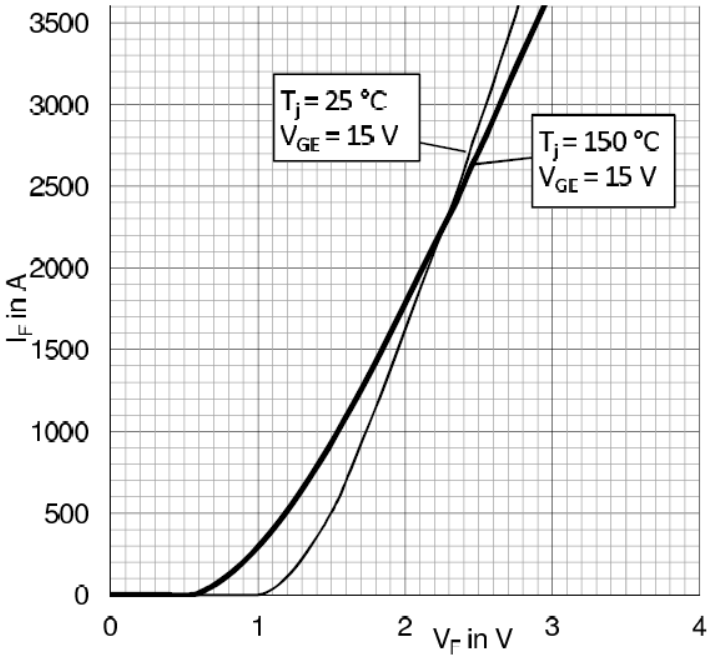


Figure 6-10: U_F versus I_F curves of SKiiP2414GB12E4-4DUW [85]

Table 6-6: Parameters of conduction losses

Parameter	Value
U_{CE}	0.8 V
R_{CE}	0.6818 mΩ
U_F	1.0 V
R_F	0.5417 mΩ

For the switching losses calculation, the energy losses versus current curves of the SKiiP2414GB12E4-4DUW as shown in Figure 6-11 are referred. Three points are extracted from each curve (E_{on}+E_{off} curve and E_{rr} curve) and applied in the Polyfit function, which then generate the switching losses approximation expressed as:

$$E_{off} + E_{on} = \int_0^T \frac{U_{DC}}{900}\left(0.04444\, i^2(t) + 604.4\, i(t) - 38890\right)\cdot 10^{-6}\ \mathrm{d}t \tag{6.13}$$

$$E_{rr} = \int_0^T \frac{U_{DC}}{900}\left(-0.001587\, i^2(t) + 47.78\, i(t) + 70630\right)\cdot 10^{-6}\ \mathrm{d}t \tag{6.14}$$

where U_{DC} is the DC voltage that the IGBT has to withstand when it is in the off-state.

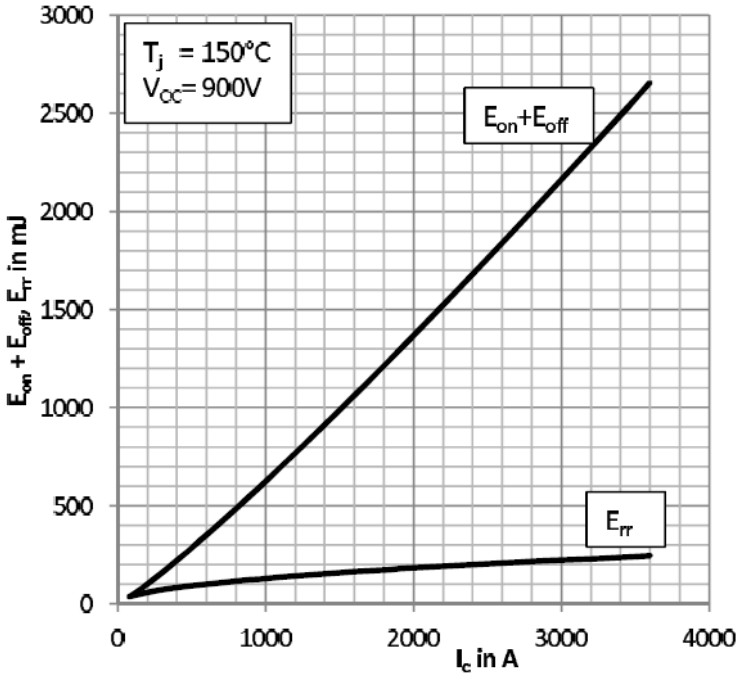


Figure 6-11: Turn-on, turn-off energy losses curves of SKiiP2414GB127E4-4DUW [85]

As the curves are given for a specific voltage value (U_{cc}=900 V), it is necessary to consider the real DC bus voltage of the converter. In order to remain conservative, the parameters of junction temperature at 150°C are used.

The switching losses fitting curves should be checked with the original curves to ensure they are accurate approximations. This checking is performed by placing the approximated curves obtained by Polyfit on the same graph of the manufacturer datasheet.

Using Eq. (6.3), (6.4) and Eq. (6.13), (6.14), the switching losses of IGBTs (T_{x1}, T_{x2}) and diodes (D_{x1}, D_{x2}, P_{x1}) are calculated.

From the calculated conduction losses and switching losses of IGBTs (T_{x1}, T_{x2}) and diodes (D_{x1}, D_{x2}, P_{x1}), the total power losses of the three-level NPC converter can be calculated. Assuming that the three-phase AC currents are sinusoidal and symmetrical, the total power losses of the three-level NPC converter can be given as:

$$P_{\text{totavg\_3L}} = \left(P_{\text{totavg\_T1}} + P_{\text{totavg\_T2}} + P_{\text{totavg\_D1}} + P_{\text{totavg\_D2}} + P_{\text{totavg\_P1}}\right) \cdot 6 \tag{6.15}$$

$$P_{\text{totmax\_3L}} = \left(P_{\text{totmax\_T1}} + P_{\text{totmax\_T2}} + P_{\text{totmax\_D1}} + P_{\text{totmax\_D2}} + P_{\text{totmax\_P1}}\right) \cdot 6 \tag{6.16}$$

6.4 Thermal analysis of converters

After the development of the power losses model of both converters, the next step is to develop their thermal model. The thermal model is necessary to derive junction temperature equations of IGBT and diode in the converter.

The generated power losses in the IGBT/diode contribute to existence of their junction temperature which could limit output current flowing through the IGBT/diode. This effect mainly occurs in the machine side converter (MSC) of the DFIG especially around synchronous speed (low frequencies) [86]. Therefore, it is necessary to analyze the thermal model in order to define the performance of the DFIG in terms of output power capability.

The thermal model of the IGBT and diode are firstly developed referring to the manufacturer application manual and datasheets. Once the thermal model is defined, a mathematical model representation of the system is derived and solved. The mathematical model is then implemented in the Matlab/Simulink model.

6.4.1 Thermal model of IGBT module

The first step in thermal modeling of an IGBT/diode is to characterize the system. Although a more detailed system model is a ninth order system, the manufacturer has stated and showed that the thermal response of the IGBT and diode can be approximated by the solution of a fourth order system [87].

The data necessary to represent the fourth order approximation of the system is provided in the manufacturer datasheet. Each fourth order system from a thermal stand point can be characterized as a fourth order R||C load which represent the thermal impedance Z_{thjs} between

junction and heat sink, as seen in Figure 6-12. This thermal equivalent circuit is also known as the Foster model [83], [87]-[91].

The manufacturer thermal model in the application notes makes some notable assumptions. First, the temperature drop from the case of the IGBT module to the heat sink is neglected due to SkiiP technology. In this technology, electrical main and auxiliary terminals are not soldered to insulated ceramic substrate but pressed. The insulated ceramic substrate is pressed to the heat sink. Second, the thermal coupling between the IGBT and the free-wheeling diode is neglected. Instead of coupling, the application notes inform the user to use the hottest modeled semiconductor device junction temperature to be the junction temperature (among semiconductor devices that generate half cycle of a fundamental pulse in a phase leg, as well as in three-level NPC converter). This assumption is made due to the semiconductor devices close proximity to each other.

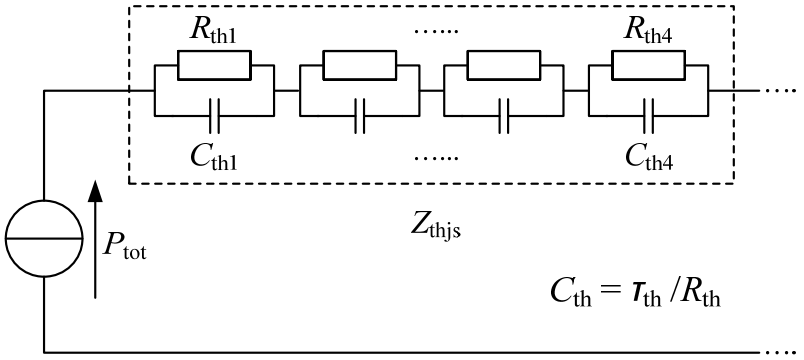


Figure 6-12: Foster model shows the simplified thermal model of IGBT and diode. Thermal impedance between the junction temperature and the heat sink [88]

6.4.2 Junction temperature for two-level converter

The thermal network of semiconductor devices which generate half cycle of a fundamental pulse in a phase leg for two-level converter is represented in Figure 6-13.

From the figure, the average junction temperature the IGBT and diode, under switching period, T_s can be calculated as:

$$T_{javg\_T} = T_S + P_{totavg\_T} \cdot Z_{thjs\_T} \tag{6.17}$$

$$T_{javg\_D} = T_S + P_{totavg\_D} \cdot Z_{thjs\_D} \tag{6.18}$$

where T_S is the heat sink temperature given as:

$$T_S = P_{totavg\_2L} \cdot Z_{thsa} + T_a \tag{6.19}$$

The thermal impedance between heat sink layer to ambient temperature of IGBT and diode are approximated as the same and represented as Z_{thsa}. T_a is the ambient temperature whose

variation depends on the temperature of the surroundings. In this study, the ambient temperature is assumed constant and taken as 65°C.

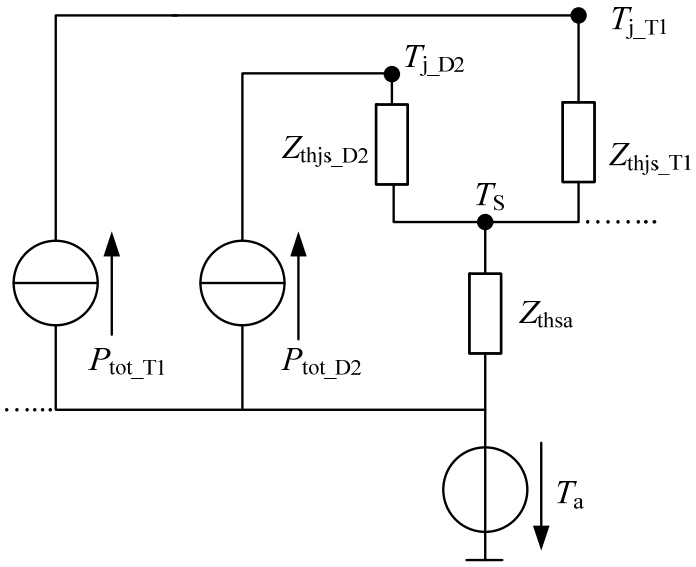


Figure 6-13: Thermal network model of IGBT diode pair in two-level converter [89]

To investigate the effect of junction temperature on the permissible output current of the converter, a maximum junction temperature of IGBT and diode have to be considered, and expressed as:

$$T_{jmax\_T} = T_S + P_{totmax\_T} \cdot Z_{thjs\_T} \tag{6.20}$$

$$T_{jmax\_D} = T_S + P_{totmax\_D} \cdot Z_{thjs\_D} \tag{6.21}$$

where the heat sink temperature is given as:

$$T_S = P_{totmax\_2L} \cdot Z_{thsa} + T_a \tag{6.22}$$

The thermal impedance values of the IGBT, diode and heat sink vary depending on the thermal resistance, time constant, total on-state time and pulse period, generally given as:

$$Z_{thjs\_T/\,D/thsa} = \sum_{i=1}^{n} R_{thi} \cdot \frac{\left(1 - \exp\left(-\frac{T}{\tau_{thi}}\right)\right)}{\left(1 - \exp\left(-\frac{T_S}{\tau_{thi}}\right)\right)} \tag{6.23}$$

Where T=T_S for average value calculation and T=t_{on} for maximum value calculation. The thermal resistances, R_{th} and time constant, τ_{th} of the IGBT, diode and heat sink are obtained from the manufacturer datasheet [84] and shown in Table 6-7. Figure 6-14 shows example of the thermal impedance characteristics of IGBT, calculated from Eq. (6.23) for different duty cycles, D=t_{on}/T_S. At the same duty cycle, the increase in turn-on time causes higher thermal impedance which leads to a higher junction temperature.

Table 6-7: Thermal parameters of IGBT, diode and heat sink in SKiiP2414GB17E4-4DUW

	R_{th} [K/W]				
	1	2	3	4	5
Z_{thjs_T}	0.0010	0.0049	0.0055	0.0017	0.0007
Z_{thjs_D}	0.0020	0.0100	0.0112	0.0034	0.0015
Z_{thsa}	0.0014	0.0050	0.0001	-	-
	τ_{th} [s]				
	1	2	3	4	5
Z_{thjs_T}	3.6500	0.4100	0.0650	0,0090	0.0008
Z_{thjs_D}	3.6500	0.4100	0.0650	0,0090	0.0008
Z_{thsa}	34.2609	5.2284	0.0005	-	-

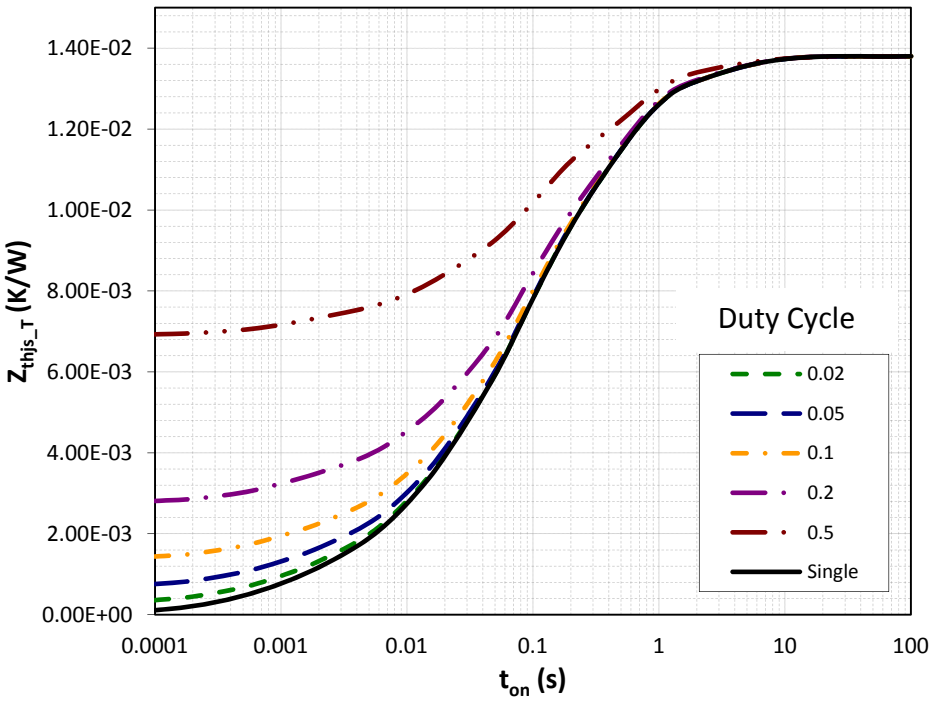


Figure 6-14: Thermal impedance characteristics of IGBT at different value of duty cycle in SKiiP2414GB17E4-4DUW

6.4.3 Junction temperature for three-level NPC converter

The thermal network of semiconductor devices which generate half cycle of a fundamental pulse in a phase leg for three-level NPC converter is represented in Figure 6-15.

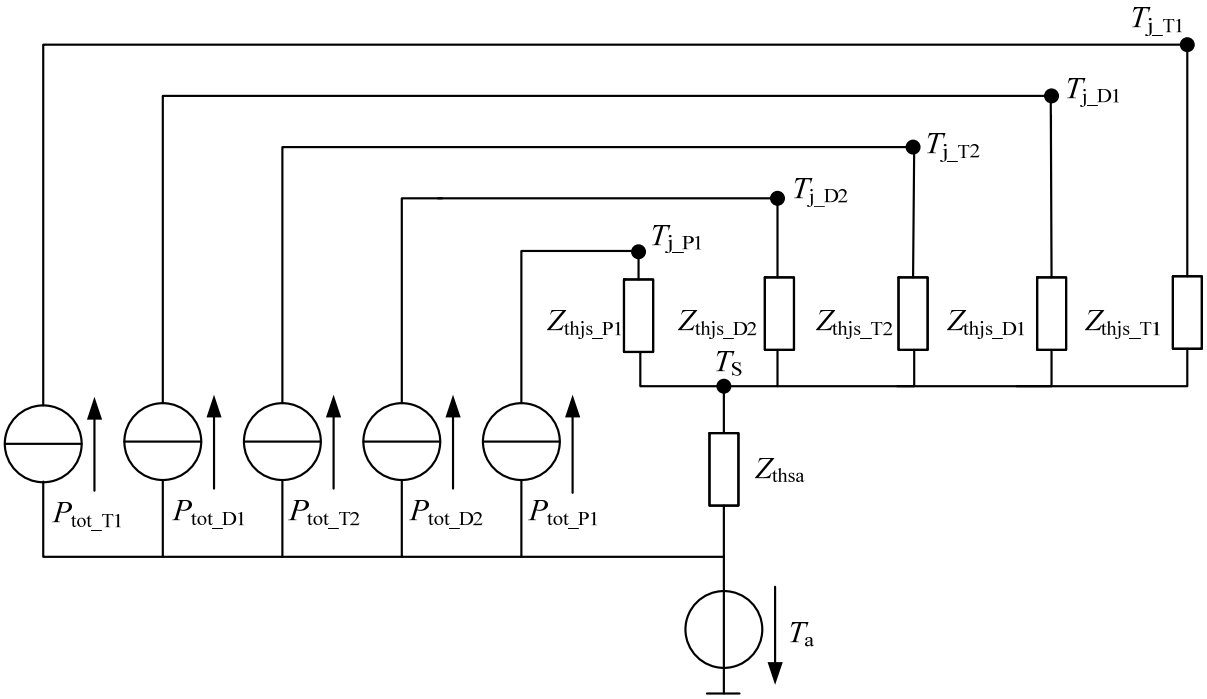


Figure 6-15: Thermal network model of T_1, D_1, T_2, D_2, P_1 in three-level NPC converter

From the figure, the average and maximum junction temperature of each semiconductor device for the three-level NPC converter are expressed as follow.

Average junction temperature:

$$T_{javg\_T1} = T_S + P_{totavg\_T1} \cdot Z_{thjs\_T1} \tag{6.24}$$

$$T_{javg\_D1} = T_S + P_{totavg\_D1} \cdot Z_{thjs\_D1} \tag{6.25}$$

$$T_{javg\_T2} = T_S + P_{totavg\_T2} \cdot Z_{thjs\_T2} \tag{6.26}$$

$$T_{javg\_D2} = T_S + P_{totavg\_D2} \cdot Z_{thjs\_D2} \tag{6.27}$$

$$T_{javg\_P1} = T_S + P_{totavg\_P1} \cdot Z_{thjs\_P1} \tag{6.28}$$

where the heat sink temperature is given as:

$$T_S = P_{totavg\_3L} \cdot Z_{thsa} + T_a \tag{6.29}$$

Maximum junction temperature:

$$T_{jmax\_T1} = T_S + P_{totmax\_T1} \cdot Z_{thjs\_T1} \tag{6.30}$$

$$T_{jmax\_D1} = T_S + P_{totmax\_D1} \cdot Z_{thjs\_D1} \tag{6.31}$$

$$T_{jmax\_T2} = T_S + P_{totmax\_T2} \cdot Z_{thjs\_T2} \tag{6.32}$$

$$T_{jmax\_D2} = T_S + P_{totmax\_D2} \cdot Z_{thjs\_D2} \tag{6.33}$$

$$T_{jmax\_P1} = T_S + P_{totmax\_P1} \cdot Z_{thjs\_P1} \tag{6.34}$$

where the heat sink temperature is given as:

$$T_S = P_{\text{totmax\_3L}} \cdot Z_{\text{thsa}} + T_a \tag{6.35}$$

The thermal impedance values of the IGBT, diode and heat sink can be derived as in Eq. (6.23). The thermal parameters used for the three-level NPC converter are obtained from the manufacturer datasheet [85] and shown in Table 6-8.

Table 6-8: Thermal parameters of IGBT, diode and heat sink in SKiiP2414GB12E4-4DUW

	R_{th} [K/W]				
	1	2	3	4	5
$Z_{\text{thjs\_T}}$	0.0011	0.0057	0.0063	0.0019	0.0009
$Z_{\text{thjs\_D}}$	0.0020	0.0100	0.0112	0.0034	0.0015
Z_{thsa}	0.0014	0.0050	0.0001	-	-
	τ_{th} [s]				
	1	2	3	4	5
$Z_{\text{thjs\_T}}$	3.6500	0.4100	0.0650	0,0090	0.0008
$Z_{\text{thjs\_D}}$	3.6500	0.4100	0.0650	0,0090	0.0008
Z_{thsa}	34.2609	5.2284	0.0005	-	-

As explained in the previous section, the power losses distribution in the three-level NPC converter is unequal. This also yields an unequal junction temperature distribution among the semiconductor devices. Some devices become hot, whereas others stay much cooler at the same time. The junction temperature in the most stressed device limit the permissible output current as well as the output power of the converter.

It has been observed that the power losses distribution is most unbalanced at certain operating points depending on the modulation index, m and the power factor, pf [3], [92]. For example, the most stressed (highest losses) devices at maximum modulation index and power factor pf =1 are the outer IGBTs. While during very small modulation index and pf = 1, the NPC diodes are the most stressed devices. Table 6-9 shows the critical operating points for the thermal design of the semiconductor devices.

Therefore, for the performance study of the converter output power capability, the calculation for power losses and junction temperature are based on the most stressed semiconductor device in one fundamental pulse period, which can be figured out during simulation.

Table 6-9: Critical operating points for thermal design of semiconductor devices [3]

Operating point	Technical characteristics		Device with T_{jmax}
	$pf = cos\ \varphi$	m	
OP1	1	1.0	Outer IGBTs
OP2	-1	1.0	Free-wheeling diodes of outer IGBTs
OP3	1	0	NPC diodes
OP4	-1	0	Inner IGBTs

7 Performance Evaluation of DFIG based Wind Turbines

According to the main objective of this thesis, which is to investigate and evaluate the performances of DFIG based wind turbines, two different cases are presented that

- using different PWM types in two-level converter
- using different converter topologies

In each case, the performances in terms of generated common mode voltage, current harmonics distortion level, power losses and reactive power capability will be analyzed and appropriate solution will be discussed.

7.1 Performance indexes

Performance indexes that contribute to the evaluation of DFIG based WT include generated common mode voltage at output of machine side converter (MSC), current total harmonic distortion in the low voltage network, converter power losses and reactive power capability which will be described in the next sections. These performance indexes are generally dependent on the converter topology and modulation technique.

7.1.1 Generated common mode voltage

The control of the IGBTs in a converter is employed by pulse width modulation (PWM) to achieve variable voltage and variable frequency output from a fixed DC bus voltage. By applying PWM in three-phase converter, a voltage will be generated between neutral point of the load and the ground which is known as common mode voltage (CMV). Figure 7-1 shows the generated CMV indicated as u_{no_conv} in MSC of DFIG system.

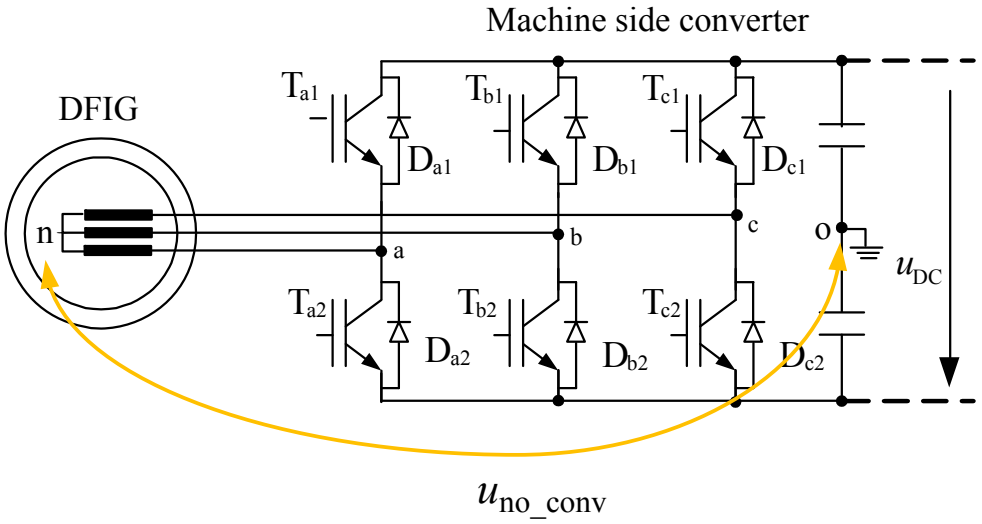


Figure 7-1: Generated common mode voltage in MSC of DFIG

The generated CMV can be expressed as Eq. (5.15). The equation shows that the output voltage of the converter is not sinusoidal. The generated CMV waveform is similar to the PWM pulse pattern since it dependent on the switching states of the converters (Table 5-3 for two-level and Table 5-5 for three-level NPC), which have been described in chapter 5. The frequency is equal to the switching frequency.

In general, only the line side current is required to be sinusoidal to satisfy IEEE standards. *LC* filters are used to damp the harmonics in pulse shape waveform and convert it to sine waveform. Therefore, the output waveform at line side converter (LSC) is sinusoidal and the generated CMV is not injected into the grid side due to transformer vector group which is in delta connection. However, since rotor circuit is not equipped with any filter, the output waveform at the MSC is not sinusoidal and the generated CMV has to be reduced to a certain level.

This generated CMV acts as a source for many unwanted problems in motor drives such as shaft voltage and bearing current due to parasitic capacitances which exists in the structure of the machine [93]. The bearing current arises from the voltage built up across the bearing due to electro-static couplings between machine windings and machine shaft/frame causing randomly appearing bearing current spikes. These bearing currents lead to bearing material erosion known as pitting and fluting. This effect is obviously occurred in the DFIG based WT, where the MSC is connected to the rotor windings compared with the stator-fed induction machine such as full-scale converter system. This is due to that the parasitic capacitances of the DFIG based WT can be more than ten times higher than in the case of stator-fed machine [94].

According to the analysis of [95], a high percentage of CMV generated by the MSC in a DFIG converts to shaft voltage. This amount is much greater than IEC-34-17 standard which is harmful phenomena and leads to bearing failures. Motor reliability studies have clarified that bearing failures account for about 40% of all motor failures [96].

7.1.2 Current total harmonic distortion

Current harmonics are virtually always present in the utility grid. Non-linear loads, power electronics loads, rectifiers and inverters in motor drives etc. are some sources which are producing harmonics. In the DFIG based WT, harmonic distortion can be produced by LSC and MSC and injected into the grid during entire rotor speed operation whether in sub-synchronous speed, super-synchronous speed or synchronous speed. Harmonics flowing in distribution networks downgrade the quality of electrical power. This can have a number of

negative effects on operation of all electrical equipment like switchgear, relays that are the guards of power system, measurement equipment, and rotating machinery.

The performance of DFIG based WT and its power quality is assessed according to the national and international standard such as EN61000-2-4 and IEEE 519, with distortion limit between 6% - 8%. The harmonics distortion can be quantified by several different methods. One of the methods is the individual harmonic distortion. Another most common method is total harmonic distortion (*THD*). The *THD* of the current in percent is defined as [97]:

$$THD = \sqrt{\sum_{h=2}^{50}\left(\frac{I_h}{I_l}\right)^2} \cdot 100 \tag{7.1}$$

where I_h is the rms current harmonic of harmonic order h and I_l is the rms current of the fundamental component. In this simulation, the current *THD* is measured at low voltage grid (LV) of the DFIG system.

7.1.3 Converter power losses

In this thesis, only converter power losses (both LSC and MSC) are taken into account. Losses in feeder cables, auxiliary components, drives, and machine (copper and iron losses of stator and rotor) are neglected. The converter power losses are generated due to the IGBTs and diodes behavior during conduction and commutations (turn-on and turn-off).

The converter power losses are about 1% - 4% of the power transferred through the converter [86]. In DFIG based WT, at full load, the active power passing through the back-to-back converter amounts to roughly 25% of total power. Although the percentage of the converter power losses generation is very small, which generally may not affect the efficiency of the DFIG system, the power losses study is important for the converter thermal analysis. The thermal analysis could help in the intelligent design of a compact and effective cooling system (especially the heat sink design) that could improve IGBT lifetime and avoids IGBT earlier power cycling failures. Thus, it also helps in reducing the cost of the converter. Converter power losses data are also important for the determination of active-reactive power capability of the DFIG system.

The power losses calculation for two-level converter and three-level NPC converter has been derived in chapter 6. In order to have some validation on the proposed methodology, a comparison on the power losses and the junction temperature has been obtained. The results from SEMISEL simulation which is an online application powered by Semikron manufacturer are compared. The SEMISEL simulation allows simulating different topologies; however it has limitation which is using only one PWM type that is SPWM. Figure 7-2 shows the

comparison between the proposed methodology with Matlab/Simulink and SEMISEL simulation of average power losses and junction temperature using SPWM. From the figure, it c an be seen that both simulation results show almost the same value.

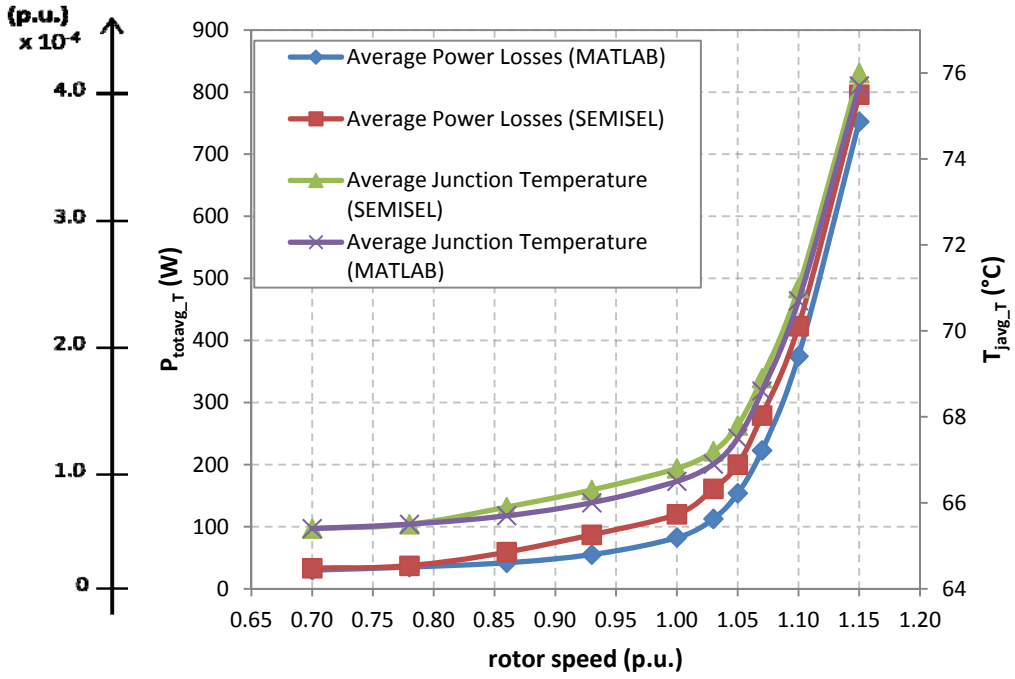


Figure 7-2: Average power losses and junction temperature of an IGBT in MSC using SPWM with Matlab/Simulink and SEMISEL simulation (for validation)

7.1.4 Reactive power capability

Converter power capability defines a converter's active and reactive power limits. For wind turbine manufacturers and/or operators, the converter power capability information is needed to assess whether their wind turbines can fulfill grid code reactive power requirements and to quantify how much their turbines and/or their wind power plants composed of these turbines can provide ancillary services such as reactive power support [98]. Figure 7-3 shows an example of two options of active power versus reactive power characteristics according to [99].

The option to be implemented depends on the particular location of the wind turbine within the grid. Currently, interest is focused on the extension of the reactive power generation range by a better utilization of the reactive power capability of the DFIG. As indicated in Figure 7-3 DFIG based WTs can supply reactive power even at zero active power.

The power capability information also can be incorporated with wind turbine controller design [86] and, thereby, with wind power plant controller design. Furthermore, transmission system operators request the power capability information from wind power plant operators in

order to model these plants and analyze their transmission system with these plants as they require power capability curves from conventional power generators.

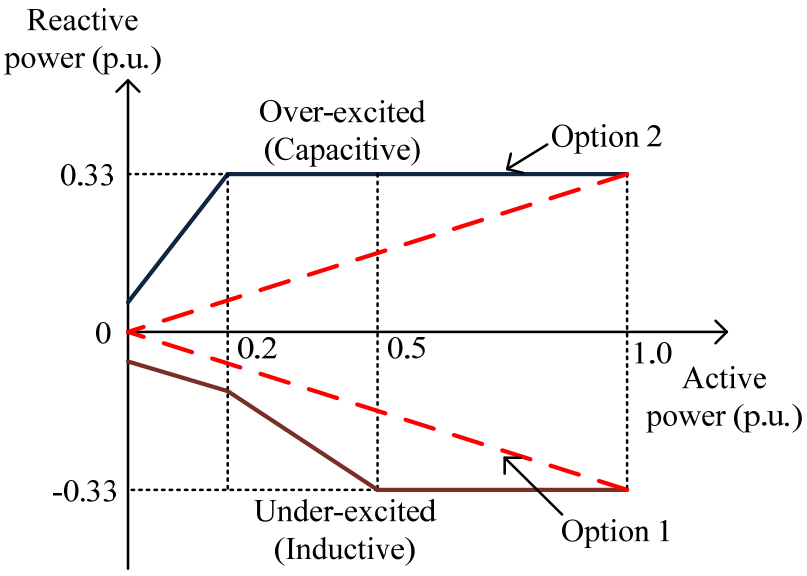


Figure 7-3: Reactive power characteristics of DFIG base wind turbines [99]

The power capability of WTs generator is subject to several limitations resulting from the voltage, current, and speed. Based on power system and generator technology, the power capability of conventional turbine generator is determined by field heating limit, end heating limit, stator heating limit, and steady state stability limit [100], [101]. For DFIG based WT, the power capability limiting factors are involved mechanical power, stator current and rotor current [86]. Figure 7-4 shows general overview of power capability limiting factors for DFIG based WT.

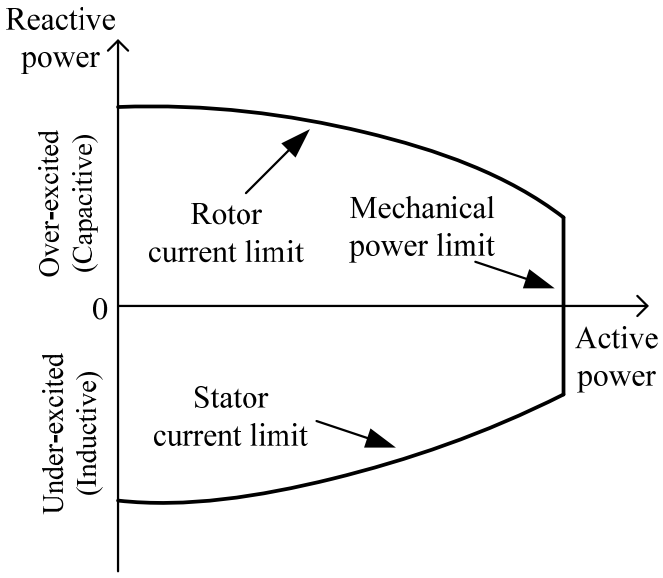


Figure 7-4: General overview of power capability limiting factors for DFIG based WT

Among the limiting factors, the rotor current limit has large affect to the power capability especially during the generator operation at around synchronous speed. Operation around synchronous speed puts a quite heavy load both in terms of frequency and current level on the MSC while the LSC is nearly unloaded. At these operating points, where frequencies of rotor voltages are at low level (below 5 Hz), the junction temperature of IGBTs and diodes in the MSC could exceed their maximum limit due to higher generated power losses. At these conditions, a current de-rating of MSC is necessary to maintain maximum junction temperature of IGBTs at about the same level as at the rated speed [86].

Reduction in the MSC current consequently reduces the output power of the MSC. As the MSC currents consist of active and reactive components, reduction of one component may be enough to limit the current magnitude by defining the priority in the control design. In this study, active current priority is defined in the MSC control. Therefore, the reactive current is reduced first, and the active current kept unchanged when the magnitude exceeds the limit. The MSC reactive current according to the MSC current limit $i_{\mathrm{MSC\_max}}$ is expressed as:

$$i_{\mathrm{MSC,q}} = \sqrt{i_{\mathrm{MSC\_max}}^2 - i_{\mathrm{MSC,d}}^2} \tag{7.2}$$

where $i_{\mathrm{MSC,d}}$ is the MSC active current in a reference frame aligned to the stator voltage.

In the LSC, the frequency of output voltage is always constant and equal to the frequency of grid voltage. The total rated current is at low level (about 0.21 p.u.) which will not cause high power losses generation. At such conditions, the IGBTs/diodes junction temperature will not exceed its limit. For typical DFIG based WT used in this thesis, the LSC current characteristic curves are plotted in Figure 7-5.

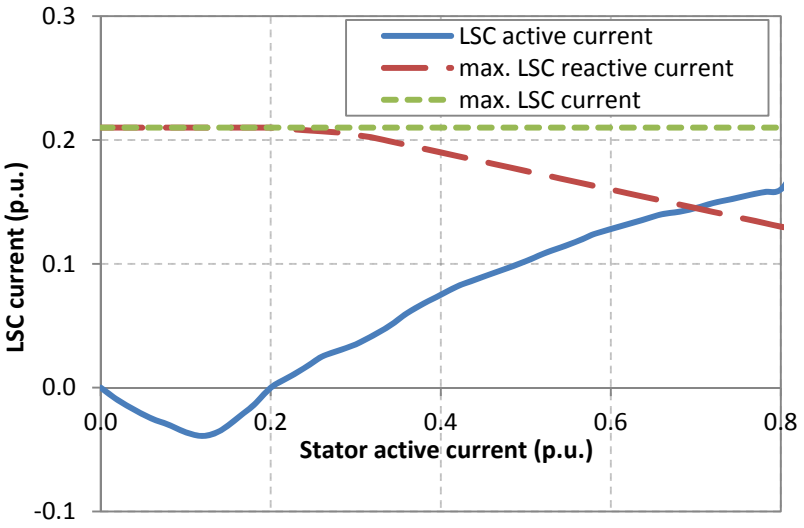


Figure 7-5: LSC current capability as a function of stator active current

The analytical equations for power output are derived from system equations of DFIG equivalent circuit (Eq. (3.23)-(3.26)) and can be expressed as [86], [102]:

$$p_{\mathrm{WTG}} = \mathrm{Re}\left\{\underline{u}_{\mathrm{S}}\,\underline{i}_{\mathrm{S}}^{*}\right\} + \mathrm{Re}\left\{\underline{u}_{\mathrm{LSC}}\,\underline{i}_{\mathrm{LSC}}^{*}\right\} \tag{7.3}$$

$$q_{\mathrm{WTG}} = \mathrm{Im}\left\{\underline{u}_{\mathrm{S}}\,\underline{i}_{\mathrm{S}}^{*}\right\} + \mathrm{Im}\left\{\underline{u}_{\mathrm{LSC}}\,\underline{i}_{\mathrm{LSC}}^{*}\right\} + q_{\mathrm{filter}} \tag{7.4}$$

$$q_{\mathrm{filter}} = \omega_{\mathrm{S}} c_{\mathrm{filter}} u_{\mathrm{S}}^{2} \tag{7.5}$$

where p_{WTG} and q_{WTG} are the active and reactive power of the DFIG, u_{S} and u_{LSC} are the complex stator and LSC voltages, and i_{S} and i_{LSC} are the complex stator and LSC currents, respectively. q_{filter} is the reactive power produced by the capacitor in the filter at LSC side.

In order to improve the reactive power capability at around synchronous speed, the basic idea is to have lower power losses in the converter. One approach is using a converter topology with low power losses performance. Another approach is using a low switching frequency of modulation technique. The performance of reactive power capability for these two approaches will be investigated in the next section.

7.2 Comparison between continuous PWM and discontinuous PWM

Different PWM types discussed in chapter 5 are applied for a 2 MW DFIG based wind turbine (WT) with back-to-back two-level converter. The main components of the DFIG were modeled throughout chapter 3 and its parameters are presented in Appendix A.1. Figure 7-6 shows the DFIG based WT system configuration used for the simulation. The system is running under steady state operation following the active power characteristic based on a manufacturer data and shown in Figure 7-7. A constant carrier frequency of 2250 Hz has been chosen for both CPWM and DPWM at both LSC and MSC. Thus, the filter at the LSC line is dimensioned with resonant frequency corresponding to the carrier frequency and double this value.

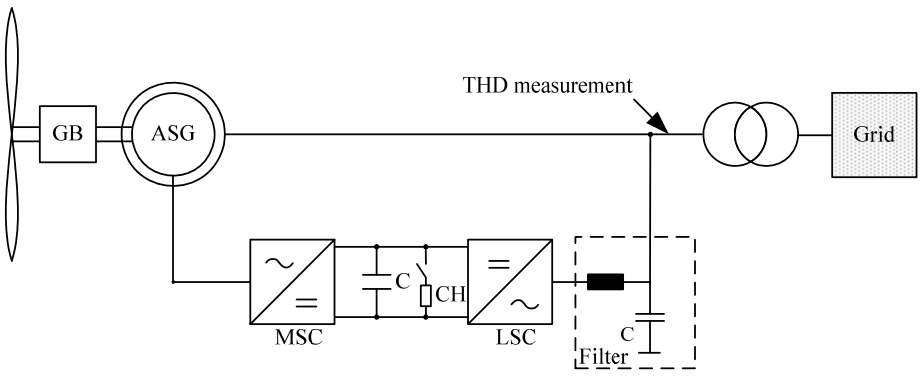


Figure 7-6: Test system of DFIG based WT

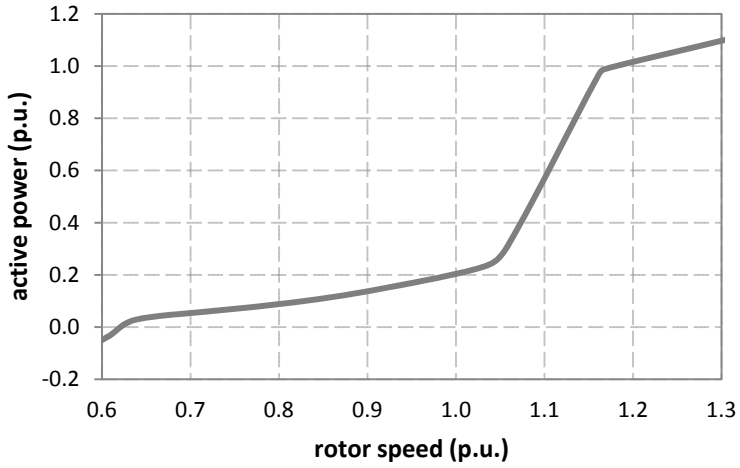


Figure 7-7: Active power characteristic of DFIG based WT used in the simulation

7.2.1 Performance analysis

Among the continuous PWM (CPWM) types, the TTHIPWM is selected which has the lowest harmonic distortion. While among the discontinuous PWM (DPWM) types, DPWM0, DPWM1 and DPWM2 are selected which have higher maximum switching losses reduction (up to 50%) compared with DPWM3, DPWMMAX and DPWMMIN. Table 7-1 shows the PWM type combinations for the back-to-back two-level converter that used for performance comparison study in this section.

Table 7-1: PWM type combinations for back-to-back two-level converter

Combination	For LSC	For MSC
1	CPWM	CPWM
2	CPWM	DPWM
3	DPWM	CPWM
4	DPWM	DPWM

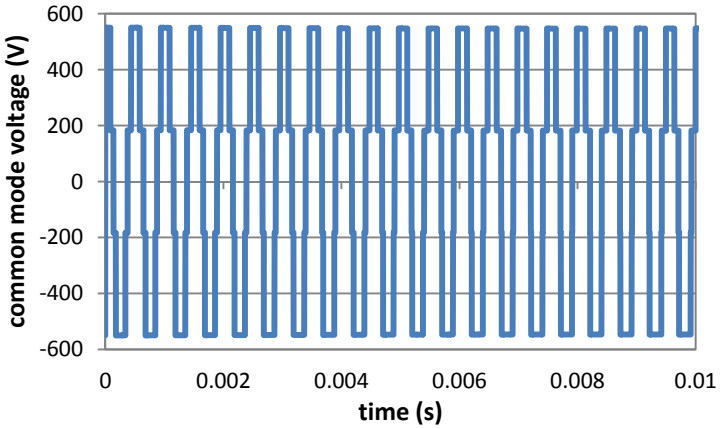
CPWM: TTHIPWM

DPWM: DPWM0, DPWM1, DPWM2

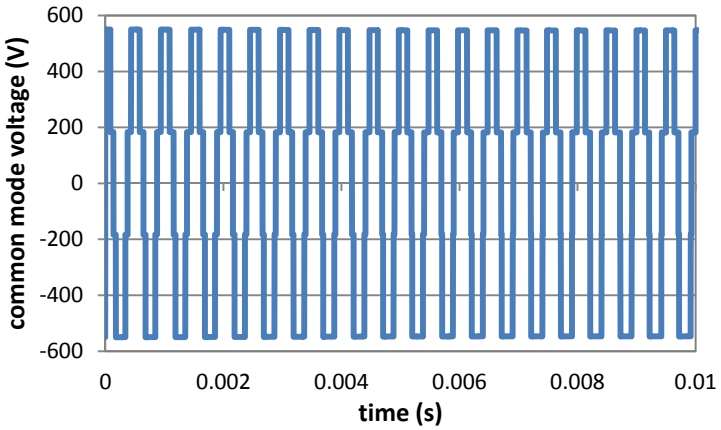
The four combinations shown in Table 7-1 are investigated in terms of generated common mode voltage, current total harmonic distortion, converter power losses and reactive power capability to have an idea on which combination is the most appropriate for LSC and MSC in the two-level converter of DFIG based WT.

7.2.1.1 Generated common mode voltage

As explained previously, the generated common mode voltage (CMV) at LSC is equal to zero. Therefore, any PWM types applying for LSC will not contribute to the generation of CMV. While at MSC, applying PWM will generate CMV. However, the generated CMV level is independent on the PWM types. Thus, any standard PWM types (either among CPWM or DPWM) generate the same level of CMV. Using Eq. (5.15), the generated CMV at MSC for the combination 1 and 2 (as examples) are shown in Figure 7-8.



(a) Combination 1



(a) Combination 2

Figure 7-8: Generated common mode voltage with different PWM types at MSC

Both figures show the same level of generated CMV at about 550 V. It can be concluded that the generated CMV for the back-to-back two-level converter is only generated in MSC and the voltage level is the same for any PWM types.

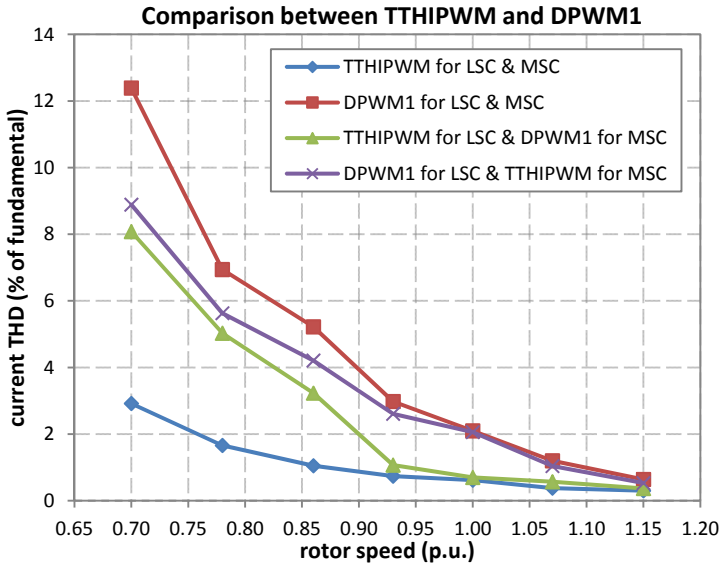
7.2.1.2 Current total harmonic distortion

The harmonics analysis considers a steady state operation during rotor speed operations of 0.70, 0.78, 0.86, 0.93, 1.00, 1.07 and 1.15 (in p.u. value) which is corresponding to the generated active power of 0.05, 0.08, 0.12, 0.16, 0.20, 0.38 and 0.90 (in p.u. value), respectively. These values are according to Figure 7-7. The measurement of current *THD* (phase a) is taken at low voltage grid using Matlab/Simulink tool of Fast Fourier Transform (FFT). The measurement point is shown in Figure 7-6.

Four combinations as stated in Table 7-1 are applied for the back-to-back two-level converter. Using Eq. (7.1), the current *THD* are obtained and shown in Figure 7-9.

When comparing the current *THD* between DPWM1, DPWM0 and DPWM2, it shows almost the same level. Later, these three PWM types are generalized as DPWM. TTHIPWM for LSC and MSC produced the lowest current *THD* while DPWM for LSC and MSC produced the highest current THD at all operation points. Applying either TTHIPWM or DPWM for MSC did not result a large different during synchronous and super-synchronous speed. However, during sub-synchronous speed TTHIPWM has to be applied for LSC and MSC.

The simulation results show that the injection of current harmonics into the grid is depending on the waveform quality. At lower rotor speed where the magnitude of rotor current is low, the waveform quality is the worst causing high current *THD* at the grid. Selecting TTHIPWM for LSC and MSC at this operation condition reduced the generation of current harmonics. At higher rotor speed, the generation of current harmonics is not as much as during lower speed operation. Thus, selecting either TTHIPWM or DPWM for both converters produced less current *THD* which is still lower than 8% limit required by the standard EN61000-2-4.



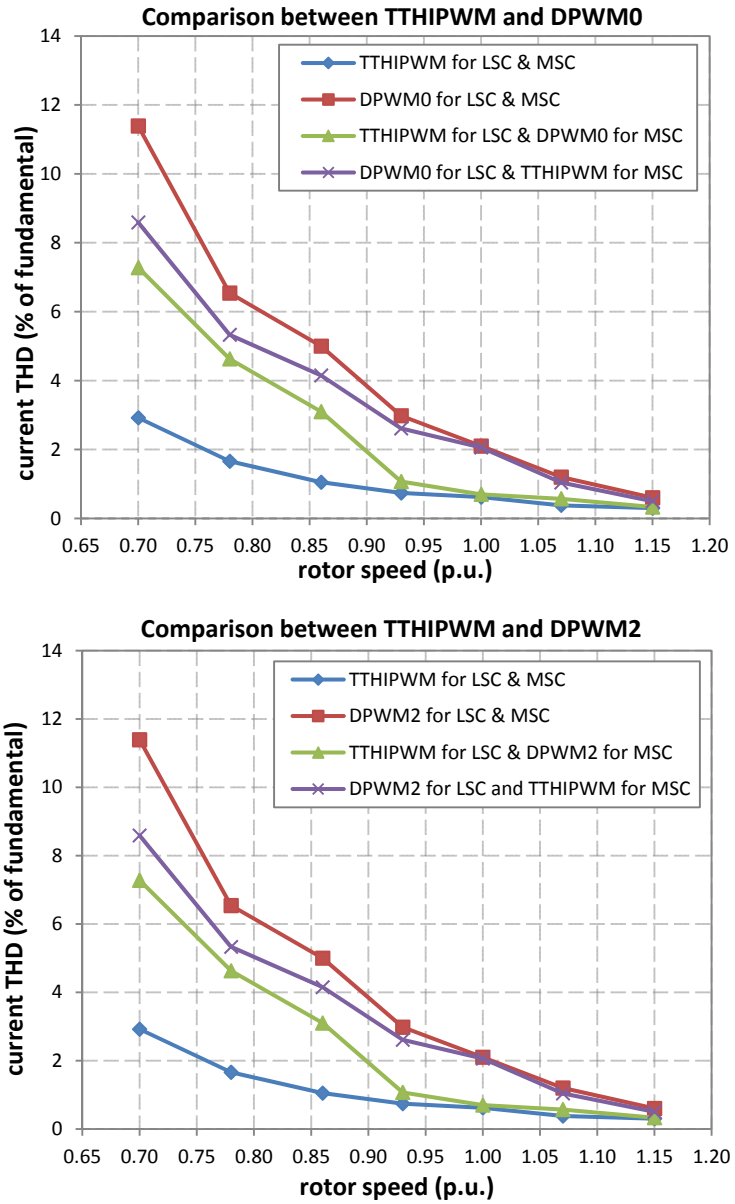


Figure 7-9: Current *THD* at different rotor speed operating points

It can be concluded that selecting CPWM for LSC and MSC (combination 1) significantly produced the lowest current *THD* injected into the grid at entire speed range of DFIG based WT.

7.2.1.3 Converter power losses

The converter power losses of both LSC and MSC are calculated during the same operating points as in the harmonics analysis. The four cases as in Table 7-1 are also applied for the back-to-back two-level converter. Using Eq. (6.11), the total power losses of MSC and LSC are calculated and shown in Figure 7-10.

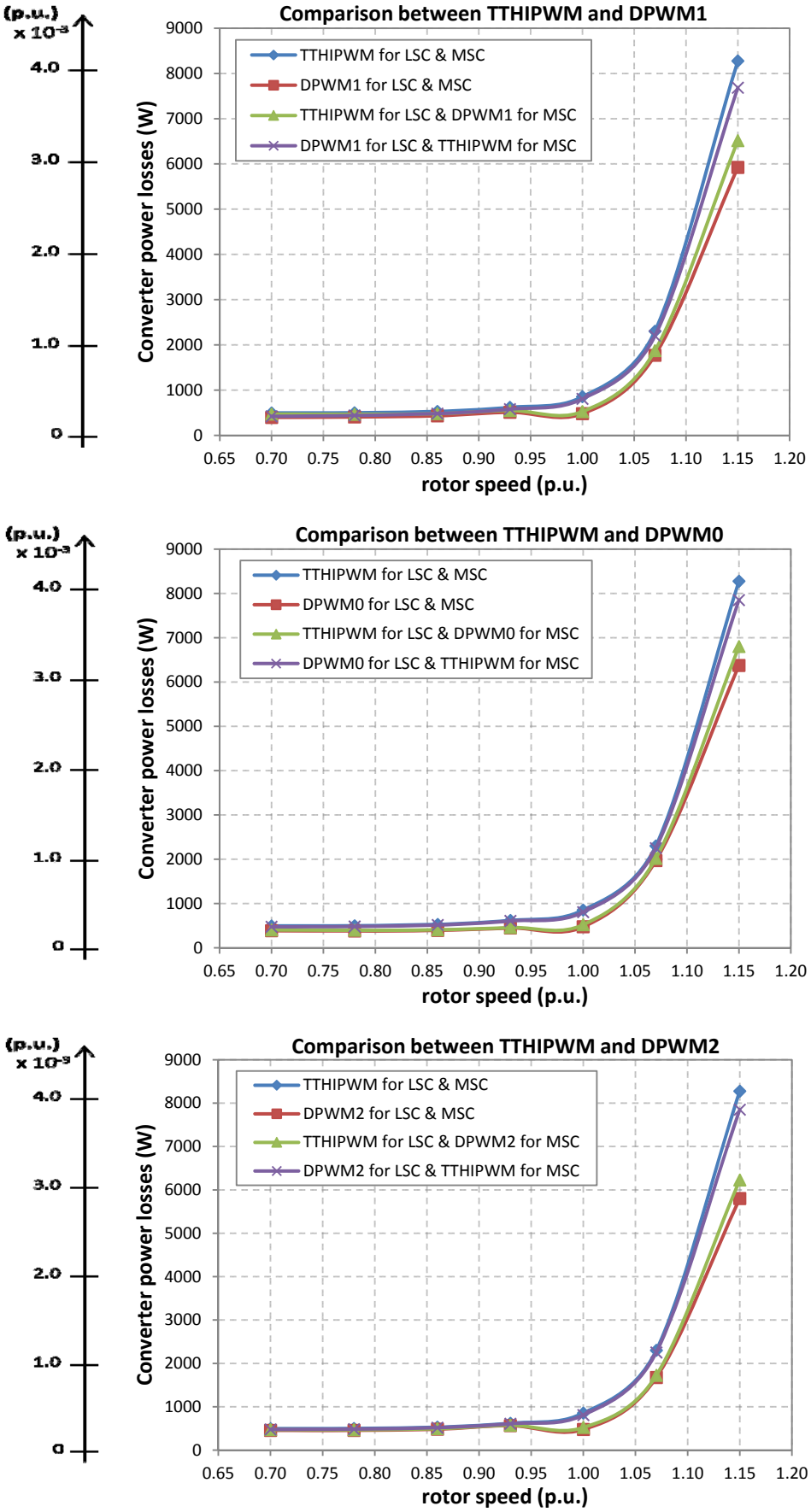


Figure 7-10: Power losses of back-to-back converter at different rotor speed operating points

In general, the simulations results show that all DPWM types applied for LSC and MSC produced the lowest power losses while TTHIPWM applied for LSC and MSC produced the highest power losses at all operation points. Since the ratio of LSC current over rotor current is small and frequency of LSC voltage is significantly larger than frequencies of MSC voltage, applying either TTHIPWM or DPWM for LSC did not show a large different. The power losses is mainly dependent on the rotor current magnitude, thus at higher speed operation, the power losses is at high level and reducing proportional with speed reduction.

Switching losses contribute the most losses in the total power losses and dependent on power factor. The rotor power factor is varying over the rotor speed operations. Therefore, the power losses in MSC are highly influenced by the DPWM types in different rotor speed operations. However, since the obtained power losses shown in the figures are the power losses of both MSC and LSC, thus the total generated power losses did not show a large different.

When comparing different DPWM types with TTHIPWM, applying DPWM0 for LSC and MSC during sub-synchronous speed produced the lowest power losses. However, this combination produced the highest power losses during super-synchronous speed. While applying DPWM2 for LSC and MSC during super-synchronous speed produced the lowest power losses. However, this combination produced the highest power losses during sub-synchronous speed.

It can be concluded that selecting DPWM for LSC and MSC (combination 4) significantly produced the lowest power losses at entire speed range of DFIG. When considering on compact design of power converters, this selection is the most preferable.

7.2.1.4 Reactive power capability

In reactive power capability study, the thermal analysis is investigated only in the MSC due to that the MSC current could exceed the IGBT junction temperature limit at low frequency of rotor voltage. The thermal analysis for different PWM types at LSC is not presented, only TTHIPMW is used. While for MSC, TTHIPWM and DPWM are applied. Thus, combination 1 and 2 as shown in Table 7-1 are selected in this simulation.

Using Eq. (6.20)-(6.23) and the simulated data of IGBT power losses, the maximum junction temperature of IGBT as a function of frequency of rotor voltage under a constant MSC output current can be expressed as shown in Figure 7-11. The results are related to the maximum permissible rotor current at rated speed with i_{MSC_max} = constant.

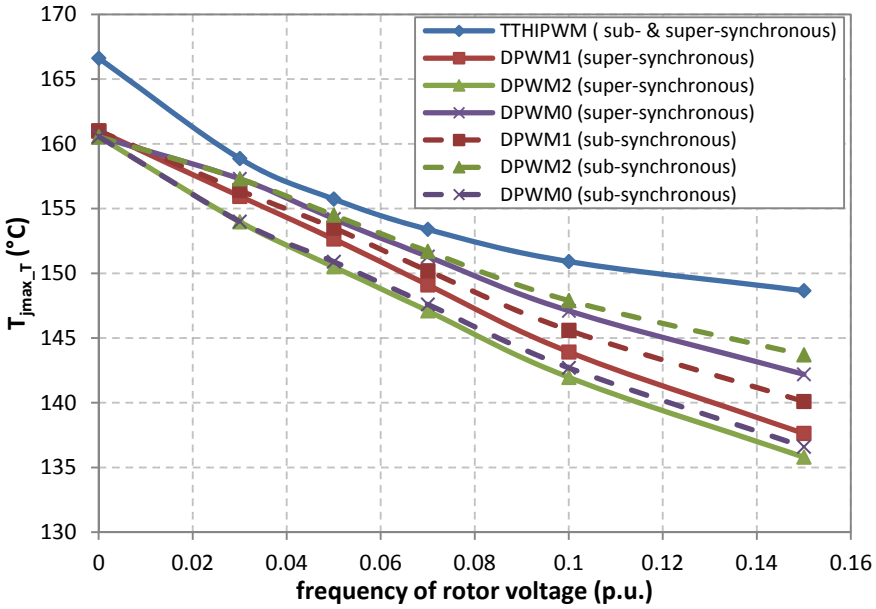


Figure 7-11: Maximum junction temperature of IGBT in MSC as a function of frequency of rotor voltage

From the figure, it can be found that the junction temperature is higher at lower frequencies of rotor voltage. During super-synchronous speed, the temperature exceeds its maximum limit of 150°C below the frequency of about 0.120 p.u. for TTHIPWM, 0.065 p.u. for DPWM1, 0.050 p.u. for DPWM2 and 0.080 p.u. for DPWM0. While during sub-synchronous speed, the junction temperature exceeds its maximum limit of 150°C below the frequency of about 0.120 p.u. for TTHIPWM, 0.070 p.u. for DPWM1, 0.080 p.u. for DPWM2 and 0.055 p.u. for DPWM0. At these conditions, the junction temperature has to be reduced to avoid IGBT failure and to increase IGBT lifetime by reducing the MSC output current. Thus, these data are necessary to characterize the maximum permissible output current of the MSC.

As explained previously, the MSC current de-rating is necessary to maintain the maximum junction temperature at about the same level as at the rated speed. In this simulation, the MSC output current is reduced to a certain value where it produces the junction temperature at maximum limit. Then, this current value is normalized to 1.11 p.u. value, which is the maximum MSC current rating. Figure 7-12 shows the maximum MSC output current in relation to frequency of rotor voltage. The diagram is corresponding to the pre-condition $T_{jmax} \leq (T_{jmax}$ at rated speed). Normally, the maximum junction temperature for the MSC output current rating shown in Figure 7-12 is much lower than 150°C to have some reserves for transient overload conditions during fault ride-through or over-speed.

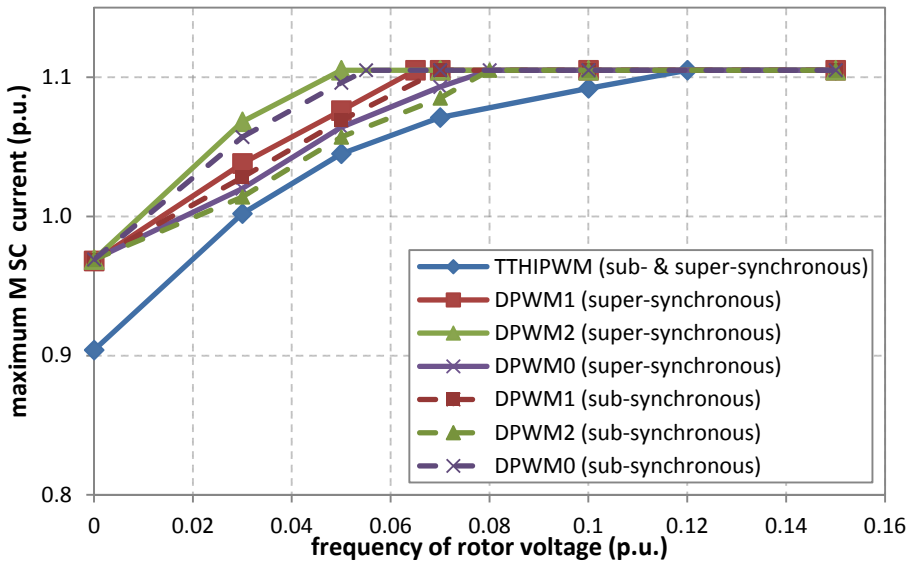


Figure 7-12: Maximum MSC output current in relation to frequency of rotor voltage

As the MSC currents consist of active and reactive components, as expressed in Eq. (7.2), reduction of one component may be enough to limit the current magnitude by defining the priority in the control design. In this simulation, active current priority is defined in the MSC control. Therefore, the reactive current is reduced first, and the active current kept unchanged when the magnitude exceeds the limit.

Figure 7-13 shows the stator reactive current as a function of active current at the rated MSC current with limitation considered in Figure 7-12 which also includes the magnetizing current. Positive reactive currents show the operation of DFIG during over-excited mode while negative reactive currents show the operation during under-excited mode.

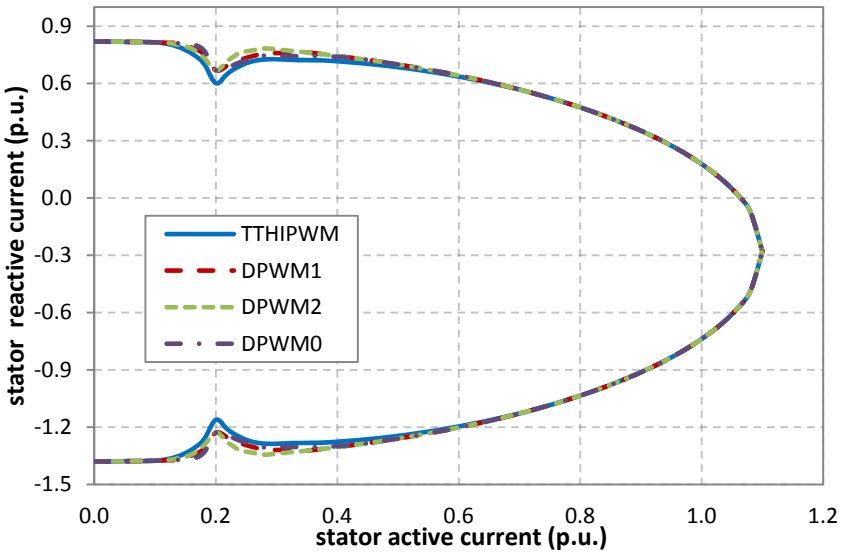


Figure 7-13: Stator reactive current capability at rated MSC current as a function of active current at nominal voltage

In order to obtain the active-reactive current capability of DFIG based WT, the stator and LSC reactive current capabilities have to be defined. For the stator reactive current capability, the stator current limitation due to heating limit, the rated MSC current limitation (as Figure 7-13) and the maximum rated stator active power have to be considered. The resulting stator reactive current capability is shown in Figure 7-14.

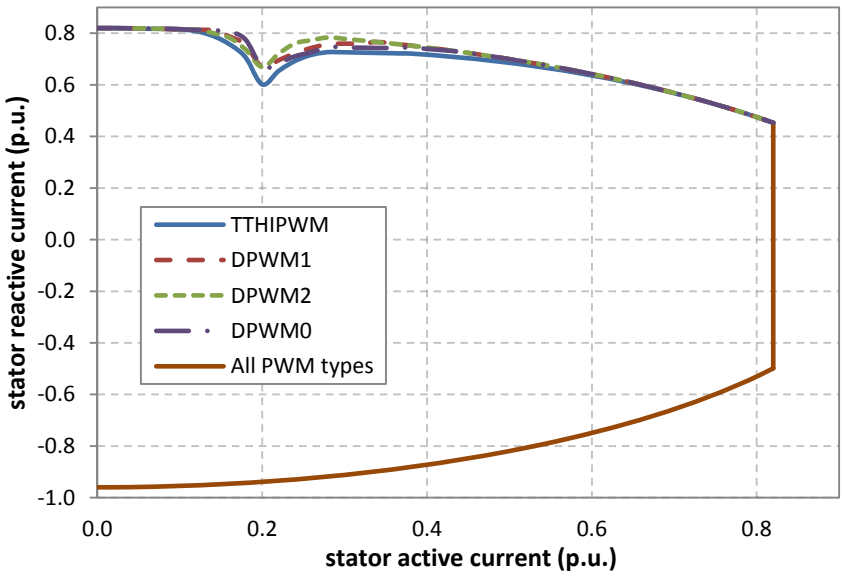


Figure 7-14: Stator reactive current capability as a function of active current at nominal voltage considering all limitations

For LSC reactive current capability, the limitation is set by the total rated current which has been explained in section 7.1.4. Combining the stator and LSC reactive current capability results in the reactive current capability of DFIG based WT. For analyzing the impact of different PWM types on the reactive current capability around synchronous speed, the DFIG reactive current capability is shown as in Figure 7-15, considering only operation during over-excited mode.

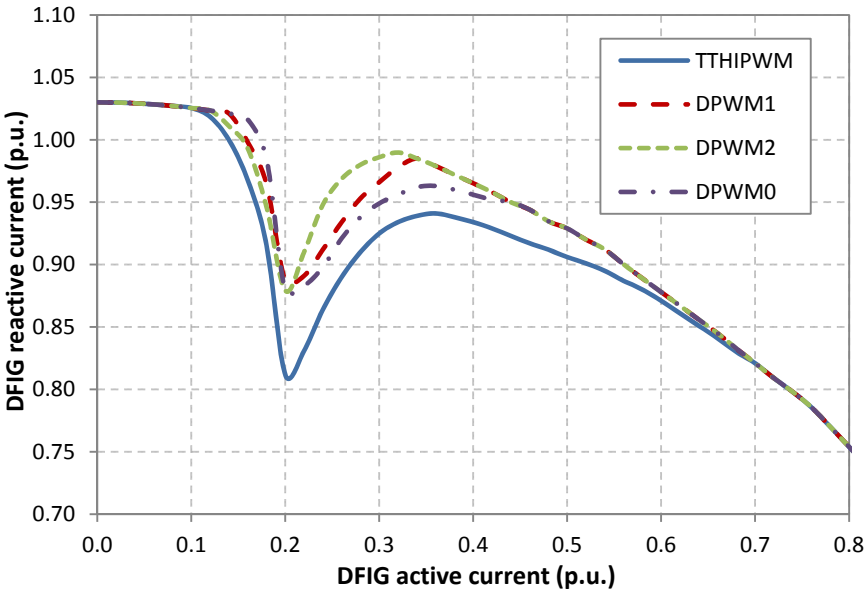


Figure 7-15: Reactive current capability of DFIG based WT around synchronous speed as a function of active current at nominal voltage

The figure shows that applying DPWM0, DPWM1 and DPWM2 increased the reactive current capability with the highest increase of about 6.8% with DPWM2 when compared with TTHIPWM during super-synchronous speed. In overall, the improvement of the reactive current capability with DPWM2 is the highest during super-synchronous speed while DPWM0 show the highest increment during sub-synchronous speed. At synchronous speed, DPWM and CPWM show the worst reduction from their maximum value with approximately 12.4% and 19.8%, respectively.

Using Eq. (7.3)-(7.5), the reactive power versus active power characteristic of DFIG by considering the relationship between active power and speed in accordance with Figure 7-7, can be shown in Figure 7-16. All limitations discussed in this section are considered. It can be shown that around synchronous operating point, de-rating in the MSC current due to the limitation in IGBT junction temperature imposes a limit on the over-excited reactive power output. Using DPWM0 and DPWM2 for the MSC improved the reactive power capability at these operating points. While on the under-excited mode, stator current limitation imposes a limit on the reactive power output. The vertical line at 1.0 p.u. represents the maximum stator active current corresponding to the rated stator active power.

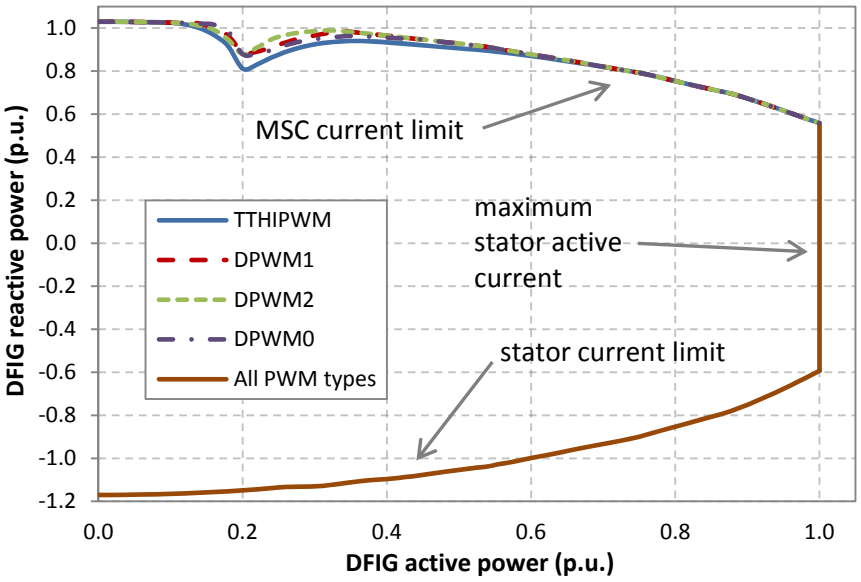


Figure 7-16: Reactive power capability of DFIG based WT in relation to active power with different PWM types at rated grid voltage and frequency

It can be concluded that the reactive power capability for the back-to-back two-level converter of DFIG based WT are improved when using DPWM types compared with CPWM types especially during the operation of generator at around synchronous speed.

7.2.2 Discussion and recommended solutions

In this section, the performances of back-to-back two-level converter for DFIG based WT have been investigated throughout comparison with different PWM types, generally between CPWM and DPWM.

The type of PWM not affected the level of generated common mode voltage (CMV). The generated CMV level at MSC is about 550 V which still in higher value. It has been studied in other literatures that the effect of generated CMV can be reduced by using filtering strategies or shaft grounding, or primarily earthing brushes in combination with zero sequence slip ring which is implemented at the rotor side. However, these methods required additional space and causes higher cost. An economical method that required no extra components is using modified PWM technique which controlling the PWM switching instants. However, reducing generated CMV via this method increases the output current harmonics of the converter, which has been investigated in [103]. The study has presented that the harmonics distortion is greatly increased more than two times higher than that of standard PWM techniques at modulation index lower than 0.5. Since the MSC of DFIG is normally operating in the range

of modulation index below 0.6, therefore, this method is not appropriate to apply for the DFIG.

Another approach to reduced generated CMV is using higher level of converter topology. In this approach, triangular carrier methods used for generation of PWM switching instants are the main factor of the generated CMV reduction. Further investigation on this approach will be presented in the next section.

Selecting CPWM for LSC and MSC is preferable for better power quality since they significantly produced the lowest current *THD* injected into the grid at entire speed range of DFIG based WT. On the contrary, when considering on compact design of power converters and improvement in reactive power capability, selecting DPWM for LSC and MSC is more preferable.

The analysis results in this section gave an idea on selecting which type of PWM to be applied for LSC and MSC that could obtain optimal performances of the DFIG based WT. One suggestion is using a simple control algorithm for PWM type selection. With this control algorithm, different PWM type can be changed and applied at certain rotor speed operation points. This can be done by putting a switch selection at different common mode voltage (CMV) calculator, where the switch will be triggered by rotor speed or active power signal following the provided control algorithm. For this simulation study, the proposed block diagram and control algorithm for PWM type selection in MSC is shown in Figure 7-17.

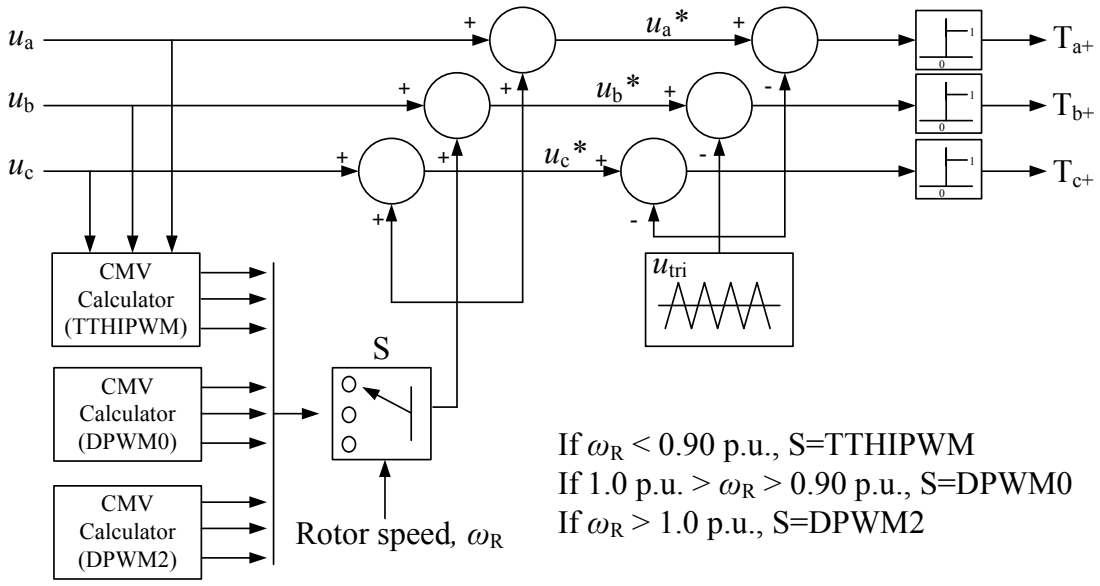


Figure 7-17: Proposed block diagram and control algorithm for PWM type selection in MSC

In this control algorithm, TTHIPWM is applied for LSC over the entire rotor speed operations. While for MSC, TTHIPWM is applied when the rotor speed is below 0.90 p.u., DPWM0 is applied when the rotor speed is operating between 0.90 p.u. and 1.0 p.u., and DPWM2 is applied when the rotor speed is above 1.0 p.u. Therefore, the DFIG based WT will has the optimal performances with less current *THD* at the grid, less converter power losses and improved reactive power capability over the entire rotor speed operations.

Figure 7-18 shows an example of the PWM modulating reference signal, rotor voltage and rotor current for "phase a" during transition at 0.90 p.u. (in figure at 0.75 s). Physically, the current waveform quality shows the same before and after transition.

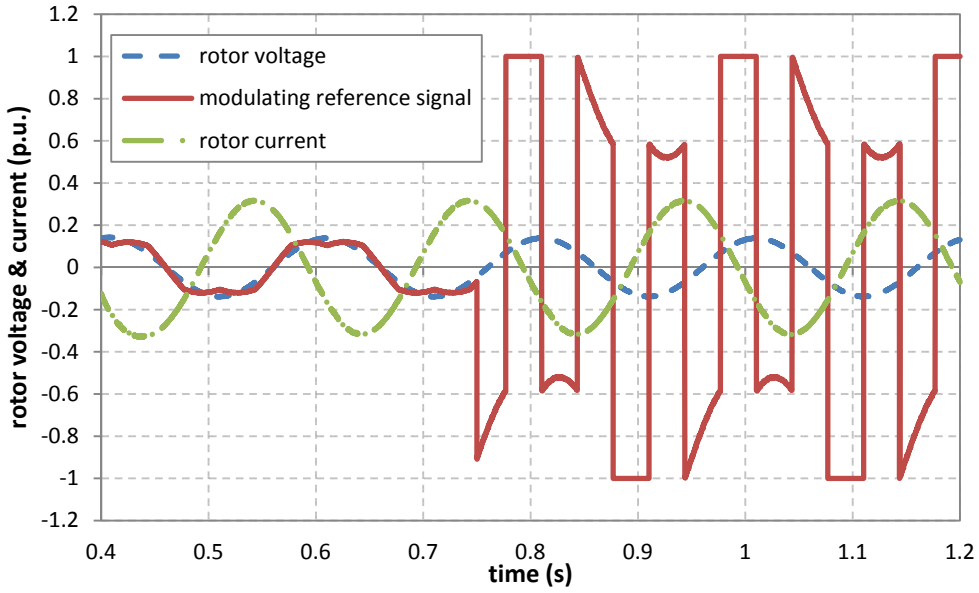


Figure 7-18: Transition from TTHIPWM to DPWM0 at 0.90 p.u. of rotor speed (phase a)

7.3 Comparison between two-level converter and three-level NPC converter

Different converter topologies, namely two-level converter and three-level NPC converter discussed in chapter 3 are applied for a 2 MW DFIG based wind turbine (WT). Performances comparison between both converter topologies will be investigated and discussed. The two-level converter has been used more widely in the wind turbine application compared to the three-level converter due to its lower cost and need smaller space. Thus, the cost of both converters will be also discussed in this section.

7.3.1 Performance analysis

Table 7-2 shows the characteristics of the two-level and three-level NPC converter used for performance comparison that will be presented in this section.

Table 7-2: Characteristics of two-level and three-level NPC converter

	Two-level converter	Three-level NPC converter
IGBT module	SKiiP2414GB17E4-4DUW	SKiiP2414GB12E4-4DUW
Modulation method	TTHIPWM	TTHIPWM
Triangular carrier method	Single carrier	PD and POD
Switching frequency	2250 Hz	2250 Hz
DC-link voltage	1100 V	1100 V

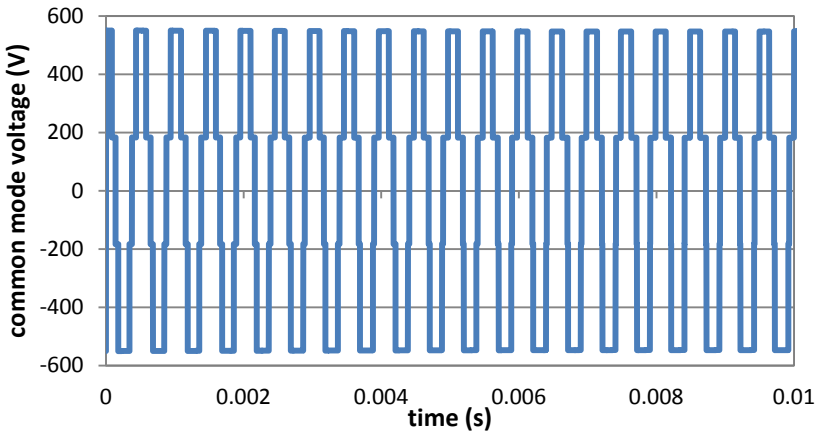
Except for the converter components, the other components in the DFIG system are remain the same value for both converter topologies, as presented in Appendix A.1. TTHIPWM is selected and applied for both converter topologies. A constant carrier frequency of 2250 Hz has been chosen for both converter topologies. Thus, the filter at the LSC line is dimensioned with resonant frequency corresponding to the carrier frequency and double this value. Both converter topologies are simulated in such a way that a good comparison is possible and enables the design of the filter with about the same size and costs.

7.3.1.1 Generated common mode voltage

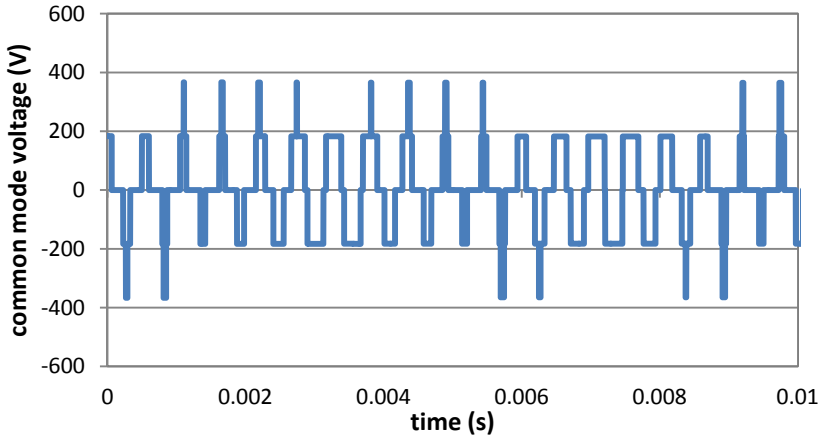
As explained previously, the generated common mode voltage (CMV) can be reduced by using higher level of converter topology with appropriate triangular carrier method. The triangular carrier methods are presented in chapter 5.

With PD method, the voltage vector of (+,+,+), (-,-,-) (refer Table 5-4) is eliminated and resulting u_{no_conv} with maximum value of $u_{DC}/3$. While with POD method, the same voltage vector in PD method, and the voltage vector of (+,+,0) (+,0,+) (0,+,+) (-,-,0) (-,0,-) (0,-,-) is eliminated and resulting u_{no_conv} with maximum value of $u_{DC}/6$. Thus, the POD method can produce lower generated CMV than the PD method.

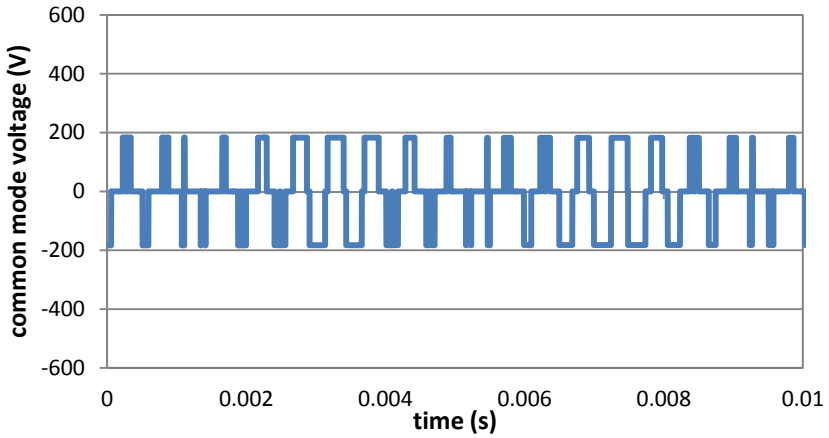
Figure 7-19 shows the generated CMV for two-level converter, three-level NPC converter with PD method and three-level NPC converter with POD method. It clearly shows from these figures that peak of generated CMV is the lowest in the case of Figure 7-19(c). The generated CMV is reduced from about 550 V in the two-level converter to about 366 V in the three-level NPC converter with PD method, and reduced to about 183 V in the three-level NPC converter with POD method.



(a) Two-level converter



(b) Three-level NPC converter with PD



(c) Three-level converter with POD

Figure 7-19: Generated common mode voltage with different converter topologies and triangular carrier methods

It can be concluded that generated common mode voltage is reduced when using the three-level NPC converter and POD method with maximum reduction of 66% when compared to

the two-level converter. This great decrement helps a lot in the stress reduction of the generator.

7.3.1.2 Current total harmonic distortion

The rotor speed operating points for the harmonics analysis are the same as in section 7.2. Using Eq. (7.1), the current *THD* are obtained and shown in Figure 7-20.

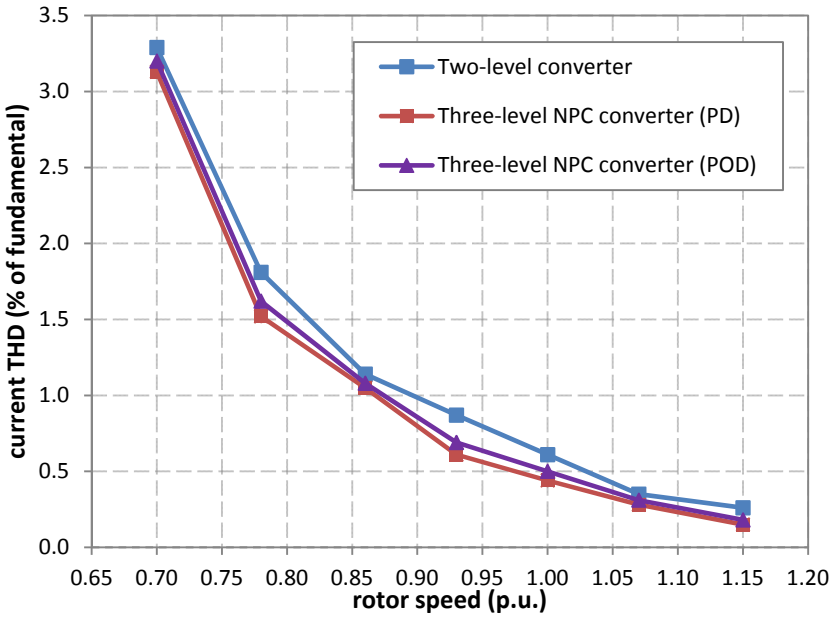


Figure 7-20: Current *THD* at different rotor speed operating points measured at low voltage grid

From the figure, it shows that the current *THD* level at each rotor speed operation is almost at the same value when using three-level NPC converter with PD or POD methods. It means that different triangular carrier methods give very less influence to the generation of harmonic distortion. Using the three-level NPC converter produced lower current *THD* than using the two-level converter with maximum different about 0.3%.

For all cases, the current *THD* at the low voltage grid of the DFIG based WT during the entire rotor speed operation points are still lower than 8% limit required by the standard EN61000-2-4. It can be concluded that for the DFIG based WT system studied in this thesis, using either two-level converter or three-level NPC converter produced acceptable low level of current *THD* at low voltage grid for the entire rotor speed operations.

7.3.1.3 Converter power losses

Following the same rotor speed operation points as in the performance analysis of current *THD*, and using Eq. (6.11) and Eq. (6.15), the converter power losses can be calculated and shown as in Figure 7-21.

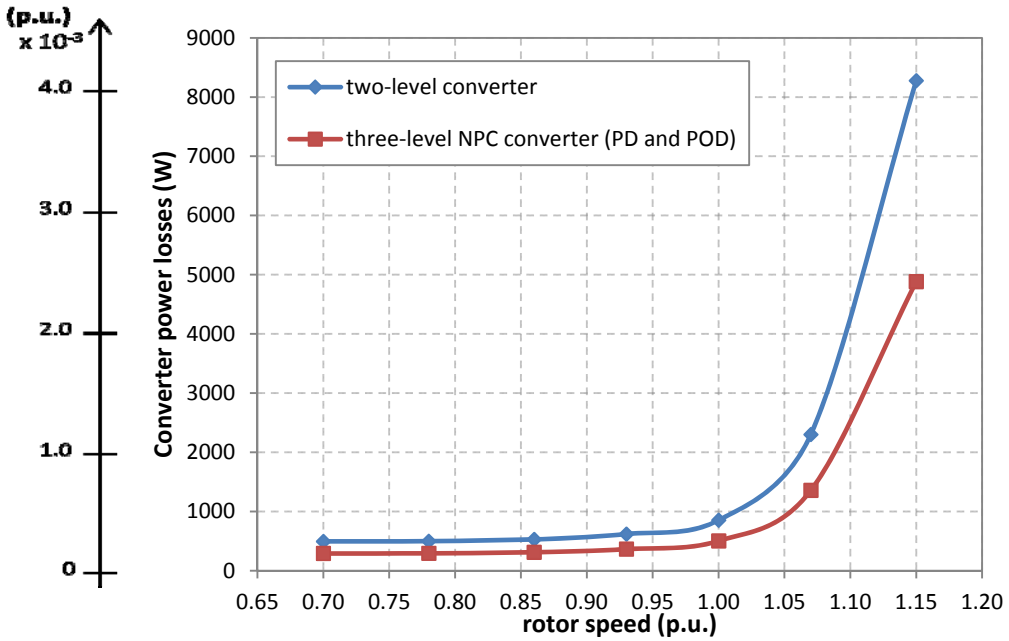


Figure 7-21: Total power losses of back-to-back converter two-level converter and three-level NPC converter (PD and POD) at different rotor speed operating points

From the figure, it clearly shows that the three-level NPC converter produced lower power losses compared to the two-level converter at the entire speed operating points of the DFIG based WT. The power losses are reduced about 40% when using the three-level NPC converter. This percentage reduction could contribute enough to the improvement in the converter output power capability and to the size reduction of cooling system, such as the heat sink.

It can be concluded that in the same DFIG system, the back-to-back three-level NPC converter produced lower power losses compared to the back-to-back two-level converter and different triangular carrier method did not causes differences in the power losses generation.

7.3.1.4 Reactive power capability

Since PD and POD method in the three-level NPC converter generated the same power losses, only PD method is used in output power analysis. Using Eq. (6.20)-(6.23) and Eq. (6.30)-(6.35), and the simulated data of IGBT/diode power losses, the maximum junction temperature of IGBT/diode as a function of frequency of rotor voltage under a constant MSC

output current can be expressed as shown in Figure 7-22. The results are related to the maximum permissible rotor current at rated speed with i_{MSC_max} = constant.

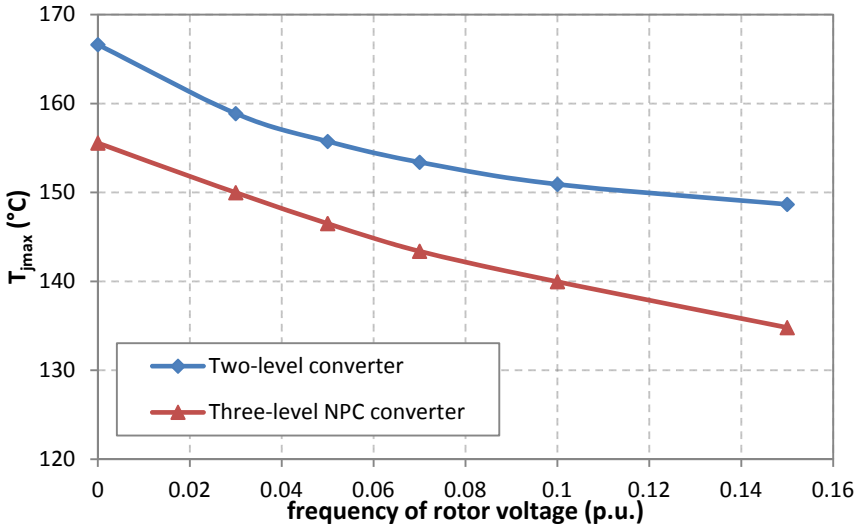


Figure 7-22: Maximum junction temperature of IGBT/diode in MSC as a function of frequency of rotor voltage

From the figure, it can be found that the junction temperature is higher at lower frequency of rotor voltage. The junction temperature exceeds its maximum limit of 150°C below the frequency of about 0.115 p.u. for two-level converter and 0.030 p.u. for three-level NPC converter. During these conditions, the MSC current has to be reduced to maintain the maximum junction temperature at about the same level as at the rated speed.

After current de-rating, the maximum MSC output current in relation to frequency of rotor voltage can be shown as in Figure 7-23. The diagram is corresponding to the pre-condition $T_{jmax} \leq (T_{jmax}$ at rated speed).

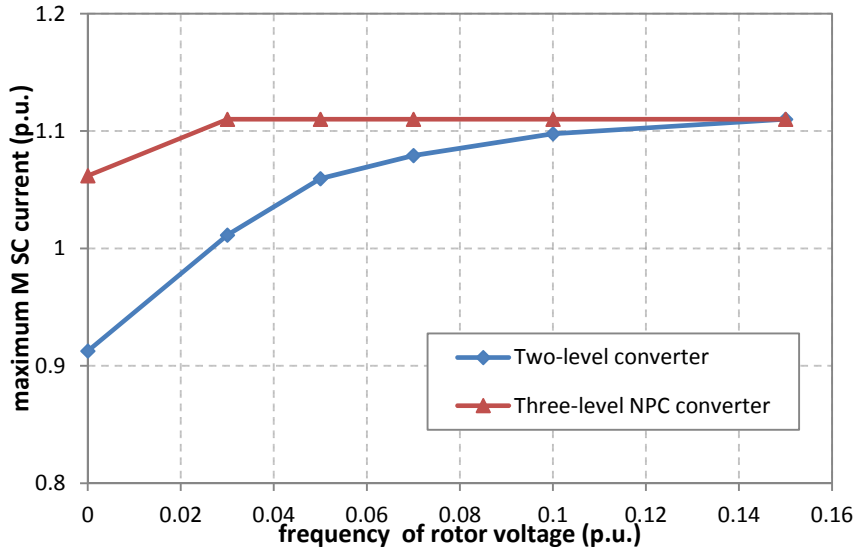


Figure 7-23: MSC output current rating in relation to frequency of rotor voltage

The stator reactive current as a function of active current at the rated MSC current with limitation considered in Figure 7-23 can be shown in Figure 7-24, which also includes the magnetizing current. Positive reactive currents show the operation of DFIG during over-excited mode while negative reactive currents show the operation during under-excited mode.

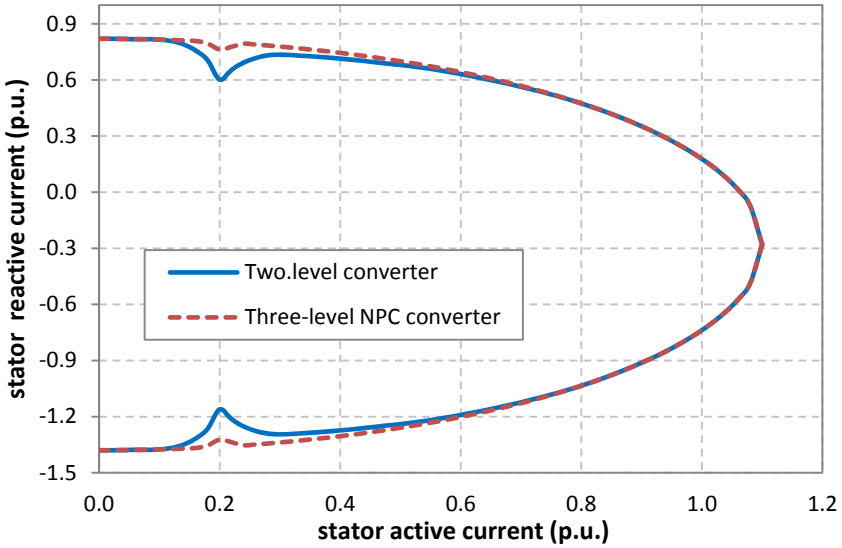


Figure 7-24: Stator reactive current capability at rated MSC current as a function of active current at nominal voltage

Considering all stator current limitation, the resulting stator reactive current capability can be shown in Figure 7-25.

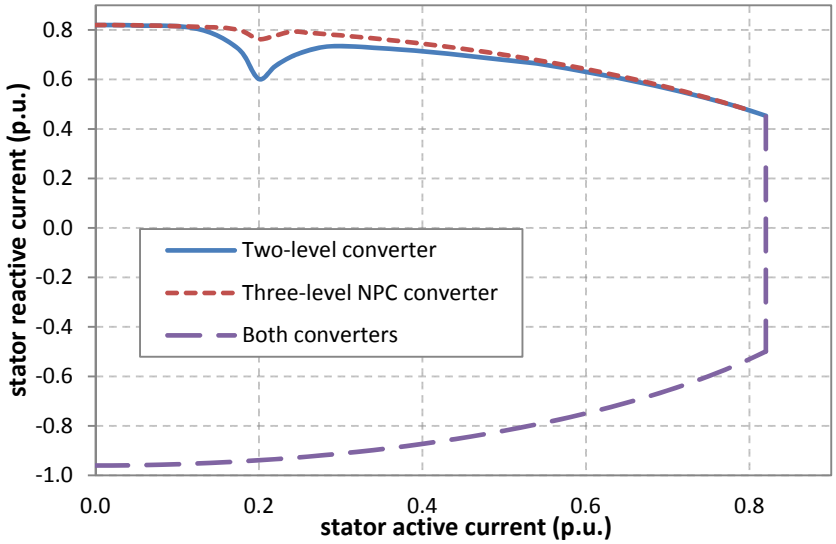


Figure 7-25: Stator reactive current capability as a function of active current at nominal voltage considering all stator current limitation

Combining the stator and LSC reactive current capability give results of the reactive current capability of DFIG based WT. For analyzing the impact of different converter topologies on

the reactive current capability around synchronous speed, the DFIG based WT reactive current capability is illustrated as in Figure 7-26, considering only operation during over-excited mode. The figure shows that using the three-level NPC converter increased the reactive current capability at synchronous speed and around synchronous speed when compared with the two-level converter. The highest increment is at synchronous speed with about 19.83 %.

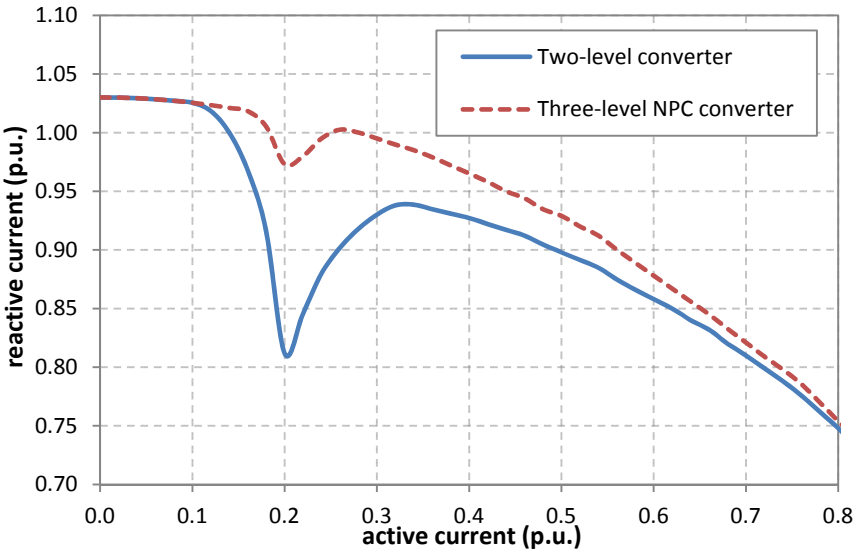


Figure 7-26: Reactive current capability of DFIG based WT around synchronous speed as a function of active current at nominal voltage

Figure 7-27 shows the resulting active-reactive power capability of DFIG based WT, which is corresponding to the active-reactive current capability mentioned previously. Generally, the results show that the three-level NPC converter increased the reactive power capability of DFIG based WT at synchronous speed and around synchronous speed when compared to that of the two-level converter. This superior performance could bring the three-level NPC converter as one of interactive converter for wind turbine manufacturers and power utility companies to be used in DFIG based WT regardless its cost.

It can be concluded that the back-to-back three-level NPC converter improved the reactive power capability of DFIG based WT at synchronous speed and around synchronous speed when compared to that of the back-to-back two-level converter. Since the cost of the converter is one of the major factors for the converter topology selection, the cost comparison will be discussed in the next section.

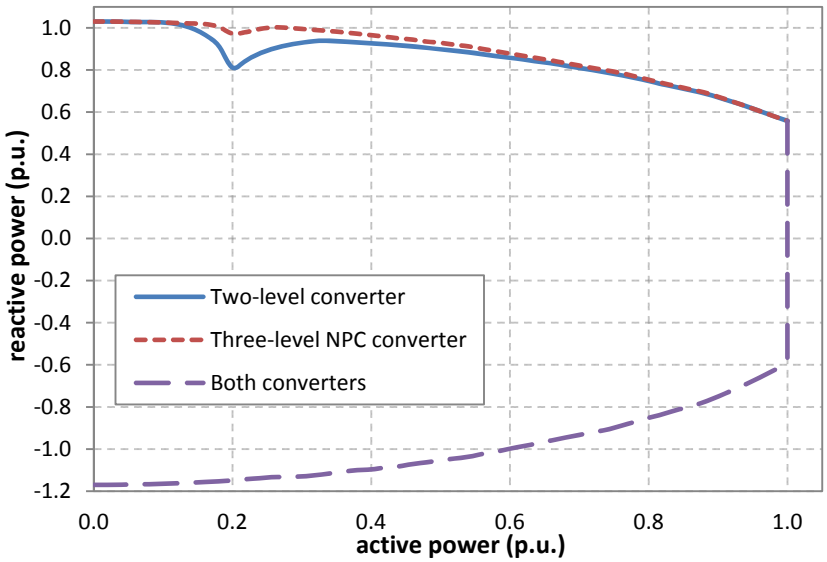


Figure 7-27: Reactive power capability of DFIG based WT in relation to active power with different converter topologies at nominal voltage

7.3.2 Discussion and recommended solutions

The performances of back-to-back three-level NPC converter have been investigated throughout comparison with back-to-back two-level converter in the DFIG based WT application. From four performances indexes presented previously, it can be generally said that the three-level NPC converter is superior to the two-level converter. For the generated common mode voltage, the triangular carrier method of POD for the three-level NPC converter produced the lowest level. However, different triangular carrier method (POD and PD) contributed less differences level in the harmonics performance and shown the same results for the converter power losses performance and reactive power capability.

Although the electrical performances are the main priority for most researchers and engineers in designing the DFIG system, on the other hand, wind turbine manufacturers and power utility companies are mostly concern on the total cost of the system. The converter cost contributes about 45% - 50% from the total cost of the DFIG system. Thus, it is important to have the converter cost analysis. Here, a comparative study on the cost of both converters is presented. The cost estimation is obtained from Semikron manufacturer and refers to some literatures [77], [104]. The cost is shown in p.u. value where the SKiiP2414GB12E4-4DUW price (~€2600) is taken as the reference. The SkiiP technology contains IGBT-diode pairs, gate drivers, heat-sink, sensors, controller interface and housing case. Table 7-3 shows the component count and cost of the two-level and three-level NPC converter.

Table 7-3: Component count and approximate cost of back-to-back two-level and three-level NPC converters

	Component count				**Approximate cost (p.u.)**			
	Two-level converter		Three-level NPC converter		Two-level converter		Three-level NPC converter	
	LSC	MSC	LSC	MSC	LSC	MSC	LSC	MSC
IGBT-diode pair	6	6	12	12	1.15	1.15	2.0	2.0
Gate driver	6	6	12	12				
Heat sink	1	1	2	2				
NPC diode	0	0	6	6	0	0	0.3	0.3
Chopper circuit	1		2		0.6		1.1	
DC-link capacitor	1		2		0.2		0.2	
Total	**28**		**68**		**3.1**		**5.9**	

The component count in the back-to-back three-level NPC converter is about 2.43 times higher than in the back-to-back two-level converter. It means that the three-level NPC converter has about two times more size/weight and need more space than the two-level converter.

The cost of the back-to-back two-level converter is about 47% less than the three-level NPC converter. This factor is one of the main reasons why the two-level converter is more preferable by the wind turbine manufacturers. However, this comparison example is based on assumption that the *LC* filter at the LSC side is designed at the same values for both converters. In practical application, the *LC* filter for three-level NPC converter is designed with smaller values where it produces harmonics distortion levels that still meet the standard requirements. In this case, the filter cost for the three-level NPC converter is about 30% less than the two-level converter [2]. Thus, the total cost of DFIG system using the three-level NPC converter could be slightly reduced.

When the DFIG system are designed to have better power system quality and higher converter efficiency, it is recommended to use back-to-back three-level converter. Although the present cost of the three-level converter is about two times higher, advance semiconductor technology and new development in converter control strategic could reduce the converter cost in the near future.

In the next chapter, a new DC-link protection scheme is proposed that make the chopper circuit redundant. This scheme may also lead to the cost reduction of the three-level NPC

converter. The characteristics behavior during grid faults and the cost analysis will be presented.

8 Dynamic Simulation of Three-Level NPC Converter

With the increase of wind energy conversion system capacity, conventional two-level converter tends to be replaced by three-level NPC converter. Additionally, current trend in cost reduction of power semiconductor devices likely makes it attractive to use of the three-level NPC converter [105], [106]. Furthermore, the three-level NPC converter has many advantages including the capacity to generate a very good quality of waveforms, the reduced switching frequency, the low stress on power devices, the low generated common mode voltage, and the low energy losses [104], [107]-[111], where some of them have been presented in the previous chapter.

In this chapter, dynamic simulation of the three-level NPC converter in DFIG based wind turbine (WT) will be presented. The study will investigate the characteristics behavior of the three-level converter during grid faults using different protection schemes for fault ride-through (FRT). A new protection scheme is proposed and the results will be compared with the conventional protection scheme. A cost evaluation of the three-level NPC converter using both protection schemes will also be presented.

8.1 Grid code requirements concerning Fault Ride-Through (FRT)

Concerning grid support during steady-state operation as well as during grid faults in the wind energy generation system, some countries like Germany have released their own grid code. According to the German grid code 2006, WTs have to ride-through the grid faults and provide a mandatory voltage support during voltage dips. The corresponding voltage control characteristic is shown in Figure 8-1 which specifies the reactive current set-point depending on the depth of the voltage drop. Accordingly, WTs have to supply at least 1.0 p.u. reactive current already when the voltage falls below 50%. The controller may include a deadband of up to ±10% and has a setting range for the gain of 0-10 p.u. with a default value of 2.0 p.u. The voltage control must take place within 20 ms after fault recognition or after activation of protection devices by providing a reactive current on the low voltage side of the generator transformer amounting to at least 2% of the rated current for each percent of the voltage dip. With conventional protection devices, the fault durations are normally in a range of some hundred milliseconds or less. However, this time duration may be decisive for the stability of the conventional generators connected to the grid and consequently for the whole system. In this regard, the dynamic response of the voltage support by power generation unit is a very

important issue. The German renewable energy law (Erneuerbare Energien-Gesetz, EEG) includes regulations concerning ancillary services [112], which address this subject by specifying timing rules for the system response to grid faults. These rules are based on the diagrams in Figure 8-2, which stipulate a rise time of less than 30 ms and a settling time of less than 60 ms considering a tolerance band between +20% and -10% of the nominal current around the set-point.

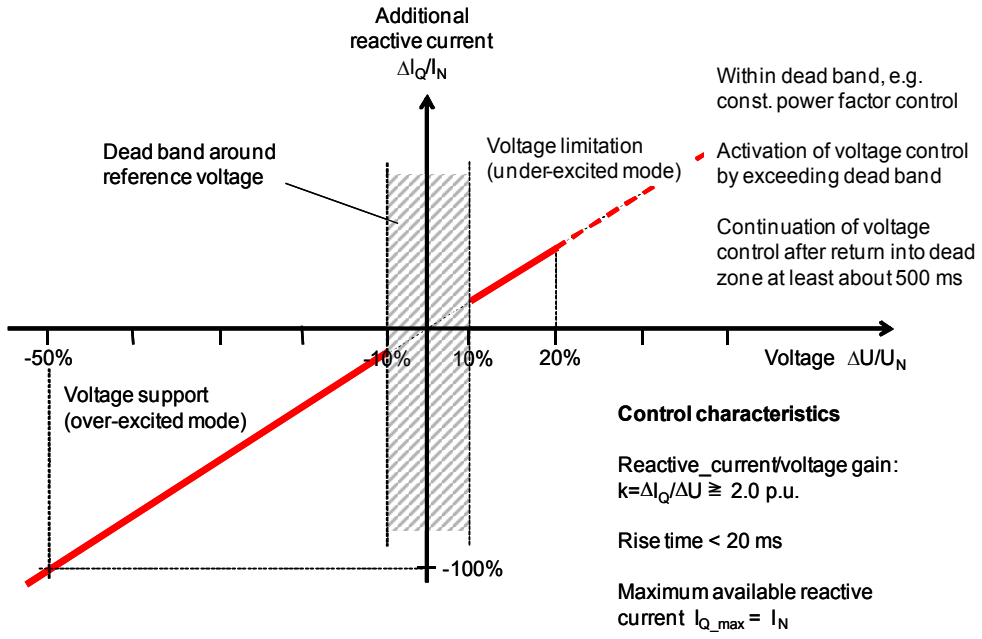


Figure 8-1: Voltage support requirement (e.ON grid code 2006)

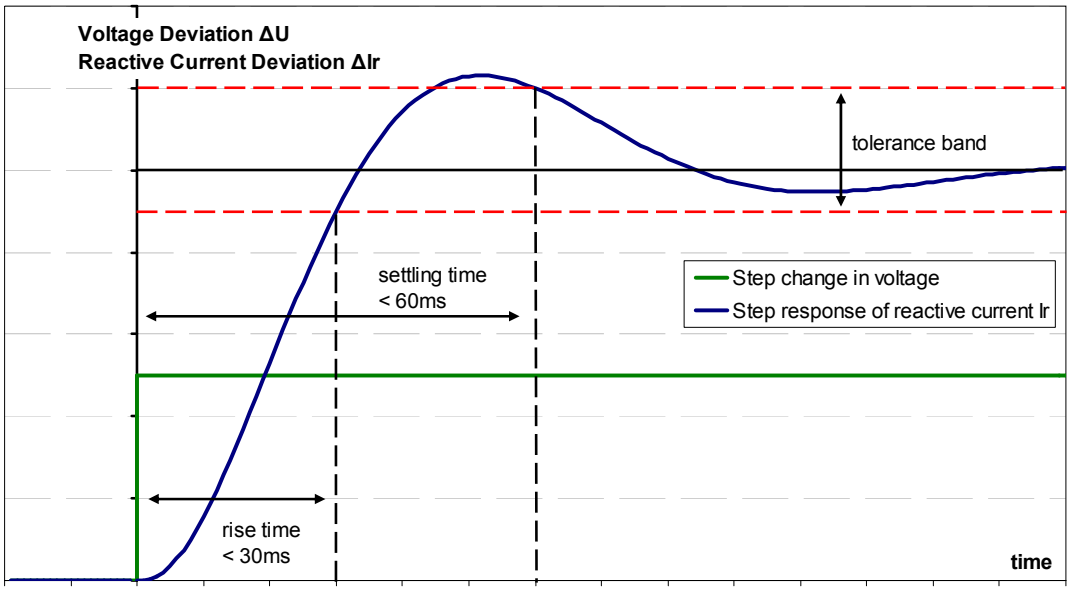


Figure 8-2: Dynamic performance requirement for voltage support according to German EEG [112]

8.2 Protection schemes for FRT

During the grid faults, DFIG based WT experience over-currents which lead also to increase DC-link voltage on the converter side. These harmful conditions may cause damages to rotor windings, converters, DC-link capacitors or induce drive train mechanical stress due to torque fluctuations. In order to avoid such damages, some special protection schemes are necessary which however should not contravene the grid code requirements.

Until nowadays, crowbar and DC-link chopper are two well known protection schemes for FRT of the DFIG. An overview of their operation principle will be presented in the next section. Additionally, a new protection scheme which has more simple operation and fewer components count is proposed as alternative of the conventional protection schemes.

8.2.1 Crowbar

Crowbar is connected between rotor circuit and MSC in the DFIG system for protecting the converter and rotor windings against over-current or DC-link over-voltage [113]. The crowbar circuit could uses diode rectifiers with a semiconductor switch or anti-parallel semiconductor switch pairs as shown in Figure 8-3. The crowbar circuit which uses common thyristor as the semiconductor switch is called passive crowbar. When self-commutated semiconductor switches (such as IGBT, IGCT, GTO) are used as the semiconductor switch, the circuit is called active crowbar.

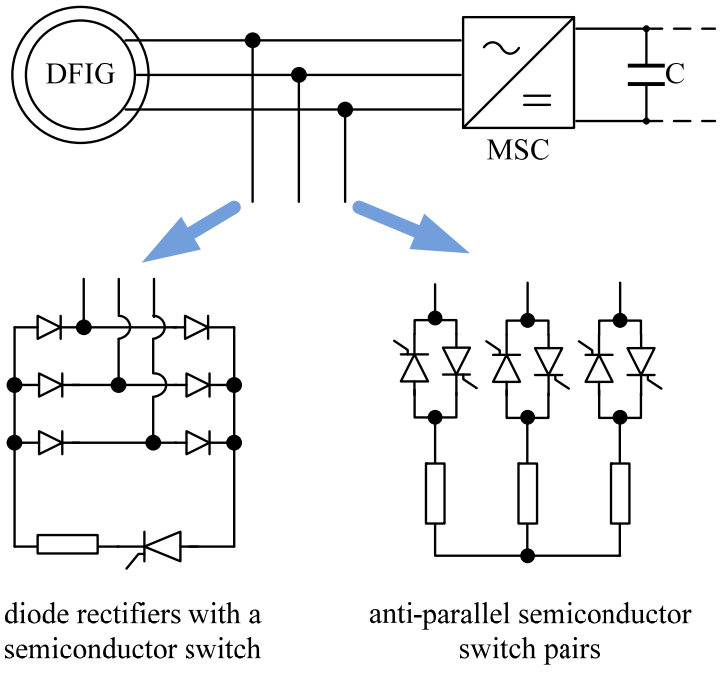


Figure 8-3: Crowbar circuit

In the passive crowbar, the system is activated during over-current on the rotor windings or over-voltage on the DC-link, which can occur after a short circuit fault at the grid side. The pulse signal to trigger the common thyristor is given when the rotor current or DC-link voltage exceeds a preset value. After crowbar triggering, it is necessary to wait for some fundamental cycles before resetting the control signal to ensure that the main transients have decayed. Since the common thyristor is only capable to turn-off at current zero-crossing and the slip frequency is quite low, the MSC has to wait some additional cycles before it can be restarted. The time duration after the crowbar triggering until the MSC restarted maybe in a range of 100-150 ms. During that duration, the generator is uncontrolled and behaves like a common induction machine. It is well-known that induction machines consume a considerable amount of reactive power and the active power adjusts oneself according to the slip. The generator changes its operating point from over-excited generator to under-excited motor operation, which is undesirable and not compliant with the grid code requirements.
A successful crowbar should remove the short circuit as soon as fault clearance. This can be done by using a self-commutated semiconductor switches instead of common thyristor. This configuration is called active crowbar. The main advantage of the active crowbar is that it can directly limit the MSC currents by short-circuiting the rotor circuit through the resistor, while it can turn-off immediately, when the rotor current is low enough. The active crowbar has better controllability, however, like the passive crowbar, the MSC still has to be deactivated during crowbar activation. The time between the disconnection and reconnection of the MSC from the rotor circuits could reach about 100 ms which still exceed the standard limit of 20 ms required by the e.ON grid code 2006. Additionally, it has a higher component count compared to DC-link chopper and cannot directly limit the DC-link voltage. Due to these advantages, nowadays, some countries like Germany are no longer use the crowbar scheme. Alternatively, they use DC-link chopper circuit as the protection device for FRT in the DFIG based WTs.

8.2.2 DC-link chopper

In order to limit the DC-link voltage during the grid faults, a chopper circuit can be added to the DC-link circuit, as shown in Figure 8-4. In the three-level NPC converter, the chopper circuit consists of two IGBTs, two freewheeling diodes and two breaking resistors. This protection scheme is not essential for FRT operation but it increases the normal range of DFIG operation by smoothing the DC-link voltage during heavy imbalances of active power on the MSC and LSC. The DC chopper control is typically based on a hysteresis. The pulse

signal to trigger the IGBTs is activated when the DC-link voltage exceeds a threshold of approximate 5-10%, and thus, the DC-link chopper is turned-on and the energy is dissipated by the braking resistors.

The IGBTs in the MSC are usually stopped when the rotor current exceeds over-current protection limit, where the value is given by semiconductor manufacturer (about 2.5 p.u. of rated current). During this condition, current from the rotor circuit still continues to flow into the DC-link through the freewheeling diodes leading to a very fast voltage increase. During the IGBT blocking time, the MSC is not controllable and not providing reactive power into the grid. However, the IGBT blocking time in this scheme is normally below 30 ms which still allowable by the standard requirement.

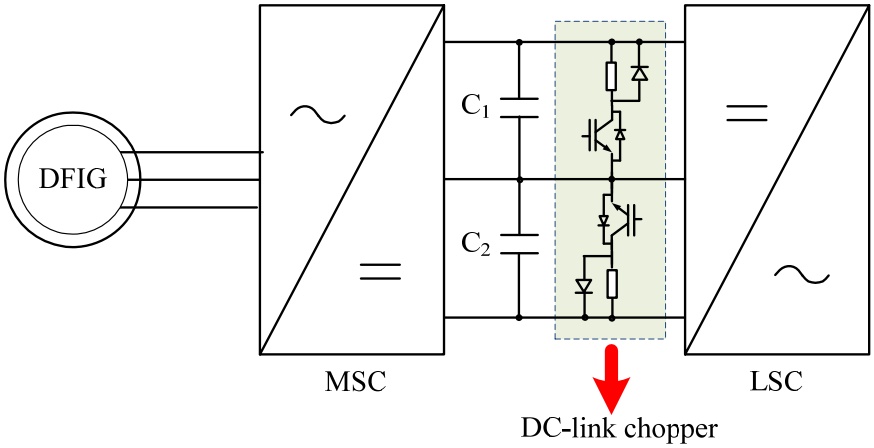


Figure 8-4: DC-link chopper circuit

8.2.3 New protection scheme with zero state control

As described previously, the DC-link chopper protection scheme requires higher cost of electrical components, such as IGBT and braking resistor. Thus, this study proposes an alternative scheme that makes the DC-link chopper redundant. The scheme uses zero state switching of the three-level NPC converter, and not applicable for two-level converter. This is due to the fact that the two-level converter has only two switching states, that is positive and negative state, while in the three-level NPC converter, it has positive, negative and zero state switching. This scheme uses the zero state switching in order to limit the DC-link voltage during grid faults.

Table 8-1 shows the switching states of the three-level NPC converter. Based on this table, turn-on and turn-off of switching devices (T_{x1}, T_{x2}, T_{x3} and T_{x4}) are controlled to determine the output phase voltage of the converter. Switching instants (1, 0) which define the turn-on and turn-off of the switching devices are generated dependent on the switching states that are

produced by pulse width modulation (PWM) carrier based technique. In this technique, three-phase modulating reference signals are compared with two triangular carrier signals 'upper carrier' and 'lower carrier'. In this way, the logical signals (+1, 0, -1) are generated, which define the switching states.

Table 8-1: Switching states of three-level NPC converter

Switching states	Switching devices				Output phase voltage
	T_{x1}	T_{x2}	T_{x3}	T_{x4}	
Positive state "+"	1	1	0	0	$u_{DC}/2$
Zero state "0"	0	1	1	0	0
Negative state "-"	0	0	1	1	$-u_{DC}/2$

Figure 8-5 shows the block diagram of the switching instants generation including the proposed scheme of zero state control. The switch S_1 will change to a constant 0 value when any phase of instantaneous rotor voltages exceeds a preset value during overshoot. The switching state will be forced to the zero state and produce zero output phase voltage at that phase leg.

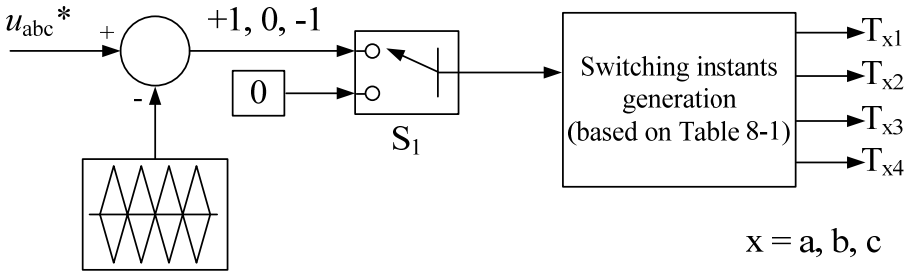


Figure 8-5: Block diagram of switching instants generation including zero state control

For more detailed description, an example of the zero state switching which occurs in "phase a" leg of the three-level NPC converter is illustrated in Figure 8-6. When any of the phases of instantaneous rotor voltages exceeds a preset value during overshoot, the phase leg is forced to be at zero state switching. An example is shown in Figure 8-6, in which the "phase a" leg is at zero state switching whereas T_{a1} and T_{a4} are turned-off with T_{a2} and T_{a3} are turned-on. The generated overshoot current in the rotor circuit is flowing into neutral point of the DC-link through T_{a3} and is not charging the DC-link capacitor. Thus, over-voltage in the DC-link can be avoided. It is assumed that the IGBTs (T_{a2} and T_{a3}) are designed with two times higher current rating than the over-current protection limit to prevent the IGBTs from being blocked due to over-current protection.

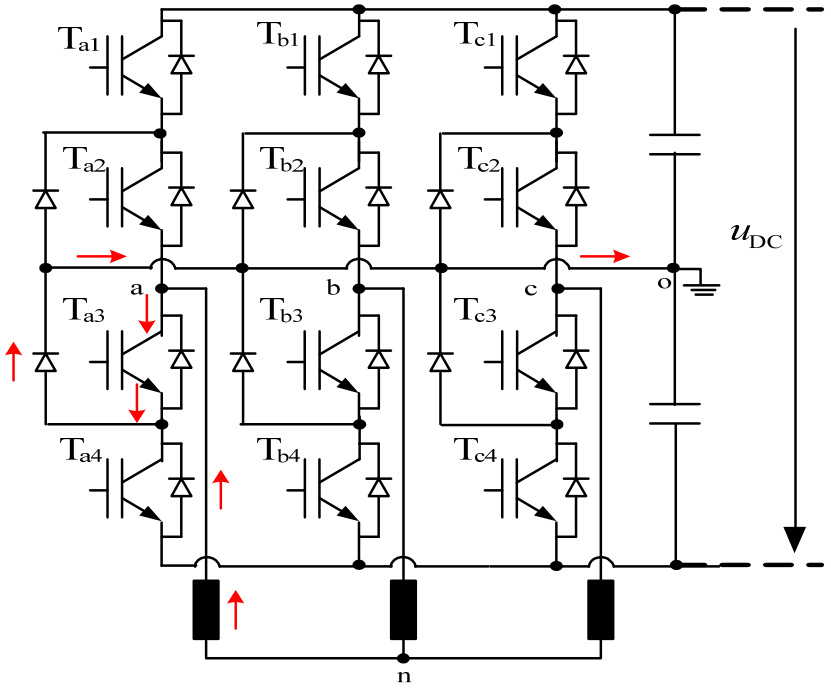


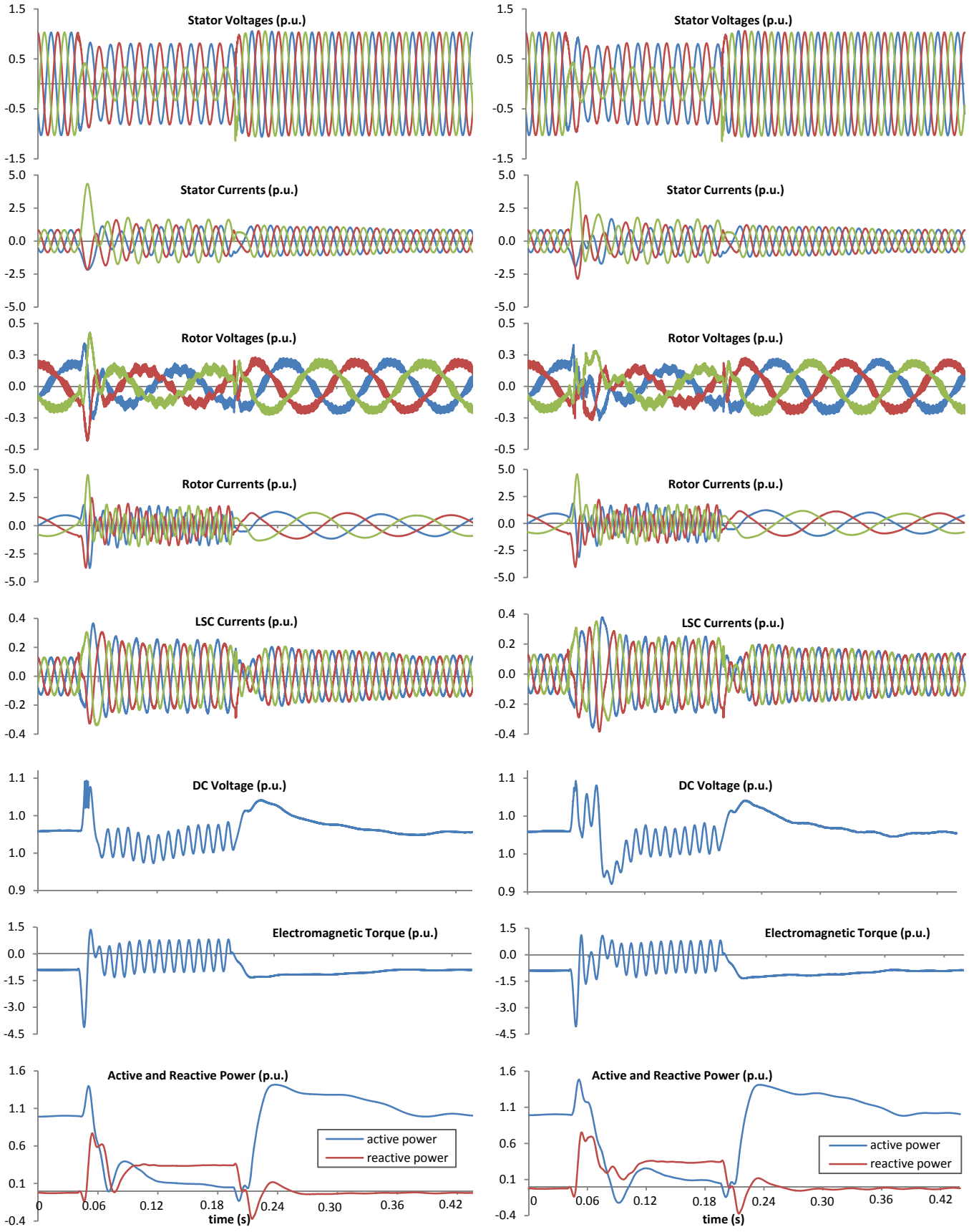
Figure 8-6: Example of zero state switching in "phase a" leg of three-level NPC converter with current flow indication

8.3 Comparative studies

In order to evaluate the behavior of the DFIG based WT using the proposed protection scheme, comparison with the conventional protection scheme, using the DC-link chopper will be carried out in this section. Two different fault conditions, namely two-phase to ground fault and three-phase fault are considered. Both the conventional protection scheme and the proposed new protection scheme are simulated in such a way that a good comparison of the two scenarios is possible. The inner IGBTs in the proposed scheme are designed with 5.0 p.u current rating to avoid IGBTs blocking.

8.3.1 Two-phase to ground fault

In this scenario the value of the fault impedance has been selected in a way that the stator voltage drops to approximate 60% of its nominal value. The fault duration is 150 ms starting from 0.04 s. Figure 8-7 shows the dynamic behavior of the DFIG based WT (a) using DC-link chopper, and (b) using zero state control.



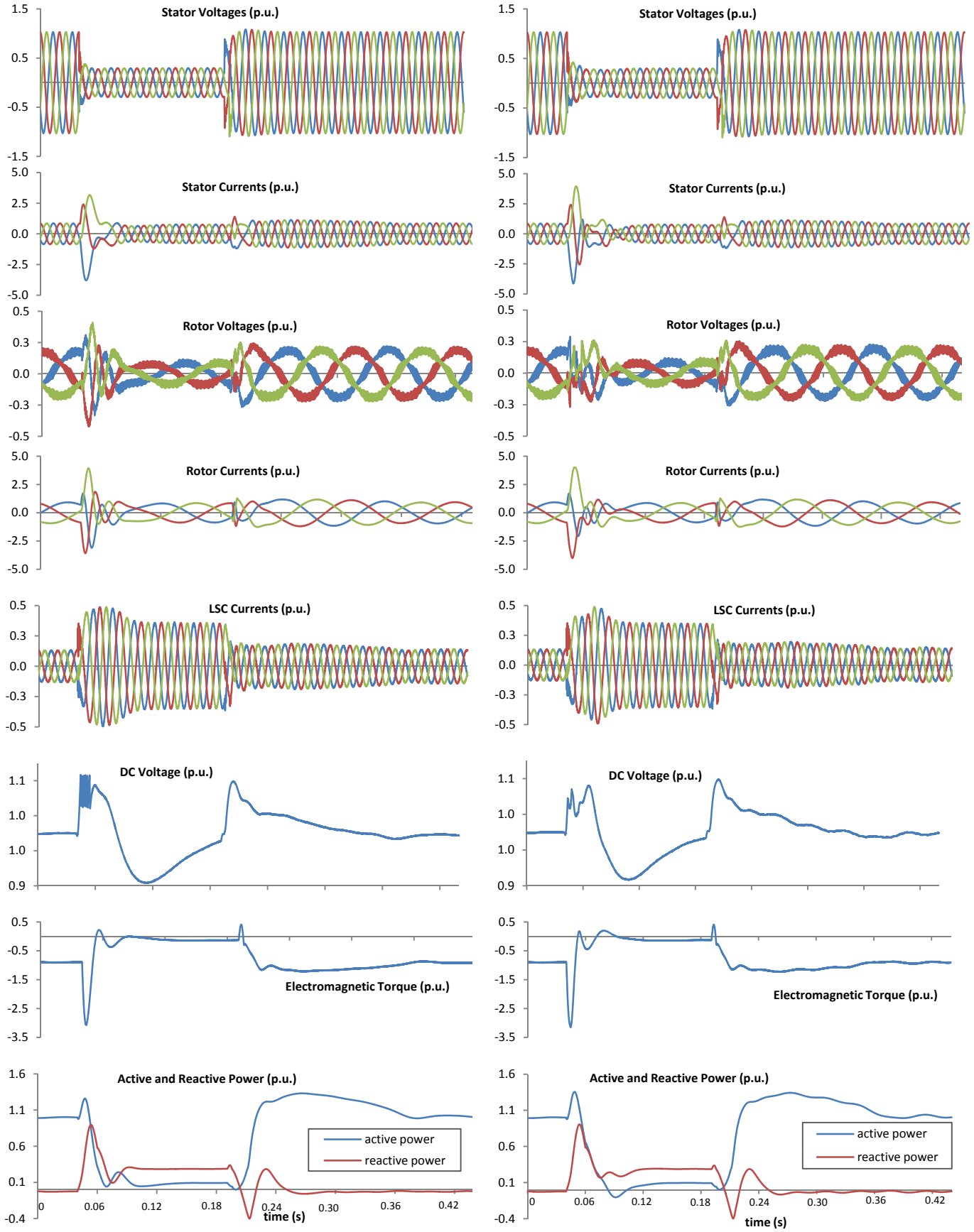
(a) Using DC-link chopper (b) Using zero state control

Figure 8-7: Dynamic behavior of DFIG based WT during two-phase to ground fault

In the case of DFIG with the DC-link protection scheme, immediately after the short circuit, the DC-link voltage rises to about the threshold value of 1.07 p.u. and activates the DC-link chopper. In the case of using zero state control, the overshoot rotor current trigger the switch controller and force the MSC to be at the zero state switching and generate zero phase voltages. This led the rotor voltages to be reduced drastically to the zero level and consequently blocked the charging of the DC-link capacitors. Thus, the DC-link voltage is increased at the beginning and then stopped at about 1.07 p.u., as shown in Figure 8-7 (b). However, the DC-link capacitors take longer discharging time of about 30 ms due to the fact that there is no external resistor to dissipate the excess energy like in the chopper circuit.
The peak stator currents are slightly higher in the Figure 8-7(b) than in the Figure 8-7(a). Since the IGBTs blocking in the MSC are avoided, the MSC in the proposed new scheme remains fully controllable during fault and increases the reactive current as well as reactive power (as shown in Figure 8-7 (b)) according to the voltage support requirement (Figure 8-1).

8.3.2 Three-phase fault

For the three-phase fault scenario the fault impedance has been set to a value, which leads to a symmetrical voltage drop to approx. 65 % in the medium voltage grid. The fault duration is 150 ms starting from 0.04 s. Figure 8-8 shows the dynamic behavior of the DFIG based WT (a) using DC-link chopper, and (b) using zero state control.
Generally, the dynamic behaviors during the three-phase fault show almost similar when compared to the dynamic behaviors during the two-phase to ground fault for both protection schemes. The DC-link chopper limits the DC-link voltage at about 1.07 p.u., while the zero state control limit the DC-link voltage at about 1.05 p.u.. Using zero state control also limit the overshoot rotor voltage at the start of the fault occurrence, due to immediate forcing the phase voltage to zero level when it exceed a preset value. Both protection schemes provide reactive currents into the grid during the faults according to the voltage support requirement.



(a) Using DC-link chopper (b) Using zero state control

Figure 8-8: Dynamic behavior of DFIG based WT during three-phase fault

8.4 Discussion and cost analysis

A new protection scheme, which can offer itself as an alternative to the DC-link chopper protection in DFIG based wind turbines, has been proposed in this thesis. The scheme is only applicable to three-level NPC converter. Generally, both conventional and the proposed protection schemes improved fault ride-through capability by limiting the DC-link voltage during the fault period. The proposed new protection scheme shows a very similar dynamic behavior with the conventional scheme in condition when the inner IGBTs of the MSC are designed for about two times higher current rating than the over-current protection limit which is about 2.5 p.u. of nominal current. Furthermore, it implements more simple operation without higher component count. The need for the inner IGBTs with higher current rating will significantly increase the cost of the MSC and has to be considered. However, the total cost of the DFIG system may be slightly reduced by the elimination of the DC-link chopper circuit.

Table 8-2 shows a comparative evaluation on component count and approximate cost of back-to-back three-level NPC converter when using DC-link chopper and zero state control schemes. It shows that using zero state control scheme slightly reduce the component count in the converter. Consequently, it will slightly reduce the size and weight of the converter. For the cost evaluation, the unit value is shown in p.u. where the price of upper IGBT-diode pair (~€195) is taken as reference. When using the zero state control scheme, the cost of inner IGBTs in the MSC is increased about 1.5 times. However, since the DC-link chopper circuit is not being used, it reduced about 14.66 p.u. value, which leads to a slight reduction (about 15%) of the total converter cost. Since this new protection scheme has the same function and shows the same dynamic behavior with the conventional scheme, even a small cost reduction, it could attract wind turbine manufacturers to use the three-level NPC converter with zero state control for the DFIG based WT application.

Table 8-2: Component count and approximate cost of back-to-back three-level NPC converter with DC-link chopper and zero state control schemes

	Component count				**Component cost (p.u.)**			
	DC-link chopper		Zero state control		DC-link chopper		Zero state control	
	LSC	MSC	LSC	MSC	LSC	MSC	LSC	MSC
Upper and lower IGBT-diode pair	6	6	6	6	6.0	6.0	6.0	6.0
Inner IGBT-diode pair	6	6	6	6	6.0	6.0	6.0	9.0
NPC diodes	6	6	6	6	4.0	4.0	4.0	5.0
Gate driver	12	12	12	12	4.0	4.0	4.0	4.0
Heat sink	2	2	2	2	5.87	5.87	5.87	5.87
Others	1	1	1	1	4.8	4.8	4.8	4.8
Chopper circuit	2		0		14.66		0	
DC-link capacitor	2		2		2.67		2.67	
Total	**70**		**68**		**78.67**		**68.01**	

9 Conclusion and Discussion

In this thesis, the performances of doubly fed induction generator (DFIG) based wind turbine (WT) during steady state operation in two alternative scenarios, namely using different PWM types and using different converter topologies, have been studied. The performance criteria include the generated common mode voltage (CMV) at machine side converter (MSC), the current total harmonic distortion in the low voltage network, the converter power losses and the DFIG reactive power capability. Additionally, the component counts in the converter and its estimate cost have been compared. In the last chapter, a new protection scheme for fault ride-through in back-to-back three-level NPC converter has been proposed as an alternative to the conventional protection scheme, using DC-link chopper. Their dynamic behaviors during grid faults have been compared and their approximate costs have been evaluated.

Wind turbines concepts have been discussed in chapter 2. The variable speed system with a partial-scale power converter, or namely the DFIG which is the most widely used type for a wind turbines application has been selected for further investigation. Then, the DFIG based WT which is generally divided into mechanical and electrical parts have been modeled and their controller design has been derived.

The study focuses on the development of back-to-back converter in terms of its topologies design and switching schemes. Two different converter topologies, namely two-level converter which is the common used topology for DFIG and three-level NPC converter which is known to having better performances have been selected. Their structure design, semiconductor switches selection and principle of switching operations were discussed.

In many semiconductor switching devices available nowadays, insulated gate bipolar transistor (IGBT) has been chosen since it has a capability of self-commutated and commonly used in converter for wind turbine application. Dependent on their availability in the market and commutation voltage, 1700 V IGBT class for the two-level converter while 1200 V IGBT class for the three-level NPC converter have been chosen.

For the switching schemes of the IGBTs, standard pulse width modulation (PWM) scheme which is classified into continuous PWM (CPWM) and discontinuous PWM (DPWM) were discussed. Generally, for constant carrier frequency, the CPWM types have lower total harmonic distortion (*THD*) than that of the DPWM types over the entire modulation range. However, for the switching losses, the DPWM types have better performance than that of the CPWM types. Among these PWM types, TTHIPWM, DPWM0, DPWM1 and DPWM2 were implemented in the DFIG system for entire speed operation range. Basically, different PWM

types contribute different performance in harmonics distortion level, power losses and output power of the converter. Additionally, for the three-level NPC converter, different triangular carrier methods contribute different generated common mode voltage level at the output of MSC. Phase opposition disposition (POD) and phase disposition (PD) have been selected and applied for the DFIG system with three-level NPC converter.

For the performance criteria of reactive power capability, a study on the thermal analysis of IGBT module has been provided. Firstly, power losses model was presented where the power losses calculation is based on parameters provided from manufacturer datasheets, in this study the Semikron. Then, thermal model of IGBT module were presented. From these models, the equations for IGBT/diode junction temperature was derived and implemented in Matlab/Simulink simulation. The reactive power capability in DFIG system is basically characterized by the permissible MSC output current which is limited by the maximum junction temperature of the IGBTs especially around synchronous operating points.

In the first performance comparison, TTHIPWM from CPWM types, and DPWM0, DPWM1, DPWM2 from DPWM types have been selected and applied for a 2 MW DFIG based WT with back-to-back two-level converter. Carrier frequency for all PWM types was taken as 2250 Hz. From the simulation results, it clearly shows that different PWM types gave strong influence to the performance of current *THD*, converter power losses and reactive power capability, and did not give effect to the performance of generated common mode voltage. The DFIG system has the lowest *THD* at the low voltage grid when CPWM was applied for both line side converter (LSC) and MSC. For having lowest converter power losses, two options were recommended whether applying DPWM for both LSC and MSC or applying CPWM for LSC and DPWM for MSC. For improvement in reactive power capability especially around synchronous speed, simulation results have shown that applying DPWM for MSC was the best choice.

In order to have optimal performances in all criteria, the study has recommended selecting PWM type dependent on the rotor speed operations. For rotor speed below 0.90 p.u., CPWM was applied for both LSC and MSC, while for rotor speed above 0.90 p.u., CPWM was applied for LSC while DPWM was applied for MSC. In other word, LSC was using CPWM at the entire rotor speed operating points, while for MSC, it has a transition point which is at 0.90 p.u. The PWM type is changing at this transition point by using a simple control algorithm for switch selection.

Rotor speed operations above 0.90 p.u. are including small range of sub-synchronous speed (0.90-1.0 p.u.), and entire range of super-synchronous speed (1.0-1.2 p.u.). For this sub-

synchronous speed range, DPWM0 was selected while for the super-synchronous speed range, DPWM2 was selected among the DPWM types since they have superior switching losses performance within these speed ranges. Therefore, for MSC, another transition point was added which is at 1.0 p.u. that changing between DPWM0 and DPWM2.

In the second performance comparison, two different converter topologies, namely back-to-back two-level converter and back-to-back three-level NPC converter were implemented in the DFIG system and their performances were investigated. Since the three-level NPC converter is less attractive to be used by wind turbine manufacturers due to its higher cost and need more space, a comparison in the cost and component count of both converter topologies were also presented. The simulation results clearly show that the back-to-back three-level NPC converter was superior compared to the back-to-back two-level converter in all performances including the generated CMV at MSC, the current *THD* at the grid, the converter power losses and the improvement in reactive power capability.

The generated CMV at MSC was reduced when using the three-level NPC converter with maximum reduction of 66% using the triangular carrier method of POD. This great decrement helps a lot in the stress reduction of the generator. The three-level NPC converter produced lower current *THD* than the two-level converter at entire rotor speed operations with about 0.3% difference. The *LC* filter at LSC side for the three-level NPC converter could be designed with smaller values where it produces harmonics distortion levels that still meet the standard requirements. In this case, the filter cost for the three-level NPC converter could be reduced about 30%.

The three-level NPC converter produced lower power losses compared to the two-level converter at the entire speed operating points of the DFIG system with reduction about 40%. These converter power losses reductions contributed to the improvement in the output power capability. The reactive power capability at around synchronous speed of the DFIG was improved with highest increment of about 19.83% at synchronous speed.

The component count in the back-to-back three-level NPC converter is about 2.43 times higher than in the back-to-back two-level converter. It means that the three-level NPC converter has about two times more size/weight and need more space than the two-level converter. The cost of the back-to-back three-level NPC converter is also about two times higher than the back-to-back two-level converter. These factors are the main reasons why the two-level converter is more preferable by the wind turbine manufacturers.

However, when the DFIG system are designed to have better power system quality and higher converter efficiency, it is recommended to use the back-to-back three-level NPC converter.

Advance semiconductor technology and new development in converter control strategic could reduce the converter cost in the near future.

This thesis also proposed a new protection scheme for fault ride-through (FRT) during grid faults. This protection scheme uses zero state switching which is applicable in three-level NPC converter. It offers itself as an alternative to the DC-link chopper protection. The proposed new protection scheme has shown a very similar dynamic behavior with the conventional scheme in condition when the inner IGBTs of the MSC were designed for about two times higher current rating than the over-current protection limit (about 2.5 p.u.). Furthermore, it implements more simple operation with slightly reduced component count. The need for the inner IGBTs with higher current rating increased the cost of the IGBTs for about 1.5 times. However, the total cost of the DFIG system is slightly reduced by the elimination of the DC-link chopper circuit. This small cost reduction could attract wind turbine manufacturers to use the three-level NPC converter for the DFIG based WT application, moreover it has superior performances in all criteria studied in this thesis.

In real practical application, the three-level NPC converter is commonly used for medium and high voltage system such as HVDC system. It is interesting to have further research for such system considering dynamic analysis and cost evaluation using the new proposed protection scheme.

The results presented in this thesis were obtained only from simulation environment. It is recommended verifying the results through experimental evaluation to check their applicability in the real world. Regarding the cost evaluation, since the cost of electrical components vary dependent on manufacturer, it is also necessary to have the cost comparison from other different manufacturers.

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Appendix

A.1. DFIG parameters

Parameter	**Symbol**	**Value**
Rated voltage	U_r	690 V
Rated frequency	f_r	50 Hz
Rated power	P_r	2000 kW
Stator resistance	r_s	0.017 p.u.
Stator leakage inductance	$l_{\sigma s}$	0.135 p.u.
Rotor resistance	r_R	0.02 p.u.
Rotor leakage inductance	$l_{\sigma R}$	0.08 p.u.
Magnetizing inductance	l_M	3.35 p.u.
Nominal speed	n_r	1500 min^{-1}
Generator inertia	J_R	1.25 p.u.
Wind rotor inertia	J_W	5.5 p.u.
Shaft stiffness	k_{sh}	455 p.u./rad
Shaft damping	d_{sh}	3.15 p.u.
MSC maximum current	i_{MSC_max}	1.11 p.u.
MSC maximum voltage	u_{MSC_max}	0.45 p.u.
LSC inductance	l_{LSC}	0.15 p.u.
LSC resistance	r_{LSC}	0.0015 p.u.
LSC maximum current	i_{LSC_max}	0.21 p.u.
LSC maximum voltage	u_{LSC_max}	1.14 p.u.

SKiiP 2414 GB17E4-4DUW

SKiiP® 4

2-pack-integrated intelligent Power System

SKiiP 2414 GB17E4-4DUW

Features

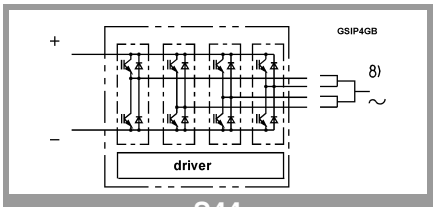
- Intelligent Power Module
- Integrated current and temperature measurement
- Integrated DC-link measurement
- Solder free power section
- IGBT4 and CAL4F technology
- T_{jmax} = 175°C
- Safety isolated switching and sensor signals
- Digital signal transmission
- 100% tested IPM
- RoHS compliant
- UL recognition in progress, file no. E242581

Typical Applications*

- Renewable energies
- Traction
- Elevators
- Industrial drives

Remarks

For further information please refer to SKiiP®4 Technical Explanation



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Absolute Maximum Ratings

Symbol	Conditions		Values	Unit
System				
V_{CC}	Operating DC link voltage		1300	V
V_{isol}	DC, t = 1 s, each polarity		5600	V
$I_{t(RMS)}$	per AC terminal, rms, sinusoidal current		500	A
$I_{max\ (peak)}$	Max. peak current of power section		3600	A
f_{out}	fundamental output frequency		1	kHz
T_{stg}	storage temperature		-40 ... 85	°C
IGBT				
V_{CES}	T_j = 25 °C		1700	V
I_C	T_j = 175 °C	T_s = 25 °C	3385	A
		T_s = 70 °C	2723	A
I_{Cnom}			2400	A
T_j	junction temperature		-40 ... 175	°C
Diode				
V_{RRM}	T_j = 25 °C		1700	V
I_F	T_j = 175 °C	T_s = 25 °C	2362	A
		T_s = 70 °C	1869	A
I_{Fnom}			2400	A
T_j	junction temperature		-40 ... 175	°C
Driver				
V_s	power supply		19.2 ... 28.8	V
V_{iH}	input signal voltage (high)		V_s + 0.3	V
dv/dt	secondary to primary side		75	kV/µs
f_{sw}	switching frequency		10	kHz

Characteristics

Symbol	Conditions		min.	typ.	max.	Unit
IGBT						
$V_{CE(sat)}$	I_C = 2400 A at terminal	T_j = 25 °C		2.12	2.49	V
		T_j = 150 °C		2.58	2.79	V
V_{CE0}		T_j = 25 °C		1.10	1.20	V
		T_j = 150 °C		1.00	1.10	V
r_{CE}	at terminal	T_j = 25 °C		0.42	0.54	mΩ
		T_j = 150 °C		0.66	0.70	mΩ
$E_{on} + E_{off}$	I_C = 2400 A T_j = 150 °C	V_{CC} = 900 V		1780		mJ
		V_{CC} = 1300 V		2840		mJ
$R_{th(j-s)}$	per IGBT switch				0.0138	K/W
$R_{th(j-r)}$	per IGBT switch				0.01	K/W

SKiiP 2414 GB17E4-4DUW

SKiiP® 4

2-pack-integrated intelligent Power System

SKiiP 2414 GB17E4-4DUW

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- Integrated current and temperature measurement
- Integrated DC-link measurement
- Solder free power section
- IGBT4 and CAL4F technology
- T_{jmax} = 175°C
- Safety isolated switching and sensor signals
- Digital signal transmission
- 100% tested IPM
- RoHS compliant
- UL recognition in progress, file no. E242581

Typical Applications*

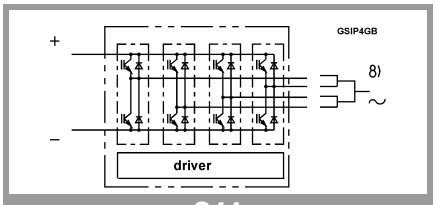
- Renewable energies
- Traction
- Elevators
- Industrial drives

Remarks

For further information please refer to SKiiP®4 Technical Explanation

Characteristics

Symbol	Conditions		min.	typ.	max.	Unit
Diode						
$V_F = V_{EC}$	I_F = 2400 A at terminal	T_j = 25 °C		2.02	2.34	V
		T_j = 150 °C		2.27	2.62	V
V_{F0}		T_j = 25 °C		1.21	1.36	V
		T_j = 150 °C		0.99	1.12	V
r_F	at terminal	T_j = 25 °C		0.34	0.41	mΩ
		T_j = 150 °C		0.53	0.63	mΩ
E_{rr}	I_F = 2400 A, T_j = 150 °C	V_R = 900 V		283		mJ
		V_R = 1300 V		456		mJ
$R_{th(j-s)}$	per diode switch				0.0281	K/W
$R_{th(j-r)}$	per diode switch				0.0241	K/W
Driver						
V_s	supply voltage non stabilized		19.2	24	28.8	V
I_{SO}	bias current @V_s= 24V, f_{sw} = 0, I_{AC} = 0			360		mA
I_S	k_1 = 47 mA/kHz, k_2 = 0.258 mA/A		= 360	+ k_1* f_{sw}	+ k_2 * I_{AC}	mA
V_{IT+}	input threshold voltage (HIGH)		0,7*V_s			V
V_{IT-}	Input threshold voltage (LOW)				0,3*V_s	V
R_{IN}	input resistance			13		kΩ
C_{IN}	input capacitance			1		nF
t_{pRESET}	error memory reset time		1.3		2.9	s
$t_{pReset(OCP)}$	Over current reset time					µs
t_{TD}	top / bottom switch interlock time			3		µs
t_{jitter}	jitter clock time			52	58	ns
t_{SIS}	short pulse suppression time			0.6		µs
t_{POR}	Power-On-Reset completed			3.5		s
V_{CEstat}	Collector-Emitter Threshold Static Monitoring Voltage			7.5		V
t_{bl}	Collector-Emitter Threshold Static Monitoring Blanking Time			6		µs
$I_{digiout}$	digital output sink current (HALT-signal)				16	mA
$V_{it+\ HALT}$	input threshold voltage HIGH HALT (Low -->High)		0,6*V_s			V
$V_{it-HALT}$	input threshold voltage LOW HALT (High --> Low)				0.4*V_s	V
$t_{d(err)}$	Error delay time (from detection to HALT), (depends on kind of error)		1.8		170	µs
I_{TRIPSC}	over current trip level		3525	3600	3675	A_{PEAK}
T_{trip}	over temperature trip level		126	130	134	°C
$T_{DriverTrip}$	over temperature PCB trip level		113	120	124	°C
V_{DCtrip}	over voltage trip level,		1300	1340	1380	V
$f0_{Uana}$	bandwidth of DC-voltage measurement @ V_{DCtrip} (-3dB)			2		kHz
$f0_{Iana}$	bandwith of current measurement @ I_{TRIPSC} (-3dB),			50		kHz
$f0_{Tana}$	bandwidth of temperature measurement @ T_{trip} (-3dB)			5		Hz



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SKiiP 2414 GB17E4-4DUW

SKiiP® 4

2-pack-integrated intelligent Power System

SKiiP 2414 GB17E4-4DUW

Features

- Intelligent Power Module
- Integrated current and temperature measurement
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- Solder free power section
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Typical Applications*

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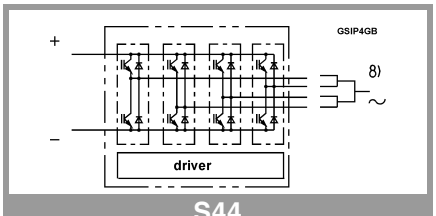
Remarks

For further information please refer to SKiiP®4 Technical Explanation



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Characteristics						
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Unit**
System						
$t_{d(on)IO}$	V_{CC} = 1300 V I_C = 2400 A T_j = 25 °C	turn on propagation delay time		2.8		µs
$t_{d(off)IO}$		turn off propagation delay time		2.6		µs
dV_{CE}/dt_{on}	T_j = 25 °C V_{CC} = 1300 V	I_C = 0 A		14		kV/µs
		I_C = 2400 A		3		kV/µs
dV_{CE}/dt_{off}		I_C = 2400 A		10		kV/µs
$R_{th(s-a)}$	flow rate = 15 l/min, T_{Fluid}=40°C, water/glycol ratio 50%:50%				0.0065	K/W
$R_{CC'+EE'}$	terminals to chip, T_s = 25 °C			0.0675		mΩ
L_{CE}	commutation inductance			4.5		nH
C_{CHC}	coupling capacitance secondary to heat sink			6		nF
C_{ps}	coupling capacitance primary to secondary			0.08		nF
I_{CES} + I_{RD}	V_{GE} = 0 V, V_{CE} = 1700 V, T_j = 25 °C			0.199		mA
M_{dc}	DC terminals		6		8	Nm
M_{ac}	AC terminals		13		15	Nm
w	SKiiP System w/o heat sink			3.22		kg
w_h	heat sink			4.25		kg

Isolation coordination acc. to EN 50178 and IEC 61800-5-1	
Maximum grid RMS voltage, line-to-line, grounded delta mains	690V+20%
Installation altitude for maximum grid RMS voltage, line-to-line, grounded delta mains	2000m
Maximum grid RMS voltage, line-to-line, star point grounded mains	690V+20%
Installation altitude for maximum grid RMS voltage, line-to-line, star point grounded mains	4000m
Maximum transient peak voltage between low voltage circuit and mains	1900V
Pollution degree acc. to IEC 60664-1 outside the moulded power section	2
Overvoltage cat. acc. to IEC 60664-1 for mains	III
Overvoltage cat. acc. to UL 840 within mains	I
Overvoltage cat. acc. to UL 840 between mains and ground	III
Overvoltage cat. acc. to UL 840 between mains and low voltage circuit	III
Basic isolation	between heat sink and mains
Reinforced isolation	between low voltage circuit and mains
Protection level acc. to IEC 60529	IP00

Environmental conditions acc. to IEC 60721					
	Storage	Transportation	Operation - stationary use at weatherprotected locations	Operation - ground vehicle installations	Operation - ship environment
Climatic conditions	1K2	2K2	3K3(1)	5K1	6K1
Biological conditions	1B1	2B1	3B1	5B1	6B1
Chemically active substances (excluded: salt spray)	1C2	2C1	3C2	5C2	6C2
Mechanically active substances	1S1	2S1	3S1	5S1	6S1
Mechanical conditions	1M3	(4)	3M6(2)	5M3(3)	6M3
Contaminating fluids	---	---	---	5F1	---

(1) 3K3: expanded temperature range: -40°C / +85°C

(2) 3M7 possible, but due to mechanic load capacity of external components like DC-Link capacitors limited to 3M6

(3) 5M3, shock only 5M2, without impact from foreign bodies, stones

(4) no declaration due to customer-specific packing

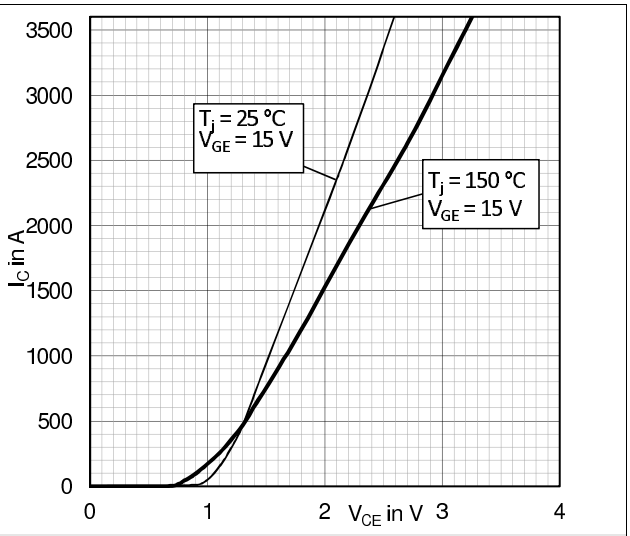


Fig. 1: Typical IGBT output characteristics

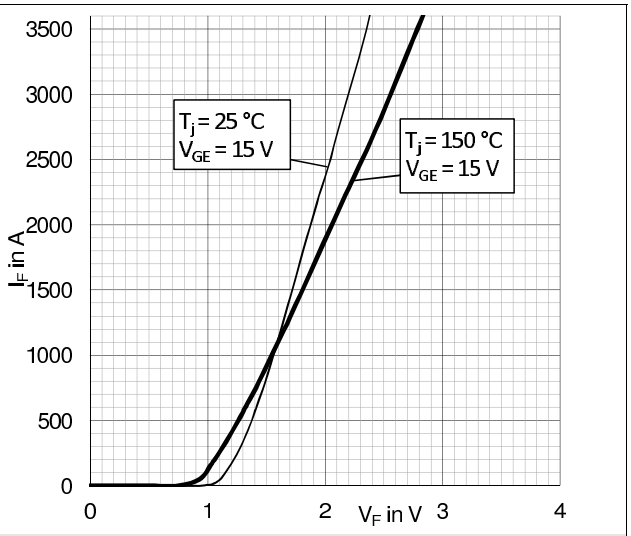


Fig. 2: Typical diode output characteristics

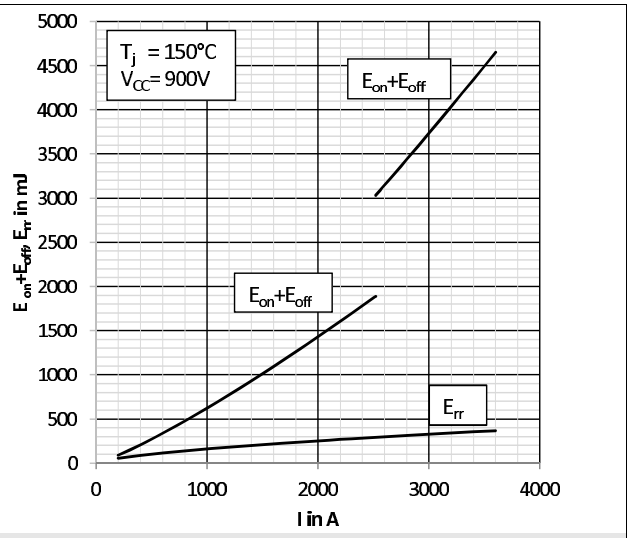


Fig. 3: Typical energy losses E = f(I_c, V_{cc}, T_j)

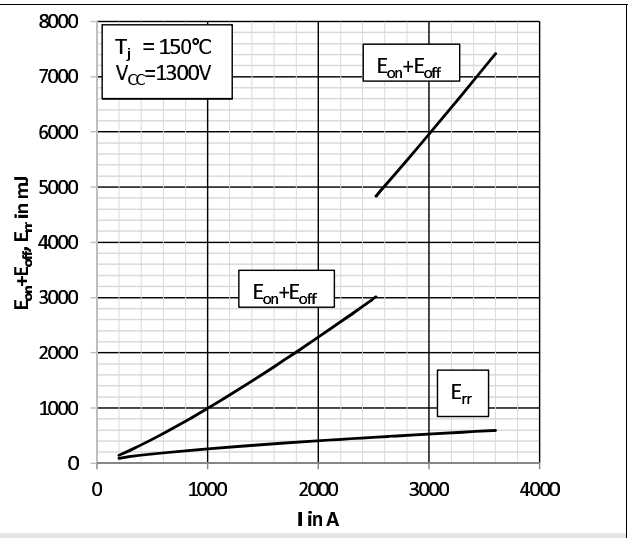


Fig. 4: Typical energy losses E = f(I_c, V_{cc}, T_j)

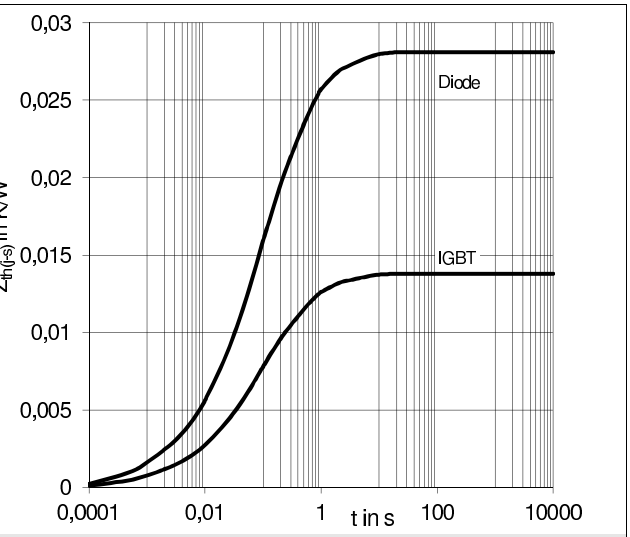


Fig. 5: Transient thermal impedance Zth(j-s)

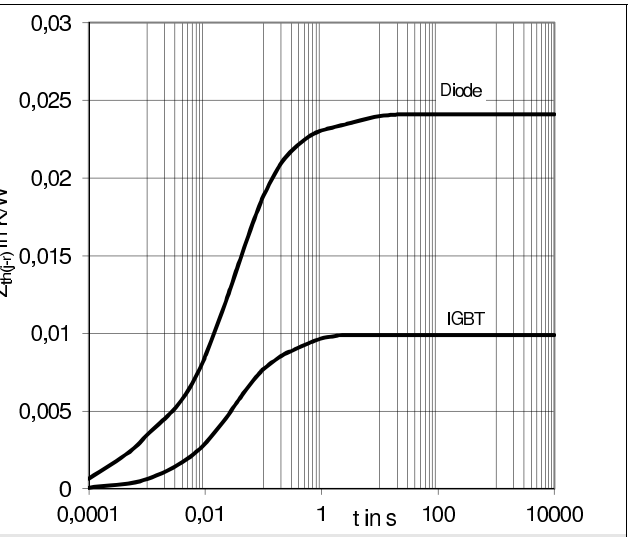


Fig. 6: Transient thermal impedance Zth(j-r)

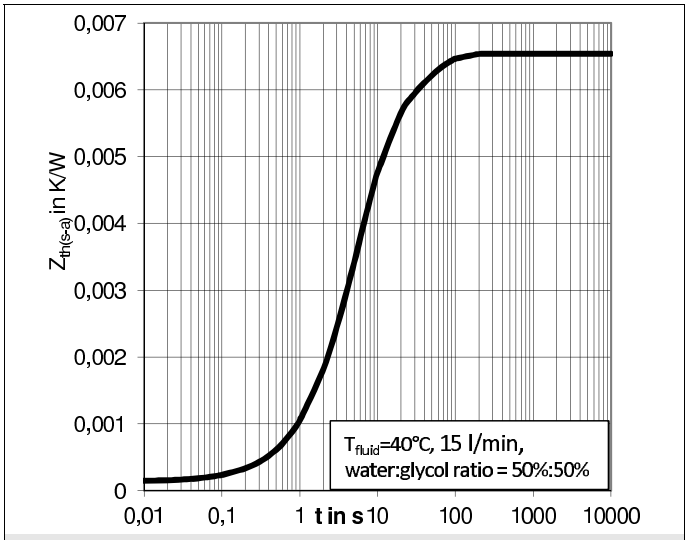


Fig. 7: Transient thermal impedance Zth(s-a)

	R_{th} [K/W]				
	1	2	3	4	5
$Z_{th(j-s)}$ I	0,0010	0,0049	0,0055	0,0017	0,0007
$Z_{th(j-s)}$ D	0,0020	0,0100	0,0112	0,0034	0,0015
$Z_{th(j-r)}$ I	0,0020	0,0048	0,0023	0,0008	
$Z_{th(j-r)}$ D	0,0012	0,0039	0,0104	0,0054	0,0032
$Z_{th(s-a)}$	0,0014	0,0050	0,0001		
	tau [s]				
	1	2	3	4	5
$Z_{th(j-s)}$ I	3,6500	0,4100	0,0650	0,0090	0,0008
$Z_{th(j-s)}$ D	3,6500	0,4100	0,0650	0,0090	0,0008
$Z_{th(j-r)}$ I	0,4500	0,0475	0,0142	0,0016	
$Z_{th(j-r)}$ D	4,1546	0,2644	0,0497	0,0107	0,0005
$Z_{th(s-a)}$	34,2609	5,2284	0,0005		

Fig. 8: Coefficients of thermal impedances

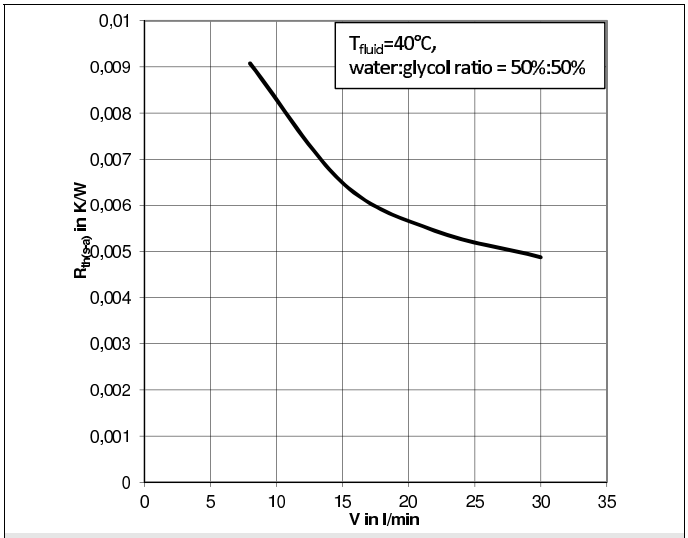


Fig. 9: Thermal resistance Rth(s-a) versus flow rate V

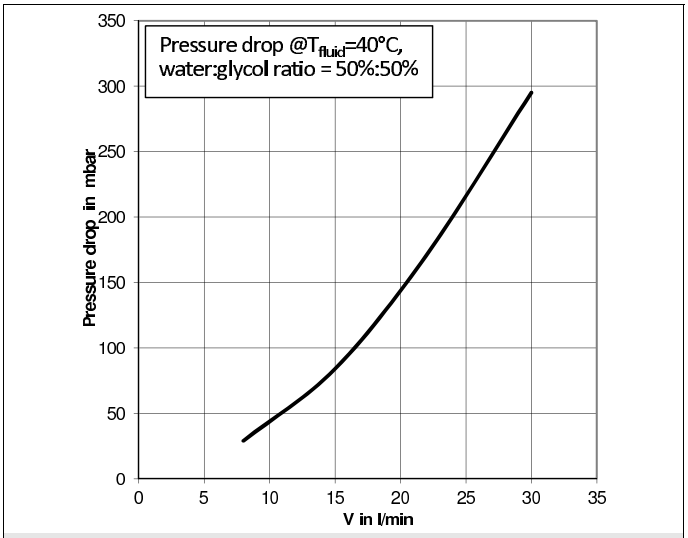
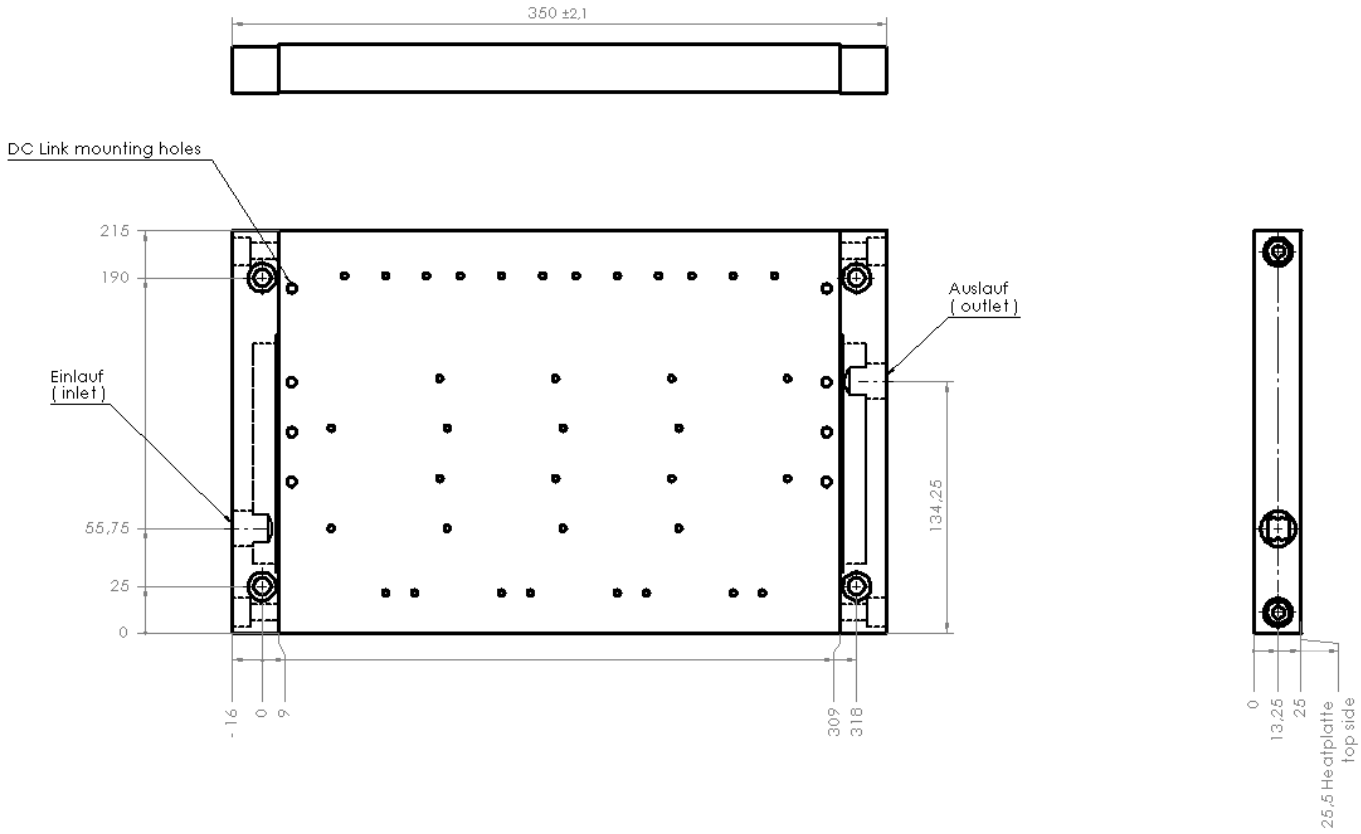


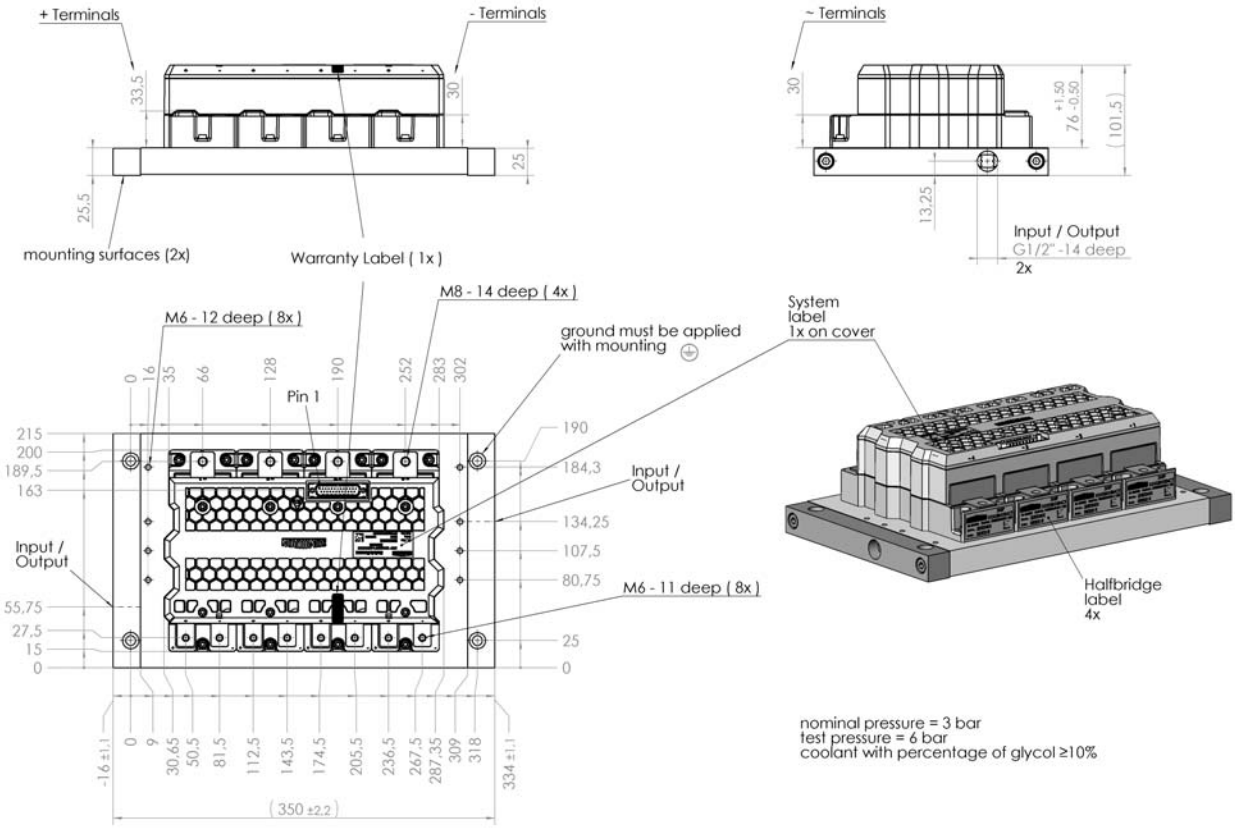
Fig. 10: Pressure drop Δp versus flow rate V



Nenndruck / Kühlsystem = 3 bar
Prüfdruck / Kühlsystem = 6 bar
Kühlmedium mit Glykolanteil ≥ 10%

nominal pressure/cooling system = 3 bar
test pressure/cooling system = 6 bar
coolant with percentage of glycol >=10%

Heat sink



This is an electrostatic discharge sensitive device (ESDS), international standard IEC 60747-1, Chapter IX

* The specifications of our components may not be considered as an assurance of component characteristics. Components have to be tested for the respective application. Adjustments may be necessary. The use of SEMIKRON products in life support appliances and systems is subject to prior specification and written approval by SEMIKRON. We therefore strongly recommend prior consultation of our staff.

SKiiP 2414 GB12E4-4DUW

SKiiP® 4

2-pack-integrated intelligent Power System

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Features

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- Solder free power section
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Typical Applications*

- Renewable energies
- Traction
- Elevators
- Industrial drives

Remarks

For further information please refer to SKiiP®4 Technical Explanation

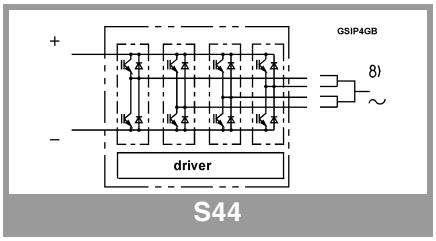
Footnotes

1) With assembly of suitable MKP capacitor per terminal

2) The specified maximum operation junction temperature T_{vjop} is 150°C

Absolute Maximum Ratings				
Symbol	**Conditions**		**Values**	**Unit**
System				
V_{CC} 1)	Operating DC link voltage		900	V
V_{isol}	DC, t = 1 s, each polarity		4300	V
$I_{t(RMS)}$	per AC terminal, rms, sinusoidal current		500	A
$I_{max\ (peak)}$	max. peak current of power section		3600	A
I_{FSM}	T_j = 175 °C, t_p = 10 ms, sin 180°		15885	A
I^2t	T_j = 175 °C, t_p = 10 ms, diode		1262	kA^2s
f_{out}	fundamental output frequency (sinusoidal)		1	kHz
T_{stg}	storage temperature		-40 ... 85	°C
IGBT				
V_{CES}	T_j = 25 °C		1200	V
I_C	T_j = 175 °C	T_s = 25 °C	3109	A
		T_s = 70 °C	2528	A
I_{Cnom}			2400	A
T_j 2)	junction temperature		-40 ... 175	°C
Diode				
V_{RRM}	T_j = 25 °C		1200	V
I_F	T_j = 175 °C	T_s = 25 °C	2369	A
		T_s = 70 °C	1878	A
I_{Fnom}			2400	A
T_j 2)	junction temperature		-40 ... 175	°C
Driver				
V_s	power supply		19.2 ... 28.8	V
V_{iH}	input signal voltage (high)		V_s + 0.3	V
dv/dt	secondary to primary side		75	kV/µs
f_{sw}	switching frequency		10	kHz

Characteristics						
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Unit**
IGBT						
$V_{CE(sat)}$	I_C = 2400 A at terminal	T_j = 25 °C		2.01	2.26	V
		T_j = 150 °C		2.49	2.69	V
V_{CE0}		T_j = 25 °C		0.80	0.90	V
		T_j = 150 °C		0.70	0.80	V
r_{CE}	at terminal	T_j = 25 °C		0.51	0.57	mΩ
		T_j = 150 °C		0.75	0.79	mΩ
$E_{on} + E_{off}$	I_C = 2400 A, T_j = 150 °C	V_{CC} = 600 V		936		mJ
		V_{CC} = 900 V		1680		mJ
$R_{th(j-s)}$	per IGBT switch				0.0159	K/W
$R_{th(j-r)}$	per IGBT switch				0.0115	K/W



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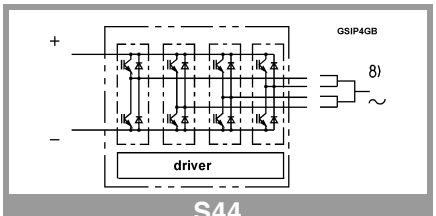

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Characteristics

Symbol	Conditions		min.	typ.	max.	Unit
Diode						
$V_F = V_{EC}$	I_F = 2400 A at terminal	T_j = 25 °C		2.33	2.65	V
		T_j = 150 °C		2.35	2.66	V
V_{F0}		T_j = 25 °C		1.30	1.50	V
		T_j = 150 °C		0.90	1.10	V
r_F	at terminal	T_j = 25 °C		0.43	0.48	mΩ
		T_j = 150 °C		0.61	0.65	mΩ
E_{rr}	I_F = 2400 A T_j = 150 °C	V_R = 600 V		159		mJ
		V_R = 900 V		200		mJ
$R_{th(j-s)}$	per diode switch				0.0281	K/W
$R_{th(j-r)}$	per diode switch				0.0241	K/W
Driver						
V_s	supply voltage non stabilized		19.2	24	28.8	V
I_{S0}	bias current @V_s= 24V, f_{sw} = 0, I_{AC} = 0			360		mA
I_s	k_1 = 33 mA/kHz, k_2 = 0.258 mA/A, f_{out} =50Hz, sinusoidal current		= 360	+ k_1* f_{sw}	+ k_2 * I_{AC}	mA
V_{IT+}	input threshold voltage (HIGH)		0,7*V_s			V
V_{IT-}	input threshold voltage (LOW)				0,3*V_s	V
R_{IN}	input resistance			13		kΩ
C_{IN}	input capacitance			1		nF
t_{pRESET}	error memory reset time		1300		2900	ms
$t_{pReset(OCP)}$	Over current reset time					µs
t_{TD}	top / bottom switch interlock time			3		µs
t_{jitter}	jitter clock time			52	58	ns
t_{SIS}	short pulse suppression time			0.6		µs
t_{POR}	Power-On-Reset completed			3.5		s
V_{CEstat}	Collector-Emitter Threshold Static Monitoring Voltage			7.5		V
t_{bl}	Collector-Emitter Threshold Static Monitoring Blanking Time			6		µs
$I_{digiout}$	digital output sink current (HALT-signal)				16	mA
$V_{it+\ HALT}$	input threshold voltage HIGH HALT (Low -->High)		0,6*V_s			V
$V_{it-HALT}$	input threshold voltage LOW HALT (High --> Low)				0.4*V_s	V
$t_{d(err)}$	Error delay time (from detection to HALT), (depends on kind of error)		1.8		170	µs
I_{TRIPSC}	over current trip level		3525	3600	3675	A_{PEAK}
T_{trip}	over temperature trip level		128	135	142	°C
$T_{DriverTrip}$	over temperature PCB trip level		113	120	124	°C
V_{DCtrip}	over voltage trip level,		950	980	1010	V

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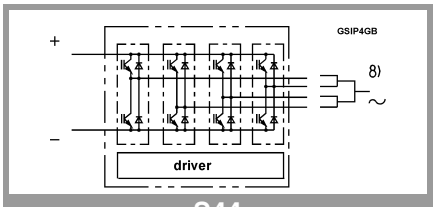
Footnotes

[1] With assembly of suitable MKP capacitor per terminal

[2] The specified maximum operation junction temperature T_{vjop} is 150°C

Characteristics						
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Unit**
System						
$t_{d(on)IO}$	V_{CC} = 600 V I_C = 2400 A T_j = 25 °C	turn on propagation delay time		2.8		µs
$t_{d(off)IO}$		turn off propagation delay time		2.6		µs
dV_{CE}/dt_{on}	T_j = 25 °C V_{CC} = 600 V	I_C = 0 A		9		kV/µs
		I_C = 2400 A		3		kV/µs
dV_{CE}/dt_{off}		I_C = 2400 A		3		kV/µs
$R_{th(s-a)}$	flow rate = 15 l/min, T_{Fluid}=40°C, water/glycol ratio 50%:50%				0.0065	K/W
$R_{CC'+EE'}$	terminals to chip, T_s = 25 °C			0.0675		mΩ
L_{CE}	commutation inductance			4.5		nH
C_{CHC}	coupling capacitance secondary to heat sink			6		nF
C_{ps}	coupling capacitance primary to secondary			0.08		nF
I_{CES} + I_{RD}	V_{GE} = 0 V, V_{CE} = 1200 V, T_j = 25 °C			0.209		mA
M_{dc}	DC terminals		6		8	Nm
M_{ac}	AC terminals		13		15	Nm
w	SKiiP System w/o heat sink			3.22		kg
w_h	heat sink			4.25		kg



S44

Isolation coordination acc. to EN 50178 and IEC 61800-5-1	
Maximum grid RMS voltage, line-to-line, grounded delta mains	480V+20%
Installation altitude for maximum grid RMS voltage,line-to-line, grounded delta mains	4000m
Maximum grid RMS voltage, line-to-line, star point grounded mains	480V+20%
Installation altitude for maximum grid RMS voltage, line-to-line, star point grounded mains	8000m
Maximum transient peak voltage between low voltage circuit and mains	1900V
Pollution degree acc. to IEC 60664-1 outside the moulded power section	2
Overvoltage cat. acc. to IEC 60664-1 for mains	III
Overvoltage cat. acc. to UL 840 within mains	I
Overvoltage cat. acc. to UL 840 between mains and ground	III
Overvoltage cat. acc. to UL 840 between mains and low voltage circuit	III
Basic isolation	between heat sink and mains
Reinforced isolation	between low voltage circuit and mains
Protection level acc. to IEC 60529	IP00

Environmental conditions acc. to IEC 60721

	Storage	Transportation	Operation stationary use at weather protected locations	Operating ground vehicle installations	Operating ship environment
Climatic conditions	1K2 (1)	2K2 (1)	3K3 (1)	5K1 (1)	6K1 (1)
Biological conditions	1B1	2B1	3B1	5B1	6B1
Chemically active substances (excluded: salt spray)	1C2	2C1	3C2	5C2	6C2
Mechanically active substances	1S1	2S1	3S1	5S1	6S1
Mechanical conditions	1M3	(4)	3M6 (2)	5M3 (3)	6M3
Contaminating fluids	---	---	---	5F1	---

(1) expanded temperature range: -40°C / +85°C. Please note: by operation near 85°C the life time of product is reduced.
(2) 3M7 possible, but due to the mechanic load capacity of external components like DC-Link capacitors limited to 3M6
(3) 5M3 without impact of foreign bodies, stones
(4) no declaration due to customer-specific packing

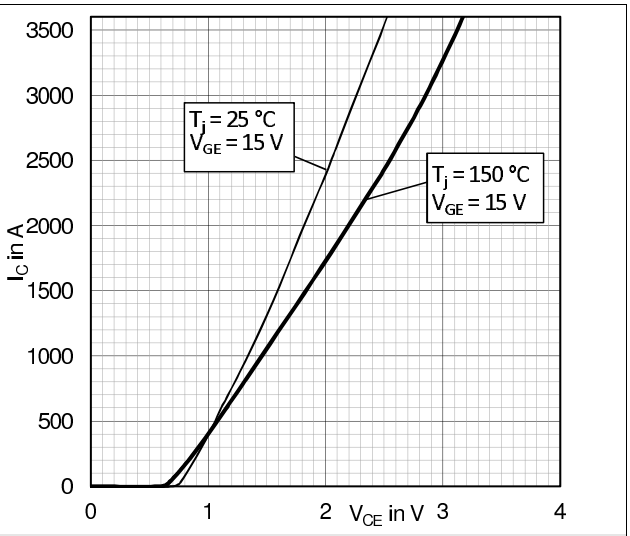


Fig. 1: Typical IGBT output characteristics

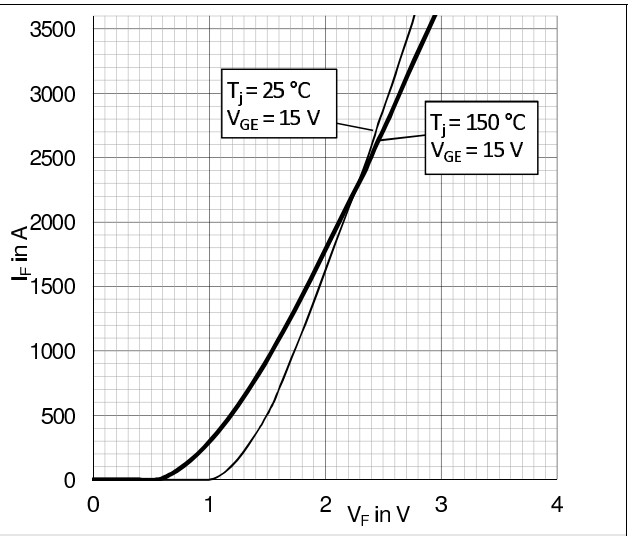


Fig. 2: Typical diode output characteristics

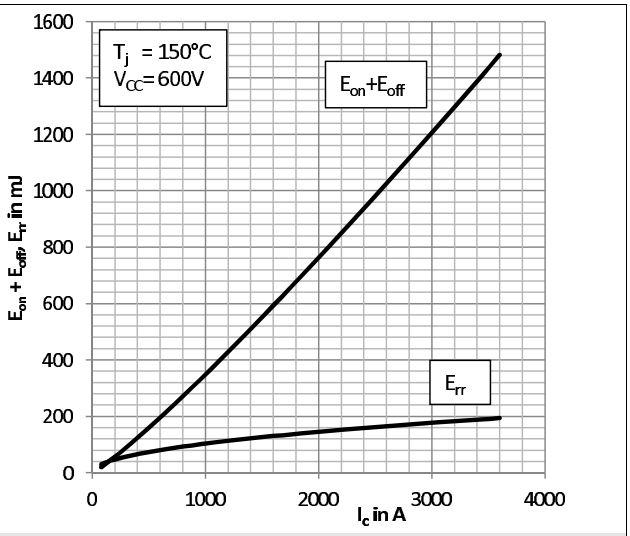


Fig. 3: Typical switching energy E = f(I_c)

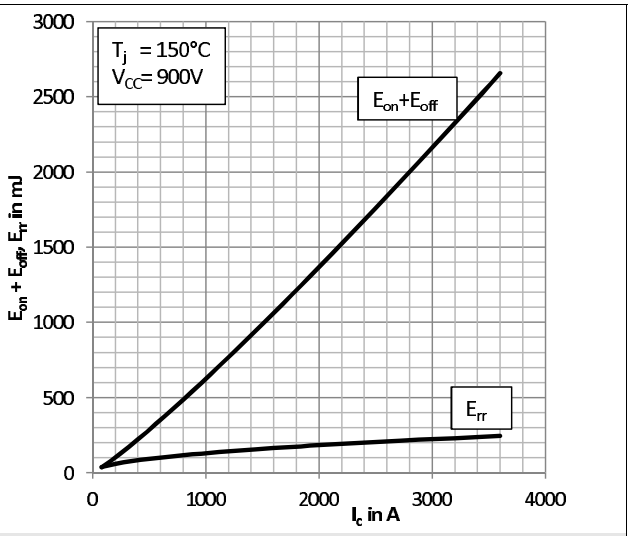


Fig. 4: Typical switching energy E = f(I_c)

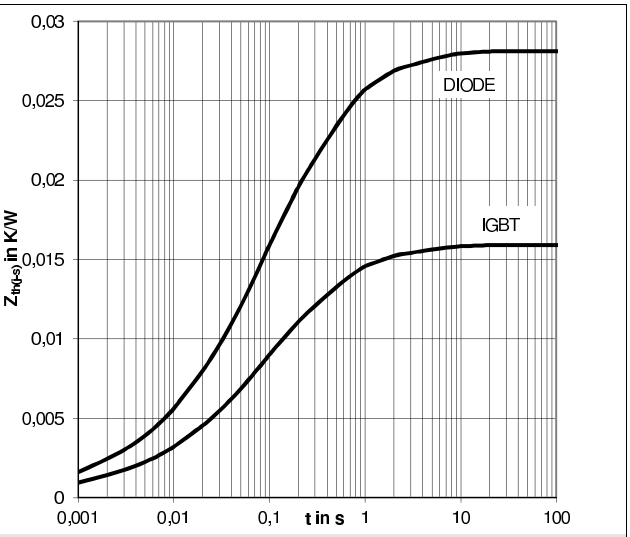


Fig. 5: Transient thermal impedance Zth(j-s)

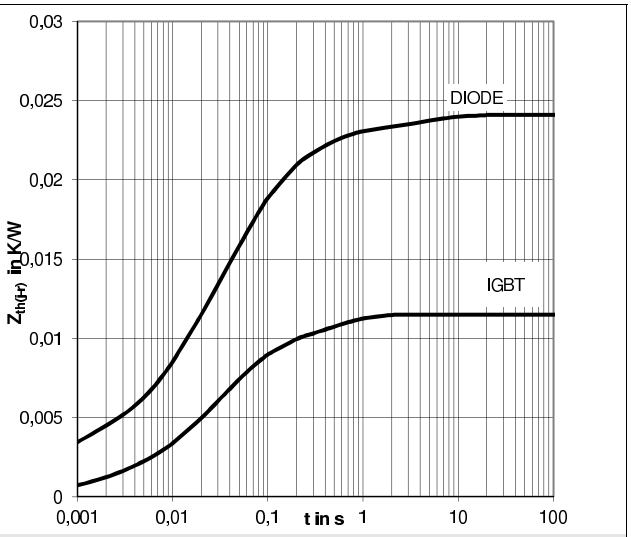


Fig. 6: Transient thermal impedance Zth(j-r)

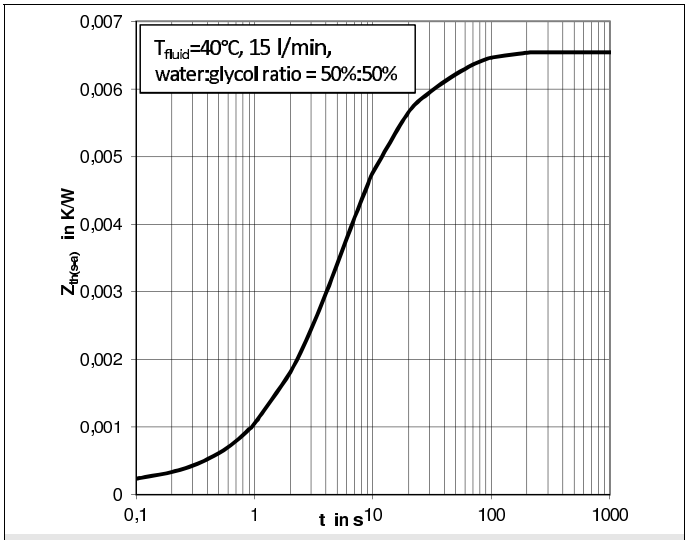


Fig. 7: Transient thermal impedance Zth(s-a)

	R_{th} [K/W]				
	1	2	3	4	5
$Z_{th(j-s)}$ I	0,0011	0,0057	0,0063	0,0019	0,0009
$Z_{th(j-s)}$ D	0,0020	0,0100	0,0112	0,0034	0,0015
$Z_{th(j-r)}$ I	0,0023	0,0056	0,0027	0,0009	
$Z_{th(j-r)}$ D	0,0012	0,0039	0,0104	0,0054	0,0032
$Z_{th(s-a)}$	0,0014	0,0050	0,0001		
	tau [s]				
	1	2	3	4	5
$Z_{th(j-s)}$ I	3,6500	0,4100	0,0650	0,0090	0,0008
$Z_{th(j-s)}$ D	3,6500	0,4100	0,0650	0,0090	0,0008
$Z_{th(j-r)}$ I	0,4500	0,0475	0,0142	0,0016	
$Z_{th(j-r)}$ D	4,1546	0,2644	0,0497	0,0107	0,0005
$Z_{th(s-a)}$	34,2609	5,2284	0,0005		

Fig. 8: Coefficients of thermal impedances

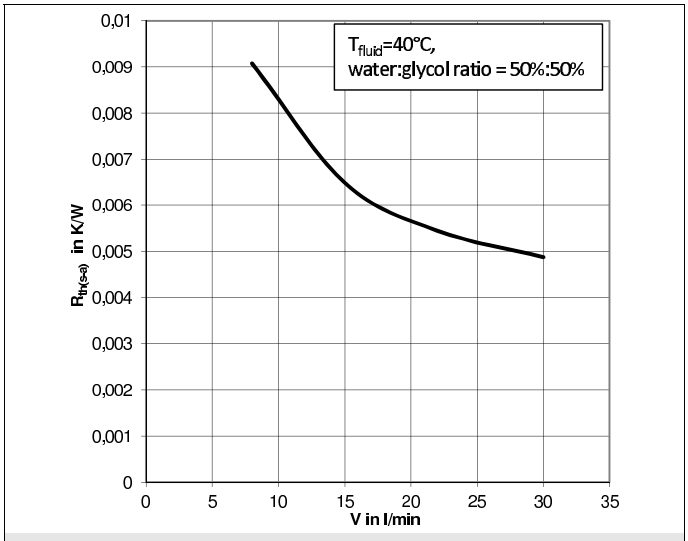


Fig. 9: Thermal resistance Rth(s-a) versus flow rate V

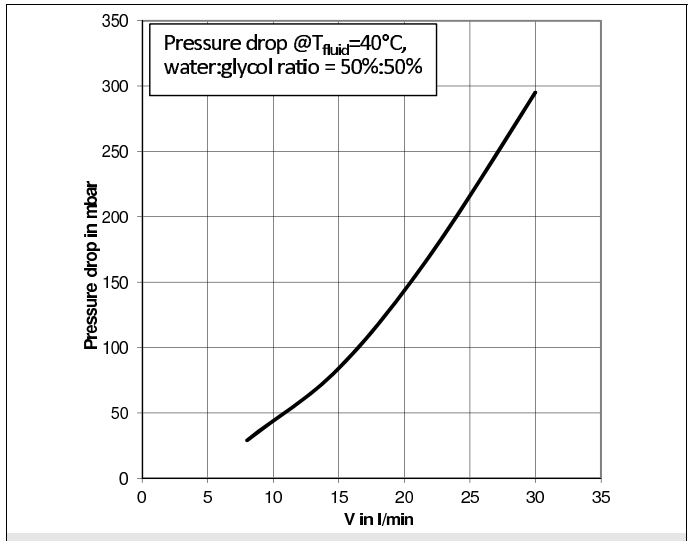
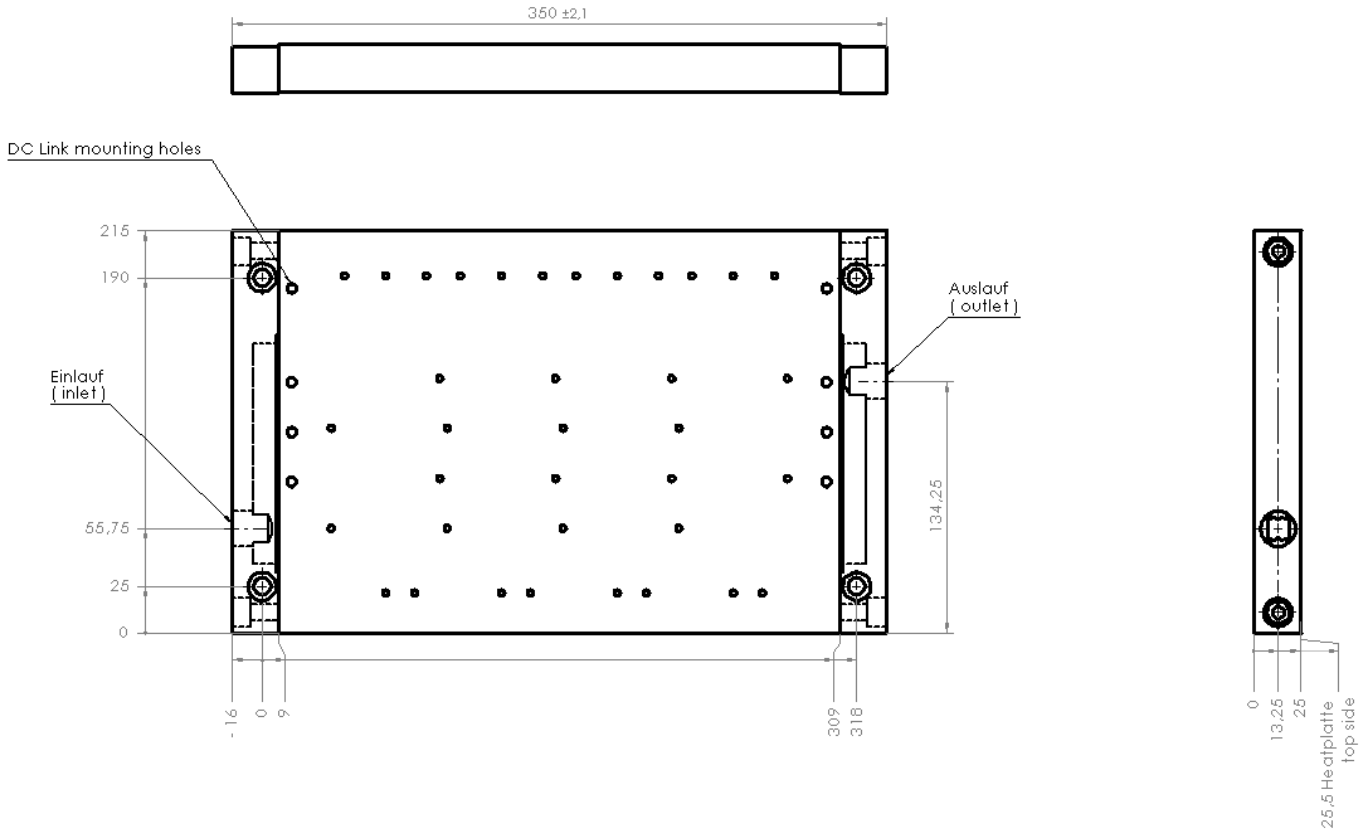


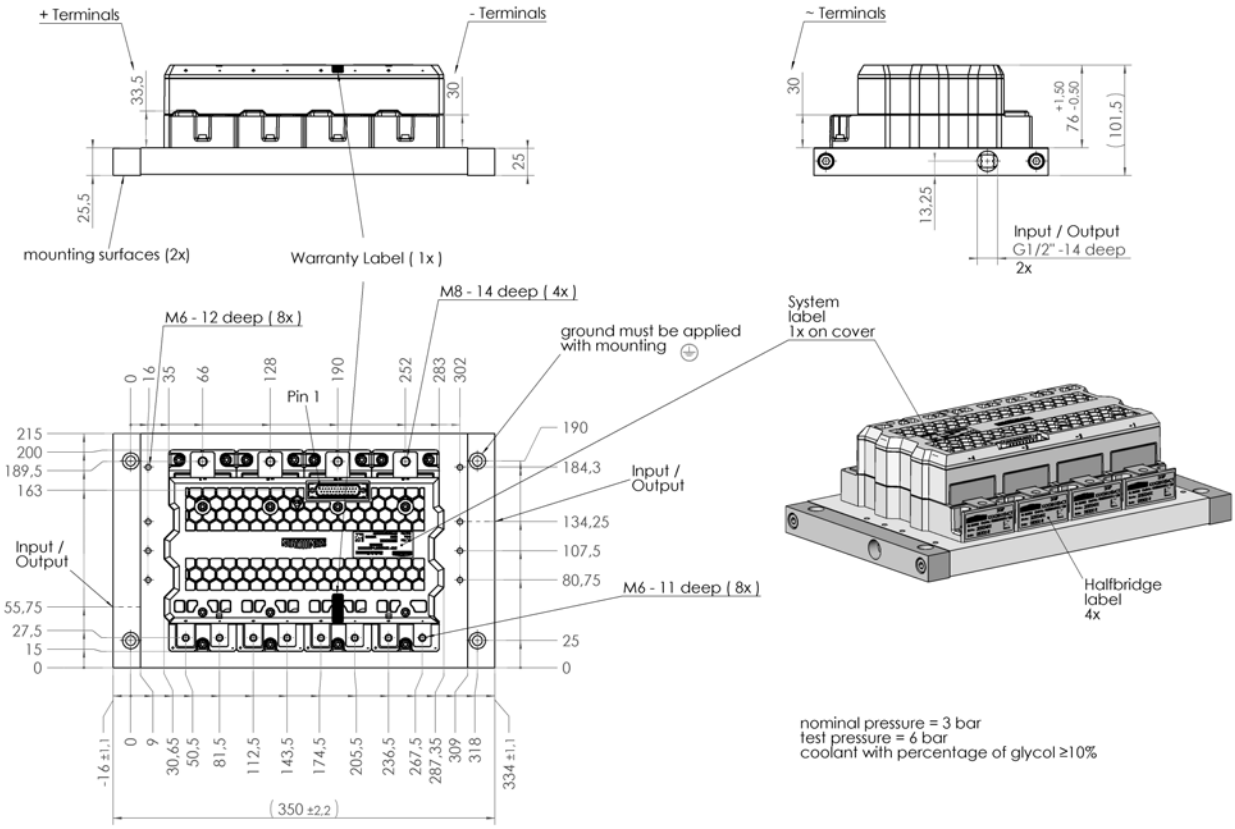
Fig. 10: Pressure drop Δp versus flow rate V



Nenndruck / Kühlsystem = 3 bar
Prüfdruck / Kühlsystem = 6 bar
Kühlmedium mit Glykolanteil ≥ 10%

nominal pressure/cooling system = 3 bar
test pressure/cooling system = 6 bar
coolant with percentage of glycol >=10%

Heat sink



This is an electrostatic discharge sensitive device (ESDS), international standard IEC 60747-1, Chapter IX

* The specifications of our components may not be considered as an assurance of component characteristics. Components have to be tested for the respective application. Adjustments may be necessary. The use of SEMIKRON products in life support appliances and systems is subject to prior specification and written approval by SEMIKRON. We therefore strongly recommend prior consultation of our staff.