High Temperature Thermoelectric Device Concept Using Large Area *PN* Junctions

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List of Symbols (unless otherwise stated)

∇ - Gradient

α - Seebeck coefficient

Δ - Change in ...

ϵ - Error

φ - Electrochemical potential

η - Efficiency

η_{D} - Ideality factor

κ - Thermal conductivity

K - Thermal conductance

λ - Mean free path

μ - Carrier mobility

Π - Peltier coefficient

Θ - Heat capacity

ρ - Electrical resistivity

σ - Electrical conductivity

Σ - Sum of ...

τ - Transit time

ω - Angular frequency

Ω - Ohms

A - Area

$D(E)$ - Density of states

$\mathbf{E}$ - Electric field

E - Energy

E_{F} - Fermi level

E_{g} - Bandgap energy

$f(E)$ - Fermi function

G - Electrical conductance

h - Plank's constant

I - Electric current

I_0 - Reverse bias current

$\mathbf{J}$ - Electric current density

$\mathbf{J}_\mathrm{q}$ - Heat current density

k_B - Boltzmann constant

K - Kelvin

L - Length

m - Meters

m_e^* - Effective mass of electrons

m_h^* - Effective mass of holes

$M(E)$ - Number of modes

n_i - Intrinsic carrier concentration

N - Newton

N_c - Effective density of states in the conduction band

N_v - Effective density of states in the valence band

N_A - Acceptor doping concentration

N_D - Donor doping concentration

$N(E)$ - Number of charge carriers

P - Power

q - Elementary charge

Q - Heat current

R - Electrical resistance

t - Time

T - Temperature

$T(E)$ - Transmission probability

T_{c} - Cold side temperature

T_{h} - Hot side temperature

V_{b} - Built in voltage

V - Volts

W - Watts

1 Introduction

> The problem is, we think we have time.
>
> Unknown

1.1 The Energy Problem

The main driving force that fuels the push for renewable energies and a reduction of fossil fuels does not seem to steam from a sense of responsibility or protection of the planet, but from an urgent need to satisfy the global energy demand as rising costs have made otherwise expensive alternative energies more competitive. Strictly speaking, thermoelectricity is not intrinsically a renewable energy because it may be implemented in the form of heat waste recovery where the wasted heat from the combustion of fossil fuel is harvested or in the form of a solar-thermal system in which solar energy is absorbed to produce heat. The latter case being the example of a renewable energy.

In order to realize the need and motivation (moral or practical) to search for alternatives to satisfy the world's energy demand, it is necessary to bring some perspective to know where renewable energies stand with respect to other energy sources and to what extent they can change the course of things. Figure 1.1 shows the distribution of fuels needed to satisfy the world energy demand in the years of 1973 and 2009. The category other*** contains the sum from alternative energies such as solar, geothermal, and wind. While

alternative energies have seen an 10-fold increase in the last 39 years, they are still lacking to be a global change as they only produce about 1 percent of the global energy today, hence research efforts should continue in order to develop successful renewable energy sources.

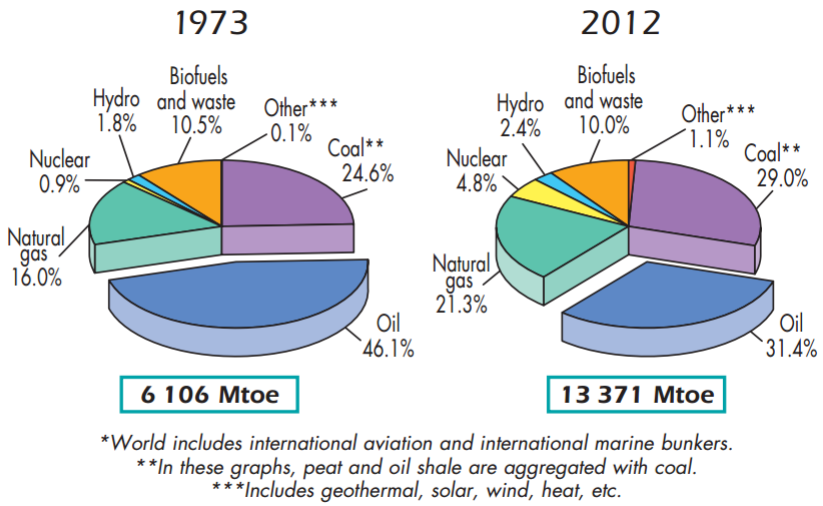

Figure 1.1: World energy as provided per different fuels [1]. (TOE is a unit of energy defined as the amount of energy released by burning one tonne of crude oil).

As far as the potential for thermoelectrics to play a role as an alternative energy, recall from Figure 1.1 that the vast majority of the world energy is produced by burning different forms of fossil fuels, which means that the efficiency of this thermodynamic process is limited by Carnot's efficiency which is defined by the operating temperatures. Carnot's efficiency for most combustion processes has remained between 20-50% [2], and this has to do with the difficulties in finding high temperature stable materials.

Figure 1.2 shows the energy distribution in the United States. The breakdown is interesting but the main point in this context is that around 60% of the total energy is wasted and most of that energy waste is in the form of heat since most of the energy comes from combustion of fossil fuels, hence theoretically there is much room where thermoelectric technologies could assist conventional fossil fuel system to be more efficient. If only 1% of all lost heat is recovered, thermoelectricity would contribute as much as all other

alternative energies combined, hence the potential for thermoelectricity is there.

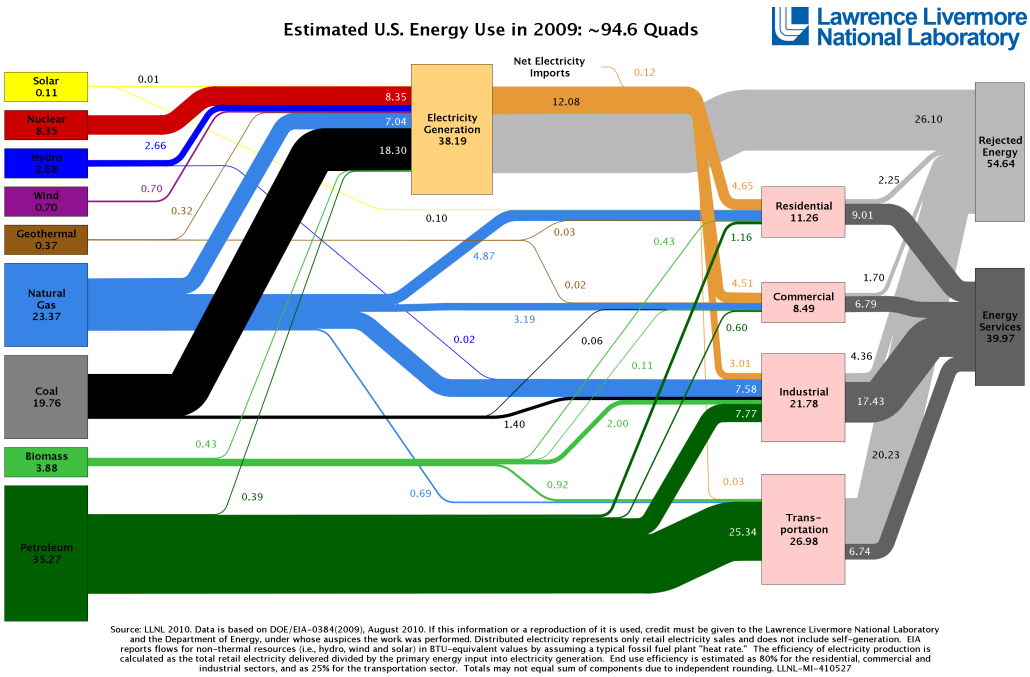

Figure 1.2: Break down of energy resources in the U.S. ($1\,\text{Quad} = 1.055 \times 10^{18}\,\text{J}$).

Thermoelectricity despite discovered almost 200 years ago remains as a low efficiency technology and this has limited its applications to deep space exploration where solar energy is no longer available. On earth most of the usage of thermoelectric devices is as solid state heat pumps and very limited commercial electricity generation applications. Thermoelectric devices are traditionally made from semiconductor materials since their electrical properties can be readily tunned. Traditionally a thermoelectric device consists of an intercalating series of p-type and n-type semiconductors connected electrically in series and thermally in parallel, sandwiched between two substrates were the interconnects are located.

In this work a new device architecture is tested experimentally; a thermoelectric generator (TEG) is built by joining the complementary doped silicon legs together forming a large area PN junction that acts a mechanical and electrical junction. The combination

of a PN junction and a TEG gives rise to the therm PN-TEG. In a PN-TEG the hot side substrate is no longer needed, and this provides technological advantages because it eases the fabrication process and opens the door for high temperature applications. The nanostructured silicon PN-TEGs presented in this work are shown to be competitive with equivalent conventional technologies, and some of the fundamental working principles are proposed and experimentally demonstrated.

2 Transport Theory

> Scientists are called to see what
> everyone else has seen and think
> what no one else has thought before.
>
> Albert Szent-Gyorgyi

2.1 The Adapated Landauer Approach

In the following sections, some of the thermoelectric phenomenon relevant to this work are introduced using an adaptation on the Landauer model. In 1957 Landauer proposed a model for metallic electrical resistance, in which he considered current as an integral over the transmission probability [3]. This model was later adapted to explain thermoelectric phenomena [4, 5], and following this adaptation, some thermoelectric aspects will be introduced. The starting point for this approach is an elastic resistor where all scattering energy is conserved and inelastic contacts that maintain equilibrium conditions where all energy transfer occurs. From this starting point, relevant thermoelectric phenomena is introduced and most importantly, it will be shown that by starting Landauer model, great insight can be gained on fundamental mechanics of thermoelectric phenomena at the quantum level that are otherwise invisible.

2.2 Electrical Current Due to Voltage Difference

From conventional electronics theory, Ohm's Law, the proportionality between unipolar electrical current density **J** and electric field **E** is derived from Drude's model and written as:

$$\mathbf{J} = \underbrace{qn\mu}_{\sigma}\mathbf{E} \tag{2.1}$$

where q is the elementary charge, n the carrier concentration, μ the mobility and σ the electrical conductivity. While equation 2.1 is extremely practical, it has abstracted much information that is important to understand some thermoelectric aspects. Consider the elastic resistor in Figure 2.1, recall that the channel is connected to ideal contacts that maintain near-equilibrium conditions. Each contact is described by a electronic thermodynamic occupation equilibrium described by the Fermi function:

$$f_{1,2}(E) = \frac{1}{1 + \exp\left(\frac{E - E_{F1,2}}{\kappa_B T_{1,2}}\right)} \tag{2.2}$$

where E is energy, E_{F} is the Fermi level which depends on the voltage of the contacts, κ_B is Boltzmann constant, T the temperature of the contacts and the subscripts refer to the contact. The Fermi function is a probabilistic description of whether a given energetic state should be filled with an electron or not, and since the contacts are connected to a battery they will try to maintain this equilibrium condition by providing any needed electrons or removing them.

If one considers that the general expression for the number of carriers at every energy level is given by:

$$N(E) = D(E)f(E) \tag{2.3}$$

where $D(E)$ is the density of states, then the differential change of the number of carriers at each contact (assume electrons for simplicity) due to a differential change in the Fermi

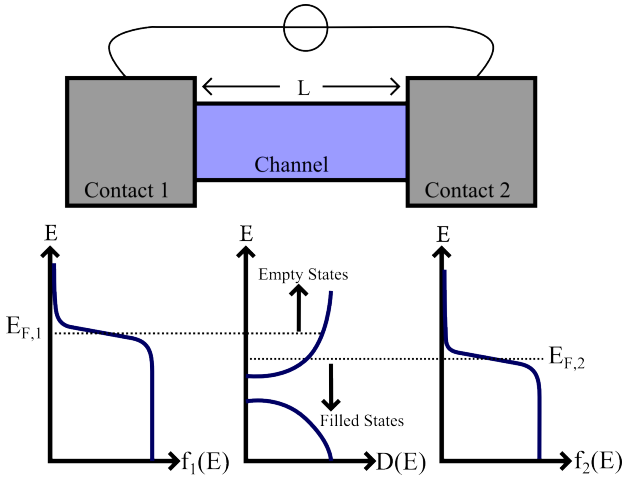

Figure 2.1: Current flow due to different Fermi functions.

function due to an applied voltage can be written as:

$$N_{1,2}(E)dE = D(E)f_{1,2}(E)dE \tag{2.4}$$

If it is assumed that all non equilibrium carriers reach the opposite contact, then the rates for the number of electrons injected or extracted per unit time between the contacts and the channel can be written as:

$$\frac{dN_{1,2}(E)}{dt} = \frac{N_{1,2}(E) - N_0(E)}{\tau(E)} \tag{2.5}$$

where $\tau(E)$ is the transit time and assumed to be the same for both contacts, and $N_0(E)$ is the number of electrons in the channel. From the rate equations above as a starting point, the electrical current in the channel can be written using Landauer's expression for conductance as follows [5]:

$$I = \frac{2q}{h}\int \frac{\lambda(E)}{\lambda(E)+L}M(E)(f_1(E) - f_2(E))dE \tag{2.6}$$

here h is Planck's constant, $\lambda(E)$ is the mean free path of the charge carriers, $M(E)$ is

known as the number of conducting channels (modes) and is related to $D(E)$, and L is the length of the conducting channel. For further reference and simplicity, written as:

$$I = \frac{2q}{h} \int T(E)M(E)(f_1(E) - f_2(E))dE \tag{2.7}$$

and for small biases after a Taylor's expansion and differentiation rewritten as:

$$I = V \underbrace{\frac{2q^2}{h} \int T(E)M(E) \left(-\frac{\partial f_0}{\partial E}\right) dE}_{G} \tag{2.8}$$

V is the applied voltage and $f_0 \approx f_1 \approx f_2$. Equation 2.8 is basically Ohm's law in a very general form. The advantage of describing current flow using the Landauer formalism is that it can be applied to any dimensional system and explaining current flow follows directly from thermodynamic arguments. There are some restrictions to equation 2.8 but the take away is that electric current flows due to a difference of the Fermi functions. A final and important remark is that as long as $T > 0\,\mathrm{K}$ electrical conduction occurs from contributions mainly from energy states between $E_{F,1}$ and $E_{F,2}$, this is seen in Figure 2.1 and in equations 2.7 and 2.8. Seeing electrical current flow in this frame will provide very important insight to understanding thermoelectric phenomenon.

2.3 Electrical Current Due to Temperature Difference

From the previous section it is clear that electrical current will flow if either (or both) the Fermi level or the temperature on the contacts differ. The same elastic resistor from the previous section is again considered, but with two fundamental differences: this time with the contacts in a shortcut configuration such that $E_F = E_{F,1} = E_{F,2}$ but at different temperatures. For simplicity the cold electrode is at $T_2 = 0\,\mathrm{K}$ with $T_1 > T_2$. A schematic

is shown in Figure 2.2.

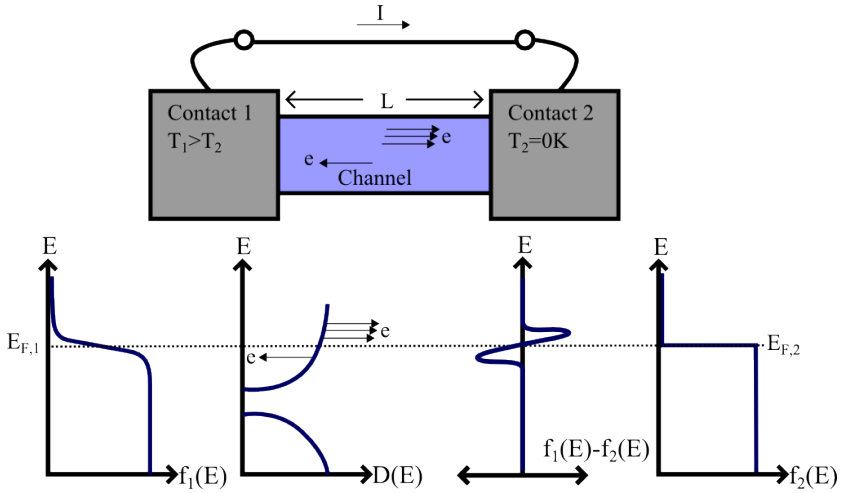

Figure 2.2: Current flow due to different temperatures

Equation 2.7 can be combined with Figure 2.2 to realize that the contribution to the electrical current for energy levels below E_F is negative since $f_1(E) - f_2(E) < 0$ for energies below E_F:

$$\frac{2q}{h}\int_0^{E_F} T(E)M(E)(f_1(E) - f_2(E))dE < 0 \tag{2.9}$$

and similarly the contribution to the electrical current for energy levels above E_F is positive since $f_1(E) - f_2(E) > 0$ above E_F:

$$\frac{2q}{h}\int_{E_F}^{\infty} T(E)M(E)(f_1(E) - f_2(E))dE > 0 \tag{2.10}$$

The net direction of the current flow is determined by $D(E)$, since $M(E) \propto D(E)$. In an n-type material with a parabolic band, $D(E)$ is larger above E_F than below and as a consequence more electrons flow in one direction than the other as sketched in Figure 2.2. For p-type semiconductors the model does not need to be modified; in the case of a p-type semiconductor, the Fermi energy is found in the valence band, and using the same analysis we can arrive at the conclusion that the direction of the electrical current will reverse.

A couple of remarks that fall out from this model: 1) It is known from thermodynamics that heat is a high entropy form of energy; very disorganized, and so converting heat to electricity sounds like a tedious and inefficient process; one would have to effectively transfer every atomic vibration into electrical power. This idea is beautifully shown by the fact that $D(E)$ does not differ by much below and above E_{F}. Although all together a large amount of current may flow, the net current output will be proportional to the difference in $D(E)$ below and above E_{F} which is small for a parabolic band assumption. 2) From this last reason the motivation to lower scale and electronic band engineering structures becomes evident because since asymmetry in $D(E)$ around E_{F} enhances the thermoelectric conversion process.

Seebeck Coefficient

The Seebeck coefficient α is defined as $\alpha = V_{\mathrm{oc}}/\Delta T$ where V_{oc} is the open circuit output voltage of an isotropic material that is exposed to a small temperature difference $\Delta T = T_h - T_c$ where T_h and T_h are the hot side and cold side temperatures at the two ends of the material where the voltage is measured. In some thermoelectric textbooks the Seebeck coefficient despite being one of the most important quantities in thermoelectricity is not derived from a solid state physics model (e.g. Boltzman theory) [6, 7, 8]. Perhaps the reason of avoiding the derivation lays in the mathematical complexity and assumptions needed to derive the Seebeck coefficient. Unfortunately this abstraction erodes insight into the inner workings of thermoelectricity. Using the Landauer approach it is possible to derive the Seebeck coefficient with much less mathematical rigor than it is required when deriving it from the Boltzmann transport equation. Here is not derived but shown how the Seebeck coefficient falls out from a solid state physics model with less mathematical rigor while retaining important information.

A starting point to see where how Seebeck coefficient comes out from the Landauer approach from is equation 2.7 since it is the general form describing electrical current. Since

the Fermi function is dependent on both the Fermi energy and temperature, $f_1(E) - f_2(E)$ can be approximated using the first term of a Taylor's series expansion around E_F and T:

$$I = \frac{2q}{h} \int T(E)M(E) \left[\frac{\partial f}{\partial E_F} \left(E_{F,1} - E_{F,2} \right) + \frac{\partial f}{\partial T} \left(T_1 - T_2 \right) \right] dE \tag{2.11}$$

allowing $q\Delta V = E_{F,1} - E_{F,2}$ and after differentiation and rearrangement of terms:

$$\begin{aligned} I = & \Delta V \underbrace{\frac{2q^2}{h} \int T(E)M(E) \left(\frac{-\partial f_0}{\partial E} \right) dE}_{G} \\ & + (T_1 - T_2) \underbrace{\left[-\frac{2q}{h} \int \frac{E - E_F}{T} T(E)M(E) \left(\frac{-\partial f_0}{\partial E} \right) dE \right]}_{G_s} \end{aligned} \tag{2.12}$$

the first term is recognized as the electrical conductance (see equation 2.7) and the second term given the name G_s. Then the current is written in the more familiar way:

$$I = G\Delta V + G_s \Delta T \tag{2.13}$$

and given open circuit conditions a proportionality between V_oc and ΔT appears which is the definiton of the Seebeck coefficient

$$V_\mathrm{oc} = - \underbrace{\frac{G_s}{G}}_{\alpha} \Delta T \tag{2.14}$$

Dividing the coefficients G_s and G from equation 2.12 shows how the Seebeck coefficient is related to some of the solid state properties of the material. This can also be shown from Boltzman theory, but in this case requiring less mathematical rigor.

$$\alpha = -\frac{k_B}{q} \frac{\int \frac{E - E_F}{k_B T} T(E)M(E) \left(\frac{-\partial f_0}{\partial E} \right) dE}{\int T(E)M(E) \left(\frac{-\partial f_0}{\partial E} \right) dE} \tag{2.15}$$

Lastly, noting that $G_s = \alpha G$, equation 2.13 is rewritten in the most familiar form:

$$I = G\Delta V + \alpha G \Delta T \tag{2.16}$$

2.4 Heat Current

At the atomic level, temperature is a concept that is defined in terms of kinetic energy. When it said that something is hot, the atoms and electrons have gained high kinetic energy and it is said that magnitude of the atomic vibrations has increased for atoms and that valence electrons occupy higher energetic states. Heat is transported by the collective vibration of atoms, by the scattering of electrons and if electrical current is flowing, by electric current.

Open Circuit Thermal Conduction

When no electric current flows, phonons transport the heat in the form of lattice vibrations and electrons transport the heat by inelastic collisions. This is known as the linear approximation of Fourier's heat law [9]:

$$Q_{\text{open}} = -K_J \Delta T \tag{2.17}$$

with $K_J = K_e + K_L$ where K_e is the electronic contribution and K_L the lattice contribution. Here care must be taken because while Fourier's law is defined in open circuit conditions, it is also valid in closed circuit conditions.

Closed Circuit Thermal Conduction

When electric current flows, electrons carry energy with them as they move along the crystal. The amount of energy that electrons carry due to current flow is measured with respect to the Fermi energy. Once again Landauer's expression for conduction in equation 2.7 is adapted easily to describe the heat that each electron will exchange at a the

abrupt interface of two materials, typically a metal-semiconductor interface. In this case each electron carries an amount of heat equal to $E - E_F$ instead of an amount of charge q. Then replacing charge for heat, leads to almost the same expression as equation 2.7:

$$Q_{\text{closed}} = \frac{2}{h} \int (E - E_F) T(E) M(E) (f_1 - f_2) dE \tag{2.18}$$

As it was done with the Seebeck coefficient, expanding with a Taylor's expansion and differentiating equation (2.18), the electronic heat transport becomes [5][1]:

$$Q_{\text{closed}} = -\alpha T G \Delta V - K_E \Delta T \tag{2.19}$$

here the closed circuit thermal conductance $K_E = \alpha \Pi G + K_J$ is introduced. Note that K_E includes the *open* circuit contribution K_J. This is because as mentioned earlier Fourier's law continues to be valid in closed circuit conditions. Finally using the substitution ($\Pi = \alpha T$) where Π is the Peltier coefficient, and substituting ΔV from equation (2.16), equation (2.19) becomes:

$$Q_{\text{closed}} = -\Pi I - K_J \Delta T \tag{2.20}$$

From equation (2.20) it follows that heat is transported when a material is subject to a temperature difference or to a voltage difference. The first term in equation (2.20) refers to the heat transported by the Peltier effect, which due to its importance in this work, will be have a dedicated section and the second term is the linear approximation of Fourier's law. Thermal conductivity measurements in short circuit conditions are very difficult, hence the thermal conductivity is usually measured in open circuit conditions ignoring the term $\alpha \Pi G$.

[1] Page 88

2.5 Coupled Tranport: Electricity and Heat

A short but important note is the interrelation between heat and electronic transport. That means that if a ΔT is applied to a material heat will flow, and (if connected to a load) electricity will flow as well. On the converse, if a ΔV is applied, electric current will flow and as a consequence heat will flow as well. Hence, in semiconductor materials, heat transport implies electric transport and vice versa. Equations (2.16) and (2.20) can be rearranged and put in vector form next to each other and as follows from the application that Callen [10] made to Onsager's reciprocal relations [11], and most recently revisited by Goupil [9]:

$$\begin{aligned} \mathbf{J} &= \sigma\mathbf{E} - \sigma\alpha\nabla T \\ \mathbf{J}_Q &= \Pi\mathbf{J} - \kappa_J\nabla T \end{aligned} \tag{2.21}$$

The relations in (2.21) describe thermal and electric transport for unipolar materials in near equilibrium conditions. Diffusion of charge carriers is neglected.

2.6 The Peltier Effect in Bipolar Semiconductors

In the previous sections a Peltier coefficient Π resulted from the heat balance equations, but the physical mechanism was not explained and it will be seen in later chapters that the Peltier effect plays a critical role in this work, hence a full section is dedicated to it. When electric current flows through the interface of two materials with different band structure, such a metal-semiconductor interface, charge carries experience a change in energy with respect to the Fermi energy as they enter or leave the semiconductor and Peltier heating or cooling occurs as shown in Figure 2.3.

The amount of energy that each electron exchanges with the lattice at the interface is

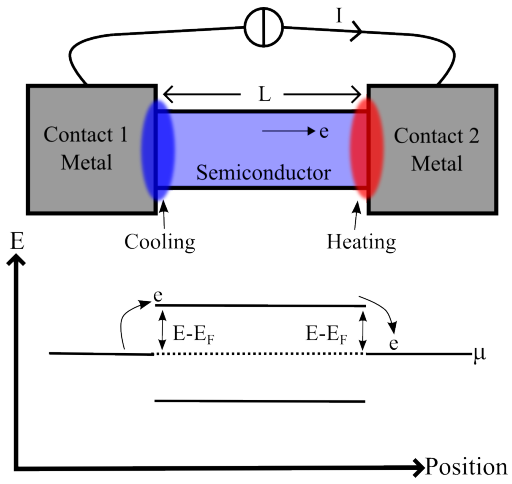

Figure 2.3: Peltier effect in an n-type semiconductor

equal to $E - E_F$. This becomes clear when equation (2.15) is combined with Thomson's relation to write the Peltier coefficient:

$$\Pi = \frac{1}{q} \frac{\int (E - E_F)\, T(E) M(E) \left(\frac{-\partial f_0}{\partial E}\right) dE}{\int T(E) M(E) \left(\frac{-\partial f_0}{\partial E}\right) dE} \tag{2.22}$$

Figure 2.3 illustrates the Peltier effect and equation (2.22) the Peltier coefficient for unipolar conduction. The Peltier heat transport at an interface between two materials A and B is traditionally written as:

$$Q_{\text{Peltier}} = I \left(\Pi_A - \Pi_B\right) \tag{2.23}$$

in equation (2.23) the assumption is that electric transport is unipolar and typically involves a metal-semiconductor interface and the Peltier coefficient of the metal is assumed to be zero. Despite extensive research and numerous publications by Gurevich and his collaborators, a question that remains open is the full description of the Peltier effect and heat fluxes in bipolar transport such as in a PN junction [12, 13, 14, 15, 16, 17].

If a bipolar device is considered, such as a PN junction, it is no longer possible to directly apply equation (2.23) to the metal-semiconductor and semiconductor-semiconductor inter-

faces, and a much more difficult case opens where special care needs to be taken to account for minority charge carriers. Amongst the first to identify this were R.N. Hall [18] in 1961 and W. Bullis in 1963 [19]. The Peltier effect can have 3 special cases in PN junctions and they are discussed in the following to show the different treatment that can be given to the thermoelectric phenomena of a PN junction.

Case 1: Non-Radiative Recombination

This is perhaps the case that fits best to the PN junctions discussed in this work, as there is no electroluminescence. In this case it is assumed that the n-type and p-type regions of the diode are much larger than the minority charge carrier diffusion length, and that all minority charge carriers recombine and releasing their energy as heat at the junction. For ease of discussion, it is assumed that they recombine in the space charge region of the diode, and ohmic voltage drops are ignored. Consider Figure 2.4 (only electrons are

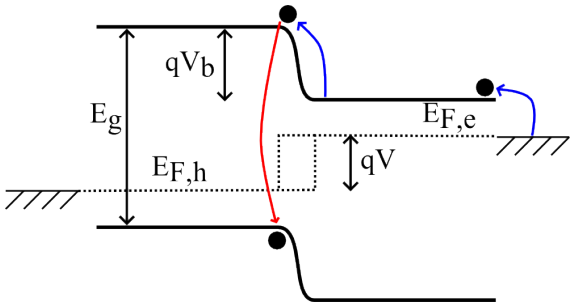

Figure 2.4: Non-radiative recombination: the blue arrows indicate cooling while the red arrow indicates heating.

shown). At the contacts, the Peltier effect does not change with respect to the previous discussion, only the quasi-Fermi energies for electrons and holes $E_{F,e}$ and $E_{F,h}$ need to be considered instead of the Fermi energy E_{F}. However, at the junction each electron must absorb heat to overcome the built in potential barrier qV_b, and as it recombines, it releases the energy E_g which gets absorbed by the lattice leading to a localized heating of the junction. Hence the heating mechanism at the junction is technically not a Peltier effect, but a non-radiative recombination heating. It is interesting to note that this effect

is dependent on the applied Voltage V since it controls the built in barrier height. Given no radiative recombination the junction heating can be expressed as [20, 7]

$$Q_{\text{recomb}} = I\frac{E_g}{q} - I\left(V_b - V\right) \tag{2.24}$$

It is important to note that a Peltier coefficient does not appear in equation (2.24). That means that in the case of non radiative recombination, Peltier cooling occurs at the metal-semiconductor interfaces with special care to take the quasi-Fermi energy instead of the Fermi energy, while heating occurs at the PN junction.

Case 2: Radiative Recombination

The second case is radiative recombination. In a thought experiment if it is assumed that all recombined charge carriers produce photons, then the PN junction will see a refrigeration effect because the energy that charge carriers absorb from the lattice at the metal-semiconductor interface and at the potential barrier, is transfered to photons. And in fact in the highly ideal case, there are no sources of heat. In reality this is quite impractical because very high quantum efficiency (photon/electron) would be required for this type of cooling to be larger than the heating mechanisms (Joule heating and non-radiative recombination) [21]. However impractical, this shows that electrical energy can be transfered to electromagnetic energy leading to a cooling of the PN junction.

Case 3: Short-leg Approximation

The third case also shows a refrigeration effect at the PN junction but for different reasons. In the short-leg approximation the semiconductor legs are assumed to be shorter than the minority diffusion length such that recombination occurs at the contacts. That means that a cooling effect will be present at the PN interface as charge carriers overcome the potential barrier, but since the semiconductor material is shorter than the minority diffusion length, the charge carriers diffuse all the way to the ohmic contacts leading to a

net cooling of the PN junction and heating of the metal-semiconductor interfaces [22, 23].

2.7 The Thomson Effect

It is noted and shown in [9] that in unipolar semiconductors the separation of the Thomson and the Peltier effect is artificial, and that they refer to the same effect which is a gradient of the Seebeck coefficient. Traditionally when spoken about the Peltier effect, the gradient in α comes from having two different materials. However when the temperature gradient is steep enough, $\alpha(T)$ will vary spatially, and differential slides of the material can be thought of as "different" materials.

Taking the divergence of the heat flux $\mathbf{J}_Q$ gives

$$\nabla \cdot \mathbf{J}_Q = T\mathbf{J} \cdot \nabla\alpha + \mathbf{J} \cdot \mathbf{E} - \frac{J^2}{\sigma} - \nabla \cdot (\kappa_L \nabla T) \tag{2.25}$$

where the term $T\mathbf{J} \cdot \nabla\alpha$ refers to the Peltier-Thomson term, and the other terms are the familiar expressions for electrical work, and electrical dissipation and heat conduction. Looking closer at the heat production from the Peltier-Thomson term one finds that

$$T\mathbf{J} \cdot \nabla\alpha = \mathbf{J} \cdot (\nabla\Pi - \alpha\nabla T) \tag{2.26}$$

and from equation (2.26) it becomes evident that the Peltier-Thomson term can take two forms: the first, in isothermal conditions the gradient in Π comes from the interface of two different materials,

$$\mathbf{J} \cdot (\nabla\Pi - \alpha\nabla T) = \mathbf{J} \cdot \nabla\Pi \tag{2.27}$$

equation (2.27) is related to the Peltier effect. A second term appears when a homogeneous

material under a temperature gradient is considered. In that case

$$\mathbf{J} \cdot (\nabla \Pi - \alpha \nabla T) = \mathbf{J} \cdot \left(\frac{d\Pi}{dT} - \alpha \right) \nabla T \tag{2.28}$$

and equation (2.28) is related to the Thomson effect. However both terms fall out from the same expression, hence the "artificial" separation. Typically, the Thomson effect is ignored because the theoretical models, the Landauer model and Onsager's relations in this case are based on a linear approximation for small disturbances which make use of temperature independent properties. In this work large temperature differences are applied, so care needs to be taken because although not treated explicitly, Thomson effects might be present.

3 Conventional Thermoelectric Generator: TEG

> Education is an admirable thing, but it is well to remember from time to time that nothing that is worth knowing can be taught.
>
> Oscar Wilde

3.1 Efficiency of the Thermoelectric Process

Although Altenkirch is credited as the first to inquire about the efficiency of the thermoelectric process in 1909 [24], Ioffe is credited as being the first to begin experimenting in the 1950's with the characterization of thermoelectric materials and devices to produce electricity using the thermoelectric figure of merit as it is known today [25, 26]. Before discussing a high temperature thermoelectric generator (TEG) as a device, the thermoelectric properties of the bulk materials is examined in the context of a constant property model (CPM). As seen in section 2.5 heat transport implies electronic transport and vice versa. This transport coupling makes thermoelectricity a challenging and interesting field.

If a monopolar, isotropic material (in this case an n-type semiconductor) with resistance R_{int} and thermal conductance K is subject to a small temperature difference $\Delta T = T_h - T_c$

and connected to a load resistance R_L, an electric current I will flow and from a one dimensional heat equation the different heating and cooling effects result.

In this case the efficiency of the thermal to electric conversion η is simply the ratio of the electrical power delivered at the load R_L and the heat extracted from the heat source on the hot side contact:

$$\eta = \frac{P_{\text{out}}}{Q_{\text{in}}} = \frac{I^2 R_L}{Q_{\text{peltier}} + Q_{\text{conduction}} - Q_{\text{joule}}} \tag{3.1}$$

Each term in the denominator of equation (3.1) is schematically shown in figure 3.1 where it is assumed that all heat transfer occurs at the electrodes. Considering the heat extracted at the hot side the efficiency can be written as:

$$\eta = \frac{R_L I^2}{\alpha T_h I + K\Delta T - \frac{1}{2} R_{\text{int}} I^2} \tag{3.2}$$

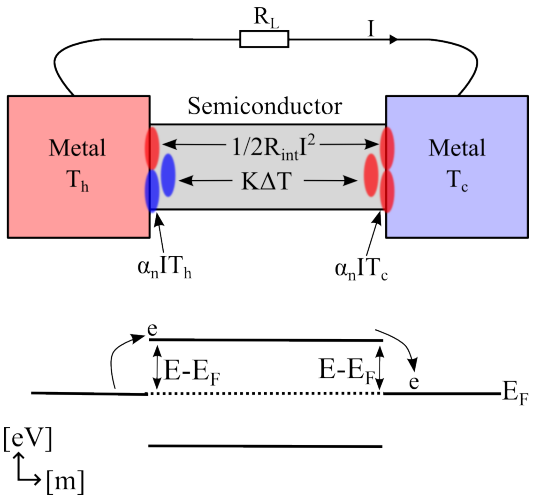

Figure 3.1: Heat fluxes in an n-type semiconductor. Heating is indicated in red and cooling in blue.

Equation (3.2) describes an ideal case for near equilibrium conditions and does not take into account convection and radiation transport. This equation is important because the

same approach will be taken in order to describe the PN-TEG. After differentiation the maximum possible efficiency at a given ΔT becomes [9]:

$$\eta_{\max} = \frac{\Delta T}{T_h} \frac{\sqrt{1+zT}-1}{\sqrt{1+zT}+\frac{T_c}{T_h}} \tag{3.3}$$

The first term is the Carnot efficiency, and zT is the widely used thermoelectric material figure of merit defined as:

$$zT = \frac{\alpha^2 \sigma}{\kappa_J} T \tag{3.4}$$

The figure of merit serves as very important parameter because it is a material property that allows different materials to be compared with respect to their potential to be used in thermoelectric devices.

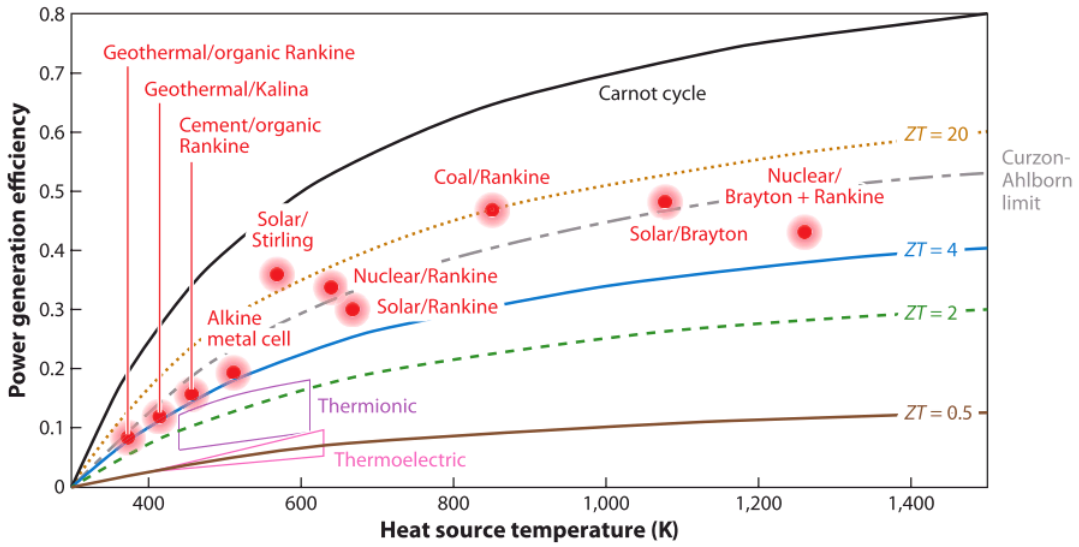

Figure 3.2: Efficiency of the thermoelectric process with $T_c = 300K$. From ref. [2].

Figure 3.2 puts the efficiency of the thermoelectric process into perspective with other heat engines. It is then obvious that to achieve a good thermoelectric efficiency, a large T_h and a large zT are required. But realizing a material with a high zT is not easy due to the

strong coupling and sometimes inverse relationships of the transport parameters α, σ, κ. This is evident in the empirical but not precise Wiedemann-Franz law:

$$\kappa_e = \sigma L_H T \tag{3.5}$$

Where L_H is the Lorentz number. That means increasing σ increases κ. Moreover, there is an inverse relationship between the Seebeck coefficient and the electrical conductivity. This can be seen in equation (2.15). Hence, there is typically an optimal point with respect to the doping concentration of some semiconductors where the three transport coefficients yield the highest zT.

In the last years there has been an evolutionary approach to increasing zT and with quite success zT has gone from a peak of approximately 0.5 in the 1950s to a range between 1-2 (with some cases above 2) at the beginning of 2010 largely based on alloying and nanostructuring [27, 28, 2, 29]. It is pointed in [30] and shown in Figure 3.3 that most commercial materials today have a figure of merit of that peaks approximately at a value of 1, and most of these materials are measured in temperatures below 600°C.

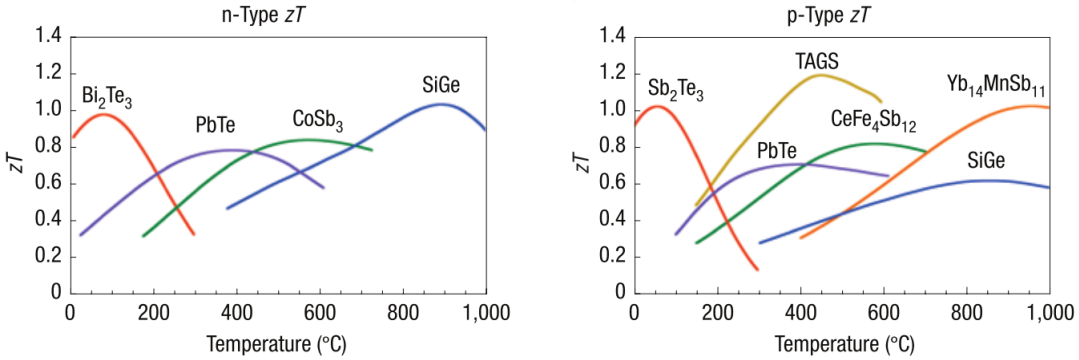

Figure 3.3: Summary of zT for different comercially available materials. From ref. [30].

Therefore the efficiency on thermoelectrics limited by an upper limit on the operating temperature and the figure of merit. It seems then safe to say that a realistic value of the

material figure of merit today is in the range of $0.5-1$ and this sets the maximum theoretical efficiency of a thermoelectric generator in the range of $2-8\%$ as seen in Figure 3.2. There are however efforts develop concentrated solar thermoelectric generators that reach a 15% efficiency [31].

3.2 From a Thermoelectric Material to a Conventional Thermoelectric Generator

There are far more aspects that can be mentioned in this work that need to be considered to make the transition from a thermoelectric material to a thermoelectric device. For example geometrical optimization of the thermoelectric legs [32, 33], of the heat exchanger [34, 35], and the electrical contacts [36], as well as the thermal and electrical load matching conditions [37, 38]. Although thermoelectric modules are commercially available today, they are mainly used as solid state coolers.

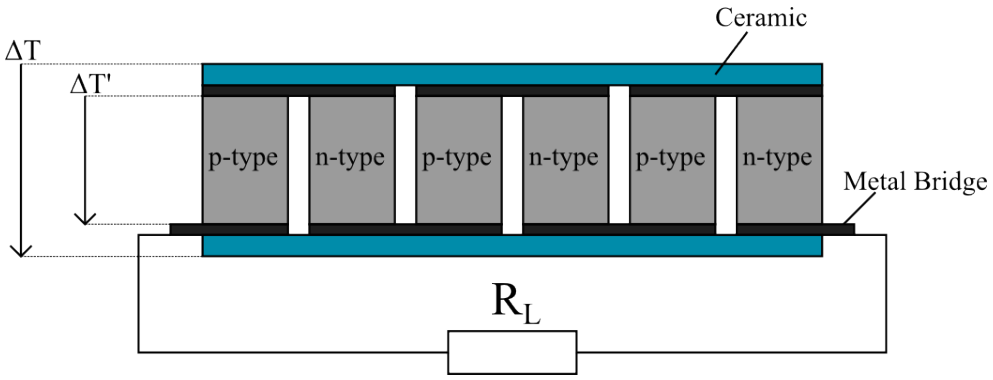

Figure 3.4: Architecture of a conventional TEG noting that $\Delta T > \Delta T'$.

A conventional thermoelectric generator (TEG), is traditionally described as alternating n-type and p-type semiconductor elements that are electrically connected in series and thermally connected in parallel as shown in Figure 3.4. A device figure of merit can be written by taking the effective electrical and thermal conductances as well as an effective

device Seebeck coefficient:

$$ZT = \frac{G_{\mathrm{TEG}}\alpha_{\mathrm{TEG}}^2}{K_{\mathrm{TEG}}}T \tag{3.6}$$

In this definition of the device figure of merit G_{TEG} is the device electrical conductance and includes the parasitic resistances coming from the electrical contacts and the metal bridges, K_{TEG} is the device thermal conductance including parasitic effects, and α_{TEG} can be approximated as the sum of the Seebeck coefficients of both materials. With these considerations the maximum efficiency of a TEG is written in basically the same form as for a bulk material:

$$\eta_{\mathrm{max,TEG}} = \frac{\Delta T'}{T_h}\frac{\sqrt{1+ZT}-1}{\sqrt{1+ZT}+\frac{T_c}{T_h}} \tag{3.7}$$

where care is taken to note that $\Delta T'$ is the temperature drop across the semiconductor legs, as shown in Figure 3.4. A calculation of ZT as it appears in equation (3.6) would require the measurement of convoluted parameters such as G_{TEG}, α_{TEG}, K_{TEG}, all of which are very difficult to measure individually in a TEG. For these reasons the device ZT is usually obtained by measuring the ratio of $P_{\mathrm{out}}/Q_{\mathrm{in}}$ or by the Harman technique as described in section 6.3.1.

As mentioned in this section there are many technological and theoretical aspects to consider when bridging the gap between a material and a device. One aspect that is important in the operation of a PN-TEG is the issue of thermal matching. As shown in Figure 3.4 a temperature drop occurs at the substrate and this is of course not desired, and a large mismatch of the thermal conductances of the thermoelectric material and the substrate considerably hinders the power output as shown in the next section.

3.3 Thermal Matching: The TEG in Operating Conditions

It has been pointed out that geometrical, cost optimizations and operating conditions need to be considered in order to continue to bring the technology forward [39, 40, 41]. In this section the impact of the ceramic substrates is considered. Analogous to electrical current, heat current can be modeled using thermal resistances as resistors and temperature differences as potential differences.

In the case of a TEG, the thermal resistances R_{hot} and R_{cold} arise from the substrates (see Figure 3.4) and the simplified equivalent thermal and electrical circuits are shown in Figure 3.5. That means that the total contact thermal conductance becomes $K_{\text{contact}}^{-1} =$

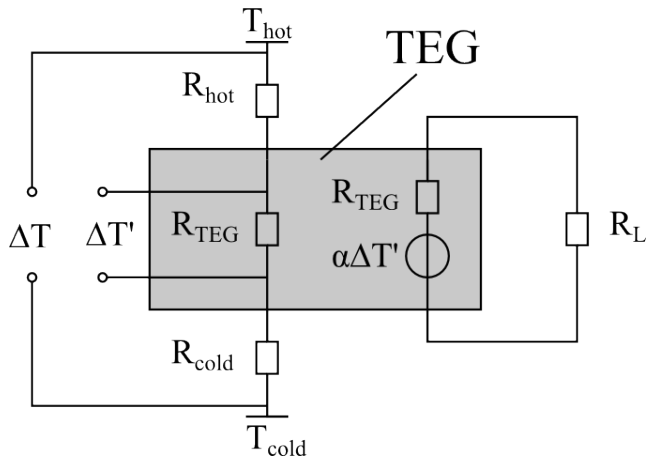

Figure 3.5: Thermal (left) and electrical (right) circuits for a TEG in operating conditions.

$K_{\text{hot}}^{-1} + K_{\text{cold}}^{-1}$, and the temperature drop across the semiconductor legs is written by the voltage divider rule

$$\Delta T' = \frac{K_{\text{contact}}}{K_{\text{TEG}} + K_{\text{contact}}} \Delta T \tag{3.8}$$

and provided that the electrical load resistance is matched to the internal electrical resistance, the maximum power output can be written as a function of the thermal conductances [39]:

$$P_{\text{max}} = \frac{(K_{\text{contact}} \Delta T)^2}{4(K_{\text{TEG}} + K_{\text{contact}})T} \frac{ZT}{1 + ZT + K_{\text{contact}}/K_{\text{TEG}}} \tag{3.9}$$

Equation (3.9) allows the evaluation of the power output as a function of the thermal conductances of the TEG including the thermal losses at the substrates at a given operation with fixed ΔT and ZT. Thermal matching can play a role as important as the actual value of ZT. Equation (3.9) is plotted in figure 3.6 and shows that a TEG with optimized thermal matching and low figure of merit $ZT = 0.5$ can deliver more power output than a TEG with $ZT = 1$ and non-optimized thermal matching.

The thermal matching ratio that separates the two points in Figure 3.6 is a factor of 8 (it is assumed that $R_{\text{hot}} = R_{\text{cold}}$). Hence the substrates play a critical role for a device in operating conditions because there is a temperature drop across each of the substrates. Hence the optimization of the thermal conductances is one of the device level optimizations that needs to be carefully considered in thermoelectric devices [42, 43]. It will be shown that in the new concept demonstrated in this work, the hot side substrate is not required, thus providing a tremendous advantage from thermal matching point of view, among other aspects that will be later discussed.

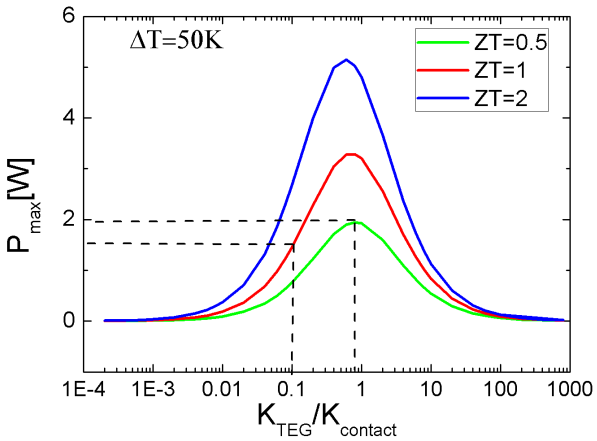

Figure 3.6: Maximum power as a function of the ratio of the thermal conductances. An optimized device with a lower figure of merit can outperform a device with a higher figure of merit if the thermal contacts of the latter are not optimized.

3.4 High Temperature Thermoelectrics

The first term in equation (3.7) is the Carnot efficiency limit and it tells us that ΔT is as important as ZT. Therefore high temperatures are a necessary condition for a high efficient thermal to electrical conversion. In light of this a strategy that can be pursued is to take a known material such as silicon that has been studied for many years, is abundant, non toxic, and compatible with actual semiconductor technologies, and operate it in a large ΔT. However this strategy does not apply only to silicon, recently Half-Heusler materials have been shown excellent thermoelectric properties at temperatures above 600°C for both n and p-type doping [44, 45].

A two dimensional plot of equation (3.7) in Figure 3.7 shows that a TEG with a low $ZT = 0.26$ would yield the efficiency as a commercially available Bi_2Te_3 TEG with $ZT = 0.8$ given that ΔT is large enough. A high efficiency number is necessary for the scientific race, but ultimately what determines the scope of the market of an energy technology is the cost of $W/\$$ and combining waste energy which has no production cost with a low cost material such as silicon could provide the necessary ingredients to make thermoelectricity a more attractive technology.

3.4.1 Silicon as a High Temperature Material

A material that has the potential to operate at high temperatures is silicon. In addition to being non-toxic and abundant, silicon is stable at high temperatures, and it is the most widely used semiconductor in the industry, which means that processing technologies that are already established and can be borrowed to process silicon, rendering the processing cost lower.

Silicon fulfills the requirement for high temperature stability. There are however challenges that need to be addressed before it can be incorporated in a high temperature device.

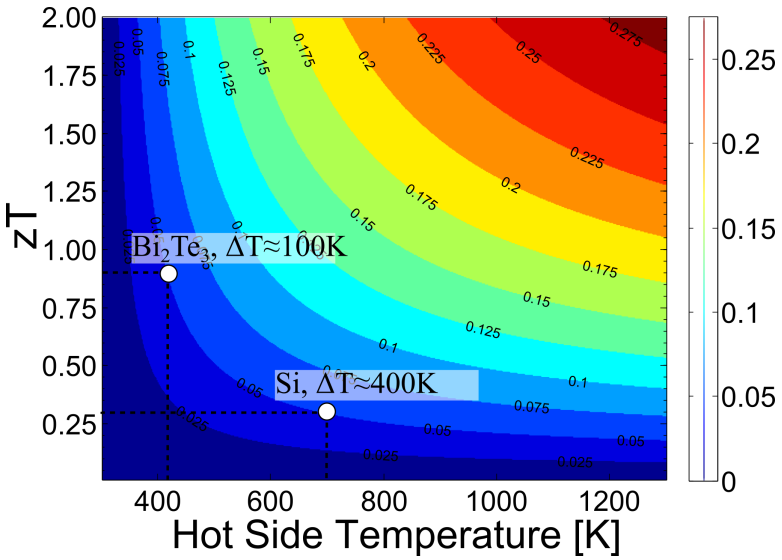

Figure 3.7: Efficiency of the thermoelectric process with $T_c = 300K$.

Firstly, intrinsic silicon is not a natural high performance thermoelectric material with a peak $zT = 0.2$ at 800 K. However nanostructuring has achieved considerable reductions in the thermal conductivity resulting in increased zT values.

The highest zT values reported on silicon have been accomplished by nanowires. There are reports of silicon nanowires with values as high as $zT = 1$ at low temperatures (200 K) [46] and reports of silicon nanowires with peak $zT = 0.6$ at 300 K [47]. Silicon nanowire structures are further away from integration into a device than bulk materials for two important reasons: 1) Lack of corroboration or inter-laboratory reproducibility of the results due to the highly specific preparation and measurement techniques and 2) technological difficulties to integrate a nanowire TEG. Despite these difficulties silicon TEGs based on nanowires have been reported [48].

At the time of writing bulk materials seem to have the highest prospect to be integrated into a device, because they overcome to a higher degree the two challenges that nanowires still have to overcome, and offers other advantages such as scalability [49]. Nanostructuring (by nanostructuring we refer to nano-domains with a crystalline structure bounded by grain

boundaries) and/or alloying have allowed to increase the peak of both n-type and p-type bulk silicon to $zT \approx 0.7$ [50, 51, 52], and even values as high as $zT = 1.2$ [53].

For these reasons, nanostructured silicon is the material used in this work. But if high temperature operation is desired the metallic contacts may be subject to undesired diffusion processes or alloying of the metal with thermoelectric material. Kessler et al. developed an anti-diffusion nickel layer to produce high temperature electrical contacts that were stable up to 600 °C [36, 54].

Higher operation temperatures would increase the Carnot efficiency and also would bring silicon into a temperature domain where its zT value peaks. A question that arises from this consideration is: If high ΔTs are desired, how adequate is the constant property model in the description of the thermodynamics? since the derivations of the efficiency were done in a near equilibrium conditions.

Reduction of Thermal Conductivity Through Nanostructures

Much of the just mentioned progress in silicon as a thermoelectric material is a consequence of a significant reduction in the thermal conductivity without compromising the electrical conductivity. From the figure of merit it is clear that a good thermoelectric material should have a high electrical conductivity and a low thermal conductivity. This is intuitive; we would like to extract as many charge carriers as possible while rejecting as many phonons as possible. This concept is sometimes referred as the "phonon-glass, electron-crystal" idea [6] because glass has a very low thermal conductivity, while crystalline semiconductors have the highest carrier mobility.

The strategies used to reduce the thermal conductivity can be understood in light of the electrical current equation (2.7) and the heat current equation (3.10) where the subtle difference between them is that in equation (3.10) each phonon carries an energy $\hbar\omega$ and follow a Bose-Einstein energetic distribution $n = 1/(\exp(\frac{\hbar\omega}{\kappa_B T}) - 1)$. With this in mind it becomes clear that a strategy to reduce the lattice thermal conductivity is to reduce

the phononic mean free path λ_{ph}, or in other words to increase the scattering centers for phonons.

$$Q_{\mathrm{open}} = \frac{1}{h}\int (\hbar\omega)\frac{\lambda_{\mathrm{ph}}(\hbar\omega)}{\lambda_{\mathrm{ph}}(\hbar\omega)+L}M_{\mathrm{ph}}(\hbar\omega)(n_1-n_2)d(\hbar\omega) \tag{3.10}$$

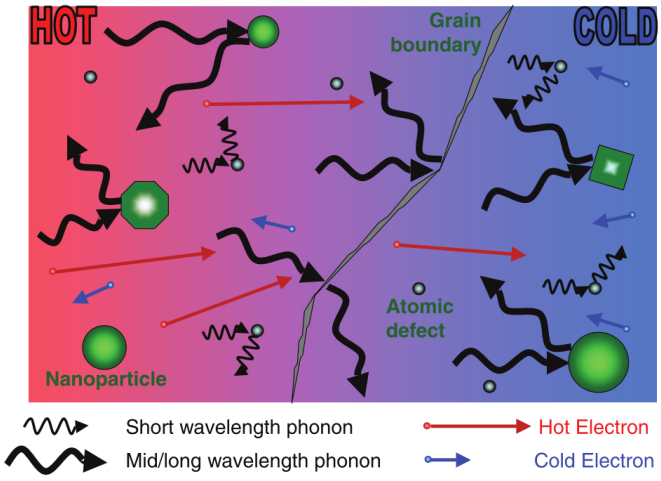

Figure 3.8: Schematic of the different phonon scattering mechanisms within a thermoelectric material. Point defects scatter short wavelength phonons while embedded nanoparticles and grain boundaries scatter longer wave phonons. From Ref. [27].

There are many strategies to reduce the phononic mean free path. For example alloying effectively introduces atomic defects that scatter phonons selectively over electrons, and in fact commercial thermoelectric devices are built on alloys of Bi_2Te_3 and Sb_2Te_3 [55]. Alloys of SiGe have also shown a reduction of the thermal conductivity for both doping types [53, 56, 52]. Other strategies are the inclusion of nanoparticles into the lattice or the introduction of grain boundaries in nanocrystalline materials [27]. Each scattering mechanism (atomic defect, nanoparticle, grain boundary) is more likely to scatter phonons with a given wavelength as shown in the schematic in Figure 3.8.

In this work the strategy is to introduce grain boundaries by compacting doped nanoparticles into bulk nanocrystalline silicon to reduce the lattice thermal conductivity. Reviews on nanostructured thermoelectrics can be found in references [27, 28, 57]. Bulk nanos-

tructured silicon in particular has been shown to have superior thermoelectric properties compared to crystalline silicon due to a reduction of the thermal conductivity by phonon scattering at grain boundaries [50, 29, 53]. Hence, the PN junctions used as thermoelectric generators are made from nanostructured bulk silicon.

3.4.2 Large Temperature Gradients and Temperature Dependent Model

A thermoelectric generator would be ideally operated in a large temperature difference, however the constant property model assumes small temperature differences because it allows the calculations for efficiency to be solved analytically. If large temperature gradients are applied, it is necessary to consider the temperature dependency of the transport coefficients: $\alpha(T)$, $\sigma(T)$, $\kappa(T)$.

Today it does not appear to be a clear consensus on how to tackle this issue. In one approach Borrego [58] showed using the same approach used in section 3.1 that it is possible to arrive to a material figure of merit z_{eff} which considers the temperature dependency of the transport coefficients

$$z_{\text{eff}} = \frac{\left(\int_{T_c}^{T_h} \alpha(T)dT\right)^2}{\Delta T \int_{T_c}^{T_h} \rho(T)\kappa(T)dT} \tag{3.11}$$

Note that in equation (3.11) the multiplication on both sides by the average temperature has been left out because the average temperature in a system where large ΔTs are allowed becomes overly defined, and it depends itself on the material parameters. Borrego's idea points in the right direction, however he did not consider the Thomson effect, which can be left out in the constant property model, but not in the temperature dependent property model as shown in section 2.7.

In a series of papers Min et al. developed an alternative method to measure the figure

merit in more realistic operation conditions (i.e. large ΔTs) in which he took into account the Thomson effect [59, 60, 61]. He arrived to the following expression for z_{eff}:

$$z_{\text{eff}} = \frac{\sigma_{\text{eff}} \left(\alpha_{\text{h}} - \beta \Delta T / 2T_{\text{h}}\right)^2}{\kappa_{\text{eff}}} \tag{3.12}$$

in this case α_{h} is the value of the Seebeck coefficient at the hot side boundary, β the Thomson coefficient, and σ_{eff} and κ_{eff} are the effective electrical and thermal conductivities at a given ΔT. There are however some problems with equation (3.12) because it was derived assuming that the open circuit thermal conductivity and the closed circuit thermal conductivity are equal $\kappa_{\text{j}} = \kappa_{\text{E}}$, and it fails to explain experimental data [59, 60].

The best approach to attack the issue of temperature dependent coefficients seems to be the Compatibility approach introduced by Snyder and Ursell [62, 63]. In this approach the starting point for the efficiency consideration takes a general form that does not require assumptions of near equilibrium conditions meaning that also Thomson transport is accounted for [62]:

$$\eta = \frac{P_{\text{out}}}{Q_{\text{in}}} = \frac{J \int_{T_{\text{c}}}^{T_{\text{h}}} \alpha dT - J^2 \int_0^l \rho dx}{J T_{\text{h}} \alpha_{\text{h}} + \kappa_{\text{h}} \nabla T_h} \tag{3.13}$$

Here the subscript h stands for the hot side heat boundary, and l for the length of the material. The compatibility approach has been used to optimize the local efficiency of the thermoelectric material by choosing the best local properties [63, 64]. However it would be interesting to see an optimization with respect of ΔT for a temperature dependent material.

There does not seem to be an established agreement on how to attack the problem of temperature dependent transport coefficients [8], and in this work large temperature gradients are used which means that in the presentation of the results care is taken to

consider that the results cannot be immediately compared to measurements done in near equilibrium conditions.

3.5 Summary: Conventional TEG

In this chapter the derivation of the thermoelectric process efficiency in the framework of a near equilibrium constant property model is shown to be important to be able to put the thermoelectric energy conversion process in context with other technologies. The thermoelectric figure of merit is a necessary but not sufficient indicator for the potential that a material has to perform as a thermoelectric material.

Aspects involving the transition from a thermoelectric material to a thermoelectric device are taken into account, and here it is pointed out that it can be misleading to concentrate all efforts and to evaluate the potential of a material merely on its zT value. There are other aspects such as the Carnot efficiency, and cost that need to be included to make a complete evaluation of a given thermoelectric material.

It is explained that silicon is chosen as a thermoelectric material because of its abundance, non-toxiticy, familiar processing technologies, and because recent advances in nanotechnology have led to a reduction in the thermal conductivity through nano-crystalls. Finally it is pointed out that if a material or device is operated in large temperature gradients, care needs to be taken when using the derivation of efficiency and zT as they might no longer seem appropriate.

4 New Device Architecture: PN-TEG

> Efficiency is doing things right.
> Effectiveness is doing the right things.
>
> Peter Drucker

4.1 Proposed Concept: PN-TEG

The heart of this work is the study of what we call a PN-TEG. The idea of a PN-TEG was formally proposed by Span et al. in a series of papers [65, 66, 67, 68] mainly with the idea to produce thin film technologies, but has also been independently investigated experimentally in bulk TEGs by [69, 70]. A PN-TEG is different form a conventional device because the electrical and mechanical connection between the n-type and p-type semiconductor legs is done by means of a PN junction as shown in Figure 4.1b.

The implications of the PN-TEG architecture are vast and condensed below. In the following chapters of this work each one of the following will be discussed.

- Advantages:
    1. Electrical contacts and ceramic substrate are not required on the hotside.
    2. Heat source can come in direct contact with the thermoelectric material, and higher hot side temperatures can be reached.

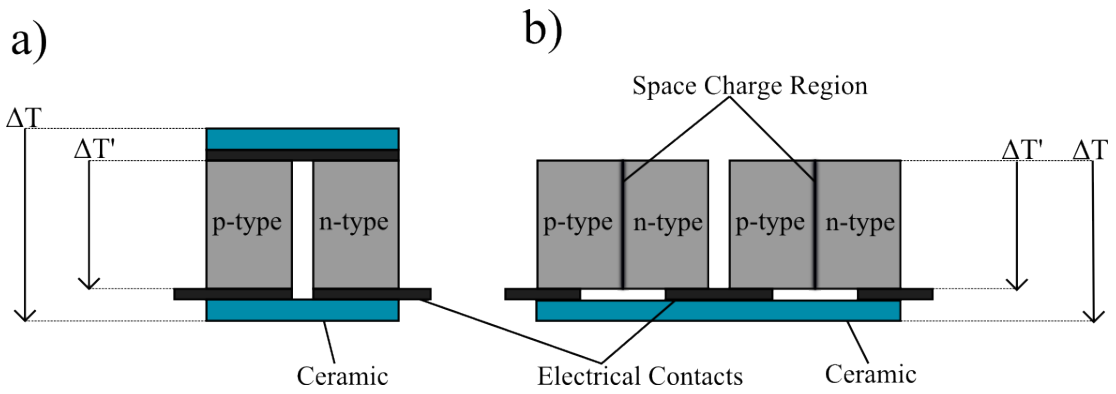

Figure 4.1: a) Conventional TEG architecture, b) PN-TEG architecture.

3. The fabrication process of a PN-TEGs is greatly simplified compared to that of a conventional TEG.

- Disadvantages:

1. At low temperatures, the space charge region acts like an electrical insulator limiting current flow.

2. As it will be shown, a PN-TEG develops internal electrical current vortices that reduce the power output.

- Theoretical Implications

1. The traditional figure of merit $zT = (\sigma\alpha^2)/\kappa_J$ cannot be immediately applied to evaluate a PN-TEG.

2. Heat and electrical current do not always flow in the same direction, rendering the description of a PN-TEG a two dimensional problem.

3. A description of excess charge carriers due to thermal generation/recombination becomes non-trivial.

4. Peltier effects at the PN junction are not fully understood.

Having the electrical contacts exclusively on the cold side has the clear technological advantage that a metallization on the hot side and the substrate is not required, that means that the temperature losses across the hot side substrate are eliminated as shown in Figure 4.1a. As an example a plot of equation (3.9) in Figure 4.2 compares the maximum power output for a conventional device with cold and hot side substrates to a device with only one substrate. As seen, the power output for a conventional TEG would double if the thermal resistance is cut by half. Hence a tremendous advantage of a PN-TEG is the abscense of the hot side substrate and thermal losses. Bear in mind that Figure 4.2 describes a conventional TEG, not a PN-TEG.

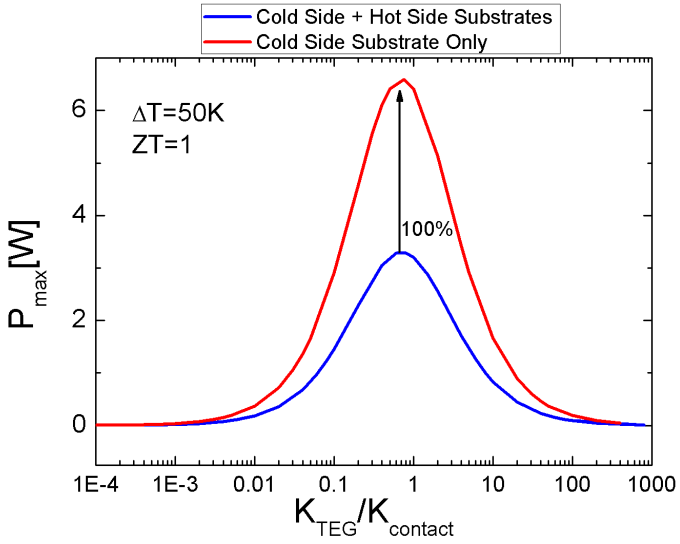

Figure 4.2: Maximum power output plotted using equation (3.9). The thermal conductance K_{contact} was doubled from the blue line to the red line to mimic the absense of one of the substrates

In addition to the technological advantage of using one substrate, Wagner et al. suggested that the thermally generated charge carriers within the PN junction will contribute to the thermoelectric driving force suggesting that a PN-TEG should outperform a conventional device [65], but this claim remains an open question in this work. Despite the open question on the efficiency comparison, it is shown in this work that in addition to

the tremendous technological advantages, nanostructured silicon PN junctions can work as thermoelectric generators, in a scalable manner, and can operate in temperature conditions that conventional commercially available generators are not able to operate. High temperature operation enables a higher Carnot efficiency and makes up for the relatively low figure of merit of silicon.

Although credit is given to Span et al. for the PN-TEG concept in their publications in late 2000 [65, 66, 67, 68]. Yang et al. recognized in 2001 that if a layer of p-type and n-type Bi_2Te_3 are pressed together, the intrinsic region in the middle can be increasingly removed to approximate a conventional device leading to some of the technological advantages already mentioned [71, 69]. A PN structure was investigated as a thermionic/thermoelectric device in ref. [72] and theoretical work in [73, 74] explored a PN junction with a temperature gradient parallel to the junction interface, as it is done in this work, but with the difference that they were concerned exclusively in the internal current loops and did not consider the possibility of using the PN junction as a TEG.

4.2 PN-TEG Proposed Theory

One of the biggest challenges of developing a theoretical framework for the description of a PN-TEG the two-dimensional nature of the transport driving forces and hence a purely analytical description of the device is very difficult. So far a description of these type of systems seems only possible with numerical calculations as it has been previously done by others to describe such PN-TEG devices [68, 65, 66, 67, 73]. To aid in the theoretical description of the PN-TEG, Sebastian Angst is acknowledged with the development of a discrete Onsager network model which is used to provide much of the analytical description of the knowledge [75]. The proposed theory is divided into three subsections: Transport, Efficiency and Optimization.

4.2.1 Simulation Details: Discrete Onsager Network

The model here described is acknowledged to Sebastian Angst [75]. This model is used to test hypotheses and verify experimental results for conventional generators and PN-TEGs. The model is a discretization of Onsager's theory. The starting point of the model is the continuous form of equation (2.21) with the addition of an expression for Joule heating. The Electric current density, the heat current density and the volumetric heat production are written as [9]

$$\begin{aligned} \mathbf{J} &= -\sigma\left(\frac{\nabla\varphi}{q} + \alpha\nabla T\right) \\ \mathbf{J}_Q &= \alpha T\mathbf{J} - \kappa_\mathrm{J}\nabla T \\ \nabla\cdot\mathbf{J}_Q &= -\frac{\nabla\varphi}{q}\mathbf{J} \end{aligned} \tag{4.1}$$

In the discretization every node is assigned a temperature T, an electrochemical potential φ, a specific heat capacitance Θ, and every bond between two neighbors i and j is characterized by an electrical conductance G_{ij}, thermal conductance K_{ij}, average temperature T_{ij} and average Seebeck coefficient α_{ij} as depicted in Figure 4.3.

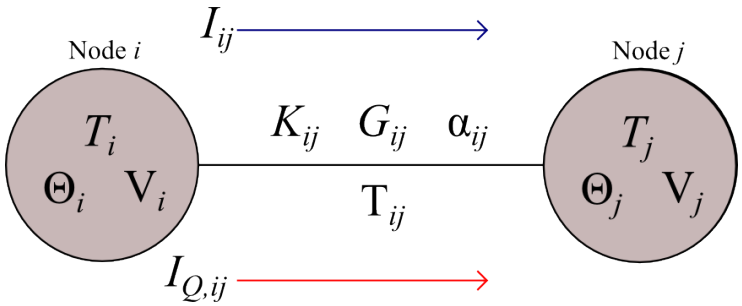

Figure 4.3: A two node bond and its variables.

With this in consideration the electrical current between nodes is calculated as

$$I_{ij} = G_{ij}\left(\frac{\varphi_i - \varphi_j}{q} + \alpha_{ij}(T_i - T_j)\right) \tag{4.2}$$

in a similar fashion the heat current is calculated as

$$I_{q,ij} = K_{ij}\,(T_i - T_j) + \Pi_{ij} I_{ij} \tag{4.3}$$

with $\Pi_{ij} = \frac{1}{2}(\alpha_i T_i - \alpha_j T_j)$. Note that equations (4.2) and (4.3) are just discrete forms of the first two equations in (4.1). This model provides at tremendous tool in analyzing the internal distribution of the electrical current in a PN-TEG because temperature dependent parameters $\alpha(T)$, $\kappa(T)$, $\sigma(T)$ can be implemented and it also provides first order approximations for the the efficiency of a PN-TEG since the heat flow can be calculated in a simulation.

4.2.2 Electrical Transport

The description of a PN-TEG begins by considering a large area PN junction and breaking it into an array of differential elements because a larger temperature difference is desired, and it is well known from diode theory that the transport properties of a diode depend exponentially on temperature. The base model is given in thermodynamic equilibrium conditions ($\Delta V = \Delta T = 0$); the PN junction is broken into differential diodes each with a linear shunt resistance R_{sh}, a non-linear shunt resistance R_{SCL}, a series resistance R_{s} and these elements are interconnected by a bulk resistance R_{bulk}. In the junction of the two materials the space charge region is depicted as a shaded area as shown in Figure 4.4a.

If the PN junction is resting in thermal equilibrium, but biased with a voltage that is small enough to ignore Joule and Peltier effects and big enough to turn on the diode closest to the electrodes, the built-in potential and therefore the space charge region near the electrodes will shrink and the electrical current density will be higher near the electrodes as sketched in Figure 4.4b.

This treatment provides a limited general idea of the electrodynamics within the PN-

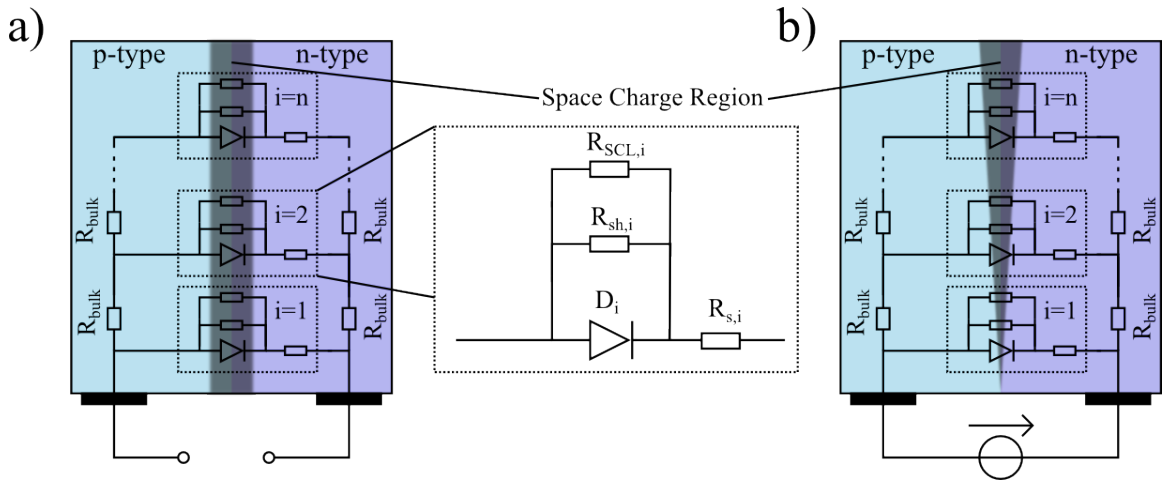

Figure 4.4: Electrical schematic of a PN junction in a) thermodynamic equilibrium and b) under a forward bias voltage.

TEG, but such a treatment will prove crucial to understand thermoelectric effects. From this idea it is clear that the current density should be described in two dimensions, but for now we consider the macroscopic current I. Hence, the current across each diode element $I_{\mathrm{D},i}$ can be approximated by adding the recombination and the diffusion currents given that $V_i >> \frac{k_B T}{q}$ [76]:

$$\begin{aligned} I_{\mathrm{D},i} &\approx \underbrace{I_{\mathrm{diff}} \exp\left(\frac{qV_i}{k_B T}\right)}_{\text{Diffusion Current}} + \underbrace{I_{\mathrm{R}} \exp\left(\frac{qV_i}{2k_B T}\right)}_{\text{Recombination Current}} \\ I_{D,i} &= I_0 \exp\left(\frac{qV_i}{\eta_D k_B T}\right) \end{aligned} \tag{4.4}$$

where I_{diff}, I_{R} and I_0 are material specific constants, V_i the voltage drop across each diode and η_{D} is known as the ideality factor and it tells whether the current is dominated by diffusion of minority charge carriers or recombination within the space charge region.

The current across the non-linear resistor $R_{\mathrm{SCL},i}$ is phenomenologically described by a space charge limited current [77], and the reasons for this are given in the Results Chapter.

$$|I_{\mathrm{SCL},i}| = |V|^{\gamma+1}, \gamma > 0 \tag{4.5}$$

Finally the current across the linear resistances $R_{\mathrm{sh},i}$, $R_{\mathrm{s},i}$ are described by Ohm's law.

The most important take away from the discussion derived from Figure 4.4 is that the PN-TEG can be though of many diode elements connected in parallel, and that when a voltage bias is applied, electrical current will flow inhomogeneosly, and close to the electrodes. The inhomogeneous current density means that analytical expressions to describe the electrical transport cannot easily be derived if at all possible. For example, how would an expression for the internal resistance look like? This is a critical point, and calls the necessity of numerical simulations, because this in turn means that the expressions needed to derive the efficiency of such a device are not available. This is discussed in detail in the Efficiency Section 4.2.6.

4.2.3 Temperature Dependence of Electric Transport

The next consideration is the following question: what happens to the electrical transport as a temperature gradient is applied to the PN junction turning it into a PN-TEG? An equivalent circuit of the PN-TEG under a temperature gradient is shown in Figure 4.5. In this schematic it is possible to see that electrical current flows in the x-direction, and that must mean that heat flows in the x-direction as well but the description of heat carried by bipolar transport is not well understood.

Another consideration is the appearance of differential voltage sources in the equivalent circuit, these voltage sources represent the thermoelectric driving force due to the Seebeck effect. The last point is that at large temperature differences the spatial symmetry of the space charge region is turned around; the space charge region becomes thinner on the hot end, and this changes the spatial current density map (compare Figures 4.4b and 4.5).

The reason for the shrinking of the space charge region on the hot end is due to an increase of intrinsic charge carriers. An indirect assessment of the space charge region can be carried by observation of the built-in voltage. The temperature dependent built in

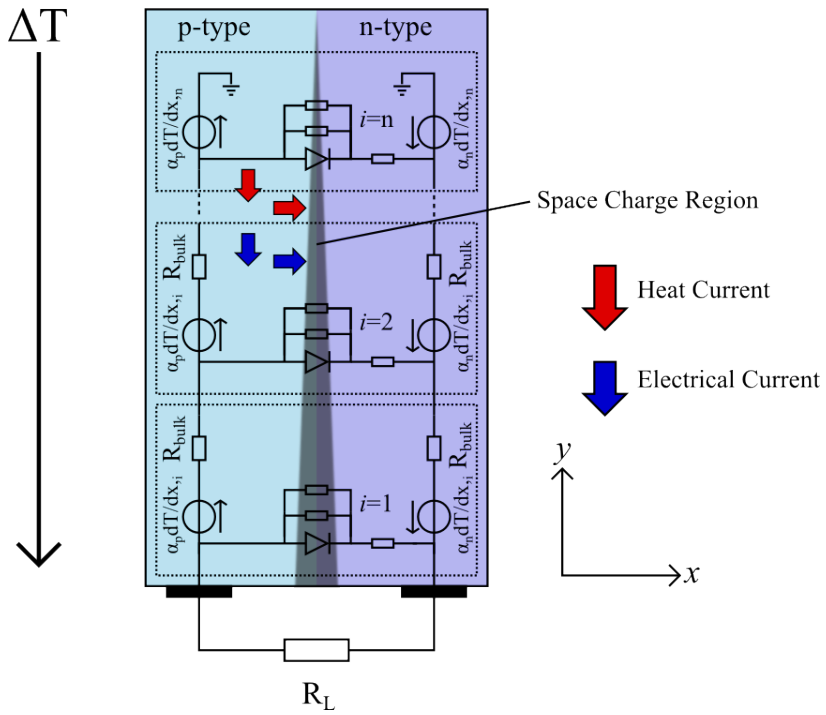

Figure 4.5: Electrical schematic of a PN-TEG under a temperature difference.

voltage $V_\mathrm{b}(T)$ of a non-degenerated diode is

$$V_\mathrm{b}(T) = \frac{k_B T}{q} \ln\left(\frac{N_\mathrm{A} N_\mathrm{D}}{n_\mathrm{i}^2(T)}\right) \tag{4.6}$$

where $N_\mathrm{A} = N_\mathrm{D} = 5{\times}10^{19}\,\mathrm{cm}^{-3}$ are the acceptor and donor concentrations and are assumed to be constant over temperature. In order to calculate the temperature dependency of $V_\mathrm{b}(T)$ it is necessary to consider the intrinsic charge carriers $n_\mathrm{i}(T)$ that get thermally excited over the bandgap

$$n_\mathrm{i}(T) = \sqrt{N_\mathrm{c}(T) N_\mathrm{v}(T)} \exp\left(-\frac{E_\mathrm{g}(T)}{2k_B T}\right) \tag{4.7}$$

here $N_\mathrm{C}(T)$ and $N_\mathrm{V}(T)$ are the effective density of states at the conduction band and valence band respectively. For equation (4.7) one should consider the temperature dependency of

the bandgap[1]

$$E_{\mathrm{g}}(T) = E_{\mathrm{g}}(0K) - \frac{\delta T^2}{T+\beta} \tag{4.8}$$

And finally, the temperature dependency of the effective density of states $N_{\mathrm{c}}(T)$ and $N_{\mathrm{v}}(T)$

$$N_{\mathrm{c}}(T) = 2\left(\frac{2\pi m_e^* k_B T}{h^2}\right)^{3/2} \tag{4.9}$$

$$N_v(T) = 2\left(\frac{2\pi m_h^* k_B T}{h^2}\right)^{3/2} \tag{4.10}$$

where $m_{e,h}^*$ is the effective mass of electrons and holes respectively.

To get a general understanding of the electrodynamics of a PN-TEG a system consisting of ideal diodes with infinite shunt resistances is considered. A simulation of a PN-TEG using the model introduced in section 4.2.1 is shown in Figure 4.6a. In this Figure the temperature is coded using a blue to red scale for cold to hot. The temperature on the hot side is 1000 K and on the cold side 300 K. The size of the arrows is correlated to the magnitude of the electrical current density $\mathbf{J}$. The built-in voltage $V_{\mathrm{b}}(T)$ for a highly doped ideal diode is calculated then using equations (4.6)-(4.10) and shown in Figure 4.6b and we note that for a highly doped system under large temperature differences, the difference in the built-in voltage between the cold side and the hot side can be of $0.45V$. This spatially defined built-in voltage acts like an electrical "gate" that opens on the hot end of the PN-TEG and closes on the cold end of the PN-TEG.

Figure 4.6a shows that the electrical current crosses the PN junction through the open "gate" on the hot end of the device, while the closed "gate" on the cold end prevents that an internal current loop develops within the PN-TEG. The main reason for the spatially defined built-in voltage $V_{\mathrm{b}}(T)$ is that the steep temperature gradient creates a steep gradient in the intrinsic charge carrier concentration $n_{\mathrm{i}}(T)$. As seen in Figure 4.6c the intrinsic

[1] $E_{\mathrm{g}}(0K) = 1.17\,\mathrm{eV}$ is the Bandgap of Silicon at $0K$ and the proportionality constants for Silicon $\delta = 4.9 \times 10^{-}4\,\mathrm{eV/K}$ and $\beta = 6.55 \times 10^2\,\mathrm{K}$ [78]

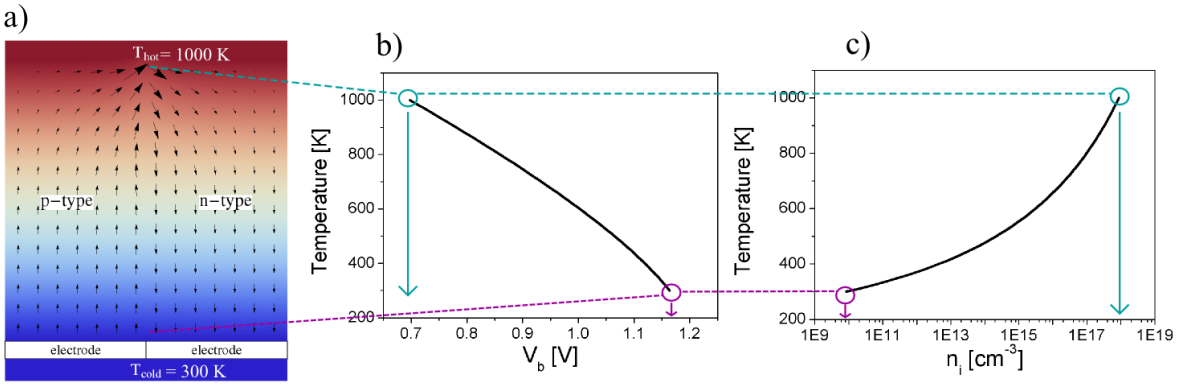

Figure 4.6: a) Electrical current density map for a PN-TEG with $N_A = N_D = 5{\times}10^{19}\,\mathrm{cm}^{-3}$. b) Built-in voltage $V_\mathrm{b}(T)$ shows a reduced potential barrier on the hot side of the PN-TEG. c) The intrinsic carrier concentration $n_\mathrm{i}(T)$ shows that the magnitude of n_i comes close to the doping concentrations $N_\mathrm{A}, N_\mathrm{D}$ on the hot end.

carrier concentration varies by 8 orders of magnitude from the cold to the hot end. In the hot end the intrinsic carrier concentration is nearly of the same magnitude as the dopant carrier concentration.

The charge carrier density n can be divided in three domains in temperature: The ionization domain, the extrinsic domain, and the intrinsic domain [76]. The ionization domain corresponds to the activation energy of the dopants ΔE and in ranges in temperature from $0K$ to T_min. The saturation domain is the temperature range $T_\mathrm{min} < T < T_\mathrm{max}$ where all dopants are active and the carrier concentration is equal to the nominal doping (N_D in this case) but the temperature is insufficient to generate carriers from the intrinsic silicon lattice. After a temperature T_max intrinsic charge carriers from the silicon lattice begin to get activated over the bandgap and this is called the intrinsic domain. This behavior is sketched in Figure 4.7.

It is desired to operate the PN-TEG near the intrinsic temperature on the hot side because note from equation (4.6) is that if $N_\mathrm{A} = N_\mathrm{D} = n_i$ the potential barrier goes to zero and we enter a flat band (zero potential barrier). The intrinsic temperature T_max can

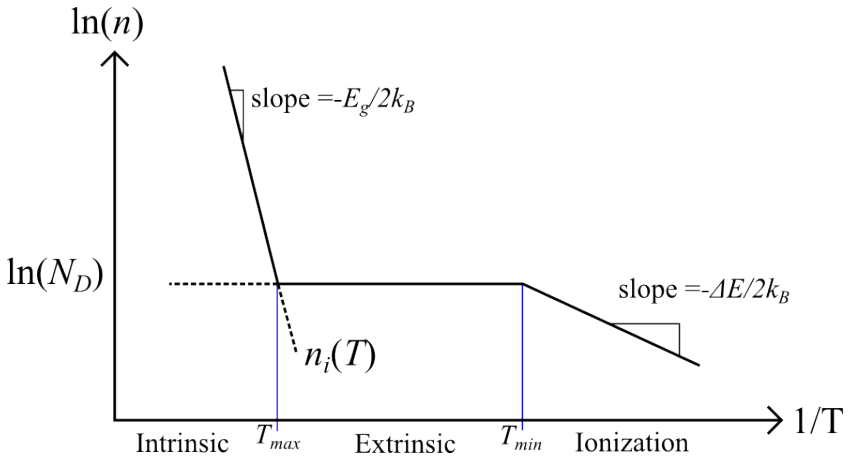

Figure 4.7: Plot of the carrier concentration for an n-type semiconductor. Adapted from [76].

be obtained by setting the doping concentration in equation (4.7) equal to the intrinsic concentration:

$$N_{D,A} = \sqrt{N_c(T_{\max})N_v(T_{\max})}\exp\left(-\frac{E_g(T_{\max})}{2k_B T_{\max}}\right) \tag{4.11}$$

But since most parameters depend on temperature is not convenient to solve equation (4.11) analytically. Using the values presented above $N_{\mathrm{A}} = N_{\mathrm{D}} = 5 \times 10^{19}\,\mathrm{cm}^{-3}$, we find that for crystalline silicon $T_{\max} > 1000\,^{\circ}\mathrm{C}$, and it is intuitive that $T_{\max}$ decreases with smaller bandgaps. Therefore smaller bandgaps are desired, and this can be done by the inclusion of intraband states and recombination defects.

4.2.4 Current Loops Within the PN-TEG

Some of the valid skepticism towards a PN-TEG is that the two semiconductor materials are electrically insulated by the space charge region [71], but as shown above the built-in potential of the PN junction can be drastically suppressed on the hot side creating a better electrical connection between the two semiconductors while maintaining a higher potential height on the cold side that insulates electric current flow. Moreover, it will be shown in section 7 that when intraband electronic states are present, the effective bandgap is

reduced further and higher internal conductances are found in systems that have many electronic defects as in ideal PN junctions.

Although not visible in Figure 4.6a because of the scaling, internal currents loops do develop, and they lead to efficiency losses. To exemplify this, Figure 4.8 shows what would happen to the electrical current distribution of the PN-TEG with zero potential barrier. And in fact this situation describes the experimental PN-TEGs better because they exhibit a low effective bandgap. Similar internal current loops in thermoelectric devices have been identified. In ref. [73] a diode structure in open circuit conditions is shown to exhibit internal current loops that are separated by the space charge region. In ref. [74] two thermoelectric legs electrically and thermally connected in parallel (much similar to a PN-TEG) are shown to develop internal current loops in open circuit conditions.

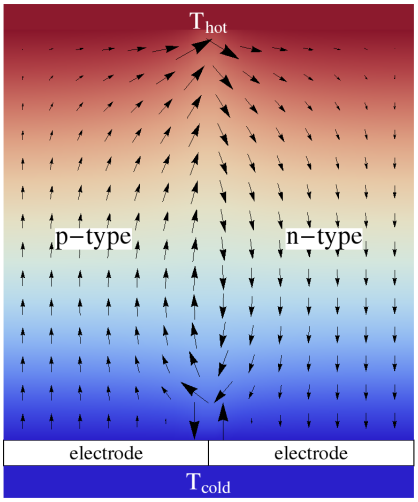

Figure 4.8: Electrical current density map at $\Delta T = 700\,\mathrm{K}$ shows that current loops will develop if no potential barrier is present. The size of the arrows is correlated to the electric current density $\mathbf{J}$.

With this discussion in mind it is expected that the PN-TEG performs optimally when high temperatures are applied on the hot side and when a large temperature gradient is conserved. In this way electrical transport is enhanced at the hot side and losses are minimized from internal current loops. Having a perfect diode system poses the difficulty

that the potential barrier is simply to high even at high temperatures and the current output is largely compromised. For this reason a system with a small potential barrier is desired, even though this means that current loops might be stronger. It will be shown that while our PN-TEGs are highly doped, and thus with a high nominal potential barrier, a high density of intraband states are introduced during the preparation, making the PN junctions as desired.

4.2.5 Thermal Generation and Internal Resistance

A very interesting aspect of a PN-TEG is that once the device is exposed to a temperature difference, its electrical properties change in the sense that the current density is redistributed. After closer examination one realizes that when the PN junction is operating as a TEG, the Seebeck effect creates a polarity that puts the diode near the hot end in reverse bias. That means that the current flow of the PN-TEG is limited by thermal generation of carriers, and is in theory voltage independent. From equation (4.4), the reverse bias current I_0 is written from diode theory as [76][2]

$$I_0(T) = A\left(\frac{qD_\mathrm{h}}{L_\mathrm{h}N_\mathrm{D}} + \frac{qD_\mathrm{e}}{L_\mathrm{e}N_\mathrm{A}}\right)n_\mathrm{i}^2(T) + A\frac{qWn_\mathrm{i}(T)}{\tau_\mathrm{g}} \tag{4.12}$$

Here $D_{\mathrm{e,h}}$ is the diffusion coefficient of electrons and holes, $L_{\mathrm{e,h}}$ the diffusion lengths of electrons and holes, A the cross sectional area of the PN junction, W the width of the depletion region and τ_g rate of thermal generation per unit volume. The first term in equation (4.12) refers to minority charge carriers that diffuse into the space charge region and are swept away by the electric field, and the second term refers to thermally excited charge carriers within the space charge region that are separated by the electric field as it was previously pointed out [68]. In the model we suggest in this work, we note that

[2]Page 491

the reverse bias current depends mainly on the hot side temperature of the PN-TEG by means of n_i. Under the scope of this discussion then, we propose an electrical model for the PN-TEG where the Seebeck voltages are small enough such that the diode appears as an open circuit and to account for the thermally generated carriers on the hot side a current source is added in parallel to the diode as shown in Figure 4.9a.

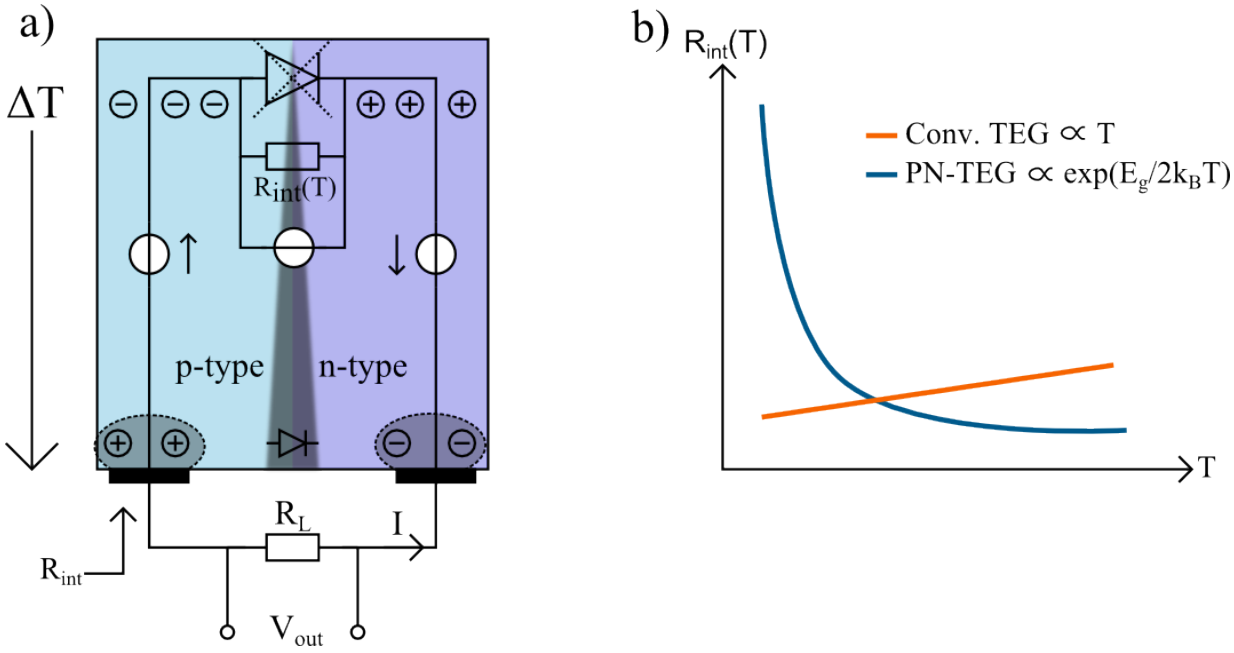

Figure 4.9: a) Electrical schematic showing the PN-TEG. The voltage sources are due to the Seebeck effect and the current source accounts for thermally generated charge carriers. b) Expected temperature response of the internal resistance.

Having the described electrical model renders the PN-TEG concept similar to the conventional TEGs, but with the fundamental difference that the internal resistance of a PN-TEG should decrease exponentially with temperature, while a conventional TEG exhibits a linear increase due to the metallic properties of the thermoelectric materials as it is sketched in Figure 4.9b.

Now we seek a more formal description of the internal resistance R_{int} of the PN-TEG. We make the assumption that the output current of a PN-TEG is dominated by the reverse bias current of the diode I_0. In equation (4.12) it is not clear which term is more dominant

and keeping in mind that $n_{\mathrm{i}} \propto \exp\left(\frac{-E_g}{2k_{\mathrm{B}}T}\right)$ and $n_{\mathrm{i}}^2 \propto \exp\left(\frac{-E_g}{k_{\mathrm{B}}T}\right)$ we write $I_0(T)$ as

$$I_0(T_{\mathrm{avg}}) \propto \exp\left(\frac{-E_{\mathrm{g}}}{\xi k_{\mathrm{B}} T_{\mathrm{h}}}\right) \tag{4.13}$$

where $1 \leq \xi \leq 2$ depending on which term on equation (4.12) is more dominating. This implies that the output current from the PN-TEG increases exponentially with the temperature as shown in equation (4.13). The internal resistance of the PN-TEG can be expressed as the ratio of the open circuit voltage V_{oc} and the short circuit current $I_{\mathrm{sc}} = I_0(T_{\mathrm{avg}})$ as long as the IV response is linear (it is shown in section 6.3.6 that the IV is linear)

$$R_{\mathrm{int}}(T_{\mathrm{avg}}) = \frac{V_{\mathrm{oc}}}{I_0(T_{\mathrm{avg}})} \tag{4.14}$$

In equation (4.14) V_{oc} can be approximated as the sum of the Seebeck coefficients multiplied by the temperature difference, and interestingly $I_0(T_{\mathrm{avg}})$ does not depend on the voltage but on the temperature, and since the absolute values are not as important as the proportionality, we write:

$$\frac{V_{\mathrm{oc}}}{I_0(T_{\mathrm{avg}})} \propto \frac{(\alpha_p + \alpha_n)\Delta T}{\exp\left(\frac{-E_{\mathrm{g}}}{\xi k_{\mathrm{B}} T_{\mathrm{h}}}\right)} \tag{4.15}$$

Which ultimately leads to the following and most important relation:

$$R_{\mathrm{int}}(T_{\mathrm{avg}}) \propto \exp\left(\frac{E_{\mathrm{g}}}{\xi k_{\mathrm{B}} T_{\mathrm{h}}}\right) \tag{4.16}$$

The relation in equation (4.16) is very important because it provides access to the effective electronic structure of the PN-TEG in the form of an effective bandgap E_{g}. Moreover, it also becomes evident that in order to achieve a low internal resistance, a low effective bandgap is desired. However, E_{g} should not be too low to prevent current vortices from forming within the PN-TEG as already discussed.

In section 7.3.4 it is shown quantitatively that the PN-TEGs exhibit the behavior described in this section. From Figure 4.9b it is expected that a PN-TEG performs poorly at low temperatures when compared to a conventional device, but at higher temperatures the PN-TEG is expected to performs optimally and compete with a conventional TEG. This is in accordance with simulations by Span, simulations using the Onsager model developed by Angst, and experimental observations presented in the results section of this work.

4.2.6 Efficiency

One of the most important quantities for any heat engine is the efficiency of the conversion process. In this section it is shown that the efficiency of a PN-TEG cannot be easily derived in an analytical way like it was done for a conventional device in section 3.1. Moreover, it is argued that a PN-TEG has the possibility to have a fundamentally different conversion efficiency than a conventional TEG. Whether the efficiency of a PN-TEG is larger than a conventional TEG is unclear, but arguments that they are different thermodynamic engines are given.

The approach in this work is to emulate to some extent the process done in section 3.1 to see what would be the general form of an expression for the efficiency of a PN-TEG. The first difference that exists between the conventional thermoelectrics and a PN-TEG, is that conventional thermoelectrics theory is a property of the material, while a PN-TEG is a device, and cannot be treated as a "sum of materials".

If a PN-TEG device is considered, the efficiency of the thermodynamic process would have would have to account for each of the heat transport terms, and the efficiency would have the following general form:

$$\eta_{\mathrm{pn}} = \frac{P_{\mathrm{out}}}{Q_{\mathrm{in}}} = \frac{R_{\mathrm{L}} I_{\mathrm{pn}}^2}{Q_{\mathrm{peltier,pn}} + Q_{\mathrm{conduction,pn}} - Q_{\mathrm{joule,pn}}} \tag{4.17}$$

In the following discussion the four terms in equation (4.17) will be individually analyzed and compared to their conjugates in the conventional TEG.

1. Conduction Heat

We begin with the term $Q_{\text{conduction,pn}}$ which is describes the Fourier heat transport. If we consider the PN-TEG in Figure 4.10, it is possible to arrive to an analytical expression for the open circuit thermal conductance:

$$Q_{\text{conduction,pn}} = (K_p + K_n)\Delta T \tag{4.18}$$

where K_p and K_n are the thermal conductances of the p and n-type bulk sections that make up the PN junction. Hence, describing the term $Q_{\text{conduction,pn}}$ is plausible as a "sum of materials". Therefore $Q_{\text{conduction,pn}}$ remains unchanged from the conventional TEG to a PN-TEG.

2. Joule Heat

Next the attention is turned to the Joule heating term $Q_{\text{joule,pn}}$. In the conventional TEG it was possible to say that that Joule heating spreads equally to the heat source and heat sink because the electrical current density was assumed to be homogeneous. However, as it was shown in the previous section, in a PN-TEG the electrical current density is not homogeneous; there is a higher current density near the hot end, and it is difficult to claim that half of the Joule heating will be deposited back to the heat source.

2. Peltier Heat

Lastly, we turn the attention to the Peltier term $Q_{\text{peltier,pn}}$. For the following explanation see Figure 4.10. At the cold end, in the metal-semiconductor interface, little doubt remains that the Peltier effect there will be a heating mechanism since majority charge carriers leave the semiconductor. However, for the efficiency consideration it is necessary to know how much heat is extracted at the hot side, but at the hot side the PN junction is reverse

biased and the heat balance needs to account for thermal generation of charge carriers plus the diffusion of excess charge carriers. How to describe this thermoelectric effect in a PN junction is not clear today; Gurevich and his colleagues have worked extensively on this problem but not yet came to a final definite description of this phenomenon in the context of traditional PN junctions [17, 16, 13, 12, 79, 80, 81, 14]. Hence, an analytical expression for $Q_{\text{peltier,pn}}$ is also not available.

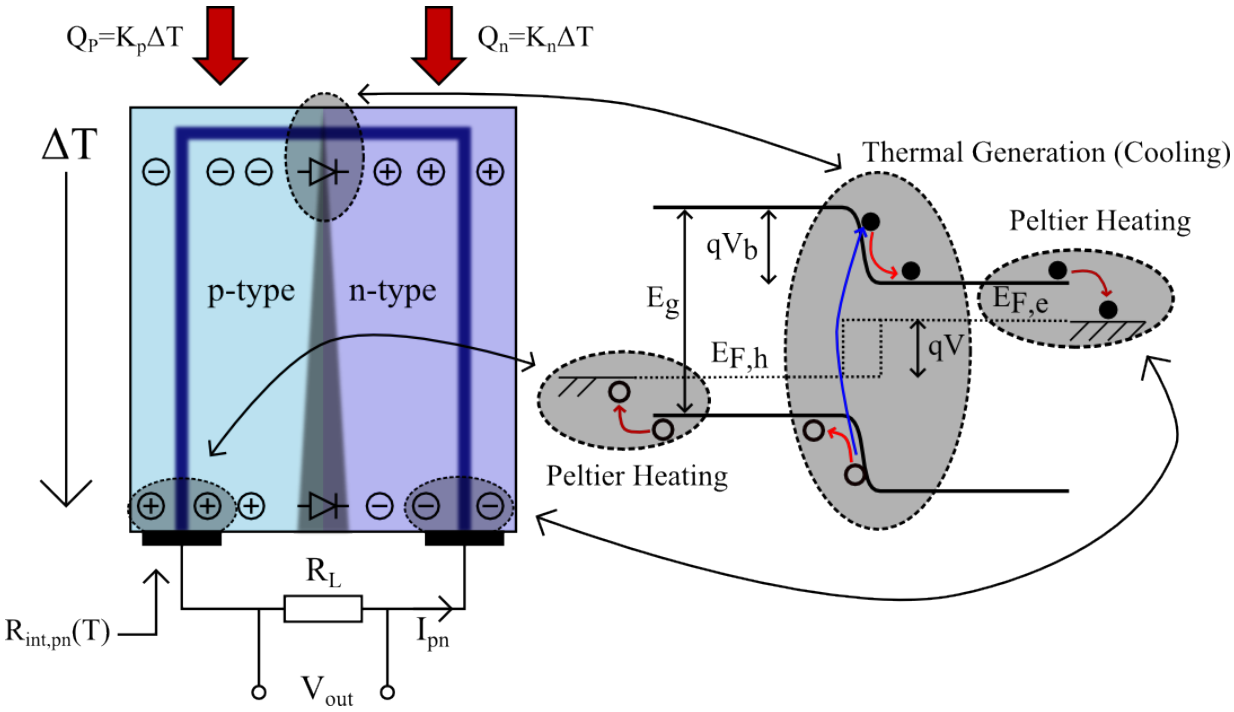

Figure 4.10: Schematic showing an overview of the transport in a PN-TEG. The blue line within the PN-TEG indicates the main electric current path. The blue arrows in the band diagram indicate cooling and the red arrows indicate heating. In a PN-TEG the hot side is reverse biased while the cold side is forward biased.

In summary, it is not possible with the current knowledge to write an analytical expression for the efficiency of a PN-TEG. In conventional thermoelectrics, the figure of merit zT appears in the derivations of the efficiency, however, since this derivation is not possible today for a PN-TEG it is not appropriate to use the conventional figure of merit zT to characterize the PN-TEGs.

Efficiency Through Numerical Calculations

The only access to the efficiency of a PN-TEG today is by numerical simulations. Simulations by Wagner et al. based on a drift diffusion model predict that PN-TEGs will outperform conventional TEGs in efficiency given at large ΔTs [65] (Figure 4.11a). This is because the diode becomes exponentially conductive at elevated temperatures. However simulations done by S. Angst using the described Onsager network show that the efficiency of a PN-TEG is lower than a conventional TEG. In Figure 4.11b simulations by Angst et al show that the power output of a PN-TEG at $\Delta T = 700\,°\mathrm{C}$ is up to a factor of six lower at the maxima. Note that from the simulations from Wagner et al. at $\Delta T = 700\,°\mathrm{C}$ the efficiency of the PN-TEG is a factor of 3.5 larger than the conventional TEG. See Figure 4.11. It is important to note that the simulations by S. Angst do not take into account concentration gradients and thermal generation of charge carriers within the space charge region.

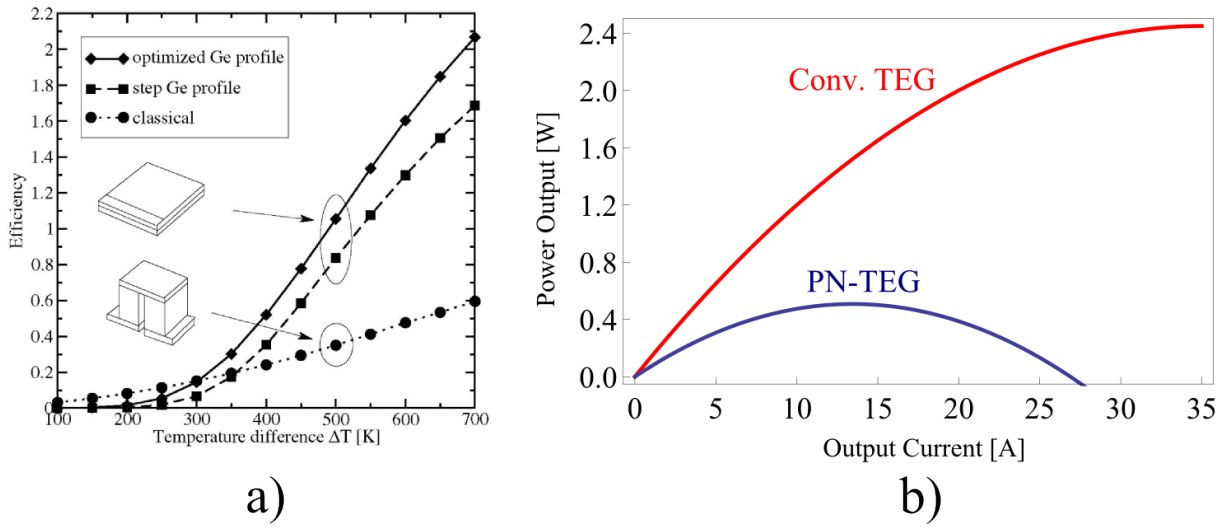

Figure 4.11: a) Drift diffusion simulation from [65] shows that PN-TEGs can outperform conventional TEGs (data given in %). b) Discrete Onsager model from S. Angst with $\Delta T = 700\,°\mathrm{C}$ shows that PN-TEGs have a lower efficiency than conventional TEGs even at high temperatures.

As seen, the question of the efficiency of a PN-TEG remains open. The fact that both

simulations predict different efficiencies for the two architectures, and the fact that there is no current established theory to describe Peltier effects in bipolar semiconductors, could be hints that the two systems are different thermodynamic engines and they simply have different intrinsic efficiencies.

Vining developed an analogy between the thermoelectric heat engine and steam engines [82]. In this analogy entropy is transported by a gas in both engines; in the thermoelectric engine entropy is transported by a Fermi gas, while in the steam engines entropy is transported by an ideal molecular gas. Vining showed that optimizing the material to achieve higher zTs is analogous to optimizing the molecular gas in a heat engine, and he also suggested that an alternative strategy would be to change the engine itself. Given the fundamental differences between a conventional TEG and a PN-TEG, it may be possible that the PN-TEG is fundamentally a different thermoelectric engine.

4.2.7 Geometrical Optimization

Experimental data in Chapter 7 shows that the PN-TEGs can be best modeled with a very low diffusion barrier, that means that internal current vortices develop more pronounced compared to the case when a diffusion barrier is present. For this reason the simulated PN-TEG with no diffusion barrier is selected as more appropriate and shown in Figure 4.12a. From the current density map it can be envisioned that if the PN junction is gradually removed at the cold side, the internal current vortices could be suppressed, leading to higher power outputs and hence efficiencies.

This effect is shown in Figure 4.12b where a simulation by S. Angst, shows that for a cutting length h the power output increases and reaches a maximum. With increasing h the output voltage is increase but also the internal resistance is increased, this leads to a optimal cut length. This is in line with a very similar experiment presented in reference [71] where the authors show that with increasing cut length h, an increased device figure of

merit is observed, however the authors find a different optimal cut length ($h \approx 0.85$). The optimal point in our simulations is found at $h \approx 0.7$ and it will be shown experimentally that the power output indeed increases with h but does not clearly follow the behavior described in Figure 4.12b.

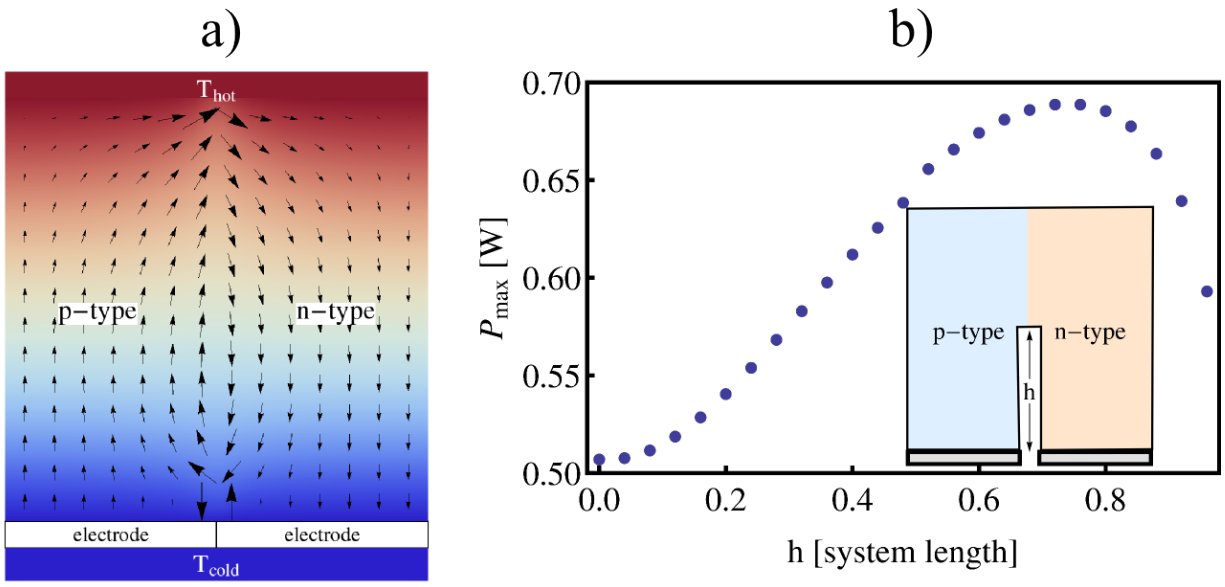

Figure 4.12: a) Current density map for a PN-TEG with no diffusion barrier at $\Delta T = 700\,\mathrm{K}$. b) Simulation shows that the power output can be increased by removing the PN junction near the cold side.

4.3 Summary: PN-TEG Theory

In this chapter the PN-TEG was introduced as a concept whose strongest advantage is the dismissal of the hot side substrate and metallization. This alleviates many technological challenges such as temperature drop across the substrate, electrical and mechanical instability of the metal-semiconductor contacts, and fabrication ease.

From the theoretical aspect it was suggested that the PN-TEG can be modeled as a reverse biased diode with a non-linear shunt resistance, and that the electrical current density is not homogeneous and has 2-dimensional components. It was suggested that the

internal resistance of a PN-TEG should decrease with temperature contrary to a conventional TEG whose internal resistance increase more or less linearly with temperature due to the degenerated doping of the semiconductor material.

Numerical simulations suggest the formation of internal current loops that lead to efficiency losses, and it is suggested that removing a fraction of the PN junction can lead to efficiency improvements. Analytical expressions for the efficiency of a PN-TEG do not seem plausible within the framework of conventional thermoelectrics. However, numerical simulations fail to reach independent agreement on the efficiency of a PN-TEG.

5 Sample preparation

> Education is what remains after one has forgotten what one has learned in school.
>
> Albert Einstein

In this work the aim is to produce large area PN junctions with a PN interface in the order of 10 mm × 10 mm. The goal to produce such large scale PN junctions is a challenge because it goes in against the technological demand to scale down electronic devices and pushes the need to innovate home made customized fabrication techniques. Three types of PN junctions produced with different technologies are reported in this work. In this chapter the three fabrication processes are described. They are:

1. **Current Assisted Sintering:** Involves the sintering and compaction of silicon nanoparticles into a bulk PN junction.

2. **Laser Assisted Cristallization:** Involves the deposition of a thin layer of Silicon nanoparticles on a silicon wafer and subsequent sintering of the nanoparticles.

3. **Current Assisted Bonding:** Involves the welding through Joule heat of two silicon wafers.

Technology 1 is the most promising for thermoelectric applications and it is the focus of

this work, while technologies 2 and 3 were intended to gain scientific understanding of the PN-TEG.

5.1 From Silicon Nanoparticles to Bulk PN Junctions: Current Assisted Sintering

There are two main strategies to produce Silicon nanoparticles, and nanoparticles in general, the so called top-down approach and the bottom-up. The top-down approach, starts with a bulk material that is broken down to nanoparticles by means of grinding (ball milling) for example. Ball milling of SiGe alloys has proven successful to produce nanoparticles for nanostructured bulk materials with superior performance [53].

To produce the nanoparticles for the Silicon PN junctions, a bottom-up approach is adopted; that means that process begins with gaseous precursors. The n-type, phosphorus doped nanoparticles are produced in a plasma reactor and the p-type, boron doped nanoparticles are produced in a hot wall reactor. The nanoparticles are later compacted using a current assisted sintering technique to produce a bulk nanostructured PN junction. The work flow is shown in Figure 5.1.

5.1.1 Nanoparticle Synthesis

The synthesis of different materials for themoelectric applications using the bottom-up approach has been demonstrated [83, 84, 85]. The synthesis of the n-type Silicon nanoparticles used in this work is acknowledged to Nils Petermann and Dr. Hartmud Wiggers while the synthesis of the p-type nanoparticles is acknowledged to the Institute of Energy and Environmental Technology (IUTA) in Duisburg, Germany. The bottom-up approach starts with gaseous precursors that are fed to a reactor. The reactor is heated to tempera-

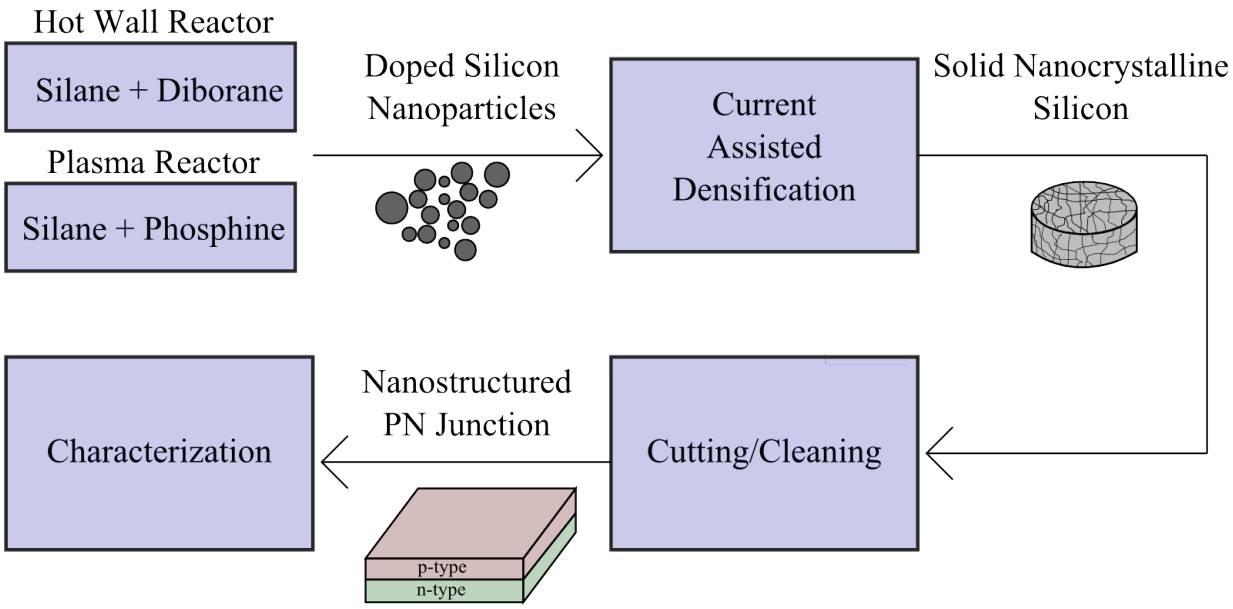

Figure 5.1: Workflow of the bottom-up approach.

tures $> 1000K$ which induces the decomposition of the precursors and result in nucleation and coagulation thus forming the doped Silicon nanoparticles that can range from a few nanometers to a few tenths of nanometers depending on precursor concentration, mass flow and pressure [86].

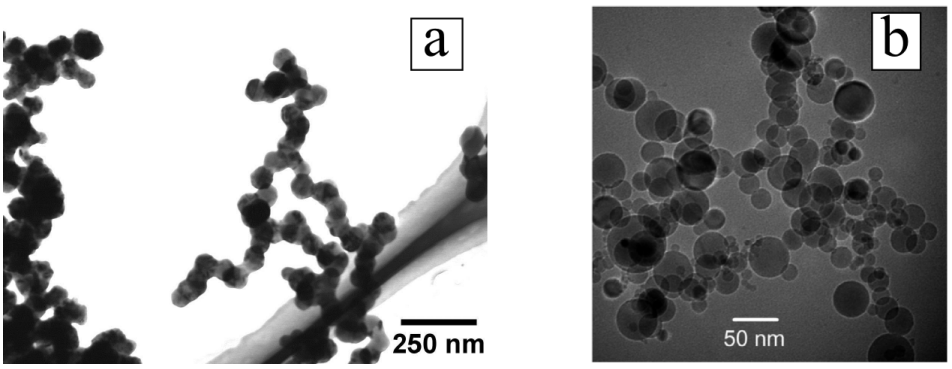

Figure 5.2: a) SEM Image of p-type, boron doped nanoparticles. b) TEM image of n-type, phosphorus doped nanoparticles. From Refs. [86, 49].

Silane (SiH_4) gas is used as precursor gas for silicon. To achieve the in-situ doping precursors are added at a percentage of the silane gas. Diborane gas (B_2H_6) gas is added to

the gas mixture to achieve boron doping while for phosphorous doping phosphine gas (PH_3) is added to the mixture. While a complete decomposition of the dopant precursors and incorporation of the dopants into the nanocrystalline powder is expected, it is also known that only a fraction of the dopants is homogeneously deposited within the nanoparticles while a considerable amount segregates on the surface [86].

The main difference between the n-type and p-type nanoparticles is that the n-type nanoparticles are produced in a microwave plasma reactor, while the p-type nanoparticles are produced in a hot wall reactor [86, 49]. The p-type nanoparticles have a mean diameter of $\approx 150\,\text{nm}$ and the n-type nanoparticles have a mean diameter of $\approx 20\,\text{nm}$, see Figure 5.2. The doping concentration is tunned by adjusting the ratio of the silane gas flow and the doping precursor (diborane or phosphine) gas flow. For example for 1% boron doping concentration, the ratio of silane to diborane is 100 to 1, and this results in a doping concentration of $N_\text{A} = 4.99 \times 10^{20}\,\text{cm}^{-3}$.

5.1.2 Densification: Current Assisted Sintering

The goal of the compaction process is to densify the nanoparticles to a bulk solid material that conserves nanoscopic features. In this case the intention is to create bulk, yet nanocrystalline silicon material with a reduced phononic thermal conductivity. To achieve the compaction of the nanoparticles a technique known by different names such as field activated sintering, spark plasma sintering, or current assisted sintering [87] (the later name adopted in this work) is used. The idea behind current assisted sintering is to force large electrical current densities through the nanoparticles while mechanical pressure is applied. In this fashion Joule heating, specifically at the nanoparticle boundaries and grain boundaries where the highest electrical resistance exists induces the sintering of the nanomaterials.

In order to densify unipolar samples the silicon nanoparticles powder is loaded into a

cylindrical graphite crucible. Two graphite dies with a diameter of 2 cm that fit inside the crucible act like electrodes and as pressure pistons. The powder is precompacted by applying 5 kN on the dies using a hydraulic press. Then the crucible and dies are loaded into a sintering unit with model FCT-Systems D40.

The peak sintering temperature for most of the reported samples in this work is 1100 °C. The cooling and heating rates used were 100 °C/min. The mechanical pressure during sintering was achieved by applying a constant force on the die pistons. The value of the force was varied between either 3 kN or 11 kN depending on sample. A schematic of the current assisted sintering process is sketched in Figure 5.3a.

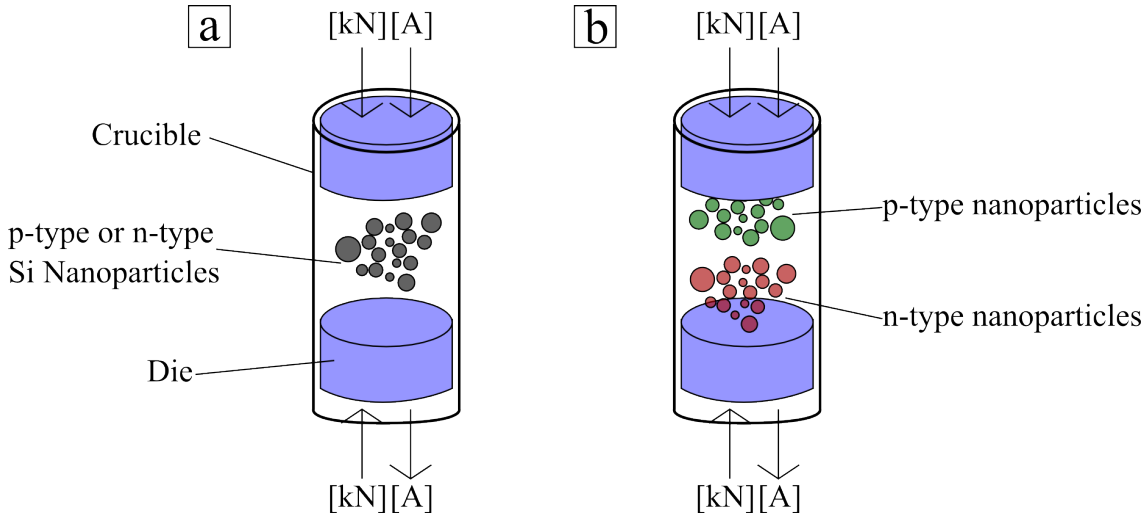

Figure 5.3: Schematic of the current assisted sintering densification process for a) unipolar nanocrystalline silicon and b) nanocrystalline PN junctions.

The melting temperature of bulk silicon is 1414 °C, however the reduced melting temperature of silicon nanoparticles allows the sintering process to be operated at considerably lower temperatures (950-1125) °C yet achieving densities above 97 % of the density of single crystalline silicon [49, 88].

Theoretical work on the dynamics of the current assisted sintering process is presented in ref. [87] where they show that percolation paths in the current leads to localized partial

or complete melting of the nanoparticles that form a viscous material that is able to rearrange as it is mechanically pressed. Experimentally, both p-type and n-type highly doped unipolar nanocrystalline silicon for thermoelectric applications has been successfully achieved using the aforementioned current assisted densification process [56, 49, 51].

With respect to the production of nanostructured PN junctions, Meseth et al. produced nanostructured silicon PN junctions by current assisted sintering, and by scanning the Seebeck effect on the surface of the sample they showed that the resulting densified sample had a spatially defined n-area and a p-type area [89]. Becker et al. used the spatial characterization of the Seebeck coefficient to show that the PN junction can be modeled as a linearly graded junction as opposed to a fragmented or an abrupt PN junction [90].

This work continues with the investigations of Meseth and Becker. So far the description of the current assisted sintering method has dealt with unipolar samples but only a small twist to the preparation process can produce nanostructured PN junctions. The process remains basically the same but instead of loading unipolar nanoparticles powder into the crucible, both p-type and n-type nanoparticles are loaded and processed as shown in Figure 5.3b. After densification the samples are cut in a geometry in the range of 10 mm × 10 mm × 5 mm with the PN interface oriented as shown in Figure 5.4. The nanostructured current assisted sintering samples are then ready for characterization.

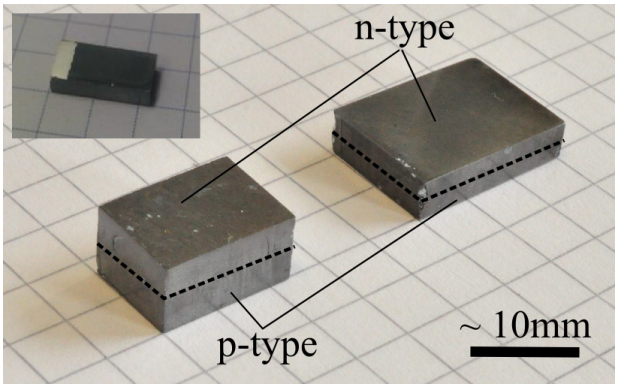

Figure 5.4: Sample PN-TEGs from the current assisted sintering process.

A summary of the nanostructured PN-TEGs is presented in Table 5.1. The sinter bias refers to the orientation of the layers during the sintering process; the layers form a forward bias configuration when the current flows from the p-type material to the n-type material as it is shown in Figure 5.3. When the stacking order of the nanoparticles is inverted an electronic reverse bias configuration is formed. The stacking order during the sintering process has an influence on the nanostructure of the PN junctions [91], and it is seen in Table 5.1 that samples prepared in the reverse bias configuration show a considerable higher internal resistance.

Table 5.1: Summary of the current assisted sintered PN-TEGs. *From the same pellet.

	PN-TEG No.	**Sinter Bias**	**Sinter Temp.**	**Sinter Force**	**Doping**	R_{int}
	2	Forward	1100 °C	11 kN	1%B, 1%P	0.311 Ω
	4	Forward	1100 °C	11 kN	1.5%B, 0.6%P	2.95 Ω
	8	Reverse	1100 °C	3 kN	1.5%B, 0.6%P	120 Ω
	10	Forward	1100 °C	3 kN	1%B, 1%P	4.32 Ω
	11	Reverse	1100 °C	3 kN	1%B, 1%P	174 Ω
	15*	Forward	1200 °C	11 kN	2%B, 1.5%P	0.358 Ω
	16*	Forward	1200 °C	11 kN	2%B, 1.5%P	0.345 Ω
	17*	Forward	1200 °C	11 kN	2%B, 1.5%P	0.502 Ω

5.1.3 Electrical Contacts

Since the nano-crystalline samples are degenerately doped, electrical contacts are not an issue for measurements but they are important to be able to solder the individual PN junctions into a prototype. For this reason the effects of the contacts are investigated. A layer of Ni is deposited on the nanostructured Si by electroless platting. This initial layer of Ni is annealed to form a NiSi that provides a better adhesion to the second layer of Ni which deposited by galvanization. Finally, a capping layer of Ag is deposited by galvanization to improve the adhesion of the solder. This recipe was developed by Kessler et al. and the contact resistance to nanocrytalline silicon was found to be in the range of

$2.66 - 1.47\,\Omega\text{cm}^2$ [36, 54].

To investigate the whether there is degradation of the electrical performance arising from the metallization on the PN-TEGs, 3 samples from the sample pellet measured before and after metallization. The samples are cut in equal geometries and processed in parallel during the contacts deposition. The PN-TEGs are selectively metalized and the undesired metallization is grinded away, leaving a contact on what would be the cold side of the PN-TEG as shown in the inset in Figure 5.4.

The results are shown in Figure 5.5. In the experiment, increasing ΔTs are applied to the PN-TEGs, and the internal resistance is extracted from the IV response in a linear domain near $0V$, the method is described in Section 6.2. Since the metallization is on the cold side, the internal resistance is plotted against the cold side temperature using the setup described in Section 6.3.3. It is observed that there is no clear trend of the effect of the metallization on the PN-TEGs. Sample 2 sees an improvement in the internal resistance after the metallization, sample 5 shows no considerable effect from the metallization, and sample 10 sees a larger internal resistance after metallization. This shows that the effects of metallization are variable, and further optimization is needed. It is important to note however that all the curves in Figure 5.5 converge at larger temperatures, meaning that the negative effects of the metallization at large temperatures are expected to decrease.

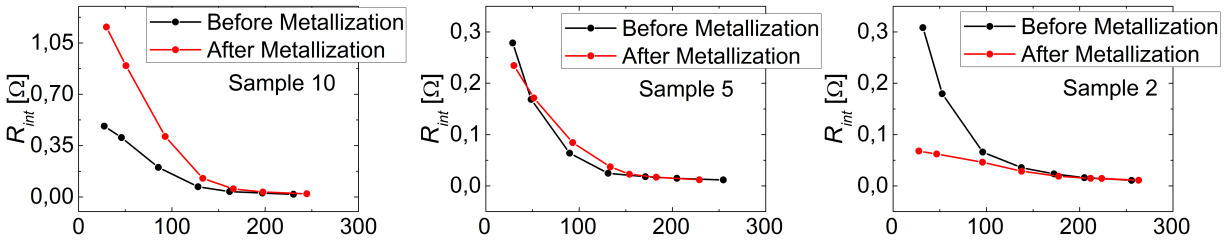

Figure 5.5: Internal resistace for 3 samples before and after metallization, plotted against the cold side temperature $T_C[K]$.

5.2 From Photovoltaic silicon PN Junctions to PN-TEGs: Laser Annealed PN Junctions

To produce the second type of thermoelectric PN junctions a technology from photovoltaics is borrowed since photovoltaic devices generally require large area PN junctions as well. Photovoltaic devices in general take advantage of highly crystalline materials because of higher mobilities and longer charge carrier mean free path. The implementation of highly crystalline silicon would go against the idea of a good thermoelectric material because of the increased phononic thermal conductivity when compared to nano-crystalline silicon. However, the goal is to produce samples that are better defined, and hence easier to study. The system, and process development of this technology in general is acknowledged to Meseth et al. [89, 92, 93]. The preparation of the samples presented in this work is acknowledged to Franziska Maculewicz [94].

The idea behind laser crystallization is to simplify the process of producing PN junctions for photovoltaic applications [93, 92]. The general idea is to deposit a thin layer of doped silicon nanoparticles on a complementary doped crystalline silicon wafer and anneal the nanoparticles layer by scanning the surface of the sample with a laser. In this way, the opposite doping between the nanoparticles and the silicon wafer form a thin emitter layer of a few hundred of nm thick (See Figure 5.6a).

The slight modification that is made in order to adapt the laser sintering process for thermoelectric applications is that instead of a doped wafer, an nominally intrinsic wafer ($1000\,\Omega\text{cm} - 100000\,\Omega\text{cm}$) is used and highly doped nanoparticles of opposite polarity are laser sintered on both sides of the wafer creating a PIN structure as shown in Figure 5.6b. The reason for using a PIN structure instead of a PN structure is to have a symmetric device. Having a symmetric device is important because the electric current flows laterally, in parallel to the PN interface, and the results are easier to interpret when the "leg"

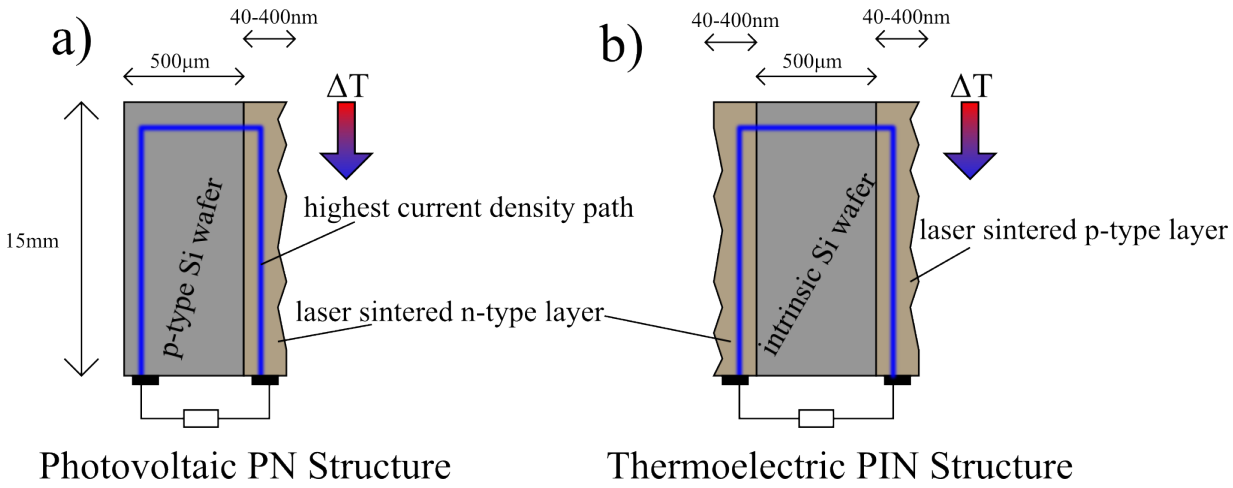

Figure 5.6: Not to scale. a) Photovoltaic PN structure used as a PN-TEG. b) PIN structure used as a PN-TEG. The symmetrical structure in b) makes the device easier to study.

resistances match.

5.2.1 Sample Preparation: Laser Annealing

The preparation of the laser sintered PIN junctions consists of 6 main steps that are illustrated in Figure 5.7 (more details can be found in ref. [94, 93, 92]):

1. **Cleaning:** The intrinsic silicon wafers are cleaned in an ultrasonic bath in Acetone, Isopropanol, and distilled water (5 minutes each).

2. **Wafer Etching:** To remove the native SiO_x layer. The wafers are etched for 60 min in hexafluorosilicic acid (HFS) at $\approx 90\,^{\circ}C$, and rinsed with distilled water.

3. **Spin Coating:** Before spin coating the doped silicon nanoparticles. The dispersion is processed in an ultrasonic bath for $\approx$ 30 min to dissolve the agglomerates and further filtered in a 0.7 μm screen. The dispersion is then spin coated at a rotational speed of 2000 cycles/min for 20 sec with an acceleration of 2000 cycles/min^2. The spin coating process is done once first with a p-type dispersion.

4. **Heating:** The dispersion solution is evaporated by heating the wafers at 125 °C for 5 min on a hot plate.

5. **Nanoparticles Etching:** In order to remove the native oxide layer that forms on the nanoparticles and achieve a more homogeneous and flat layer, the samples are once more etched in hexafluorosilicic acid as in step 2, with a reduced etching time of 2 min.

6. **Laser Assisted Annealing:** The nanoparticles thin film is annealed by using a 248 nm laser (Model: ATLEX-300-SI- KrF) operating with a pulse duration of $4 - 6$ ns. The laser beam is converted to a tophat Gaussian line profile of $10 \times 26\,\mu$m and the sample is scanned with a speed of 9.3 mm min^{-1}. The optical power from the laser anneals the nanoparticles layer and incorporates it into the wafer.

7. Steps 3-6 are repeated with an n-type dispersion on the opposite side of the wafer.

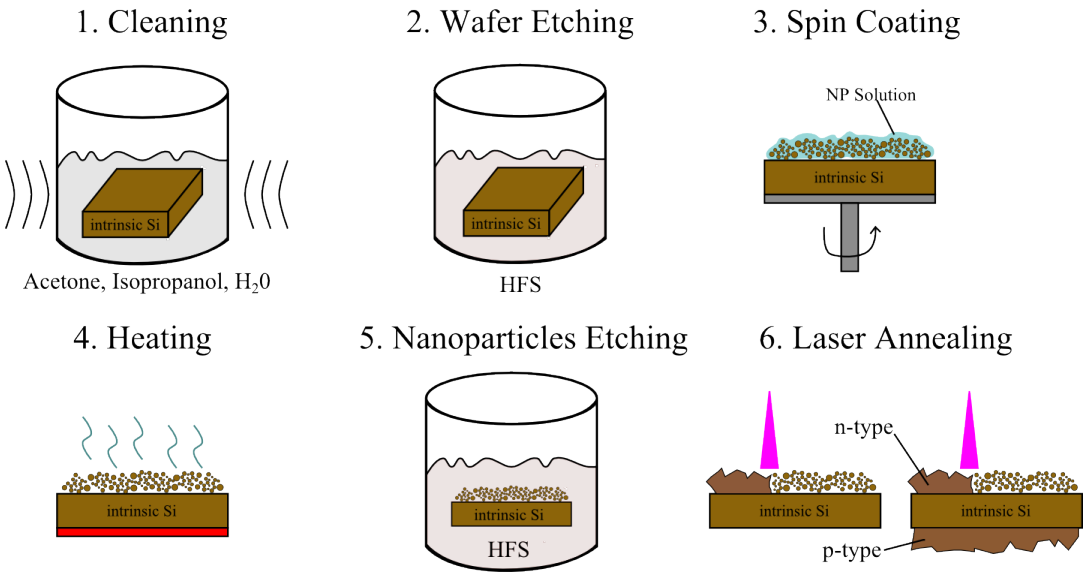

Figure 5.7: Not to scale. Preparation process of the laser annealed PN structures.

The process described above produces PIN structures that are used as PN-TEGs. Having a high, degenerated nominal doping concentration of the dispersion, $N_A = N_D = 5 \times$

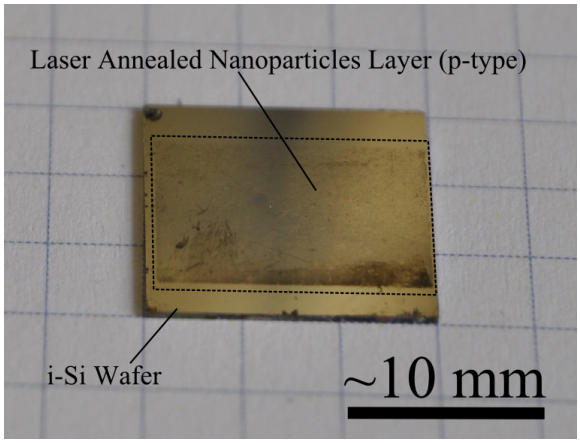

Figure 5.8: One side of a laser annealed PN junction. The same type of structure is found on the other side.

$10^{20}\,\mathrm{cm}^{-3}$, facilitates the electrical contacting to the PN-TEGs and reduces the problems associated with Schottky barriers. Since the wafers are bigger than the laser line, a PN interface is formed only on a fraction of the wafer. A photograph of a sample is shown in Figure 5.8.

5.3 Si PN Junctions from Wafers: Current Assisted Bonding

While the realization of crystalline PN junctions from the laser annealing process is quite successful, the very thin conductive layers result in very high internal resistance, since the electrical current flows in a cross sectional area that is at largest $15\,\mathrm{mm} \times 400\,\mathrm{nm}$ (shaded area in Figure 5.9a). In order to alleviate this problem, a third type of PN junctions is produced. The approach in the current assisted welding method is to take two doped wafers of opposite polarity and weld them together to create a well defined bulk PN junction, with a crystalline material, and a larger lateral cross-sectional area $15\,\mathrm{mm} \times 500\,\mu\mathrm{m}$ of as shown in the shaded area in Figure 5.9b.

Hot wafer bonding has been successfully demonstrated with direct bandgap semiconductors, specifically for light emitting and high speed electronics [95, 96, 97]. The original idea demonstrated by Liau and Mull consists of pressing the wafers together at elevated temperatures [95]. Since the hot wafer bonding requires elevated temperatures, above 1000 °C, diffusion of the dopants is expected and the process must be as short as possible. Nonetheless, this technique has been successfully applied to produce large area PN junctions for optoelectronic applications [96, 97].

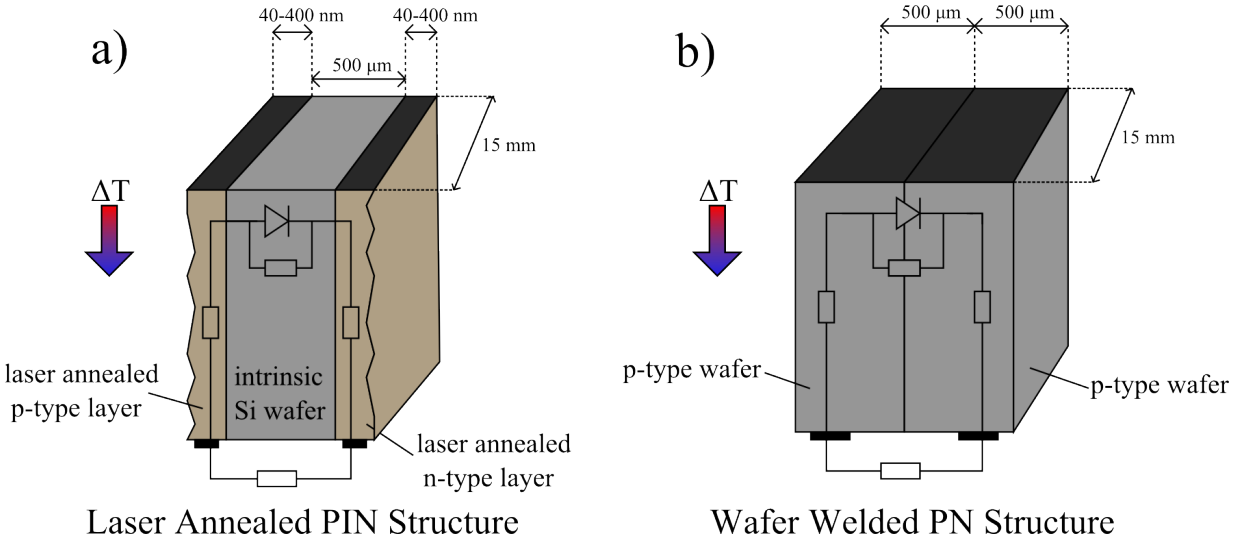

Figure 5.9: a) The very thin doped layers of the laser annealed samples results in large internal resistance. b) This problem can be alleviated by transforming the thin film PN junction into a bulk PN junction with larger cross sectional area (shaded).

Because the hot wafer bonding requires very large temperatures, near the melting point of the materials, an enclosed reactor is required in general. The idea of the welding assisted setup here described is to create a pilot prototype that is much simpler and flexible in design and operation. The basic working principle of the welding assisted setup is to mechanically stack two oppositely doped wafers and force a large current through them. Since the larger resistance is expected at the junction of the two wafers, the majority of the heat dissipation occurs there thus welding the wafers together. The construction and development of the

setup is acknowledged to D. Albrecht in the frame of his bachelor thesis [98]. The setup is discussed in detail in the following sections.

5.3.1 Current Assisted Welding Setup

For the following description refer to Figure 5.10a. The wafer welding setup is composed by two steel punches that hold the wafers in place and serve as electrodes. Prior to welding, the wafers are etched using HFS to remove the surface oxide layer. Pressure is achieved by tightening two plates on top of the punches with screws. Between the punches, the n-type and p-type wafers are stacked on top of one another to form a "forward bias" configuration with respect to the current flow. An electrical current in the range of $0 - 15\,\mathrm{A}$ flows through the punches and wafers. Since most of the voltage drop is expected to occur at the wafer-wafer interface, the majority of the electrical power is should be dissipated at the PN interface, hence partially melting the wafers and creating a mechanical bond. However heat might not be the only bonding mechanism, as electromigration and atomic diffusion could be as well occurring. Temperature sensors are located 1mm away from the wafers to provide approximate temperature readings of the wafers.

The process is automated using LabView. The system is driven by the current flowing through the punches which is ramped up in steps of $100\,\mathrm{mA}$ until it reaches a value in the rage of $10 - 20\,\mathrm{A}$, depending on sample. Between each step a hold time of $10\,\mathrm{sec}$ is programmed. The voltage and power output, as well as the temperatures on the punches is monitored. A sample output protocol is shown in Figure 5.10b. The temperature near the wafers as well as the welding power parameters (currrent, voltage, power) are monitored. The entire process takes about $20\,\mathrm{min}$ after which the PN-TEGs are ready.

This welding setup is intended as a prototype to explore the potential of current assisted welding and for this reason, it has several aspects that should be further developed. For example, the thermocouples do not provide the actual temperature of the wafers, or in

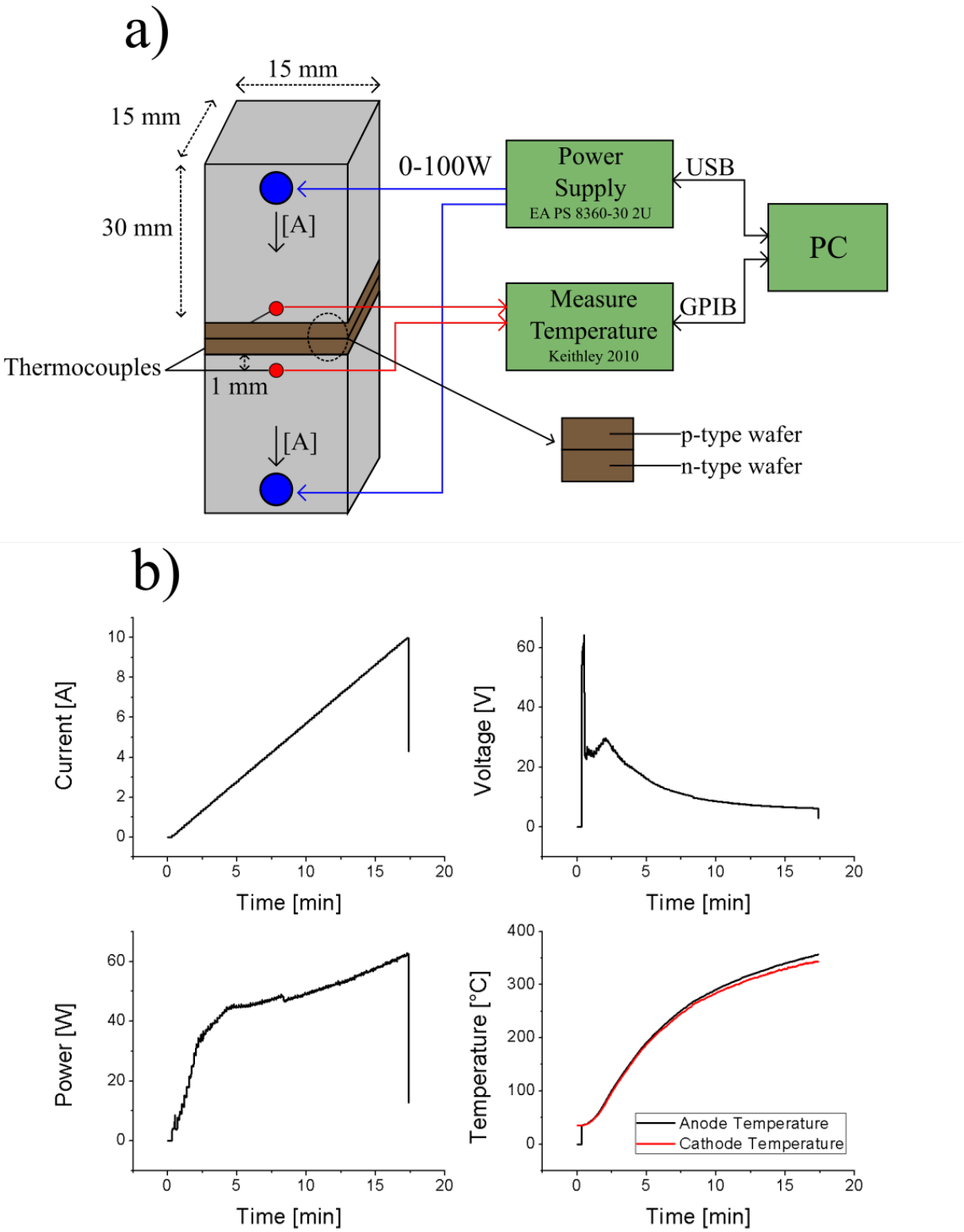

Figure 5.10: Schematic of the home built wafer welding setup.

particular of the PN junction. For a more controlled process it would be important to know the temperature of the junction. Also, the pressure on the punches is adjusted merely by hand, and it would be desirable to have a controlled pressure system. However, this technique proves successful in welding wafers that ultimately respond as diodes and can be used as TEGs. A PN junction produced by the wafer welding setup is shown in Figure 5.11.

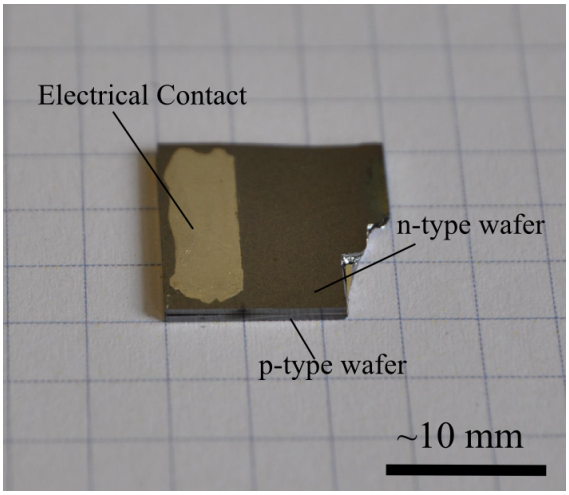

Figure 5.11: PN junction prepared by the current assisted welding method. The two wafers can be distinguished in the lower left corner where they are slightly misaligned.

5.3.2 Electrical Contacts

After the wafers have been welded, electrical contacts are deposited. The wafers used for the production of the PN junctions are highly doped $N_A = N_D = 10^{19}\,\mathrm{cm}^{-3}$ or non degenerated $N_A = N_D = 10^{15}\,\mathrm{cm}^{-3}$. Aluminum contacts are deposited using chemical vapor deposition with a nominal thickness of 300 nm and thermally annealed at 450 °C for 5 sec with a heating ramp of 45 °C/sec based on ref. [99].

To verify the annealing process of the electrical contacts on the non-degenerated samples, contacts are deposited on the surface of the wafers as shown in Figure 5.12a and the IV

characteristic measured using a 2-point measurement with a Keithley 4200 prior to the annealing step. After the annealing step the IV characteristic is measured again.

Here the analysis is separated between n-type and p-type. In Figure 5.12b it can be seen that the n-type wafers do not show a considerable improvement from the annealing step. However in Figure 5.12c it can be seen that the p-type wafer shows a tremendous improvement in conductance of 3 orders of magnitude. After the annealing step, both types of wafers are brought to the same conductance range which makes sense since both types of wafers have the same nominal doping concentration. Here it is important to recall that the recipe used for the annealing step was made for n-type wafers, but from our experiments there was no improvement for the n-type wafers, instead the improvement was seen for the p-type wafers.

The annealing step does not improve the conductance of the highly doped samples (not shown). It is shown in ref. [98] that more important than tempering the highly doped samples, it is to etch the surface oxide layer. After etching the samples, the contacts are evaporated and good Ohmic contacts are formed bringing the conductance of the samples to the same range. This is shown in Figure 5.13. Note that the conductance levels of the highly doped samples is much larger than the non-degenerated samples and that the conductance of the n-type wafer is larger than the p-type wafer since electrons have a higher mobility than holes in silicon.

5.4 Summary of Sample Preparation

The main goal is to produce large area, highly doped PN junctions. In this work we employ three methods to produce the PN junctions that are operated as PN-TEGs. All three methods are proven to be successful to fabricate the PN junctions. However, each process produces different types of PN junctions, each with different electrical and thermoelectrical

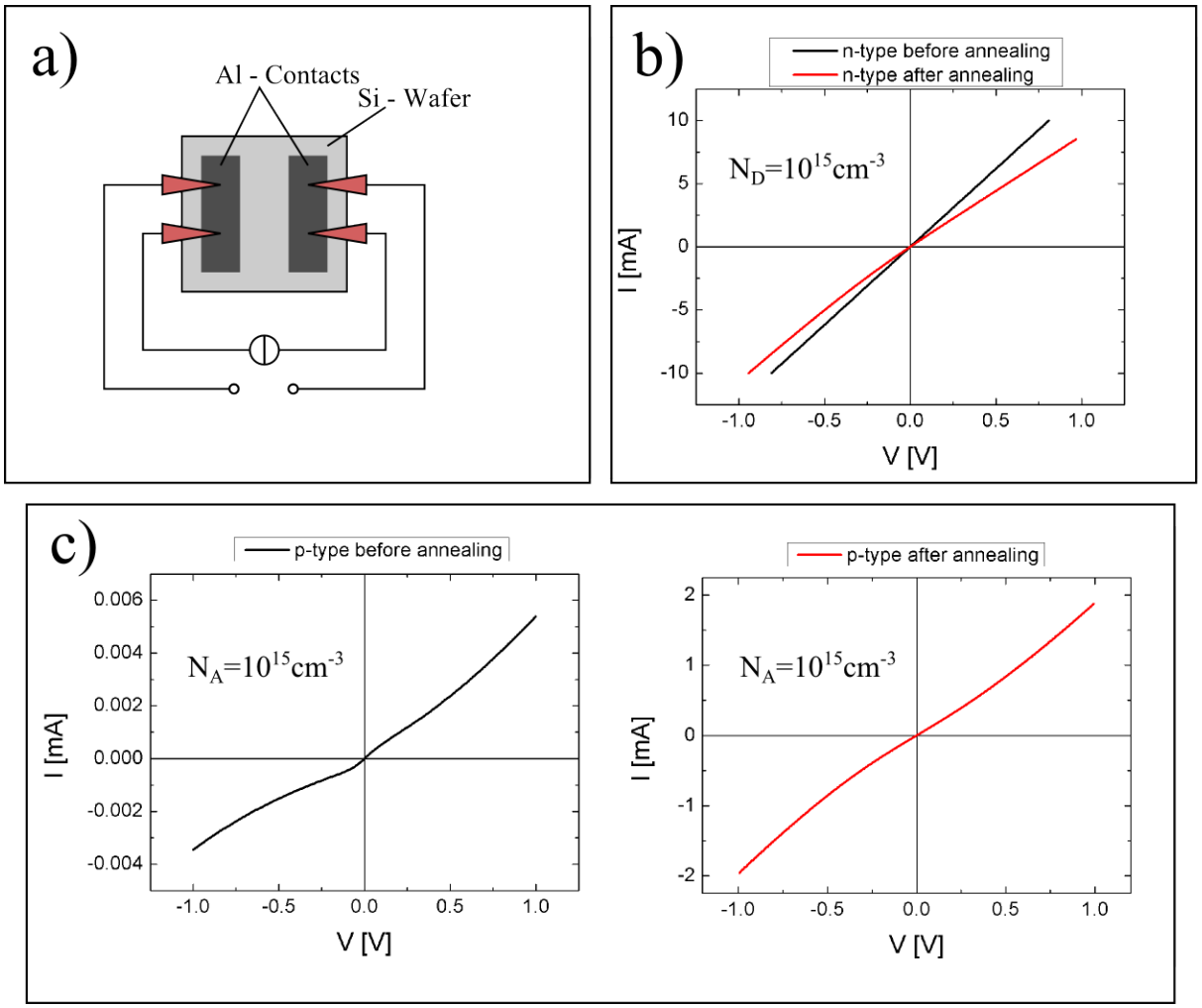

Figure 5.12: a) Schematic showing the deposited contacts and measurement. b) IV characteristics show no improvement of annealing the n-type wafers. c) IV characteristics show that the conductance can be improved by 3 orders of magnitude on p-type samples by annealing.

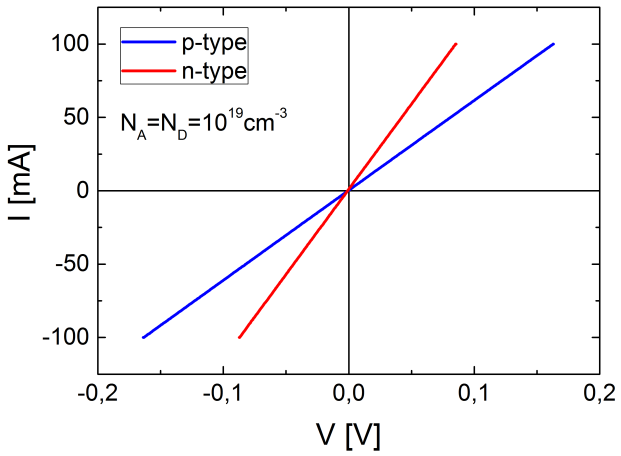

Figure 5.13: IV response of the samples after etching and deposition of the contacts with no thermal treatment.

properties, this is schematically drawn in Figure 5.14.

The general motivation to produce different types of PN junctions is that while nanocrystalline PN junctions are better thermoelectrics, they are less ideal diodes electronically speaking and that makes the interpretation of some of the results more difficult. Therefore the motivation to produce more crystalline samples that have poor thermoelectric characteristics but are better defined structurally and electronically, and this facilitates the understanding of some underlying phenonomena in the general operation of the PN-TEGs.

The discussion of the results will concentrate on the nanostructured PN junctions prepared by the current assisted sintering method because this type of PN junction shows the most promising results as a thermoelectric generator. It will be shown in future chapters that nanostructured PN junction TEGs can perform in the same output power range as a conventional device while the other two types of generators perform poorly from the thermoelectric standpoint but help in the fundamental understanding of the electrodynamics.

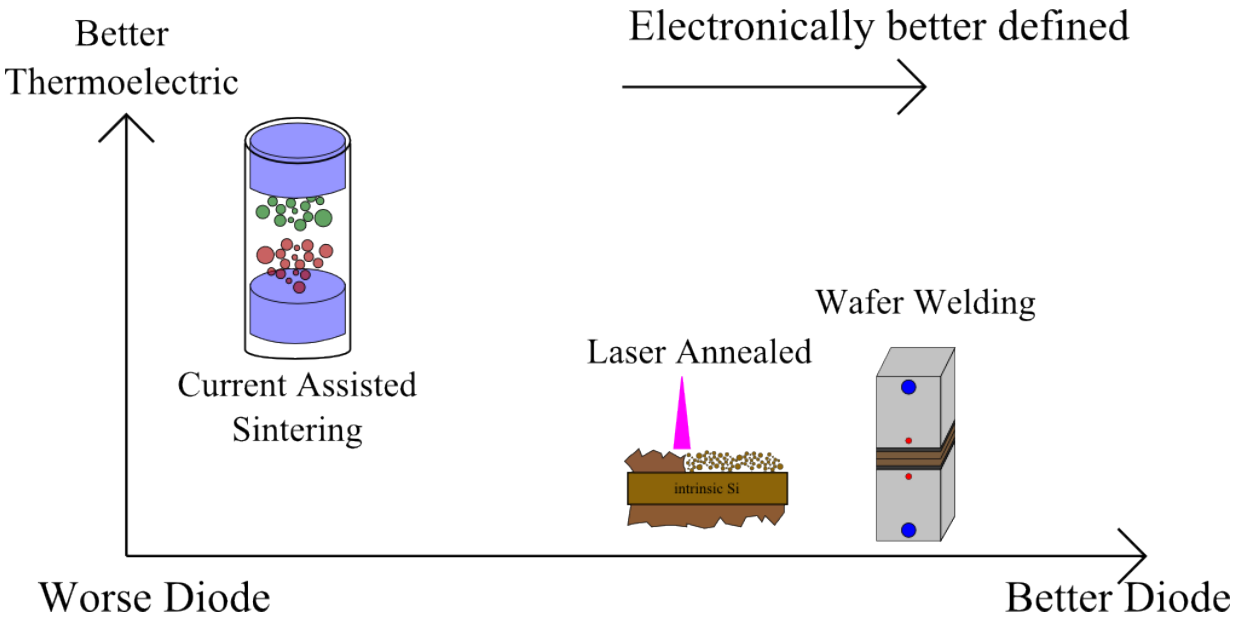

Figure 5.14: Relationship between highly ideal diodes and thermoelectric performance.

6 Metrology and Characterization

> Start by doing what's necessary; then
> do what is possible; and suddenly
> you are doing the impossible.
>
> Fracis of Assisi

The metrology and characterization of the PN-TEGs is a challenging topic for two main reasons: There is very little experimental work done of these type of devices, that means that the instrumentation has to be designed and developed for the purpose of characterizing the PN-TEGs in high temperature environments. A secondary aspect that is challenging is that a PN-TEG is not clearly defined within the theoretical frame of thermoelectrics as it was shown in Chapter 4 where the fundamental theory of the PN-TEG was introduced. If it is unclear how to define the some of the working parameters of a PN-TEG, the question of *what quantity should be measured?* also becomes poorly defined in the case of some parameters, not all.

Some of the characterization will naturally employ standard methods such as an Scanning Electron Microscope (SEM). The metrology and characterization of the PN-TEGs is divided into three main categories and every category will seek to answer specific questions:

- **Structural Characterization:** The use of commercial equipment such as a Scanning Electron Microscope (SEM) and in-house developed methods like the Optically Beam Induced Voltage (OBIV) technique.

How are the two materials joined together at the microscale?

- **Electronic Characterization:** Development of necessary hardware to use standard techniques to characterize the pure electronic properties of the PN-TEGs.

  What is the ideality factor of the PN-TEGs (diodes)?

  What is the effective bandgap of the PN-TEGs?

- **Thermoelectric Characterization:** Development of metrology and techniques to characterize the PN-TEGs when operated in high temperature conditions.

  What is the power output, the device Seebeck coefficient and internal resistance of the PN-TEGs?

In a sense, the characterization follows a bottom-up approach as well. First the structure of the samples is examined, to gain a firs degree inspection of the device. This is followed by the electronic characterization which provides deeper understanding of the PN junction in particular. And finally, the PN-TEG is tested in operating conditions and the thermoelectric response is obtained.

6.1 Structural Characterization

The structural characterization is made by using a commercial SEM (Model: JSM-7500F from the company Jeol), and by a home-made optical induced voltage technique. The OBIV technique is one of a family of measurements that fall under the scanning light stimulation measurements. In this family of measurements a monochromatic light beam (typically a laser) scans the surface of the sample and the a change in the electronic response is monitored. In this way it is possible to measure an optically induced resistivity change, or Seebeck effect imaging [100, 101, 102].

For the characterization of the PN-TEGs a monochromatic light source with $\lambda = 532\,\text{nm}$ or $\lambda = 808\,\text{nm}$ scans the surface of the PN-TEG and the optically induced voltage is measured at every coordinate in a 2-dimensional space (here λ refers to wavelength). The measurements are acknowledged to L. Bitzer and the technique is described more in detail in ref. [100].

If the energy of the incident light on the semiconductor surface is larger than the bandgap of the semiconductor, light is absorbed and electron hole pairs (EHP) are generated. The generated EHPs might recombine non radiatively leading to the emission of phonons (local heating), or if the EHPs are generated near a space charge region, there is a probability that the EHPs are separated and become majority charge carriers leading to an optically induced voltage. In the wafer welded samples the PN junction is "buried" under the p-type wafer, hence, the longer wavelength is applied on the wafer welded samples since the absorption coefficient is significantly reduced in the infrared range and this allows longer penetration depths to be achieved and generate EHPs near the space charge region [103]. See Figure 6.1 for reference.

In an optically induced voltage measurement then, the voltage can arise due to a thermoelectric effect (local heating) or due to a photovoltaic effect. In our case the injected optical power is too low to produce non-negligible temperature gradients. If the optically induced voltage is due to the photovoltaic effect, it is possible to gain great insight on the electronic/spatial nature of the PN junction. In other words, it is possible to "see" the PN junction in the spatial domain.

The nanostructured PN-TEG is scanned in a plane perpendicular to the PN interface while the wafer welded PN-TEG is scanned in a plane parallel to the PN interface, as shown schematically in Figure 6.1. The third type of PN-TEGs, the laser annealed samples have been previously measured with this technique [92]. The output from a measurement is a 2-dimensional plot of the optically induced voltage at every coordinate. An OBIV

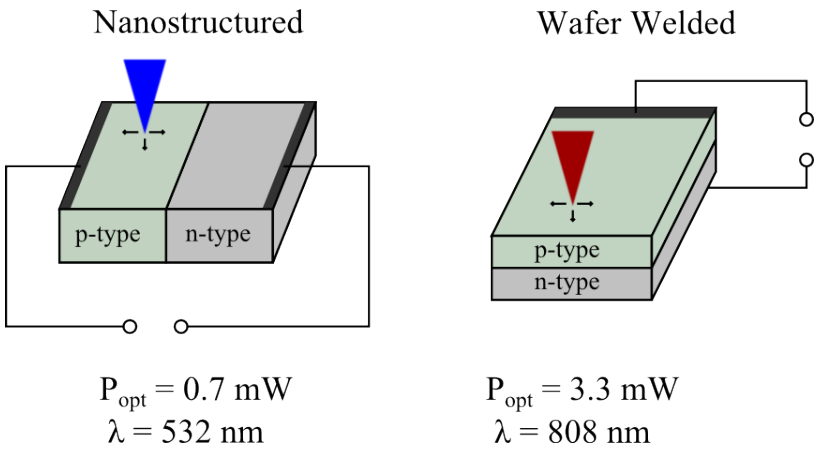

Figure 6.1: Schematic of the OBIV Measurements and the different parameters used.

measurement is valuable because it provides information on the electronic and structural nature of the PN junctions as it is shown in the results section.

6.2 Electronic Characterization of the PN Junctions

In the bottom-up characterization idea, after having learned something about how the PN-TEGs look like, we proceed to study the electronic response of the PN-TEGs when a voltage is applied. This is a very important step preceding the thermoelectric characterization, because in the thermoelectric characterization a ΔV and a ΔT are both present, whereas in the electrical characterization only a ΔV is present.

6.2.1 Equivalent Circuit and Extracted Parameters

The most important characterization data of the PN-TEGs is the Current-Voltage characteristic, or IV scan which can be done under $\Delta T = 0$ or $\Delta T > 0$. This section thermal equilibrium is assumed. The characteristic parameters obtained in thermal equilibrium widely predict the performance under a temperature gradient while shedding light into the composition of the PN-TEGs.

The proposed model is shown in Figure 6.2 and is very similar to the basic model used in photovoltaics; a diode in parallel with a shunt resistance and a non-linear space charge limited current (SCL) resistor (the reason for the introduction of this non-linear element comes in the Results chapter). In series to that, is a series resistance. All resistances are assumed to be linear unless otherwise noted. Here is important to note that this electrical model applies to thermal equilibrium conditions.

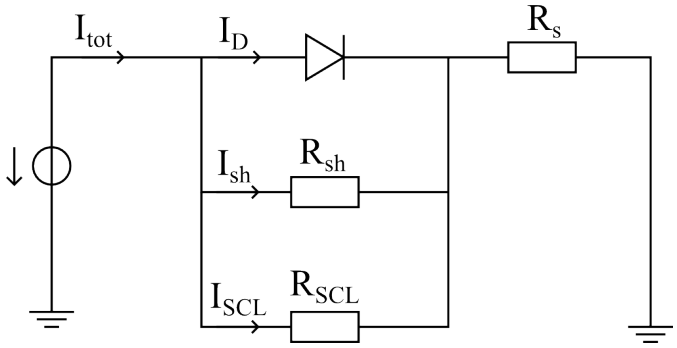

Figure 6.2: Equivalent Circuit of the PN-TEGs.

The goal then is to extract the values of the resistances R_{sh}, R_{SCL}, R_{s}, and in doing this, access to an approximation of the ideality factor is gained. While the characteristic parameters just mentioned are obtained in a thermal equilibrium, they still hold most of their meaning when a temperature gradient is applied, only some minor considerations need to be made. The process to extract the desired parameters is done by calculation of the current flowing through each element, namely I_{tot}, I_{sh}, I_{SCL}, I_{D}, as shown in equivalent circuit in Figure 7.7.

6.2.2 Effective Bandgap

Theory

An electro-thermal method is used to investigate the bandgap of the PN junctions as opposed to photospectrometry. The advantage of using an electro-thermal method is the

simplicity of the experiment. In this method, the temperature of the sample is varied and the IV response is observed. In a widely used method the reverse bias current I_0 is measured at a fixed reverse bias for different temperatures and then plotted in a logarithmic scale against $1/T$, where the slope of the plot is a factor of the bandgap [76, 104].

In our case however, instead of taking the reverse bias current and plotting it against $1/T$, the slope of the IV scan around 0 V, or the internal resistance is taken and plotted against temperature. This is not exactly the same as taking the reverse bias current, because in taking the resistance around zero bias, the diode is lumped with the shunt and SCL resistances. Therefore the term "effective" bandgap, because it is more important to know the effective bandgap of the PN-TEG as a device, than it would be to separate the currents (I_D, I_sh, I_SCL), and determine the bandgap with respect to I_D only.

As explained in section 4.2.5, the temperature dependence of the internal resistance of the PN-TEG can be linearized because the open circuit voltage is in the order of mV and expressed as the ratio of the output circuit voltage and the short circuit current

$$R(T_\mathrm{avg}) = \frac{V_\mathrm{oc}}{I_\mathrm{sc}(T)} \tag{6.1}$$

If we recall that the open circuit voltage V_oc is given by the factor of the temperature difference and the sum of the Seebeck coefficients, and the short circuit current is dominated by the reverse diode current I_0 then the internal resistance can be written as

$$R(T_\mathrm{avg}) = \frac{(\alpha_p + \alpha_n)\Delta T}{A\left(\frac{qD_\mathrm{h}}{L_\mathrm{h}N_\mathrm{D}} + \frac{qD_\mathrm{e}}{L_\mathrm{e}N_\mathrm{A}}\right) n_\mathrm{i}^2(T) + A\frac{qW}{\tau_\mathrm{g}} n_\mathrm{i}(T)} \tag{6.2}$$

In equation 6.2 we recognize that the terms in the denominator have the strongest dependency on the temperature by means of $n_\mathrm{i}(T)$. Therefore, the temperature response of the

internal resistance can be expected in the following form:

$$R(T_{avg}) \propto \exp\left(\frac{E_g}{\xi k_B T}\right) \tag{6.3}$$

where $1 \leq \xi \leq 2$. Here ξ is not to be confused with the ideality factor η_{D}; it refers to whether the current is dominated by $n_{\mathrm{i}}(T)$ or $n_{\mathrm{i}}^2(T)$. This means that the effective bandgap can be extracted from the slope of $R(T_{\mathrm{avg}})$ as shown in equation (6.3) and this value can have a factor of 2 in the uncertainty. The uncertainty in measuring the effective bandgap is high, however useful to gain an idea of the order of magnigute.

Here it is important to recall that electrical characterizations can be done in thermal equilibrium or under a temperature difference. For this reason , a distinction is made between the thermal equilibrium bandgap $E_g|_{\Delta T=0}$ and the temperature gradient bandgap $E_g|_{\Delta T\neq 0}$, however the process from the electrical point of view is the same in both conditions.

Procedure

There area two ways to heat up the sample. In the first method the PN-TEGs are heated up homogeneously using the furnace described in Section 6.3.1. In the second method the PN-TEGs are heated by increasing the temperature difference across the boundaries of the sample using the Monkey Setup described in section 6.3.2.

In any case the process from the electrical point of view is the same; the slope of the IV curve is taken in the voltage range of $-100\,\mathrm{mV} \leq V \leq 0\,\mathrm{mV}$ as shown in Figure 6.3. The inverse of the slope is the value of R_{int} and this value is plotted against the inverse of the temperature, and from the slope of this plot access to the equivalent bandgap E_{g} is extracted. Recalling that $1 \leq \xi \leq 2$ means that the extracted bandgap has an uncertainty factor of 2. The interpretation of the results is presented in the Results chapter.

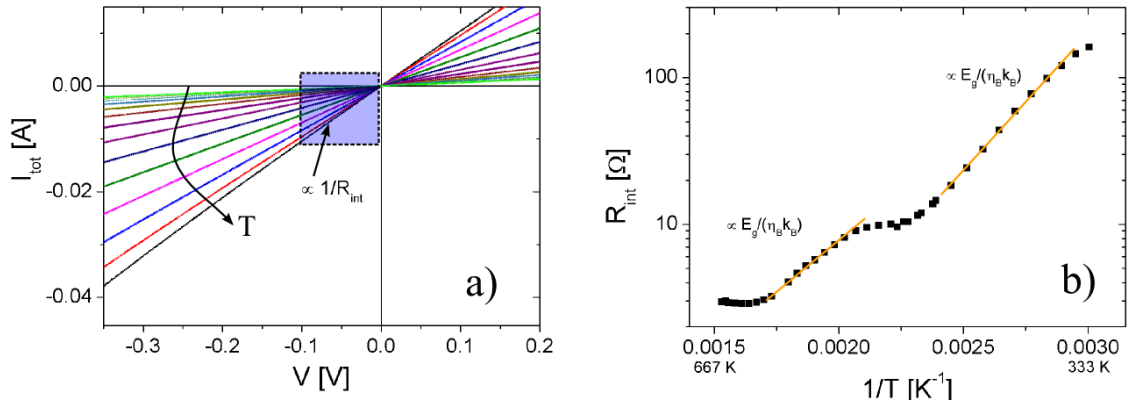

Figure 6.3: a) IV scan at increasing temperatures shows the extraction of R_{int}. b) Plot of R_{int} vs $1/T$ and the extraction of the equivalent bandgap.

6.3 Thermoelectric Characterization of the TEGs

For the homogeneous heating of the samples the Harman setup will be used. In this setup, homogeneous heating is accomplished by radiating infrared light sources arranged in a confocal configuration. This setup serves a dual purpose; it is used to measure the temperature dependent conductance of the PN-TEGs and it is also used to measure the thermoelectric figure of merit of conventional TEGs.

For the temperature gradient based measurements, the monkey setup is employed. In this setup a temperature gradient is accomplished by heat conduction through a Ohmic heater on one end of the sample, while the other end is cooled down by a water cooled heat sink. This setup is exclusively designed for PN-TEGs. Both systems were designed and built in the framework of this thesis.

6.3.1 The Harman Setup

As already mentioned this setup is designed to measure the device figure of merit on conventional TEGs, and with minimal hardware modification it can be used to perform temperature dependent conductance measurements on the PN-TEGs. Firstly the hardware

is described. Measuring the device ZT is important because it allows us to compare a silicon conventional TEG to a silicon PN-TEG. Measuring the temperature dependent conductance of the PN-TEGs is important to gain understanding on the diffusion barrier height.

Hardware: The Furnace

An overview of the hardware is shown in Figure 6.4a; a glass tube serves as a vacuum chamber at a pressure of approximately 10^{-6} mBar. The reflector is made of 6 infrared lamps arranged in a confocal configuration as shown in Figure 6.4b so that the light is concentrated at the position of the sample holder. The reflector is cooled down with water flowing through it. Since gold is known to have superior reflecting properties in the infrared range of the spectrum, the reflector is covered with a thin layer of gold. Although the vacuum chamber can be heated to over 1000°C, the presented measurements will not exceed 700°C, and in this range the chamber can be controlled through a proportional integral differential (PID) controller and a power supply to ± 0.05°C.

In the case of Harman measurements, the TEGs are mounted on four steel tabs which are cut hollow to reduce thermal contacts (Figure 6.4c) and then enclosed in a steel heat shield that adds thermal inertia and aids to a more homogeneous heating of the TEG (Figure 6.4d). This heat shield proves to be of crucial need because even in such a quasi-static temperature inside the chamber, the PID control loop dynamically adjusts the output and without the heat shield, this modulation in heating power creates temperature inhomogeneities in the TEG which are reflected in the IV curves. A thermocouple is present inside the heat shield to provide reading of the TEG's temperature while the PID loop is fed with the external thermocouple (Figure 6.4c).

For the conductivity measurements the only thing that needs to be modified in the hardware is the sample holder; the holder shown in Figure 6.4c is replaced with the one described in section 6.3.3.

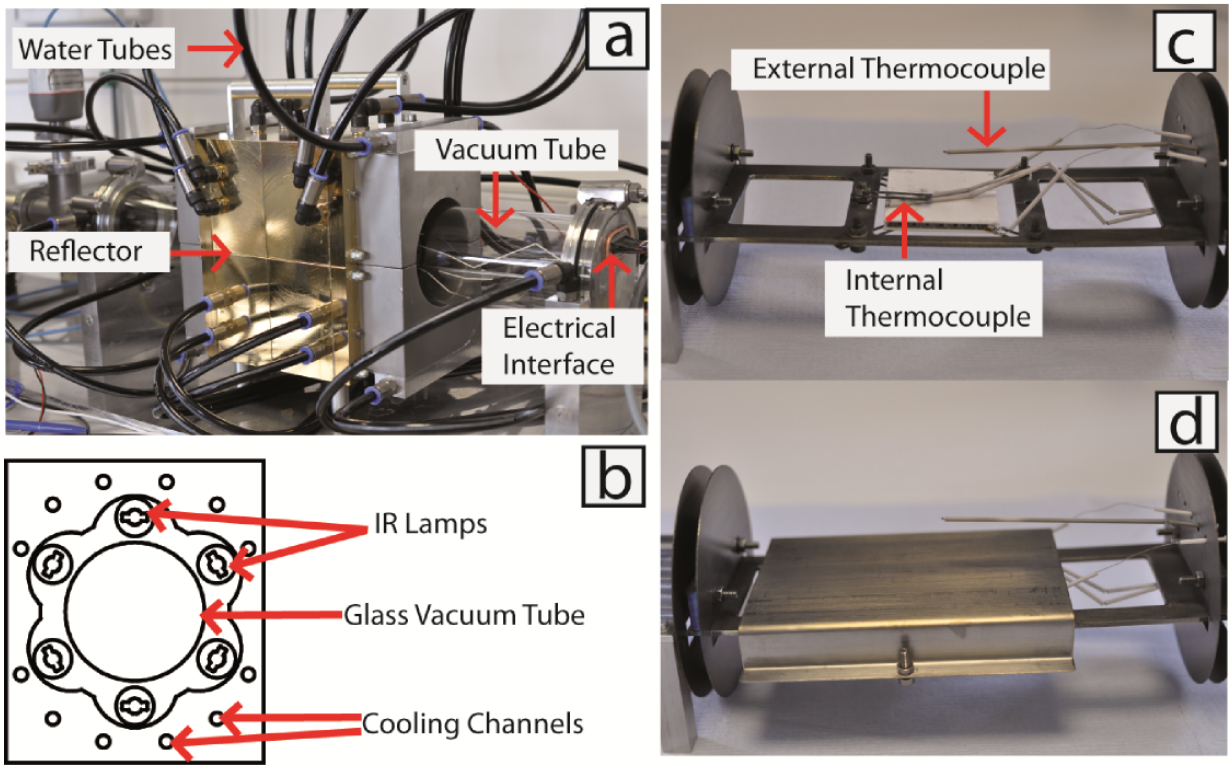

Figure 6.4: Oven construction schematic. a) overview, b) cross-sectional view of the reflector, c) sample holder, d) heat shield. From [105].

The Harman Technique: Measuring ZT on conventional TEGs

The Harman technique is used to measure the device figure of merit ZT. This technique is very valuable because it makes it possible to measure ZT in terms of two voltages and furthermore the quantity ZT accounts for the parasitic effects in the device whereas the material figure of merit zT is a material property. Harman realized that when a steady state current I_{dc} is applied to a thermoelectric material, and given that adiabatic conditions exist, the heat transported by the Peltier effect is equal and opposite to the heat transported by the open circuit thermal conductivity [106]

$$\alpha I_{\mathrm{dc}} T = \kappa_{\mathrm{J}} \Delta T_{\mathrm{p}} (A/L) \tag{6.4}$$

where ΔT_{p} is the temperature difference developed by the Peltier effect, A the cross sectional area perpendicular to the current density and L the length along the current density. Under these conditions the temperature difference ΔT_{p} gives rise to an additional Seebeck voltage that couples to the Ohmic voltage and the total voltage drop across the specimen can be written as

$$V_{\mathrm{tot}} = I_{\mathrm{dc}} \rho (L/A) + \alpha \Delta T_{\mathrm{p}} \tag{6.5}$$

And after equations (6.4) and (6.5) are combined, the material figure of merit can be written as:

$$zT = \frac{\alpha \Delta T_{\mathrm{p}}}{I_{\mathrm{dc}} \rho (L/A)} = \frac{V_{\mathrm{Seebeck}}}{V_{\mathrm{Ohmic}}} \tag{6.6}$$

But equation (6.6) is valid for a single thermoelectric leg. When more legs are incorporated into a conventional generator, the heat fluxes from each leg can be superimposed leading to a device figure of merit

$$ZT = \frac{\alpha_{\mathrm{TEG}} \Delta T_{\mathrm{p}}}{I_{\mathrm{dc}} R_{\mathrm{TEG}}} = \frac{V_{\mathrm{Seebeck}}}{V_{\mathrm{Ohmic}}} \tag{6.7}$$

where α_{TEG} is the effective Seebeck coefficient of the TEG and can be approximated as

the sum of the Seebeck coefficients of the unipolar materials

The key to Harman setup is to determine V_{Ohmic} and V_{Seebeck}. This in principle is easy, but technologically can be challenging. In Figure 6.5 the transient voltage response of a commercial TEG shows the quantities of interest. A time domain technique like the one shown would resolve the quantities immediately however, sampling speed becomes a problem is very high precision is desired because precision is greatly sacrificed for high sampling rates [107].

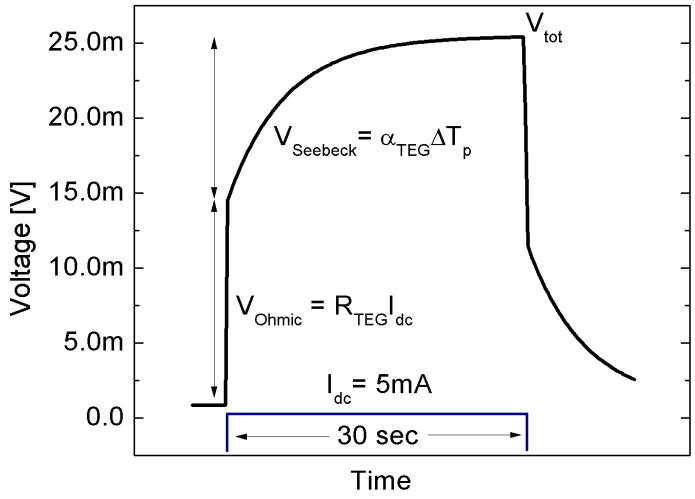

Figure 6.5: Transient voltage response of a TEG. A DC current pulse is applied for 30 seconds.

For this reason we implemented a four-wire AC/DC Harman technique in which the steady state voltage V_{tot} is measured in the time domain, I_{dc} is known and R_{TEG} is carefully measured using an AC signal at 10 kHz. When and AC signal with high enough frequency is applied to the TEG, Peltier effects do not have enough time to develop a temperature gradient and so only the Ohmic voltage V_{Ohmic} is observed. With V_{Ohmic} and V_{tot} known, V_{Seebeck} can be easily calculated and ZT is measured for different temperatures. More

details about the setup can be found in [105].

Harman Technique: Procedure

In Figure 6.6 the systems diagram shows the integration and the models of the instrumentation that was used. The vacuum chamber is first evacuated to an approximate pressure of 10^{-6} mBar. After the evacuation the heating process is be started, the heating rate is 10 °C/min. The power source is modulated by the temperature controller to deliver electrical power to the lamps. After the chamber temperature has been within 0.5 °C of the target setpoint for 30 min , the electrical measurements are allowed to start. A thermocouple $TC1$ inside the vacuum chamber provides temperature reading for the temperature controller, while an internal thermocouple $TC2$; a thermocouple inside the heat shield provides the temperature of the TEG. For the models of the instrumentation used, see Figure 6.6.

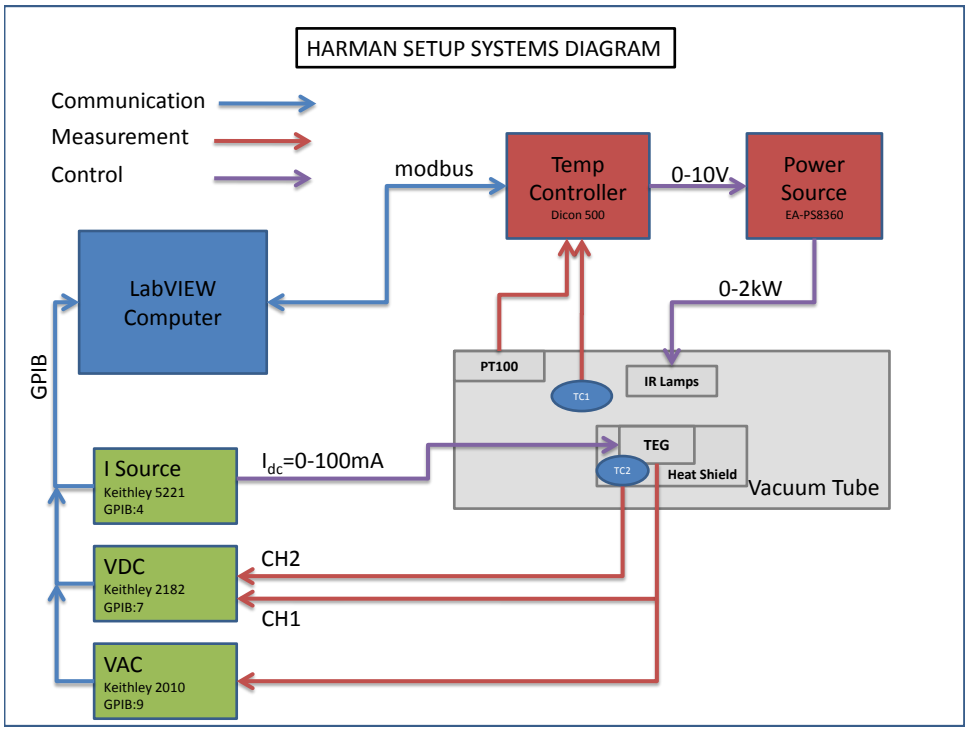

Figure 6.6: System Schematic of the Harman Setup.

The Harman setup was validated by measuring a commercial Bi_2Te_3 based TEG and

comparing the results with a Harman system developed by the Fraunhofer Institute of Physical Measurements in Freiburg, Germany where a similar furnace but a different electrical approach was used. The results show an excellent agreement with a maximum difference in the measured ZT of 4.3% [105]. A. Becker is acknowledged for the early design stages of the setup.

Homogeneous temperature on PN-TEGs

The Harman technique is used exclusively with conventional TEGs. However the same furnace can be used to perform temperature dependent measurements on the PN-TEGs by replacing sample holder used in the Harman technique (Figure 6.4b) with the sample holder that was described in Figure 6.9.

6.3.2 The Monkey Setup

It has been noted by some authors that while the thermoelectric figure of merit is a valuable quantity (typically measured with small ΔTs), in order to properly characterize a thermoelectric material, or a device, a large temperature gradient should be used because these are the desired operation conditions [59, 60, 61, 108, 109]. For this reason the Monkey setup simulates real operating conditions with ΔTs in the order of hundreds of °C.

This section describes the hardware integration of the setup and the following sections deal with the data analysis. In this setup the PN-TEGs are mounted in a water cooled heat sink as depicted in Figure 6.7. Here is important to note that the electrical contacts are made exclusively at the cold side. At the opposite end of the PN-TEG a silicon nitride resistor is pressed against the PN-TEG as a heat source. The hot and cold side temperatures are measured by two c-type thermocouples positioned as shown in Figure 6.7. The entire system is enclosed in a vacuum chamber that can be evacuated to a pressure of approximately 10^{-1} mBar. Care was taken to keep the power lines away from the measurement lines. Since thermocouples measure a relative change in temperature, the

reference temperature is measured with a thermistor *PT100*.

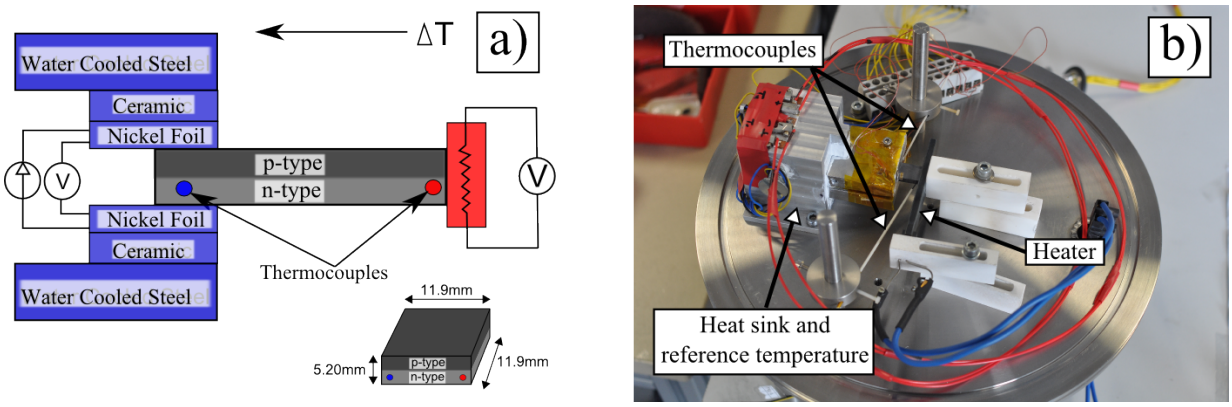

Figure 6.7: a) Schematic of the sample holder. b) Actual setup.

Although the heater can reach temperatures over 1000°C, the experiments remain under 800°C on the hot side because the heat sink reaches a heat saturation level and the sample holder has to remain below 300°C. Power is delivered to the heater using a EA-PS8360 power source from EA Elektro Automatik with typical power values between $10 - 150\,\mathrm{W}$. After a given power setpoint is established, a stabilization time between $4 - 6\,\mathrm{min}$ allows the system to reach steady state condition after which the electrical measurement (IV scan) is performed. It should be mentioned that neither temperatures (hot side or cold side) are controlled, a steady state power out is sent to the heater and this develops the temperature fields.

The reason for controlling the heating power and not the temperatures is simplicity; at this stage of the research it is more important to build a metrology setup that can test the PN-TEGs in large temperature gradients because this has not been done before than it is to control the hot and cold side temperatures. A reason to have precise control of the temperatures would be have more insight into the Seebeck coefficient, but as it has been noted, the PN-TEG is a device, and the meaning of a Seebeck coefficient in a device in large temperature gradients, losses clarity as discussed in the next sections.

The error in the electrical measurements is discussed in section 6.3.3, while the error in

the temperature measurements corresponds to one standard deviation of 10 consecutive temperature readings. A screenshot of the LabView interface is shown in Figure 6.8. Normally a heating and cooling cycle is done to detect hysteresis in the measurements.

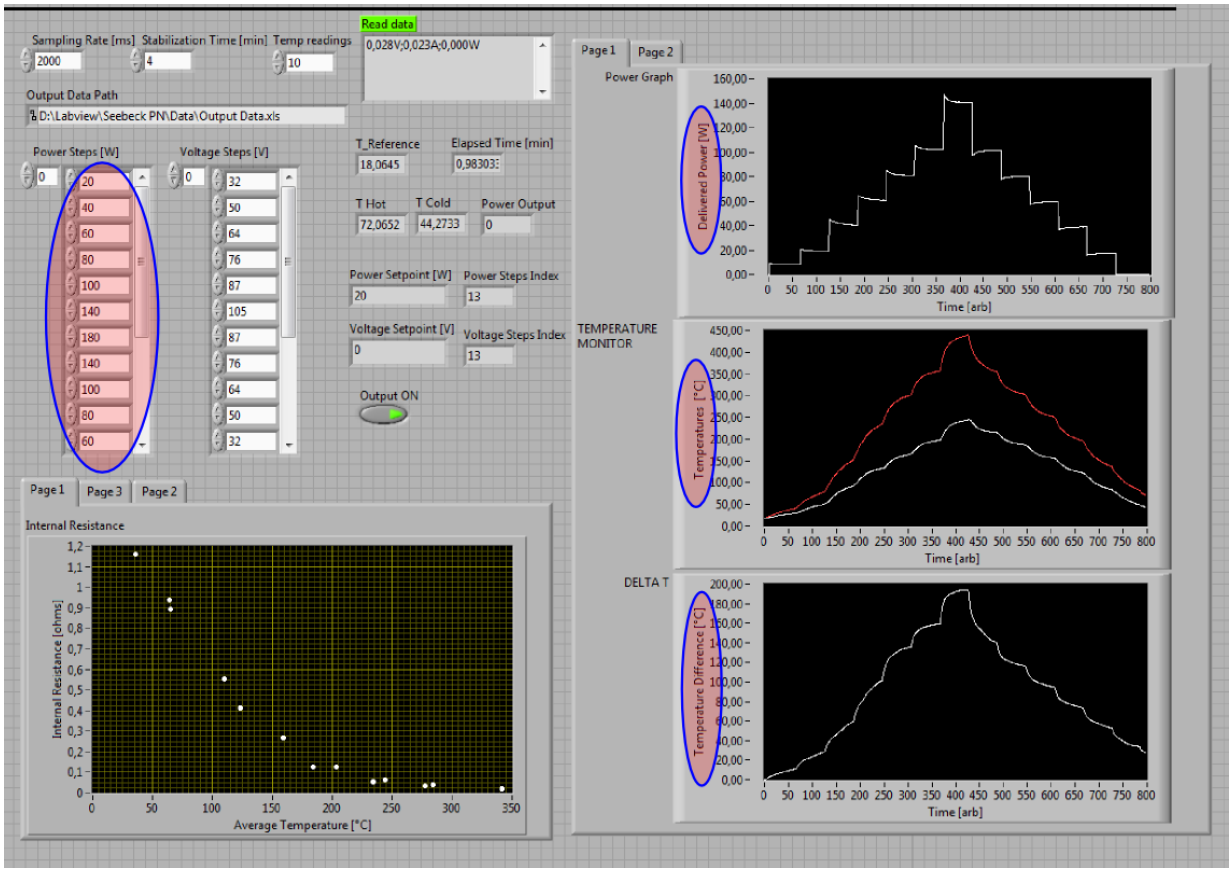

Figure 6.8: Screenshot of the LabVIEW interface. The red circles point to the most important parameters.

6.3.3 Electrical Measurements: Hardware

All the IV scans in this work have been done using a Source Measure Unit (SMU) in a four-wire configuration to eliminate wire resistances. The data presented throughout this work was collected using a Keithley 2616A source meter. Only when explicitly noted the data was collected using a Keithley 4200-SCS semiconductor characterization system. In

both cases the IV scans are automated using a LabView interface.

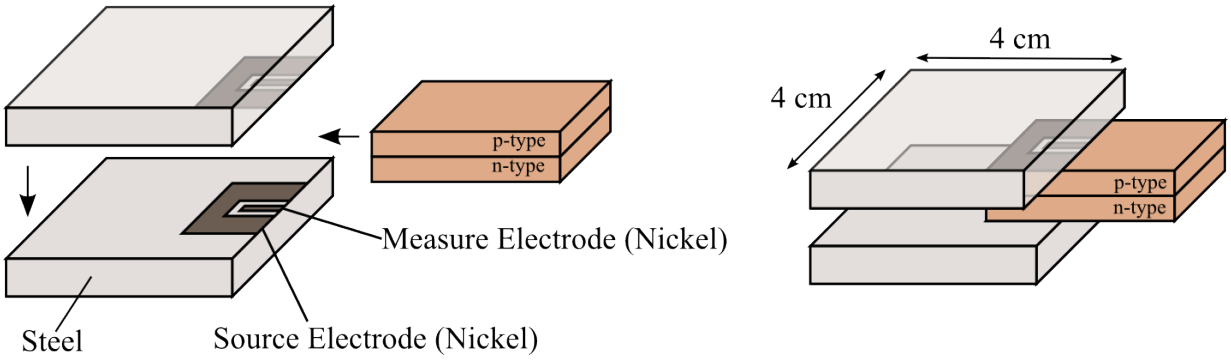

Figure 6.9: Schematic showing how the electrical contacts are done.

To measure the IV curves the samples are mounted in an apparatus depicted in Figure 6.9, which is a subsystem of a bigger setup, but for now the discussion is focused to the electrical measurement only. The electrodes are designed to deliver a 4-wire measurement all the way to the sample eliminating the wire resistance. A big electrode sources the current, while a much smaller electrode senses the voltage on the surface of the sample. Two steel plates or jaws close upon the PN junction holding it in place and making electrical contact, the pressure is adjusted by hand with two screws that hold the jaws together.

Error Analysis and Uncertainty

To alleviate the random error in the measurement of the temperature, 10 consecutive temperature readings are averaged. The standard deviation is typically much smaller than the mean and for this reason error bars are not plotted in the graphs. Of course there are systematic errors that arise from the position of the thermocouples. For example the hot side temperature is underestimated because the hot side thermocouple is located as close as possible to the heat source, without risking that the thermocouple could accidentally get in touch with the heat source. Another source of error here comes from the the spatial position of the thermocouples, at this is is done manually.

The electrical measurement is believed to me more robust because the parameters are

extracted from a linear fit of the IV scan on a four wire configuration. A least square method is used to perform a best linear fit to the current I in Labview by minimizing the residue ϵ according to the following equation:

$$\epsilon = \frac{1}{N}\sum_{i=1}^{N}(I_{\mathrm{fit},i} - I_{\mathrm{meas},i})^2 \tag{6.8}$$

where N is the number of IV elements, $I_{\mathrm{fit},i}$ the i^{th} element of the best linear fit and $I_{\mathrm{meas},i}$ is the measured value of the i^{th} element.

From the linear fit a slope $G_{\mathrm{int}} = R_{\mathrm{int}}^{-1}$ is obtained as well as the short circuit current I_{sc} and the open circuit voltage V_{oc}. Since the residue ϵ is the weighted uncertainty of the fit, it can be used to visualize the extrema points of the fit and minimum and maximum slopes as sketched in Figure 6.10.

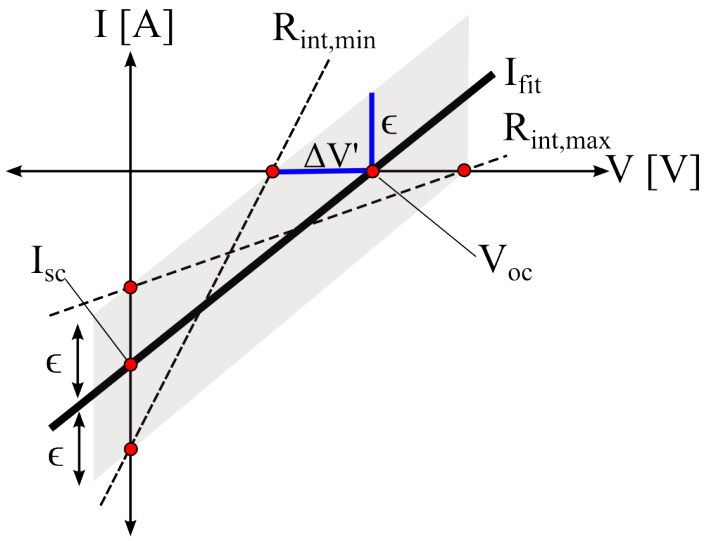

Figure 6.10: Sketch showing the important parameters in the error analysis. The shaded area represents the uncertainty in the measurement.

From the minimum and maximum slopes, the error in the resistance measurement is then defined as an average of the difference between the fit and the minimum and maximum

values

$$R_{\text{int,error}} = \frac{|R_{\text{int}} - R_{\text{int,min}}| + |R_{\text{int}} - R_{\text{int,max}}|}{2} \tag{6.9}$$

The minimum and maximum resistance values are obtained by visual inspection of the IV plot as shown in Figure 6.10;

$$R_{\text{int,min}} = \frac{V_{\text{oc}} - \Delta V'}{|I_{\text{sc}} - \epsilon|} \tag{6.10}$$

and

$$R_{\text{int,max}} = \frac{V_{\text{oc}} + \Delta V'}{|I_{\text{sc}} + \epsilon|} \tag{6.11}$$

the only term missing in equations (6.10) (6.11) is $\Delta V'$ but this can be extracted from further inspection in Figure 6.10 (see blue lines), combined with the following relation:

$$R_{\text{int}} = \frac{\Delta V'}{\epsilon} \Rightarrow \Delta V' = \epsilon R_{\text{int}} \tag{6.12}$$

Finally combining equations (6.9) to (6.12), the error in the internal resistance measurement $R_{\text{int,error}}$ can be calculated from the parameters that are extracted from the linear fit

$$R_{\text{int,error}} = \frac{1}{2}\left|R_{\text{int}} - \frac{V_{\text{oc}} - \epsilon R_{\text{int}}}{|I_{\text{sc}} - \epsilon|}\right| + \frac{1}{2}\left|R_{\text{int}} - \frac{V_{\text{oc}} + \epsilon R_{\text{int}}}{|I_{\text{sc}} + \epsilon|}\right| \tag{6.13}$$

The calculated error is typically in the order of hundreds of $n\Omega$, and for this reason sometimes it is not useful to plot the error bars since their order of magnitude is much smalled compared to the absolute values. Note that in Figure 6.10 $I_{sc} \leq 0$, that is because in this example the PN junction is subject to a ΔT. In thermal equilibrium $I_{sc} \approx 0$ but this makes no mathematical difference in the derivation.

6.3.4 Electrical Conductivity-Conductance

The total internal resistance of a PN-TEG is measured as explained in section 6.3.3, but in this section more focus is given to the interpretation of these measurements. In order to compare the PN-TEG architecture to other thermoelectric materials, it would be desired to have a value for the electrical conductivity. This would make it possible to compare the PN-TEGs with other materials using the thermoelectric figure of merit.

However, the extraction of a conductivity becomes elusive due to the two dimensional nature of the current density. To clarify this, the concept of electrical resistance is revisited in its vector definition as the ratio of the voltage and the current

$$R = \frac{\int \mathbf{E} \cdot d\mathbf{l}}{\iint \sigma \mathbf{E} \cdot d\mathbf{S}} \tag{6.14}$$

If the electric field is assumed to be constant ($\mathbf{E} = E\mathbf{a}_x$) as sketched in Figure 6.11a, the solution to equation (6.14) provides a relationship between, R, σ and the geometry of the specimen, given that the specimen is rectangular or cylindrical, in the well known equation

$$R = \frac{1}{\sigma}\frac{L}{A} \tag{6.15}$$

It is from equation 6.15 that it is possible to calculate the electrical conductivity from a macroscopic resistance given that the electric field acts homogeneously and the geometry is known. This is the typical measurement of electrical conductivity in bulk thermoelectric materials.

However in the case of a PN-TEG, the electric field is not homogeneous; it changes in magnitude and direction as shown in section 4.2.2 and independently developed in ref. [73]. A sketch in Figure 6.11b shows the current paths within the PN-TEG. In such a device, how could equation (6.14) be applied? if one took equation (6.15) as an approximation,

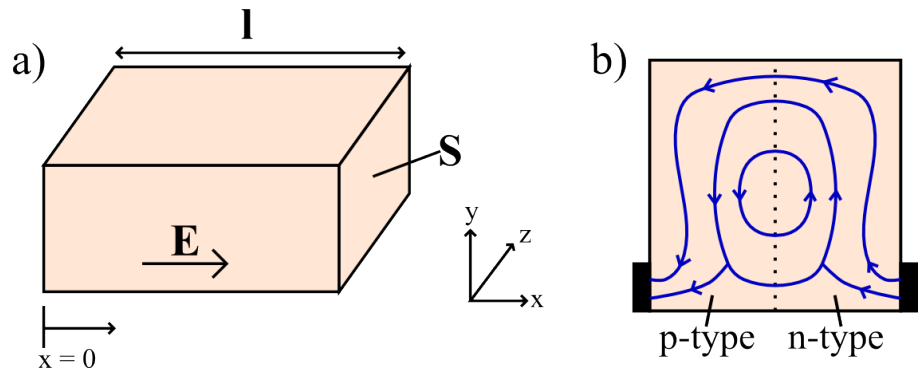

Figure 6.11: a) Geometry of a homogeneous resistor used to solve equation (6.14). b) Inhomogeneous electrical field in a PN-TEG make it difficult to find an analytical value of R.

which values should be taken for L and A? This means that there is no easy analytical solution to equation (6.14), and so extracting the electrical conductivity of a PN-TEG does not seem possible in a traditional way. Numerical simulations would be needed.

The best approach to compare a PN-TEG with another thermoelectric material or device is to look at the resistance values as opposed to the resistivity values. Therefore for a PN-TEG the internal resistance will be a very important parameter. A final comment is that if the heat flux could be accurately measured, a value for the efficiency of the thermal-electric conversion could be calculated and this would be of tremendous value. However, at the moment, the are unresolved challenges to measure the heat influx in a relatively small sample at such high temperatures where radiation transport cannot be neglected.

6.3.5 Device "Seebeck" Coefficient

Theoretical Method

The apparent simple definition of the Seebeck coefficient as the ratio of Seebeck voltage and the temperature difference does not translate to trivial measurements. On the contrary, the apparent simplicity has lead to non ideal practices and has complicated the interlaboratory verification of reported values of zT [110, 111].

Numerous different setups have been developed to measure the Seebeck coefficient throughout the years [112, 113, 114, 115, 116, 117]. For this reason it emphasized that even though in this work a coefficient with the units of V/K is extracted from the measurements, strictly speaking it is not the same as the Seebeck coefficient. Although this coefficient is largely based on the Seebeck coefficient, in the sense that it carries the same information and the measurements of a PN-TEG equivalent Seebeck coefficient are largely based on the measurements of the traditional Seebeck coefficient, and they will be compared with some reservations.

There are two main methods to measure the Seebeck coefficient; the integral (large ΔT) and the differential (small ΔT). The derivation of the Seebeck coefficient for a monopolar material in section 2.3 was done assuming near equilibrium conditions (small ΔT). In this case the Seebeck coefficient can be obtained by the ratio of the Seebeck voltage V_s and the applied temperature difference:

$$\alpha = \frac{V_\mathrm{s}}{\Delta T} \tag{6.16}$$

this is known as the differential method. In this method, the specimen is brought to an average temperature, and a small temperature gradient is produced, typically of a few °C. In this way the Seebeck coefficient is measured for different temperatures.

If large non equilibrium conditions are present (large ΔT) the linearity assumption in equation (6.16) cannot longer be assumed and an integral over the temperature would be required to know V_s

$$V_\mathrm{s}(T_\mathrm{c}, T_\mathrm{h}) = \int_{T_\mathrm{c}}^{T_\mathrm{h}} \alpha(T) dT \tag{6.17}$$

If the derivative with respect to T_h is taken, equation 6.17 can be rewritten as [110]

$$\alpha(T_\mathrm{h}) = \frac{dV_\mathrm{s}(T_\mathrm{c}, T_\mathrm{h})}{dT_\mathrm{h}} \tag{6.18}$$

This is known as the integral method. In this method, the cold side temperature is held constant while the hot side temperature is increased to create large ΔTs. A continuous representation of the data is obtained by a data fit and at the temperature of interest, the derivative of the function yields the Seebeck coefficient. A graphical representation of both methods is shown in Figure 6.12. Each method has its advantages and disadvantages and

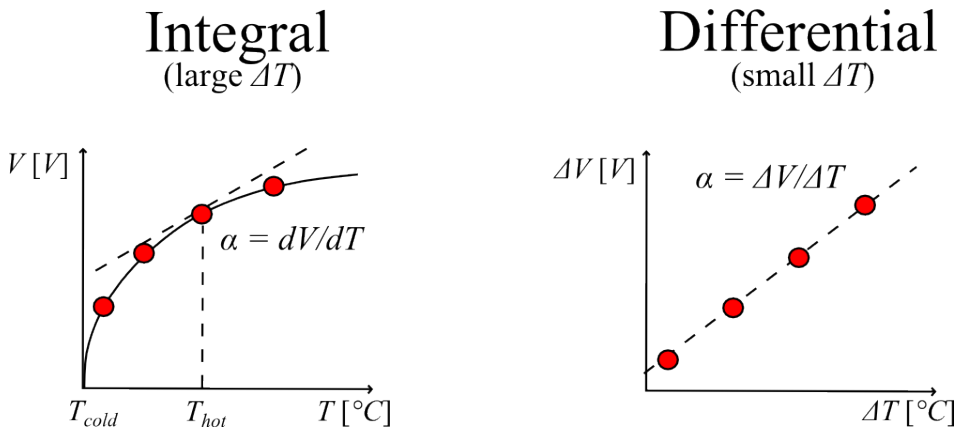

Figure 6.12: Illustrations of the integral and differential methods. Adapted from [110].

in general, the differential method is more widely used because of the technical ease of a small ΔT. However, our setup as already mentioned, applies a large temperature gradient but the temperature cold side temperature is not fixed; therefore it is not possible to apply the integral method in its strict definition.

To measure the device Seebeck coefficient equivalent, a mixture of the two methods is used; a large temperature difference will be applied as in the integral method. Yet, the open circuit voltage V_{oc} is divided by ΔT as done in the differential method and the PN-TEG equivalent Seebeck coefficient is then

$$\alpha_{\mathrm{eff}}(T_{\mathrm{h}}, T_{\mathrm{c}}) = \frac{V_{\mathrm{oc}}(T_{\mathrm{c}}, T_{\mathrm{h}})}{\Delta T} \tag{6.19}$$

Here is important to recall that α_{eff} is not a material property, but a device property. And it combines contribution of the p-type material α_p, the contributions of the n-type

material α_p, and the internal losses due to the current vortices. For this reason, it is expected that $\alpha_{\text{eff}} \leq \alpha_p + \alpha_n$ for a given temperature. It is understood that measuring α_{eff} in large temperature gradients introduces some questions since ΔT is in the same order of magnitude as T_{avg}, the latter becomes largely a function of the end temperatures. Another aspect is that large ΔTs might produce gradients in carrier concentrations that can contribute to V_{oc} [118].

Practical Method

A top view schematic is shown in Figure 6.13. Care was taken to keep the power lines away from the signal lines. The thermocouples are C-type and note that there is a small gap between the thermocouple and the hottest and coldest points. This is a source of error because ΔT is underestimated. The thermocouples are positioned by hand and this is a source of systematic error however the random error from the temperature reading is mitigated by taking 10 temperature readings every time.

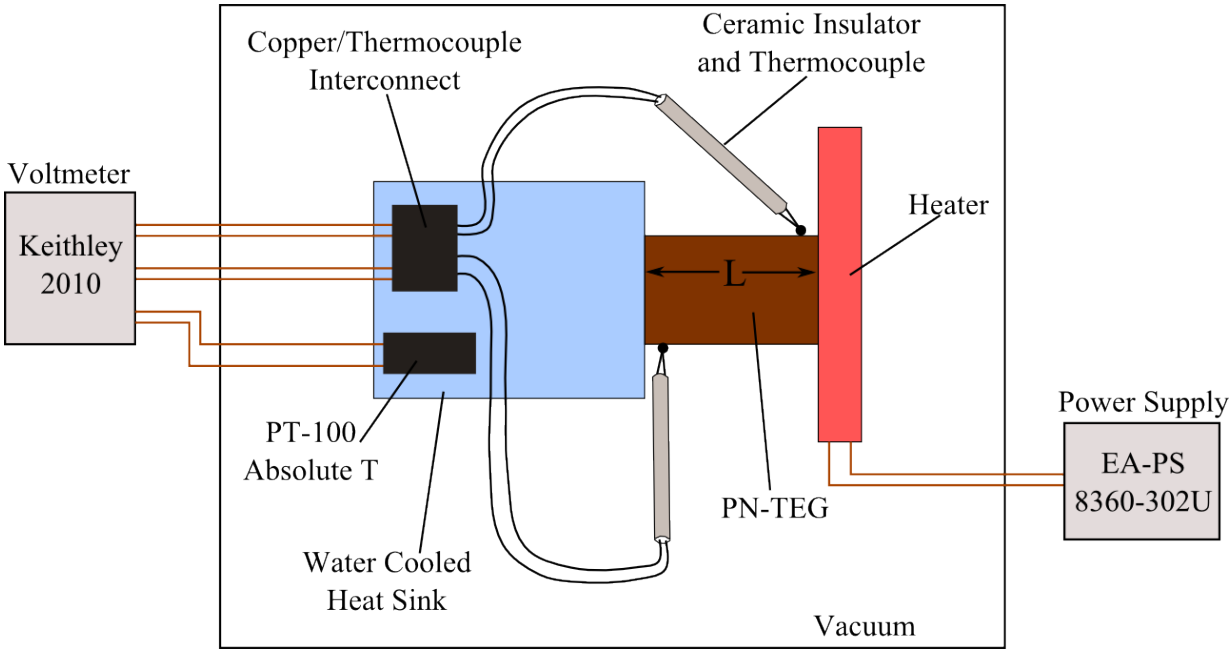

Figure 6.13: Top view schematic of the monkey setup. Thermocouple wires are black, while copper wires are redish-orange.

Figure 6.14a shows the standard deviation of the 10 temperature measurements divided by the actual temperature measurement for the cold side and hot side thermocouples thus showing effective in reducing the random error. Systematic sources of error in the measurement of the temperature comes from the positioning of the thermocouples, since this is done by hand.

So far the discussion has ignored any thermoelectric contributions coming from the copper wires at the interconnect. Temperature logs indicate that the temperature difference between the cooling block and the ambient is less than 4°C. That means that the copper wires will give rise to a maximum thermoelectric voltage of 7.36 μV using $\alpha_{\mathrm{cu}}(T = 27°\mathrm{C}) = 1.84\,\mu\mathrm{V/K}$ which translates to a temperature error of less than 0.5 °C[1]. For this reason it seems reasonable to neglect the thermoelectric effect from the copper wires.

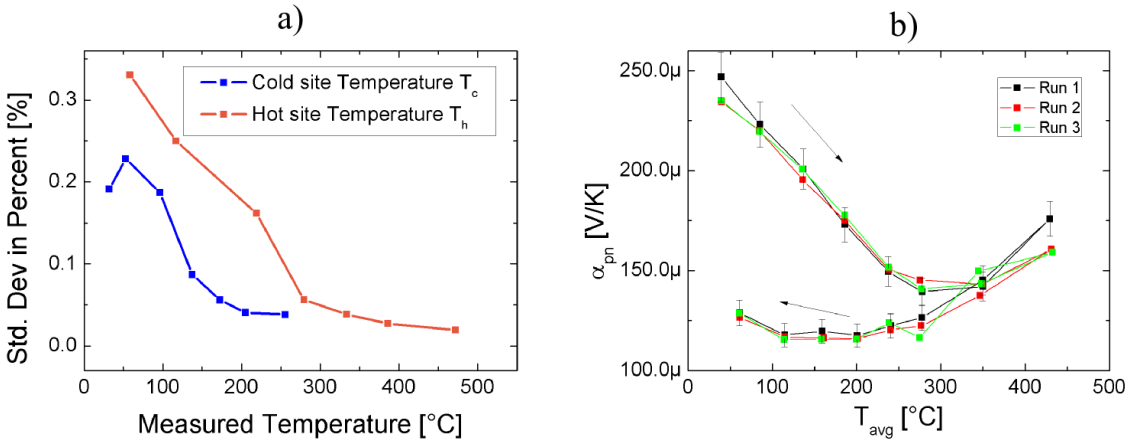

Figure 6.14: a) Standard deviation of the temperature measurements divided by the average temperature. b) Repeated measurements with 5% error bars to guide the eye.

While the random error in the temperature measurements can be significantly mitigated, more subject to uncertainty is the measurement of the Seebeck voltage. Figure 6.14b shows three sequential measurements with 5% error bars for reference, in this experiment the sample was not removed from the holder. This provides an idea of the random error in the

[1] $\Delta V = 13\,\mu\mathrm{V} \Rightarrow \Delta T = 1\,°\mathrm{C}$ for the C-type thermocouple.

Seebeck voltage. Systematic errors in the Seebeck voltage come from the manual mounting of the PN-TEG such as the electrical and thermal contact pressure.

6.3.6 Power Output

The power output is perhaps the most important quantity extracted from a PN-TEG. It is calculated from R_{int} and α_{eff} that is the motivation to carefully measure and remain conscious of the uncertainty sources of the two quantities. Similar to what is done in photovoltaics, the power output is obtained from the IV scan in the fourth quadrant. Here we take advantage of the the linear IV relation in this domain. It is true that the PN-TEG exhibits a non-linear IV characteristic, but V_{oc} is small enough that the IV characteristic appears linear.

Given that there is a linear IV characteristic the current can be described as

$$I = I_{\text{sc}} + G_{\text{int}} V \tag{6.20}$$

Equation (6.20) can be multiplied by V to turn it into a power, and differentiated to find the maximum power output. This occurs at halfway from V_{oc} and I_{sc} and defines the maximum power output that will be broadly used throughout this work:

$$P_{\text{max}} = \left| \frac{1}{2} V_{oc} \frac{1}{2} I_{sc} \right| \tag{6.21}$$

This is illustrated in Figure 6.15a. If the PN-TEG is low performing, the complete IV curve can be obtained. That means that V_{oc} and I_{sc} can be explicitly measured. However, when the PN-TEG is a high performance one, only V_{oc} can be measured and I_{sc} has to be extrapolated because the SMU is not able to sink more than 1A (which is a large current for a high precision SMU). This shown in Figure 6.15b, the solid lines represent the

measurement and the dashed lines represent the extrapolation. Note the different scales in current between figure a and b. An algorithm scans the appropriate voltage domain protecting the sinking current in the SMU from reaching a saturation level. A value of $P_{\max}$ is extracted for every ΔT.

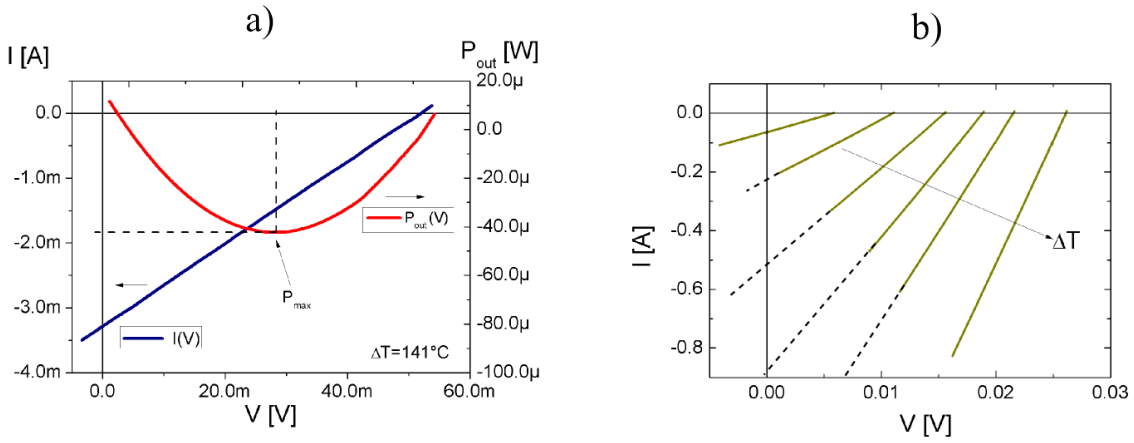

Figure 6.15: a) Graphical representation of equations (6.21) and (6.21) for $\Delta T = 141\,^{\circ}\mathrm{C}$. b) When a high performance PN-TEG is measured an extrapolation is necessary because of the high output currents.

7 Results and Discussion

> Man is born free and everywhere he is in chains.
>
> Jean-Jacques Rousseau

7.1 Structural Characteristics

In the following subsections we seek to shed light to the structural composition of the PN junction itself. A profound study can be made on the structural analysis of the samples, but since the focus of this topic is at the device layer, the structural characteristics are limited to two main methods; SEM microscopy and an optical beam induced voltage measurements.

7.1.1 Current Assisted Sintering PN-TEGs

The first insight to the structure that was formed during the current assisted sintering process can be obtained by means of a local measurement of the Seebeck coefficient [119]. Previous investigations on current assisted sintering PN junctions using a Seebeck micro-probe that measures the local Seebeck coefficient have shown that after the densification process, a p-type doped domain and a n-type domain are present [89, 91]. Moreover it is suggested in ref. [91] that the PN interface has a linearly graded transition from p-type to n-type. This is in line when one considers that during the sintering process, semi

molten materials partially diffuse. Understanding that the preparation process is not well controlled, a rather inhomogeneous and poorly defined PN junction would be expected.

This is confirmed by SEM images and OBIV measurements. A small piece of a PN-TEG was etched to remove surface oxidation prior to imaging in the SEM. In Figure 7.1a a cross sectional image of a PN interface is shown. The boron doped domain can be identified in the top half because of the more granular nature of the nanostructured. The phosphorous doped domain is on the bottom. A transition from dopant type can be seen although not abrupt, this is labeled as "junction" and can be seen in the middle, and from this SEM image it is possible to envision that the dopants are not contained in a step function distribution. Figure 7.1b show a higher resolution SEM image where again the junction appears to be gradual and it also can be seen in the bottom half the nanocrystalline structure that reduces the lattice thermal conductivity.

An OBIV measurement done on a different fragment of a sample shows a very inhomogeneous voltage output in Figure 7.1c. The first question that arises from this measurement is whether the voltage is photo-induced or thermally-induced. A photo-induced voltage would mean that electron-holes were created and separated. A thermally-induced voltage would mean that the light beam was absorbed in the form of electron-hole pairs, but non-radiative recombination leads to a local heating and heating of the junction creates the effect of a thermocouple.

There are a couple of arguments to claim that the observed voltage is optically induced. Along the interface we interpret the high peaks in the voltages in Figure 7.1c as local domains where diode structures have been formed and electron-hole pairs can be generated and separated by the photovoltaic effect. In those regions with low voltage readings, poor diode structures have been formed that effectively act like shunt resistances and space charge limited current elements as discussed earlier.

It is possible to make the hypothesis that if the observed effect is thermally induced, the

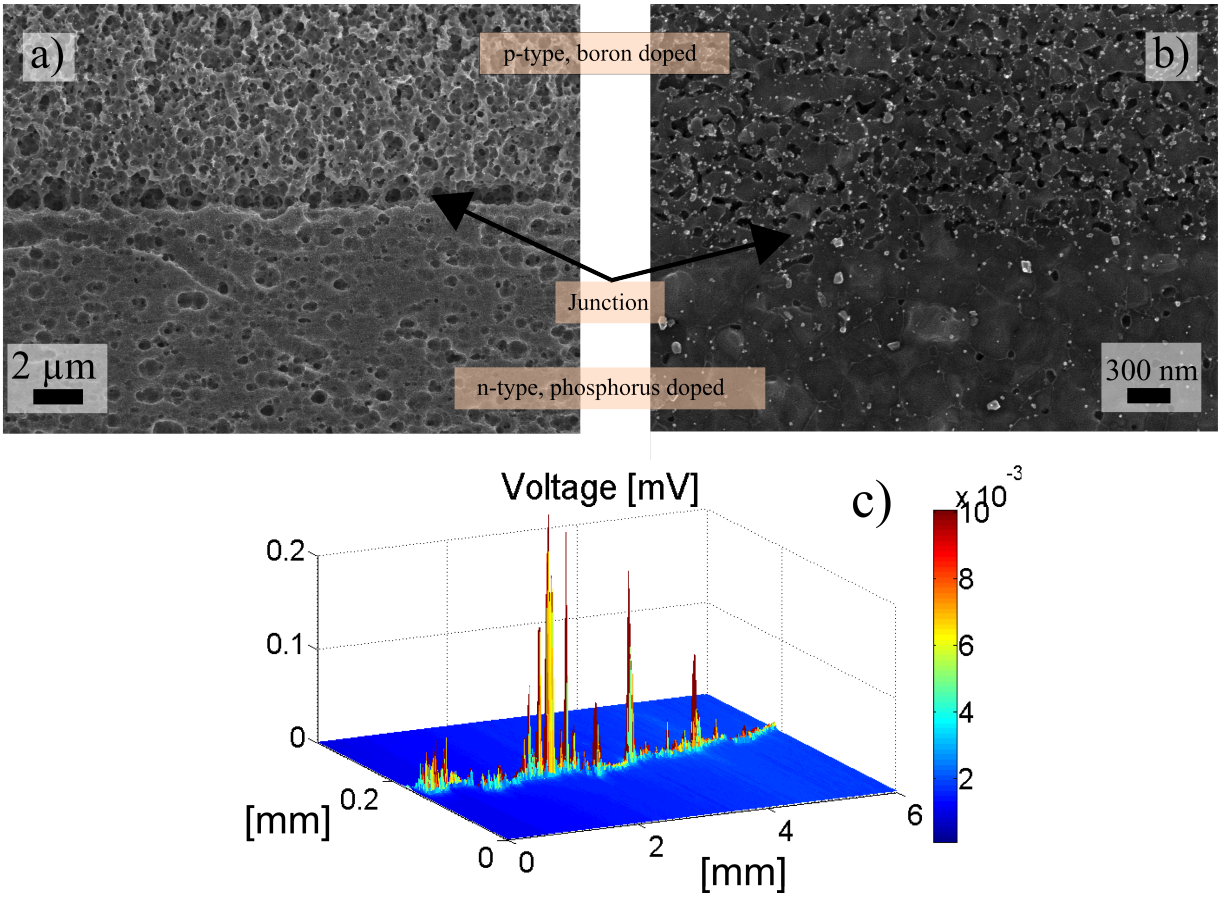

Figure 7.1: a-b) SEM images of a nanostructured PN junction. c) OBIV measurement on a nanostructured PN junction.

voltage peaks would be expected to have the same height due to the diffusive nature of heat, and a larger voltage would be induced in the rest of of the body where no significant voltage is measured in our samples.

To test this hypothesis the sample measured in 7.1c, is covered with a 500 μm thick glass substrate which is covered on one side with an optical absorbing graphite layer and makes a thermal contact to the sample through a thin layer of thermal paste as shown in Figure 7.2. The measurement shows a more homogeneous voltage peak and a longer spatial extension of the peaks. It is important that this is not a conclusive experiment because the tails of the peak can be extended by thermal diffusion in the glass and thermal paste.

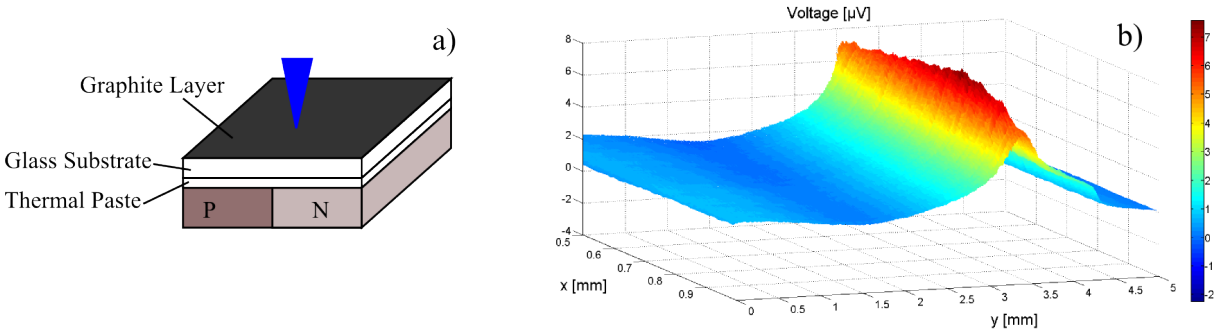

Figure 7.2: a) Schematic of the experiment; an optical absorption layer is introduced to rule out optical effects. b) OBIV measurement showing the influence of purely thermal effects (measurement acknowledged to L. Bitzer)

The structural analysis of a PN-TEG prepared by the current assisted sintering method shows that a poorly defined PN interface develop. Evidence for carrier compensation strengthens the theory of non linear shunt resistances and shows that a very ideal diode should not be expected from this preparation technique. It will be shown later in the chapter that this is actually a desired condition, to have a highly non ideal diode as a PN-TEG.

7.1.2 Laser Annealing PN-TEGs

Since the current assisted sintering process produces linearly graded, not so well defined PN junctions, it is desired to produce better defined samples that facilitate the physical understanding at the price of a reduced thermoelectric performance. A comprehensive analysis of the structural and electrical properties of the laser annealed layers is given in ref. [120] where they show that using highly doped nanoparticles and high enough pulse energy density, conductivity levels in the order $1 - 0.1\,\Omega^{-1}\mathrm{cm}^{-1}$ can be achieved which translates to effective doping levels of the annealed layers of $10^{15} - 10^{17}\,\mathrm{cm}^{-3}$. Further studies show that the doping level varies with depth, and reaches hundreds of nanometers [92, 93]. It has been shown that diode structures can be formed by complementary doping of a Si crystalline wafer and Si nanoparticles. Meseth et al. showed that p-type and n-type Si nanoparticles deposited on complementary doping wafers form nearly identical diodes electronically speaking [92].

The PN structures follow the preparation and recipes used by previous authors so it assumed that the structural properties do not vary considerably. From this knowledge we expect the doped layers of the PIN structures to be also in the order of hundreds of nanometers, and thicker because the Si wafer is undoped. A cross-sectional OBIV measurement like the one done on the current assisted sintering samples becomes more difficult due to the thin film nature of the PN and PIN junctions. However top view OBIV measurements have been performed on laser annealed PN structures and they show a homogeneous spatial response [92]. SEM images in Figure 7.3a,b show that a granular layer forms after the laser annealing step, in line with previous results [92, 93].

The take away from the structural analysis of the laser sintered diodes is that the provide means for a better defined diode that is easier to model. However this has two drawbacks that limit the thermoelectric performance: One is that the lateral conductive layers, are very thin and not homogeneously doped which has the effect that the internal resistance

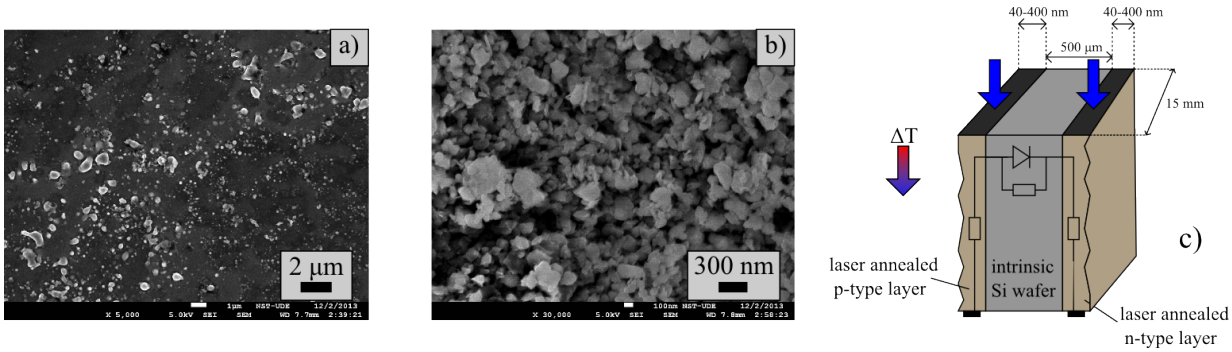

Figure 7.3: a-b) SEM Images of a p-type layer after annealing. The porosity matches to what has been previously observed [92, 93]. c) Structure schematic of a PIN sample showing with the blue arrows the high resistance seen in the lateral layers.

seen by the PN-TEG increases considerably when one considers the PN-TEG as a voltage driven device as shown schematically in Figure 7.3c. The second drawback is that since the PN interface is better defined, a higher shunt resistance will be be formed and this reduces further the thermoelectric performance.

7.1.3 Wafer Welding PN-TEGs

The wafer welding PN-TEGs are prepared with an in-house setup built for this purpose. During the welding process a strong localization of the current is observed in the form of hot spots that glow red as shown in Figure 7.4b. This indicates that a strongly concealed current path develops, and from this idea the bonding or the PN interface formation is expected to be inhomogeneously formed since the bonding is expected to occur mainly due to Joule heating. Part of the reason for the strong localization of the current is that the electrodes do not make a flat contact with the wafers as shown in Figure 7.4a. Hence it is expected that a mechanical bond forms in some areas where in others no mechanical or electrical bond be formed at all, and this is supported from OBIV measurements.

The SEM images were taken on sample no. 10 on a section where a strong bond had

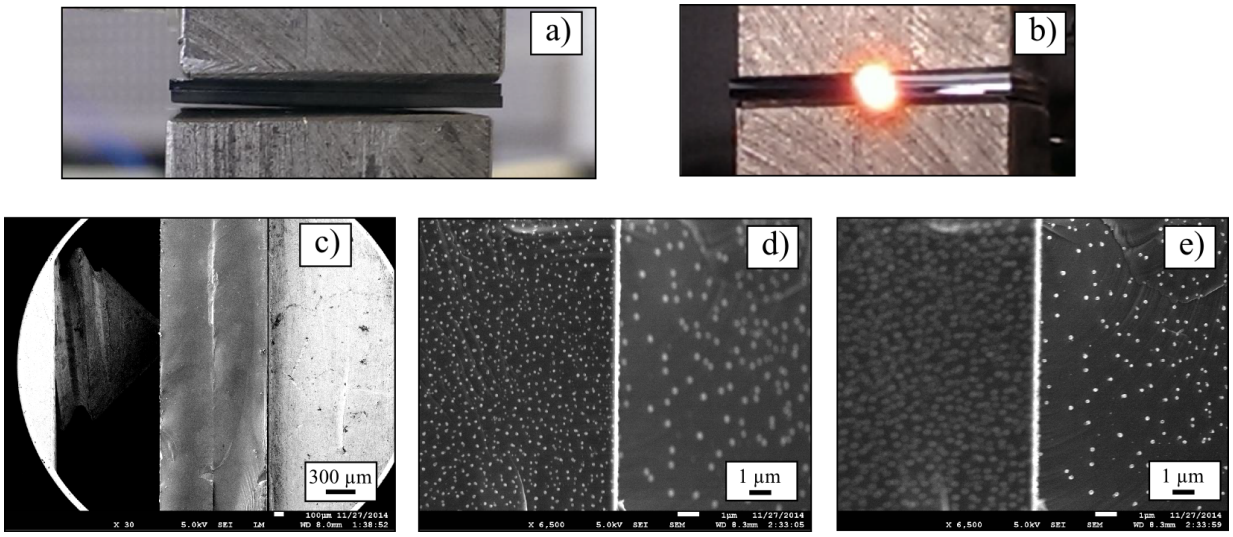

Figure 7.4: a) Fotograph showing the curved contact between the electrodes and the wafers. b) Fotograph showing a hot spot during the welding process. c) Cross-sectional SEM image of PN junction, the n-type wafer is on the left and the p-type on the right on all SEM images. d) High magnification of the PN junction focused on the n-type wafer and e) on the p-type wafer. The bright line in the middle in d) and e) indicates the presence of a non conducting layer.

been formed. In Figure 7.4c the two wafers can be seen held by a screw on the left and the sample holder on the right. The n-type wafer is on the left and the p-type wafer is on the right. Figure 7.4d shows a higher magnification image focused on the n-type and Figure 7.4e is focused on the p-type wafer. The bubbles seen in d) and e) are believed to be oxides formed during the welding process, since the welding process is done in ambient conditions. The side that was imaged was exposed to air during the welding process.

In Figures d) and e) the non-conductive layer in the middle is attributed to the formation of a space charge region. From the SEM images the width of the non-conductive layer is $\approx 300\,\text{nm}$ however, using equation (7.1)[1] the nominal width of the depletion region $W_0 = 1.26\,\mu\text{m}$. It is not clear why the actual depletion region is smaller than expected but if the junction is not crystalline and defects are formed during the welding process, this

[1] $\epsilon_{si} = 11.9$

would limit the diffusion of carriers leading to a smaller depletion region.

$$W_0 = \left[\frac{2\epsilon_0 \epsilon_{si} \left(N_A + N_D \right) V_0}{q N_A N_D} \right]^{1/2} \tag{7.1}$$

For this type of PN junctions OBIV measurements prove to be very useful[2]. In Figure 7.5 OBIV measurements are presented for 4 different samples together with the voltage and current readings from the welding process (recalling that the welding process is modulated by the current which increases from 0 to 20 A). It can be seen that for the last 3 of the 4 samples a very strong localization of the bonding can be observed. The strong localization of the bonding is believed to be due to a percolation of the current path during the bonding process. From the welding protocol it becomes evident that samples with highly localized bonding experienced a voltage spike during the initial stage of the bonding process. During this voltage spike it is believed that a current path forms and is enhanced with increasing current. On the other hand, sample 2 in Figure 7.5 shows a more homogeneous bonding, and no voltage spike.

7.1.4 Summary of Structural Characteristics

The structural analysis shows that each method of fabrication produces different characteristics on the PN junctions. The current assisted sintered samples have thick lateral conducive layers in the order of mm and show a nano-crystalline structure with a gradual transition from p-type to n-type with few spatial domains where space charge regions have been formed. The laser annealed samples have a significantly thin lateral layers of a few hundred of nm. The advantage of the laser annealed samples is that the PN junction is more homogeneous. The wafer welding PN junctions alleviate the problem of having thin lateral layers by using two complementary doped wafers but the PN junctions are shown

[2]Measurements acknowledged to L. Bitzer

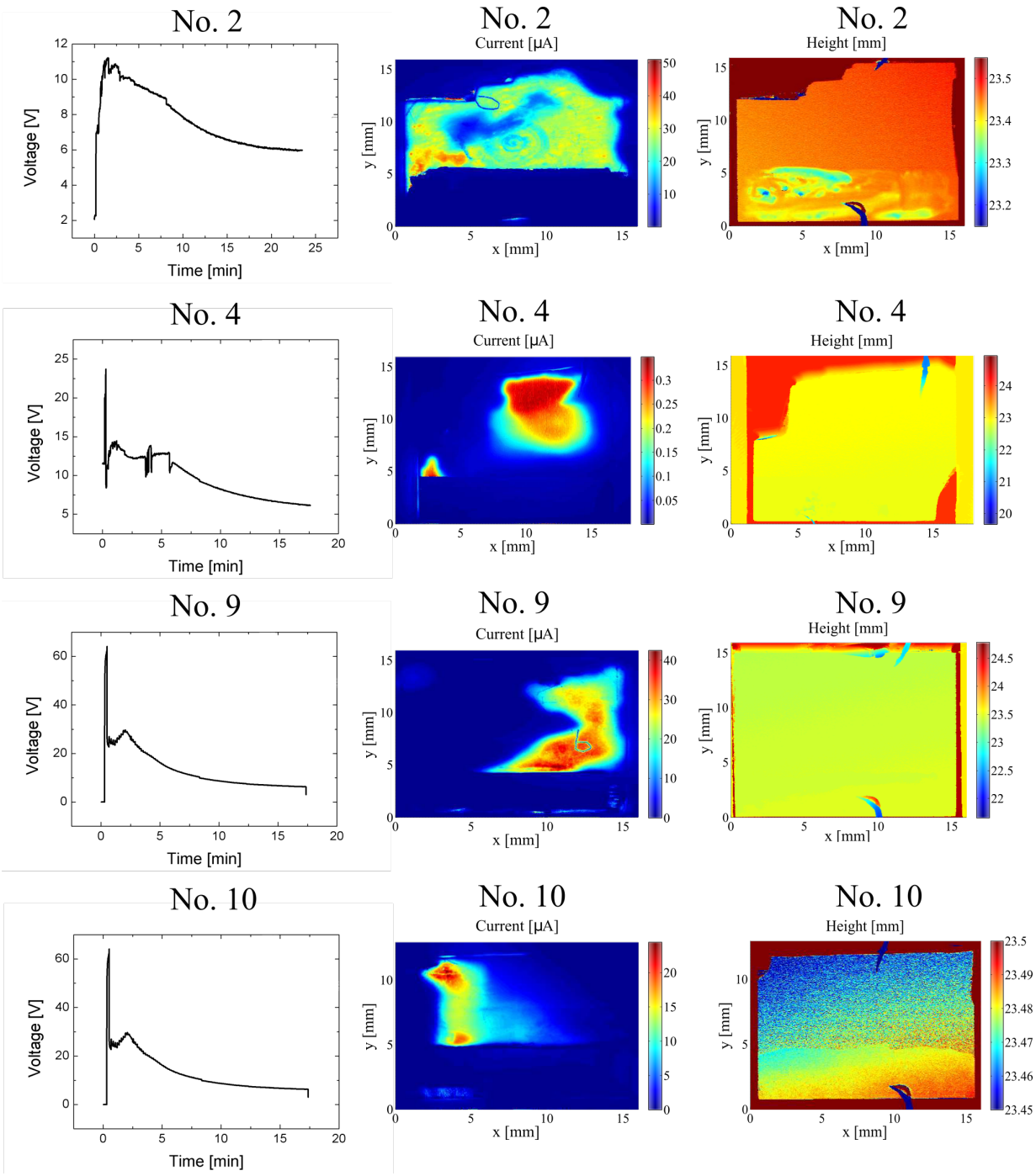

Figure 7.5: From left to right: Welding voltage readings vs time, OBIV measurement, topography of the sample. The localized active region in samples 4,9, and 10 is linked to the voltage spike in the early stage of the welding process.

to be highly inhomogeneous. A summary is presented in Table 7.1.

Table 7.1: Summary of the structural characteristics of the PN-TEGs.

	Current Assisted Sintering	**Laser Annealed**	**Wafer Welding**
Microstructure	Nano-crystalline	Crystalline	Crystalline
PN Junction	Homogeneously poorly defined	Homogeneously highly defined	Homogeneous in localized domains
Nominal Doping	$3 - 10 \times 10^{20}\,\mathrm{cm}^{-3}$	$5 \times 10^{20}\,\mathrm{cm}^{-3}$	$10 \times 10^{15}\,\mathrm{cm}^{-3}$
Layer Thickness	$2 - 5\,\mathrm{mm}$	$200 - 1000\,\mathrm{nm}$	$500\,\mu\mathrm{m}$
Electrical Contacts	Electroless Nickel	None	CVD Aluminum

7.2 Electrical Characteristics

7.2.1 Commercial Diode as Reference

The bandgap of a commercial silicon diode model *1n4004* is measured for reference using the Harman setup (section 6.3.1). This measurement serves as a guide to interpret the measurements of the PN-TEGs fabricated in this work because the bandgap of the commercial diode can be assumed to be 1.1 eV whereas in the fabricated PN-TEGs the effective bandgap is not known. This assumption shows that at high temperatures, the slope of I_0 in an Arrhenius plot follows E_g which means that the current is dominated by n_i^2 since $n_\mathrm{i}^2 \propto \exp\left(\frac{-E_g}{k_B T}\right)$ and in the lower temperatures the reverse current is dominated by a mixture of n_i and n_i^2 as show in Figure 7.6. This is similar to what has been found in Ge diodes [121]. With this reference measurement we learn that with no knowledge of the bandgap, it is possible to calculate it within a factor of 2 from the actual value from the following equation

$$R_\mathrm{int}(T_\mathrm{avg}) \propto \exp\left(\frac{E_\mathrm{g}}{\xi k_\mathrm{B} T_h}\right) \tag{7.2}$$

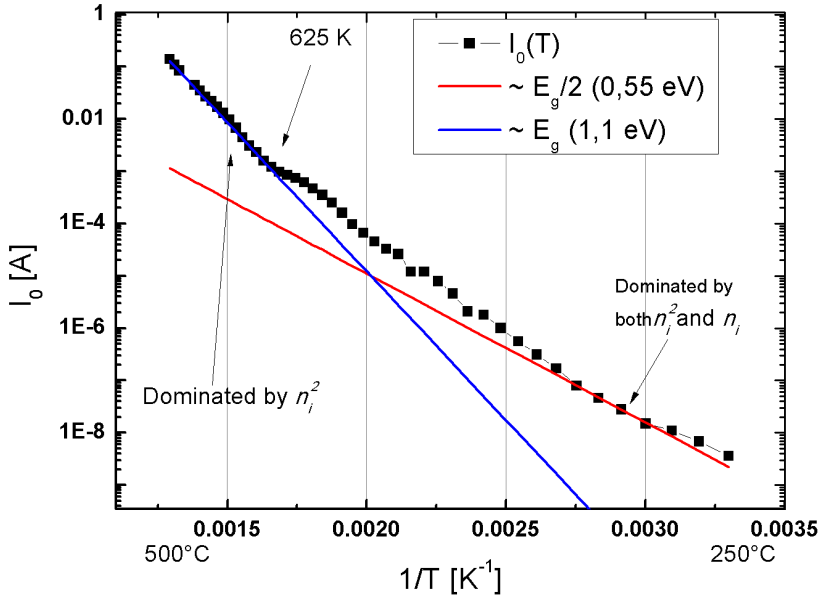

Figure 7.6: Reverse bias current I_0 of the commercial silicon diode plotted against $1/T$ with $\Delta T = 0$.

7.2.2 Electrical Properties: Current Assisted Sintering PN-TEGs

General Electrical Transport

A sample IV scan from a nanostructured PN-TEG is shown in Figure 7.7, as it turns out, the amount of information that can be learned about the sample is more than what it would appear. At first glance, there appears to be no diode element in this sample because of the apparent current symmetry of the IV scan. However after closer inspection, it turns out that a forward voltage of $1.5V$ produces a current slightly larger than a reverse voltage of the same magnitude. This means that however small, a rectifying effect is present, meaning that a very poor diode was formed. The fact that a very poor diode was formed, will be a key to the outstanding performance of the nanostructured PN-TEGs.

The process for the extraction of the mentioned parameters is rather standard, however

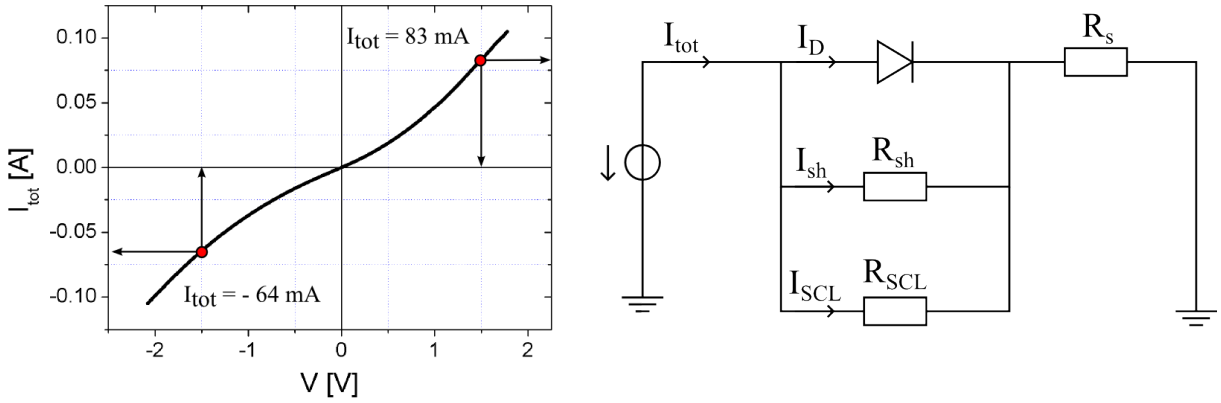

Figure 7.7: Left: IV scan of a nanostructured PN-TEG. Right: equivalent circuit of the PN-TEG in thermal equilibrium

since it will be argued that there is a non-linear component in the PN-TEGs due to a space charge limited current, the process will be described with some detail. It is worth to mention that this process is not done for every sample, the main reason of extracting every equivalent resistance is to show that the TEGs can be understood as having a SCL current element, and this can be linked to the preparation and structure of the nanostructured PN-TEGs.

For the following discussion, refer to Figure 7.8. In the nanostructured PN-TEGs, it is assumed that in the low bias region ($-150\,\mathrm{mV} < V < 150\,\mathrm{mV}$), the diode does not conduct and that R_{sh} is much smaller than R_{SCL}, then from the slope within this voltage domain, one obtains

$$R_{\mathrm{sh}} + R_{\mathrm{s}} = \left(\frac{dI_{\mathrm{tot}}}{dV}\right)^{-1}, -150\,\mathrm{mV} < V < 150\,\mathrm{mV} \tag{7.3}$$

The series resistance R_{s} is extracted from the high bias domain were the diode is assumed to be in flatband condition or shortcut

$$R_{\mathrm{s}} = \left(\frac{dI_{\mathrm{tot}}}{dV}\right)^{-1}, 1.4\,\mathrm{V} < V < 1.7\,\mathrm{V} \tag{7.4}$$

This produces the values for the two linear resistances R_{sh} and R_{s} and the current flowing through the shunt resistor I_{sh} can be calculated as

$$I_{\mathrm{sh}} = \frac{V - I_{\mathrm{tot}} R_{\mathrm{s}}}{R_{\mathrm{sh}}} \tag{7.5}$$

Since I_{sh} is known, it can be subtracted from the IV scan and R_{sh} can be eliminated from the equivalent circuit in Figure 7.8. This will help in explaining the argumentation for the I_{SCL} term.

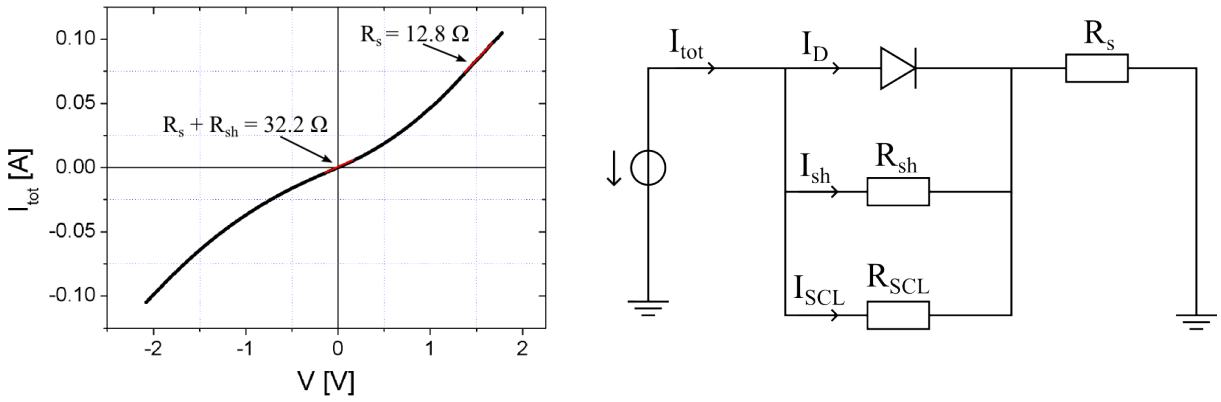

Figure 7.8: Left: IV scan of a nanostructured PN-TEG showing the domains used for fitting. Right: equivalent circuit of the PN-TEG in thermal equilibrium

In the new equivalent circuit, shown in Figure 7.9, I_{sh} is subtracted from I_{tot} and R_{sh} is removed from the equivalent circuit, that means that current in reverse bias can only flow through R_{SCL}, and the voltage domain $V < 0$ is fully controlled by this non linear element. The question then arises of *How to connect the inclusion of this non-linear element to a physical structural composition?*

In ref. [77] it is proposed that this nonlinear, power law dependency of the current with respect to voltage can be explained with a SCL current. They also propose the physical origin and while their work is in the context of thin film solar cells, it can be applied to our bulk PN junctions. According to ref. [77] in a material with a high density of intraband

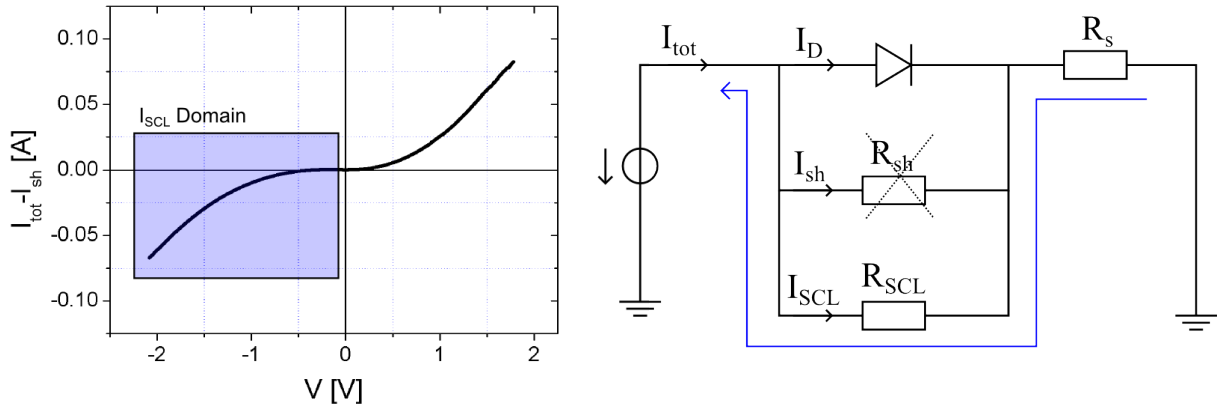

Figure 7.9: IV scan and equivalent circuit after the subtraction of I_{sh}.

states the current can be written as

$$|I_{SCL}| = C\,|V|^{\gamma+1} \tag{7.6}$$

where C is a constant and $\gamma > 1$. A very good power law fit with adjusted residual value of 0.999 can be done on the reverse bias domain in Figure 7.9, giving the the term I_{SCL} as described in equation 7.6 with $C = 0.011\,\mathrm{A}$ and $\gamma = 1.49$. If the term I_{SCL} is subtracted from the IV scan and removed from the equivalent circuit we are left with I_D.

The final output after the shunt and SCL elements have been accounted for results in the isolation of the diode current I_{D} as shown in Figure 7.10. In this figure a rectifying effect can be more clearly seen, which was not visible in the initial IV scan. Once I_D has been isolated, it is possible to inquiry what ideality factor comes out. But before that, more reasons are provided for the space charge limited current term.

Why a space charge limited current?

A space charge limited current occurs when current flowing through lightly doped or semi-insulating materials builds a space charge and develops an internal field that opposes the

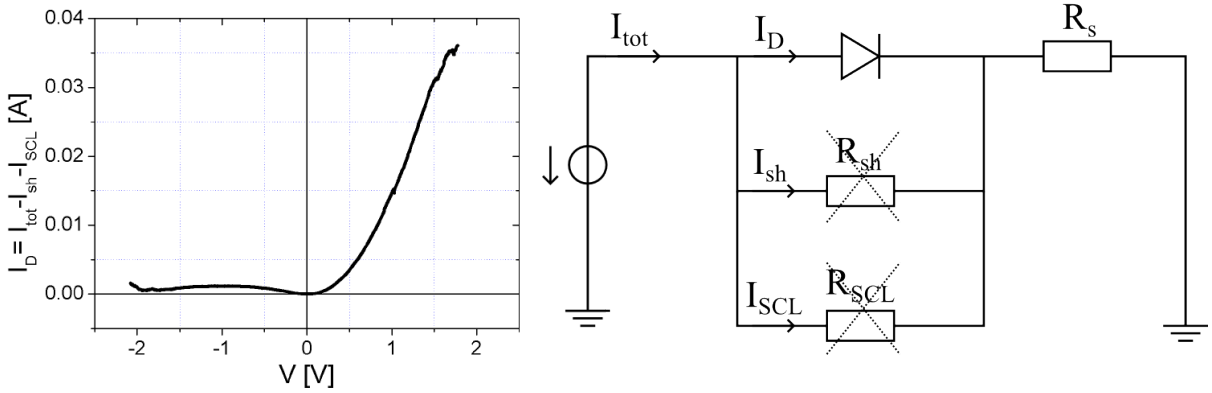

Figure 7.10: IV plot after the diode current I_{D} has been isolated. The positive current in reverse bias arises from errors due to the assumptions.

current flow (hence the term space charge limited). In our nanostructured PN junctions, the convergence of the complementary semiconductors develops a space charge region or intrinsic layer that arises from the intermixing of the powders previous and during the sintering process, since the sintering process reaches temperatures above 1000 °C in which impurity diffusion becomes active and particles are semi molten and mobile. These two mechanisms would lead to a carrier concentration compensation, and the formation of a mixture of a space charge region and an intrinsic layer [90].

In Figure 7.11 a band diagram of the nanostructured PN junction shows that a space charge limited current can be justified if a high density of intraband states is present within the space charge region or intrinsic layer. In that case charge carriers do not have to overcome the potential barrier, instead they can flow through the intraband states in the space charge region, and given that the concentration of carriers is expected to be low, a space charge would form due to the current flow. This also explains why I_{SCL} is much larger than I_{D}; charge carriers are more likely to hop through defect states than they are to overcome the potential barrier.

This fits together with the high density of intraband states required for a description

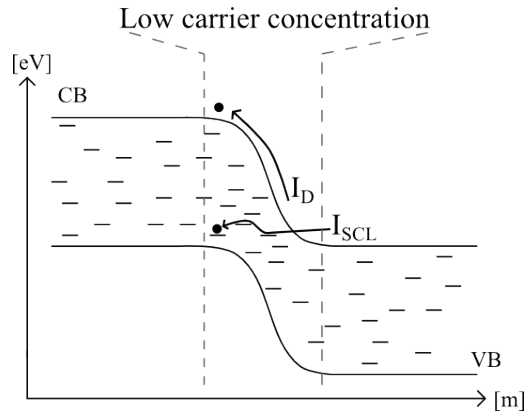

Figure 7.11: Band diagram of a PN junction showing SCLC transport.

by a space charge limited current in equation 7.6, and also in [122, 123] it is shown that SCLC is the dominating transport mechanism in intrinsic nanostructured silicon which fits perfectly to the argumentation here made.

Ideality Factor

It is important to recall that an ideality factor from I_{tot} does not make sense in the case of the nanostructured PN junctions because the IV response is not exponential, therefore the ideality factor is extracted from I_{D} even though $I_{\text{D}} << I_{\text{tot}}$ with the purpose to show that some diode structures have been formed at the microscopic level. When the extracted diode current I_{D} is plotted in a logarithmic scale, it is possible to get an idea of the range of values that the ideality factor η_{D} takes. In Figure 7.12 I_{D} is plotted with guidelines of the minimum and maximum values of η_{D}. Conventional diode theory dictates that an ideality factor only makes sense for values between 1 and 2 [76], however more advanced theory can explain higher ideality factors in silicon heterostructures as high as 10 [124].

In the scope of this work it is not so important to describe the ideality factor of our diodes because they do not have a single ideality factor, as it is to understand that a inhomogeneous PN structure has been formed, and that the range of ideality factors fall in a range that makes sense. The ideality factor of the nanostructured PN-TEGs can be

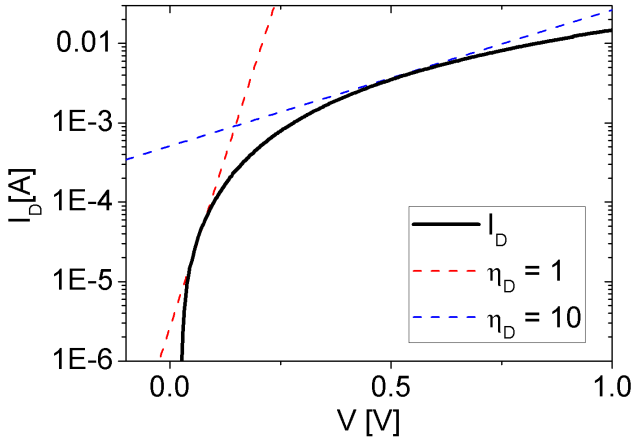

Figure 7.12: Logarithmic plot of the diode current I_D with minimum and maximum ideality factor plots.

approximated in the range of 1-10 which is quite high compared to the other types of PN-TEGs.

Effective Bandgap

It seems clear from the highly symmetric IV characteristic of the nanostructured PN-TEGs that the effective bandgap can be expected to be much lower than the nominal value of 1.1 eV for silicon. Using the method described in Section 6.2.2 the internal resistance of the PN-TEG is measured for different temperatures in two different conditions: $\Delta T = 0$ and $\Delta T > 0$.

Figure 7.13a shows the measurements done on sample no. 8. For the thermal equilibrium measurement (squares), the first thing to notice is that similar to the commercial diode, there are two domains with different slopes. The two observed slopes correspond to effective bandgaps of $E_{\mathrm{g,eff}} = 0.275\,\mathrm{eV}$ (blue line) and $E_{\mathrm{g,eff}} = 0.350\,\mathrm{eV}$ (red line). These bandgap values are maximum because recall that $R(T) \propto \exp\left(\frac{E_{\mathrm{g}}}{\xi k_{\mathrm{B}} T}\right)$ and it was assumed that $\xi = 1$ putting the maximum effective bandgap of the nanostructured PN junctions considerably below the 1.1 eV of crystalline silicon. Assuming the worst case scenario of uncertainty,

$\xi = 2$, one could say that the effective bandgap of sample no. 8 would be a value of $0.137\,\text{eV} \leq E_{\text{g,eff}} \leq 0.350\,\text{eV}$.

The same type of measurement can be done with a temperature gradient (stars). Recall that in a temperature gradient measurement, the sample is heated by increasing ΔT and in this case $T = (T_h + T_c)/2$. The measurement under temperature gradient shows a single slope and interestingly the effective bandgap is approximated to a value of $E_{\text{g,eff}} = 0.300\,\text{eV}$ which somewhat in the middle from of the two values observed in thermal equilibrium.

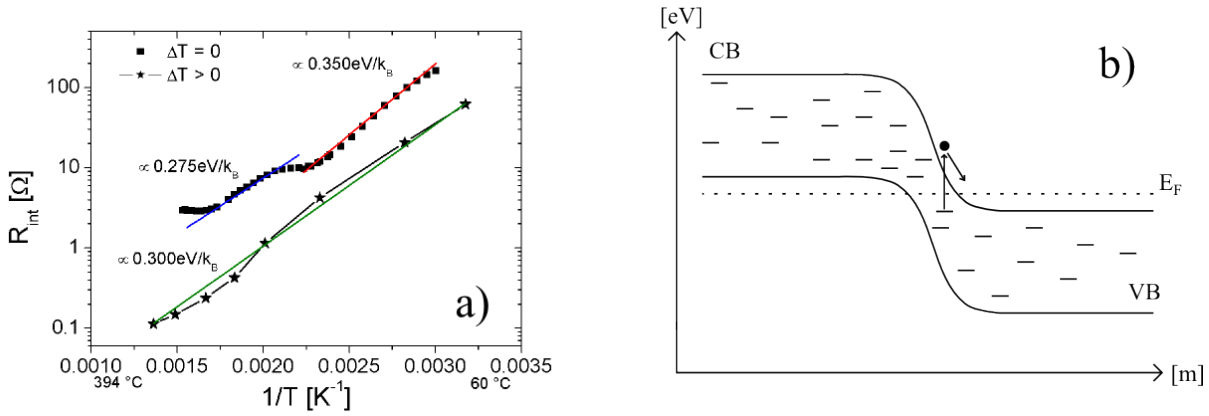

Figure 7.13: a) Estimation of the effective bandgap for $\Delta T = 0$ (squares) and $\Delta T > 0$ (stars) on sample no. 8. b) Electronic structure of the diodes showing the reduced effective bandgap.

The reason for the reduced bandgap in the nanostructured PN junctions is believed to be due to a high density of intraband states as sketched in Figure 7.13b. This explains why electric current can flow in both reverse and forward bias. It also goes in hand with the space charge limited current transport which requires a high density of intraband states. And it can be correlated to the preparation of the nanostructured PN-TEGs since powder intermixing before and during the sintering process leads to the introduction of electronic defects that manifest as intraband states.

Figure 7.14a shows the measurement of internal resistance as a function of average temperature for the different nanostructured PN-TEGs (squares). A good approximation

can be made to each measurement (solid lines with matching colors) and a maximum effective bandgap $E_{\mathrm{g,eff},\Delta T>0}$ can be extracted with $\xi = 1$. A summary of the extracted values of $E_{\mathrm{g,eff},\Delta T>0}$ is shown in Figure 7.14b. They range from 150 meV − 300 meV which is roughly one third of the bandgap of crystalline silicon. The take away from this data is that regardless of the preparation parameters, the PN-TEGs exhibit low effective bandgaps and it is possible to connect the electric characteristics to the structural characteristics and the preparation process.

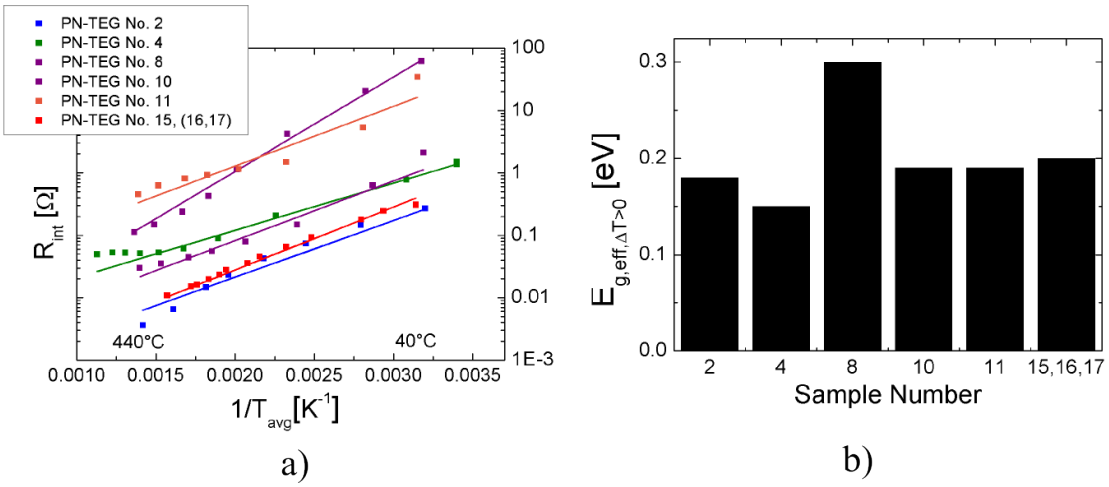

Figure 7.14: a) Arrhenius plot of R_{int} for different nanostructured PN-TEGs. b) Extracted effective bandgap values under a temperature difference from a).

7.2.3 Electrical Properties: Laser Annealed PN-TEGs

In order to maintain the focus on the current assisted sintering PN-TEGs, only one selected PIN-TEG prepared by the laser annealing method is presented as a representative of the laser annealed samples with the understanding that each sample varies considerably and a summary is given at the end of the section. A more complete description of different samples prepared by the laser annealing method can be found in ref. [94].

The IV response shows a highly asymmetric response (Figure 7.15a). The same electrical

model as before applies with the exception that the space charge limited element does not apply here; a diode in parallel with a linear shunt resistance R_{sh}, in series with a series resistance R_{s}. The same process used in Section 7.2.2 is applied to extract the internal resistance and the results are summarized in table 7.2. Note that these values are considerably higher than what was obtained for the current assisted sintering samples. The ideality factors can be estimated on $I_{\mathrm{tot}} \approx I_{\mathrm{D}}$ to meaningful values of $0.5 \leq \eta_{\mathrm{D}} \leq 2.7$ as shown for an exemplary sample in Figure 7.15b. The ideality factor of the laser annealed samples is considerably lower than the ideality factor of the current assisted sintering samples as expected since the preparation of the laser sintering PN junctions is more controlled.

In this case the non-linear space charge limited current element R_{SCL} does not apply because it makes no physical sense since the intrinsic wafer is not expected to have a high density of intraband traps in the main body. Intraband traps are expected but on the sides of the intrinsic wafer where the nanoparticle layers were annealed with the laser. The intraband states are responsible for a reduced effective bandgap when thermal generation is present but do not conduct current in forward and reverse bias as shown in Figure 7.15d.

The effective bandgap under a temperature difference $E_{\mathrm{g,eff},\Delta T>0}$ can be estimated in the higher temperature regime in the order of 0.270 eV with $\xi = 1$ as shown in Figure 7.15c. This value is lower than expected since it was believed that the laser annealed PN-TEGs would produce a more crystalline structure than the current assisted PN-TEGs. A summary of the PIN diodes prepared by the laser annealing process is shown in Table 7.2.

7.2.4 Electrical Properties: Wafer Welded PN-TEGs

A summary of samples produced by the laser welding method is presented in table 7.3. Note that R_{int} and η_{D} are in the same range as the samples produced by the laser method. The doping concentration of the wafers is not optimal since a good thermoelectric should

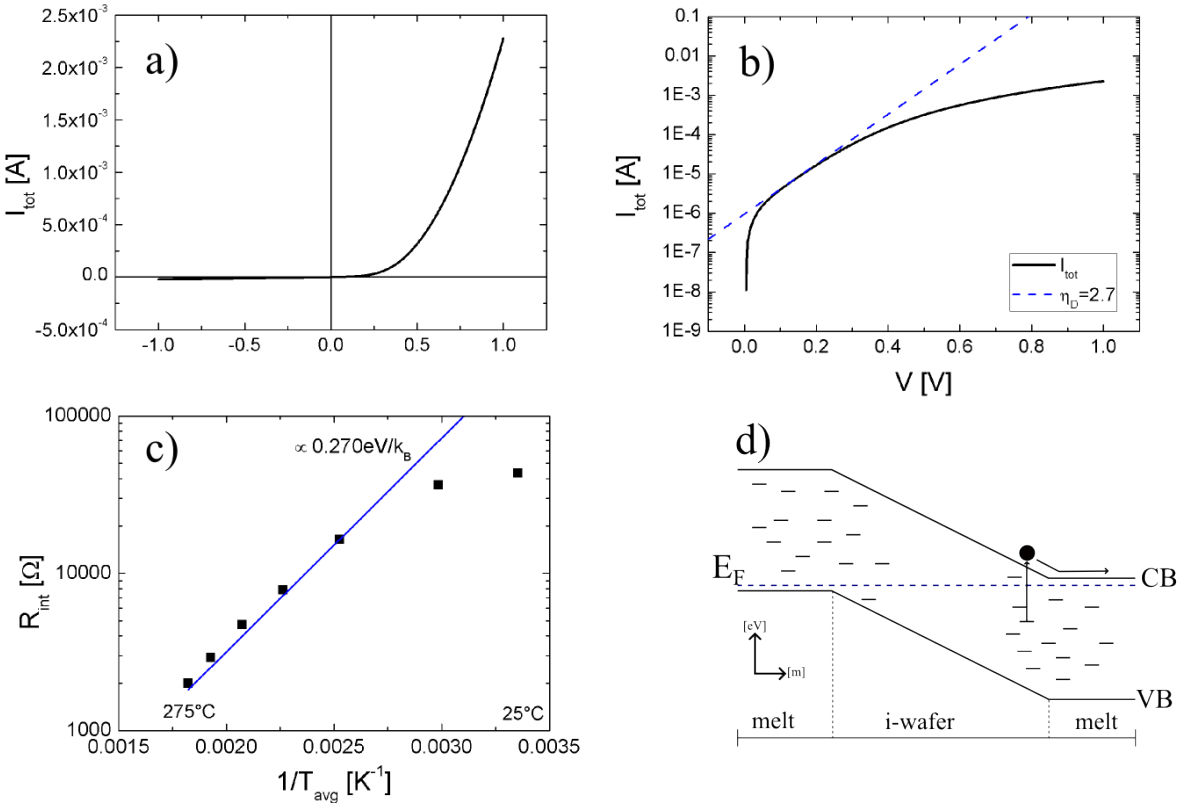

Figure 7.15: a) IV response of a laser annealed PIN diode. b) Logarithmic scale of the IV curve showing the estimation of the ideality factor. c) Arrhenius plot of R_{int} to estimate the effective bandgap under a temperature difference. d) Electronic structure of the PIN diodes showing the reason for the reduced effective bandgap when thermally generated carriers are excited.

Table 7.2: Summary of the different samples prepared by the laser annealing method. *Sample presented in this section.

	Sample No.	Type	Doping $N_{\text{A}} = N_{\text{D}}$ [cm^{-3}]	R_{int} [Ω]	η_{D}
	L07A*	PIN	5×10^{20}	44.3 k	0.5-2.7
	L07B	PIN	5×10^{20}	91.2 k	0.5-2.3
	L07C	PIN	5×10^{20}	73.4 k	0.1-2.3
	L08A	PIN	5×10^{20}	63.6 k	0.7-2.0
	L08B	PIN	5×10^{20}	79.4 k	1.0-2.0

have a higher doping concentration, but data generated from these samples important because it sheds light into the general phenomenological description of the PN-TEGs.

Table 7.3: Summary of the different samples prepared by the wafer welding method. *Sample presented in this section.

	Sample No.	Doping $N_A = N_D$ [cm^{-3}]	R_{int} [Ω]	η_D
	S2*	10^{15}	57.1 k	1.2-6.2
	S4	10^{15}	391 k	1.9-5.4
	S9	10^{15}	48.5 k	0.6-4.4
	S10	10^{15}	29,9 k	0.8-4.7

The effective bandgap under a temperature difference $E_{g,eff,\Delta T>0}$ is extracted for a representative sample from Figure 7.16a. This value is estimated $E_{g,eff,\Delta T>0} = 0.280\,eV$ with $\xi = 1$ which is in the same range as both the laser annealed and the nanostructured PN junctions. Again the reason for the reduced effective bandgap is the presence of intraband states but since these defects are believed to be localized only at the melt between the two wafers, see Figure 7.16b. This is the reason why a space charge limited current does not occur in the wafer welded PN-TEGs.

Samples prepared by the laser annealed method and the wafer welding method are expected to be similar electronically since they produce more defined PN interfaces than the current sintering method (note the similarity between Figures 7.15c and Figure 7.16a). It will be shown in the next section that their thermoelectric performance is also similar.

7.2.5 Summary of Electrical Characteristics

In this section the electrical properties of the PN-TEGs prepared by the three different methods were presented. Focus was given to the nanostructured PN-TEGs, and it was shown that this type of generators is the least ideal diode electrically speaking since the samples exhibit a relatively large ideality factor and a very low shunt or internal resistance in the order of hundreds of mΩ. It was shown that the nanostructured PN-TEGs can

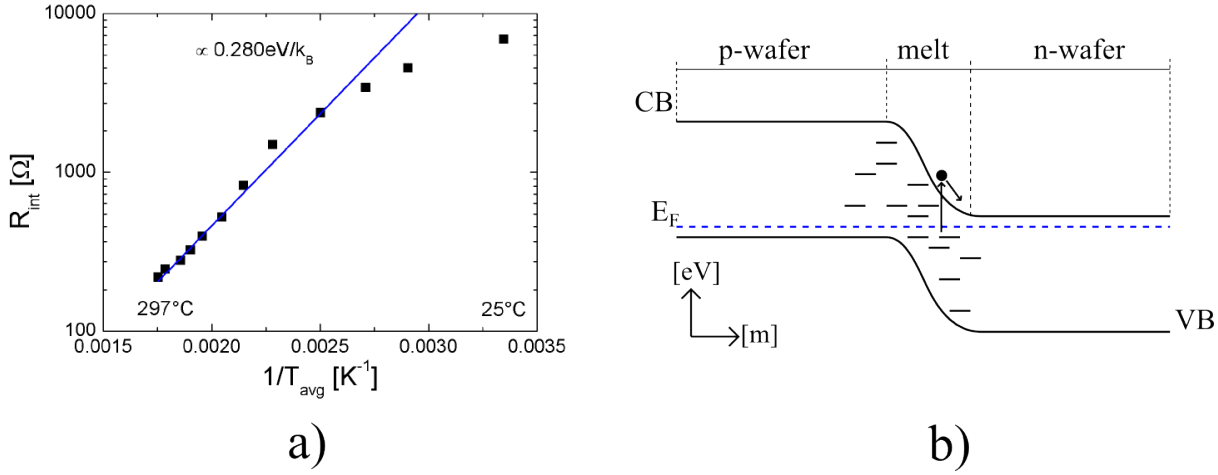

Figure 7.16: a) Arrhenius plot of the wafer welded PN junctions used to estimate the effective bandgap under a temperature difference.

be modeled with a diode in parallel with a linear and a non linear space charge limited current elements, all in series to a linear series resistance. The low ideality of the diodes (electrically speaking) is attributed to a very high density of intraband states everywhere on the volume of the PN-TEGs that as a consequence lower the effective bandgap of the PN junctions to values on the order of few hundreds of meV.

More ideal from the electronic point of view, are the PN-TEGs prepared by the laser annealing method and the wafer welding method. These PN-TEGs exhibit lower ideality factors and larger internal resistance values. The effective bandgap of these PN junctions was also in the order of a few hundreds of meV and this is is attributed to the presence of intraband states near the junctions of the different materials.

7.3 Thermoelectric Characteristics

This is perhaps the most important section of this thesis. Here the thermoelectric performance of the PN-TEGs is characterized by a device "Seebeck coefficient", a coefficient in V/K that quantifies the thermally generated voltage per temperature difference, and by

the maximum power output as a function of temperature difference. A limitation of the work here presented is that the heat current through the PN-TEGs is not known and so the efficiency cannot be calculated. Since it is not clear how to normalize the power output, judgment of the performance of a PN-TEG alone by the maximum power output is most meaningful when it can be compared to a known reference, and to achieve this simulations by S. Angst are introduced.

Unlike what was done in the previous section, the thermoelectric characteristics of the different types of PN-TEGs will be compared in parallel. First effective Seebeck coefficient of the different PN-TEGs will be compared and understood with the proposed theory. Next the power output will be presented. It will also be shown that a geometrical optimization can be made to raise the power output of the PN-TEGs by removing part of the PN junction.

7.3.1 Effective Seebeck Coefficient

The effective Seebeck coefficient $\alpha_{\text{eff}} = V_{\text{oc}}/\Delta T$ varies from sample to sample and this makes it difficult to explain the particular α_{eff} for every sample. However, there are certain properties of α_{eff} that are common to most samples and such properties can be explained from the model and the proposed theory. In Figure 7.17 the measurement of α_{eff} is plotted for different nanostructured PN-TEGs. As a relative reference the line is the sum of the absolute values of α from the best mono-polar nanostructured silicon from the same sources and using the same equipment that was used to prepare the PN-TEGs [49, 51].

We note that there is a relationship between internal resistance and the magnitude of α_{eff}; the samples with higher internal resistance show higher values of α_{eff}. This makes sense because of the inverse relationship between conductance and α. Moreover, samples that are prepared with the highest nominal doping concentration tend to have lower internal resistance values and lower α_{eff} as expected.

Another interesting point is that α_{eff} does not monotonously increase in Figure 7.17 as it would be expected from the monopolar highly doped silicon samples. For every nanostructured PN-TEG (and in fact for every type of PN-TEGs) α_{eff} decreases after a given temperature. According to the theory developed in chapter 4, as temperature increases the differential diodes become more conductive and the internal losses due to current vortices increase, leading to a reduced gain of output voltage per temperature difference. It is not possible to predict at what point in temperature this will occur because the samples are very inhomogeneous, so the properties of the differential equivalent diodes are unpredictable.

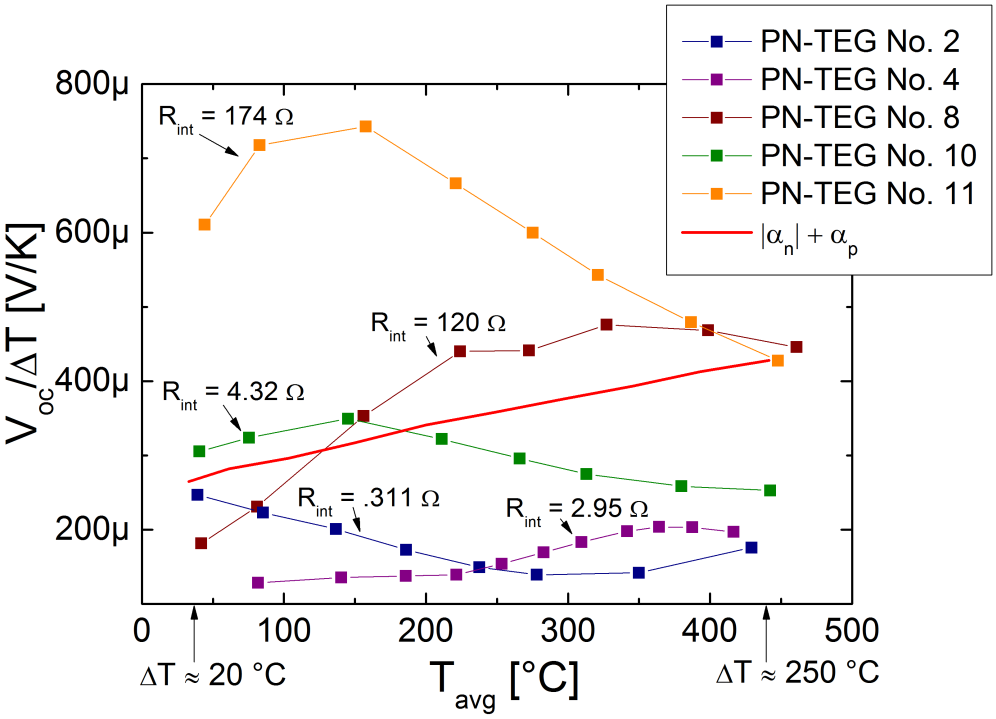

Figure 7.17: α_{eff} of different nanostructured PN-TEGs. The solid line is the sum of the absolute values of α_p and α_n from previously measured monopolar nanostructured silicon [49, 51].

In Figure 7.18 α_{eff} is plotted in black for an exemplary laser annealed PN-TEG in black and in red for a exemplary wafer welded PN-TEG. It makes sense that these PN-TEGs

show a similar response in α_{eff} since both types of TEGs are believed to have a more defined PN junction compared to the nanostructured PN-TEGs. While the shape of α_{eff} in Figure 7.18 is similar, the scaling in both axes is different. This is because a higher α_{eff} is expected with lower doping concentration and the laser annealed samples were prepared with a nominal doping concentration of $N_{\text{A}} = N_{\text{D}} = 5 \times 10^{20}\,\text{cm}^{-3}$ while the doping concentration of the wafer welded samples is much lower $N_{\text{A}} = N_{\text{D}} = 10^{15}\,\text{cm}^{-3}$. Again despite missing a specific resistivity, the total internal resistance finds a relationship with the magnitude of α_{eff}.

It is interesting that α_{eff} shows a similar response between the aforementioned PN-TEGs, and in fact α_{eff} shows a similar behavior in all three types of PN-TEGs in the sense that α_{eff} decreases for higher temperatures despite that they are prepared by completely different methods. Here is important to note that with increasing ΔT, V_{oc} increases as well but at a slower rate. It is shown in the next section that this problem is partially alleviated by cutting a fraction of the PN junction.

7.3.2 Geometric Optimization

In order to achieve the geometrical optimization proposed in section 4.2.7, a PN-TEG is cut into an initial geometry of $4\,\text{mm} \times 3\,\text{mm} \times 11\,\text{mm}$. After metallization, the PN-TEG is soldered into a commercially available insulating metal substrate as shown in Figure 7.19b. An insulating metal substrate is essentially printed circuit board that has a metal core instead of the more common polymer core. The advantage of the metal core over the polymer is a highly increased thermal conductivity that allows more heat flow from the PNG through the board into the heat sink. The PN-TEG is measured, desoldered, cut, and re-soldered, to produce measurements at different cut lengths h.

These measurements are shown in Figure 7.19a. A very strong trend indicates that for increasing cut length h, the effective Seebeck coefficient increases. And it is notorious that

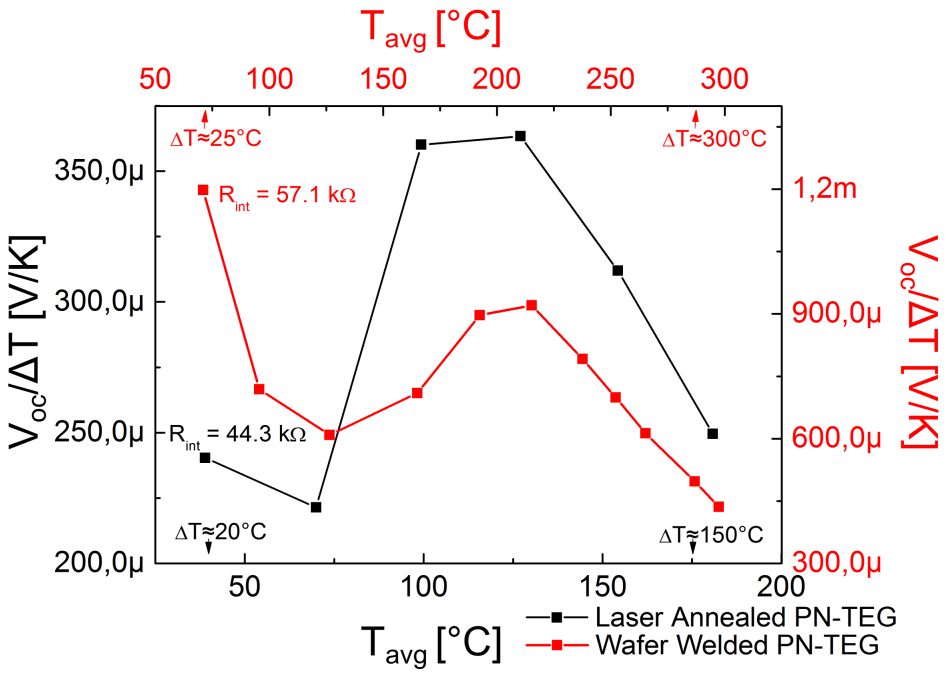

Figure 7.18: α_{eff} for an exemplary laser annealed PN-TEG (black) and an exemplary wafer welded PN-TEG (red). More measurements can be found in refs. [94, 98].

for the last two cuts (6 mm and 8 mm), α_{eff} maintains a positive slope with temperature for high temperatures which is unique among all the PN-TEGs that have been prepared by the different methods. This is an indication that the internal loops or voltage drops across the PN interface are reduced, leading to a larger output voltage per temperature difference at the cost of increased internal resistance.

The results match with a very similar experiment done on Bi_2Te_3 PN junctions, where in the same manner, the PN junction was gradually removed and the authors found an increase of α_{eff} with the cut length h [69].

The improvement in α_{eff} translates to an enhanced power output. Simulations by S. Angst on a PN-TEG with constant α, σ, κ show that the maximum power output for different cut lengths $P_{\text{max},h>0}$ normalized by the power with no cut $P_{\text{max,h=0}}$ exhibits an optimal cut length percentage of approximately 0.72 as shown in Figure 7.20a. Experimen-

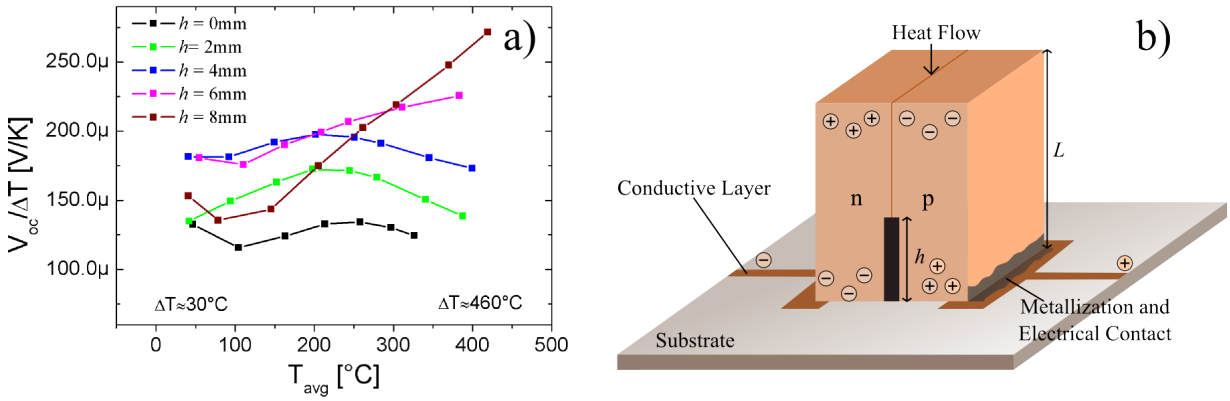

Figure 7.19: a) α_{eff} for different cut lengths h. b) Schematic of the PN-TEG and the substrate used to mount it.

tally, it can be shown that indeed there is a maximum in $P_{\text{max},h>0}/P_{\text{max},h=0}$ as shown in Figure 7.20b. However, the peak occurs at a different value of h/L which is not surprising given that the model is described with a homogeneous material and PN interface, and the experimental samples are highly inhomogeneous as it has been shown. The reason for the peak is a trade off between increasing α_{eff} with cutting length but also increasing R_{int}, and it is obvious that as $h \to L$, $R_{\text{int}} \to \infty$.

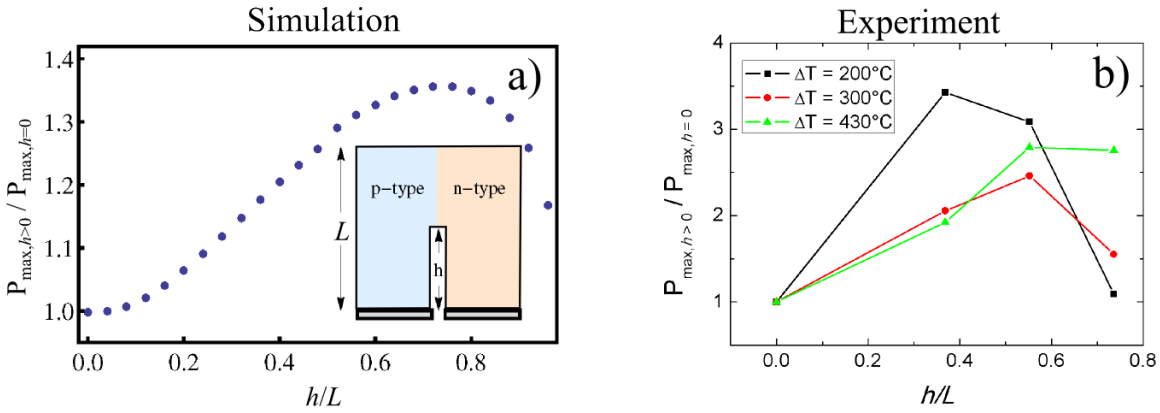

Figure 7.20: a) Simulation by S. Angst shows an optimal cut length percentage at approximately 0.72. b) Experimental data for different ΔTs shows that indeed a peak with respect to the cut length percentage occurs.

7.3.3 Power Output

The power output is the most important quantity that characterizes the PN-TEGs. Conventionally the figure of merit and/or the efficiency are used to describe thermoelectric generators, however we refrain from using the figure of merit without a proper theoretical fundation, and since the heat current through the PN-TEG is not known the efficiency cannot be calculated.

For these reasons we appeal to compare the power output of PN-TEG with simulations of a conventional TEG using the discrete form of Onsager relations, and with experimental data of a conventional TEG built with the same materials as the PN-TEG. The experimental PN-TEG was cut such that the cross-sectional area of each leg is $A/2 = 1$ and the length $L = 1$. The simulated conventional TEG is given the same geometry as the PN-TEG, solving the issue that the specific conductivities are not known in the PN-TEG (see sketches in Figure 7.21). The simulation is fed with temperature dependent $\alpha(T)$, $\kappa(T)$ and $\sigma(T)$ from measurements of monopolar nanostructured p-type and n-type silicon prepared by the same process as the nanostructured silicon in the PN-TEGs [51, 49]. The third element in the comparison is the power contribution of a single thermocouple pair of a conventional TEG built using nanostructured silicon processed by the same methods as the PN-TEG [54, 125].

For the case of the PN-TEG and the simulated conventional TEG a normalization of $P_{\max}$ is not necessary because they have the same geometry. However the geometry of a single thermocouple from the generator in ref. [54] differs from the others. Some authors normalize the maximum output power $P_{\max}$ by the area of the thermoelectric material or the area of the complete device to describe the areal power density [126, 127]. When $P_{\max}$

of a single thermocouple is divided by the thermoelectric material area $2A$

$$\frac{P_{max}}{2A} = \frac{V_{oc}^2}{8L(\rho_n + \rho_p)} \tag{7.7}$$

the length L of the thermoelectric material is left as a variable, and so is the areal power density. For this reason we normalize also by the length L as follows:

$$P_0 = \frac{P_{max}L}{2A} = \frac{V_{oc}^2}{8(\rho_n + \rho_p)} \tag{7.8}$$

The plot of P_0 is shown in Figure 7.21 together with the schematic of the different devices that are compared. The first thing to note is that the conventional experimental TEG (stars) delivers less power than the conventional simulated TEG (solid black line). That makes sense since the simulation assumes no parasitic thermal or electrical contacts. The experimental TEG could was measured up to $\Delta T \approx 150\,°\text{C}$ in order to protect the TEG. A power law fit (dashed line) is done on the experimental TEG data to get an idea of the performance if the conventional TEG could be subject to higher ΔTs.

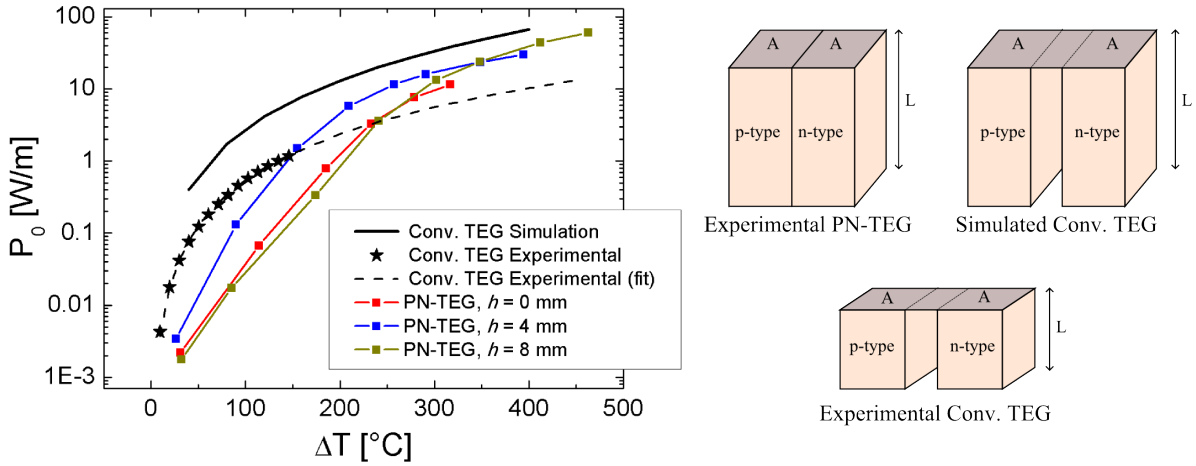

Figure 7.21: Normalized maximum power output (left) and schematic of the different devices (right).

The power output of a PN-TEG for different cut length h is shown in colors. It can be seen that the PN-TEG performs poorly at low ΔTs but it would outperform the experimental TEG at large ΔTs except that the experimental TEG could not be measured in these high temperatures, highlighting the potential of the PN-TEG architecture. In order to compare the PN-TEG to a conventional TEG at large temperature differences, simulations are needed and it can be seen that the PN-TEG approaches the simulation of a parasitic-free TEG. The good thermoelectric performance of the PN-TEG at large ΔTs is a consequence of the reduced internal resistance. Recall from the bandgap measurements that the internal resistance of a PN-TEG decreases monotonically with temperature. This is not the case of a conventional TEG where the internal resistance increases with temperature since the semiconductor is a quasi-metal.

In Figure 7.22 the normalized power output P_0 of the three types of PN-TEG is presented. Here the best sample from each type of PN-TEGs is selected. It is clear that the nanostructured PN-TEG produced by the current assisted sintering method yields the best performance by orders of magnitude. The wafer welded and laser annealed PN-TEGs perform in a closer range due to their structural and electronic similarities. The reason for the poor thermoelectric performance of the wafer welded and laser annealed PN-TEGs is believed to be due to a lack of a high density of traps states (both are built with quasi-crystalline wafers) which results in a more defined PN structured with higher internal resistance that limits the current output.

Focusing now on the nanostructured PN-TEGs, a summary of the normalized power output P_0 of the nanostructured PN-TEGs in Figure 7.23 shows that all samples seem to perform in a relatively small window. However PN-TEG 4 and 8 show an inferior performance, and one can trace a similarity between PN-TEGs 4 and 8 in that both samples were prepared with the lowest n-type doping concentration. From conventional diode theory having lower levels of doping concentration would widen the depletion region.

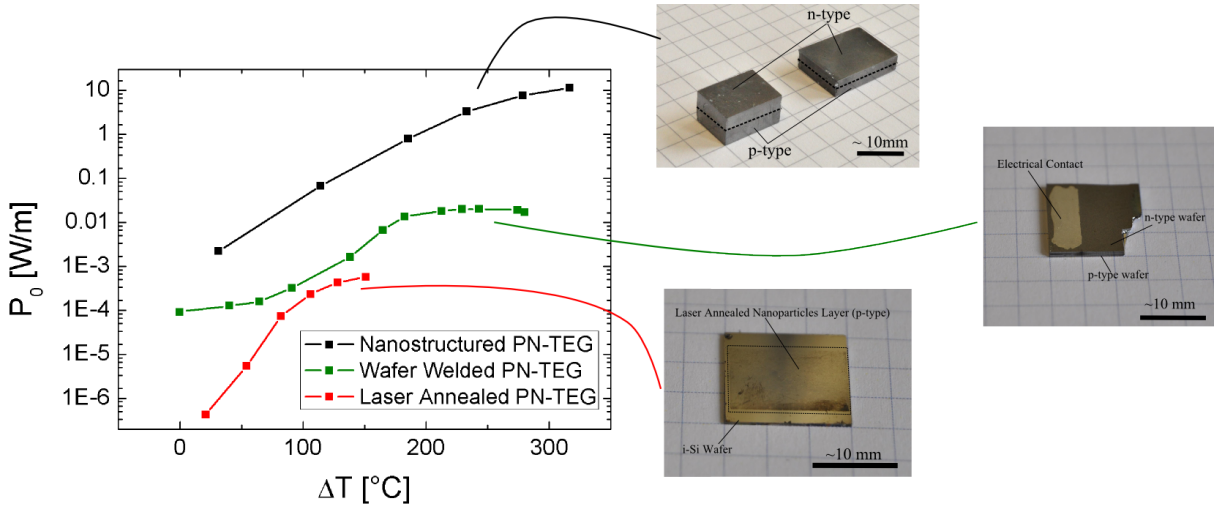

Figure 7.22: Normalized maximum power output of the three different types of PN-TEGs produced in this work.

In light of this having lower doping concentrations is thought to enhance the intrinsic layer formed during the sintering process and as a consequence the output current is of the TEG is limited. Moreover, PN-TEG 15 which shows the highest power output has been prepared with the highest doping concentration (see table 5.1). Therefore a direction for further research would be to use high nominal doping concentrations.

7.3.4 PN-TEG and Conventional TEG: Comparison

Comparison 1: Matching geometries

As mentioned earlier a rigorous one-to-one comparison between a PN-TEG and a conventional TEG is not possible with the present knowledge. However, under some assumptions, some comparisons can be made. In the previous section a PN-TEG was compared to the simulation of a conventional TEG, where the two devices had the same geometry. The advantage of this comparison is that the simulation can come into high temperature ranges where an experimental conventional TEG would otherwise not be stable. However, a conventional TEG can be built with the same geometry and materials as a PN-TEG and

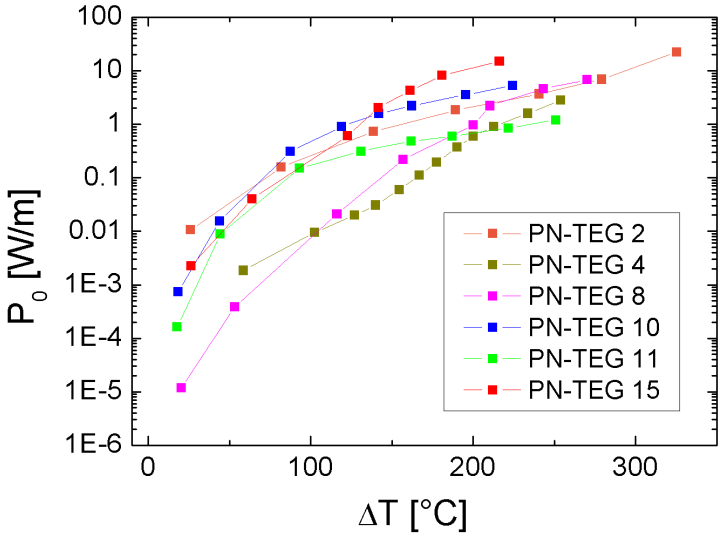

Figure 7.23: Normalized maximum power output of the nanostructured PN-TEGs.

measured in the same equipment using lower temperature differences.

A sketch of the experiment is shown in Figure 7.24. A PN-TEG with the given geometry is prepared, and a conventional TEG is built from the same source materials and geometry as the PN-TEG. In the case of the conventional TEG, there is no substrate on the hot side but nickel is used as metallization as described in section 5.1.3, and the two semiconductor legs are joined my a copper interconnect. The copper interconnect is joined to the nickel metallization using a commercial silver adhesive. A ceramic fin is placed between the semiconductor legs of the conventional TEG to provide mechanical robustness because during the measurement pressure is applied perpendicular to the temperature gradient and this produces a torque that has to be sustained by the weak mechanical bond at metallic bridge (Figure 7.24b).

A fair comparison could be made if it is assumed that the thermal conductance of the two devices is the same. In open circuit conditions this is an easier claim because the materials and the dimensions are the same. However when electric current flows, this becomes more complicated because Peltier effects on the PN-TEG are not fully understood. However,

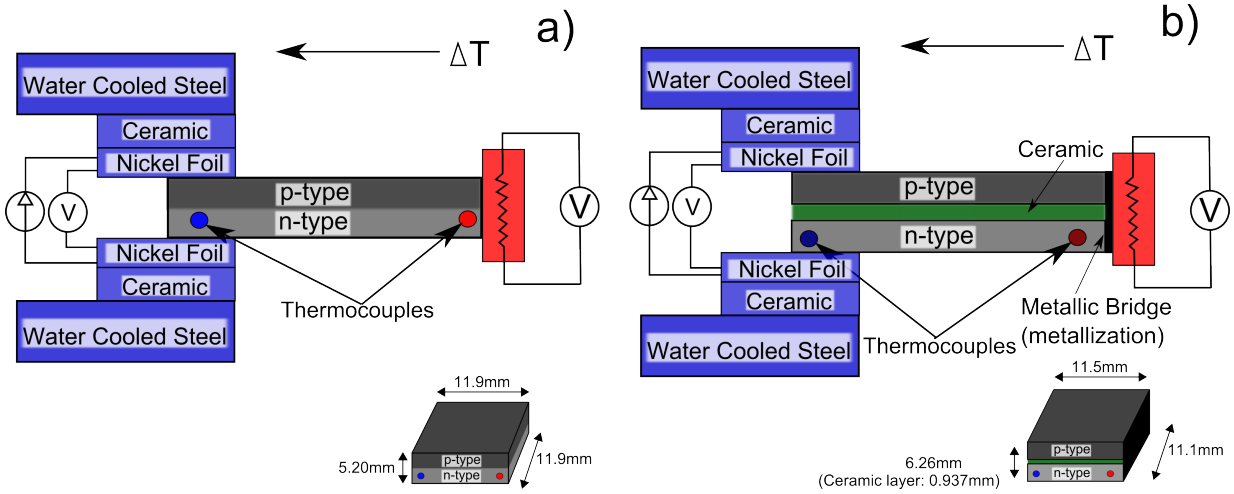

Figure 7.24: a) Schematic of the PN-TEG and the measuring setup. b) Schematic of the conventional TEG. The dimensions of the thermoelectric material are equal.

the main point of concern is a technological one; the delicate process of metallization and assembly produced a conventional TEG with an internal resistance in the order of few Ohms at room temperature when the expected value would be of hundreds of milli Ohms.

More reasons to believe that the electrical contacts on the conventional TEG were defective comes from the temperature response of the internal resistance which is plotted in Figure 7.25a. We note that R_{int} of the PN-TEG exhibits an exponential decrease in temperature as expected, while R_{int} of the conventional TEG shows a linear increase with temperature. This abnormal behavior is believed to have a source in the silver adhesive paste used to attach the copper bridge because the nickel metallization on the nanostructured-silicon has been more extensively tested [54].

Since the open circuit voltage is immune to defective electrical contacts, a measurement of the effective Seebeck coefficient provides a more meaning comparison. As expected from the proposed theory the α_{eff} of the conventional TEG is higher than α_{eff} of the PN-TEG as shown in Figure 7.25b. This is because the PN-TEG develops internal voltage drops. Moreover α_{eff} of the conventional TEG sees a linear increase with temperature which is what one would expect from the sum of the Seebeck coefficients of the mono-polar materials.

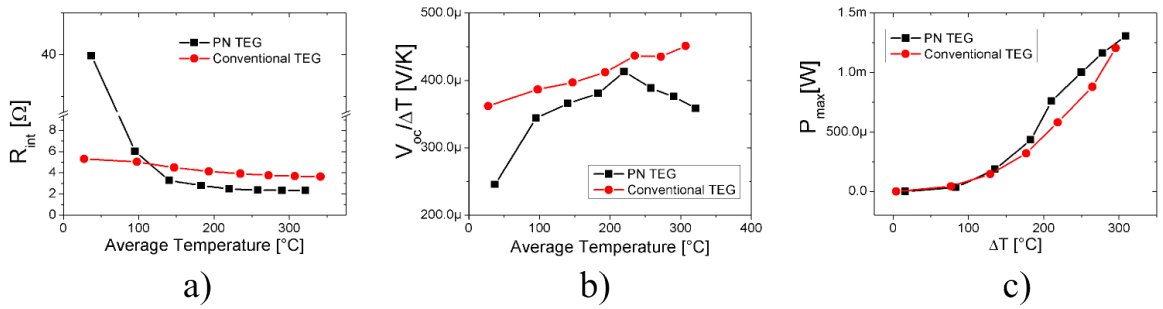

Figure 7.25: a) Internal resistance, b) effective Seebeck coefficient and c) maximum power output of a conventional TEG and a PN-TEG with matching geometry. PN-TEG 8 was used.

The maximum power output in Figure 7.25c shows that both devices produce nearly the same power. However this should not be taken as a true comparison of the intrinsic technologies because the defective electrical contacts on the conventional TEG limit its performance. The entire experiment serves the purpose of highlighting the aforementioned difficulties of high temperature stable electrical contacts and the technological advantages of the PN-TEG architecture. A second attempt was done to produce a conventional TEG but was unsuccessful.

Comparison 2: Figure of Merit

From the rigorous point of view it would not be appropriate to use the thermoelectric figure of merit to describe a PN-TEG for reasons given in chapter 4. However, the qualities that the figure of merit describes also apply to a PN-TEG; a high electrical conductivity and effective Seebeck coefficient are desired combined with a low thermal conductivity. For this reason to make a conservative comparison, the device figure of merit of a conventional TEG is compared with the equivalent of a PN-TEG.

A conventional TEG with 64 legs, 32 thermocouple pairs, made from nanostructured silicon prepared by the same source materials and densification [54] was measured using the Harman technique described in section 6.3.1. The advantage of the Harman technique is that it provides a direct measurement of the device figure of merit ZT by measuring two

voltages.

The figure of merit of a PN-TEG requires some assumptions in any case. It has been shown in this work that the effective Seebeck coefficient can be extracted as well as the internal resistance. In light of this, the thermal conductance is missing to complete the figure of merit. In order to calculate the thermal conductance, thermal conductivity values are taken from the literature. In that case the figure of merit of a PN-TEG can be written as

$$ZT_{\mathrm{PN}} = \frac{\alpha_{\mathrm{eff}}^2}{R_{\mathrm{int}} K_{\mathrm{PN}}} T_{\mathrm{avg}} \tag{7.9}$$

with

$$K_{\mathrm{PN}} = \frac{A}{L} (\kappa_p + \kappa_n) \tag{7.10}$$

where A and L are the cross sectional area and the length of the thermoelectric material as defined in Figure 7.21 and $\kappa_p(T)$ and $\kappa_n(T)$ are obtained by doing a linear regression on the data from previously measured nanostructured monopolar silicon in a range of $20 - 400\,^{\circ}\mathrm{C}$ [51, 49].

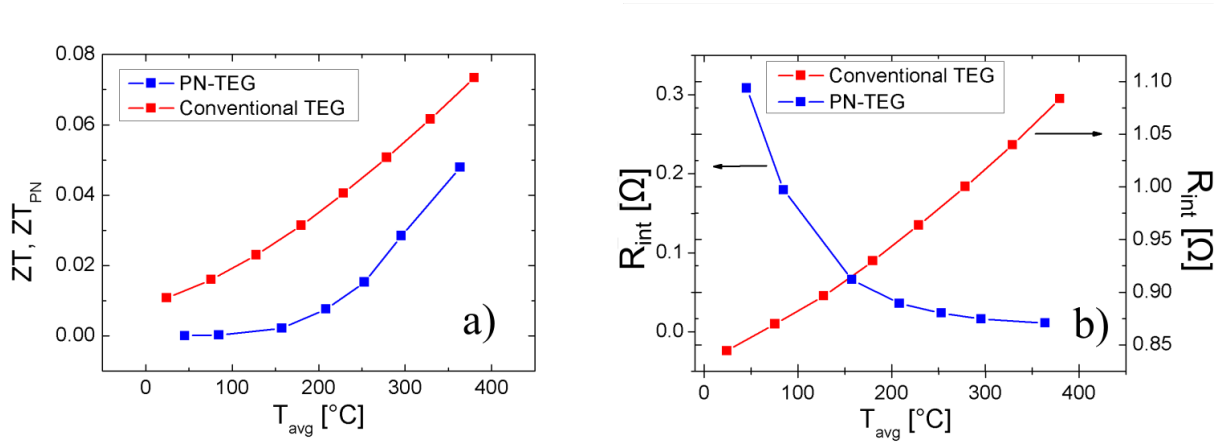

Figure 7.26: a) Figure of merit of a conventional TEG, ZT measured by the Harman technique and calculated figure of merit of a PN-TEG, ZT_{PN}. b) Internal resistance of a conventional TEG measured by the Harman technique and of a PN-TEG measured by the Monkey setup.

In Figure 7.26a ZT and ZT_{PN} are shown. The absolute values need to be taken with care because of the assumptions made, but it is interesting (and expected) that the PN-TEG shows a higher ZT_{PN} at high temperatures. This goes in line with what has been previously shown. Here it is important to recall that the Harman technique uses near equilibrium conditions, $\Delta T < 1\,^{\circ}\mathrm{C}$ while the Monkey setup used to characterize the PN-TEG uses large temperature differences $\Delta T > 100\,^{\circ}\mathrm{C}$ which makes the average temperature somewhat ambiguous.

Judging from Figure 7.26a one would conclude that the PN-TEG has an inferior performance, but recall from Figure 7.21 that when power output is considered, the PN-TEG performs better than the conventional TEG and also is measured in a temperature range where the conventional TEG cannot be measured, this information is not seen when one looks at the figure of merit. This highlights the difficulties that arise if one tries to describe a PN-TEG with the conventional figure of merit.

Figure 7.26b is interesting because it highlights yet another fundamental difference between a conventional TEG and a PN-TEG. The internal resistance of a conventional TEG rises with temperature as expected, but the internal resistance of a PN-TEG decreases with temperature. The decrease in internal resistance of the PN-TEG is the source of the high power output at high temperatures. It is true that the junction of complementary semiconductors creates an electrically isolating layer, but it is also true that if a high density of traps is present and high temperatures are applied, this layer becomes highly conductive.

7.3.5 High Temperature Stability and Reproducibility

Up to now the discussions have used large ΔTs but very little has been said about the absolute values of the boundary temperatures. One of the strongest advantages of a PN-TEG architecture is that it opens the door for high temperature applications. In this section it is shown that the PN-TEG can sustain temperatures as high as $770\,^{\circ}\mathrm{C}$ on the

hot side without suffering negative degradation. This temperature is at the time of writing limited by the heating and cooling power of the setup not by aspects related to the PN-TEG itself. So it is very likely that this temperature can be pushed higher with a more advanced setup.

In order to investigate the temperature stability of the nanostructured PN-TEGs, a sample is measured and after every measurement the hot side temperature is incremented. The data in Figure 7.27a shows that after an initial run, the internal resistance of the PN-TEG remains largely unchanged over measurements up to a maximum hot side temperature of 770 °C. The data points are crowded but that is what we expected to see. In Figure 7.27b the maximum power output of the PN-TEG remains largely unchanged despite increasing hot side temperatures. This shows to some extent that the PN-TEGs can be subject to hot side temperatures up to 770 °C without suffering degradation. There are two factors that will limit the temperature operation of the PN-TEGs; the temperature difference and the hot side temperature. The temperature difference in this work is of 450 °C at maximum but that is limited by the cooling power saturation of the monkey setup. As the hot side temperature is pushed further reactions such as oxidation and dopant diffusion are expected to occur when reaching the thousands of °C.

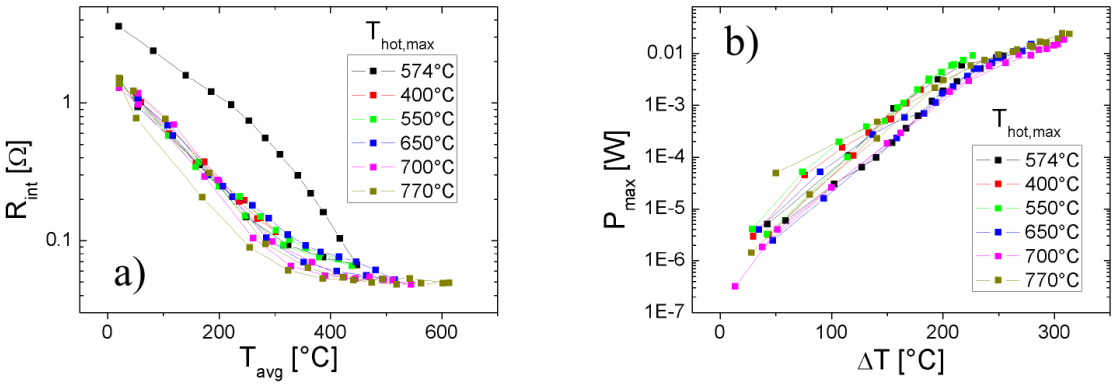

Figure 7.27: a) Internal resistance and b) maximum power output of PN-TEG 4.

Not so much data is available on high temperature TEGs but taking a couple of published results the PN-TEG presented in this work indeed offers the possibility for high temperature applications where conventional TEGs cannot operate. Table 7.4 shows the PN-TEG compared to other types of generators built with different materials. The temperature difference is important because it shows to what degree the complete device is able to stand the thermal stresses. The hot side temperature is obviously important because together with ΔT, these quantities define the operating conditions and integration of the technology to real world applications. In the case of the PN-TEG, both quantities are currently limited by the setup, and it should be able to push them further.

Table 7.4: Summary of different TEGs and their maximum reported operating temperatures.

	Author	Material	$\Delta T_{\max}$	$T_{\mathrm{h,max}}$
	This work	Nanostructured silicon PN-TEG	450 °C	770 °C
	Bartholome [126]	Half-Heusler	527 °C	547 °C
	Kessler [54]	Nanostructured silicon	300 °C	600 °C
	Lertsatitthanakorn [128]	Bi_2Te_3	150 °C	240 °C

Reproducibility and control of the process is a big issue at this point of the research. Very few parameters have been changed and yet the PN-TEGs vary largely from one another. Normally one sintered pellet produces one PN-TEG. But in order to know more about the internal homogeneity of the sintered pellet, a bigger pellet (80 mm in diameter vs 20 mm) was sintered using the parameters from PN-TEG 15 (see table 5.1) and cut in over 50 PN-TEGs [3]. Figure 7.28 shows R_{int} for the different PN-TEGs and in a solid line is the calculated mean. The standard deviation in percentage of the mean is of 30%, a value that is quite high. That means that the internal inhomogeneities need to be addressed and corrected before thinking of producing a homogeneous batch of pellets. It is to some

[3] Same geometry as PN-TEG 15.

degree understandable that the internal inhomogeneities are that large given that the precompation of the complementary powders is done by hand in a highly artistic process.

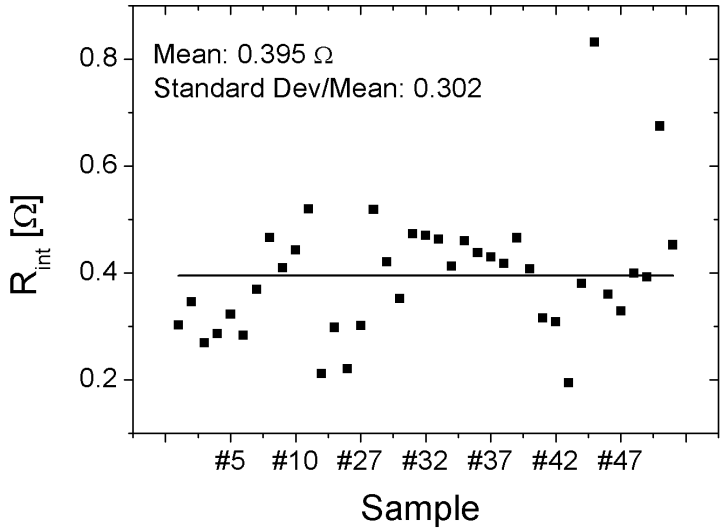

Figure 7.28: Internal resistance for different PN-TEGs from the same sintered pellet. The solid line is the mean value.

7.3.6 Summary of Results and Discussion

In this chapter the characteristics of the PN-TEGs are broken intro three categories: structural characteristics, electrical characteristics and thermoelectric characteristics. In the structural characteristics section it was shown that the nanostructured PN-TEGs exhibit a gradual dopant transition and a nanostructured bulk characteristic with a high density of grain boundaries and defects that reduce the lattice thermal conductivity. The laser annealed and wafer welded PN-TEGs offer a more defined PN junction structure without the benefit of the reduced thermal conductivity but with the advantage that they are easier to study.

Electronically speaking all three types of PN-TEGs show a very low effective bandgap value, in the order of hundreds of milli eV. However, only the nanostructured PN-TEGs

are believed to have a high density of intraband states in the whole volume whereas the laser annealed and the wafer welded PN-TEGs are believed to have a high density of trap states only on the surface of the wafers. As a result, the nanostructured PN-TEGs have a much smaller internal resistance which provides yet another advantage thermoelectrically speaking.

It was shown that a nanostructured PN-TEG can be operated in temperature regimes where conventional TEGs cannot be operated. And simulations have been used to produce data in this high temperature domain that show that the PN-TEG can compete with the conventional architecture. Furthermore it was shown that a geometrical optimization can be done to reduce the internal losses both experimentally and by numerical simulations. Of the three types of PN-TEGs the nanostructured offer the higher thermoelectric performance and it is yet to be optimized with respect to the preparation parameters.

8 Conclusions and Outlook

> More than machinery we need humanity. More than cleverness, we need kindness and gentleness. Without these qualities, life will be violent and all will be lost.
>
> Charlie Chaplin

8.1 Conclusions

In this work an alternative device architecture for thermoelectric generators has been proven functional and offers advantages over the conventional architecture. The PN-TEGs proposed in this work are made by joining the thermoelectric materials to make a PN junction where the contacts are made exclusively at the cold side. A working principle is proposed where the PN-TEGs can be understood as an array of differential diodes at different temperatures. It was suggested that the diodes at the hot side boundary become reversed bias but highly conductive due to the high temperature. Simulations done by S. Angst using a discrete from of Onsager's relations in a square grid corroborate this hypothesis and furthermore show that internal losses develop due to internal current vortices that from inside the PN-TEG.

Silicon was selected as the material of choice to produce the PN-TEGs because of its scalability potential and lower cost. However crystalline silicon has a high thermal conductivity and in order to reduce the lattice thermal conductivity, nanostructured silicon is produced in a bottom-up approach by compacting doped nanoparticles into bulk materials of nearly the same density of crystalline silicon. Nanostructured PN-TEGs show highly non-ideal diode characteristics but outstanding thermoelectric characteristics. Because of the non-ideal diode characteristics of the nanostructured PN-TEGs, more defined structures are produced by laser annealing doped silicon nanoparticles on top a silicon wafer to produce laser annealed PN-TEGs or by welding two wafers together by means of Joule heating to produce wafer welded PN-TEGs. These structures show better diode characteristics but inferior thermoelectric performance. However, they are useful in testing the proposed theory.

Two measurement setups were designed to test thermoelectric modules. The monkey setup was built to measure the PN-TEGs in large temperature differences. The name was given because an early prototype resembled a monkey, see Figure 8.1. The Harman setup was built to measure the figure of merit of conventional TEGs and to perform temperature dependent measurements. The results show that the nanostructured PN-TEGs can be operated to a maximum hot side temperature of 770°C and temperature difference of 450°C. Furthermore it was shown that nanostructured PN-TEGs can be used in temperature ranges where conventional devices cannot be operated thus opening the door for high temperature applications. The results obtained from the measurements of the PN-TEGs were understood with the proposed theory thus showing that the proposed description was compatible.

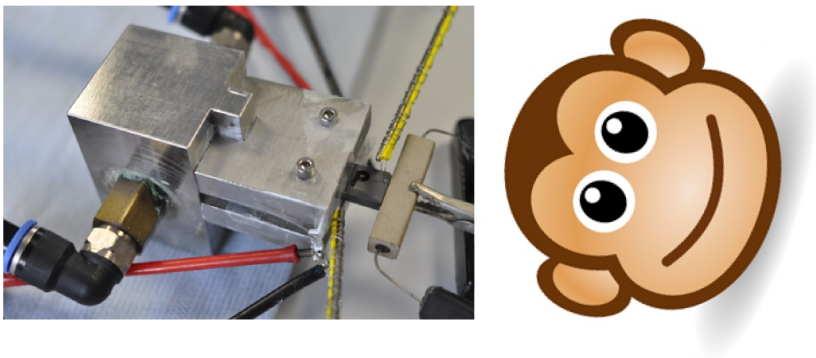

Figure 8.1: Monkey Setup.

8.2 Outlook

A more controlled way should be found if the PN-TEGs are to be produced from nanoparticles. Perhaps the biggest question that has been raised is *what is the efficiency of a PN-TEG?* given that the figure of merit cannot be directly applied and that Peltier effects are not fully understood. The best approach to get an insight into the efficiency of a PN-TEG would be to measure the heat flowing through the device. This will have to be done carefully and perhaps with a radical approach because only a few materials can be used in such high temperatures and coupled to that is the necessity to account for radiation transport.

So far the only optimization was investigated with respect to the geometry but the preparation parameters have been remained largely constant. S. Angst has shown that an optimal working point can be found with respect to the bandgap as well, and it is not so clear what would be the best doping concentration as well. This work has used silicon as a system material but the architecture is not material limited, that means that the same should in theory be possible with other material systems.

The demonstrated architecture could find applications where large temperatures are desired. For example in solar concentration thermoelectric applications [129, 130] where

the simplified design could lower the cost of the produced energy, which is the ultimate parameter that determines the application that the technology finds. Another aspect where this design could be applied is in the automobile industry where the heat waste recovery occurs at the exhaust pipe at a few hundred degrees. This has to do partially with the material used (Bi_2Te_3) [131]. However a PN-TEG could be operated closer to the engine where an active cooling mechanism is already in place, taking advantage of higher temperatures.

9 Publications

1. **R. Chavez**, S. Angst, K. Maize, A. Gondorf, G. Schierning, D. Wolf, A. Lorke, A. Shakouri. Thermoreflectance Imaging of Percolation Effects and Dynamic Resistance in Indium Tin Oxide Nanoparticle Layers. *Journal of Applied Physics* 112(8), 083705 2012.
   DOI: http://dx.doi.org/10.1063/1.4757960

2. V. Kessler, M. Dehnen, **R. Chavez**, M. Engenhorst, J. Stoetzel, N. Petermann, K. Hesse, T. Huelser, M. Spree, G. Schierning and R. Schmechel. Electrical Contact Resistance of Electroless Nickel to Nanocrystalline Silicon and the Fabrication of a Thermoelectric Generator. *Materials Research Society* 1553, 2013.
   DOI: http://dx.doi.org/10.1557/opl.2013.863

3. **R. Chavez**, A. Becker, V. Kessler, M. Engenhorst, N. Petermann, H. Wiggers, G. Schierning, R. Schmechel. A new Thermoelectric Concept Using Large Area PN Junctions. *Materials Research Society* 1543, 2013.
   DOI: http://dx.doi.org/10.1557/opl.2013.954

4. A. Becker, **R. Chavez**, N. Petermann, G. Schierning, R. Schmechel. A Thermoelectric Generator Concept using a p-n Junction: Experimental Proof of Principle. *Journal of Electronic Materials* 42(7):2291-2300, 2013.
   DOI: http://dx.doi.org/10.1007/s11664-012-2399-5

5. **R. Chavez**, A. Becker, M. Bartel, V. Kessler, G. Schierning, and R. Schmechel. Note: High Resolution Alternating Current/Direct Current Harman Technique. *Review of Scientific Instruments* 84:106106, 2013.
   DOI: http://dx.doi.org/10.1063/1.4825118

6. **R. Chavez**, S. Angst, J. Hall, J. Stoetzel, V. Kessler, L. Bitzer, F. Maculewicz, N. Benson, H. Wiggers, D. Wolf, G. Schierning, R. Schmechel. High Temperature Thermoelectric Device Concept Using Large Area PN Junctions. *Journal of Electronic Materials* 43(6):2376-2383, 2014.
   DOI: http://dx.doi.org/10.1007/s11664-014-3073-x

7. V. Kessler, M. Dehnen, **R. Chavez**, M. Engenhorst, J. Stoetzel, N. Petermann, K. Hesse, T. Huelser, M. Spree, C. Stiewe, P. Ziolkowski, G. Schierning, R. Schmechel. Fabrication of High-Temperature-Stable Thermoelectric Generator Modules Based on Nanocrystalline Silicon. *Journal of Electronic Materials* 43(5):1389-1396, 2014.
   DOI: http://dx.doi.org/10.1007/s11664-014-3093-6

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Bibliography

[1] Key World Energy Statistics. Technical report, International Energy Agency, 2014.

[2] Ali Shakouri. Recent Developments in Semiconductor Thermoelectric Physics and Materials. *Annual Review of Materials Research*, 41(1):399–431, 2011.

[3] R Landauer. Spatial Variation of Currents and Fields Due to Localized Scatterers in Metallic Conduction. *IBM Journal of Research and Development*, 1(3):223–231, 1957.

[4] Supriyo Datta. *Quantum Transport Atom to Transistor*. Cambridge University Press, 2005.

[5] Mark Lundstrom and Changwook Jeong. *Near-Equilibrium Transport: Fundamentals And Applications*. World Scientific Publishing Co. Pte. Ltd., 2013.

[6] G. Nolas, J. Sharp, and H. Goldsmid. *Thermoelectrics: Basic Principles and New Materials Developments*. Springer, 2001.

[7] D M Rowe, editor. *Thermoelectrics Handbook Macro to Nano*. CRC Press, 2006.

[8] D.M. Rowe, editor. *Thermoelectrics and its Energy Harvesting*. Taylor & Francis Group, 2012.

[9] Christophe Goupil, Wolfgang Seifert, Knud Zabrocki, Eckart Müller, and G. Jeffrey Snyder. Thermodynamics of Thermoelectric Phenomena and Applications. *Entropy*, 13:1481–1516, 2011.

[10] Herbert B. Callen. The Application of Onsager's Reciprocal Relations to Thermoelectric, Thermomagnetic, and Galvanomagnetic Effects. *Physical Review*, 73(11):1349–1358, 1948.

[11] Lars Onsager. Reciprocal Relations in Irreversible Processes. I. *Physical Review*, 37:405–426, 1931.

[12] Yuri G. Gurevich, O. Yu Titov, G. N. Logvinov, and O.I. Lyubimov. Nature of thermopower in bipolar semiconductors. *Physical Review B*, 51(11):6999–7004, 1995.

[13] Yu. G. Gurevich and J. E. Velazquez-Perez. The role of non-equilibrium charge carriers in thermoelectric cooling. *Journal of Applied Physics*, 114:033704, 2013.

[14] Igor Lashkevych and Yury G. Gurevich. Boundary Conditions for Thermoelectric Cooling in pn Junction. *International Journal of Thermophysics*, 32:1086–1097, 2011.

[15] Igor Lashkevych, Carlos Cortes, and Yuri G. Gurevich. Physics of thermoelectric cooling: Alternative approach. *Journal of Applied Physics*, 105(5):053706, 2009.

[16] Yu G Gurevich and G N Logvinov. Physics of thermoelectric cooling. *Semiconductor Science and Technology*, 20:R57–R64, 2005.

[17] O.Yu. Titov, G. Gonzalez de la Cruz, G.N. Logvinov, and Yu.G. Gurevich. New Physical Point of View on the Peltier Effect. In *Proceedings ICT '97. XVI International Conference on Thermoelectrics, 1997.*, pages 661–663, 1997.

[18] R. N. Hall. An Analysis of the Performance of Thermoelectric Devices Made From Long-Lifetime Semiconductors. *Solid-State Electronics*, 2:115–122, 1961.

[19] W. Murray Bullis. Minority Carrier Thermoelectric Cooling. *Journal of Applied Physics*, 34:1648, 1963.

[20] K. Pipe, R. Ram, and A. Shakouri. Bias-dependent Peltier coefficient and internal cooling in bipolar devices. *Physical Review B*, 66:125316, 2002.

[21] G. Dousmanis, C. Mueller, H. Nelson, and K. Petzinger. Evidence of Refrigerating Action by Means of Photon Emission in Semiconductor Diodes. *Physical Review*, 133(1A):A316–A318, 1964.

[22] K.P. Pipe, R.J. Ram, and A. Shakouri. Internal cooling in a semiconductor laser diode. *IEEE Photonics Technology Letters*, 14(4):453–455, 2002.

[23] Osamu Yamashita. Internal cooling efficiency of a junction diode. *Applied Physics A*, 104:551–558, 2011.

[24] Edmund Altenkirch. Über den Nutzeffekt der Thermosäule. *Physikalische Zeitschrift*, 10:560, 1909.

[25] E.K. Vedernikov, M.V., Iordanishvili. A . F . Ioffe and Origin of Modern Semiconductor Thermoelectric Energy Conversion. *Conference onThermoelectrics, 1998. Proceedings ICT 98. XVII International*, pages 37–42, 1998.

[26] A.F. Ioffe and L.S. Stilbans. Physical problems of thermoelectricity. *Reports on Progress in Physics*, 22:169, 1959.

[27] Christopher J Vineis, Ali Shakouri, Arun Majumdar, and Mercouri G Kanatzidis. Nanostructured thermoelectrics: big efficiency gains from small features. *Advanced materials*, 22:3970–3980, 2010.

[28] A. J. Minnich, M. S. Dresselhaus, Z. F. Ren, and G. Chen. Bulk nanostructured thermoelectric materials: current research and future prospects. *Energy & Environmental Science*, 2:466–479, 2009.

[29] Gabi Schierning. Silicon nanostructures for thermoelectric devices: A review of the current state of the art. *Physica Status Solidi (a)*, pages 1–15, 2014.

[30] G Jeffrey Snyder and Eric S Toberer. Complex thermoelectric materials. *Nature materials*, 7:105–114, 2008.

[31] M.L. Olsen, E.L. Warren, P.A. Parilla, E.S. Toberer, C.E. Kennedy, G.J. Snyder, S.A. Firdosy, B. Nesmith, A. Zakutayev, A. Goodrich, C.S. Turchi, J. Netter, M.H. Gray, P.F. Ndione, R. Tirawat, L.L. Baranowski, A. Gray, and D.S. Ginley. A High-temperature, High-efficiency Solar Thermoelectric Generator Prototype. *Energy Procedia*, 49:1460–1469, 2014.

[32] C. Suter, Z.R. Jovanovic, and A. Steinfeld. A 1kWe thermoelectric stack for geothermal power generation Modeling and geometrical optimization. *Applied Energy*, 99:379–385, 2012.

[33] S A Omer and D G Infield. Design optimization of thermoelectric devices for solar power generation. *Solar Energy Materials & Solar Cells*, 53:67–82, 1998.

[34] Benjamin David, Julien Ramousse, and Lingai Luo. Optimization of thermoelectric heat pumps by operating condition management and heat exchanger design. *Energy Conversion and Management*, 60:125–133, 2012.

[35] P.M. Mayer and R.J. Ram. Optimization of Heat Sink Limited Thermoelectric Generators. *Nanoscale and Microscale Thermophysical Engineering*, 10:143–155, 2006.

[36] V. Kessler, M. Dehnen, R. Chavez, M. Engenhorst, J. Stoetzel, N. Petermann, K. Hesse, T. Huelser, M. Spree, G. Schierning, and R. Schmechel. Electrical Contact Resistance of Electroless Nickel to Nanocrystalline Silicon and the Fabrication of a Thermoelectric Generator. In *Materials Research Society Vol. 1553*, volume 1553, 2013.

[37] Frédéric J. Lesage and Nicolas Pagé-Potvin. Experimental analysis of peak power output of a thermoelectric liquid-to-liquid generator under an increasing electrical load resistance. *Energy Conversion and Management*, 66:98–105, 2013.

[38] Y. Apertet, H. Ouerdane, C. Goupil, and Ph. Lecoeur. Influence of thermal environment on optimal working conditions of thermoelectric generators. *Journal of Applied Physics*, 116:144901, 2014.

[39] Y. Apertet, H. Ouerdane, O. Glavatskaya, C. Goupil, and P. Lecoeur. Optimal working conditions for thermoelectric generators with realistic thermal coupling. *EPL (Europhysics Letters)*, 97:28001, 2012.

[40] A. Rezania, L.a. Rosendahl, and H. Yin. Parametric optimization of thermoelectric elements footprint for maximum power generation. *Journal of Power Sources*, 255:151–156, 2014.

[41] Kazuaki Yazawa and Ali Shakouri. Cost-efficiency trade-off and the design of thermoelectric power generators. *Environmental science & technology*, 45:7548–7553, 2011.

[42] Pablo Camacho-Medina, Miguel Olivares-Robles, Alexander Vargas-Almeida, and Francisco Solorio-Ordaz. Maximum Power of Thermally and Electrically Coupled Thermoelectric Generators. *Entropy*, 16:2890–2903, 2014.

[43] Alexander Vargas-Almeida, Miguel Olivares-Robles, and Pablo Camacho-Medina. Thermoelectric System in Different Thermal and Electrical Configurations: Its Impact in the Figure of Merit. *Entropy*, 15:2162–2180, 2013.

[44] Xiao Yan, Giri Joshi, Weishu Liu, Yucheng Lan, Hui Wang, Sangyeop Lee, J W Simonson, S J Poon, T M Tritt, Gang Chen, and Z F Ren. Enhanced thermoelectric figure of merit of p-type half-Heuslers. *Nano letters*, 11:556–560, 2011.

[45] Giri Joshi, Xiao Yan, Hengzhi Wang, Weishu Liu, Gang Chen, and Zhifeng Ren. Enhancement in Thermoelectric Figure-Of-Merit of an N-Type Half-Heusler Compound by the Nanocomposite Approach. *Advanced Energy Materials*, 1:643–647, 2011.

[46] Akram I Boukai, Yuri Bunimovich, Jamil Tahir-Kheli, Jen-Kan Yu, William a Goddard, and James R Heath. Silicon nanowires as efficient thermoelectric materials. *Nature*, 451:168–171, 2008.

[47] Allon I Hochbaum, Renkun Chen, Raul Diaz Delgado, Wenjie Liang, Erik C Garnett, Mark Najarian, Arun Majumdar, and Peidong Yang. Enhanced thermoelectric performance of rough silicon nanowires. *Nature*, 451(7175):163–7, 2008.

[48] Y Li, K Buddharaju, N Singh, G Q Lo, and S J Lee. Chip-Level Thermoelectric Power Generators Based on High-Density Silicon Nanowire Array Prepared With Top-Down CMOS Technology. *IEEE Electronic Device Letters*, 32(5):674–676, 2011.

[49] Victor Kessler, Devendraprakash Gautam, Tim Hülser, Mathias Spree, Ralf Theissmann, Markus Winterer, Hartmut Wiggers, Gabi Schierning, and Roland Schmechel. Thermoelectric Properties of Nanocrystalline Silicon from a Scaled-Up Synthesis Plant. *Advanced Engineering Materials*, pages 379–385, 2012.

[50] Sabah K. Bux, Richard G. Blair, Pawan K. Gogna, Hohyun Lee, Gang Chen, Mildred S. Dresselhaus, Richard B. Kaner, and Jean-Pierre Fleurial. Nanostructured

Bulk Silicon as an Effective Thermoelectric Material. *Advanced Functional Materials*, 19:2445–2452, 2009.

[51] G. Schierning, R. Theissmann, N. Stein, N. Petermann, A. Becker, M. Engenhorst, V. Kessler, M. Geller, A. Beckel, H. Wiggers, and R. Schmechel. Role of oxygen on microstructure and thermoelectric properties of silicon nanocomposites. *Journal of Applied Physics*, 110:113515, 2011.

[52] Zahra Zamanipour, Xinghua Shi, Arash M. Dehkordi, Jerzy S. Krasinski, and Daryoosh Vashaee. The effect of synthesis parameters on transport properties of nanostructured bulk thermoelectric p-type silicon germanium alloy. *Physica Status Solidi (a)*, 209(10):2049–2058, 2012.

[53] X. W. Wang, H. Lee, Y. C. Lan, G. H. Zhu, G. Joshi, D. Z. Wang, J. Yang, a. J. Muto, M. Y. Tang, J. Klatsky, S. Song, M. S. Dresselhaus, G. Chen, and Z. F. Ren. Enhanced thermoelectric figure of merit in nanostructured n-type silicon germanium bulk alloy. *Applied Physics Letters*, 93(19):193121, 2008.

[54] V. Kessler, M. Dehnen, R. Chavez, M. Engenhorst, J. Stoetzel, N. Petermann, K. Hesse, T. Huelser, M. Spree, C. Stiewe, P. Ziolkowski, G. Schierning, and R. Schmechel. Fabrication of High-Temperature-Stable Thermoelectric Generator Modules Based on Nanocrystalline Silicon. *Journal of Electronic Materials*, 43(5):1389–1396, 2014.

[55] Yi Ma, Qing Hao, Bed Poudel, Yucheng Lan, Bo Yu, Dezhi Wang, Gang Chen, and Zhifeng Ren. Enhanced thermoelectric figure-of-merit in p-type nanostructured bismuth antimony tellurium alloys made from elemental chunks. *Nano letters*, 8(8):2580–2584, 2008.

[56] N Stein, N Petermann, R Theissmann, G Schierning, R Schmechel, and H Wiggers. Artificially nanostructured n-type SiGe bulk thermoelectrics through plasma enhanced growth of alloy nanoparticles from the gas phase. *Journal of Materials Research*, 26(15):1872–1878, 2011.

[57] Paothep Pichanusakorn and Prabhakar Bandaru. Nanostructured thermoelectrics. *Materials Science and Engineering: R: Reports*, 67(2-4):19–63, 2010.

[58] Jose M Borrego. Approximate Analysis of the Operation of Thermoelectric Generators with Temperature Dependent Parameters. *IEEE Transactions on Aerospace*, 2:4–9, 1964.

[59] Gao Min. ZT Measurements Under Large Temperature Differences. *Journal of Electronic Materials*, 39(9):1782–1785, 2010.

[60] Gao Min, D M Rowe, and K Kontostavlakis. Thermoelectric figure-of-merit under large temperature differences. *Journal of Physics D: Applied Physics*, 37(8):1301–1304, apr 2004.

[61] Gao Min and D M Rowe. A novel principle allowing rapid and accurate measurement of a dimensionless thermoelectric figure of merit. *Measurement Science and Technology*, 12(8):1261–1262, 2001.

[62] G. Snyder and Tristan Ursell. Thermoelectric Efficiency and Compatibility. *Physical Review Letters*, 91(14):148301, 2003.

[63] W. Seifert, E. Müller, and S. Walczak. Local optimization strategy based on first principles of thermoelectrics. *Physica Status Solidi (a)*, 205(12):2908–2918, 2008.

[64] Wolfgang Seifert, Knud Zabrocki, G. Jeffrey Snyder, and Eckhard Müller. The com-

patibility approach in the classical theory of thermoelectricity seen from the perspective of variational calculus. *Physica Status Solidi (a)*, 207(3):760–765, 2010.

[65] M Wagner, G Span, S Holzert, and T Grassert. Design Optimization of Large Area Si / SiGe Thermoelectric Generators EF-. In *International Conference on Simulation of Semiconductor Processes and Devices*, pages 397–400, 2006.

[66] M Wagner, G Span, S Holzer, and T Grasser. Thermoelectric power generation using large-area Si/SiGe pn-junctions with varying Ge content. *Semiconductor Science and Technology*, 22:S173–S176, 2007.

[67] G. Span, M. Wagner, S. Holzer, and T. Grasser. Thermoelectric Power Conversion using Generation of Electron-Hole Pairs in Large Area p-n Junctions. *2006 25th International Conference on Thermoelectrics*, pages 23–28, 2006.

[68] Gerhard Span, Martin Wagner, Tibor Grasser, and Lennart Holmgren. Miniaturized TEG with thermal generation of free carriers. *Rapid Research Letters*, 1(6):241–243, 2007.

[69] Sang Seok Kim, Shigeo Yamamoto, Tatsuhiko Aizawa, and Atsushi Yamamoto. Experimental and Theoretical Evaluation on Thermoelectricity for SPS Joined p-n Module in BiTe System. *Materials Transactions*, 46(7):1506–1513, 2005.

[70] T Kumpeerapun, V Kosalathip, H Scherrer, A Dauscher, W Onreabroy, and I Sripichai. Fabrication of p-n junctions of Bi-Sb-Te thermoelectric materials. pages 2–4, 2007.

[71] J.Y. Yang, T. Aizawa, A. Yamamoto, and T. Ohta. Effects of interface layer on thermoelectric properties of a pn junction prepared via the BMA-HP method. *Materials Science and Engineering: B*, 85:34–37, 2001.

[72] P. L. Hagelstein and Y. Kucherov. Enhanced figure of merit in thermal to electrical energy conversion using diode structures. *Applied Physics Letters*, 81(3):559–561, 2002.

[73] D. Fu, A. Levander, R. Zhang, J. Ager, and J. Wu. Electrothermally driven current vortices in inhomogeneous bipolar semiconductors. *Physical Review B*, 84:045205, 2011.

[74] Y. Apertet, H. Ouerdane, C. Goupil, and Ph. Lecoeur. Thermoelectric internal current loops inside inhomogeneous systems. *Physical Review B*, 85:033201, 2012.

[75] Sebastian Angst. *Ph.D. Thesis to be published*. PhD thesis, 2014.

[76] S.O. Kasap. *Principles of Electronic Materials and Devices*. Tata McGraw-Hill, 2007.

[77] S. Dongaonkar, J. D. Servaites, G. M. Ford, S. Loser, J. Moore, R. M. Gelfand, H. Mohseni, H. W. Hillhouse, R. Agrawal, M. a. Ratner, T. J. Marks, M. S. Lundstrom, and M. a. Alam. Universality of non-Ohmic shunt leakage in thin-film solar cells. *Journal of Applied Physics*, 108:124509, 2010.

[78] Simon M. Sze and Kwok Ng. *Physics of Semiconductor Devices*. Wiley-Interscience, 2006.

[79] Igor Lashkevych, Carlos Cortes, and Yuri G. Gurevich. Physics of thermoelectric cooling: Alternative approach. *Journal of Applied Physics*, 105:053706, 2009.

[80] Yury G. Gurevich, G.N. Logvinov, O.I. Lyubimov, and O.Yu. Titov. Thermopower and Thermal Transport in Metal-p-Type Semiconductor-Metal Structure. In *16th International Conference on Thermoelectrics.*, number 1 997, pages 476–480, 1997.

[81] L. Villegas-Lelovsky, G. González de la Cruz, and Yu.G. Gurevich. Electron and phonon thermal waves in semiconductors: the effect of carrier diffusion and recombination on the photoacoustic signal. *Thin Solid Films*, 433:371–374, 2003.

[82] Cronin B Vining. The Thermoelectric Process. In *Materials Research Society Symposium*, volume 478, pages 3–13, 1997.

[83] Xingkai Duan, Junyou Yang, Wei Zhong, Wei Zhu, Siqian Bao, and Xi'an Fan. Synthesis of Bi2Te3 nanopowders by vacuum arc plasma evaporation. *Powder Technology*, 172:63–66, 2007.

[84] T Tokiai, T Uesugi, M Nosaka, A Hirayama, K Ito, and K Koumoto. Thermoelectric properties of Mn-doped iron disilicide ceramics fabricated from radio-frequency plasma-treated fine powders. *Journal of Materials Science*, 32:3007–3011, 1997.

[85] F. Brochin, B. Lenoir, X. Devaux, R. Martin-Lopez, and H. Scherrer. Preparation and transport properties of polycrystalline Bi and BiSiO nanocomposites. *Journal of Applied Physics*, 88(6):3269, 2000.

[86] Nils Petermann, Niklas Stein, Gabi Schierning, Ralf Theissmann, Benedikt Stoib, Martin S Brandt, Christian Hecht, Christof Schulz, and Hartmut Wiggers. Plasma synthesis of nanostructures for improved thermoelectric properties. *Journal of Physics D: Applied Physics*, 44:174034, 2011.

[87] D Schwesig, G Schierning, R Theissmann, N Stein, N Petermann, H Wiggers, R Schmechel, and D E Wolf. From nanoparticles to nanocrystalline bulk: percolation effects in field assisted sintering of silicon nanoparticles. *Nanotechnology*, 22:135601, 2011.

[88] G. Schierning, R. Theissmann, H. Wiggers, D. Sudfeld, a. Ebbers, D. Franke, V. T.

Witusiewicz, and M. Apel. Microcrystalline silicon formation by silicon nanoparticles. *Journal of Applied Physics*, 103(8):084305, 2008.

[89] M. Meseth, P. Ziolkowski, G. Schierning, R. Theissmann, N. Petermann, H. Wiggers, N. Benson, and R. Schmechel. The realization of a pn-diode using only silicon nanoparticles. *Scripta Materialia*, 67:265–268, 2012.

[90] A Becker, G Schierning, R Theissmann, M Meseth, and N Benson. A sintered nanoparticle p-n junction observed by a Seebeck microscan. *Journal of Applied Physics*, 111(May):054320, 2012.

[91] A. Becker, S. Angst, A. Schmitz, M. Engenhorst, J. Stoetzel, D. Gautam, H. Wiggers, D. E. Wolf, G. Schierning, and R. Schmechel. The effect of Peltier heat during current activated densification. *Applied Physics Letters*, 101(1):013113, 2012.

[92] Martin Meseth, Bernd Christian Kunert, Lucas Bitzer, Frederik Kunze, Sebastian Meyer, Fabian Kiefer, Martin Dehnen, Hans Orthner, Nils Petermann, Malin Kummer, Hartmut Wiggers, Nils-Peter Harder, Niels Benson, and Roland Schmechel. Excimer laser doping using highly doped silicon nanoparticles. *Physica Status Solidi (a)*, 210(11):2456–2462, 2013.

[93] Martin Meseth, Kais Lamine, Martin Dehnen, Sven Kayser, Wolfgang Brock, Dennis Behrenberg, Hans Orthner, Anna Elsukova, Nils Hartmann, Hartmut Wiggers, Tim Hülser, Hermann Nienhaus, Niels Benson, and Roland Schmechel. Laser-doping of crystalline silicon substrates using doped silicon nanoparticles. *Thin Solid Films*, 548:437–442, 2013.

[94] F. Maculewicz. *Thermoelectric properties of laser crystallized silicon diodes for a thermoelectric concept using large area PN junctions.* Master thesis, University Duisburg Essen, 2013.

[95] Z. L. Liau and D. E. Mull. Wafer fusion: A novel technique for optoelectronic device fabrication and monolithic integration. *Applied Physics Letters*, 56(8):737, 1990.

[96] F. A. Kish, F. M. Steranka, D. C. DeFevere, D. A. Vanderwater, K. G. Park, C. P. Kuo, T. D. Osentowski, M. J. Peanasky, J. G. Yu, R. M. Fletcher, D. a. Steigerwald, M. G. Craford, and V. M. Robbins. Very high-efficiency semiconductor wafer-bonded transparent-substrate (AlGa)InP/GaP light-emitting diodes. *Applied Physics Letters*, 64(21):2839, 1994.

[97] F. Salomonsson, K. Streubel, J. Bentell, M. Hammar, D. Keiper, R. Westphalen, J. Piprek, L. Sagalowicz, a. Rudra, and J. Behrend. Wafer fused p-InP/p-GaAs heterojunctions. *Journal of Applied Physics*, 83(2):768, 1998.

[98] Dennis Albrecht. *Preparation and characterization of large area PN junctions for thermoelectric applications.* Bachelor thesis, University of Duisburg Essen, 2014.

[99] C. S. Pai, E. Cabreros, S. S. Lau, T. E. Seidel, and I. Suni. Rapid thermal annealing of Al-Si contacts. *Applied Physics Letters*, 46(7):652, 1985.

[100] L. A. Bitzer, M. Meseth, N. Benson, and R. Schmechel. A new adaptive light beam focusing principle for scanning light stimulation systems. *The Review of scientific instruments*, 84:023707, 2013.

[101] Luis-David Patiño Lopez, Stefan Dilhaire, Stéphane Grauby, M Amine Salhi, Younès Ezzahri, Wilfrid Claeys, and Jean-Christophe Batsale. Characterization of thermoelectric devices by laser induced Seebeck electromotive force (LIS-EMF) measurement. *Journal of Physics D: Applied Physics*, 38:1489–1497, 2005.

[102] Stefan Dilhaire, Amine Salhi, Stéphane Grauby, and Wilfrid Claeys. Laser Seebeck Effect Imaging (SEI) and Peltier Effect Imaging (PEI): complementary investigation methods. *Microelectronics Reliability*, 43(9-11):1609–1613, 2003.

[103] Martin A Green. Solar Energy Materials & Solar Cells Self-consistent optical parameters of intrinsic silicon at 300 K including temperature coefficients. *Solar Energy Materials & Solar Cells*, 92:1305–1310, 2008.

[104] Peter J. Collings. Simple measurement of the band gap in silicon and germanium. *American Journal of Physics*, 48(3):197–199, 1980.

[105] R Chavez, A Becker, M Bartel, V Kessler, G Schierning, and R Schmechel. Note : High resolution alternating current / direct current Harman technique. *Review of Scientific Instruments*, 84:106106, 2013.

[106] T. C. Harman. Special Techniques for Measurement of Thermoelectric Properties. *Journal of Applied Physics*, 29(9):1373, 1958.

[107] Richard J. Buist. A New Method For Testing Thermoelectric Materials and Devices. *XI International Conference on Thermoelectrics*, 1992.

[108] Gao Min. Principle of determining thermoelectric properties based on IV curves. *Measurement Science and Technology*, 25:085009, 2014.

[109] R. Amatya, P. M. Mayer, and R. J. Ram. High temperature Z-meter setup for characterizing thermoelectric material under large temperature gradient. *The Review of scientific instruments*, 83:075117, 2012.

[110] J. Martin, T. Tritt, and C. Uher. High temperature Seebeck coefficient metrology. *Journal of Applied Physics*, 108(12):121101, 2010.

[111] J. Martin. Apparatus for the high temperature measurement of the Seebeck coefficient in thermoelectric materials. *The Review of scientific instruments*, 83:065101, 2012.

[112] C. Wood, a. Chmielewski, and D. Zoltan. Measurement of Seebeck coefficient using a large thermal gradient. *Review of Scientific Instruments*, 59(6):951, 1988.

[113] A.T. Burkov, A Heinrich, P. P. Konstantinov, T. Nakama, and K. Yagasaki. Experimental set-up for thermopower and resistivity measurements at 100 to 1300 K. *Measurement Science and Technology*, 12:264–272, 2001.

[114] Zhenhua Zhou and Ctirad Uher. Apparatus for Seebeck coefficient and electrical resistivity measurements of bulk thermoelectric materials at high temperature. *Review of Scientific Instruments*, 76(2):023901, 2005.

[115] C. Wood, D. Zoltan, and G. Stapfer. Measurement of Seebeck coefficient using a light pulse. *Review of Scientific Instruments*, 56(5):719, 1985.

[116] V. Ponnambalam, S. Lindsey, N. S. Hickman, and Terry M. Tritt. Sample probe to measure resistivity and thermopower in the temperature range of 300 to 1000 K. *Review of Scientific Instruments*, 77(7):073904, 2006.

[117] Shiho Iwanaga, Eric S Toberer, Aaron LaLonde, and G Jeffrey Snyder. A high temperature apparatus for measurement of the Seebeck coefficient. *The Review of scientific instruments*, 82:063905, 2011.

[118] Z. Trousil. Bulk Photo-Voltaic Phenomenon. *Czech Journal of Physics*, 6:96–98, 1956.

[119] Ho-Ki Lyeo, A. A. Khajetoorians, Li Shi, Kevin P Pipe, Rajeev J Ram, Ali Shakouri, and C K Shih. Profiling the thermoelectric power of semiconductor junctions with nanometer resolution. *Science*, 303:816–8, 2004.

[120] Robert Lechner, Andre R. Stegner, Rui N. Pereira, Roland Dietmueller, Martin S. Brandt, Andre Ebbers, Martin Trocha, Hartmut Wiggers, and Martin Stutzmann.

Electronic properties of doped silicon nanocrystal films. *Journal of Applied Physics*, 104:053701, 2008.

[121] D. Scansen and S.O. Kasap. Excess noise, gain and dark current in Ge avalanche diodes. *Canadian Journal of Physics*, 70:1070, 1992.

[122] M. A. Rafiq, Y. Tsuchiya, H. Mizuta, S. Oda, Shigeyasu Uno, Z. a. K. Durrani, and W. I. Milne. Charge injection and trapping in silicon nanocrystals. *Applied Physics Letters*, 87(18):182101, 2005.

[123] T A Burr, A A Seraphin, E Werwa, and K D Kolenbrander. Carrier transport in thin films of silicon nanoparticles. *Physical Review B*, 56(8):4818–4824, 1997.

[124] Fereydoon Namavar, H. Paul Maruska, and Nader M. Kalkhoran. Visible electroluminescence from porous silicon np heterojunction diodes. *Applied Physics Letters*, 60(20):2514, 1992.

[125] Victor Kessler. *Hochtemperaturstabile thermoelektrische Generatoren auf Basis von nanokristallinem Silizium*. Ph.d. thesis., University Duisburg Essen, 2014.

[126] Kilian Bartholomé, Benjamin Balke, Daniel Zuckermann, Martin Köhne, Michael Müller, Karina Tarantik, and Jan König. Thermoelectric Modules Based on Half-Heusler Materials Produced in Large Quantities. *Journal of Electronic Materials*, 43(6):1775–1781, 2014.

[127] Sascha Populoh, Oliver Brunko, Krzysztof Galazka, Wenjie Xie, and Anke Weidenkaff. Half-Heusler (TiZrHf)NiSn Unileg Module with High Powder Density. *Materials*, 6:1326–1332, 2013.

[128] C. Lertsatitthanakorn. Electrical performance analysis and economic evaluation of

combined biomass cook stove thermoelectric (BITE) generator. *Bioresource technology*, 98:1670–4, 2007.

[129] Lauryn L. Baranowski, G. Jeffrey Snyder, and Eric S. Toberer. Concentrated solar thermoelectric generators. *Energy & Environmental Science*, 5(10):9055, 2012.

[130] Daniel Kraemer, Bed Poudel, Hsien-Ping Feng, J Christopher Caylor, Bo Yu, Xiao Yan, Yi Ma, Xiaowei Wang, Dezhi Wang, Andrew Muto, Kenneth McEnaney, Matteo Chiesa, Zhifeng Ren, and Gang Chen. High-performance flat-panel solar thermoelectric generators with high thermal concentration. *Nature materials*, 10:532–8, 2011.

[131] M.a. Karri, E.F. Thacher, and B.T. Helenbrook. Exhaust energy conversion by thermoelectric generator: Two case studies. *Energy Conversion and Management*, 52:1596–1611, 2011.