RADIATION DAMAGE EFFECTS IN CHARGE COUPLED DEVICES

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Abstract

The effects of Sr^{90} beta radiation and Co^{60} gamma radiation on the operation of EEV buried channel charge coupled devices (CCDs) have been studied. This work was instigated by the need to qualify CCDs for the SLD vertex detector. However, the work is also relevant to other small signal, low noise applications. The results of the batch qualification are presented and the data base of ionising radiation effects on EEV CCDs has been extended to include the effects of irradiation whilst clocking at 180K.

Particular attention has been aimed at investigating the charge transfer degradation due to low levels of bulk defects. The measured energy level, capture cross section and introduction rate of the main radiation induced defect agrees well with published results for the Si-E centre. Annealing studies are also presented. A model for the charge transfer degradation is proposed. This includes the effects of temperature, readout rate, signal density and irradiation type and energy.

Observations are also presented on the effect of irradiation on the noise characteristics of the single stage output circuit. For low noise applications the output is run in buried channel mode. In this mode the increase in noise is dominated by the change in the operating point of the output MOSFET.

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Foreword

This thesis presents the results of an investigation into the effects of radiation on buried channel charge coupled devices (CCDs).

The work described was carried out over a three year period at Brunel University, as part of a CASE award from EEV, Chelmsford. The main aim was to contribute to the understanding of radiation damage of CCDs. Particular attention was paid to low signal applications such as X-ray astronomy and charged particle detection.

The work was initiated by T. Roy and S.J. Watts to establish the suitability of the EEV UT101 CCD for the SLD vertex detector which is now installed at the Stanford Linear Collider [1]. This work was continued by the author to investigate the batch to batch variation in the radiation hardness of the devices as part of the batch qualification. This was necessary as 480 devices are employed in the detector. These had to be procured from several different batches. Observations were also made on the effect of clocking during irradiation. The result of thinning the gate oxide of the CCD was investigated as a precursor to the development of a radiation hard CCD by EEV.

It soon became clear that a detailed understanding of the effects of radiation induced bulk defects on the charge transfer efficiency was lacking from the literature, especially for low signal levels encountered in X-ray astronomy and particle physics. The consequence of very low levels of bulk defects was investigated by the author and a model for the degradation established. The results of this investigation are presented in this thesis. A general model for the charge transfer degradation has been lacking in the past but is necessary for the systems designer to establish the effect of a radiation environment on the CCD, without lengthy and expensive tests. For example, the space environment consists of a wide spectrum of damaging particles. This spectrum can be calculated and inserted into the model to obtain the effective mission lifetime. Such a prediction cannot be made by simple device qualification as the complex space environment cannot be realistically mimicked here on earth. Some of the results obtained for this thesis have been published in references [2] and [3].

Observations are also presented on the effect of beta radiation on the noise performance of the output circuit. A detailed investigation on the effect of radiation on the output circuit has not before been presented in the literature. To the author's

knowledge there has also been no reported observation on the effect of beta radiation on the noise from buried channel MOSFETs, especially as a function of temperature.

Most irradiations were carried out using a convenient Sr^{90} beta source. The 'standard' source of ionising radiation used by most workers is the Co^{60} gamma source. The equivalence of the two sources was checked by carrying out additional tests on Co^{60} irradiated devices. The results of these tests are presented.

Chapter one of this thesis describes the operation of a typical charge coupled device and in particular the EEV UT101 and UT102 devices used in the investigations. The relevant radiation effects in semiconductor devices are covered. The generally excepted picture of radiation damage in CCDs is presented. Typical applications of CCDs utilising low signal levels in a radiation environment are discussed. Chapter two gives the general experimental procedure used for the radiation studies. This includes the operation of the CCD and irradiation details. The subject of dosimetry is covered. The subsequent four chapters give the details and results of the investigations undertaken together with relevant theory that has not been given in chapter one.

The final chapters provide a summary of the results and conclusions. The subject of radiation effects in CCDs is a very large one and suggestions for further investigation are given.

Relevant references are given at the end of the chapter to which they refer.

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1) T. Roy, S.J. Watts and D. Wright, "Radiation effects on imaging charge coupled devices", Nucl. Inst. Meth., A275, 545-557, 1989.

2) P. Acton, G. Agnew, R. Cotton, S. Hedges, A.K. McKemey, M. Robbins, T. Roy, S.J. Watts, C.J.S. Damerell, R.L. English, A.R. Gillman, D. Su and F.J. Wickens, "Future potential of charge coupled devices as detectors of ionising radiation", Nucl. Inst. Meth., A305, 504-511, 1991.

3) M.S. Robbins, T. Roy and S.J. Watts, "Degradation of the transfer efficiency of a buried channel charge coupled device due to radiation damage by a beta source", Proceedings of the First European Conference on Radiation and its Effects on Devices and Systems, 327-332, 1991. To be published in IEEE Trans. Nucl. Sci.

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I gratefully acknowledge the valuable discussions with fellow members of the European Working group on the Radiation Damage of CCDs. In particular I would like to thank Dr. Gordon Hopkinson from SIRA and Professor Andrew Holmes-Siedle from BNF-Fulmer. I would especially like to thank Andrew for a valuable discussion on the train from Newcastle.

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Abbreviations and Acronyms

ADC	Analogue to Digital Converter
BCCD	Buried Channel Charge Coupled Device
CAMAC	Computer Automated Measurement and Control standard
CASE	Cooperative Award in Science and Engineering
CCD	Charge Coupled Device
CDS	Correlated Double Sampling
CERN	European Centre for Particle Physics
CPE	Charged Particle Equilibrium
CTE	Charge Transfer Efficiency
CTI	Charge Transfer Inefficiency
DLTS	Deep Level Transient Spectroscopy
DSI	Dual Slope Integration
ECL	Emitter Coupled Logic
EEV	English Electric Valve Company, Waterhouse Lane, Chelmsford, Essex, England.
EPER	Extended Pixel Edge Response
ESA	European Space Agency
ESR	Electron Spin Resonance
FET	Field Effect Transistor
LET	Linear Energy Transfer
MIP	Minimum Ionising Particle
MNOS	Metal Nitride Oxide Silicon

MOS	Metal Oxide Silicon
MOSFET	Metal Oxide Silicon Field Effect Transistor
MPP	Multipin Phase
NIEL	Non Ionising Energy Loss
NIM	Nuclear Instrument Module standard
PKA	Primary Knock-on Atom
RTS	Random Telegraph Signal
SCCD	Surface Channel Charge Coupled Device
SILEX	Semiconductor Intersatellite Laser Experiment
SLAC	Stanford Linear Accelerator Centre
SRH	Shockley Read Hall
TV	Television
(=/-)	Transition from doubly negative charge state to singly negative charge state
(-/0)	Transition from singly negative charge state a neutral charge state

CHAPTER ONE

Introduction

1.1. Theory of CCD Operation

This section describes the operation of a charge coupled device. The basic ideas of device operation are presented by first looking at surface channel MOS structures and CCDs. These ideas are extended to include the operation of the buried channel CCD. The buried channel CCD is the device type employed in work described in subsequent chapters.

1.1.1. The CCD Concept

In essence a charge coupled device (CCD) consists of a closely spaced array of electrodes on a continuous insulator layer that covers the semiconductor substrate [1,2]. This forms an array of MOS capacitors. The signal is represented by a charge packet. Under the correct operating conditions the position of the charge packet can be controlled by potentials applied to the gates of the capacitors.

The basic element of a CCD is a MOS capacitor operated in deep depletion. When a voltage is applied to the gate of a MOS capacitor the energy bands in the semiconductor bend. If the applied field is in a direction so as to repel majority charge carriers from the silicon-insulator interface the interface will become depleted of majority carriers. The band diagram for a MOS capacitor on a p-type substrate is shown in Figure 1.1 a). Here the majority charge carriers are holes. The electron potential at the interface is lower than in the bulk semiconductor by an amount Φ_{so}

and so a potential well of depth Φ_{so} is formed at the semiconductor-insulator interface under the electrode. This is not an equilibrium situation and electrons will tend to fill this potential well by thermal generation. Electrons will continue to collect at the interface until the strong inversion condition at the surface is reached. At this point the surface potential will be approximately twice the bulk potential of the semiconductor. This 'filling' takes a finite time and is known as the storage time for the MOS capacitor (typically around 1 second at room temperature, increasing exponentially as the temperature is reduced). The band diagram for a partially full well is shown in Figure 1.1 b). Electrons that are intentionally injected from an input diffusion or by optical means etc. will collect under the electrode and

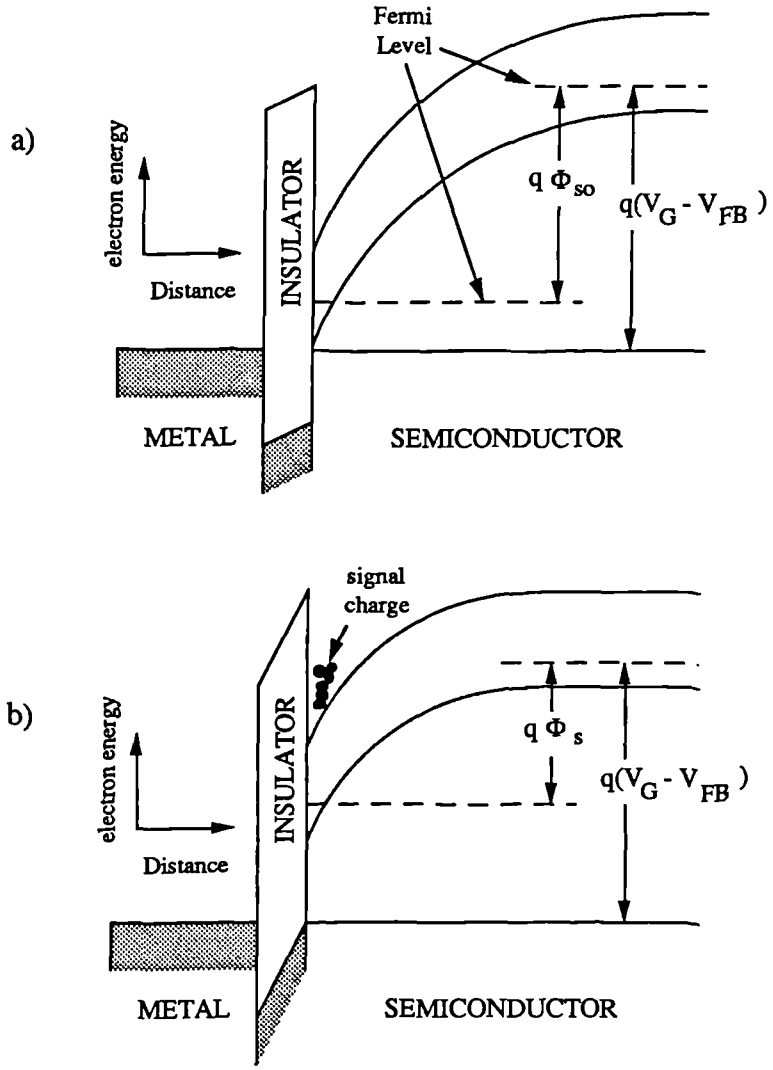

Figure 1.1 The Energy-band diagrams for a surface channel MOS capacitor. a) Deep depletion. b) Well partially filled with signal charge.

constitute signal charge above a thermally generated background.

Consider the MOS capacitor shown in Figure 1.1. The potential applied to the electrode will appear across the insulator and the substrate. Therefore the relation between the electrode voltage, V_G, and the potential at the interface, Φ_S, is obtained from

$$V_G - V_{FB} = \Phi_S + V_{ox} \tag{1.1}$$

where V_{FB} is the flat band voltage and V_{ox} is the potential across the oxide. However

$$V_{ox} = (\text{mobile charge density} + \text{fixed charge density})/C_o$$

$$= (q\,N + q\,N_A\,W)/C_o \tag{1.2}$$

where C_o is the capacitance per unit area of the insulator, q is the electronic charge, N is the number of mobile electrons per unit area and N_A is the acceptor density in the semiconductor. The depletion layer width, W, can be obtained by solving the Poisson equation using the depletion approximation and is given by

$$W = \sqrt{(2\varepsilon_S\Phi_S / qN_A)} \tag{1.3}$$

where ε_S is the permittivity of the semiconductor. Combining (1.1), (1.2) and (1.3) and solving for Φ_S gives

$$\Phi_S = V_g - \frac{qN}{C_o} - \frac{qN_A\varepsilon_S}{C_o^2}\left(\left(1+\frac{2C_o(C_oV_g - Nq)}{qN_A\varepsilon_S}\right)^{1/2}-1\right) \tag{1.4}$$

where $V_g = V_G - V_{FB}$. Thus the potential at the surface of the MOS capacitor in deep depletion is controlled by the voltage applied to the electrode, the oxide capacitance and the dopant density of the substrate, usually silicon. If an array of closely spaced MOS capacitors is constructed then electrons will collect under the electrode with the highest potential. A schematic of a three bit, three phase, n-channel CCD is shown in Figure 1.2 a). The nine MOS capacitors form the main part of the CCD. The input gate and drain and the output gate and drain are the input and output structures that injects and detects the charge packets. The effect of gate voltage on the surface potential for an empty well is illustrated in Figure 1.2 b).

From equation (1.4) it can be seen that an increase in the substrate doping or a decrease in insulator capacitance will give a lower potential at the surface. This can be utilised as method of confining charge to a well defined channel in the CCD as

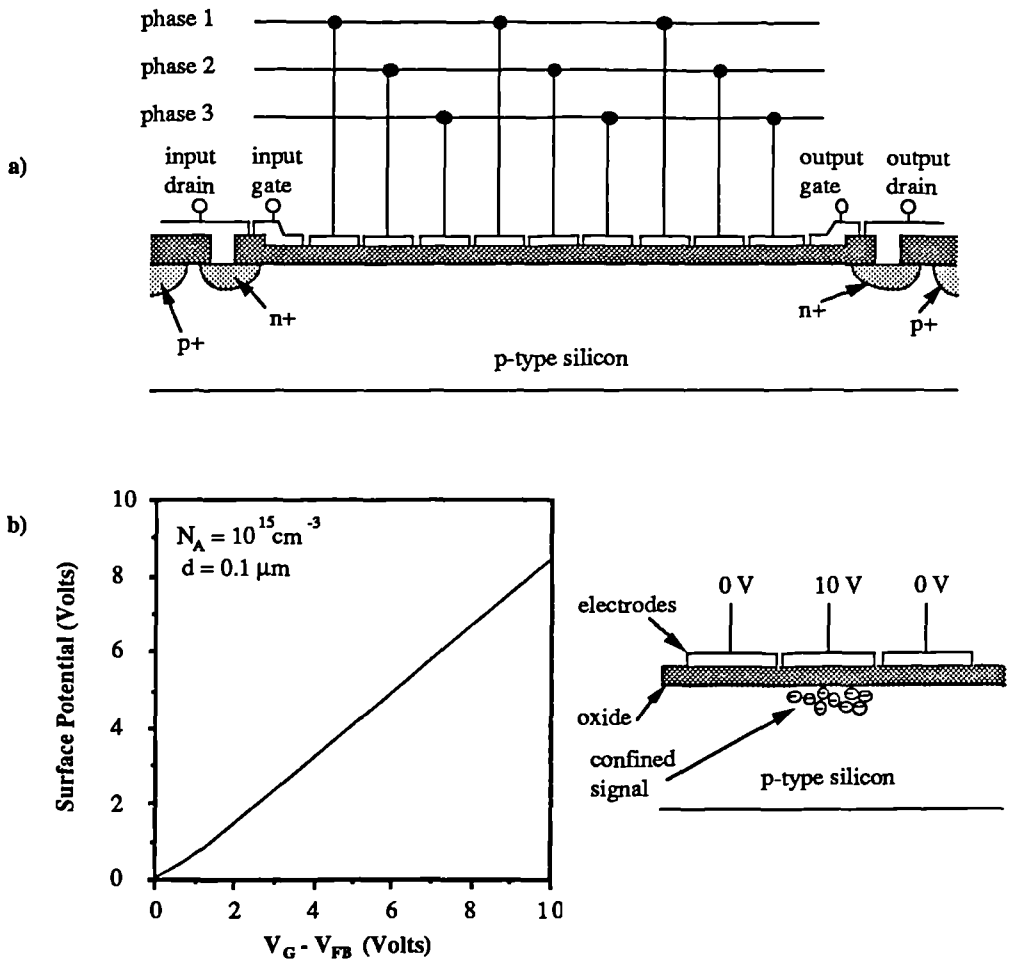

Figure 1.2. A schematic of a 3 phase silicon CCD showing how charge is confined under the electrode with the highest potential.

shown in Figure 1.3. Here the relation between surface potential for zero signal charge for a silicon structure is shown as a function of both oxide thickness and substrate doping. Two typical structures used for forming the so called "channel stops" are also shown.

Charge can be moved through the device by applying a sequence of pulses to the electrodes. For a uniform substrate and insulator the minimum number of phases required for the charge to move in one direction is three. A typical charge transfer sequence is shown in Figure 1.4. Charge is initially collected under the gates with the highest potential. When the charge is to be transferred, phase 1 goes low as phase 2 is pulsed high. The electrons will then flow to the next gate. Phase 2 then goes low as phase 3 is set high. This sequence is continued until the charge packet is moved out of the device.

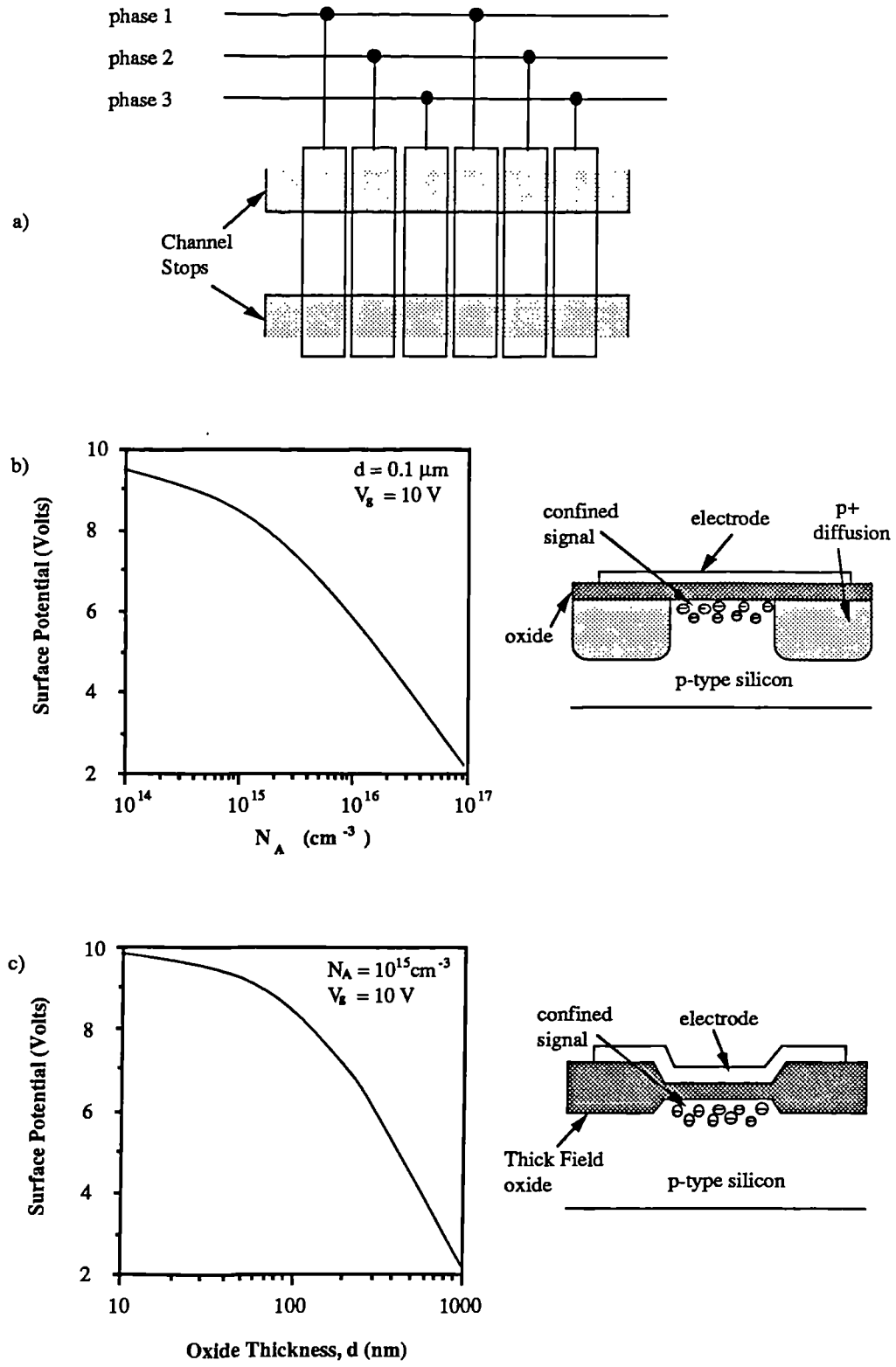

Figure 1.3. Methods for confining the signal to a well defined channel. The oxide capacitance per unit area is given by $C_o = \varepsilon_o/d$ where ε_o is the permittivity of the oxide.

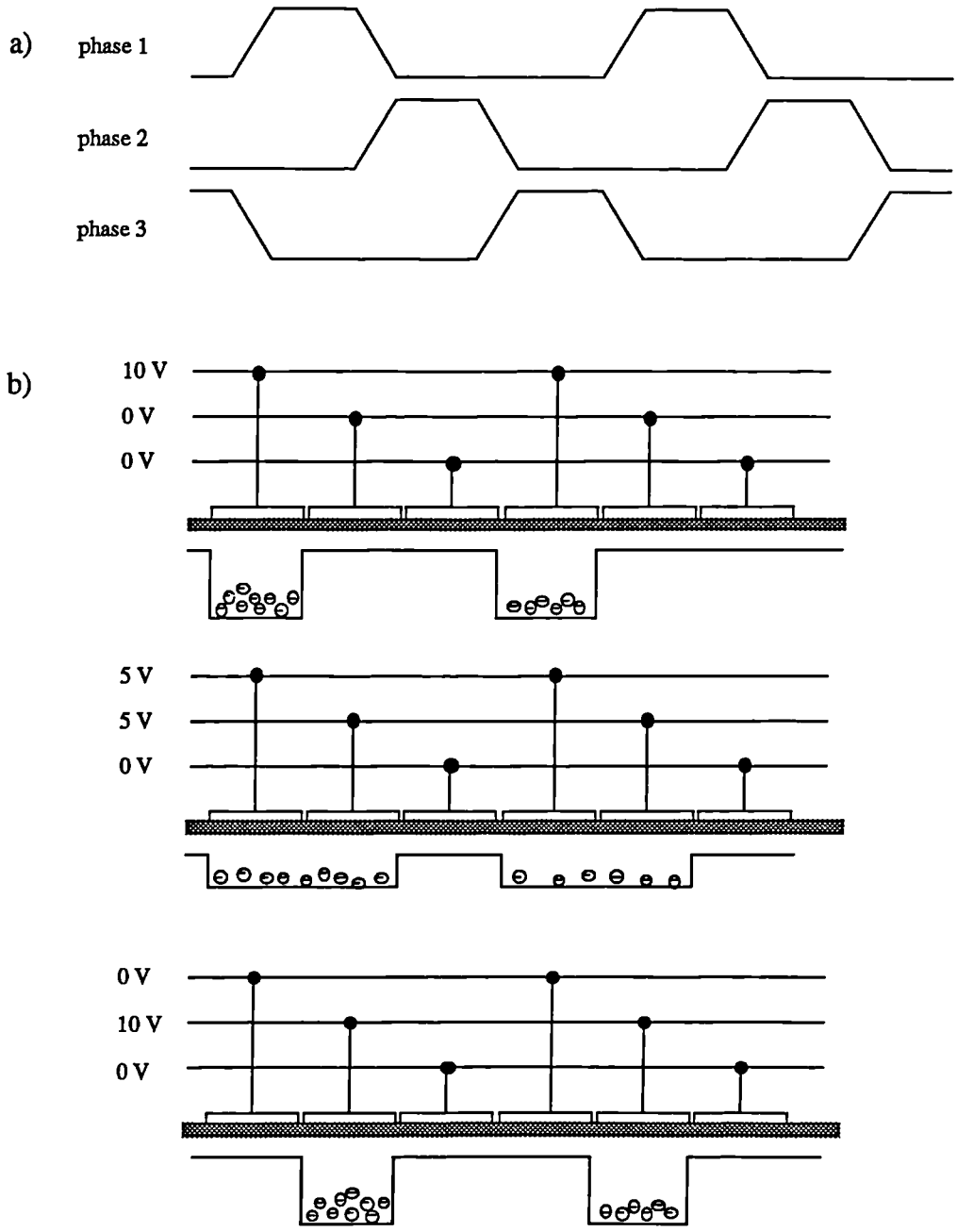

Figure 1.4. The transfer of charge through the CCD. a) A typical drive pulse sequence. b) A schematic of the charge transfer from one electrode to the next.

1.1.2. A CCD Array

A CCD array can be formed by dividing long strips of electrode with channel stops to prevent lateral spreading of charge along the length of the electrode. Thus a structure can be formed which is made up of a two dimensional array of potential wells. If an optical image, for example, is formed on this structure then any photogenerated electrons will be collected in a potential well at, or near their point of creation. Therefore two dimensional optical information can be converted into two dimensional electrical information.

Figure 1.5 shows a typical 3-phase imaging array. The array is constructed by laying down horizontal electrodes that are divided vertically by channel stops. A picture element (pixel) is formed from three electrodes bounded by two channel

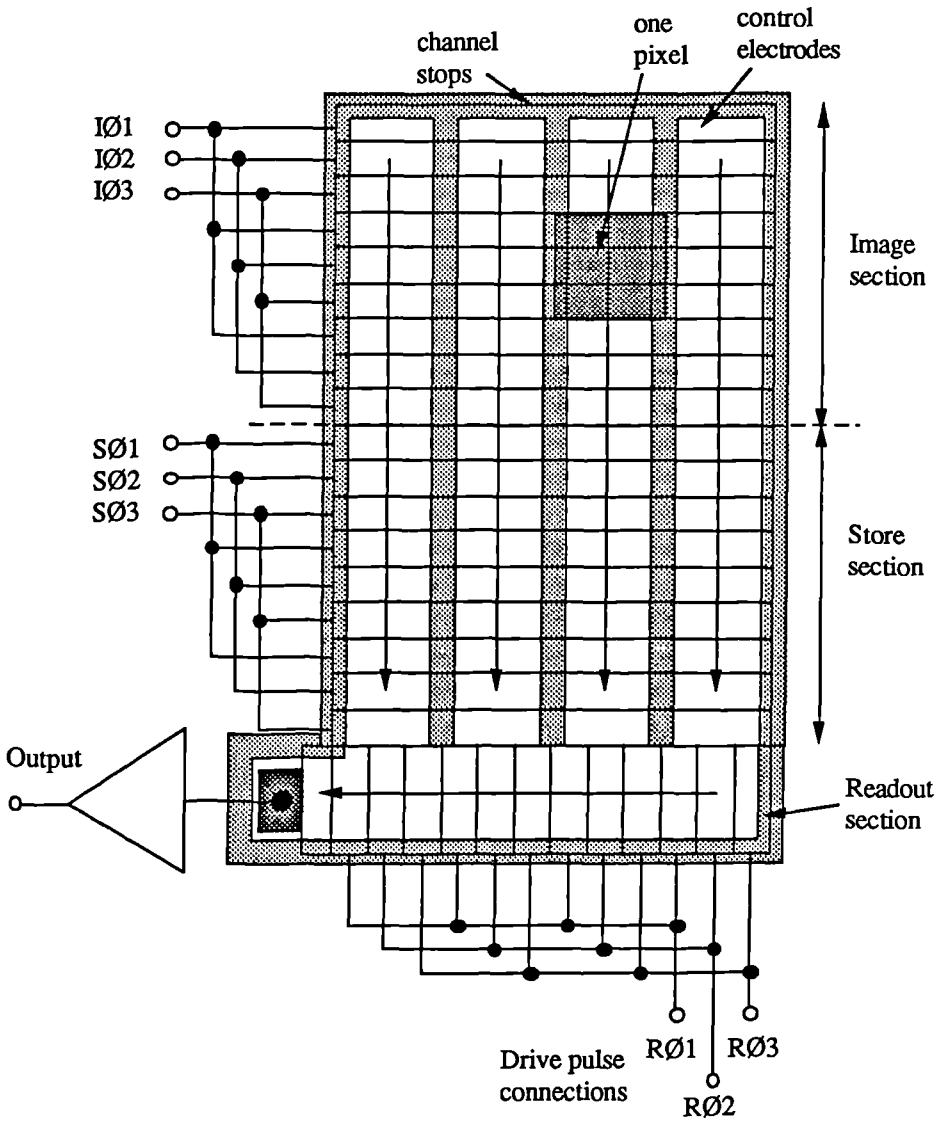

Figure 1.5. A schematic of a frame transfer CCD.

stops. The CCD illustrated is known as a frame transfer device.

The electrodes are grouped to form two regions, the image section and the store. A linear CCD array runs horizontally at the bottom of the device to form a readout register. Both the store and readout sections are shielded from light by a metal layer on or just above the device. The optical image is formed on the image section of the device and the photogenerated charge is collected under the set of electrodes that have been positively biased. The time for collection is known as the integration time and is typically 20 ms for standard television applications. After this time the charge is rapidly transferred from the image section to the store region by clocking the phases in both sections. This transfer takes around 1.6 ms. The charge is then transferred one line at a time to the readout register. One phase of the readout register is held high so that the horizontal information is preserved after the transfer has taken place. When a line has been transferred to the readout register the register is clocked to move the charge, one pixel at a time, to the output circuit where the level of charge is detected. The transfer process thus converts an area distribution of charge signal into a line format for sequential readout. The readout of each line takes 52 μs for TV imaging. While the readout is taking place a second image is being collected ready to be transferred once the readout of the first image has been completed. During the frame transfer light is still incident on the image area and so the image is slightly smeared during the transfer process. This smearing is dependent on the rate at which the transfer takes place.

If the photogenerated charge is in excess of the maximum that can be stored in the potential well it can spill over to adjacent pixels. In a frame transfer CCD a local overload usually spreads in the vertical direction giving vertical lines to the image. This is known as blooming. To prevent this, the excess carriers must be disposed of so the rest of the image is not degraded. Various antiblooming structures are incorporated into many devices. Usually CCD imagers have antiblooming drains between the imaging sites.

1.1.3. The Buried Channel CCD

In the previous sections it has been shown that signal charge can be localised by using simple MOS structures and then clocked out of the device. The device structure described allows the charge to be transferred at the semiconductor-insulator interface. Such devices are known as surface channel CCDs or SCCDs. Early on in the development of the CCD it was realised that the interaction of the signal charge packets with defects at the semiconductor-insulator interface causes a loss of signal. It was suggested in the original paper of Boyle and Smith [3] that

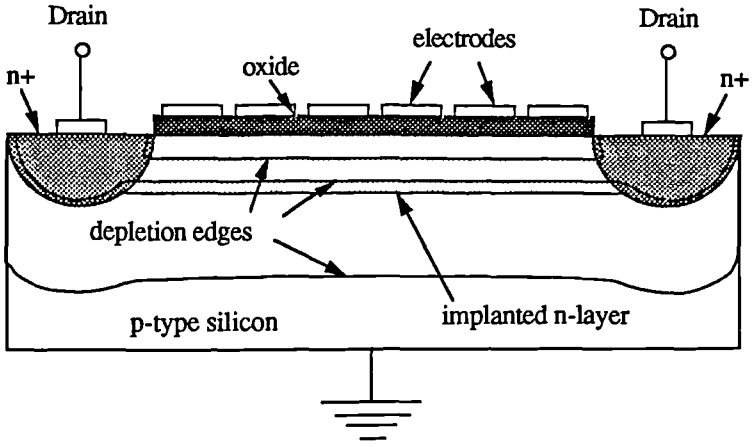

Figure 1.6. A schematic cross section of a buried channel CCD showing the edges of the depletion layers before 'punch through'

the loss could be reduced by several orders of magnitude if the signal was transferred in a channel away from the interface. Buried channel test structures were first fabricated and described by Walden *et al* [4] in 1972. In essence an n-buried channel CCD (BCCD) consists of an n-type semiconductor layer on a p-type substrate with n^+ drains at the end of the channel, as shown in Figure 1.6.

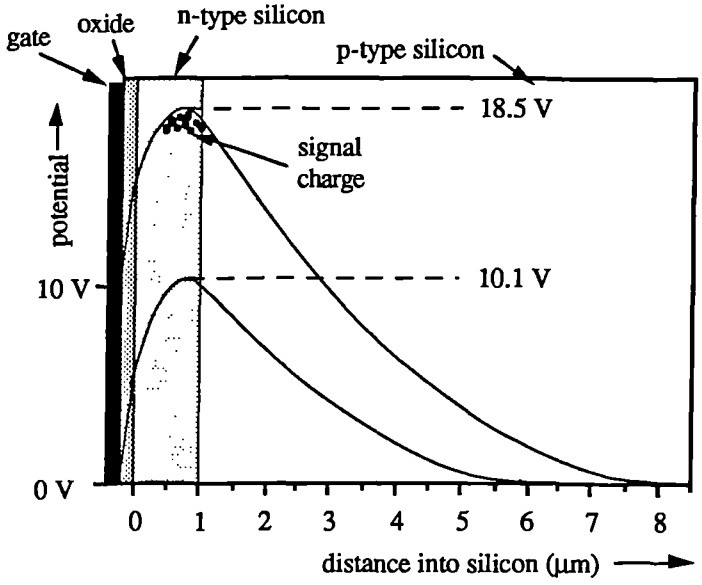

Figure 1.7. The potential distribution for a buried channel device. Oxide thickness = 0.2 μm, implantation depth = 1μm, n-layer dopant density = 10^{16} cm^{-3}, substrate dopant density = 5 10^{14} cm^{-3}.

If the voltage applied to the drain contacts is increased the depletion layer at the insulator-silicon interface will meet the depletion layer between the n-layer and p-type substrate. This is known as the 'punch through' condition. Punch through will occur for a drain voltage that is dependent on the dopant density of the n-layer etc. For practical devices this will be between 5 and 20 Volts.

Once the shallow n-layer is completely depleted, the potential distribution under the electrodes is independent of the drain voltage and is controlled by the electrode voltage only. The potential distribution can be obtained by solving the Poisson equation using the depletion approximation. The result, assuming an ideal step doping profile, is shown in Figure 1.7. It can be seen that the potential minimum for electrons lies at around 0.7 μm from the interface for the device parameters shown. Thus the signal charge collected in the potential well will have minimum interaction with the interface.

1.1.4. The Charge Transfer Processes

The transfer of charge between one electrode and the next is known as charge coupling. Both drift and diffusion contribute to the transfer of charge. Consider an idealised surface channel CCD model for the transfer of charge between two electrodes (Figure 1.8). At time $t < 0$ the charge is held under electrode A by the application of a high potential on A. At $t = 0$ a potential is applied to electrode B which is greater than that applied to A. There will be an abrupt increase in surface potential between the electrodes and electrons will tend to flow to B. As electrons flow to B the charge distribution under A will become non uniform and so there

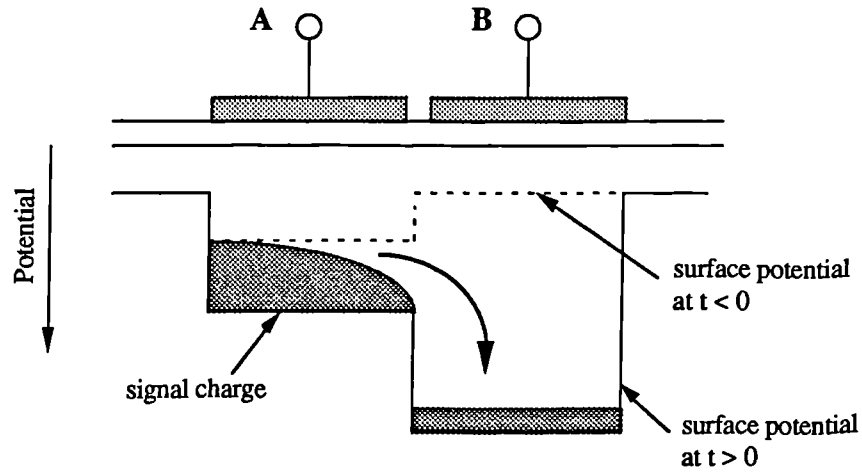

Figure 1.8. An idealised model showing the transfer of charge. The dashed line represents the surface potential at $t < 0$.

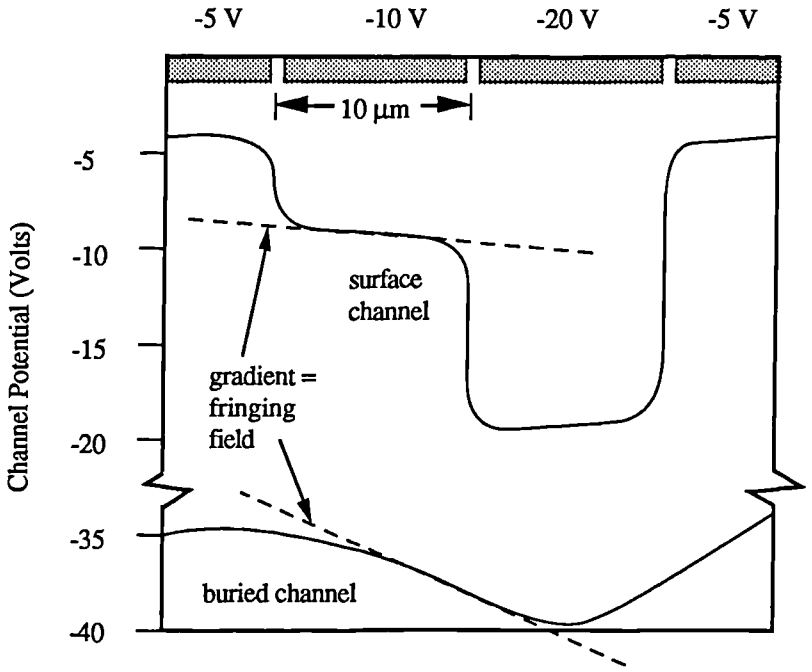

Figure 1.9. The potential along a p-channel CCD. For the surface channel device the surface potential is shown. The minimum potential is shown for the buried channel device.

will be an electric field induced in the direction of the flow of charge. This 'self-induced' field aids the transfer of charge. In the final stage of charge transfer the charge density under A is almost uniform and the 'self-induced' fields are very low. The charge is then transferred by thermal diffusion.

The above assumes that the surface potential, in the absence of charge, is constant under electrode A and then changes abruptly to a new value under electrode B. However in reality, the potential under A is affected by the voltages applied to B due to the coupling of the electrostatic potentials. This results in a longitudinal electric field at the surface even without signal charge. This field is known as the 'fringing field'. Therefore the last fraction of the signal charge is transferred by drift in this 'fringing field' rather than by thermal diffusion. The 'fringing field' increases with increasing oxide thickness, clock voltage swing and depletion layer width. The 'fringing fields' for a buried channel CCD [4] are larger than those of a surface channel CCD as shown in Figure 1.9.

If insufficient time is allowed for the transfer of charge then some of the signal will be left behind. The importance of the 'fringing field' is illustrated in Figure 1.10 which shows the fraction of charge not transferred as a function of time for a surface channel device. The charge transfer efficiency (CTE) is defined as the

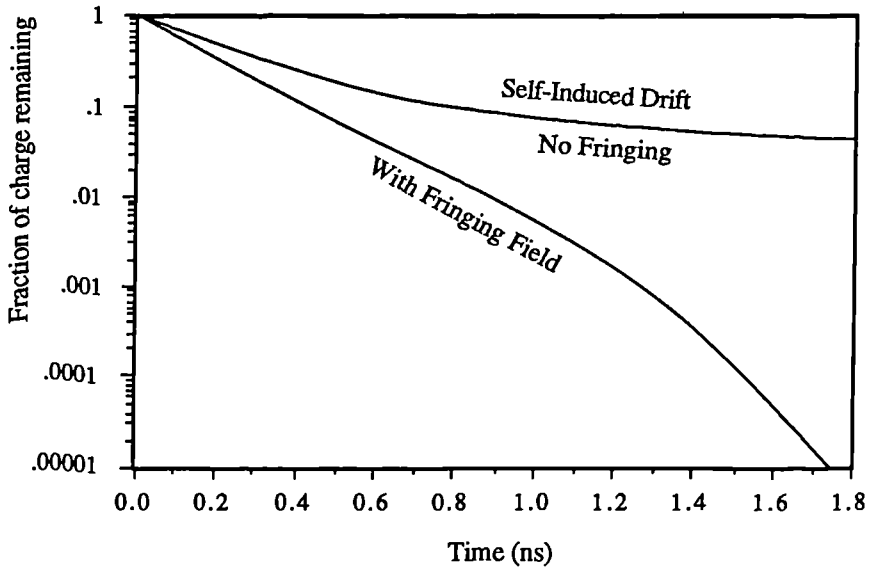

Figure 1.10. The fraction of remaining charge for a surface channel CCD showing the importance of the fringing field. The gate length = 4 μm and the oxide thickness = 200 nm. (After Carnes *et al* [5])

fraction of charge transferred to the next electrode although it can also be defined as the fraction of charge transferred from one pixel to the next. The second definition is more convenient for uneven times spent under each gate. The charge transfer inefficiency (CTI) is defined as 1 - CTE. An increase in the 'fringing field' allows the signal to be transferred more quickly and so a greater clocking rate can be achieved without a significant reduction in the CTE. Thus buried channel devices are preferred for high speed applications.

The CTE is affected by the trapping of signal charge by states within the band gap of the silicon. Surface channel devices are affected by the traps at the silicon-insulator interface. Charge in a buried channel device only interacts with traps within the bulk silicon. The density of these traps is several orders of magnitude less than those at the interface and so the CTI is significantly less than for a surface channel CCD. A more detailed explanation of the effect of bulk traps on the CTE is given in Chapter 4.

1.1.5. Output Circuits and Charge Detection

Eventually the charge that is moved through the CCD has to be detected and converted into a useful signal. There are several charge detection circuits that can

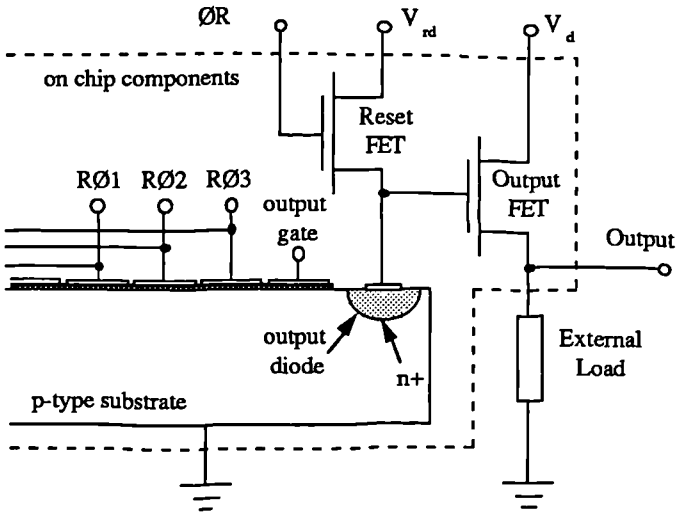

Figure 1.11. A typical CCD output circuit.

be employed at the output of a CCD. The most common detection circuit, known as the floating diffusion circuit, is shown in Figure 1.11. The charge is dumped onto a capacitor consisting of a reverse biased output diode and the stray capacitances on the output circuit. The change in voltage across this capacitance is then measured.

In operation, before charge is transferred from the readout register to the capacitance at the gate of the output FET (the output node), the capacitance is charged to the potential of V_{rd} by turning the reset FET 'on'. The reset FET is then turned 'off'. Charge can now be clocked onto the output node thus partially discharging the capacitance causing the potential on it to drop. This change in potential is proportional to the charge transferred from the CCD. The output FET buffers this signal to drive the following circuitry.

Careful design is required to prevent feedthrough from the clocks and the reset pulse from swamping the output. The output gate is DC biased and helps shield the output from the feedthrough of the RØ3 pulse. Often a dummy output circuit is fabricated identical to the one shown. The output from this circuit will contain the feedthrough pulses but not the signal. Therefore the feedthroughs can be eliminated by the use of a differential amplifier.

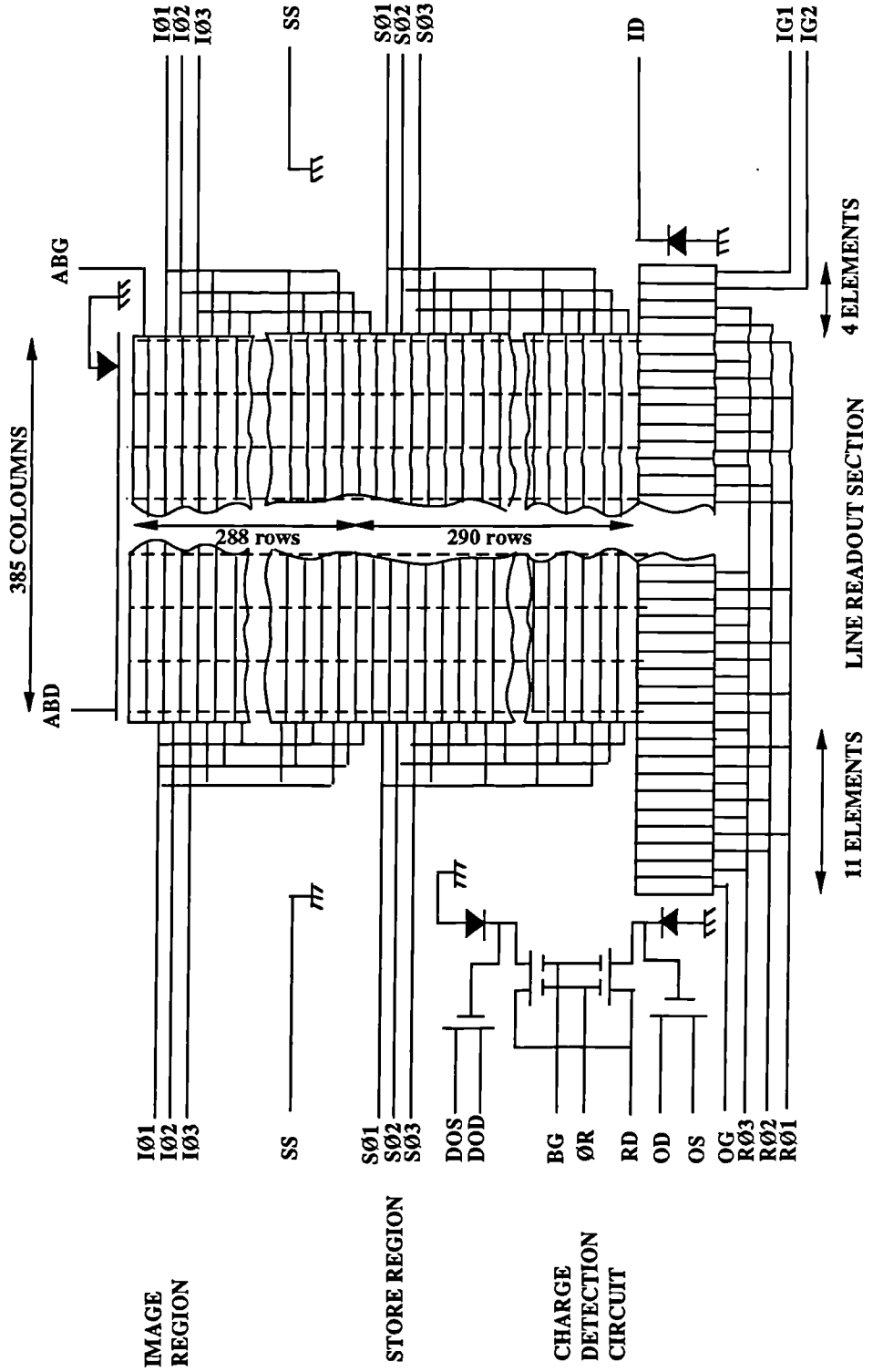

Figure 1.12. A Schematic layout of the EEV UT101 CCD.

1.1.6. The EEV UT101 and UT102 CCDs

The device used for most of this present study was the UT101, a 3 phase buried channel charge coupled device from EEV, England (Figure 1.12). This device was originally intended for optical imaging although it has been used successfully in the NA32 particle physics experiment at CERN. This CCD is no longer generally available but it is the device on which all the other EEV CCDs are based.

There are 288 by 385 pixels in the image area and 290 by 385 in the store section making a total of more than 200,000 pixels. Each gate is around 7 μm by 22 μm making a total pixel area of 22 μm by 22 μm and a total active area of 8.47 mm by 12.7 mm. The devices used did not have a metallised shield over the store region and so it could be used in a full frame mode, with the image and store being clocked together to form one continuous active area.

The output circuit is of the type described in the previous section. A dummy output circuit is also employed. A structure is included at the end of the readout register which consists of two gates and a drain. This allows charge to be injected by applying suitable potentials to the gates. No anti-blooming structures have been added to the device although structures labelled the antiblooming gate and the antiblooming drain can be found above the image area. These can also be used to inject charge. There are also gate protection structures on the device to protect the gates from electrostatic damage.

A cross section through the CCD is shown in Figure 1.13. The device is manufactured on a Czochralski grown, p-type silicon substrate with a doping concentration of ~5 10^{18} cm^{-3}. This forms an ohmic contact to a 20 μm p-type epitaxial layer grown with a doping concentration of ~5 10^{14} cm^{-3}. The substrate acts as a getter for impurities in the epitaxial layer. Therefore any impurities in the epitaxial layer will be attracted to the substrate and so the silicon through which the signal charge is stored and transferred will be almost free from these unwanted impurities.

To form the buried channel, phosphorus is implanted in strips to create a 1 μm n-type layer with a doping concentration of ~10^{16} cm^{-3}. The p-type silicon between the strips acts as channel stops. The gate insulator is formed from a sandwich of a SiO_2 layer and a Si_3N_4 layer the standard insulator thickness being 160 nm. The Si_3N_4 layer reduces the risk of gates shorting to the substrate via pinholes in the oxide. The nitride layer acts as a passivation layer protecting the underlying layers

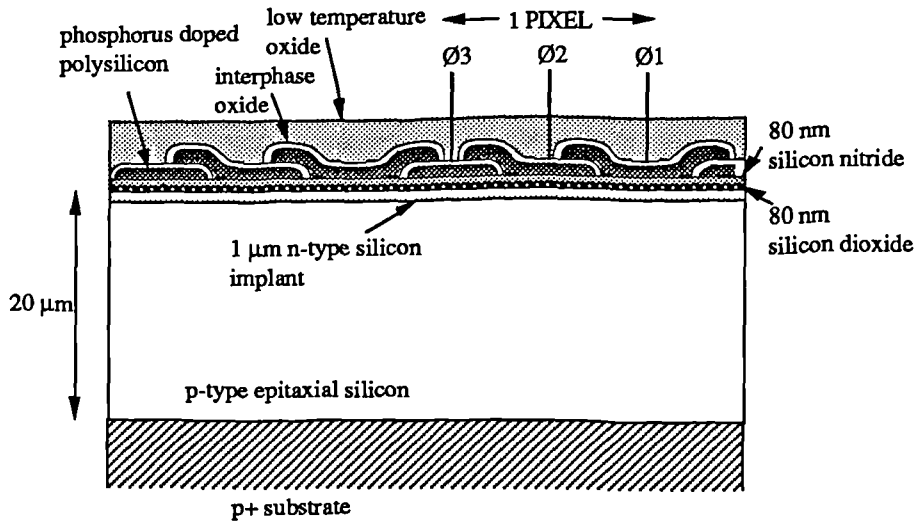

Figure 1.13. A schematic cross section of the EEV UT101 and UT102 buried channel charge coupled devices.

from etchants and dopants used in processing. It also allows the growth of the three level polysilicon gate structure.

The standard application for this device is television imaging and so the gates have to be transparent to light of optical wavelengths. This is achieved by employing semi-transparent polycrystalline silicon for the gates. To reduce its resistivity the polysilicon in doped with phosphorus. It has been shown that optimum charge transfer is obtained for minimal spacing between the gates. This has been accomplished by employing overlapping gate technology.

The EEV UT102 device is almost identical to the UT101 but without the input structures at the end of the readout register.

1.2. Damaging Radiation Effects in Materials

1.2.1. What is the Threat?

The radiation that usually degrades the performance of electronic devices is made up of energetic electrons, protons, neutrons or ions. These may originate from nuclear reactions, the natural space environment, particle accelerators or from secondary sources such as Compton electrons produced by gamma rays. Two classes of interaction must be considered when investigating the effect of radiation on semiconductor devices. Those are interactions that cause ionisation and those that

cause atomic displacements. These two causes of device degradation coexist in general but their relative importance depends on the energy and nature of the incident radiation.

The main mechanism for energy loss by charged particles traversing through a material is via inelastic collisions with atomic electrons. This results in the atomic electrons being either raised to an excited state (excitation) or to an unbound state (ionisation). Charged particles can interact elastically with the positive charge of the nucleus through the process of Rutherford scattering. Energetic neutrons also interact with the nucleus elastically. Such an interaction can be described as a hard sphere collision [6].

The energy transferred to the nucleus can be sufficient to displace the atom from its lattice position. If an atom is displaced, it may have sufficient energy to displace many other atoms.

Inelastic collisions with the atomic nucleus may also be important. In these interactions the incident particle raises the nucleus to an excited state. The nucleus then de-excites, emitting an energetic nucleon. The recoiling nucleus can then be displaced from its lattice site. Inelastic collisions can be important for high energy protons and thermal neutrons.

1.2.2. Ionisation

1.2.2.1. Ionisation by charged radiation

The energy lost by ionisation and excitation accounts for most of the energy lost by a charged particle traversing a material. The rate of energy loss along the path of the ion through the material (-dE/dx) is known as the stopping power. The energy loss for ions can be described by the expression of Bethe, ie.

$$-\frac{dE}{dx} = \frac{4\pi q^4 z^2}{m_e v^2} NZ\left(\ln\frac{2m_e v^2}{I} - \ln(1-\beta^2) - \beta^2\right)$$

zq and v are the charge and velocity of the incident particle, Z and N are the atomic number and number density of the target material, m_e is the electron rest mass and q is the electronic charge. I is the average excitation and ionisation potential of the target and $\beta \equiv v/c$. The term in brackets varies only slowly with particle energy and so the stopping power varies approximately as $1/v^2$ (ie. inversely with particle energy).

This expression also shows that the stopping power is strongly dependent on the charge of the incident particle. The greater the charge on the ion the greater the rate of energy loss. The Bethe equation is in reasonable agreement with experiment at high energies. However it breaks down at lower energies as no account is taken of charge exchange with the target. As the incident ion picks up electrons from the target, the actual stopping power becomes significantly less than that calculated.

In order to calculate the stopping power for energetic electrons, the Bethe equation has to be modified to take into account the fact that the energy loss is via collisions between identical particles. The equation for the stopping power has been calculated by Bethe for excitation and ionisation of the target material and is given by

$$-\left(\frac{dE}{dx}\right)_c = \frac{4\pi q^4 z^2 NZ}{m_e v^2}$$
$$\times\left(\ln\frac{2m_e v^2 E}{2I^2(1-\beta^2)} - \ln 2\left(2\sqrt{1-\beta^2} - 1 + \beta^2\right) + (1-\beta^2) + \frac{1}{8}\left(1-(1-\beta^2)\right)^2 \right)$$

Due to its low mass, the electron will follow a much more tortuous path when traversing the target than heavily charged particles. The electron will experience large accelerations so it will lose energy by emitting electromagnetic radiation (bremsstrahlung). The stopping power due to this process is

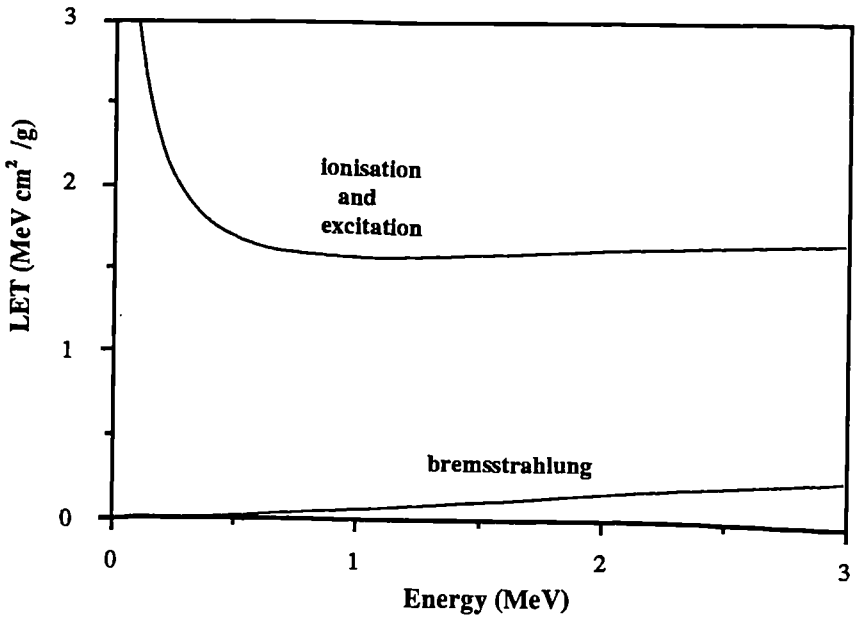

Figure 1.14. The LET for electrons through silicon.

$$-\left(\frac{dE}{dx}\right)_r = \frac{q^4 NEZ(Z+1)}{137 m_e^2 c^2}\left(4\ln\frac{2E}{m_e c^2} - \frac{4}{3}\right).$$

The total stopping power for electrons is thus

$$\frac{dE}{dx} = \left(\frac{dE}{dx}\right)_c + \left(\frac{dE}{dx}\right)_r.$$

The linear energy transfer (LET) is defined as the stopping power divided by the density of the material. The total LET for electrons through silicon is shown in Figure 1.14. It can be seen that the energy loss by bremsstrahlung is a small fraction of the total energy loss except at high energies. The rate of energy loss by ionisation will be greatest for low energy electrons. The LET reaches a minimum at around 800 keV and then starts to rise slowly due to relativistic effects. If the energy of any charged particle is higher than that required for the LET to be a minimum then the particle is known as a minimum ionising particle or a MIP. The LET for a minimum ionising particle is almost constant for all incident particles and is approximately 1.6 MeV cm^2/g for silicon.

1.2.2.2. Ionisation by uncharged radiation

Photons and neutrons carry no charge and therefore cannot interact via the coulomb force, which dominates the charge loss mechanism for charged particles. However, significant ionisation is observed due to the interaction of secondary particles produced by the radiation. For example, the main ionising effects of neutrons are in fact due to the ionisation by recoil atoms. The main interaction mechanisms by photons are given below. The details of the interactions can be found in reference [7].

Unlike charged particles, which lose energy continuously as they pass through the target by simultaneous interaction with many target atoms, photons interact with a target atom with complete or partial transfer of the photon energy to an electron. The photon either disappears altogether or is scattered through large angles. Photons can interact with matter in several ways, depending on their energy. The major interaction mechanisms are the photoelectric effect, compton scattering and pair production. The relative importance of these mechanisms is illustrated in Figure 1.15. The plot shows the regions of photon energy where each of the effects dominate. These regions are dependent on the target material as shown.

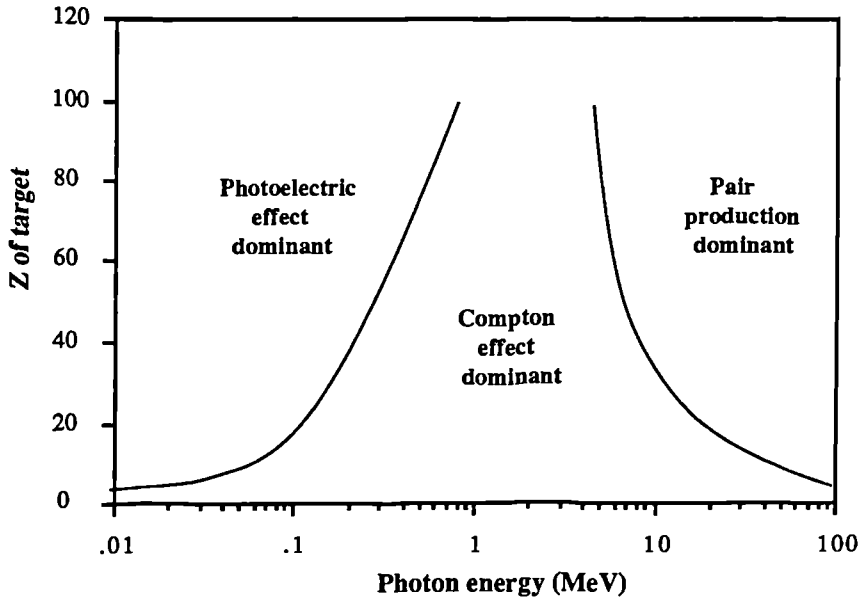

Figure 1.16. The relative importance of the three major types of photon interaction.

The photoelectric effect involves the photon interacting with an atomic electron. The photon is completely absorbed and the electron is ejected from the atom with an energy equal to the original photon energy minus the binding energy of the electron in its original atomic shell.

Compton scattering involves the elastic scattering of the photon from atomic electrons. These electrons can be regarded as being free as the energy transferred is very much greater than the binding energy. The energy of the recoil electron is dependent on the scattering angle. If the photon is deviated only slightly from its original direction then little energy will be transferred to the electron. However, if the photon is scattered back along its original path then almost all of it energy is transferred. Compton scattering is the dominant interaction for 1 MeV gammas emitted by the Co^{60} radioactive source.

If the photon energy exceeds twice the rest mass energy of an electron, pair production is energetically possible. In this interaction, the photon is converted to an electron and a positron in the field of an atomic nucleus. The energy carried by the photon, above the energy required to create the pair, is converted into kinetic energy shared by the electron and positron.

The secondary electrons produced by the above process will lose energy by excitation and ionisation of the target in the manner described in the previous section. The secondary electrons produced by the photoelectric effect are low

energy so their ionisation effects are felt close to the original photon interaction. However, those electrons from the compton effect and pair production can lead to a long ionisation trail.

1.2.2.3. The units of dose

The amount of ionising radiation incident on a material is known as the dose. The SI unit of dose is the Gray. One Gray corresponds to a deposited energy of 1 J/kg = 6.24 10^{18} eV/kg . An alternative unit to the Gray is the rad. 100 rads corresponds to 1 Gray. It will become clear that the result of energy deposition in the material is dependent on the material, the energy and nature of the incident radiation. Therefore it is necessary, when quoting a dose, to state the material and radiation to which it is referring.

1.2.3. Atomic Displacements

While most interactions between the incident energetic charged particles and atoms in the target material transfer energy via ionisation and excitation a small fraction impart enough energy to the nuclei to dislodge them from their lattice position forming a Frenkel defect. High energy neutrons do not directly cause ionisation and their main mechanism for energy loss is by collisions with the nucleus and therefore by causing these defects. The energy that must be imparted to create a Frenkel defect has been estimated by Seitz [8] to be around four times the sublimation energy for the atom. For silicon the mean energy required is around 20 eV. The primary knock on atom (PKA) will rapidly come to rest by losing energy either by ionisation and excitation or by causing further Frenkel defects.

1.2.3.1. Displacement damage due to high energy electrons

High energy electrons can collide with the nucleus of an atom in the target material and scatter elastically in its coulombic field. Employing relativistic kinematics it can be shown that the maximum energy that can be transferred to a nucleus of mass M by an electron of energy E is given by [9]

$$T_m \approx \frac{2(E+2m_ec^2)E}{Mc^2}$$

where m_e is the electronic rest mass. The nucleus will be displaced from its lattice position if T_m is greater than a threshold energy, T_d. This implies that for a

displacement threshold of 20 eV, the minimum electron energy required to cause displacements is around 210 keV in silicon. For electrons with energies above this value the probability of an atomic displacement can be described in terms of a displacement cross section, $\sigma(E)$. Using the cross section, the density of PKAs produced by a fluence, Φ, of electrons with an energy E is given by

$$N = n\,\sigma(E)\,\Phi$$

where n is the number density of target atoms.

When an electron is scattered by a nucleus it will scatter in a direction that is dependent on the energy of the electron and the recoil energy of the nucleus, the angle being governed by the conservation laws for energy and momentum. The maximum energy is imparted to the nucleus when the incident electron is scattered back along its original path. The distribution of scattering angles is described by the Rutherford cross section which is obtained by treating scattering between two point charges [6]. In terms of the energy transferred to the nucleus, T, the differential cross section is

$$\frac{d\sigma}{dT} = \frac{\pi Z^2 e^4}{4E^2}\left(\frac{m_e+M}{M}\right)^2 \frac{T_m}{T^2}$$

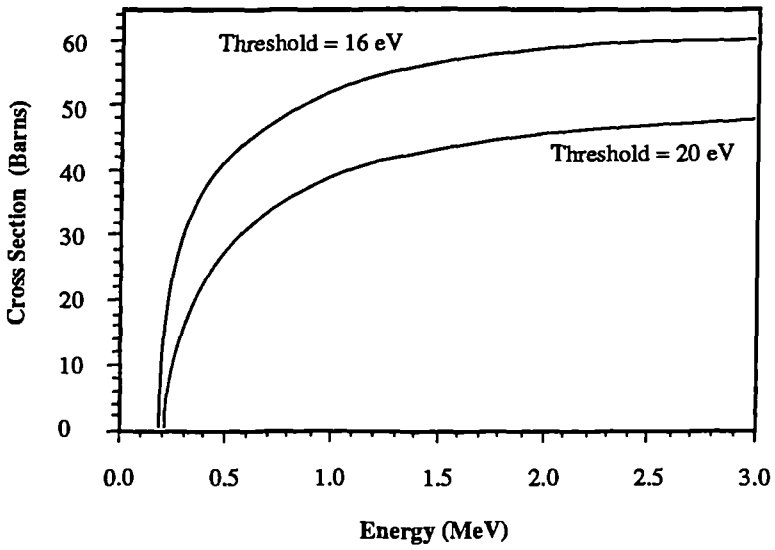

Figure 1.17. The cross section for atomic displacement in silicon using the McKinley and Feshbach approximation. Assumed threshold energies of 16 eV and 20 eV are shown.

where Z is the atomic number of the target.

This classical result has been modified by Darwin to include relativistic effects and Mott has taken a quantum mechanical approach to the problem. A good approximation to this rigorous quantum mechanical correction has been given by McKinley and Feshbach which is valid for low Z materials (around 10% error for copper). Using these differential cross sections, the cross section for atomic displacement, $\sigma(E)$, can be calculated by integrating the differential cross section from the threshold energy to the maximum energy that can be imparted to the nucleus. The result using the McKinley-Feshbach differential cross section is shown in Figure 1.17. This indicates that the density of PKAs will increase rapidly as the electron energy increases from that required to impart the threshold energy but then the density remains almost constant for energies above 3 MeV.

Multiple atom displacement occurs when the PKA has sufficient energy so that it in turn can displace secondary atoms via atom-atom collisions. The secondary displaced atoms may also have enough energy to cause further displacements. The number of secondary displaced atoms depends on the spectrum of the PKAs which in turn depends on the energy of the incident electron. The mean energy of the PKA, can be obtained from the differential cross section for energy transfer, ie.

$$\overline{T} = \int_{T=T_d}^{T_m} T\frac{d\sigma}{dT}dT \Bigg/ \int_{T=T_d}^{T_m} \frac{d\sigma}{dT}dT.$$

For Coulombic scattering this yields

$$\overline{T} = \frac{T_d T_m}{T_d + T_m}\ln\left(\frac{T_m}{T_d}\right) \approx T_d \ln\left(\frac{T_m}{T_d}\right) \qquad (1.5).$$

This implies that the mean energy imparted to the PKA by the incident electron is very much less than the maximum that can be transferred .

The displacement cascade can be well described by Monte Carlo simulations (e.g. TRIM-91). However an approximate but enlightening solution to the problem of multiple displacements has been developed by Kinchin and Pease [10]. According to their analytical solution, the mean number of displacements per PKA, ν, is given by

$$\begin{aligned} \nu &= 1 && \text{for } T_d < \overline{T} < 2T_d \\ \nu &= \frac{\overline{T}}{2T_d} && \text{for } \overline{T} > 2T_d \end{aligned} \qquad (1.6)$$

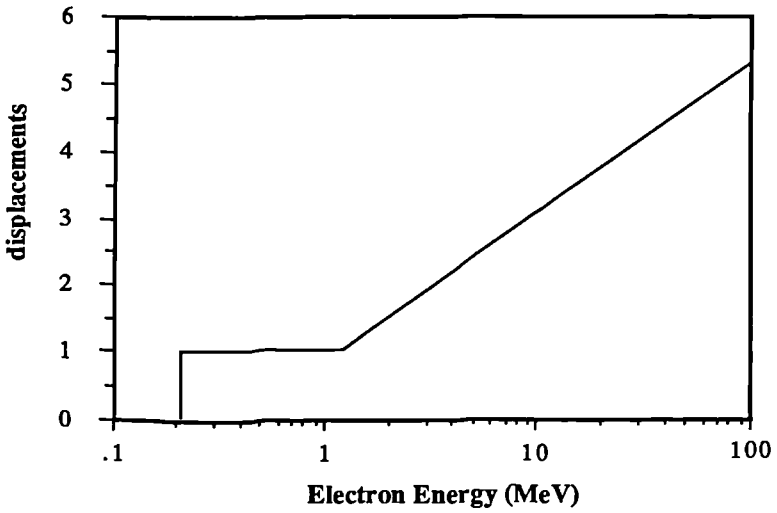

Figure 1.18. The mean number of displacements per primary displacement as a function of electron energy. $T_d = 20$ eV.

The result for ν as a function of incident electron energy is given in Figure 1.18. From this it can be seen that if an atom is displaced by a 4 MeV electron then, on average, there will be a second atom displaced by the PKA. If an atom is displaced by a 50 MeV electron then on average there will be a total of 4.6 displacements. It must be remembered that the above is obtained for a very crude model as it does not contain correct partitioning of the energy lost by ionisation and by nuclear collisions. However the result indicates that ν is proportional to $\overline{T}$. Even for more rigorous calculations, the proportionality factor does not differ significantly from $1/2T_d$ [6].

In silicon, the interstitial atoms that result from the displacement damage are not electrically active. On the other hand, the vacancies are extremely mobile even at temperatures as low as 100K, and move around the lattice, either recombining with interstitials or a small number form stable defect complexes which can act as effective recombination centres. Much effort has been undertaken to understand the nature of these complexes using such tools as electron spin resonance (ESR) and deep level transient spectroscopy (DLTS).

There are many stable defect complexes that are introduced by displacement damage. Summaries of the defects produced by electron irradiation are given in [11] and [12]. The dominant electron induced complexes in phosphorus doped n-type silicon are the Si-E and Si-A centres. These complexes introduce acceptor levels within the band gap. Also produced is the divacancy which is amphoteric

and is particularly important in p-type silicon. Watkins and Corbett [13] established that the Si-E centre was a vacancy trapped next to a substitutional phosphorus atom. The Si-A centre was first observed by Bemski *et al* [14] and has been shown to be a vacancy-oxygen pair [15]. The divacancy is a stable configuration of paired vacancies [16]. The introduction rate (defined as the defect density divided by the electron fluence) of each of these three complexes depends on a number of factors. For example, the introduction rate for the divacancy is dependent on the charge state of the vacancies [17]. The density of divacancies appears to increase in importance for high electron energies [18] but in some studies the divacancy is not observed at all [11]. An increase in the introduction rate of the Si-E centre is observed with increased phosphorus content [12] and the introduction rate of the Si-A centre is dependent on the oxygen content. Since oxygen and phosphorus compete for vacancies from the same source, the introduction rate of the Si-A centre and Si-E centre depends on both the oxygen and phosphorus concentration. The relationship is determined by the ability for the oxygen and phosphorus to trap the vacancies. The ratio of the Si-A centre to the Si-E centre concentration has been used to calculate the amount of oxygen in the sample. A simple model gives

$$\frac{n_A}{n_E} = \frac{\sigma_{ov} N_O}{\sigma_{pv} N_p}$$

where n_A, n_E, N_O and N_p are the concentrations of the Si-A centre, the Si-E centre, oxygen and phosphorus respectively. σ_{ov} and σ_{pv} are the vacancy capture coefficients of oxygen and phosphorus. The ratio σ_{ov}/σ_{pv} has been determined to be 0.073±0.006 [19]. This implies that, for an equal concentration of oxygen and phosphorus in the silicon sample, the introduction rate of the Si-A centre is less than 10% that of the Si-E centre.

The actual measured values of the position of these levels within the band gap of the silicon varies from one investigator to another. The Si-E centre appears to have an acceptor level in the range 0.42±0.06 eV below the conduction band edge and the Si-A centre an energy level of 0.17±0.02 eV below the conduction band. The divacancy is more complicated and the energy level depends on its charge state. It often appears with two acceptor levels in the upper half of the band gap, one in the same range as the Si-E centre associated with the (=/-) transition on the emission of an electron and one at around 0.23 eV below the conduction band corresponding to the (-/0) transition [20]. It also introduces a donor level in the lower half of the band gap at around 0.35 eV above the valence band.

The picture associated with the radiation induced levels is a complicated one. Recent evidence has shown that even the simple picture of the Si-E centre may require modification in the light of recent evidence of metastability of the defect complex [21]. However the simple models appear to suffice when considering the effect of radiation on electronic components.

1.2.3.2. Displacement damage due to protons and neutrons

For illustration only elastic scattering is considered. Protons and neutrons have a mass that is around 2000 times greater than the mass of an electron. This means that classical mechanics can be used to calculate the maximum energy that can be transferred to a nucleus in the target for proton or neutron energies below around 100 MeV, ie.

$$T_m = \frac{4mM}{(m+M)^2} E$$

where m is the mass of the proton or neutron. For a 5 MeV particle T_m is 670 keV compared with a T_m of 2.3 keV for a 5 MeV electron. From this alone it can be seen that the damage caused by protons and neutrons will be much greater than by electrons of the same energy.

As the proton is charged, the scattering is coulombic and can be described by the Rutherford cross section. The total cross section for displacement is in the order of $5\ 10^{-20}$ cm^2 for a 5 MeV proton [22] approximately 3 orders of magnitude greater than the cross section for a 5 MeV electron. Therefore it can be expected that the number of PKAs will be approximately 1000 times higher. The mean energy transferred to the PKA by a proton can be calculated from (1.5) and the mean number of displacements per PKA from (1.6). A PKA created by a 5 MeV proton will, on average, create a further 4.2 displacements whereas a PKA from a 5 MeV electron will produce 1.2 more displacements.

From the above it is evident that a proton will cause far more displacement damage than an electron of the same energy. The proton damage will be highly inhomogeneous due to the high number of secondary displacements which occur near the site of the primary displacement.

The damage caused by neutrons differs from that caused by protons and electrons as they are uncharged. They are not scattered by the coulomb field of the nucleus and therefore the scattering cannot be described in terms of the Rutherford cross

section. Instead the interaction of neutrons can be described in terms of hard sphere collisions. The differential cross section, for energy transfer, is [6]

$$\frac{d\sigma}{dT} \approx \frac{\text{constant}}{T_m} \qquad (1.7).$$

The total elastic scattering cross section of light elements is in the order of the geometric cross section of the atomic nucleus $\approx 10^{-24}$ cm^2. This value is very much less than the cross section for displacement by high energy electrons or protons. Therefore the number of PKAs is relatively small. However the mean energy given to a displaced silicon atom is approximately $T_m/2$ yielding around 8000 secondary displacements for a PKA formed by a 5 MeV neutron. This will be an over estimate because inelastic events also play a role in the collision process. However, it does show that there will be a very large number of secondaries produced for each PKA. Most of these displacement cascades of secondaries will be less than around 1000 Å long and there will be 1 to 3 terminal sub-clusters of damage per track. The terminal sub-clusters have a typical dimension of 50 Å [23].

The defect complexes produced by neutrons and protons are essentially the same as those produced by electrons. However, in the past it has been thought that the stable complexes caused by neutrons act as extended defects. This has been shown not to be the case and all defect complexes act as atomic defects [23] and that the displacement damage effects are most readily explained on the basis of stable defects acting as isolated recombination and trapping centres.

1.2.3.3. Annealing of the Damage

If a defect complex is given enough thermal energy then it will move around the lattice of the semiconductor. It may break up or combine with other defects. Either way, the original complex will be removed from the material. This is known as annealing.

If the temperature is low enough during irradiation the vacancies and interstitials produced will be immobile. As the temperature is raised the interstitial starts to move around the lattice and can recombine with the immobile vacancies. At higher temperatures, the vacancies that remain start to move. The temperature at which this motion starts depends on the charge state of the vacancies. A negatively charged vacancy moves around the lattice freely at a much lower temperature than a vacancy with no charge. The mobile vacancies eventually recombine or combine with impurities within the silicon. The resultant vacancy defect complexes remain

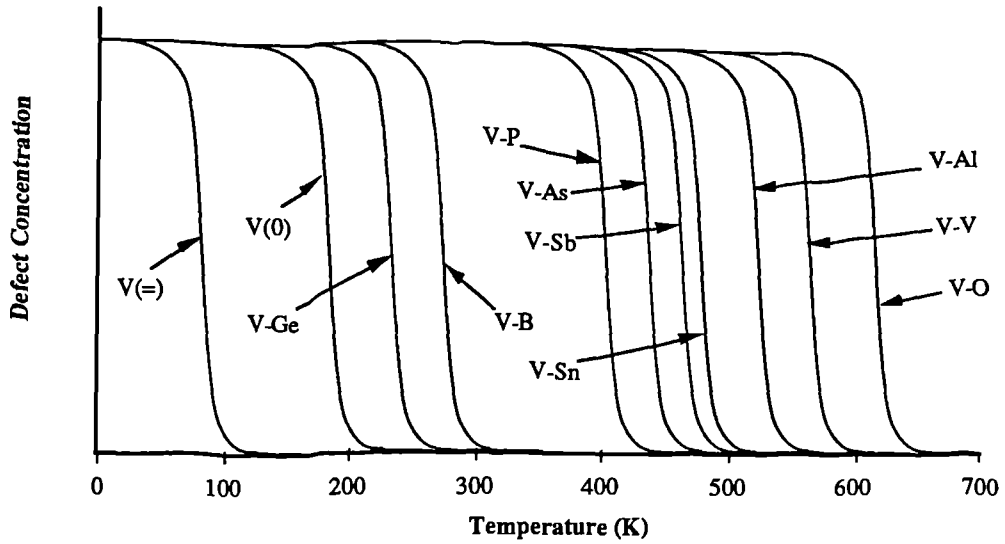

Figure 1.19. A schematic of vacancy and vacancy-impurity pair annealing stages (after Watkins [24])

stable until the temperature reaches a certain limit which is dependent on the nature of the complex. Above this temperature the complex can freely move around the lattice. This is illustrated in Figure 1.19 which shows the annealing of certain vacancy-impurity pairs in silicon.

1.3. The Effect of Radiation on Semiconductor Devices

1.3.1. The effect of defect complexes on semiconductor devices

The levels within the band gap of semiconductors, due to radiation induced defect complexes, have several effects which are illustrated in Figure 1.20. Figure 1.20a) illustrates the process of recombination. Here a charge carrier is captured at the defect centre and subsequently a carrier of opposite sign is trapped at the same centre. The rate of recombination depends on the density of the centre, the free carrier concentration, the electron and hole capture cross sections for the centre and on the position of the level within the band gap. There are four processes that determine the recombination rate via a single level in the band gap. Those are, electron capture by the level, electron emission from the level back to the conduction band, hole capture by the level and the emission of a hole from the level to the valence band. The total rate of recombination can be calculated using Shockley, Read, Hall (SRH) statistics [25,26] and is given as

$$R = \frac{\sigma_n \sigma_p v_{th} N_t (np - n_i^2)}{\sigma_n (n + n_i \exp(E_t - E_i)/kT) + \sigma_p (p + n_i \exp(E_i - E_t)/kT)}$$

where σ_n and σ_p are the electron and hole capture cross sections, v_{th} is the thermal velocity of the charge carriers (assumed the same for electrons and holes), N_t is the trap density, n and p are the electron and hole densities, n_i is the intrinsic carrier density, E_i is the intrinsic Fermi level and E_t is the energy level of the centre.

In thermal equilibrium R=0 which implies that $np = n_i^2$. This is the familiar law of mass action. For simplicity the capture cross sections can be set equal to σ giving

$$R = \frac{\sigma v_{th} N_t (np - n_i^2)}{n + p + 2 n_i \cosh((E_t - E_i)/kT)} \qquad (1.8).$$

This rate reaches a maximum when E_t is equal to E_i. Therefore the most effective traps for recombination are situated around the centre of the band gap. The mean time a minority carrier spends in its band before recombining is known as the minority carrier lifetime. Radiation induced recombination centres cause this lifetime to decrease. A degradation in the minority carrier lifetime is the main cause of the gain degradation in bipolar transistors.

In the depletion region of a device n and p are very much less than the intrinsic carrier concentration and equation (1.8) simplifies to

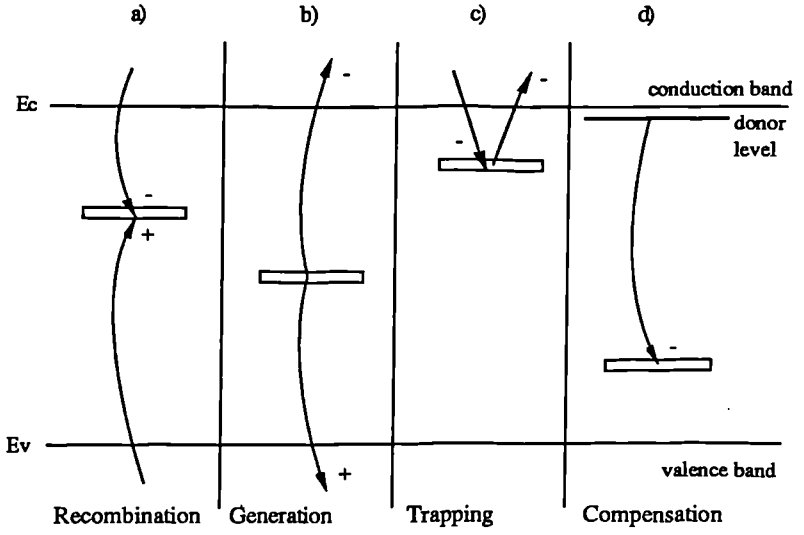

Figure 1.20. The effects of radiation induced levels within the band gap of a semiconductor.

$$R = -\frac{\sigma v_{th} N_t n_i}{2\cosh((E_t - E_i)/kT)} \qquad (1.9).$$

In this case the rate of recombination is negative indicating that electron hole pairs are being generated. This is the process shown in Figure 1.20b). This can be seen as the alternate emission of an electron and hole from the level. Alternately it can be viewed as the thermal excitation of a bound electron from the valence band to the level which is then followed by the excitation of that electron to the conduction band. The rate of generation is also a maximum for traps near mid gap. Therefore radiation induced levels near mid gap, in the depletion region of devices, contribute to the leakage and dark currents.

If a charge carrier is captured at a defect centre, and is later emitted back to its band before a recombination event can take place, the level is generally called a trap. The process of an electron being trapped from the conduction band is shown in figure 1.20c). Traps caused by radiation are the main cause of CTE degradation in CCDs. A more detailed study of this is given in a later chapter.

The compensation of donors (or acceptors) is shown in Figure 1.20d). Here the free electrons available from the donor level are compensated by deep lying radiation induced acceptors. The result is a reduction in the equilibrium majority carrier concentration, with the material appearing more intrinsic as far as the carrier concentration is concerned. This is particularly important at high doses in high resistivity material.

The charged radiation induced defect centres also act as scattering centres. This can be seen in the decrease in the mobility of the charge carriers for very high radiation fluences.

1.3.1.1. The application of NIEL

Section 1.3.3 gives quite a complicated picture of displacement damage. Therefore it is somewhat surprising that the effects of one radiation type and energy can be successfully extrapolated to the effects of another radiation type and energy, in some situations, by employing the calculated nonionising energy loss (NIEL) shown in Figure 1.21.

There exists a large database of displacement damage effects due to the irradiation of microelectronic devices by neutrons. This arises from extensive nuclear weapons research programs. Such a wealth of knowledge does not exist for other

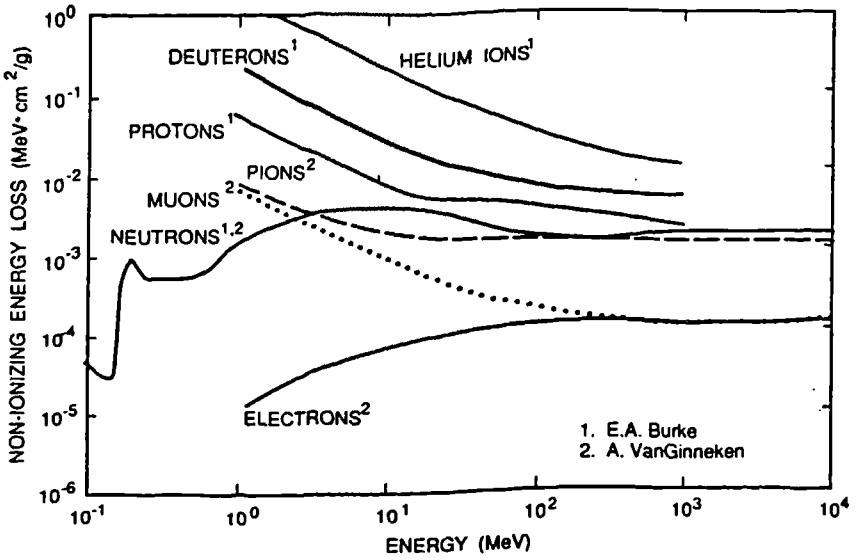

Figure 1.21. The calculation of the nonionising energy deposition in silicon.

radiation types and therefore it has been necessary to extrapolate the neutron results to estimate the effects of high energy electrons and protons for example. Successful extrapolation has recently been achieved when considering minority carrier lifetime effects [27] and carrier removal [28]. The reduction of the common emitter DC gain for a bipolar transistor due to the degradation of the minority carrier lifetime is given as an example. The degradation is given by the Messenger-Spratt equation [29]

$$\frac{1}{h_{fe}} = \frac{1}{h_{feo}} + K\Phi$$

where h_{feo} and h_{fe} are the gains before and after irradiation, Φ is the irradiating particle fluence and K is the damage factor which is dependent on the total number of recombination centres produced and therefore dependent on the nature and energy of the radiation. It has been found that K varies almost linearly with NIEL over a wide range of energies and particle types. This implies that the total number of stable defects produced is virtually independent of the PKA spectrum. This relationship between the measured damage constant and the calculated NIEL is illustrated in Figure 1.22. The NIEL gives no information about the individual trap types, energy level in the band gap or their cross sections. Therefore, its relevance to individual applications where these parameters are important, has to be investigated.

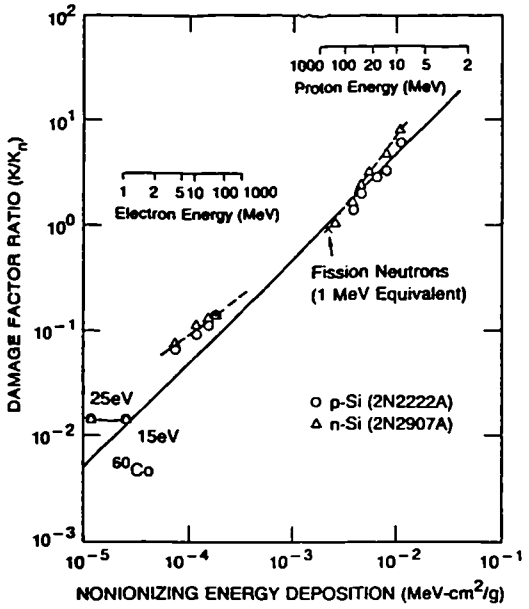

Figure 1.22. The damage factor normalised to 1 MeV neutrons as a function of calculated NIEL for electrons, protons and neutrons. The solid line shows the linear relationship [30].

1.3.2. The effect of ionising radiation on semiconductor devices.

1.3.2.1. The creation of electron-hole pairs

If the target material is an insulator or semiconductor then atomic electrons that have been given enough energy by the incident radiation can be excited from the valence band of the material to the conduction band. The amount of electron energy above that required to bridge the band gap is either used to create secondary electron hole pairs or transferred to the lattice in the form of thermal energy. The electron, after dissipating this energy, may then reside in an energy state near the bottom edge of the conduction band.

The mean energy deposited by the ionising radiation that is required to form an electron hole pair, E_p, in a semiconductor is approximately given by the empirical relationship

$$E_p \approx 2.67\, E_g + 0.87$$

where E_g is the band gap of the semiconductor [31]. The energy required in an insulator is approximately two times the band gap. Some values of E_p are shown in Table 1.1.

	Si	GaAs	SiO2
Band Gap (eV)	1.12	1.35	9
Mean Energy For e-h pair (eV)	3.6	4.8	18

TABLE 1.1. The band gap and threshold energy for e-h production by ionising radiation.

The number of charge carriers created along the path of the ionising particle can then be found from

$$\int_0^L \rho \frac{LET(x)}{E_p} dx.$$

where the integral is over the path of the particle and ρ is the density of the target.

The electron-hole pairs created by ionisation takes the semiconductor or insulator out of equilibrium. The charge carriers move by diffusion where there is a concentration gradient and they will drift in the presence of an electric field. They may recombine with other carriers or they may be trapped at sites with energy levels within the band gap.

An important figure when considering the effect of ionising radiation on electronic components is the fraction of charge that escapes initial recombination. This depends on the electric field and the nature of the incident radiation [32]. The initial recombination will be greater the higher the generated charge density, ie. initial recombination will be higher for heavily ionising radiation than for a lightly ionising particle. In the presence of an electric field the electrons and holes produced by the ionising radiation will be swept apart. The higher the electric field the quicker they will be separated, leaving less time for the initial recombination. Therefore the fraction of charge that escapes initial recombination will be higher for higher fields. This can be seen in Figure 1.23 where the fractional yield from 12 MeV electron irradiation approaches one for electric fields greater than 2 MV/cm.

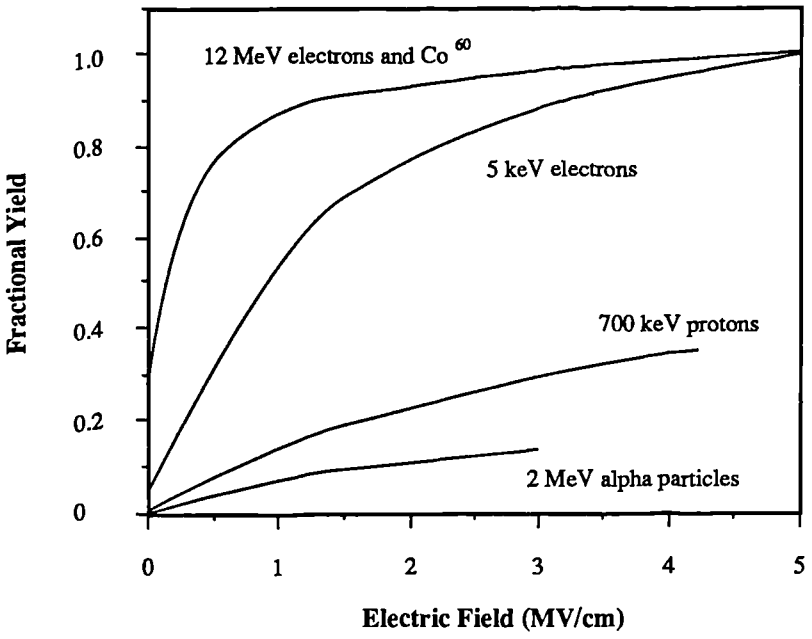

Figure 1.23. The fraction of radiation induced charge that escapes initial recombination.

In general, unless the rate of energy deposition by ionising radiation is very high, there will be no permanent damage to the bulk of semiconductor devices due to the electron-hole pairs produced. However, the electron hole pairs that are created will be separated in the presence of an electric field and form a current pulse. This current pulse may cause logic gates to switch and memory elements to lose their information. In detectors, the charge generated by ionising radiation will form an unwanted background that may mask the required signal.

1.3.2.2. The effect on MOS structures

Ionising radiation can cause permanent effects at the surface of the semiconductor and in insulating layers. For illustration the MOS capacitor will be used as it applicable to the degradation of CCDs due to ionising radiation. Consider a uniformly doped MOS capacitor before irradiation. The voltage that is applied to the gate of the capacitor that makes the electron or hole density the same at the SiO_2-Si interface as in the bulk silicon is known as the flat band voltage, V_{fb}. For an ideal MOS capacitor V_{fb} is zero. However, in reality this will deviate from zero due to the work function difference between the gate electrode and the semiconductor, charge in the insulator and charged interface states. The flat band voltage is thus

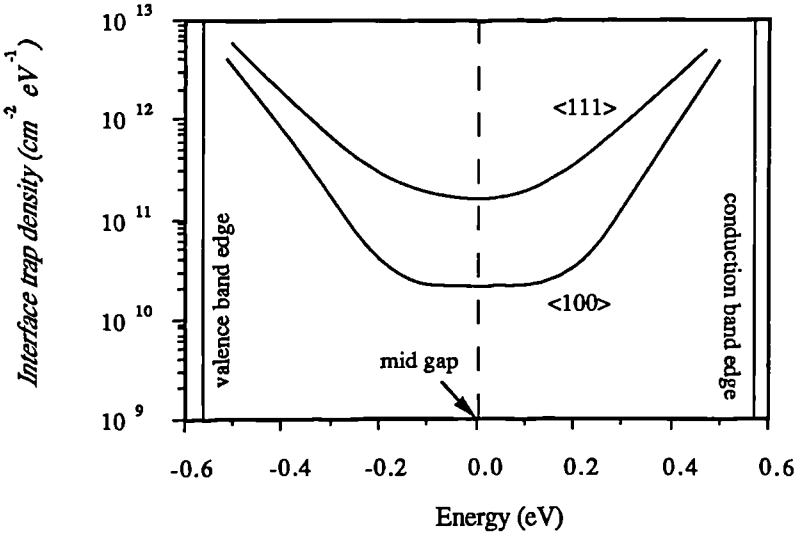

Figure 1.24. The interface state density in oxidised silicon [33].

$$V_{fb} = \phi_{ms} - \int_0^d \frac{x\rho(x)}{C_o d}\,dx - \frac{Q_{it}}{C_o}$$

where ϕ_{ms} is the work function difference, Q_{it} is the charge trapped in interface states, $\rho(x)$ is the charge distribution within the oxide, C_o is the insulator capacitance and d is the oxide thickness.

Interface states occur at the SiO_2-Si interface and are due to a lattice mismatch between the silicon and silicon dioxide, impurities or disconnected chemical bonds. The interface states are energy levels within the band gap of the silicon that can readily exchange charge with the bulk silicon. The density of interface states, D_{it}, is generally found to be continuous throughout the band gap and increases towards the band edges. A typical distribution is shown in Figure 1.24.

The amount of charge due to the interface states depends on the density of interface states and on the position of the Fermi level at the interface. It has been found that the states below the middle of the silicon band gap are donor like (neutral when filled with an electron and positive when empty) and those in the upper half of the band gap are acceptor like (negatively charged when filled with an electron and neutral when empty). If the Fermi level was at mid gap then Q_{it} would be zero as the density of interface states in the upper half of the band gap is approximately equal to the density in the lower half. However, in the flat band condition, the Fermi level will be either in the upper half of the band gap for an n-type substrate or

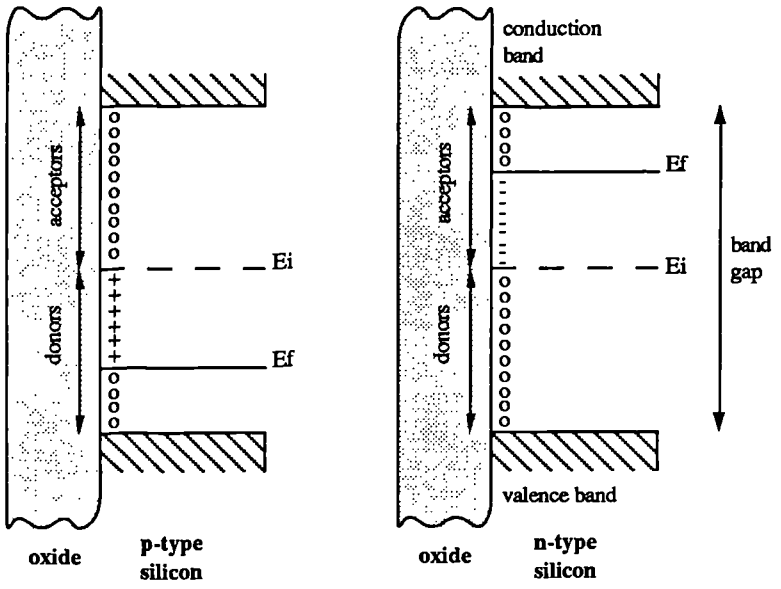

Figure 1.25. The charge state of interface states for p and n type substrates.

in the lower half for a p-type substrate. The charge state of the interface states is illustrated in Figure 1.23. For an n-type substrate, the interface states will give a net negative charge at the flat band condition whereas they will give a net positive charge for a p-type substrate. The charge due to interface states is therefore

$$Q_{it} = q \int_{E_f}^{E_i} D_{it}(E)\, dE.$$

If a MOS device is exposed to ionising radiation, both the density of charge within the oxide and the density of interface states will increase. The flat band voltage will change by an amount known as the flat band voltage shift, ΔV_{fb}. The flat band voltage shift can be written as

$$\Delta V_{fb} = \Delta V_{ot} + \Delta V_{it}$$

where ΔV_{ot} is the shift due to radiation induced charge within the oxide and ΔV_{it} is the shift due to the increased interface state density.

$$\Delta V_{ot} = -\int_{0}^{d} \frac{x\rho_i(x)}{C_o d}\, dx \quad \text{and} \quad \Delta V_{it} = -q \int_{E_f}^{E_i} \frac{\Delta D_{it}(E)}{C_o}\, dE$$

where $\rho_i(x)$ is the density of charge in the oxide due to the ionising radiation and $\Delta D_{it}(E)$ is the change in the interface state density.

$\rho_i(x)$ is dependent on many factors including the quality of the oxide, the rate and nature of the irradiation and the temperature. Electron-hole pairs are created along the path of the ionising radiation through the oxide. In the previous section it was shown that a fraction of these will recombine. If an electric field is present, the electron-hole pairs will be separated and the recombination will be significantly reduced. Electrons are extremely mobile in SiO_2 even at low temperatures and those that do not recombine rapidly move out of the insulator leaving a net positive charge and a negative flat band voltage shift. The actual time for removal is dependent on the applied field but in general the electrons will be swept out within a few picoseconds. In contrast to the motion of electrons, holes move very slowly and their transport is by a complicated trap hopping process. As holes are transported through the oxide the positive charge distribution will change. If there is no permanent hole trapping then the holes will eventually be swept out of the device and there will be a total recovery of the flat band voltage shifts. The hole mobility is a strong function of temperature. Therefore the time for flat band voltage recovery will also show a strong temperature dependence. This is illustrated in Figure 1.26.

This assumes that there will be no electron or hole trapping. However there will be

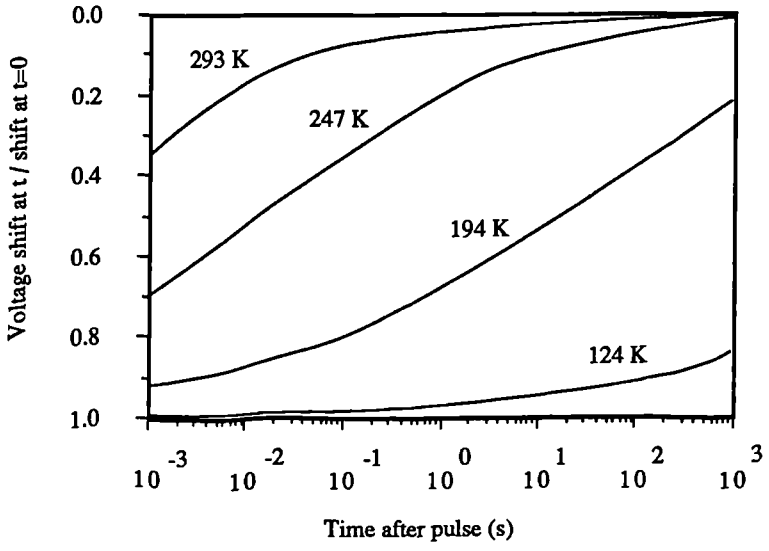

Figure 1.26. The normalised flat band voltage recovery with little hole trapping as a function of temperature following a short ionising radiation pulse [34].

hole traps in the vicinity of the Si/SiO_2 interface and at the gate silicon interface. The trap densities range from 10^{12} cm^{-2} to 10^{13} cm^{-2} and depends on the manufacturing process [35]. There will also be electron trapping in the oxide which takes place throughout its bulk. However the electron traps are at least 1000 times less effective than the hole traps.

If the field across the oxide is such that the radiation induced holes move towards the Si/SiO_2 interface then a fraction of the holes are trapped at the interface and remain to form a sheet of positive charge. The position of the charge sheet for different gate biases is shown in Figure 1.27, together with the gate insulator structure of the UT101 CCD. For good quality but unhardened oxides, that is to say those that have not been produced especially to reduce the hole traps, the total fraction of radiation induced holes that form this sheet can be as high as 20% and can be as low as 1% for hardened oxides.

The deposition of 1 rad(SiO_2) of ionising radiation implies that there will be 3.5 10^{15} electron hole pairs produced per kg of SiO_2 assuming that 18 eV is required for each electron hole pair. If the fraction of trapped holes is F_t, absorbed dose in the oxide is D and the fraction electron hole pairs that escape initial recombination is F_e then the amount of charge per cm^2 forming this sheet is

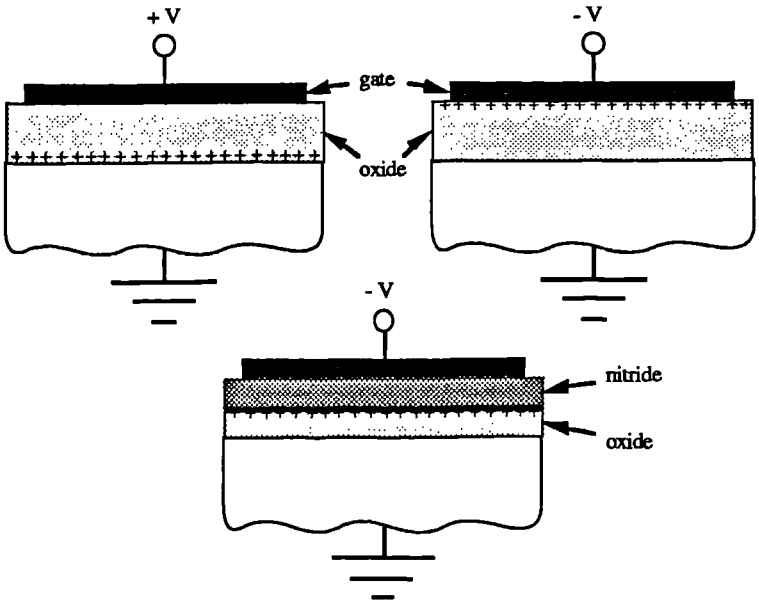

Figure 1.27. A schematic of the position of the positive charge sheet for MOS and MNOS structures.

$$Q_{ot} = 7.7\ 10^{12}\ qdDF_tF_e \qquad (1.10).$$

As this sheet is at the Si/SiO_2 interface it causes a flat band voltage shift given by

$$\Delta V_{ot} = Q_{ot}/C_o = dQ_{ot}/\varepsilon_o.$$

This reduces to

$$\Delta V_{ot} = -\ 3.6\ 10^{-8}\ d^2\ D\ F_tF_e$$

where d is the oxide thickness measured in nanometres. From this it can be seen that there is a very strong oxide thickness dependence. One way to significantly reduce the flat band voltage shifts is to reduce the thickness of the gate oxides. If F_e is 1 which would be the case for 5 MeV electron irradiated samples, with an oxide field of 5 MV/cm and F_t was 10% then a flat band voltage shift for a sample with a 100 nm oxide would be around -0.4 Volts per 10 krad. For a 50 nm oxide this reduces to -0.1 Volts per 10 krad.

The above would hold for devices where the motion of holes is in the direction of the bulk silicon. In devices where the field is such that the holes move towards the gate then the flat band voltage shift is reduced to almost zero when the motion of holes is complete. This can be seen in the room temperature curve of Figure 1.28. This also shows the effect of low temperature irradiation. There is an overall increase of the flat band voltage shift at temperatures below around 200K as relatively shallow trapping centres are able to retain the trapped holes. At

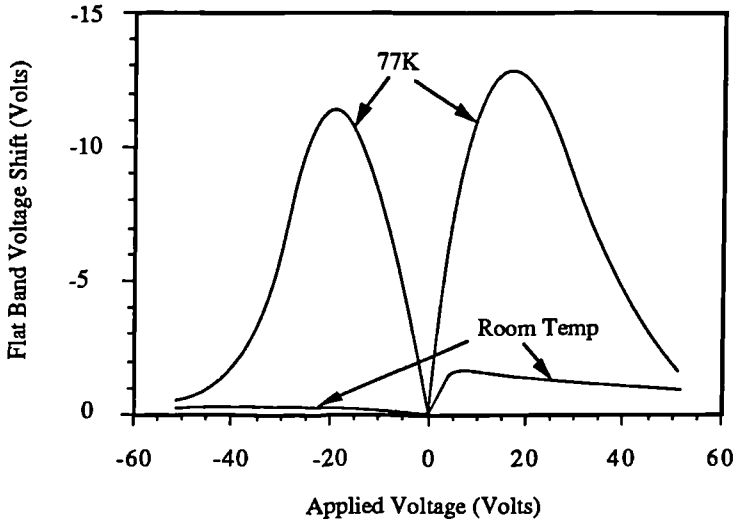

Figure 1.28. Flat band voltage shift at 10^5 rad(Si) versus applied voltage for MOS capacitors irradiated at 77 K and at room temperature. (After Srour *et al* [36])

temperatures as low as 77K the holes remain virtually fixed at the point of creation and so there will be significant voltage shift even with a negative gate bias. However, as the device is warmed up to room temperature, the holes start to move and the flat band voltage shift is reduced to that which would have been obtained if the MOS structure had been irradiated at room temperature.

The field in the insulator is in the optimal direction for the UT101 CCD when biased during irradiation. However, a complication arises as a Si_3N_4/SiO_2 sandwich structure is employed for the gate insulator. Little net radiation induced charge is left in the nitride layer as electron and hole recombination is high due to their similar mobilities and those that do escape initial recombination are trapped near their point of creation even at room temperature. Therefore the nitride layer can be regarded as being radiation hard [37]. The electrons produced in the oxide are swept out into the bulk silicon. The holes move slowly towards the nitride layer and they are trapped at the Si_3N_4/SiO_2 interface forming a sheet of positive charge. The amount of charge per cm^2 in the sheet is given by equation 1.10 where d in this case is the thickness of the oxide layer. This causes a flat band voltage given by

$$\Delta V_{ot} = Q_{ot}/C_n = d_n Q_{ot}/\varepsilon_n.$$

where C_n is the capacitance per unit area of the nitride, d_n is the thickness of the nitride and ε_n is the permittivity of the nitride. This reduces to

$$\Delta V_{ot} = - 1.9\ 10^{-8}\ d\ d_n D\ F_t F_e \qquad (1.11)$$

if d and d_n are in nanometres. This implies that if $F_e = 1$ and $F_t = 10\%$ then for an insulator layer of 100 nm with equal thicknesses of Si_3N_4 and SiO_2 the flat band voltage shift would be -0.05 Volts per 10 krad.

The change in the interface state density, ΔD_{it} , with irradiation is dependent on several factors [38]. For example, the increase is greater for wet grown oxides than dry oxides and is dependent on the oxide thickness. It appears that the interface state build up is virtually independent of ionising radiation energy and increases in proportion to D^n where n ranges between 0.6 and 0.9. As in the preirradiation case, those radiation induced states in the upper half of the band gap appear to be acceptor like and those in the lower half of the gap behave as donors. They have a similar distribution in the band gap as unirradiated samples. However, for high doses there is an increase in the upper half of the band gap, forming a peak around 0.2-0.3 eV above mid gap.

ΔV_{it} resulting from the increased interface state density will be negative for a p-type substrate but positive for an n-type substrate. This implies that an increase in interface state density serves to enforce the flat band voltage shift due to the trapped oxide charge for a p-type substrate but reduces the total flat band voltage shift for an n-type substrate. The total flat band voltage shift, ΔV_{fb}, for n-type samples is dominated by the trapped oxide charge at low doses and is negative. However, at high doses the effect of the interface states starts to dominate due to the saturation of hole traps and the flat band voltage can return to its preirradiation value. For even higher doses the flat band voltage shift can become positive.

As well as effecting the flat band voltage, an increase in interface state density causes a decrease in the surface mobility of MOSFETs. The radiation induced states also increase the generation recombination and trapping processes at the interface which are important for CCD operation.

The process by which ionising radiation increases the interface state density is not yet completely understood. A thorough review of the subject has been given by Oldham *et al* [39]. There are three basic sets of models to explain the build up of interface states:

i) A two stage model where radiation generated holes free hydrogen ions in the SiO_2 bulk as they transport through the oxide. The liberated hydrogen ions then under go a dispersive hopping transport to the Si/SiO_2 interface where they are converted to interface traps.

ii) Injection models, in which neutral hydrogen diffuses to the interface. When the hydrogen reaches the interface it could be converted into a trap by the chemical reaction that followed electron injection from the substrate.

iii) Trapped hole models where a hole is trapped near the Si/SiO_2 interface and eventually converts into an interface state. For example, the so-called bond strain gradient (BSG) model assumes that a radiation induced hole is trapped in a narrow strained region near the Si interface. The Si-O bonds are more strained closer to the interface. The trapping process breaks a Si-O-Si bond, leading to a trivalent Si atom which is not mobile and a mobile non-bridging oxygen. The non-bridging oxygen propagates to the interface, relieving more and more strain as it goes. When it reaches the interface, an unspecified reaction occurs and an interface state results.

It is likely that one or more processes are involved in the interface state generation.

1.3.3. Radiation Effects in CCDs

As apparent from the previous sections, CCDs are sensitive to both ionising and bulk damage effects. They are also very susceptible to transient ionising radiation induced loss of stored information. A review of the main radiation effects of concern has been given in reference [40]. The main points are given below.

Ionising radiation causes charge build up in the gate insulator giving a change in the ideal operating voltages which in turn decreases the charge handling capability and increases the power consumption. If the voltage shift is great enough the CCD will cease to operate. Ionising radiation also causes the interface state density to increase. This increase reduces the charge transfer efficiency in surface channel devices and increases the dark current in both surface and buried channel CCDs. Unless suppressed, this increase in dark current limits the CCD operation to a maximum dose dependent on the integration time. For a TV application this limit is in the order of 100 krad(Si) at room temperature for an unhardened device. The details of the effect of voltage shifts and dark current generation are given in Chapter 3.

Bulk damage causes the charge transfer efficiency to degrade. It also causes increased charge carrier recombination leading to a reduction in the minority carrier lifetime and diffusion length. As a result, the sensitivity of the CCD is reduced. Protons, neutrons and heavy ions tend to produce clusters of damage resulting in local areas of high dark current (dark current spikes).

Earliest work on radiation damage of CCDs showed that the radiation tolerance of the devices could be increased if the following guidelines are followed:

i) Buried channel structures should be used so the CTE is not degraded by the increase in interface state density.

ii) n-channel structures should be used as the voltage shifts are reduced. In such devices the field in the insulator causes radiation induced holes to move away from the Si/SiO_2 interface.

iii) A planar insulator should be employed so that voltage shifts are equal under adjacent electrodes. Unequal voltage shifts cause potential barriers to form that prevent the transfer of charge.

iv) The design must allow control over the surface potential between electrodes. Otherwise "potential pockets" will form, reducing the charge transfer efficiency. This control can be achieved by employing overlapping gate technology.

v) The reverse bias applied to the buried channel must be large enough to keep the channel depleted after irradiation. The voltage shifts increase the reverse bias required for depletion. Alternatively, a tracking system can be employed to monitor the voltage shifts which can then make corrections to the applied biases.

However, even if the design of the CCD is optimised using the above techniques, it will still be sensitive to bulk damage. This is particularly important for low signal application.

1.4. CCDs as detectors of ionising particles

CCDs have been successfully used to detect X-rays for X-ray astronomy applications and minimum ionising particles (MIPs) for high energy particle physics applications. Both these situations involve small signals (~1000 electrons) in an otherwise dark background. This is in contrast to a typical signal size of 50,000 electrons superimposed on a bright background for standard optical imaging applications. Both X-rays and MIPs generate charge within the bulk silicon of the CCD. However the distribution of generated charge differs, as shown in Figure 1.29.

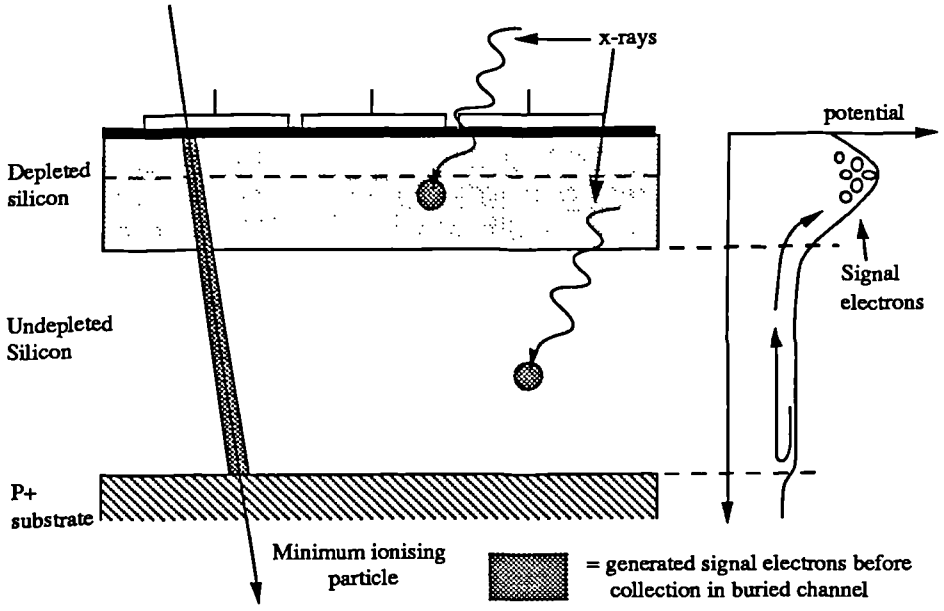

Figure 1.29. A schematic cross section of a CCD showing how minimum ionising particles and X-rays deposit charge.

1.4.1. The application for high energy particle physics

CCDs have been used to track the passage of minimum ionising particles produced in particle physics experiments. A minimum ionising particle crossing the CCD, leaves a radial column of charge within 1 μm of its trajectory. Charge in the depleted silicon is rapidly collected into the buried channel due to the high fields in this region. Charge from the undepleted silicon diffuses into the channel. The potential barrier between the epitaxial p-type silicon and the p^+ substrate reflects almost all of the electrons that diffuse towards it (>95%). As a consequence, most of the charge generated in the epitaxial layer is collected. Typically, for the EEV CCD, 3-4 pixels collect the charge with about 80% in the central pixel [41]. The charge in the outer pixels allows the determination of the centroid of the cluster. This helps to improve the spatial resolution.

Particle physics requires detectors with high spatial resolution (around 5 μm), good two track resolution, and minimum mass [42]. Minimum ionising particles typically deposit a signal of around 1300 electrons in the "standard" UT101 CCD. However, due to Landau fluctuations, the minimum signal size can be as low as 300 electrons. If the epitaxial layer is increased to 50 μm from 20 μm, the typical signal size increases to 3250 with a minimum signal size of 1750 electrons. These devices are only employed to measure the spatial position of particles so good energy resolution is not necessary. This implies that the charge transfer efficiency is not as critical a parameter as in X-ray spectroscopy.

1.4.2. The application for the detection of X-rays

X-rays convert to an electron via the photoelectric effect. These electrons have a very short range in silicon (around 1 μm for a 10 keV electron). Therefore charge deposition is very localised. Charge from an X-ray converting in the depleted silicon is rapidly collected into a single pixel. An X-ray converted in the undepleted silicon gives rise to a multiple pixel hit as the charge diffuses to adjacent pixels.

CCDs have proved very important in space-borne X-ray astronomy applications [43]. They provide excellent energy resolution combined with the intrinsically high spatial resolution. The energy resolution performance is obtained by looking at events isolated to a single pixel as the resolution is degraded by signal spread. The number of single pixel hits can be increased by increasing the depletion depth. This can be accomplished by utilising a higher resistivity epitaxial material. To detect the lowest energy photons it is necessary to illuminate the CCD through the thinnest possible dead layer. The CCD can be thinned to match the total thickness to the

depletion depth and then illuminated from the back. Utilising thinned devices enables X-rays to be imaged down to 280 eV [44]. However, of particular interest for spectroscopic applications are the 6-7 keV iron line complexes. For these energies the CCD can be illuminated from the front. The signal size obtained for a 6 keV X-ray is around 1700 electrons.

1.5. Operating CCDs as particle detectors in a radiation environment.

1.5.1. Astrophysics' environment

The CCDs intended for extraterresrial, X-ray spectroscopic applications are very sensitive to bulk displacement damage as charge transfer degradation due to bulk defects seriously degrades the energy resolution. There will be a variation in the amount of signal lost dependent on the pixel position. This impedes the energy calibrations. Further more, the signal to noise of the measurements is degraded due to the shot noise fluctuations in the charge loss. Outside the protection provided by the Earth's atmosphere, there are several sources of radiation that are a hazard to CCDs. Two of these sources stem from solar activity whilst the third originates from sources outside the solar system.

One of the major threats to the operation of CCDs is the occurrence of solar flares which are connected to an increase in solar activity. This activity fluctuates with an eleven year periodicity although the true cycle length is thought to be 22 years. Accompanying the solar flares large proton fluxes are produced. These proton emissions are observed essentially at the maximum solar activity. The sporadic emission can last between several hours and several days and energies up to several hundred MeV can be produced with fluences above 10^{10} cm^{-2}. Some of these events are accompanied by the emission of electrons and heavy ions whose spectra and composition are variable from one event to another.

The Sun's gaseous halo (the corona) is at a very high temperature. The lighter constituents have enough thermal energy to be continuously ejected into space. The density of this 'solar wind' decreases as the distance from the Sun squared. It is mainly composed of protons and electrons whose energy is less than a few keV. The flux of particles is dependent on the solar activity and may vary as much as a factor 20. As the particles are low energy their effect on CCDs should be negligible.

Cosmic radiation constitutes a background which is continually supplied with ions whose energy can be as high as several TeV. It originates from far off galactic and extra galactic localised sources although, by the time it reaches the solar system, it appears isotropic. This source of radiation produces localised clusters of damage in the CCD.

The main cause for concern is the effect of high energy protons and electrons that form radiation belts around the planets of the solar system. The radiation belts around the Earth are the most important as a large majority of applications are for observation in an Earth orbit. If the energy and angle of incidence of the incoming charged particles is favourable then they may be trapped in the Earth's magnetic field and form radiation belts (Van Allen belts). The trapped particles gyrate around the magnetic field lines and oscillate between two mirror points. Trapped electrons form two zones, an inner zone and an outer zone. The fluxes in the outer zone can exceed those of the inner zone by about an order of magnitude. The energy of the inner zone electrons is less than around 5 MeV whilst the energy of the outer zone electrons can be greater than 7 MeV. In contrast the energetic trapped protons (>5 MeV) cannot be assigned zones. The energy of the trapped protons can be as high as a few hundred MeV and decreases for trajectories further from the Earth.

Most electronic components can be shielded from a majority of the hazardous radiation. However, by necessity, CCDs intended for X-ray astronomy have to be left unshielded in the direction of observation. Mechanical shutters can be employed when crossing the radiation belts. However, this introduces an unwanted complexity to the design of the payload and increases the experiment's mass where mass restraints are critical. Therefore, careful choice of the satellite's orbit is necessary to reduce the interaction with the radiation belts. Typical ionising dose for a mission such as the European Space Agency's X-ray spectroscopic mission, the XMM, is expected to be around 13 krad(Si) for a ten year mission with a proton fluence of around 10^9 cm^{-2} [45].

1.5.2. The high energy particle physics' environment

The radiation tolerance for CCDs intended for a particle physics application is not as critical as the X-ray astronomy application. CCDs have been used in the NA32, fixed target experiment at CERN and are being employed in the SLD vertex detector at SLAC. In the NA32 experiment, the CCDs were placed 10 mm and 20 mm down stream of a copper target onto which a beam of 200 GeV/c pions was incident. The purpose of the CCDs was to detect and map the trajectory of the minimum ionising debris of the interaction. The main cause for concern was the

damage produced by the 200 μm beam traversing the CCDs. This caused a localised area of damage, equivalent to an ionising dose of 100 krad(Si) over the life time of the experiment.

The SLD vertex detector uses CCDs to investigate the minimum ionising products from the electron positron interaction. Two linear beams with a centre of mass energy of 100 GeV are brought to a collision at a single interaction point. The vertex detector surrounds the interaction point but the beams themselves are not incident on the CCDs. Typical concerns for the CCDs of the vertex detector [46] are due to the ionising radiation originating from synchrotron radiation from the beams in the final bending magnets and quadrupoles. Direct synchrotron radiation is screened by a series of masks but secondary scattering and X-ray fluorescence are important. The ionising dose experienced by the CCDs closest to the interaction point is expected to be less than 10 krad(Si) per year. Neutron backgrounds from the beam dumps have also been considered but are not thought to be significant.

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CHAPTER TWO

General Experimental Details

2.1. Introduction

In order to investigate the effect of radiation on the performance of the CCDs it is necessary to characterise the performance before and after irradiation. There are several parameters of importance and the details of the experimental techniques employed to obtain these parameters are given in the relevant chapters. In this chapter the common experimental procedures are described.

2.2. The operation of the CCDs

2.2.1. Drive Electronics

For most of the measurements on the degradation it was necessary for the CCD to be running. That is to say, suitable biases and clock pulses had to be employed to move signal charge packets around the device. The system used to drive the CCDs originated from the prototype electronics for the NA32 experiment at CERN [1]. A block diagram of the electronics is shown in Figure 2.1.

Before the CCD could be clocked, the CAMAC module (labelled master controller) had to be loaded with a user defined instruction set from the PDP11 microcomputer. This defined the sequence of functions to be executed by the triplet generators. The master controller provided the triggers for each triplet generator. The triplet generators provided the timing information for the pulses to be applied to

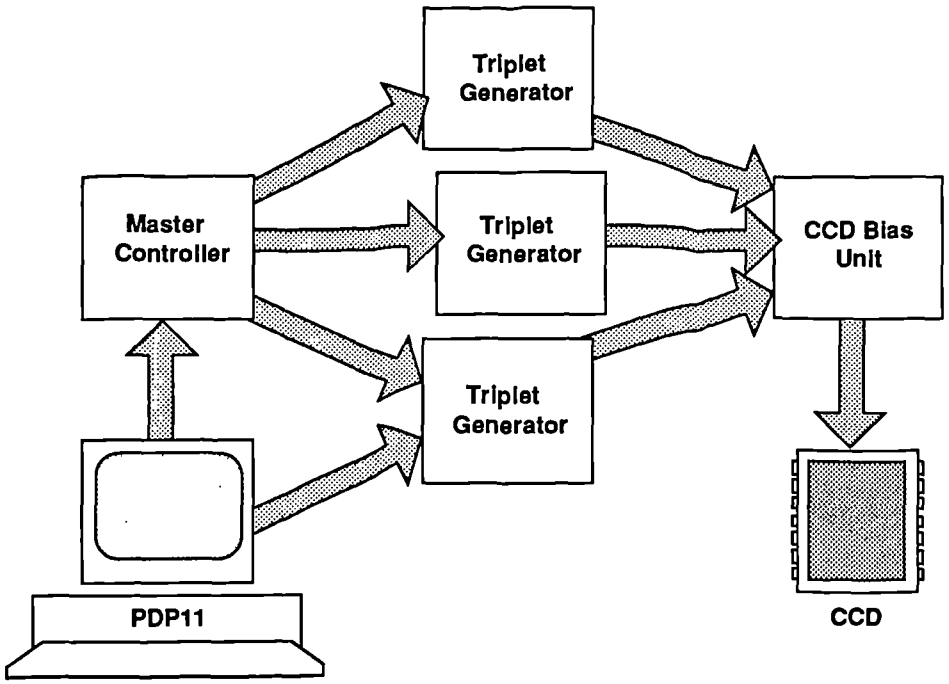

Figure 2.1. The CCD drive electronics.

the gates of the CCD. There were three triplet generators, one for the image section, the store section and the readout register. Each supplied three pulses, one for each phase of the CCD. The pulse width and delay were set up by the user via the PDP11. This provided a very flexible system allowing almost any drive pulse sequence. For example, in order to clock charge down one row and then out of the device, the commands to provide an image section triplet, followed by a store triplet, followed by 400 readout triplets would be loaded into the master controller. The master controller could be set up to provide a continuous sequence of triplets, allowing the CCD to be clocked continuously. It could also be configured to provide a user defined integration time before the collected signal was clocked out of the device.

Along with the drive pulses, it was also necessary to provide a suitable reset pulse to apply to the reset FET of the output circuit after every pixel had been transferred to the output node.

The pulses from the triplet generators were ECL logic levels. These pulses had to be modified to the required shape and amplitude by the CCD bias unit. This also provided the DC levels for the output circuit and substrate etc. The bias unit was 10 m from the CCD but the clock drivers were provided locally. The maximum readout rate achievable using this system was around 1 MHz although generally a readout rate of 83 kHz was employed.

2.2.2. Obtaining an image from the CCD

In general, for most of the work described in this thesis, it has not been necessary to obtain an image from the device. Instead, the output voltage levels were monitored using oscilloscopes, and the dark currents measured using a high input impedance voltmeter connected across a resistor. However, as part of the batch qualification of the CCDs destined for the SLD vertex detector, it was specified that the devices had to continue to image a weak beta source after irradiation. A schematic of the imaging system employed is shown in Figure 2.2.

The on-chip output FET of the CCD was set up as a source follower and the output taken to a preamplifier situated close to the CCD. After the preamplifier of gain 7.0, the signal was fed to a main NIM amplifier with a variable gain. This was typically set to 40 although higher gains could be achieved by cascading several amplifiers. In order to remove "reset" noise (see chapter 5) correlated double sampling was employed utilising a dual slope integrator (DSI). The output of the main amplifier was integrated over the time set by the timer module with no signal present at the output node of the CCD, i.e. during the period between the reset of the output node and the transfer of signal charge. The DSI was then gated off while signal charge was being transferred to the output node. The DSI was then gated on again, once the transfer of charge was complete, for a period equal to the first but with the opposite sign of integration. The final output level of the DSI reflected the

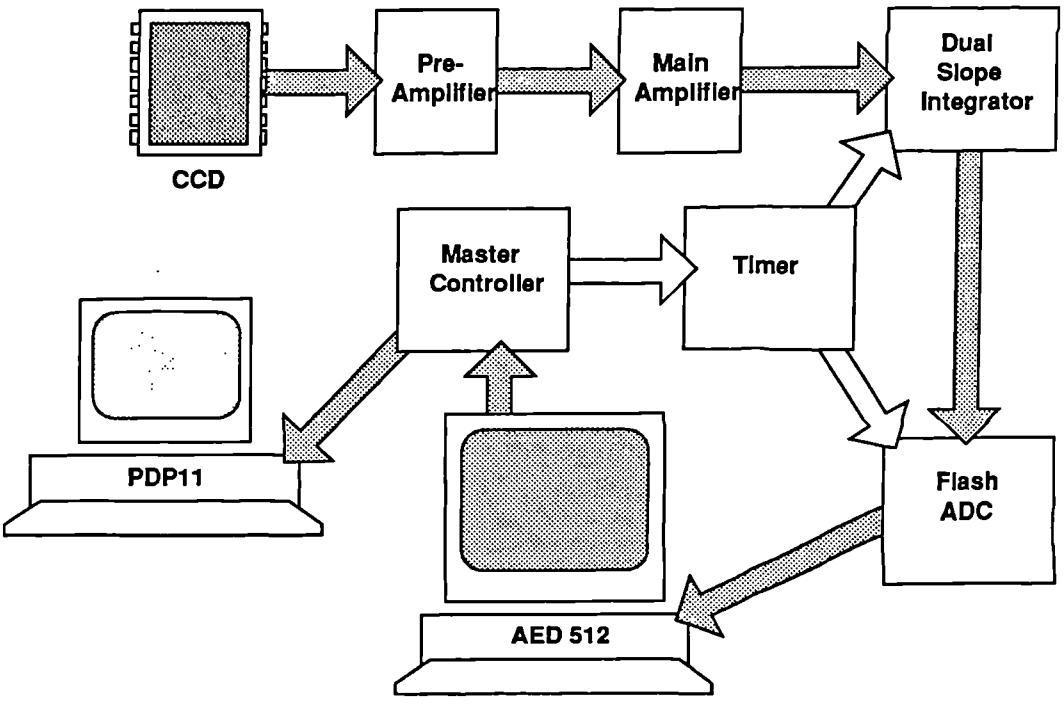

Figure 2.2. The image acquisition system.

difference between the output of the CCD with and without signal charge, and so the reset noise was removed. For maximum stability, the trigger for the timing module was derived from the readout register triggers from the master controller.

The final DSI level was sensed by a 6-bit flash ADC, and the digital output from each pixel was sent to the memory of an AED 512 colour graphics terminal. This allowed an image to be inspected on the screen with various colour maps. A direct memory access via CAMAC allowed the rapid transfer of frames of data between the AED 512 and the PDP11.

2.2.3. Temperature control

For many applications it is necessary to cool devices to reduce thermally generated backgrounds to insignificant levels. To mimic actual device operation, and to perform measurements on device degradation, it was necessary to provide a cooling system for the devices under test. It was also necessary to provide a heated environment to investigate the possibility of annealing the radiation induced damage.

Cooling was achieved by passing cold nitrogen gas, that had been boiled off from liquid nitrogen, through a narrow steel tube that had been welded to a copper plate. The CCD was clamped to the copper plate and good thermal contact was achieved by employing a small amount of silicone grease between the plate and the CCD. The temperature of the CCD was monitored via two "T-Type" thermocouples buried in the copper plate. To prevent icing the CCD was housed in a vacuum chamber that was evacuated to below 10^{-4} torr by using rotary and diffusion pumps. Using this cooling system the temperature could be brought down to 90K, from room temperature, within half an hour.

A 100Ω, 100W resistor was mounted below the copper plate. This enabled the CCD to be heated by passing a current through the resistor. The maximum temperature that could be achieved was approximately 450K. It was also possible to purge the vacuum system with nitrogen so annealing studies could be carried out in a nitrogen atmosphere.

The above allowed a crude but effective temperature control system to be employed by utilising a CAL9000 proportional temperature control unit. The input to the control unit was connected to one of the thermocouples and the output switched the voltage across the heating resistor. A suitable flow rate of cold nitrogen gas was set manually (the lower the required temperature, the greater the flow). This then remained fixed. When the temperature of the CCD approached the required

temperature from above the controller started to allow current through the resistor, thus reducing the rate of cooling. As the CCD started to warm up the controller turned the current off, allowing the CCD to be cooled again. Providing that there was sufficient supply of liquid nitrogen, the CCD could be kept at the required temperature for a couple of days. By setting a suitable control current and gas flow rate, the temperature could be controlled to within ±1K.

2.3. Irradiation Details

2.3.1. Irradiation using a Sr^{90} beta source

Sr^{90} is a convenient source of damaging radiation as it can be used within the laboratory without the bulky shielding that is required for gamma sources. The spectra of the betas from a Sr^{90} source is actually composed of betas from the $Sr^{90} \rightarrow Y^{90}$ decay with an end point energy of 549 keV and the $Y^{90} \rightarrow Zr^{90}$ decay with an end point energy of 2283 keV [2]. There are equal numbers of beta particles emitted from the source from each of the decays. The energy spectra calculated from the momentum spectra given in [3] is shown in Figure 2.3.

A Sr^{90} source, with a nominal activity of 20 mCi, was mounted at the end of a brass plunger, housed in a shuttered lead container. The source mounting is illustrated in Figure 2.4. With the shutter open the source could travel approximately 2 cm towards the opening. Keeping the shutter closed, the housing was bolted onto the irradiation rig. When exposure was to commence, the shutter

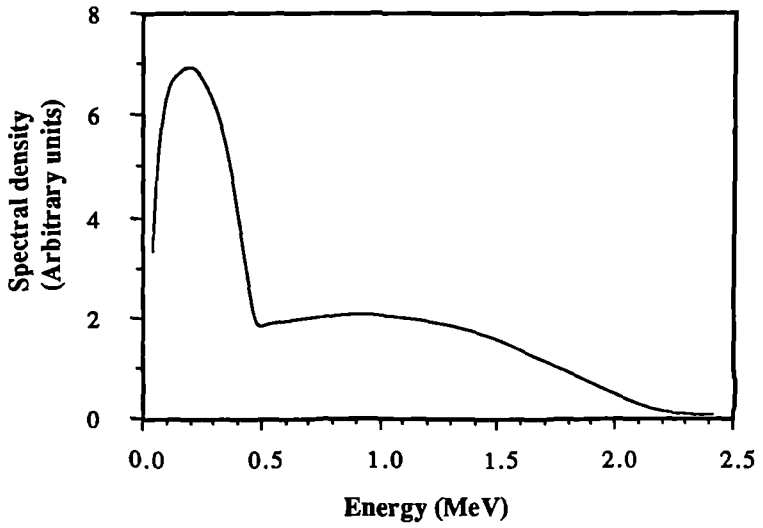

Figure 2.3. The energy spectra of the betas from Sr^{90}.

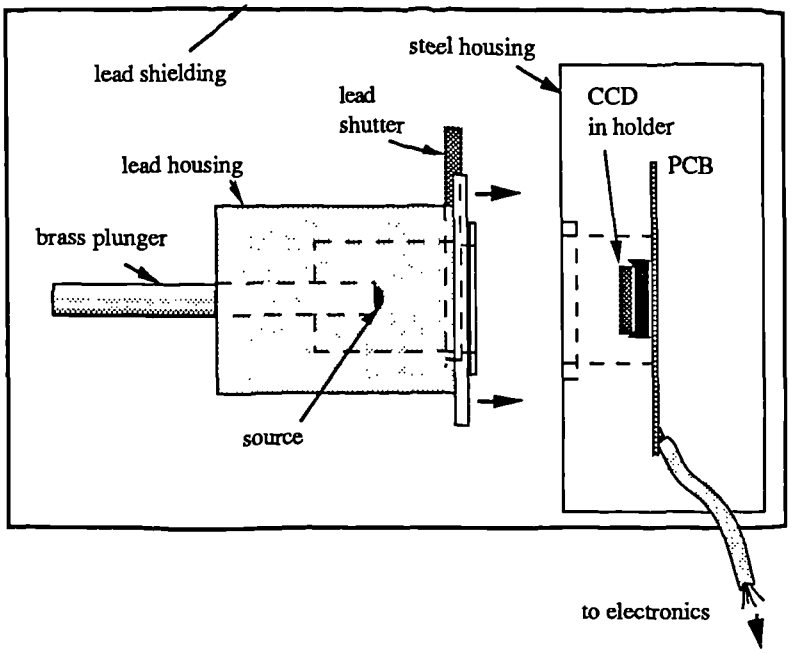

Figure 2.4. A schematic of the source enclosure and radiation rig.

could be opened and the source position altered to obtain the required dose rate at the CCD.

The radiation rig consisted of an aluminium enclosure with a mounting able to accept a CCD. Electrical connections were available to bias the gates, drains and substrate of the CCD. This was necessary to allow initial monitoring of the dose. However, after the initial adjustment of the dose rate, the CCD was generally kept unbiased during irradiation, with all the connections grounded. Most of the irradiations were carried out at room temperature. However, low temperature irradiations could be carried out, whilst the device was clocking, by placing the source over the main vacuum rig.

2.3.2. Irradiation using a Co^{60} gamma source

Co^{60} irradiations were undertaken to provide a check of the Sr^{90} dose measurements. Unlike the betas from Sr^{90}, high energy gamma rays can deposit a uniform dose throughout a sample, even in relatively thick objects. Co^{60} is also the source of ionising radiation used by most workers concerned with radiation hardness testing. Therefore it was important to be able to relate the Sr^{90} results to Co^{60} irradiations.

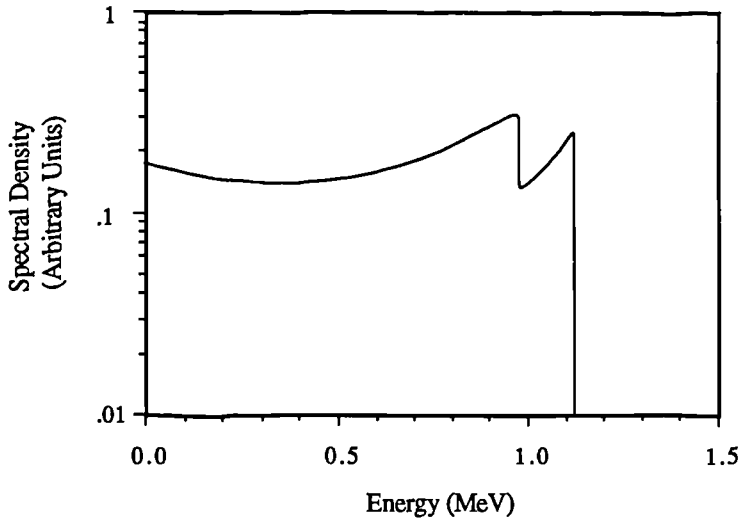

Figure 2.5. The energy distribution of the secondary electrons from Co^{60} irradiation of a silicon sample.

Co^{60} decays, via beta decay with a half life of 5.26 years, to a metastable state of Ni^{60}. The metastable Ni^{60} decays to its ground state via two successive transitions with the emission of a 1.17 MeV and a 1.33 MeV gamma ray. These gamma ray photons then impart their energy to electrons in the irradiated sample predominantly by Compton scattering. These electrons go on to damage the material. The energy distribution of these secondary electrons has been calculated for silicon samples [4] and is shown in Figure 2.5.

In order that the dose distribution is constant through the sample it is necessary that charged particle equilibrium (CPE) exists. By definition, CPE exists when the total energy carried out of a mass element by electrons is equal to the energy carried into it by electrons. Consider a beam of gamma ray photons incident on a homogeneous sample as in Figure 2.6. An elemental volume near the front face of the slab would have more electrons scattered out of it than are scattered in. Therefore less ionising dose is received at points before this elemental volume than after it. However, further into the sample a depth is reached where CPE is achieved. The minimum thickness of material required to achieve CPE is approximately equal to the range of the highest energy secondary electron [5]. The range for a 1 MeV electron in silicon is approximately 2 mm. Therefore it is clear that, unless material is placed between the source and the CCD, there will be a dose gradient through the device. This implies that the measured dose would be greater than that deposited in the insulator layers.

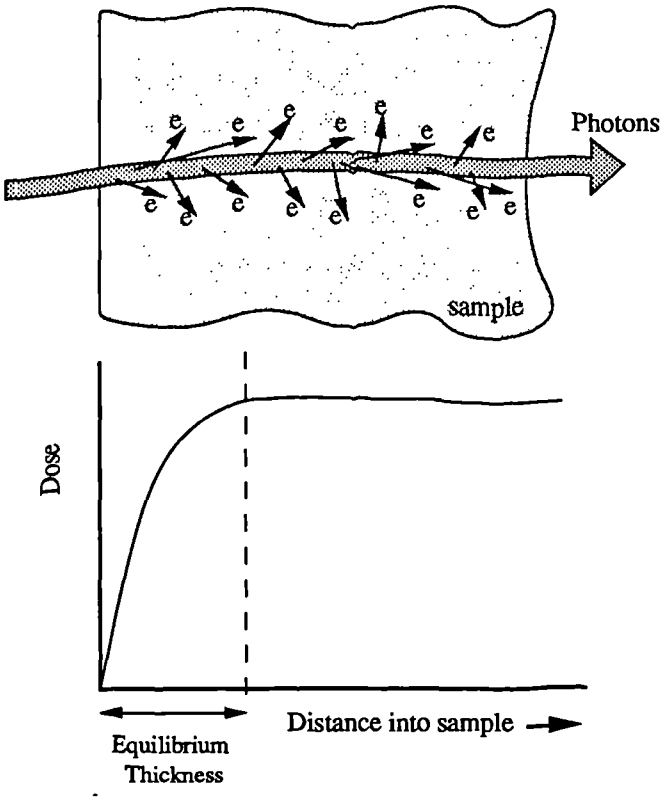

Figure 2.6. The distribution of dose through a homogeneous sample.

The devices were irradiated at the radiation facility situated within the department of physics. This consists of a large shielded cell housing a Co^{60} source. At the time of the measurements the source strength was 4.5 Ci The source was attached to the end of a wire spigot. When not in use it was housed underground but could be wound out to the end of a flexible cable. Once deployed, the source was housed in an outer brass capsule. The wall thickness of the capsule was around 5 mm thus ensuring that CPE was obtained. This could be placed anywhere within the shielded cell. For the irradiations the source was set up at the centre of the cell, around 3m from the concrete walls, to reduce low energy scattered gammas. The CCD under test was mounted on a PCB enclosed in a light tight plastic box with a large 300 μm Mylar window. Electrical connections were made from the CCD to a control room outside the cell in order to measure the dose. The position of the CCD relative to the source could be adjusted remotely to obtain the required dose rate. A dose rate of 1 krad/h was obtained for a source-device distance of around 10 cm.

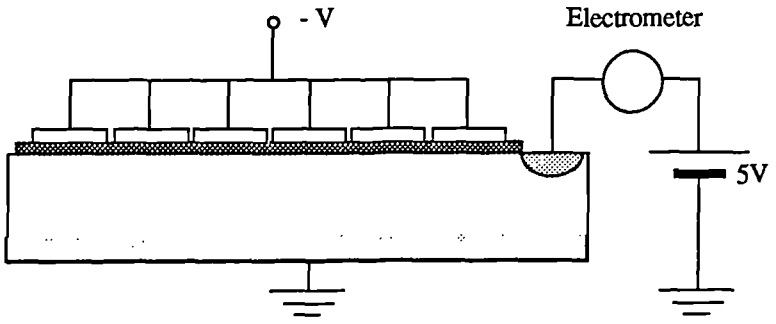

Figure 2.7. The CCD connections for the dose measurements.

2.3.3. Dosimetry

The dose was measured by monitoring the current induced in the CCD at the start of irradiation. All the gates were connected together to form a large depletion mode MOSFET. All the drains were connected together and the current between the drains and earth was monitored using a Keithley 617 electrometer (Figure 2.7). The measured current is shown in Figure 2.8 as a function of the voltage applied to the gate electrodes. It is apparent that the measured radiation induced current is

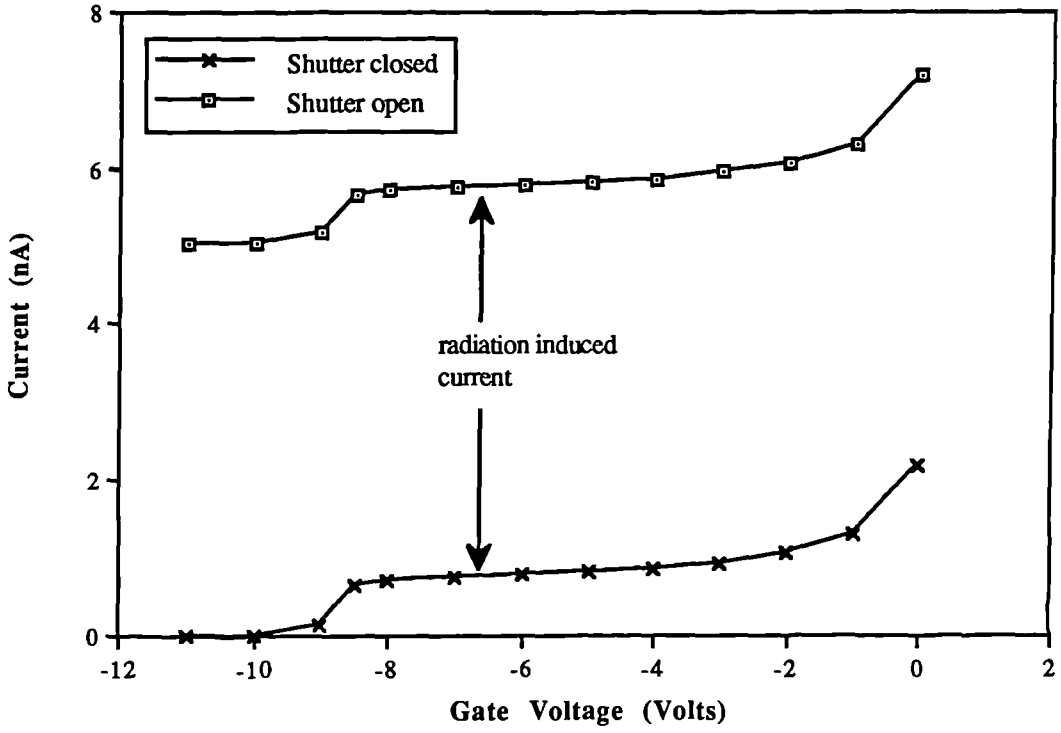

Figure 2.8. The measured current for the derivation of the dose rate obtained using the Sr^{90} source.

independent of the gate voltage.

In order to calculate the dose rate, it is assumed that all the electron-hole pairs are collected from the epitaxial layer. This layer is 20±2 μm deep and the device area is 8.5 mm by 12.7 mm. Assuming that it takes 3.6 eV to liberate one electron hole pair then the dose rate in krad per hour is given by

$$\frac{dD}{dt} = \frac{5.1I}{d}$$

where I is the measured current in nA and d is the expitaxial thickness in μm.

This is a convenient method for measuring the dose rate. However, some electron hole pairs created in the substrate can diffuse into the epitaxial layer thus contributing to the current. The actual dose rate will therefore be lower than that measured. The substrate is doped p-type with 5 10^{18} cm^{-3} boron atoms. According to [6] such an impurity concentration gives a minority carrier lifetime in the order of 100 ns and a diffusion constant of 4 cm^2s^{-1} at 300K. This gives a diffusion length around 6 μm. The actual value will be even lower than this as the substrate acts as a getter for impurities originally in the epitaxial layer and the impurity density could be significantly higher than the dopant density. Therefore the charge contribution from the substrate will be insignificant when compared with

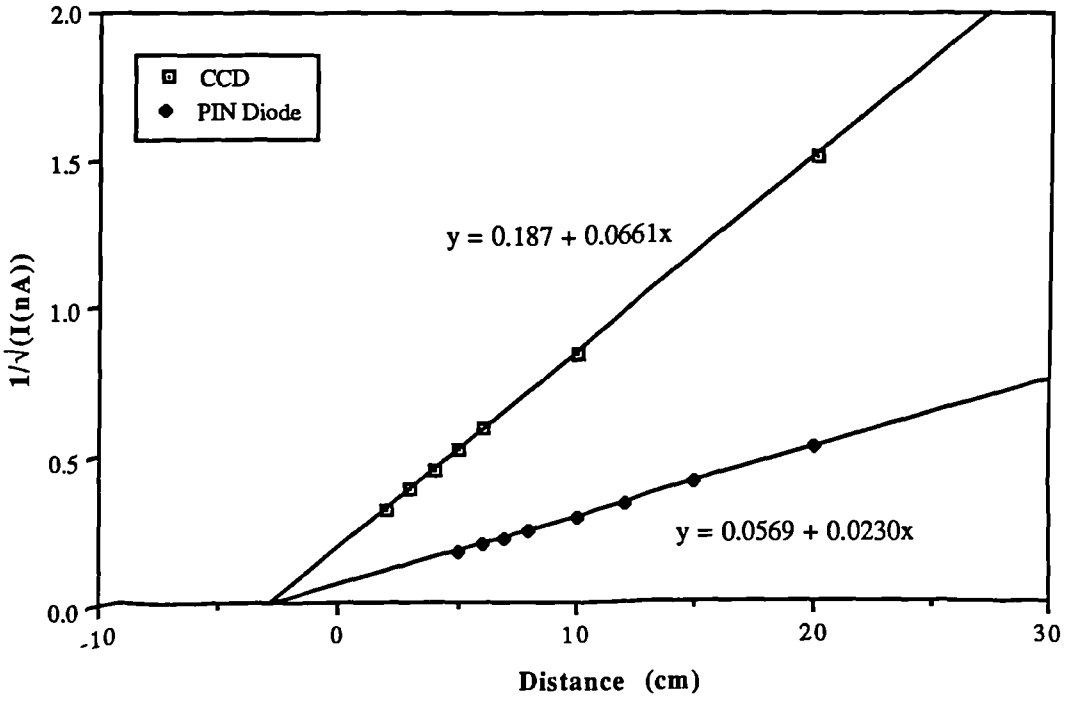

Figure 2.9. The measured (induced current)$^{-0.5}$ versus measured distance for the CCD and a Hamamatsu S1723-03 PIN diode.

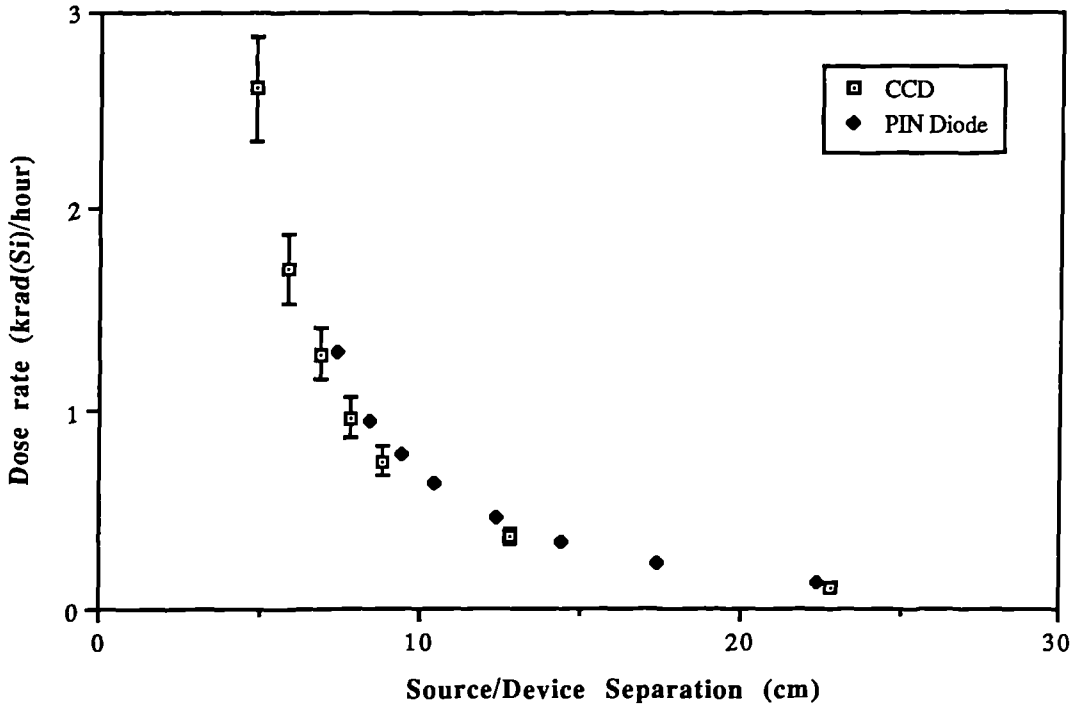

Figure 2.10. The calculated dose rate versus distance curves using the data from Figure 2.9.

the uncertainty in the epitaxial thickness.

To check the validity of this, ionisation current was measured as a function of distance from a Co^{60} source for both the CCD and a Hamamatsu S1723-03 PIN diode. This diode has an active area of 1 cm^2 and is fully depleted with a reverse bias of 25 Volts. The device capacitance when fully depleted is 70 pF implying a depletion depth of 150 μm which is comparable with the device's effective thickness [7]. When measuring the current from the photodiode the reverse bias was set at 40 Volts. A plot of the reciprocal of the square root of the induced current versus distance is shown in Figure 2.9. The distance was measured from the mylar window of the sample housing to the source's outer casing. The value that must be added to the measured distance to get the true source/sample separation is simply given by the offset on the distance axis.

The result of the calculated dose versus source/sample separation is given in Figure 2.10. The error bars on the CCD results are due to the uncertainty in the epitaxial thickness. The agreement between the results shows that the contribution due to the current from the substrate is insignificant.

A second possible problem arises as beta particles from the Sr^{90} source continuously lose energy as they pass through material. Therefore some of the low energy betas that originate from scattering by the collimator and source housing etc., will be stopped in the passivation, gate and insulator layers. These layers are approximately 2-3 μm thick in total. This implies that there will be more energy deposited in the insulator layer than that calculated by the energy deposited in the epitaxial layer. The range of a 10 keV beta particle is around 2 μm so any betas with an energy lower than this will not get to the gate insulator of interest which is less than 0.2 μm thick. The neglect of the surface layers will, to some extent, be cancelled out by neglecting the effect of the substrate when calculating the dose. However, it will be shown in Chapter 6 that the dose calculated using the Co^{60} source gives the same voltage shifts as a Sr^{90} irradiated sample. This implies that the surface layers have little effect on the dose calculations for the gate insulator.

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CHAPTER THREE

The Change in Operating Voltages and Dark Current Due to irradiation

3.1. Introduction

Tests on the effects of Sr^{90} irradiation on the voltage shifts and dark current of the UT101 CCD have been carried out by Roy *et al* [1]. These indicate that a voltage shift in the order of 0.7 Volt per 50 krad is expected if a device is unpowered during room temperature irradiation and an increase in dark current of 7 nA at 298K after 50 krad. The increase in dark current depends on the mode of operation of the device. In this present work, similar tests were carried out as part of the batch qualification for the SLD vertex detector. The measurements were also undertaken to establish the effect of irradiation whilst the device was running at low temperature. As part of a proposal for the European Teleman program, it was also necessary to investigate the radiation hardness of a UT102 device with a thinner than standard gate oxide as a precursor to further development of a radiation hard CCD.

3.2. The effect of trapped oxide charge on CCD operation

In section 1.4.2 it was shown how radiation induced charge can become trapped in insulator layers and the affect this has on the flat band voltage of MOS capacitors.

When charge becomes trapped in the gate insulator of CCDs the effect is to change the effective operating voltages. If this change is too great the CCD may cease to operate. Figure 1.7 showed the potential through a CCD with the approximate parameters of the UT101 device. It is clear that the channel potential will be approximately 10 volts above the potential applied to the gate assuming that the flat band voltage is zero. If holes are trapped in the oxide due to irradiation, and the gate voltage remains fixed, the channel potential will increase by an amount approximately equal to the magnitude of the flat band voltage shift. Assuming that the voltage shift is uniform across the device, charge will continue to be transferred without degradation. However, the potential applied to the various n^+ implants throughout the device will appear within the silicon. These potentials are not affected by radiation induced charge as no insulator layers are involved. This causes problems when regions of silicon controlled by a gate potential meet regions controlled by potentials applied directly via an implant.

As an illustration, the effect of trapped positive charge on the charge transfer to the output node of the CCD is shown in Figure 3.1. For charge to be efficiently transferred to the output node it is necessary that the channel potential under the output gate be less than the potential at the node, which is pinned at V_{rd}. Therefore the change in the channel potential under the output gate will eventually cause device failure due to the incomplete transfer of charge to the output if the applied biases are not modified. V_{rd} is usually set to 17 Volts whilst the potential on the output gate is 2 Volts, giving a channel potential of 12 Volts. Therefore a voltage shift of about 5 Volts is required before the biases need changing.

This gives a convenient method for monitoring the voltage shift. At room temperature there will be a background signal due to thermally generated charge. This charge is clocked onto the output node and then passed down the V_{rd} line when the output node is reset. This constitutes a current, I_{rd}, which was monitored by measuring the voltage drop across a 10 MΩ resistor using a Thurlby 1503-HA high input impedance multimeter. This was found to be preferable to using an electrometer as it was less susceptible to fluctuations caused by external signals. If the voltage applied to V_{rd} was reduced then a point would be reached when charge could no longer be transferred to the output node and so the measured current drops. As a device is irradiated the point at which the charge can no longer be transferred occurs for a higher V_{rd}. This is shown in Figure 3.2.

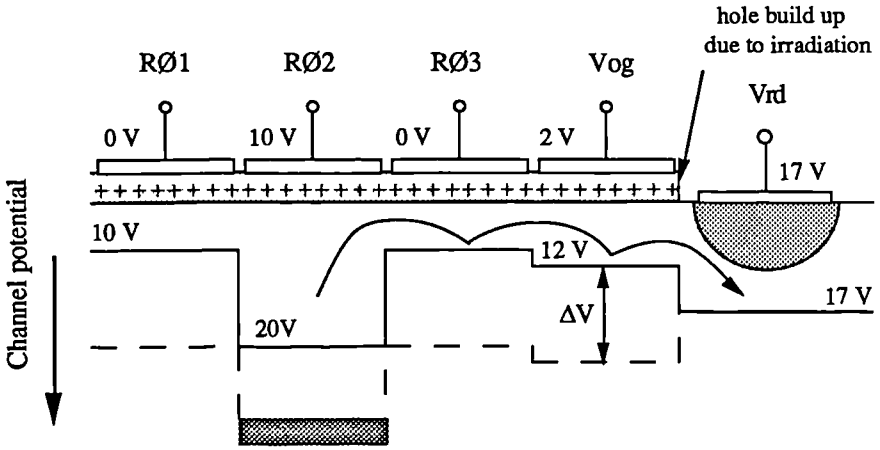

Figure 3.1. The effect of trapped positive charge on the transfer of charge to the output node. The dashed line indicates the channel potential after irradiation.

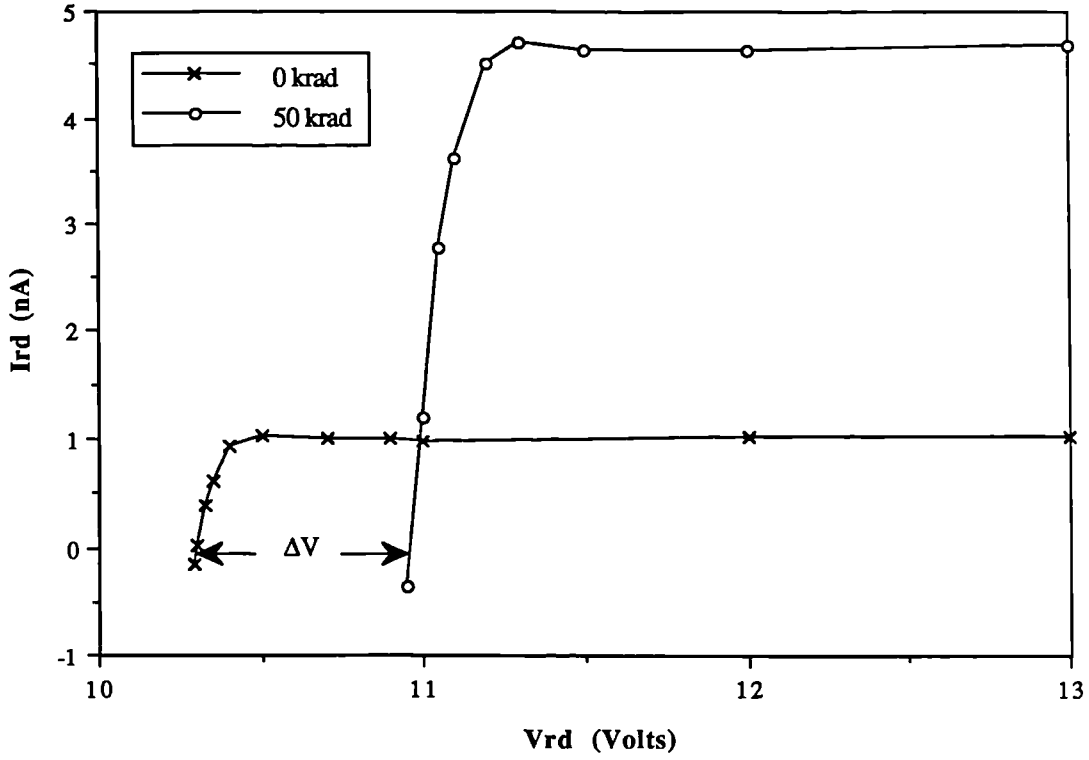

Figure 3.2. A typical result of a I_{rd} vs V_{rd} measurement for a device before and after irradiation at room temperature, with all connections grounded

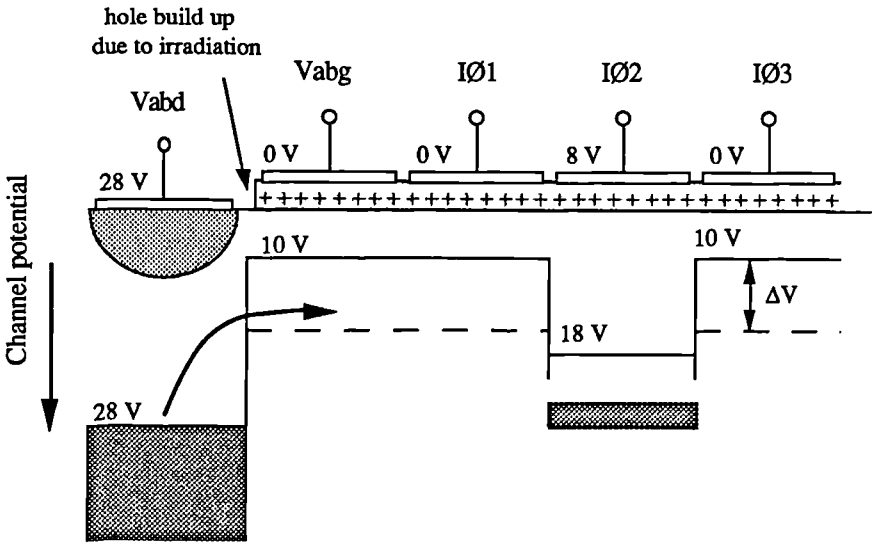

Figure 3.3. The effect of trapped positive charge on the injection of charge from the antiblooming drain structure. The dashed line indicates the channel potential after irradiation.

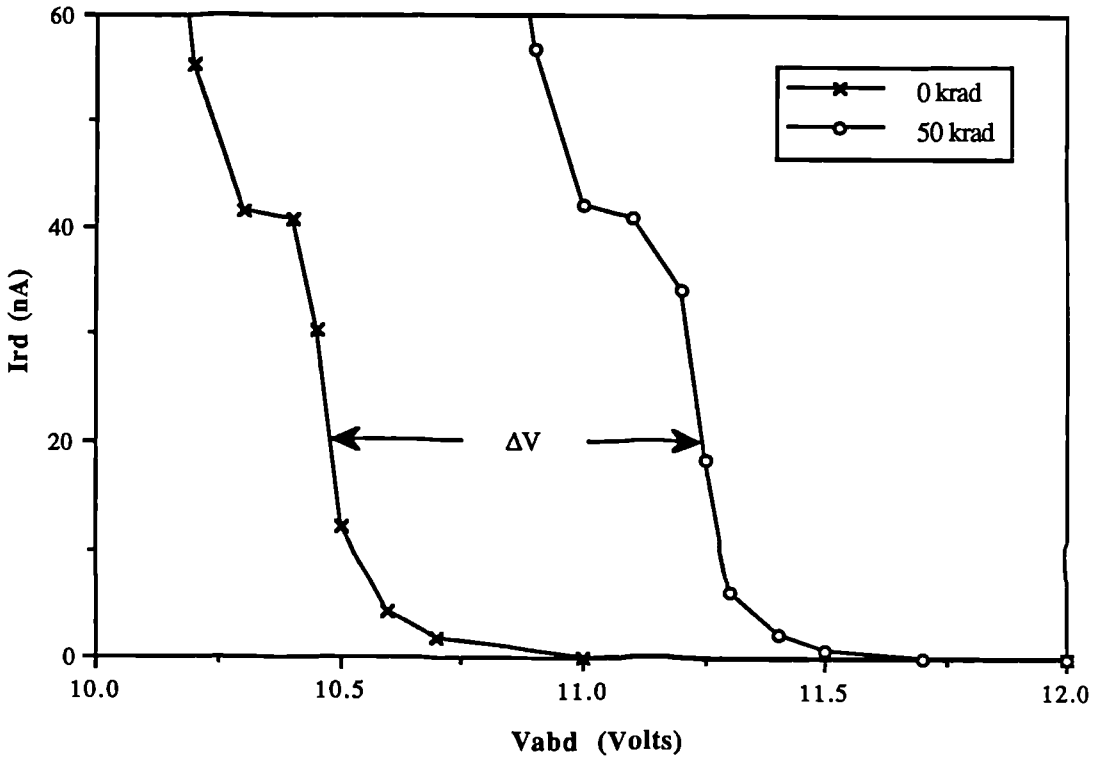

Figure 3.4. A typical result for an I_{rd} vs V_{abd} measurement for a device before and after irradiation. The measurement was performed at 180K.

The radiation induced voltage shift can also be measured by monitoring the current that is injected into the device via the n^+ implants. If the potential applied to the antiblooming drain structure, V_{abd}, is reduced there will come a point when charge will start to be injected into the image section of the CCD. As this charge is clocked out of the device there will be an increased I_{rd}. The value of V_{abd} at which injection starts is approximately equal to the channel potential under the antiblooming gate.

As the device is irradiated, the channel potential increases. The value of V_{abd} at which injection commences also increases. This is illustrated in Figure 3.3. The voltage shift can be monitored by measuring the current as a function of V_{abd}. A typical result is given in Figure 3.4. Charge injection from the drain structure is potentially catastrophic for device operation. The maximum voltage that can be applied to the drain structures is around 30 Volts. Therefore a voltage shift of about 19 Volts is required before the device fails through this mechanism.

Trapped oxide charge also affects the on-chip output circuit. The voltage shift causes a reduction in the threshold voltage required to turn the reset FET "on". Therefore there will come a point when the reset FET will be unable to be turned "off" without a change in the operating voltages. This change in threshold voltage could be monitored by injecting a small signal (10 mV square wave) down the V_{rd}

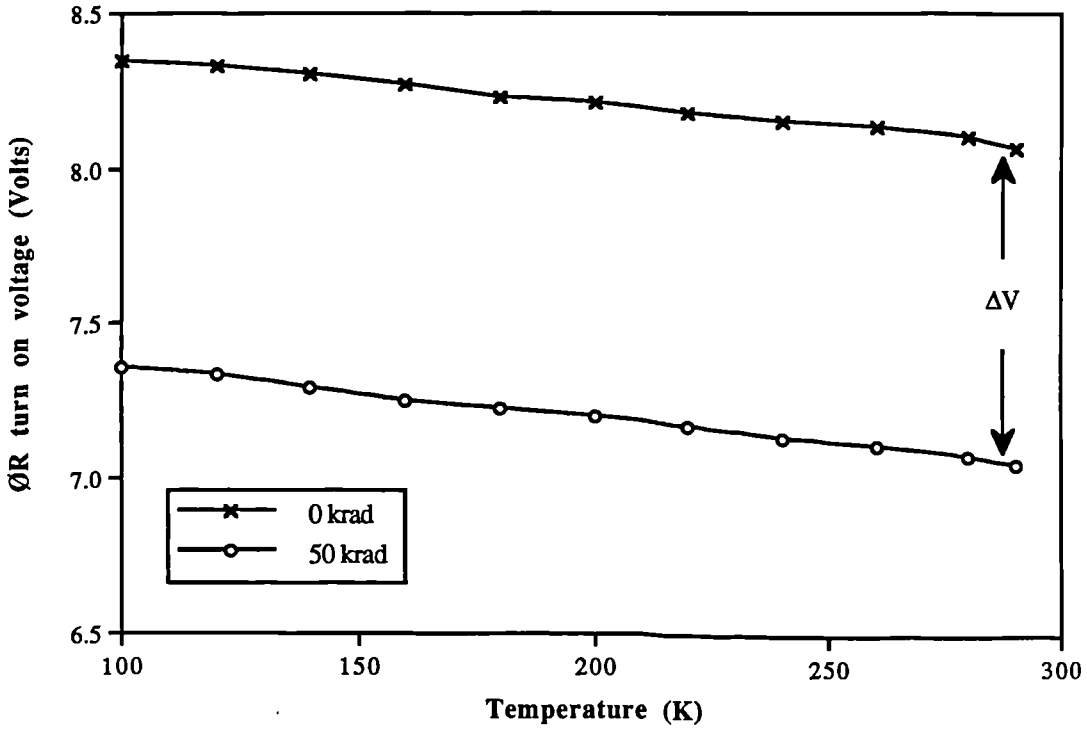

Figure 3.5. A typical result for the reset FET "turn on voltage" measured before and after irradiation.

line with the device biased but static. The output of the device was taken to a preamplifier and then to an oscilloscope. The voltage applied to the gate of the reset FET was reduced until a signal could no longer be observed. At this point the reset FET can be regarded as being "off". The effect of irradiation on this "off" voltage is shown in Figure 3.5. In order to reset the output node, a 0 to 10 Volt pulse is usually applied to gate of the reset FET. Therefore, if the reset FET turns "off" at 8 Volts then an 8 Volt shift can be tolerated before adjustment is necessary. However, it must be noted that the value of this "off" voltage varied from batch to batch and was as low as 0.5 Volts for one device tested.

The output circuit is generally set up as a source follower. Therefore, if the gate voltage remains fixed (ie. keeping V_{rd} fixed) then hole build up in the gate oxide of the output FET causes the source voltage to increase. By monitoring the source voltage, an indication of the flat band voltage shift can be obtained. This is discussed in more detail in Chapter 5 where the affect of the output FET's operating point on it's noise performance is investigated. A typical measurement of the source voltage before and after irradiation is given in Figure 3.6. In fact it was more convenient to measure the source voltage of the dummy output FET which

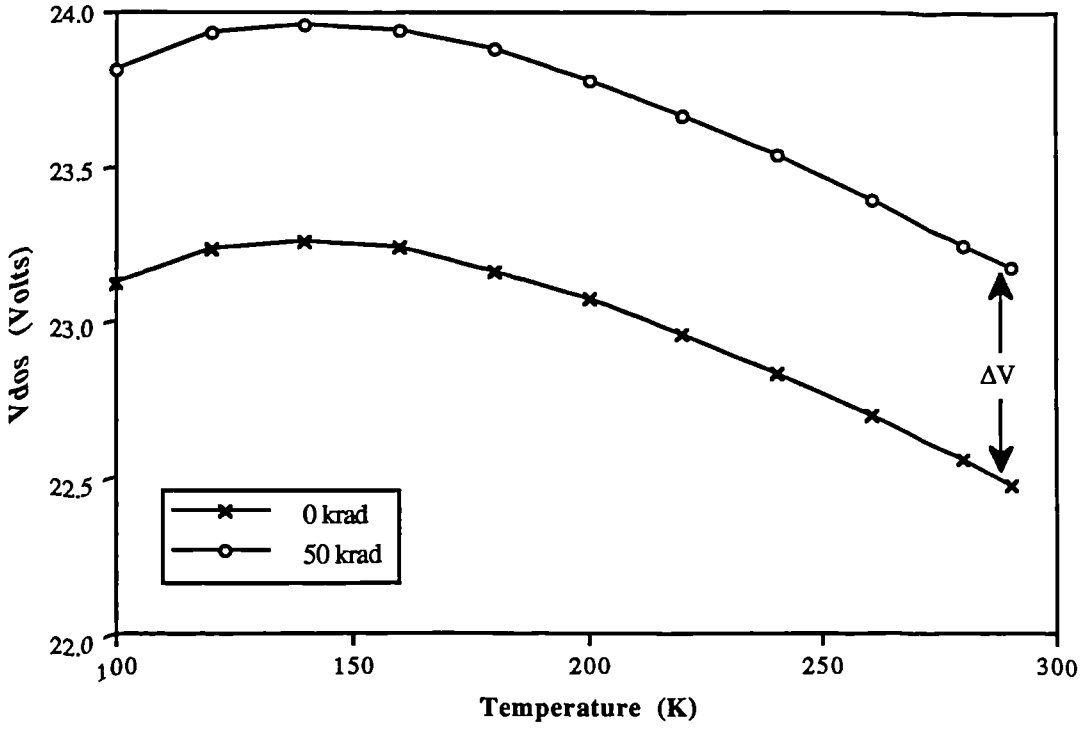

Figure 3.6. The effect of irradiation on the source voltage of the dummy output FET. The drain voltage = 28 V and V_{rd} = 17V. The load was 22 kΩ.

was identical to the real output FET.

3.3. The increase in dark current due to irradiation

In sections 1.3.1 it was shown that defects within the depletion region of a semiconductor device can act as generation centres for electron hole pairs. If the cross section for the capture of an electron is the same as that for a hole then the generation rate is given by

$$G_B = \frac{\sigma v_{th} N_t n_i}{2\cosh((E_t-E_i)/kT)} = \frac{n_i}{2\tau_o}$$

where σ is the capture cross section, v_{th} is the thermal velocity, N_t and E_t are the density and energy level of the generation centre and n_i and E_i are the intrinsic carrier concentration and Fermi level. τ_o is known as the effective lifetime within the depletion region. If the generation centres are distributed in energy throughout the band gap then the total generation rate per unit volume is given by

$$G_B = \int_{E_v}^{E_c} \frac{\sigma v_{th} n_i D_t(E_t)}{2\cosh((E_t-E_i)/kT)}\, dE_t$$

where $D_t(E_t)$ is the density of centres per unit energy. If the traps are uniformly distributed then this simplifies to

$$G_B \approx \frac{\pi \sigma v_{th} n_i D_t kT}{2}.$$

In this case τ_o can be written as

$$\tau_o = \frac{1}{\pi \sigma v_{th} D_t kT}.$$

This is equal to the case where $\pi D_t kT$ states are situated at E_i. Therefore it can be concluded that, for the case of defects that are distributed within the band gap, it is only those traps located within a few kT from mid gap which are effective generation centres.

Similarly, as the surface of the CCD is depleted, the surface states also act as generation centres with a generation rate per unit surface area given by

$$G_S \approx \frac{\pi\sigma v_{th} n_i D_s kT}{2} = \frac{s_o n_i}{2}$$

where D_s is the surface state density per unit area per eV near mid gap. s_o is the surface recombination velocity.

The generated charge collects in the buried channel and provides an unwanted background to the signal. This background is known as dark current. The dark current per unit area from the bulk silicon is

$$J_B = qG_B x_d = \frac{q x_d n_i}{2\tau_o}$$

where q is the electronic charge and x_d is the depletion width (~7 μm for the EEV UT101 CCD). For the surface contribution we have

$$J_S = qG_S = \frac{q s_o n_i}{2}.$$

τ_o and s_o are both temperature dependent. However, the main temperature dependence of these currents comes from the dependence of the intrinsic carrier concentration which is given by

$$n_i = (N_c N_v)^{1/2} \exp(-E_g/2kT).$$

There will also be a contribution to the dark current from charge diffusing to the depletion region from the undepleted silicon. The depletion region, under the gates of the CCD, extends into the p-type layer. At the edge of the depletion region, the minority concentration is zero and increases exponentially to the thermal equilibrium value towards the substrate. The profile of the minority carriers can be written as

$$n = \frac{n_i^2}{N_A}(1-\exp(-x/L_n))$$

where L_n is the minority carrier diffusion length and is equal to $(D_n\tau_n)^{1/2}$, D_n is the diffusion constant and τ_n is the minority carrier lifetime. This constitutes a concentration gradient for minority carriers. Therefore minority carriers flow down this concentration gradient into the buried channel. This diffusion current is given by

$$J_{dif} = qD_n \left.\frac{dn}{dx}\right|_{x=0} = \frac{qD_n n_i^2}{L_n N_A}.$$

Therefore the diffusion current will show an approximate $\exp(-E_g/kT)$ dependence. The total current density, J, is simply the sum of the above contributions, ie.

$$J = J_B + J_S + J_{dif}$$

$$= \frac{qx_d n_i}{2\tau_o} + \frac{qs_o n_i}{2} + \frac{qD_n n_i^2}{L_n N_A}.$$

All these terms show an increase as the device is irradiated. s_o increases due to the increase in surface state density, τ_o and L_n both decrease due to the increased density of defects within the bulk silicon.

The increase in the dark current due to ionising radiation is dominated by the increase in surface state density. Therefore any method that reduces the contribution from the surface states will dramatically improve the radiation hardness. Saks has shown [2] that the generation of charge from interface states can be significantly reduced by partially inverting the Si/SiO_2 interface. In the normal mode of operation, the substrate is held at 0 Volts and the gates are biased positively. Consequently the interface is depleted of both electrons and holes and generation from the surface states can occur. If the substrate voltage is increased (or equivalently the gate voltage decreased) there comes a point when the surface is attractive to holes. This occurs when the surface potential becomes equal to the substrate potential. Holes can be supplied by the channel stops and so the surface

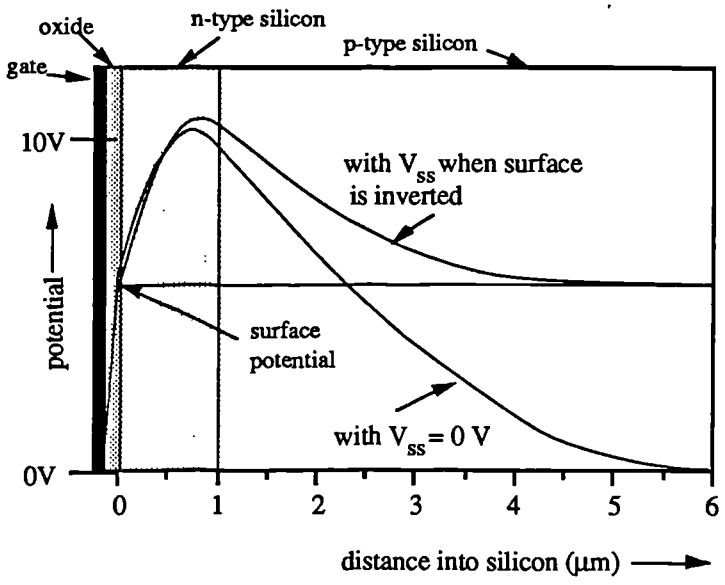

Figure 3.7. The potential through the CCD showing the onset of inversion under the electrode when the substrate potential is increased to the surface potential. V_{ss} = substrate voltage.

will invert and becomes fixed at the substrate potential. This is the situation illustrated in Figure 3.7. Any subsequent increase in the substrate potential causes the density of holes at the interface to increase. Due to the high density of holes, the dark current generation from this region is suppressed. This suppression can be seen in the measurement of the dark current versus substrate potential shown in Figure 3.8. This measurement was made with the device static, with all the gates connected together to form a large depletion mode MOSFET and the reset FET was biased "on". All the drains were joined and connected to the V_{rd} line, down which the current was measured. At low substrate voltages the surface of the device is depleted and dark current is freely generated from this region. As the substrate potential is increased the dark current is reduced at the point when the surface potential equals the substrate potential (at $V_{ss} \approx 3$ Volts for an unirradiated device). The dark current remains constant until the substrate potential becomes greater than the channel potential. At this point the measured dark current drops to a very small value but no imaging would be possible due to the collapse of the potential well structure.

A standard device, such as the UT101, cannot be clocked with the whole device

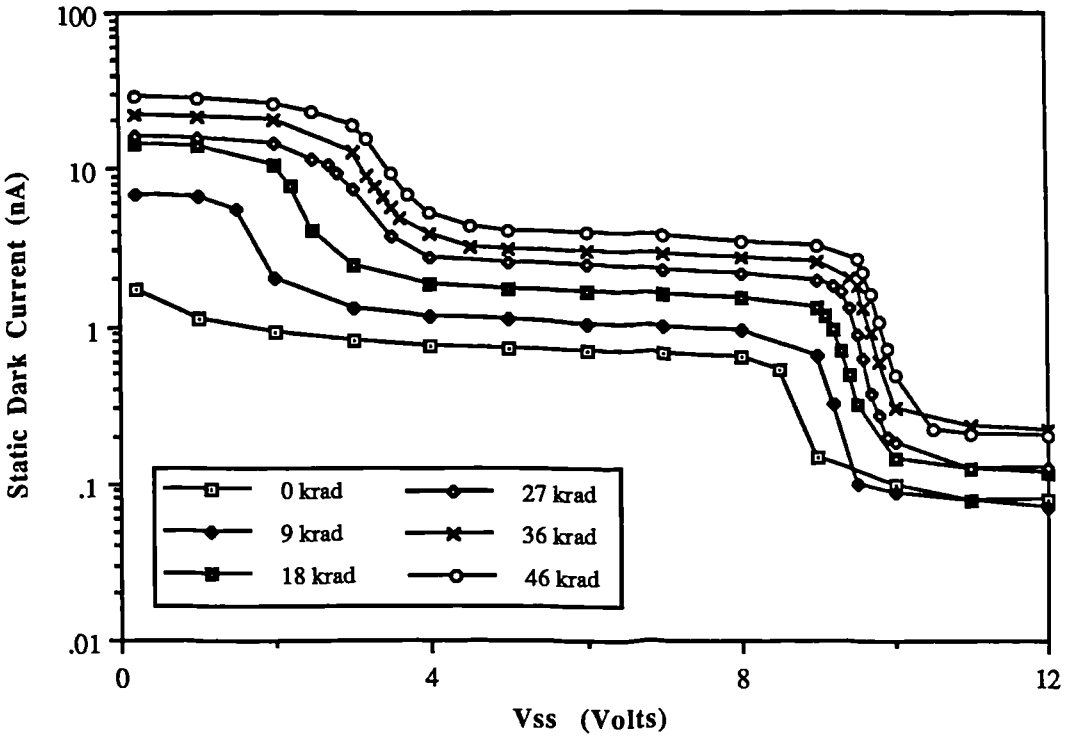

Figure 3.8. The dark current measured at 290K in a static device as a function of substrate voltage. The gate potential is set at 0 Volts. A similar result is obtained with the device clocking.

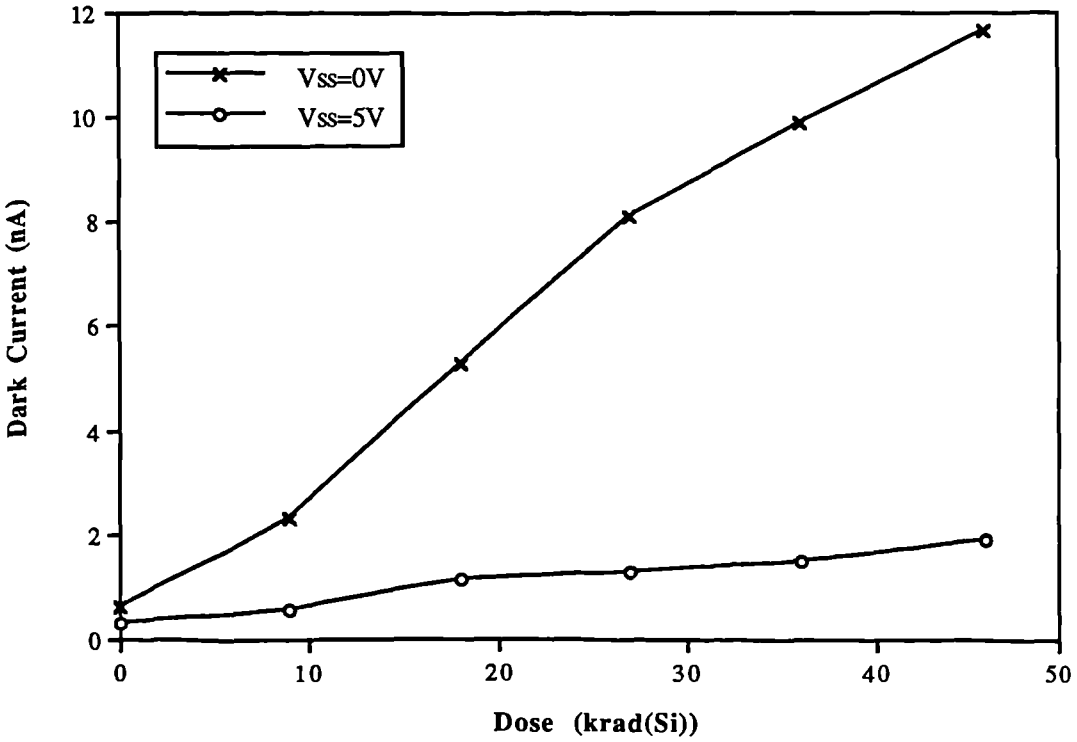

Figure 3.9. The dark current measured at 280K.

area inverted as the gate potentials will be unable to control the channel potential. In this case no potential wells are formed and signal charge will not be able to be confined. However, operation is possible by ensuring that the surface under one phase remains depleted. Figures 3.9 shows the effect of irradiation on the dark current measured at 280K. These results were taken with the device clocking continuously and shows the improvement that can be achieved by applying 5 Volts to the substrate thus inverting the surface under two of the phases. The improvement is significantly greater than expected by assuming that the surface under two of the phases is inverted. Burke *et al* [3] have shown that when the surface of a CCD is switched from inversion to depletion, the surface generation rate remains low for a characteristic time period before recovering to its steady state value. If this time period is greater than the period of the clocks then a large fraction of the total surface dark current will be suppressed. Therefore, the improvement that can be achieved is dependent on the clocking frequency and the integration time.

Devices that include an additional implant, such as virtual phase devices, can operate in full inversion. These devices, however, show a tendency for the generation of radiation induced, dark current spikes due to the high electric fields present [4]. CCDs have also been fabricated to allow full inversion during signal integration only. These devices, known as multipin phase (MPP) CCDs, also

include an additional implant but are not subject to the high fields of the virtual phase devices.

3.4. The effect of irradiation whilst running at low temperature

From sections 1.3.2 it was shown that the flat band voltage shift is a strong function of field within the oxide. If the device is clocking during irradiation, the electric field in the insulator will be in the order of 3 10^5 Vcm^{-1}. Therefore the electron hole pairs produced by the radiation will be swept apart rapidly. However, if the device is unbiased during irradiation, the fields within the gate insulator are only due to the charge within the oxide and so are very much lower. This implies that a greater fraction of radiation induced holes will initially recombine when the device is unbiased and so it is expected that the voltage shifts should be higher when the device is irradiated whilst running.

The CCD is often operated at low temperatures. For example, the CCDs used in the SLD vertex detector are operated at 180K. If a device is irradiated with a short burst of ionising radiation the voltage shifts evolve with time with a time constant that increases with decreasing temperature. However, if the device is irradiated at 180K almost all of the holes would have been transported to the Si_3N_4 interface within a few minutes. As irradiations are performed over a period of a few hours little effect of the low temperature was expected to be seen.

A device was irradiated at room temperature with all connections grounded at a rate of 1 krad/hour. Approximately every ten hours the CCD was transferred to the vacuum rig and the voltage shift was measured at 180K by monitoring I_{rd} and varying V_{abd}. A device from the same wafer was cooled to 180K and set up to run in full frame mode with the readout register clocking at 83 kHz with the substrate potential fixed at 5 Volts. Whilst the device was clocking, the source was placed over the CCD and the current monitored to obtain the dose rate. The source could not be placed as close to the CCD as in the irradiation rig and the maximum dose rate that could be achieved was around 250 rad/hour. Every two hours the I_{rd} versus V_{abd} measurement was performed without removing the source and without warming the device. The result of the comparison is given in Figure 3.10. The unbiased data indicates an initial sharp rise in the voltage shift. However the shift then appears to increase linearly with dose at a lower rate. This is possibly due to two sources of hole traps with one being rapidly filled. These results are consistent with those reported by Roy *et al* and show a shift of 0.014 Volts per krad(Si) after

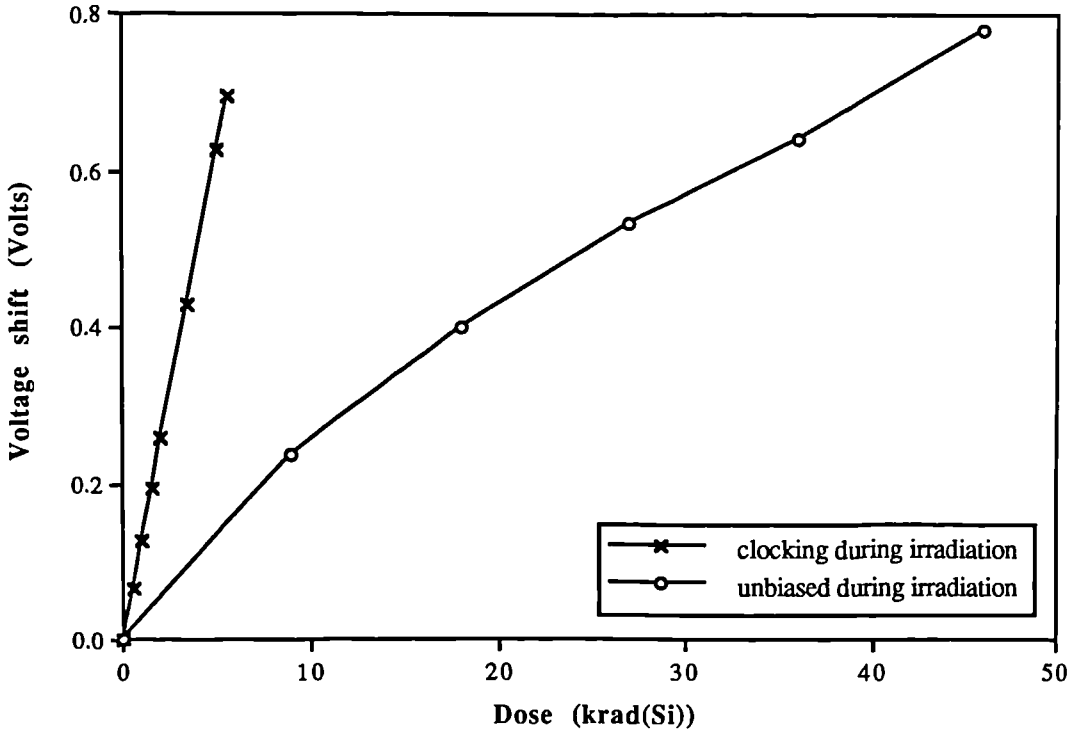

Figure 3.10. A comparison between irradiation carried out with a device running at 180K and a device unbiased at room temperature.

the initial rise. The results with the device clocking show a linear dependence of the voltage shift with dose and increases by 0.12 Volts per krad(Si). Therefore the voltage shift with the device clocking is approximately nine times worse than when all connections are grounded during irradiation.

The voltage shift measured depends on the trapped oxide charge under the antiblooming gate. The potential applied to this gate remained fixed at 0 Volts during irradiation and so does not give a measure of the voltage shifts experienced by parts of the device where the fields are fluctuating. However the Si/SiO_2 interface under the gates with zero applied bias is pinned at the substrate voltage giving a field of 3.9 10^5 Vcm^{-1}. If 7 Volts is applied to the gates then the field decreases to 3.4 10^5 Vcm^{-1}. There is only a small difference so there should be little effect.

To check the effect of low temperature irradiation the CCD was left clocking after the irradiation had ceased, without warming the device. After two hours the voltage shift was measured again and no short term annealing was observed. The source voltage of the dummy output FET was monitored as the device was warmed up to room temperature at a rate of 10°C/min. The device remained clocking at room

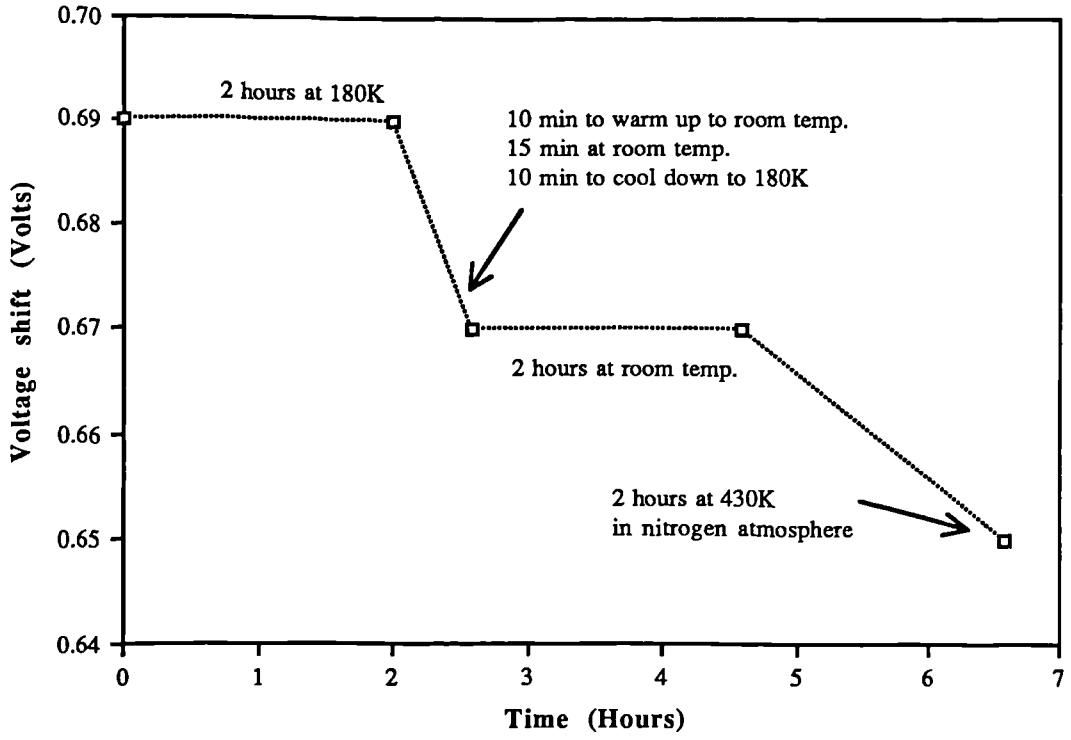

Figure 3.11. The annealing of the voltage shift

temperature for 15 minutes and then cooled back down to 180K. The source voltage versus temperature curve measured whilst cooling was almost identical indicating that very little annealing had taken place. When the voltage shift was measured, by performing an I_{rd} versus V_{abd} measurement, it showed an improvement of 20 mV. The voltage shift was measured again at 180K after 2 hours at room temperature. No further improvement was observed. An improvement of a further 20 mV was seen after the device was heated in a nitrogen atmosphere for two hours at a temperature of 430K. The history of the voltage shift is shown in Figure 3.11. This overall reduction of the voltage shift is negligible showing that hole transport within the oxide was almost complete by the time the device was initially tested.

The dark current, measured after the device had warmed up the first time, was consistent with the dark current of the device irradiated unbiased, at room temperature.

When comparing these results with other workers, it must be remembered that voltage shifts are a function of the density of hole traps within the oxide, the oxide thickness and the field within the oxide. The presence of a nitride layer also has a significant effect. Therefore the voltage shifts are a strong function of the processing technology employed. This will vary from one manufacturer to another.

However, a comparison is useful when considering which CCDs to employ for an application and the results here are compared with those obtained for devices manufactured by Thompson-CSF. Like the EEV CCDs, the Thompson devices tested by Hopkinson [5,6] were manufactured without special regard for radiation hardness. These devices were intended for scientific application and were tested for ESA's Semiconductor Intersatellite Laser Experiment (SILEX) program. After Co^{60} irradiation they showed a voltage shift of 0.09 Volts per krad(Si) for devices running during irradiation and 0.024 Volts per krad(Si) with all connections grounded. These voltage shifts are of the same order as those found in this work.

3.5. Batch qualification for the SLD Vertex detector.

The SLD Vertex detector consists of 480 UT101 CCDs. The suitability of the devices to run in the radiation environment of SLD has been established by Roy *et al.* However, only a limited number of devices were tested. Therefore, as so many devices were being employed, it was necessary to check the radiation hardness of each batch. It was conceivable that the quality of the gate insulator could change from batch to batch. This would imply that the magnitude of the voltage shifts would vary. It was also possible that the threshold voltages could vary if the implantation of the n-layer was not repeatable. A lower threshold voltage would give a lower headroom for acceptable flat band voltage shifts. Any variation in the dark current generation was not of great concern as the vertex detector was to be cooled to 180K. However, a measure of the dark current gave an indication of the quality of the device. It was also important that there should be no local areas of high dark current (dark current spikes or white spots) either before or after irradiation. These spikes can originate from localised clusters of bulk damage or breakdown of the gate insulator causing local thermal spikes or photon generation. The amount of charge a dark current spike can generate is dependent on the integration time but can easily fill a potential well. The full well capacity for the UT101 CCD is around 10^5 electrons whereas the signal generated by a minimum ionising particle is around 1620 electrons. The electronics for the vertex detector was designed to handle the signal from such particles but would be saturated by the dark current spikes.

The actual specification for the batch qualification is laid out in Brunel University contract number BRU/PHY/89/2. In addition to the radiation hardness, the batch qualification was to check for the quality of the devices, reliability (using burn in tests) and reliable wire bonding. These checks were carried out at EEV and the

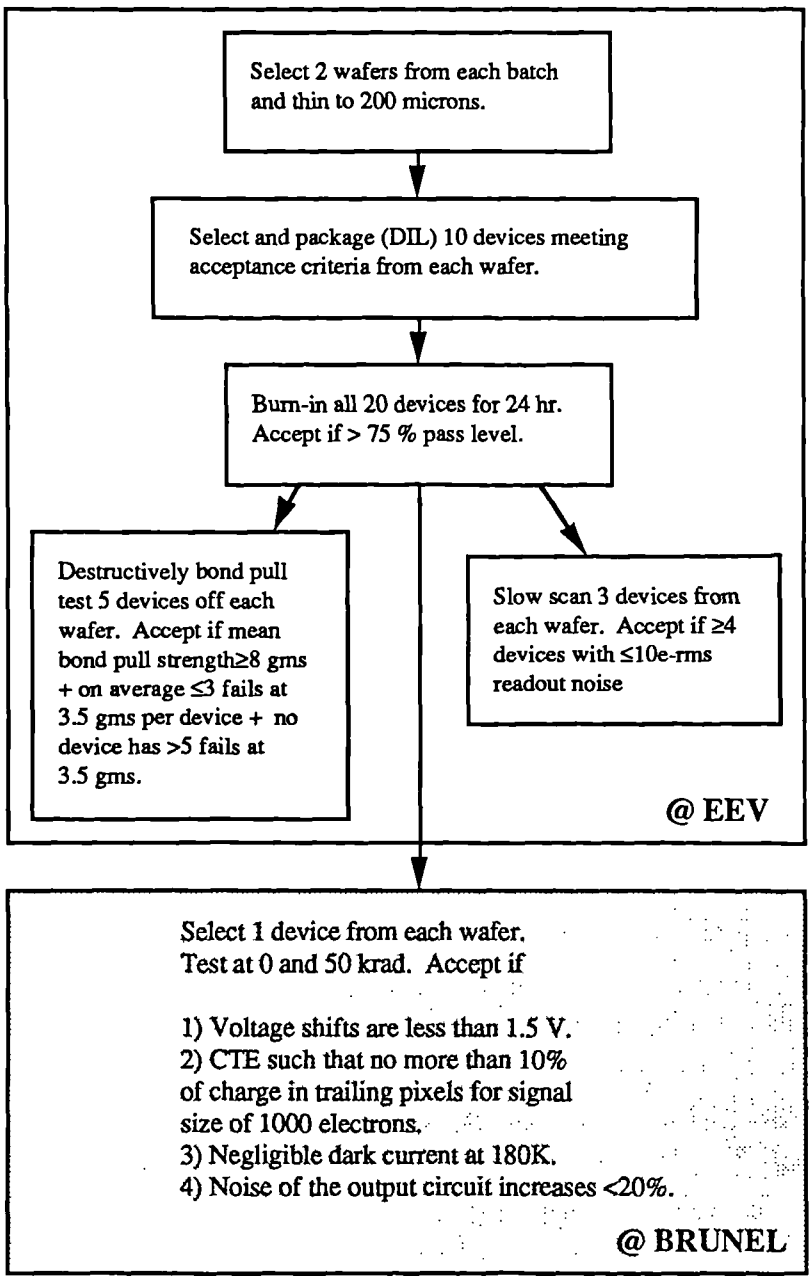

Figure 3.12. The batch qualification procedure.

results can be found in reference [7]. If sample CCDs from a batch passed these preirradiation tests, further devices were passed to Brunel for radiation testing. The flow diagram for the batch qualification agreed between Brunel and EEV is given in Figure 3.12. The radiation qualification involved the testing of two packaged devices from each batch, each device from a different wafer.

Measurements were made before irradiation and after 50 krad(Si) from the Sr^{90} source. The irradiations were carried out at room temperature, with all connections grounded, at a rate of 1 krad(Si) per hour. The radiation qualification of the devices

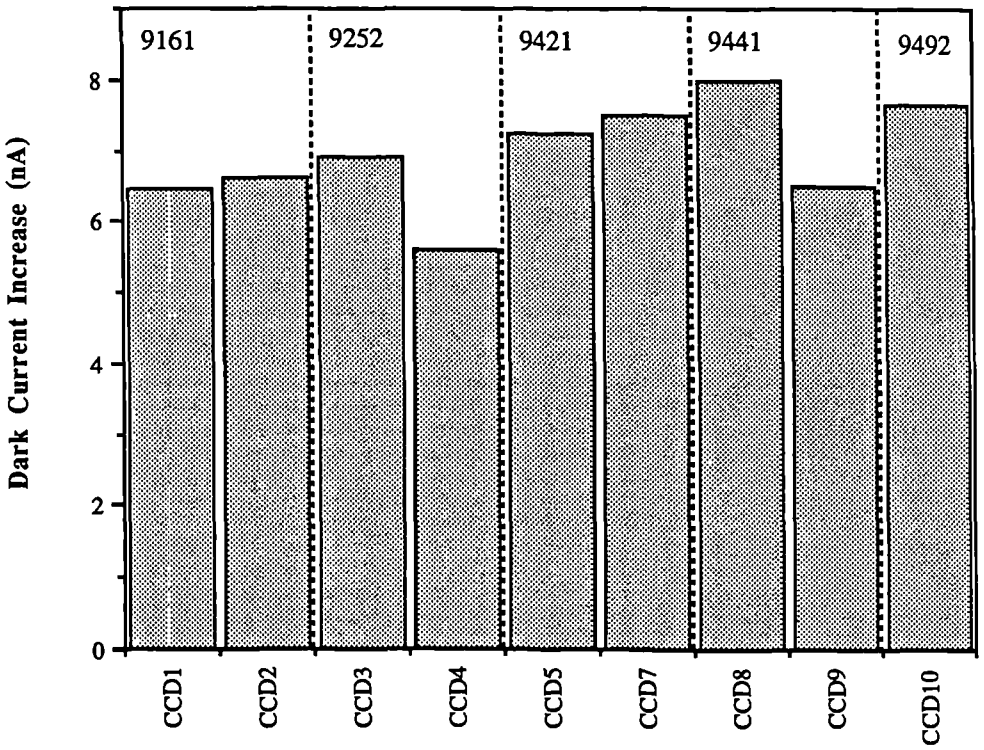

Figure 3.13. The dark current increase measured at 295K after 50 krad(Si). The batch identification numbers are shown.

included the measurement of the voltage shifts and dark current. The procedure for measuring the voltage shifts has been previously described in this chapter. The dark current was measured with the device continuously clocking and the substrate voltage set so that the Si/SiO_2 interface was inverted under two of the phases. A dark image from the device under test was obtained at 180K to ensure that no dark current spikes were present. Charge transfer measurements were not undertaken as part of the qualification as the experimental methods had not been fully developed at the time. A rough check was made on the noise performance of the output circuit and no problems were highlighted.

All the devices tested showed a consistent increase in the dark current, illustrated in Figure 3.13. This implies that the processing conditions remained very constant from one wafer to another and between batches. This consistency is also apparent when the voltage shift measurements are compared (Figure 3.14). However, the measurements did highlight a deficiency in the specification of the acceptance criteria. The voltage shifts measured on the devices from batch 9252 were well within the 1.5 volt acceptance limit and consistent with other batches. However, the threshold voltages were much lower than standard devices. This meant that the

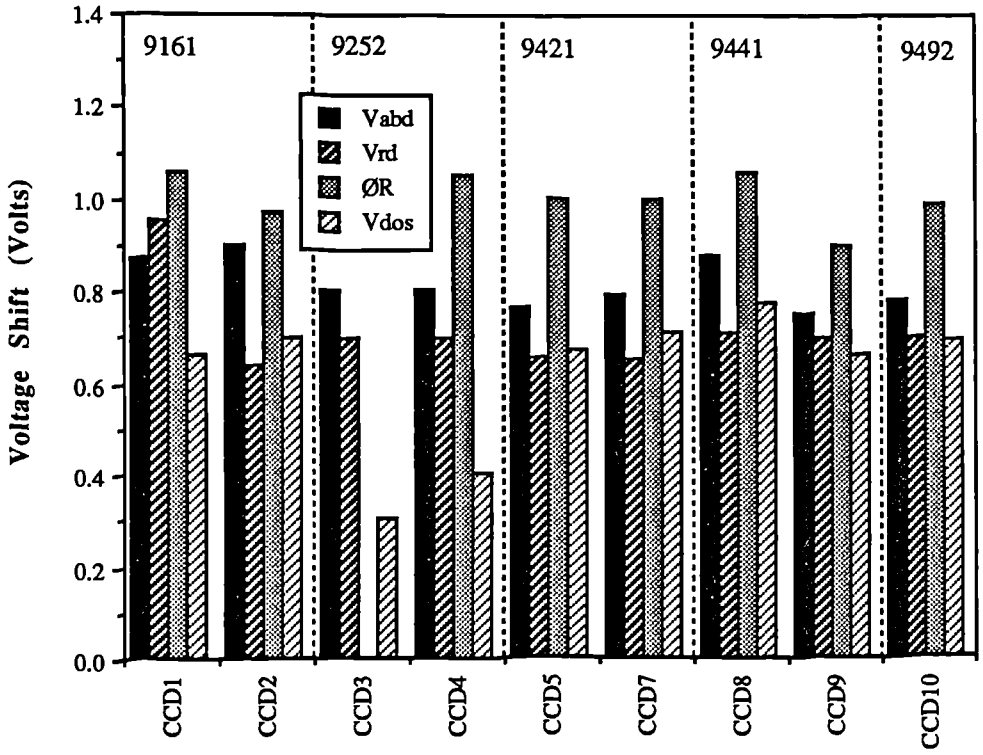

Figure 3.14. The batch to batch variation in the voltage shifts after 50 krad(Si).

output FET was not biased in saturation with the usual voltage levels. In addition, the output node of CCD3 could not be reset after a voltage shift of 0.5 Volts. This was clearly unacceptable. It later transpired that this batch had received a final passivation that was not well controlled. It seems likely that the high temperature of this passivation drove the dopant atoms of the n-layer further into the device than expected. This batch was eventually rejected.

3.5. The TELEMAN program

The commission of the European Communities runs a program called TELEMAN with the object to develop advanced robots that can operate in hazardous or disordered nuclear environments. The program consists of several projects, one of which involves the development of a radiation hard CCD camera for the vision system of such robots. It is intended that this camera should survive an accumulated dose of more than 100 Mrad. BNF-Fulmer has co-ordinated a bid to develop such a CCD camera [8]. The team consists of BNF-Fulmer, a research establishment in Wantage; EEV, the CCD manufacturer and Exavision, a French camera manufacturer. Brunel and Leicester Universities are acting as consultants to

BNF-Fulmer. If successful in the bid it will be Brunel's role to monitor new radiation hard technology developed by EEV and to make suggestions for further improvement.

The CCD will be shielded, to some extent, from the full dose of 100 Mrad. However a device must be able to survive doses of a few tens of Mrad. The EEV devices at present can continue operating with doses up to 200 krad(Si) for optical imaging applications. One possible approach to providing a more radiation hard CCD is to reduce the oxide thickness so as to reduce the amount of radiation generated holes that are available to be trapped at the Si_3N_4/Si interface This has been done by EEV and the preliminary tests on a UT102 CCD were carried out at Brunel as part of the Teleman proposal.

It was shown in section 1.3.2 that the voltage shift due to trapped oxide charge in the sandwich insulator of the CCD is given by

$$\Delta V_{ot} = -1.9\ 10^{-8}\ d\ d_n D\ F_t F_e$$

where D is the dose in rad(Si), F_t is the fraction of trapped holes, F_e is the fraction that escape initial recombination, d_n and d are the nitride and oxide thickness respectively, measured in nanometres. The UT102 CCD supplied by EEV had a 40 nm oxide compared with the standard oxide thickness of 80 nm. Therefore, assuming negligible contribution to the voltage shifts by interface states, the voltage shift is expected to be halved. This new device was irradiated to 30 krad with all connections grounded. It showed a voltage shift of 0.3 Volts. A standard device shows a voltage shift of about 0.6 Volts after 30 krad. These results are fully consistent with the above model and show promise that a reduction to an oxide thickness of 10 nm should give a least an 8 fold improvement in the voltage shifts. The oxide cannot be reduced to below 10 nm as direct tunnelling of electrons from the silicon to the nitride layer becomes possible. This then leads to unstable behaviour which is undesirable for CCD operation. Improvements will also be achieved by reducing the nitride thickness. It is not known how thin the nitride layer can become before unreliability and low device yield becomes a problem. Care must also be taken not to increase the gate capacitance significantly otherwise driving the CCD will become difficult.

The voltage shifts can also be reduced by providing a gate oxide with fewer hole traps. EEV have attempted this by stripping off the gate oxide, through which the n-layer had been implanted, and growing a new, low temperature oxide. This new layer should have fewer hole traps. However measurements are not yet available.

Even with these improvements, the voltage shifts will have to be monitored and applied voltages altered to allow operation into the proposed Megarad range.

3.6. Summary

This chapter has extended the information on the radiation hardness of the EEV CCDs to include the voltage shift and dark current measurements made for a device that had been irradiated whilst clocking at 180K. The voltage shift increases from 0.014 Volts per krad(Si) for a device unbiased during irradiation to 0.12 Volts per krad(Si) for a device running continuously. The voltage shifts showed little short term annealing and a high temperature anneal in nitrogen did not accelerate recovery significantly. The dark current was not found to be dependent on the state of the CCD during irradiation.

The batch qualification of the CCDs for the SLD vertex detector showed a consistent dark current increase and voltage shift from wafer to wafer and from batch to batch. However, measurements indicated that care must be taken when defining the acceptance criteria. It was found that the voltage shift that could be tolerated varied from batch to batch.

Initial studies for the TELEMAN program showed that a significant reduction of the voltage shifts can be obtained by thinning the oxide layer of the gate insulator. This looks promising for the development of an ultra-radiation hard CCD for imaging applications.

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CHAPTER FOUR

Charge Transfer Degradation

4.1. Introduction

Many scientific users of CCDs are interested in signal sizes in the order of a thousand electrons. This signal packet has to be transported, with minimal loss, through the bulk silicon. This has presented many processing challenges and now charge transfer efficiencies (CTEs) of better than 0.99999 per transfer are readily available in commercial devices. It is ultimately limited by the presence of bulk traps due to impurity centres or defect complexes. The degradation of the CTE due to the presence of bulk traps has been studied extensively in the past. The main concern has been with process induced effects such as the presence of impurity centres from gold, sulphur [1] or iron atoms [2].

The effect on the CTE of fast neutron irradiation has been presented by Saks [3] and Srour *et al.* [4]. There have been various studies on the effect of protons and gammas, for example [5,6]. In this chapter the change in the CTE, or equivalently the charge transfer inefficiency (CTI=1-CTE), of the EEV UT101 CCD due to the increase in a bulk trapping level by the beta radiation from a Sr^{90} source is described. It was the goal of this work to develop an understanding of the CTE reduction and find ways to reduce the degradation.

In order to predict the effects of a radiation environment on CCD operation the provision of a model for the degradation is essential. This model should take into account the CCD configuration, mode of operation and radiation type. Such

models have been attempted in the past using data from proton damage [7,8] but with some omissions and shortcomings.

4.2. The theory of CTE degradation

A model for the effect of bulk traps on the reduction of CTE has been given by Mohsen and Tompsett [9]. However, this model assumes that the CCD runs with equal phases and that the emission time constant for electrons is very much greater than the capture time constant. In this present work, it was found necessary to expand this model to include the effects of clock timing on incomplete charge trapping.

When a charge packet moves through otherwise depleted silicon, electrons from the signal will be trapped by impurity centres and damage complexes that form discrete energy levels within the forbidden band gap. The processes that can lead to a change in trap occupancy are shown in Figure 4.1. These processes are (a) capture of electrons from the conduction band, (b) the emission of electrons from the trap to the conduction band, (c) the capture of electrons from the trap to the valence band (equivalent to the capture of holes from the valence band) and (d), the emission of electrons from the valence band to the trap (equivalent to the emission of holes from the trap to the valence band). The rate of change of trap occupancy is given by the sum of the rates for these four processes, i.e.

$$\frac{dn_t}{dt} = \frac{N_t - n_t}{\tau_{nc}} - \frac{n_t}{\tau_{ne}} - \frac{n_t}{\tau_{pc}} + \frac{N_t - n_t}{\tau_{pe}}$$

where n_t is the density of captured electrons, N_t is the trap density, τ_{ne} and τ_{pe} are

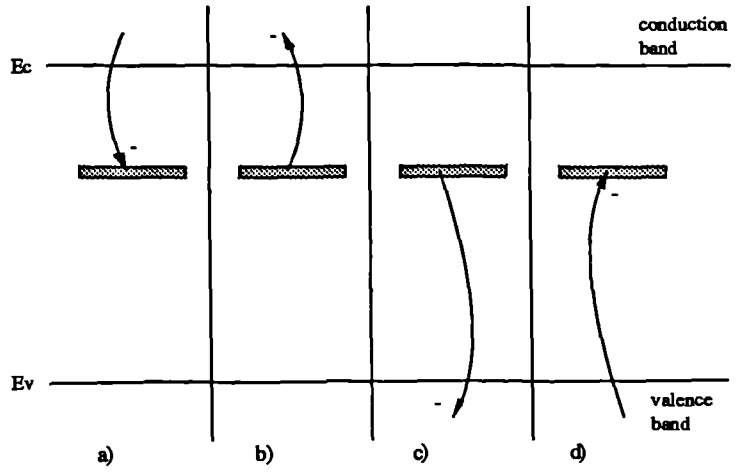

Figure 4.1. The change in the occupancy of bulk traps.

the electron or hole emission time constants, τ_{nc} and τ_{pc} are the electron or hole capture time constants. The four terms represent the processes (a), (b), (c) and (d) respectively. The time constants for emission and capture are given by

$$\tau_{ne} = (\sigma_n X_n v_{nth} N_c \exp((E_t-E_c)/kT))^{-1} \qquad \tau_{pe} = (\sigma_p X_p v_{pth} N_v \exp((E_v-E_t)/kT))^{-1}$$

$$\tau_{nc} = (\sigma_n v_{nth} n_s)^{-1} \qquad \tau_{pc} = (\sigma_p v_{pth} p_s)^{-1}$$

Where σ_n and σ_p are the electron and hole capture cross sections, v_{nth} and v_{pth} are the average thermal velocities, n_s and p_s are the free electron and hole densities, N_c and N_v are the effective density of states in the conduction and valence bands, E_t, E_c and E_v are the trap, conduction band and valence band energy levels, T is the absolute temperature and k is the Boltzmann's constant. X_n and X_p are "entropy factors" that account for the entropy change accompanying electron or hole emission from the trap [10,11 and 12 page 341].

In a buried channel charge coupled device the charge packet consists of electrons in an otherwise depleted n-type layer. Therefore the capture of holes can be ignored. For traps below the middle of the gap, $\tau_{pe} \ll \tau_{ne}$ hence they will always be occupied by an electron even with no charge packet present. Therefore only traps in the upper half of the band gap have to be considered. For these traps $\tau_{ne} \ll \tau_{pe}$ so the only processes of importance are electron capture from the conduction band and emission into it. The rate of change of trap occupancy simplifies to

$$\frac{dn_t}{dt} = \frac{N_t-n_t}{\tau_{nc}} - \frac{n_t}{\tau_{ne}} \qquad (4.1)$$

When a charge packet first arrives under a gate of a CCD, some of the signal electrons will be captured by the bulk traps. By solving equation (4.1), the density of trapped charge is given as

$$n_t = \frac{N_t\tau_{ne}}{\tau_{nc}+\tau_{ne}} (1-\exp(-t_g(1/\tau_{nc}+1/\tau_{ne}))) \qquad (4.2)$$

where t_g is the time the signal spends under a gate. When the charge packet moves to the next gate the signal density drops to zero and the traps start to emit their charge. By the time another charge packet comes along, some of those traps that have been filled by the previous charge packet may not be empty. Those traps that still have their trapped charge do not contribute to the CTI. The density signal lost to the available traps is given by

$$N_{lost} = n_t(1-\exp(-t_o/\tau_{ne}))$$

$$= \frac{N_t \tau_{ne}}{\tau_{nc}+\tau_{ne}} (1-\exp(-t_o/\tau_{ne}))(1-\exp(-t_g(1/\tau_{nc}+1/\tau_{ne}))) \qquad (4.3).$$

where t_o is the time between charge packets. If $\tau_{ne} \gg \tau_{nc}$, which would be the case for a deep trapping level below room temperature, then this simplifies to

$$N_{lost} = N_t(1-\exp(-t_o/\tau_{ne}))(1-\exp(-t_g/\tau_{nc}))$$

$$= N_t(1-\exp(-t_o/\tau_{ne}))F \qquad (4.4)$$

Where F is a "filling factor" and can be regarded as being the probability that a trap will be filled during the time a signal spends under the gate. If t_g is approximately greater than $2\tau_{nc}$ then this "filling factor" will be unity.

Some of the trapped charge may be emitted back into the signal thus reducing the density of lost charge. If $t_o \gg \tau_{ne}$ then the only contribution of importance is the charge emitted back into the signal when under the adjacent electrode. N_{lost} is then reduced by at least a factor $\exp(-t_{g+1}/\tau_{ne})$. This is important when the emission time constant is less than approximately twice the time the signal spends under the gate. In this case the density of lost charge becomes

$$N_{lost} = \frac{N_t \tau_{ne}}{\tau_{nc}+\tau_{ne}} \exp(-t_{g+1}/\tau_{ne})\ (1-\exp(-t_g(1/\tau_{nc}+1/\tau_{ne}))).$$

In the case of the UT101 CCD, three gates make up a pixel. If the CTI is defined as the fraction of charge lost as a signal packet is transferred from one pixel to another (Section 1.1.4.), the CTI will be given by

$$CTI = \sum_{i=1}^{3} N_i/n_s \qquad (4.5)$$

where the sum is over the three gates that make up a pixel and n_s is the effective signal density. N_i is the density of charge lost when the signal is under gate i. The maximum CTI is given by $3N_t/n_s$.

The above model assumes that the trap density is uniform and the electric fields within the CCD are low enough so that the emission rates from the traps are field independent. This would be a reasonable assumption for the fields usually encountered within the CCD. However, the effect on the emission rates from shallow traps could be significant [13].

4.3. The methods for measuring the CTI

4.3.1. X-ray response

There are several methods that can be employed to measure the charge transfer inefficiency. One method, often used in the qualification of CCDs for low level operation, is to map the response of the CCD to a flat field of monoenergetic x-rays, such as those from an Fe^{55} source. The x-rays interact via the photoelectric effect and produce approximately 1600 electrons per interacting photon. These electrons constitute a signal in the CCD which is clocked out of the device. The CCD is continuously exposed to x-rays and read out. The magnitude of the single pixel hits can be monitored. Those hits recorded close to the output node will show little signal lost due to a finite CTI. The signal magnitude of these single pixel hits can be taken as the signal size before any transfer has taken place. Those furthest from the output will be affected the most and will show the greatest pulse height degradation. The fraction of charge lost is a measure of the charge transfer inefficiency. This method was not thought to be suitable for the present investigation as it does not provide the flexibility required, either to control the signal size nor the sparseness of the data.

4.3.2. Extended pixel edge response

The extended pixel edge response (EPER) technique involves uniformly illuminating the CCD. The image is then read out but extra clock cycles are applied so as to measure the charge deferred to trailing pixels due to the finite CTI. According to Janesick [14] the CTI is given by the ratio of the trailing charge to the charge in the final pixel of the column, divided by the number of transfers. This method provides a convenient "standard" CTI measurement as it is independent of clocking rate and time between signal packets etc. and gives a CTI figure for a given CCD technology. However, it does not mimic actual device operation as the device is uniformly illuminated. For many applications, including x-ray astronomy, only a small fraction of the total pixels include signal charge, the remaining device being empty. Therefore a technique was required that provided sparse data in a controlled manner.

4.3.3. Periodic pulse technique

It was fortunate that the UT101 CCD provides a structure at the end of the readout register by which charge can be injected into the device. This enables the most suitable method for measuring the CTI, known as the periodic pulse technique, to

be employed. This method allows the required control over the signal size and frequency. The periodic pulse technique has been described by Mohsen and Tompsett [9] and by Collet [1]. A group of several consecutive signal packets, of equal size, are injected into the CCD and the output of the device monitored. The CTI can be obtained by measuring the signal size of the first, A, and last, B, charge packets in the group at the output. Assuming that all the traps causing a finite CTI have been filled by the previous charge packets, the size of the last packet gives the size of the first packet in the group before any transfers have taken place. The CTI, defined as the fraction of charge lost when a signal packet is transferred from one pixel to the next, can be calculated from

$$CTI = 1 - (A/B)^{1/N} \approx (B-A)/(NB) \text{ if the CTI is small.}$$

Here N is the total number of pixels through which the charge has had to transfer to get to the output.

4.4. The measurements on the increase of the CTI with radiation

4.4.1. The injection of charge

The periodic pulse technique requires the reliable injection of charge into the CCD. The structure at the end of the readout register of the UT101 CCD enables several different methods of charge injection. Two of these methods, dynamic injection and potential equilibration, were investigated for subsequent use.

The dynamic injection technique is illustrated in Figure 4.2. In this case, a voltage is applied to the input diode. When the RØ1 phase goes high the input gates are pulsed together. Signal charge floods the area under the input gates, and the first

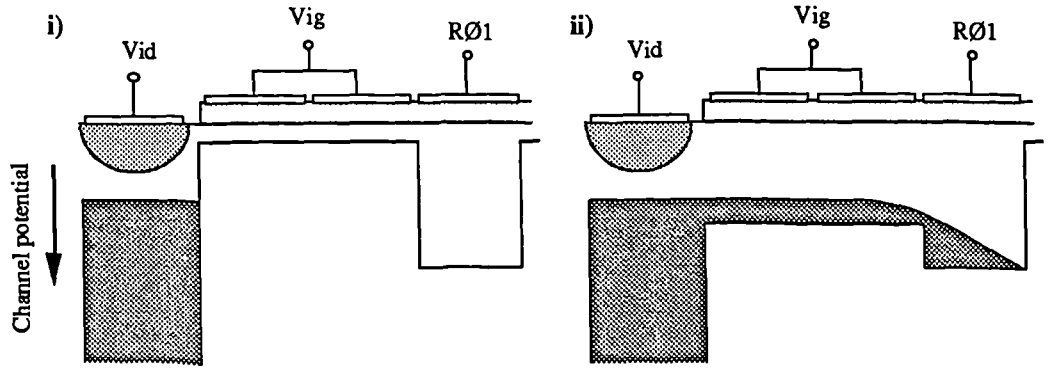

Figure 4.2. The input of charge by dynamic injection.

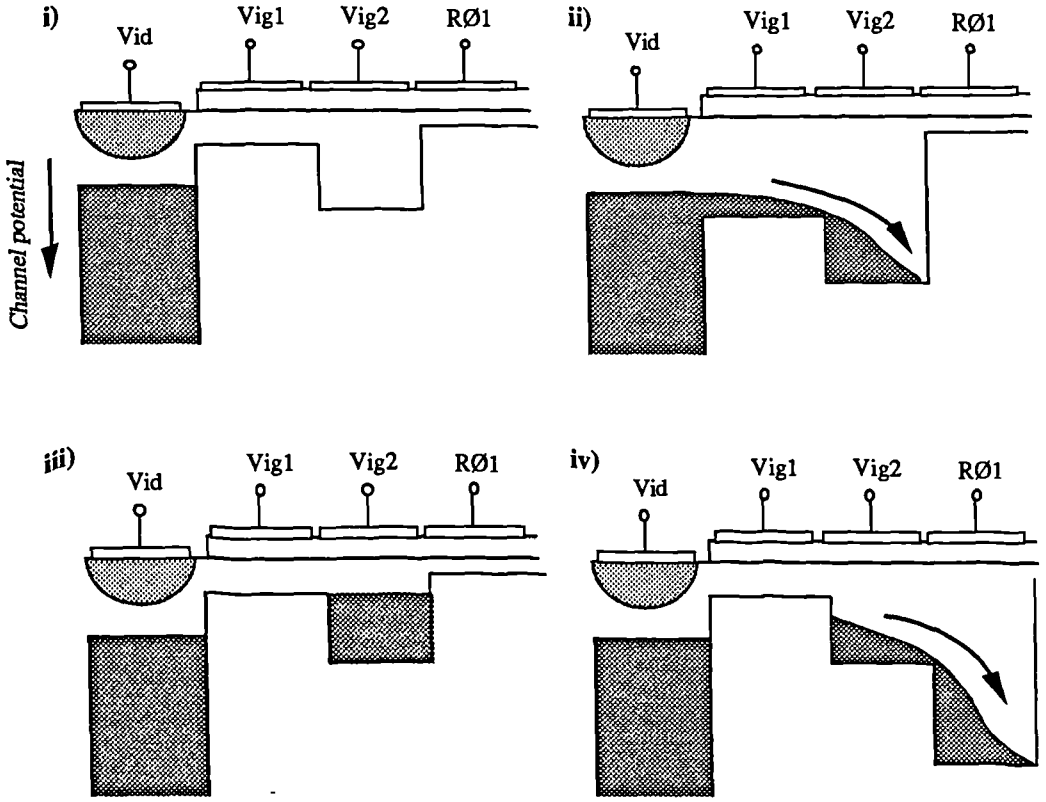

Figure 4.3. The injection of charge by potential equilibration.

RØ1 gate, to a level determined by the potential applied to both the input diode and the input gates and also the integration time set by the pulse width. When the input gates are pulsed off, the signal charge is trapped under RØ1. This charge will be subsequently clocked along the readout register and out of the device. This method of injecting charge is very simple to implement as it requires only one pulse to be applied to the input gates when the RØ1 phase goes high.

The potential equilibration or "fill and spill" technique is illustrated in Figure 4.3. It uses both the input gates, V_{ig1} and V_{ig2}, which are biased so that the potential applied to V_{ig2} is greater than V_{ig1} by an amount , ΔV. Whilst the potential under RØ1 remains low, the input gates are pulsed high, keeping ΔV constant. Charge then flows from the input diode to the area under these input gates. As the pulse goes low charge flows back to the diode. No charge can flow along the readout register as a potential difference exists between RØ1 and V_{ig1}. However, there will be an amount of charge left under V_{ig2}. When RØ1 subsequently goes high, this charge flows under the adjacent RØ1 electrode ready to be clocked through the device. The amount of charge that is transferred in dependent of ΔV and not on the biasing on the input diode or on the integration time. This gives a distinct

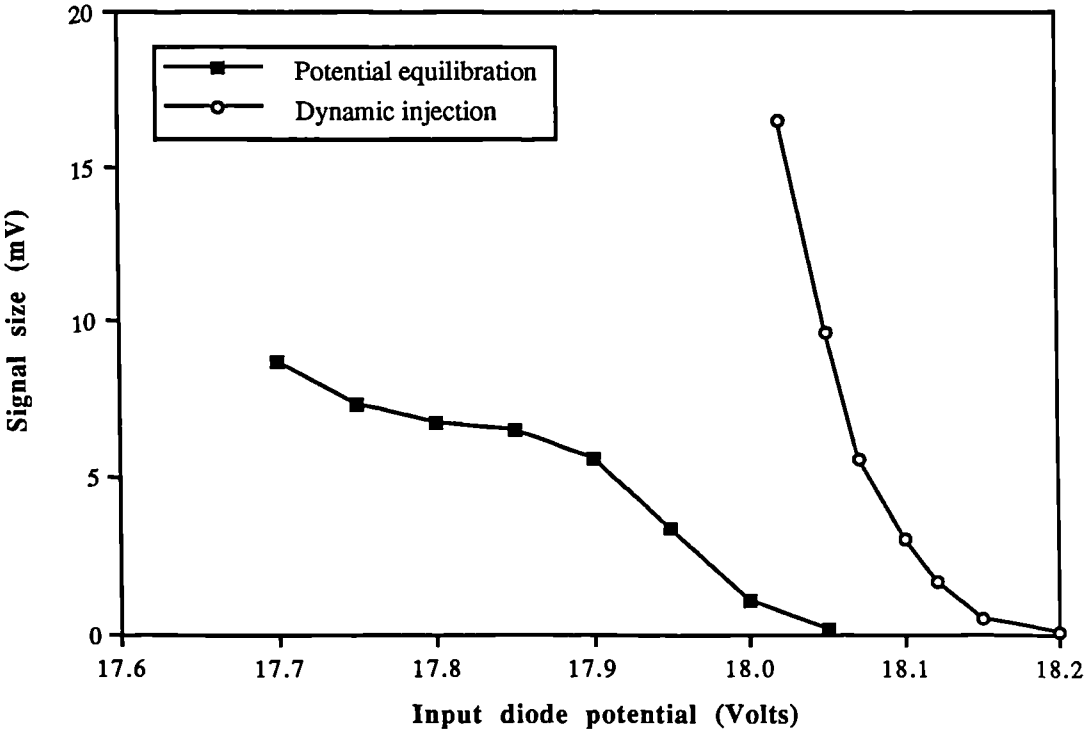

Figure 4.4. The injected signal size measured at the output as a function of potential applied to the input diode.

advantage over the dynamic injection method as the input of charge is well controlled.

The difference between the two methods is illustrated in Figure 4.4. Here the signal level measured at the output of the device, after pre amplification, is presented as a function of potential applied to the input diode. The signal level is a very strong function of diode potential when using the dynamic injection method. This leads to difficulties when small signals have to be injected. However, if the diode potential is low enough to allow complete filling of the potential well under V_{ig2}, the signal size is virtually independent of the diode potential when the potential equilibration technique is employed. If the diode potential is set too low charge is able to flood the readout register. If the applied potential is set somewhere above this point, then the amount of charge is only dependent on the difference between V_{ig1} and V_{ig2}. An added advantage of this method is that the amount of charge injected is virtually independent of the temperature. Therefore the potential equilibration technique was the method used to inject charge for most of following work.

4.4.2. The measurement of the CTI

To form the signal for the periodic pulse technique, ten consecutive charge packets were injected into the readout register. This injection was constantly repeated with a time, t_o, between injections. In order to inject charge, two pulses had to be applied to the input gates. These pulses were supplied by Hewlett Packard 8015A and 8116A pulse generators, triggered by the CCD master controller. The number and frequency of the injections could be controlled by the user, via the PDP11 microcomputer.

For most of the measurements the readout register was clocked at 83 kHz with uneven phases, RØ1 and RØ3 both being 500 ns wide (Figure 4.5). This implies that the time the signal spent under a gate connected to the RØ1 and RØ3 phases was 500 ns and those connected to the RØ2 phase was 12 μs. The clock rise and fall time was set by hardware to 50 ns. It was found that a clock cross over (overlap) of less than 50% has a significant effect on the transfer of charge. Therefore the clock edges were set so that they crossed over at 85% of their maximum amplitude.

As a device is irradiated the dark current increases. To prevent dark current from the image and store sections effecting the measurements, these regions were clocked up a row (i.e. away from the readout register) every time a row from the readout register was clocked out. For most of the measurements the burst of ten consecutive charge packet was injected once a row, giving a t_o of around 5 ms. However, in order to calculate the energy level of the main electron traps, the signal

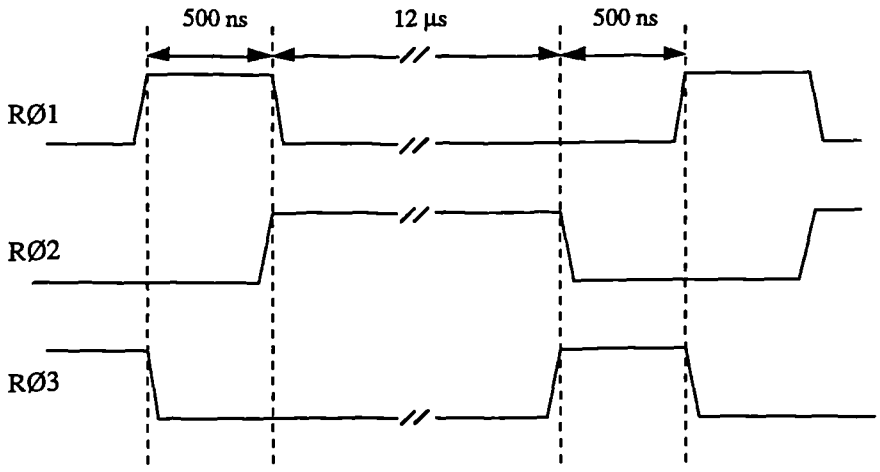

Figure 4.5. The timing diagram of the drive sequence for the readout register.

was injected more frequently to give a range of t_o from 500 μs to 5 ms.

The output of the CCD (gain ~0.7) was taken to a preamplifier (gain ~5) then to a main amplifier (gain ~10) and monitored using a Hewlett Packard 54100A digitising oscilloscope. The signal measured on the oscilloscope, V_{out}, could be converted into the number of signal electrons, N_{sig}, using the following expression

$$N_{sig} = \frac{C_n V_{out}}{qG}$$

where q is the electronic charge, C_n is the output node capacitance and G is the voltage gain of the on-chip amplifier/off-chip amplifier combination. This was measured by sending a 10 mV square wave down the V_{rd} line and monitoring the output. The output node capacitance was measured by monitoring the dark current flowing down the reset line, I_{rd}, and noting the magnitude of the output due to the dark current, V_{dark}. The output node capacitance is then simply

$$C_n = \frac{GI_{rd}}{fV_{dark}}$$

where f is the readout frequency. C_n has been calculated to be 0.15 pF which implies that, for a signal size of 1000 electrons and a gain of 35, the output signal would be around 35 mV.

By averaging over 1000 rows, the error in the measurement of the CTI is mainly determined by the resolution limitation of the oscilloscope. The CTI was calculated from

$$CTI = 1 - \left(\frac{A-x}{B-x}\right)^{1/N} \approx \frac{B-A}{N(B-x)}$$

where A and B are the magnitudes of the signal in first and last pixel of the group of ten respectively and x is the output from the pixels not containing signal charge. N is the number of pixels in the readout register and is 400 for the UT101 device. Assuming that the errors measuring A, B and x are independent and equal to ξ, the error in measuring the CTI, δCTI is given by

$$(\delta CTI)^2 = \xi^2\left(\frac{\partial CTI}{\partial A}\right)^2 + \xi^2\left(\frac{\partial CTI}{\partial B}\right)^2 + \xi^2\left(\frac{\partial CTI}{\partial x}\right)^2$$

$$\approx \frac{2\xi^2}{N^2(B-x)^2}\left(1 - N(CTI) + N^2(CTI)^2\right).$$

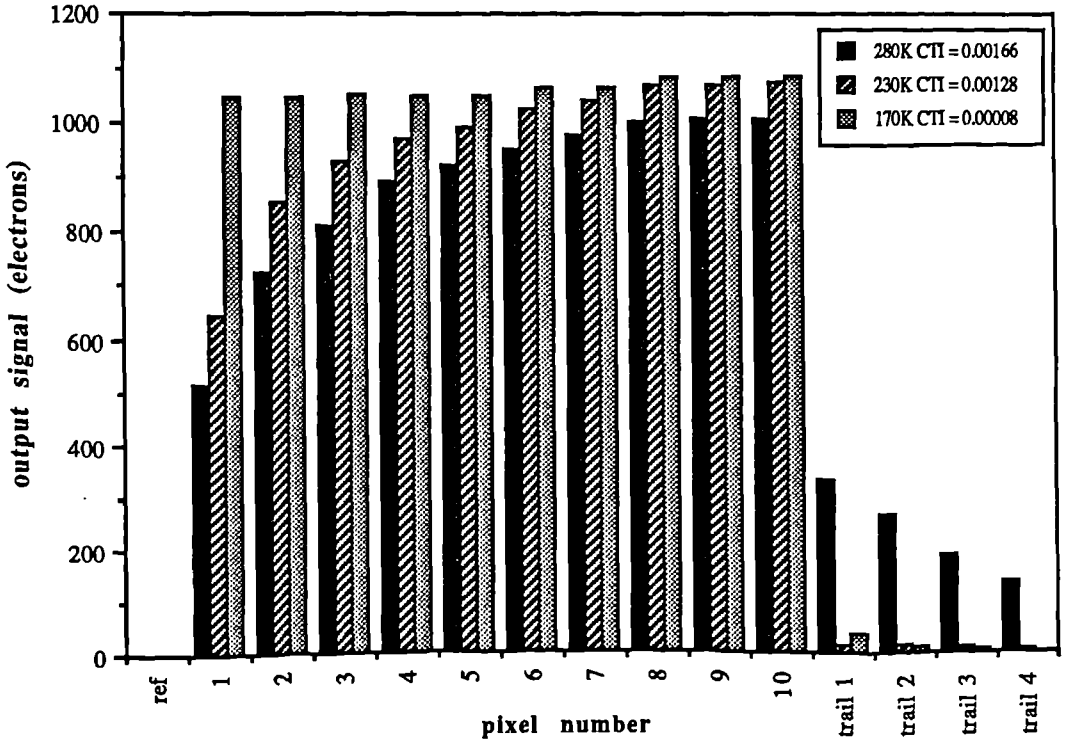

Figure 4.6. The measured output for a device that had received 40 krad(Si).

This shows that the error increases for small charge packets. The resolution limitation of the oscilloscope gave an error on the signal measurement of 0.2 mV for a 35 mV signal (1000 electrons). For a CTI of 5 10^{-5} the error on the CTI measurement is around 2 10^{-5}. For a CTI of 100 10^{-5} this goes down to 1 10^{-5}.

Typical output signals from an irradiated device are given in Figure 4.6. The readings taken at 170K show little difference between the signal from the first and the last charge packet in the group of ten and the CTI is good. However, as the device is warmed to 230K, an increase in the CTI is apparent as the size of the first signal packet is reduced. The CTI is even worse at 280K and it is apparent that the emission time constant for the traps is quite short as significant charge is being re-emitted into the trailing pixels.

4.4.3. The CTI as a function of Temperature and Dose.

The results for the CTI measurement of an irradiated device are shown in Figure 4.7. Here the device was irradiated at room temperature with all connections grounded. No significant difference was observed for devices irradiated whilst clocking at 180K. The time between the bursts of signal was 5 ms with a charge

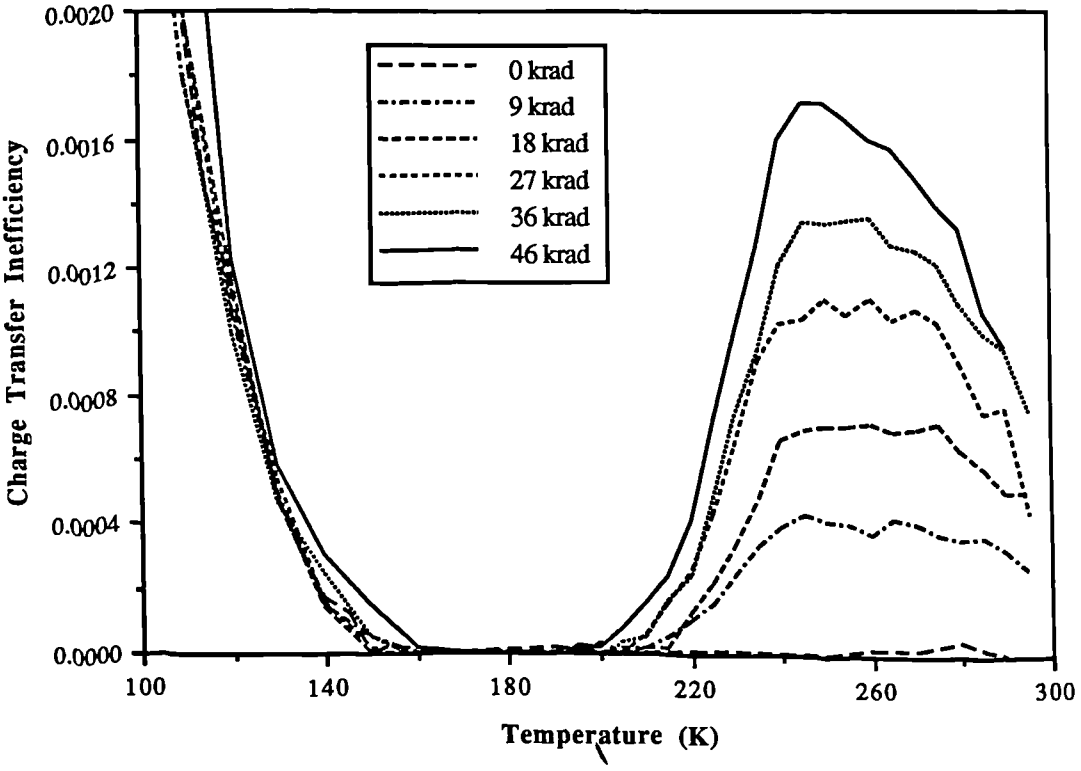

Figure 4.7. The CTI versus temperature for a signal size of 1000 electrons and a t_o of 5 ms.

packet size of 1000 electrons. A peak can be clearly seen emerging at 250K. This is due to an increasing density of a bulk trapping level, the peak value being given by three times the ratio of the trap density to the signal density. On the low temperature side of the peak the emission time constant for the trap is low enough so that some of the traps remain filled by the time the next burst of signal comes along. The CTI is thus reduced from its maximum value. On the high temperature side of the peak some of the trapped charge is emitted back into the signal before it moves to the next electrode. The CTI is also lower as the dark current tends to increase the effective signal density and acts as a "fat zero". A "fat zero" is the term applied to a deliberately injected background signal intended to reduce the CTI. For small signal applications, this background charge is undesirable as it considerably increases the noise on the signal.

The CTI measured as a function of dose at 250K, for two devices from different batches, is shown in Figure 4.8. At this temperature the CTI is a maximum. The CTI increases linearly with dose indicating a linear relationship between the introduction rate of the trap and the irradiating fluence. The consistency between batches is encouraging as far as the development of a model is concerned.

The CTI below 160K does not appear to change significantly with irradiation but does increase to high levels as the temperature is reduced. This peak is due to a trap with an emission time constant that is short enough at 160K to allow all the trapped charge to be emitted back into the signal whilst under the adjacent electrode. Therefore the energy level of this trap is much nearer the conduction band edge than the trap causing the peak at 250K. It could be due to the Si-A centre being present before irradiation. This has an energy level of 0.18 eV below the conduction band edge. The Si-A centre is an oxygen related complex and it is possible that there is a high level of oxygen within the bulk silicon which assists with the gettering process. However, this requires further investigation as it is known that the oxygen impurities compete for the vacancies produced by the irradiation [15] and so an increase in the peak should be observed.

It is also possible that this trapping is by the donor level (known as "carrier freeze out"). CTE degradation at low temperatures attributed to the donor level has been observed by Banghart *et al* [13]. However, from their measurements they indicated no significant charge trapping above 80K due to the reduction of the emission time constant by field effects. Their measurements were made at a clock frequency of 3 MHz and large signal packets (~100,000 electrons). It will be shown in later sections that the signal size and readout rate have a significant effect on the CTI.

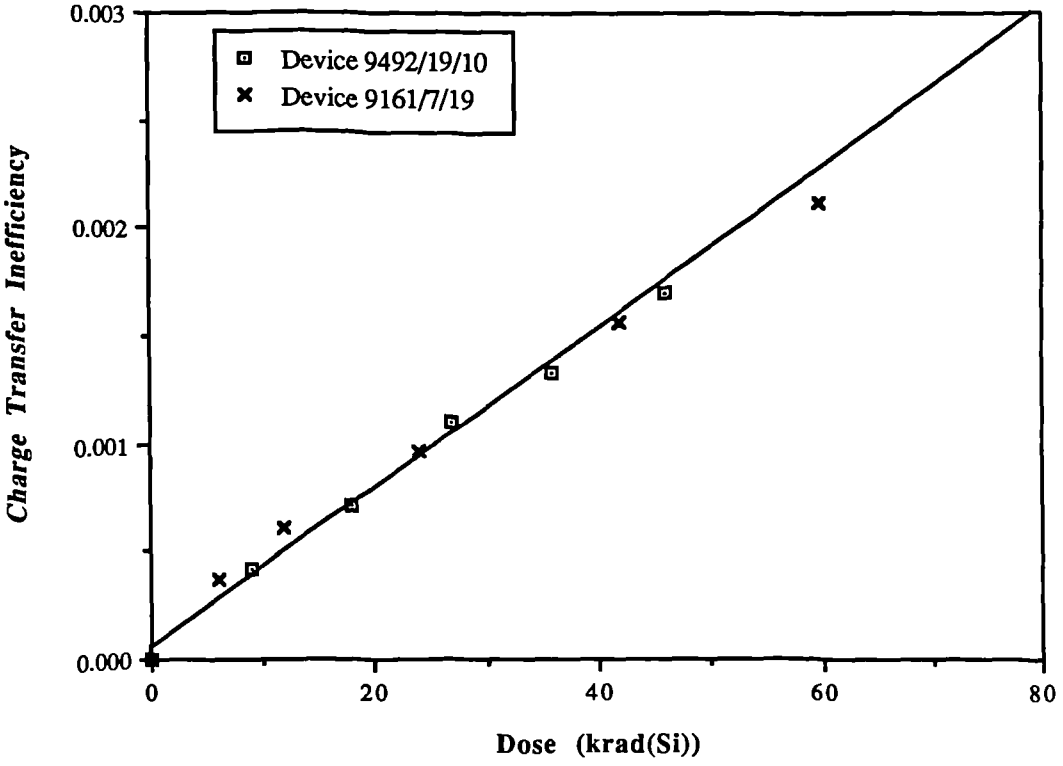

Figure 4.8. The CTI increase at 250K as a function of dose. The two sets of points are from two devices from different batches.

For small signal levels, as used in the experiments presented in this work, the CTI is significantly worse than for larger charge packets. Therefore it is possible that "carrier freeze out" effects are being observed here.

4.4.4. The measurement of the energy level of the main radiation induced defect.

Following the method of Collet [1] the energy level and capture cross section of the radiation induced trap can be calculated if the time between the bursts of signal, t_o, is varied. Some of the results of the CTI versus temperature measurement for a device that had received 30 krad, using a signal size of 10,000 electrons, is shown in Figure 4.9. As the time between bursts of signal decreases, less time is available for the traps to emit their charge. Therefore the low temperature side of the peak shifts towards higher temperatures where the emission time constant is reduced. At the point on this side of the peak where the CTI is half its maximum value, at $T_{1/2}$, half of the trapped electrons have been emitted in the time t_o. Therefore the electron emission time constant can be calculated from

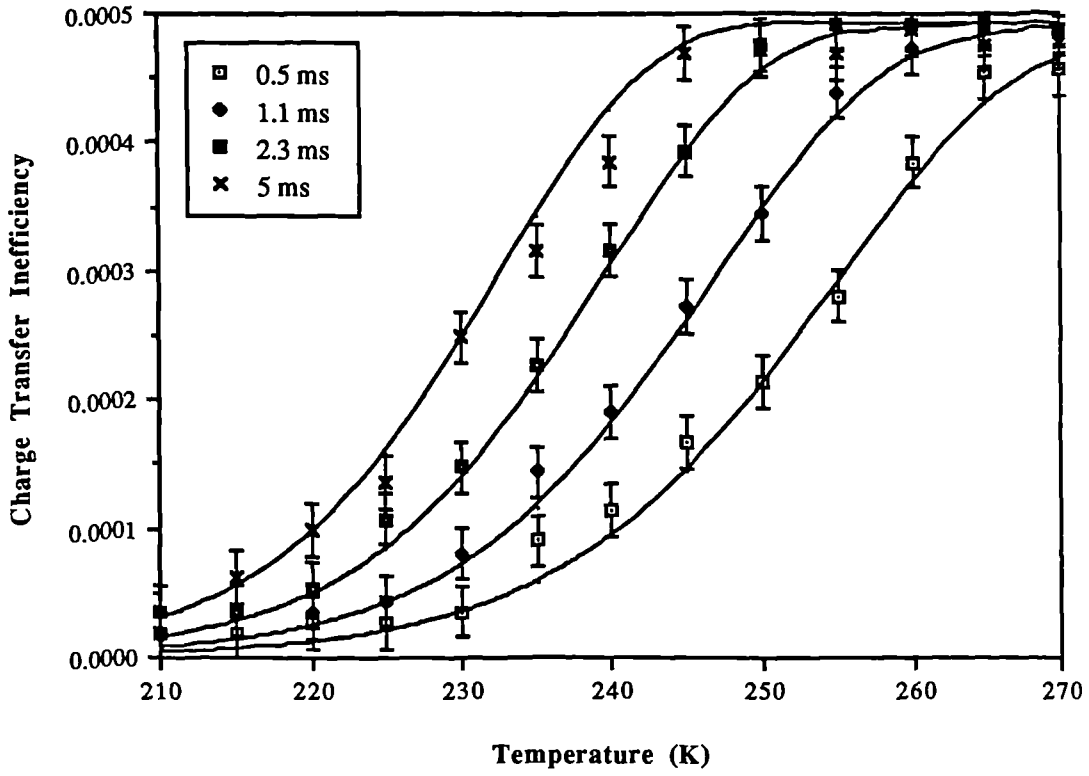

Figure 4.9. The shift in the peak as the time between the signal burst is altered. The device had received approximately 30 krad(Si) and the signal level was 10,000 electrons.

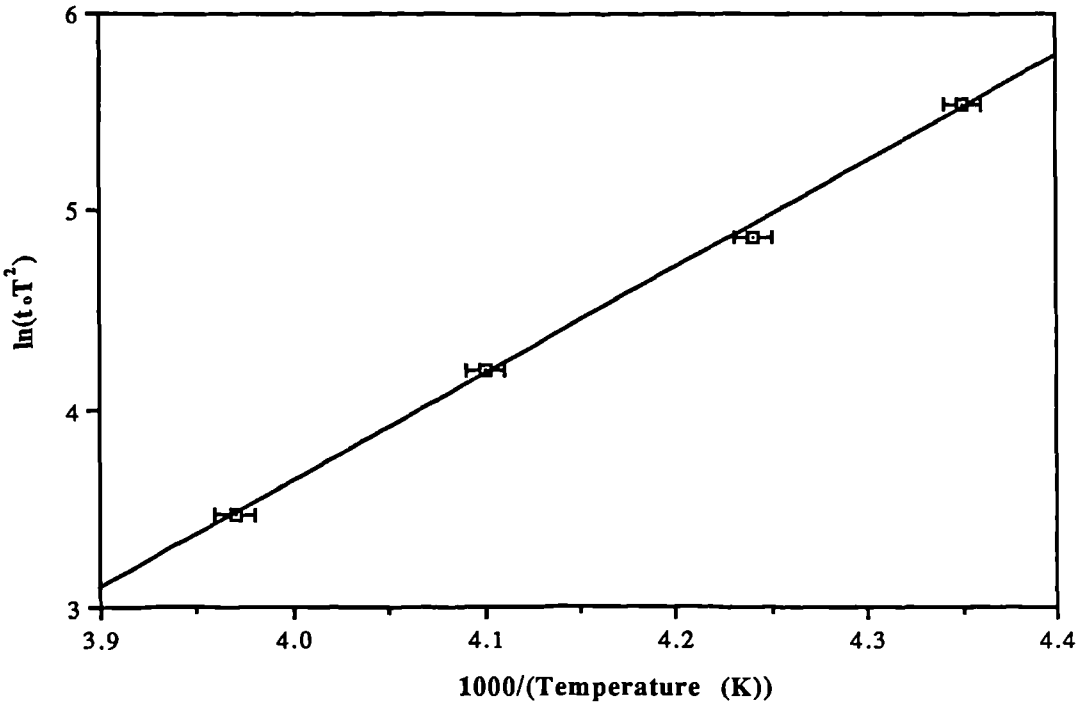

Figure 4.10. A plot of $\ln(t_o T_{1/2}^2)$ versus 1000/T to obtain the energy level and capture cross section of the trap.

$\tau_{ne} = t_o/\ln 2.$

Combining this with the emission time constant given in section 4.2 and calculating the known constants yields

$$E/kT_{1/2} = \ln(t_o X_n \sigma_n T_{1/2}^2\ 10^{22})$$

where E is the energy level of the trap below the conduction band edge.

Assuming there is no temperature dependence of the cross section, the gradient of the $\ln(t_o T^2)$ versus T^{-1} graph (Figure 4.10) gives the energy level of the trap causing the peak and the intercept on the ordinate axis allows an estimate of $X_n\sigma_n$. Using the measured data, the energy level has been calculated to be 0.47 ± 0.03 eV below the conduction band edge and $X_n\sigma_n$ estimated to be $(6 \pm 2)\ 10^{-15}$ cm^2. These values are consistent with those of the Si-E centre (Table 2). The solid curves plotted in Figure 4.9 were obtained by using this data to calculate the emission time constant. This was substituted into equation (4.5) in order to calculate the CTI, assuming that the "filling factor" is unity and that no trapped charge is emitted back into the signal. The value of N_t/n_s was calculated from the maximum measured value of the CTI.

E_C-E_t (eV)	σ_n (cm^{-2})	Reference
0.4	_	G.D. Watkins *et al*, Phys. Rev., **134**, 1359, 1964.
0.471	_	J.W. Walker *et al*, Phys. Rev. B, **7**, 4587, 1973.
0.44	» 10^{-16}	L.C. Kimerling, Inst. Phys. Conf. Series, **31**, 221, 1977.
0.456	3.7 10^{-15}	S.D. Brotherton *et al*, J. App. Phys., **53**, 5720, 1982.
0.45	1.1 10^{-16}	C.A. Londos, Phys. Stat. Sol. (a), **113**, 503, 1989.
0.42	_	O.O. Awadelkarim *et al*, Phys. Stat. Sol. (a), **120**, 539, 1990.

TABLE 4.1. Some measurements of the energy level and capture cross sections attributed to the Si-E centre that can be found in the literature.

There are many measurements on the energy level of the Si-E centre and some of those found in the literature are shown in Table 4.1. However, there are few measurements for the capture cross section and there appears to be a large discrepancy between those measurements that are published. Brotherton and Bradley [16] have measured X_n to be 1.7 for the Si-E centre by comparing electron capture data with thermal emission rates using DLTS. Therefore the capture cross section from this present work is calculated to be $(3 \pm 1)\ 10^{-15}\ cm^2$. This is in very good agreement with the Brotherton and Bradley result of $(3.7 \pm 0.2)\ 10^{-15}\ cm^2$. However cross sections as low as $10^{-16}\ cm^2$ have also been published.

4.4.5. Signal density effects and the estimation of the trap density.

In order to estimate the radiation induced trap density, it is first necessary to calculate or measure the signal density. The distribution of signal charge can be calculated by solving the Poisson equation. A simplified one dimensional approach to the problem has been taken by Kent [17]. In this case, a p-channel device was analysed with both a stepped impurity profile and a Gaussian impurity distribution. Here a similar approach has been taken to estimate the charge distribution for the EEV CCD.

A reliable measurement of the doping profile for the UT101 CCD is not available. However, it has been shown that the impurity distribution for the ion implanted buried channel of a CCD that has undergone subsequent high temperature

processing, is closer to a uniform distribution than the expected Gaussian [18]. Therefore a uniform distribution is used for the calculations.

The exact method for the calculation is given in Appendix 1 and some of the results are presented in Figure 4.11. Here the donor density was 10^{16} cm^{-3} and an implant depth of 1 μm. The calculations provided a one dimensional charge distribution through the CCD. In order to calculate the amount of charge in the signal, the results were integrated and multiplied by the gate area (7μm by 22μm). This is clearly only an approximation as it assumes that the potential well holding the charge has a sharp cut off between gates. A more accurate approach to the problem requires the solution of the Poisson equation in two dimension. This was not regarded as being appropriate due to the uncertainty in the exact distribution of the implant. However, the results obtained do give an indication as to the order of magnitude signal density expected for a given signal size. For example, at 300K the calculated peak signal density for a charge packet containing 1,000 electrons is 6.2 10^{13} cm^{-3}. For a signal size of 10,000 electrons the peak signal density rises to 5.8 10^{14} cm^{-3}. For very large signal packets the peak signal density reaches a maximum given by the donor concentration. As the temperature decreases, the

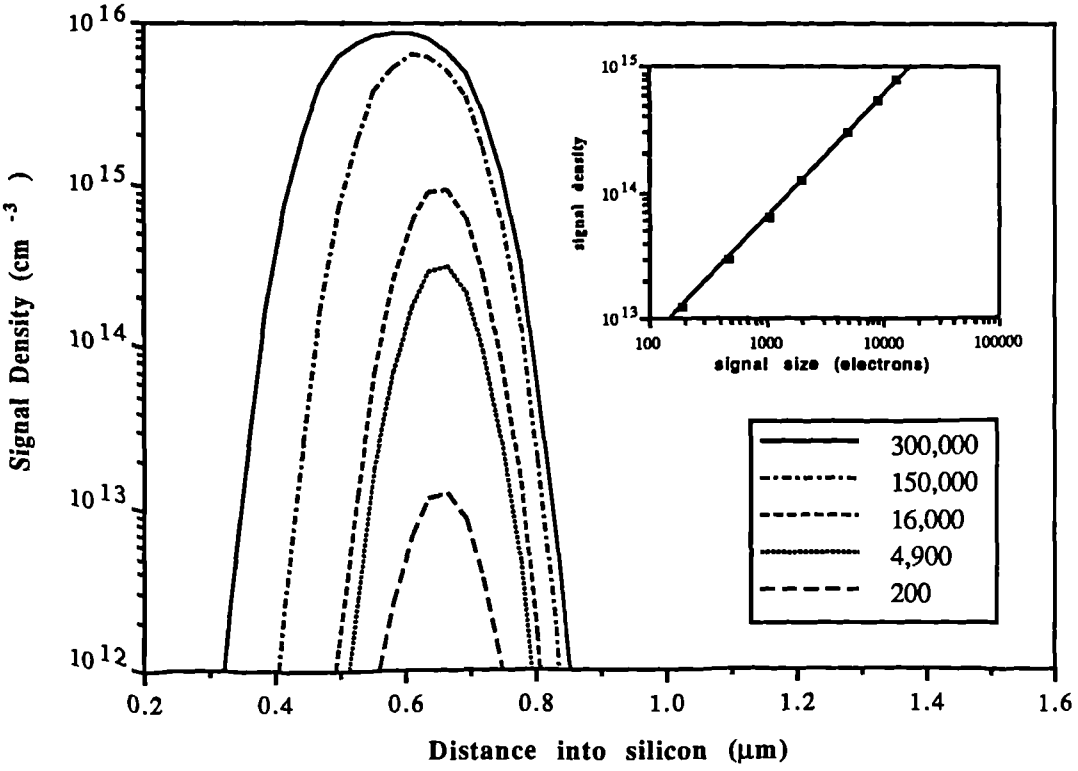

Figure 4.11. The calculated charge distribution for the UT101 CCD for various charge packet sizes at 300K. The inset shows the peak signal density as a function of signal size.

thermal energy of the signal electrons goes down and the signal packet contracts. Therefore the signal density goes up. For example a 1,000 electron signal has a peak signal density of 7.0 10^{13} cm^{-3} at 250K compared with 7.5 10^{13} cm^{-3} at 200K.

From these calculations it is clear that the effective signal density for a signal containing 1,000 electrons will be between 10^{13} cm^{-3} and 10^{14} cm^{-3}. Using the data for the capture cross section, the capture time constant for the traps could be as low as 1 μs. Therefore, if the signal spends less time than this under a gate, then the "filling factor" from equation (4.4) will be significantly less than unity.

The effect that the time the signal spends under a gate has on the "filling factor" is shown by the measurements given in Figure 4.12. Here the CTI was measured at 250K for an irradiated device as a function of the time the signal spent under two of the three gates of a pixel, keeping the overall readout frequency constant at 83 kHz. Care was taken to ensure that the clock cross overs remained unaltered. The time the signal spent under a gate connected to the RØ2 phase was around 12 μs so it can be assumed that the "filling factor" for this phase in unity. However the time spent under the gates connected to RØ1 and RØ3 is very much less than 12 μs so

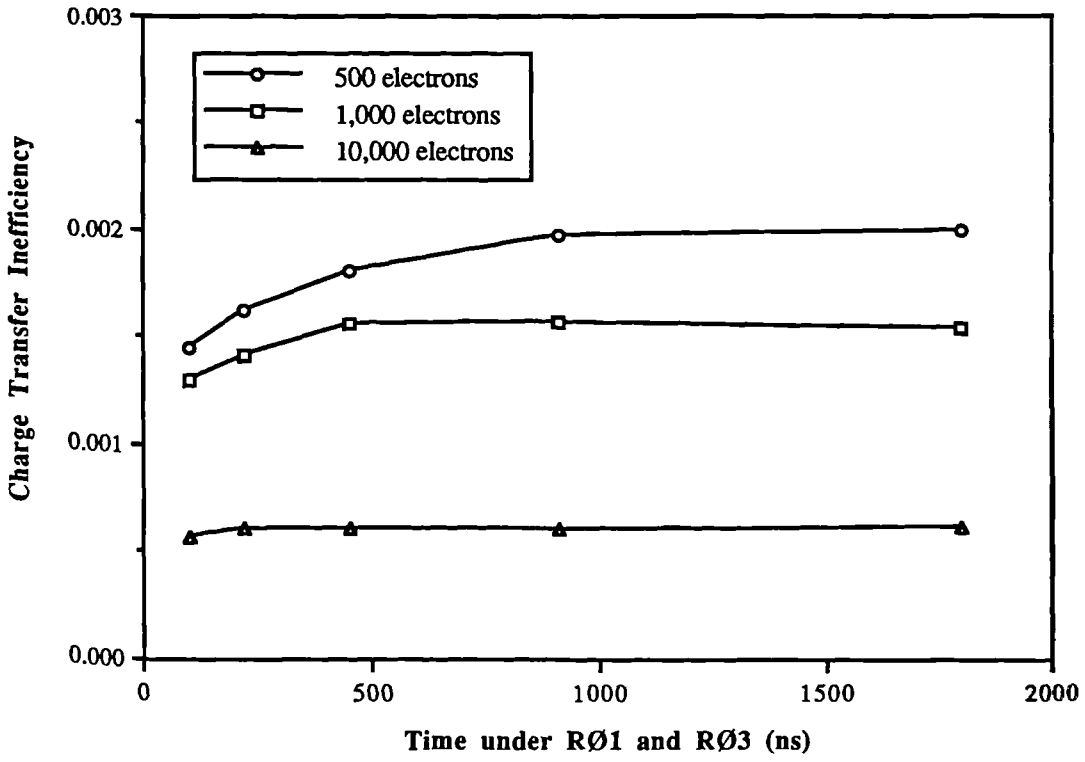

Figure 4.12. The variation of CTI as a function of the time the signal spends under RØ1 or RØ3.

there exists the possibility of incomplete charge trapping.

It is apparent from the measurements that the CTI is worse for small signals. This is as expected from the calculations of the signal density. It can also be seen from the figure that, as the time under RØ1 and RØ3 is reduced, the "filling factor" becomes smaller and the CTI improves. The point at which this improvement starts is around twice the capture time constant for the traps. As the capture cross section is known, a measurement of the capture time constant allows an estimate of the effective signal density.

The results for a signal size of 500, 1,000 and 10,000 electrons are shown in Table 4.2. A tentative comparison with the results of the calculation are also made. The calculated values of the signal density appear to be in good agreement with the measured effective signal densities. However, the calculated values of the peak signal density are not consistent with the magnitude of the maximum CTI when the "filling factor" is unity. For example, from the calculations the signal density for a 1,000 electron signal in approximately double that of a 500 electron signal, whereas, from maximum CTI values the signal density should be around 25% higher. This discrepancy can be attributed to the approximation of a stepped doping profile. The variation of the measured signal density as a function of signal size is shown in Figure 4.13.

An indication of the importance of the signal density is graphically illustrated in Figure 4.14. Here the CTI is plotted as a function of signal size for an irradiated device at a temperature of 180K, the temperature at which the CTI is a minimum. The CTI for signal sizes above 1000 electrons is around 5 10^{-5} which is only just acceptable for x-ray spectroscopic applications [8]. However, for smaller signal sizes the CTI dramatically increases to around 40 10^{-5} for a 300 electron charge packet. This would seriously degrade the resolution of x-ray spectrometers.

Signal size (electrons)	measured capture time constant (ns)	measured signal density (10^{13} cm^{-3})	calculated peak signal density (10^{13} cm^{-3})
500±5%	400±100	3±1	3.8
1,000±5%	200±50	6±2	7.0
10,000±5%	<100	>13	63.9

TABLE 4.2. The measurement of the effective signal density.

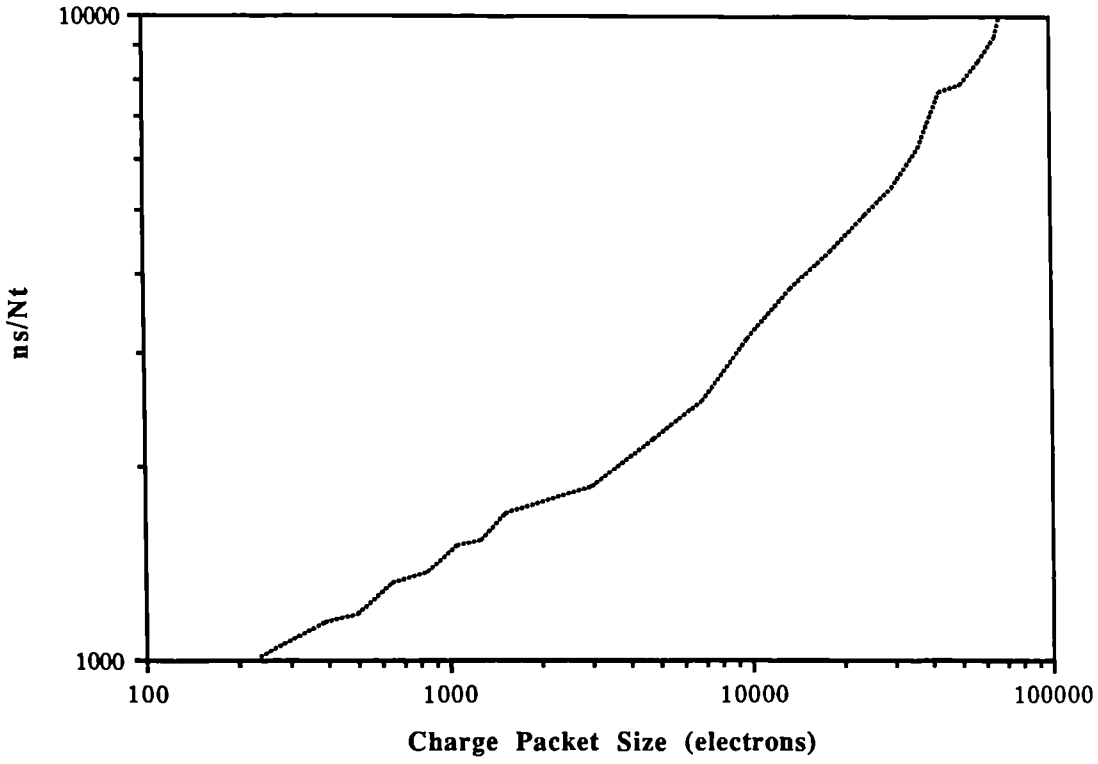

Figure 4.13. The measured ratio of the effective signal density to trap density for a device that had received 60 krad(Si).

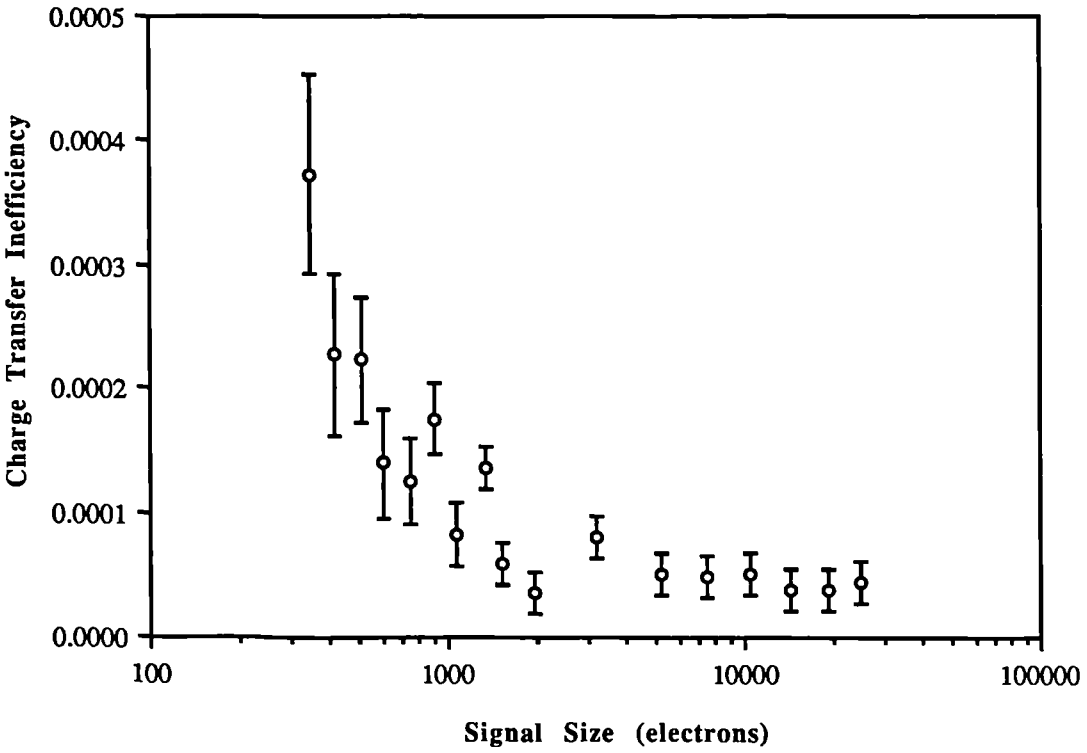

Figure 4.14. The variation of the CTI as a function of signal size measured at 180K. The device had received 60 krad(Si).

Having obtained the effective signal density, it is now possible to estimate the density of the radiation induced traps. Using a value of 6 10^{13} cm^{-3} for the signal density for a signal size of 1000 electrons, the CTI measurements from Figure 4.7 can be converted to the trap density as a function of dose. The results are shown in Figure 4.15. The introduction rate of a radiation induced defect is defined as the trap density divided by the particle fluence. In order to calculate the introduction rate for the centre found in this work, it is first necessary to convert the ionising dose measured in rads to a particle fluence. The beta spectrum from the Sr^{90} source is composed of a range of energies and not all of the betas are minimum ionising. However, the only realistic way to obtain the effective fluence from the source was to convert the dose measured in rad(Si) into a fluence of minimum ionising particles. 1 rad(Si) deposited in the epitaxial layer of the CCD corresponds to a minimum ionising electron fluence of 4 10^{7} cm^{-2}. Therefore the introduction rate is calculated to be (0.020±0.006) cm^{-1}. The error is dominated by the uncertainty in the measurement of the signal density. Kimerling [19] stated that the introduction rate increases with increasing phosphorus content and so care must be taken when comparing results with other workers. Walker and Sah [20] gave an introduction rate of 0.015 cm^{-1} for 1 MeV irradiated samples with a phosphorus concentration of

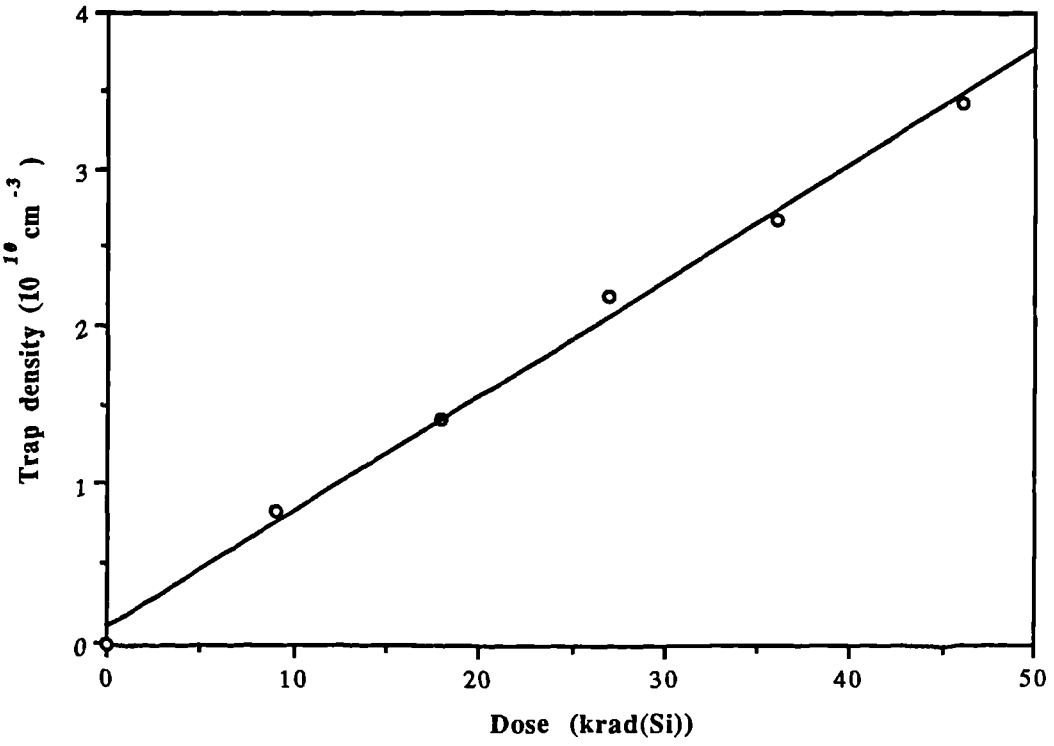

Figure 4.15. The variation of the calculated trap density as a function of dose.

5 10^{15} cm^{-3} which agrees well with the result from this work.

4.4.6. Annealing of the damage.

If sufficient thermal energy is given to the silicon lattice then the radiation induced defects will become mobile. They will then move around and eventually break up or recombine with other defects, forming a different defect complex. At a given temperature, the number of defects of a certain type remaining after a time t is given by

$$N = N_0 \exp(-t/\tau)$$

where N_0 is the original number of defects and τ is a characteristic time that depends on the defect type and temperature and takes the form

$$\tau = \nu^{-1} \exp(E_a/kT)$$

where E_a is the activation energy which depends on the type of defect and ν is known as the frequency factor. For the annealing of the Si-E centre Hirata *et al* [21] found that the frequency factor for defects created by 2 MeV electron and Co^{60} irradiated phosphorus doped silicon was in the order of 10^8 Hz with an activation

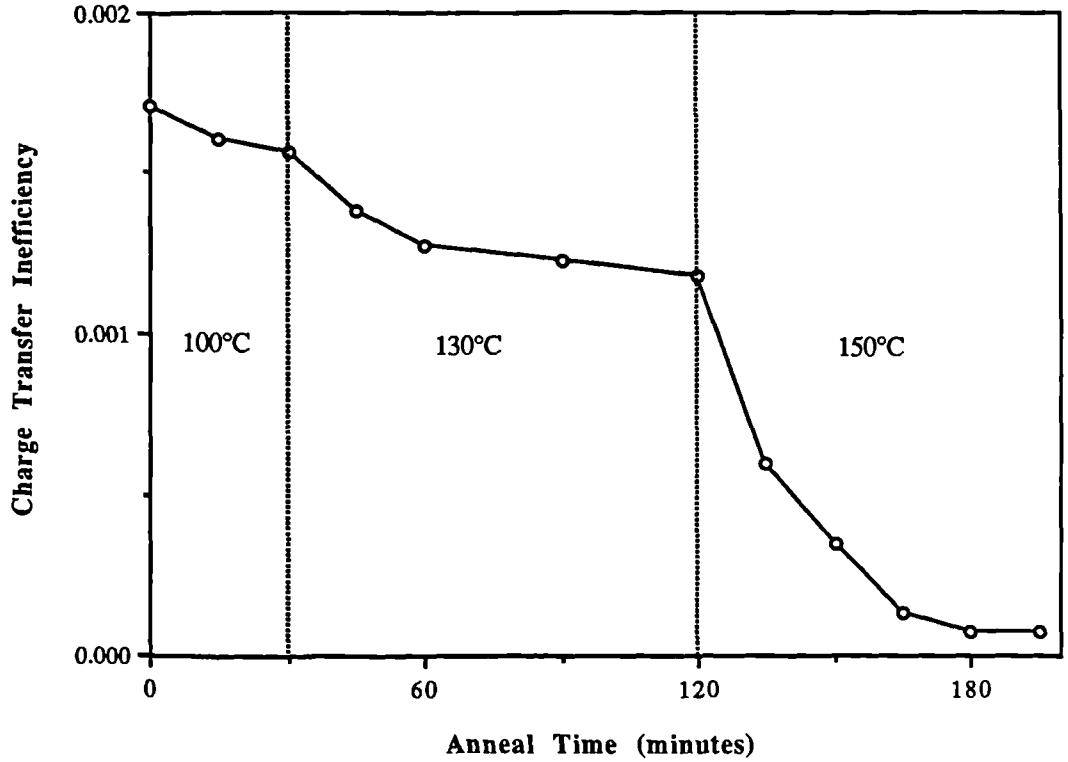

Figure 4.16. The improvement in the CTI at 250K as a function of total anneal time.

energy 0.94 eV. This implies that 90% of the defects would have annealed out if the sample was heated to 150 °C for one hour. According to the theory presented in section 4.2, the maximum CTI is proportional to the trap density. Therefore it is reasonable to assume that if the dominant radiation induced trap is the Si-E centre the CTI should be significantly reduced by heating the CCD to a temperature around 150 °C.

To check the effect of this anneal on the operation of the EEV CCD an irradiated device was heated in a nitrogen atmosphere. After the anneal time the CCD was rapidly cooled down to 250K and the CTI measured. The annealing was repeated at 100°C, 130°C and 150°C until no further reduction in the CTI was observed. The result is shown in Figure 4.16. There is insufficient data here to enable an estimate of the activation energy for the anneal. However, it is clear that heating to 150°C significantly reduces the CTI at 250K.

The anneal was found to increase the dark current to about three times its preanneal value. However, this increase was only observed in the early anneal stages. Further anneal stages showed little additional increase. The anneal performed in Section 3.4 also showed this behaviour.

The CTI versus temperature measurement for another device is given in Figure

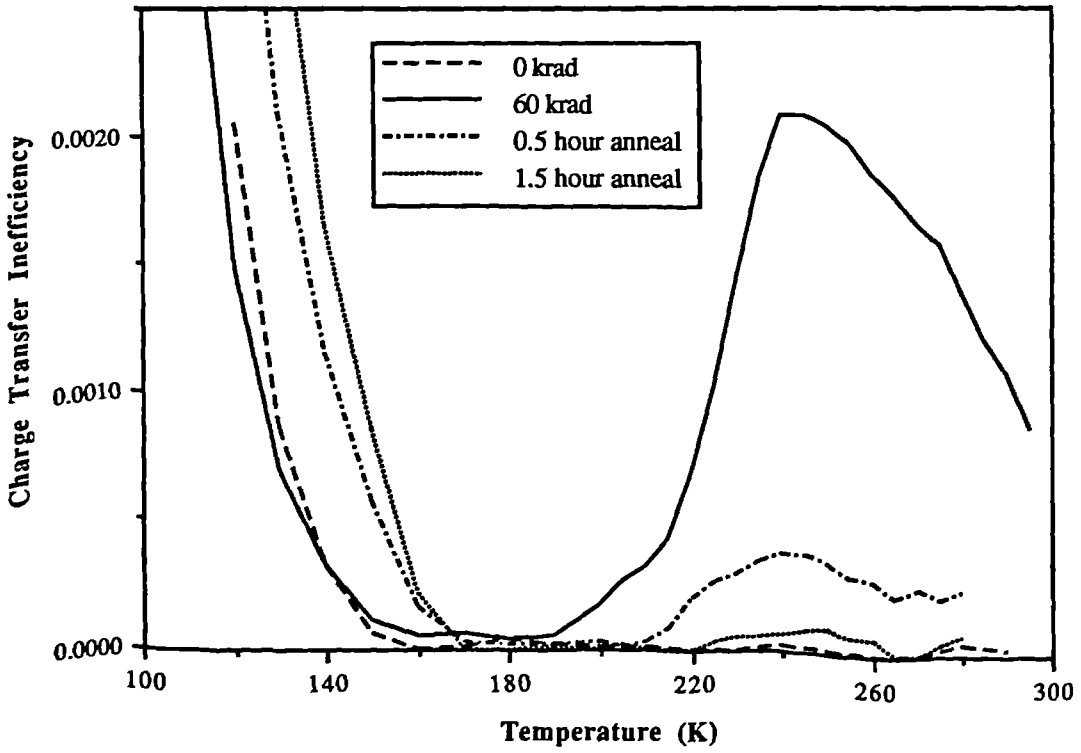

Figure 4.17. The effect of a 160°C anneal.

4.17. The preirradiation curve is presented, along with the curve after 60 krad(Si), the curve after half an hour at 160°C and another taken after a further hour at 160°C. The CTI at 250K does not return to its preirradiation value. This is due to other radiation induced complexes being present with a similar position within the band gap compared with the Si-E centre. However, as the 150°C anneal does not remove this defect, the activation energy for migration of the complex must be higher than the Si-E centre. The main candidate for this defect is the divacancy. This has an activation energy of around 1.3 eV so will require an annealing temperature of approximately 400°C.

It is apparent that, as the irradiation induced peak is being removed, the low temperature "tail" increases. This could be due to the introduction of a trapping centre with a deeper energy level than the trap causing the pre-anneal low temperature "tail". Hirata *et al* [21] suggested that the Si-E centre anneals by the recombination with an oxygen complex. No suggestion for energy levels nor the structure of this new complex was given. Walker and Sah [20] showed that, as the Si-E centre anneals, the density of a defect with an energy level of 0.24 eV below the conduction band edge increases. They attributed the annealing of the Si-E centre to the dissociation of the phosphorus and vacancy. It was assumed that the vacancy went on to combine with another defect, forming a new defect complex. However, there has been little additional evidence for this new complex.

4.5. Summary

The CTI has been measured using the periodic pulse technique for signal sizes as low as 200 electrons. The CTI was found to be a function of temperature, clock timing, signal density and time between signal charge packets. The maximum CTI increases at a rate of around 3.5 10^{-5} per krad(Si) with a signal size of 1000 electrons for Sr^{90} irradiated devices. The main radiation induced defect has been attributed to the Si-E centre with an energy level of 0.47±0.03 eV below the conduction band edge and a capture cross section of 3±1 10^{-15} cm^2. This defect has been shown to anneal out at a temperature of 150°C. However there appears to be a new shallower defect created in its place.

The CTI was found to improve for high signal levels and short times spent under the gates. A method has been found to estimate the effective signal density for small charge packets. The measured signal density was found to be consistent with calculated values. Using the measured signal density, the introduction rate of the Si-E centre was estimated to be 0.020±0.006 cm^{-1}.

4.6. Discussion

4.6.1. A model for CTI degradation

The work described in this chapter has shown that below 250K, where there is no background charge, the change in the CTI with dose, D, from a Sr^{90} source, can be reasonably described by the following relationship;

$$\Delta CTI = \text{Constant} \times \frac{D}{n_s} G(t_o,T) \sum_{i=1}^{g} F_i$$

$$= 7\ 10^8 \frac{D}{n_s} G(t_o,T) \sum_{i=1}^{g} F_i$$

with the dose measured in krad(Si) . Here g is the number of phases, F is the filling factor and G is a function of the mean time between charge packets and the temperature. For a device clocking continuously with a fixed time between signal packets the function G is given by

$$G(t_o,T) = 1\text{-}\exp(-t_o/\tau_{ne}) = 1\text{-}\exp(-42600\ t_o\ T^2 \exp(-5446/T)) \qquad (4.6)$$

where the mean time between charge packets, t_o, is measured in ms. In reality, especially for X-ray astronomical applications, the signal will be distributed throughout the device and integrated before it is read out. If the integration period is long compared with the emission time constant for the radiation induced traps then the traps in pixels not containing signal charge will be empty when readout commences. Therefore the function G for a charge packet will be unity until the charge is moved to a point in the device where charge had been collected during the integration. As the charge packet moves past this point the function G is given by (4.6). The CTI calculated by simply using (4.6) will be an under estimate. The value of G that should be used corresponds to the value of G averaged over all the transfers to the readout register. This depends on the position of the signal packet in the column. The actual value of G will be lower than this as some of the traps assumed empty will still contain charge from previous integrations. G increases for signal packets closer to the readout register as a greater fraction of traps that the signal passes over are empty. Setting G to unity gives a worst case estimate of the CTI.

The filling factor, F, depends on the time the signal spends under a gate, t_g, the temperature, T, and the signal density, n_s, and is given by

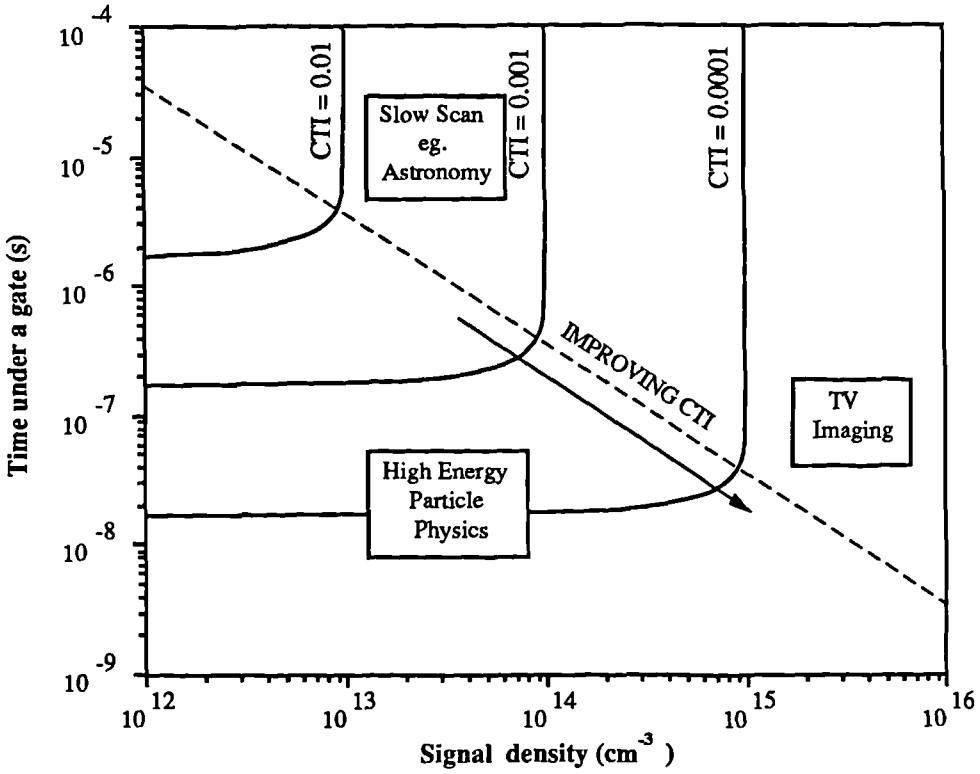

Figure 4.18. A contour plot showing how the time the signal spends under a gate and the signal density effects the maximum CTI at 250K. The device has received 50 krad(Si). Equal phases are assumed. The dashed line is given by $t_g = 2\tau_{nc}$.

$$F = 1\text{-}\exp(-t_g/\tau_{nc}) = 1\text{-}\exp(-3.6\ 10^{-9}\ t_g\ T^{1/2}\ n_s)$$

It is useful to investigate the "filling factor" when $t_g \gg \tau_{nc}$ and when $t_g \ll \tau_{nc}$. The result is

$F = 1$ when $t_g \gg \tau_{nc} = 2.8\ 10^8\ T^{-1/2}\ n_s^{-1}$

$F = t_g\ \sigma_n v_{th} n_s = 3.6\ 10^{-9}\ t_g\ T^{1/2}\ n_s$ when $t_g \ll \tau_{nc}$.

An illustration of the model is given in Figure 4.18 assuming G=1 and that the CCD is a three phase device. Here the effect of changing the signal density and clock timing is clearly illustrated. Typical applications are also shown. For situations where $t_g \ll \tau_{nc}$ (i.e. when the "filling factor" is significantly less than one) the CTI is virtually independent of the signal density.

4.6.1.1. An extension of the model to other types of irradiation

A useful extension to the model would be to include other radiation types and energies. It has been shown that the dominant radiation induced defect responsible for the CTE degradation of CCDs due to proton and neutron irradiation is also the Si-E centre [3,6]. Experimentally it has been shown that there exists a strong correlation between the non-ionising energy loss (NIEL) and the damage factors for different types of irradiation [22]. Therefore, as the defect species produced in CCDs appear constant from one irradiation type to another, it is proposed here that the model for CTE degradation from Sr^{90} irradiation may be extended to include the effects of other irradiations. By replacing the dose with the particle fluence, Φ, and including the NIEL, the model becomes

$$\Delta CTI = \frac{(0.020\pm0.006)\Phi}{n_s} \frac{NIEL}{NIEL_{e^-}} G(t_o,T) \sum_{i=1}^{g} F_i$$

where NIEL and $NIEL_{e^-}$ are the values of the non-ionising energy lost by the irradiating particle and by 1 MeV electrons respectively. The NIEL for 1 MeV electrons is 10^{-5} MeVcm^2/g. The maximum CTI for a three phase device is therefore

$$\Delta CTI = \frac{(0.06\pm0.02)\Phi}{n_s} \frac{NIEL}{10^{-5}\ MeVcm^2/g}.$$

To check the validity of this model, the calculated CTI can be compared with CTI increases measured by other workers. Holland and co-workers have measured the CTI performance of EEV CCDs after exposure to 1.5 and 10 MeV protons [8]. They measured the CTI by monitoring the response to 5.9 keV x-rays from an Fe^{55} source and showed that the CTI increases linearly with fluence. They performed a CTI versus temperature measurement which showed a peak at 200K but no indication of the clock timing, nor the sparseness of the data was given. Their results showed that the CTI at 200K increased by 0.001 after a fluence of ~6 10^8 cm^{-2}, 1.5 MeV protons whereas a fluence of 3.9 10^9 cm^{-2} is required to increase the CTI by the same amount for protons with an energy of 10 MeV. The values of the NIEL for 1.5 MeV and 10 MeV protons are 4 10^{-2} MeVcm^2/g and 7 10^{-3} MeVcm^2/g respectively. The x-rays generated by the Fe^{55} source deposit a signal of around 1650 electrons. As the structure of the CCD tested was the same as the UT101 CCD, the effective signal density was around 8±2 10^{13} cm^{-3}. Therefore a fluence of 6 10^8 cm^{-2}, 1.5 MeV protons gives a CTI increase of 0.002±0.001 from

the model. A fluence of 3.9 10^9 cm^{-2}, 10 MeV protons also gives a calculated CTI increase of 0.002±0.001. The data shows that the NIEL can be used to compare fluences of different energies and the model gives good agreement with the actual CTI values. Considering the difference in the experimental technique, and the assumption that the CTI was at a maximum, the agreement, within a factor two, is very encouraging.

Care must be taken when comparing the model with results taken from devices from other manufacturers. Unless stated, the effective signal density will not be known. Also, due to the possible differences in phosphorus content, the introduction rate of the Si-E centre may be somewhat different to that calculated here. However Saks investigated 15 MeV neutron irradiated CCDs with a similar buried channel to the UT101 CCD [3]. The effective signal density was not stated but the introduction rate for the Si-E centre was given as 7 ± 50% cm^{-1}. The NIEL for 15 MeV neutrons is 5 10^{-3} $MeVcm^2/g$. Therefore, using the model, the introduction rate is calculated to be

$$\frac{\Delta N_t}{\Delta \Phi} = (0.020 \pm 0.006) \frac{NIEL}{NIEL_{e^-}} = 10 \pm 3 \text{ cm}^{-1}.$$

Once again, the agreement of the model with experimental data is excellent.

4.6.1.2. Limitations of the model

The model presented here has been formulated on the assumption that the dominant radiation induced defect is the Si-E centre. If other defects are present in significant numbers the model will have to be modified. However, as mentioned in the previous section, results from other workers have shown that the Si-E centre is dominant for the device structures and range of irradiating particles tested. Also, if large numbers of vacancies produced go on to form other defects, then the introduction rate for the Si-E centre will differ from the value presented here. Therefore the model must be used with care for device structures significantly different from the EEV UT101 CCD.

The model is based on irradiations carried out using betas with a range of energies from a Sr^{90} source. Therefore it may not be realistic to make the simplifying assumption that the betas from the source behave as if they have a mean energy of 1 MeV. The model may also show a greater CTI degradation than that measured, when applied to proton or neutron damage, as it has been shown by Dale *et al* [22] that the damage factors for electron irradiation deviate slightly from the linear

dependence on the NIEL as the damage produced is sparse. This implies that there will be less recombination of the initial damage so there will be a greater rate of stable defect production. However, the comparison of the model with results obtained from other workers are encouraging.

The model assumes that the NIEL, and therefore the displacement damage, is uniform throughout the buried channel. This is a reasonable assumption for 1 MeV electrons. However for protons with energies below approximately 1 MeV, NIEL will not be constant and so a Monte Carlo simulation would be required [23].

The model does not include the effects of background charge on CCD operation. Therefore it's use is limited to situations where dark current is low and that signal is superimposed on an otherwise dark background, such as x-ray spectroscopy. Any background signal will tend to reduce the CTI.

4.6.2. A comparison with other models

It is useful to discuss the similarities and differences between the model for CTE degradation presented here and those from other workers. Only two 'general' models have been published to date and those have been derived from proton damage measurements.

A model presented by Janesick *et al* [7] gave the change in CTI as

$$\Delta CTI = \frac{D_t A_p \Phi \, RTI}{S}$$

where D_t is the total number of displacements calculated by the TRIM-89 Monte Carlo simulation of the displacement cascades, A_p is the pixel area, S is the number of electrons in the signal and RTI is an empirical normalising factor that accounts for vacancy annihilation.

This shows a linear dependence on the particle fluence as in the model presented above but the effect of temperature and clock rate are not modelled. The use of the calculated D_t and RTI factor allows its application to be extended to low energy protons. Theoretical calculation of the peak signal density for a stepped doping profile gives a signal density that is roughly proportional to the signal size and inversely proportional to the gate area. However, measurements from this current work show that a $\sqrt{S}$ dependence is more appropriate for small signals. This will be somewhat device dependent as it depends on the doping density and profile of the buried channel.

Holland *et al* [8], also gave the CTI increasing linearly with proton fluence and device area. Their model can be written as

$$\Delta CTI = \text{Constant} \times \Phi A_p \, NIEL \exp(T/22.1) \, f(\text{clock period}).$$

Here f is an unknown function of the clock period and was inserted as different CTI values were observed for the image and readout sections of their devices. This model is largely an empirical fit to their data and takes no account of signal size, nor of the sparseness of data. The change in CTI with temperature, predicted from this model, can only be valid for their particular situation and, as a general model, must be treated with care.

4.6.3. Methods for reducing the loss of CTE

It is almost an impossible task to attempt to reduce the CTE degradation by reducing the number of trapping centres produced by the incident radiation. Therefore one must concentrate on the task of reducing the effect of these traps on CCD operation. The work performed here has given some indication as to ways to reduce the degradation. The effect of the introduction of an electron trapping level may be reduced by doing three things

i) Select a suitable operating temperature
ii) Increase the effective signal density
iii) Decrease the time a signal spends under a gate.

The optimum operating temperature depends on the expected time between signal packets. In most scientific applications this time may not be well defined. However, operating the device at 180K will reduce the influence of the trapping centre.

It has been found from calculations, that the signal density may be increased by decreasing the pixel area. Holland *et al* [8] have had some reported success with this. They showed that the CTI does in fact scale linearly with pixel area. This is illustrated in their model. A second approach is to confine small signals to the centre of the channel by forming a "notch" or "supplementary buried channel". This is achieved by implanting an additional narrow n-type strip along the centre of the standard buried channel. Holland *et al* showed little improvement with these devices but Janesick *et al* showed that the effect could be significant [24].

The signal density will also increase with increasing dopant density of the buried channel. However, further work is necessary to establish the effect of the dopant

density on the introduction rate of the Si-E centre. Increasing the dopant density of the implant increases the electric field applied across the insulator. Therefore the dopant density is limited by the electric field required for breakdown of the gate insulator which has been found to be above 2 MV/cm [25]. This would occur for a dopant density above 5 10^{16} cm^{-3}.

The signal charge packet can be moved closer to the oxide by increasing the potential applied to the gates. The dopant density increases towards the oxide and so the signal density should increase. In fact, an improvement of around 10% has been achieved by increasing the gate potentials by 2 volts for signal sizes of 1,000 and 10,000 electrons.

The time the signal spends under a gate may be reduced by increasing the readout rate. In some situations this may not be possible due to noise restrictions. In this case, two of the three drive pulses may be reduced, keeping the overall clock period constant. The CTI may then be reduced by as much as a factor 2/3 and a longer sampling time of the output signal would also be possible.

The model for the CTE degradation has shown that the effects of changing the time the signal spends under a gate and the signal density are not independent. Increasing the signal density will have little effect on the CTI if the "filling factor" is significantly less than one. This is evident from the plot given in Figure 4.18. For a future particle physics application, with a readout rate of 20 MHz, there will be little point in trying to increase the signal density. However, for an astronomy application, with a slow readout rate of 40 kHz, a factor ten increase in signal density will give an order of magnitude improvement in the CTI.

The loss of CTE can be substantially recovered by undertaking an anneal at 150°C. An improvement in the CTI has also been observed after a thermal anneal of damage caused by Co^{60} irradiation [6] and by 10 MeV protons [8]. However, the increase of the CTI at low temperatures has not previously been noted. This may be significant when choosing a suitable operating temperature for the device.

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CHAPTER FIVE

The Change in the Noise Characteristics of the Output Circuit

5.1. Introduction

There are four sources of noise that are potentially important for CCD operation. These are

i) shot noise associated with the generation of signal charge,
ii) the generation of dark current,
iii) noise from trapping by bulk states
iv) and noise from the output amplifier.

For low noise applications the CCD is usually cooled to below 200K to reduce the dark current. Due to the low density of bulk states in modern CCDs the noise is then dominated i) and iv). Low noise operation is particularly important for x-ray astronomy where the limit to attainable energy resolution is determined by the statistical fluctuations in the size of the collected charge packets. An electron hole pair is liberated for each 3.6 eV of x-ray photon energy. If a monoenergetic x-ray photon has an energy E then the variance in the number of measured electrons in the signal is given by

$$N^2 = n^2 + FE / 3.6$$

where n is the noise in electrons associated with the CCD output and F is the Fano factor (~0.115). Even for output noise of only 10 electrons r.m.s. the output noise will dominate the energy resolution for x-ray energies of less than 3 keV.

As the device is irradiated the noise characteristics of the output amplifier will change. Along with this change there will be an increase in the bulk trapping states that degrade the charge transfer efficiency. The shot noise fluctuations in the charge lost from the signal will also become important. However, this chapter is concerned with the noise associated with the output amplifier.

There has been very little work undertaken on the radiation hardness of the output circuitry. However most reports on the radiation damage of CCDs show no significant increase in the output noise. Holland *et al* gave no significant increase up to a proton fluence of 10^{10} cm^{-1} [1] and Hopkinson noted no increase up to the highest dose tested of 20 krad(Si) from Co^{60} [2]. At first sight this is somewhat surprising as it is known that ionising radiation increases the surface state density and oxide trapped charge. These parameters are often linked to the noise performance of MOSFETs. It was the purpose of the work described in this chapter to investigate the noise performance of the UT101 CCD's output circuit and to establish if there are situations when the noise performance will deteriorate with irradiation.

5.2. Output Amplifier Noise

A schematic of the output amplifier of the UT101 CCD is shown in Figure 5.1. This output stage is common to many other CCDs. The load can either be a resistor or a constant current source. Experience has shown that for low noise operation a resistor is preferred as constant current sources give higher noise levels.

The operation of the output circuit is described in Section 1.1.5. The description is repeated here for clarity. Before charge is transferred from the readout register to the capacitance (the output node) at the gate of the output FET, the capacitance is charged to a potential set by V_{rd} by turning the reset FET "on". The reset FET is then turned "off". Charge can now be clocked onto the output node thus partially discharging the capacitance which causes the potential on it to drop. This change in potential is proportional to the charge transferred from the CCD. The output MOSFET buffers this signal to drive the following circuitry.

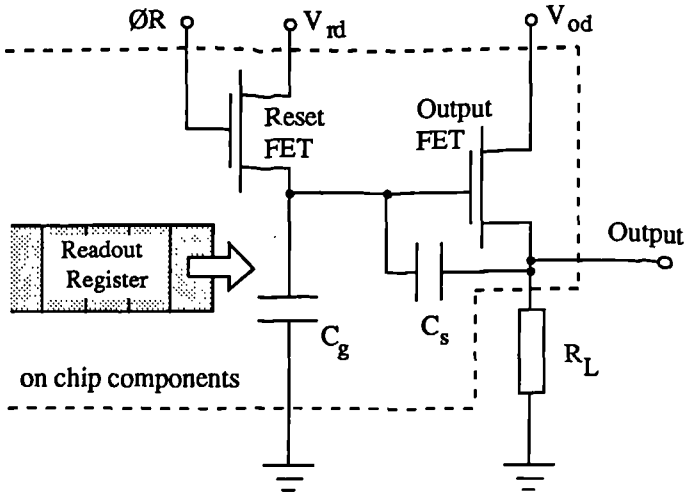

Figure 5.1. A schematic of the output stage of the UT101 CCD. C_s is the gate-source capacitance and C_g is the sum of all other capacitances from the gate to ground.

Johnson noise in the channel of the reset transistor will give rise to fluctuations in the potential to which the output node is reset. This is known as reset noise. The noise from this source in equivalent electrons r.m.s. is given by

$$N_{reset} = (kTC_n)^{1/2}/q.$$

where k is the Boltzmann's constant, T is the absolute temperature, C_n is the effective output node capacitance (~0.15 pF) and q is the electronic charge. N_{reset} is in the order of 150 electrons at room temperature and must be removed for low level imaging. This noise can be eliminated by using the technique of correlated double sampling (CDS). A CDS system involves sampling the output after the reset pulse and then with the signal present. The difference between the two

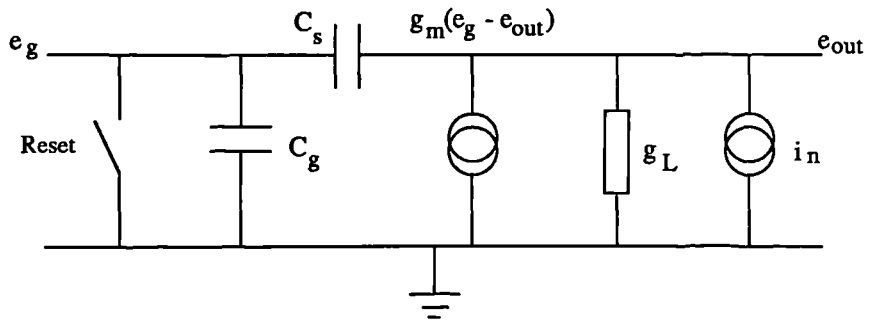

Figure 5.2. The small signal equivalent circuit of the output stage shown in Figure 5.1.

samples is taken and the reset noise is eliminated as it is common to both samples.

The small signal equivalent circuit is shown in Figure 5.2. The gate and the output voltages are given by e_g and e_{out} respectively. The output is taken when the reset FET is "off" and so the switch in the equivalent circuit can be regarded as being open. The effective capacitance, C_n, at the gate of the MOSFET is given by Miller's theorem as

$$C_n = C_g + C_s(1 - A) \tag{5.1}$$

Where A is the voltage gain of the amplifier, C_s is the gate to source capacitance and C_g is the sum of all the other capacitances from the gate to ground. In the case of the source follower the gain is given by

$$A = \frac{g_m}{g_m + g_L}.$$

where g_L is the sum of the source-drain conductance and the load conductance and g_m is the transconductance of the FET. It is assumed throughout this work that the substrate to source transconductance is very much less than the gate to source conductance. The effective gate capacitance is in the order of 0.15 pF and the channel resistance of the reset FET in the "off" state is greater than $10^{12}\ \Omega$. Therefore the noise from the reset FET, when in the "off" state, will be bandwidth limited by the bandwidth determined by this RC time constant. This limit is below 1 Hz is ignored in the following sections as CDS also significantly reduces this source of noise.

Further noise in the output circuit comes from the output MOSFET and additional load components. This noise will be dominated by thermally generated Johnson noise which has a flat or white frequency characteristic and the ubiquitous flicker or "1/f" noise which is the generic term for noise with a $1/f^{\gamma}$ shaped noise power spectra where γ is not necessarily equal to one. Both these sources create fluctuations in the drain current that can be referred back to the gate as fluctuations in the number of electrons on the output node. Assuming these noise sources are uncorrelated, the total noise current, i_n, is given by

$$i_n^2 = i_j^2 + i_f^2$$

where i_j is the Johnson noise source and i_f is the "1/f" noise source. If a signal, e_{out}, appears at the source, the equivalent charge at the gate is given by

$$q = C_n\, e_{out} / A = (C_g + C_s(1 - A))\, e_{out} / A. \tag{5.2}$$

If a noise source, i_n, is present then we have,

$$i_n = g_L e_{out} + g_m(e_{out} - e_g) \tag{5.3}$$

C_g and C_s form a potential divider giving

$$e_g = e_{out}\, C_s / (C_g + C_s). \tag{5.4}$$

Combining (5.3) and (5.4) and substituting into (5.2) gives the noise in terms of equivalent r.m.s. fluctuations in the charge at the gate of the output FET as

$$q_n = (i_n / g_m)(C_g + C_s) \tag{5.5}.$$

Therefore the noise charge is proportional to the total capacitance connected to the gate of the output FET. This result is also derived in [3].

5.2.1. Thermal (Johnson) Noise

Thermal noise arises from the velocity fluctuations of the charge carriers in a resistive material. The thermal noise can be thought of as the mechanism by which the state of thermal equilibrium is maintained. A random departure from this state of equilibrium is followed, on average, by a relaxation back towards it. These fluctuations give rise to a fluctuation in the current flowing through the device and hence adds a source of noise. This thermal noise is often referred to as Johnson noise. The Johnson noise from the load resistor per unit bandwidth is given by

$$i^2_{load} = 4kT/R_L$$

and the noise from the MOSFET per unit bandwidth can be expressed as

$$i^2_{FET} = 4kT\alpha g_m$$

where α can range between 2/3 and 10 in practical situations depending on the gate and drain voltages, oxide capacitance, and substrate doping. According to Klaassen and Prins [4], the value of α for a surface channel MOSFET with a substrate dopant density of less than $5\ 10^{16}$ cm^{-3} is given by

$$\alpha = \frac{(V_g - V_T)^2 - V_d(V_g - V_T) + \frac{1}{3}V_d^2}{(V_g - V_T)V_d - \frac{1}{2}V_d^2} \tag{5.6}$$

where V_g is the applied gate potential, V_T is the threshold voltage and V_d is the drain voltage. For a MOSFET operating in saturation $(V_g - V_T) \approx V_d$ and the well known result is obtained that $\alpha \approx 2/3$. From first order theory we have

$$g_m = \beta V_d \quad \text{and} \quad g_{ds} = \beta ((V_g - V_T) - V_d).$$

where g_{ds} is the mutual conductance of the MOSFET and β is the transistor gain factor. Substituting into equation (5.6) gives

$$\alpha \approx \frac{g_{ds}^2 + g_m g_{ds} + \frac{1}{3} g_m^2}{g_m g_{ds} + \frac{1}{2} g_m^2} \qquad (5.7).$$

The total thermal noise per unit bandwidth is given by

$$i_j^2 = i_{load}^2 + i_{FET}^2 = 4kT(1/R_L + \alpha g_m) \qquad (5.8).$$

This noise source will vary as the device is irradiated as g_m and g_{ds} are dependent on the operation point of the FET and so are sensitive to the threshold voltage shifts.

5.2.2. Flicker ("1/f") Noise

The flicker noise will also increase with irradiation and will dominate the noise at low frequencies. To date there has been little work on the effect of radiation on the noise performance of MOSFETs and even less on depletion mode devices running in buried channel mode. Much of the research that has been undertaken on flicker noise of surface channel MOSFETs has been concerned with using the noise measurement as a non destructive way of determining the radiation hardness of the device. The "1/f" noise is high for low quality oxides. These oxides will have a greater density of hole traps so the radiation hardness will be poor. Scofield *et al* [5,6,7] established a strong correlation between preirradiation noise in surface channel devices and their post irradiation trapped charge but no such correlation was observed between the 1/f noise and the increase the charge trapped in interface states. It as been found by Meisenheimer *et al* [8,9] that the "1/f" noise increases with irradiation and the increase is also dependent on the oxide trapped charge but not on the interface state density. This work was carried out on surface channel devices, ie. the conducting channel was at the Si/SiO_2 interface.

The output FET of the UT101 CCD can be run in either surface or buried channel mode depending on the biases applied. In buried channel operation, the current carrying channel runs away from the interface, within the bulk silicon. In the work

described in this chapter it will be established that the 1/f noise of the output FET does in fact increase with irradiation but the increase is dependent on the mode of operation of the FET.

The phenomenon of "1/f" noise in MOSFETs is still not fully understood despite persistent study for more than three decades. In essence, theories can be put into three main groups.

i) Theories based on the number fluctuation model of A. L. McWhorter [10]. Here noise is assumed to originate from the random trapping and emission of charge carriers. These trapping centres can be within the semiconductor bulk, within the insulator or at the silicon-insulator interface. The relevance of each contribution will depend on the mode of operation, the trap densities and the temperature.

ii) Theories based on mobility fluctuations. This is described by the Hooge empirical relation [11]. A quantum mechanical approach to the problem has been taken by Handel where mobility fluctuations are treated as stemming from fundamental sources such as carrier scattering and Bremsstrahlung [12].

iii) Theories attempting to combine the number and mobility fluctuation models. Clearly there will be a contribution to the noise from both sources. However work by Reimbold has shown [13] that carrier fluctuation appears to dominate the "1/f" noise in MOSFETs. Meisenheimer *et al* [8] showed that the number fluctuation theory fitted their experimental data well. Therefore, only number fluctuation theories are considered here.

5.2.2.1. The power spectra for the trapping process

Consider a trapping centre within a semiconductor. This trap can either contain an electron or be empty. If the mean time the trap is in a filled state is τ and the mean time the trap is in an empty state is σ then the probability of being at any time in a filled state is given by

$$P_1 = \tau/(\tau+\sigma).$$

The probability of being in an empty state is

$$P_0 = \sigma/(\tau+\sigma).$$

As the trap can only be in either a filled or empty state, the process of trapping is described using binomial statistics. Therefore, if there are N traps, the mean squared fluctuation in the number of traps that are filled is given by

$$\langle \delta N^2 \rangle = NP_1P_0 = NP_1(1-P_1).$$

The function $P_1(1\text{-}P_1)$ is a sharply peaked function implying that the noise will be a maximum when $\tau = \sigma$. This is illustrated in Figure 5.3 which shows the dependence of $P_1(1\text{-}P_1)$ on τ/σ.

Assuming that, after a deviation from equilibrium, the number of filled traps returns to the equilibrium number, NP_1, exponentially with a time constant τ_0, then this can be regarded as being a relaxation process. Therefore, the autocorrelation function for the fluctuation is given by [14]

$$\phi(\Delta t) = \langle \delta N^2 \rangle \exp\left(-\frac{|\Delta t|}{\tau_0}\right).$$

The power spectral density for the process is given by the Wiener-Khintchine theorem as the Fourier transform of the autocorrelation function. Therefore the power spectra is

$$S(\omega) = 4\int_0^{\infty} \phi(\Delta t)\cos(\omega\Delta t)\,d(\Delta t) = \frac{4\phi(0)\tau_0}{1+\omega^2\tau_0^2}$$

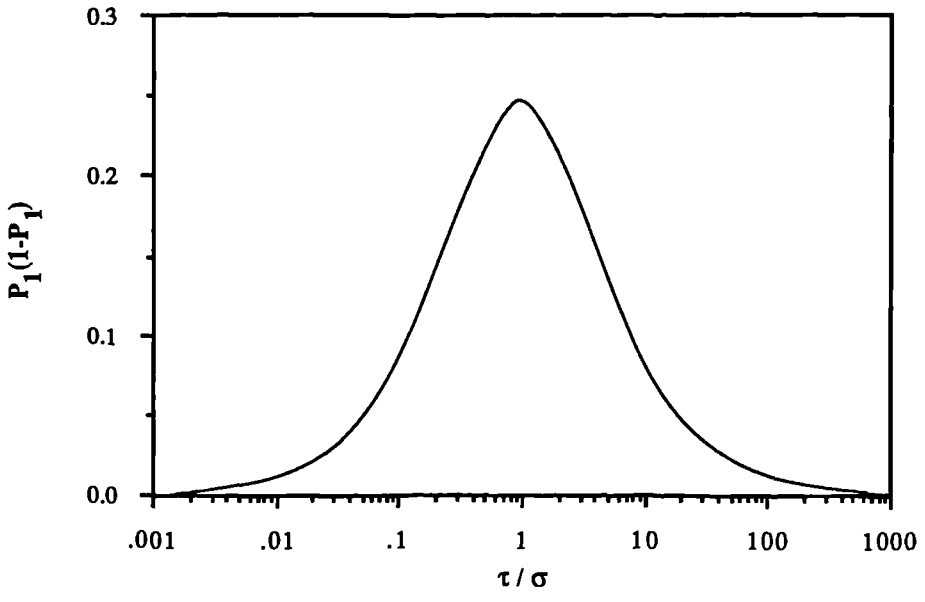

Figure 5.3. The factor P_1 (1 - P_1) as a function of τ/σ.

$$= \frac{4\langle \delta N^2 \rangle \tau_0}{1+\omega^2\tau_0^2}$$

This implies that the noise from a source that has a single characteristic time constant has a Lorentzian shaped spectra, being flat at low frequencies and falling off as $1/f^2$ at higher frequencies. This cannot describe the noise from surface channel MOSFETs as this generally has a 1/f shaped power spectrum. However, the following section will show that the 1/f spectrum can be obtained if there is a wide dispersion in the characteristic time constants.

5.2.2.2. Surface Channel MOSFETs in Inversion

A real surface n-channel MOSFET below saturation, in strong inversion mode can now be considered. The term surface channel implies that the conducting channel is at the Si/SiO_2 interface. To describe the noise processes it is necessary to separate the effect of traps at the Si/SiO_2 interface that can readily exchange charge with the bulk silicon (known as interface states or traps) and those traps within the oxide (known as oxide traps). An electron can be removed from the conduction band of the silicon by trapping at the interface or within the oxide by the tunnelling mechanism.

First consider trapping at the interface. The traps will be distributed in energy through the band gap of the silicon and can act as generation/recombination centres or as trapping centres. The trap is said to be filled if it contains an electron and empty if it does not. The mean capture and emission times can be calculated using Shockley-Reed-Hall (SRH) statistics and have been given in Section 4.2. The mean rate for the empty to filled transition is given by

$$\frac{1}{\sigma} = \frac{1}{\tau_{nc}} + \frac{1}{\tau_{pe}}$$

where τ_{nc} and τ_{pe} are the electron capture and hole emission time constants. The mean rate for the filled to empty transition is

$$\frac{1}{\tau} = \frac{1}{\tau_{pc}} + \frac{1}{\tau_{ne}}$$

where τ_{pc} and τ_{ne} are the hole capture and electron emission time constants respectively. Therefore the mean rate for the process is given by

$$\frac{1}{\tau_0} = \frac{1}{\tau} + \frac{1}{\sigma} = \frac{1}{\tau_{nc}} + \frac{1}{\tau_{pe}} + \frac{1}{\tau_{ne}} + \frac{1}{\tau_{pc}} \qquad (5.9).$$

According to Sah [15], $\langle \delta N^2 \rangle = N_t f(1-f)$ where N_t is the trap density at an energy E and f is the Fermi occupation factor and is a sharply peaked function around the equilibrium pseudo Fermi level at the interface. Therefore only traps around the pseudo Fermi level need be considered. At inversion this lies within the upper half of the band gap. Therefore $\tau_{ne} \ll \tau_{pe}$, $\tau_{pc} \gg \tau_{nc}$ and $\tau_{nc} \approx \tau_{ne}$ for traps at the pseudo Fermi level. This implies that $\tau_0 \approx \tau_{nc}/2 \approx 5$ ns for a minority carrier density of 10^{16} cm^{-3} at the interface. This characteristic time is very short and so does not account for the "1/f" noise below 200 MHz. Therefore traps that give a longer characteristic time must be responsible for the observed noise. These traps must lie within the oxide itself and the generally accepted picture is that communication is via the tunnelling process. The traps within the oxide are filled by the tunnelling of electrons from the conducting channel. The traps will be emptied by the tunnelling of a hole. Most models assume that the characteristic time for the tunnelling process is of the form

$$\tau_o = \alpha \exp(2Ky) \tag{5.10}$$

where y is the distance into the oxide and K is related to the barrier height. This is in the order of 10^8 cm^{-1}. The constant α is related to the attempt frequency at the potential barrier and to the capture cross section of the trap and is in the order of 10^{-10} s. This shows that the characteristic times can range from less than 100 ps to many thousands of seconds, depending on the position of the trap within the oxide. A characteristic time greater than 10^3 s is obtained for a trap lying further than 1.5 nm from the Si/SiO_2 interface. This implies that traps that are responsible for the observed noise must lie within a few angstroms of the interface.

If it is assumed that the occupation of traps within the oxide is given by the Fermi

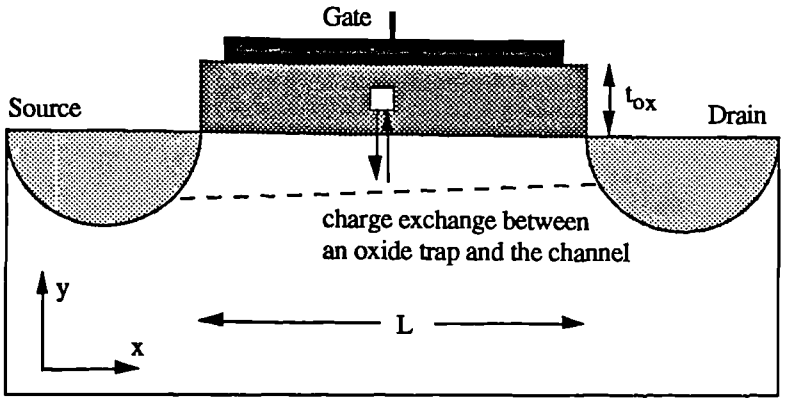

Figure 5.4. A schematic of a surface channel MOSFET.

factor of the pseudo Fermi level at the interface, then $\langle \delta N^2 \rangle$ can be replaced by $N_t f(1-f)$ as for trapping by interface states. It can be seen, once again, that only traps with an energy around the pseudo Fermi level contribute significantly to the noise.

The effect that the charge fluctuations have on the noise characteristics of surface channel MOSFETs has been the subject of many investigations (eg. [16,17,18,19]). However, a simple derivation of the gate referred noise voltage is given here to illustrate the effect of the wide range of possible of time constants.

Consider a simple enhancement mode MOSFET shown in Figure 5.4. Noise will be generated by the capture and emission of charge from the element $W\delta x\delta y$. If $N_t(E,y)$ is density of traps per unit volume per eV within the oxide at (x,y) then the power spectra for the number fluctuation in the channel is

$$S_{\delta N}(\omega) = \frac{4N_t(E,y)f(1-f)\tau_0}{1+\omega^2\tau_0^2} W\delta E\delta x\delta y$$

The traps that are important are situated near the Si/SiO_2 interface at a distance into the oxide that is very much less than the oxide thickness. Therefore a fluctuation in the number of trapped charge gives a fluctuation in the effective gate voltage of

$$\delta V_g = \frac{q\delta N}{LWC_o}$$

where L and W are the channel length and width respectively and C_o is the capacitance per unit area of the oxide. Thus the power spectra for the noise referred to the gate of the MOSFET is given by

$$S_{\delta V}(\omega) = \frac{q^2 S_{\delta N}(\omega)}{(LWC_0)^2} = \frac{4q^2 N_t(E,y)f(E,x)(1-f(E,x))\tau_0(x,y)}{WL^2C_0^2(1+\omega^2\tau_0^2(x,y))}\delta E\,\delta x\,\delta y$$

This has to be integrated over all the traps within the oxide. If it is assumed that the Fermi level is constant along the length of the channel, ie. well below saturation, and the trap density is uniform through the oxide then the total gate referred power spectrum is given by

$$S_V(\omega) = \frac{4q^2kTN_t(E_f)}{WLC_0^2}\int_{y=0}^{t_{ox}} \frac{\tau_0(y)}{(1+\omega^2\tau_0^2(y))}\delta y$$

where $N_t(E_f)$ is the oxide trap density around the pseudo Fermi level at the interface. The time constant, τ_0, increases with distance into the oxide and is given by equation (5.10). It ranges from approximately zero to infinity. Therefore, by changing variable, the power spectra is

$$S_V(\omega) = \frac{2q^2kTN_t(E_f)}{KWLC_0^2} \int_{\tau_0=0}^{\infty} \frac{1}{(1+\omega^2\tau_0^2)} \delta\tau_0 = \frac{q^2kTN_t(E_f)}{2KWLC_0^2 f}$$

This is the power spectra often quoted for "1/f" noise of MOSFETs and shows that the noise is independent of the gate and drain voltage and varies inversely with frequency due to the wide dispersion of the characteristic time constants. The variation of the noise with temperature is dependent on the energy distribution of the traps. If the trap density is not dependent on E the noise will show a linear temperature dependence. If N_t varies throughout the band gap, then this will be reflected in the temperature dependence of the noise. This arises as the Fermi level moves towards the conduction band for a fixed gate and drain voltage as the temperature is reduced.

This model assumes that the traps are uniformly distributed through the oxide. If the trap density decreases away from the Si-SiO_2 interface the noise will have a "1/f$^\gamma$" shaped spectrum where γ is less than 1.

It has been noted by Fu and Sah [17] that direct tunnelling into and out of traps within the oxide requires the energy lost by an electron to be up to half the silicon band gap energy. They stated that this was greater than could be accounted for by any known mechanism. Therefore an intermediate state was essential. The direct tunnelling model was modified to include communication via interface states. In their model, the carriers in the conduction and valence bands communicate with the fast surface states located at the interface through the SRH processes. The carriers then tunnel into or out of the oxide traps located at some distance away from the interface elastically. However, the results were essentially the same as those presented above and they showed that the noise was effectively independent of interface state density at strong inversion.

5.2.2.3. Buried channel devices

If an n-type layer is implanted at the Si/SiO_2 interface then the surface of the device can be depleted whilst still maintaining a current carrying channel within the bulk of the silicon device. Thus interaction with traps within the oxide is reduced. This is

known as a buried channel mode of operation. The output FET of the UT101 CCD has the potential to run in buried channel mode.

By investigating random telegraph signal (RTS) currents in many MOSFETs, Kandiah *et al* [20,21] have established that there are two time constants, one for tunnelling into the trap and the other for tunnelling out of the trap. These are given by

$$\tau_{in} = \exp(2K_e y)/4nv_{nth}\sigma_n \quad \text{and} \quad \tau_{out} = \exp(2K_h y)/4pv_{hth}\sigma_h.$$

Here n and p are the electron and hole densities averaged over a Debye length of the Si-SiO_2 interface. The characteristic time constant is obtained from

$$\frac{1}{\tau_0} = \frac{1}{\tau_{in}} + \frac{1}{\tau_{out}}.$$

The use of this is complicated if the desired result is an analytical solution for the power spectrum as a function of various biases or as a function of temperature. For a depletion mode device running with the conducting channel at the SiO-SiO_2 interface, the gate referred noise characteristics will be somewhat as previously described ie. independent of drain voltage and with a 1/f shaped spectrum. However it can be seen that, as the carrier concentration at the interface is reduced, the characteristic time for the tunnelling processes will increase significantly. If a depletion mode device is operated with the conducting channel running in the bulk of the silicon the density of charge carriers will be low at the interface and the characteristic times will be very long. Therefore there will be little "1/f" noise generated by traps within the oxide.

If the interface is depleted the noise will be dominated by emission from the interface states. The emission time for electrons will equal the emission time for holes for interface states at mid band. Therefore alternate emission of electrons and holes from the interface states around mid band will mainly determine the noise characteristics of the depletion MOSFET running in buried channel mode. If we assume that the electron and hole emission times are equal then we have a single time constant governing the noise process. Therefore the trapping noise will be of the form

$$S_v(\omega) = \frac{F\tau_0}{(\omega\tau_0)^2 + 1}.$$

Here F will be a function of device area and the interface trap density at mid band etc. Kandiah *et al* have found the function F to be given by

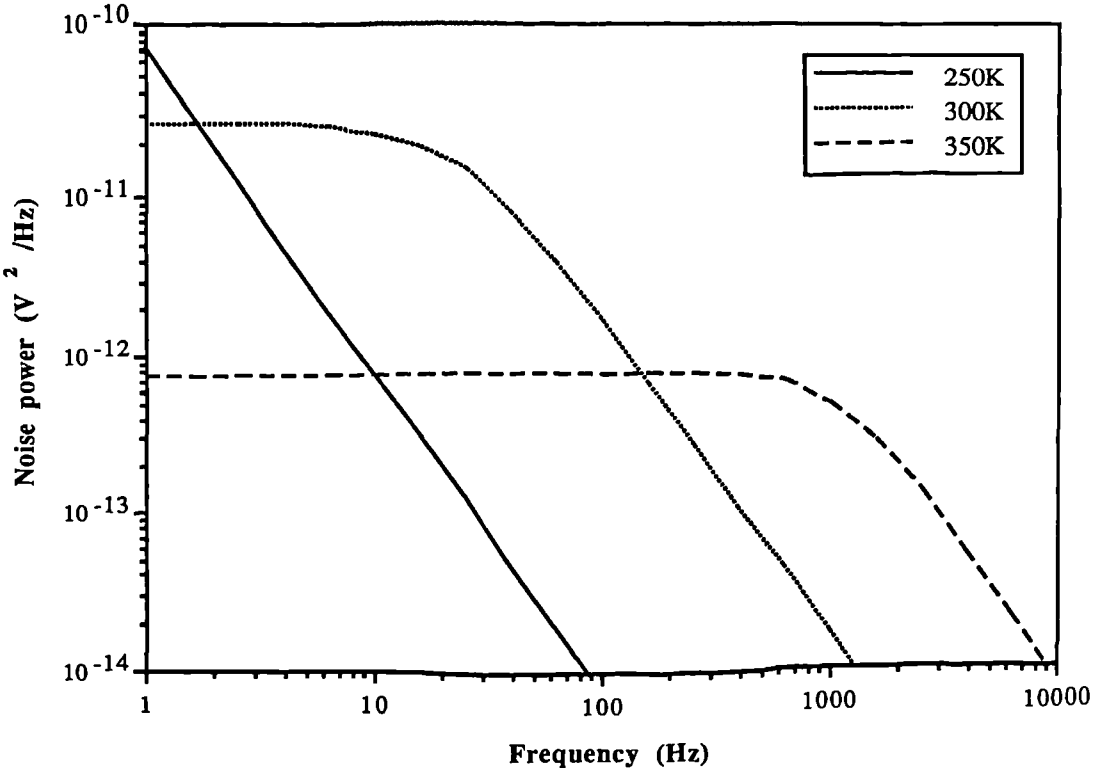

Figure 5.5. The calculated noise power from the interface states as a function of frequency assuming the interface is depleted. The device area is 64μm by 5μm, insulator capacitance is 29 $nFcm^{-2}$ and the interface trap density is 3.10^{10} $cm^{-2}eV^{-1}$.

$$F = \frac{4N_{ss}kTq^2}{3WLC_0^2}.$$

where N_{ss} is the density of interface states at mid gap. τ_0 will be given by

$$\tau_0 = \frac{\exp(E_g/2kT)}{N_v v_{pth}\sigma_h + N_c v_{nth}\sigma_n}.$$

This noise has a Lorentzian shaped spectra, being flat at low frequencies and falling off as $1/f^2$ at higher frequencies. The results for the calculated noise power spectra are shown in Figures 5.5. The device parameters used are those of the UT101 on-chip MOSFET with a reasonable choice of interface state density. The cross sections were set equal to 10^{-15} cm^2. The dependence on temperature of the gate referred noise voltage density at various frequencies is given in Figure 5.6. The temperature for the highest noise at any fixed frequency is dependent only on the band gap of Si. Therefore the noise peaks occur at the same position in all depletion mode MOSFETs.

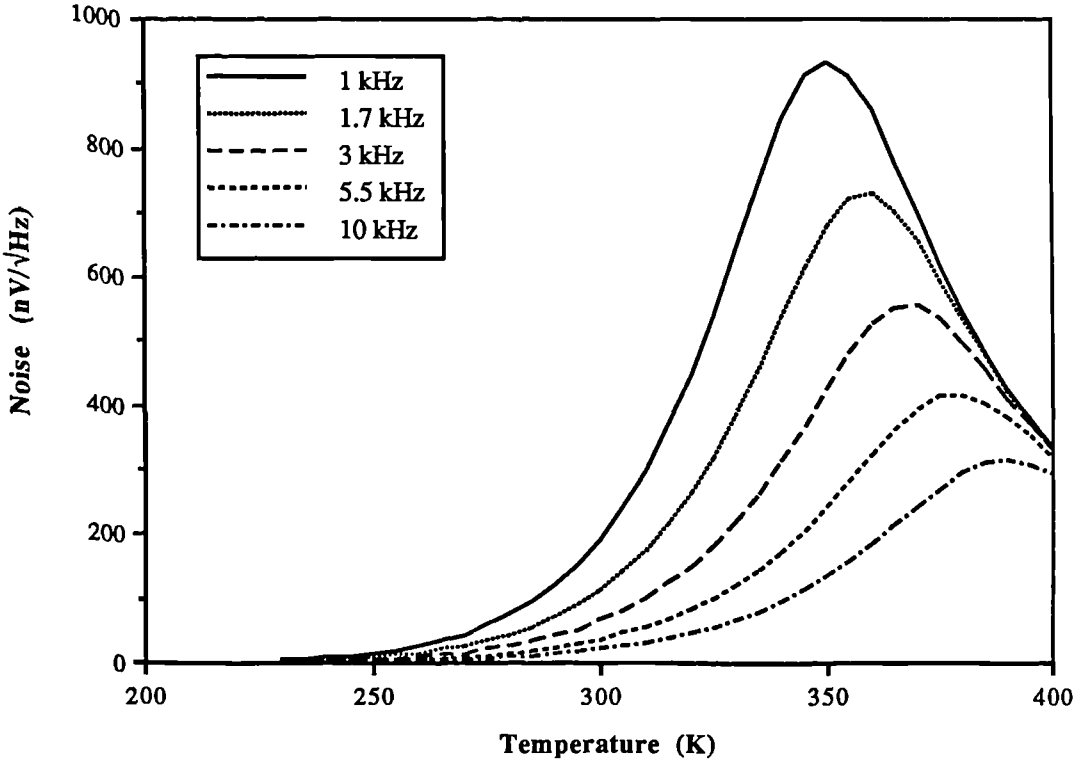

Figure 5.6. The calculated gate referred noise from the interface states as a function of temperature assuming the interface is depleted. The device parameters are as in Figure 5.5.

Bulk traps within the silicon will also give a Lorentzian shaped noise power spectra. These have been treated by Kandiah and also by Murray *et al* [22]. It is only those traps in, or adjacent to the channel, or at the Si-SiO_2 interface that contribute significantly to the noise. Those near the drain will contribute the most. The capture and emission time for an electron trap will be given by τ_{nc} and τ_{ne} respectively. The maximum noise will occur when $\tau_{nc} = \tau_{ne}$. τ_{nc} is dependent on the local carrier density and so is a function of the position of the trap within the channel. τ_{ne} is a strong function of temperature. As the temperature is varied, noise peaks will appear due to individual traps. The peaks will appear at a temperature that is dependent on the energy of the trap below the conduction band edge.

5.3. The noise measurement of the output FET

In order to make measurements in all parts of its characteristics, the output of the CCD was set up as in Figure 5.7. The reset FET was left in the "on" state to prevent charge build up at the gate of the output FET. The effective channel resistance of the reset FET in the "on" state is around 10^4 Ω. The implications of

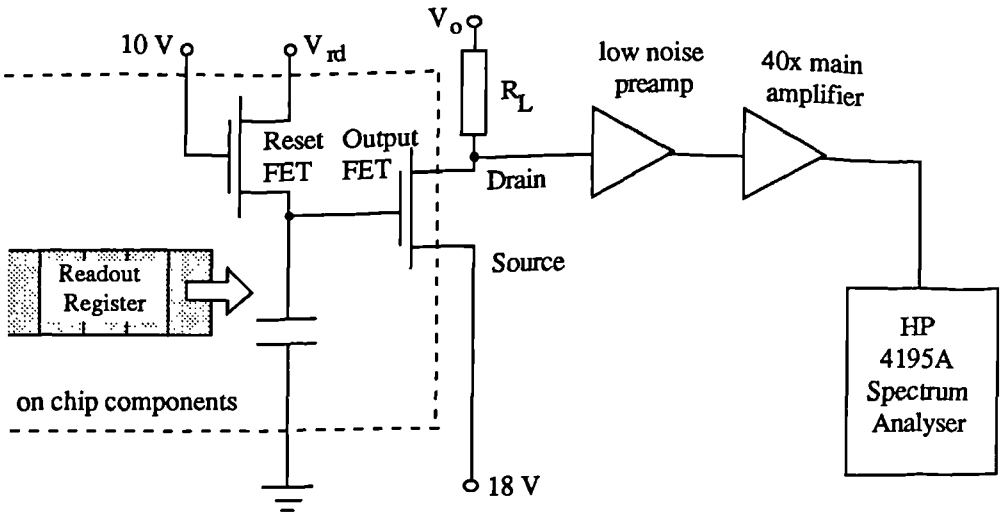

Figure 5.7. The output configuration employed for noise measurements.

this are that the noise from the reset FET will no longer be bandwidth limited to 1 Hz as in the "off" state. The Johnson noise of the reset FET multiplied by the gain will appear at the output up to 100 MHz. This will only be important at high frequencies where the "1/f" noise from the output FET is not dominant. Therefore the following measurements are restricted to low frequencies. There will be little "1/f" noise from the reset FET at the output as the drain voltage is approximately equal to the source voltage.

To ensure the 'punch through' condition (Section 1.1.3) was satisfied for the rest of the CCD, as in actual device operation, V_{rd} has to be greater than 10V. So that a significant range of gate/source voltages can be applied to the output FET, the source was set to 18V giving a source substrate voltage of 18V. This value of source substrate voltage is around the value for the output set up as a source follower in the buried channel mode of operation. This remained fixed throughout the experiment. The substrate had to be held at a potential less than V_{rd} so that the output node of the CCD remained reverse biased. The gate voltage of the output FET could be controlled by varying V_{rd}.

The output FET characteristics were obtained by varying V_{rd} and V_o. The drain current was measured by monitoring the voltage drop across the load resistor. To measure the gain of the system 10mV pulses were applied to the V_{rd} line via a coupling capacitor and the output observed using a digital oscilloscope. Any noise measurements taken were referred back to the gate of the output FET by dividing by the measured gain. The noise voltage was measured between 1 kHz and 10 kHz,

the limits being set by the bandwidth of the preamplifier and by white noise sources. Each noise measurement was averaged over 400 readings which took approximately 15 minutes. The noise of the external components was measured to be less than 10 nV/$\sqrt{Hz}$ in this range. This is very much less than the measured output noise from the channel of the FET for drain-source voltages greater than 1 Volt. The preamplifier used for the noise measurements was a.c. coupled with an input impedance of 100 kΩ.

The effective output node capacitance, C_n, was measured with the CCD in standard configuration (Figure 5.1) using the method described in Section 4.4.2. For this measurement an a.c. coupled, transimpedence preamplifier was employed. This has effectively a zero input impedance for a.c. signals. Therefore the load conductance of the source follower tends to infinity and the gain of the source follower tends to zero. From equation (5.1) it can be seen that C_n will thus tend to $C_g + C_s$.

The irradiations were carried out using a Sr^{90} beta source at a rate of 1 krad/hour. During irradiation the device was at room temperature, with all connections grounded. The noise was measured in all parts of its characteristics before and after irradiation.

5.4. Experimental results

The characteristic curves before and after irradiation are shown in Figures 5.8. The change in characteristics after 150krad(Si) can be attributed to a flat band voltage shift of 2V (Figure 5.9). This is consistent with other measurements on the flat band voltage shifts.

Typical results for the gate referred noise, measured using the spectrum analyser, are given in Figure 5.10. Both spectra were taken at room temperature with V_{ds} of 4 Volts. For surface channel operation V_{gs} was 0 Volts and for buried channel operation V_{gs} was -6 Volts. These clearly show the difference between the noise power spectra taken with the output FET biased so the conducting channel is at the Si/O_2 interface and the spectra taken with the conducting channel lying within the bulk silicon. The noise obtained in surface mode is significantly higher than in buried mode in the observed frequency range. It is also clear that the noise has a greater dependence on frequency with the conducting channel away from the interface.

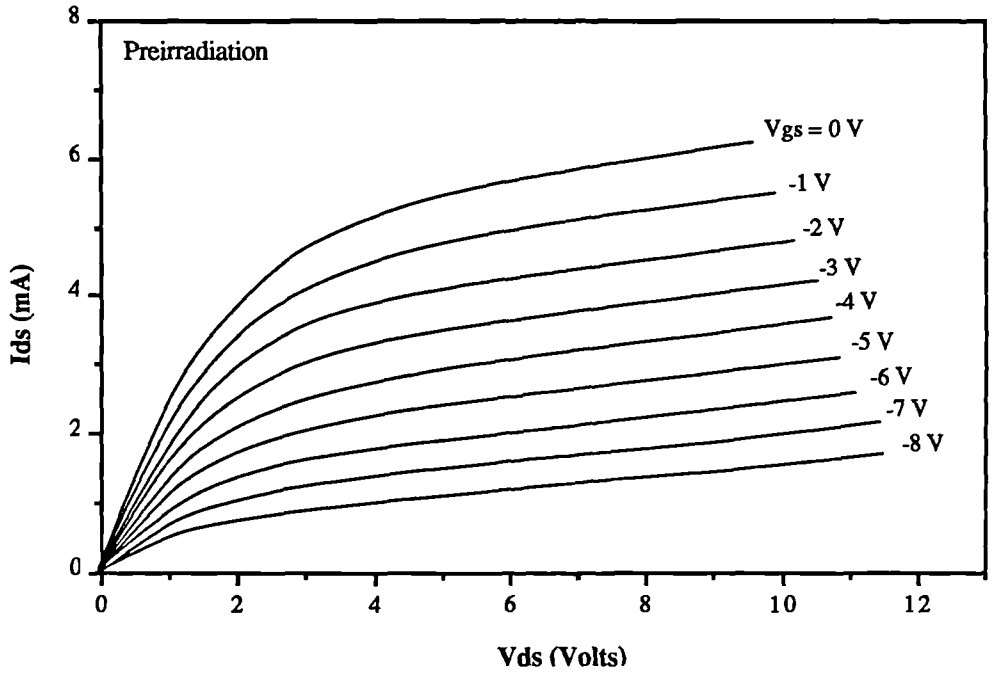

Figure 5.8(a). The characteristics of the output FET before irradiation.

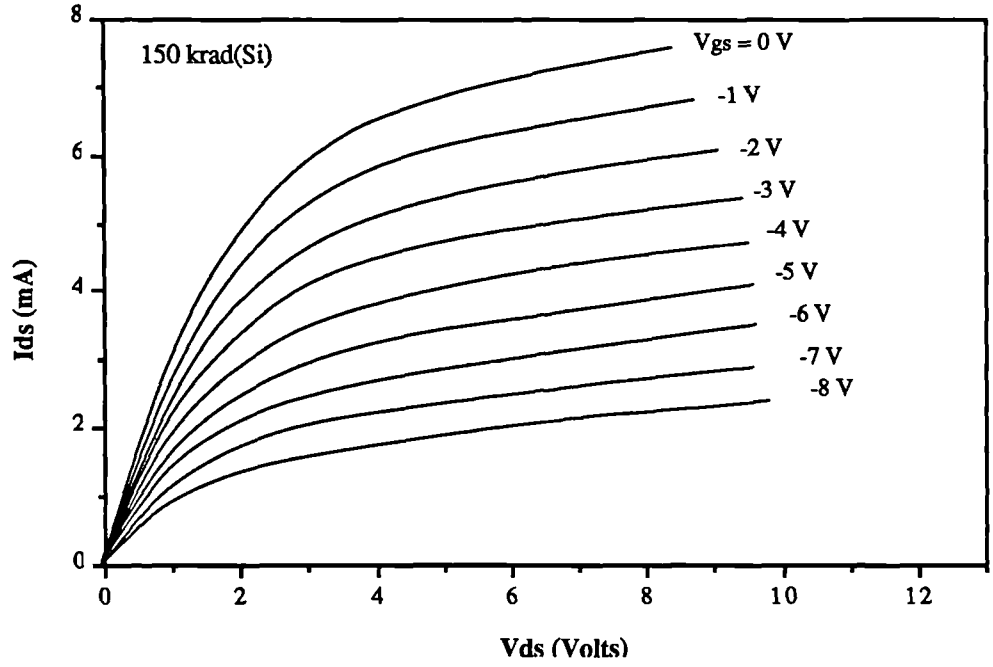

Figure 5.8(b). The characteristics of the output FET after 150 krad(Si).

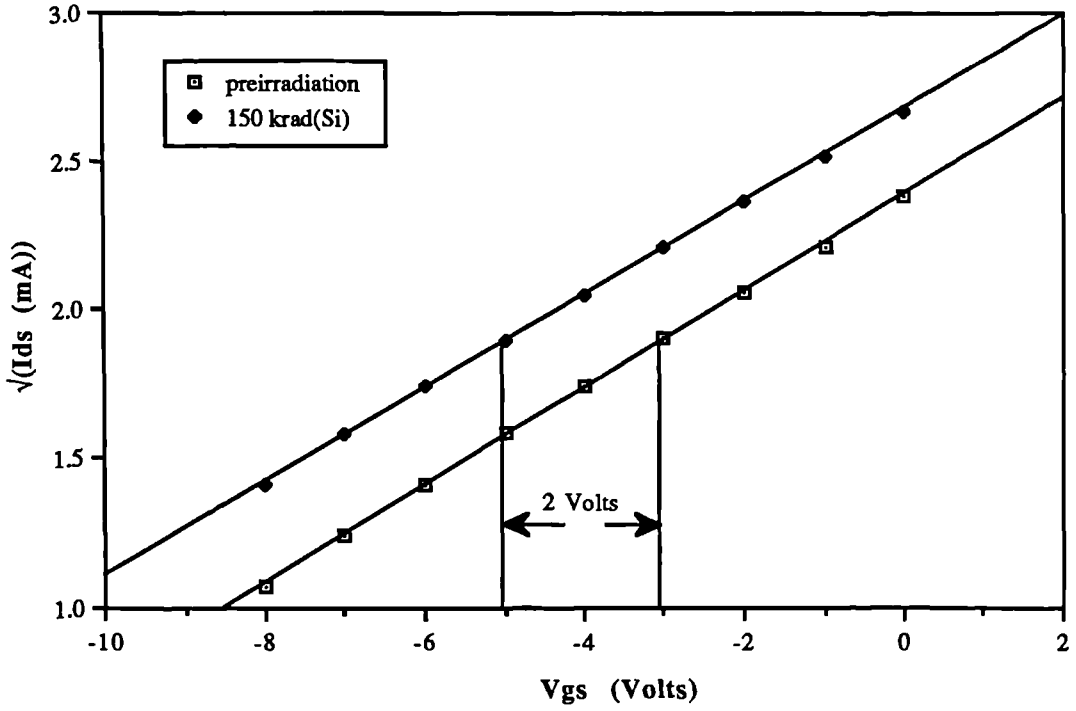

Figure 5.9. $\sqrt{I_{ds}}$ as a function of V_{gs} before and after irradiation showing the 2 Volt shift.

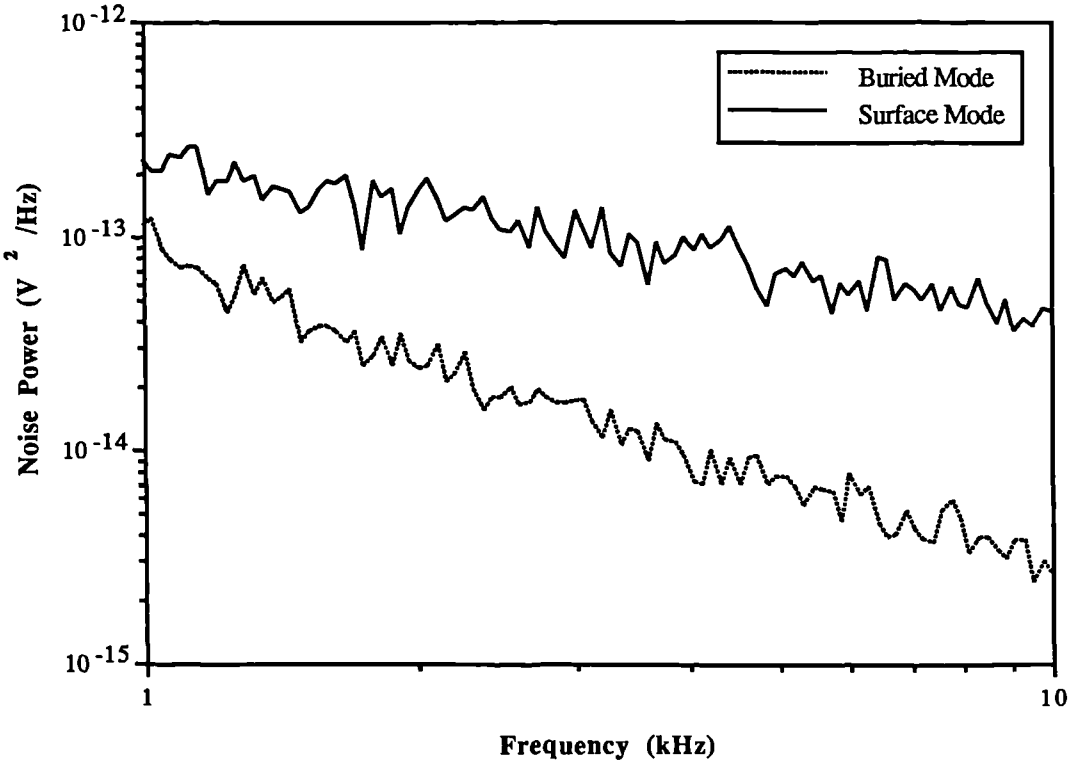

Figure 5.10. Typical noise power spectra for the gate referred noise before irradiation.

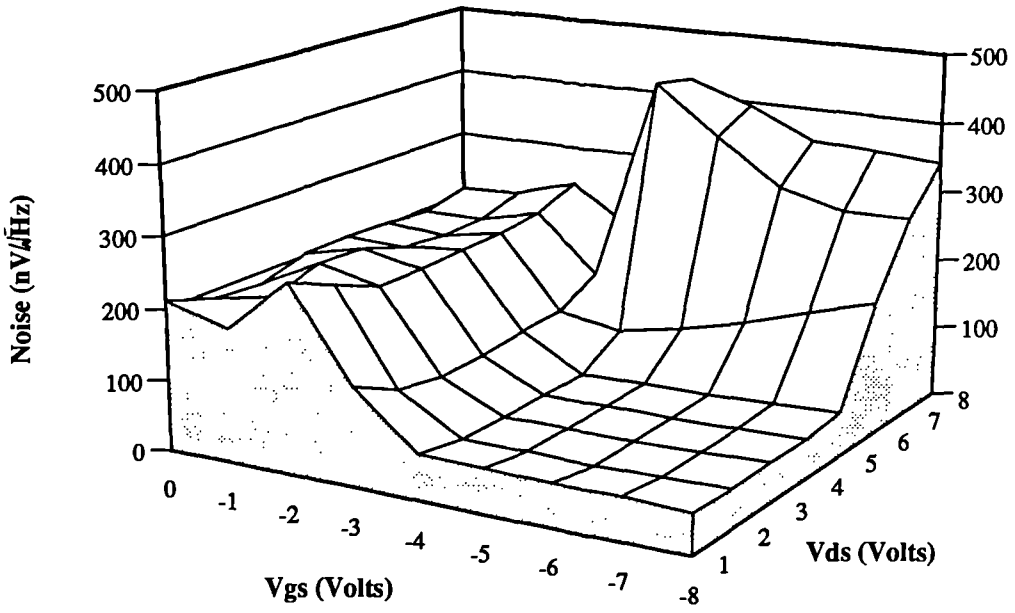

Figure 5.11 (a). The 10 kHz noise map for the device before irradiation.

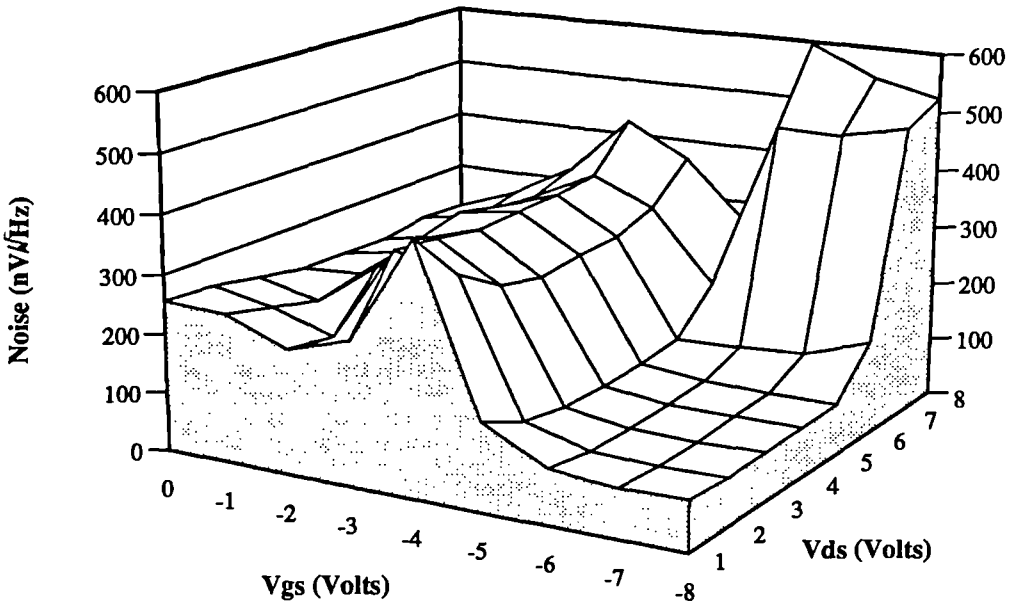

Figure 5.11 (b). The 10 kHz noise map for the device after 150 krad(Si)

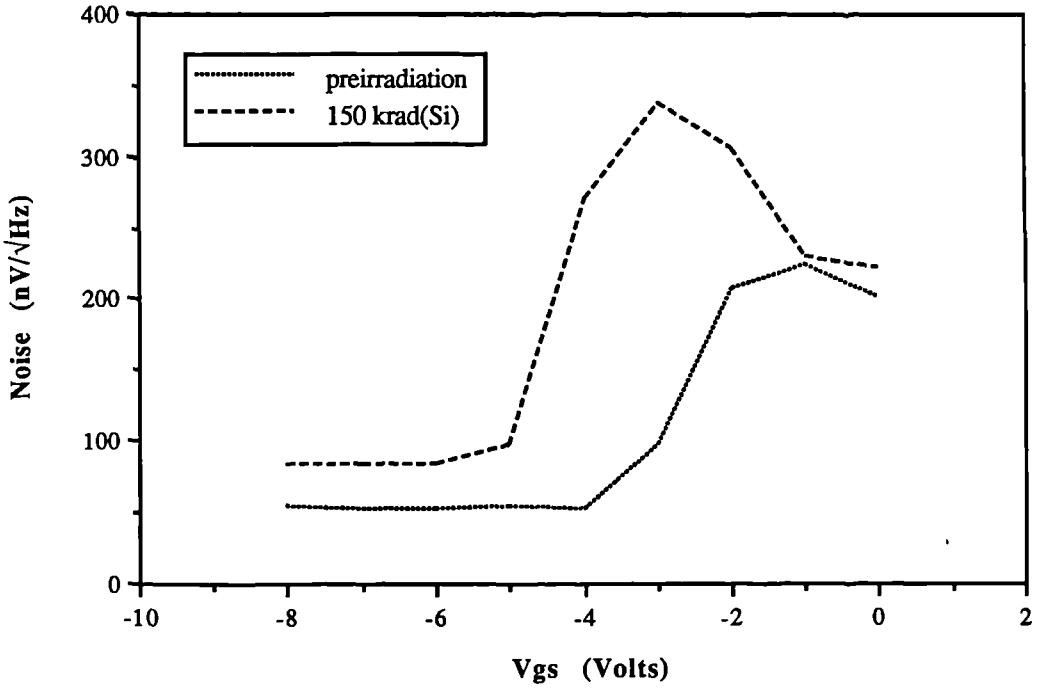

Figure 5.12. The variation of gate referred noise for V_{ds} = 4 Volts.

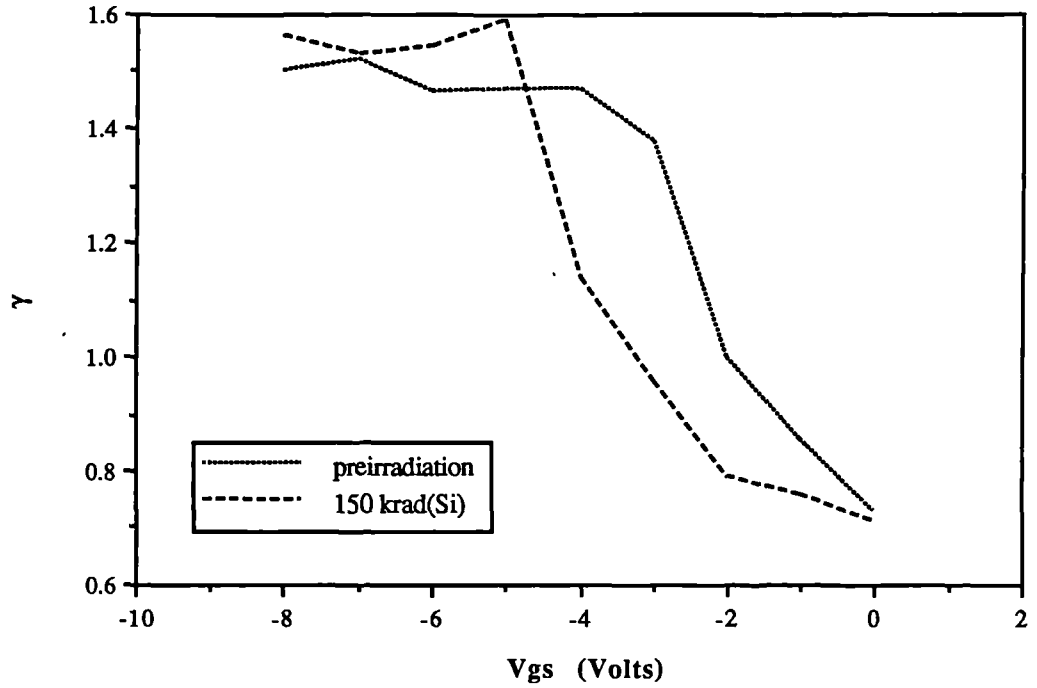

Figure 5.13. The variation of the γ factor for V_{ds} = 4 Volts.

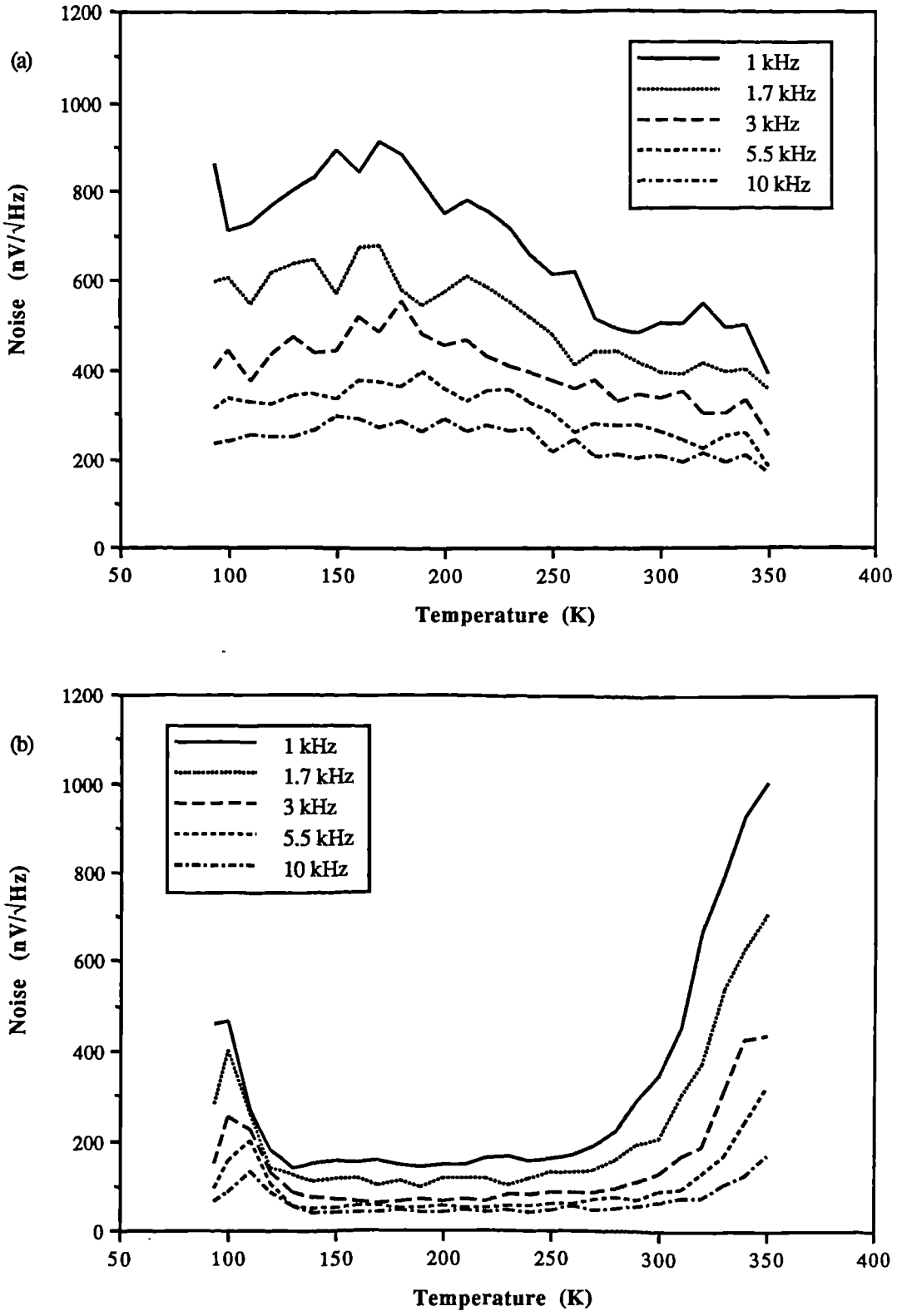

Figure 5.14. Gate referred noise voltage as a function of temperature before irradiation for the output running in (a) surface (b) and buried channel mode.

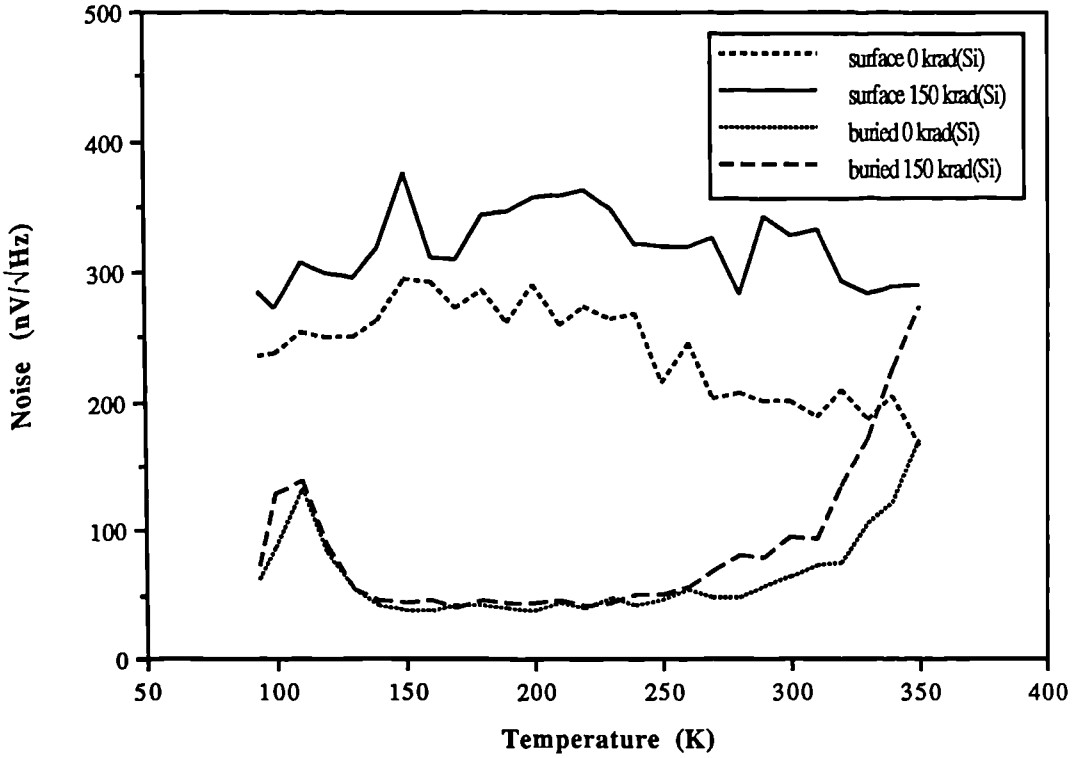

Figure 5.15. Gate referred noise at 10 kHz before and after irradiation

The measured gate referred noise at 10kHz is shown in Figures 5.11. Here the noise was measured at 295K, for a series of gate and source-drain voltages. It is clear from these plots when the conducting channel lies within the bulk silicon, as the noise is significantly reduced. The variation of the gate referred noise for a fixed V_{ds} is shown in Figure 5.12. The noise power was found to have a "1/f$^{\gamma}$" spectrum where γ ranged between 0.8 and 1.5 depending on the point of operation. The variation in γ as the gate voltage is changed is shown in Figure 5.13. When the device is in buried channel mode γ is in the order of 1.5 showing that the majority of the noise is either coming from the interface states at mid band or bulk defects. When the FET is operating in surface channel mode γ is around 0.8 showing that the noise is determined mainly from traps within the oxide. The gate referred noise is almost constant with varying V_{ds}. However when the device is running in buried channel mode, the noise increases sharply for V_{ds} greater than 5 Volts. It is possible that this can be attributed to carrier multiplication effects at the drain. In this range γ was around 0.4. As expected, the point at which surface conduction starts shifts towards lower gate voltages as the device is irradiated.

The noise was measured as a function of temperature, keeping V_{ds} fixed. Typical results for the output FET before irradiation are presented in Figure 5.14. The percentage fluctuation on the noise measurement is inversly proportional to the

square root of the sample size [23]. Therefore the actual fluctuation is greater the higher the mean noise level. This can be observed in the figures. These measurements were undertaken before and after irradiation. In order to account for the flat band voltage shifts, the gate voltage was reduced by the amount of the voltage shift. This implied that the device was kept at the same operating point, i.e. the source-drain current was the same before and after irradiation. For all the measurements V_{ds} was kept fixed at 4 Volts. For the MOSFET in buried channel mode the gate voltage was set to -6 Volts before irradiation and -8 Volts after 150 krad. For surface channel mode the gate voltage was set to 0 Volts and -2 Volts after irradiation. Typical results are shown in Figures 5.15.

5.5. Discussion

For a device running in surface channel mode the gate referred noise increases by around 50% after 150 krad(Si). This increase cannot be caused by an increase in the interface states as it has been shown that interface states cannot be a major cause of "1/f" noise when there is high signal density at the interface. Measurements of noise on n-channel and p-channel surface mode MOSFETs by Meisenheimer, Scofield and Fleetwood *et al* [5] have shown that there is no correlation between the increase in noise and the interface trappped charge up to 10 kHz. This is consistent with the hypothesis that the increase in noise is independent of the density of interface states. In their studies where an n-channel device was biased during irradiation, they also found approximately 50% increase in the noise after 150 krad. The increase in noise power after irradiation appeared to be linked only to the radiation induced charge in the oxide. Meisenheimer proposed two possible mechanisms for the increase in noise. The first involves the modification of the energy or capture cross section of the electron traps by the strong local electric fields due to the trapped holes. The second assumes that the capture of a radiation induced hole may also add a new electron trapping site within the oxide.

For a device operating in buried channel mode, the only significant increase in noise occurs at temperatures above 250K. The preirradiation noise measurements compare favourably with those made by Kandiah on MOSFETs in CCDs [24,25]. The noise peak at around 100K can be explained by a bulk trapping level having an activation energy less that 0.2 eV below the conduction band edge. This could also be linked to the low CTE at these temperatures. The significant "1/f" type noise between 130K and 200K is somewhat of a mystery and it appears to be an artefact of the CCD manufacturing process. Kandiah has attributed this to the combination of shallow depletion under the gate and hole trapping due to poorly defined lateral

edges of the MOSFET channel. Further work has still to be done to clarify the situation. It is not clear why there is no significant increase in noise in this region as the processes involved in the noise generation should be essentially the same as in the surface channel mode of operation and thus some change with irradiation would be expected

The noise above 200K can be seen to be dominated by the generation of electrons and holes by interface states at mid band. The preirradiation noise versus temperature data is consistent with Figure 5.6. Using the model of Kandiah, it can be seen that the preirradiation interface trap density at mid band is in the order of 3 10^{10} cm^2eV^{-1}. After 150 krad this rises to around 5 10^{10} cm^2eV^{-1}. After 150 krad the dark current from the surface increases by around 30 times the preirradiation value. If it is assumed that the dark current for a CCD running in normal mode of operation is dominated by generation/recombination from the interface states then it can be seen that the dark current increase is not consistent with the increase in noise. It may be possible that the noise from this source is being suppressed by some unknown mechanism. It may also be possible that there is a maximum density of traps that can contribute to the noise. After this maximum density has been reached any further increase in interface state density will not add to the noise. This can be checked by making noise measurements as a function of dose. None of the proposed models allow for this eventuality.

Any noise due to low levels of radiation induced bulk defects will be masked by the "interface" noise source and by the "excess" noise at lower temperatures.

From the above it can be seen that there are several questions that remain unanswered. The solution to these problems may lead to a better understanding of the noise generating processes and also to more rigorous models.

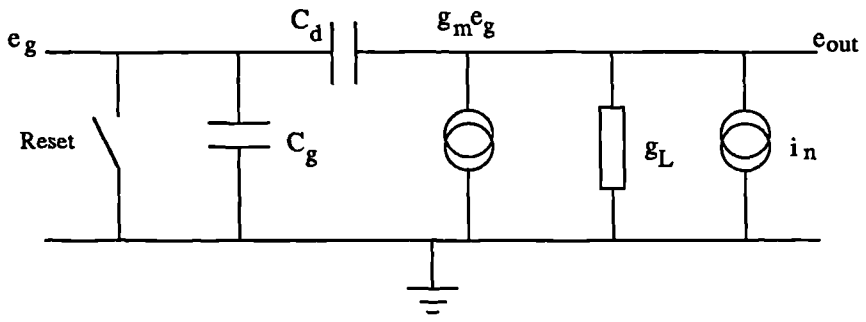

Figure 5.16. The small signal equivalent circuit for the output configuration used for the noise measurements

5.5.1. Implications for low noise application

Before attempting to estimate the noise that would be obtained if the output of the device was passed through signal processing electronics, it is first necessary to relate the measured noise to the noise that would be obtained with the output in "standard" configuration. That is as in Figure 5.1 with its small signal equivalent circuit in Figure 5.2. The small signal equivalent circuit for the output set up for the noise measurements is shown in Figure 5.16. C_d is the source to drain capacitance and C_g is the sum of all other capacitances from the gate of the output FET to ground. During the measurements the reset FET is "on" and so this capacitance can be regarded as being shorted to ground. For low frequencies the voltage gain of the circuit is $A = g_m/g_L$ where g_m is the transconductance of the output FET and g_L is the sum of the conductance of the load and the channel conductance. With the reset FET "on", a noise source, i_n , will give an output voltage of i_n/g_L. Therefore the measured gate referred noise voltage is given by

$$e_{meas} = \frac{i_n}{g_L A} = \frac{i_n}{g_m}.$$

Comparing this with equation (5.5) gives the equivalent noise in terms of r.m.s.

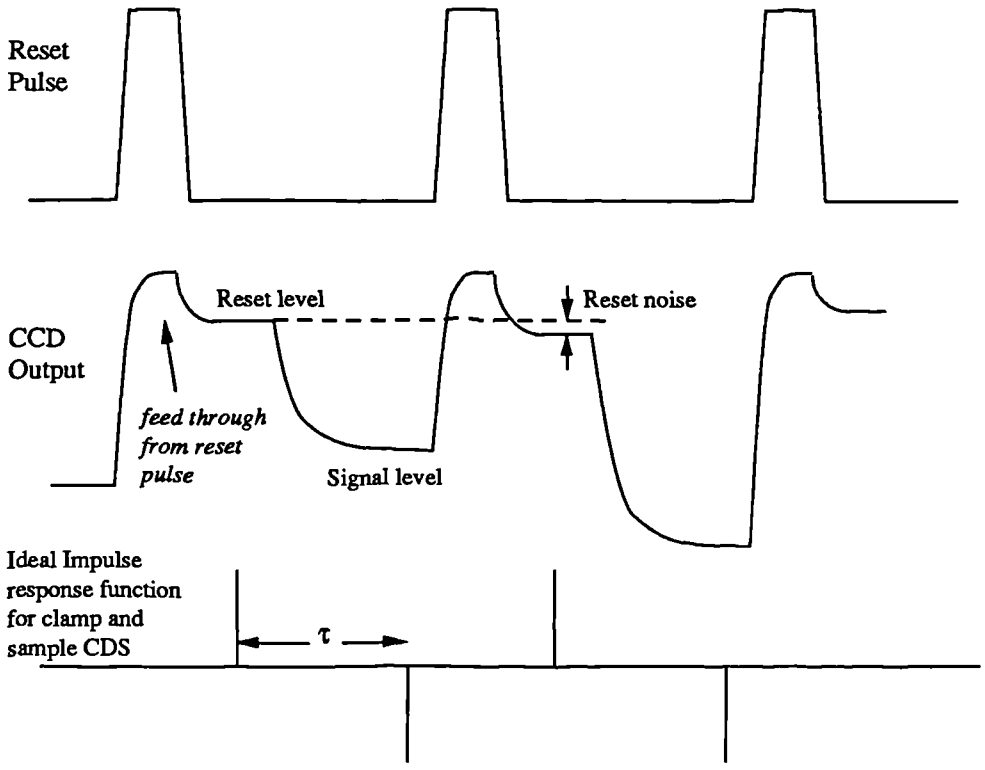

Figure 5.17. The CCD output and the ideal impulse response function for clamp and sample correlated double sampling.

fluctuation in the charge that would be obtained with the CCD operating with the output in "standard" configuration. That is

$$q_n = e_{meas}\,(C_g + C_s).$$

As previously discussed in Section 5.2, the technique of correlated double sampling is usually used for low noise applications. This signal processing method will also modify the noise from the channel of the output FET. The effect on the noise will depend on the method of implementing CDS [26]. For the following discussion the simple method of sample and hold will be used for illustration. The output from the CCD when clocking is shown in Figure 5.17 along with the ideal response function of the clamp and sample process. The CDS processor will clamp at the output voltage at time t_0 and the signal measured at a time t_1. The difference in the measurements is then taken to obtain the signal level without the reset noise. This process acts as a filter with amplitude response given by

$$H_{cds}(f) = 2\sin(\pi f\tau)$$

where τ is the time between the samples. To complete the signal processing, an anti aliasing filter with amplitude response, $H_a(f)$, has to be employed. Ideally this has a cut off frequency given by the Nyquist limit, $(2\tau)^{-1}$. The total noise power after transmission through the CDS system is given by

$$P = \int_0^{\infty} H_a(f)^2 H_{cds}(f)^2 N(f)\,df = \int_0^{1/2\tau} H_{cds}(f)^2 N(f)\,df$$

where N(f) is the noise power density from the output of the CCD. N(f) is made up of the "1/f" component, $N_{1/f}(f)$, and a white noise component, $N_w(f)$, ie.

$$N(f) = N_{1/f}(f) + N_w(f).$$

Only the "1/f" noise component could be measured. Therefore, in order to estimate the total noise after passing through the CDS system, the white noise power has to be calculated. The gate referred white noise from the channel and the load per unit bandwidth for the output set up for the noise measurements is

$$e_w^2 = 4kT(1/R_L + \alpha g_m)/g_m^2$$

The measured "1/f" noise component is designated $e_{meas}(f)$. Therefore, the total number of equivalent noise electrons squared that would appear at the gate of the output FET in the normal configuration after CDS, is given by

$$n^2 = \frac{4(C_g + C_s)^2}{q^2} \int_0^{1/2\tau} \left(4kT \frac{1 + \alpha R_L g_m}{R_L g_m^2} + e_{meas}^2 \right) \sin^2 \pi\tau f \, df$$

where q is the electronic charge. This integral has to be numerically solved to obtain n which will be a function of sample time. The results at 200K for the buried and surface channel mode for a load resistor of 10 kΩ is shown in Figure 5.17. Here it is assumed that the effect of flat band voltage shifts can be corrected for. This implies that the output FET is at the same operating point before and after irradiation. $C_g + C_s$ was taken to be 0.15 pF. The approximate value of α is given by equation (5.7) but this has yet to be verified experimentally for the device structure used here. For the device operating in buried channel mode g_m was 0.445 mS. In surface channel mode g_m was 0.69 mS. In both cases α is approximately 1 giving a calculated gate referred white noise voltage of 5.2 nV/√Hz. The gate referred white noise for a buried channel device measured at 200K using a wide bandwidth preamplifier, averaged between 0.5 MHz and 5 MHz, was 12 nV/√Hz. This includes the noise contribution from the reset FET. The channel resistance of the reset FET is in the order of 10^4 Ω [27]. Therefore the noise due to the reset

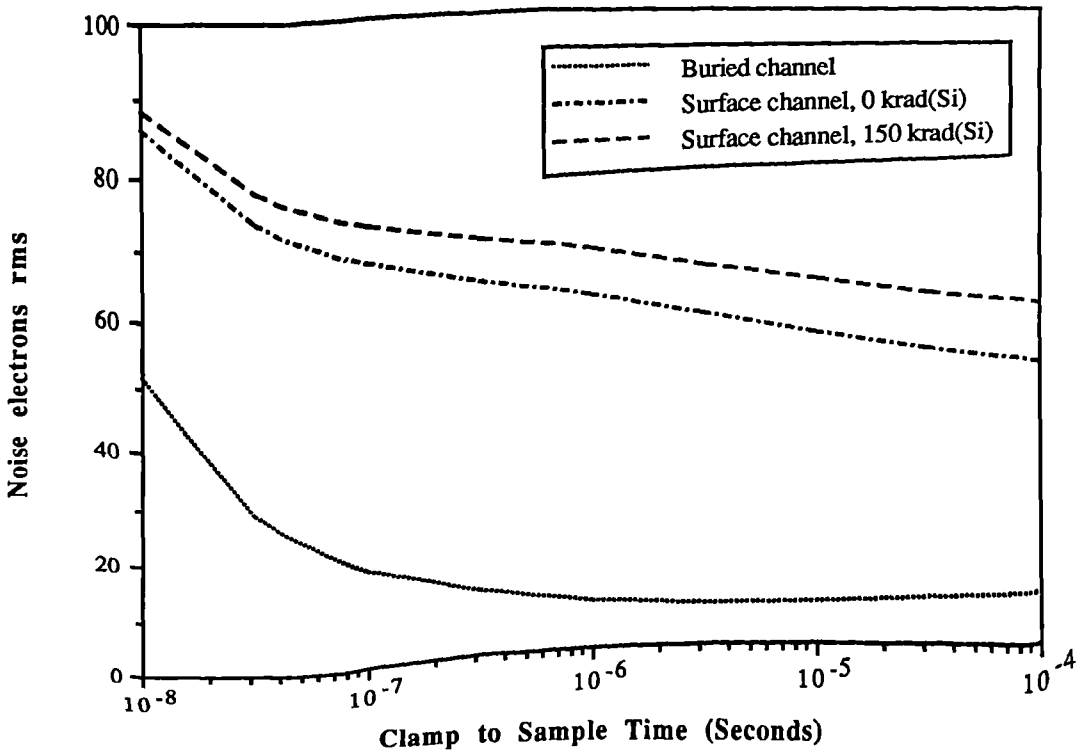

Figure 5.18. The equivalent gate referred noise after signal processing with a theoretical CDS system. The temperature is 200K. There is no change in the buried channel noise after irradiation.

FET would be 10.5 nV/√Hz. Subtracting this from the measured noise in quadrature gives the noise of the output FET as 5.8 nV/√Hz. This shows that the calculated value of α is reasonable. The buried channel result given in Figure 5.18 is consistent with the calculated and measured noise after CDS given in [3].

The case where there is no correction to the flat band voltage shifts is now considered. For low noise applications the output is run in buried channel mode with, for example, a 22 kΩ load resistor and a drain voltage of 28 Volts. V_{rd} is usually set in the region of 17 Volts giving a source voltage of around 24 Volts before irradiation. The variation of source voltage with varying V_{rd} is found by adding a "load line" to the measured characteristic curves. The results are shown in Figure 5.19. It can be seen here that even with a flat band voltage shift of 7 Volts the device will stay in buried channel mode of operation as this depends on the gate-source voltage. The effect of V_{rd} on g_m and g_{ds} is shown in Figure 5.20. A radiation induced voltage shift decreases g_m and increases g_{ds}. For a device running in buried channel mode at 200K the change in noise will be due to a change in g_m and g_{ds}.

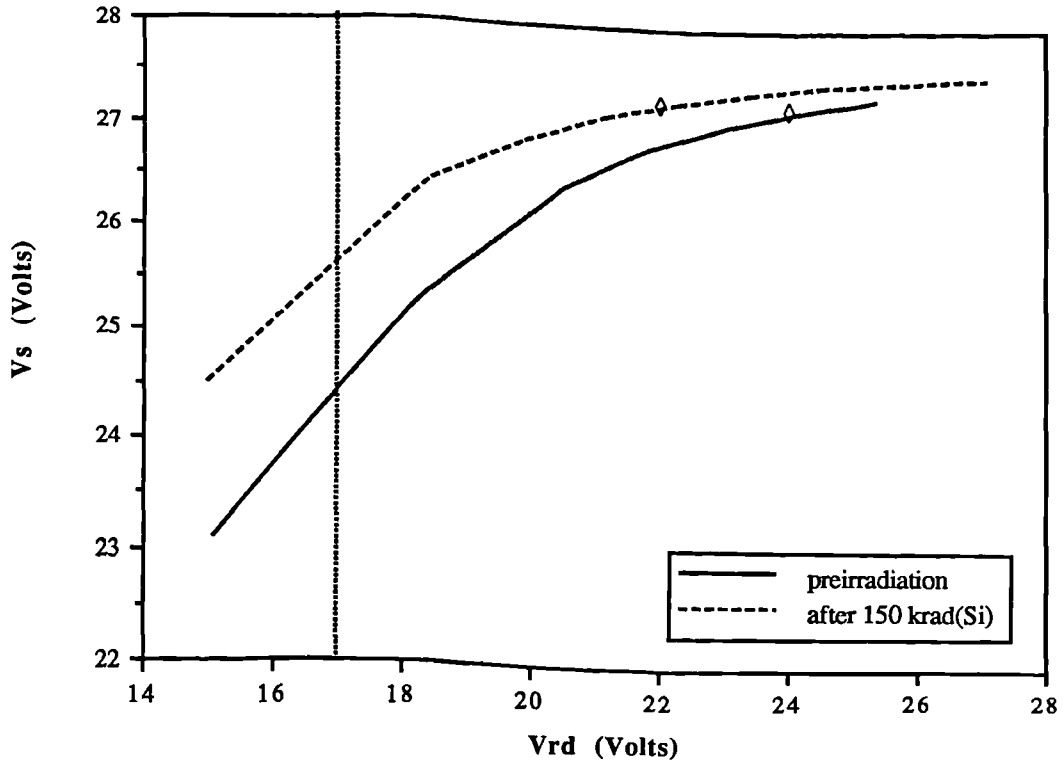

Figure 5.19. The output source voltage, with a 22KΩ load, as a function of V_{rd} before and after irradiation. The diamonds show the onset of surface conduction and the vertical line the normal operation point.

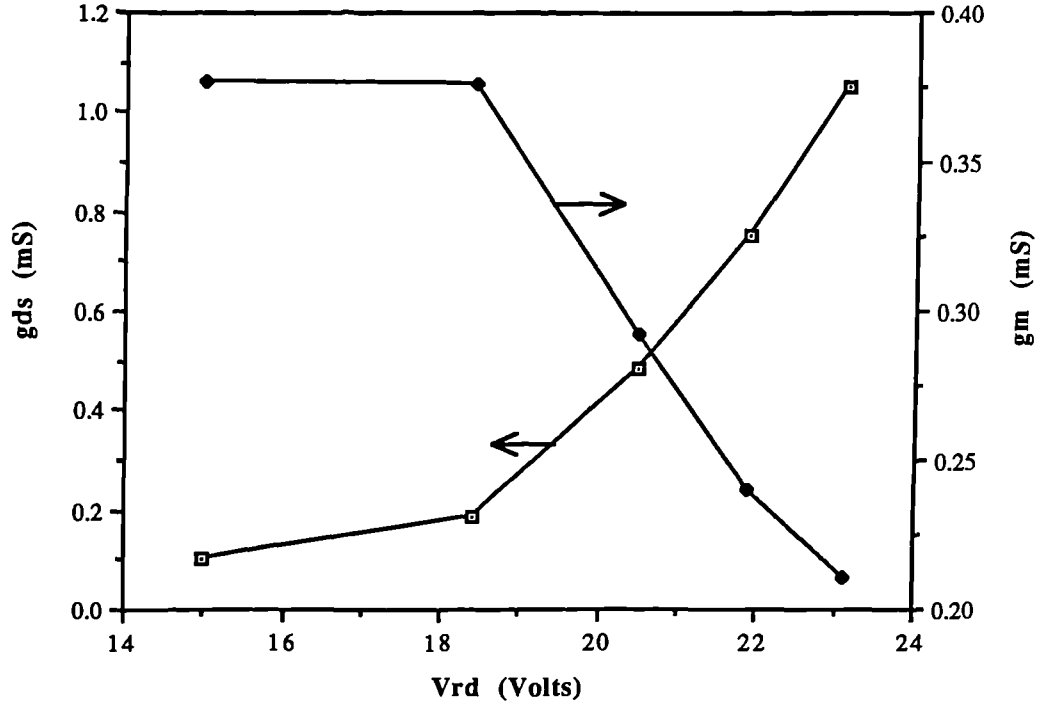

Figure 5.20. g_{ds} and g_m as a function of V_{rd} before irradiation.

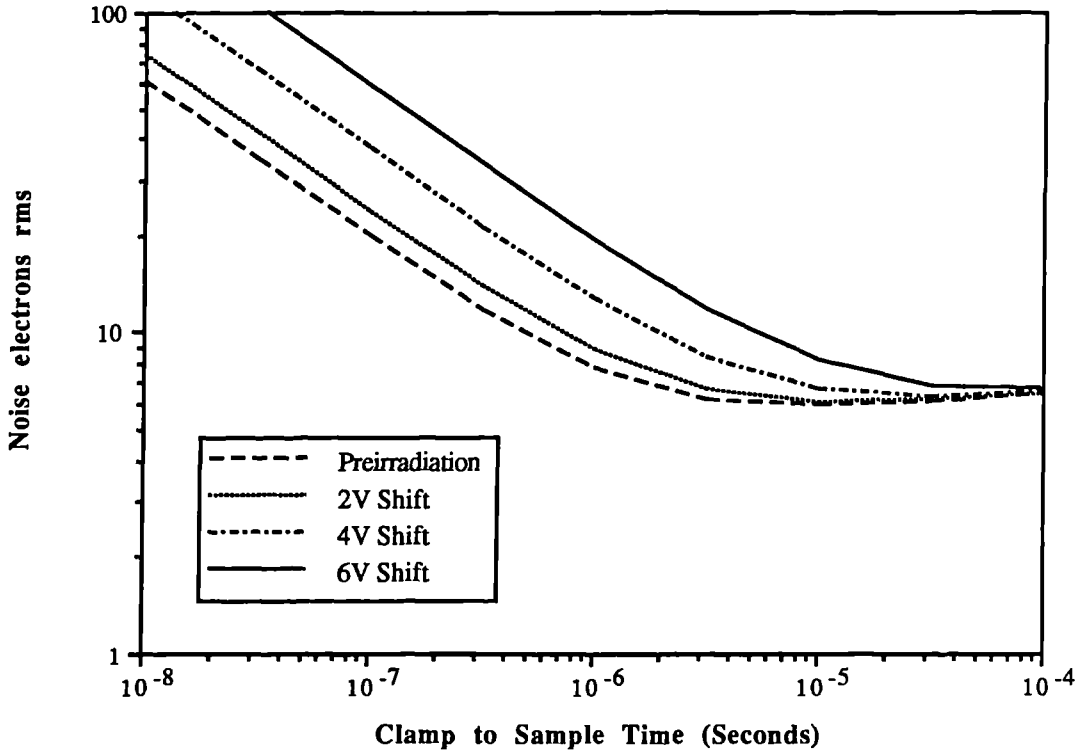

Figure 5.21. The gate referred noise after CDS showing the effect of flat band voltage shifts.

The gate referred noise after CDS, assuming a drain voltage of 28 Volts, V_{rd} of 17 Volts and a 22 kΩ load, is shown in Figure 5.21. Along with the preirradiation noise, the noise curves for a flat band voltage shift of 2, 4 and 6 Volts are also shown. This shows that the change in noise due to the change in operating point of the output MOSFET will be small at low clock frequencies but will increase significantly at higher sampling rates.

5.6. Summary

Beta radiation has been shown have an effect on the noise performance of the output circuit of the UT101 CCD. The noise from the output FET has been measured for a series of bias voltages before and after irradiation. The results show that the onset of surface channel mode of operation is only dependent on the gate-source voltage. In this mode the noise is significantly higher than when the surface of the MOSFET is depleted of mobile charge. The noise has also been measured as a function of temperature. The preirradiation results are consistent with measurements made by Kandiah. However after irradiation the results indicate that improvements in the models are necessary. The magnitude of the noise increase has been shown to be dependent on the mode of operation and on the temperature of the device.

The magnitude of the effect after correlated double sampling has been established. If the device is cooled to 200K there is no increase if the device is run in buried channel mode. If flat band voltage shifts cannot be corrected for then there will be a danger that an excessive flat band voltage shift will force the output FET to conduct at its surface, thus dramatically increasing the noise. However, this does require a large shift in the threshold voltage. Before this happens, the change in the operating point of the output FET will give an increase in the white noise component and thus an increase in noise dependent on the sampling rate. For a sampling rate of 40 kHz, typical of x-ray astronomy applications, a 6 Volt shift will increase the noise from 6 electrons r.m.s. to around 10 electrons r.m.s. From the measurements presented in Chapter 3 a 6 Volt shift would occur for an ionising dose of 400 krad(Si) with the device unbiased during irradiation. If the device was biased during irradiation a 6 Volt shift would occur for a dose of 50 krad(Si). A typical dose expected for a low noise space application is around 10 krad(Si). Therefore the increase in noise will not be significant.

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CHAPTER SIX

A Comparison Between Sr^{90} Irradiation and Co^{60} Irradiation

6.1. Introduction

This chapter gives the results of a comparison between irradiating the CCD with the betas from a Sr^{90} source and the gammas from a Co^{60} source. The irradiation details have been given in chapter two. Two devices from the same wafer were employed for the investigation. The irradiations were carried out at room temperature with all connections grounded, at a rate of 1 krad(Si) per hour.

6.2. Results

The devices were characterised before and after irradiation. The result for the voltage shift measured by monitoring the reset current whilst varying V_{abd} at 180K is given in Figure 6.1. The voltage shift is measured to be 0.85 Volts after 60 krad(Si) from both sources. This implies that the measurement of the dose rate from the Sr^{90} source does not suffer from the problem of significant energy deposition in the insulator due to the low energy betas.

The difference between the sources can be observed in Figure 6.2 which gives the charge transfer inefficiency measurement as a function of temperature. The charge packet size was 1,000 electrons with 5 ms between bursts of signal. It is evident that irradiating with the Co^{60} source gives an the introduction rate of the Si-E centre

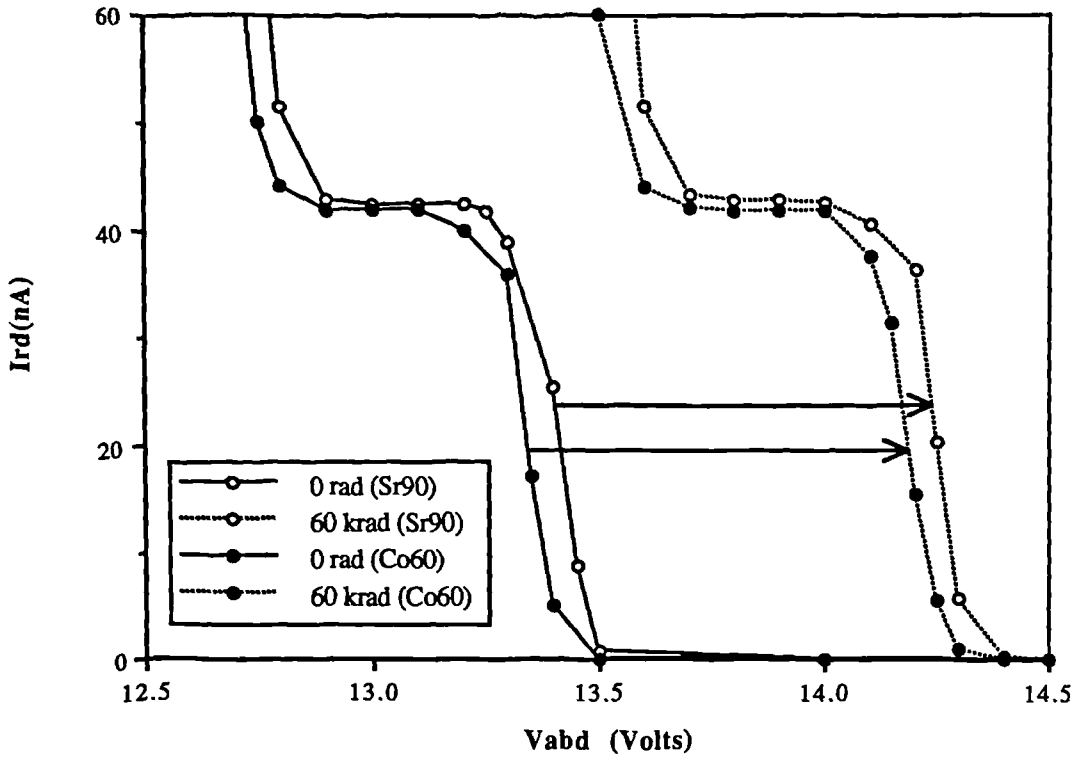

Figure 6.1. A comparison of the voltage shifts obtained using a Sr^{90} beta source and a Co^{60} gamma source.

which is approximately 25% lower than the Sr^{90} irradiated sample. This follows from the lower primary damage caused by the Compton electrons produced by the Co^{60} gammas which have a maximum energy of 1.1 MeV compared with the maximum beta particle energy of 2.3 MeV from the Sr^{90}.

A comparison between the dark current increase is given in Figure 6.3. Here the dark current increase for the Co^{60} irradiated device is divided by the increase caused by irradiation with the Sr^{90} source. The bulk result is acquired by running the device with the surface partially inverted as described in Section 3.3. The majority of the dark current in this situation will be from the bulk of the device. Dark current from both the bulk and the surface is obtained by running the device without the Si/SiO_2 interface inverted. The surface only contribution is obtained by subtracting the dark current obtained with the interface partially inverted from the result obtained with no surface inversion. The results show that the dark current increase is lower for the Co^{60} irradiated device. However there is a greater difference in the bulk contribution to the dark current, once again implying that the bulk damage is lower by approximately 25%.

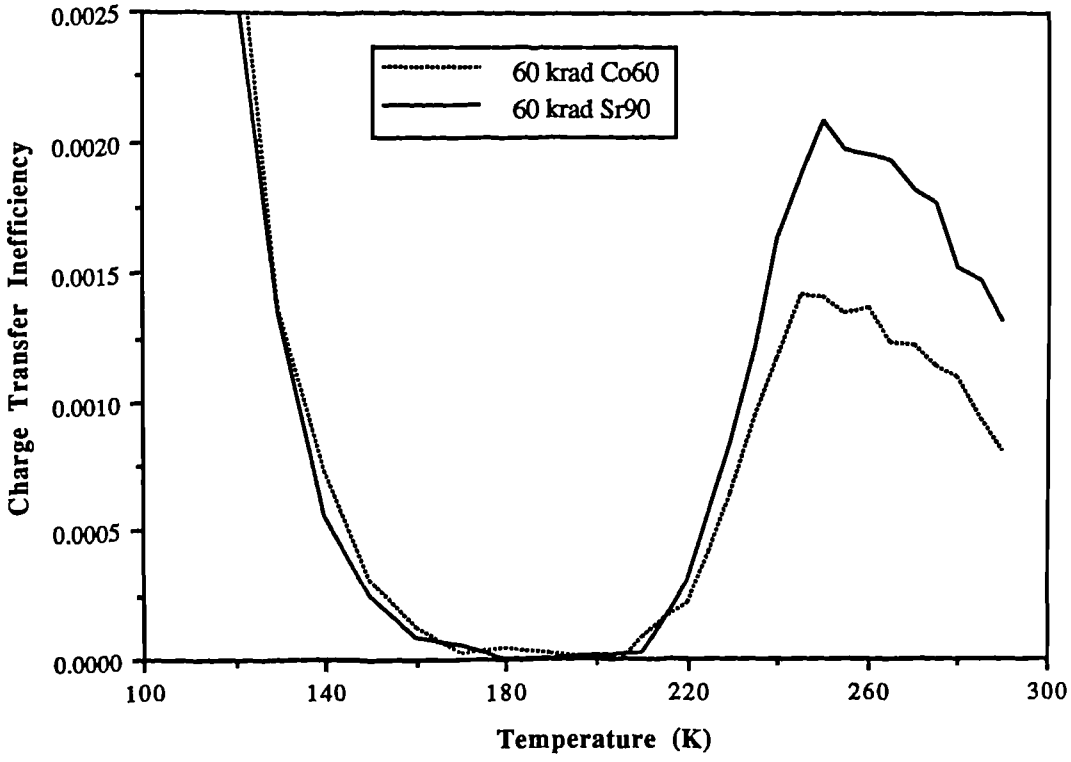

Figure 6.2. A comparison between the CTI measurements.

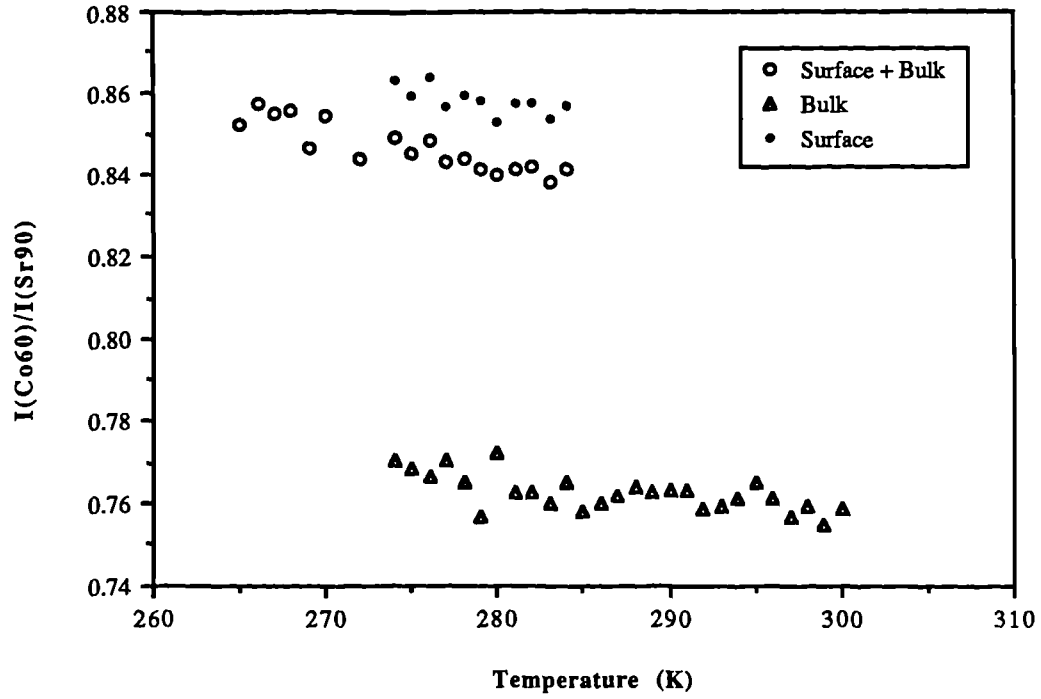

Figure 6.3. The dark current due to Co^{60} irradiation divided by the dark current due to Sr^{90} irradiation for a dose of 60 krad(Si).

6.3. Summary

The ionisation damage of the oxide measured by irradiation from the Co^{60} source is equivalent to the result obtained when the Sr^{90} source is employed. However, the bulk damage has been found to be approximately 25% less than obtained when using the Sr^{90} betas.

CHAPTER SEVEN

A Summary of Results

This chapter brings together the results presented in the preceding chapters

7.1. Flat band voltage shifts and dark current

The voltage shift measured on an EEV UT101 CCD has been found to be 0.014 Volts per krad(Si) after an initial sharp rise for a device unpowered during irradiation. This increases to 0.12 Volts per krad(Si) if the device is left running during irradiation. Irradiating the device biased does not effect the dark current increase. Typically the dark current increases by 12 nA at 280K after 50 krad(Si) with zero potential applied to the substrate. This decreases to 2 nA after 50 krad(Si) with 5 Volts applied to the substrate. In this case the device was running continuously at a readout rate of 83 kHz. Irradiating the device at 180K and heating to room temperature had little effect on the voltage shift. Neither did heating the device to 430K for two hours in a nitrogen atmosphere. However, this heat treatment did cause a three fold increase in the dark current.

Thinning the oxide layer of the Si_3N_4/SiO_2 gate insulator structure reduces the voltage shifts. Halving the oxide thickness has been found to increase the radiation hardness by a factor two.

7.2. Batch Qualification

The voltage shift and dark current increase was found to be consistent over the five batches of devices tested. The voltage shift that could be tolerated did vary. This was significant on only one of the batches tested.

7.3. Charge transfer degradation

The CTE degradation has been successfully measured using the periodic pulse technique for signal sizes as low as 200 electrons. The main radiation induced defect causing a CTE reduction in Sr^{90} irradiated devices has been found to be the Si-E centre. The energy level of this centre has been measured as 0.47±0.03 eV below the conduction band edge and the capture cross section as (3±1) 10^{-15} cm^2. The CTI is a function of temperature, signal density, time the signal spends under a gate and the sparseness of the data. A method for estimating the effective signal density has been given. From this measurement the introduction rate of the Si-E centre has been calculated to be 0.020±0.006 cm^{-1}. A model for the degradation has been given that can be extended to other radiation types and energies. The loss of CTE can be successfully recovered by heating the device to 150°C for two hours. However, the annealing of the Si-E centre is accompanied by the increase in CTI at low temperatures, probably due to the formation of another defect.

7.4. Noise from the output circuit

The noise from the output circuit has been found to increase with irradiation. However, this increase is dependent on the mode of operation. For applications where the noise is critical, the device is normally run with the output MOSFET in buried channel mode and correlated double sampling is usually employed. In this situation the noise increase is dominated by the change in the operation point of the output MOSFET due to the voltage shifts. If the device is clocked at a rate of 40 kHz, the noise increase is less than 4 electrons r.m.s. up to doses of 50 krad(Si) with the device biased during irradiation and up to 400 krad(Si) with the device unbiased. The noise increase gets larger as the sampling rate increases.

7.5. Comparison between Co^{60} irradiation and Sr^{90} irradiation

The voltage shifts measured using a Co^{60} source have been found to be identical to those from a Sr^{90} source. However, the bulk damage appears to be approximately 25% lower.

CHAPTER EIGHT

Conclusion

8.1. Consequences for specific applications

Most of the effects of beta and gamma radiation on the EEV charge coupled devices have been established. The importance of each degradation mechanism is dependent on the application. If the biases can be changed then the effect of trapped oxide charge can mostly be corrected for. If the applied biases cannot be changed then the device will eventually fail. The failure mechanisms due to the voltage shifts for the "standard" EEV UT101 device are given in Table 8.1. Also shown are the typical ionising doses for failure assuming the voltage shifts cannot be rectified.

The charge transfer efficiency is dependent on several factors so it is hard to define a device lifetime due to the charge transfer degradation mechanism without knowing the exact environment and the sparseness of the data. However, a worse case value of the CTI increase can be obtained by setting the G factor and the filling factor of the model to one (Section 4.6.1).

As an example of the understanding of device degradation the CCDs of the SLD vertex detector are considered. For the SLD vertex detector, tracking the passage of minimum ionising particles would be degraded if more than 20% of the charge was lost from the hit pixel. Therefore the maximum CTI that can be tolerated is in the order of 6 10^{-4}. From the model, assuming that G and F are unity, this would occur for a fluence of 5 10^{9} cm^{-2} 1 MeV neutrons or 10 GeV pions. However, G

Failure Mode	Typical allowed voltage shift (Volts)	Maximum dose with the device **unbiased** during irradiation (Krad(Si))	Maximum dose with the device **biased** during irradiation (Krad(Si))
Charge injection from the drains	~19	1,400	160
Inability to reset output circuit	~8	570	70
Dark current from surface no longer suppressed	~4	290	30
Output MOSFET starts to run in surface channel mode	~6	430	50
Output node not attractive to signal electrons	~5	360	42

TABLE 8.1. Main failure modes due to trapped oxide charge.

will be much less than unity as the detector is being operated at 180K and background hits help to keep the traps filled. Therefore the critical fluence would be significantly higher than this. In terms of tracks from the interaction of the electrons and positrons, at the SLAC linear collider, the fluence expected is several orders of magnitude lower than the critical value and so can be ignored. Thus neutrons originating from the SLC beam dumps are the main concern. The life of the detector will be significantly greater than 5 years if the experienced fluence is less than 10^9 cm^{-2}, 1MeV equivalent neutrons per year. Before the detector was installed the neutron fluence around the interaction point was measured as ~10^{11} cm^{-2} per year [1]. This was clearly unacceptable. However, since then, much effort has been put into reducing this value and it is now down to immeasurable levels [2]. Most of the expected ionising dose of 10 krad(Si) per year for the vertex detector originates from X-rays which do not cause displacement damage. The drive electronics are versatile enough to allow manual correction for the flat band voltage shifts, up to a shift of at least 10 Volts. Therefore the voltage shifts are not of concern.

To take another example, over the life of the NA32 experiment, a region of 200 μm by 1 cm received 25 10^{11}, 200 GeV pions. Some sign of degradation (signal loss) from this region was observed towards the end of the experimental run. Reasonable results were still obtained from the damaged region due to the traps

being filled by signal charge and the fast clocking conditions. There was also some signs of annealing of the bulk damage.

8.2. Further work

Further work is required to fully validate the model of CTE degradation for types of radiation other than Sr^{90} betas. Work is also necessary to completely understand the effect of radiation on the MNOS structure. This is necessary as there are situations where the voltage shifts are unacceptable. If a CCD TV camera is required to operate up to doses of 10 Mrad(Si) or the application does not allow the additional electronics required to track the voltage shifts then a more radiation hard gate insulator is required. No work has yet been undertaken on the gate insulator structure where the oxide layer has been regrown after ion implantation. The present work has shown that a significant improvement in the radiation hardness can be achieved by thinning the oxide layer. However it is not known how thinning the oxide effects the device reliability. In fact the effect of irradiation on the reliability of devices is a topic that deserves attention.

The increase in noise has been found to be insignificant for the simple output circuit of the UT101 CCD. However, the faster two and three stage amplifiers found on some of the newer devices have yet to be investigated. Further investigation into the noise performance of buried channel MOSFETs after irradiation could lead to a better understanding of the preirradiation "1/f" noise of both surface and buried channel MOSFETs.

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APPENDIX 1

The Calculation of the Distribution of Charge Through the CCD

This appendix describes the calculation of the charge distribution through a buried channel CCD. The method employed is that of Kent [1] who gave the charge distribution for two particular device structures. The calculations have had to be repeated for the EEV UT101 CCD.

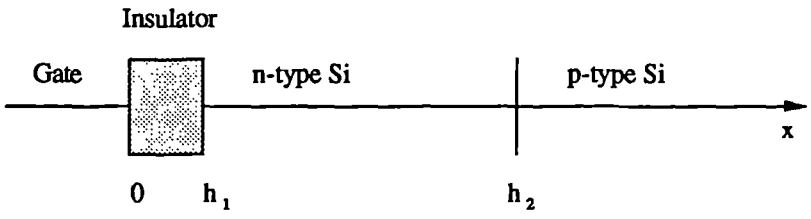

Figure A1.1. The buried channel device structure

Consider the buried channel structure illustrated in Figure A1.1. In one dimension the device can be split into three regions. These regions are

$0 \leq x \leq h_1$ Region 1, the silicon dioxide which has a relative dielectric constant of $K_O = 4$.

$h_1 \leq x \leq h_2$ Region 2, n-type silicon with donor density of $N_D(x)$ and dielectric constant $K_S = 12$.

$h_2 \leq x \leq \infty$ Region 3, p-type silicon with acceptor density of $N_A(x)$ and dielectric constant K_S.

The point at $x = 0$ is a perfectly conducting boundary held at a potential V_0. The potentials within the three regions, ϕ, satisfy the one dimensional Poisson equation.

Region 1 $$\frac{d^2\phi}{dx^2} = 0$$

Region 2 $$\frac{d^2\phi}{dx^2} = \frac{-q}{K_s\varepsilon_0}(N_D - n(x))$$

Region 3 $$\frac{d^2\phi}{dx^2} = \frac{q}{K_s\varepsilon_0}(N_A - p(x) + n(x))$$

where ε_0 is the permittivity of free space, n(x) and p(x) are the free electron and hole densities respectively. The band diagram for the buried channel structure is given in Figure A1.2. The most general expression for n(x) is

$$n(x) = \int_{E_c(x)}^{\infty} N(E)F_e(E)dE$$

where N(E) is the density of states, $F_e(E)$ is the Fermi distribution for electrons and $E_c(x)$ is the conduction band edge. This gives

$$n(x) = N_c \int_{E_c(x)}^{\infty} \frac{\sqrt{(E - E_c(x))}}{1 + \exp((E - E_{fe})/kT)}dE \approx N_c \int_{E_c(x)}^{\infty} \frac{\sqrt{(E - E_c(x))}}{\exp((E - E_{fe})/kT)}dE$$

where E_{fe} is the pseudo-Fermi level for the electrons and N_c is the constant

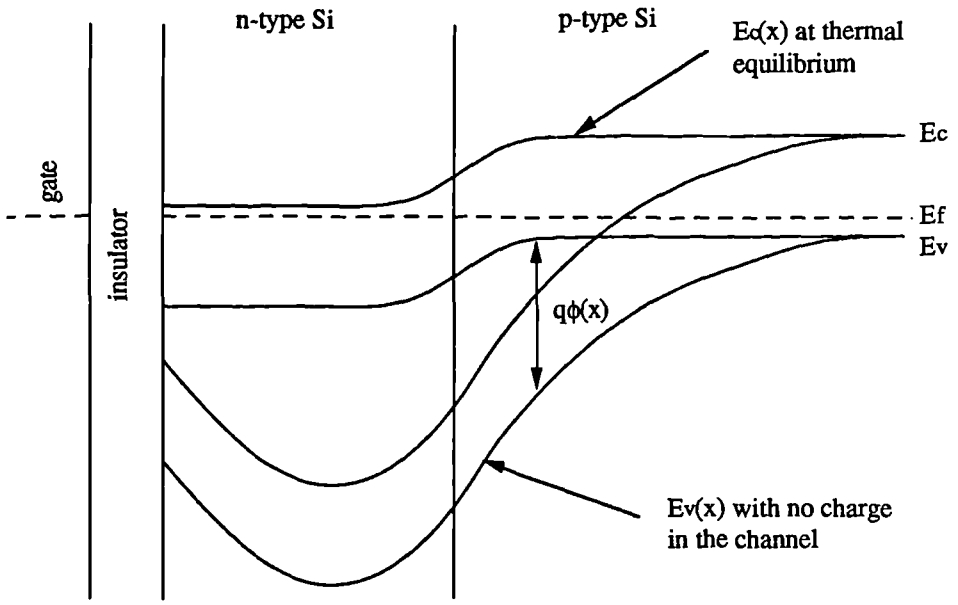

Figure A1.2. The band diagram for a buried channel structure.

$$N_c = 4\pi(2m_c/h^2)^{3/2}$$

where m_c is the density of states effective mass for electrons in the conduction band and h is Planck's constant. By changing variable, n(x) becomes

$$n(x) = N_c(kT)^{3/2}\int_0^{\infty}\frac{\varepsilon^{1/2}}{\exp(\varepsilon+\eta'-q\phi(x)/kT)}d\varepsilon$$

where $\varepsilon = (E-E_c(x))/kT$, $E_c(x) = E_c - q\phi(x)$, E_c is the conduction band edge at $x = \infty$ and $\eta' = (E_c - E_{fe})/kT$. This reduces to

$$n(x) = N_c(kT)^{3/2}\Gamma(3/2)\exp\left(\frac{q\phi}{kT}-\eta'\right)$$

where $\Gamma(n)$ is the gamma function given by

$$\Gamma(n) = \int_0^{\infty} x^{n-1}\exp(-x)dx.$$

A similar expression can be obtained for the density of free holes.

$$p(x) = N_v(kT)^{3/2}\Gamma(3/2)\exp\left(\eta-\frac{q\phi}{kT}\right).$$

Here $\eta = (E_v - E_f)/kT$ where E_v is the conduction band edge at $x = \infty$ and E_f is the equilibrium Fermi level for holes. N_v is a constant given by

$$N_v = 4\pi(2m_v/h^2)^{3/2}$$

where m_v is the density of states effective mass for holes in the valence band.

At $x = \infty$ $\phi(\infty) = 0$ and $p(\infty) = N_A$. This implies that

$$\frac{\exp(-\eta)}{(kT)^{3/2}\Gamma(3/2)} = \frac{N_v}{N_A} \quad \text{and}$$

$$\frac{N_c}{N_A} = \frac{N_v}{N_A}\times\frac{N_c}{N_v} = \left(\frac{m_c}{m_v}\right)^{3/2}\frac{\exp(-\eta)}{(kT)^{3/2}\Gamma(3/2)}.$$

This gives

$$n(x) = N_A\left(\frac{m_c}{m_v}\right)^{3/2}\exp\left(\frac{q\phi}{kT}-(\eta'+\eta)\right) \quad \text{and}$$

$$p(x) = N_A \exp\left(-\frac{q\phi}{kT}\right).$$

The parameter η is dependent on the equilibrium Fermi level and η' is dependent on the pseudo Fermi level for electrons and is fixed for the total amount of free charge. The total amount of free signal per unit area in the device is given by

$$S = \int_{h1}^{\infty} n(x)\,dx \qquad \text{(A1.1)}$$

In reality the determination of η' is difficult, so the alternative scheme of choosing η' and calculating the resulting charge is employed. The set of equations that have to be solved become

Region 1 $$\frac{d^2\phi}{dx^2} = 0 \qquad \text{(A1.2)}$$

Region 2 $$\frac{d^2\phi}{dx^2} = \frac{-qN_A}{K_s\varepsilon_0}\left(\frac{N_D}{N_A} - \left(\frac{m_c}{m_v}\right)^{3/2}\exp\left(\frac{q\phi}{kT} - \rho_0\right)\right) \qquad \text{(A1.3)}$$

Region 3 $$\frac{d^2\phi}{dx^2} = \frac{qN_A}{K_s\varepsilon_0}\left(1 - \exp\left(-\frac{q\phi}{kT}\right) + \left(\frac{m_c}{m_v}\right)^{3/2}\exp\left(\frac{q\phi}{kT} - \rho_0\right)\right) \qquad \text{(A1.4)}$$

where the parameter ρ_0 replaces $\eta+\eta'$. The boundary conditions are

$$\phi(0) = V_0$$

$$\phi(\infty) = 0$$

and the continuity equations are

$$\phi_-(h_1) = \phi_+(h_1)$$

$$K_o\frac{d\phi_-(h_1)}{dx} = K_s\frac{d\phi_+(h_1)}{dx}$$

$$\phi_-(h_2) = \phi_+(h_2)$$

$$\frac{d\phi_-(h_2)}{dx} = \frac{d\phi_+(h_2)}{dx}$$

The system of differential equations (A1.2), (A1.3) and (A.4) together with the boundary and continuity equations have to be solved numerically by the method of finite differences. The exact method for the solution has been given by Kent and

will not be repeated here. However, a Fortran program employing the techniques is given at the end of this section. This program can calculate the charge distribution through both n and p channel devices. The operation scheme can be summarised as follows,

i) A value of ρ_0 is chosen corresponding to a small total charge.
ii) Solve for $\phi(x)$, thus determining n(x).
iii) Integrate n(x) to find the total charge per unit area.
iv) Increment ρ_0 by $\Delta\rho$ and repeat steps ii), iii) and iv).

To check the operation of the program, the results are compared with those of Kent. Figure A1.3 shows the charge distribution through a p-channel device calculated by Kent . The device had a substrate dopant density of 10^{14} cm^{-3} and an implant of density 2 10^{15}. The oxide thickness was 200 nm, the implantation depth was 5 μm and the gate potential was -4 Volts. The distance into the silicon is plotted in terms

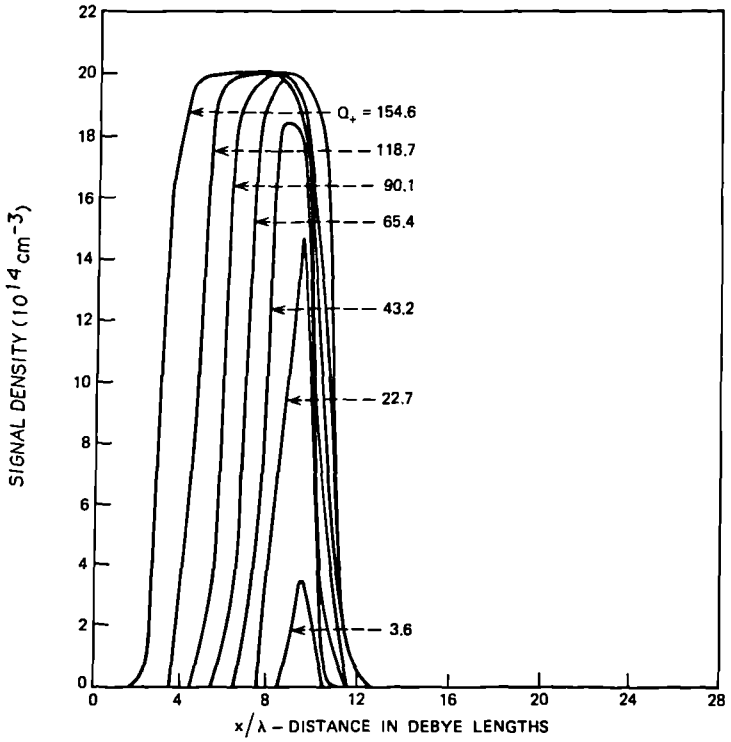

Figure A1.3. The charge distribution calculated by Kent. The parameter Q_+ is defined in the text.

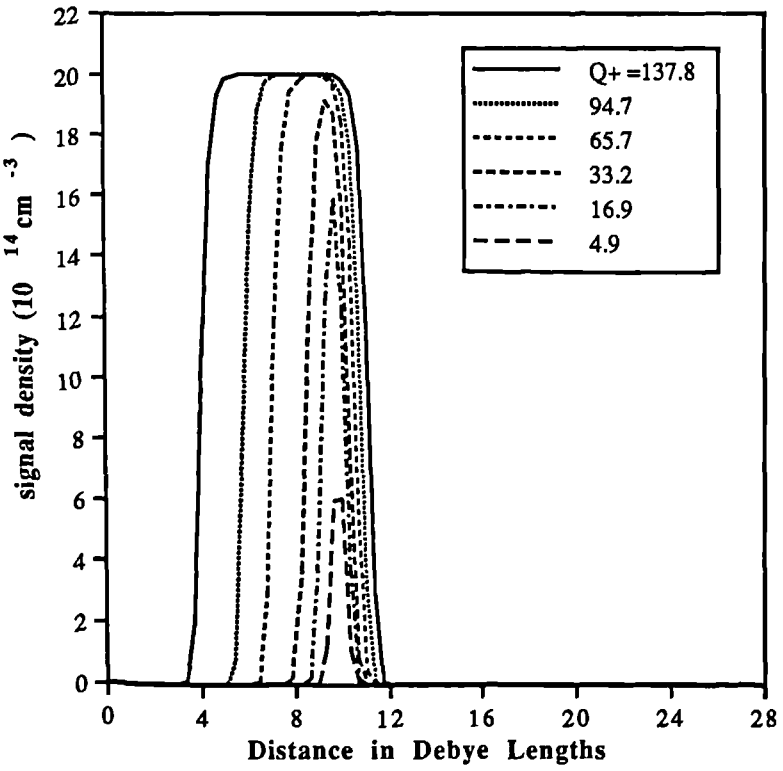

Figure A1.4. The charge distribution calculated for the present work. Q_+ is defined in the text.

of the Debye length, λ.

$$\lambda = \sqrt{kTK_s\varepsilon_o/q^2N} \approx 0.415\ \mu m$$

where N is the dopant density of the lightly doped substrate. The signal density distribution is plotted as a function of a parameter, Q_+.

$$Q_+ = S/(100\lambda)$$

where S is the number of charge carriers per μm^2 and λ is measured in μm. The calculations were repeated using the current program and the results are shown in Figure A1.4. The agreement is good showing that the calculation is reliable. An additional check is shown in Figure A1.5 which shows the calculated potential distribution through a similar device structure to the EEV UT101 CCD with zero signal charge. The numerical calculation obtained from the program is compared with the analytical solution that has been obtained by solving the Poisson equations assuming the depletion approximation [2]. Once again the agreement is good.

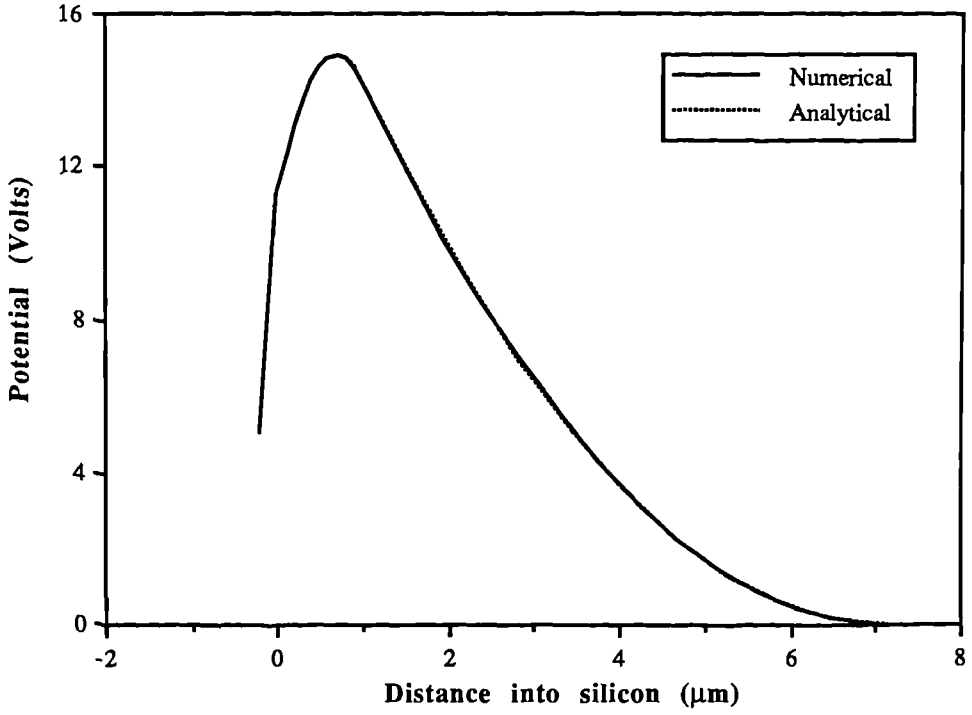

Figure A1.5. The potential distribution through an n-channel CCD with $N_D = 10^{16}$ cm^{-3} and $N_A = 5\ 10^{14}$ cm^{-3}. The implantation depth is 1 μm and the oxide thickness 200 nm. The gate voltage is 5 Volts and there is no signal charge.

```
      PROGRAM CHADEN
*************************************************************************
*     PROGRAM TO CALCULATE THE CHARGE DENSITY THROUGH A BURIED          *
*     CHANNEL CCD.                                                      *
*     THE DOPING PROFILE IS APPROXIMATED TO A STEP FUNCTION             *
*************************************************************************
*     THIS IS FOR AN N AND P CHANNEL DEVICE.                            *
*     THE INPUT IS READ FROM A FILE CHADEN.SET                          *
*     THE OUTPUT IS WRITTEN TO FILES WHOSE NAMES ARE USER DEFINED       *
*************************************************************************
*     DETAILS CAN BE FOUND IN :                                         *
*     W.H.KENT,THE BELL SYSTEM TECH.JOU.,52,P1009-1024,1973.            *
*************************************************************************
*           M.S.ROBBINS  BRUNEL UNIVERSITY  27-3-91                     *
*************************************************************************
      PARAMETER(N=150,NUMMX=9)
      DOUBLE PRECISION A(N,N),V(N),AI(N,N)
      DOUBLE PRECISION H1,H2,L,QMAX
      DOUBLE PRECISION DO,DP,DN,DP2,DN2,NEWV,RHO,ANS,W,Z,DZ,X(N),VMIN
      DOUBLE PRECISION QQ,Q(N),ZMAX(NUMMX),ACC,T,D1,D2,ND,NA,TEMP,LAMDA
      DOUBLE PRECISION KT,DOR,DPR,DNR,MAXV,VG,S,VGATE,M,S1,S2,RSTORE(N)
      INTEGER N1,N2,N3,INDX(N),CNT,NUM,TP
      CHARACTER*30 POTENT
      CHARACTER*32 FILEV
      CHARACTER*12 FILEIN
      CHARACTER*1 TYPE
```

```
      FILEIN='CHADEN.SET'
* CNT IS THE ASCII VALUE FOR THE NUMBER OF THE RESULTS FILE
* 49 IS THE ASCII VALUE FOR '1'
      CNT=49
      POTENT='                    '
* READ IN USER DEFINED VARIABLES FROM THE FILE 'CHADEN.SET'
      OPEN(10,STATUS='UNKNOWN',FILE=FILEIN)
* SKIP THE TITLE
      READ(10,*)
      READ(10,*)
      READ(10,'(A30)')POTENT
* OPEN FILE FOR RESULTS
      OPEN(8,STATUS='UNKNOWN',FILE=POTENT)
* COPY INPUT FILE
      OPEN(7,STATUS='UNKNOWN',FILE=POTENT//'.SET')
      WRITE(7,*)'      Set Up File For CHADEN.EXE'
* ARE WE DEALING WITH AN N OR P CHANNEL DEVICE
      READ(10,'(A1)')TYPE
      WRITE(7,'(1X,A1)')TYPE
      IF(TYPE.NE.'N'.AND.TYPE.NE.'P')THEN
            WRITE(6,*)'DEVICE TYPE NOT KNOWN'
            GOTO 1000
      ENDIF
      IF(TYPE.EQ.'N')THEN
            TP=-1
            M=0.404
      ELSE
            TP=1
            M=2.48
      ENDIF
      READ(10,*)ND
      WRITE(7,*)ND
      READ(10,*)NA
      WRITE(7,*)NA
      S=ND/NA
      READ(10,*)T
      WRITE(7,'(F5.3)')T
      READ(10,*)D1
      WRITE(7,'(F5.2)')D1
      READ(10,*)D2
      WRITE(7,'(F5.2)')D2
      READ(10,*)N1
      WRITE(7,*)N1
      READ(10,*)N2
      WRITE(7,*)N2
      READ(10,*)N3
      WRITE(7,*)N3
      READ(10,*)TEMP
      WRITE(7,'(F6.1)')TEMP
      KT=1.38E-23*TEMP
      READ(10,*)VGATE
      WRITE(7,'(F4.1)')VGATE
* CONVERT GATE VOLTAGE TO THERMAL VOLTS
      VG=TP*1.6E-19*VGATE/KT
* ACC IS THE MAXIMUM RESIDUAL REQUIRED
      READ(10,*)ACC
      WRITE(7,'(F6.4)')ACC
* HOW MANY DATA SETS DO WE REQUIRE?
      READ(10,*)NUM
WRITE(7,*)NUM IF(NUM.GT.NUMMX)
      NUM=NUMMX
      DO I = 1,NUM
            READ(10,*)ZMAX(I)
```

```
                WRITE(7,'(F9.1)')ZMAX(I)
                ZMAX(I)=TP*ZMAX(I)
        END DO
        CLOSE(10)
        CLOSE(7)
* LAMDA IS ONE DEBYE LENGTH
        LAMDA=((KT*4.15E25/NA)**0.5)*10000
        H1=T/LAMDA
        H2=(T+D1)/LAMDA
        L=(T+D1+D2)/LAMDA
        DO=H1/(N1-1)
        DOR=T/(N1-1)
        DN=(H2-H1)/(N2-N1)
        DNR=D1/(N2-N1)
        DP=(L-H2)/(N3-N2)
        DPR=D2/(N3-N2)
        DP2=DP*DP
        DN2=DN*DN
        Z=ZMAX(1)
*  NOW TO SET UP THE MATRICES
50      DO I=1,N3
                DO J=1,N3
                        A(I,J)=0
                        AI(I,J)=0
                END DO
                V(I)=0
                Q(I)=0
        END DO
* NOW TO SET UP THE X ARRAY
        X(1)=-T
        DO I=2,N1
                X(I)=X(I-1)+DOR
        END DO
        DO I=N1+1,N2
                X(I)=X(I-1)+DNR
        END DO
        DO I=N2+1,N3
                X(I)=X(I-1)+DPR
        END DO
* NOW SET UP THE A MATRIX
        A(1,1)=1
        A(N3,N3)=1
        DO I=2,N3-1
                A(I,I-1)=1
                A(I,I)=-2
                A(I,I+1)=1
        END DO
        A(N1,N1-1)=-2*DN/DO
        A(N1,N1)=11+2*DN/DO
        A(N1,N1+1)=-18
        A(N1,N1+2)=9
        A(N1,N1+3)=-2
        A(N2,N2-3)=-2/DN
        A(N2,N2-2)=9/DN
        A(N2,N2-1)=-18/DN
        A(N2,N2)=11*(1/DN+1/DP)
        A(N2,N2+1)=-18/DP
        A(N2,N2+2)=9/DP
        A(N2,N2+3)=-2/DP
*  NOW INVERT THIS MATRIX
        CALL INVMAT(A,AI,INDX,N,N3)
*  WE CAN NOW START THE ITERATIVE SOLUTION OF V *  W
*  SET TO 0.5 SO ITERATIONS ARE UNDERRELAXED
```

```
      W=0.5
100   CONTINUE
* THIS IS NOW THE LOOP THROUGH ALL V(I)S
* V() IS THE SOLUTION SET AND GIVEN IN THERMAL VOLTS
      R=0
      DO J=1,N3
            CALL CALRHO(J,V(J),RHO,Z,N1,N2,N3,DN2,DP2,S,VG,M)
            RSTORE(J)=RHO
      END DO
      DO I=1,N3
            S1=0
            S2=0
            DO J=1,I-1
                  S1=S1+AI(I,J)*RSTORE(J)
            END DO
            DO J=I+1,N3-1
                  S2=S2+AI(I,J)*RSTORE(J)
            END DO
            CALL RTSOL(I,V(I),0.1,ANS,AI,N,S1,S2,N1,N2,N3,DN2,DP2,Z,S,VG,M)
            NEWV=V(I)+W*(ANS-V(I))
* R IS THE RESIDUAL
            R=R+DABS(NEWV-V(I))
* UPDATE V(I)
            V(I)=NEWV
            CALL CALRHO(I,V(I),RHO,Z,N1,N2,N3,DN2,DP2,S,VG,M)
            RSTORE(I)=RHO
      END DO
* IF THE RESIDUAL IS LESS THAN 10 THEN START TO OVER RELAX THE ITERATIONS
      IF(R.LT.10)W=1
* IF THE RESIDUAL IS GREATER THAN ACC THEN CONTINUE WITH THE ITERATIONS
      IF(R.GT.ACC)GOTO 100
* IF WE HAVE REACHED A Z WE ARE INTERESTED IN,
* CALCULATE THE CHARGE DENSITY AND PRINT OUT THE RESULTS
      IF(Z.GE.ZMAX(CNT-48))THEN
*     CALCULATE THE CHARGE DISTRIBUTION
            CALL CHGDIS(Z,V,N,N1,N2,N3,Q,QQ,DP,DN,M,QMAX)
*     Q IS THE CHARGE DENSITY DISTRIBUTION, NORMALISED TO
*     DOPING DENSITY OF SUBSTRATE
*     QQ IS THE INTEGRATED CHARGE DENSITY DISTRIBUTION
*     MAKE A NEW NAME FOR THE OUTPUT FILE
            FILEV=POTENT//CHAR(CNT)
            OPEN(9,STATUS='UNKNOWN',FILE=FILEV)
*     WRITE THE OUTPUT FILES BUT MUST CONVERT V TO VOLTS
*     AND Q INTO CHARGE DENSITY (CM^-3)
            VMAX=0
            DO I=1,N3
                  WRITE(9,*)X(I),TP*V(I)*8.614E-5*TEMP,Q(I)*NA
                  IF(DABS(V(I)).GT.VMAX)VMAX=DABS(V(I))
            END DO
*     CONVERT QQ TO NUMBER OF HOLES PER MICRON^2
*     LAMDA IN MICRONS AND ND IN CM^-3

            QQ=QQ*NA*LAMDA*1E-12
            WRITE(9,*)TP*Z,QQ,VMAX
            WRITE(8,*)QQ,QMAX*NA
            CLOSE(9)
*     WRITE TO SCREEN WHERE WE ARE AT
            WRITE(6,99)FILEV,'VMAX =',VMAX,' Q =',QQ
 99         FORMAT(A32,A7,F7.1,A4,F7.1)
*     HAVE WE ANY MORE ZS WE ARE INTERESTED IN
            IF((CNT-48).GE.NUM)GOTO 1000
            CNT=CNT+1
      END IF
```

```
      DZ=DABS(Z-ZMAX(CNT-48))
      IF(DZ.GT.10.00)DZ=10.000
      Z=Z+DZ
      GOTO 100
200   CONTINUE
1000  CLOSE(8)
      END
*************************************************************************
      SUBROUTINE CHGDIS(Z,V,N,N1,N2,N3,Q,QQ,DP,DN,M,QMAX)
* SUBROUTINE TO CALCULATE THE CHARGE DISTRIBUSTION
      DOUBLE PRECISION V(N),Q(N),Z,QQ,DP,DN,M,QMAX,GRAD
      INTEGER N1,N2,N3
      QQ=0
      QMAX=0
      DO I = N1,N3
            Q(I)=M*EXP(Z-V(I))
            IF(Q(I).GT.QMAX)QMAX=Q(I)
      END DO
      DO I = N1,N2-1
            QQ=QQ+DN*(Q(I)+Q(I+1))/2
      END DO
      IF(Q(N2).GT.1.)THEN
            GRAD=(Q(N2-1)-Q(N2))/DN
            QQ=QQ+(Q(N2)**2)/(2*GRAD)
      ENDIF
      RETURN
      END

      SUBROUTINE CALRHO(J,VIN,RHO,Z,N1,N2,N3,DN2,DP2,S,VG,M)
* SUBROUTINE TO CALCULATE RHO IN THE VARIOUS REGIONS
      DOUBLE PRECISION RHO,VIN,Z,DN2,DP2,S,VG,M
      IF(J.EQ.1)THEN
            RHO=VG
            RETURN
      ENDIF
      IF(J.LE.N1.OR.J.EQ.N2.OR.J.EQ.N3)THEN
            RHO=0
            RETURN
      ENDIF
      IF(J.GT.N1.AND.J.LT.N2)THEN
            RHO=(S-M*DEXP(Z-VIN))*DN2
            RETURN
      ENDIF
      IF(J.GT.N2)THEN
            RHO=(EXP(VIN)-1-M*DEXP(Z-VIN))*DP2
            RETURN
      ENDIF
      END

      SUBROUTINE FD(RT,F,DF,AI,N,I,S1,S2,N1,N2,N3,DN2,DP2,Z,S,VG,M)
* SUBROUTINE TO RETURN THE FUNCTION AND DERIVITIVE OF THE FUNCION THAT
* IS TO BE SOLVED
      DOUBLE PRECISION AI(N,N),RT,F,DF,S1,S2,DN2,DP2,Z,RHO,S,VG,M
      CALL CALRHO(I,RT,RHO,Z,N1,N2,N3,DN2,DP2,S,VG,M)
      F=RT-S1-S2-AI(I,I)*RHO
* MUST FIND OUT WHAT SECTION OF THE DEVICE WE ARE DEALING WITH
      IF(I.EQ.1)DF=1
      IF(I.EQ.N1.OR.I.EQ.N2.OR.I.EQ.N3)DF=1
      IF(I.GT.N1.AND.I.LT.N2)THEN
            DF=1-AI(I,I)*DN2*M*EXP(Z-RT)
      ENDIF
      IF(I.GT.N2.AND.I.LT.N3)THEN
            DF=1-AI(I,I)*DP2*(EXP(RT)+M*EXP(Z-RT))
```

```
      ENDIF
      RETURN
      END

      SUBROUTINE RTSOL(I,VIN,ACC,ANS,AI,N,S1,S2,N1,N2,N3,DN2,DP2,Z,S,VG,M)
* NEWTON RAPHSON SOLUTION TO THE TRANSENDENTAL EQUATION
      PARAMETER(JMAX=1000)
      DOUBLE PRECISION ANS,AI(N,N),RTNEWT,F,DF,S1,S2,DN2,DP2,Z,S,VG,M
      RTNEWT=VIN
      DO 11 J=1,JMAX
* GET THE VALUE OF THE TRANSENDENTAL EQUATION AND ITS DERIVATIVE
            CALL FD(RTNEWT,F,DF,AI,N,I,S1,S2,N1,N2,N3,DN2,DP2,Z,S,VG,M)
            DX=F/DF
* CALCULATE THE NEW VALUE OF VIN
            RTNEWT=RTNEWT-DX
            ANS=RTNEWT
            IF(ABS(DX).LT.ACC)RETURN
11    CONTINUE
      WRITE(6,*)'EXCEEDED MAX ITERATIONS'
      END

      SUBROUTINE INVMAT(A,Y,INDX,NP,N)
*  THIS SUBROUTINE CALCULATES THE INVERSE OF AN NP BY NP DOUBLE PRECISION
*  MATRIX A WHICH IS DESTROYED.  THE ANSWER IS HELD IN Y.
      DOUBLE PRECISION A(NP,NP),Y(NP,NP)
      DIMENSION INDX(NP)
      DO 12 I=1,N
            DO 11 J=1,N
                  Y(I,J)=0
11          CONTINUE
            Y(I,I)=1
12    CONTINUE
      CALL LUDCMP(A,N,NP,INDX,D)
      DO 13 J=1,NP
            CALL LUBKSB(A,N,NP,INDX,Y(1,J))
13    CONTINUE
      END

      SUBROUTINE LUDCMP(A,N,NP,INDX,D)
      PARAMETER  (NMAX=150,TINY=1.0E-30)
      DOUBLE PRECISION A(NP,NP),VV(NMAX),D,AAMAX,SUM,DUM
      INTEGER INDX(NP)
      D=1.
      DO 12 I=1,N
            AAMAX=0
            DO 11 J=1,N
                  IF(ABS(A(I,J)).GT.AAMAX)AAMAX=DABS(A(I,J))
11          CONTINUE
            IF(AAMAX.EQ.0.) PAUSE 'SINGULAR MATRIX'
            VV(I)=1./AAMAX
12    CONTINUE
      DO 19 J=1,N
            DO 14 I=1,J-1
                  SUM=A(I,J)
                  DO 13 K=1,I-1
                        SUM=SUM-A(I,K)*A(K,J)
13                CONTINUE
                  A(I,J)=SUM
14          CONTINUE
            AAMAX=0.0
            DO 16 I=J,N
                  SUM=A(I,J)
                  DO 15 K=1,J-1
```

```
                        SUM=SUM-A(I,K)*A(K,J)
15                  CONTINUE
                    A(I,J)=SUM
                    DUM=VV(I)*DABS(SUM)
                    IF (DUM.GE.AAMAX)THEN IMAX=I
                        AAMAX=DUM
                    ENDIF
16              CONTINUE
                IF(J.NE.IMAX)THEN
                    DO 17 K=1,N
                        DUM=A(IMAX,K)
                        A(IMAX,K)=A(J,K)
                        A(J,K)=DUM
17                  CONTINUE
                    D=-D
                    VV(IMAX)=VV(J)
                ENDIF
                INDX(J)=IMAX
                IF(A(J,J).EQ.0.)A(J,J)=TINY
                IF(J.NE.N)THEN
                    DUM=1./A(J,J)
                    DO 18 I=J+1,N A(I,J)=A(I,J)*DUM
18                  CONTINUE
                ENDIF
19      CONTINUE
        RETURN
        END

SUBROUTINE LUBKSB(A,N,NP,INDX,B)
        DOUBLE PRECISION A(NP,NP),B(NP),SUM
        INTEGER INDX(NP)
        II=0
        DO 12 I=1,N
                LL=INDX(I)
                SUM=B(LL)
                B(LL)=B(I)
                IF(II.NE.0)THEN
                    DO 11 J=II,I-1 SUM=SUM-A(I,J)*B(J)
11                  CONTINUE
                ELSE IF (SUM.NE.0.)THEN
                    II=I
                ENDIF
                B(I)=SUM
12      CONTINUE
        DO 14 I=N,1,-1
                SUM=B(I)
                IF(I.LT.N)THEN
                    DO 13 J=I+1,N
                        SUM=SUM-A(I,J)*B(J)
13                  CONTINUE
                ENDIF
                B(I)=SUM/A(I,I)
14      CONTINUE
        RETURN
        END
```

Set Up File For CHADEN.

```
 KENT            file name for results
N               Channel type (N or P)
1.E16           Implantation density (cm^-3)
5.E14           Substrate density (cm^-3)
0.2             Oxide thickness (microns)
```

1.	Implantation depth (microns)
20.	Substrate layer thickness (microns) or point at which V=0
4	N1
40	N2
60	N3
300.0	Temperature
4.	Gate voltage
0.0001	Accuracy
9	Number of curves
2000.	ρ_o for no charge
1258.	ρ_o for increasing charge
1100.	"
1020.	"
920.	"
785.	"
605.	"
460.	"
390.	"
	"

References for appendix 1

1) W.H. Kent, "Charge distribution in buried channel charge coupled devices", Bell Syst. Tech. J., 52, 1009-1024, 1973.

2) M.J. Howes and D.V. Morgan, "Charge coupled devices and systems", Published by John Wiley and Sons, 1980.