Uncertainty of Calibration Standards for On-wafer Measurements over 110 GHz

Chong Li[a,c], Chen Liu[a,b], Aihua Wu[a,b], Nick Ridler[a]

[a]National Physical Laboratory, Hampton Road, Teddington, Middlesex, TW11 0LW, UK
[b]Hebei Semiconductor Research Institute, Hezuo Road, Shijizhuang, China
[c] now with University of Glasgow, University Avenue, Glasgow, G12 8LT, UK

Chong.Li@Glasgow.ac.uk

Abstract

We present preliminary results on uncertainty analysis on calibration standards for on-wafer S-parameter measurements over 110 GHz. At these frequencies, manufacturing tolerance is comparable to the sizes of calibration standards. Thus accurate knowledge about the actual dimensions of calibration standards becomes critical for definition of standard models and estimating uncertainty of the measurement results. In this work, we use three dimensional measurement tools namely surfaceprofiler, optical interferometer, and Scanning Electron Microscope (SEM) to characterise calibration standards on commercial calibration substrates. Numerical software was also used to investigate the effect of manufacturing tolerance on electrical parameters and finally uncertainty of definition of the calibration standards was anlaysed.

I. Background

The definition of calibration standards is important for calibrating a vector network analyser (VNA) and measuring the S-parameters of a device-under-test (DUT). As shown in Fig.1 the uncertainty of standard definition is one of the three uncertainty sources of the system calibration and affect the total uncertainty of the measurement [1].

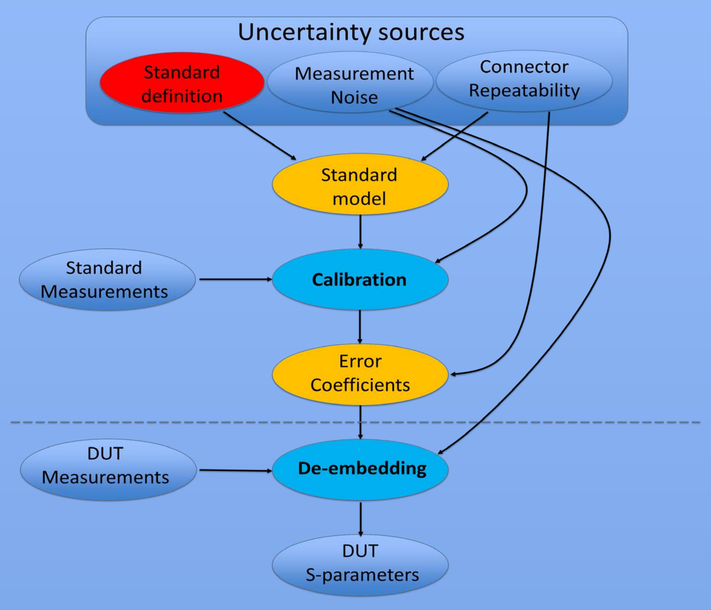

Fig. 1 Uncertainty propagations for S-parameter measurements

II. Standards for On-wafer Calibrations

Typical calibration standards used for on-wafer measurements include short, open, load, thru and (or) line. Fig. 2 shows some examples from two commercial calibration substrates for application over 110 GHz. The uncertainty contributors for each type of the standards are listed in Table I [2]. All contribution factors are directly or indirectly related to their dimensions. For example, the thickness of conductor affects losses and parasitic inductance. The width of signal conductor and gap width affects characteristic impedance, line delay, and parasitic inductance. Therefore, manufacturing tolerances affect the uncertainty of the definition of standard models.

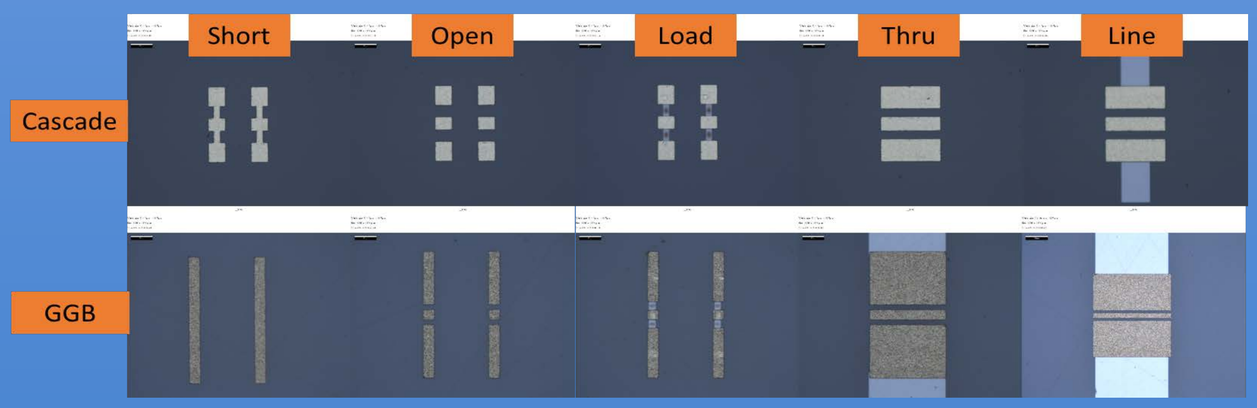

Fig. 2 Optical images of commercial calibration standards for applications above 110 GHz from two manufacturers namely Cascade and GGB.

Table I Contribution factors to commonly used calibration standards

	Short	Open	Load	Thru	Line	Comments
Delay (τ)	Y	Y	Y	Y	Y	Delay line length
Characteristic Impedance (Zc)	Y	Y	Y	Y	Y	Line characteristic impedance
Losses (L)				Y	Y	
Parasitic inductances (Ln)	Y	Y	Y			Including higher order modes
Parasitic resistances (R)	Y	Y	Y			R_{series} and R_{shunt}

III. Characterisations and Simulations

Three different tools namely optical interferometer, scanning electron microscope (SEM) and surfaceprofiler, have been used to characterise the dimensions of the calibration standards.

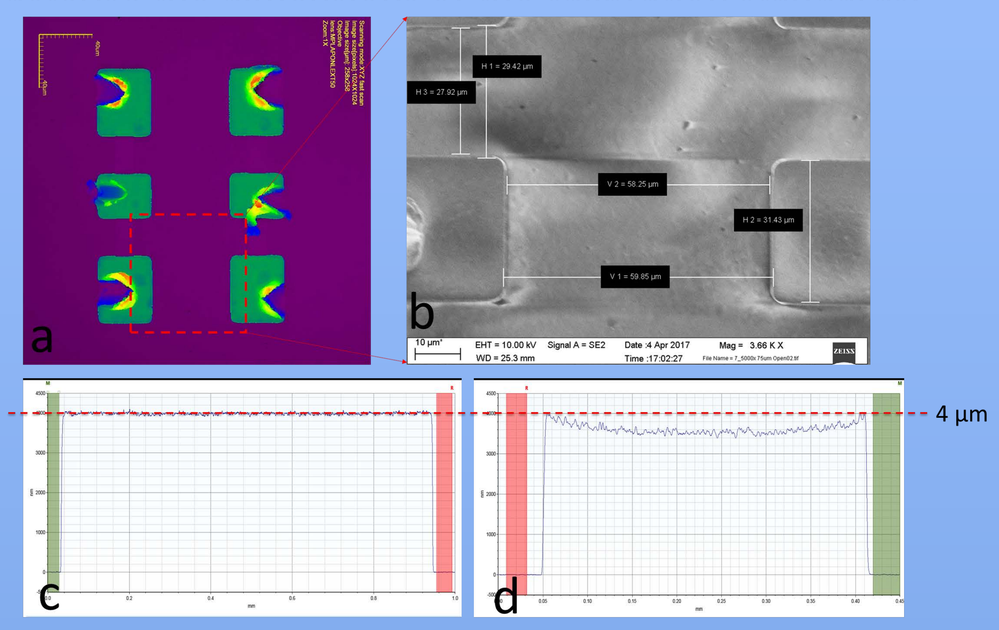

Fig. 3 Illustration of Cascade's opens measured using optical interferometric technique (a), SEM technique (b), and measurement results of a line on Cascade's substrate (c) and a line on GGB's substrate (d).

IV. Results and Future work

Measurement results indicate the conductors have up-to 1.5% variation laterally for both substrates and 15% and 25% variation vertically i.e. the thickness for Cascade and GGB, respectively. Numerical simulation (Fig.4) using CST shows the lateral variation leads to 1.2% change on Zc. The variation in thickness leads to 2% and 3% change on attenuation constant at 220 GHz for Cascade and GGB, respectively [4].

Future work will focus on putting all contribution factors into the definitions of the calibration standards and then implement an uncertainly analysis for S-parameters of a DUT.

Table II Measured thicknesses of the conductor and the resistors on both substrates

		Conductor	Resistors
Cascade	Nominal	4 µm	60 nm
	Measured	3.5 µm - 4.1 µm	50 nm- 70 nm
GGB	Nominal	4 µm	60 nm
	Measured	3.4 µm - 4.4 µm	50 nm- 70 nm

$$L = (L0) + (L1 \times F) + (L2 \times F^2) + (L3 \times F^3)$$

$$C = (C0) + (C1 \times F) + (C2 \times F^2) + (C3 \times F^3)$$

$$\text{Loss}\left(\frac{\Omega}{s}\right) = \frac{\text{loss (dB)} \times Z_0(\Omega)}{4.3429(\text{dB}) \times \text{delay(s)}}$$

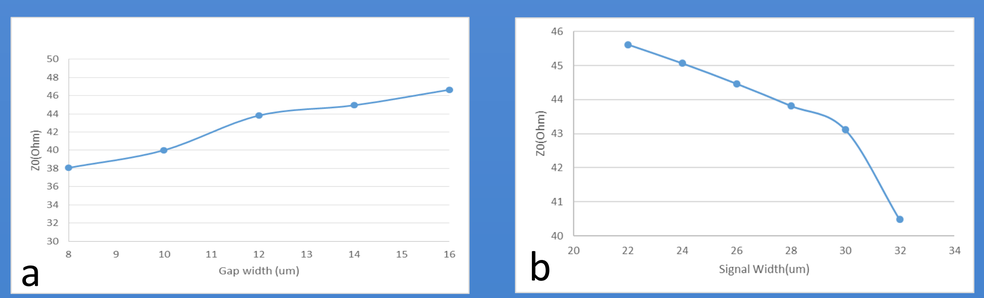

Fig. 4 Numerical simulation on the characteristic impedance of CPW lines as changes of gap (a) and signal (b) width at frequency of 220 GHz.

Reference

1. A. Ferrero and M. Garelli, "A unified theory for S-parameter uncertainty evaluation," IEEE Trans. Microw. Theory Tech., vol. 60, no. 12, pp. 3844–3855, Dec. 2012.
2. V. Teppati et al., "Accuracy of microwave transistor f_T and f_{MAX} extractions," IEEE Trans. Electron Devices, vol. 61, no. 4, pp. 984–999, Apr. 2014.
3. R. N. Simon, "Coplanar waveguide, circuits, components, and systems, " Ch8, Wiley-IEEE Press, April 2001.