Active Filters: A Unified Approach

A thesis submitted for the degree of Doctor of Philosophy

by

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Dedicated to

my wife Fariba, my children Nasim and Reza, my mother and my late father

with love and respect

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ABSTRACT

The increase in the occurrence of non-linear loads in power systems has caused considerable concern to power utilities and manufacturers of power electronics equipment. To alleviate the problems caused by generation of current harmonics, there has been considerable interest in the use of active filters. This thesis presents a unified approach to the design of active filter configurations. It is shown that this approach offers a systematic method of classifying existing structures and it can be used for developing new circuits.

CONTENTS

Symbols and Abbreviations

Symbols

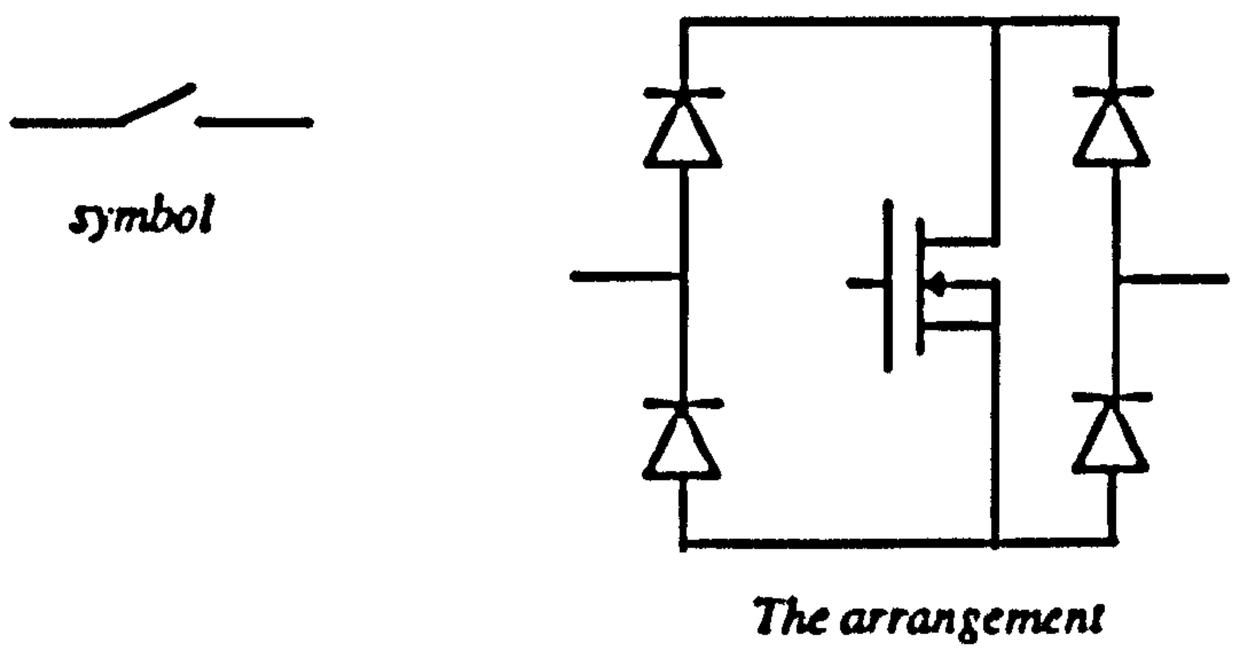
Lower and upper case symbols are used to represent instantaneous and rms quantities, respectively. Peak values are represented by upper case symbols with ' ^ '. Subscripts i, dc, f, and l indicate quantities related to the ac input supply, dc supply, filter and load respectively. Subscripts n = 1, 2, 3, . . . and dis denote the harmonics and the total distortion component, respectively.

C	capacitance, F
L	inductance, H
R	resistance, Ω
V and v	voltage, volt
I and i	current, amp
P_{av}	average power, W
S	apparent power, VA
η	efficiency

θ	is the angle by which the supply current lags supply voltage
μ	distortion factors that equals to I_{i1}/I_i
COS θ_i	displacement factor
f	frequencey, hertz
ω	$2\pi f$, radian /sec

The symbols and arrangements that are used for unidirectional and bi-directional switches are shown in the following Figures.

The unidirectional switch



The bi-directional switch

Abbreviations

MOSFET	metal-oxide-semiconductor field effect transistor
THD	total harmonic distortion

PF	power factor
SW	switch

CHAPTER ONE

Introduction

This introductory chapter is concerned with three aspects of this investigation: (a) the background information relating to the problems being investigated and the objectives of this research, (b) the historical perspective and the review of published work and (c) the outline of the author's contribution and achievements.

1.1 Background Information and Objectives

1.1.1 Background Information

In recent years there has been a considerable growth in the use of non-linear and time-varying loads such as large industrial static converters down to power supplies for small domestic electronic devices. High efficiency, compact size and ease of control, coupled with the ever decreasing cost of power electronics and associated technologies, makes the use of these circuits very attractive for all power conditioning applications.

There are however a number of serious drawbacks associated with power electronics circuits; the most serious being the tendency to draw non-sinusoidal current from the supply. This distortion of the supply current results in degradation of the power factor and if the level of current harmonics is high, they interact with the network impedance causing voltage distortion.

Harmonics can also cause problems in a variety of other ways. One of the most destructive and costly of these, is through resonance between power factor correction capacitors and system inductance. This resonance can lead to large currents and the possible degradation of capacitors, which in turn could lead to catastrophic breakdown.

Furthermore, the harmonics which are injected back into the mains supply can interfere with other consumers connected to the supply. Power converters are also responsible for the generation of RFI and EMI [Arrilaga 85].

Power systems as a whole are also affected by harmonics through increased losses in transmission equipment, eddy currents in transformer and motor laminations, as well as harmonic torque in ac machines [Arrillaga 85].

Nonlinear and time-varying loads are classified into identifiable and unidentifiable loads, depending on whether they are easy to detect at the point of connection. Large capacity diodes or thyristor rectifiers, cycloconverters installed by high and medium-voltage consumers are typical identifiable harmonic-producing loads. On the other hand, single-phase diode rectifiers with capacitive smoothing are representative of unidentified loads. Examples of these are TV sets and personal computers. Although a single-phase diode rectifier generates a negligible amount of harmonic current, the total amount of harmonic current produced by large number of single-phase diode rectifiers has become dominant in power distribution systems [Rjoual 95, Akagi 95].

With increasing demands on the quality of supply being placed on electricity distribution utilities, it is likely that there will soon be stringent regulations regarding the amount of distortion and power factor degradation that any consumer may impose on the supply. In recent years, the quality of power supply has become an important issue and recommended harmonic limits have been published by various organizations; among them are updated IEEE519 and IEC standards [IEEE Std.519 92, IEC 90].

Generally individual low power and high power consumers are required to be responsible for limiting the current harmonics caused by power electronics equipment, while the

electric utility companies are responsible for limiting voltage harmonics at the point of common coupling in power transmission and distribution systems [Xu 94].

1.1.2 Aims and objectives

Under normal conditions, the power supply can be assumed to be a sinusoidal voltage source.

$$v_s(t) = \hat{V}_m \sin \omega t$$

A non-linear load consists of fundamental component and higher-order harmonics represented by [Hsu 96]:

$$i_L(t) = \sum_{n=1}^{\infty} \hat{I}_n \sin(n\omega t + \theta_n) \qquad (1)$$

Therefore the instantaneous load power can be expressed as

$$p_L(t) = v_s(t) i_L(t)$$

$$= \hat{I}_1 \hat{V}_m \sin^2 \omega t \cos\theta_1 + \hat{I}_1 \hat{V}_m \sin \omega t \cos \omega t \sin \theta_1 + \sum_{n=2}^{\infty} \hat{V}_m \sin \omega t \hat{I}_n \sin(n\omega t + \theta_n) \qquad (2)$$

In this equation the first term is the real power, the second term is the reactive power and the third term represents the harmonic power, i.e.

$$p_{reactive}(t) + p_{harmonic}(t) = \hat{I}_1 \hat{V}_m \sin \omega t \cos \omega t \sin \theta_1 + \sum_{n=2}^{\infty} \hat{V}_m \sin \omega t \hat{I}_n \sin(n\omega t + \theta_n) \qquad (4)$$

Because of the wide spread use of non-linear loads it is not possible to eliminate current harmonics totally from supply systems, because it is very difficult to estimate in advance the distribution and level of current harmonics in a network. For some problems , such

as interference with telecommunication systems, it is more economical to protect these systems locally [Arrillaga 85].

A more realistic objective can be to reduce the problem to an acceptable level at the point of common coupling with other consumers as recommended by harmonic standards. Many research papers and methods have been proposed to solve these problems. One approach is to use power converters, such as boost regulators, which do not generate significant current harmonics [Dakyo 95].

Use of filters, active or passive, must ensure that they do not interfere with the load requirement. This implies that series passive filters may be used, provided that they are used in conjunction with shunt filters, so that load requirements are met [Fukuda 95, Peng 93].

Figure 1.1 shows the diagram of a system used for filtering current harmonics using shunt filters. The filter is connected in parallel with the load and should operate in a manner such that the total current drawn by the filter and the load is sinusoidal.

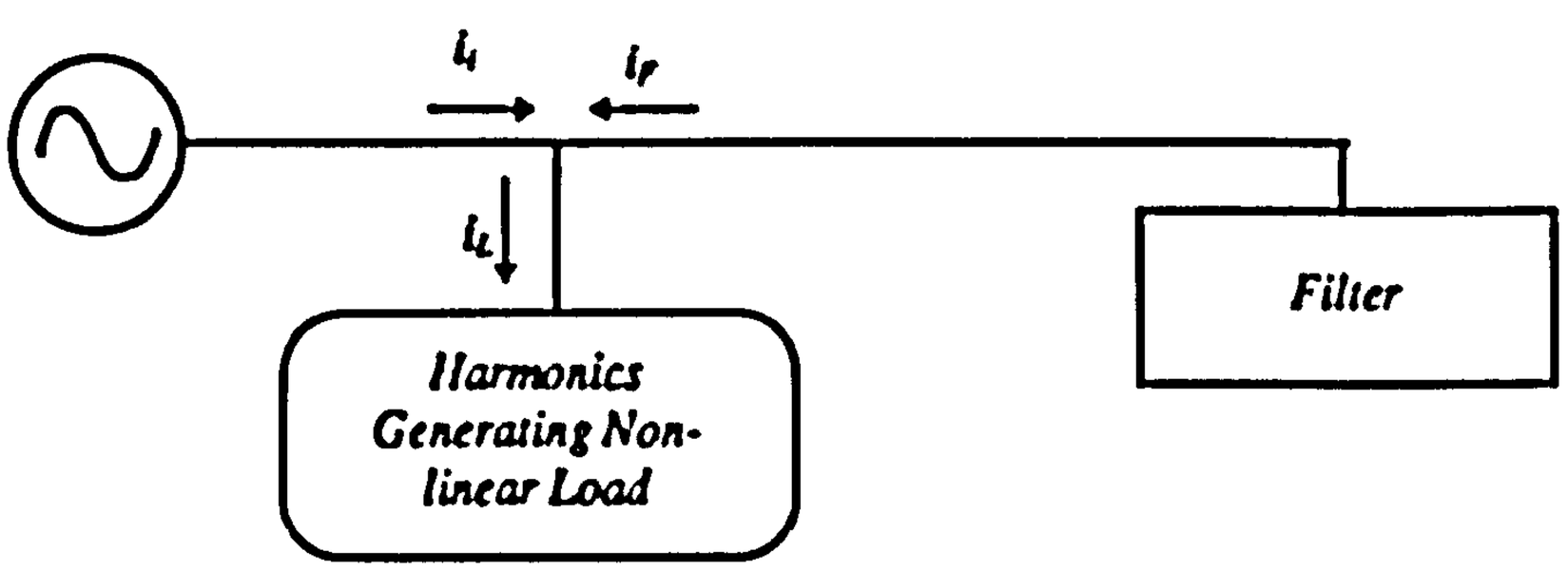


Figure 1.1 Principal of shunt filtering technique

As equations (1) and (2) show, a non-linear load requires both reactive as well as harmonic power. If ideally, a shunt filter compensates for both these powers, then the supply current would be sinusoidal and in phase with the supply voltage i.e.

$$i_1(t) = \hat{I}_1 \cos\theta_1 \sin\omega t = \hat{I}_a \sin\omega t \quad (4)$$

where $$\hat{I}_a = \hat{I}_1 \cos\theta_1 \quad (5)$$

However the supply must provide not only the real power of the load, but also the losses associated with the filters [Cavallini 94].

Passive LC filters and power capacitors have been used to attenuate the current harmonics and improve power factor conventionally. The passive filters although effective have a number of limitations. Individual filter sections are required for controlling each harmonic and therefore overall harmonic current compensation may be uneconomical. Whilst passive filters are reliable and easy to design, their performance depends on network impedance and are sensitive to supply voltage distortion. Also there is a possibility of voltage and current amplification due to parallel and series resonance phenomena [Pereira 95, Cavallini 94].

Active filtering techniques, unlike passive filters, provide flexibility such that they can cope with the variation in the filtering requirements, as the load and system conditions vary. The active filters rather than introducing resonance in the network can be used to dampen existing resonance [Le 93, Pereira 95]. Significant changes in their characteristics can be achieved just by software measures, without hardware modification, provided the filters are adequately rated. The combined topology of these

filters (series-connected) with passive filters, reduce greatly the aforementioned problems of using only passive filters [Rastogi 95, Pouliquen 95, Peng 93].

Active filters are inherently time varying structures, because they are controlled via switches and their associated switching patterns. Various configurations have been proposed in the past and in the main they employ voltage or current source inverters [Grady 90].

The active filters can be classified according to their configurations and control strategies as discussed later in this chapter.

1.2 Historical Perspective and Review of Published Work

1.2.1 Historical perspective

The harmonics in power systems, particularly harmonics caused by static converters, have been the subject of concern for many years. In 1945 a classical paper on harmonic generation by static converters was written by J.C.Read [Read 45] which was followed by a large number of papers in this topic during the 1950s and 1960s. These papers were summarised in a book by Kimbark [Kimbark 71] which contains over 60 references. Since 1975, the subject of power system harmonics has been regularly discussed at international meetings and extensive bibliographies were produced. A complete book on power system harmonics has been published by J.Arrillaga, D.A.Bradley and P.S.Bodgere in 1985 which contains the description, theory and design

of passive filters. A close examination of published work indicates that until recently only passive filtering techniques were the subjects of concern. There have been several attempts to achieve harmonic current control by other means including:

- Triple harmonic injection in 1968,1969 [Bird 69]
- Magnetic flux compensation in 1972 [Sasaki 71]
- D.C ripple injection in 1980 [Baird 80]
- Thyristorised harmonic cancellation device in 1980 [Emanuel 80]
- Switching taps of interphase reactor [Miyairi 86]
- Increasing the number of rectification pulses [Arrillaga 85]
- Boost converters [Rastogoi 94, Dakyo 95]

The last two methods are used to improve the characteristics of particular nonlinear loads in order to reduce distortion, so strictly speaking they cannot be called filtering methods. The others are filtering techniques which use active elements. Most of these methods are concerned with harmonic reduction in specific cases of static high power converters and can not be generalised. These methods are usually employed to reduce harmonics over a limited range. Some of these techniques overcome some of the limitations associated with passive filters but still have serious drawbacks.

At present a great deal of research has been devoted to the problem of harmonic elimination by active filtering methods using circuit configurations, which can be used at network level rather than for individual loads. The most recent developments in this area include the following.

- Switched capacitor techniques[Mehta 90]
- Voltage source converters [Machmoum 95, Jou 95]
- Current source converters [Hayashi 88, Fukuda 95]

A detailed study of the published papers relating to these techniques has been carried out. A brief description of these methods together with their relative merits is summarised below to identify the present trends.

1.2.2 Review of Active Filtering Methods

The active filters can be classified in a number of different ways. They can be divided into active dc and active ac types. The former has been employed to compensate for voltage or current harmonics on the dc side of power converters such as in HVDC systems [Bottino 95, Delaney 95]. However in this thesis, the emphasis is on active ac filters and the term 'active filter' is used for ac types only.

1.2.2.1 Switched-capacitor filters

The method, as shown in the Figure 1.2 and described in [Mehta 90], consists of two capacitors in parallel with two bi-directional switches in series with each capacitor. The combination is connected to the mains via an inductor. The two switches are operated in antiphase so that the current flows through them alternately. The values of the capacitors, the inductor and the pattern of switching functions define the filter characteristics.

Two strategies for control of active filters have been used in the past: analytical methods and pattern recognition techniques. In the analytical methods the switching pattern is

generated by detailed analysis of the current waveshapes. With the pattern recognition approach, the system is trained with samples of practical waveforms to identify the required switching pattern from previously learnt data. Both methods are carried out in the frequency domain and are amenable to on-line or off-line strategies.

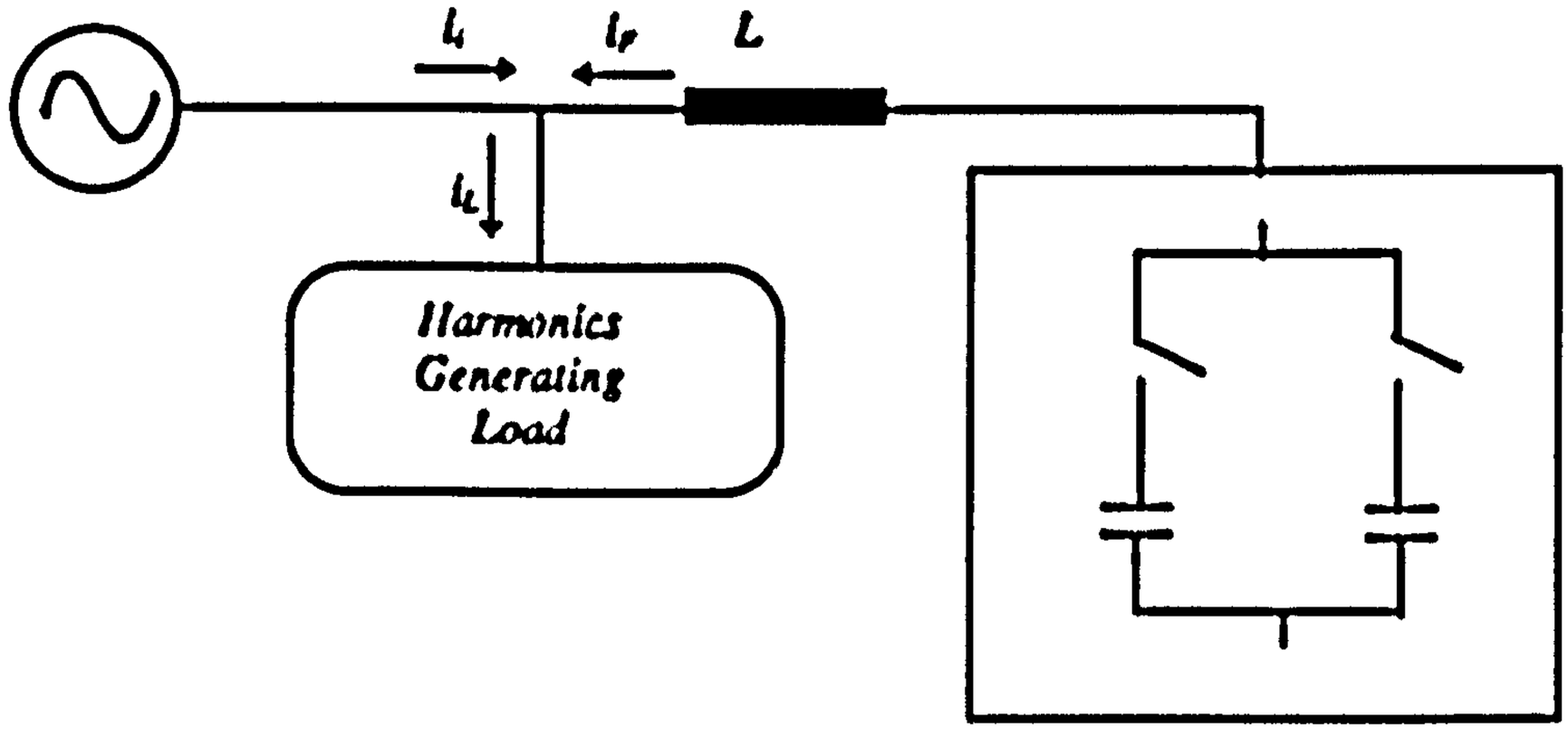


Figure 1.2 The switched capacitor filter

In this analytical method, the switching pattern and circuit parameters are optimised to minimise the difference between load current harmonics and filter current harmonics, which is called the error function. This control technique is carried out in frequency domain for off-line control, such that if the coefficients of harmonics in the load and filter currents are denoted respectively by C_n and X_n, the error function, J, which is minimised, is given by

$$J = \sum_{n=3}^{N(\max)} \sqrt{C_n^2 - X_n^2}$$

Figure 1.3 outlines a typical experimental set-up which is used in the pattern recognition method. It uses a 486, 33 MHz computer. In practice the whole system could be built on a custom chip using well established microelectronics technology

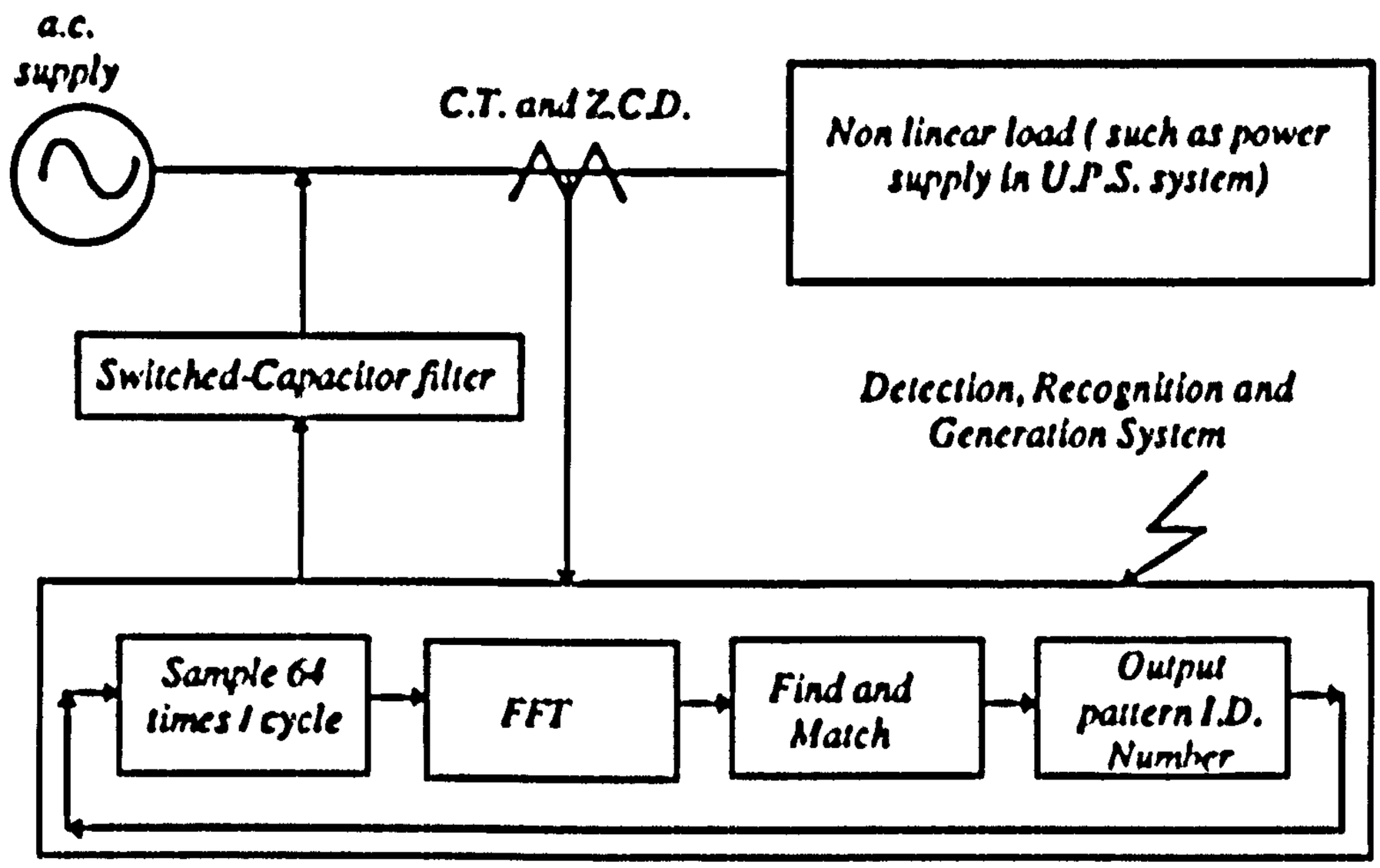


Figure 1.3 The pattern recognition method

The zero-crossing detector synchronizes the system with the mains, and the current transformer monitors the current. The 486 machine samples the waveform and via the FFT software, the frequency spectrum is determined. Using a range of loads, the system is taught predictable events (waveforms). During commissioning or actual operation of the circuit, the sampled waveform is processed, and the system finds the best appropriate match with the stored information.

In the event that the match is not accurate, it is possible to intervene, teach and update the 'knowledge-base' in the machine. It is claimed that the main benefit of this approach is that it is significantly faster, because the system does not require any time for on-line calculations. Also it is more adaptable and capable of modification in service [Darwish 93].

1.2.2.2 Voltage-source and current-source configurations

Two fundamental approaches, in conjunction with voltage-type and current-type converters, incorporating control strategies, either in time or frequency domain, have been proposed in recent publications [Sactleo 95].

The voltage-source and the current-source configurations are illustrated in Figures 1.4 and 1.5. The converters, in principle, are standard voltage-source or current-source devices where either the voltage or current on the dc side is maintained constant. In both cases, the dc source receives its power from the ac power system, either through the switching action or through a separate charging circuit [Malesani 91].

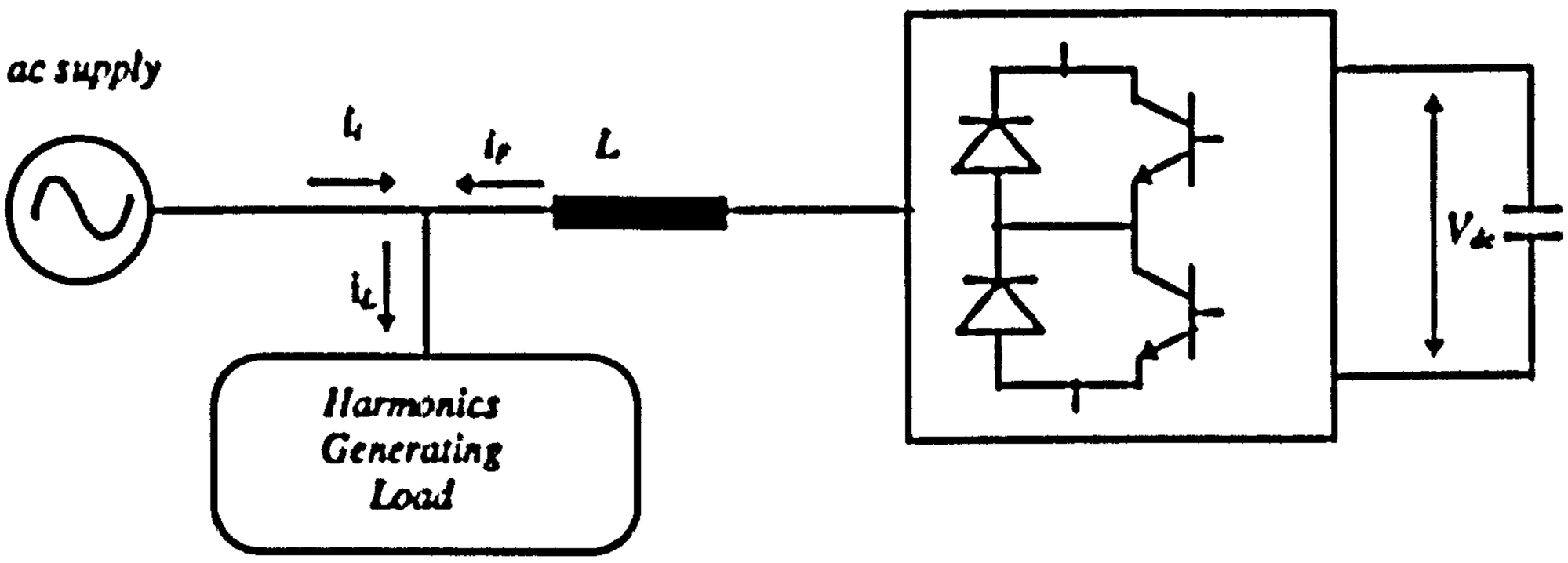


Figure 1.4 Voltage-type Active Filter

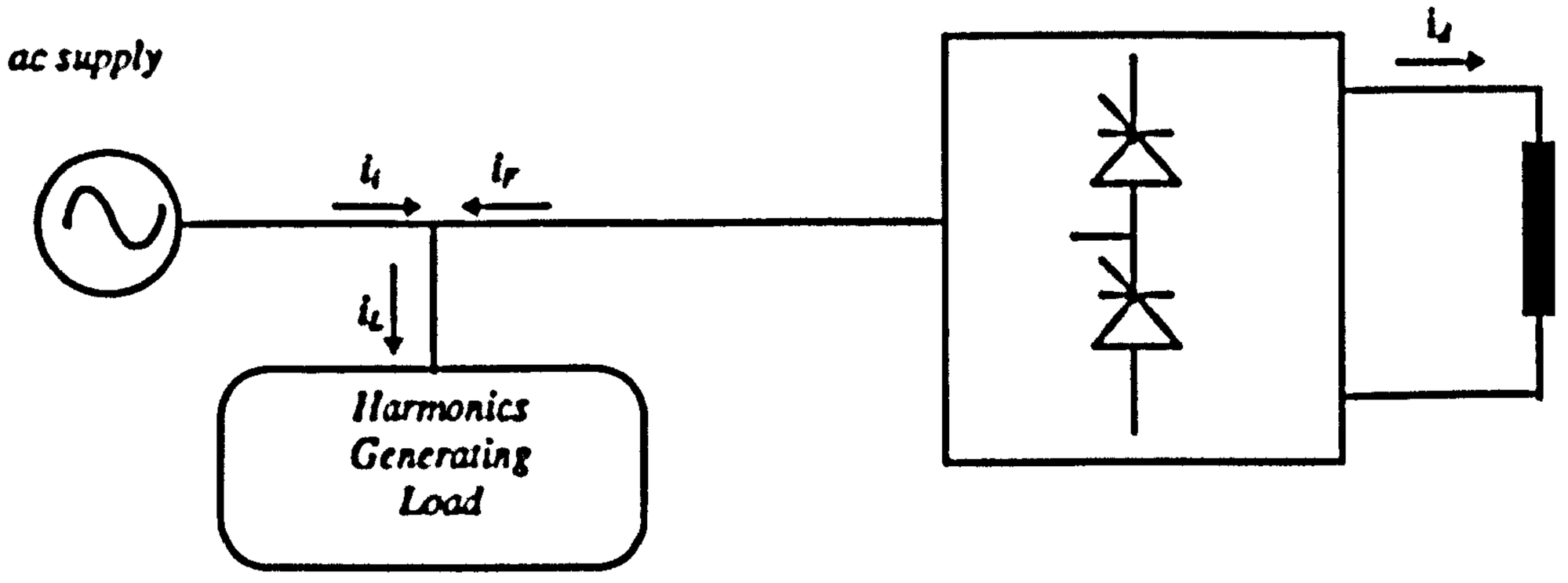


Figure 1.5 Current-type Active Filter

Some references propose that these types of active filters may be used in conjunction with conventional tuned harmonic high-pass filters. These hybrid systems offer the advantages of reduced converter size and cost [Fukuda 95]. It is not possible to identify in the literature a clear trend as to which type is preferred. The choice depends on the source of harmonic current at the specified bus, equipment cost, and amount of correction desired.

Voltage-type converters have an advantage in that they can be readily operated in parallel to increase the overall rating [Komatsugi 86]. Generally voltage-type converters are lighter and less expensive than current-type converters. The main drawback of voltage-type converters lies in the increased complexity of their control systems. For systems with several converters connected in parallel, this complexity is greatly increased.

Current-type converters are, on the other hand, claimed to be simple and more reliable Higher losses are their main drawback. Losses are less important in low-power applications but very important in high-power applications. Since voltage type converters are easily configured for parallel operation, they are likely to be used for network-wide compensation.

Current-type will continue to be popular for single-node distortion problems. In other words, electricity utility interest is likely to be focused on voltage-type converters, while industrial users will most likely use both types.

The control strategy

The control strategy in time-domain, is based on the principle of holding instantaneous voltage or current within some reasonable tolerance limits, with respect to the supply voltage. An instantaneous error function is computed 'on-line', and it is the difference between actual and reference waveforms.

Time-domain control strategy can be classified as:

- Triangular-wave
- Hysteresis

The triangular-wave method [Peng 88] is the easiest to implement. It can be used to generate either a two-state or three-state switching function. A two-state switching function consists of a dc source that can be connected either positively or negatively, as illustrated by e'(t) in Figure 1.6.

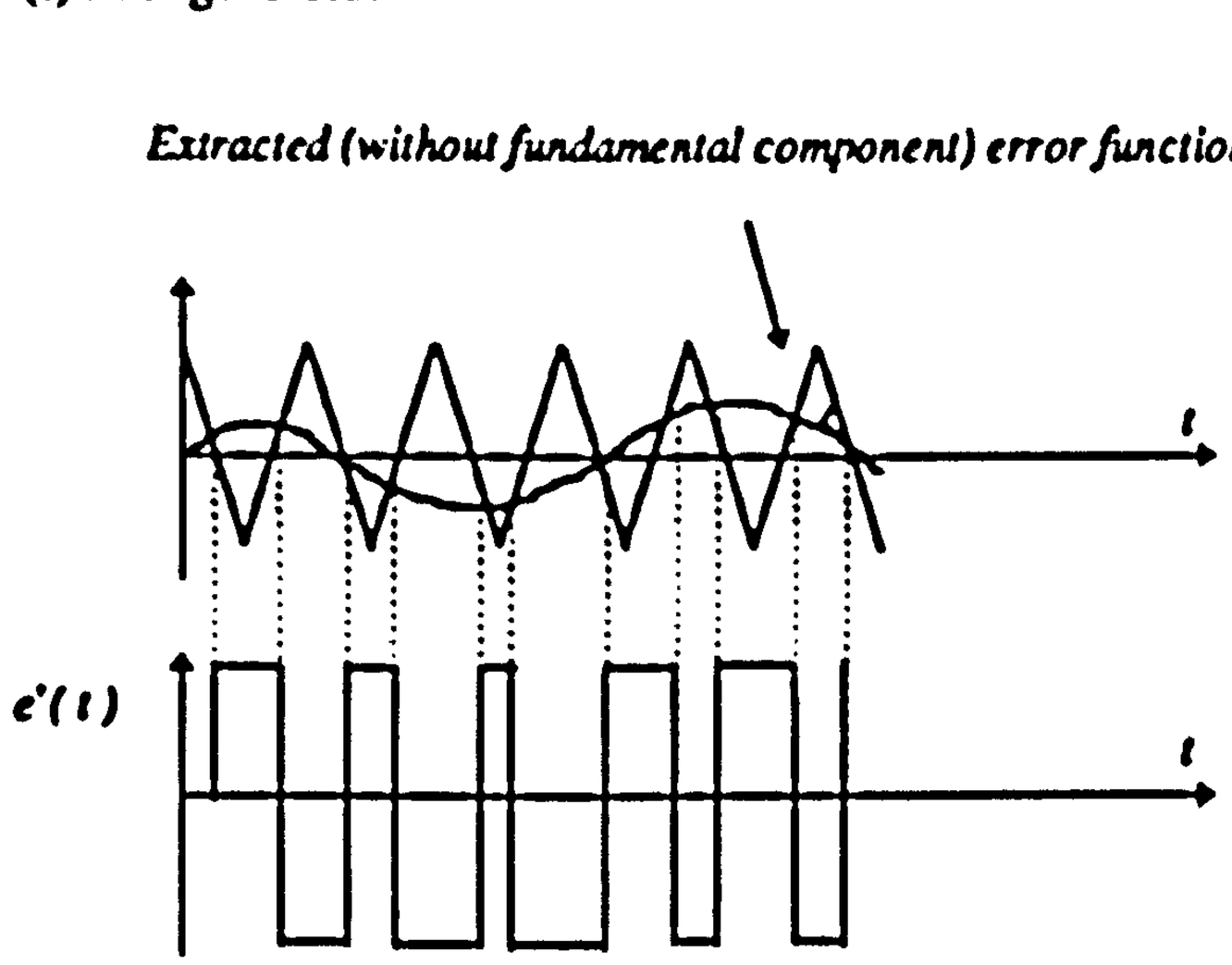


Figure 1.6 Control strategy with two states triangle-waveform method

A three-state switching function can be positive, negative, or zero (off). Therefore the inverter is always 'on', when a two-state function is used, but it can be turned off when a

three-state function is employed. For a current-source converter, the off-state corresponds to the inductor being short-circuited through a free-wheeling diode.

As shown in Figure 1.6, the extracted error function e(t) for the triangle-wave method is compared to a higher-frequency triangle carrier wave up to 50 Khz [Grady 90]. The inverter is switched each time the two curves cross, and the result is an injected signal, e'(t), that produces equal but opposite distortion. The net effect is reduction of the extracted error and compensation of distorted waveforms.

The most commonly proposed time-domain control technique is the Hysteresis method [Saetieo 95]. Preset upper and lower tolerance limits are compared to the extracted error signal. As long as the error is within the tolerance band, no switching action is taken. Switching action occurs whenever the error leaves the tolerance band. When using a two-state switching function, the inverter is always 'on'. However, when a three-state switching function is used, the inverter is 'off', as long as the error is within the tolerance band. The injected signal, e'(t), for this case is illustrated in Figure 1.7.

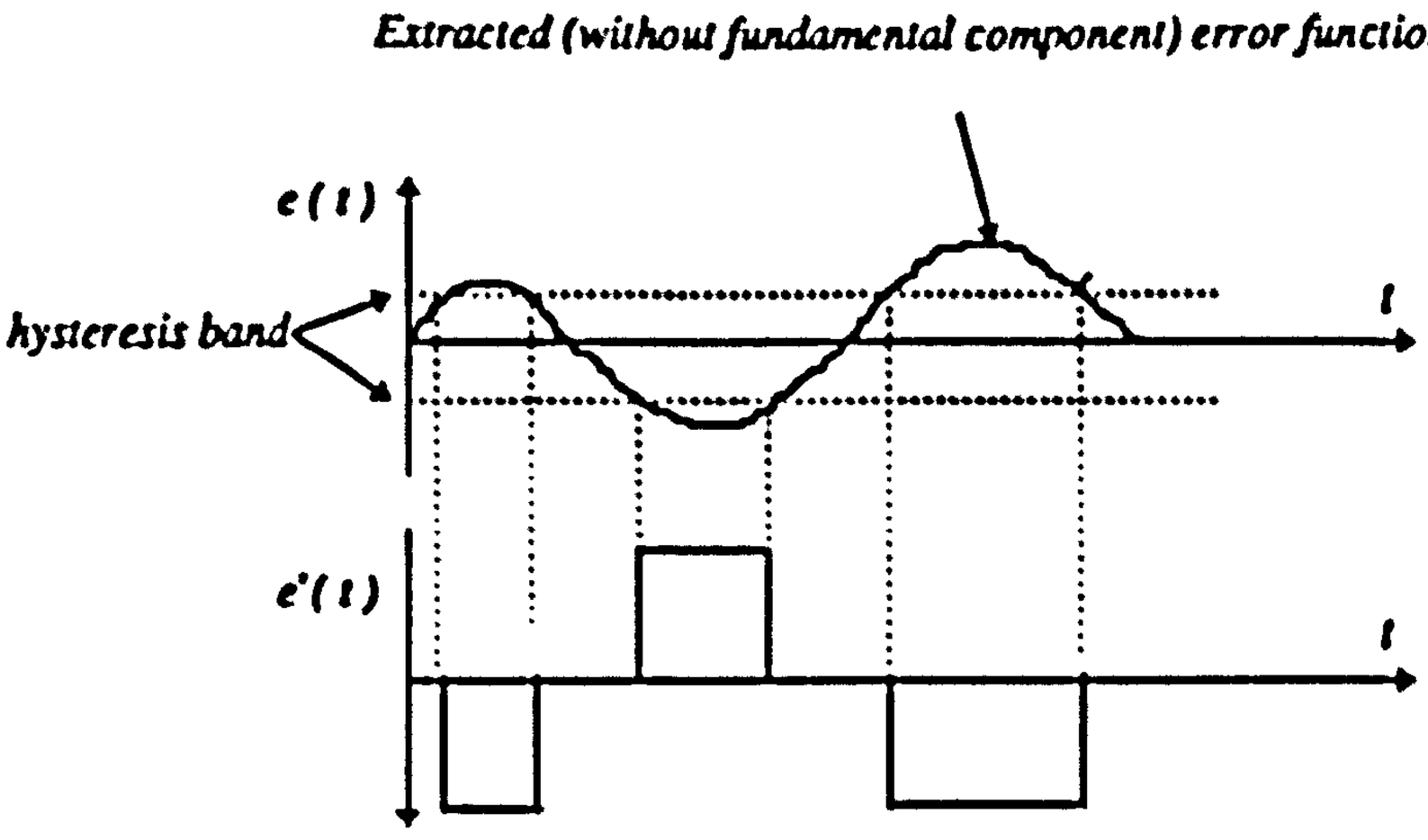


Figure 1.7 Control strategy with hysteresis

Control strategy in the frequency-domain is based on the principle of Fourier analysis and periodicity of the distorted voltage or current waveform to be corrected. The recent references [Choe 89] use Fourier transforms to determine the harmonics to be injected. Once the Fourier transform is obtained, an inverter switching function is computed to produce the distortion-cancelling output. The inverter switching frequency must be more than twice the highest compensating harmonic frequency [Choe 89].

The operating principle for frequency-domain converters is illustrated in Figure 1.8. Extracted error e (t) is obtained using a 50 Hz filter circuit. Next, the Fourier transform of e(t) is taken. Finally, a compensating switching function e'(t) is constructed by solving a set of nonlinear equations to determine the precise switching times. This can be accomplished with either two-state or three-state strategies as shown in Figure 1.9. The nonlinear equations are usually linearised about some operating point.

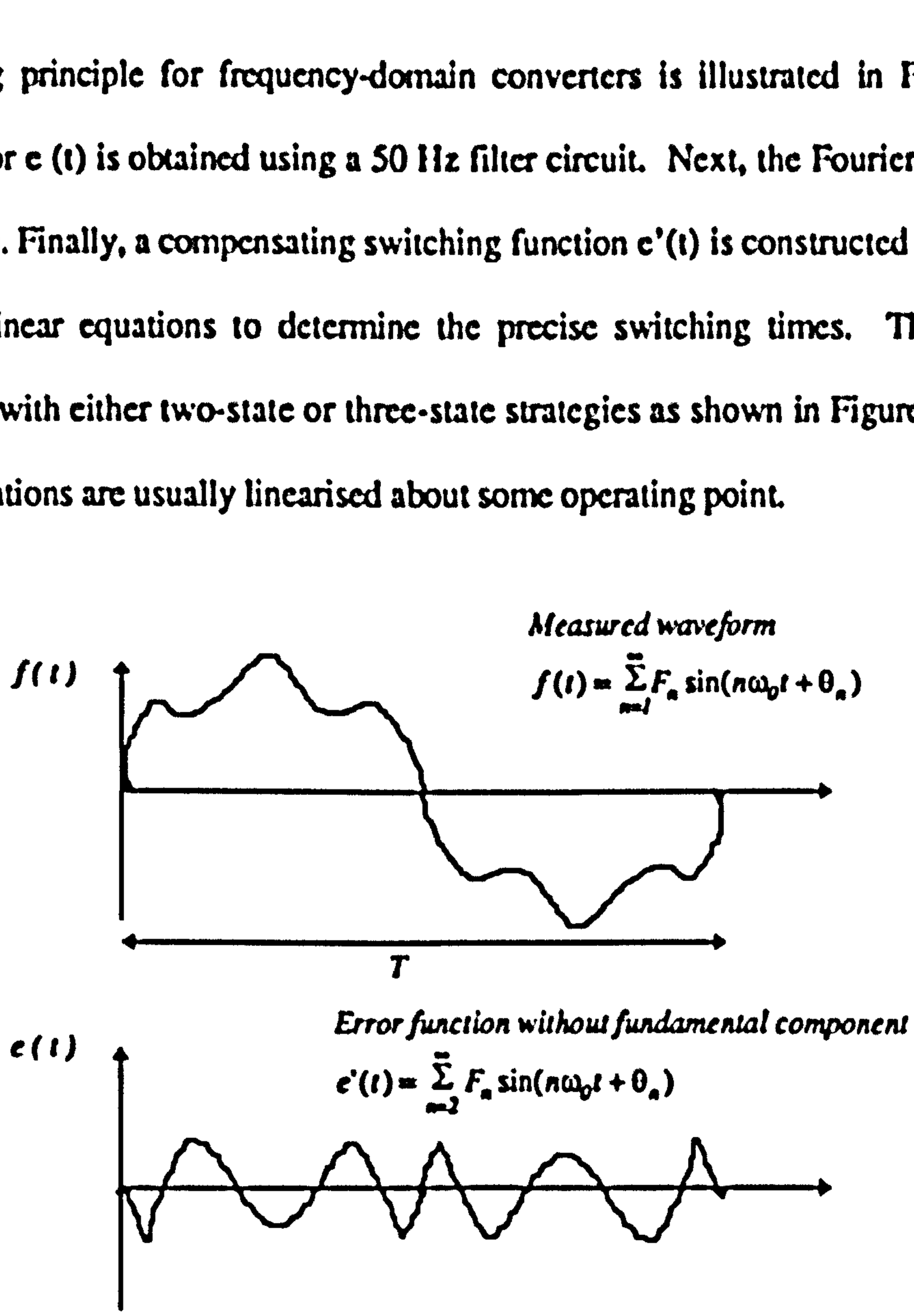


Figure 1.8 Measured waveform and extracted error signal for frequency-domain control strategy

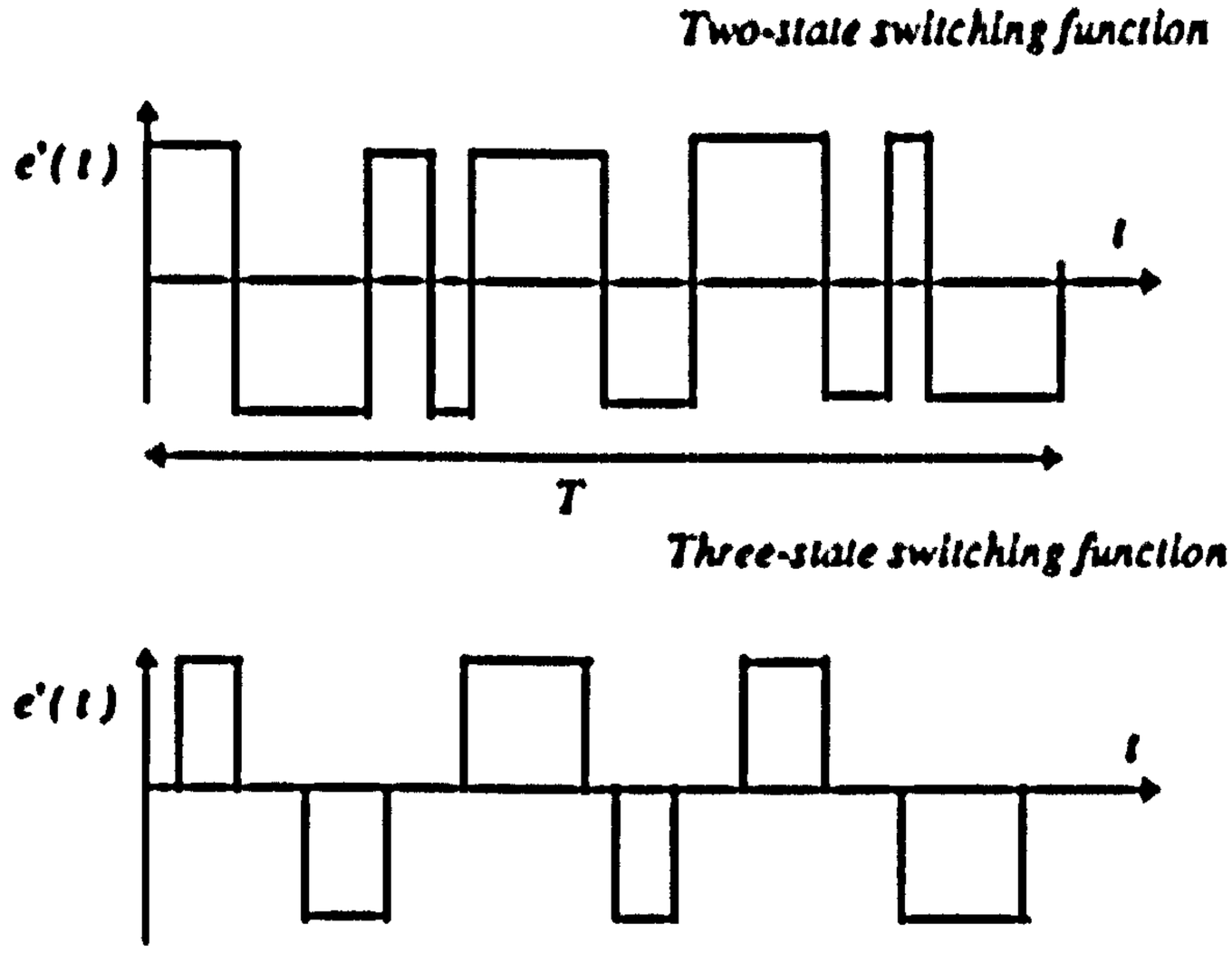


Figure 1.9 Two-state and three state switching functions in frequency-domain control strategy

The main disadvantage is that the computation time required can be very high, thereby reducing the speed of response. This time can be reduced by using expert systems.

1.3 Author's Contribution

Whilst the research into active filters extends over the past decade, it is only very recently [Akagi 95] that there has been any serious implementation of this technique. Over this period a number of different approaches have been proposed and investigated. However, there has been a lack of any coherent theoretical basis for the various techniques proposed. The author's aim was to carry out a critical survey of existing techniques and attempt to produce a generalized approach.

The author claims to have made the following contributions.

- In chapter 1 the existing active filter circuits and their control techniques are critically reviewed.
- The aim of all active filters is to match the filter current to the harmonic current drawn by non-linear loads. This is generally achieved using approximation methods which aim to generate the required waveshape of the filter current within some set boundaries. In chapter 2 the author has proposed that these approximation methods can be classified into the following categories.

  (i) continuous piecewise linear approximation

  (ii) continuous piecewise non-linear approximation

  (iii) discontinuous piecewise linear approximation

- The aim of these methods is to linearise the overall effect of non-linear loads using active filters.

- It is recognised that the control of energy flow in storage elements (L and C), particularly L, plays a key role in active filters. This fact together with the approximation techniques, is employed to propose functional diagrams which are used to classify existing circuits and develop new structures.

- Several new circuits are proposed, and simulated results are given, to identify the major characteristics of these structures.

- Chapter 3 contains the details of design of the new circuits incorporating two criteria;

  (i) optimisation based on minimisation of total current harmonic distortion.

(ii) optimisation based on minimisation of total apparent power (power factor correction and minimisation of power consumption in the filters).

- The optimisation methods together with the details of computer programs written by the author are included in the appendices.

CHAPTER TWO

Techniques for Synthesising Active Filters

This chapter focuses on the principles of this work. The design criteria of active filtering techniques are discussed and a generalised approach for synthesising active filters is developed. It is shown that the existing circuits fall within this generalised approach. The main contribution of this approach, however, is that it can be used for developing new circuits. A number of new circuits which have been developed are described, analysed and simulation results are presented.

2.1 The Principle of Active Filtering Method

Figure 2.1 shows the principle of the method used for filtering unwanted current harmonics caused by non-linear loads using shunt active filters [Cavillini 94,Akagi 95]. The active filter is connected in parallel with the load so that the total current drawn from the supply is purely sinusoidal, and ideally, the filter current should contain no fundamental component of current. This requires that the structure of the active filter should be time varying in nature such that the overall system is linear. Therefore the magnitude, the order and the phase of the individual current harmonics drawn by the filter should be controlled.

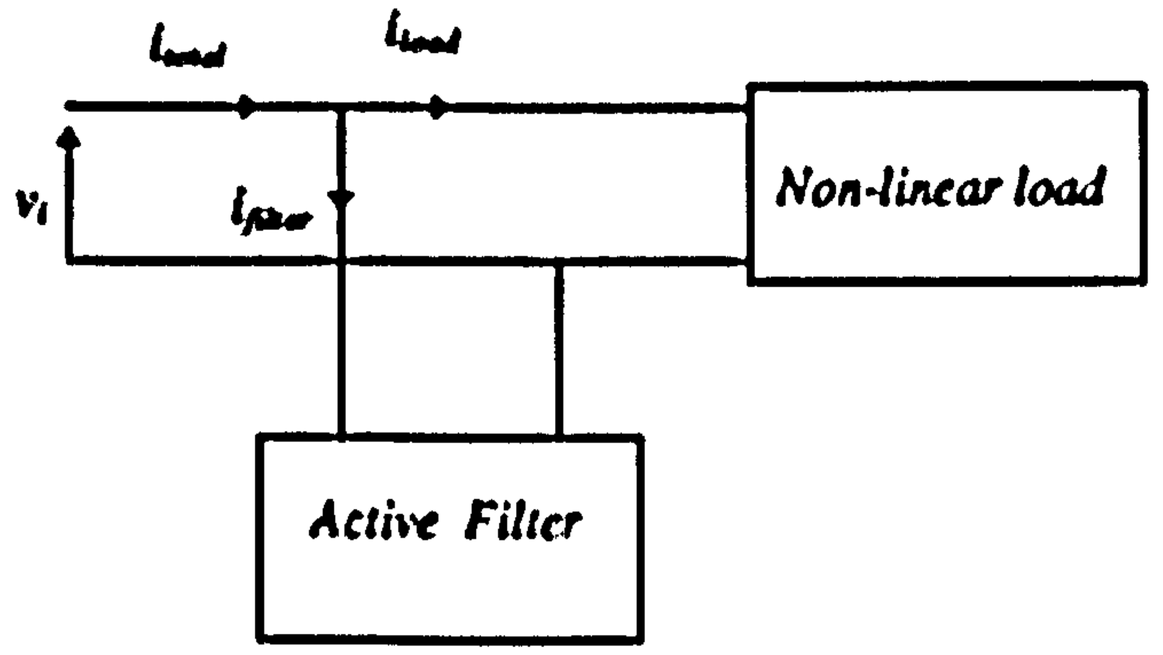


Figure 2.1 Principle of active filtering technique

2.2 Criteria for Design of Active Filters

The design of active filters must meet a number of important criteria:

- The rate of rise of current (di /dt) in the circuits should not exceed the specified limits of the semiconductor switches, otherwise the switches would be damaged.
- The voltage and current ratings of the switches should be within the specified limits.
- For economic reasons, the power dissipation should be minimized as much as possible and the component count should be low.

- Since the passive circuit elements in the active filters are fixed at the design stage, the flexibility required should be achieved through judicious selection of switching patterns which may require on-line control.
- Ideal active filters should not consume any real power. However because active filters use reactive elements, in general certain amount of real and reactive power consumption is inevitable. Whenever possible, the reactive power should be maintained in the leading mode so that, if anything, power systems would benefit from the introduction of such devices.

2.3 Specification of the current in active filter applications

For active filter applications, as already explained, the requirement is that the supply current should be sinusoidal. The supply current consists of nonlinear-load and filter currents:

$$i_{supply} = i_{load} + i_{active\ filter} = k \sin(\omega t + \theta)$$

or

$$i_{active\ filter} = -i_{load} + k \sin(\omega t + \theta)$$

where k is a scaling factor based on the real power demand of the load and filter current and θ is the phase of the fundamental current

Therefore the filter current waveform should approximate the required shape. This can be achieved by tracking the required current waveform within set boundaries. The author has proposed a classification of seven different tracking techniques. In the following sections these techniques are described, and it is shown that the currently

employed approach for constructing active filters, as well as the new circuits proposed here, employ one of these tracking techniques.

(a) Piecewise linear approximation: As shown in Figure 2.2, the filter current is continuous but its rate of change, di /dt, is varied (positive or negative) such that its magnitude is maintained within specified boundaries by employing a suitable switching function. In practice, as will be shown, this is achieved by changing circuit topologies which control the flow of energy between the supply and the filter as well as the distribution of energy within the filter

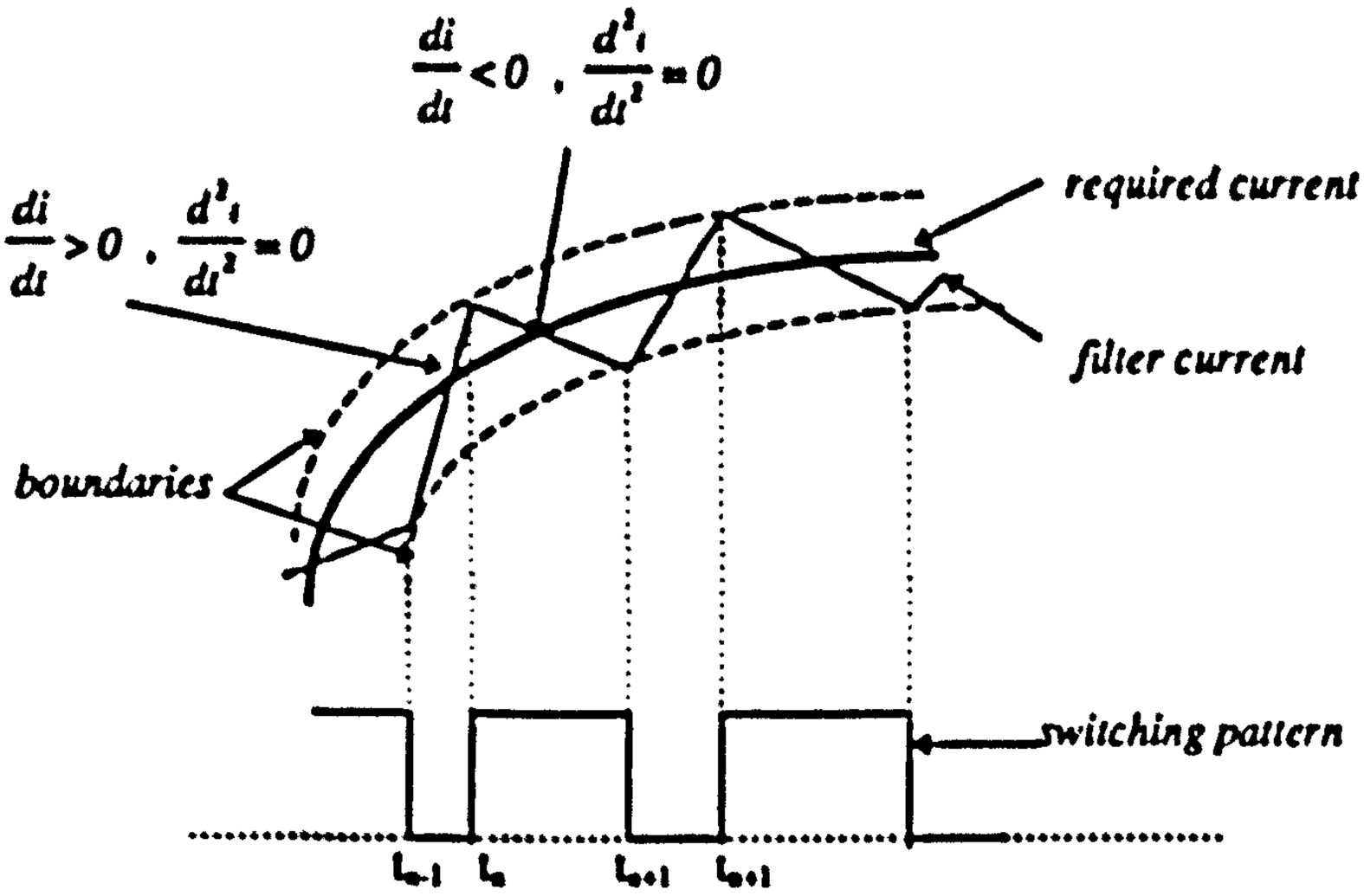


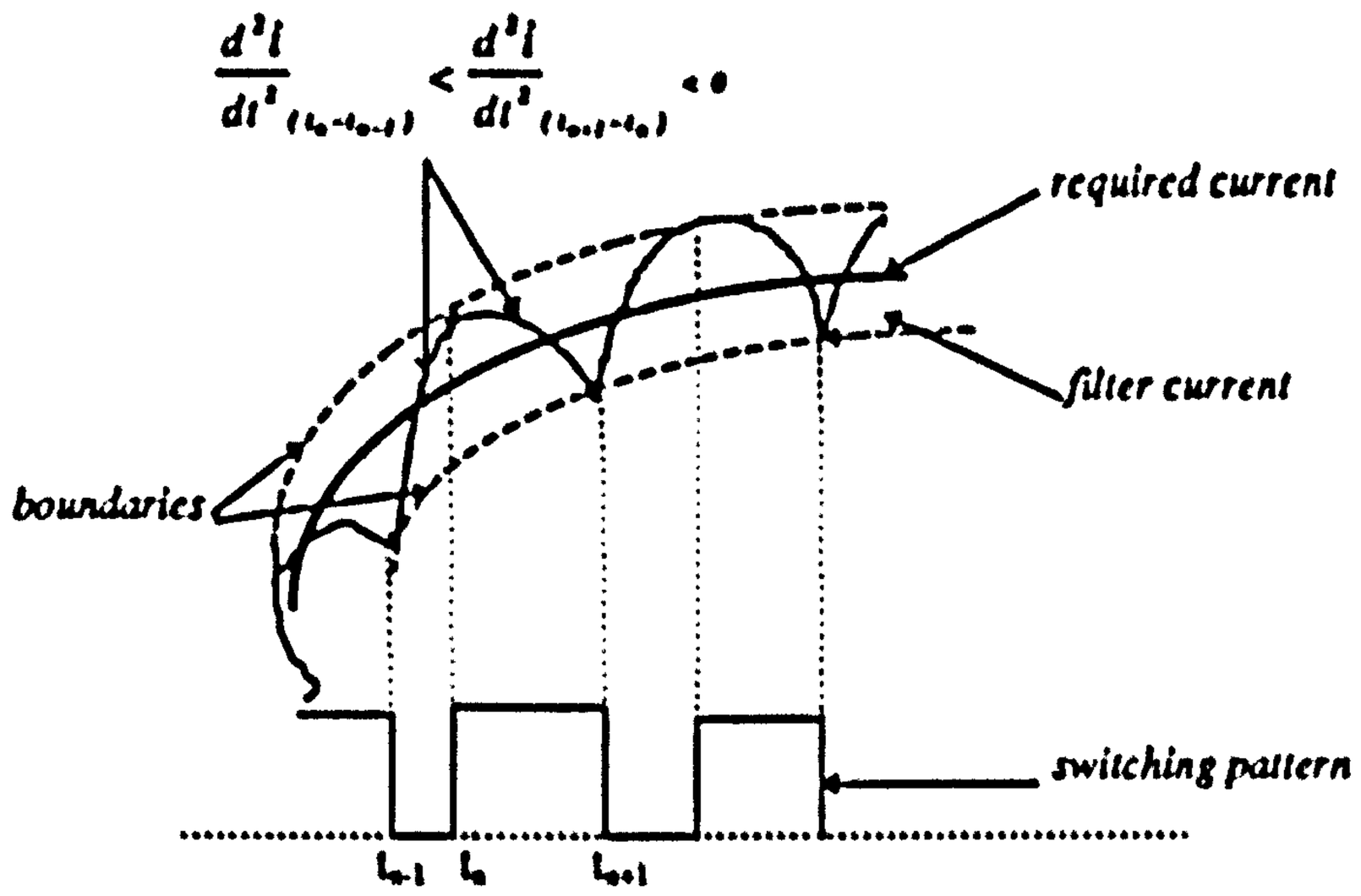
Figure 2.2 The Piecewise Linear approximation method.

For the filter current to track the required waveshape the following condition should be satisfied

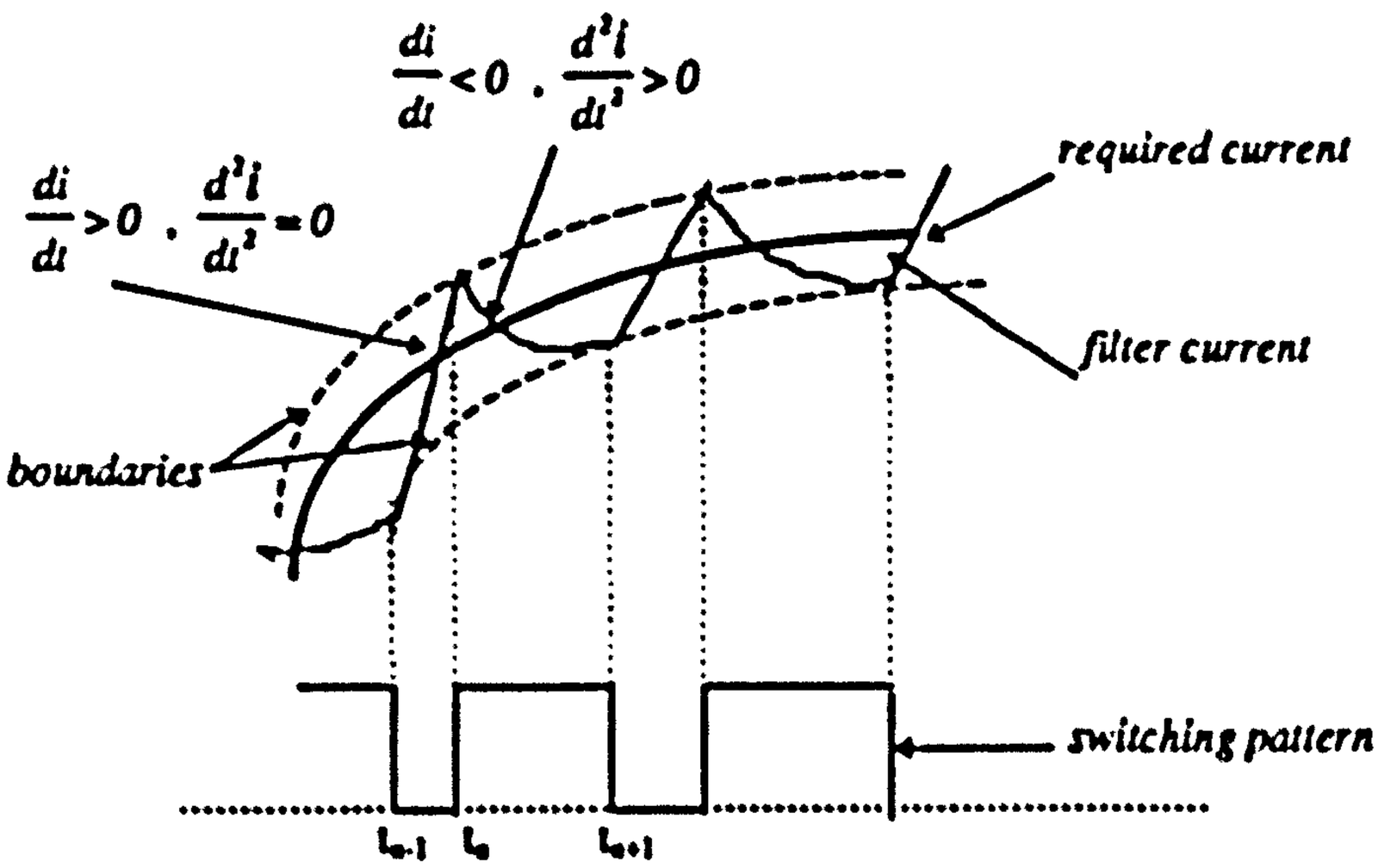
$$\left|\frac{di}{dt}_{\text{filter}}\right| > \left|\frac{di}{dt}_{\text{required current}}\right|$$

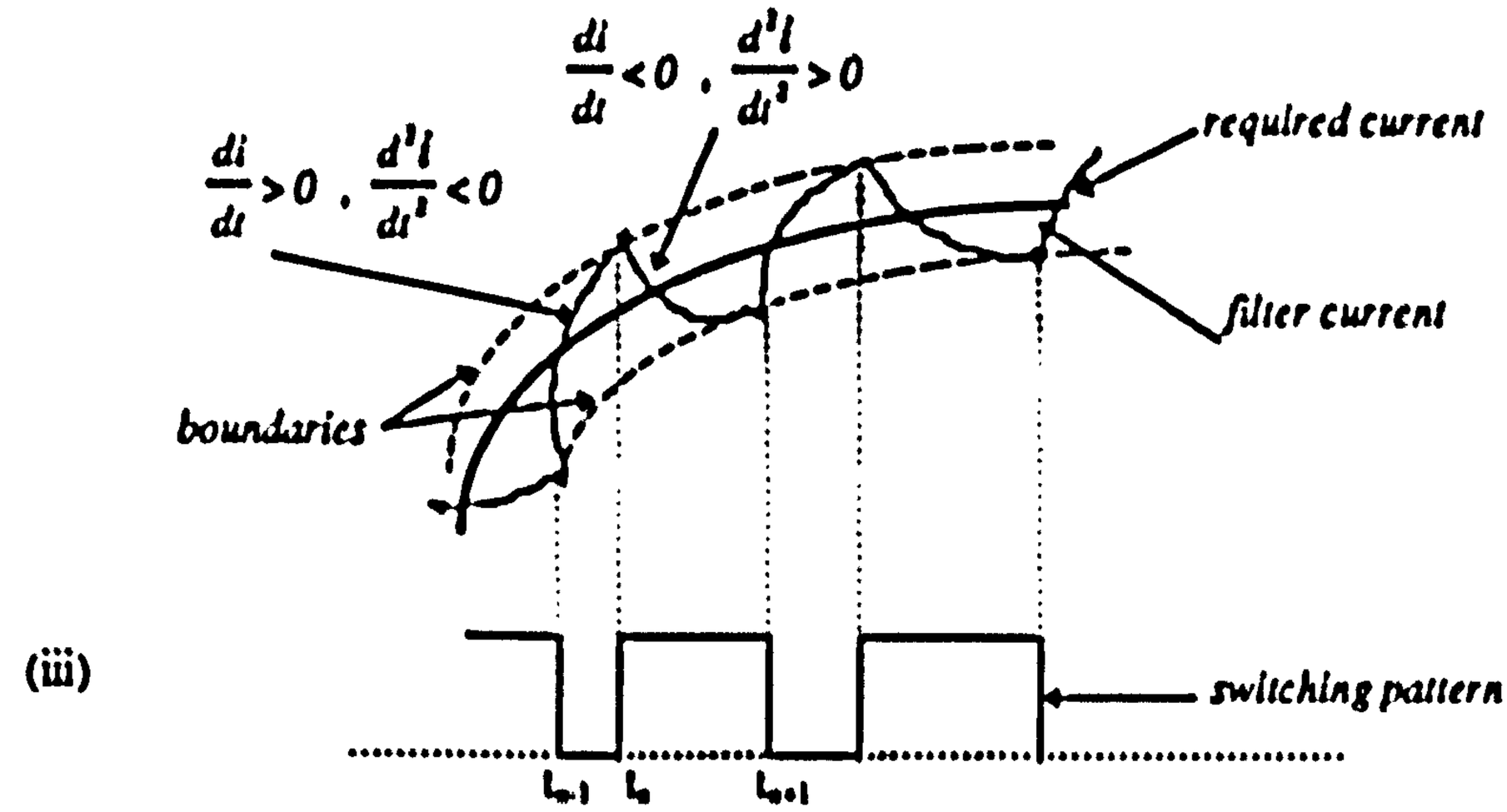
(b) Piecewise nonlinear approximation: This method is illustrated in Figures 2.3. As in method (a), the filter current is continuous but here its rate of change, di /dt, is varied as well as d^2i/dt^2 (positive or negative) such that its magnitude is maintained within specified boundaries by employing a suitable switching function

(i)



(ii)





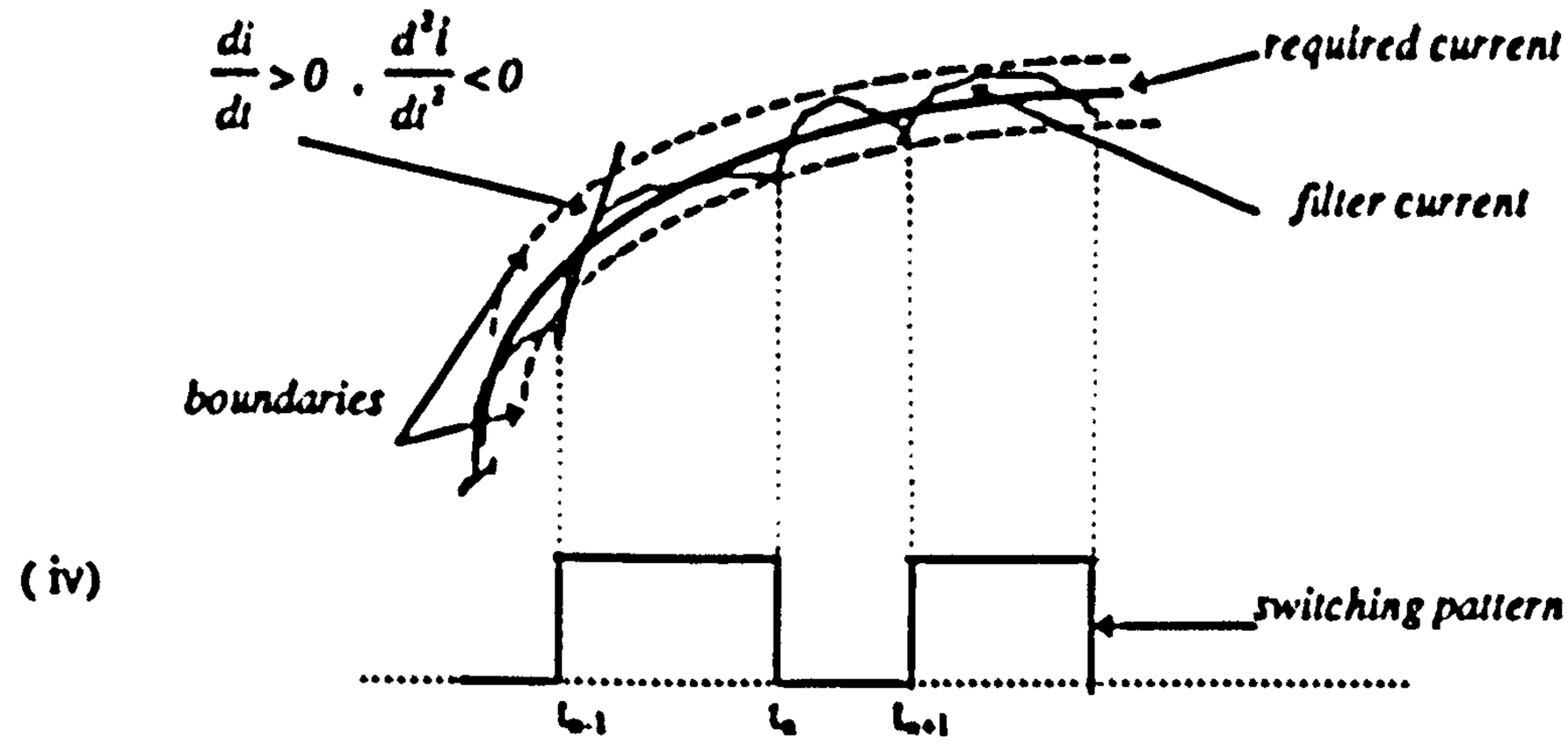


Figure 2.3 The Piecewise Nonlinear approximation with four different strategies

For the filter current to track the required waveshape, the initial values of the rate of change of the current at the instant of switching should satisfy the following conditions

$$\left| \frac{di}{dt}_{\text{switching instant}} \right| > \left| \frac{di}{dt}_{\text{required current}} \right|$$

$$\left| \frac{d^2i}{dt^2}_{\text{switching instant}} \right| > \left| \frac{d^2i}{dt^2}_{\text{required current}} \right|$$

It should be noted that in strategy (i) it is only necessary to satisfy the first of the above conditions for alternate switching instants only.

(c) Piecewise Linear discontinuous approximation: In this method as shown in Figure 2.4, the filter current is discontinuous and its rate of change, di /dt, is constant.

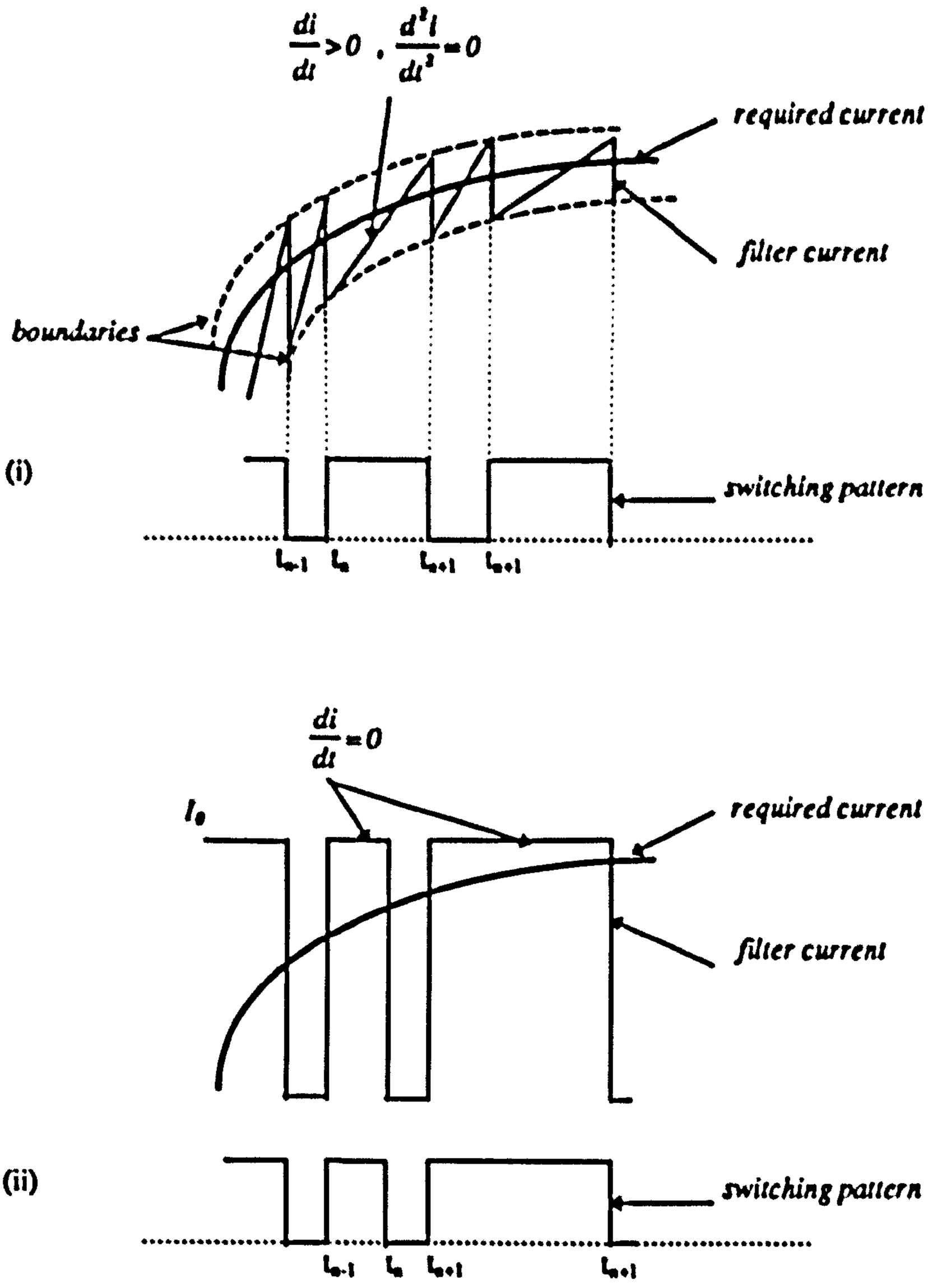


Figure 2.4 The Piecewise Linear discontinuous approximation method.

In the strategy (ii) the filter current is a square-wave function with constant magnitude I_0. In this strategy because of severity of discontinuity, the filter current cannot approximate to the required current with an acceptable difference. However, by appropriate selection of switching instants, the low frequency components of this waveform can match the required current.

For the filter current to track the required waveshape the following conditions for the two strategies should be satisfied respectively;

for strategy (i)

$$\left| \frac{di}{dt}_{filter} \right| > \left| \frac{di}{dt}_{required\ current} \right|$$

$$| I_{filter} |_{matching\ times} < | I_{required\ current} |$$

and for strategy (ii).

$$I_0 > (\pi/4) I_n$$

$$M \geq (N+1)/2,\ N = 1,3,5,\ldots$$

Where I_n is the peak value of the harmonic component 'n',which has the maximum value among other components in the required current, M is the number of pulses within a quarter period and N is the maximum order of harmonics to be eliminated [KIM 87].

2.4 Role and importance of energy storage elements in active filter structure

As explained in Chapter 1, for the purpose of harmonic current suppression, the active filter should provide the instantaneous harmonic power required by the load, and to improve the power factor it could also compensate for the lagging reactive power. This means that the required characterisitics of the active filter can be achieved using energy storage elements in conjunciton with the switching pattern of the switches.

If in these structures, the losses in the switches and inductors are neglected, then the instantaneous power that is handled by these structures is contained within the storage elements. The instantaneous power in a capacitor and an inductor are given by:

$$P_{Capacitor}(t) = v_C i_C = v_C\left(C\frac{dv_C}{dt}\right) = \frac{C}{2}\frac{dv_C^2}{dt}$$

$$P_{Inductor}(t) = v_L i_L = \left(L\frac{di_L}{dt}\right) i_L = \frac{L}{2}\frac{di_L^2}{dt}$$

Thus the instantaneous distribution of energy within a given structure depends on the size of the circuit elements, voltage, current and their derivatives relating to those elements. Generally the basic principle of active filters is to control the flow of energy between the supply and the filter by altering the circuit topology via switches.

The variation of stored energy in an inductor is proportional to the rate of change of current in it, and that for the capacitor is equal to the rate of change of voltage across it. Since the objective of active filters is to control current and its rate of change, rather than voltage, inductors are inherently better for this purpose. Also since the voltage across an inductor is proportional to the rate of change of current in it, this rate of change can be controlled by controlling the voltage across the inductor. These two factors underline the various techniques employed for constructing filter structures as will be shown in this chapter.

In the following sections the various configurations are described and their relative merits discussed. The simulation results are presented for the new configurations. These

results provide a picture of the behavior of the circuits and are backed up by the experimental results in the next chapter. The computer programs for these circuits are shown in Appendix C.

2.5 Basic techniques for building Active filters

There are two methods of controlling the voltage across inductors and thereby the rate of change of current in it. In one case the voltage at one terminal of the inductor is fixed whilst the other terminal is allowed to 'float'. In the alternative mode both the terminals are allowed to 'float'. The term 'float' is used here with a very specific meaning. For example, if the potential of one terminal of an inductor is determined by a fixed voltage source whilst the potential of the other terminal depends on its connection to alternative points in the circuit, then the second terminal is referred to as the 'floating' terminal. The alternative configurations are discussed below with the view to classifying the existing circuits and synthesizing new structures.

2.5.1 One terminal of the inductor fixed and the other floating

In this mode the current in the inductor is the input current into the filter and is continuous which is its main characteristic. There are eight different structures.

(1) Floating terminal alternately connected to the positive and negative voltage source (piecewise linear approximation)

The functional arrangement for this is shown Figure 2.5

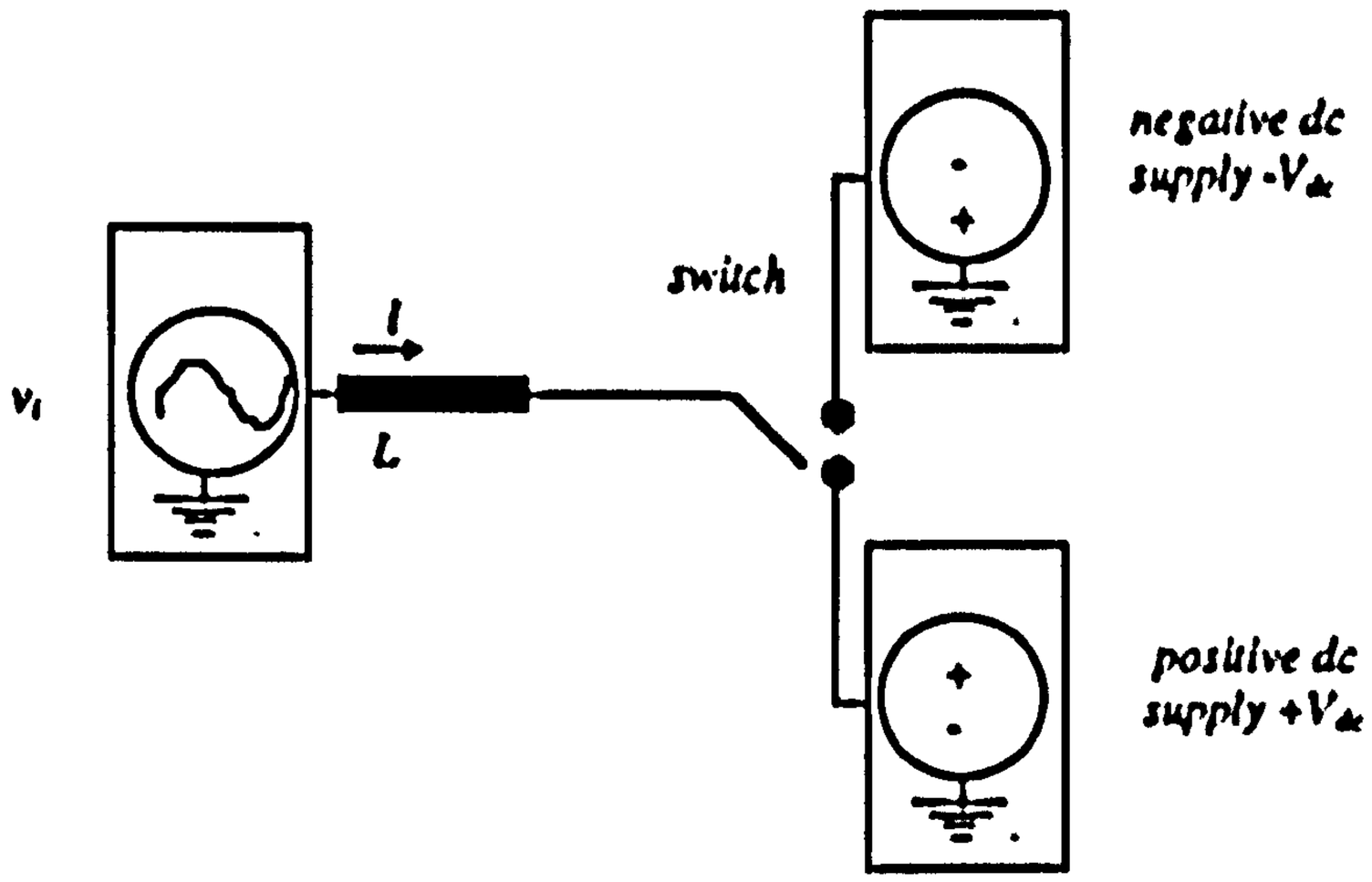


Figure 2.5 Functional Diagram

In each case the rate of change of current in the inductor can be computed as follows.

When the switch is connected to the positive dc supply

$$\frac{di}{dt} = \frac{v_i - V_{dc}}{L}$$

When the switch is connected to the negative dc supply

$$\frac{di}{dt} = \frac{v_i + V_{dc}}{L}$$

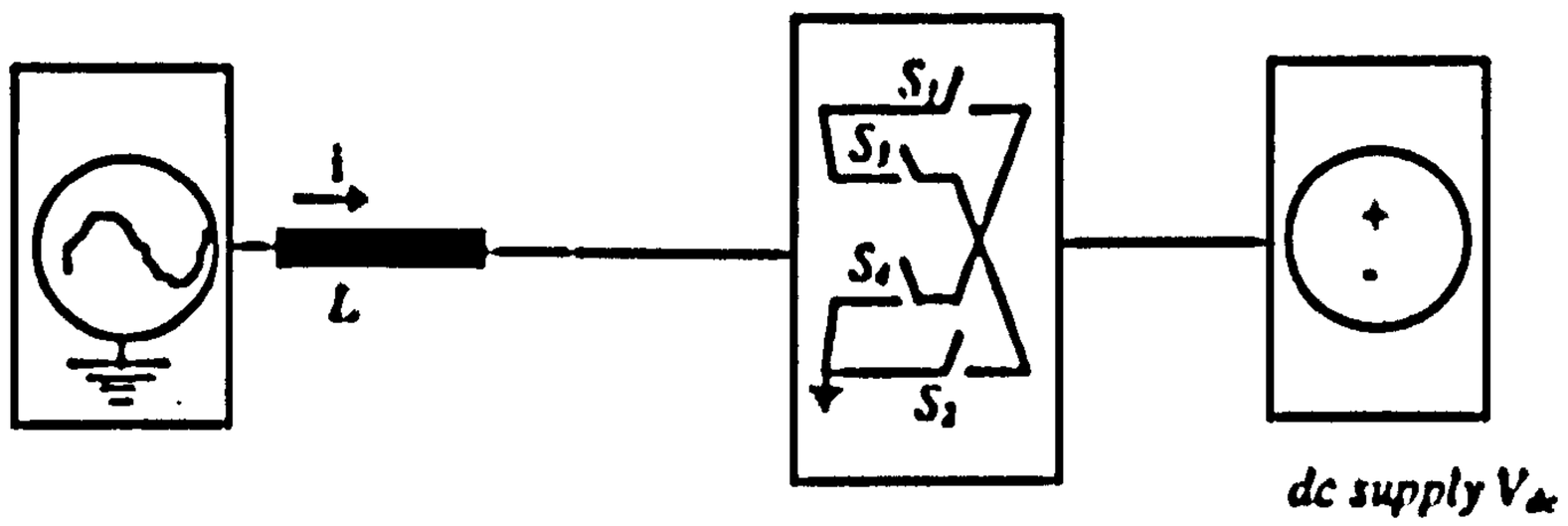
where V_{dc} is greater than v_i.

Assuming that the instantaneous value of the supply voltage during the switching periods is constant, the second derivative of the filter current is approximately zero:

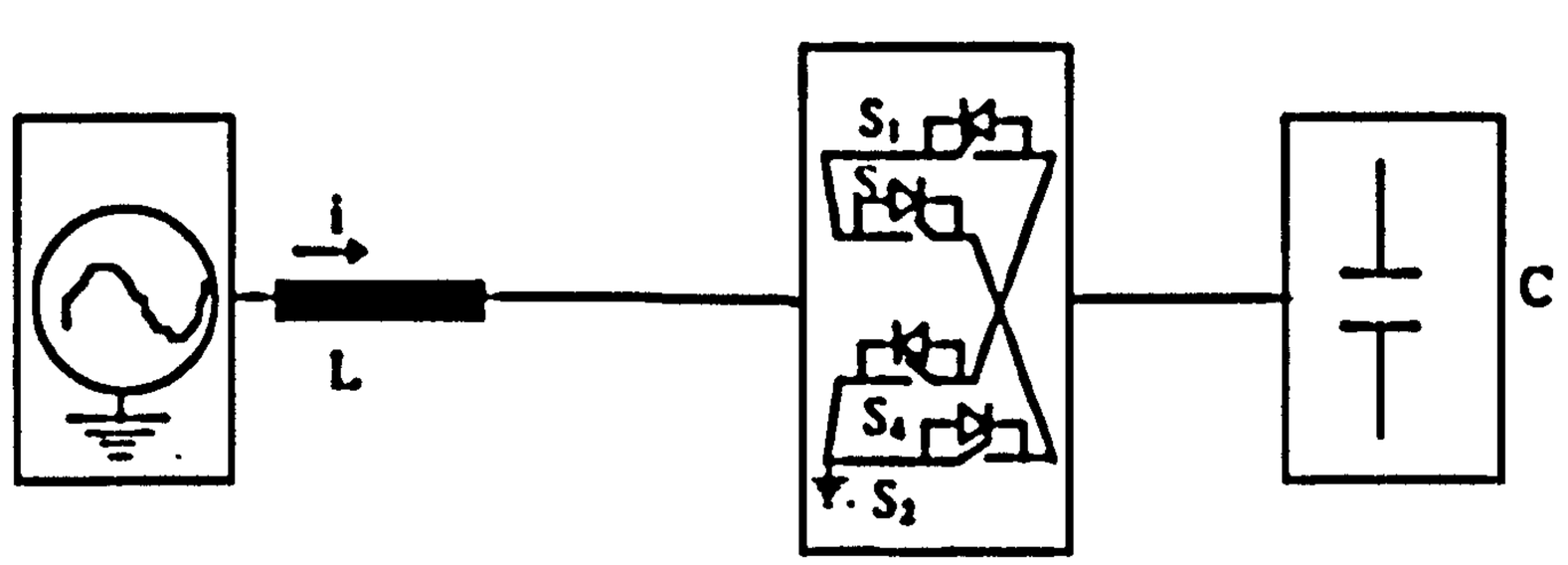
$$\frac{d^2i}{dt^2} = \frac{1}{L}\frac{dv_i}{dt} \approx 0$$

This shows that the filter current is composed of piecewise linearised segments as discussed in section 2.3. This mode of controlling the rate of change of current in the inductor can be implemented as shown in Figure 2.6 (a) in which a single dc source is

used by incorporating a bridge arrangement for the switches. Instead of a dc voltage supply as in Figure (a), the alternative approach is to use a capacitor as in (b) [Machmoum 95]. The pairs of switches S_1, S_2 and S_3, S_4 operate synchronously in anti-phase and their order of operations changes every other half-cycle to guarantee the odd symmetry for the filter current.



(a)



(b)

Figure 2.6 Practical circuits a and b

The main disadvantage of this approach is that the circuit is inflexible, in that, for a given size of inductor, the rate of change of current is approximately constant because of the fixed dc voltage. Therefore to track the required current waveshape with an acceptable accuracy, a compromise has to be achieved between the size of the inductor and the switching frequency i.e. smaller the inductor higher the required switching frequency.

(2) Floating terminal alternately connected to a dc voltage and ground (piecewise linear approximation):

The functional arrangement for this is shown in Figure 2.7 below.

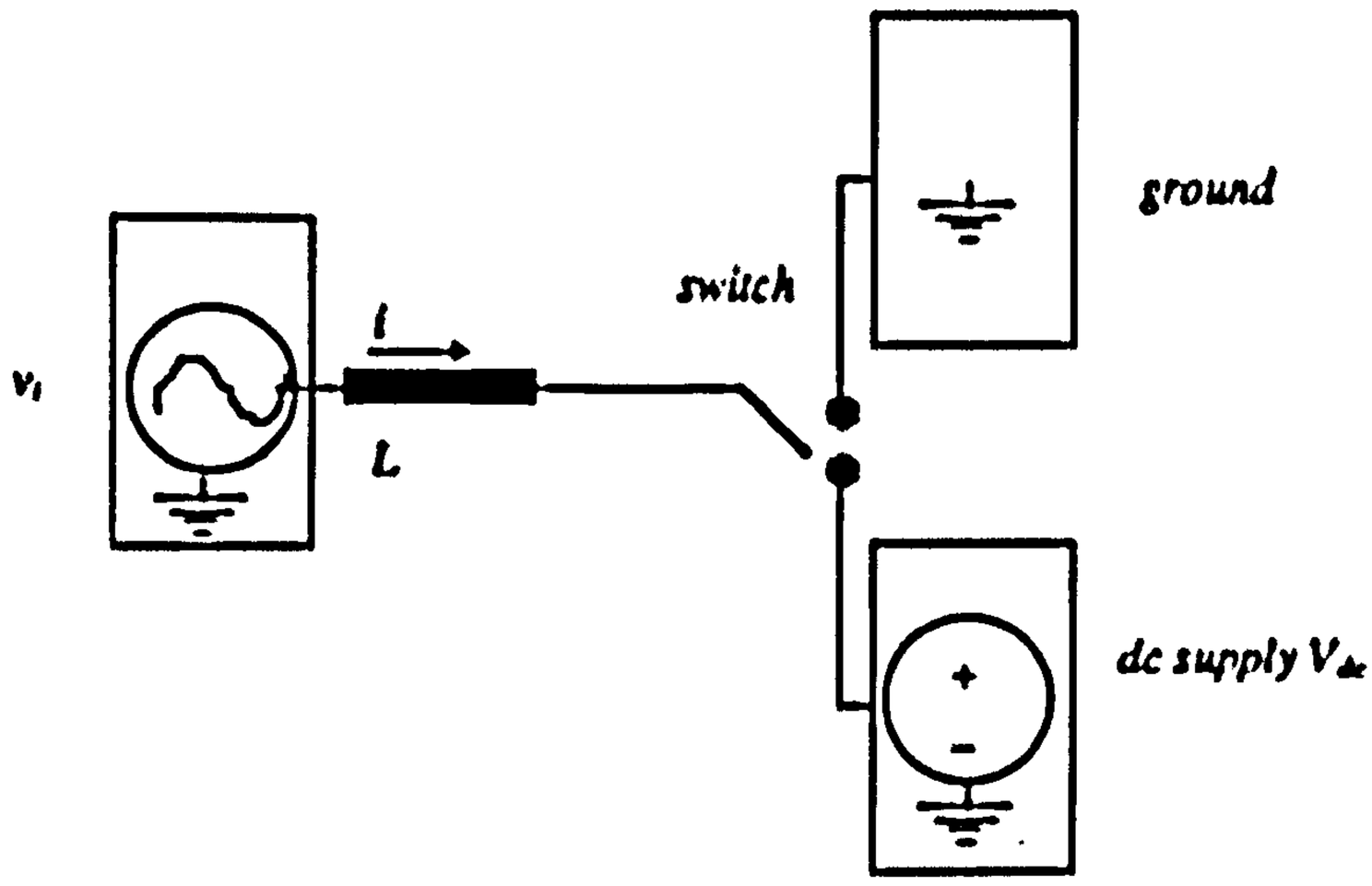


Figure 2.7 Functional diagram

In each position of the switch the rate of change of current in the inductor can be computed as follows.

When the switch is connected to the ground

$$\frac{di}{dt} = \frac{v_i}{L}$$

When the switch is connected to the dc supply

$$\frac{di}{dt} = \frac{v_i - V_{dc}}{L}$$

where V_{dc} is greater than v_i.

Again assuming that the instantaneous value of the supply voltage during the switching period is constant, the second derivative of the filter current is approximately zero:

$$\frac{d^2i}{dt^2} = \frac{1}{L}\frac{dv_i}{dt} = 0$$

This shows that the filter current as in the technique (a) above is composed of piecewise linearised segments.

This mode of controlling the rate of change of current in the inductor can be implemented using exactly the same practical circuit as the one used for the previous configuration shown in Figure 2.6. However the pairs of switches S_3 and S_4 and S_1 and S_2 are used for different task as explained in [Torrey 95]. Whilst the switches S_1 and S_2 operate synchronously in anti-phase, the switch S_3 is 'on' during the negative half-cycle and the switch S_4 is 'on' during the positive half-cycle.

As in the previous circuit of scheme (1), the choice of the size of the inductor, L, is a matter of compromise. The ability of the filter to track the required current improves as the filter inductance is made smaller. However the switching frequency has to be increased to keep the tracking error within acceptable limits.

(3) Floating terminal alternately connected to two capacitors of different sizes

(piecewise non-linear approximation):

The functional diagram for this approach is shown in Figure 2.8.. The following equations can be written for two positions of the switch.

When the switch is connected to the capacitor C_1 :

$$\frac{di}{dt} = \frac{v_i - v_{c1}}{L}$$

$$\frac{d^2i}{dt^2} = \frac{1}{L}\frac{d(v_i - v_{c1})}{dt} = -\frac{1}{L}\frac{dv_{c1}}{dt} = -\frac{i}{LC_1}$$

When the switch is connected to the capacitor C_2

$$\frac{dI}{dt} = \frac{V_1 - V_{c2}}{L}$$

$$\frac{d^2I}{dt^2} = \frac{1}{L}\frac{d(V_1 - V_{c2})}{dt} = -\frac{1}{L}\frac{dV_{c2}}{dt} = -\frac{I}{LC_2}$$

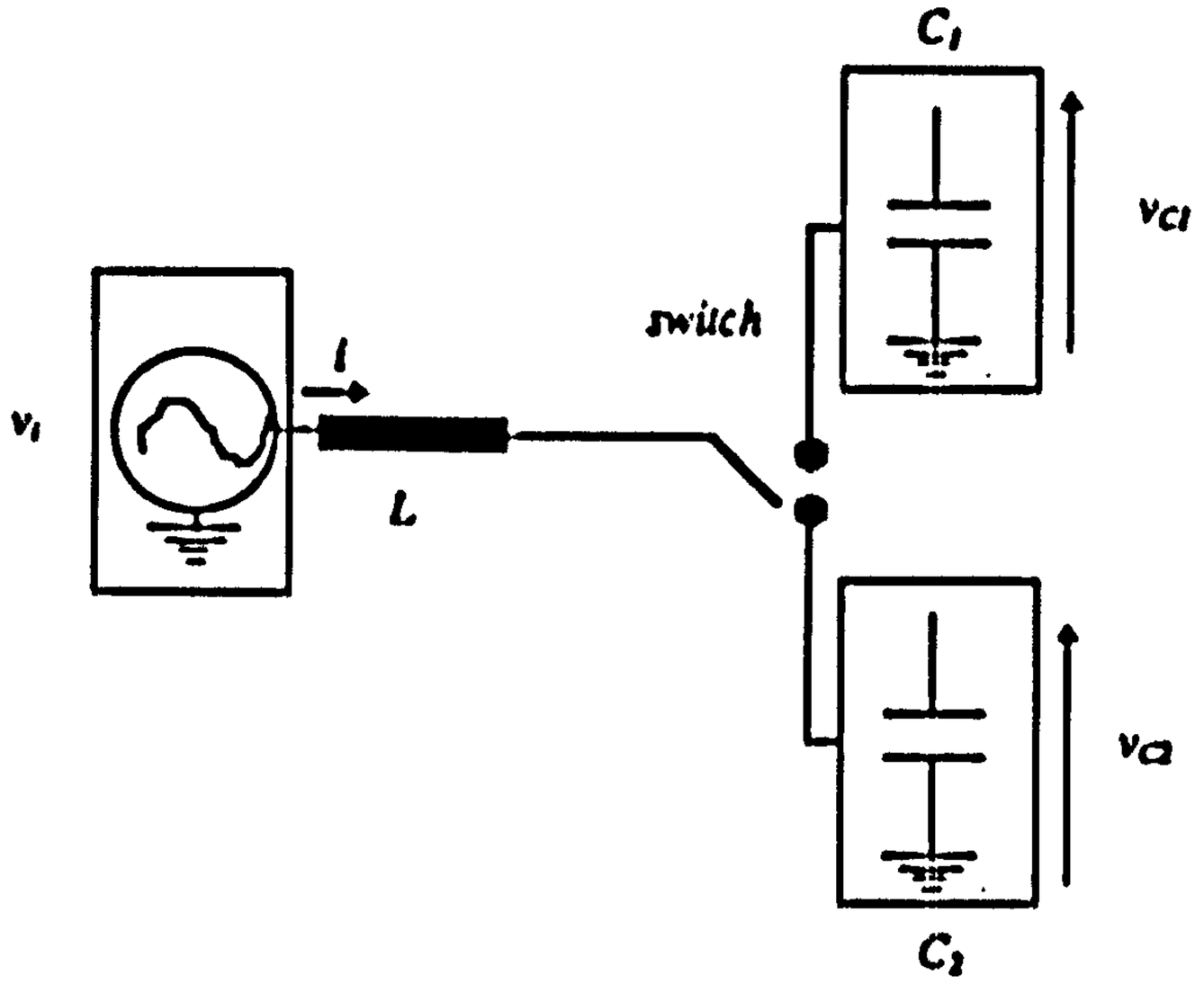


Figure 2.8 Functional diagram

The size of the two capacitors are chosen to be unequal with a large difference in order to cope with the requirements of piecewise non-linear approaximation method (b-i). This provides a large difference in the second derivatives of the filter current as implied by the above equations.

To satisfy the first condition of the approximation method, the magnitude of the rate of change of the filter current should be higher than that of the required current at the alternate switching instants. Therefore as the equations show the size of the inductor should be relatively small.

The basic requirement of this circuit is that the resonant frequency associated with the two capacitors and the inductor should be less than the switching frequency, to prevent this frequency component from appearing in the filter current. It becomes necessary to select a relatively large value of inductance or capacitance. This of course limits the rate of change of current which can be achieved. Nevertheless the choice of capacitor and inductor values and the switching pattern is a matter of compromise [Mehta 90].

The main drawback of this circuit is that the voltage across the capacitors remains unchanged during their 'off' states so that for a given size of inductor, the initial rate of change of current is determined by the previous 'on' states. Since this does not allow the control over the initial rate of change of current in the inductor at the instants of switching, the circuit is inflexible.

Figure 2.9 shows a practical implementation of this circuit

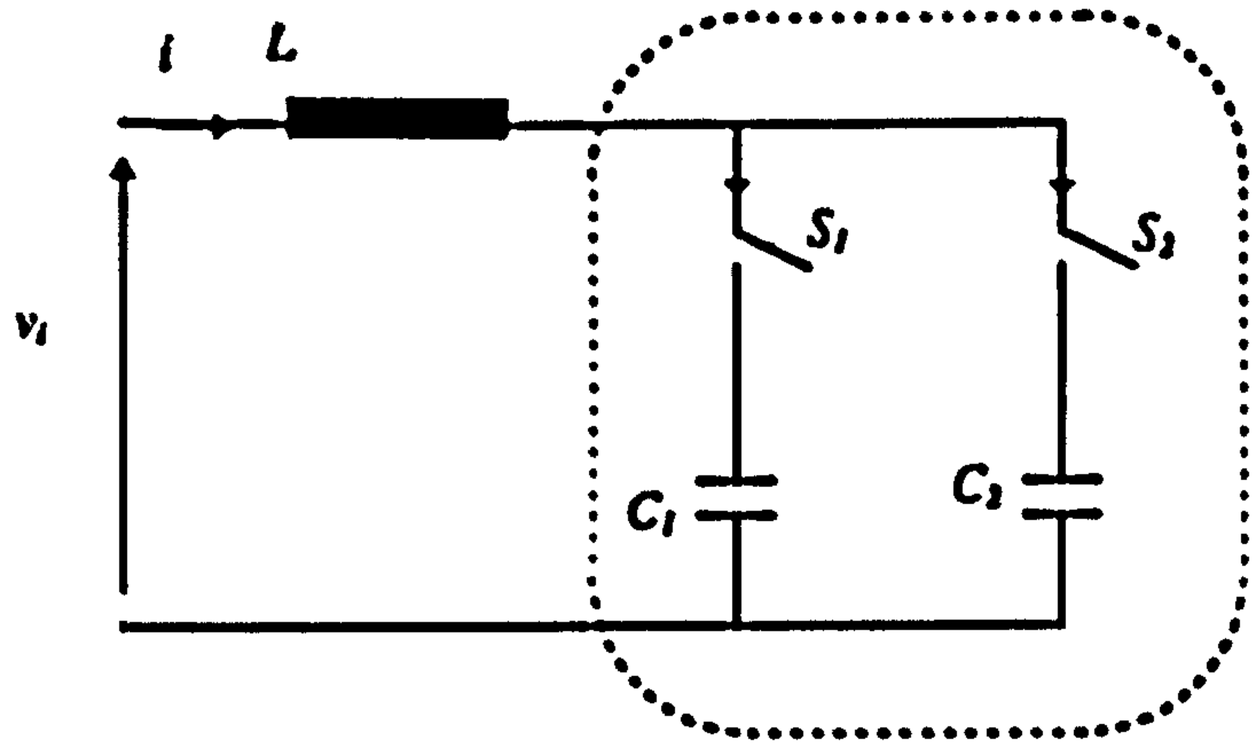


Figure 2.9 Practical circuit

(4) Floating terminal connected alternately to a capacitor and the ground

(piecewise non-linear approximation)

This is the first of several new arrangements proposed by the author and is illustrated by its functional diagram in Figure 2.10. This is an example of the piecewise non-linear approximation method (b-ii).

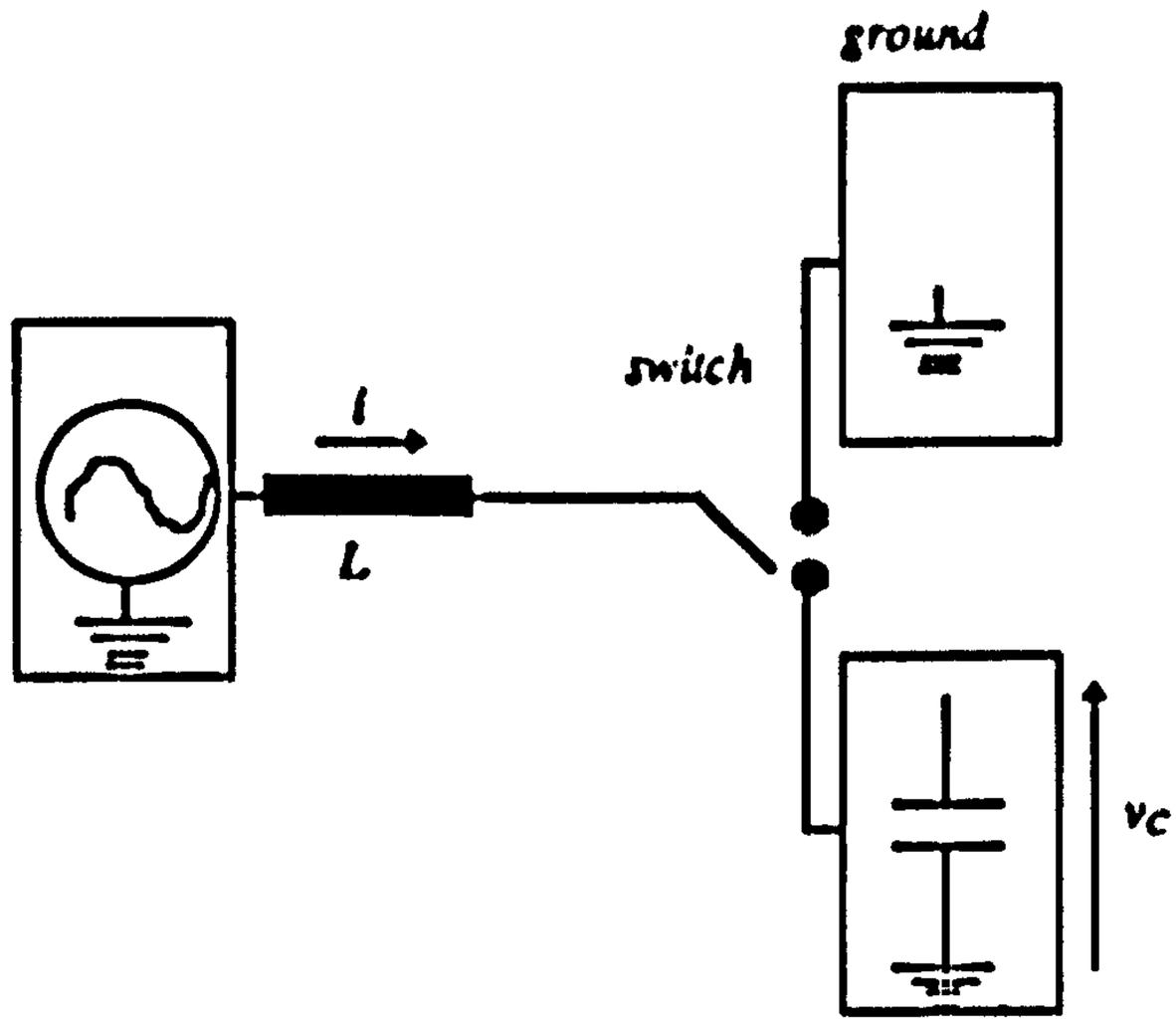


Figure 2.10 Functional diagram

The rate of change of current in the inductor for this arrangement can be calculated as follows.

When the switch is connected to the ground

$$\frac{di}{dt}=\frac{v_i}{L}$$

When the switch is connected to the capacitor

$$\frac{di}{dt}=\frac{v_i-v_c}{L}$$

$$\frac{d^2i}{dt^2}=\frac{1}{L}\frac{d(v_i-v_c)}{dt}=-\frac{1}{L}\frac{dv_c}{dt}=-\frac{i}{LC}$$

These equations show that the rate of change of current in the inductor, when the inductor is connected to the ground, is of the same polarity as the supply voltage. To obtain the rate of change of the current of the polarity opposite to that of the supply (or occasionally with the same polarity of supply but opposite d^2i/dt^2), the inductor is connected to the capacitor. Figure 2.11 shows a practical implementation of this circuit. Simulation results are shown in Figures 2.12 and 2.13.

Similar to the previous circuit, the resonant frequency of the L-C components should be less than the switching frequency. A relatively large value of L would limit the rate at which the current in the inductor can change. Therefore it is preferable to use a relatively small inductor in conjunction with a relatively high switching frequency as will be shown in Chapter 3.

This circuit has a very simple structure and is quite flexible. This approach suffers from the same drawback as techniques (1) and (2), i.e. to track the required current, the switching frequency has to be quite high.

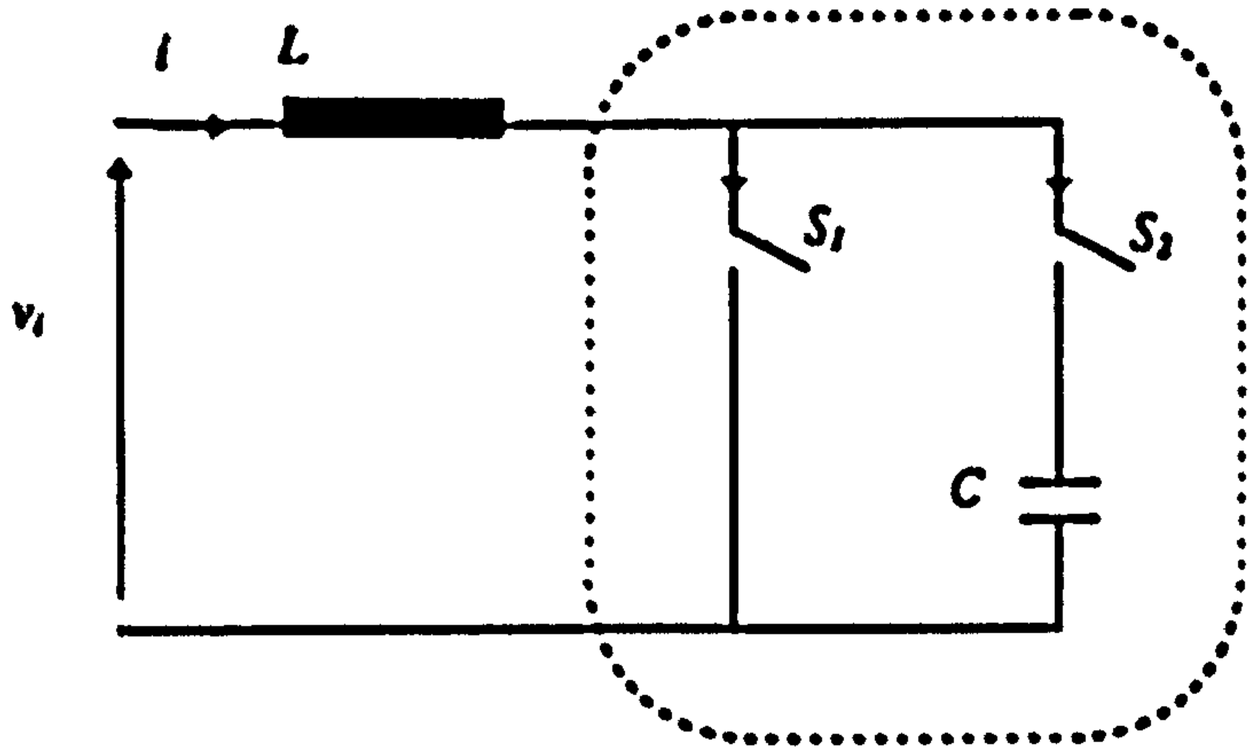


Figure 2.11 Practical circuit (new)

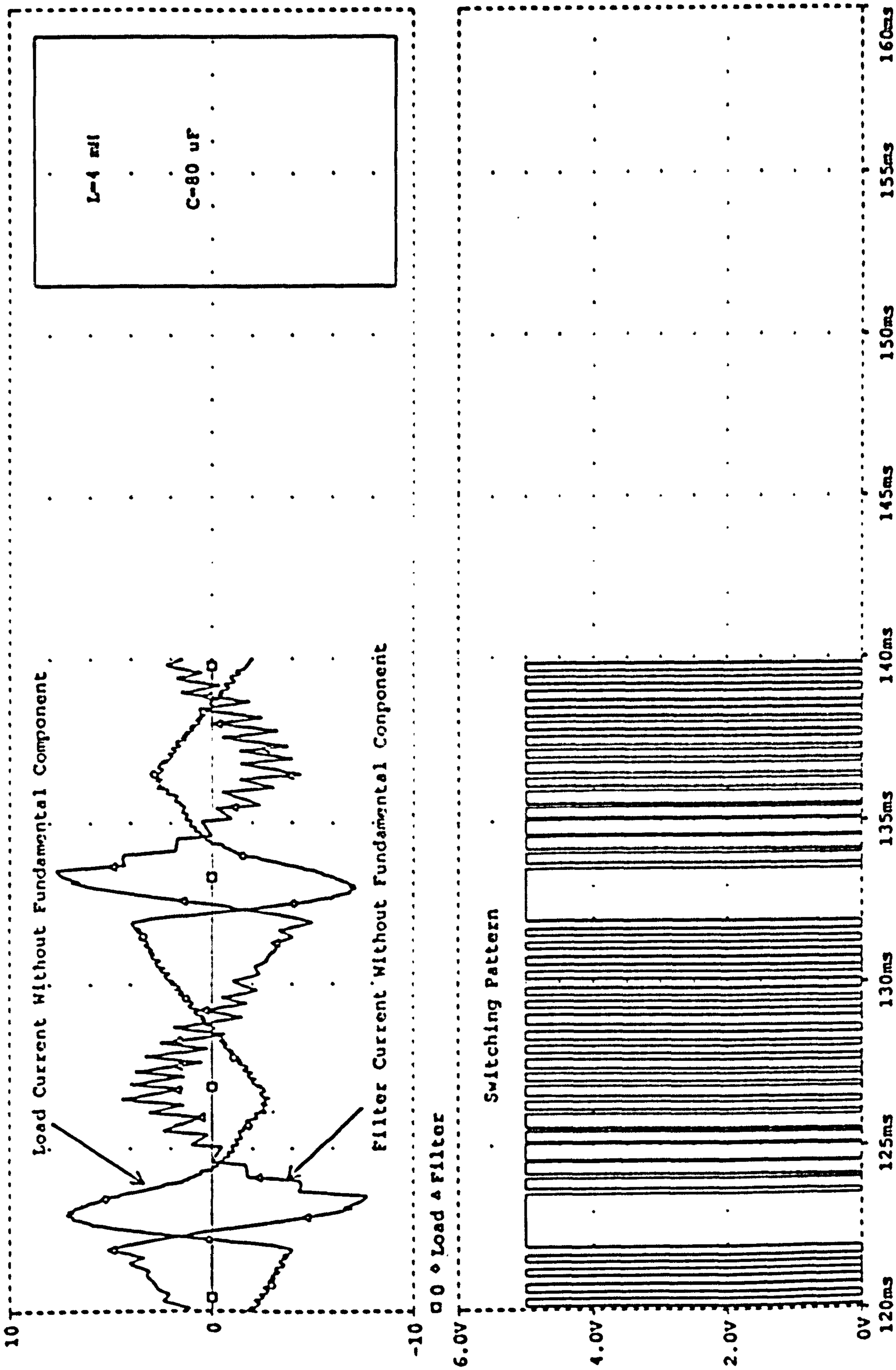


Figure 2.12 Simulation results of scheme No.4 section 2.5.1

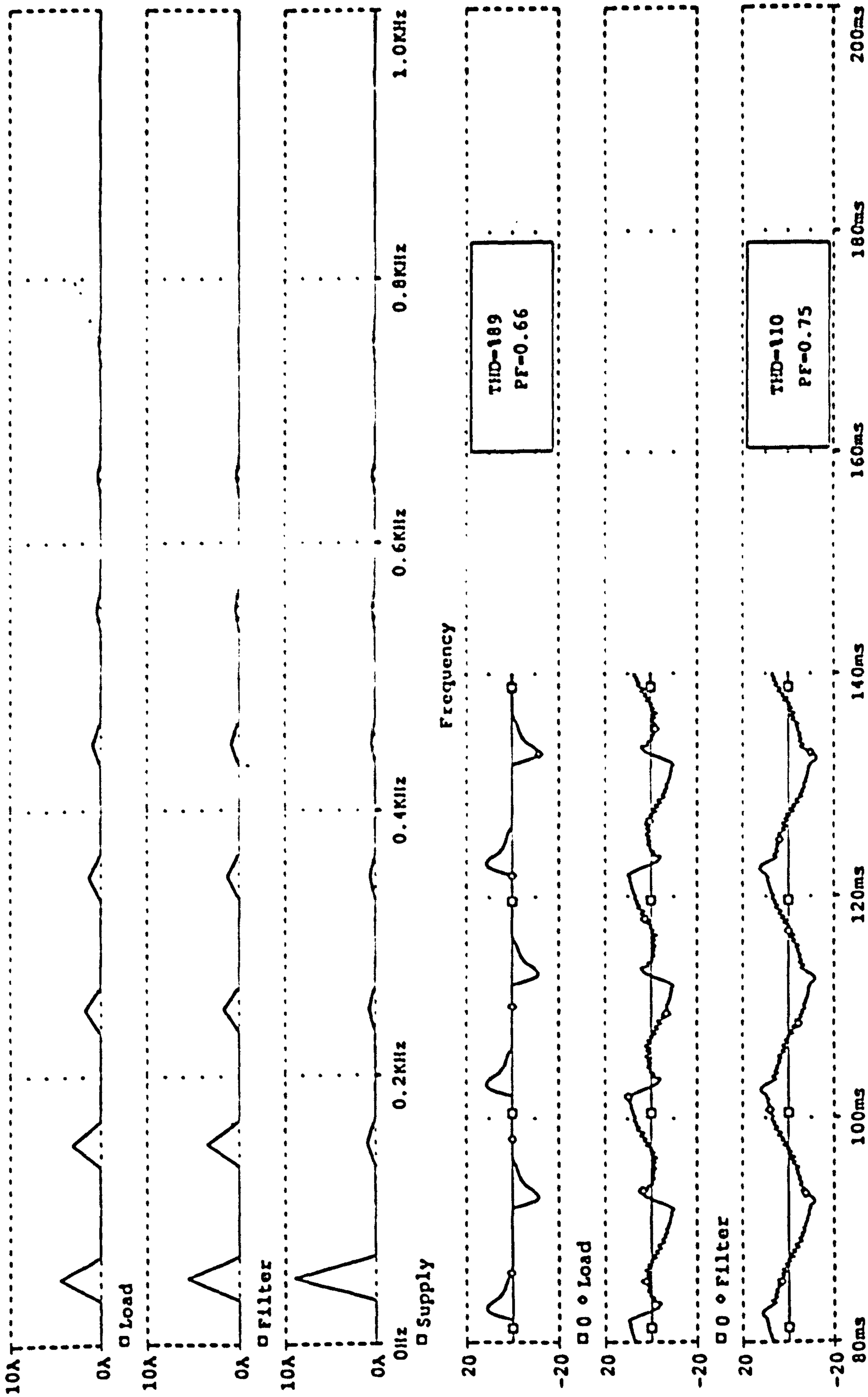


Figure 2.13 Second simulation results of scheme No.4 section 2.5.1

(5) Floating terminal connected to the opposite ends of a capacitor (piecewise nonlinear approximation)

This is a new arrangement and its functional diagram is shown in Figure 2.14 .

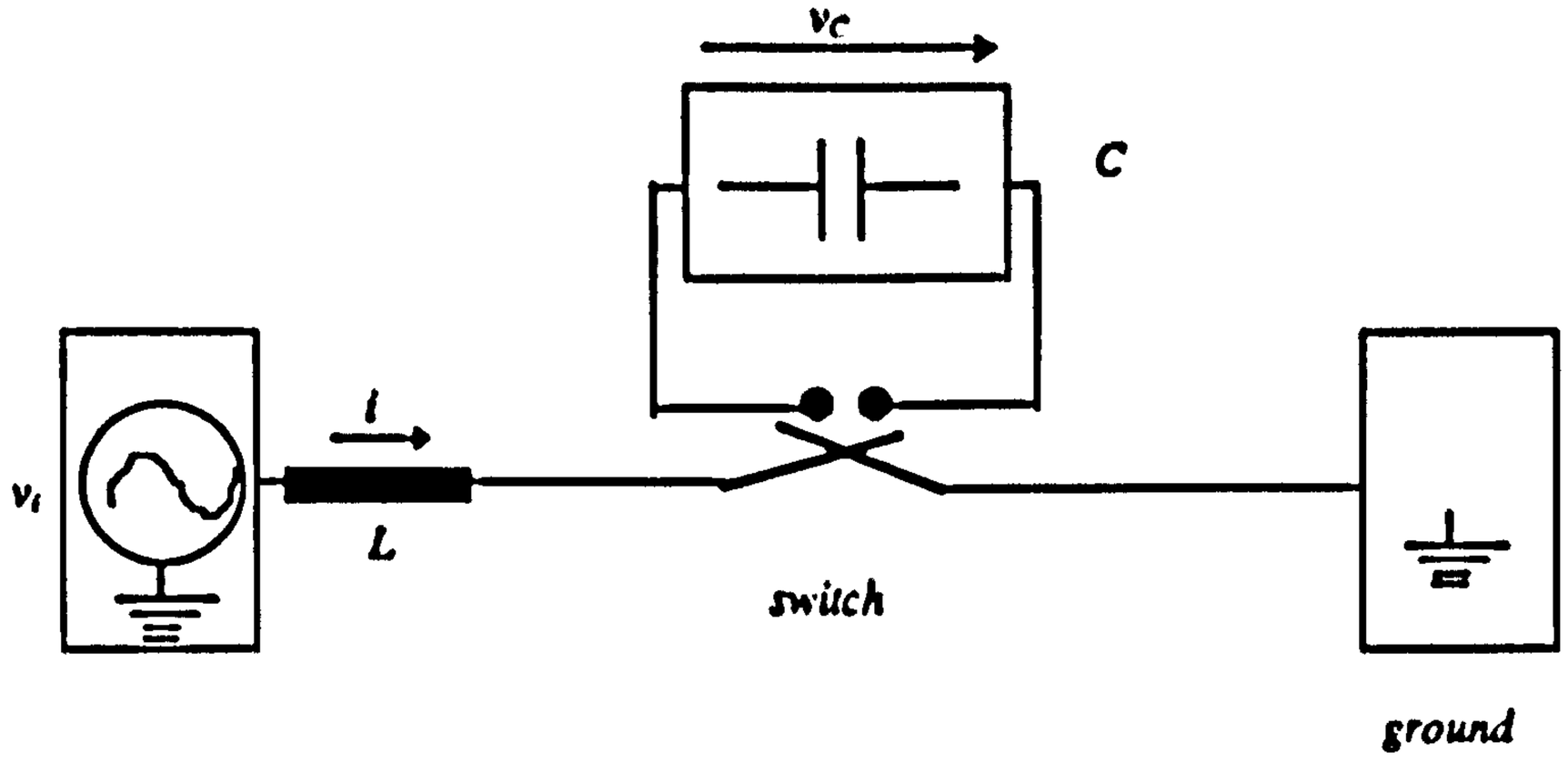


Figure 2.14 Functional diagram

The following equations apply to the two different states of the structure.

When the switch is in the position shown in the functional diagram

$$\frac{di}{dt} = \frac{v_i - v_C}{L}$$

$$\frac{d^2i}{dt^2} = \frac{1}{L}\frac{d(v_i - v_C)}{dt} = -\frac{1}{L}\frac{dv_C}{dt} = -\frac{i}{LC}$$

When the switch is in the alternative position

$$\frac{di}{dt} = \frac{v_i + v_C}{L}$$

$$\frac{d^2i}{dt^2} = \frac{1}{L}\frac{d(v_i + v_C)}{dt} = \frac{1}{L}\frac{dv_C}{dt} = -\frac{i}{LC}$$

As the above equations show, the polarity of the rate of change of current (di /dt) is dictated by the value of the voltage across the capacitor with respect to the input voltage. This makes the circuit more flexible compared with arrangement (3).

The basic requirement for this circuit, similar to the previous circuits, is that the resonance frequency of the L-C components should be less than the switching frequency. A relatively large value of the inductor limits the rate of the change of current and therefore a relatively large capacitor is preferred [Kanani-1 95].

Use of a relatively larger capacitor is the main disadvantage of this circuit so that as the equations show, this limits the second derivative of the filter current. Therefore for rapid variation in the required current, the circuit cannot satisfy the second condition of nonlinear approximation method (b).

Figure 2.15 shows the practical implementation of the circuit. The pairs of switches S_1, S_2 and S_3, S_4 operate synchronously in anti-phase to connect the floating terminal of the inductor to the capacitor terminals alternately. Circuit simulation results are shown in Figures 2.16 and 2.17.

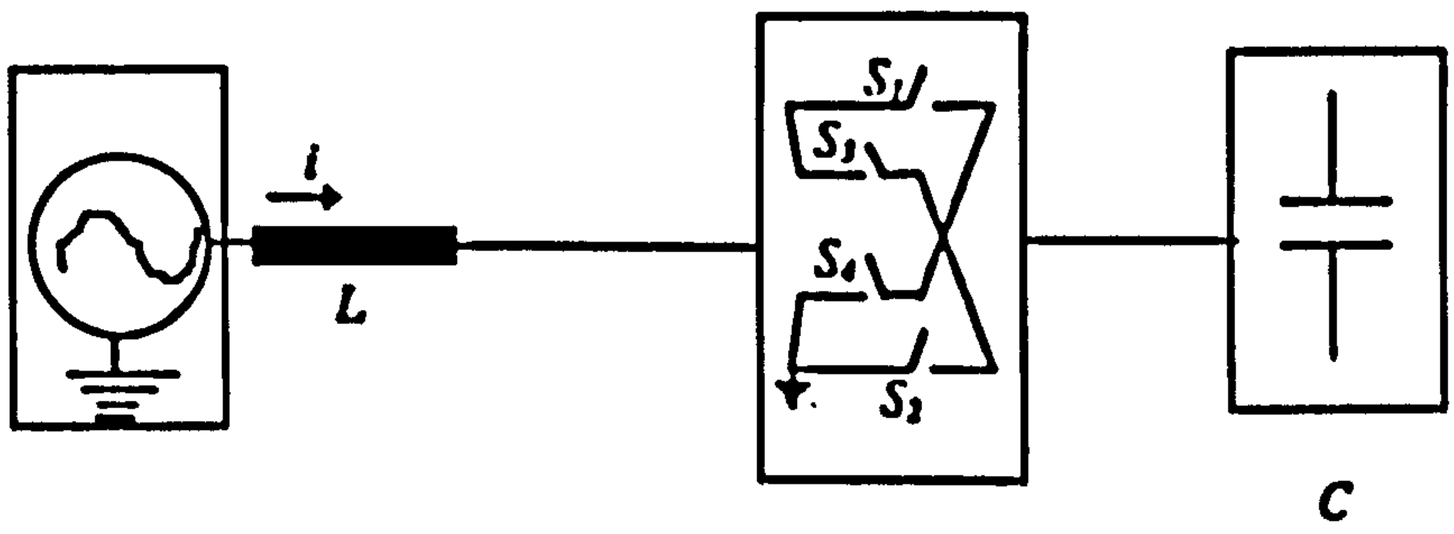


Figure 2.15 Practical circuit (new)

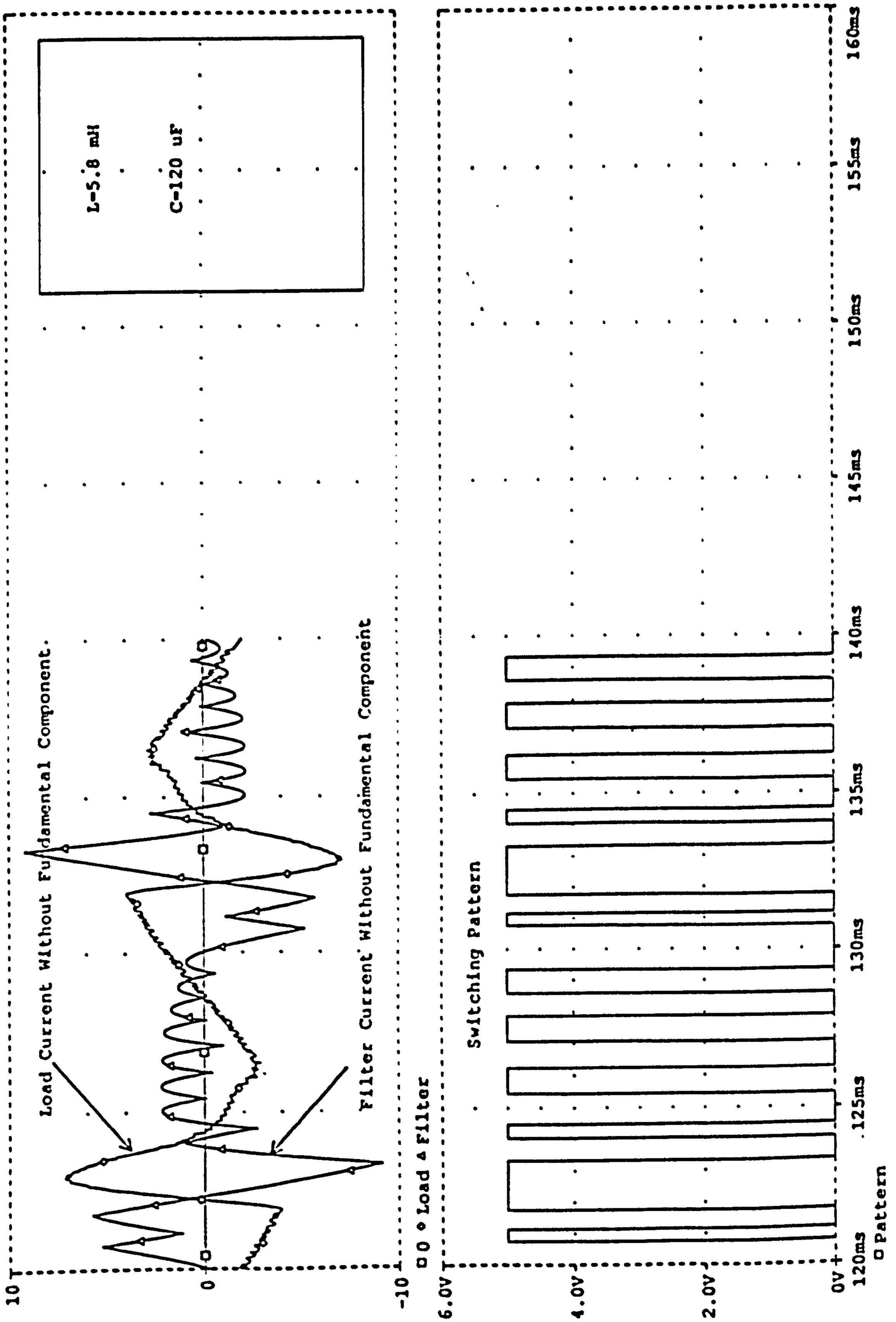


Figure 2.16 Simulation results of scheme No.5 section 2.5.1

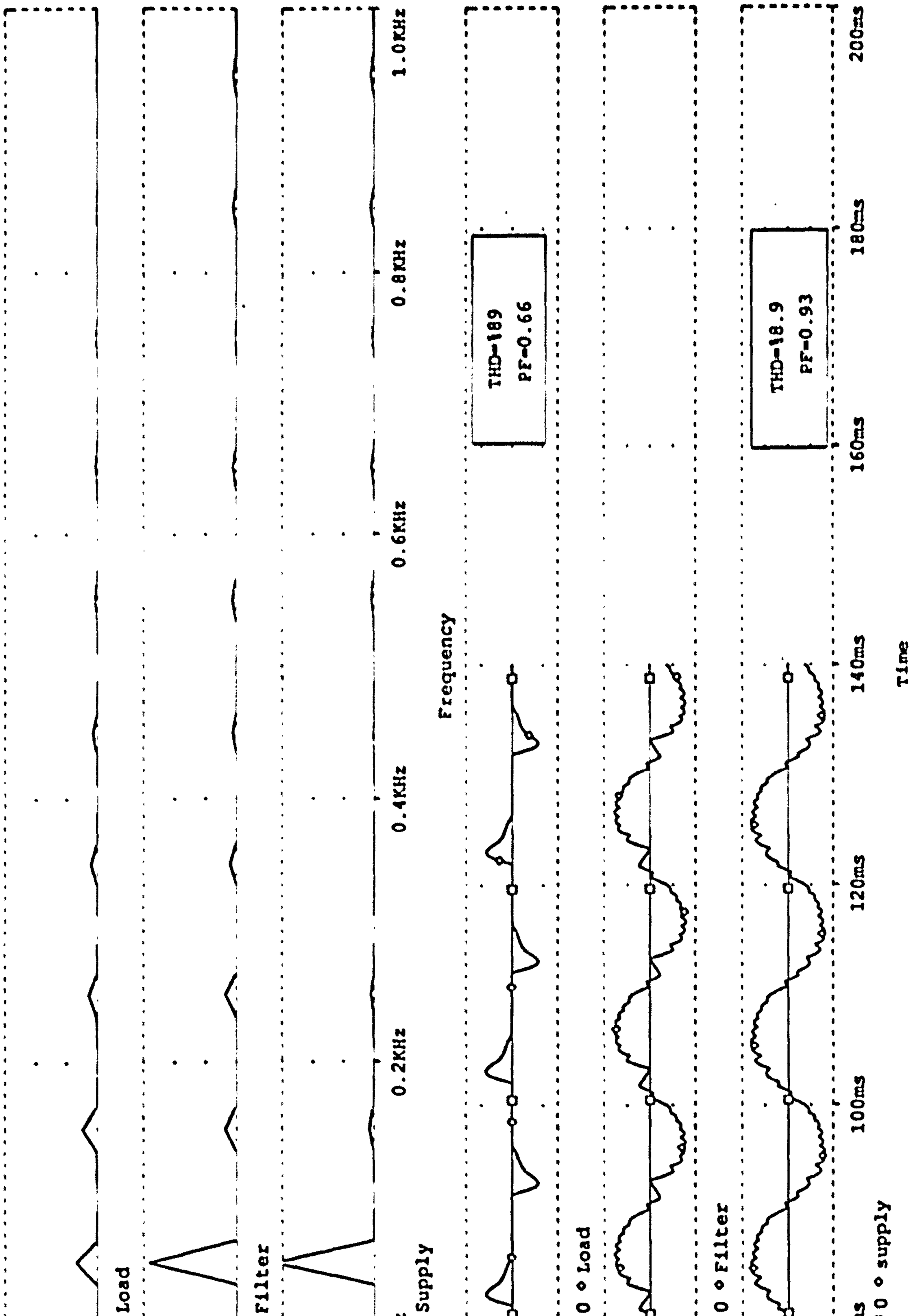


Figure 2.17 Simulation results of scheme No.5 section 2.5.1

(6) Two capacitors alternately connected to the floating terminal of the inductor and an auxiliary inductor (piecewise non-linear approximation)

In this new topology, shown in Figure 2.18, unlike the previous approaches above, the capacitors exchange energy alternately with auxiliary inductor as well the supply. This provides a greater flexibility over the control of the initial values of di / dt via the control of voltages across the capacitors as required by the approximation method (b-iv). The current in the resonant circuit (La, C1) or (La, C2) does not appear at the terminals of the filter and thus has no effect on the filter current [Kanani-2 95].

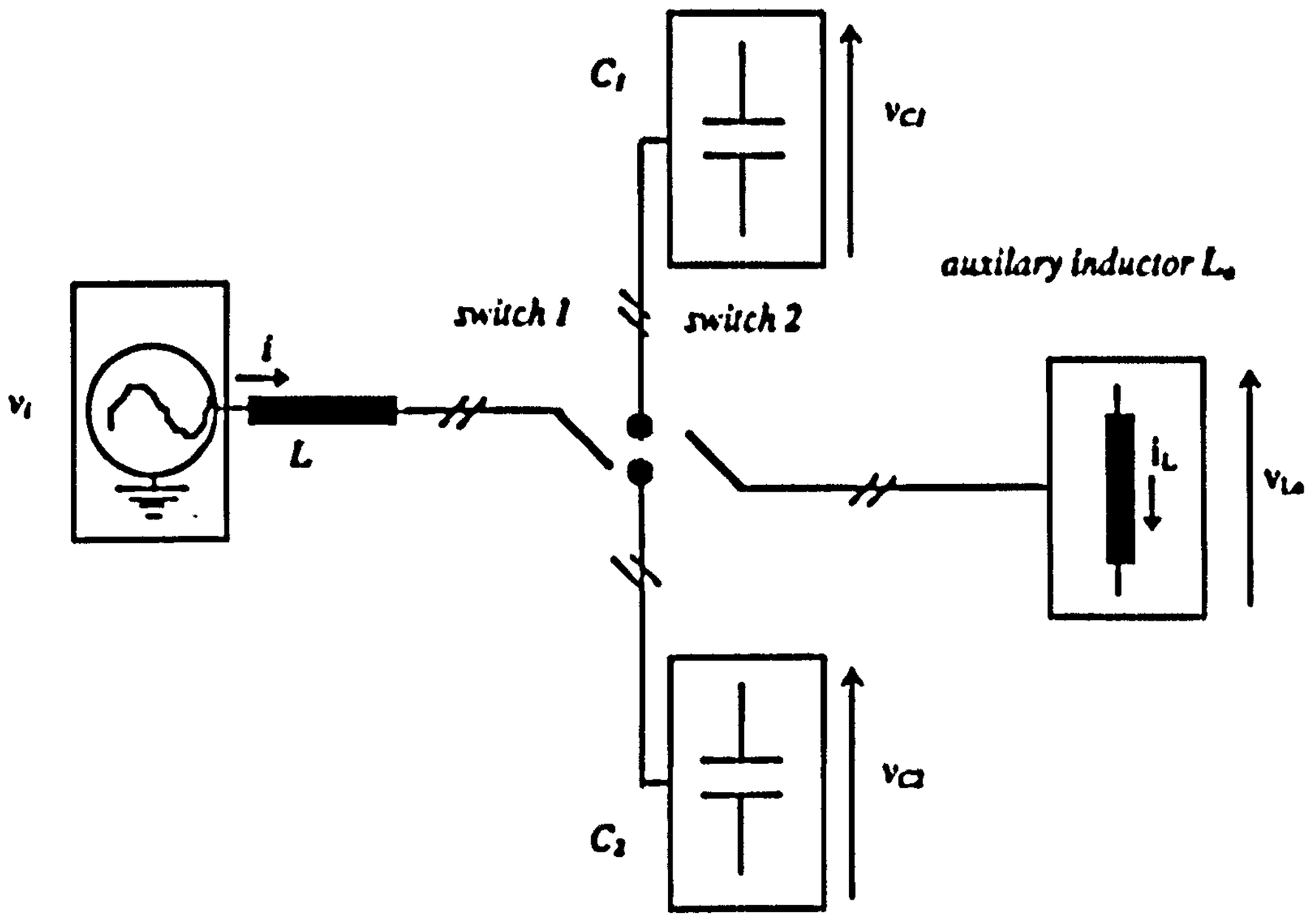


Figure 2.18 Functional diagram

The equations relating the circuit parameters are obtained as follows. When the capacitor C_1 is connected to the input supply and capacitor C_2 is connected to the auxiliary inductor L_a

$$\frac{di}{dt} = \frac{v_i - v_{c1}}{L}$$

$$\frac{d^2i}{dt^2} = \frac{1}{L}\frac{d(v_i - v_{c1})}{dt} = -\frac{1}{L}\frac{dv_{c1}}{dt} = -\frac{i}{LC_1}$$

$$\frac{di_L}{dt} = \frac{v_{c2}}{L_o}$$

When the capacitor C_2 is connected to the input supply and capacitor C_1 is connected to the auxiliary inductor L_o

$$\frac{di}{dt} = \frac{v_i - v_{c2}}{L}$$

$$\frac{d^2i}{dt^2} = \frac{1}{L}\frac{d(v_i - v_{c2})}{dt} = -\frac{1}{L}\frac{dv_{c2}}{dt} = -\frac{i}{LC_2}$$

$$\frac{di_L}{dt} = \frac{v_{c1}}{L_o}$$

For this circuit, as in the previous circuits, the resonance frequency of the inductor L and the capacitors should be less than the switching frequency. This makes it necessary to select a relatively large value of inductor or capacitor. Although, in this circuit, this does not have a significant effect on the rate of change of filter current, it limits the magnitude of the second derivitive; the choice of the sizes of the capacitors and the inductor is a matter of compromise. The practical implementation is shown in Figure 2.19 and presented in [Kanani-2 95]. Simulation results are shown in Figures 2.20 and 2.21.

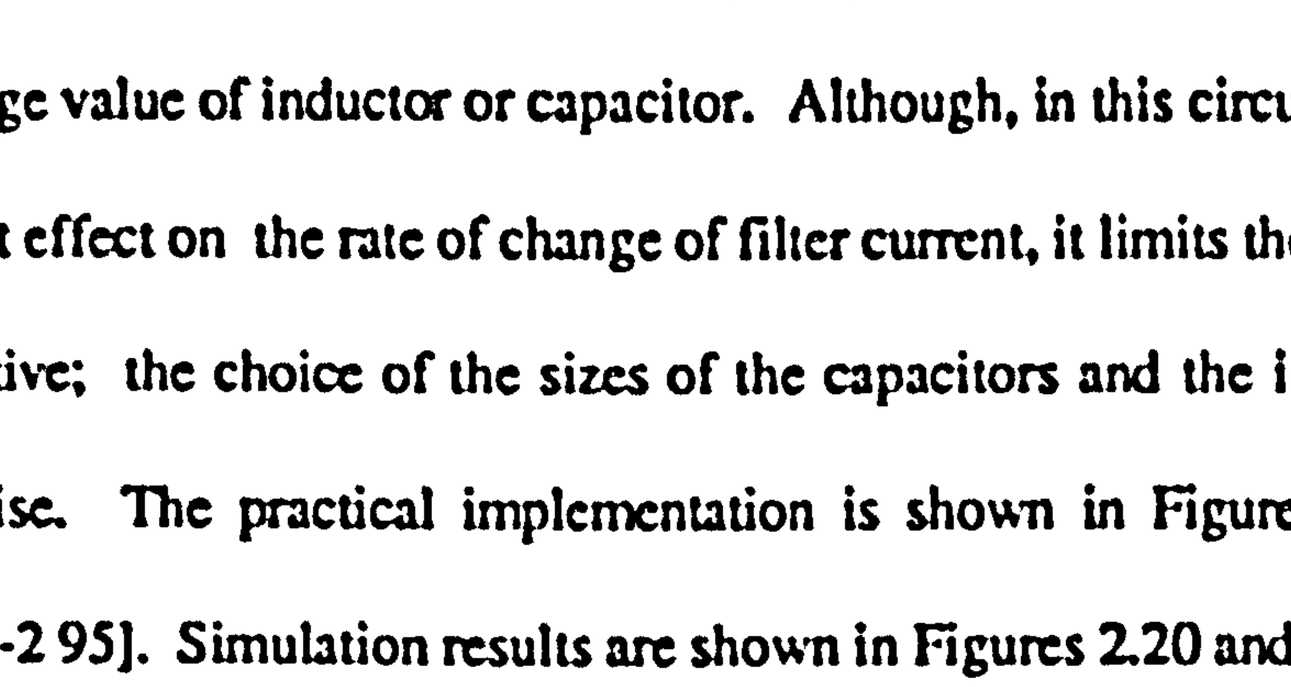


Figure 2.19 Practical circuit (new)

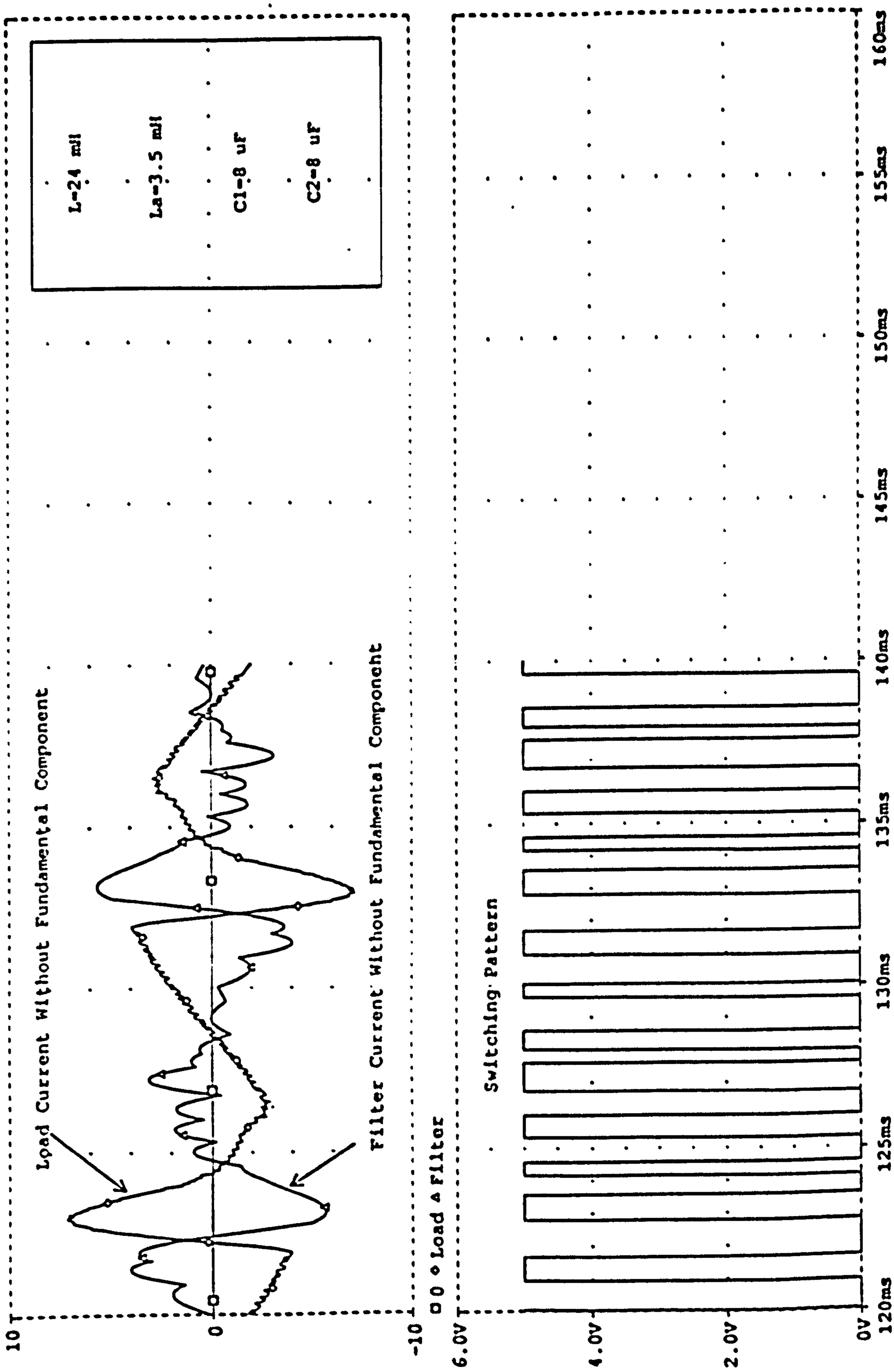


Figure 2.20 Simulation results of scheme No.6 section 2.5.1

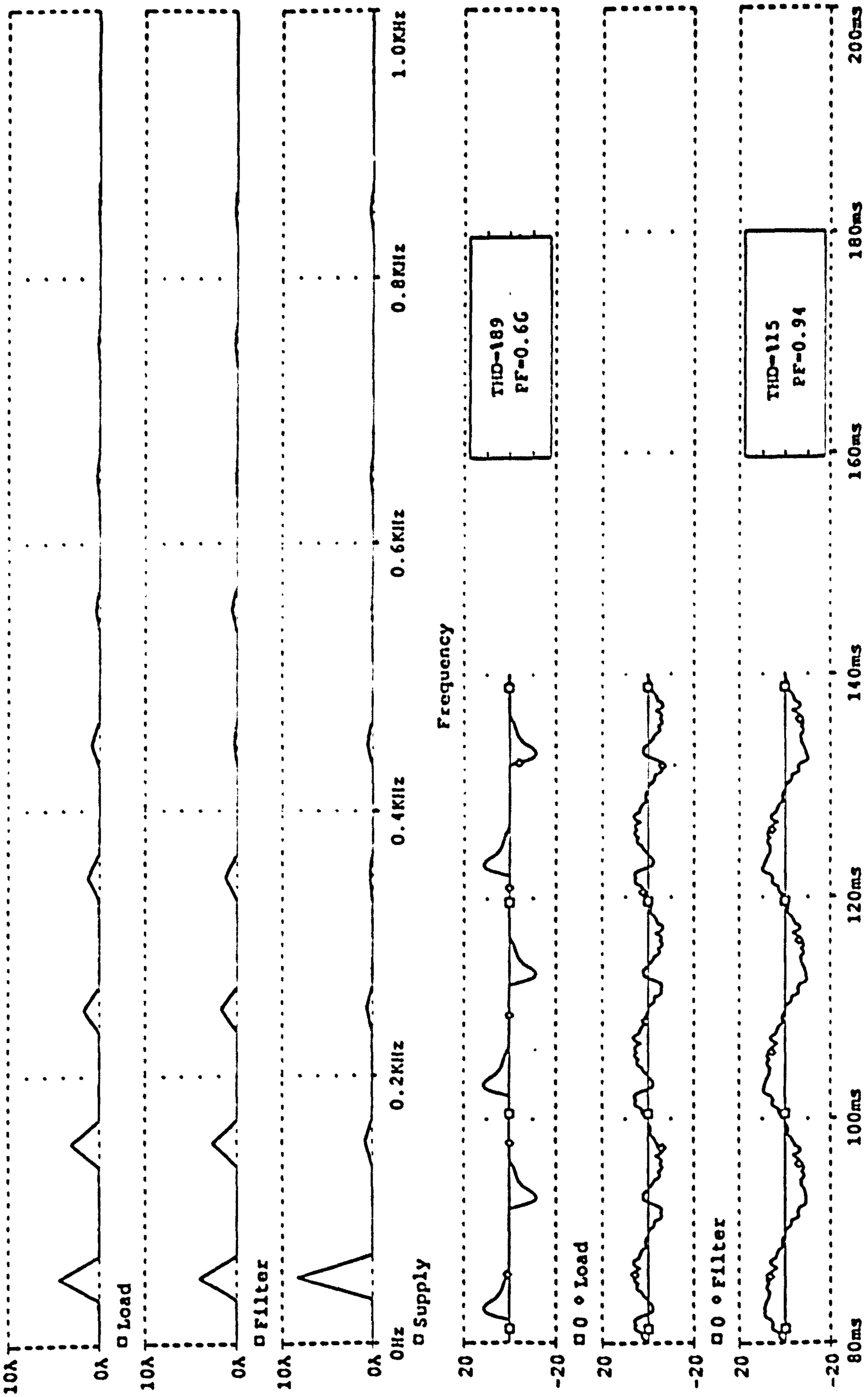


Figure 2.21 Second simulation results of scheme No.6 section 2.5.1

Compared with the previous circuits this configuration has increased losses because it uses an extra inductor.

(7) Floating terminal alternately connected to the two terminals of a resonant circuit, two capacitors and an auxiliary inductor (piecewise nonlinear approximation)

This is a new arrangement and is shown in Figure 2.22.

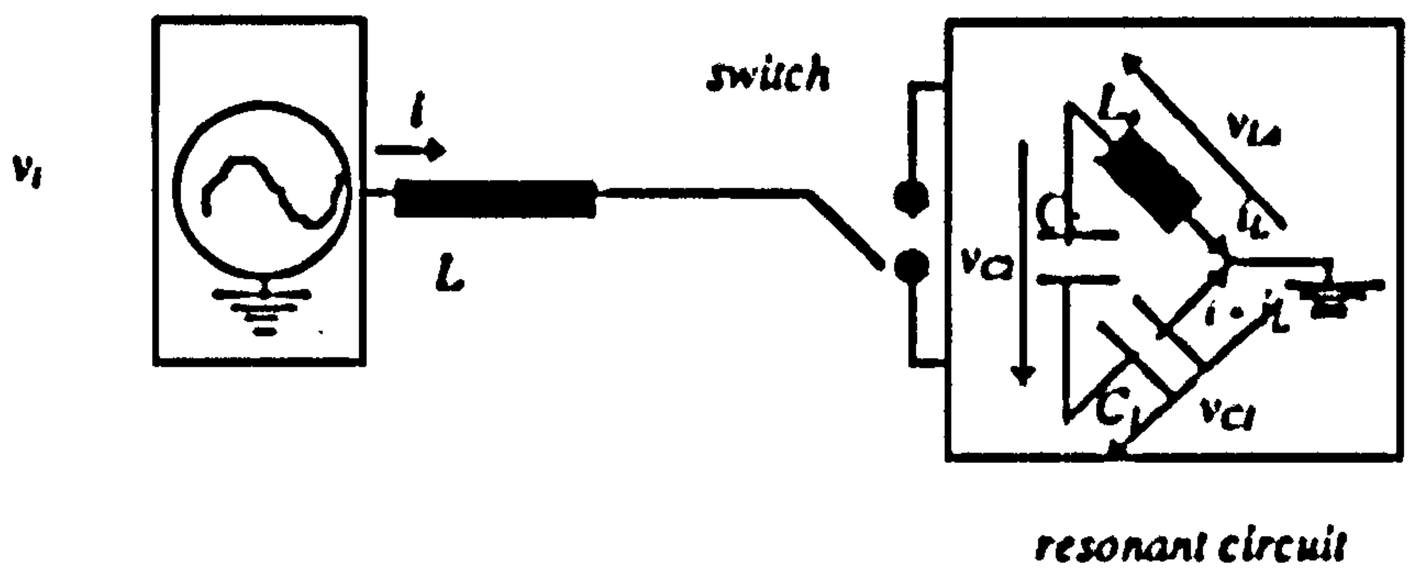


Figure 2.22 The functional diagram

As shown in the functional diagram, the voltage at the floating terminal of the inductor is equal to the voltage, v_{C1} , across capacitor 1 in one state and in other state it is equal to the voltage, v_{C1}- v_{C2}, across the two capacitors in series.

The two states of the switch can be represented by the following equations.

When the switch is in the position shown in the functional diagram

$$\frac{di}{dt} = \frac{v_i - v_{c1}}{L}$$

$$\frac{d^2i}{dt^2} = \frac{1}{L}\frac{d(v_i - v_{C1})}{dt} = -\frac{1}{L}\frac{dv_{C1}}{dt} = \frac{-i + i_L}{LC_1}$$

$$\frac{di_L}{dt} = \frac{v_{C1} - v_{C2}}{L_a}$$

$$\frac{dv_{C2}}{dt} = \frac{I_L}{C_2}$$

When the switch is in the alternative position

$$\frac{di}{dt} = \frac{v_i - v_{L_2}}{L} = \frac{v_i - v_{C1} + v_{C2}}{L}$$

$$\frac{d^2I}{dt^2} = \frac{1}{L}\frac{d(v_i - v_{C1} + v_{C2})}{dt} = \frac{1}{L}\left(\frac{dv_{C1}}{dt} - \frac{dv_{C2}}{dt}\right) = \frac{-I + I_L}{LC_1} + \frac{-I + I_L}{LC_2}$$

$$\frac{di_L}{dt} = \frac{v_{C1} - v_{C2}}{L_a}$$

$$\frac{dv_{C2}}{dt} = \frac{-(I - I_L)}{C_2}$$

These equations show that the change in di /dt of the filter current at the instant of switching is controlled by voltage, v_{C2}, across capacitor 2. This facilitates the control over the initial values of the rate of change of current as required for nonlinear approximation of the required current. Figure 2.23 illustrates a method of implementing this mode of control. The simulation results are shown in Figures 2.24 and 2.25.

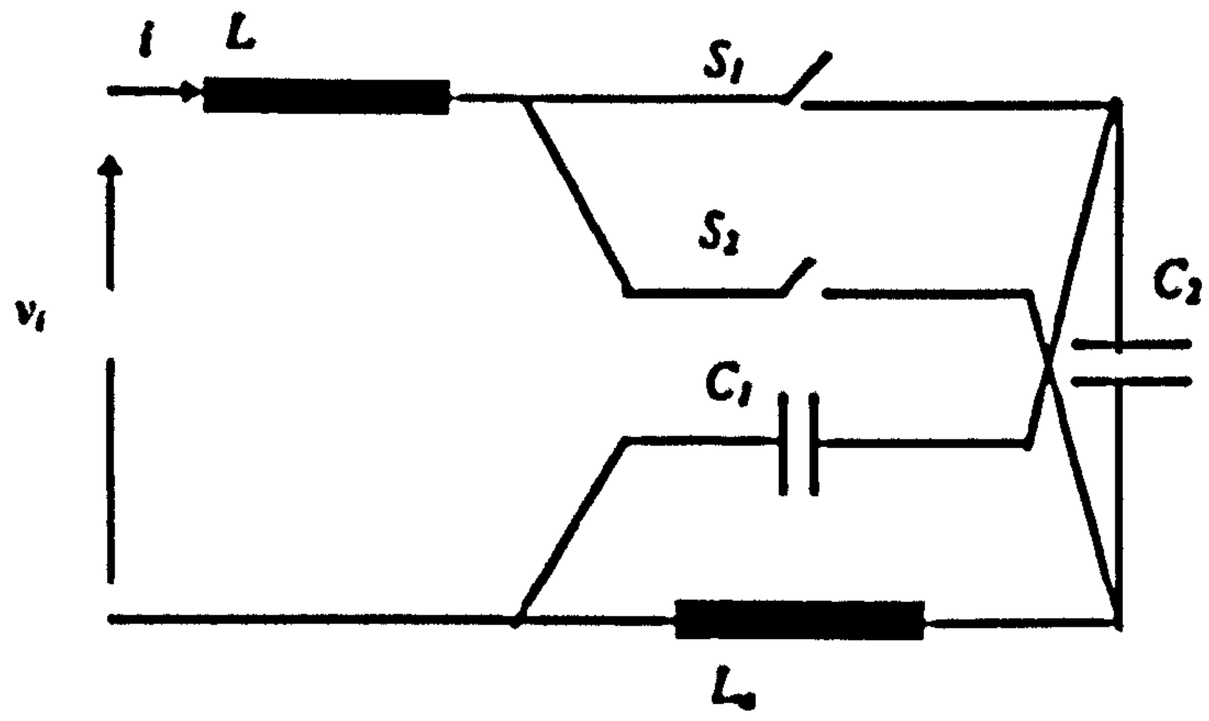


Figure 2.23 Practical circuit (new)

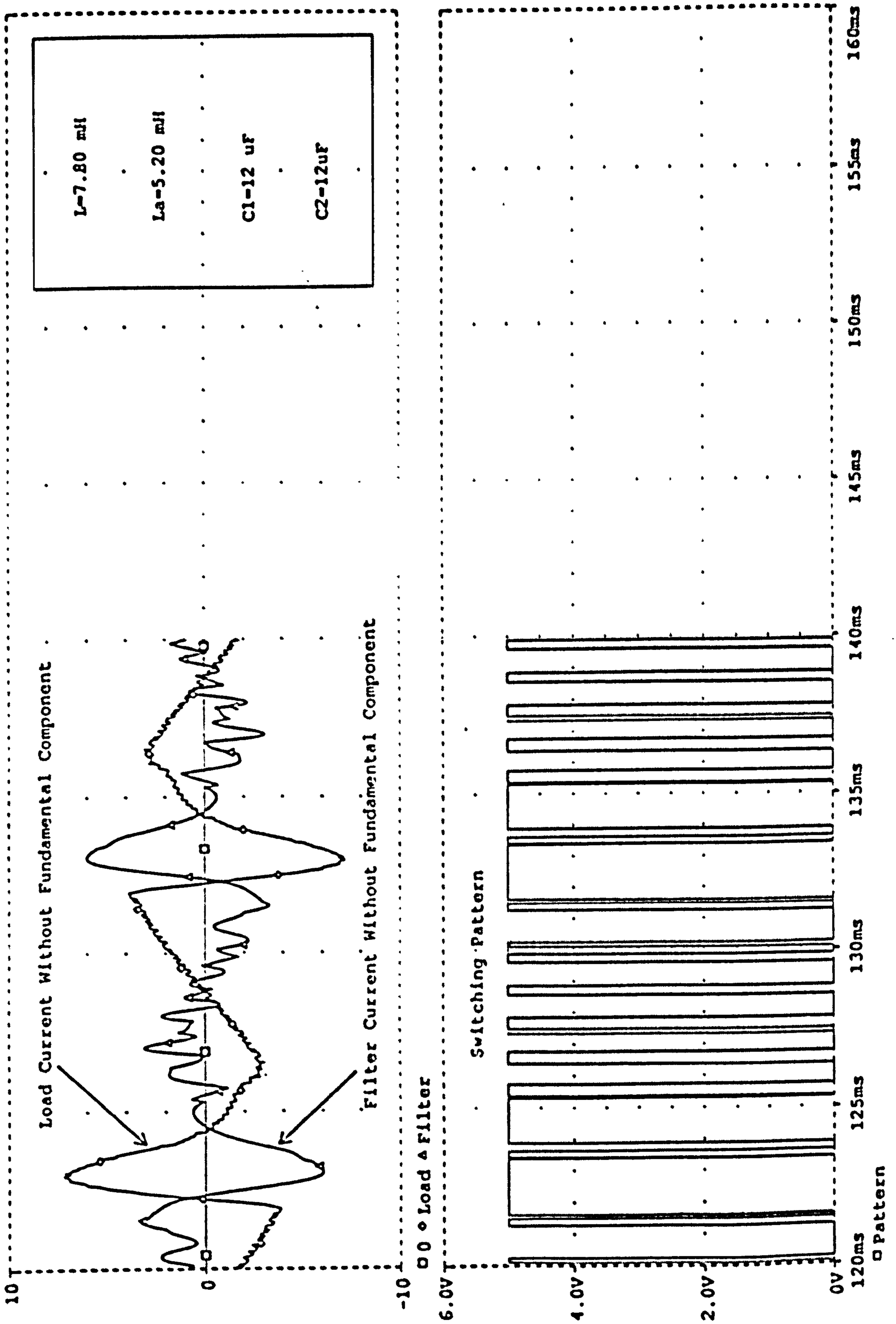


Figure 2.24 Simulation results of scheme No.7 section 2.5.1

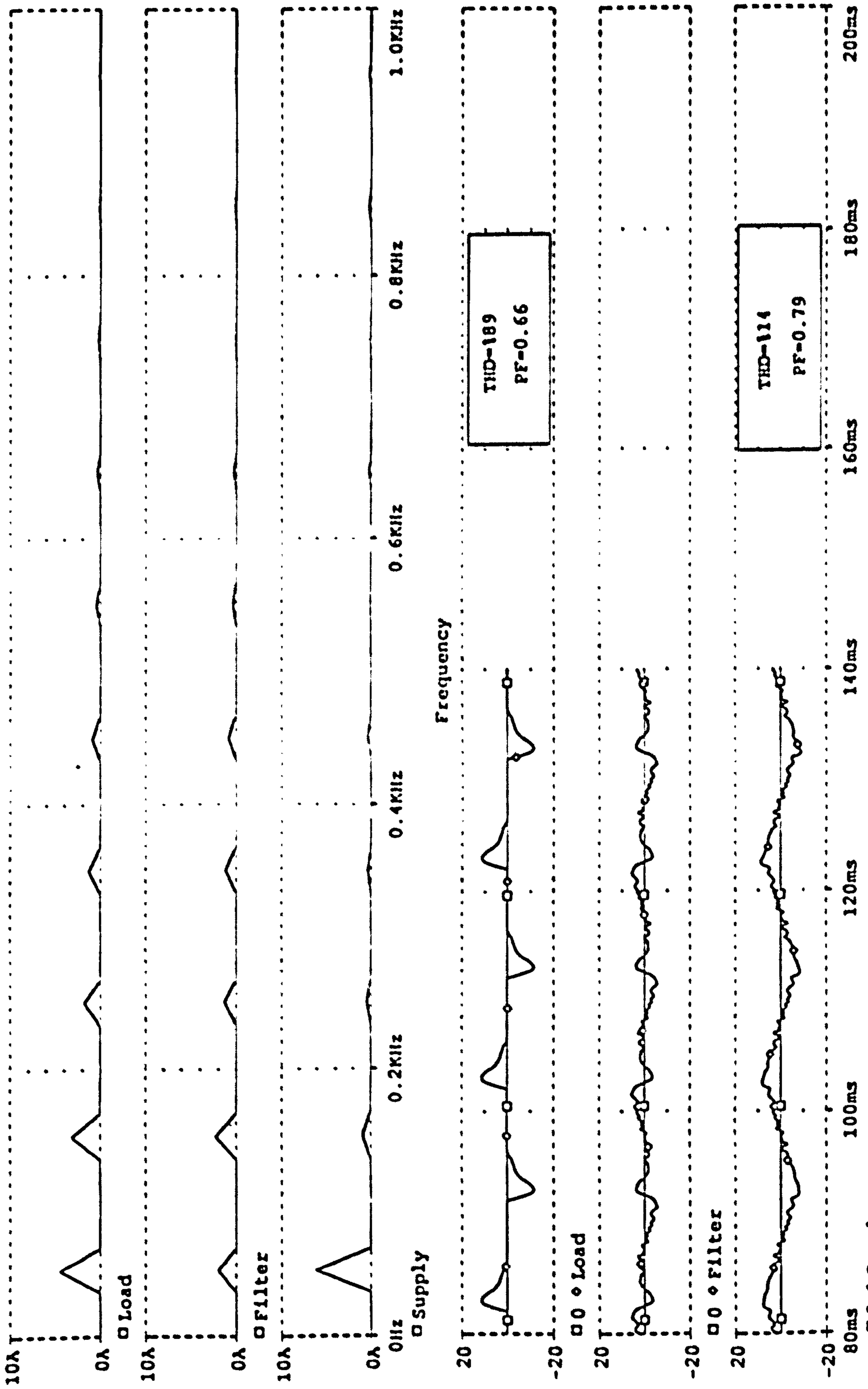


Figure 2.25 Second simulation results of scheme No.7 section 2.5.1

The disadvantage of achieving non-linear approximation using the resonant circuit here is that there is a presence of relatively high frequency harmonics in the resonant-loop. However these can be attenuated by using a relatively larger inductor or high frequency switching. Nevertheless the selection of components and switching patterns is a matter of compromise as described in Chapter 3.

(8) Floating terminal alternately connected to the two terminals of a resonant circuit - one capacitor and two auxiliary inductors (piecewise nonlinear approximation)

This is an alternative method of achieving piecewise non-linear approximation. This new arrangement is shown in Figure 2.26

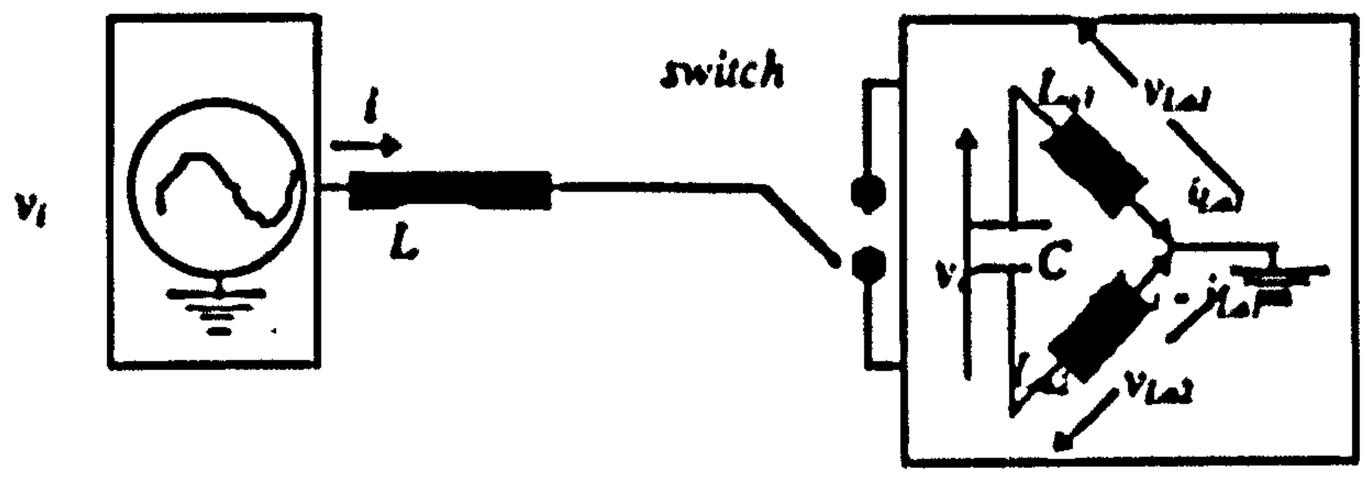


Figure 2.26 Functional diagram

As shown in the functional diagram, the voltage of the floating terminal of the inductor is equal to the voltage, v_{Le1} . across the inductor, L_{e1}, in one state and in other state it is equal to the voltage, v_{Le2}, across the inductor, L_{e2}.

The voltage across the inductor, L_{e2}, is given by

$$v_{Le2} = L_{e2}\frac{d(i-i_{Le1})}{dt} = L_{e2}\left(\frac{di}{dt} - \frac{di_{Le1}}{dt}\right)$$

Replacing $\frac{di_{L1}}{dt} = \frac{v_{L1}}{L_{a1}}$ in the above equation gives:

$$v_{L2} + \frac{L_{a2}}{L_{a1}} v_{L1} = L_{a2} \frac{di}{dt}$$

The relation between the voltages across the two inductors and voltage across the capacitor in the resonance circuit can be expressed by the following equation:

$$v_{L1} - v_{L2} = v_C$$

Solution of the above equations gives the voltage across the auxiliary inductors in terms of voltage across the capacitor and the rate of change of current di/dt.

$$v_{L1} = \frac{v_C - L_{a2} \frac{di}{dt}}{1 - \frac{L_{a2}}{L_{a1}}}$$

$$v_{L2} = \frac{v_C + L_{a1} \frac{di}{dt}}{1 - \frac{L_{a1}}{L_{a2}}}$$

Then the equations relating the two states of the switch are summarised below.

When the switch is in the position shown in the functional diagram

$$\frac{di}{dt} = \frac{v_i - v_{L2}}{L} = \ldots = \frac{v_i + \frac{L_{a2}}{(L_{a1} + L_{a2})} v_C}{L + \frac{L_{a1} L_{a2}}{(L_{a1} + L_{a2})}}$$

Assuming that the supply voltage is constant during the switching periods

$$\frac{d^2 i}{dt^2} = \frac{L_{a2}}{L(L_{a1} + L_{a2}) + L_{a1} L_{a2}} \frac{dv_C}{dt} = \frac{L_{a2}}{L(L_{a1} + L_{a2}) + L_{a1} L_{a2}} \frac{-i_{La}}{C}$$

$$\frac{di_{La}}{dt} = \frac{v_{La1}}{L_{a1}} = \frac{v_C + L_{a2}\frac{di}{dt}}{L_{a1} - L_{a2}}$$

When the switch is in the alternative position

$$\frac{di}{dt} = \frac{v_i - v_{La1}}{L} = \ldots = \frac{v_i - \frac{L_{a1}}{(L_{a1}+L_{a2})}v_C}{L + \frac{L_{a1}L_{a2}}{L_{a1}+L_{a2}}}$$

$$\frac{d^2i}{dt^2} = \frac{-L_{a1}}{L(L_{a1}+L_{a2})+L_{a1}L_{a2}}\frac{dv_C}{dt} = \frac{L_{a1}}{L(L_{a1}+L_{a2})+L_{a1}L_{a2}}\frac{i_{La}-i}{C}$$

$$\frac{di_{La}}{dt} = \frac{v_{La1}}{L_{a1}} = \frac{v_C + L_{a2}\frac{di}{dt}}{L_{a1} - L_{a2}}$$

The above equations show that the rate of change of current is controlled by the voltage across the capacitor with respect to the input voltage. Compatred with the previous circuit this circuit employs three inductors thereby introducing higher losses.

Figure 2.27 illustrates a method of implementing this mode of control and Figures 2.28 and 2.29 show the simulation results.

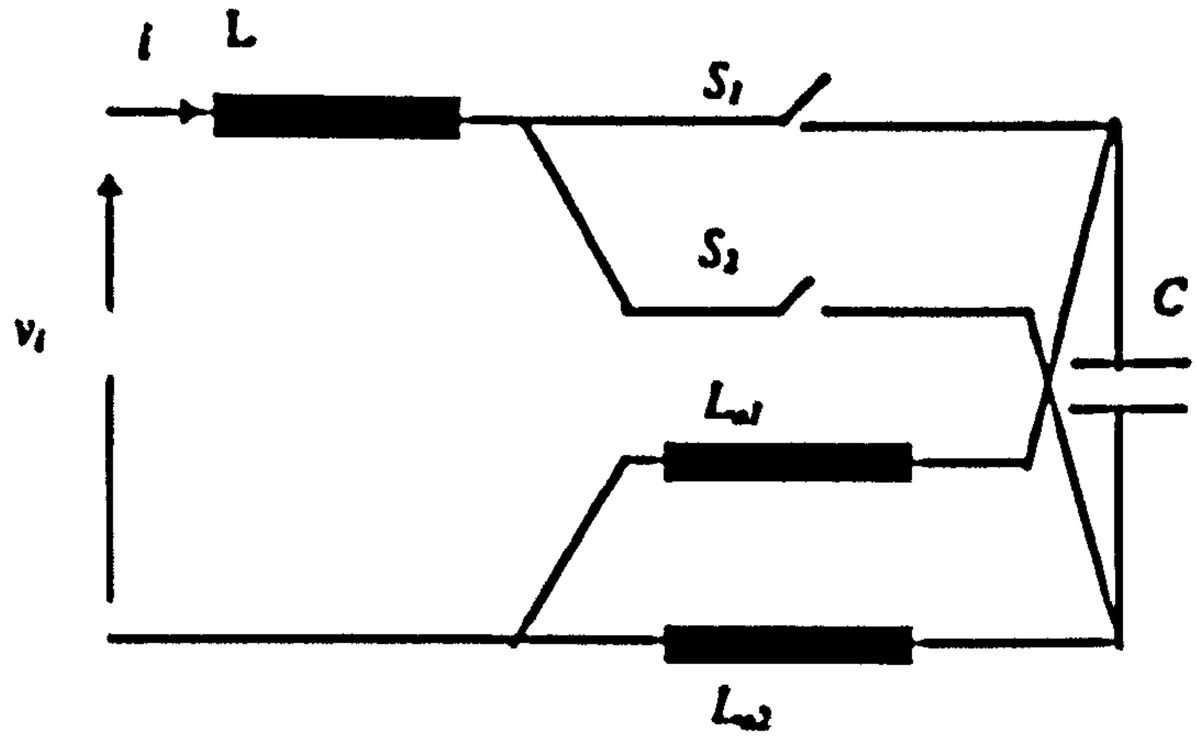


Figure 2.27 Practical circuit (new)

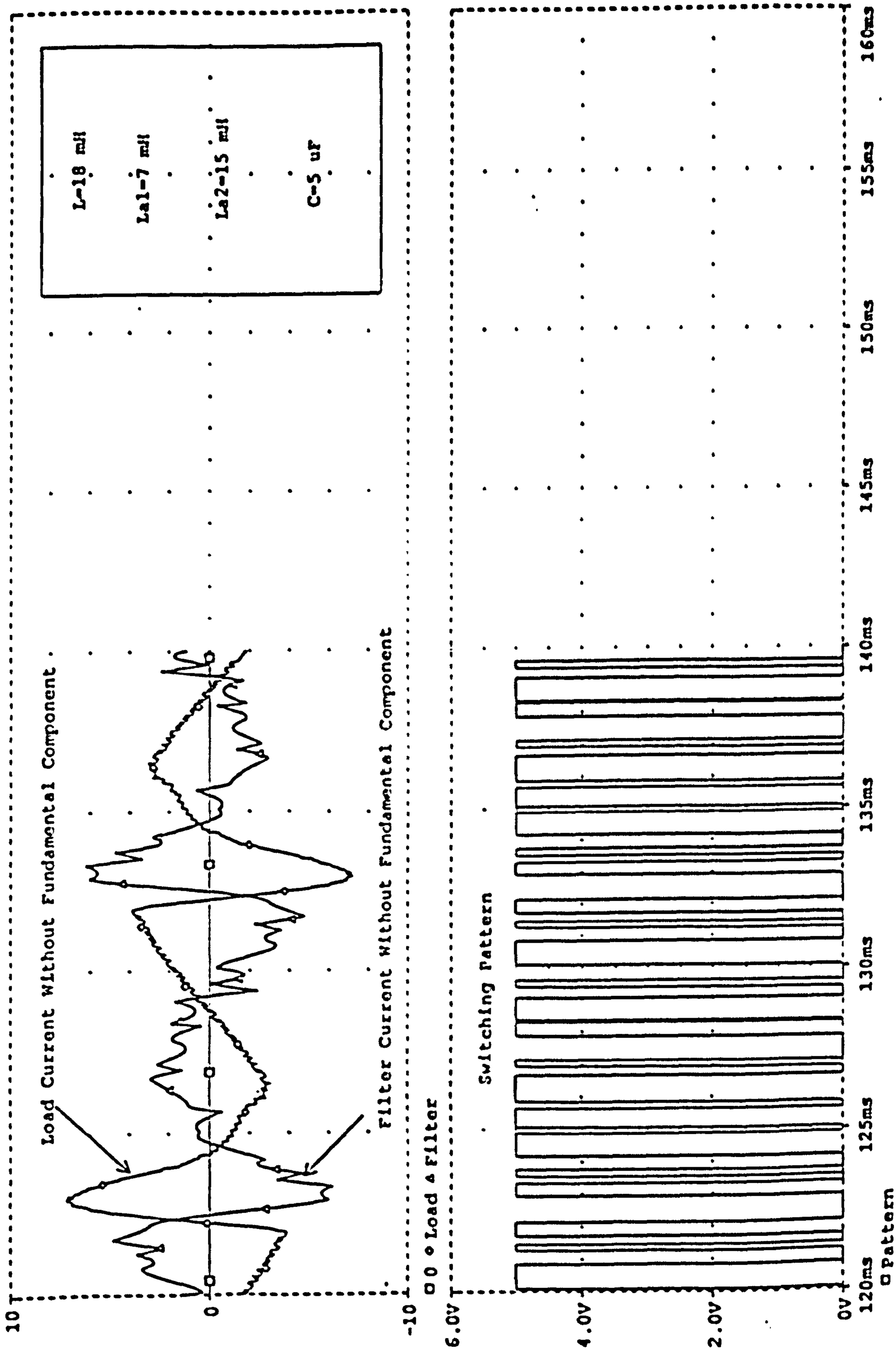


Figure 2.28 Simulation results of scheme No.8 section 2.5.1

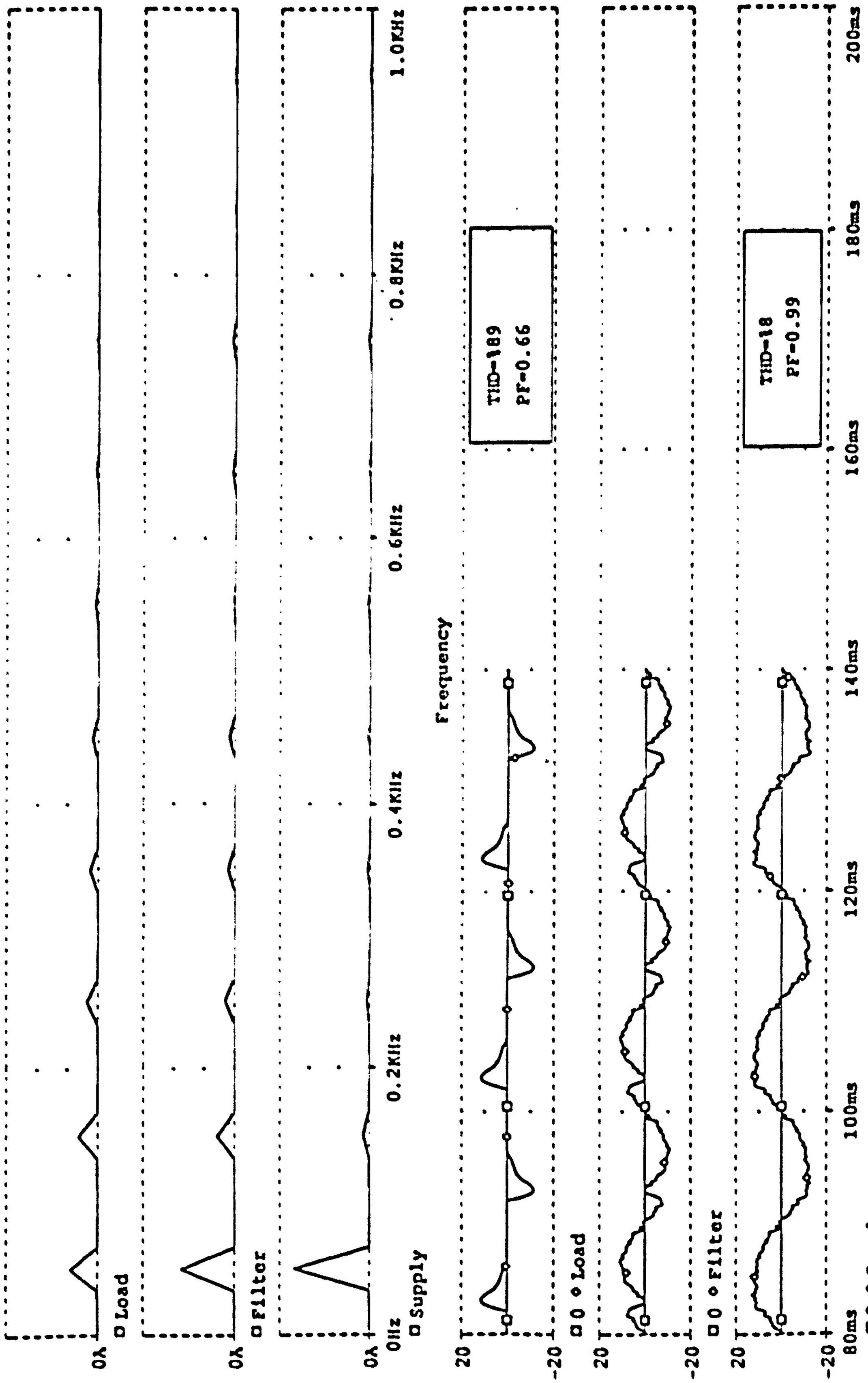


Figure 2.29 Second simulation results of scheme No.8 section 2.5.1

2.5.2 Both terminals of the inductor floating

The group of circuits in this category belong to the piecewise linear discontinuous mode.

The main distinguishing characteristic of these circuits is that the filter current has significant quantity of higher order harmonics and therefore it may be necessary in some of these circuits to include passive filters.

(1) The floating terminals are alternately connected to the supply and short circuited (piecewise linear discontinous approximation method)

This arrangement is shown in Figure 2.30. The filter current is the sum of the currents in the two inductors during their connection periods to the supply and related as follows.

When inductor 1 is connected to the supply and the other one is short-circuited:

$$i = i_1$$

$$\frac{di}{dt} = \frac{di_1}{dt} = \frac{v_1}{L_1}$$

$$\frac{di_2}{dt} = 0$$

When inductor 2 is connected to the supply and the other one is short-circuited.

$$i = i_2$$

$$\frac{di}{dt} = \frac{di_2}{dt} = \frac{v_1}{L_2}$$

$$\frac{di_1}{dt} = 0$$

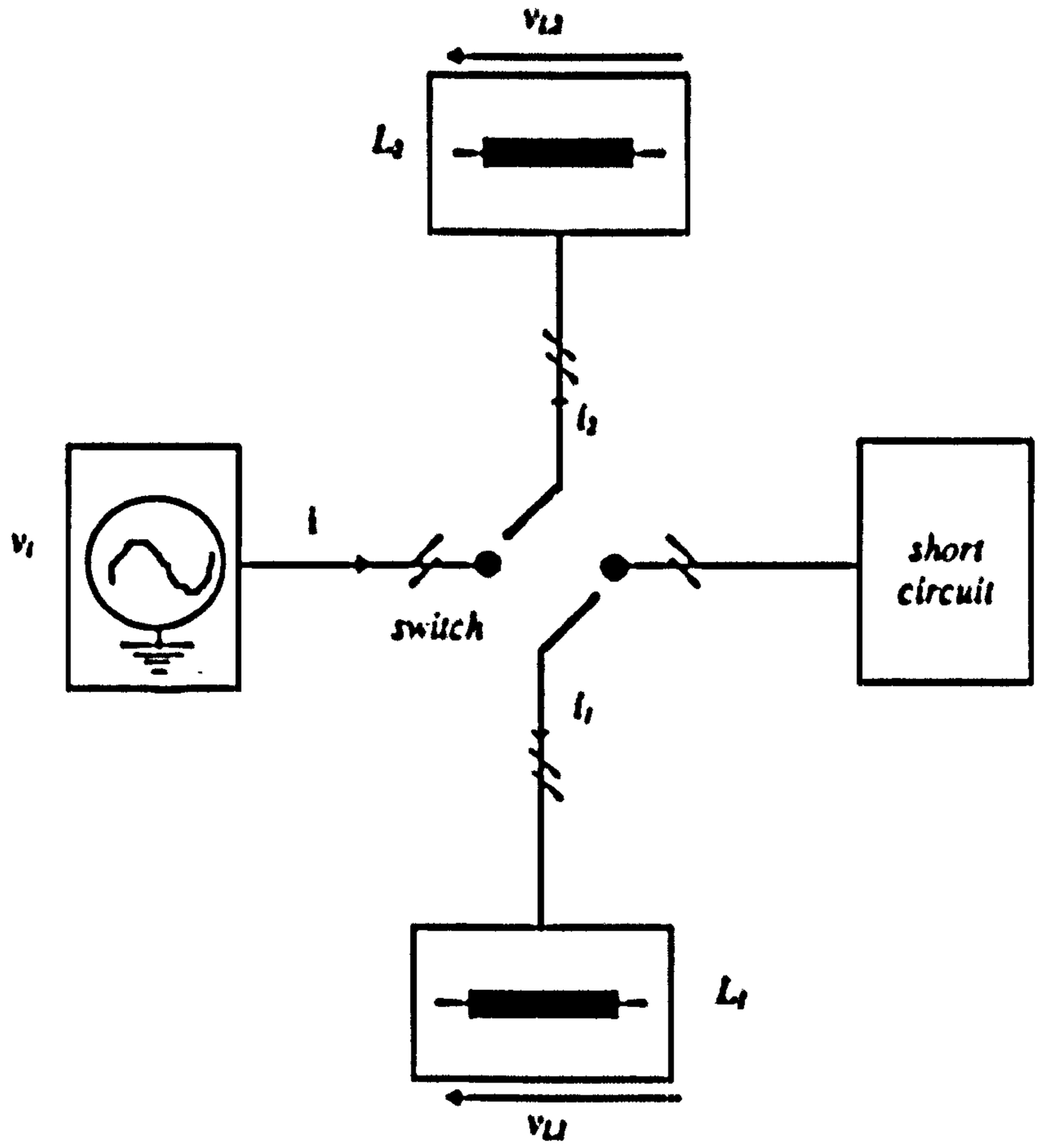


Figure 2.30 Functional diagram

These equations show that the di/dt of the current in the inductor is of the same polarity as the supply voltage when they are connected to it. The current in the inductors, when they are short-circuited, remains constant, assuming that there are no losses in the inductors. This implies that the inductors are energised during one half-cycle of the supply voltage and deenergised during the other half-cycle of the supply. Therefore, compared with the previous structures, the fundamental component of the current has a much higher magnitude. Further, the rate at which the filter current can be controlled is slower than in the previous circuits, making this circuit rather inflexible. The practical implementation of this circuit is shown in Figure 2.31 .

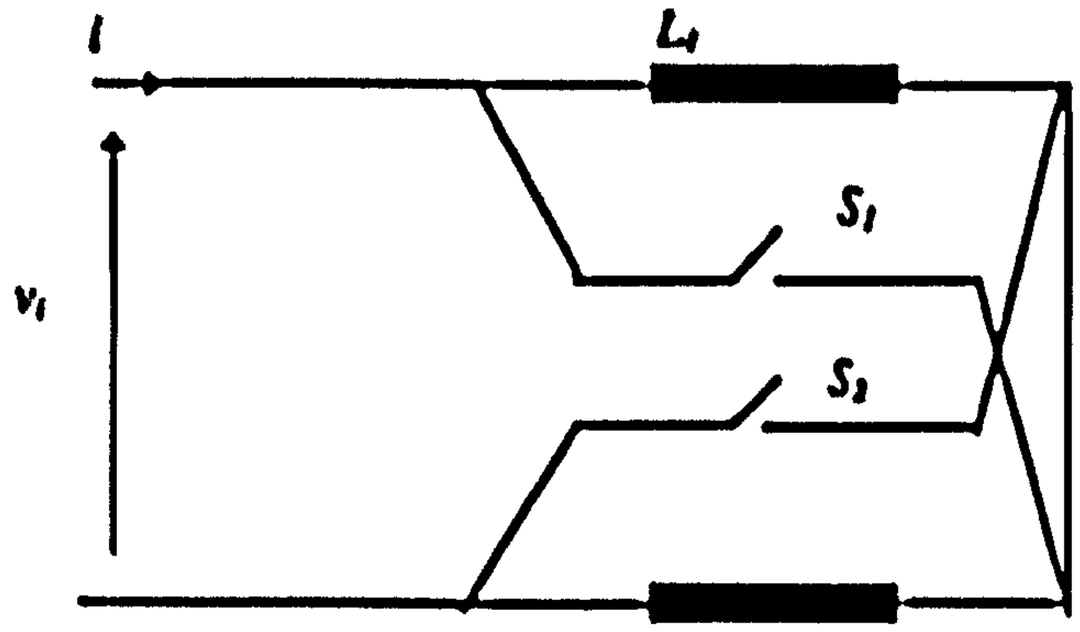


Figure 2.31 Practical circuit

(2) Floating terminals alternately connected to the supply and a capacitor

(piecewise linear discontinuous approximation)

The new arrangement is shown in Figure 2.32. The filter current is the sum of the two inductors currents during their connection periods to the supply.

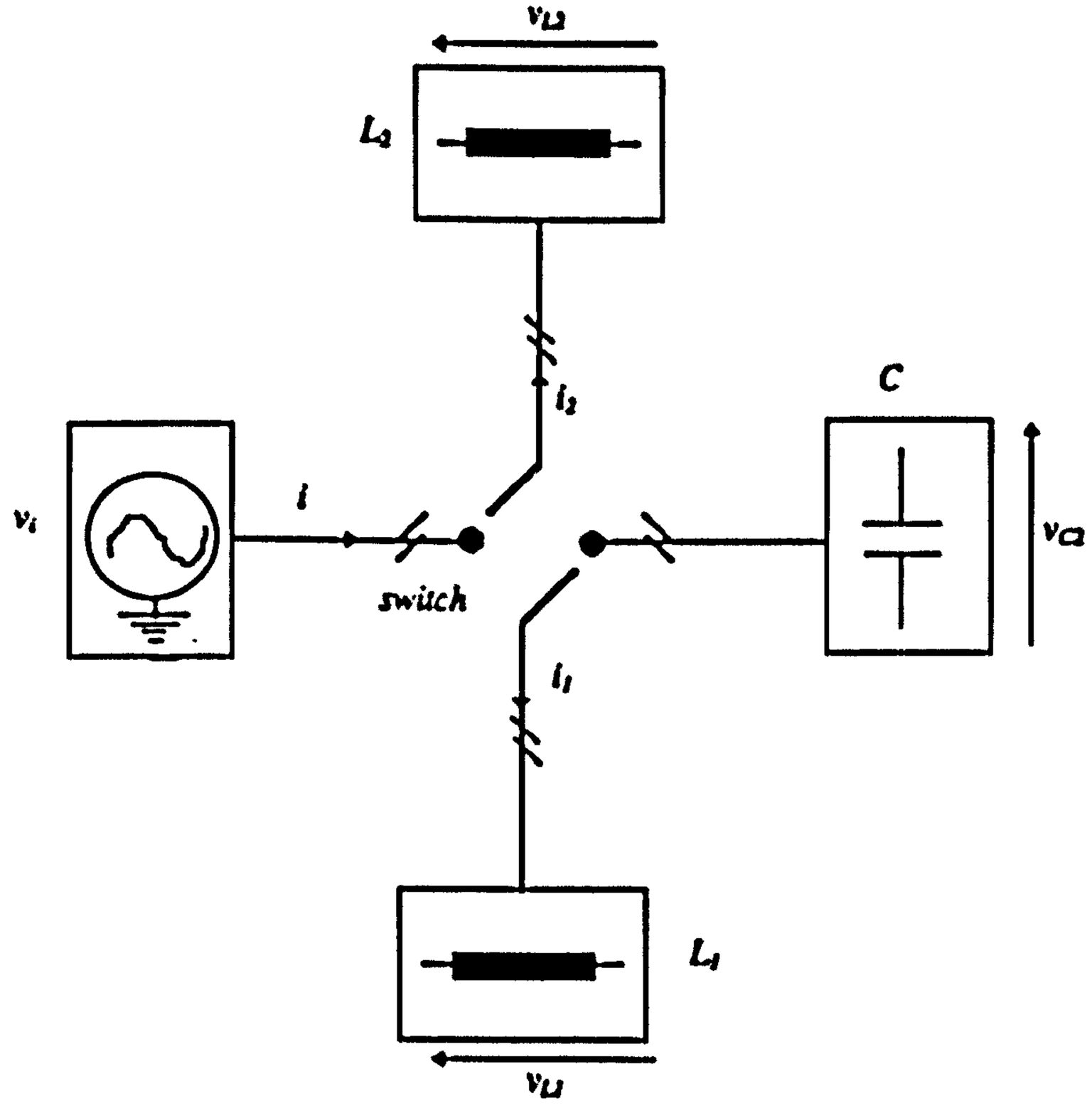


Figure 2.32 Functional diagram

The following equations can be written for two states of the switches.

When L_1 is connected to the supply and the other one is in parallel with the capacitor :

$$i = i_1$$

$$\frac{di}{dt} = \frac{di_1}{dt} = \frac{v_i}{L_1}$$

$$\frac{di_2}{dt} = \frac{v_c}{L_2}$$

When L_2 is connected to the supply and the other one is in parallel with the capacitor :

$$i = i_2$$

$$\frac{di}{dt} = \frac{di_2}{dt} = \frac{v_i}{L_2}$$

$$\frac{di_1}{dt} = \frac{v_c}{L_1}$$

The equations show that the di/dt of the current in the inductor is of the same polarity as the supply voltage when they are connected to it. In the previous circuit (1), the current in the inductor is controlled by the supply voltage. However in this circuit, currents in the inductors can be controlled more flexibly via the resonant circuits. It should be noted that the resonant current within the filter does not appear in the filter current. A practical implementation for this approach is shown in Figure 2.33 and simulated results are illustrated in Figure 2.34 and 2.35.

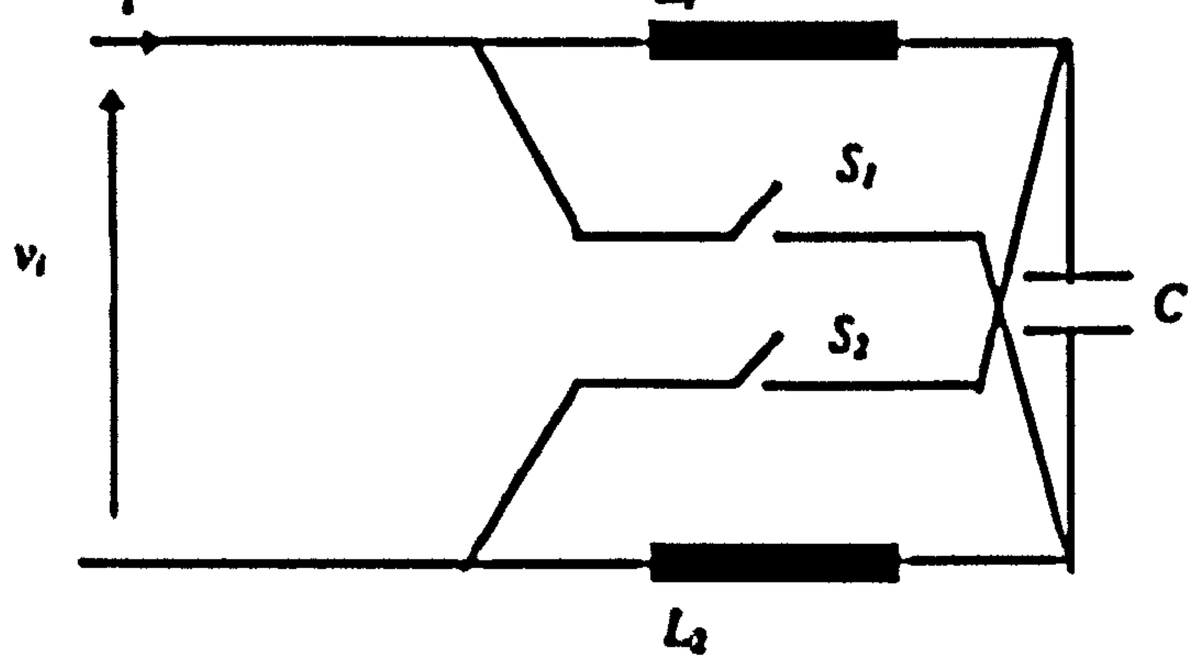


Figure 2.33 Practical circuit (new)

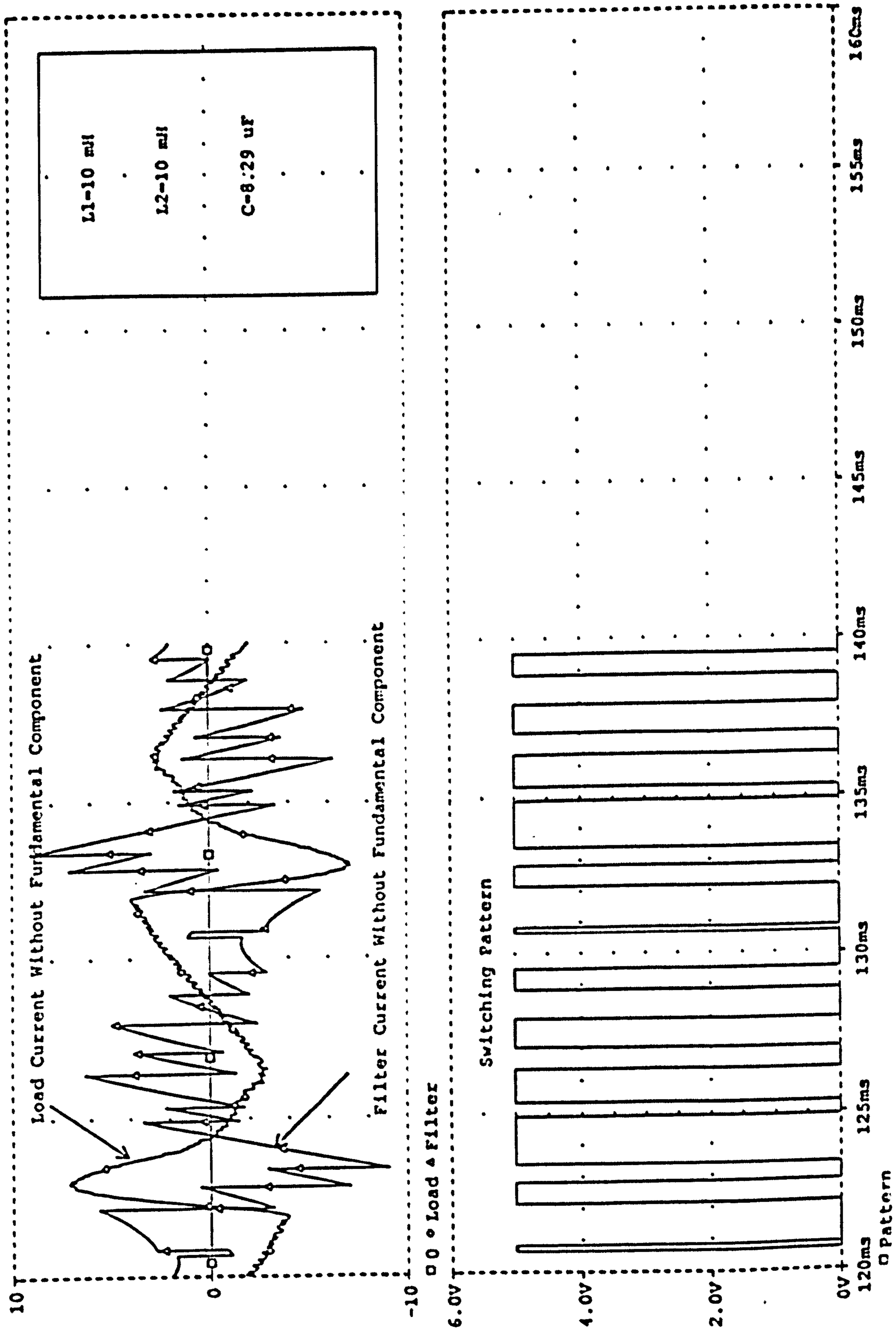


Figure 2.34 Simulation results of scheme No.2 section 2.5.2

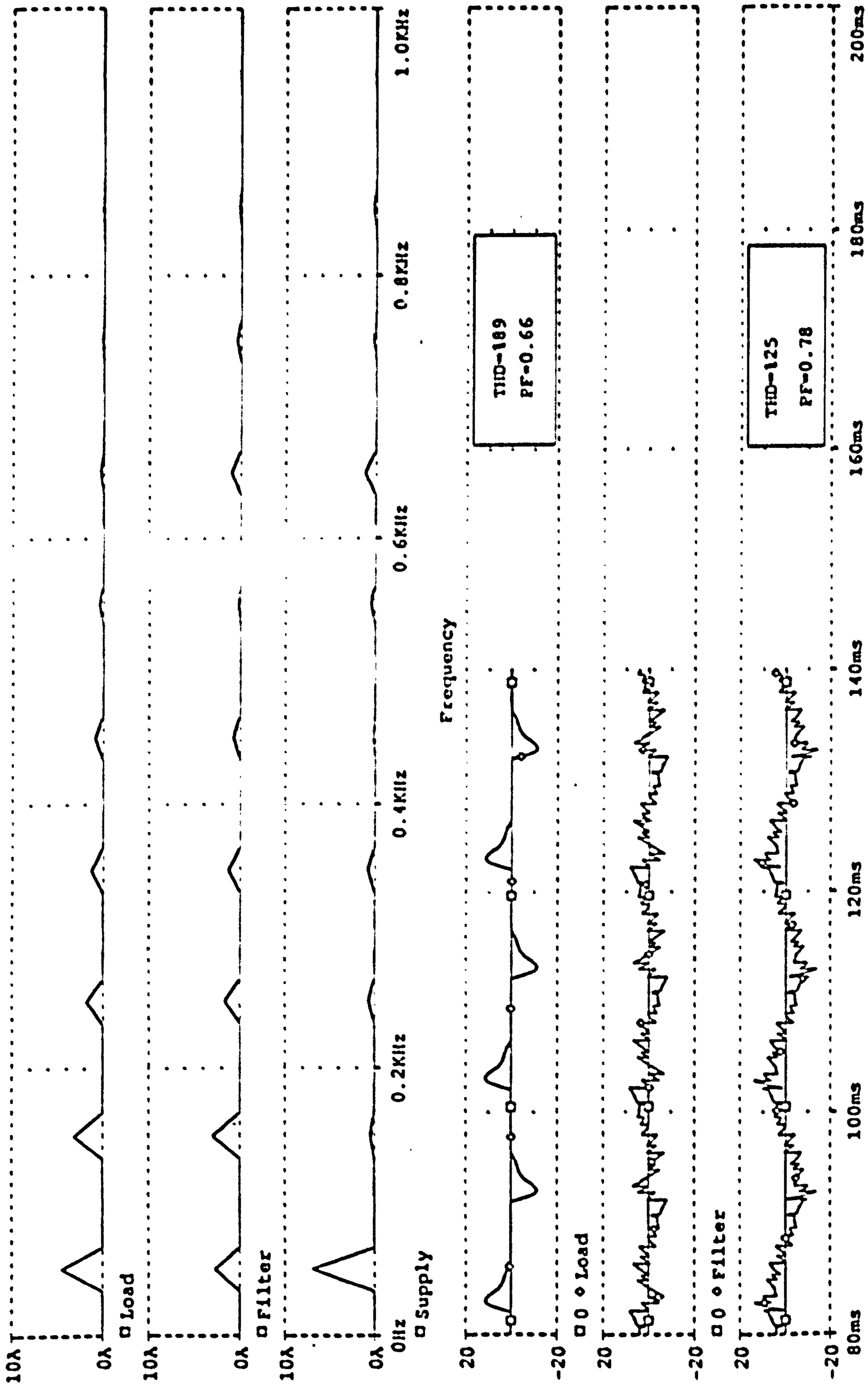


Figure 2.35 Second simulation results of scheme No.2 section 2.5.2

This circuit has basically the same drawback as those for techniques (1), (2) and (4) in section 2.5.1 in that for a given size of inductor, the circuit does not have the flexibility to track any rapid variations in the required current. In those circuits it was possible to increase the switching frequency to overcome this problem. However in this circuit the switching frequency is limited because of the time required for the inductor to energise and deenergise via the capacitor.

(3) Floating terminals of the inductor alternately connected to the two supply terminals

The arrangement is shown in Figure 2.36.

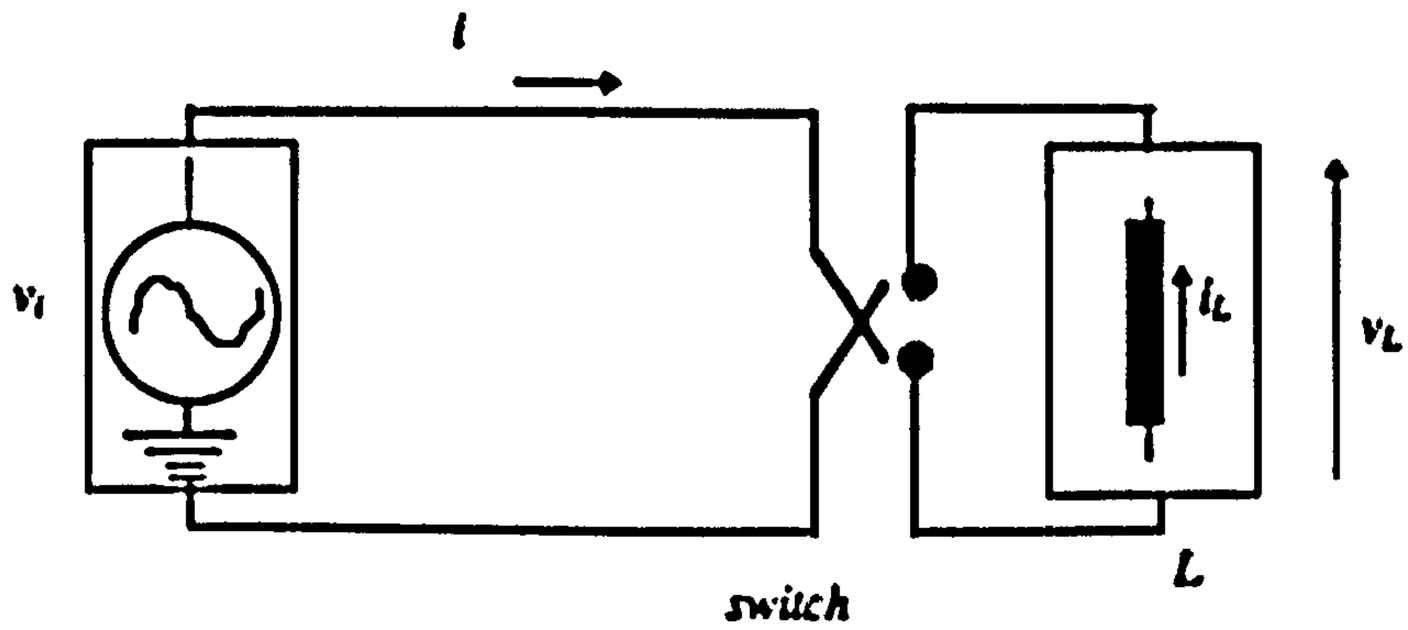


Figure 2.36 Functional diagram

This approach can be represented in the two states by the following equation.

When the switch is in the position shown in the functional diagram

$$i = i_L$$

$$\frac{di_L}{dt} = \frac{di}{dt} = \frac{v_L}{L}$$

When the switch is in the alternative position

$$i = -i_L$$

$$\frac{di_L}{dt} = -\frac{di}{dt} = -\frac{v_L}{L}$$

Because of the 'severity' of the discontinuity in the filter current i.e. at every instant of switching it changes from a negative to a positive value, the filter current contains a much higher proportion and magnitude of higher order harmonics. In practice to alleviate this problem, often an auxiliary passive low-pass series filter is employed [Hayashi 88] as shown in Figure 2.37. Of course it would also be possible to use another active filter instead.

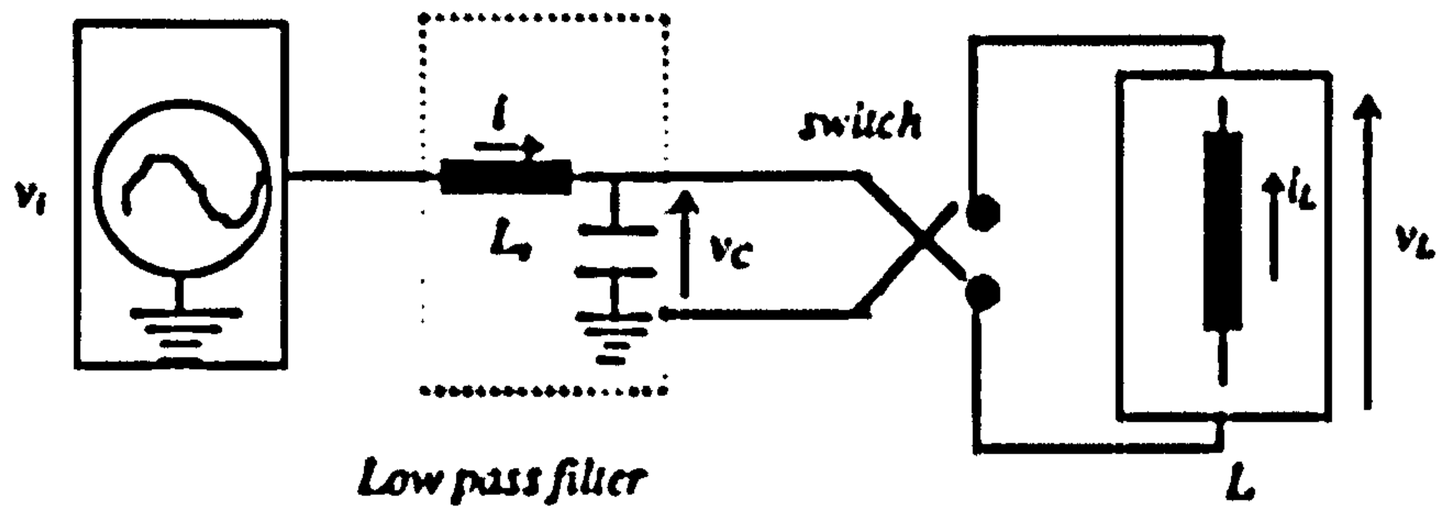


Figure 2.37 Functional diagram including passive filter

The rate of change of current, di /dt, in this modified arrangement can be represented by the following equation.

$$\frac{di}{dt} = \frac{v_i - v_c}{L_s}$$

This implies that the di /dt is a continuous function because the voltage across the capacitor is continuous. Assuming that the supply voltage during the switching periods is constant, then

$$\frac{d^2i}{dt^2} = \frac{1}{L_s}\frac{d(v_i - v_c)}{dt} = -\frac{1}{L_s}\frac{dv_c}{dt}$$

The rate of change of voltage across the capacitor depends on the position of the switch and can be expressed by the following equations.

When the switch is in the position shown in the functional diagram

$$\frac{dv_C}{dt} = \frac{I - I_L}{C}$$

$$\frac{di_L}{dt} = \frac{v_C}{L}$$

If the switch is in the alternative position

$$\frac{dv_C}{dt} = \frac{I + I_L}{C}$$

$$\frac{di_L}{dt} = \frac{v_C}{L}$$

These equations imply that the rate of change of the capacitor voltage varies with the switching operation and as a consequence this can provide the required flexibility over the control of the rate of change of the filter current. This approach is another example of the use of piecewise non-linear approximation method.

A practical implementation of this method is shown in the Figure 2.38. The pairs of switches S_1 ,S_2 and S_3 , S_4 operate in anti-phase. The simulation results are presented in Figures 2.39 and 2.40.

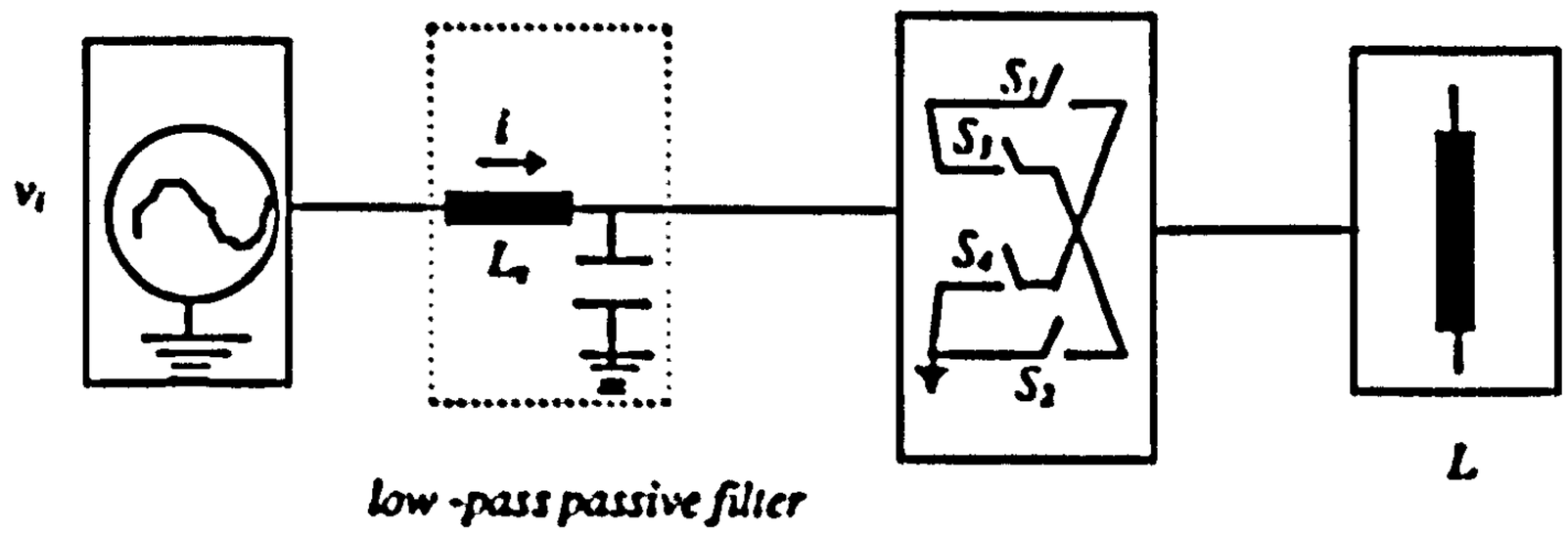


Figure 2.38 Practical circuit (new)

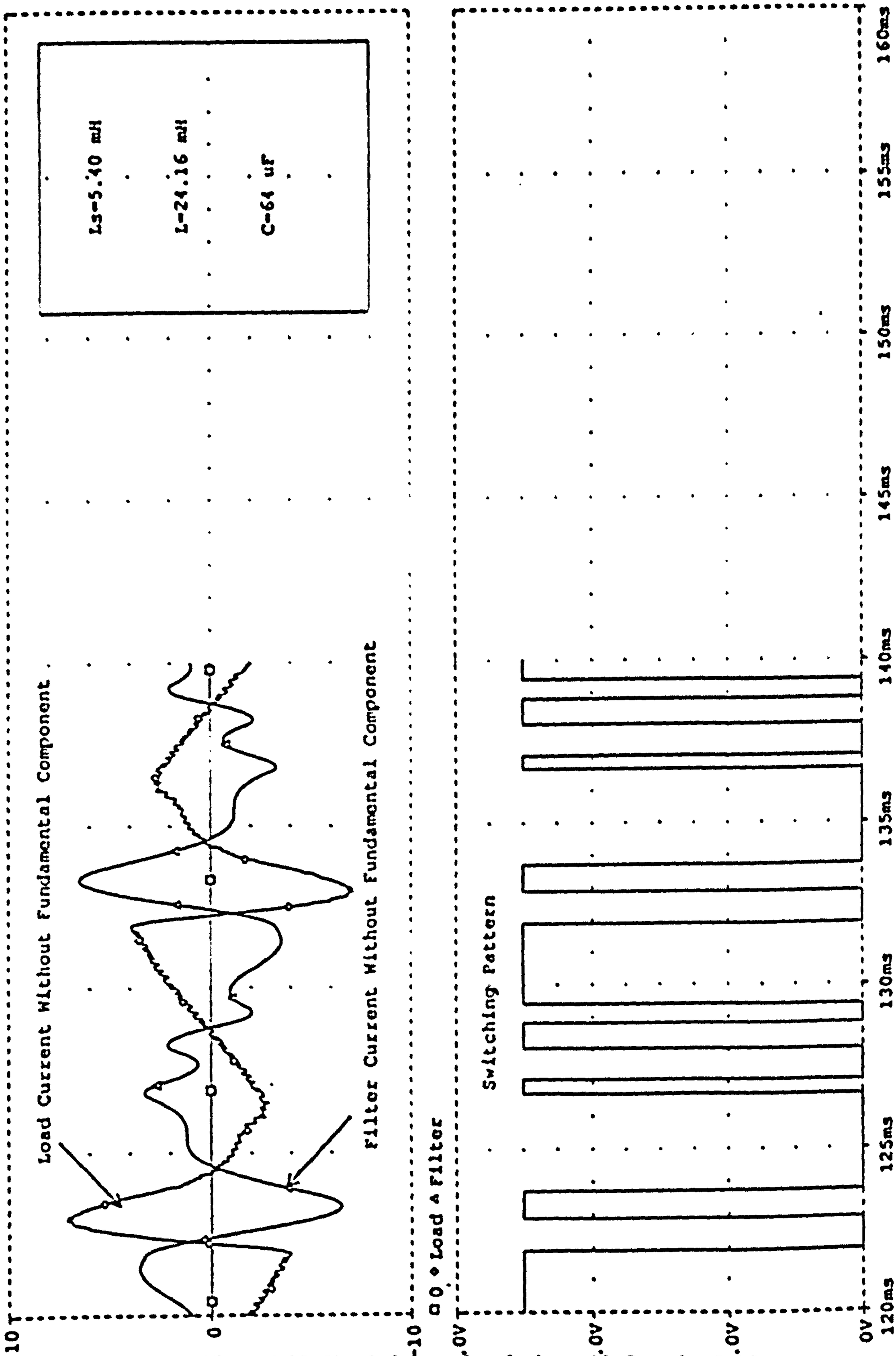


Figure 2.39 Simulation results of scheme No.3 section 2.5.2

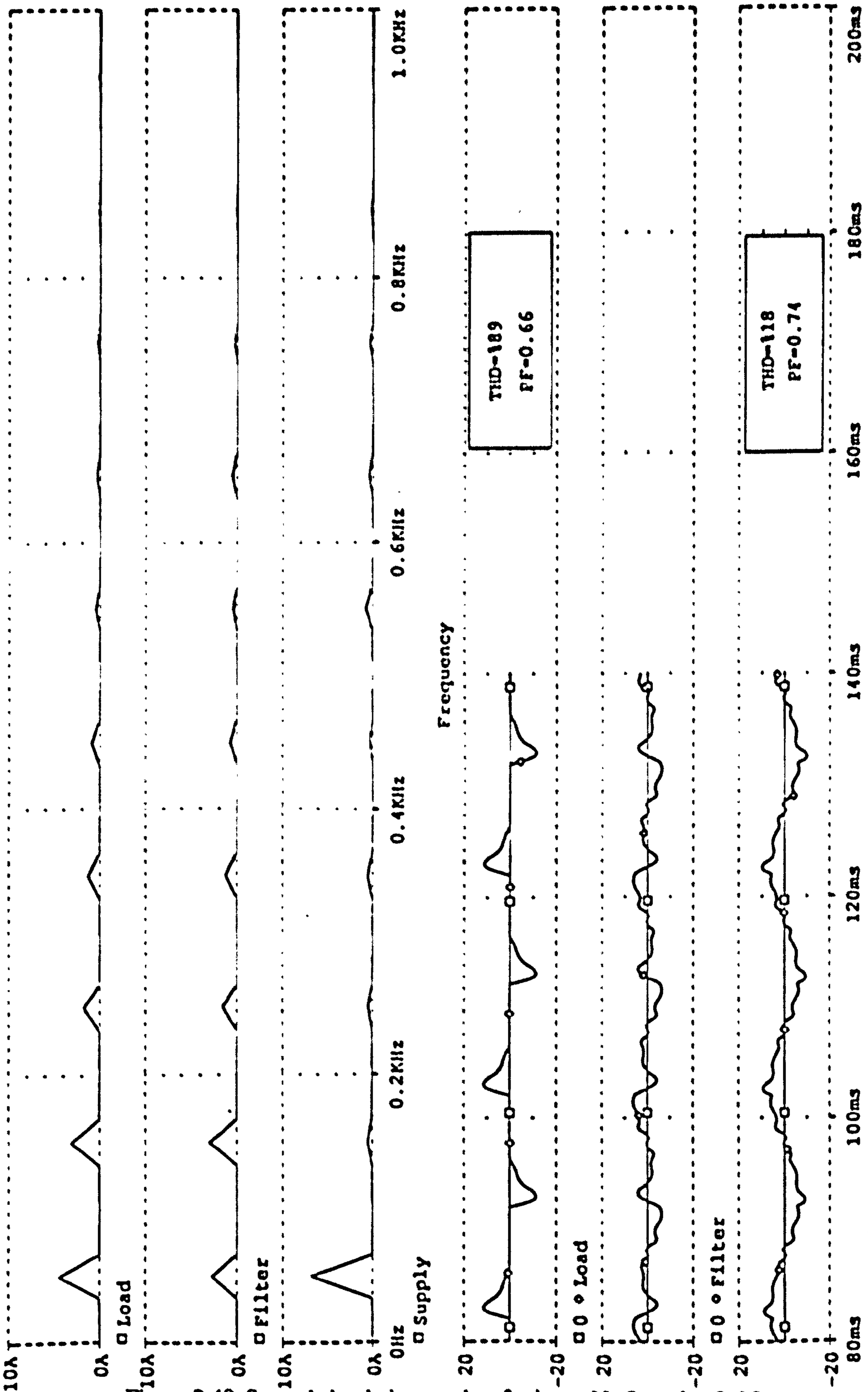


Figure 2.40 Second simulation results of scheme No.3 section 2.5.2

The disadvantage of this approach is that presence of the current transients associated with the low-pass filter (for example when the circuit is switched on). It is possible to overcome this problem by inserting damping resistors which of course introduce losses [Hayashi 88].

2.5.3 Constant current source as a storage element

In this arrangement, as shown in Figure 2.41, the constant current source is achieved using a large inductance in a rectifier circuit [Fukuda 95, Choe 89,Chicharo 93].

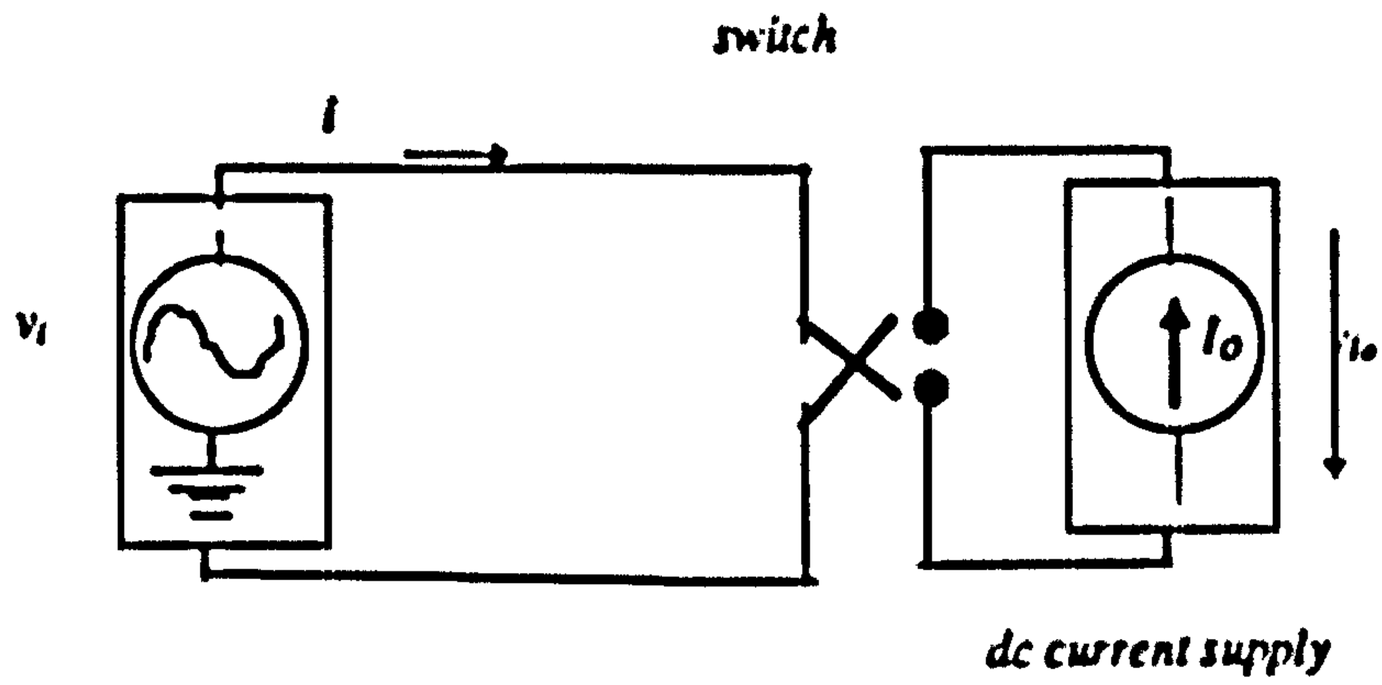


Figure 2.41 Functional diagram

The equations for the circuit are as follows.

If the switch is in the position shown in the functional diagam

$$v_{io} = v_i \,,\; i = I_o$$

If the switch is in the alternative position.

$$v_{io} = -v_i \,,\; i = -I_o$$

For most practical situations it is not necessary for filters to generate even harmonic currents and therefore the filter current must have odd symmetry which can be achieved by reversing the order of switching every half cycle.

Clearly the filter current has a square waveform with magnitude I_o and this approach is an example of the discontinous linear approximation technique (c-ii). Similar to the topology shown in Figure 2.37, this technique can not provide the piecewise approximation which is acceptable. However, by appropriate selection of switching instants, the low frequency (0.5 to 1khz) components of this waveform can match the required current. To cancel the higher order harmonics it is necessary to use a passive high pass filter. A practical implementation of this approach is shown in Figure 2.42.

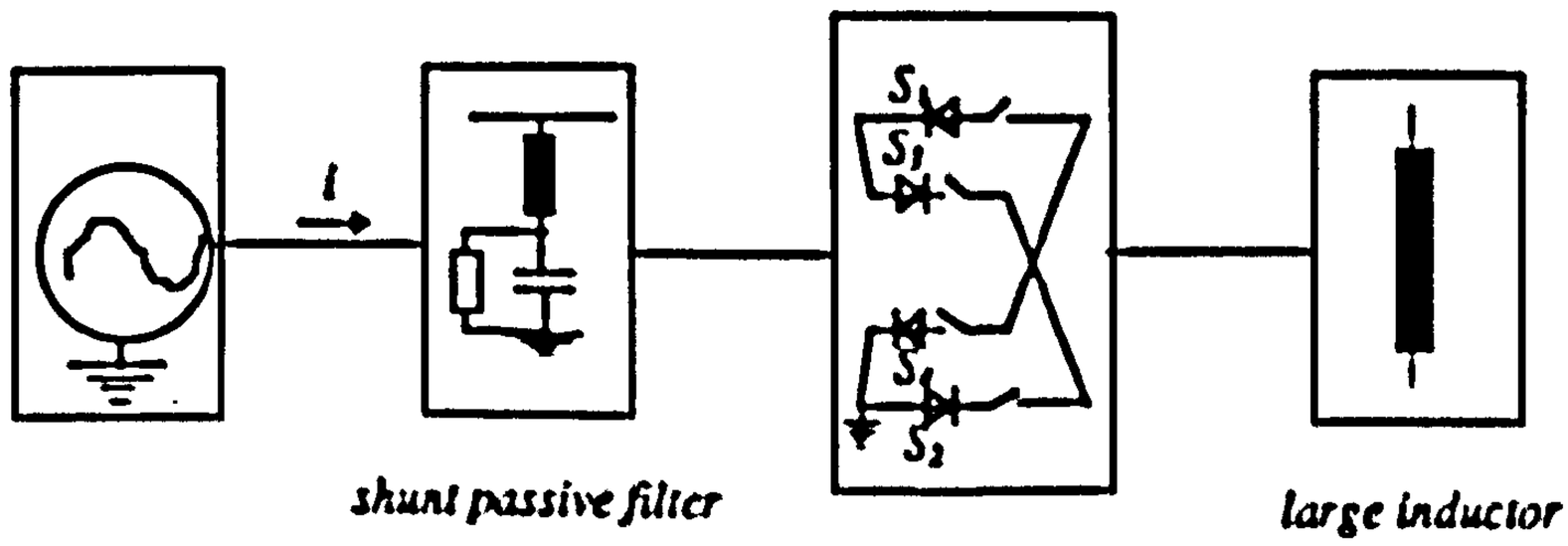


Figure 2.42 Practical circuit

2.6 Conclusion

It is shown that the operation of active filters is based on the manner in which the filter current tracks the harmonic currents due to non-linear loads. In particular, it is shown that tracking techniques are based on the control of two factors: di/dt and d^2i/dt^2 in the

filter current. In the linear tracking techniques di/ dt is controlled and in the non-linear ones both di/ dt and d2i/ dt2 are the controlling factors.

In the structures based on the linear tracking techniques, high switching frequency is employed to track the rapid variation in the harmonic load-current. But in the structures based on non-linear tracking techniques, it is the second derivative of the filter current which is controlled and the switching frequencies are lower. Therefore the switching losses in the linear techniques are higher than those in the non-linear circuits. However the disadvantage of the non-linear technique is that the filter current is affected by the resonance associated with the filter circuit elements This drawback can be overcome by applying constraints on the size of the circuit elements and switching frequencies such that

$$f_{resonance\ current} < f_{switching\ frequency}$$

$$\frac{1}{2\pi\sqrt{LC}} < f_{switching\ frequency}$$

$$LC > \frac{1}{4\pi^2 f^2_{switching\ frequency}}$$

These techniques can be subdivided into continuous and discontinuous filter-current modes. In the discontinuous current mode the filter current contains higher order current harmonics which are not required. In contrast, in the continuous-current mode there are much less higher order current harmonics.

Based on this approach, existing active filter circuits have been classified and seven new circuits have been developed, analysed and simulated. Three of these new structures have been designed, built and tested in Chapter 3

CHAPTER THREE

Operation and Performance of Proposed Active Filters

On the basis of the unified approach outlined, seven new circuits were proposed and theoretically investigated in Chapter 2. To assess the accuracy of the simulated results three circuits were built and the results of experimental investigation are given in this chapter.

The optimising criteria used for formulating the switching patterns and the circuit parameters are based on two alternative objectives: (a) minimisation of total harmonic distortion (THD) and (b) minimisation of total apparent power demand. The minimisation of total apparent power demand takes into account the power factor improvement as well as losses in the filter.

3.1 Performance Criteria for Active Filters

The performance of an active filter is evaluated by measurement of three parameters, in before and after filtering : Total Harmonic Distortion, Power Factor and Efficiency. It is assumed that the supply does not contain any voltage harmonic distortion.

The three parameters and associated symbols are defined as follows.

- Total Distortion Component of supply current, $I_{dt} = \sqrt{I_t^2 - I_{t1}^2} = \sum_{h=2}^{\infty} I_h^2$
- Total Harmonic Distortion in the supply current, $\%THD = 100 \times \frac{I_{dt}}{I_1}$
- Distortion Factor $\mu = \frac{I_{t1}}{I_t}$
- Displacement Factor , $\cos\theta_1$ (θ_1 is the angle by which i_{t1} lags v_t)
- Power Factor $PF = \mu \cos\theta_1$.
- Average Power $P_{av} = V_t\ I_{t1}\ \cos\theta_1$
- Apparent Power $S = V_t\ I_t$
- Efficiency $\eta = \frac{P_{av,load}}{P_{av,load} + P_{av,res}}$

3.2 Operation and Performance of Active Filter Scheme No. 4 (Section 2.5.1)

The active filters shown in Figures 3.1and 3.2 are used to control harmonic currents in a rectifier circuit feeding capacitive and inductive loads respectively. The filter consists of three switches, one capacitor, one inductor and a by-pass resistor. Switches S1 and S2 operate in anti-phase such that they carry the input current alternately.

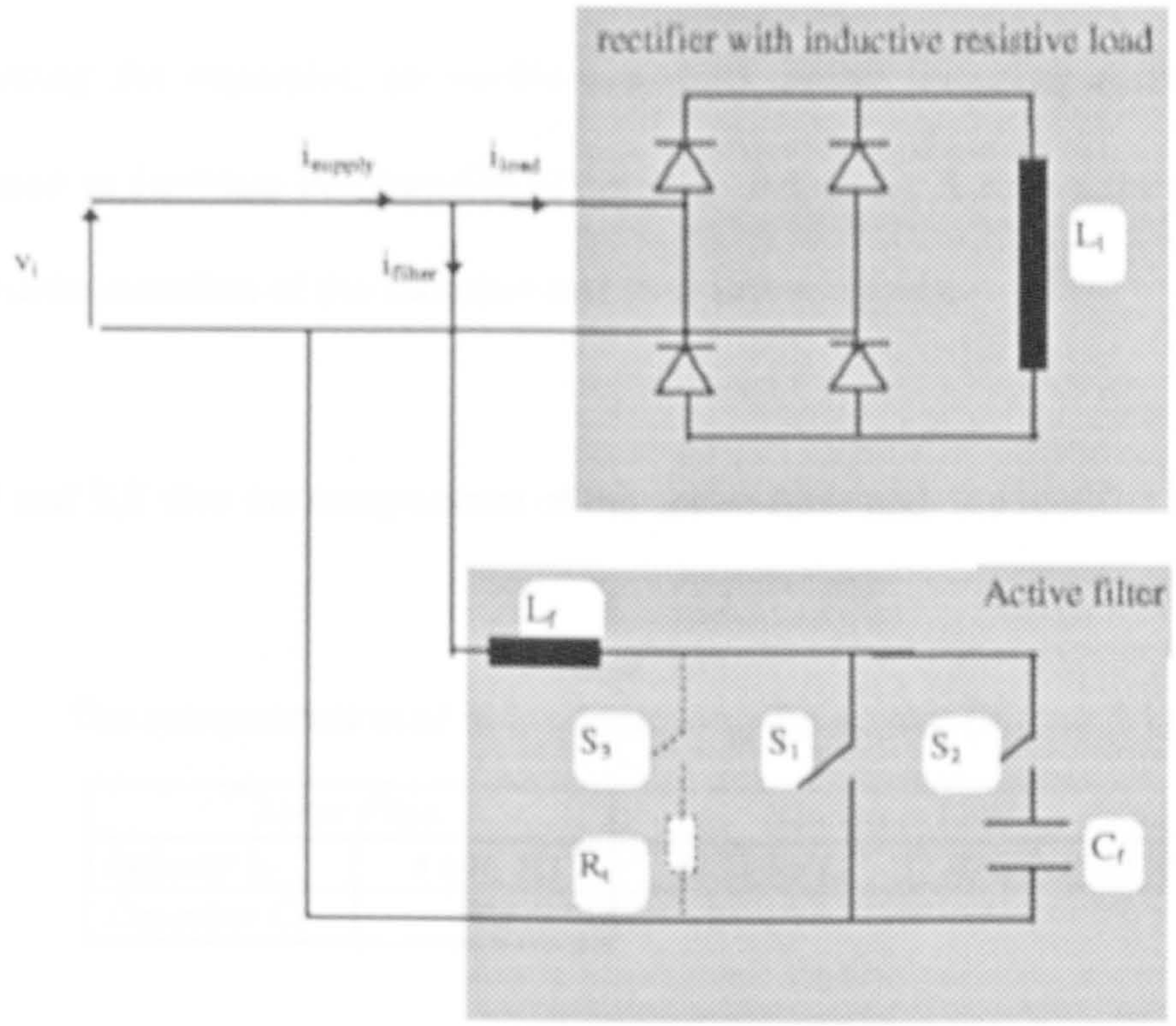


Figure 3.1 System configuration with a rectifier-inductive resistive load

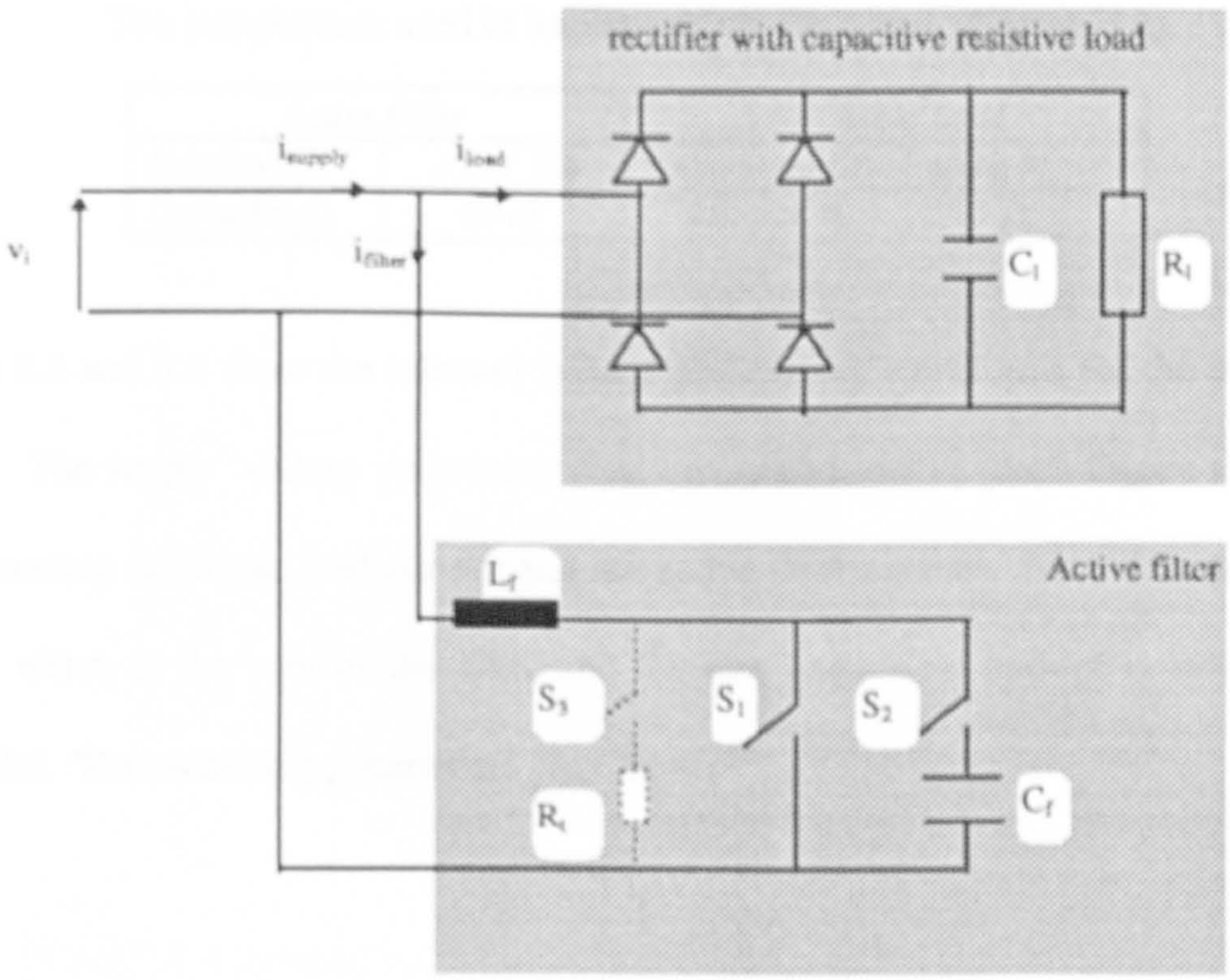


Figure 3.2 system configuration with a rectifier -capacitive resistive load

Since the transfer of current from one path to the other requires finite time, to avoid short-circuiting the capacitor, an auxiliary by-pass circuit including a resistor (10-20 ohms) is used to facilitate this transfer of current. Appendix A shows the details of the practical implementation of the switches and their driver circuits.

Tables 3.1 and 3.2 give the components of the active filter and the rectifier loads.

Table 3.1
The components used in implementing the system (Figure 3.1)

Active Filter		*Non linear Load*	
Inductor L_f	*4 mH, 1Ω*	*Inductor L_1*	*80 mH,1.9Ω*
Capacitor C_1	*80u*		

Table 3.2
The components used in implementing the system (Figure 3.2)

Active Filter		*Non linear Load*	
Inductor L_f	*4 mH, 1Ω*	*Capacitor C_1*	*600 μF*
Capacitor C_1	*80 uF*	*Resistor R_1*	*26.5 Ω*

Figures 3.3 and 3.4 show the relevant voltage and current waveforms for the two types of load. The supply voltage peak value (line - neutral) is 60 V. Each Figure shows the corresponding nonlinear load current and the active filter current. Note that the supply current which is the sum of the filter and the non-linear load current is substantially sinusoidal. The switching patterns are also shown.

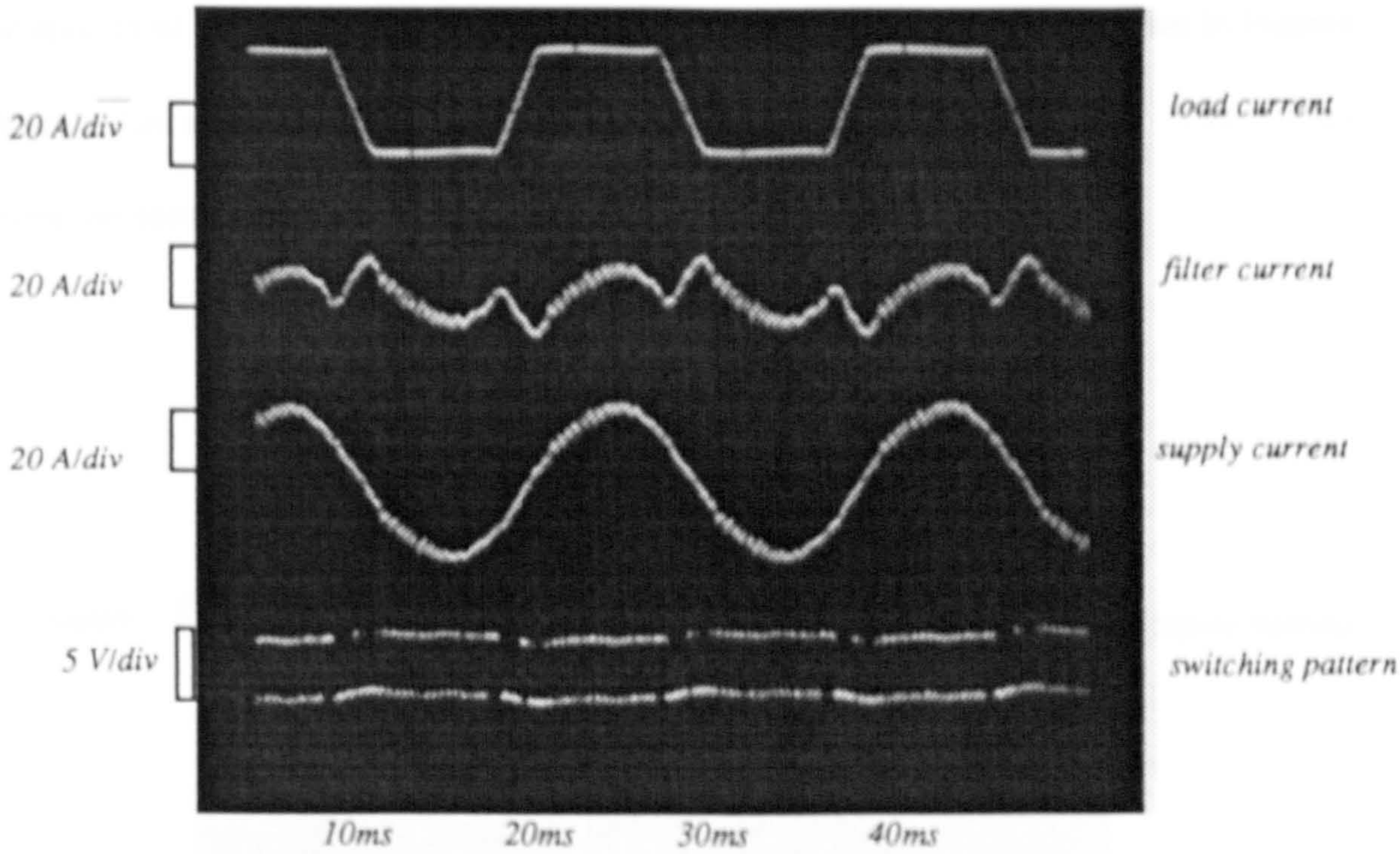


Figure 3.3 The performance of the system with a rectifier-inductive resistive load

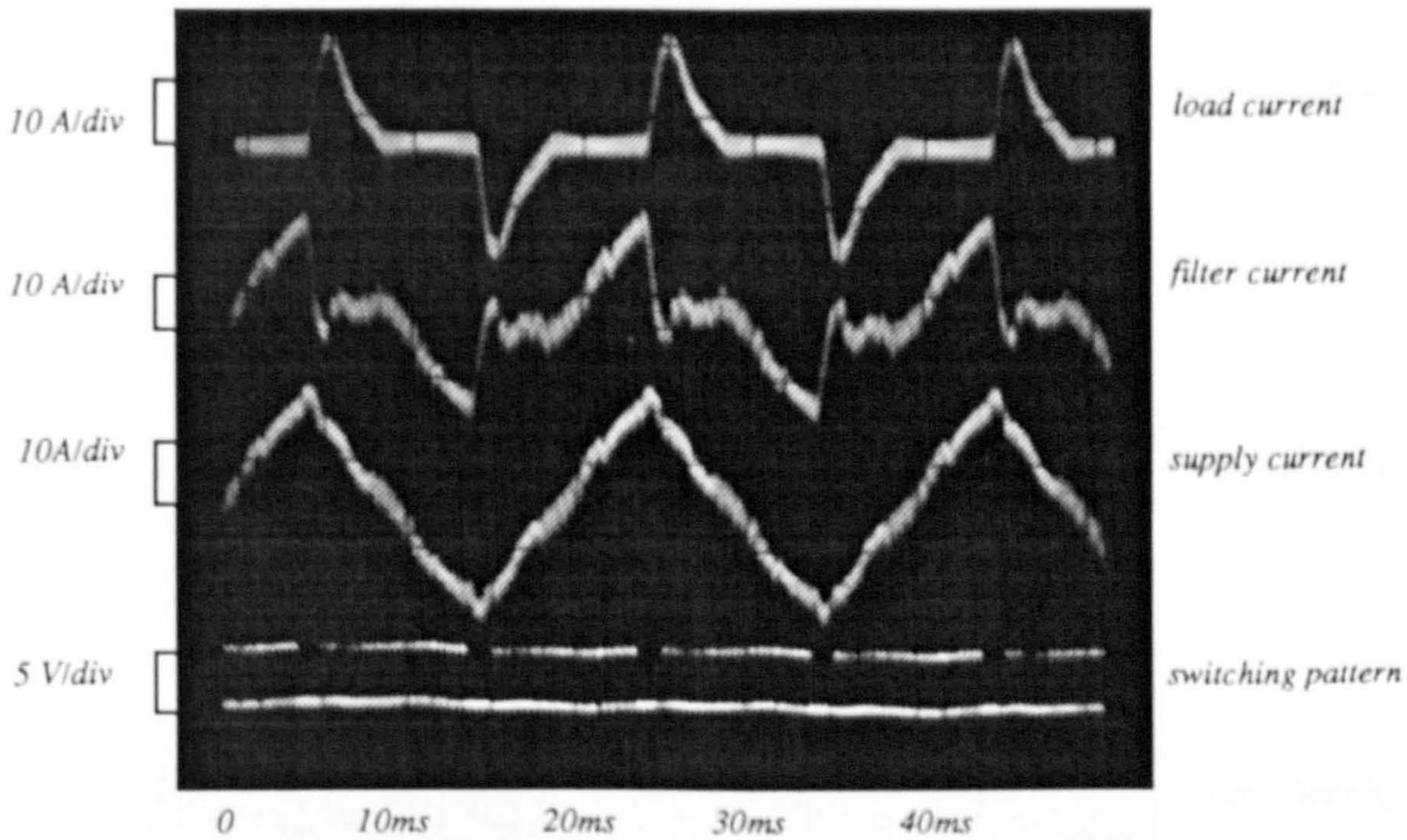


Figure 3.4 The performance of the system a rectifier-capacitive resistive load

The spectra of the supply current with and without the active filters are shown in Figures 3.5 and 3.6 showing significant reductions in the current harmonics. The circuit simulation results are shown in Figure 3.7

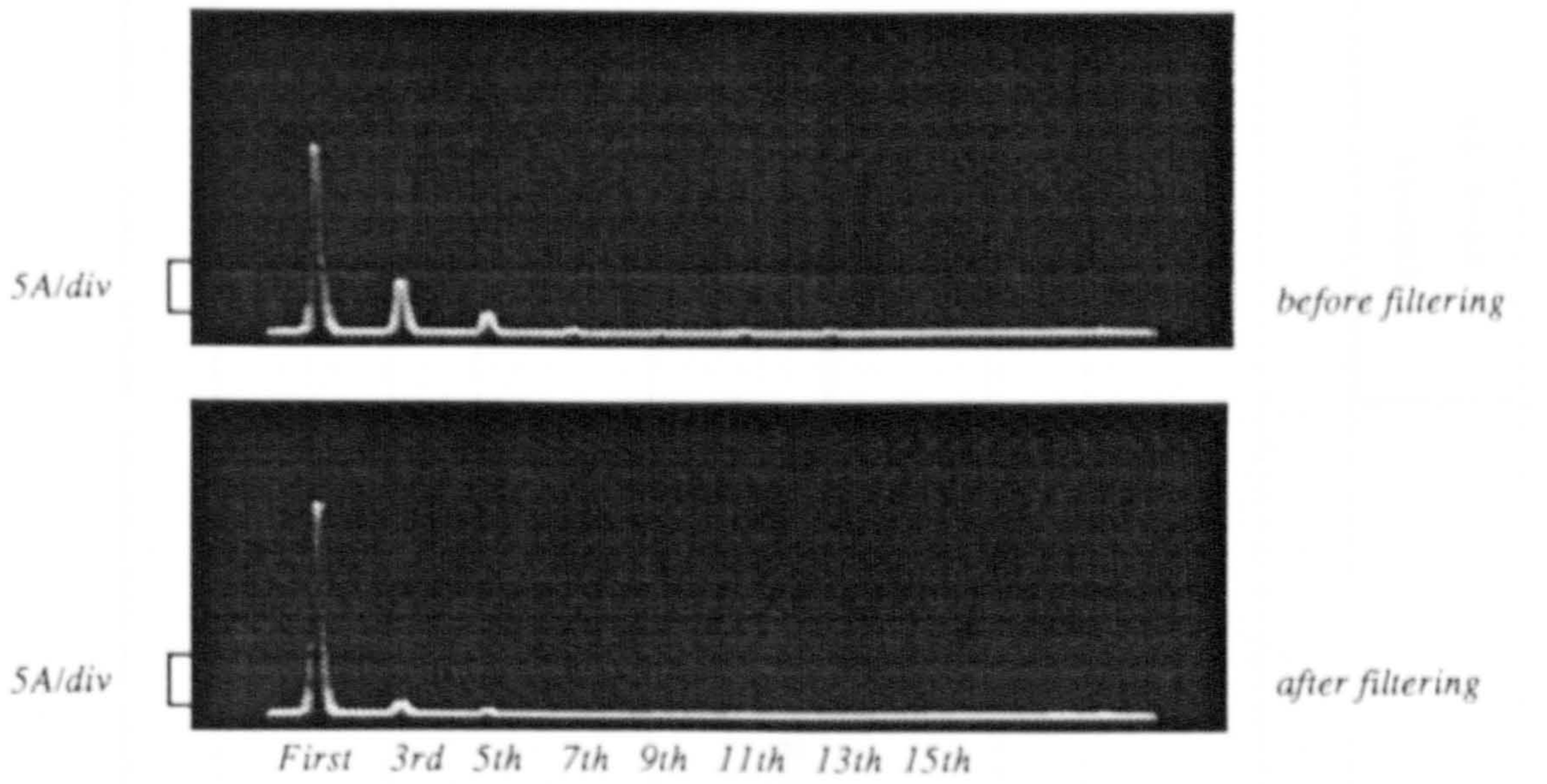


Figure 3.5 The frequency spectra of the system with a rectifier-inductive resistive load

Figure 3.6 The frequency spectra of the system with a rectifier-capacitive resistive load

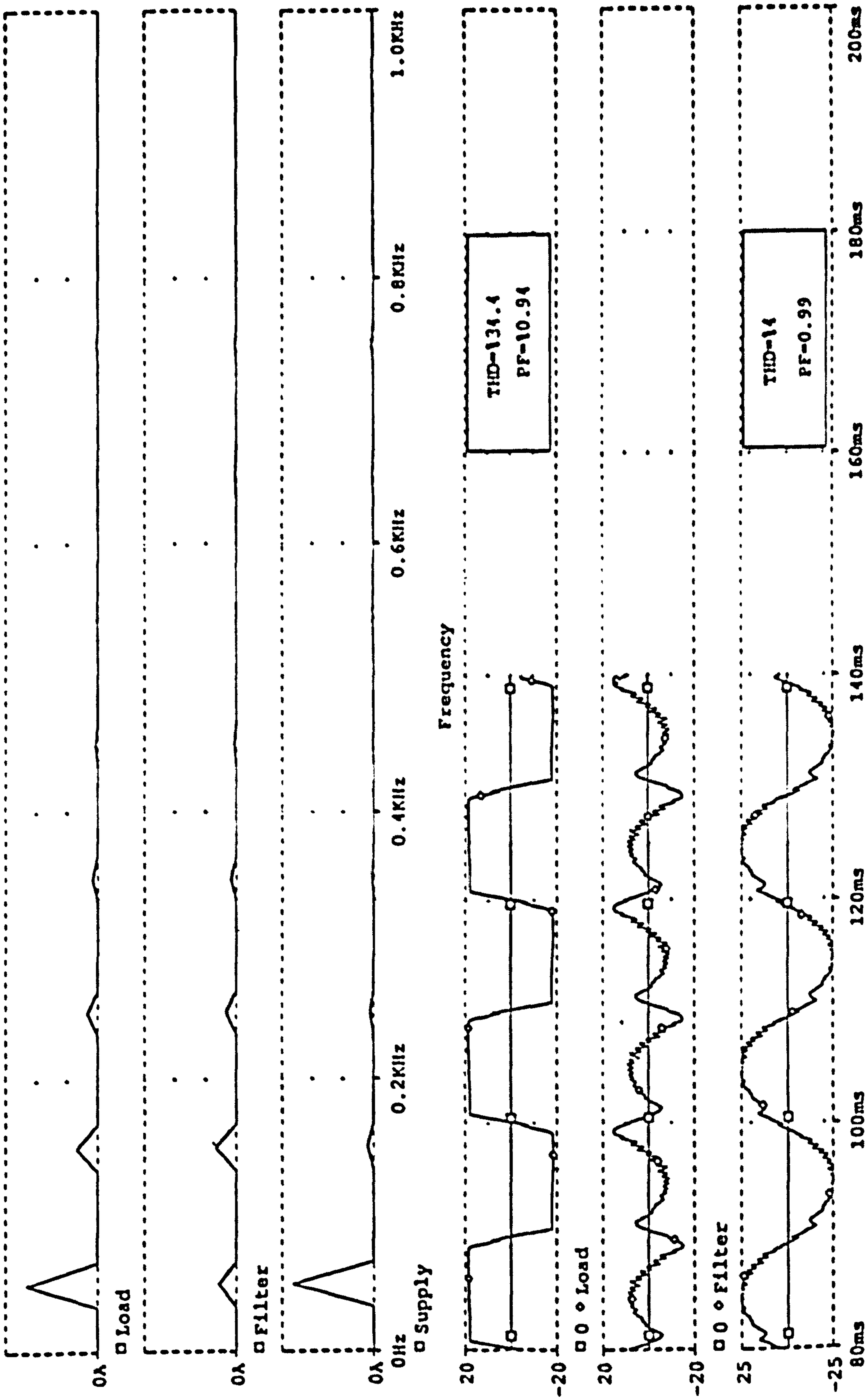


Figure 3.7 Simulation results of system configuration (Figure 3.1)

Tables 3.3 and 3.4 provide a summary of the performance of the system, including the total harmonic distortion (THD), the power factor (PF) of the resulting supply current and the efficiency of the filter.

Table 3.3
Harmonic performance of system with a rectifier-inductive resistive load

	Before Filtering		*After Filtering*	
The rms value of supply current				
I_t	*17.19*		*18.49*	
Fourier Components of the supply current				
Harmonics No	*Amplitude*	*Phase (radian)*	*Amplitude*	*Phase (radian)*
I_1	*16.17.(100)*	*-0.0896*	*18.31.(100)*	*0.095*
I_3. (I_3/I_1)	*482.(29.8)*	*-0.208*	*0.00.(0.0)*	*1.297*
I_5. (I_5/I_1)	*2.43.(15.0)*	*-0.383*	*0.06.(0.3)*	*-0.618*
I_7.(I_7/I_1)	*1.19.(7.3)*	*-0.601*	*0.04.(0.2)*	*-0.775*
I_9. (I_9/I_1)	*0.51.(3.1)*	*-0.960*	*0.12.(0.7)*	*4.074*
I_{11}.(I_{11}/I_1)	*0.21.(1.3)*	*4.368*	*0.23.(1.3)*	*4.564*
I_{13}.(I_{13}/I_1)	*0.23.(1.4)*	*3.365*	*0.15.(0.8)*	*-1.446*
I_{15}.(I_{15}/I_1)	*0.30.(1.9)*	*2.8588*	*0.16.(0.9)*	*3.756*
I_{17}.(I_{17}/I_1)	*0.28.(1.7)*	*2.599*	*0.17.(0.9)*	*2.480*
I_{19}.(I_{19}/I_1)	*0.23.(1.4)*	*2.470*	*0.36.(2.0)*	*2.305*
I_{21}.(I_{21}/I_1)	*0.15.(0.9)*	*2.396*	*0.00.(0.0)*	*2.605*
I_{23}.(I_{23}/I_1)	*0.08.(0.5)*	*2.428*	*0.09.(0.5)*	*1.769*
I_{25}.(I_{25}/I_1)	*0.03.(0.2)*	*3.141*	*0.03.(0.2)*	*2.279*
I_{27}.(I_{27}/I_1)	*0.05.(0.3)*	*3.821*	*0.11.(0.6)*	*-0.921*
I_{29}.(I_{29}/I_1)	*0.06.(0.4)*	*3.908*	*0.02.(0.2)*	*3.591*
I_{31}.(I_{31}/I_1)	*0.08.(0.5)*	*3.773*	*0.02.(0.2)*	*-1.081*
I_{33}.(I_{33}/I_1)	*0.08.(0.5)*	*3.463*	*0.09.(0.5)*	*2.734*
I_{35}.(I_{35}/I_1)	*0.07.(0.4)*	*3.226*	*0.24.(1.3)*	*3.353*
I_{37}.(I_{37}/I_1)	*0.06.(0.4)*	*2.946*	*0.06.(0.4)*	*-1.476*
I_{dc}	*5.55*		*0.63*	
THD	*34.4 %*		*3.52 %*	
The harmonic and phase displacement and power factors of supply current				
μ	*0.94*		*0.99*	
$COS\,\theta_t$	*0.99*		*0.99*	
PF	*0.93*		*0.98*	
The real power of load and dissipation power of active filter and efficiency				
P_{dc} (W)	*679.10*		*769.3*	
η	*0.88*			

Table 3.4
Harmonic performance of system with a rectifier-capacitive resistive load

	Before Filtering		After Filtering	
The rms value of supply current				
I_1 (rms)	6.30		8.28	
Fourier Components of the supply current				
Harmonics No	Amplitude	Phase (radian)	Amplitude	Phase (radian)
I_1	4.66 (100)	0.364	8.20 (100)	0.746
I_3, (I_3/I_1)	3.28 (70.6)	4.342	0.00 (0.0)	-0.244
I_5, (I_5/I_1)	1.84 (39.4	2.367	0.00 (0.0)	0.078
I_7, (I_7/I_1)	1.35 (28.9	0.625	0.10 (1.2)	0.251
I_9, (I_9/I_1)	0.93 (19.9)	-1.331	0.11 (1.3)	-0.732
I_{11}, (I_{11}/I_1)	0.43 (9.2)	3.205	0.21 (2.5)	3.317
I_{13}, (I_{13}/I_1)	0.31 (6.6)	1.864	0.29 (3.6)	2.287
I_{15}, (I_{15}/I_1)	0.19 (4.0)	0.237	0.27 (3.3)	0.184
I_{17}, (I_{17}/I_1)	0.12 (2.5)	-0.822	0.25 (303)	-1.087
I_{19}, (I_{19}/I_1)	0.12 (2.5)	3.659	0.14 (1.7)	3.269
I_{21}, (I_{21}/I_1)	0.08 (1.7)	1.946	0.23 (2.8)	1.324
I_{23}, (I_{23}/I_1)	0.08 (1.7)	0.608	0.23 (2.8)	2.893
I_{25}, (I_{25}/I_1)	0.06 (1.2)	-0.564	0.08 (0.9)	3.632
I_{27}, (I_{27}/I_1)	0.04 (0.8).	-1.567	0.08 (0.9)	-1.065
I_{29}, (I_{29}/I_1)	0.04 (0.8)	3.194	0.12 (1.4)	1.728
I_{31}, (I_{31}/I_1)	0.04 (0.8)	1.469	0.16 (1.9)	0.187
I_{33}, (I_{33}/I_1)	0.06 (1.2)	0.009	0.16 (1.9)	1.142
I_{35}, (I_{35}/I_1)	0.06 (1.2)	-1.067	0.13 (1.5)	3.324
I_{37}, (I_{37}/I_1)	0.03 (06)	3.895	0.13 (1.5)	-1.410
The distortion component of the supply current and the Total Harmonic Distortion				
I_{dI}	4.2		0.9	
THD	%89.6		%11.24	
The harmonic and phase displacement and power factors of supply current				
μ	0.74		0.99	
$COS\ \theta_1$	0.93		0.73	
PF	0.69		0.73	
The real power of load and dissipation power of active filter and efficiency				
P_{av} (W)	183.9		253.4	
η	0.73			

These Tables relate to the situation where the filter operation is optimised for the reduction of total harmonic distortion. The reduction achieved is different for the two

types of rectifier loads . For the rectifier circuit with the inductive load the power factor without the filter is already very high and therefore the effect of the filter is negligible and the filter efficiency is high (0.88). For the rectifier circuit with the capacitive smoothing the reduction in the total harmonic distortion achieved is 87% but the filter efficiency is low (0.73) .

To optimise the system with the aim of improving the power factor and maximising the efficiency one approach is to minimise the apparent power. With this approach, a high operating efficiency can be achieved but the reduction in the THD is obviously not as high as the previous case. These facts are summarised in Tables 3.5 and 3.6

Table 3.5
Comparison of two optimisation approaches of system with a rectifier-inductive resistive load

	THD	*PF*	*η*	I_L
Before filtering	*34.44%*	*0.93*	*1.00*	*17.19*
After filtering (for THD_{min})	*3.52%*	*0.98*	*0.88*	*18.5*
After filtering (for S_{min})	*23%*	*0.98*	*0.98*	*16.82*

Table 3.6
Comparison of two optimisation approaches of system with a rectifier-capacitive resistive load

	THD	*PF*	*η*	I_L
Before filtering	*89.69%*	*0.69*	*1.00*	*6.30*
After filtering (for THD_{min})	*11.24%*	*0.73*	*0.73*	*8.28*
After filtering (for S_{min})	*18.65%*	*0.69*	*0.88*	*7.67*

3.3 Operation and Performance of Active Filter Scheme No. 6 (Section 2.5.1)

The active filters shown in Figures 3.8 and 3.9 are used to control harmonic currents in a rectifier circuit feeding capacitive and inductive loads respectively. The filter consists of

three switches, two capacitors, two inductors and a by-pass resistor. Switches S1 and S2 operate in anti-phase such that they carry the input current alternately.

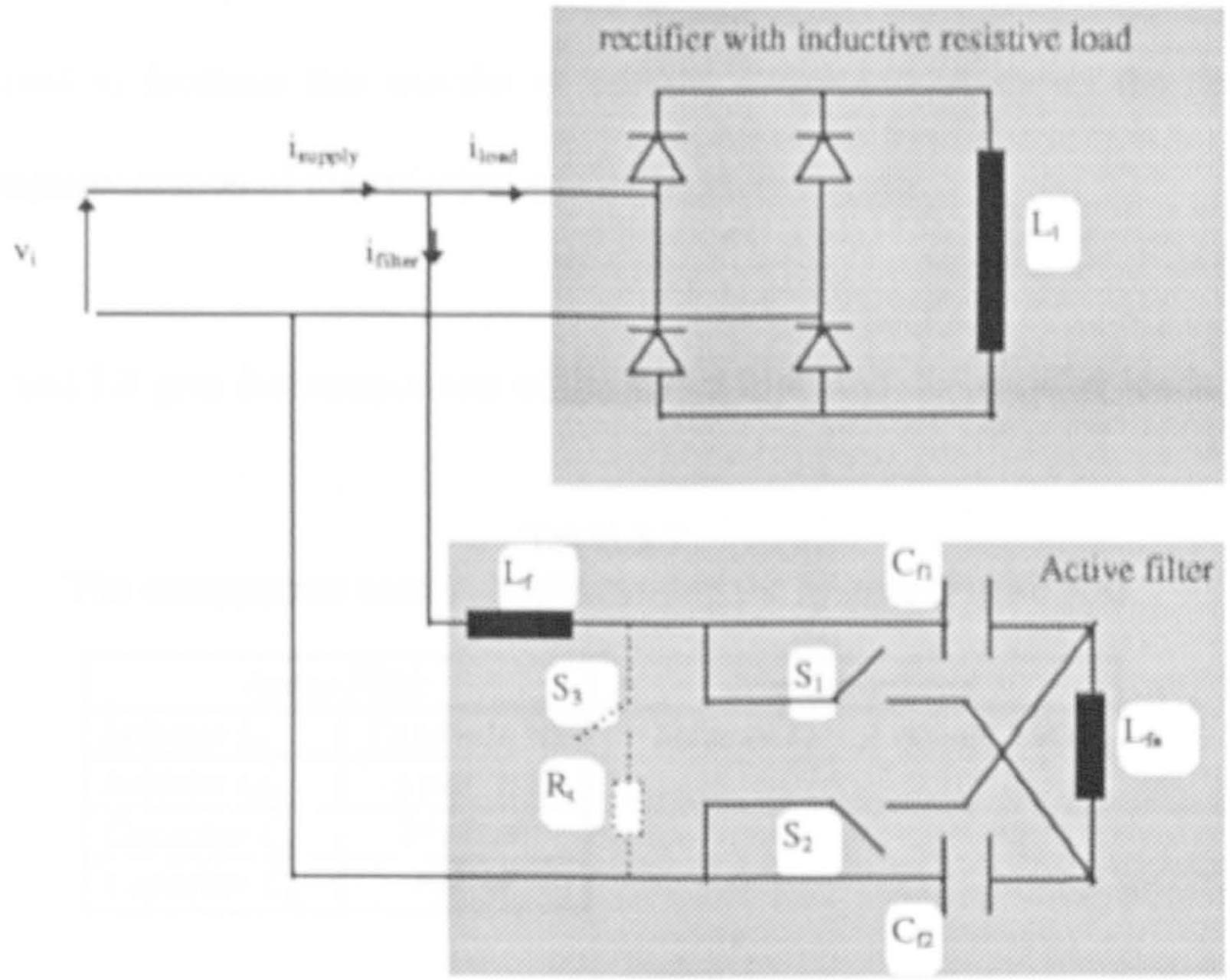


Figure 3.8 system configuration with a rectifier-inductive resistive load

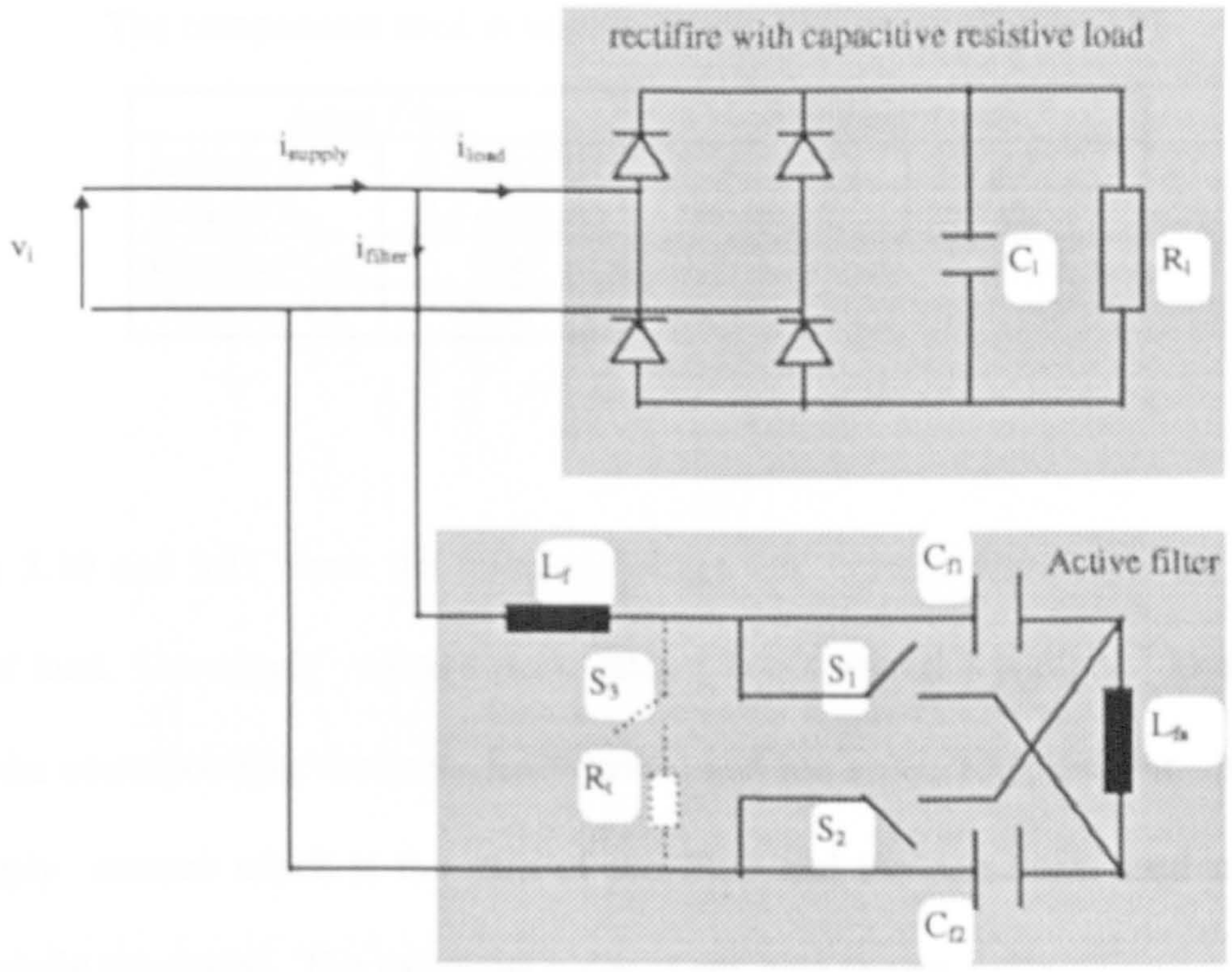


Figure 3.9 system configuration with a rectifier-capacitive resistiveload

Since the transfer of current from one path to the other requires finite time, to avoid short-circuiting the capacitor an auxiliary by-pass circuit including a resistor (10-20 ohms) is used to facilitate this transfer of current. Appendix A shows the details of practical implementation of the switches and their driver circuits.

Tables 3.7 and 3.8 give the components of the active filter and the rectifier loads.

Table 3.7
The components used in implementing the system (Figure 3.8)

Active Filter		*Non linear Load*	
Inductor L_f	*13.15 mH,3Ω*	*Inductor L_1*	*80 mH,1.9Ω*
Inductor L_{fo}	*3 mH, 1Ω*		
Capacitor C_p	*29.68 uF*		
Capacitor C_n	*100 uF*		

TABLE 3.8
The components used in implementing the system (Figure 3.9)

Active Filter		*Non linear Load*	
Inductor L_f	*15.3mH,3.1Ω*	*Capacitor C_1*	*600 μ F*
Inductor L_{fo}	*12.6 mH,2.4Ω*	*Resistor R_1*	*26.5 Ω*
Capacitor C_p	*16 uF*		
Capacitor C_n	*80 uF*		

Figures 3.10 and 3.11 show the relevant voltage and current waveforms for the two types of load. The supply voltage peak value (line - neutral) is 60 V. Each Figure shows the corresponding nonlinear load current and the active filter current. Note that the supply current which is the sum of the filter and the non-linear load current is substantially sinusoidal. The switching patterns are also shown.

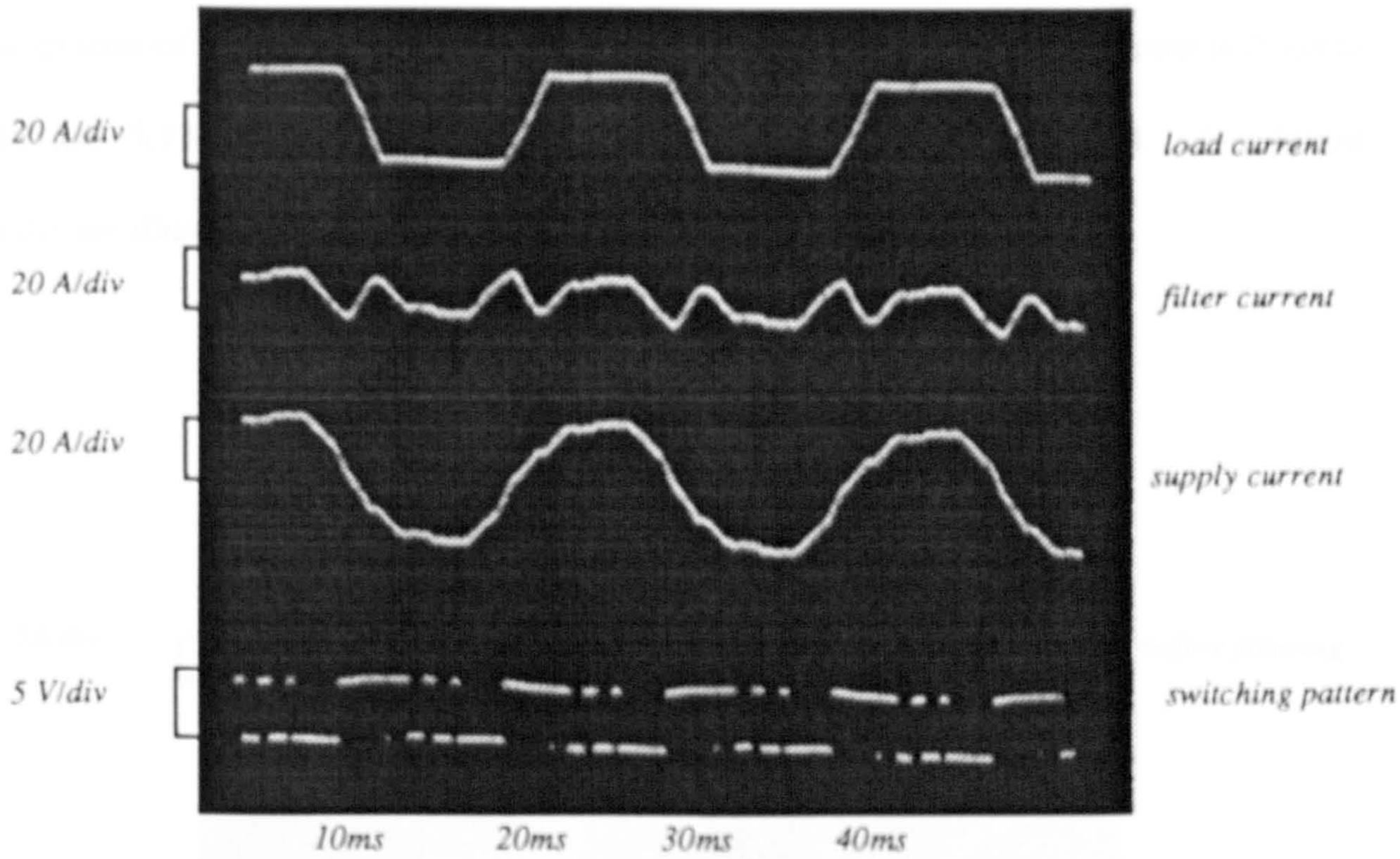


Figure 3.10 The performance of system with a rectifier-inductive resistive load

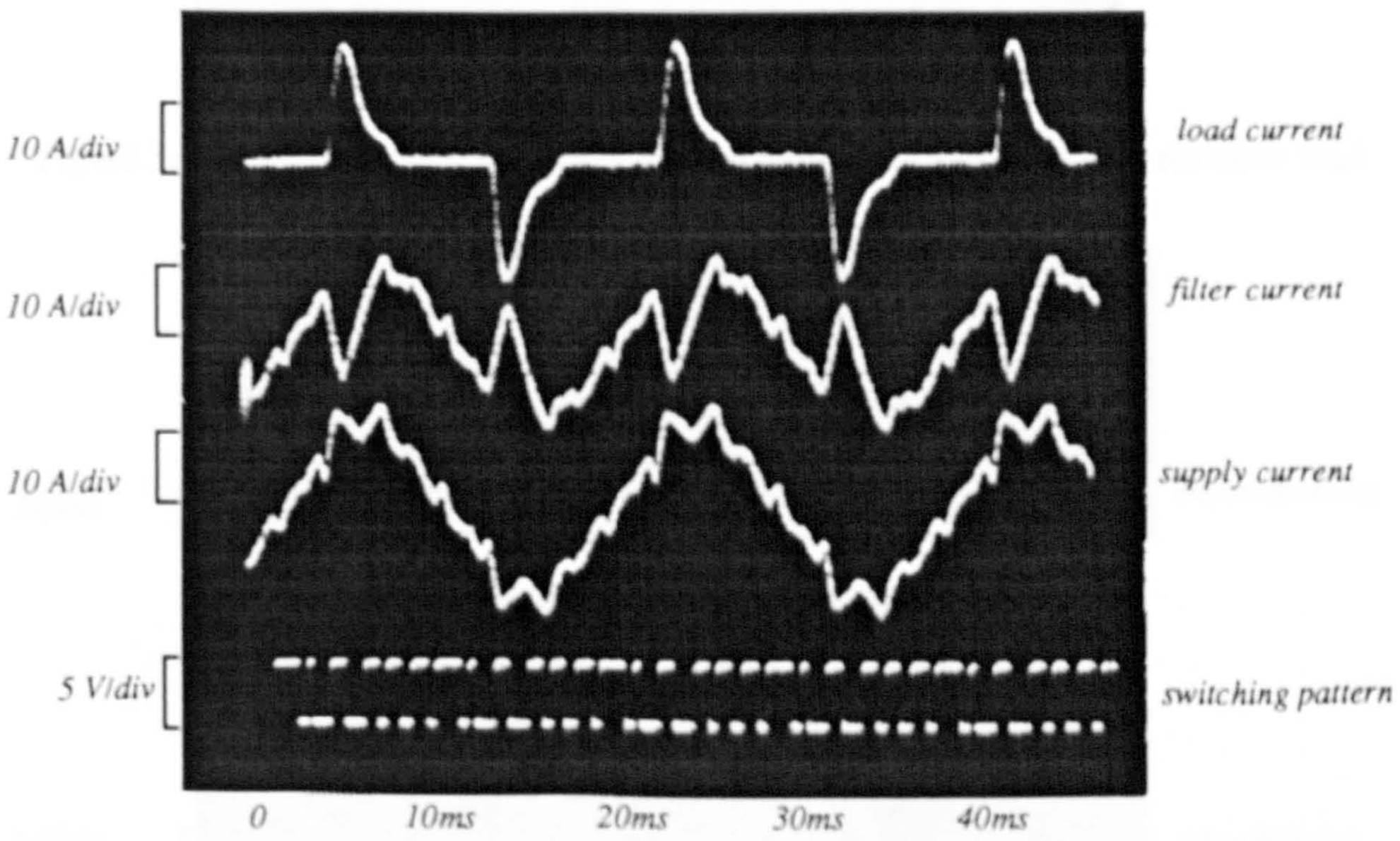


Figure 3.11 The performance of the system with a rectifier-capacitive resistive load

The spectra of the supply current with and without the active filters are shown in Figures 3.12 and 3.13 showing significant reductions in the current harmonics. Simulation results are illustrated in Figure 3.14.

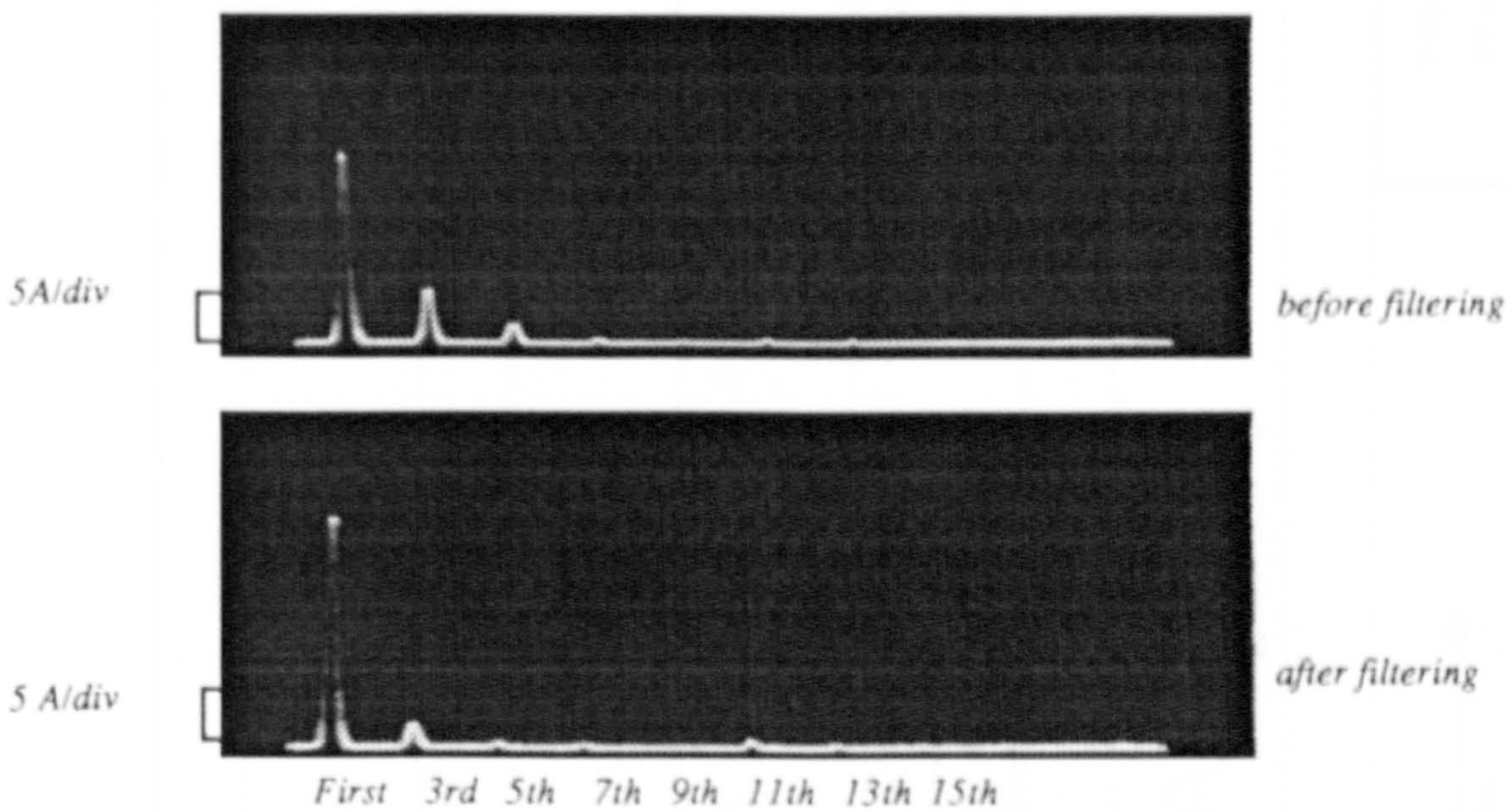


Figure 3.12 The frequency spectra of system with a rectifier-inductive resistive load

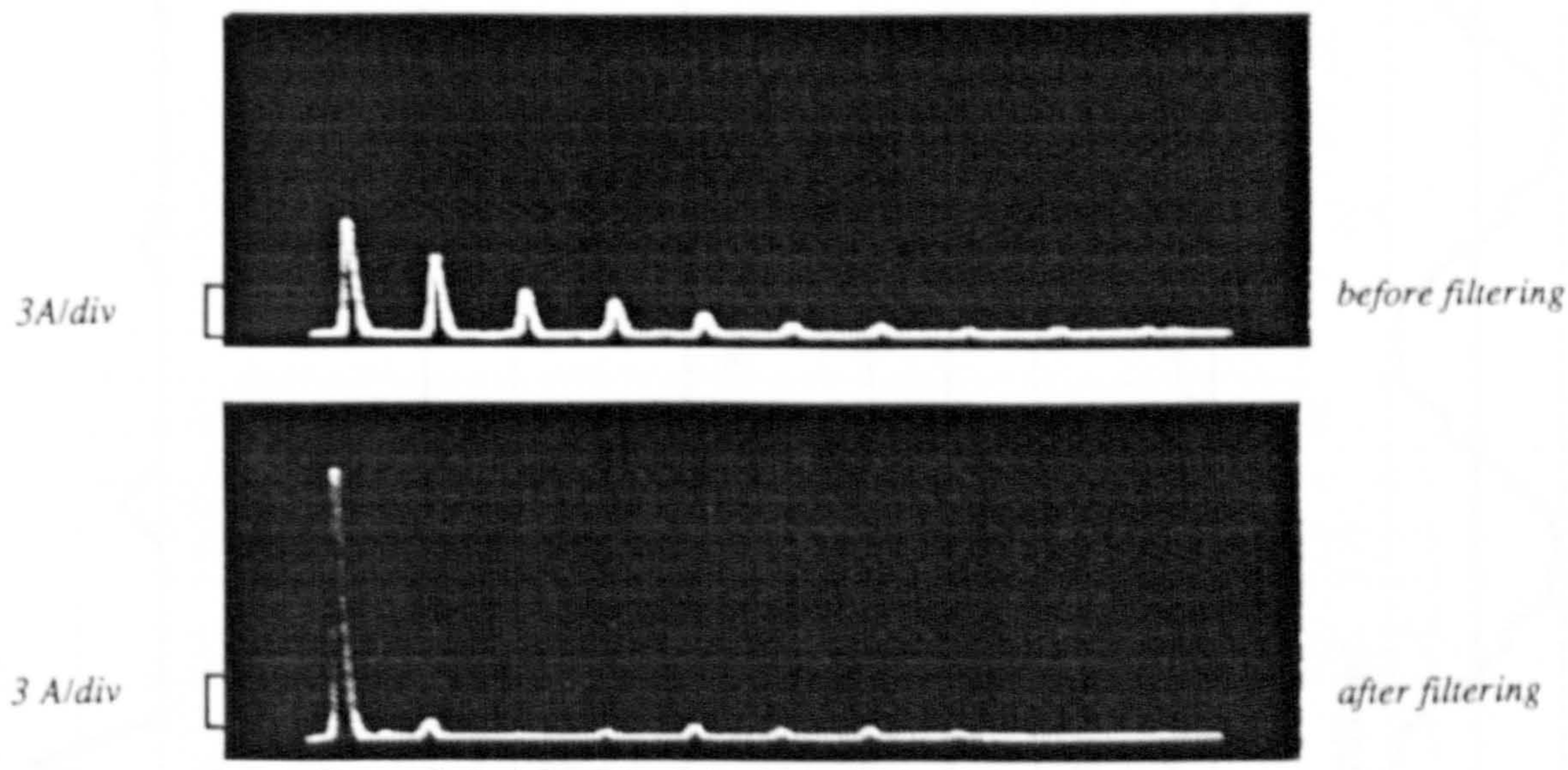


Figure 3.13 The frequency spectra of system with a rectifier-capacitive resistive load

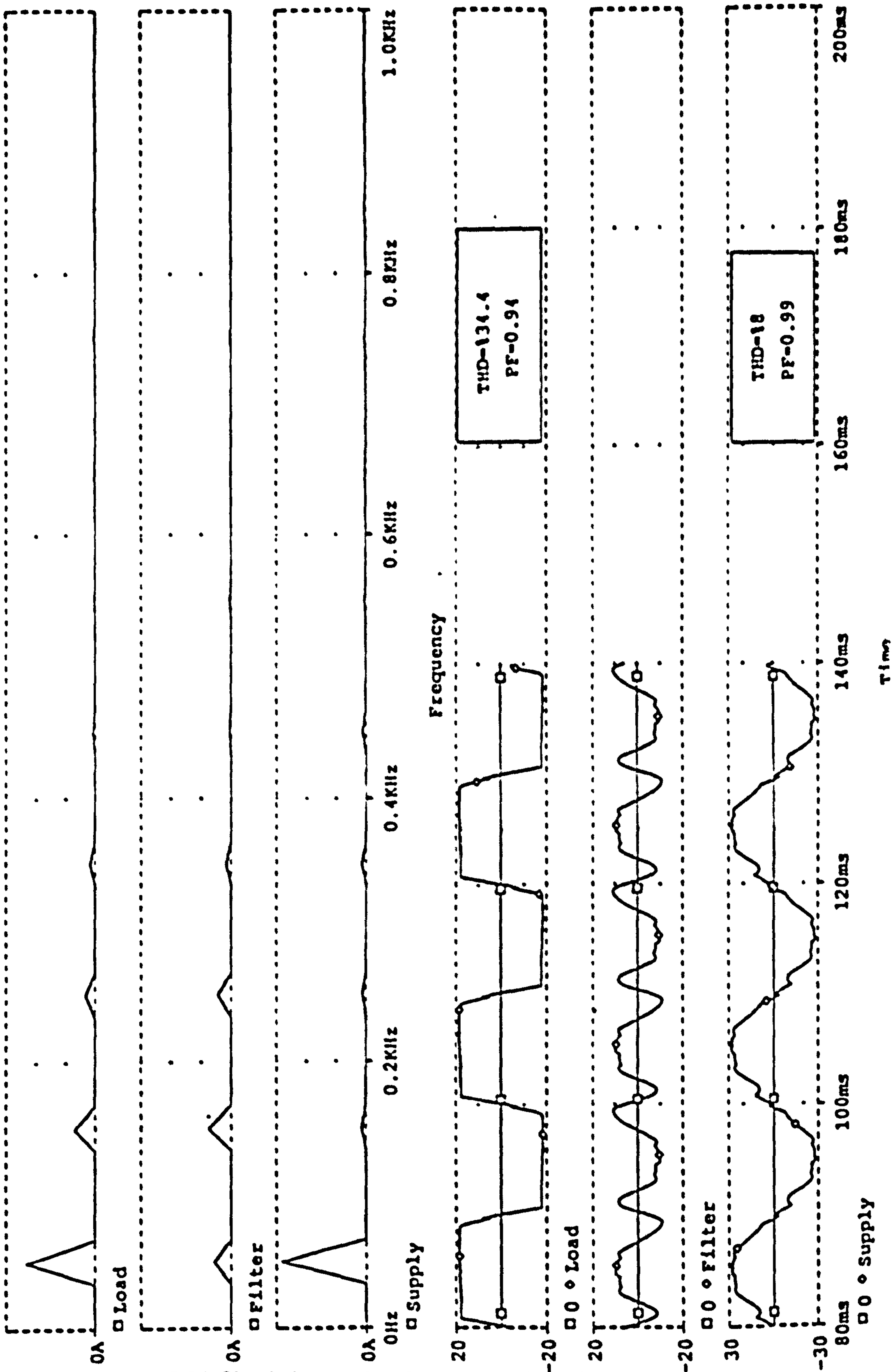


Figure 3.14 Simulation results of system configuration (Figure 3.8)

Tables 3.9 and 3.10 provide a summary of the performance of the system including the total harmonic distortion (THD), the power factor (PF) of the resulting supply current and the efficiency of the filter.

Table 3.9
Harmonic performance of system with a rectifier-Inductive resistive load

	Before Filtering		After Filtering	
The rms value of supply current				
I_1	17.19		19.26	
Fowier Components of the supply current				
Harmonics No	Amplitude	Phase (radian)	Amplitude	Phase (radian)
I_1	16.17, (100)	-0.0896	19.07, (100)	-0.037
I_3, (I_3/I_1)	4.82, (29.8)	-0.208	1.23, (6.47)	0.011
I_5, (I_5/I_1)	2.43, (15.0)	-0.383	0.50, (2.65)	-1.124
I_7, (I_7/I_1)	1.19, (7.3)	-0.601	0.51, (2.72)	-0.283
I_9, (I_9/I_1)	0.51, (3.1)	-0.960	0.47, (2.51)	-0.394
I_{11}, (I_{11}/I_1)	0.21, (1.3)	4.368	0.35, (1.86)	3.652
I_{13}, (I_{13}/I_1)	0.23, (1.4)	3.365	0.26, (1.40)	3.365
I_{15}, (I_{15}/I_1)	0.30, (1.9)	2.8588	0.29, (1.57)	2.775
I_{17}, (I_{17}/I_1)	0.28, (1.7)	2.599	0.34, (1.82)	2.778
I_{19}, (I_{19}/I_1)	0.23, (1.4)	2.470	0.23, (1.22)	2.669
I_{21}, (I_{21}/I_1)	0.15, (0.9)	2.396	0.14, (0.77)	1.810
I_{23}, (I_{23}/I_1)	0.08, (0.5)	2.428	0.15, (0.83)	3.192
I_{25}, (I_{25}/I_1)	0.03, (0.2)	3.141	0.02, (0.11)	0.625
I_{27}, (I_{27}/I_1)	0.05, (0.3)	3.821	0.06, (0.34)	3.883
I_{29}, (I_{29}/I_1)	0.06, (0.4)	3.908	0.07, (0.38)	3.919
I_{31}, (I_{31}/I_1)	0.08, (0.5)	3.773	0.07, (0.45)	4.182
I_{33}, (I_{33}/I_1)	0.08, (0.5)	3.463	0.08, (0.42)	3.140
I_{35}, (I_{35}/I_1)	0.07, (0.4)	3.226	0.08, (0.47)	3.364
I_{37}, (I_{37}/I_1)	0.06, (0.4)	2.946	0.04, (0.24)	2.477
The distortion component of the supply current and the Total Harmonic Distortion				
I_{d1}	5.55		1.69	
THD	34.4 %		8.89%	
The harmonic and phase displacement and power factors of supply current				
μ	0.94		0.99	
$COS\ 0_1$	0.99		0.99	
PF	0.93		0.98	
The real power of load and dissipation power of active filter and efficiency				
P (W)	679.10		801	
η	0.84			

Table 3.10
Harmonic performance of the system with a rectifier-capacitive resistive load

	Before Filtering		*After Filtering*	
The rms value of supply current				
I_1 *(rms)*	*6.30*		*7.84*	
Fourier Components of the supply current				
Harmonics No	*Amplitude*	*Phase(radian)*	*Amplitude*	*Phase(radian)*
I_1	*4.66(100)*	*0.364*	*7.77(100)*	*0.192*
I_3. (I_3/I_1)	*3.28(70.6)*	*4.342*	*0.10(1.3)*	*-1.398*
I_5. (I_5/I_1)	*1.84(39.4*	*2.367*	*0.04(0.6)*	*3.415*
I_7. (I_7/I_1)	*1.35(28.9*	*0.625*	*0.18(2.4)*	*1.031*
I_9. (I_9/I_1)	*0.93(19.9)*	*-1.331*	*0.31(4.1)*	*-1.414*
I_{11}. (I_{11}/I_1)	*0.43(9.2)*	*3.205*	*0.24(3.1)*	*0.566*
I_{13}. (I_{13}/I_1)	*0.31(6.6)*	*1.864*	*0.06(0.9)*	*1.858*
I_{15}. (I_{15}/I_1)	*0.19(4.0)*	*0.237*	*0.27(3.5)*	*0.178*
I_{17}. (I_{17}/I_1)	*0.12(2.5)*	*-0.822*	*0.20(2.7)*	*0.254*
I_{19}. (I_{19}/I_1)	*0.12(2.5)*	*3.689*	*0.08(1.1)*	*-0.777*
I_{21}. (I_{21}/I_1)	*0.08(1.7)*	*1.946*	*0.17(2.3)*	*2.447*
I_{23}. (I_{23}/I_1)	*0.08(1.7)*	*0.608*	*0.06(0.9)*	*0.302*
I_{25}. (I_{25}/I_1)	*0.06(1.2)*	*-0.564*	*0.05(0.7)*	*-0.956*
I_{27}. (I_{27}/I_1)	*0.04(0.8).*	*-1.567*	*0.11(1.5)*	*2.802*
I_{29}. (I_{29}/I_1)	*0.04(0.8)*	*3.194*	*0.13(1.8)*	*3.399*
I_{31}. (I_{31}/I_1)	*0.04(0.8)*	*1.469*	*0.02(0.3)*	*1.016*
I_{33}. (I_{33}/I_1)	*0.06(1.2)*	*0.009*	*0.03(0.4)*	*4.659*
I_{35}. (I_{35}/I_1)	*0.06(1.2)*	*-1.067*	*0.0(0.0)*	*0.204*
I_{37}. (I_{37}/I_1)	*0.03(06)*	*3.895*	*0.0(0.0)*	*4.518*
The distortion component of the supply current and the Total Harmonic Distortion				
I_{dist}	*4.2*		*0.65*	
THD	*89.6%*		*8.4%*	
The harmonic and phase displacement and power factors of supply current				
μ	*0.74*		*0.99*	
$COS\ \theta_1$	*0.93*		*0.98*	
PF	*0.69*		*0.97*	
The real power of load and dissipation power of active filter and efficiency				
P (W)	*183.9*		*323.06*	
η	*0.58*			

These Tables relate to the situation where the filter operation is optimised for the reduction of total harmonic distortion. The reduction achieved is different for the two types of rectifier loads . For the rectifier circuit with the inductive load the power factor

without the filter is already very high and therefore the effect of the filter is negligible and the filter efficiency is relatively high (0.84). For the rectifier circuit with the capacitve smoothing the reduction in the total harmonic distortion achieved is 90% but the filter efficiency is low (0.56).

To optimise the system with the aim of improving the power factor and maximising the efficiency one approach is to minimise the apparent power. With this approach as shown in the Tables 3.11 and 3.12, a high operating efficiency can be achieved but the reduction in the THD is not substantial. These facts are summarised in these Tables.

Table 3.11
Comparison of two optimisation appraches of system with a rectifier-inductive resistive load

	THD	*PF*	*η*	*I_L*
Before filtering	*34.4%*	*0.93*	*1.00*	*17.19*
After filtering (for THD_{min})	*8.88%*	*0.98*	*0.84*	*19.26*
After filtering (for S_{min})	*25.54%*	*0.96*	*0.98*	*16.85*

Table 3.12
Comparison of two optimisation appraches of system with a rectifier-capacitive resistive load

	THD	*PF*	*η*	*I*
Before filtering	*89.69%*	*0.69*	*1.00*	*6.30*
After filtering (for THD_{min})	*8.4%*	*0.97*	*0.58*	*7.84*
After filtering (for S_{min})	*37.19%*	*0.88*	*0.85*	*5.74*

3.4 Operation and Performance of Active Filter Scheme No. 7 (Section 2.5.1)

The active filters shown in Figures 3.15 and 3.16 are used to control harmonic currents in a rectifier circuit feeding capacitive and inductive loads respectively. The filter consists of three switches, two capacitors, two inductors and a by-pass resistor.

Switches S1 and S2 operate in anti-phase such that they carry the input current alternately.

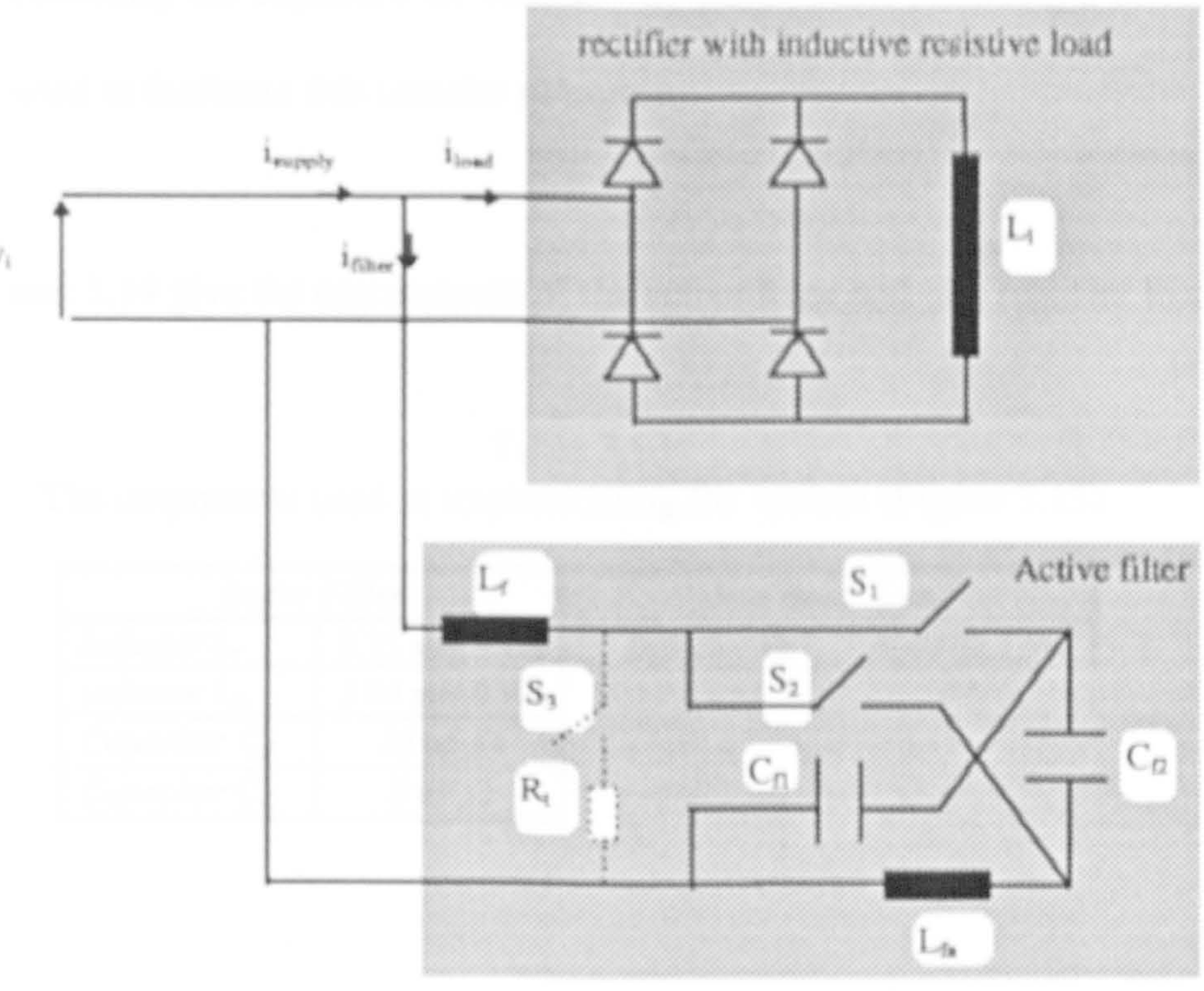


Figure 3.15 system configuration with rectifier-inductive resistive load

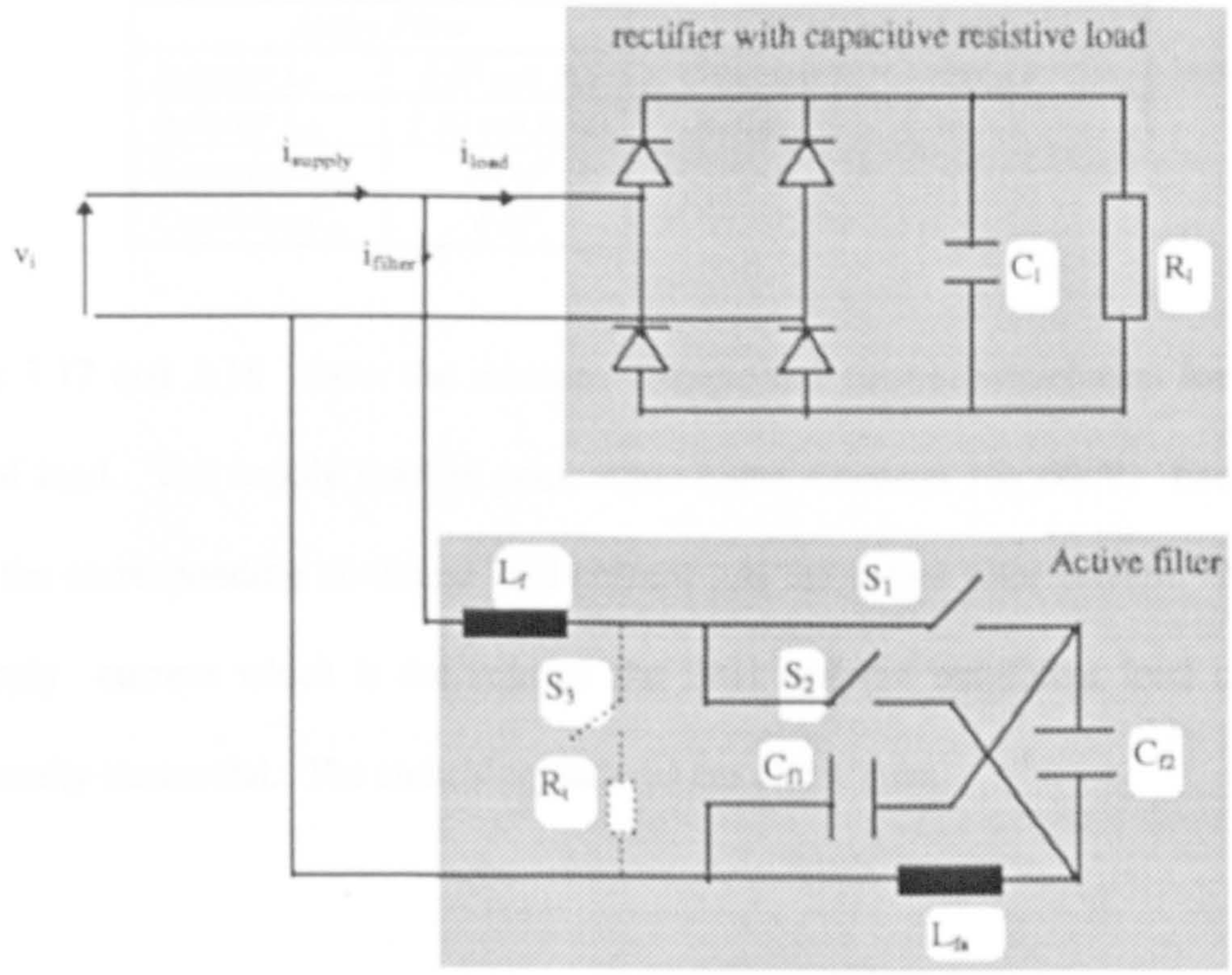


Figure 3.16 system configuration with rectifier-capacitive resistive load

Again, since the transfer of current from one path to the other requires finite time, to avoid short-circuiting the capacitor an auxiliary by-pass circuit including a resistor (10-20 ohms) is used to facilitate this transfer of current.

Tables 3.13 and 3.14 give the components of the active filter and the rectifier loads.

Table 3.13
The components used in implementing the system (Figure 3.15)

Active Filter		*Non linear Load*	
Inductor L_f	*9.75 mH,3.1Ω*	*Inductor L_l*	*80mH,1Ω,1.9Ω*
Inductor L_{fo}	*2.84 mH,0.9Ω*		
Capacitor C_{fl}	*25 uF,Ω*		
Capacitor C_{fl}	*8 uF,Ω*		

Table 3.14
The components used in implementing the system(Figure 3.16)

Active Filter		*Non linear Load*	
Inductor L_f	*8.80 mH,3Ω*	*Capacitor C_l*	*600 μ F*
Inductor L_{fo}	*3.30 mH,0.9Ω*	*Resistor R_l*	*26.5Ω*
Capacitor C_{fl}	*11 uF*		
Capacitor C_{fl}	*8 uF*		

Figures 3.17 and 3.18 show the relevant voltage and current waveforms for the two types of load. The supply voltage peak value (line - neutral) is 60 V. Each Figure shows the corresponding nonlinear load current and the active filter current. Note that the supply current which is the sum of the filter and the non-linear load current is substantially sinusoidal. The switching patterns are also shown.

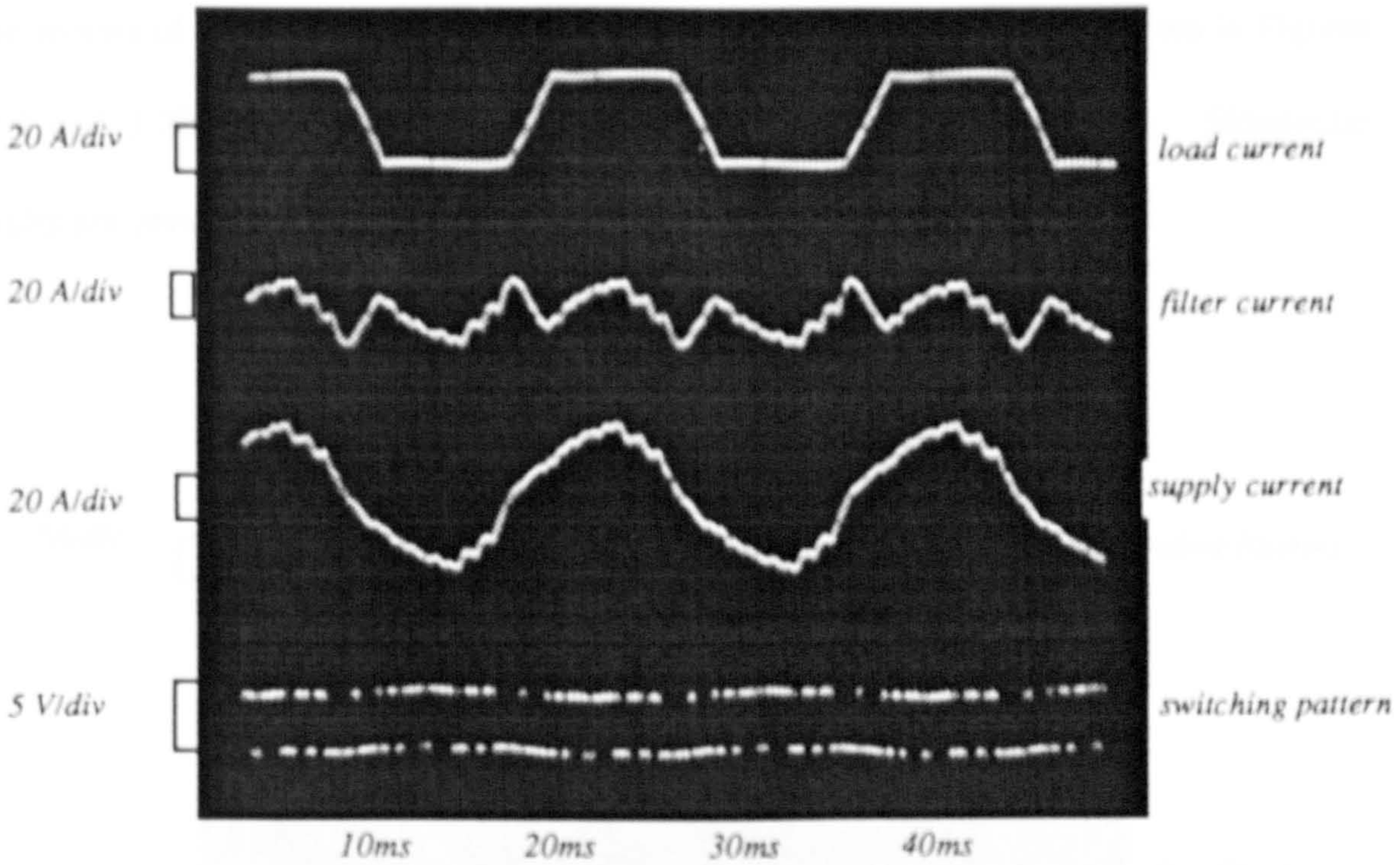


Figure 3.17 The performance of system with rectifier-inductive resistive load

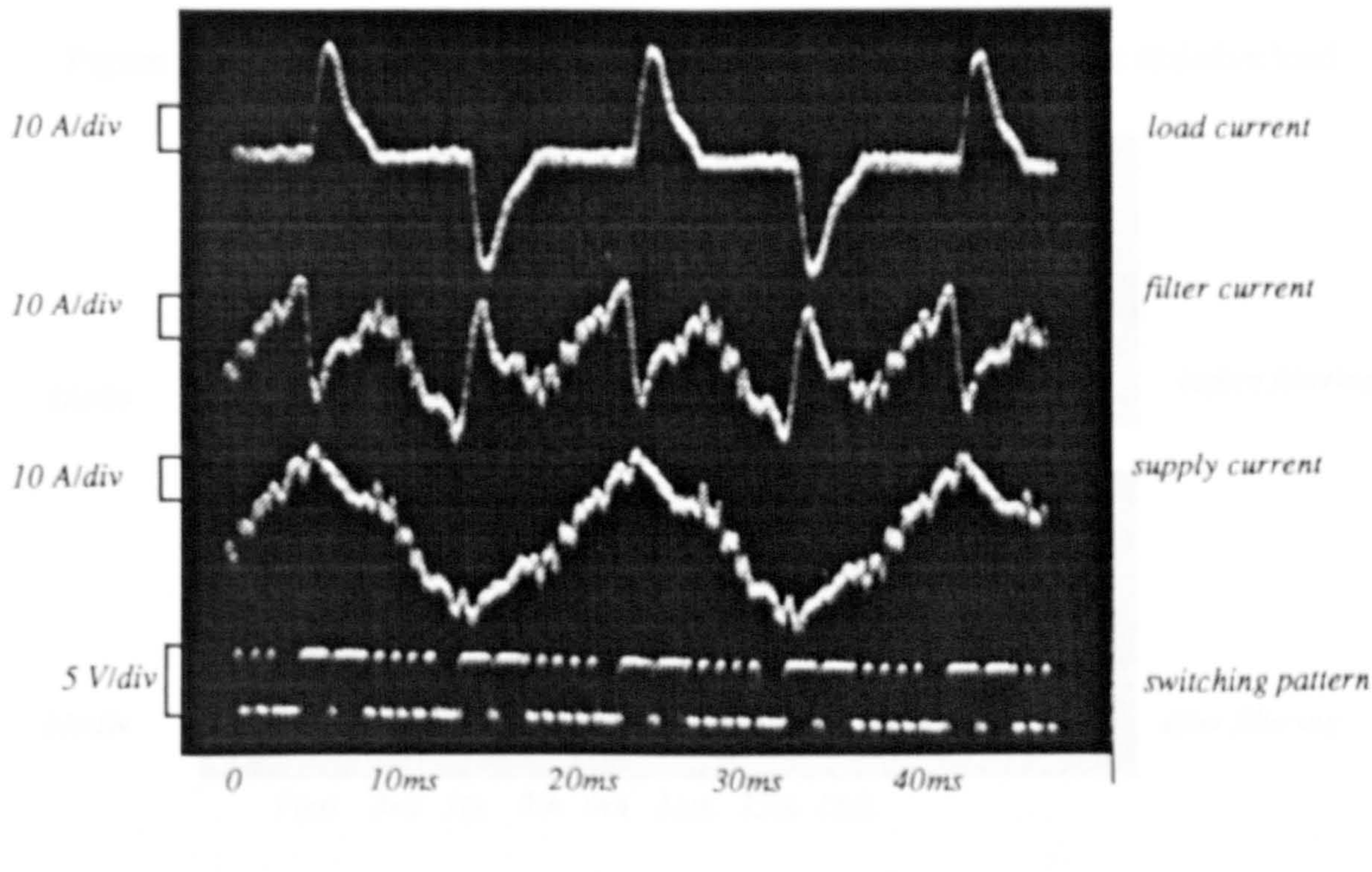


Figure 3.18 The performance of system with rectifier-capacitive resistive load

The spectra of the supply current with and without the active filters are shown in Figures 3.19 and 3.20 showing significant reductions in the current harmonics. Simulation results are presented in Figure 3.21.

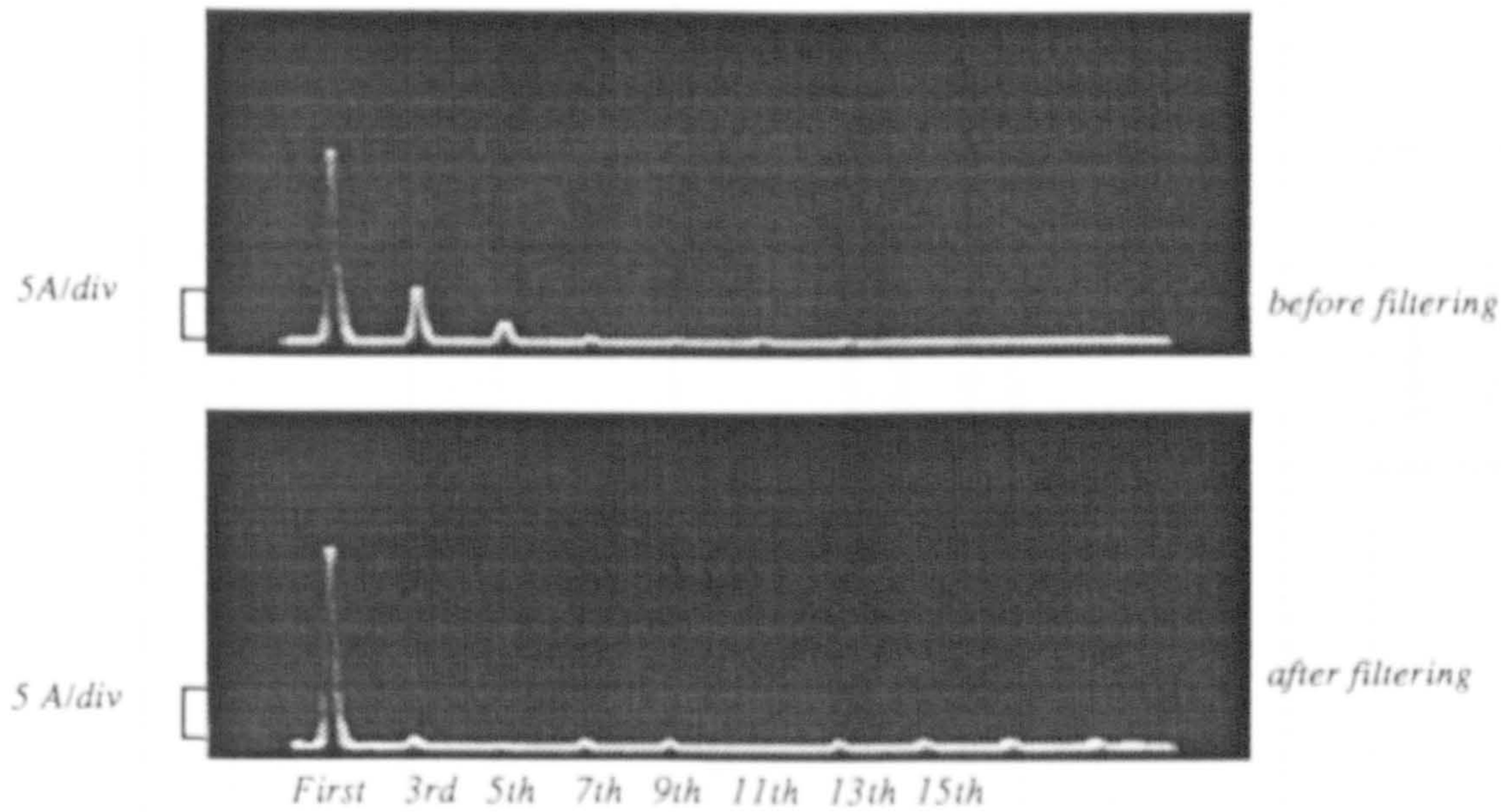


Figure 3.19 The frequency spectra of system with rectifier-inductive resistive load

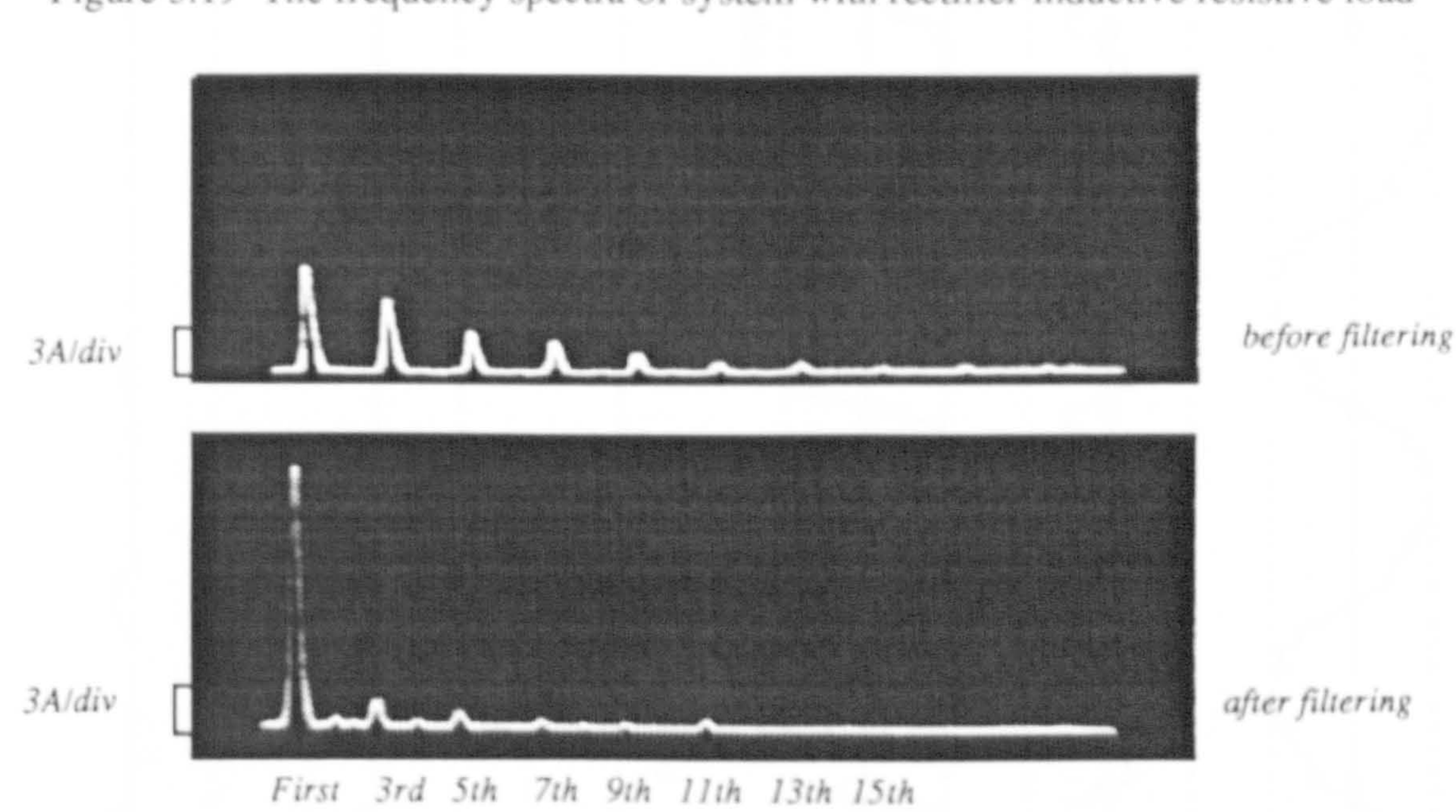


Figure 3.20 The frequency spectra of system with rectifier-capacitive resistive load

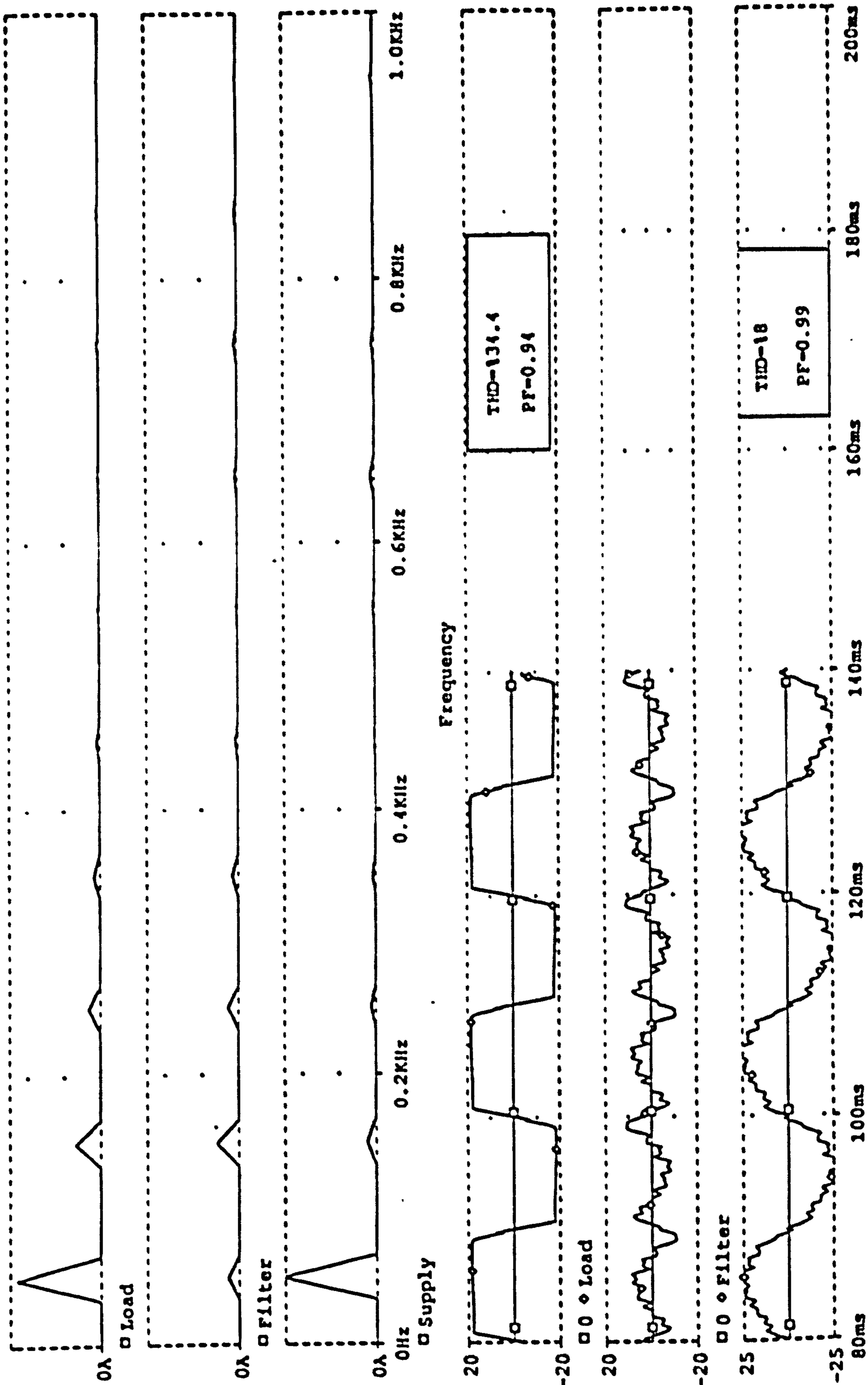


Figure 3.21 Simulation results of system configuration (Figure 3.15)

Tables 3.15 and 3.16 provide a summary of the performance of the system including the total harmonic distortion (THD), the power factor (PF) of the resulting supply current and the efficiency of the filter

Table 3.15
Harmonic performance of system with rectifier-inductive resistive load

	Before Filtering		*After Filtering*	
The rms value of supply current				
I_1 *(rms)*	*17.19*		*18.48*	
Fourier Components of the supply current				
Harmonics No	*Amplitude*	*Phase(radians*	*Amplitude*	*Phase (radian)*
I_1	*16.17. (100)*	*-0.0596*	*18.30. (100)*	*-0.028*
I_3. (I_3/I_1)	*4.82. (29.8)*	*-0.208*	*0.14. (0.79)*	*1.735*
I_5. (I_5/I_1)	*2.43. (15.0)*	*-0.383*	*0.13. (0.76)*	*-0.905*
I_7. (I_7/I_1)	*1.19. (7.3)*	*-0.601*	*0.01. (0.09)*	*3.162*
I_9. (I_9/I_1)	*0.51. (3.1)*	*-0.960*	*0.49. (2.72)*	*4.561*
I_{11}. (I_{11}/I_1)	*0.21. (1.3)*	*4.368*	*0.16. (0.90)*	*-1.061*
I_{13}. (I_{13}/I_1)	*0.23. (1.4)*	*3.365*	*0.69. (3.79)*	*3.754*
I_{15}. (I_{15}/I_1)	*0.30. (1.9)*	*2.8588*	*0.42. (2.31)*	*-0.176*
I_{17}. (I_{17}/I_1)	*0.28. (1.7)*	*2.599*	*0.21. (1.48)*	*0.941*
I_{19}. (I_{19}/I_1)	*0.23. (1.4)*	*2.470*	*0.52. (2.86)*	*2.563*
I_{21}. (I_{21}/I_1)	*0.15. (0.9)*	*2.396*	*0.31. (1.72)*	*4.387*
I_{23}. (I_{23}/I_1)	*0.08. (0.5)*	*2.428*	*0.33. (1.84)*	*3.395*
I_{25}. (I_{25}/I_1)	*0.03. (0.2)*	*3.141*	*0.27. (1.53)*	*3.139*
I_{27}. (I_{27}/I_1)	*0.05. (0.3)*	*3.821*	*0.49. (2.70)*	*-0.019*
I_{29}. (I_{29}/I_1)	*0.06. (0.4)*	*3.908*	*0.26. (1.47)*	*3.882*
I_{31}. (I_{31}/I_1)	*0.08. (0.5)*	*3.773*	*0.12. (0.69)*	*4.394*
I_{33}. (I_{33}/I_1)	*0.08. (0.5)*	*3.463*	*0.09. (0.54)*	*4.649*
I_{35}. (I_{35}/I_1)	*0.07. (0.4)*	*3.226*	*0.05. (0.30)*	*3.150*
I_{37}. (I_{37}/I_1)	*0.06. (0.4)*	*2.946*	*0.06. (0.37)*	*3.549*
The distortion component of the supply current and the Total Harmonic Distortion				
I_{d1}	*5.55*		*1.42*	
THD	*34.4 %*		*7.78 %*	
The harmonic and phase displacement and power factors of supply current				
μ	*0.94*		*0.99*	
$COS\,\theta_1$	*0.99*		*0.99*	
PF	*0.93*		*0.98*	
The real power of load and dissipation power of active filter and efficiency				
P (W)	*679.10*		*768.63*	
η	*0.88*			

Table 3.16
Harmonic performance of system with rectifier-capacitive resistive load

	Before Filtering		After Filtering	
The rms value of supply current				
I_s (rms)	6.30		7.56	
Fourier Components of the supply current				
Harmonics No	Amplitude	Phase (radian)	Amplitude	Phase (radian)
I_1	4.66(100)	0.364	7.50(100)	0.209
I_3. (I_3/I_1)	3.28(70.6)	4.342	0.24(3.3)	4.286
I_5. (I_5/I_1)	1.84(39.4)	2.367	0.12(1.8)	2.110
I_7. (I_7/I_1)	1.35(28.9)	0.625	0.14(2.0)	1.409
I_9. (I_9/I_1)	0.93(19.9)	-1.331	0.14(1.9)	-0.269
I_{11}. (I_{11}/I_1)	0.43(9.2)	3.205	0.10(1.4)	0.033
I_{13}. (I_{13}/I_1)	0.31(6.6)	1.564	0.18(2.5)	1.020
I_{15}. (I_{15}/I_1)	0.19(4.0)	0.237	0.30(4.1)	-0.113
I_{17}. (I_{17}/I_1)	0.12(2.5)	-0.822	0.18(2.5)	-0.275
I_{19}. (I_{19}/I_1)	0.12(2.5)	3.689	0.00(0.2)	1.626
I_{21}. (I_{21}/I_1)	0.08(1.7)	1.946	0.26(3.5)	2.054
I_{23}. (I_{23}/I_1)	0.08(1.7)	0.608	0.06(1.0)	3.967
I_{25}. (I_{25}/I_1)	0.06(1.2)	-0.564	0.22(3.0)	-1.544
I_{27}. (I_{27}/I_1)	0.04(0.8).	-1.567	0.06(1.0)	1.483
I_{29}. (I_{29}/I_1)	0.04(0.8)	3.194	0.02(0.4)	-1.441
I_{31}. (I_{31}/I_1)	0.04(0.8)	1.469	0.06(1.0)	2.939
I_{33}. (I_{33}/I_1)	0.06(1.2)	0.009	0.06(1.0)	3.714
I_{35}. (I_{35}/I_1)	0.06(1.2)	-1.067	0.16(2.2)	3.004
I_{37}. (I_{37}/I_1)	0.03(06)	3.895	0.22(3.1)	2.901
The distortion component of the supply current and the Total Harmonic Distortion				
I_{di}	4.20		0.77	
THD	89.6%		10.38%	
The harmonic and phase displacement and power factors of supply current				
μ	0.74		0.99	
$COS\,\theta_i$	0.93		0.97	
PF	0.69		0.97	
The real power of load and dissipation power of active filter and efficiency				
P (W)	183.9		315.0	
η	0.58			

These Tables relate to the situation where the filter operation is optimised for the reduction of total harmonic distortion. The reduction achieved is different for the two

types of rectifier loads . For the rectifier circuit with the inductive load the power factor without the filter is already very high and therefore the effect of the filter is negligible and the filter efficiency is relatively high (0.88). For the rectifier circuit with the capacitive smoothing the reduction in the total harmonic distortion achieved is 91% but the filter efficiency is low (0.58) .

To optimise the system with the aim of improving in the power factor and maximising the efficiency one approach is to minimise the apparent power. With this approach as shown in the Tables 3.17 and 3.18, a high operating efficiency can be achieved but the reduction in the THD is obviously not as high as the previous case. These facts are summarised in Tables.

Table 3.17
Comparison of two optimisation approaches of system with rectifier-inductive resistive load

	THD	*PF*	*η*	I_L
Before filtering	*34.4%*	*0.93*	*1.0*	*17.19*
After filtering (for THD_{min})	*7.78%*	*0.98*	*0.88*	*18.48*
After filtering (for S_{min})	*13.75%*	*0.98*	*0.94*	*18.07*

Table 3.18
Comparison of two optimisation approaches of system with rectifier-capacitive resistive load

	THD	*PF*	*η*	I_L
Before filtering	*89.69%*	*0.69*	*1.0*	*6.30*
After filtering (for THD_{min})	*10.38%*	*0.97*	*0.58*	*7.50*
After filtering (for S_{min})	*21%*	*0.83*	*0.86*	*5.93*

3.5 Conclusion

There is close agreement between the results of the simulation study on the new circuits with the experimental work. All three circuits were optimised for best performance in respect of THD which was achieved in the region of %3 to 11%. On this basis, Scheme No. 4 (section 2.5.1) has superior performance in reduction of harmonics with high efficiency. Scheme No 6 and 7.(section 2.5.1) have lower efficiency but their effect on the improvement in the power factor are greater.

CHAPTER FOUR

Conclusions and Future Work

The unified approach for the classification, design and synthesis of active filters proposed in this work has been shown to be viable. With this approach the basic parameters which control the characteristics of active filters are easily identified, thereby providing a useful procedure for selection of suitable circuits for various applications. The main features of this approach are summarised in this chapter

The work carried out was limited to the application of active filters for controlling current harmonics generated by non-linear loads in ac power systems. There is considerable scope for applying this approach to the control of voltage harmonics in ac systems which is also outlined here.

4.1 Conclusions

The results of this study including the design, analysis and experimental work on a number of new circuits are summarised below.

1. The classification method proposed in this thesis is based on techniques of 'tracking' the required filter current by controlling di /dt and $d^2 i/ dt^2$ of the filter current.

2. Since the filtering requirements for non-linear loads are likely to vary, it does not seem possible to find a single topology which would meet all the requirements. Therefore the unified approach allows the designer to select the most appropriate approximation tracking technique and the associated circuit configuration for a given application.

3. Since the unified approach is based on the control of di /dt and d^2i /dt^2 the key element in active filters is an inductor. It is the control of energy flow in the inductor which defines the characteristics of the filters. This control is achieved through the control of voltage across the inductor in a number of different ways which in turn, define the various circuit configurations.

4. The compensation strategy and the corresponding circuit topology can be selected on the basis of the factors to be optimised. In this work the new circuits were optimised to reduce THD and the apparent power consumed by non-linear loads including the filters.

5. The effectiveness of three proposed active filters have been assessed by applying them to two types of loads: a rectifier circuit with inductive smoothing (i.e. low level of input current harmonics) and a rectifier circuit with capacitive smoothing (i.e. high level of input current harmonics). It is confirmed that it is possible to improve the THD as well as the overall power factor.

6. It is shown that, for most of the proposed schemes, the resonant current of the L-C components in the active filters can be prevented from appearing in the supply current by reaching a compromise between the size of the circuit elements and the switching frequency. This of course has the advantage of reducing the apparent power demand in the system.

7. The switching frequencies (2 kHz to 4 kHz) in the proposed schemes are generally not high, therefore the losses in the switches (especially the switching losses) are much less than those in the inductor. No attempt was made to reduce the losses in the inductors, for example by selection of special cores which may have the effect of increasing the overall cost.

8. Whilst the experimental work was based on a low voltage, low power system, the principles outlined are applicable to high voltage and power ratings provided that suitable switches are available.

4.2 Future Work

The experimental work was carried out on open-loop systems. The switching patterns for the various circuits were precalculated using the optimisation method described in Appendix B. In practical applications this approach would be too slow for on-line control. There is considerable scope for work on methods of operating these types of filters in a closed loop environment. Since it is not possible to predict current harmonics in power systems with the required degree of accuracy, the investigation on use of neural networks would prove fruitful.

The unified approach proposed in this work is equally applicable to the construction of active series filters for control of voltage harmonics in power systems. Recently, a combined system of shunt passive and series active filter has been proposed by the several authors [Peng 93, Rastogi 94, Herve 95]. Figure 4.1 illustrates a general diagram of series active filtering technique. The series active filter is controlled to present a low impedance at the fundamental frequency and high resistance to the supply and load harmonics.

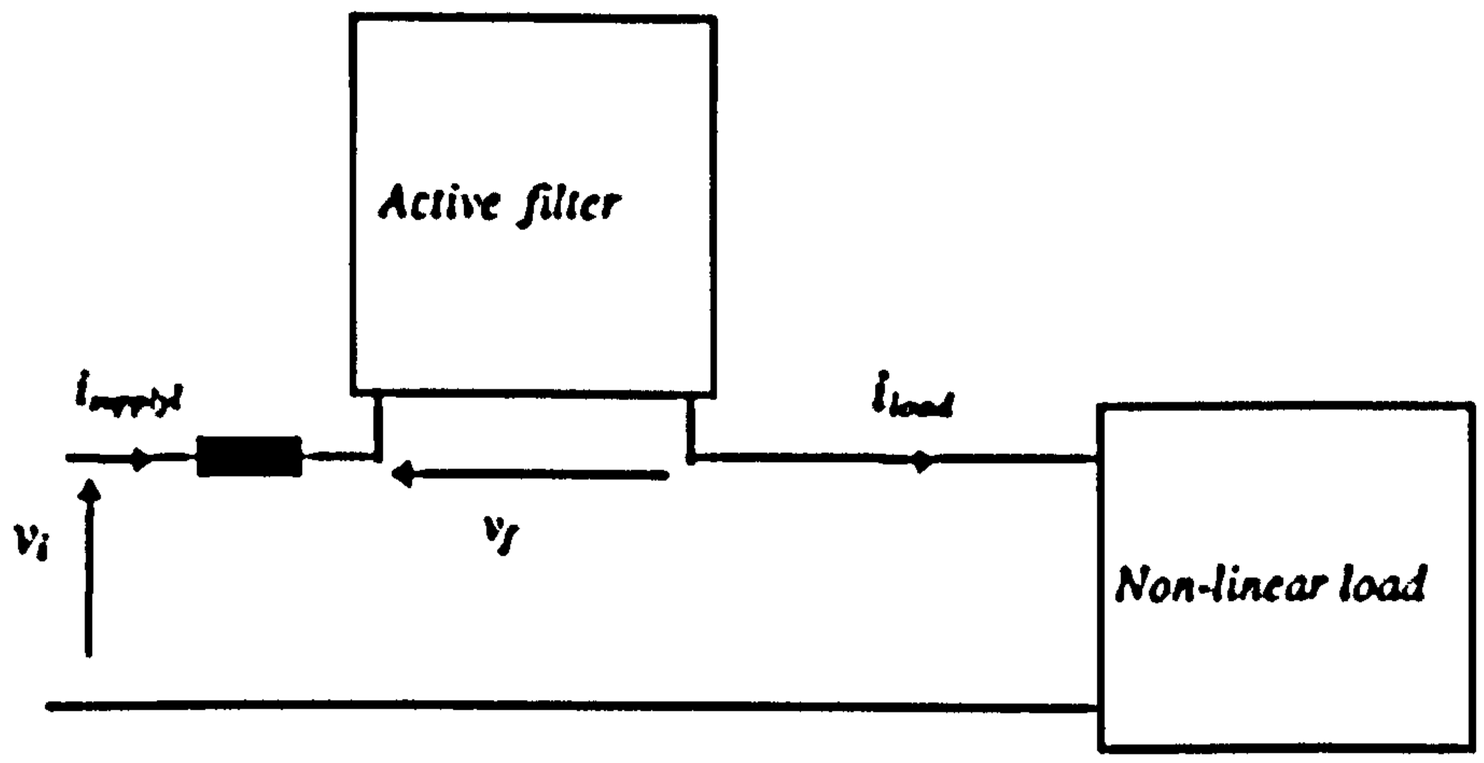


Figure 4.1 Principle of series active filter technique

It was shown in chapter two that the basic principle of active filters for controlling current harmonics is to control the flow of energy between the supply and the filter by altering the circuit topology via switches and the management of energy flow in the inductive elements of the filters. This principle can be extended to provide a unified approach to the classification of series filters for control of voltage harmonics as follows.

The variation of the stored energy in a capacitor is proportional to the rate of change of voltage across it and can be expressed as:

$$P_{Capacitor}(t) = v_C i_C = v_C\left(C\frac{dv_C}{dt}\right) = \frac{C}{2}\frac{dv_C^2}{dt}$$

Since the objective of series active filters is to control the voltage and its rate of change, rather than the current, capacitors are inherently better for this purpose. The classification technique proposed for the active current harmonic filters can be extended to the voltage harmonic filters. Three typical configurations with relevant equations are given below .

(a) Both capacitor terminals fixed:

The arrangement is illustrated in Figure 4.2. The pairs of switches S_1, S_2 and S_3, S_4 operate synchronously in anti-phase. The following equations represents two states of the structure:

When the pair of switches S_1, S_2 are in the 'on' state

$$\frac{dv_f}{dt} = \frac{i_{source} + i_L}{C}$$

When the pair switches S_3, S_4 are in the 'on' state

$$\frac{dv_f}{dt} = \frac{i_{supply} - i_L}{C}$$

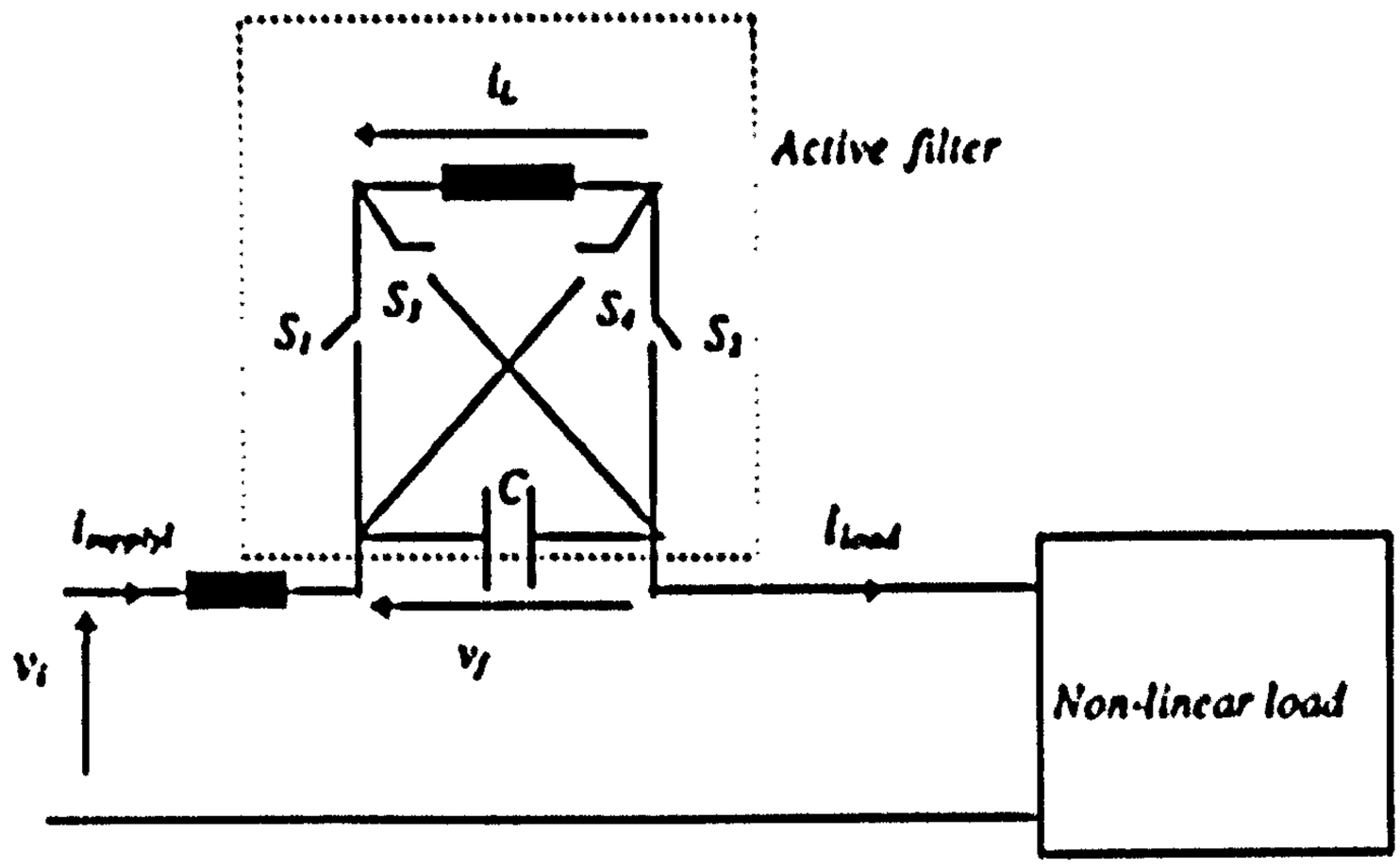


Figure 4.2 Proposed scheme (a) for series active filter

(b) <u>One capacitor terminal floating and the other fixed</u>:

The arrangement is shown in Figure 4.3.

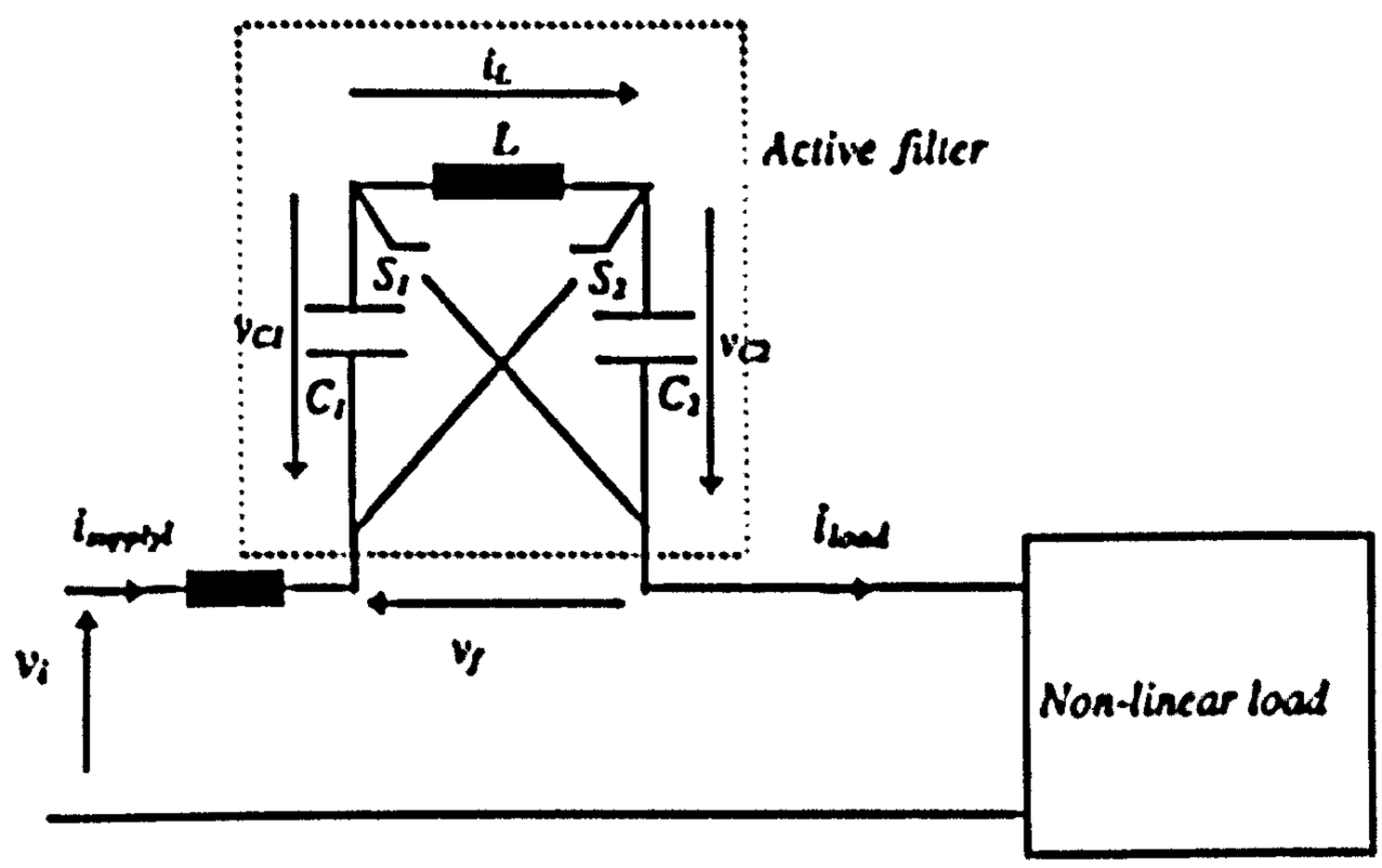


Figure 4.3 Proposed scheme (b) for series active filter

The two switches S_1 and S_2 operate in anti-phase. The rate of change of voltage across the capacitor for this configuration can be computed with the following equations:

When switch S_1 is in the 'on' state

$$\frac{dv_f}{dt} = \frac{dv_{C1}}{dt} = \frac{I_{supply}}{C_1}$$

$$\frac{dv_{C2}}{dt} = -\frac{I_L}{C_2}$$

When switch S_2 is in the 'on' state

$$\frac{dv_f}{dt} = \frac{dv_{C2}}{dt} = \frac{I_{supply}}{C_2}$$

$$\frac{dv_{C1}}{dt} = -\frac{I_L}{C_1}$$

(c) Both capacitor terminals floating:

The arrangement is shown in Figure 4.4.

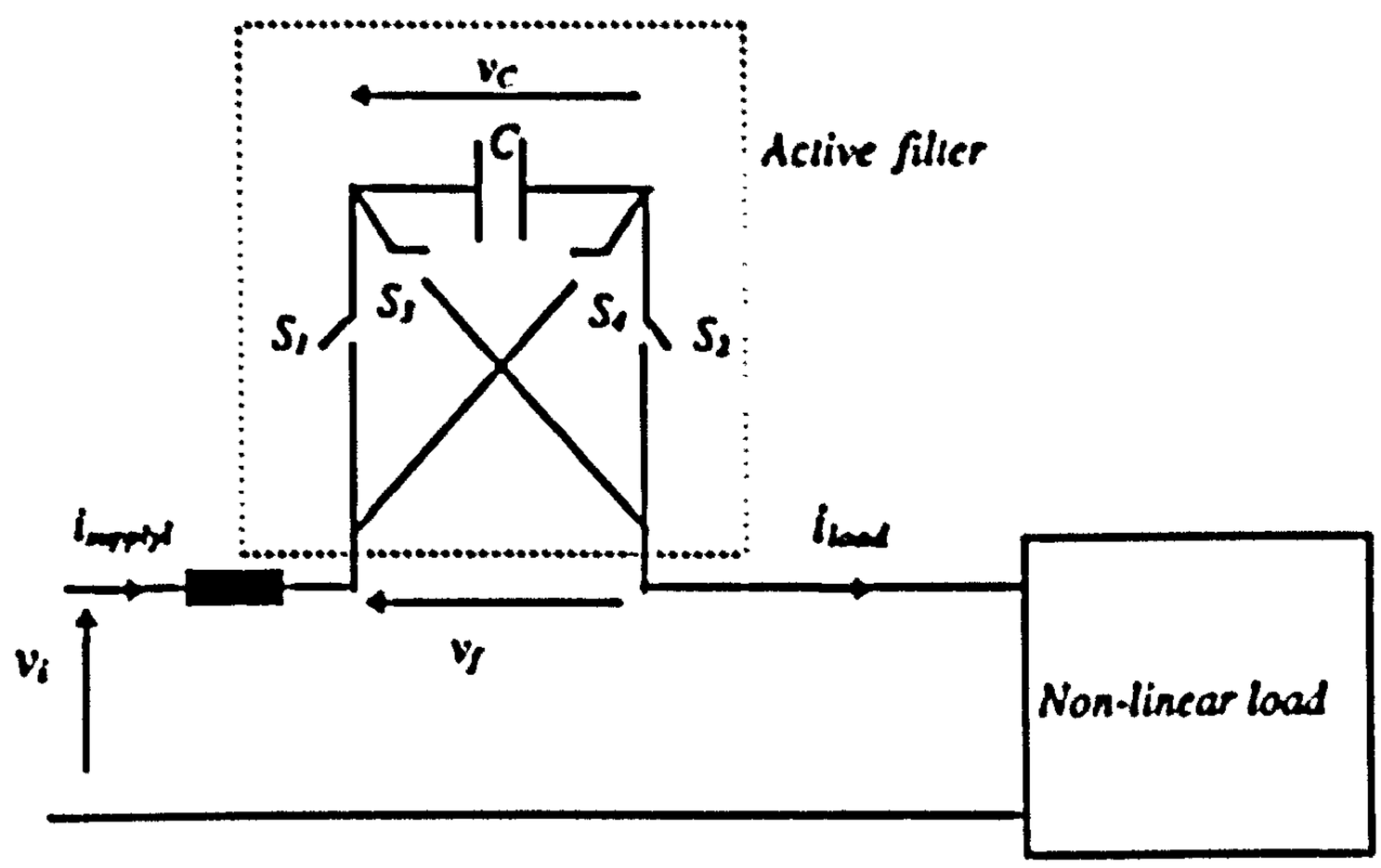


Figure 4.4 Proposed scheme (c) for series active filter

The pairs of switches S_1, S_2 and S_3, S_4 operate synchronously in anti-phase. The following equations apply for the two states of the structure:

When the pair of switches S_1, S_2 are in the 'on' state

$$\frac{dv_f}{dt} = \frac{dv_C}{dt} = \frac{I_{switch}}{C}$$

When the pair of switches S_3, S_4 are in the 'on' state

$$\frac{dv_f}{dt} = -\frac{dv_C}{dt} = \frac{I_{switch}}{C}$$

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APPENDIX A

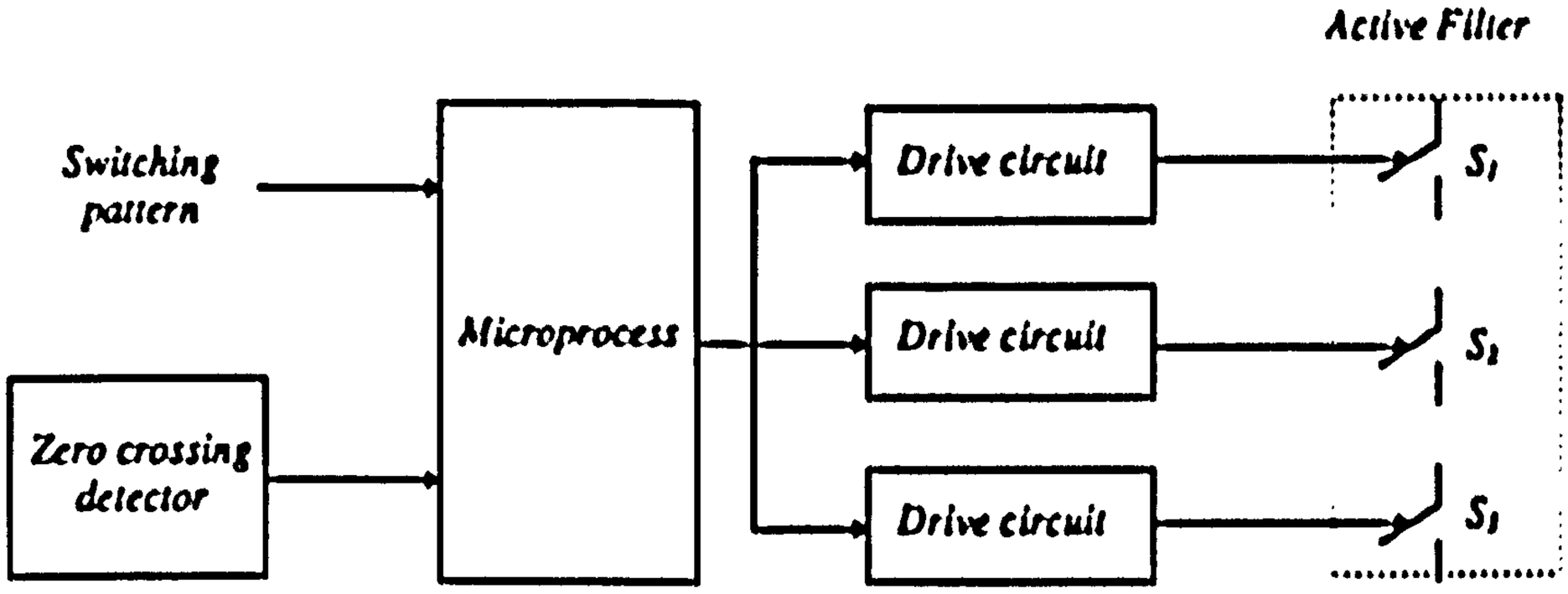
Microprocessor Control of Active Filters

The switching pattern are evaluated using the optimisation method as described in Appendix B. It was shown in chapters 2 and 3 that the switching pattern which is used to control the switches in the active filters has to be varied as the load conditions change.

The control of active filters requires a fast, accurate and flexible controller. The microprocessor-based controllers can provide all these features. In particular, flexibility can be achieved through software. An Intel SDK-86 microprocessor development board which is programmed in machine code is used for this purpose. In this appendix the software design and experimental setup with complete driver circuits for the switches are detailed.

A.1 Software Design

Figure A.1 shows the block diagram of the controller.



A.1 Block diagram of the controller

The appropriate switching patterns that are evaluated theoretically for a number of load conditions are stored in suitable addresses in the microprocessor EPROM. Each address is labeled by one of the parameters (such as the magnitude of the load resistance), relating to the load condition and is specified with a number.

When this parameter is entered through the keyboard or a digital input port, the program which is written in 8086 assembly language searches for the corresponding switching pattern. Before generating the switching pattern, the program should wait and receive a trigger pulse from the zero crossing detector. This synchronieses the timing of the switching pulses with the supply voltage. The program then transmits the required switching pulses to the driver circuits via the output ports. The flowchart shown in Figure A.2 describes the procedure for generating switching patterns. The listing of the assembly program can be found at the end of this appendix

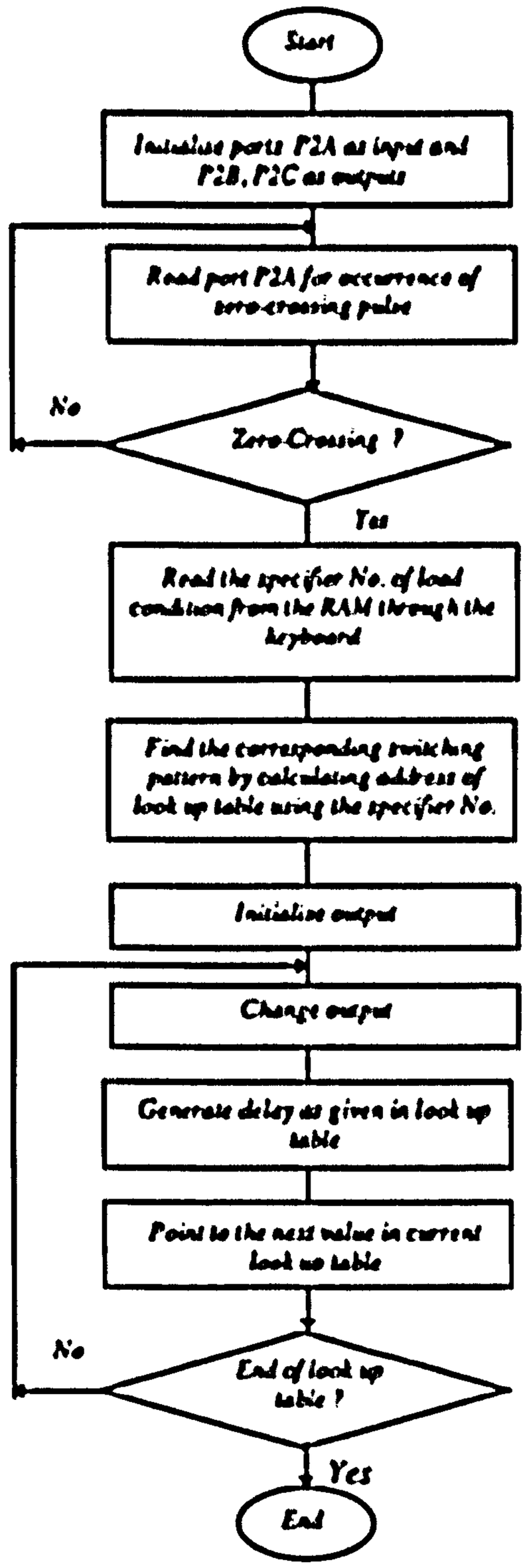


Figure A.2 Flowchart of 8086 program

A.2 Switch Implementation

The most popular semiconductor devices are thyristors, gate-turn off types (GTO's), BJTs, and MOSFETs. These devices have their own particular features that make them especially suited to a particular application. For example, the thyristor is capable of

passing high currents and blocking large voltages, the BJT is a fast switching device, and the MOSFET is simple to drive and has a low 'on' resistance.

In this work, the author has limited the supply voltages to 60 V, so the need for high blocking voltage is not that great. More important factors are the simplicity of driving, low switching losses and high switching speed. Consequently the MOSFET IRFP462 was selected which is a N-channel device with maximum drain source voltage of 500 V, maximum drain current of 17 Amp, and 'on' resistance of 0.35 Ω.

As explained in the list of symbols, since the MOSFET is a one-way switch, it has to be connected to a bridge rectifier to operate as a bi-directional switch shown in Figure A.3.

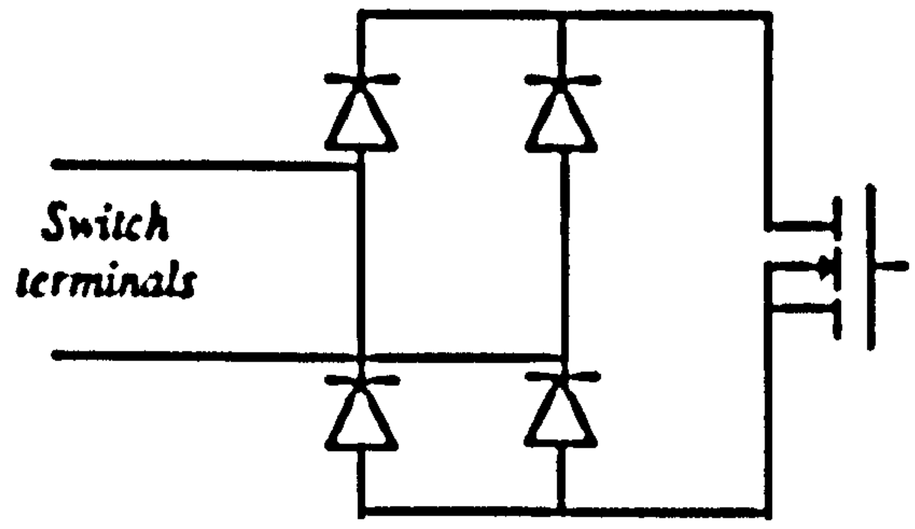


Figure A.3 The bi-directional switch implementation

A.3 The Need for Isolation

The MOSFETs need the control signal to be applied across the gate and source. This is straightforward when all the sources are connected together, but in this application, the source terminals can not be connected together due to the presence of the bridge rectifier. Therefore separate isolated power supplies should be used for the switches, i.e. neither of the output terminals is connected to the ground. To apply the control

signals to the three isolated driver circuits, opto-isolaters are necessary. The 6N137 opto-isolator which incorporates high speed logic circuits and has a propagation delay of the order of 50ns are suitable for this application.

A.4 Complete Driver Circuit

The driver circuit used is shown in the Figure A.4. To provide the necessary 5 volts for the opto-isolator logic from the 15 volts for the MOSFET driver a simple potential divider using two resistors, 100Ω and 200 Ω, were used. The 4.7 kΩ pull-up resistor at the output of the opto-isolator was found to give the fastest response.

To prevent any possible damage to the driver circuits in the event that a MOSFET fails a resistor is inserted at the output of the driver. The capacitor in parallel with the resistor is to ensure that high switching speed is maintained. The Zener diode at the output of the MOSFET driver is for extra protection in case of large voltage spikes on MOSFETs.

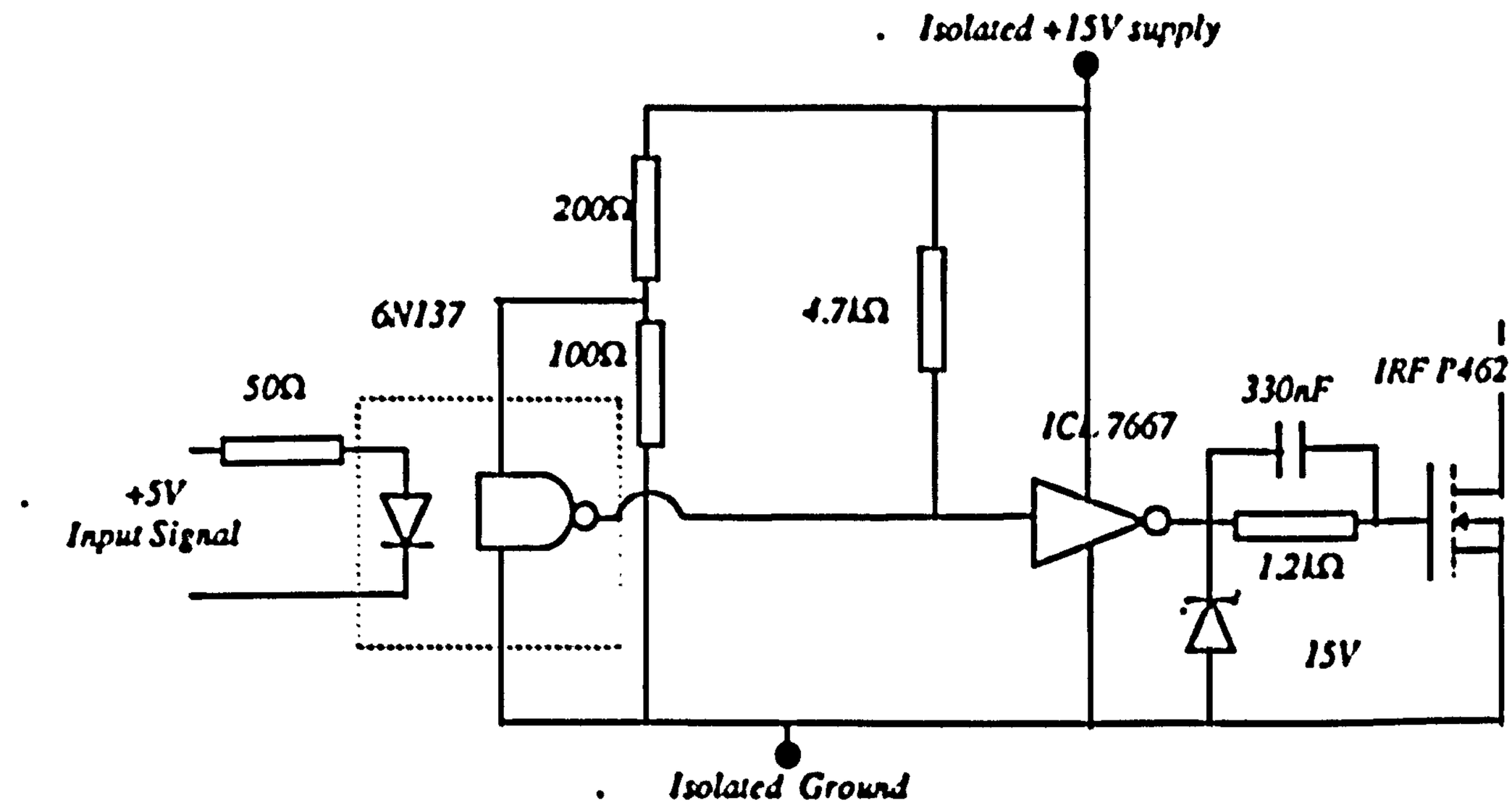


Figure A.4 The complete driver Ccircuit

Assembly program

```
80286.TAB
INTEL
DUMMY SEGMENT PARA AT 100 'CODE'
; This program generate the switching pattern for the active filter scheme 4 -section 2.5.1
; The No.of the required tables should be supplied via the keyboard to the address 150

        MOV DX, 0FFFEH          ;ENABLE PORT P2
        MOV AL, 90H             ;MAKE PORT A AS INPUT PORT B, C AS OUTPUT
        OUT DX, AL

ZCROSS  MOV DX, 0FFF8H          ;ADDRESS OF PORT 2A TO DX
LOOP    IN  AL, DX              ;SYNCHRONIES WITH ZERO CROSSING DETECTOR
        AND AL, 01H
        JZ  LOOP
        MOV DI, 0H

START   MOV SI, 150H            ;READ TABLE NUMBER
        MOV DX, 0FFFCH          ;ADDRESS OF PORT 2C TO DX
        MOV CL, [SI]
        MOV BX, OFFSET TABLE    ;BX CONTAINS TABLES ADDRESS
        XOR CH, CH              ;CLEAR TOP 8 BITS OF C
        SHL CX, 1               ;MAKE WORD ADDRESS (MULTIPLY BY 2)
        ADD BX, CX              ;POINT INTO TABLE
        MOV SI, CS:[BX]         ;ADDRESS OF SWITCH PATTERN TO SI
        MOV CX, CS:[SI]         ;LOAD CONTENTS OF SI INTO CX
        MOV AH, 03H

SWITCH  MOV AL, 10H
        OUT DX, AL
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        ADD SI, 2H              ;POINT TO NEXT WORD IN TABLE
        MOV BX, CS:[SI]         ;GET NEXT WORD FROM TABLE
        MOV AL, AH
        XOR AL, 0FH
        MOV AH, AL
        OUT DX, AL

DELAY   DEC BX                  ;GENERATE DELAY
        JNZ DELAY
        SUB CX, 02H
        JNZ SWITCH
        ADD DI, 01H
        CMP DI, 02H
        JE  ZCROSS
        JMP START
```

```
TABLE   WORD TAB0, TAB1

; TAB0 contains a switching pattern for elimination of harmonic current of a rectifier circuit with
smoothing  inductor
; The compensation achieved:  NH_max=37, THD=0.02
; Filter components: L= (4mH,1.9Ω), C=80u
; Nonlinear load components: Bridge rectifier, L=80m, R_L=1.9Ω

TAB0    WORD  0B21H, 0141H, 0721H, 0011H, 06C1H, 0011H, 05A1H
        WORD  0821H, 0041H, 04C1H, 0411H, 0291H, 02E1H, 03D1H
        WORD  0191H, 0311H, 0461H, 0461H, 0291H, 0361H, 02E1H
        WORD  0431H, 0281H, 0421H, 02D1H, 03F1H, 02E1H, 05B1H
        WORD  02E1H, 03D1H, 02B1H, 0451H, 0291H, 03A1H, 0331H
        WORD  0471H, 0331H, 0401H, 04C1H, 01D1H, 04F1H, 0011H
        WORD  0661H, 0131H, 04F1H, 0321H, 0721H, 0011H, 06C1H
        WORD  0011H, 05A1H, 0821H, 0041H, 04C1H, 0411H, 0291H
        WORD  02E1H, 03D1H, 0191H, 0311H, 0461H, 0461H, 0291H
        WORD  0361H, 02E1H, 0431H, 0281H, 0421H, 02D1H, 03F1H
        WORD  02E1H, 05B1H, 02E1H, 03D1H, 02B1H, 0451H, 0291H
        WORD  03A1H, 0331H, 0471H, 0331H, 0401H, 04C1H, 01D1H
        WORD  04F1H, 0011H, 0661H, 0131H, 04F1H, 01E1H

; TAB1 contains a switching pattern for elimination of harmonic current of a rectifier circuit with
smoothing  capacitor
; The compensation achieved: NH_max=37, THD=0.017
; Filter components:  L= (4mH,1.9Ω), C=80uF
; Nonlinear load components:  Bridge rectifier, C=600uF, R_L=26.5Ω

TAB1    WORD  0B2H, 019H, 03BH, 033H, 03EH, 03FH, 033H
        WORD  038H, 032H, 03DH, 076H, 002H, 06DH, 002H
        WORD  055H, 004H, 058H, 027H, 051H, 01DH, 05DH
        WORD  012H, 075H, 010H, 051H, 019H, 068H, 01FH
        WORD  041H, 027H, 052H, 023H, 03EH, 023H, 045H
        WORD  02CH, 03EH, 029H, 041H, 035H, 04BH, 032H
        WORD  037H, 02BH, 03BH, 02DH, 03BH, 033H, 03EH
        WORD  03FH, 033H, 038H, 032H, 03DH, 076H, 002H
        WORD  06DH, 002H, 055H, 004H, 058H, 027H, 051H
        WORD  01DH, 05DH, 012H, 075H, 010H, 051H, 019H
        WORD  068H, 01FH, 041H, 027H, 052H, 023H, 03EH
        WORD  023H, 045H, 02CH, 03EH, 029H, 041H, 035H
        WORD  04BH, 032H, 037H, 02BH, 03BH, 014H

        END
```

APPENDIX B

Evaluation of Switching Pattern and Circuit Parameters by General Optimisation Method

A number of on - line and off - line switching pattern strategies [Choe 88, Akagi 88, Peng 88] have been reported in the literature which are suitable for active filter applications. Exact comparison of the performance and capability of the different active filter circuits through their theoretical and practical results require that the switching pattern and parameters are evaluated using the same method.

This appendix is concerned with a general optimisation method that can be used for all active filter circuits which are developed using the generalised approach in chapter 2. The method is suitable for determining the circuit parameters and switching pattern for constant and varying load conditions.

B.1 Load with fixed condition

With reference to the Figure B-1, if the coefficient of harmonics of $i_{supply} = i_{filter} + i_{load}$ are A_n and B_n, the functions

$$J = I_{rms} = f_1(t,x) = \sum_{n=1}^{NH_{max}} \sqrt{A_n^2 + B_n^2} \qquad \text{and}$$

$$J = I_1 = f_2(t,x) = \sum_{n=1}^{n=1} \sqrt{\frac{A_n^2 + B_n^2}{2}}$$

called the cost functions [Round 94] are the measure of supply current harmonics distortion and its effective value (apparent power) respectively. Where vector, t, denotes the switching instants and, x, denotes the size of the circuit elements. NH_{max} is the maximum range of frequency to be eliminated..

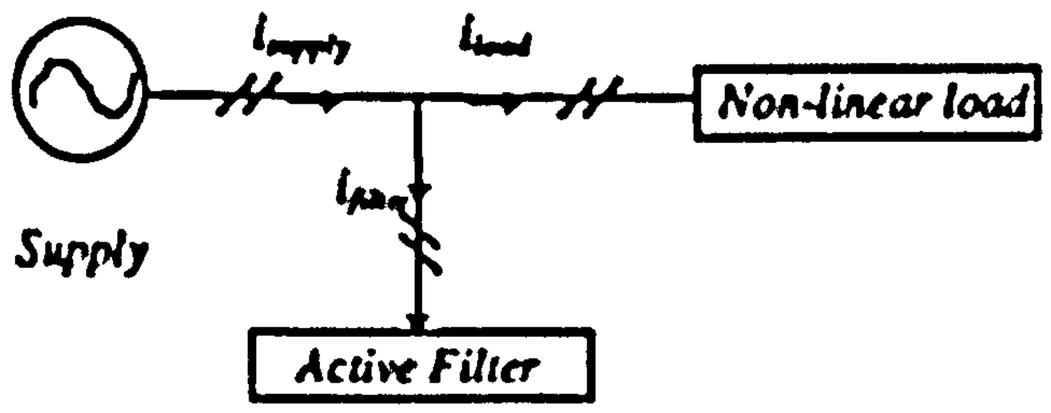


Figure B-1 Principal of shunt active filtering technique

The objective is to minimise the cost function by optimising the switching pattern and the circuit parameters subject to the following constraints.

- The switching instants should be in the order $0 \le t_1 \le t_2 \le \ldots \le \pi / \omega$ and also its pattern must have a half-wave symmetry to eliminate even harmonics.

- The circuit parameters should satisfy the limitations outlined in chapter 2 regarding the filtering requirements for each configuration.

The summary of algorithm used is shown in the Figure B-2 and described below.

(1) The starting points, t^0, for switching instants are calculated as the midpoints of pulses in a uniform switching pattern or can be taken as random values $t_1^0, t_2^0, t_3^0 \ldots, t_n^0$ (n is the number of switching instant in each half period) and also the starting values for the size of elements, x^0 are taken some random practical values (m is the number of elements in the circuit). For simplicity the two set of variables, vector matrix $[\ t\ ]_{n\times 1}$ and $[\ x\ ]_{m\times 1}$ are substituted by one vector matrix $[\ y\ ]_{n+m}$ such that $[\ y_1^0, y_2^0, \ldots, y_n^0, y_{n+1}^0, y_{n+2}^0, \ldots, y_{n+m}^0]^T = [\ t_1^0, t_2^0, t_3^0 \ldots, t_n^0, x_1^0, x_2^0 \ldots, x_m^0\ ]^T$

(2) The filter current i_f for the above switching points is calculated using Runge Kutta method for analysis of filter.

(3) The total current is calculated $i_{supply} = i_{load} + i_{filter}$

(4) The harmonic coefficients of the total current up to NH_{max} are evaluated and the cost function J is calculated

(5) The conjugate direction method [Luenberger, 73] is modified and employed to minimize the cost function and determine the optimum values of the switching instants and the circuit parameters as follows:

(a) The gradient of the cost function , J ' respect to the switching instants and circuit paramcters is evaluated.

$$g = \nabla J = [\, g_1, g_2, \ldots, g_n, g_{n+1}, g_{n+2}, \ldots, g_{n+m} \,]$$

$$= [\, \frac{\partial J}{\partial_{r_1}}, \frac{\partial J}{\partial_{r_2}}, \ldots \frac{\partial J}{\partial_{r_n}}, \frac{\partial J}{\partial_{r_{n+1}}}, \frac{\partial J}{\partial_{r_{n+2}}}, \ldots \frac{\partial J}{\partial_{r_{n+m}}} \,]$$

(b) The direction of the steepest descent is set to be equal to g^0 which is the initial value of g that is obtained respect to the initial values of switching pattern and circuit parameters,

$d^0 = - g^0$ or

$[\, d_1^0, d_2^0, \ldots, d_n^0, d_{n+1}^0, d_{n+2}^0, \ldots, d_{n+m}^0 \,] = - [\, g_1^0, g_2^0, \ldots, g_n^0, g_{n+1}^0, g_{n+2}^0, \ldots, g_{n+m}^0 \,]$

(c) $\tau = [\tau_1, \tau_2, \ldots, \tau_n, \tau_{n+1}, \tau_{n+2}, \ldots, \tau_{n+m}]^T$ are set to the small numbers that are proportional to the size of the steepest descent $d = [d_1, d_2, \ldots, d_n, d_{n+1}, d_{n+2}, \ldots, d_{n+m}]$ so that if for example s_i, is the number of digits of d_i then $\tau_i = 10^{-s_i}$

For i =1, 2, 3, . . .n+m

(d) The values of the switching instants and circuit parameters (elements) are evaluated by the following expression:

$y_1 = y_1^0$

$y_2 = y_2^0$

. . . .

$y_1 = y_1^0 + \alpha_4 d_1^0$ where $\alpha_4 = \tau_4$.

....

$y_{n+m} = y_{n+m}^0$

(e) The cost function J for the above switching instants and circuit parameters are recalculated and plotted against α_4.

(f) The initial switching pattern and circuit parameters are reset with the new values and α_4 is incremented and steps from d to e are repeated until the minimum value of J is found.

(g) The direction of the steepest descent d is evaluated as

$$d = -g^0 + \beta d^0 \quad \text{where} \quad \beta = \frac{g^T g}{g^{0T} g^0}.$$

(h) The starting switching instants and circuit parameters are reset by the new evaluated values of $y = [\, y_1, y_2, \ldots, y_n, y_{n+1}, y_{n+2}, \ldots, y_{n+m} \,]^T$

(i) The initial values of d and g are reset by the new values that occur at J_{min}.

(j) steps from c to i are repeated until the minimum value of J_{min} is obtained.

If the cost function J reaches zero, i.e., the total harmonics up to NH_{max} are canceled.

The main complete program that is written in Fortran language is shown in appendix C.

B.2 load with varying condition

For varying load conditions the aim is to determine the switching pattern whilst maintaining fixed values of the circuit parameters. The summary of the algorithm used is shown in Figure B.3 where i represents the varying load condition.

(1) The parameters and the switching pattern for the circuit are evaluated for one of the load conditions by the method described above.

(2) The values of circuit elements are reset to these values.

(3) The switching pattern for the filter with the evaluated parameters are optimized for different conditions of load and stored, and also the values of cost functions for each case are calculated and averaged.

(4) The above process is repeated for i = 2, 3, ... , k to achieve the minimum average of the cost functions. The corresponding values of the circuit elements at this minimum are considered as the best values. The corresponding switching patterns are the most optimum.

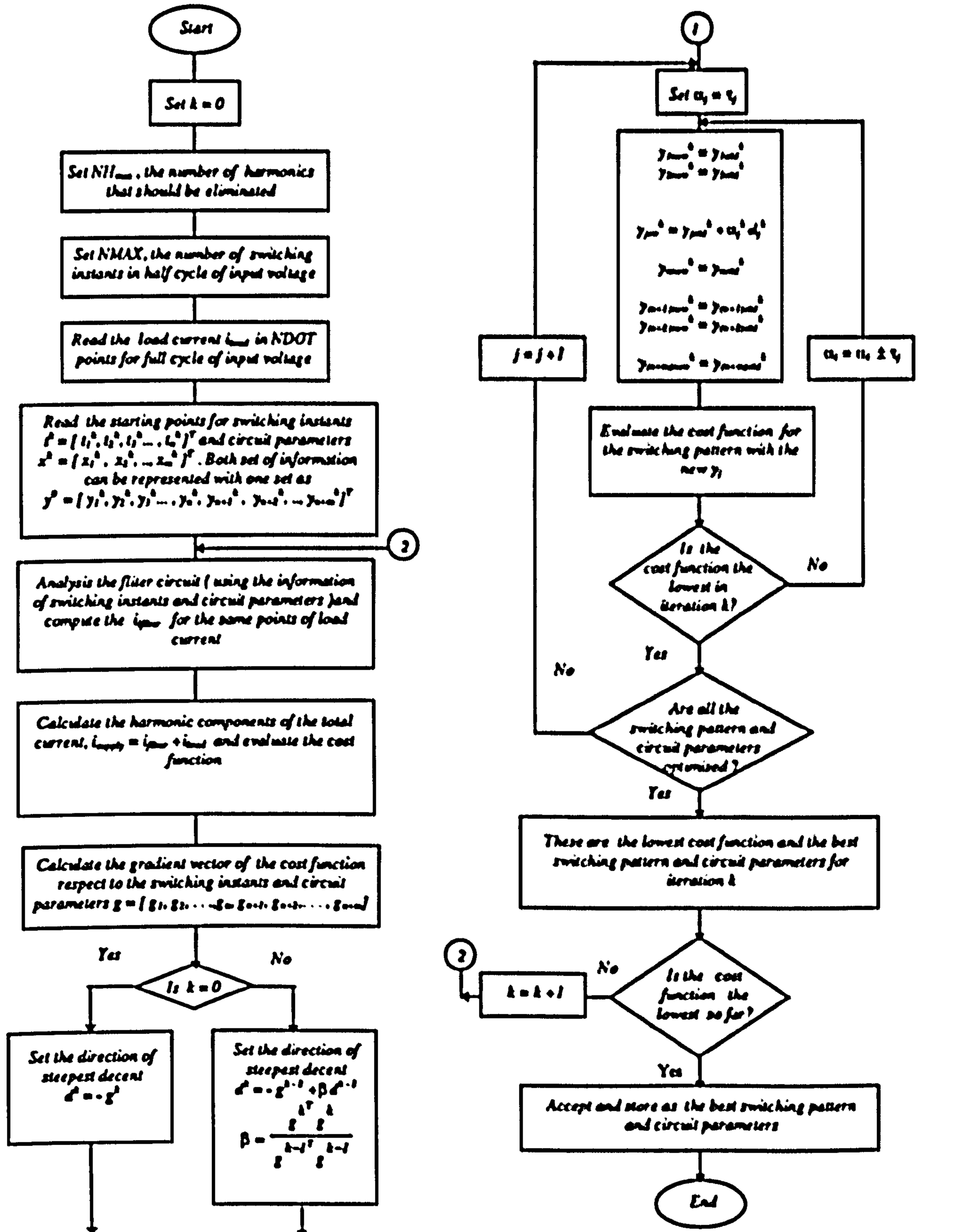


Figure B.2 Flowchart of optimisation method for the load with fixed condition

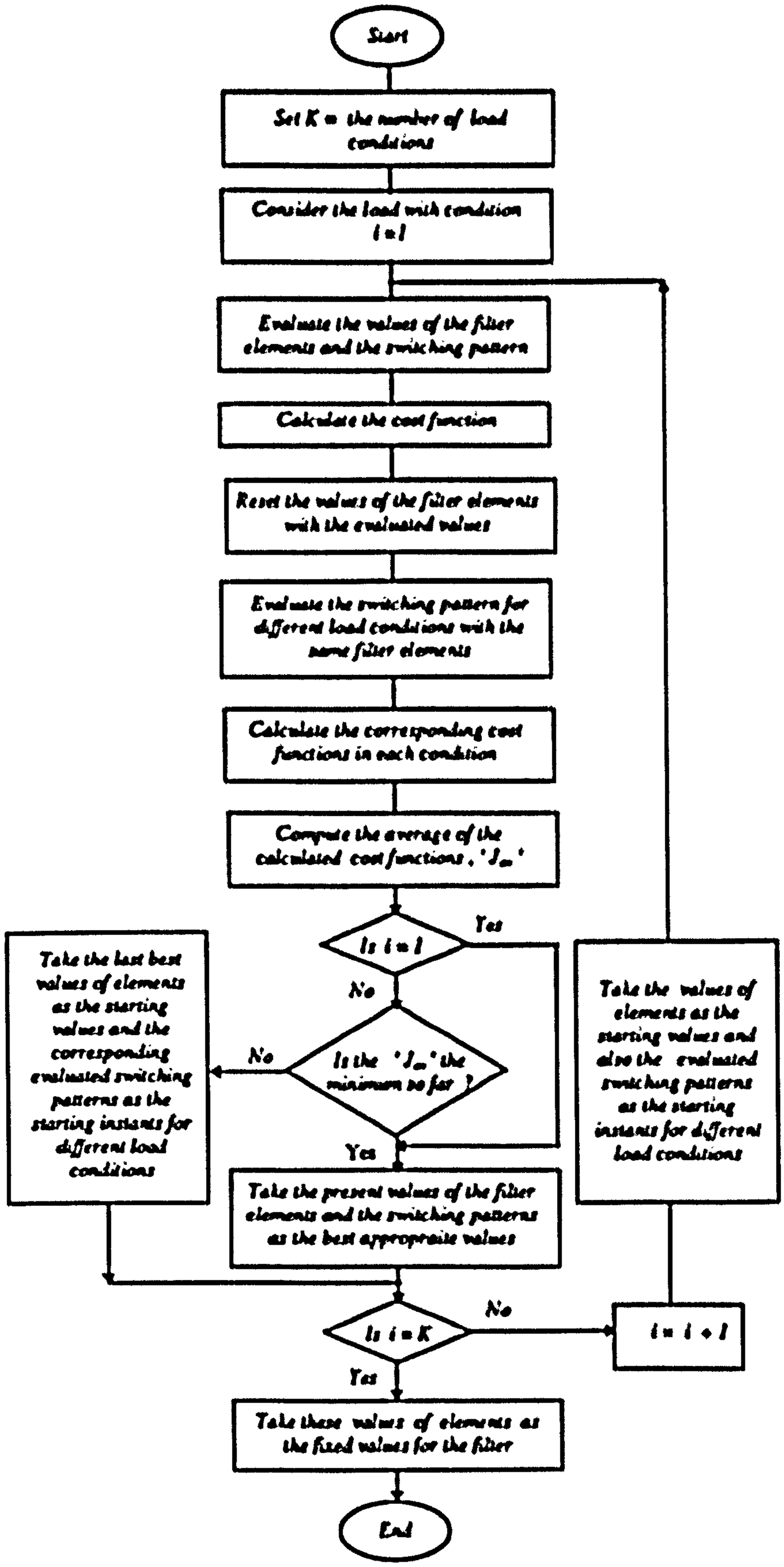


Figure B.3 Flowchart of optimisation method for a load with varying condition

APPENDIX C

FORTRAN Program for Optimisation Method

Detailed in Appendix B

The program consists of a main program and three subroutines; 'FUNC', 'FUNCERR' and 'DERRO'. In the main program, one of two Functions; 'THD' and 'Apparent power' as a cost function is chosen for minimisation and the sampling points of the load current are read. The active filter scheme for investigation is selected and the parameters and initial values for elements of the circuit are set. The main program also resets the switching instants and circuit parameters with new values after each iteration of execution of the program and finally the optimised switching pattern and circuit parameters are stored in to the output file. The analysis of active filter circuit for any evaluated switching pattern in any iteration is performed in a subroutine program 'FUNC', using Rung-Kutta method. Subroutine FUNCERR evaluates the cost function and related factors for any new operating conditions. The gradient vector of cost function with respect to the switching instants and circuit parameters and the direction of the steepest descent [Luenberger 73] are calculated in the subroutine 'DERRO.

C.1 Main Program

•The Following parameters and files should be specified before starting the program.

- MTS, may be set to 1 for minimisation of total harmonic distortion or 0 for the
- minimisation of effective value of supply current (Apparent Power)
- NMAX, is the number of switching instants in half cycle
- NHMAX, is the maximum order of harmonics which are required to eliminate
- NDOT, is the number of sampling of load current
- Peak value of sinusoidcal input supply voltage
- NELEMI, is the number of inductive elements
- NELEM, is the total number of inductive and capacitive elements
- SIZIN, Limited value for size of inductive elements
- SIZCAP, Limited value for size of capacitive elements
- The values of sampling points of load current should be supplied to the file called " load ".
- The initial values of inductive and capacitive elements should be supplied respectively to the file called "elements"in the order $L_1, L_2, L_3, \ldots, C_1, C_2, C_3, \ldots$

•After execution of the program, the information about optimised switching instants and circuit

•parameters can be found in the file called "results". This file also contains all the parameters

•related to the performance of active filter such as Total harmonic distortion (THD), Efficiency

•(η) and Apparant power (S) at optimised operating condition.

```
      PARAMETER (MTS=1)
      PARAMETER (NMAX= 24, NHMAX= 37, NDOT= 2000, VM=80)
      PARAMETER (NELEMI= 2, NELEM= 4, SIZIN= 10.E-3, SIZCAP= 100.E-6)
      PARAMETER (IN1= 10, IN2= 20, IN3= 30, OUT= 40, KM= 100)
      INTEGER        COUNTER, SE, SG
      real       CUL (NDOT), CERR (NDOT)
```

```
real        T (NDOT), TINO (NMAX), TIN (NMAX/2), TK (NMAX), TC (NMAX)
real        X (NELEM), XO (NELEM), XK (NELEM), XC (NELEM)
real)       C (NMAX), CO (NMAX), COFF (NMAX)
real        CX (NELEM), CXO (NELEM), COFFX (NELEM),
real        DA (0: KM, NMAX/2DAX (0: KM, NELEM),
EXTERNAL    FUNC, DERRO, FUNCERR
INTRINSIC   COS, SIN, ATAN
PARAMETER (PER= 20.0E-03, HPER= 10.0E-03)
PI= 4.0*ATAN (1.0)
OPEN (IN1, FILE ='load')
OPEN (IN2, FILE ='instants')
OPEN (IN3, FILE ='elements')
OPEN (OUT, FILE ='results')
TIME= 0.0
DO 1 JJ= 1, NDOT/2
READ (10, *) CUL (JJ)
IF (JJ.GT.NTRIGER) THEN
T (JJ)= TIME+DELTIME
TIME= T (JJ)
DELTIME= PER/NDOT
 CUL (JJ+NDOT/2)= -CUL (JJ)
T (JJ+NDOT/2)= T (JJ)+HPER
ENDIF
1 CONTINUE
   DELTAT= T (2)-T (1)
   READ (30, *) (XO (I), I= 1, NELEM)
   READ (20, *) (TINO (I), I= 1, NMAX/2)
```

```
      DO 2 I= 1, NMAX/2
      TINO (I)= (2*I-1)*PER/ (2*NMAX)
      TIN (I)= TINO (I)
2     CONTINUE
      DO 21 I= 1, NELEM
      X (I)= XO (I)
21    CONTINUE
      WRITE (40, *),'"The Initial Values of Switching Instants"'
      WRITE (40, 19) (TIN (I), I= 1, NMAX/2)
      WRITE (40, *),'"The Initial Values of Circuit Elements"'
      WRITE (40, 19) (X (I), I= 1, NELEM)
      NW= 0
      COUNTER= 1
      NH= NHMAX
4     CALL FUNC (VM,CUL, CERR, T, TIN, X, NDOT, NMAX, NELEM, PER)
      CALL FUNCERR (MTS,NW, CUL, CERR, NH, NDOT, AJT)
      AJ0= AJT
      AJK= AJ0
      IF (COUNTER.EQ.1) THEN
      AJC= AJK
      END IF
      K= 0
3     DO 44 J= 1, NMAX/2
      CO (J)= 0.0
44    CONTINUE
      DO 45 J= 1, NELEM
      CXO (J)= 0.0
```

```
45  CONTINUE
19  FORMAT (1F20.12)
    DTIN= T (2)-T (1)
    DX= 1.0E-3
    CALL DERRO (MTS, NW, NELEMI, COFF, COFFX, NII, CUL, TIN, X, PER, DTIN, DX, DA
   +          , DAX, K, KM, T, NMAX, NELEM, NDOT,VM)
    DO 50 J= 1, NMAX/2
    SG= 0
    SE= 0
37  C (J)= CO (J)+COFF (J)
40  TIN (J)= TINO (J)+C (J)*DA (K, J)
    TIN (J+NMAX/2)= TIN (J)+HPER
    IF ( (TIN (J).LE.(J-1)*PER/NMAX).OR.(TIN (J).GT.(J)*PER/NMAX).
   + OR.(TIN (J).LE.DELTAT).OR.(TIN (J).GE.HPER-DELTAT)) THEN
    C (J)= 0.9*C (J)
    GO TO 40
    END IF
    CALL FUNC (VM,CUL, CERR, T, TIN, X, NDOT, NMAX, NELEM, PER)
    CALL FUNCERR (MTS,NW, CUL, CERR, NH, NDOT, AJT)
     IF (AJT.LT.AJ0) THEN
    AJ0= AJT
    TINO (J)= TIN (J)
    TINO (J+NMAX/2)= TINO (J)+HPER
    CO (J)= C (J)
    GO TO  37
     ELSE IF (AJT.GT.AJ0) THEN
    COFF (J)= -COFF (J)
```

```
      CO (J)= CO (J)+COFF (J)
      TIN (J)= TINO (J)
      TIN (J+NMAX/2)= TIN (J)+HPER
      SG= SG+1
      IF (SG.LT.2) GO TO 37
      ELSE
        CO (J)= C (J)
        TIN (J)= TINO (J)
        TIN (J+NMAX/2)= TIN (J)+HPER
        SE= SE+1
        IF (SE.LT.5) GO TO 37
        END IF
        WRITE (6, *), "AJT, AJC, AJK, AJ0, K, J, SG, SE"
        WRITE (6, 69), AJT, AJC, AJK, AJ0, K, J, SG, SE
69    FORMAT (1X, 4F12.6, 4I4)
50    CONTINUE
      DO 51 J= 1, NELEM
      SG= 0
      SE= 0
38    CX (J)= CXO (J)+COFFX (J)
      X (J)= XO (J)+CX (J)*DAX (K, J)
      IF (J.LE.NELEMI.AND.X (J).GT.SIZIN.OR.J.GT.NELEMI.AND.
     +    X (J).GT.SIZCA) THEN
      X (J)= XO (J)
      END IF
      CALL FUNC (VM,CUL, CERR, T, TIN, X, NDOT, NMAX, NELEM, PER)
      CALL FUNCERR (MTS,NW, CUL, CERR, NH, NDOT, AJT)
```

```
      IF (AJT.LT.AJ0) THEN
      AJ0= AJT
      XO (J)= X (J)
      CXO (J)= CX (J)
      GO TO 38
      ELSE IF (AJT.GT.AJ0) THEN
      COFFX (J)= -COFFX (J)
      CXO (J)= CXO (J)+COFFX (J)
      X (J)= XO (J)
      SG= SG+1
      IF (SG.LT.2) GO TO 38
      ELSE
      CXO (J)= CX (J)
      X (J)= XO (J)
      SE= SE+1
      IF (SE.LT.5) GO TO 38
      END IF
      WRITE (6, *), "AJT, AJC, AJK, AJ0, K, J, SG, SE"
      WRITE (6, 69), AJT, AJC, AJK, AJ0, K, J, SG, SE
   51 CONTINUE
      IF (AJ0.LT.AJK) THEN
      K= K+1
      AJK= AJ0
      DO 23 I= 1, NMAX
      TK (I)= TIN (I)
   23 CONTINUE
      DO 24 J= 1, NELEM
```

```
      XK (J)= X (J)
24    CONTINUE
      GO TO 3
      ELSE
      IF (K.EQ.0.) THEN
      K= K+1
      AJ0= AJK
      GO TO 3
      END IF
      WRITE (40, *)'*************************'
      WRITE (40, *)'AJK, NH, COUNTER'
      WRITE (40, 32), AJK, NH, COUNTER
32    FORMAT (1F12.8, 2X, I3, I3)
      IF (NH.LT.NHMAX) THEN
      NH= NH+2
      GO TO 48
      END IF
      END IF
      IF (AJK.LT.AJC) THEN
      COUNTER= COUNTER+1
      AJC= AJK
      DO 33 I= 1, NMAX
      TC (I)= TK (I)
33    CONTINUE
      DO 34 J= 1, NELEM
      XC (J)= XK (J)
34    CONTINUE
```

```
NII= 3
GO TO 48
ELSE
NW= 1
CALL FUNCERR (MTS,NW, CUL, CERR, NII, NDOT, AJT)
AJmin= AJC
    WRITE (40,'("AJmin, NHMAX, COUNTER")')
    WRITE (40, 32), AJmin, NHMAX, COUNTER
     WRITE (40,'("The Final Optimised Switching IInstants")')
    WRITE (40, 12) (TC (I), I= 1, NMAX)
    WRITE (40,'("The Final Optimised Circuit Elements")')
    WRITE (40, 12) (XC (I), I= 1, NELEM)
    END IF
12  FORMAT (1F12.8)
    CLOSE (10)
    CLOSE (20)
    CLOSE (30)
    CLOSE (40)
    STOP
    END
```

C.2 Subroutine 'FUNCERR' For Evaluation of Cost Function and the Related Parameters to the Performance of Active Filter

```
SUBROUTINE FUNCERR (MTS,NW, X, Y, NII, NDO, AJT)
rcal    X (NDO), Y (NDO), NDAMPy, NDAMPx
INTRINSIC  SIN, COS, ATAN, SQRT
PI= 4.0*ATAN (1.0)
```

```
      WP= NDO
      SIGMAOy= 0.0
      DO 2 N= 1, NH, 2
      SUMUy= 0.0
      SUMVy= 0.0
      DO 1 I= 1, NDO
      SUMUy= SUMUy+Y (I)*SIN (I*2.0*PI*N/WP)
      SUMVy= SUMVy+Y (I)*COS (I*2.0*PI*N/WP)
1     CONTINUE
      Uy= 2.0*SUMUy/WP
      Vy= 2.0*SUMVy/WP
      AMPy= SQRT ( (Uy**2+Vy**2)/2.)
      IF (Uy.LT.0.0) THEN
      PHy = ATAN (Vy/Uy)+PI
      ELSE
      PHy= ATAN (Vy/Uy)
      END IF
      IF (N.EQ.1) THEN
      AMP1y= AMPy
      PH1y= PHy
      END IF
      SIGMAy= SIGMAOy+AMPy**2.
      SIGMAOy= SIGMAy
      DAMPy= AMPy*SQRT (2.)
      NDAMPy= AMPy/AMP1y
      IF (NW.EQ.1) THEN
      WRITE (40, *), " Harmonics No., Amplitude, Phase after filtering"
```

```
      WRITE (40, 25), N, DAMPy, PHy
      END IF
25    FORMAT (3X, 2F12.6, I6)
2     CONTINUE
      SIGMAOx= 0.0
      DO 4 N= 1, NH, 2
      SUMUx= 0.0
      SUMVx= 0.0
      DO 3 I= 1, NDO
      SUMUx= SUMUx+X (I)*SIN (I*2.0*PI*N/WP)
      SUMVx= SUMVx+X (I)*COS (I*2.0*PI*N/WP)
3     CONTINUE
      Ux= 2.0*SUMUx/WP
      Vx= 2.0*SUMVx/WP
      AMPx= SQRT ( (Ux**2+Vx**2)/2.)
      IF (Ux.LT.0.0) THEN
      PHx = ATAN (Vx/Ux)+PI
      ELSE
      PHx= ATAN (Vx/Ux)
      END IF
      IF (N.EQ.1) THEN
      AMP1x= AMPx
      PH1x= PHx
      END IF
      SIGMAx= SIGMAOx+AMPx**2.
      SIGMAOx= SIGMAx
      DAMPx= AMPx*SQRT (2.)
```

```
      NDAMPx= AMPx/AMP1x
      IF (NW.EQ.1) THEN
      WRITE (40, *), " Harmonic No., Amplitude, Phase before filtering"
      WRITE (40, 25), N, DAMPx, PHx
      END IF
4     CONTINUE
      THDy= SQRT (SIGMAy-AMP1y**2.)/AMP1y
      THDx= SQRT (SIGMAx-AMP1x**2.)/AMP1x
      IF (NW.EQ.1) THEN
      WRITE (40, *), "Total Harmonic Distortion values after and before filtering"
      WRITE (40, 26), THDy, THDx
      END IF
26    FORMAT (3X, 2F12.6)
      DPFy= COS (PH1y)
      DPFx= COS (PH1x)
      PFy= DPFy/SQRT (1+THDy**2.)
      PFx= DPFx/SQRT (1+THDx**2.)
      EFF=  (AMP1x*DPFx)/ (AMP1y*DPFy)
      IF (MTS.EQ.1) THEN
      AJT= THDy
      ELSE
      AJT= SQRT (SIGMAy/2.)
      END IF
      IF (NW.EQ.1) THEN
      WRITE (40, *), "Power Factor values after and before filtering, Efficiency, Cost Function"
      WRITE (40, 27), PFy, PFx, EFF, AJT
      END IF
```

```
27   FORMAT (3X, 4F12.6)
     END
```

C.3 Subroutine DERRO for Evaluation of Gradient of Cost Function (respect to the switching instants and circuit parameters) and the Direction of Steepest Descent

```
     SUBROUTINE DERRO (MTS,NW, NELEMI, COFF, COFFX, NII, CUL, TIN, X, PER, DTIN,
+                                   DX, DA, DAX, K, KM, T, NMA, NELEM, NDOT,VM)
  PARAMETER (NM= 100, NDO= 2000, KN= 100, NELE= 10)
  real      DJ (0: KN, NM/2), DDJ (KN), DA (0: KM, NMA/2), CUS (NDOT)
  real      TIND (NM), DJT (0: KN, NM/2), CERRX (NDO), CERRXX (NDO)
  real      T (NDOT), DDTJ (KN), COFF (NMA), COFFX (NELEM)
  real      PER, DTIN, TIN (NMA), X (NELEM), XD (NELE), DAX (0: KM, NELEM)
  real      DJX (0: KN, NELE), DJTX (0: KN, NELE)
  INTRINSIC  ABS, EXP
  EXTERNAL   FUNC, FUNCERR
  CALL FUNC (VM,CUL, CERRX, T, TIN, X, NDOT, NMA, NELEM, PER)
  CALL FUNCERR (MTS,NW, CUL, CERRX, NH, NDOT, AJTX)
  DO 7 I= 1, NMA/2
  DO 5 J= 1, NMA/2
  IF (J.EQ.I) THEN
  TIND (J)= TIN (J)+DTIN
  ELSE
  TIND (J)= TIN (J)
     END IF
5    CONTINUE
     CALL FUNC (VM,CUL, CERRXX, T, TIND, X, NDOT, NMA, NELEM, PER)
     CALL FUNCERR (MTS,NW, CUL, CERRXX, NH, NDOT, AJTXX)
```

```
      DJT (K, I)= AJTXX-AJTX
      DJ (k, I)= DJT (K, I)/DTIN
7     CONTINUE
      DO 17 I= 1, NELEM
      IF (I.GT.NELEMI) THEN
      DX= DX*1.E-3
      END IF
      DO 15 J= 1, NELEM
      IF (J.EQ.I) THEN
      XD (J)= X (J)+DX
      ELSE
      XD (J)= X (J)
      END IF
15    CONTINUE
      CALL FUNC (VM,CUL, CERRXX, T, TIN, XD, NDOT, NMA, NELEM, PER)
      CALL FUNCERR (MTS,NW, CUL, CERRXX, NII, NDOT, AJTXX)
      DJTX (K, I)= AJTXX-AJTX
      DJX (K, I)= DJTX (K, I)/DX
17    CONTINUE
      J= 1
      DO 9 I= 1, NMA/2
      DDJ (K)= FJ0+2.*DJ (K, I)**2.0+DJX (K, J)**2.0
      DDTJ (K)= FTJ0+4.* (DJ (K, I)-DJ (K-1, I))*DJ (K, I)+
     +          (DJX (K, J)-DJX (K-1, J))*DJX (K, J)
      FJ0= DDJ (K)
      FTJ0= DDTJ (K)
      IF (J.LT.NELEM) THEN
```

```
      J= J+1
      END IF
9     CONTINUE
      FJ0= 0.0
      FTJ0= 0.0
      J= 1
      DO 10 I= 1, NMA/2
      IF (K.EQ.0) THEN
      DA (K, I)= -DJ (K, I)
      DAX (K, J)= -DJX (K, J)
      ELSE
      KNI= DDJ (K)/DDJ (K-1)
      KNTI= DDTJ (K)/DDJ (K-1)
      DA (K, I)= -DJ (K, I)+KNTI*DA (K-1, I)
      DAX (K, J)= -DJX (K, J)+KNTI*DAX (K-1, J)
      END IF
50    IF (ABS (DA (K, I)).GT.1.E18) THEN
      DA (K, I)= 0.99*DA (K, I)
      GO TO 50
      END IF
51    IF (ABS (DAX (K, J)).GT.1.E18) THEN
      DAX (K, J)= 0.99*DAX (K, J)
      GO TO 51
      END IF
      S= 0.0
60    COFF (I)= 0.2*10.** (-S)
      IF (COFF (I)*ABS (DA (K, I)).GT.10.0**-4) THEN
```

```
      S= S+1.0
      GO TO 60
      END IF
      S= 0.0
61  COFFX (J)= 0.2*10.** (-S)
      IF (J.LE.NELEMI.AND.COFFX (J)*ABS (DAX (K, J)).GT.10.0**-4) THEN
      S= S+1.0
      GO TO 61
      END IF
      S= 0.0
62  COFFX (J)= 0.2*10.** (-S)
      IF (J.GT.NELEMI.AND.COFFX (J)*ABS (DAX (K, J)).GT.10.0**-6) THEN
      S= S+1.0
      GO TO 62
      END IF
      IF (J.LT.NELEM) THEN
      J= J+1
      END IF
10  CONTINUE
      END
```

C.4 Subroutine 'FUNC' for Analysis of the Proposed Active Filter circuits

C.4.1 Scheme No.4 of section 2.5.1

```
SUBROUTINE FUNC (VM, CUS, CERR, T, TIN, X, ND, NMAX, NELEM, PER )
PARAMETER (NDO=2000, NM=100 )
real CUF (NDO ), TIN (8*NMAX ), T (ND ), TIME, CERR (NDO )
real   TI (8*NM ), CUS (NDO ), X (NELEM )
```

```
PARAMETER (RL=2 )
 INTEGER  SP
EXTERNAL RUNG, FUNCHAR
INTRINSIC  SIN, ATAN, COS
DO 2 NN=0, 8*NMAX, NMAX/ 2
DO 2 I=1, NMAX/ 2
    TIN (I+NMAX/ 2 )=PER/ 2+TIN (I )
    TI (I+NN )=TIN (I )+PER*NN/ NMAX
2  CONTINUE
    DELTAT=T (2 )-T (1 )
    CUR=0.0
    Vc1=0.0
    Vc2=0.0
    TIME=0.0
    J=1
DO 4 JJ=1, 8*ND
IF (TIME.LE.TI (J ))THEN
SP=1
CALL RUNG (DELTAT, CUR, Vc, VM, X (1 ), RL, X (2 ), TIME, SP )
ELSE IF ( (TIME.GT.TI (J )).AND. (TIME.LE.TI (J+1 )))THEN
SP=0
CALL RUNG (DELTAT, CUR, Vc, VM, X (1 ), RL, X (2 ), TIME, SP )
ELSE
J=J+2
END IF
IF (JJ.GT.6*ND.AND.JJ.LE.7*ND )THEN
CUF (JJ-6*ND )=CUR
```

```
      CERR (JJ-6*ND )=CUS (JJ-6*ND )+CUF (JJ-6*ND )
      END IF
      TIME=TIME+DELTAT
4     CONTINUE
      END

      SUBROUTINE RUNG (DELTAT, CUR, Vc, VM, L, R, C, TIME, SP )
      INTRINSIC  SIN, ATAN, EXP
      real       W, L, R, C
      INTEGER    SP
      PI=4.*ATAN (1. )
      W=2.*PI*50.
      IF (SP.EQ.1 )THEN
      SI1= (VM*SIN (W*TIME )-RL*CUR )/ L
      SI2= (VM*SIN (W* (TIME+DELTAT/ 2. ))-RL* (CUR+SI1*DELTAT/ 2. ))/ L
      SI3= (VM*SIN (W* (TIME+DELTAT/ 2. ))-RL* (CUR+SI2*DELTAT/ 2. ))/ L
      SI4= (VM*SIN (W* (TIME+DELTAT ))-RL* (CUR+SI3*DELTAT ))/ L
      CUR=CUR+ (SI1+2.*SI2+2.*SI3+SI4 )/ 6.*DELTAT
      Vc=Vc
      ELSE
      SI1= (VM*SIN (W*TIME )-RL*CUR-Vc )/ L
      SK1=CUR/ C
      SI2= (VM*SIN (W* (TIME+DELTAT/ 2. ))-RL* (CUR+SI1*DELTAT/ 2. )
     +      -(Vc+SK1*DELTAT/ 2. ))/ L
      SK2= (CUR+SI1*DELTAT/ 2. )/ C
      SI3= (VM*SIN (W* (TIME+DELTAT/ 2. ))-RL* (CUR+SI2*DELTAT/ 2. )
     +      -(Vc+SK2*DELTAT/ 2. ))/ L
```

```
      SK3= (CUR+SI2*DELTAT/ 2. )/ C
      SI4= (VM*SIN (W* (TIME+DELTAT ))-RL* (CUR+SI3*DELTAT )
     +       - (Vc+SK3*DELTAT ))/ L
      SK4= (CUR+SI3*DELTAT )/ C
      CUR=CUR+ (SI1+2.*SI2+2.*SI3+SI4 )/ 6.*DELTAT
      Vc=Vc+ (SK1+2.*SK2+2.*SK3+SK4 )/ 6.*DELTAT
      END IF
      END
```

C.4.2 Scheme No.5 of section 2.5.1

```
      SUBROUTINE FUNC (VM, CUS, CERR, T, TIN, X, ND, NMAX, NELEM, PER )
      PARAMETER (NDO=2000, NM=100 )
      real CUF (NDO ), TIN (8*NMAX ), T (ND ), TIME, CERR (NDO )
      real  TI (8*NM ), CUS (NDO ), X (NELEM )
      PARAMETER ( RL=1.4 )
      INTEGER  SP
      EXTERNAL RUNG
      INTRINSIC  SIN, ATAN, COS
      DO 2 NN=0, 8*NMAX, NMAX/ 2
      DO 2 I=1, NMAX/ 2
      TIN (I+NMAX/ 2 )=PER/ 2+TIN (I )
      TI (I+NN )=TIN (I )+PER*NN/ NMAX
2  CONTINUE
      DELTAT=T (2 )-T (1 )
      CUR=0.0
      Vc=0.0
      TIME=0.0
```

```
      J=1
      DO 4 JJ=1, 8*ND
      IF (TIME.LE.TI (J ))THEN
      SP=1
      CALL RUNG (DELTAT, Vc, CUR, VM, X, NELEM, RL, TIME, SP )
      ELSE IF ( (TIME.GT.TI (J )).AND. (TIME.LE.TI (J+1 )))THEN
      SP=0
      CALL  RUNG (DELTAT, Vc, CUR, VM, X, NELEM, RL, TIME, SP )
      ELSE
      J=J+2
      END IF
      IF (JJ.GT.6*ND.AND.JJ.LE.7*ND )THEN
      CUF (JJ-6*ND )=CUR
      CERR (JJ-6*ND )=CUS (JJ-6*ND )+CUF (JJ-6*ND )
      END IF
      TIME=TIME+DELTAT
4     CONTINUE
      END

      SUBROUTINE  RUNG (DELTAT, Vc, CUR, VM, X, NELEM, RL, TIME, SP )
      INTEGER    SP
      INTRINSIC  SIN, ATAN
      real       L, C, X (NELEM )
      PI=4.*ATAN (1. )
      W=2.*PI*50.
      L=X (1 )
      C=X (2 )
```

```
      IF (SP.EQ.1 )THEN
      SI1= (VM*SIN (W*TIME )-RL*CUR-Vc )/ L
      SK1=CUR/ C
      SI2= (VM*SIN (W* (TIME+DELTAT/ 2. ))-RL* (CUR+SI1*DELTAT/ 2. )
     +     - (Vc+SK1*DELTAT/ 2. ))/ L
      SK2= (CUR+SI1*DELTAT/ 2. )/ C
      SI3= (VM*SIN (W* (TIME+DELTAT/ 2. ))-RL* (CUR+SI2*DELTAT/ 2. )
     +     - (Vc+SK2*DELTAT/ 2. ))/ L
      SK3= (CUR+SI2*DELTAT/ 2. )/ C
      SI4= (VM*SIN (W* (TIME+DELTAT ))-RL* (CUR+SI3*DELTAT )
     +     - (Vc+SK3*DELTAT ))/ L
      SK4= (CUR+SI3*DELTAT )/ C
      CUR=CUR+ (SI1+2.*SI2+2.*SI3+SI4 )/ 6.*DELTAT
      Vc=Vc+ (SK1+2.*SK2+2.*SK3+SK4 )/ 6.*DELTAT
      ELSE
      SI1= (VM*SIN (W*TIME )-RL*CUR+Vc )/ L
      SK1=-CUR/ C
      SI2= (VM*SIN (W* (TIME+DELTAT/ 2. ))-RL* (CUR+SI1*DELTAT/ 2. )
     +     + (Vc+SK1*DELTAT/ 2. ))/ L
      SK2=- (CUR+SI1*DELTAT/ 2. )/ C
      SI3= (VM*SIN (W* (TIME+DELTAT/ 2. ))-RL* (CUR+SI2*DELTAT/ 2. )
     +     + (Vc+SK2*DELTAT/ 2. ))/ L
      SK3=- (CUR+SI2*DELTAT/ 2. )/ C
      SI4= (VM*SIN (W* (TIME+DELTAT ))-RL* (CUR+SI3*DELTAT )
     +     + (Vc+SK3*DELTAT ))/ L
      SK4=- (CUR+SI3*DELTAT )/ C
      CUR=CUR+ (SI1+2.*SI2+2.*SI3+SI4 )/ 6.*DELTAT
```

```
      Vc=Vc+ (SK1+2.*SK2+2.*SK3+SK4 )/ 6.*DELTAT
      END IF
      END
```

C.4.3 Scheme No.6 section 2.5.1

```
      SUBROUTINE FUNC (VM, CUS, CERR, T, TIN, X, ND, NMAX, NELEM, PER )
      PARAMETER (NDO=2000, NM=100 )
      real CUF (NDO ), TIN (8*NMAX ), T (ND ), TIME, CERR (NDO )
      real   TI (8*NM ), CUS (NDO ), X (NELEM )
      PARAMETER (RL=2.4, RLa=1.4 )
       INTEGER  SP
      EXTERNAL RUNG, FUNCHAR
      INTRINSIC   SIN, ATAN, COS
      DO 2 NN=0, 8*NMAX, NMAX/ 2
      DO 2 I=1, NMAX/ 2
      TIN (I+NMAX/ 2 )=PER/ 2+TIN (I )
      TI (I+NN )=TIN (I )+PER*NN/ NMAX
    2 CONTINUE
      DELTAT=T (2 )-T (1 )
      CUR1=0.0
      CUR2=0.0
      Vc1=0.0
      Vc2=0.0
      TIME=0.0
      J=1
      DO 4 JJ=1, 8*ND
      IF (TIME.LE.TI (J ))THEN
```

```
      SP=1
      CALL RUNG (DELTAT, Vc1, Vc2, CUR1, CUR2, VM, X (1 ), RL, X (2 ), RLa,
     +                  X (3 ), X (4 ), TIME )
      CUR=CUR1
      ELSE IF ( (TIME.GT.TI (J )).AND. (TIME.LE.TI (J+1 )))THEN
      SP=0
      CALL RUNG (DELTAT, Vc2, Vc1, CUR1, CUR2, VM, X (1 ), RL, X (2 ), RLa,
     +                  X (4 ), X (3 ), TIME )
      CUR=CUR1
      ELSE
      J=J+2
      END IF
      IF (JJ.GT.6*ND.AND.JJ.LE.7*ND )THEN
      CUF (JJ-6*ND )=CUR
      CERR (JJ-6*ND )=CUS (JJ-6*ND )+CUF (JJ-6*ND )
      END IF
      TIME=TIME+DELTAT
4     CONTINUE
      END

      SUBROUTINE RUNG (DELTAT, Vca, Vcb, CUR1, CUR2, VM, L, RL, La, RLa,
     +                  C1, C2, TIME )
      INTRINSIC  SIN, ATAN, EXP
      real       W, L, La, C1, C2
      PI=4.*ATAN (1. )
      W=2.*PI*50.
      SI1= (VM*SIN (W*TIME )-Vca-RL*CUR1 )/L
```

```
SK1=CUR1/C1
SI2= (VM*SIN (W* (TIME+DELTAT/2. ))- (Vca+SK1*DELTAT/2. )-
+       RL* (CUR1+SI1*DELTAT/2. ))/L
SK2= (CUR1+SI1*DELTAT/2. )/C1
SI3= (VM*SIN (W* (TIME+DELTAT/2. ))- (Vca+SK2*DELTAT/2. )-
+       RL* (CUR1+SI2*DELTAT/2. ))/L
SK3= (CUR1+SI2*DELTAT/2. )/C1
SI4= (VM*SIN (W* (TIME+DELTAT ))- (Vca+SK3*DELTAT )-
+       RL* (CUR1+SI3*DELTAT ))/L
SK4= (CUR1+SI3*DELTAT )/C1
CUR1=CUR1+ (SI1+2.*SI2+2.*SI3+SI4 )/6.*DELTAT
Vca=Vca+ (SK1+2.*SK2+2.*SK3+SK4 )/6.*DELTAT
SII1= (-Vcb-RLa*CUR2 )/La
SKK1=CUR2/C2
SII2= (- (Vcb+SKK1*DELTAT/2. )-RLa* (CUR2+SII1*DELTAT/2. ))/La
SKK2= (CUR2+SII1*DELTAT/2. )/C2
SII3= (- (Vcb+SKK2*DELTAT/2. )-RLa* (CUR2+SII2*DELTAT/2. ))/La
SKK3= (CUR2+SII2*DELTAT/2. )/C2
SII4= (- (Vcb+SKK3*DELTAT )-RLa* (CUR2+SII3*DELTAT ))/La
SKK4= (CUR2+SII3*DELTAT )/C2
CUR2=CUR2+ (SII1+2.*SII2+2.*SII3+SII4 )/6.*DELTAT
Vcb=Vcb+ (SKK1+2.*SKK2+2.*SKK3+SKK4 )/6.*DELTAT
END
```

D.4.4 Scheme No.7 of section 2.5.1

```
SUBROUTINE FUNC (VM, CUS, CERR, T, TIN, X, ND, NMAX, NELEM, PER )
PARAMETER (NDO=2000, NM=100 )
```

```
      real CUF (NDO ), TIN (8*NMAX ), T (ND ), TIME, CERR (NDO )
      real  TI (8*NM ), CUS (NDO ), X (NELEM )
      PARAMETER (RL=2.4, RLa=1.4 )
      INTEGER  SP
      EXTERNAL RUNG, FUNCHAR
      INTRINSIC  SIN, ATAN, COS
      DO 2 NN=0, 8*NMAX, NMAX/ 2
      DO 2 I=1, NMAX/ 2
      TIN (I+NMAX/ 2 )=PER/ 2+TIN (I )
      TI (I+NN )=TIN (I )+PER*NN/ NMAX
2     CONTINUE
      DELTAT=T (2 )-T (1 )
      CUR=0.0
      CURL=0.0
      Vc1=0.0
      Vc2=0.0
      TIME=0.0
      J=1
      DO 4 JJ=1, 8*ND
      IF (TIME.LE.TI (J ))THEN
      SP=1
      CALL RUNG (DELTAT, Vc1, Vc2, CUR, CURL, VM, X (1 ), RL, X (2 ), RLa,
     +                X (3 ), X (4 ), TIME, SP )
      ELSE IF ( (TIME.GT.TI (J )).AND. (TIME.LE.TI (J+1 )))THEN
      SP=0
      CALL RUNG (DELTAT, Vc1, Vc2, CUR, CURL, VM, X (1 ), RL, X (2 ), RLa,
     +                X (3 ), X (4 ), TIME, SP )
```

```
      ELSE
      J=J+2
      END IF
      IF (JJ.GT.6*ND.AND.JJ.LE.7*ND )THEN
      CUF (JJ-6*ND )=CUR
      CERR (JJ-6*ND )=CUS (JJ-6*ND )+CUF (JJ-6*ND )
      END IF
      TIME=TIME+DELTAT
4     CONTINUE
      END

      SUBROUTINE RUNG (DELTAT, Vca, Vcb, CUR, CURL, VM, L, RL, La, RLa,
     +                 C1, C2, TIME, SP )
      INTRINSIC  SIN, ATAN, EXP
      real       W, L, La, C1, C2
      INTEGER    SP
      PI=4.*ATAN (1. )
      W=2.*PI*50.
      IF (SP.EQ.0 )THEN
      SI1= (VM*SIN (W*TIME )-Vca-RL*CUR )/ L
      SK1= (CUR-CURL )/ C1
      SKK1=CURL/ C2
      SII1= (Vca-Vcb-RLa*CURL )/ La
      SI2= (VM*SIN (W* (TIME+DELTAT/ 2. ))- (Vca+SK1*DELTAT/ 2. )-
     +      RL* (CUR+SI1*DELTAT/ 2. ))/ L
      SK2= (CUR+SI1*DELTAT/ 2.- (CURL+SII1*DELTAT/ 2. ))/ C1
      SKK2= (CURL+SII1*DELTAT/ 2. )/ C2
```

```
 SII2= (Vca+SK1*DELTAT/2.- (Vcb+SKK1*DELTAT/2. )-
+      RLa* (CURL+SII1*DELTAT/2. ))/ La
 SI3= (VM*SIN (W* (TIME+DELTAT/2. ))- (Vca+SK2*DELTAT/2. )-
+      RL* (CUR+SI2*DELTAT/2. ))/ L
 SK3= (CUR+SI2*DELTAT/2.- (CURL+SII2*DELTAT/2. ))/ C1
 SKK3= (CURL+SII2*DELTAT/2. )/ C2
 SII3= (Vca+SK2*DELTAT/2.- (Vcb+SKK2*DELTAT/2. )-
+      RLa* (CURL+SII2*DELTAT/2. ))/ La
 SI4= (VM*SIN (W* (TIME+DELTAT )- (Vca+SK3*DELTAT )-
+      RL* (CUR+SI3*DELTAT ))/ L
 SK4= (CUR+SI3*DELTAT- (CURL+SII3*DELTAT ))/ C1
 SKK4= (CURL+SII3*DELTAT )/ C2
 SII4= (Vca+SK3*DELTAT- (Vcb+SKK3*DELTAT )-
+      RLa* (CURL+SII3*DELTAT ))/ La
 CUR=CUR+ (SI1+2.*SI2+2.*SI3+SI4 )/ 6.*DELTAT
 Vca=Vca+ (SK1+2.*SK2+2.*SK3+SK4 )/ 6.*DELTAT
 CURL=CURL+ (SII1+2.*SII2+2.*SII3+SII4 )/ 6.*DELTAT
 Vcb=Vcb+ (SKK1+2.*SKK2+2.*SKK3+SKK4 )/ 6.*DELTAT
 ELSE
 SI1= (VM*SIN (W*TIME )-Vca+Vcb-RL*CUR )/ L
 SK1= (CUR-CURL )/ C1
 SKK1=- (CUR-CURL )/ C2
 SII1= (Vca-Vcb-RLa*CURL )/ La
 SI2= (VM*SIN (W* (TIME+DELTAT/2. ))- (Vca+SK1*DELTAT/2. )
+       + (Vcb+SKK1*DELTAT/2. )-RL* (CUR+SI1*DELTAT/2. ))/ L
 SK2= (CUR+SI1*DELTAT/2.- (CURL+SII1*DELTAT/2. ))/ C1
 SKK2=- (CUR+SI1*DELTAT/2.- (CURL+SII1*DELTAT/2. ))/ C2
```

```
 SII2= (Vca+SK1*DELTAT/2.- (Vcb+SKK1*DELTAT/2. )-
+        RLa* (CURL+SII1*DELTAT/2. )/ La
 SI3= (VM*SIN (W* (TIME+DELTAT/2. ))- (Vca+SK2*DELTAT/2. )
+      + (Vcb+SKK2*DELTAT/2. )-RL* (CUR+SI2*DELTAT/2. )/ L
 SK3= (CUR+SI2*DELTAT/2.- (CURL+SII2*DELTAT/2. )/ C1
 SKK3=- (CUR+SI2*DELTAT/2.- (CURL+SII2*DELTAT/2. )/ C2
 SII3= (Vca+SK2*DELTAT/2.- (Vcb+SKK2*DELTAT/2. )-
+        RLa* (CURL+SII2*DELTAT/2. )/ La
 SI4= (VM*SIN (W* (TIME+DELTAT )- (Vca+SK3*DELTAT )
+      + (Vcb+SKK3*DELTAT )-RL* (CUR+SI3*DELTAT )/ L
 SK4= (CUR+SI3*DELTAT- (CURL+SII3*DELTAT )/ C1
 SKK4=- (CUR+SI3*DELTAT- (CURL+SII3*DELTAT )/ C2
 SII4= (Vca+SK3*DELTAT- (Vcb+SKK3*DELTAT )-
+        RLa* (CURL+SII3*DELTAT )/ La
 CUR=CUR+ (SI1+2.*SI2+2.*SI3+SI4 )/ 6.*DELTAT
     Vca=Vca+ (SK1+2.*SK2+2.*SK3+SK4 )/ 6.*DELTAT
     CURL=CURL+ (SII1+2.*SII2+2.*SII3+SII4 )/ 6.*DELTAT
     Vcb=Vcb+ (SKK1+2.*SKK2+2.*SKK3+SKK4 )/ 6.*DELTAT
     END IF
     END
```

C.4.5 Scheme No.8 of section 2.5.1

```
     SUBROUTINE FUNC (VM, CUS, CERR, T, TIN, X, ND, NMAX, NELEM, PER )
     PARAMETER (NDO=2000, NM=100 )
     real CUF (NDO ), TIN (8*NMAX ), T (ND ), TIME, CERR (NDO )
     real   TI (8*NM ), CUS (NDO ), X (NELEM )
     PARAMETER (RL=8.5, RLa1=2.4, RLa2=1.4 )
```

```
      INTEGER  SP
      EXTERNAL RUNG, FUNCHAR
      INTRINSIC  SIN, ATAN, COS
      DO 2 NN=0, 8*NMAX, NMAX/ 2
      DO 2 I=1, NMAX/ 2
      TIN (I+NMAX/ 2 )=PER/ 2+TIN (I )
      TI (I+NN )=TIN (I )+PER*NN/ NMAX
2     CONTINUE
      DELTAT=T (2 )-T (1 )
      CUR=0.0
      CURL=0.0
      Vc=0.0
      TIME=0.0
      J=1
      DO 4 JJ=1, 8*ND
      IF (TIME.LE.TI (J ))THEN
      SP=1
      CALL RUNG (DELTAT, Vc, CUR, CURL, VM, X (1 ), RL, X (2 ), RLa1,
     +                X (3 ), RLa2, X (4 ), TIME, SP )
      ELSE IF ( (TIME.GT.TI (J )).AND. (TIME.LE.TI (J+1 )))THEN
      SP=0
      CALL RUNG (DELTAT, Vc, CUR, CURL, VM, X (1 ), RL, X (2 ), RLa1,
     +                X (3 ), RLa2, X (4 ), TIME, SP )
      ELSE
      J=J+2
      END IF
      IF (JJ.GT.6*ND.AND.JJ.LE.7*ND )THEN
```

```
      CUF (JJ-6*ND )=CUR
      CERR (JJ-6*ND )=CUS (JJ-6*ND )+CUF (JJ-6*ND )
      END IF
      TIME=TIME+DELTAT
    4 CONTINUE
      END

      SUBROUTINE RUNG (DELTAT, Vc, CUR, CURL, VM, L, RL, La1, RLA1,
     +                 La2, RLA2, C, TIME, SP )
      INTRINSIC  SIN, ATAN, EXP
      real       W, L, La1, La2, C
      INTEGER    SP
      PI=4.*ATAN (1. )
      W=2.*PI*50.
      IF (SP.EQ.1 )THEN
      SI1= (VM*SIN (W*TIME )-La1*SII1-RLa1*CURL-RL*CUR )/ L
      SK1= (CUR-CURL )/ C
      SII1= (Vc+La2*SI1- (RLa1+RLa2 )*CURL+RLa2*CUR )/ (La1+La2 )
      SI2= (VM*SIN (W* (TIME+DELTAT/ 2. ))-La1*SII2-
     +      RLa1* (CURL+SII1*DELTAT/ 2. )-RL* (CUR+SI1*DELTAT/ 2. ))/ L
      SK2= (CUR+SI1*DELTAT/ 2.- (CURL+SII1*DELTAT/ 2. ))/ C
      SII2= (Vc+SK1*DELTAT/ 2.+La2*SI2-
     + (RLa1+RLa2 )* (CURL+SII1*DELTAT/ 2. )+RLa2* (CUR+SI1*DELTAT/ 2. ))/ (La1+La2 )
      SI3= (VM*SIN (W* (TIME+DELTAT/ 2. ))-La1*SII3-
     +      RLa1* (CURL+SII2*DELTAT/ 2. )-RL* (CUR+SI2*DELTAT/ 2. ))/ L
      SK3= (CUR+SI2*DELTAT/ 2.- (CURL+SII2*DELTAT/ 2. ))/ C
      SII3= (Vc+SK2*DELTAT/ 2.+La2*SI3-
```

```
+ (RLa1+RLa2)* (CURL+SII2*DELTAT/2.)+RLa2* (CUR+SI2*DELTAT/2.)/ (La1+La2)
 SI4= (VM*SIN (W* (TIME+DELTAT))-La1*SII4-
+      RLa1* (CURL+SII3*DELTAT)-RL* (CUR+SI3*DELTAT)/L
 SK4= (CUR+SI3*DELTAT- (CURL+SII3*DELTAT)/C
 SII4= (Vc+SK3*DELTAT+La2*SI4-
+      (RLa1+RLa2)* (CURL+SII3*DELTAT)+RLa2* (CUR+SI3*DELTAT)/(La1+La2)
CUR=CUR+ (SI1+2.*SI2+2.*SI3+SI4)/6.*DELTAT
Vc=Vc+ (SK1+2.*SK2+2.*SK3+SK4)/6.*DELTAT
CURL=CURL+ (SII1+2.*SII2+2.*SII3+SII4)/6.*DELTAT
ELSE
SI1= (VM*SIN (W*TIME)+La2*SII1+RLA2*CURL- (RLa2+RL)*CUR)/ (L+La2)
SK1= (-CURL)/C
SII1= (Vc+La2*SI1- (RLa1+RLa2)*CURL+RLa2*CUR)/(La1+La2)
SI2= (VM*SIN (W* (TIME+DELTAT/2.))+La2*SII2+
+      RLa2* (CURL+SII1*DELTAT/2.)- (RLa2+RL)* (CUR+SI1*DELTAT/2.)/(L+La2)
 SK2= (- (CURL+SII1*DELTAT/2.)/C
 SII2= (Vc+SK1*DELTAT/2.+La2*SI2-
+      (RLa1+RLa2)* (CURL+SII1*DELTAT/2.)+RLa2* (CUR+SI1*DELTAT/2.)/(La1+La2)
 SI3= (VM*SIN (W* (TIME+DELTAT/2.))+La2*SII3+
+ RLA2* (CURL+SII2*DELTAT/2.)- (RLa2+RL)* (CUR+SI2*DELTAT/2.)/(L+La2)
 SK3= (- (CURL+SII2*DELTAT/2.)/C
 SII3= (Vc+SK2*DELTAT/2.+La2*SI3-
+ (RLa1+RLa2)* (CURL+SII2*DELTAT/2.)+RLa2* (CUR+SI2*DELTAT/2.)/ (La1+La2)
 SI4= (VM*SIN (W* (TIME+DELTAT))+La2*SII4+
+ RLa2* (CURL+SII3*DELTAT)- (RLa2+RL)* (CUR+SI3*DELTAT)/ (L+La2)
 SK4= (- (CURL+SII3*DELTAT)/C
 SII4= (Vc+SK3*DELTAT+La2*SI4-
```

```
+ (RLA1+RLA2 )* (CURL+SII3*DELTAT )+RLA2* (CUR+SI3*DELTAT )/ (La1+La2 )
  CUR=CUR+ (SI1+2.*SI2+2.*SI3+SI4 )/ 6.*DELTAT
  Vc=Vc+ (SK1+2.*SK2+2.*SK3+SK4 )/ 6.*DELTAT
  CURL=CURL+ (SII1+2.*SII2+2.*SII3+SII4 )/ 6.*DELTAT
  END IF
  END
```

C.4.6 Scheme No.1 of section 2.5.2

```
      SUBROUTINE FUNC (VM, CUS, CERR, T, TIN, X, ND, NMAX, NELEM, PER )
      PARAMETER (NDO=2000, NM=100 )
      real CUF (NDO ), TIN (8*NMAX ), T (ND ), TIME, CERR (NDO )
      real  TI (8*NM ), CUS (NDO ), X (NELEM )
      PARAMETER (RL1=2, RL2=2 )
      INTEGER  SP
      EXTERNAL RUNG, FUNCHAR
      INTRINSIC  SIN, ATAN, COS
      DO 2 NN=0, 8*NMAX, NMAX/ 2
      DO 2 I=1, NMAX/ 2
      TIN (I+NMAX/ 2 )=PER/ 2+TIN (I )
      TI (I+NN )=TIN (I )+PER*NN/ NMAX
2     CONTINUE
      DELTAT=T (2 )-T (1 )
      CUR1=0.0
      CUR2=0.0
      TIME=0.0
      TIME1=0.0
      TIME2=0.0
```

```
CUbo=0.0
J=1
DO 4 JJ=1, 8*ND
IF (TIME.LE.TI (J ))THEN
SP=1
TIME2=TIME
CALL RUNG (DELTAT, CUR2, CUR1, VM, X (2 ), RL2, X (1 ), RL1,
+        TIME, TIME1, CUbo )
CUR=CUR2
IF (TIME.GT. (TI (J )-DELTAT ))THEN
CUbo=CUR2
END IF
ELSE IF ( (TIME.GT.TI (J )).AND. (TIME.LE.TI (J+1 )))THEN
SP=0
TIME1=TIME
CALL RUNG (DELTAT, CUR1, CUR2, VM, X (1 ), RL1, X (2 ), RL2,
+        TIME, TIME2, CUbo )
CUR=CUR1
IF (TIME.GT. (TI (J+1 )-DELTAT ))THEN
CUbo=CUR1
END IF
ELSE
J=J+2
END IF
IF (JJ.GT.6*ND.AND.JJ.LE.7*ND )THEN
CUF (JJ-6*ND )=CUR
```

```
      CERR (JJ-6*ND )=CUS (JJ-6*ND )+CUF (JJ-6*ND )
      END IF
      TIME=TIME+DELTAT
4     CONTINUE
      END
```

```
      SUBROUTINE RUNG (DELTAT, CURa, CURb, VM, La, RLa, Lb, RLb,
     +                 TIME, TIMEO, CUbo )
      INTRINSIC  SIN, ATAN, EXP
      real       W, La, Lb
      W=8.* ATAN (1)* 50.
      SI1=VM*SIN (W*TIME )/ La -RLa*CURa/ La
      SI2=VM*SIN (W* (TIME+DELTAT/ 2. )/ La-RLa* (CURa+SI1*DELTAT/ 2. )/ La
      SI3=VM*SIN (W* (TIME+DELTAT/ 2. )/ La-RLa* (CURa+SI2*DELTAT/ 2. )/ La
      SI4=VM*SIN (W* (TIME+DELTAT )/ La-RLa*CURa+ (SI3*DELTAT )/ La
      CURa=CURa+ (SI1+2.*SI2+2.*SI3+SI4 )/ 6.*DELTAT
      CURb=CUbo*EXP (-RLb* (TIME-TIMEO )/ Lb )
      END
```

C.4.7 Scheme No.2 of section 2.5.2

```
      SUBROUTINE FUNC (VM, CUS, CERR, T, TIN, X, ND, NMAX, NELEM, PER)
      PARAMETER (NDO=2000, NM=100)
      real CUF (NDO), TIN (8*NMAX), T (ND), TIME, CERR (NDO)
      real  TI (8*NM), CUS (NDO), X (NELEM)
      PARAMETER (RL1=1.4, RL2=1.4)
      INTEGER  SP
      EXTERNAL RUNG, FUNCHAR
```

```
      DO 2 NN=0, 8*NMAX, NMAX/2
      DO 2 I=1, NMAX/2
      TIN (I+NMAX/2)=PER/2+TIN (I)
      TI (I+NN)=TIN (I)+PER*NN/NMAX
2     CONTINUE
      DELTAT=T (2)-T (1)
      CUR1=0.0
      CUR2=0.0
      Vc=0.0
      TIME=0.0
      J=1
      DO 4 JJ=1, 8*ND
      IF (TIME.LE.TI (J))THEN
      SP=1
      CALL RUNG (DELTAT, Vc, CUR1, CUR2, VM, X (1), RL1, X (2), RL2, X (3), TIME)
      CUR=CUR1
      ELSE IF ( (TIME.GT.TI (J)).AND. (TIME.LE.TI (J+1)))THEN
      SP=0
      CALL RUNG (DELTAT, Vc, CUR2, CUR1, VM, X (2), RL2, X (1), RL1, X (3), TIME)
      CUR=CUR2
      ELSE
      J=J+2
      END IF
      IF (JJ.GT.6*ND.AND.JJ.LE.7*ND)THEN
      CUF (JJ-6*ND)=CUR
      CERR (JJ-6*ND)=CUS (JJ-6*ND)+CUF (JJ-6*ND)
      END IF
```

```
      TIME=TIME+DELTAT
4     CONTINUE
      END

      SUBROUTINE RUNG (DELTAT, Vc, CURa, CURb, VM, La, RLa, Lb, RLb, C, TIME)
      INTRINSIC  SIN, ATAN, EXP
      real       W, La, Lb, C
      W=8.* ATAN (1.)*50.
      SI1= (VM*SIN (W*TIME)-RLa*CURa)/ La
      SI2= (VM*SIN (W* (TIME+DELTAT/ 2.))-RLa* (CURa+SI1*DELTAT/ 2.))/ La
      SI3= (VM*SIN (W* (TIME+DELTAT/ 2.))-RLa* (CURa+SI2*DELTAT/ 2.))/ La
      SI4= (VM*SIN (W* (TIME+DELTAT))-RLa*CURa+ (SI3*DELTAT)/ La
      CURa=CURa+ (SI1+2.*SI2+2.*SI3+SI4)/ 6.*DELTAT
      SII1= (Vc-RLb*CURb)/ Lb
      SK1=-CURb/ C
      SII2= ( (Vc+SK1*DELTAT/ 2.)-RLb* (CURb+SII1*DELTAT/ 2.))/ Lb
      SK2=- (CURb+SII1*DELTAT/ 2.)/ C
      SII3= ( (Vc+SK2*DELTAT/ 2.)-RLb* (CURb+SII2*DELTAT/ 2.))/ Lb
      SK3=- (CURb+SII2*DELTAT/ 2.)/ C
      SII4= ( (Vc+SK3*DELTAT)-RLb* (CURb+SII3*DELTAT))/ Lb
      SK4=- (CURb+SII3*DELTAT)/ C
      CURb=CURb+ (SII1+2.*SII2+2.*SII3+SII4)/ 6.*DELTAT
      Vc=Vc+ (SK1+2.*SK2+2.*SK3+SK4)/ 6.*DELTAT
      END
```

C.4.8 Scheme No.3 of section 2.5.2

```
      SUBROUTINE FUNC (VM, CUS, CERR, T, TIN, X, ND, NMAX, NELEM, PER )
      PARAMETER (NDO=2000, NM=100 )
```

```
real CUF (NDO ), TIN (8*NMAX ), T (ND ), TIME, CERR (NDO )
real   TI (8*NM ), CUS (NDO ), X (NELEM )
PARAMETER (RLs=2, RL=2 )
INTEGER  SP
EXTERNAL RUNG
DO 2 NN=0, 8*NMAX, NMAX/ 2
    DO 2 I=1, NMAX/ 2
    TIN (I+NMAX/ 2 )=PER/ 2+TIN (I )
    TI (I+NN )=TIN (I )+PER*NN/ NMAX
2   CONTINUE
    DELTAT=T (2 )-T (1 )
    CUR=0.0
    CURL=0.0
    Vc=0.0
    TIME=0.0
    J=1
    DO 4 JJ=1, 8*ND
    IF (TIME.LE.TI (J ))THEN
    SP=1
    CALL RUNG (DELTAT, Vc, CUR, CURL, VM, X, NELEM, RLs, RL, TIME, SP )
    ELSE IF ( (TIME.GT.TI (J )).AND. (TIME.LE.TI (J+1 )))THEN
    SP=0
    CALL RUNG (DELTAT, Vc, CUR, CURL, VM, X, NELEM, RLs, RL, TIME, SP )
    ELSE
    J=J+2
    END IF
    IF (JJ.GT.6*ND.AND.JJ.LE.7*ND )THEN
```

```
      CUF (JJ-6*ND )=CUR
      CERR (JJ-6*ND )=CUS (JJ-6*ND )+CUF (JJ-6*ND )
      END IF
      TIME=TIME+DELTAT
4     CONTINUE
      END
```

```
      SUBROUTINE RUNG (DELTAT, Vc, CUR, CURL, VM, X, NELEM, RLs, RI, TIME, SP )
      INTEGER    SP
      INTRINSIC  SIN, ATAN
      real       Ls, C, X (NELEM ), L
      W=8.* ATAN (1. )*50.
      Ls=X (1 )
      L=X (2 )
      C=X (3 )
      IF (SP.EQ.1 )THEN
      SI1= (VM*SIN (W*TIME )-RLs*CUR-Vc )/ Ls
      SII1= (Vc-RI*CURL )/ L
      SK1= (CUR-CURL )/ C
      SI2= (VM*SIN (W* (TIME+DELTAT/ 2. ))-RLs* (CUR+SI1*DELTAT/ 2. )
     +       - (Vc+SK1*DELTAT/ 2. ))/ Ls
      SII2= (Vc+SK1*DELTAT/ 2.-RI* (CURL+SII1*DELTAT/ 2. ))/ L
      SK2= (CUR+SI1*DELTAT/ 2.-CURL-SII1*DELTAT/ 2. )/ C
      SI3= (VM*SIN (W* (TIME+DELTAT/ 2. ))-RLs* (CUR+SI2*DELTAT/ 2. )
     +       - (Vc+SK2*DELTAT/ 2. ))/ Ls
      SII3= (Vc+SK2*DELTAT/ 2.-RI* (CURL+SII2*DELTAT/ 2. ))/ L
      SK3= (CUR+SI2*DELTAT/ 2.-CURL-SII2*DELTAT/ 2. )/ C
```

```
      SI4= (VM*SIN (W* (TIME+DELTAT ))-RLs* (CUR+SI3*DELTAT )
     +       - (Vc+SK3*DELTAT ))/ Ls
      SII4= (Vc+SK3*DELTAT-RI* (CURL+SII3*DELTAT ))/ L
      SK4= (CUR+SI3*DELTAT-CURL-SII3*DELTAT )/ C
      CUR=CUR+ (SI1+2.*SI2+2.*SI3+SI4 )/ 6.*DELTAT
      CURL=CURL+ (SII1+2.*SII2+2.*SII3+SII4 )/ 6.*DELTAT
      Vc=Vc+ (SK1+2.*SK2+2.*SK3+SK4 )/ 6.*DELTAT
      ELSE
      SI1= (VM*SIN (W*TIME )-RLs*CUR-Vc )/ Ls
      SII1= (-Vc-RI*CURL )/ L
      SK1= (CUR+CURL )/ C
      SI2= (VM*SIN (W* (TIME+DELTAT/ 2. ))-RLs* (CUR+SI1*DELTAT/ 2. )
     +       - (Vc+SK1*DELTAT/ 2. ))/ Ls
      SII2= (- (Vc+SK1*DELTAT/ 2. )-RI* (CURL+SII1*DELTAT/ 2. ))/ L
      SK2= (CUR+SI1*DELTAT/ 2.+CURL+SII1*DELTAT/ 2. )/ C
      SI3= (VM*SIN (W* (TIME+DELTAT/ 2. ))-RLs* (CUR+SI2*DELTAT/ 2. )
     +       - (Vc+SK2*DELTAT/ 2. ))/ Ls
      SII3= (- (Vc+SK2*DELTAT/ 2. )-RI* (CURL+SII2*DELTAT/ 2. ))/ L
      SK3= (CUR+SI2*DELTAT/ 2.+CURL+SII2*DELTAT/ 2. )/ C
      SI4= (VM*SIN (W* (TIME+DELTAT )-RLs* (CUR+SI3*DELTAT )
     +       - (Vc+SK3*DELTAT ))/ Ls
      SII4= (- (Vc+SK3*DELTAT )-RI* (CURL+SII3*DELTAT ))/ L
      SK4= (CUR+SI3*DELTAT+CURL+SII3*DELTAT )/ C
      CUR=CUR+ (SI1+2.*SI2+2.*SI3+SI4 )/ 6.*DELTAT
      CURL=CURL+ (SII1+2.*SII2+2.*SII3+SII4 )/ 6.*DELTAT
      Vc=Vc+ (SK1+2.*SK2+2.*SK3+SK4 )/ 6.*DELTAT
      END IF
      END
```

PUBLISHED PAPERS

1. Paper published in Electronics Letters Vol.31 N0.13, June 95

2. Paper presented in 6th European Conference EPE95, September 95

AN ACTIVE FILTER FOR ELIMINATING CURRENT HARMONICS CAUSED BY NON-LINEAR CIRCUIT ELEMENTS

Z.D.Koozehkanani, P.Mehta, M.K.Darwish

Indexing terms:Active Filters,Current-harmonics

In recent years there has been an increasing concern over the introduction of current harmonics in power supply systems due to the use of non-linear loads such as television receivers, personal computers and thyristors for controlling electric motors, lamps and heaters. Conventional filtering techniques which use passive filters are inflexible in that they can not cope with the variation in the filtering requirements as the load and system conditions vary. This paper presents the development of an active filter which can be connected across the offending non-linear load and is capable of self-tuning and overcomes the disadvantages of the conventional passive filters.

Principle of operation: Fig. 1 illustrates the principle of the proposed technique used for filtering of current harmonics generated by a non-linear load. As shown, the filter is connected across the supply in parallel with the load. The filter consists of two capacitors, two inductors and two bi-directional switches. The switches are operated in antiphase so that the filter current through the inductor, L_1, flows through the capacitors alternately. When one of the capacitors carries the filter current and the other one resonates with the inductor, L_2 The resonant current within the filter dose not appear at the terminals of the filter and thus has no effect on the current. This in fact signifies the difference between this circuit and the conventional resonant filter. The rate of rise of current and the amplitude depends mainly on the size of capacitors and the initial voltages on them. These factors are function of the switching pattern. These two factors provides considerable flexibility in shaping the waveform of current drawn by the filter. If the phases, magnitudes and the frequency of the various current harmonics are controlled such that they match the undesirable current harmonics drawn by the non-linear load, the supply current is free of current harmonics. The key to the control of the filter is to determine the appropriate switching function for the switches as shown below.

*Analysis and experimental results:*Assuming the direction of the currents in figure 1 and using the notations k=1, h=2 when switch 1 is closed and switch 2 is open and vice versa, the circuit can be represented by the following equations:

$$\frac{di}{dt} = \frac{v_i - v_{c_k} - R_{L_1} i_1}{L_1} \quad (1)$$

$$\frac{dv_{c_k}}{dt} = \frac{i_1}{C_k} \quad (2)$$

$$\frac{di_2}{dt} = \frac{-v_{c_h} - R_{L_2} i_2}{L_2} \quad (3)$$

$$\frac{dv_{c_h}}{dt} = \frac{i_2}{C_h} \quad (4)$$

where R_{L1} and R_{L2} are the resistances of the two inductors. Since the input current and the current in the inductor L_2 and the voltage across the capacitors are continuos, the initial conditions for the equations in one state is the final conditions in the previous state. The switching pattern associated with the switches together with the circuit parameters determine the level and order of harmonics in the filter current.

For the circuit to operate as an active filter, the aim is to determine a switching pattern appropriate to the harmonics to be eliminated in the non-linear load current. If the coefficient of harmonics of $I_{load} = I_{fund} + I_{load}$ are A_n and B_n, the function $J = f(t) = \sum_{n=3}^{NHmax} \sqrt{A_n^2 + B_n^2}$ called the cost function is the measure of harmonics in the total current where vector t denotes the switching instants in switching pattern and NHmax is the maximum range of frequency to be eliminated. The objective is to minimise the cost function by optimising the switching pattern. The conjugate direction method [3] is employed to achieve this. The summary of algorithm used is given below.

step1: For the starting switching instants (t_0) compute

$g_0 = \nabla f(t_0)^T$ and set $d_0 = -g_0$

step2 .For k=0,1,2,...n-1

a)Set $t_{k+1} = t_k + a_k d_k$ where a_k minimise $f(t_k + a_k d_k)$

b)Compute $g_{k+1} = \nabla f(t_{k+1})^T$

c)Unless k =n-1, set $d_{k+1} = -g_{k+1} + b_k d_k$.

$$b_k = \frac{g_{k+1}^T g_{k+1}}{g_k^T g_k}$$

step3: Replace t_0 by t_n and go back to step1

Fig. 2 shows the input current waveform and its spectrum for a rectifier load with capacitive filter which is typical of the input stage of power supplies in most equipment. Figure 3 shows the corresponding waveforms with the active filter connected to the circuit. This was achieved by optimising for forty one harmonics.

Conclusion: This novel approach for design of active filters provides an alternative method of controlling current harmonics generated by non-linear loads such as rectifiers. Whilst a conventional filter circuit can only attenuate a range of harmonics, the proposed approach can achieve almost complete elimination. It would be suitable for applications where the magnitude, phase and range of current harmonics are not predictable, on-line control of the filter would provide a good solution.

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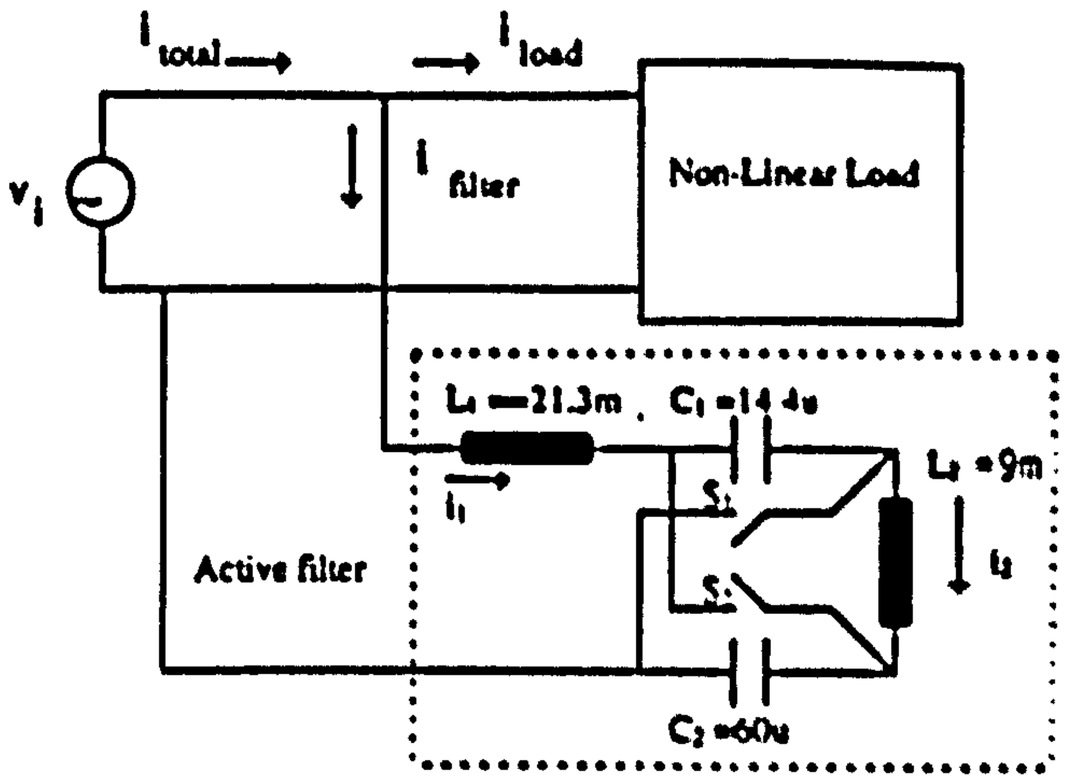

Fig.1:*Principle of active filtering technique*

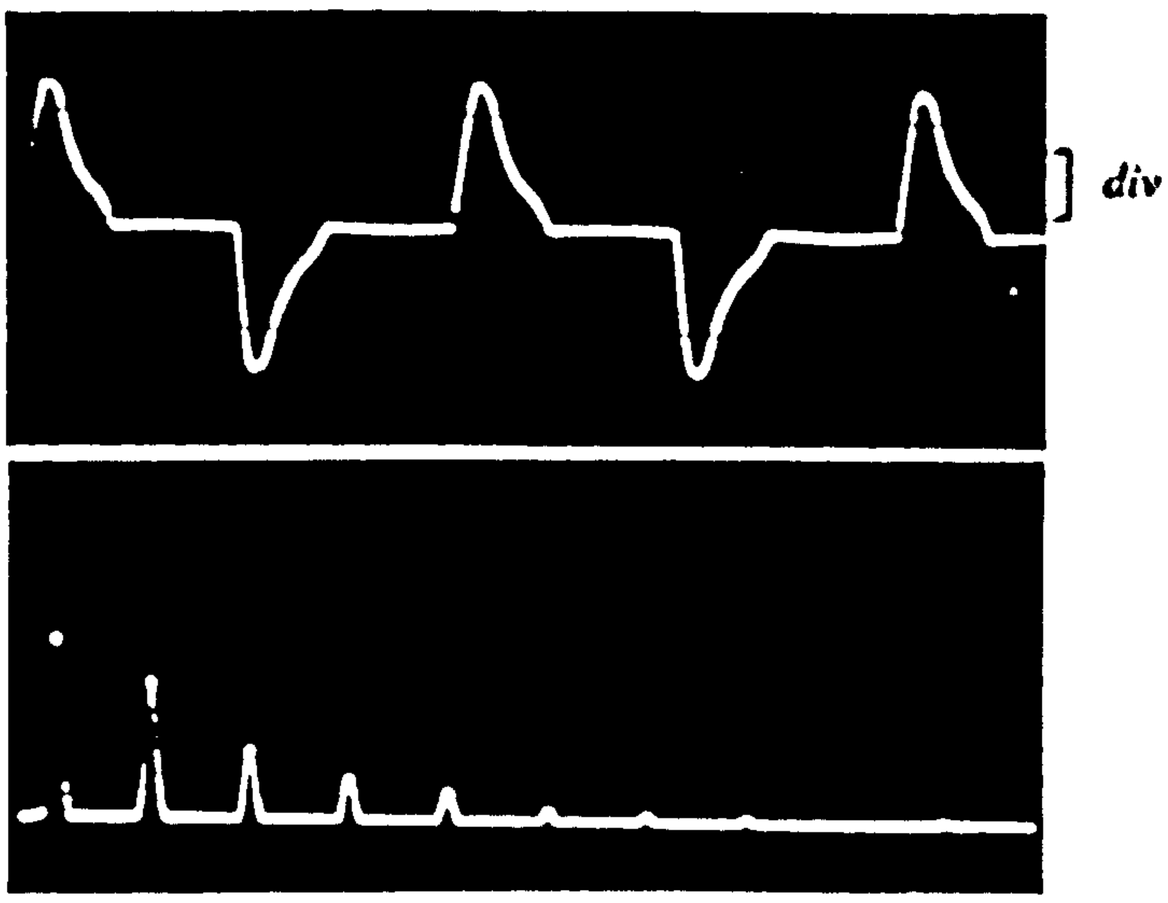

Fig 2 :*The current waveform of load (2A/div) and its spectrum*

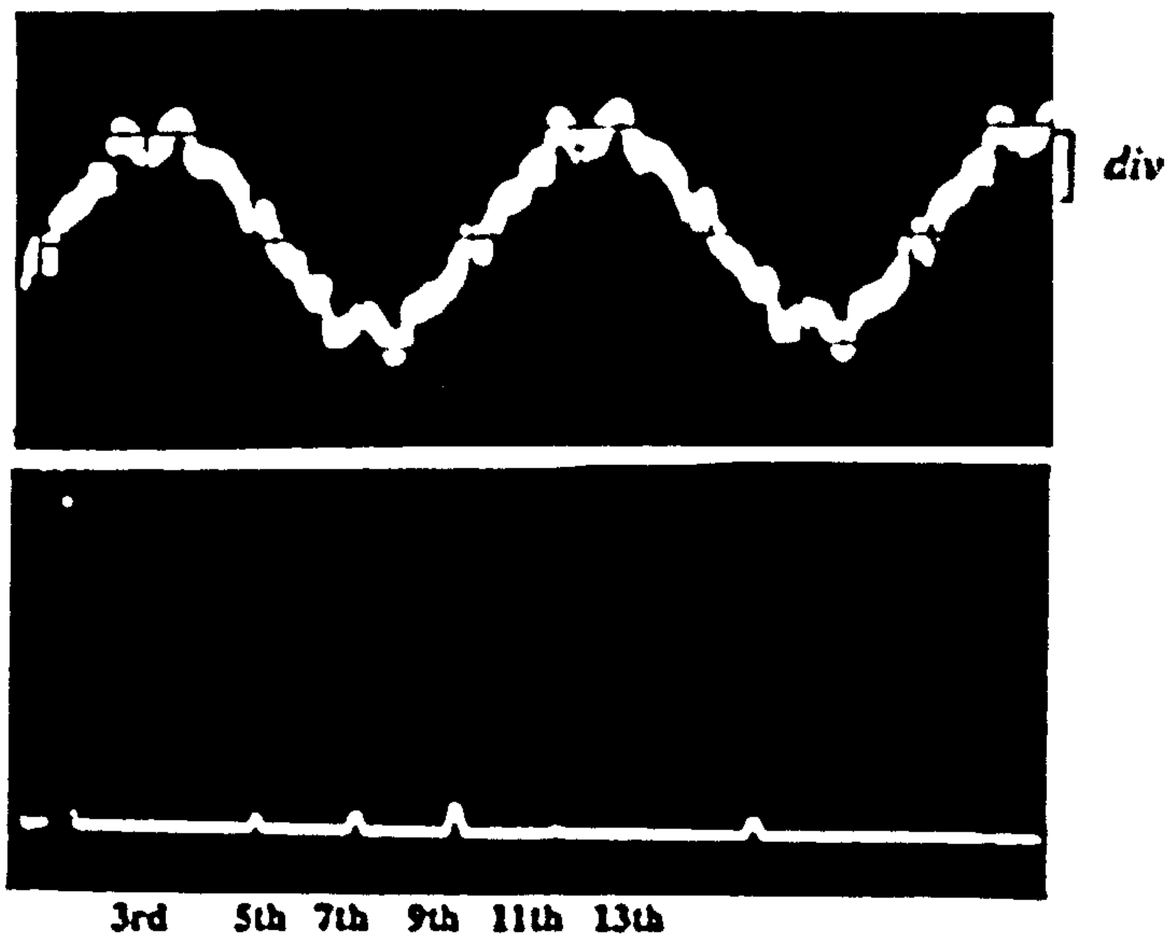

Fig 3 :*The current waveform (2A/div) after compensation and its spectrum*

ACTIVE SYMMETRICAL LATTICE FILTER FOR HARMONIC CURRENT REDUCTION

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Abstract In recent years there has been increasing concern over the introduction of current harmonics in power supply systems due to the use of non-linear loads such as thyristor converters. This has resulted in considerable interest in the development of active filters suitable for eliminating a range of current harmonics. This paper presents the development of active filters which are derived from the conventional symmetrical lattice circuits. To assess the effectiveness of this approach the filter is used to reduce current harmonics in a rectifier circuit feeding a capacitive load.

Keywords. Active filter ,Current harmonics

PRINCIPLE OF ACTIVE LATTICE FILTER

Figure 1 shows the principle of the technique used for filtering current harmonics generated by a non-linear load. The active filter is connected in parallel with the load and it is in fact a non-linear device itself. This filter could be a switched-impedance element or another converter (1).

This paper presents two configurations of active filters which are derived from a conventional symmetrical lattice filter by replacing some of the passive elements by switches. In the first configuration as shown in Figure 2, the pairs of bi-directional switches S_1 and S_2 and S_3 and S_4 operate synchronously and in anti-phase. To avoid short circuiting the capacitor during the transfer of current from one set of switches to the other, a small resistor with a switch across it is included in series with the capacitor. This switch is opened during the transfer of current between the two pairs of main switches. The second configuration is a modification of the first circuit by replacing one pair of switches with inductors of the same size; the two switches operate synchronously. The filters are connected to the mains via inductors. The rate of rise of current in the first circuit changes with the change in the polarity of the voltage on the capacitor during switching operation. The disadvantage of this circuit is that at high switching frequency the fundamental component of current drawn from the supply is quite significant and it is not totally reactive.

In the second circuit the switching operation changes not only the polarity of voltage across the capacitor but also the impedance of the filter from being inductive to capacitive and vice versa. These two factors in the second circuit provide considerable flexibility in shaping the waveform of current drawn by the circuit.

The various current harmonics in the circuit are controlled such that they have the same magnitude but are in anti-phase to the undesirable current harmonics drawn by the non-linear load, thereby eliminating harmonics in the supply current. The key to the control of the filter is to determine the appropriate switching function for the switches as shown below.

ANALYSIS AND EXPERIMENTAL RESULTS

Analysis of the fist circuit

Considering the direction of the currents in the circuit of Figure 2, the circuit can be represented by the following equations:
When a pair of switches are in the 'on'state

$$\frac{di}{dt} = \frac{v_1 - R_1 i - v_C}{L_1} \qquad (1)$$

$$\frac{dv_C}{dt} = \frac{i}{C} \qquad (2)$$

When the other pair of switches are in the 'on' state

$$\frac{di}{dt} = \frac{v_1 - R_1 i + v_C}{L_1} \qquad (3)$$

$$\frac{dv_C}{dt} = \frac{-i}{C} \qquad (4)$$

where R_1 is the resistance of the inductor. Since the voltage across the capacitor and the current through the inductor must be continuous the initial conditions for the equations in one state are the final conditions for the previous state.

Analysis of the second circuit

Assuming the direction of the currents as shown in the circuit of Figure 3, the circuit can be represented by the following equations:

When the switches are in the 'off' state

$$i_{sw} = 0$$

$$i = i_L = i_C$$

$$\frac{di}{dt} = \frac{v_i - (R_s + 2R_L)\, i - v_C}{L_s} \qquad (5)$$

$$\frac{dv_C}{dt} = \frac{i}{C} \qquad (6)$$

When the switches are in the 'on' state

$$i = i_L + i_{sw}$$

$i_L = i_{sw} + i_C$ and then $i_C = i - 2i_{sw}$

$$\frac{di}{dt} = \frac{v_i - R_s\, i + v_C}{L_s} \qquad (7)$$

$$\frac{dv_C}{dt} = \frac{i_C}{C}$$

replacing i_C from $i_C = i - 2\, i_{sw}$

$$\frac{dv_C}{dt} = \frac{i - 2\, i_{sw}}{C} \qquad (8)$$

In this state the capacitor is in parallel with the inductors and hence

$$L\frac{di_L}{dt} + R_L\, i_L = -\, v_C$$

since $i_L = i - i_{sw}$

$$\frac{di_{sw}}{dt} = \frac{v_C + R_L(i - i_{sw})}{L} + \frac{di}{dt} \qquad (9)$$

where R_s and R_L are the resistance values of the inductors L_s and L respectively.

The input current and the voltage across the capacitor are continuos, the initial conditions for one state are the final conditions for the previous state. The initial condition for the current in the switch, i_{sw}, is zero. To prevent the possibility of high voltages appearing across the switches during the transition from the 'on' to the 'off' state, the snubber circuits, not shown, have to be included.

The switching pattern associated with the switches together with the circuit parameters determine the magnitude and order of harmonics.

For the circuit to operate as an active filter, the aim is to determine a switching pattern appropriate to the harmonics to be eliminated in the load current.

Load with fixed condition:

If the coefficient of harmonics of $i_{load} = i_{filter} + i_{load}$ are A_n and B_n the function:

$J = f(t,x) = \sum_{n=3}^{NH_{max}} \sqrt{A_n^2 + B_n^2}$, called the cost function, is the measure of harmonics in the total current where the vector, t, x, and NH_{max} are the switching instant, the circuit parameters and the maximum range of frequency to be eliminated respectively.

The objective is to minimise the cost function by optimising the switching pattern and the magnitude of the circuit parameters. To achieve this, initially the cost function is minimised for NH_{max}=3. Then the resulting switching pattern and the parameter values are used as starting values to minimise the cost function for NH_{max}=5 and this process continues for higher NHmax values. The summary of the algorithm used is given below.

1) The starting points, t_0, for switching instants are calculated as the midpoints of pulses in a uniform switching pattern or can be taken as random values t_1^0, t_2^0, t_3^0... , t_m^0 (m is the number of switching instant in each period) and also starting values for elements x_0 are taken randomly, x_1^0, x_2^0 ...., x_n^0 (n is the number of independent elements in the circuit).

2) The filter current, i_f, for the above switching instants and circuit parameters is calculated using Rung Kutta method.

3) The total current is calculated using $i_t = i_l + i_f$.

4) The harmonic coefficients of total current up to NH_{max} are evaluated and the cost function J is calculated.

5) The conjugate direction method with modification is employed to minimise the cost function and determine the optimum values of the switching instants and circuit parameters as follows:

a) The gradient of the cost function are evaluated with respect to the switching instants and circuit parameters

$$g^0 = \nabla J = [g^0_1, g^0_2, \ldots, g^0_{m+n}]^T$$

$$= \left[\frac{\partial J}{\partial t_1}, \frac{\partial J}{\partial t_2}, \ldots, \frac{\partial J}{\partial t_m}, \frac{\partial J}{\partial x_1}, \frac{\partial J}{\partial x_2}, \ldots, \frac{\partial J}{\partial x_n}\right]^T$$

b) The direction of the steepest descent is set to be equal to g^0 which is the initial value of g, $d^0 = -g^0$ or $[d_1^0, d_2^0, d_3^0, \ldots, d_{m+n}^0]^T = [g_1^0, g_2^0, g_3^0, \ldots, g_{m+n}^0]^T$

c) The small numbers proportional to the size of the steepest descent values are calculated and β_i (i =1,2,3,...., m+n) are set to these values. For example if S_i is the number of digits of d_i^0 then $\beta_i = 10^{-(S_i+1)}$

For i = 1, 2, 3, ..., m+n

d) The values of the switching instants and circuit parameters are evaluated by the following expression: $t = t^0 + \beta\, d.^0$ and $x = x^0 + \beta\, d^0$ where $t^0 = [\, t_1^0, t_2^0, t_3^0 \ldots, t_m^0\,]^T$ are the starting switching instants and $x^0 = [\, x_1^0, x_2^0, \ldots, x_n^0\,]^T$ are the starting values for circuit elements and $\beta = [\beta_1, \beta_2, \ldots, \beta_i \ldots, \beta_{m+n}]^T$, $\beta_i = 10^{-(S_i+1)}$, $\beta_1 = \beta_2 = \ldots = \beta_{m+n} = 0$.

e) The cost function J for the above switching instants and circuit parameters are recalculated.

f) β_i is incremented and steps from d to e are repeated until the minimum value of J is found.

g) The gradient of the cost function with respect to the new switching instants and parameters are calculated and the direction of the steepest descent d is evaluated as:

$$d = -g^0 + b^0\, d^0 \quad \text{where} \quad b^0 = \frac{g^T g}{g^{0T} g^0}.$$

h) The starting switching instants $t^0 = [\, t_1^0, t_2^0, t_3^0 \ldots, t_m^0\,]^T$ are reset by the new evaluated values of $t = [\, t_1, t_2, t_3 \ldots, t_m\,]^T$ and also the starting values of circuit elements $x^0 = [\, x_1^0, x_2^0, \ldots, x_n^0\,]^T$ are reset by the new evaluated values $x = [\, x_1, x_2, \ldots, x_n\,]^T$.

i) The values of d^0 and g^0 are reset by the values of d and g that occur at J_{min}

j) steps from c to j are repeated until the minimum value of J_{min} is obtained.

If the cost function J reaches zero, i.e., all harmonics up to NH_{max} are cancelled and the filter would be an ideal filter.

Load with varying condition:

For varying load conditions the aim is to determine the switching pattern whilst maintaining fixed values of the circuit parameters. The summary of the algorithm used is shown in Figure 4 where i represents the varying load condition.

1) The parameters and the switching pattern for the circuit are evaluated for one of the load conditions by the method described above.
2) The values of circuit elements are reset to these values.
3) The switching pattern for the filter with the evaluated parameters are optimised for different conditions of load and stored, and also the values of cost functions for each case are calculated and averaged
4) The above process is repeated for i = 2, 3, ... , k to achieve the minimum average of the cost functions. The corresponding values of the circuit elements at this minimum are considered as the best values. The corresponding switching patterns are the most optimum.

Figures 5 and 6 show the unfiltered load current (I_{load}), the filter current, the current waveform after compensation and the switching pattern for the two configurations respectively. Figure 7 shows the spectrum of the uncompensated load current. Figures 8 and 9 illustrate the corresponding spectrum of current after compensation for the two circuits respectively. It should be noted that, whilst there is a significant reduction in the current harmonics, there is an increase in the fundamental component of the input current. This increase should not cause any problems because it is capacitive in nature.

Conclusion

The novel approach for design of active filters presented here provides an alternative method of controlling current harmonics generated by non-linear loads such as rectifiers. Whilst a conventional filter circuit can only attenuate a range of harmonics, the proposed approach can achieve almost complete elimination. Since the on-line control of the filter is feasible the proposed approach is suitable for applications where the magnitude, phase and range of current harmonics are not predictable.

The two circuits presented here belong to a family of active filters at present under investigation at Brunel University.

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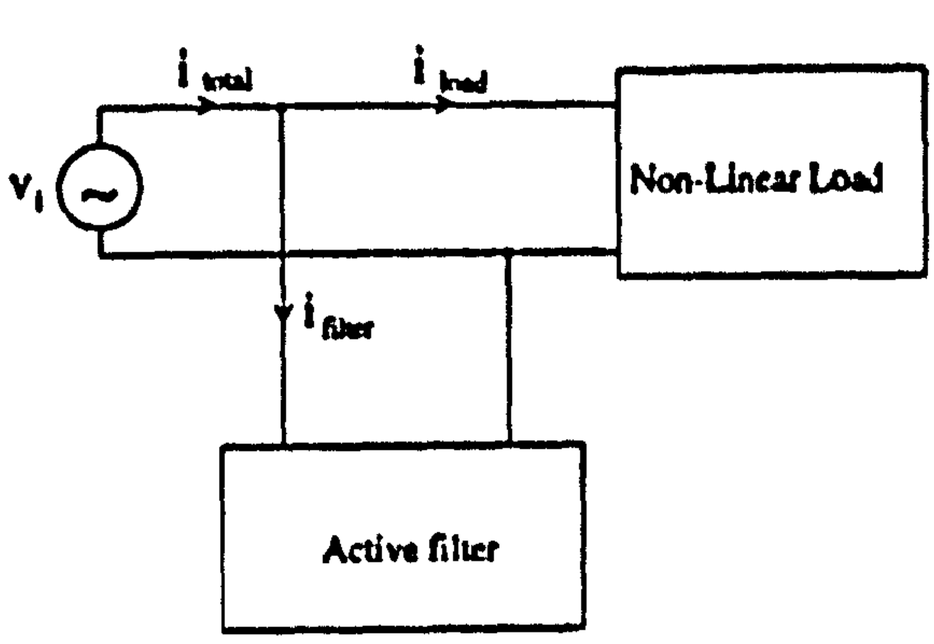

Figure 1
Principle of active filtering technique

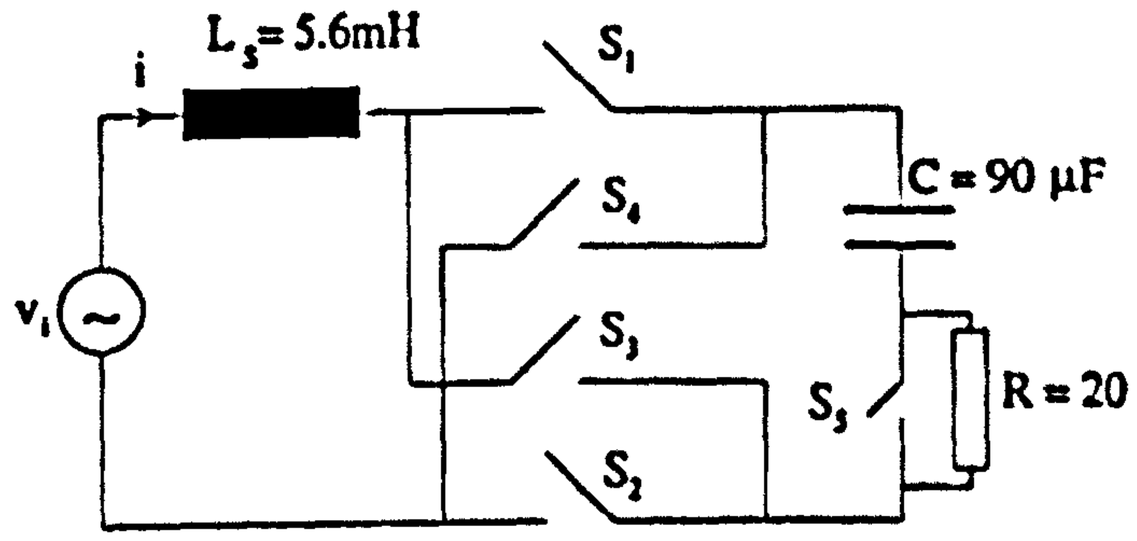

Figure 2
The proposed active filter

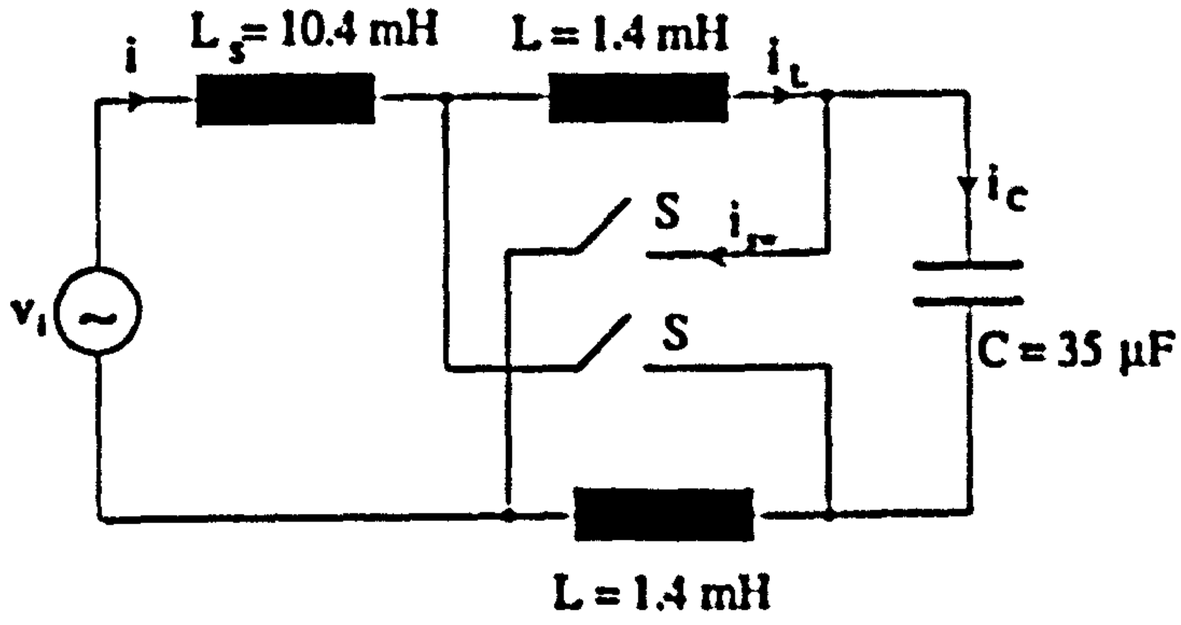

Figure 3
The second proposed active filter

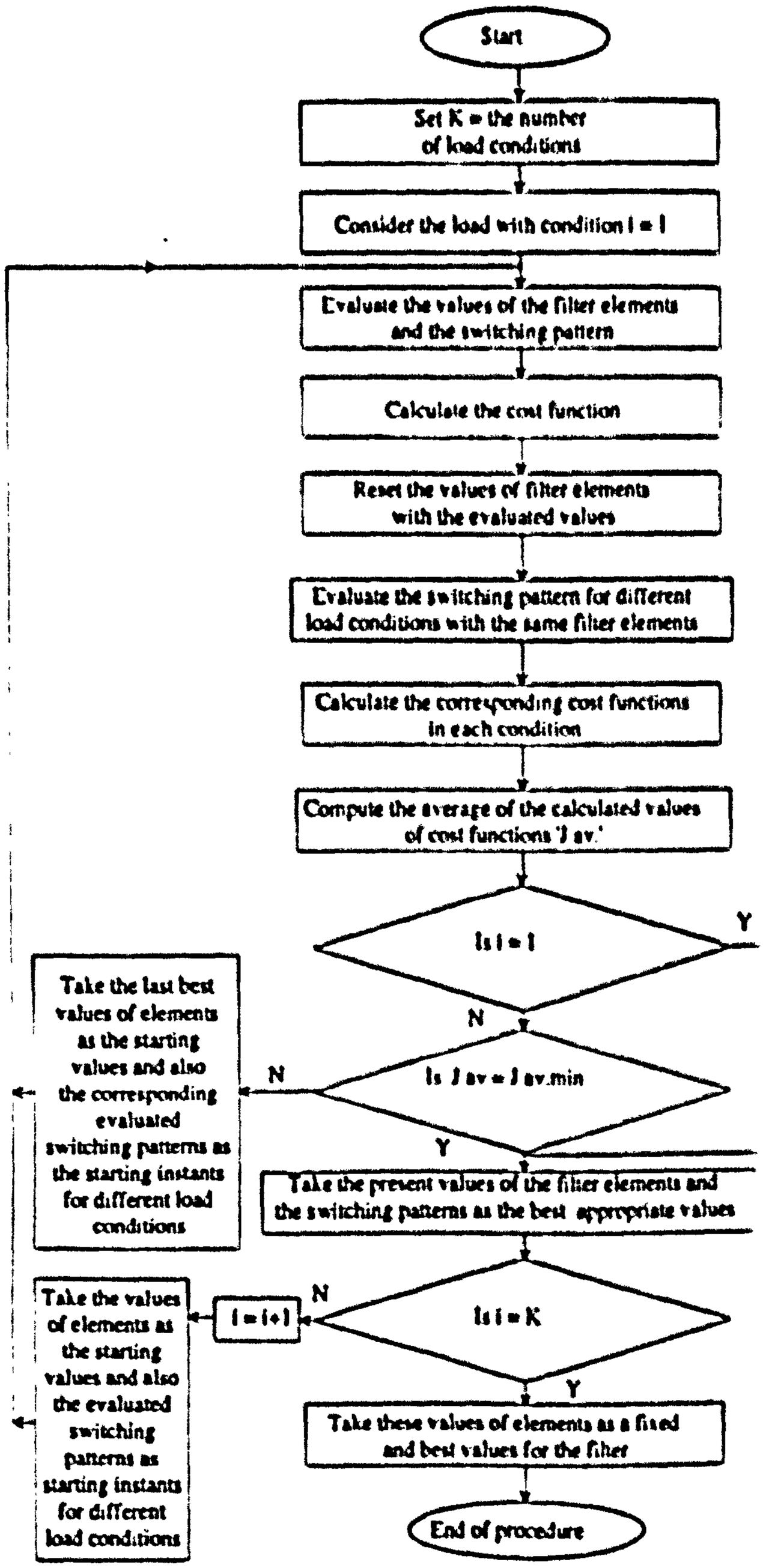

Figure 4
Flowchart for evaluating the active filter parameters and switching pattern for a load with varying conditions

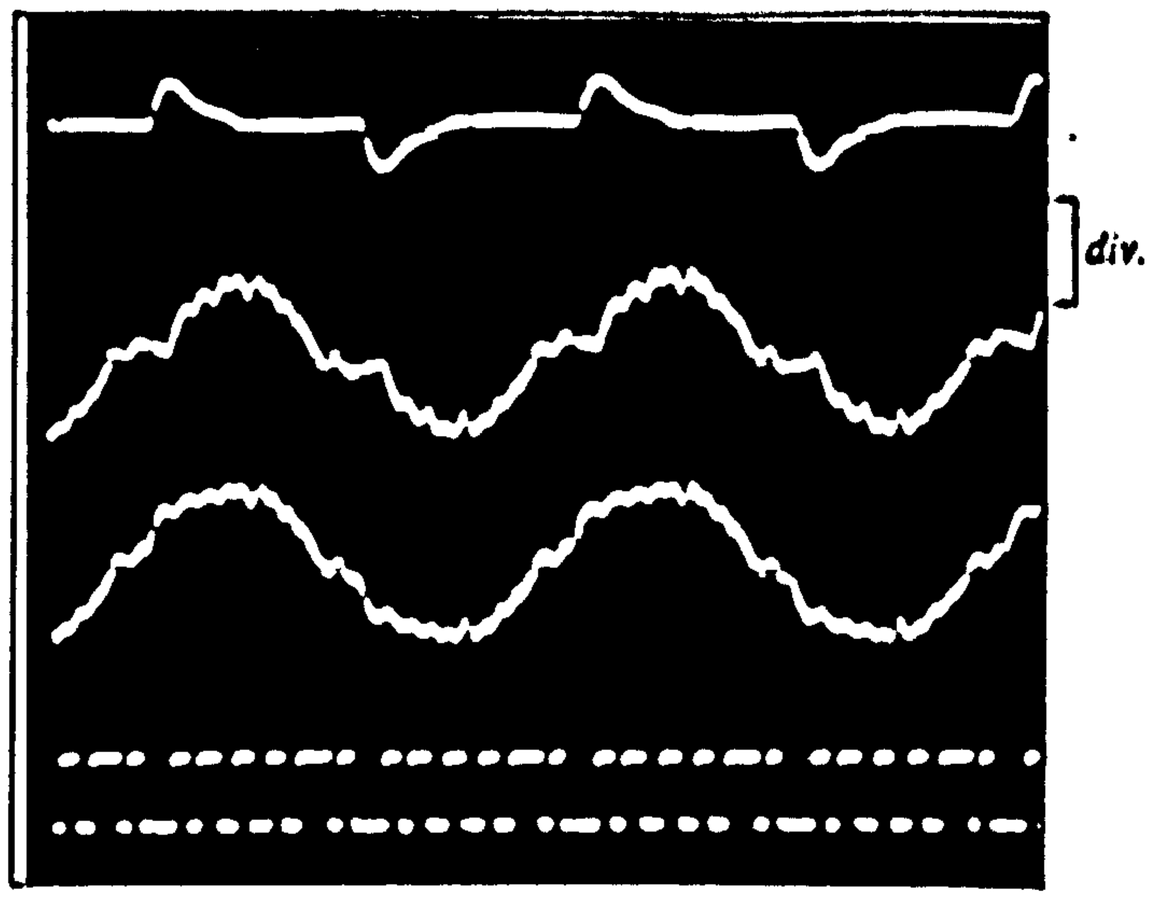

Figure 5
Load current, filter current, compensated current and the switching pattern *(4A/div.)*

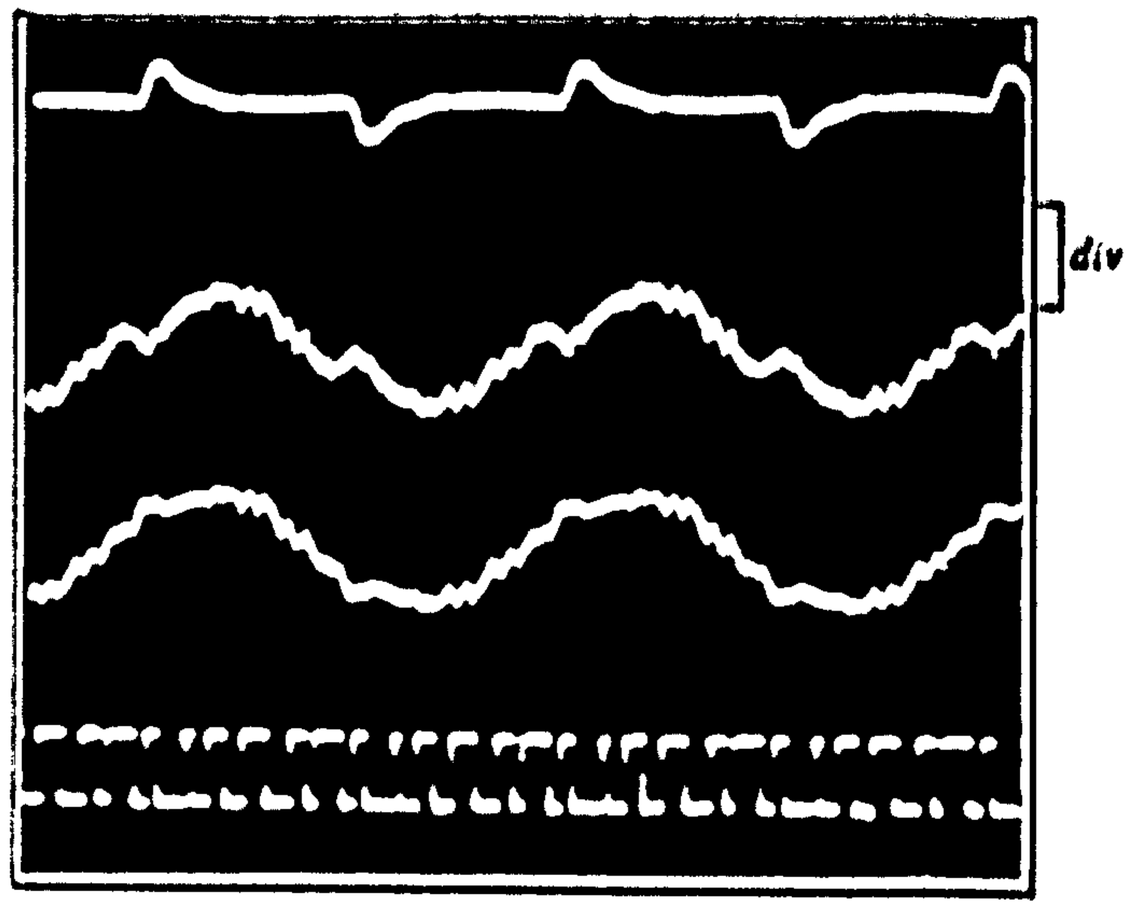

Figure 6
Load current, filter current, compensated current and the switching pattern for the second configuration *(4A/div.)*

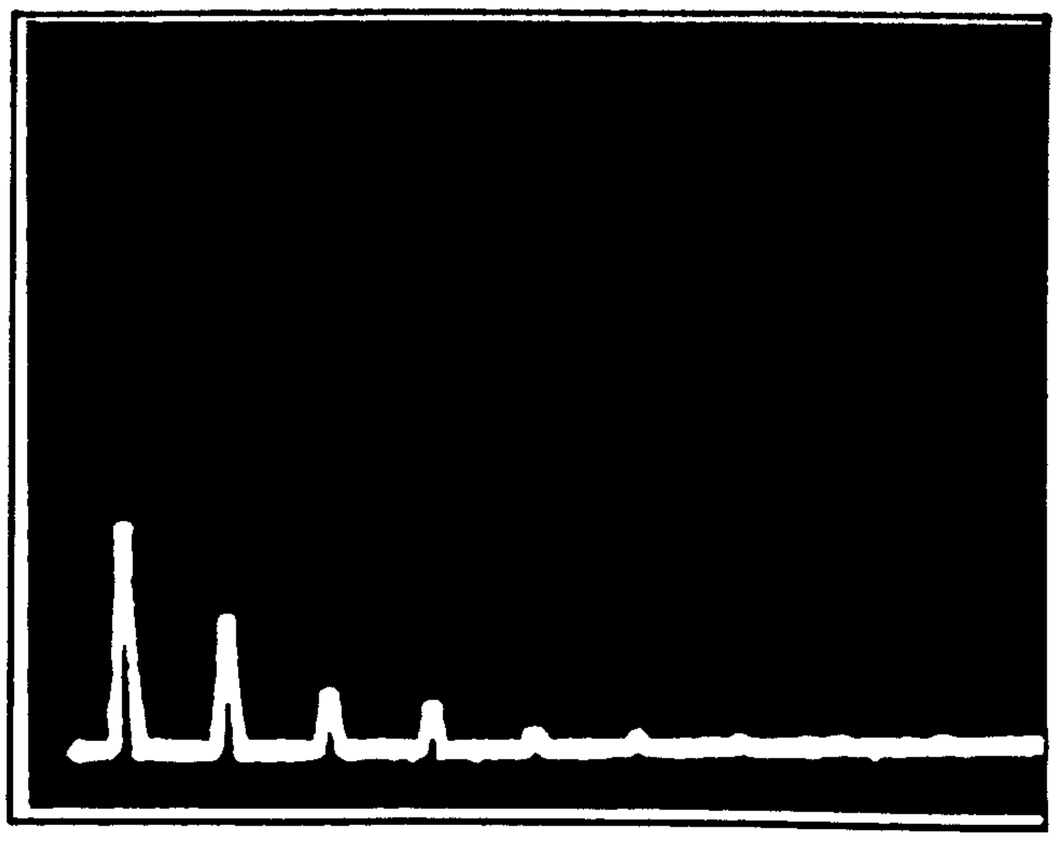

Figure 7
Spectrum of the load current (50Hz, 150Hz, 250Hz, . . .)

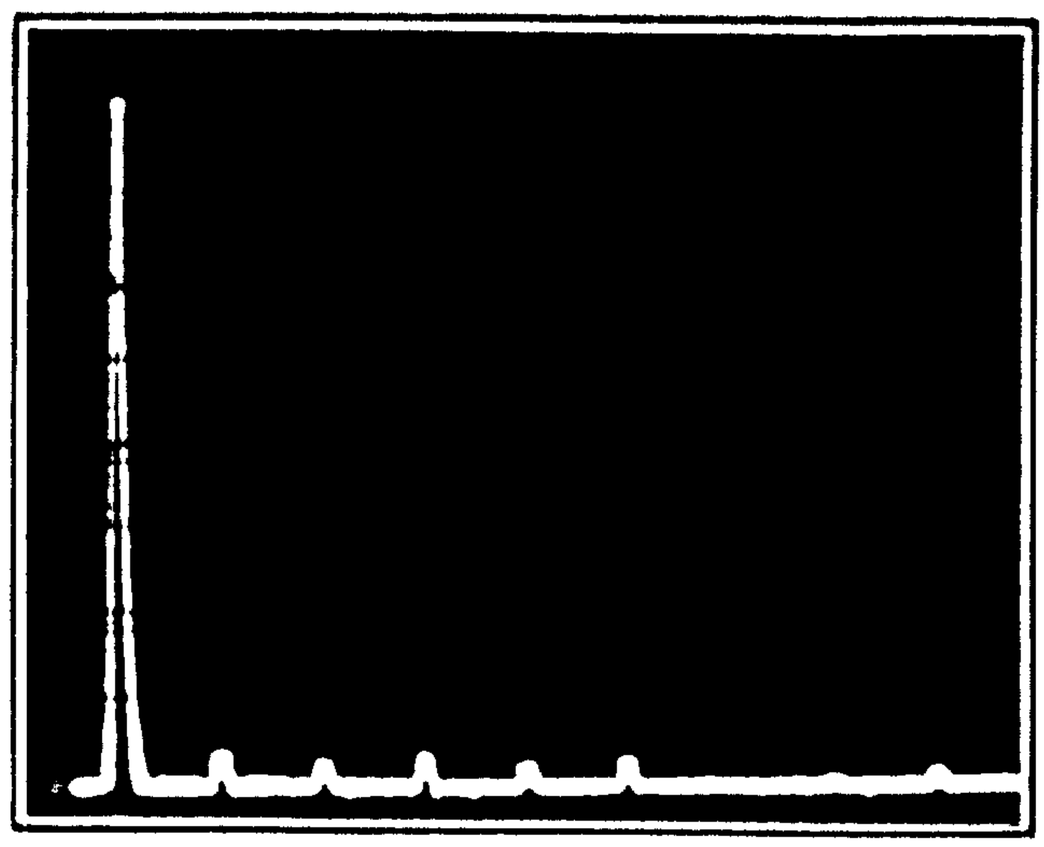

Figure 8
Spectrum of the current after compensation (50Hz, 150Hz, 250Hz, . . .)

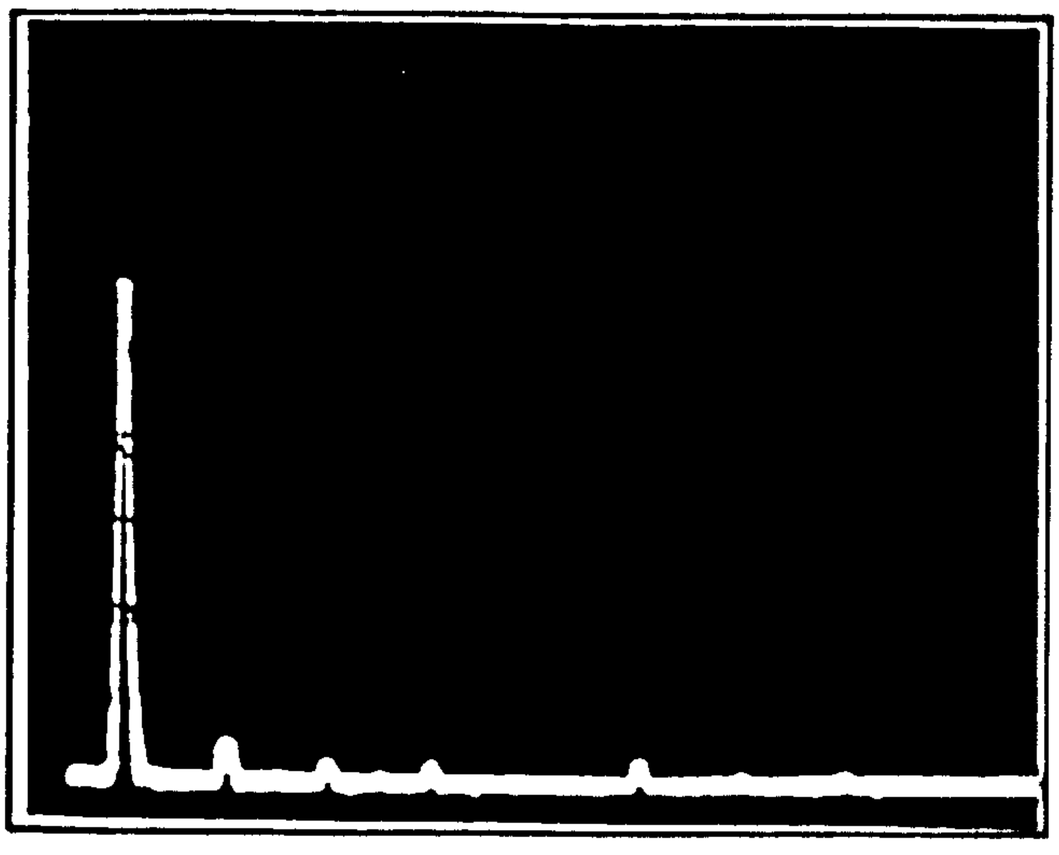

Figure 9
Spectrum of the current after compensation in the second configuration (50Hz, 150Hz, 250Hz, . . .)