Paths Towards High Efficiency Silicon Photovoltaics

Thesis by

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To my family

Acknowledgments

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Abstract

While photovoltaics hold much promise as a sustainable electricity source, continued cost reduction is necessary to continue the current growth in deployment. A promising path to continuing to reduce total system cost is by increasing device efficiency. This thesis explores several silicon-based photovoltaic technologies with the potential to reach high power conversion efficiencies.

Silicon microwire arrays, formed by joining millions of micron diameter wires together, were developed as a low cost, low efficiency solar technology. The feasibility of transitioning this to a high efficiency technology was explored. In order to achieve high efficiency, high quality silicon material must be used. Lifetimes and diffusion lengths in these wires were measured and the action of various surface passivation treatments studied. While long lifetimes were not achieved, strong inversion at the silicon – hydrofluoric acid interface was measured, which is important for understanding a common measurement used in solar materials characterization. Cryogenic deep reactive ion etching was then explored as a method for fabricating high quality wires and improved lifetimes were measured.

As another way to reach high efficiency, growth of silicon-germanium alloy wires was explored as a substrate for a III-V on Si tandem device. Patterned arrays of wires with up to 12% germanium incorporation were grown. This alloy is more closely lattice matched to GaP than silicon and allows for improvements in III-V integration on silicon.

Heterojunctions of silicon are another promising path towards achieving high efficiency devices. The GaP/Si heterointerface and properties of GaP grown on silicon were studied. Additionally, a substrate removal process was developed which allows the formation of high quality free standing GaP films and has wide applications in the field of optics.

Finally, the effect of defects at the interface of the amorphous silicon heterojuction cell was studied. Excellent voltages, and thus efficiencies, are achievable with this system, but the voltage is very sensitive to growth conditions. We directly measured lateral transport lengths at the heterointerface on the order of tens to hundreds of microns, which allows carriers to travel towards any defects that are present and recombine. This measurement adds to the understanding of these types of high efficiency devices and may aid in future device design.

Contents

List of Figures

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List of Publications

Portions of this thesis have been drawn from the following publications:

- H. Emmer and H. A. Atwater, "Measurement of silicon surface inversion induced by buffered hydrofluoric acid," *In Preperation*, 2015.
- D. B. Turner-Evans, H. Emmer, C. T. Chen, and H. A. Atwater, "Flexible, transparent contacts for inorganic nanostructures and thin films," *Advanced Materials*, vol. 25, no. 29, pp. 4018–4022, 2013. DOI:10.1002/adma.201300927
  Contributed to wire growth and processing efforts, supported measurements
- C. T. Chen*, H. S. Emmer*, S. Aloni, D. B. Turner-Evans, and H. A. Atwater, "Cu-catalyzed vapor-liquid-solid growth of sige microwire arrays with chlorosilane and chlorogermane precursors," *Crystal Growth & Design*, vol. 15, no. 8, pp. 3684–3689, 2015. DOI:10.1021/acs.cgd.5b00097 *equally contributing authors.
- D. B. Turner-Evans, C. T. Chen, H. Emmer, W. E. McMahon, and H. A. Atwater, "Optoelectronic analysis of multijunction wire array solar cells," *Journal of Applied Physics*, vol. 114, no. 1, pp. –, 2013. DOI:10.1063/1.4812397
  Supported device design and simulation efforts
- C. T. Chen, D. B. Turner-Evans, H. Emmer, S. Aloni, H. Atwater, *et al.*, "Design and growth of iii-v on si microwire array tandem solar cells," in *Photovoltaic Specialists Conference (PVSC), 2013 IEEE 39th*, pp. 3397–3401, IEEE, 2013. DOI:10.1109/PVSC.2013.6745178
  Contributed to silicon wire growth and processing efforts
- H. Emmer, C. T. Chen, R. Saive, D. Friedrich, Y. Horie, A. Arbabi, A. Faraon, and H. A. Atwater, "Fabrication of free standing crystalline gallium phosphide thin films," *In Preperation*, 2015.

Chapter 6 draws heavily from:

- ©2013 IEEE. Reprinted, with permission, from H. Emmer, M. Deceglie, Z. Holman, A. Descoeudres, S. De Wolf, C. Ballif, and H. Atwater, "Experimental measurement of lateral transport in the inversion layer of silicon heterojunction solar cells," in *Photovoltaic Specialists Conference (PVSC), 2013 IEEE 39th*, pp. 1229–1231, June 2013. DOI:10.1109/PVSC.2013.6744362
- ©2014 IEEE. Reprinted, with permission, from M. G. Deceglie, H. S. Emmer, Z. C. Holman, A. Descoeudres, S. De Wolf, C. Ballif, H. Atwater, *et al.*, "Scanning laser-beam-induced current measurements of lateral transport near-junction defects in silicon heterojunction solar cells," *Photovoltaics, IEEE Journal of*, vol. 4, no. 1, pp. 154–159, 2014. DOI:10.1109/JPHOTOV.2013.2289353
  Contributed to experimental design, test device design and fabrication, measurement and analysis

Chapter 1

Introduction

1.1 Introduction

Photovoltaics hardly need any introduction today. This technology has successfully made its way from a laboratory curiosity, to a niche product, and finally to an important, mainstream electricity generation source. In the five year period of 2009-2014, total worldwide installed solar capacity has doubled three times from 22 GWp (Gigawatts of peak power output) to 177 GWp. As of 2014, photovoltaics provide 1% of the total electricity produced worldwide[1] and rapid growth is expected to continue.

This rapid growth is driven by a similarly rapid drop in prices. In 2010, the United States Department of Energy set a then-lofty goal of reaching total system installed costs of $1/Wp by 2020; this goal has likely already been met, five years early, in utility-scale installations [2]. Grid parity, as defined by the levelized cost of energy (LCOE) produced by a photovoltaic system equaling the cost of current retail electricity rates, has been surpassed in regions of 30 countries worldwide [2]. The passing of this critical threshold will fuel the continuation of rapid solar industry growth in the coming years.

The overarching goal of research efforts in the field of photovoltaics is continuing the reduction of total system costs, which enables the continued growth in the deployed photovoltaic capacity worldwide. This thesis explores technologies that hold potential to reduce the cost of silicon based photovoltaic systems by reducing the quantity of silicon material used and improving device efficiency. Improvements in efficiency have the potential to reduce total system costs by reducing the balance of system costs. As shown in figure 1.1, the module only makes up a small part of the cost of a residential photovoltaic installation. Many of the other (balance of system) costs, both hard costs like racking and wiring and soft costs like logistics, scale inversely with efficiency. Put simply, if the efficiency of a module increases by 10%, you are able to get 10% more power out of a system with the same amount of racking, labor, and warehouse space. Improvements in materials and device design and processing can directly reduce the module costs and improvements in device efficiency

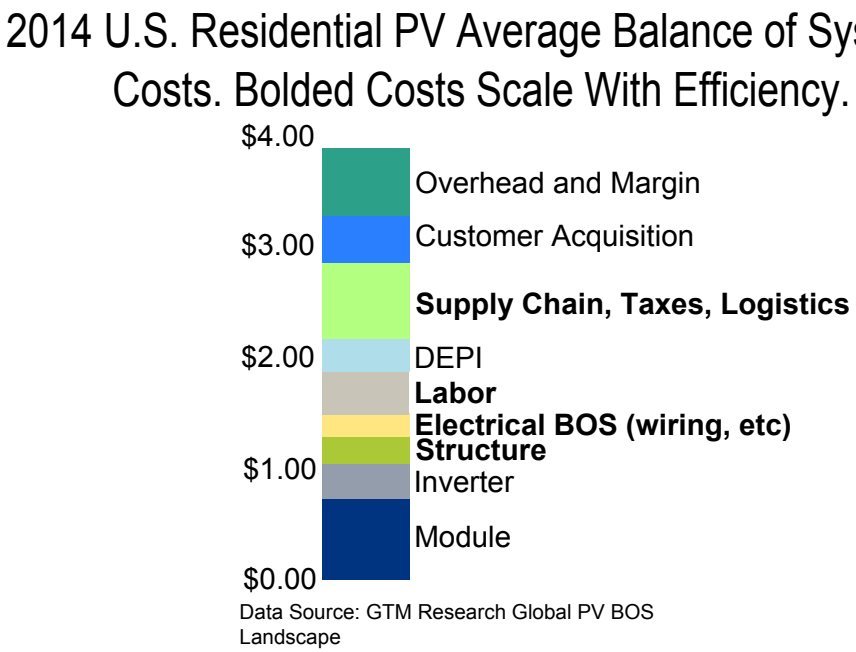


Figure 1.1: Breakdown of balance of systems costs in average 2014 United States residential PV installations. Bolded categories are expected to scale with efficiency.

can drive down the total cost of an installed photovoltaic system by reducing the balance of system costs.

1.2 Photovoltaic Device Operation and Performance

Total power conversion efficiency is the most important parameter in comparing the performance of photovoltaic devices in the majority of applications. We can break the efficiency down into three components:

$$\eta = \frac{V_{OC} J_{SC} FF}{P_{in}}$$

Where V_{OC} is the voltage at open circuit, J_{SC} is the current density at short circuit, and FF is the fill factor, defined by the fraction or percentage of $V_{OC}J_{SC}$ that can be extracted from a cell at the maximum power point. This is shown visually in figure 1.2: The fill factor is the ratio of the area of the dark shaded rectangle to the light shaded rectangle.

1.2.1 Open Circuit Voltage

The fundamental operation of a photovoltaic device requires two basic steps. First, a photon must be absorbed by the material, causing the generation of an electron-hole pair. Second, the electron

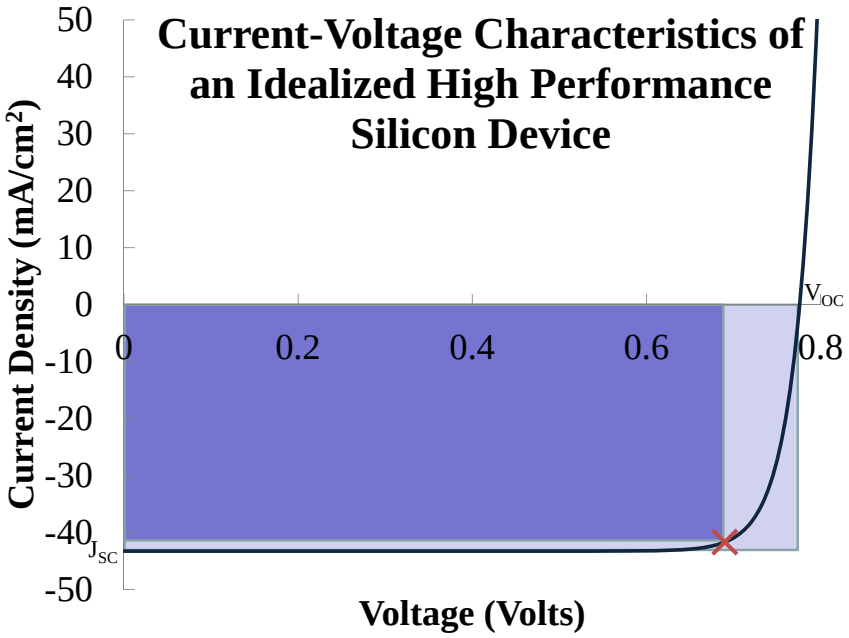


Figure 1.2: Current-voltage characteristics of an idealized high performance silicon solar cell. Short circuit current density and open circuit voltage are labeled at the axis intercepts and the maximum power point is marked with an $\times$.

and hole must be collected outside of the device at different energies. This is most often achieved using a semiconductor material and some form of a p-n junction. The p and n type regions can support different quasi-Fermi levels, or chemical potentials, fulfilling the second requirement. Like a Fermi level, the quasi-Fermi level describes a population distribution, in this case the population of minority carriers in each region. Therefore, the chemical potential difference, or voltage, established in a device is a function of the minority carrier population excited in the semiconductor material. It is not, as commonly thought, a result of the built in potential of a p-n junction [3]. The open circuit voltage can be given as:

$$V_{OC} = \frac{kT}{q} \ln\left(\frac{(N_A + \Delta n)\Delta n}{n_i^2}\right)$$

where Δn is the excess minority carrier concentration, or the injection level. The injection level can then be related to device parameters by:

$$\Delta n = \frac{\Phi}{W}\tau_{eff}$$

where Φ is the absorbed solar flux, W is the thickness of the device, and τ_{eff} is the effective minority carrier lifetime.

Thus, in order to increase the minority carrier density and the voltage of a device, there are three possible strategies. First, Φ could be increased. This is the strategy taken in concentrating photovoltaic modules, and indeed the voltages and therefore efficiencies under concentration are higher than under one sun. The second option is to reduce the thickness of the absorbing material. The final parameter, the lifetime, is a measure of the overall material and surface interface quality.

1.2.2 Short Circuit Current

The short circuit current is a measure of how much light is converted to electron hole pairs and subsequently extracted from the device. In a high quality device, the vast majority of the generated electron hole pairs can be collected. Therefore, improvements to the short circuit current require an increase in the amount of incident light absorbed. Incident light can be lost to either reflection or incomplete absorption — light that enters and exits the material without being absorbed. There is a tradeoff between improvements in V_{OC} and J_{SC} that can be achieved by thinning the device. A high efficiency photovoltaic will incorporate light trapping which allows thin materials, which have higher voltages, to effectively absorb light and have high current as well.

1.2.3 Fill Factor

As defined earlier, the fill factor measures the squareness of the current-voltage characteristic. The fill factor is a function of V_{OC}, but the parameters that effect it the most are the series and shunt resistances, R_S and R_{SH}. These are generally considered engineering issues, somewhat removed from the design of the device. However, when considering new device geometries, it is important to consider, for example, the influence of base doping or transparent conductive oxide conductivity on R_S.

1.3 Past, Present, and Future

For many years, the majority of solar cells sold were fabricated using a simple and cost effective design, consisting of a multi- or mono-crystalline p-type wafer with an aluminum back surface field/rear contact, a diffused phosphorous emitter, silicon nitride front passivation/antireflective coating, and silver screen printed front contacts. While there were many advances in device designs and record cells throughout the 1980s [4], few of these made any impact on industrially realizable designs. Industrial innovation yielded better and cheaper wafers, but the basic design remained unchanged for the majority of devices [5].

This trend of inexpensive, simple devices dominating the market is likely beginning to shift. Several high efficiency device designs which were once considered exotic and expensive are currently on the market, and signs point to higher efficiency devices becoming more common in the future. For example, Sunpower, which manufactures devices based on the high efficiency interdigitated back contact design, is currently one of very few profitable device manufacturers based in the United States. Sanyo/Panasonic has manufactured the HIT silicon heterojunction device for years, and SolarCity/Silevo is currently in the process of building the largest solar cell fab in the United States based on this high efficiency technology. Recently, researchers have developed a version of the passivated emitter, rear locally diffused (PERL) cell, which held the record for silicon device efficiency until recently, using only inexpensive process steps, achieving a 19.4% efficiency [6] industrially relevant device. It seems likely that this design will become widespread in the coming years.

The ultimate goal of photovoltaics research is to develop a low cost, deployable technology. As the photovoltaic industry continues to scale up, there will be significant investment in developing tools and techniques to continue reducing the cost of processes which may currently be expensive. While original critics of Sunpower may have thought that patterning the interdigitated contacts would be too expensive, or the high quality wafers required for these devices would cost too much, the enabling process technologies have improved and proved to be commercially viable. Even atomic layer deposition [7] and ion implantation [8], both once widely thought to be cost prohibitive in solar applications, have recently received significant attention and will likely be viable in the near future.

Therefore, it is important to continue to research high efficiency devices, separate from the ability to make a commercially viable process today.

The work in this thesis explores the limits of high efficiency devices from two different, but related, angles. First, we examine the potential of microwires for use in extremely thin high efficiency devices. Next, we explore the properties of the gallium phosphide/silicon and amorphous silicon/crystalline silicon heterojunction systems. As explored further, the latter is an enabling technology for the former. I believe that in the future, photovoltaics will be both high efficiency *and* low cost, and extremely thin heterojunction devices are likely candidates to achieve this.

Chapter 2

Advances in Silicon Microwire Photovoltaics

2.1 Introduction

The wire array photovoltaics project began several years before my arrival in the Atwater group, and some great achievements were made by the dozen or so students, post-docs, and professors working on this project. Notably, growth of high fidelity pattered wire arrays was achieved with a variety of catalyst materials [9] and over large area substrates [10]. Wire arrays were shown to absorb as much light as conventional wafer-based modules using only a small fraction of the material [11]. Large area devices achieved efficiencies of 9% [12], while single wire devices showed potential for efficiencies up to 17% [13]. Following these successes, a start-up company was spun out of our labs with the goal of bringing this technology to market.

The original motivation for the wire array photovoltaic project was to create a waferless silicon photovoltaic device. The patterning and growth processes were developed such that the silicon wafer which was used as the growth substrate would become a reusable piece of capital, rather than a consumable part of the photovoltaic module. A potentially scalable process to utilize this technology is:

1. A new silicon wafer with a thermal oxide is patterned by photolithography or imprint lithography
2. Copper catalyst particles are deposited in holes in the oxide by electrodeposition
3. Wires are grown by a vapor liquid solid chemical-vapor-deposition process from the copper catalyst particles, with p-n junction formed in situ
4. The wires are cleaned and sidewalls passivated
5. A flexible polymer is used to fill the spaces between the wires

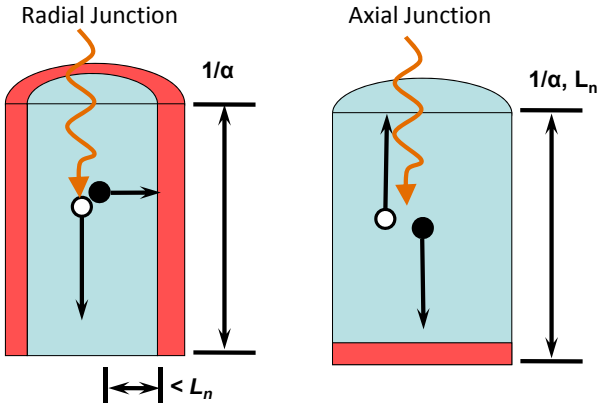


Figure 2.1: Schematic of radial and axial junction devices. The axial junction geometry minimizes junction area and parasitic absorption, but requires longer minority carrier diffusion lengths, greater than the length of the wire rather than the radius, to extract carriers.

6. Wires are mechanically removed from the growth substrate contacted, and installed into a module

7. The substrate is reused many times, repeating from step #2

The wire devices previously developed had a junction in the radial direction, as shown schematically in figure 2.1. This device geometry has the advantage of allowing the use of lower quality material by orthogonalizing the directions of light absorption and carrier collection [14]. In a planar solar cell, the minority carrier diffusion length (L_D) must be much greater than the device thickness t, while the optical absorption length α must be less than the thickness. This requirement ensures that light is fully absorbed in the cell and that carriers generated by light absorbed at the back of the cell can diffuse up to the junction and be extracted. The orthogonalization of these characteristic lengths means that we no longer require that $L_D > t > \alpha$. Light is absorbed throughout the entire length of the wire device, while carriers can be extracted from the much smaller radius. Therefore, lower material quality as measured by L_D, can be tolerated while still yielding good current collection and decent efficiencies. However, if L_D is long, higher efficiencies can be achieved in an axial junction geometry, which minimizes the junction area and thus dark current. We explore the feasibility of improving device efficiency by transitioning to axial devices by evaluating the achievable minority carrier diffusion length.

During my tenure at Caltech, the price of a solar grade silicon wafer fell by an impressive 16% annually, resulting in a wafer that costs less than one third of what it did when the silicon wire project began [15]. The focus on this project, and my own research focus, has therefore shifted from developing a low cost but moderate efficiency technology to realizing other potential advantages of these unique structures. Due to their high light absorption and high aspect ratio, micron-scale wires

are uniquely positioned for use in very high efficiency (>25%) photovoltaic devices. First, the high aspect ratio geometry of arrays of vertically oriented wires allows the potential to grow out defects in the horizontal direction and allow high quality, defect-free growth in the vertical direction [16]. Thus, vertically oriented wires could act as an ideal substrate for growth of tandem photovoltaics. To this end, we investigated the growth of silicon-germanium alloy wires, which is presented in Chapter 3. Second, these wires, which have radii on the order of the wavelength of light, were found to absorb light very strongly — in some cases even exceeding the traditional $4n^2$ geometrical light trapping limit. This allows for the use of less material, and consequentially operation at higher injection levels and voltages. Progress towards devices based on this goal is presented in Chapter 4.

Prior to shifting focus away from VLS grown silicon wires, the broad goals of the silicon wire project were to continue on the path towards developing a commercially viable technology, which involved improving device efficiency and simplifying and improving the reproducibility of our growth process. Progress towards this goal included developing an in situ junction formation process which both provided a simple process and a means for measuring material quality, and investigation of our wire growth process at different temperature regimes.

2.2 In Situ Phosphorus Doping

Previously, only p-type doping was performed in situ by flowing boron trichloride (BCl_3) during growth. The original decision to grow p-type silicon wires and form junctions by diffusion doping n-type emitters was likely due to safety concerns; BCl_3 gas and solid phosphorus diffusion sources are significantly less hazardous than phosphine (PH_3) gas. Solar cells with p-type bases also provide a number of other potential advantages. First, electrons have higher mobilities than holes, and therefore the minority carrier diffusion length is longer in p-type material given equal electron and hole lifetimes. Second, while it does not result in the highest efficiency device, it is a simple process to form both a back contact and back surface field in p-type silicon by firing aluminum onto the rear. Finally, it is well known that phosphorous diffusion acts to getter metal impurities, including copper and iron which are likely present in our VLS wire material, from silicon [17]. The potential disadvantage of p-type base material, and one of the major forces driving the conventional photovoltaic industry towards n-type wafers, is the formation of boron-oxygen dimers, which form a deep level trap [18]. However, this is more relevant in very high quality material; residual copper and other metal impurities or surface effects will dominate the lifetime of wires, rather than B-O complexes.

Despite the noted advantages of p-type base material, it was desirable to add the capability to grow n-type material as well. The original goal was to use n-type silicon as photoanodes in a photoelectrochemical water splitting device [19]. Upon my arrival to Caltech, a bottle of dilute

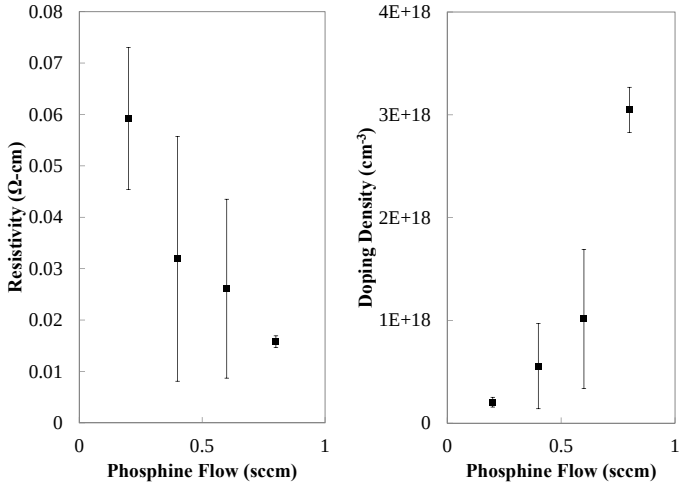


Figure 2.2: Phosphine doping calibration. Resistivity was measured with four point measurements, and doping density inferred from resistivity using standard mobility values [20].

phosphine (PH_3, 500 ppm in H_2) had recently been added to the wire growth CVD reactor located in the Noyes lab. This added capability opened up the door to the growth of in situ junctions, as described in the next section.

Initial growths were performed at low flow rates, and the effects of doping characterized by measuring resistivity using four point contacts. The measured resistivites and the corresponding expected doping concentrations are shown in figure 2.2. Anecdotally, the growth rate and fidelity seemed to drop slightly compared to undoped growths when using PH_3 doping, but at the time of the initial characterization, the growths were not reproducible enough to well quantify these effects. This would be in contrast to the increase in growth rate and fidelity observed in growths using BCl_3 doping. Despite these effects, it was possible to grow high quality arrays of n-doped wires with in situ phosphine doping.

As observed more directly and discussed further in the next section, it was observed that the phosphorus created a heavily doped core by diffusing in from the sidewalls during growth. The resistivity measured following a surface etch was significantly higher than before. This contrasts with the p-type growths, in which the measured resistivity does not significantly change after the cleaning and surface etch process.

2.3 In Situ Junction Formation

The state of the art junction formation process for microwire array solar cell fabrication in our group was a fairly complicated process which involved several steps. First, the wire array is oxidized to

create a diffusion masking oxide. A polymer infill is then used to define the junction height, and the oxide above the polymer is etched away, leaving a "boot" at the bottom which prevented the n^+ emitter from shorting to the p^+ substrate/back surface field region. The array is then cleaned before a diffusion doping step is performed to create a p-n junction. A schematic of this process and more details are available elsewhere [12].

In contrast, an in situ junction formation process offers many advantages over the diffusion junction formation process. The first advantage to this process is simplicity and reproducibility. Achieving a reproducible polymer infill height has consistently been one of the more challenging steps in the device fabrication process. When considering scaling up production, an in situ junction formation is not only easier to perform reproducibly, but also eliminates two high temperature or vacuum deposition steps, allowing for a lower device cost.

Another advantage, and the original motivation for developing this process, is that junction formation does not require a high temperature step after growth. These devices can therefore be used to probe the material quality of the wire as it is grown, and separate out any influence of other processing steps which could add (or remove) impurities. Another possible option that fulfills these requirements would mimic the previously used radial junction process, but replace the thermal oxidation with a low temperature plasma enhanced chemical vapor deposition (PECVD) or physical vapor deposition oxide deposition, and replace the diffusion doping step with a PECVD amorphous silicon (a-Si) deposition. However, the capability to deposit n^+ doped a-Si was not yet available in our labs at this time; additionally, this process would still require the poorly controlled polymer infill step.

Finally, the end result of the in situ junction formation process will be an axial junction device. As described previously, the axial junction has the potential to achieve higher efficiencies than radial junction devices, but will require high material quality.

2.3.1 Growth of Wires with In Situ Junctions

The most successful process for growing in situ junctions turned out to be the simplest. The growth process began using the same techniques to pattern and grow p-doped wire arrays, but three quarters of the way through the growth, the dopant gas was switched to phosphine. The maximum phosphine flow rate was used, and it is expected that this gave doping concentrations in the 10^{19} cm^{-3} range, based on measurements at lower flow rates.

One potential concern was the abruptness of the junction. The growth rate of the wires varied from about 5-10 microns per minute. It is estimated that the residence time of the reactor is approximately one minute, resulting in a worst case junction that is graded along a 10 micron length. An attempt was made to grow wires with a more abrupt junction by pausing the growth and purging the base dopant before introducing the emitter dopant. The $SiCl_4$ and BCl_3 flows were

stopped, leaving the H_2 carrier gas purging the system, for two minutes or more minutes. This corresponds to approximately two times the gas residence time in the reactor. This resulted in a defective region visible in figure 2.3. Without further investigation, it seems as though the defective growth begins as the precursor concentration in the reactor and the catalyst particle decays, and a second, larger, defect occurs as growth resumes. All samples in which growth was paused and resumed had very high series resistance and poor diode ideality. The samples without a pause had quite good ideality (<2) and reasonable series resistance. Light beam induced current measurements on unpassivated wires, as shown in the following section, resulted in a small spot, indicating that the junction is fairly abrupt. This is not surprising; it is expected that the flow of gasses in the reactor growth tube is reasonably laminar, and the diffusion through the gas mix would be a much smaller effect than mixing within the growth tube. Further improvement would require both better measurements of junction profile, and design of a reactor which minimizes dead time and gas mixing.

It is also important to note that good devices were only obtained in the first growth in which phosphorous was introduced in the tube. Subsequent growths resulted in single wire devices which gave ohmic behavior, implying that the phosphorous from the tube sidewalls was mobile enough to cause the base to become n-type. Thus, the usual growth process involved doing two or three intrinsic or p-doped growths to condition a new tube, and once high fidelity, stable growth is realized, performing a single in situ junction forming growth. In a scaled process, it may be possible to remove the doped surface growth by etching in potassium hydroxide; this was not attempted, as the small tubes used in that reactor are inexpensive enough to simply replace.

2.3.2 Measurements of In Situ Junctions in Single Wires

The main techniques used to characterize the in situ grown wires were current-voltage (IV) and light beam induced current (LBIC) measurements on single wires. Single wires were contacted according to the following process:

1. Wires are cleaned on-substrate. Cleaning process varied, as described below, but generally consisted of RCA cleans to remove the copper catalyst and surface contamination.

2. A razor blade was used to mechanically scrape wires off the growth substrate and disperse wires in isopropanol.

3. The wires dispersed in isopropanol are spun onto a low pressure CVD silicon nitride coated silicon wafer, for 30 seconds at 300 RPM, 30 second at 600 RPM, and 1 minute at 1200 RPM.

4. Microchem LOR10a is spun on the substrate at 1500 RPM for 30 seconds to aid in liftoff after contacting the wires with thick metal.

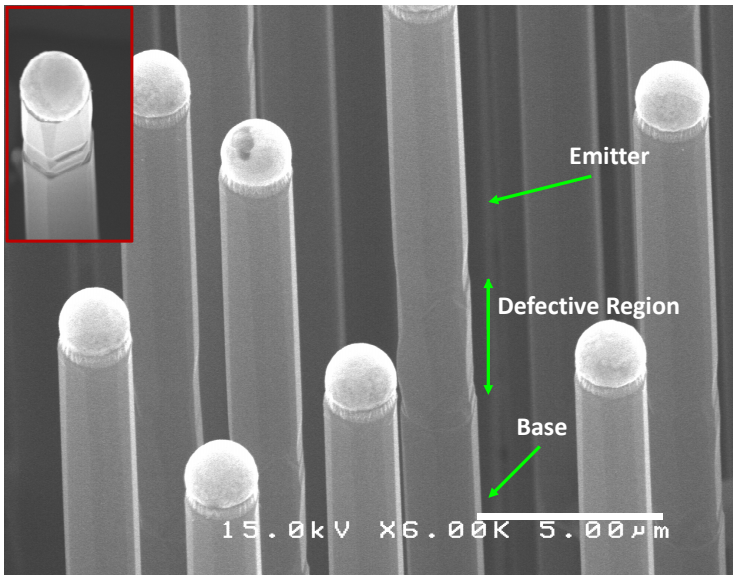


Figure 2.3: Attempt at in situ junction growth with a pause to purge the base dopant. Inset (upper left) shows the wire at near-normal incidence, with the same scale, showing higher contrast in the defective region.

5. Individual wires are patterned using Shipley S1813 photoresist and a dark field mask to allow multiple exposures on each chip.

6. Contacts are formed with about 1 µm of metal. Both aluminum capped with silver and gold capped with titanium were used successfully. The aluminum contacts require an anneal at 200-400 °C

Current-voltage measurements are presented in this section using a current density, normalized to an approximate cross sectional wire area. Note that for wires, this is different from the total junction area, as relevant in dark current measurements, and potentially different from the light absorption cross section. This is because these wires, which have dimensions on the order of the wavelength of light, may absorb light beyond their physical extents. While for these reasons it is difficult to extract actual large area device parameters from individual wire measurements, it is straightforward and valuable to compare single wires from different samples using these techniques.

Light beam induced current measurements were performed with a Zeiss LSM 710 scanning confocal microscope. The wire current output is fed into a home built transimpedance amplifier with a gain of 100 kΩ and into the microscope through a connector spliced into the photomultiplier tube input. The microscope software is then able to form an image from the photocurrent signal. The scale of the current intensity can be measured using a calibrated photodiode, and the quantum efficiency can be extracted from the measurement. However, current data is presented here in arbitrary

units, useful as a comparison between different areas of the same sample. Ideally, the intensity of the photocurrent signal in the base, moving away from the junction, can be fit to an exponential which corresponds to the diffusion length L_D in the wire base. However, as discussed in the following sections, generation of current in the base, even combined with an exponential decay, is often indicative of the presence of a radial carrier separation and collection path, rather than a long diffusion length into the base.

Following growth, the samples were cleaned to remove the copper catalyst, and single wire contacts were made. Immediately following growth, a thin n-type region was present throughout the length of the wire, forming a lightly doped emitter shell around the base core. Evidence of this is shown in figure 2.4, in both the IV curve and light beam induced current (LBIC) image. Current was collected throughout the length of the wire, with no surface passivation applied. Additionally, the low open circuit voltage of approximately 300 mV and high series resistance both result from the thin, high sheet resistance emitter shell that formed during growth. The high resistance caused an extremely low fill factor of 27%, and the resulting single wire device total power conversion efficiency was approximately 2%.

A potassium hydroxide etch was used to remove the n-doped region from the surface. Considering the growth time and temperature, $\sqrt{Dt}$ for phosphorous diffusion into silicon is about 20 nm, so the target etch depth was approximately 30 nm. The samples were etched in 40% KOH for 1 minute and 30 seconds at room temperature. After this, a second RCA 2 clean was used to remove any remaining metal ions. Resulting device IV curves and LBIC images are shown in figure 2.5, and reveal that the radial junction was successfully removed. Once the surface etch is performed, reasonable diode characteristics are revealed, but recombination in the base region prevents electrons from reaching the axial junction for collection. As a result, the total photocurrent is very low, and only the region right around the junction lights up in LBIC measurements.

Silicon nitride (SiN_x) and amorphous silicon (a-Si) were used as surface passivation treatments, and these samples were also characterized with I-V curves and LBIC microscopy. Results from a champion SiN_x passivated device are shown in figure 2.6. While full current collection was achieved in the base, the open circuit voltages were lower than expected for a high performing axial junction device. The champion device had a Voc of 475 mV, while the average voltage obtained from single wire devices was 406 mV. The likely cause of this is a high density of fixed positive charges at the Si/SiN_x interface well known to be present in PECVD deposited films [21]. These interface fixed charges cause inversion at the outer surface of the SiN_x coated base region. This inverted region induces a radial junction, and thus provides a path for electrons to reach the n-doped silicon emitter as majority carriers.

The a-Si, on the other hand, passivates the surface but the carrier collection length in the axial region remains extremely low, likely limited by the lifetime, and consequently diffusion length, in the

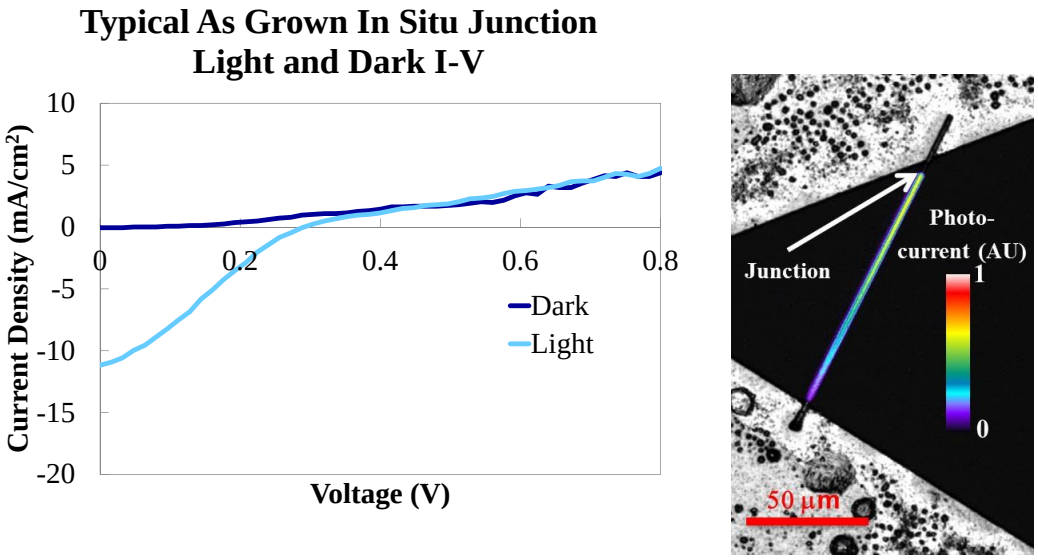


Figure 2.4: (left) Current-voltage characteristic of a typical in situ junction device, following cleaning to remove the catalyst particle but without a surface etch. $V_{OC} = 291$ mV and $J_{SC} = 11.20$ mA/cm^2. (right) Light beam induced current measurements reveal current collection from the entire base region, with moderate decay.

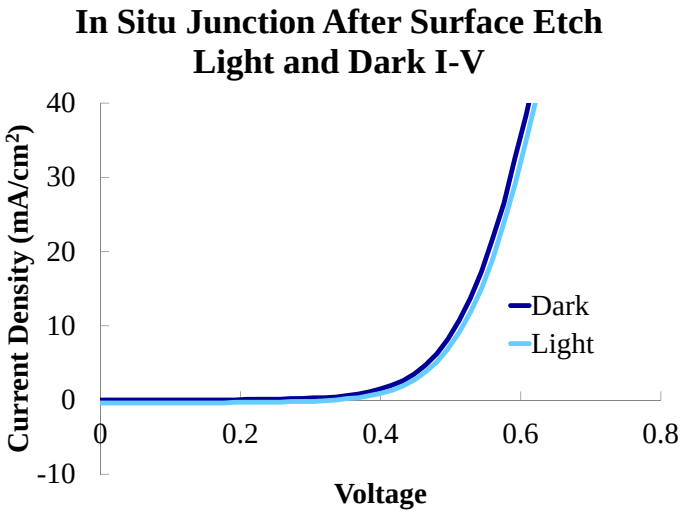


Figure 2.5: Current-voltage characteristic of the champion situ junction device following a KOH surface etch. $V_{OC} = 336$ mV and $J_{SC} = 0.40$ mA/cm^2. All other samples exhibited unmeasurably small photoresponse. Light beam induced current measurements (not pictured) reveal current collection from a very small region, on the order of one micron, near the junction.

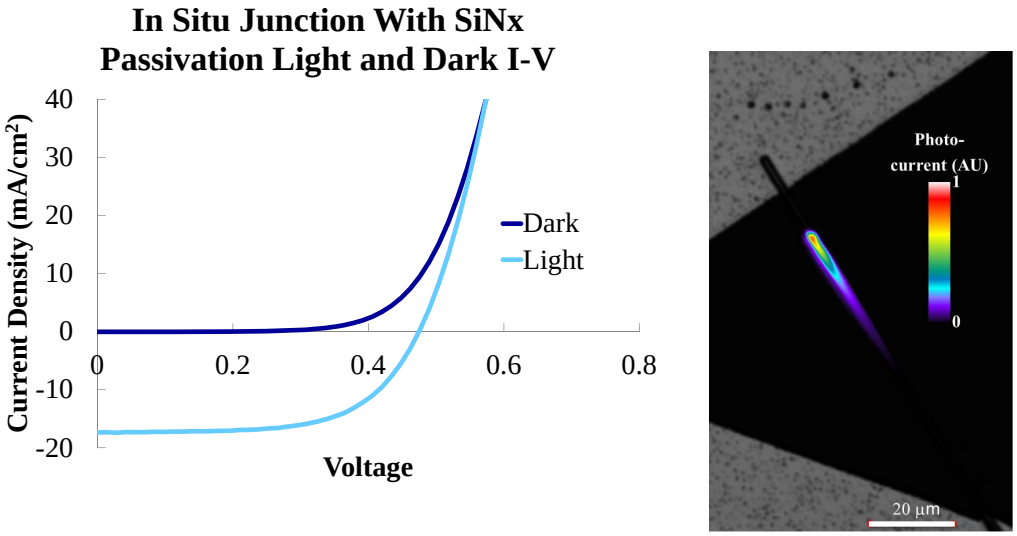


Figure 2.6: Current-voltage characteristic (left) and light beam induced current measurement (right) of a champion in situ junction device, following surface clean and etch and SiN_x passivation. Current is normalized to the exposed base region area. $V_{OC} = 475$ mV and $J_{SC} = 17.4$ mA/cm^2. Light beam induced current measurements reveal a characteristic collection length of 9.3 µm, with excellent fit to a single exponential decay ($R^2 = 0.998$).

bulk. Current-voltage and LBIC measurements of a typical sample are shown in figure 2.7. The open circuit photovoltages are consistently measureable, a significant improvement over the unpassivated devices. The champion device exhibited a photovoltage of 406 mV.

Current-voltage characteristics measured in the dark provide additional evidence that the a-Si effectively passivates the sidewall surfaces. As shown in figure 2.8, the dark current is suppressed by a-Si passivation, and actually increases in the SiN_x coated sample compared to the bare one. The sensitivity of this measurement and the ability to fit dark current parameters J_{01} and J_{02} was hampered by the small size of the device and extremely small absolute currents (picoamperes) at low bias voltages. Additionally, the a-Si passivation used here caused an increase in series resistance, as evidenced by the dark current curve becoming less linear at lower voltages. The deposition could likely be optimized, resulting in a thinner passivating film which would not provide the same series resistance, and absorb less light. Regardless of the shortcomings of the measurement, it is clear that the a-Si sample exhibited significantly reduced dark current, evidence of effective surface passivation. Thus, surface passivation alone is not sufficient to increase the current collection length in the base.

This picture of current collection increasing due to surface inversion helps to explain the results of previous work on diffusion doped wire devices with radial and axial regions [13]. In these devices, silicon nitride passivation resulted in an increase in current extracted from the axial junction region of the wire, but resulted in a lower overall voltage than amorphous silicon passivated samples. An increase in current due to passivating a recombination active surface should be accompanied by

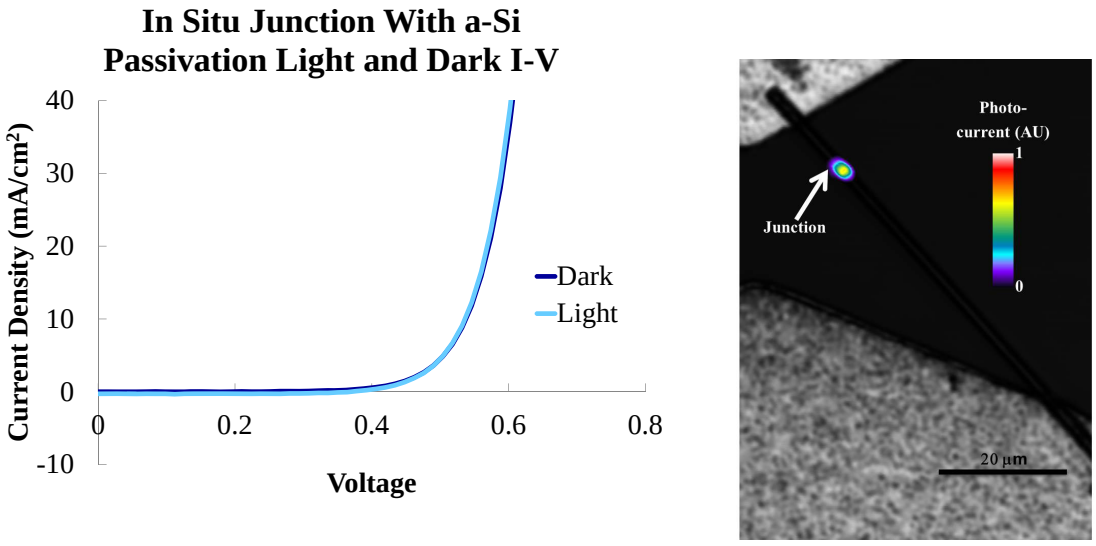


Figure 2.7: Current-voltage characteristic (left) and light beam induced current measurement (right) of a in situ junction device, following surface clean and etch and amorphous silicon passivation. Current is normalized to the exposed base region area. $V_{OC} = 370$ mV and $J_{SC} = 0.3$ mA/cm^2. Light beam induced current measurements reveal collection from only the region within approximately 1 µm from the junction.

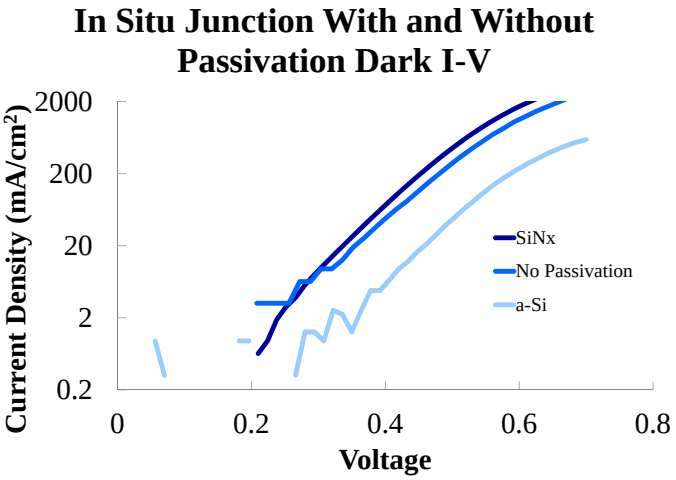


Figure 2.8: Dark I-V curves of in situ junctions. Dark currents are normalized to the axial junction area, the wire cross section. Amorphous silicon provides effective passivation, resulting in a shift in the dark current curve. The small increase in dark current in the SiN_x coated sample could result from the increased junction area induced by fixed charges in the SiN_x layer, as described.

an increase in voltage; the best explanation for the trend observed is that the improved current collection was caused by surface inversion, rather than surface passivation, and resulted in decreased voltage due to the increase in junction area in defective material.

2.4 Material Quality Measurements

One key measure of material quality is the overall effective lifetime, τ_{eff} of photogenerated minority carriers. The effective lifetime is given by $\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}} + \cdots$. In silicon, the most important contribution to τ_{bulk} is Shockley-Reed-Hall recombination, the recombination of free carriers through defect states within the band gap.

As discussed earlier, the original goal of developing an in situ junction formation process was to measure, and eventually improve, the electronic quality of as-grown silicon wires.

2.4.1 Light Beam Induced Current with Chemical Passivation

In order to assess the bulk material quality, the influence of the surface must be eliminated. While it is not a practical method for a complete solid state device, excellent surface passivation can be achieved by submerging the sample in a variety of different solutions. These include:

1. Strong acidic solutions, with the best performance from hydrofluoric acid [22]
2. Iodine in alcohol (methanol or ethanol) [23]
3. Quinhydrone in alcohol (methanol or ethanol) [24]
4. Strong basic solutions, such as 40% sodium hydroxide[25]

We attempted to apply this same principle to light beam induced current diffusion length measurements by submerging the sample in solution during measurement. The first method, passivation in acidic solutions, was deemed most appropriate. Basic solutions etch silicon, and the wires would be fully consumed after exposure to bases. Attempts were made to use the alcohol based solutions, but due to their high volatility, it was difficult to take measurements prior to the solution evaporating, even when care was taken to cover the sample. It may be possible to fully seal the sample within an alcohol containing environment to take this measurement, but instead acids were used, as in previous work in our group [13]. First, single wires were patterned and contacted as described previously. Next, a second photolithography step was used, leaving a protective coating of photoresist over the contacts and a well which allowed the acid to come in contact with the wire.

Measurements were first taken with a drop of 18 MΩ deionized water as a control. The results are shown in figure 2.9; this measurement puts an upper limit on the LBIC spot size as a Gaussian with $\sigma = 0.595\,\mu\text{m}$. In situ grown axial junction samples with different post growth processing methods

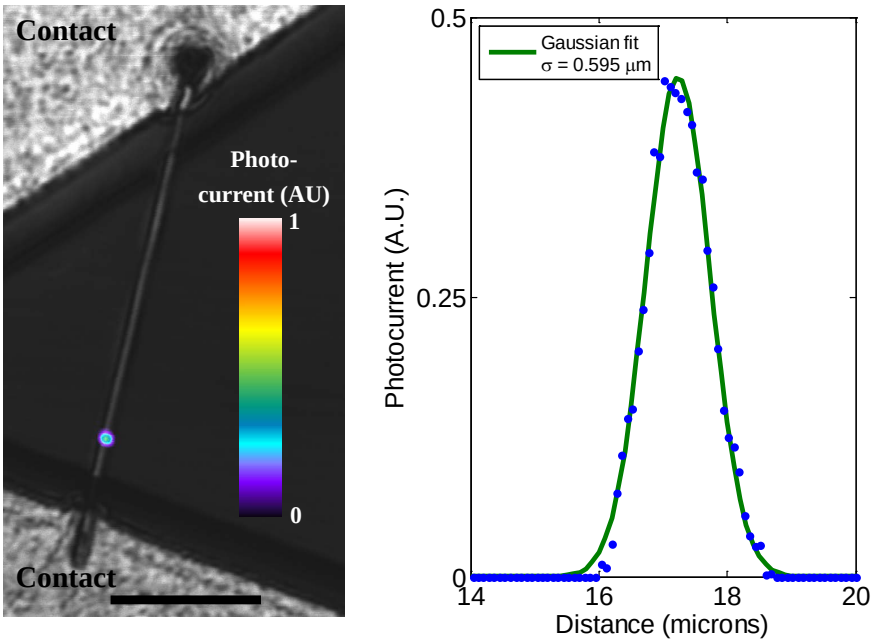


Figure 2.9: Control measurement of the sample shown in figure 2.10B, submerged in DI water. Only the junction reveals current collection, indicating a sharp axial junction with extremely short diffusion length, as expected in the sample without surface passivation. A profile of the light beam induced current measurement (right) fits a Gaussian of $\sigma = 0.595\,\mu m$ with $R^2 = 0.996$. This corresponds to an upper limit on the illumination spot size. Scale bar is 20 microns.

were measured with light beam induced current measurements using a buffered hydrofluoric acid (BHF, Buffer HF Improved, Transene) surface treatment. The results, as shown in figure 2.10, show current collection throughout the base of the wire on the samples which has a post-growth oxidation step. This data was initially interpreted as an improved diffusion length after post-growth oxidation. However, upon further analysis, it became clear that as in the case of silicon nitride passivation, the hydrofluoric acid was causing the outer surface of the wire to become inverted and form an induced radial current collection path.

The most convincing piece of evidence in support of the hydrofluoric acid inverting the surface is the lack of diffusion towards recombination active surfaces. This can be seen clearly in samples which had a large gap between the contact and liquid passivation, as shown in figure 2.10 C. The unpassivated region between the contact and the well of BHF exhibits high surface recombination, and no current is extracted from this region, as evidenced by the dark LBIC measurement. If the remainder of the device was exhibiting good passivation and an axial junction, we would expect a decay in the LBIC profile in this device. This is because a carrier generated in the center of the active region of this device should have an equal probability of diffusing to either the recombination active area or the axial p-n junction. Assuming the lifetime of the carriers is long enough to result

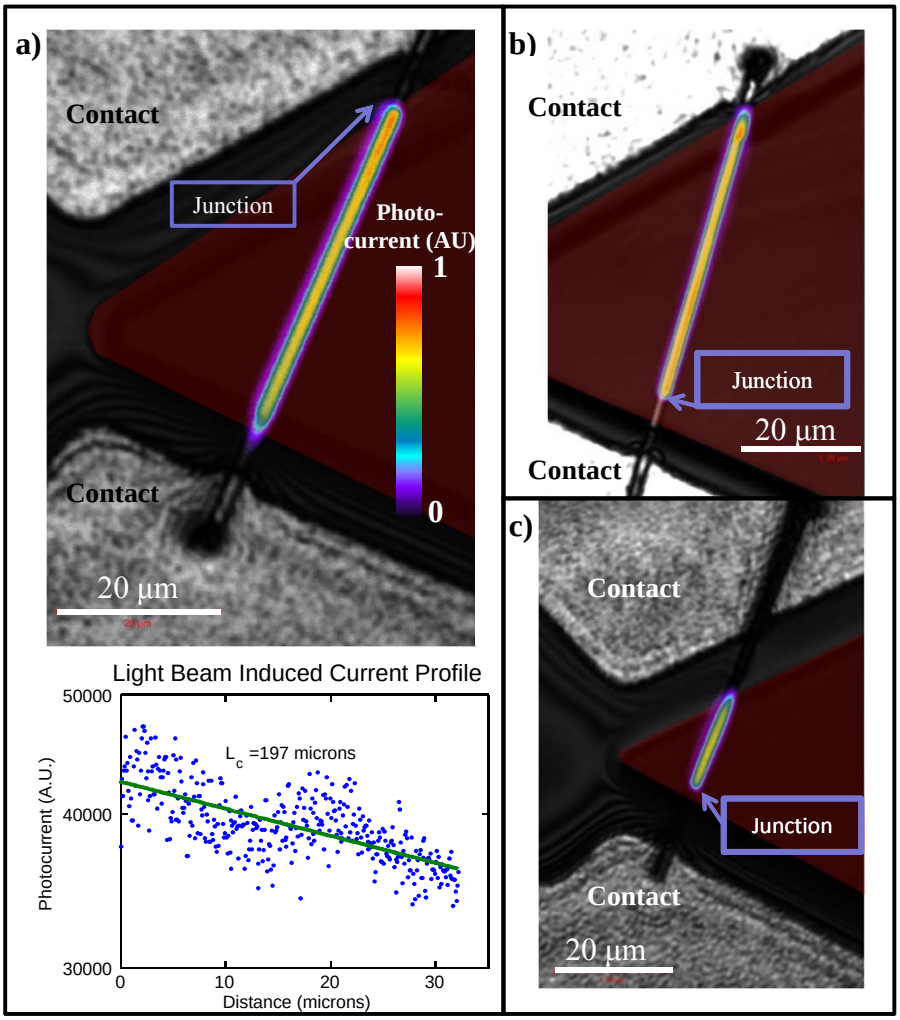


Figure 2.10: Light beam induced current measurements in false color overlaid on optical images of wires with axial junctions submerged in buffered hydrofluoric acid (BHF). The photoresist well which cotains the HF is highlighted in red. Below sample A is a line scan of the photocurrent, showing little decay and a high apparent diffusion length. Sample B again clearly shows a long diffusion length in the base and short in the emitter, even when submerged in BHF. Sample C shows an extremely fast decay of photocurrent outside the well containing BHF, which strongly suggests that the BHF is inverting the surface inducing a radial junction.

in a diffusion length that is longer than the length of the wire, this situation can be modeled as a one-dimensional random walk. Carriers which reach the recombination active region will be lost, and the ones which reach the junction collected. For the ideal case with a long lifetime, the result will be a LBIC profile linearly decaying between a maximum at the junction and zero by the recombination active region. As the diffusion length reduces to the order of the length of the wire, the linear decay profile will be convoluted with an exponential decay with characteristic length of the diffusion length. In order to achieve constant collection from all regions of the device, the entire base would need to have excellent passivation for minority carriers, including the region around the back contact.

Neither a linear nor exponential decay across the length of the wire was observed, as shown in figure 2.10. Instead, collection is relatively constant throughout the length of the wire, and rapidly decaying away from the region where the wire surface is no longer in contact with hydrofluoric acid. This implies that the surface must be inverted, providing a second path for carrier separation and extraction in the radial direction.

2.4.2 Lifetime Measurements

2.4.2.1 Motivation

Lifetimes were measured directly in order to corroborate the diffusion length measurements. The two quantities are related by:

$$L = \sqrt{D\tau_{eff}}$$

where D is the minority carrier diffusivity, related to the mobility μ by the Einstein relation:

$$D = \frac{\mu k_B T}{q}$$

The maximum attainable value for the electron diffusivity D_e is approximately $36.5\,\mathrm{cm^2\,s^{-1}}$, corresponding to an electron mobility μ_e of $1400\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. In order to obtain a diffusion length of 197 µm, as extracted from the measurement in figure 2.10 A, at minimum, τ_{eff} would need to be greater than 10 µs. This requirement becomes even stricter in doped or otherwise defective silicon material, where the mobility, and therefore diffusivity, is reduced. A realistic upper bound considering the base doping of our silicon wire material of $1-5\times10^{17}$ $\mathrm{cm^{-3}}$ is likely closer to 20 µs, assuming $\mu_e = 700\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and $D_e = 18\,\mathrm{cm^2\,s^{-1}}$. That is, in order for the measured light beam induced current decay to correspond to a diffusion length rather than surface inversion, the minority carrier lifetime in the wire must be longer than 20 µs.

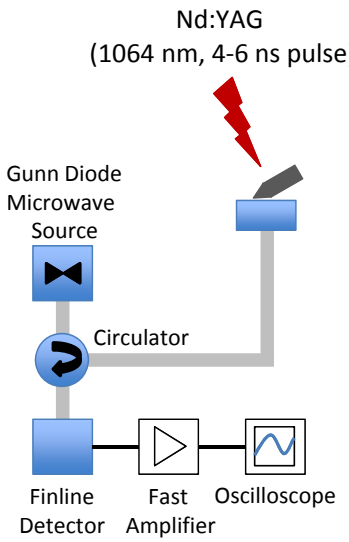


Figure 2.11: Schematic of microwave detected photoconductivity decay setup.

2.4.2.2 Measurement

Lifetime measurements on silicon wires were performed using a home built microwave detected photoconductivity tool. The illumination source is a Nd:YAG laser which provides a 30-240 µJ, 3 mm diameter, 4 ns pulse. A schematic of the measurement apparatus is shown in figure 2.11. Lifetimes of uncleaned, unpassivated vapor-liquid-solid grown wires as low as 20 ns were measured, proving the minimum measureable lifetime was quite low.

It is normally most informative to measure the lifetime at different, known minority carrier densities, but it is difficult to know the exact minority carrier density in this configuration. Some light will scatter or be absorbed in the centrifuge tube and liquid passivation. Also, while 1064 nm light is absorbed only weakly in silicon, and we can assume that the generation will be uniform in a wafer, these wires have the potential to form large clumps where the beam will be significantly attenuated, causing a distribution of injection levels inside the wires. Neglecting these attenuating effects, the maximum injection level excited by the 30-240 µJ pulse ranges from 5.4×10^{16} to $4.3 \times 10^{17}\,\mathrm{cm}^{-3}$; we expect the actual excess carrier density of this measurement to be somewhat lower, but likely within an order of magnitude of these values.

One reason that it is important to know the injection level of the measurement is to get information about the recombination mechanism. An idealized plot of lifetime as a function of injection level for a silicon device is shown in figure 2.12 [26]. While the exact density is not known, the recombination mechanism can be predicted by considering the trend in lifetime as a function of laser intensity. All measurements on VLS wires showed either a flat or an increasing trend, characteristic

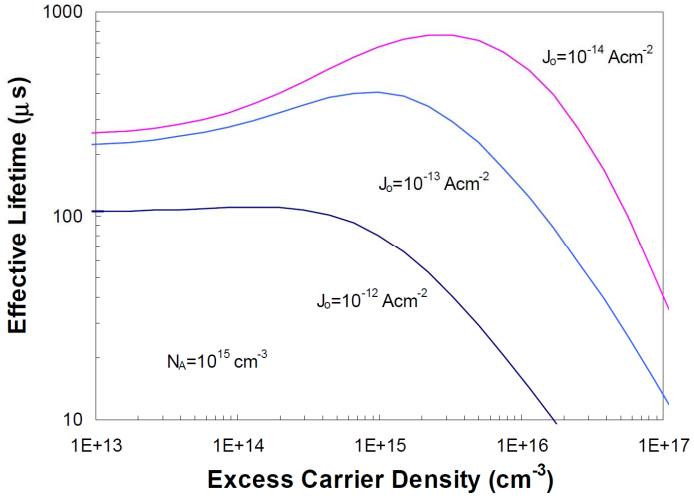


Figure 2.12: Typical curve of lifetime as a function of carrier injection level due to a combination of physical mechanisms: SRH, Auger, and emitter recombination. The increase in lifetime is caused by the transition to high level injection SRH statistics and the strong decrease at high injection levels is caused by Auger recombination. From [26].

of Shockley-Reed-Hall recombination, or the transition from low to high level injection, respectively. Had the lifetime been limited by Auger recombination, the lifetime would decrease with increasing injection. This recombination regime likely corresponds to the injection levels most relevant to flat plate (non-concentrating) photovoltaic devices, and thus, the lifetime extracted can be considered a relevant lifetime governing device operation.

2.4.2.3 Results

The lifetime of undoped wires grown prior to and cleaned with the same process as the axial junction wires shown in figure 2.10 was measured. Intrinsic silicon has a larger change in conductivity under illumination than doped material, and therefore provides significantly more microwave photoconductivity decay signal, which is important to be able to measure microwires. The lifetimes measured are considered an upper bound for the devices made with doped material. Champion lifetimes, measured at a laser intensity of 60 µJ per pulse, were 250 ns with BHF passivation and 430 ns under 6 M hydrochloric acid. There are several possible reasons for the higher lifetime provided by HCl passivation, including improved wetting of the wire surface (hydrofluoric acid renders the silicon surface hydrophobic), and the potential for hydrochloric acid to clean any remaining metal impurities from the wire surface. Still, the highest lifetimes measured were far below the 10-20 µs required to

obtain a diffusion length of 197 µm. Assuming the same upper bound on D_e of $18\,\mathrm{cm}^2\,\mathrm{s}^{-1}$ for the doped base, this corresponds to an upper bound on diffusion length of 27 µm, significantly shorter than the measured collection length, again implying that the collection must be governed by radial collection through an inverted surface.

2.4.3 Summary and Discussion

In summary, these wires present many challenges in both measuring and achieving high material quality. While they present a unique opportunity to visually measure the collection length directly through light beam induced current measurements, great care must be taken to ensure that the surface is not inverted, and the measurement corresponds to the actual diffusion length. The best way to do this is to use a dielectric passivation with known fixed charge of opposite sign of the doping in the base region, such as silicon nitride for n-base devices or alumina for p-base devices. Unfortunately, the arrival of our atomic layer deposition tool and achievement of good passivation with ALD alumina on silicon wafers coincided with a long period of downtime for the wire growth reactor. Additionally, lifetime measurements with acid passivation provide compelling evidence that the bulk material quality of the VLS grown wires is poor, and diffusion lengths will be short; these lifetime measurements may be a more reliable way to assess material quality in the future.

2.5 High and Low Temperature Growth

The vapor-liquid-solid growth process is a relatively complicated, with several steps which could be affected by temperature. Early work studying VLS growth of various semiconductor materials breaks the process down into four basic steps [27]:

1. transport of precursors in the gas phase to the liquid interface
2. chemical reactions at the liquid catalyst interface and subsequent intake of silicon into the liquid
3. transport of silicon through the liquid to the liquid/solid interface
4. crystallization of silicon from the supersaturated liquid at solid interface

It is fairly easy to rule out steps 1 and 3 as rate limiting steps by observing the effect of changing precursor concentration in the tube and the growth rates of different diameter wires, with different catalyst height. However, there is less convincing evidence for or against steps 2 and 4, and it is possible that both can play a role in determining the growth rate [28].

Aside from determining the rate of one or more activated steps of the growth process, temperature plays an important role in two additional steps. The first is the temperature required for liquid

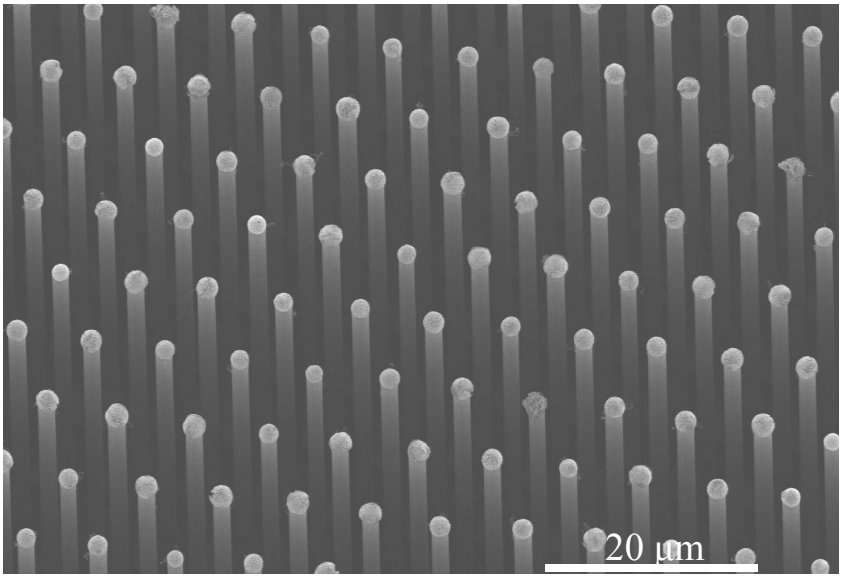


Figure 2.13: High fidelity silicon wire growth performed at 900 °C

catalyst particle formation. The catalyst is generally either a liquid metal alloy or silicide [28], and formed by annealing a metal which has been deposited on the growth substrate. The second is in determining the rate of competing processes and chemical reactions, such as sidewall growth and etching and catalyst evaporation. Our typical copper catalyzed silicon wire growth process is most successful in a relatively narrow temperature range around 1000 °C [9], and it turned out that these second processes have the greatest influence in determining the optimal growth temperature.

2.5.1 Low Temperature Growth

The original goal for attempting silicon wire growths at temperatures below 1000 °C was to attain higher germanium content in SiGe alloy microwires, as discussed in the following chapter. However, there are several reasons that reduced growth temperature is desirable in a silicon process. First, while fully optimizing the cost of a commercial process will require more careful analysis, a reduced growth temperature has the potential to consume less energy during the growth process. Second, equilibrium impurity concentration generally increases exponentially as a function of temperature, and it is possible that growths at a lower temperature will end up with higher material quality.

As discussed by Kayes et al. [9], copper catalyzed silicon growths were of low quality below 950 °C, including kinks and disoriented growth. It was found that high quality growth could be achieved at 900 °C by first annealing the sample at 1000 °C under hydrogen for 5 minutes, then ramping

down to 900 °C over 15 minutes before initiating growth. An image from such a growth is shown in figure 2.13. Similar improvements were made to growth of germanium wires on silicon substrates by Dan Turner-Evans. This provides evidence that the catalyst formation step was preventing high quality growth at temperatures below 950 °C. The cause of this is not immediately obvious; copper and silicon form a eutectic at 802 °C [29], and increasing the temperature of a copper particle in the presence of a large supply of silicon is not expected to cause a phase transition, but simply an increase in the solubility of silicon within the liquid phase. Initial investigation with EDS showed incorporation of oxygen into the catalyst particle prior to growth, suggesting that the composition may be more complicated than the Cu-Si phase diagram suggests. Further work would be required to determine the mechanism that this annealing step plays in the formation of the catalyst particle.

2.5.2 High Temperature Growth

After observing wires which were tapered to a point on the edge of certain low quality silicon wire growths, attempts were made to reproduce the conditions that led to this type of growth. Tapered wires are desirable because they have inherent anti-reflective properties by presenting a gradual change in the index from air to silicon [30], as well as a potential for increased light trapping near the band-edge by changing the mode profile at different points within the wire [31]. It was found that increasing the growth temperature was an effective way to grow tapered wires.

Various growths performed at 1050 °C are shown in figure 2.14. The mechanism for tapering is most likely the removal of the catalyst particle during growth, rather than sidewall deposition, as seen in other nanowire systems [32]. A wire tapered almost to a complete point, with a small catalyst particle with size very similar to the diameter at the top of the wire remaining, is shown in figure 2.14 D. Additionally, the base diameter does not increase in these tapered wires. It is not clear if the catalyst removal is due to evaporation, etching of the catalyst by the chloride species present during growth, or migration of the catalyst particle away from the tip by some other mechanism.

Wires tapered by this method develop step-like faceting as the wire tapers, as shown in figure 2.14 B. The likely cause of this is the energy difference between the relaxation of the catalyst to its preferred shape and the creation of an additional silicon surface. That is, under normal conditions, growth resulting in vertical sidewalls is stable with a preferred liquid-solid contact angle between the catalyst particle and the top surface of the wire, which dictates both the wire diameter and the shape of the catalyst particle [33]. As material is removed from the catalyst, instead of the wire diameter immediately changing, the shape of the catalyst particle changes until there is sufficient energetic driving force to create a new horizontal surface while relaxing the catalyst. This results in step-like tapering of the wire, rather than gradual tapering.

Initial optical characterization of these samples was inconclusive due to the difficulty in controlling the volume of silicon and with polymer infill uniformity. However, the anti-reflective properties of

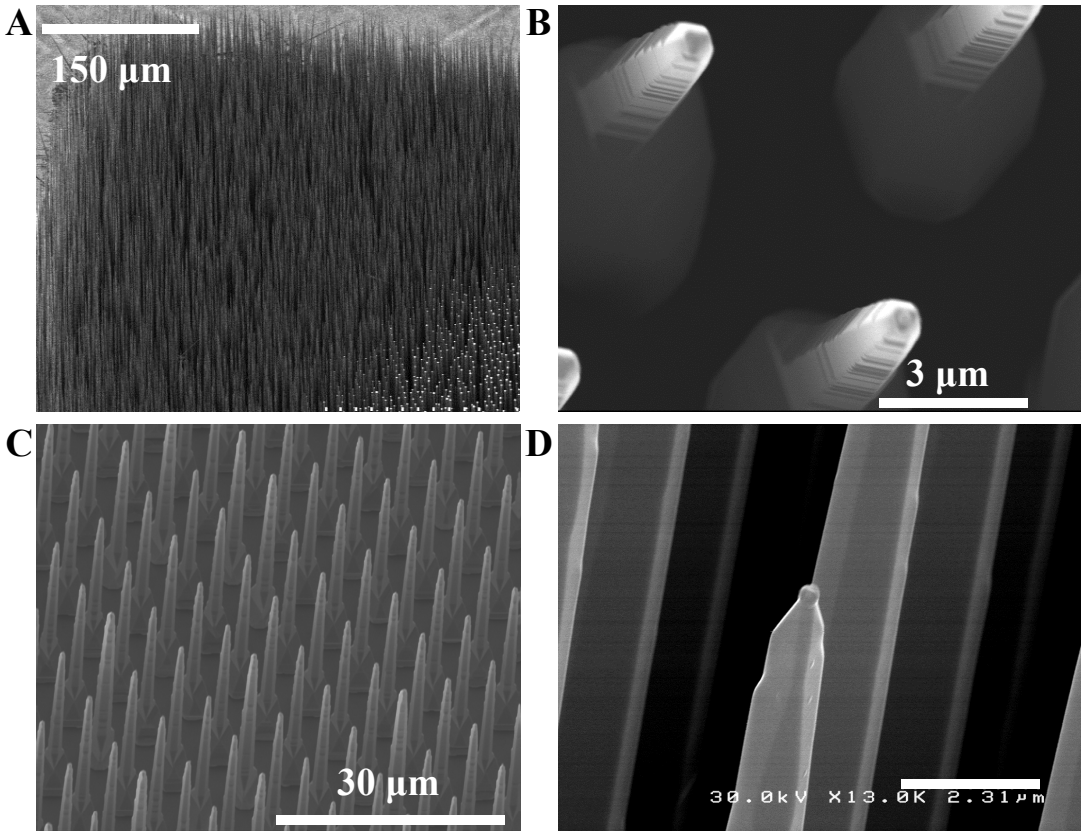


Figure 2.14: Various tapered silicon wire growths. A: Corner of a low quality silicon wire growth performed at 1000 °C, showing unintentionally tapered wires. The light spots in the bottom right of the image are wires which are not fully tapered to a point, with some catalyst particle remaining and appearing bright. B-D: High fidelity tapered wires grown at 1050 °C.

as-grown on substrate spikes are readily apparent by simply observing samples with spikes at the edges; regions with spikes appear significantly blacker than regions with straight wires. Further measurements of these VLS grown tapered wires, including measurements after incorporating the anti-reflective coating and scattering particles, were not performed.

2.6 Conclusions and Outlook

Several new aspects of silicon wire growth were studied, namely in situ n-type doping using phosphine, in situ junction formation, electronic quality of the resulting material, and the effects of temperature on growth. When care was taken to avoid misinterpreting an inverted surface, diffusion length and lifetime measurements indicate that the as-growth material quality of these wires is relatively poor. The work presented here helps to better understand the capabilities and limitations of VLS grown silicon wires, with strong implications in the commercialization of this technology. However, as noted in the introduction, this technology is currently significantly less attractive than when the project began. We now turn our attention to designs with the potential to reach high efficiency, both by using materials other than silicon, and by using a silicon-based process with higher electronic quality material.

Chapter 3

Silicon Germanium Alloy Microwires

3.1 Introduction

After successfully developing silicon wire growth processes and processing techniques to form photovoltaic devices, we wished to explore similar structures which could obtain higher efficiencies or improved photoelectrochemical performance. Growth of silicon germanium alloy wires, which could be used as a lattice-matched substrate for III-V growth, was desirable for these reasons.

First, high efficiency devices can be achieved by using tandem designs, which use additional materials to extract more voltage from higher energy photons. These architectures are most often realized by growing epitaxial stacks of III-V materials on a lattice matched substrate. By varying the dimensions of the SiGe wire and III-V layer independently, these wires present the opportunity to operate in current matched conditions in several geometries, including conformal growth of a III-V shell on the wire core and selective growth of a spherical or hemispherical III-V region at the tip [34]. These particular two junction devices achieve a maximum theoretical and simulated efficiency of 40% and 35%, respectively, using a wire composition of $Si_{0.1}Ge_{0.9}$.

A second application of interest for these wires is use in photoelectrochemical water splitting devices. The high surface area of microwires allows the integration of catalyst particles without shading a significant portion of the front surface [35].Silicon microwires alone will not provide enough voltage for this application; water splitting requires an operating voltage in excess of 1.7 V [36], which necessitates the use of a tandem device in order to achieve this reaction potential plus over potential. In these devices, total conversion efficiency is less important than reaching that threshold voltage — below that voltage, the device will not operate at all. Silicon germanium wires, which allow variation of lattice constant, enable the growth of high quality, lattice matched tandem devices which output voltage sufficient for the water splitting reaction.

In addition to forming a potential substrate for lattice matched growth, there is a potential

to also grow non-lattice matched materials on SiGe wires. It has been shown that high aspect ratio structures, such as wires, have the ability to grow out defects laterally [16]. By changing the composition of the high aspect ratio structure, epitaxial layers of different compositions can be grown on top. This strategy can be used to either integrate III-V materials with silicon devices, or simply as an inexpensive growth substrate for III-V devices. Still, additional Ge content in these wires, shifting the lattice constant towards the target, could only be beneficial in achieving the goal of low defect growth by reducing the density of defects which must be grown out laterally.

A majority of the existing work on SiGe wire growth has been focused on vapor liquid solid growth of nanowires using silane and germane precursors with Au catalysts at low pressures [37] [38] [39] and full compositional control has been demonstrated [38] in these growth systems. Much of the existing work has resulted in forests of wires with various sizes and orientations. In contrast to this, atmospheric pressure Cu-catalyzed vapor-liquid-solid growth of silicon wires with tetrachlorosilane has been shown to generate vertically aligned, monodisperse arrays of microwires with micron scale diameters and heights [9]. Aside from allowing for the growth of well patterned, high fidelity arrays by etching non-catalyzed growth [40], chlorinated precursors offer several other advantages when used in chemical vapor deposition growth compared to their hydride counterparts. Chlorosilane based growth results in a very high growth rate [9] [41] compared to silane [42]. Finally, chloride based precursors are safer than hydrides, due to their lower toxicity and flammability [43].

We explored atmospheric pressure, Cu-catalyzed, vapor-liquid-solid growth of SiGe alloy microwire arrays using chlorosilane and chlorogermane precursors. Similar to Si wire arrays, the SiGe alloy microwire arrays can be grown over 1 cm^2 areas with excellent adherence to the patterned oxide template on Si (111) substrates. To the best of our knowledge, this is the first report of Cu-catalyzed vapor-liquid-solid growth of these alloys with chloride precursors. An increase in the Ge precursor flow led to an expected increase in Ge content and an unexpected reduction of the growth rate. Germanium incorporation in the wires was limited to approximately 12%.

3.2 Growth

3.2.1 Reactor Modifications

Growths were performed in the "Big Blue" reactor which has previously been used for growth of silicon microwires in our group. Several modifications were performed prior to the growth of SiGe alloy wires in order to improve the reproducibility, ease, and safety of reactor operation. The previous configuration of the reactor was entirely manually controlled, including manually actuated valves and a three zone furnace which supported only front panel operation. The modifications included installing pneumatically controlled valves, temperature controllers and pressure gauges with communications interfaces, and connecting them, along with the mass flow controllers, to a

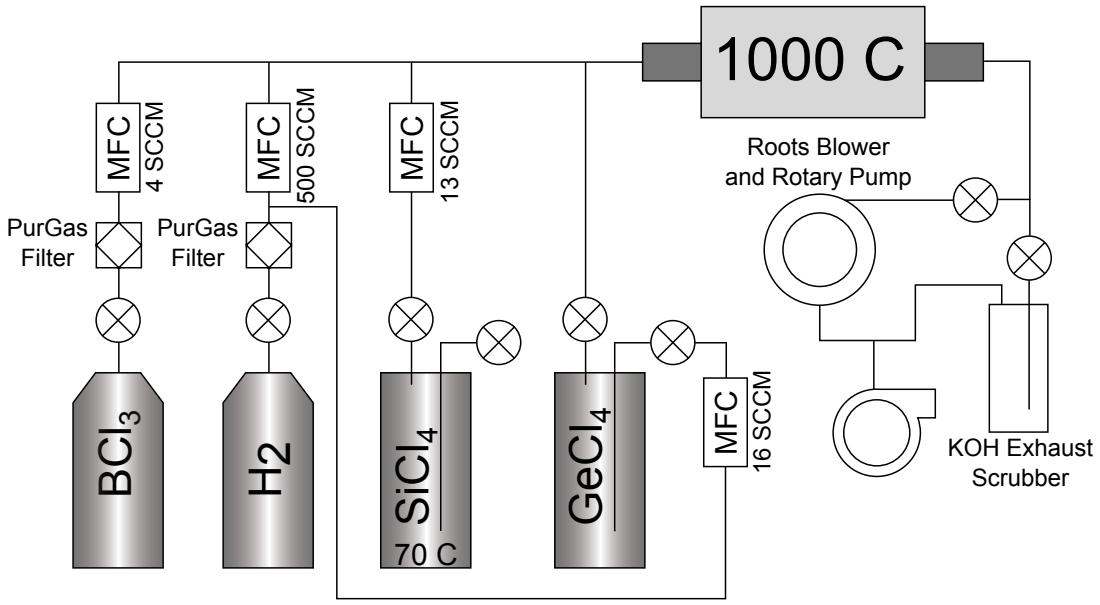


Figure 3.1: Schematic of the wire growth CVD reactor, with typical growth parameters shown.

computer with a LabView interface.

There were several advantages to the new configuration. First, growths could be performed with minimal operator input, increasing total throughput. Second, the timing of flow control and temperature ramps was improved, allowing for improved reproducibility between growths. Finally, this configuration allowed the incorporation of interlocks to prevent potential (and previously occurring) user errors, such as sucking potassium hydroxide from the exhaust scrubber into the vacuum pump, or running the process without sealing the reactor.

Following the modifications, we experimented with bubbling both the $SiCl_4$ and $GeCl_4$ sources. After difficulty obtaining good silicon growths, we switched back to evaporating the $SiCl_4$, as the reactor had previously been configured. It seems unlikely that the bubbling of the precursor was the cause of the poor growth, but more likely that some contamination was being introduced in one of the lines upstream from the $SiCl_4$ bubbler. A similar reactor in Lewis group labs has bubbled $SiCl_4$ with both helium and hydrogen with good results. The $GeCl_4$ source remained bubbled with H_2, as shown in figure 3.1. The most successful modification in improving growth quality was the addition of Nanochem PuriFilter gas purification filters on the hydrogen and dopant gas lines, which effectively removed oxygen and water vapor from the source gasses. The same filters were added to the Lewis group reactor with similar success.

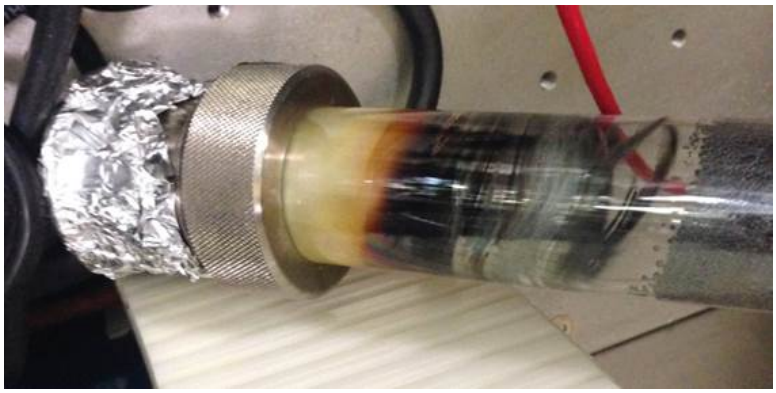


Figure 3.2: Picture of SiGe growth tube, showing germanium species present on the upstream cold zone of the tube (to the left of the clear section).

3.2.2 SiGe Growths

High Purity (6N, Alfa Aesar) Cu-catalyst patterned Si (111) substrates were prepared with standard photolithographic liftoff processes, as in our silicon wire growth process described earlier. Substrates were cleaved to 1 cm^2 pieces and loaded onto a boat in our atmospheric pressure hot wall chemical vapor deposition reactor at 750 °C. Typical growth parameters include 1 slm of H_2 carrier gas, bubbled H_2 carrier gas through a nominally 32 °C $GeCl_4$ cylinder, and collection of the overpressure from a $SiCl_4$ cylinder heated to 85 °C at a growth temperature of 1000 °C. We used molar flow rates of 0-98 µmol min^{-1} $GeCl_4$, 430 µmol min^{-1} $SiCl_4$, and 4 $\times 10^4$ µmol min^{-1} H_2. After growth, samples were cooled slowly to 750 °C inside the tube before removal.

Consistent with the work of Soman et al. on thin film growth [44], contamination from adventitious Ge species, likely chlorides and oxides of germanium, on reactor surfaces makes reproducibility more challenging than for pure silicon growth. In our case contamination resulted in growth of disordered nano- and microwire forests instead of vertical microwires. These species appeared as white and yellow to light brown regions on the tube sidewalls, including the cold zones of the tube, as shown in figure 3.2. This contrasts with pure silicon growths, in which no deposition was observed in cold zones and only clean, black silicon deposition occurred on the hot sidewalls of the tube. Improved reproducibility was achieved by alternating SiGe wire growths with pure Si growth, in effect keeping the reactor in a steady state. Still, in order to maintain growth quality, it was necessary to change the growth tube more often than is necessary with pure silicon growths. Evidence of the contamination appears when unloading and loading the sample; the compounds on the sidewalls released a vapor when exposed to air. Germanium has a complex series of chlorides, oxides, and hydroxides that can form. It is likely that some of the negative effects of the growth are a result of chlorides forming hydroxides and oxides when exposed to air, and releasing oxygen or water vapor into the growth tube when heated during the reaction. It may be possible to fully oxidize these species, rendering them inert and avoiding the need to replace the tube; however, the

growth process is extremely sensitive to oxygen contamination, so this was not attempted.

3.3 Characterization and Discussion

3.3.1 Compositional

Compositions of wires were measured using an FEI Nova 200 SEM with Ametek EDAX Genesis 7000 and a Sapphire energy dispersive spectroscopy (EDS) detector. This allowed for rapid measurement with spatial resolution on the order of the diameter of the wire. As expected, the Ge content of the wire arrays increases with increasing Ge flow. The calculated gas phase composition was always greater than that of the resulting wire array. Possible causes of this are:

1. higher activity of chlorogermane compared to chlorosilane on the tube sidewalls, resulting in a lower gas phase ratio at the sample than in the upstream gas mix.

2. the chlorogermane cracks and incorporates less efficiently at the copper catalyst particle.

3. silicon crystalizes from the supersaturated catalyst melt more efficiently, resulting in increasing Ge concentration in the catalyst.

The composition of the catalyst particle showed significantly higher germanium content. For example, in a sample with gas phase molar ratio of [Ge]/[IV] = 18.6% and solid phase composition of 13%$_{at}$ Ge, the EDS of the catalyst particle revealed a solid phase composition with [Ge]/[IV] = 36%. There are several possible explanations for this. Examination of the Cu-Si and Cu-Ge phase diagrams reveals a large difference in eutectic temperature (802 °C vs 640 °C) and a small difference in the solubility of Si and Ge in liquid Cu (31% vs. 36%), both of which could play a role in the Ge enrichment of the Cu catalyst and the reduction in growth rate discussed in the next section. The Ge enrichment of the catalyst could be due to a smaller driving force for nucleation of Ge-rich versus Si-rich alloys. It is more energetically favorable for Ge to remain as a liquid in the catalyst particle, rather than to crystallize. Furthermore, at growth temperatures, the liquid catalyst droplet is saturated with Si before precursors are introduced because it is in direct contact with the Si substrate, which favors initial Si-rich supersaturation. Reducing the $SiCl_4$ flow rate while keeping the $GeCl_4$ flow rate constant did not result in higher compositional content. Once growth begins, the strain energy of nucleating alloy material with increased Ge content may play a key role in preventing higher Ge incorporation as the size of the wires leads to their strain relief behavior being more bulk-like. This would explain the Ge enrichment of the catalyst compared to the growing solid wire material.

Finally, while the catalyst showed increasing germanium content, the composition of the wires appeared to be uniform throughout the full length. If the germanium concentration in the catalyst

was increasing during growth, we would expect the germanium content of the wire to increase as well. Therefore, it is likely not this effect alone that caused suppression of the germanium content compared to the gas phase concentration, but there was likely some interplay between other processes which resulted in a steady state at different catalyst and crystalline material compositions.

Composition measurements were confirmed by Chris Chen using both x-ray diffraction and EDS in a transmission electron microscope (TEM). The enhanced germanium content in the catalyst measured by EDS in the SEM appeared as a separate phase in the TEM images, which likely crystalized while cooling the supersaturated catalyst after growth. Regions were measured with compositions of $Si_{0.43}Ge_{0.57}$ and $Si_{0.22}Ge_{0.78}$.

3.3.2 Morphology and Growth Rate

Figure 3.3 depicts the morphology of $Si_{1-x}Ge_x$ wires with increasing $GeCl_4$ flow as the flow of $SiCl_4$ was held constant. At low $GeCl_4$ flow rates, the wire arrays appear to be largely identical to their Si counterparts, but, as this rate is increased, the morphology of the wires gradually changes from vertical to heavily tapered and faceted sidewalls. The growth rate also changes dramatically, falling from $7\,\mu m\,min^{-1}$ to $1\,\mu m\,min^{-1}$ as the Ge molar flow fraction was increased to 18.6%. Attempts to grow with a gas phase Ge molar fraction of 25.7% resulted in little to no growth.

The cause of the sidewall faceting and tapering is likely the same as observed in silicon wire growth at elevated temperatures, as explored in section 2.5.2. In this case, it is likely that increased etching of the copper catalyst particle is caused by the presence of additional chloride species from the chlorogermane precursor, rather than the elevated temperatures. Still, this results in the same stepped taper structure. Additionally, since the tapering angle is a function of both the catalyst removal rate and the vertical wire growth rate, the reduction in growth rate will cause an increase in tapering even at the same catalyst removal rate. A similar effect is likely responsible for the wide wire bases, due to the difference in the surface energy between the catalyst particle and the SiO_2 growth mask during initiation compared to the vapor environment during growth. We also attempted growths at 950 °C, after annealing at 1000 °C. These low temperature growths resulted in a large increase in disordered growth, so we could not fairly compare its effects on the wire sidewall morphology. We attribute the disordered growth to decreased HCl sidewall etching; while we were able to grow high quality silicon wires at this temperature, the SiGe growths were generally more difficult to grow, either due to increased sensitivity to contamination or additional sources of contamination, as described earlier. Attempts by Dan Turner-Evans to grow pure Ge microwire arrays with Cu catalysts at lower temperatures (800 °C) resulted in similarly disordered growths [45].

Despite the reduced growth rate and tapering, $Si_{0.88}Ge_{0.12}$ wires reached lengths of over 60 µm. After incorporating an anti-reflective coating, scattering particles, and back reflector, this should

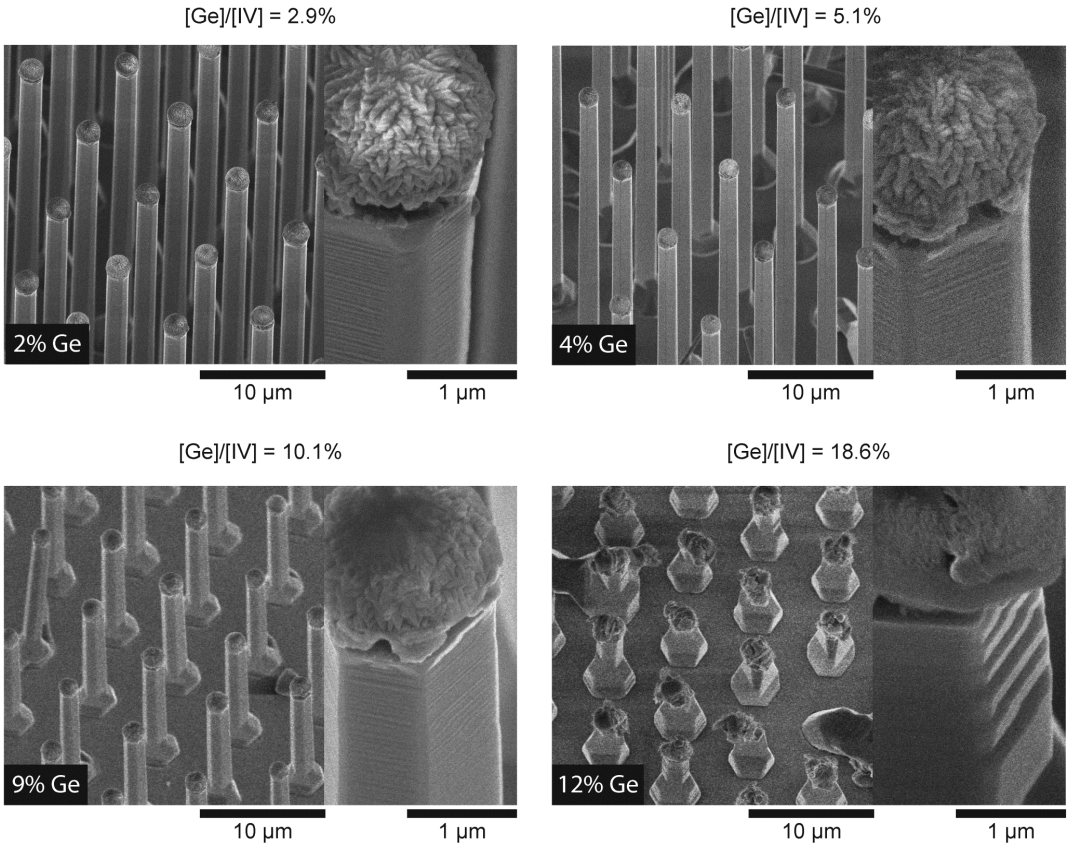


Figure 3.3: Scanning electron micrographs of $Si_{1-x}Ge_x$ wire arrays grown with increasing GeCl4 flow rates and constant SiCl4 flow for 10 minutes. The growth rate drops from 7 µm min^{-1} to 1 µm min^{-1} as the gas phase [Ge]/[IV] ratio is increased from 2.9% to 18.6 %. Large sidewall facets are introduced gradually as the [Ge]/[IV] ratio increases until they dominate the sidewall morphology at [Ge]/[IV] = 18.6%.

be sufficient to absorb as much light as a wafer based cell [11]. It should be possible to reach even longer lengths by depositing a larger copper catalyst particle.

3.3.3 Doping

Four point measurements were made on single wires using the method commonly used to measure the doping in silicon wires. Wires were removed from the growth substrate with a razor blade, suspended in isopropyl alcohol, and spun onto a silicon nitride coated wafer. Individual wires were then patterned using a Suss MA6 mask aligner, Shipley 1813 photoresist, and Microchem LOR10A liftoff resist. Patterned substrates were metalized in an electron beam evaporator with two depositions of approximately 500nm each, with the sample tilted at 45 degrees and rotated in

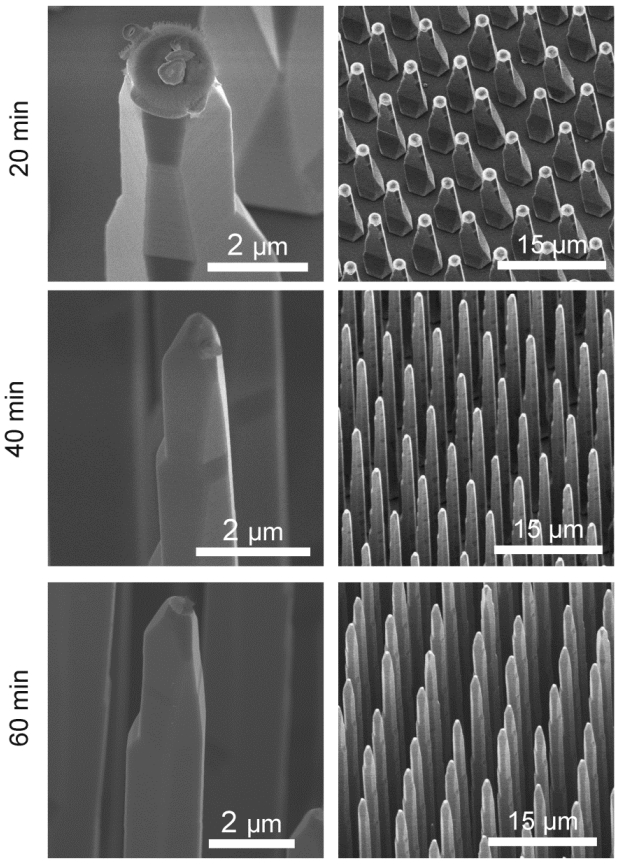


Figure 3.4: Wire arrays grown at [Ge]/[IV] = 18.6% for an extended period of time as imaged with scanning electron microscopy. The wires have a highly faceted, tapered morphology that persists for over long growth times with minimal catalyst volume left after longer growth times.

between depositions. Several metals were used, including 400 nm of Al followed by 100 nm of Ag, and 100 nm Au followed by 400 nm Ti. The yield for contacting $Si_{0.9}Ge_{0.1}$ wires with this method was extremely low; the slow growth rate and high degree of tapering made contacting both the thick base and the tip very difficult.

Four point measurements were performed on wires from a sample with approximately 10% Ge content, doped in-situ with a 4 sccm flow of 0.25% BCl_3 diluted in H_2. This dopant flow yields a resistivity of 0.1 Ω-cm in pure silicon wires. Measurements on this sample yielded a resistivity of 18.7 +/- 4.3 Ω-cm, implying a lower level of doping than for growth of pure silicon microwires.

Aside from electronic doping, we anecdotally observe a higher growth rate and less non-vertical growth while adding BCl_3 to pure silicon wire growths. This could be a result of either additional chlorine species in the gas mix etching spurious growth or boron aiding the catalytic action of the copper silicide catalyst. We did not observe these effects when comparing undoped and doped SiGe growths. Either explanation could still be valid; the SiGe grows already have more HCl in the gas mix, so adding more may not have as much impact. Also, as mentioned above, the composition of the catalyst particle is different, and the addition of boron may not change the activity of the germanium rich catalyst.

3.3.4 Optical

Due to the lower bandgap of germanium (0.66 eV), we expect SiGe alloys to have a narrower bandgap than pure silicon. According to the data tabulated by Humlicek, we expect a shift in the bandgap of approximately 40 meV for 10% Ge wires [46]. We performed transmission measurements on clumps of Si and $Si_{0.9}Ge_{0.1}$ microwires in an attempt to measure the badgap shift. These samples were prepared by scraping wires off the growth substrate and sandwiching them between two glass cover slips with Crystalbond wax. Transmission measurements were made using both the UV-Vis-IR spectrophotometer with integrating sphere located in the MMRC labs and the SARP setup in Watson 247. However, several factors made it difficult to extract the absorption coefficient, which is required to extrapolate the band gap from these measurements. First, non-uniformities of these clumps of wires made it impossible to define a particular thickness of material. Additionally, we expect the absorption in the near IR region to be enhanced by scattering between the wires, whether they are arranged in clumps or peeled off in periodic arrays [47]. Finally, wave optical effects may provide additional absorption enhancement near the band edge [11] [48], leading to even higher uncertainty in calculating the absorption coefficient in these materials.

Photoconductivity measurements were performed on single wire samples in another attempt to measure the optical band gap. While the wave optical enhancement of these wires may still be present, the amount of material is held constant between measurements. An SEM image of a contacted wire is shown in figure 3.5. Photoconductivity was performed by measuring the change in

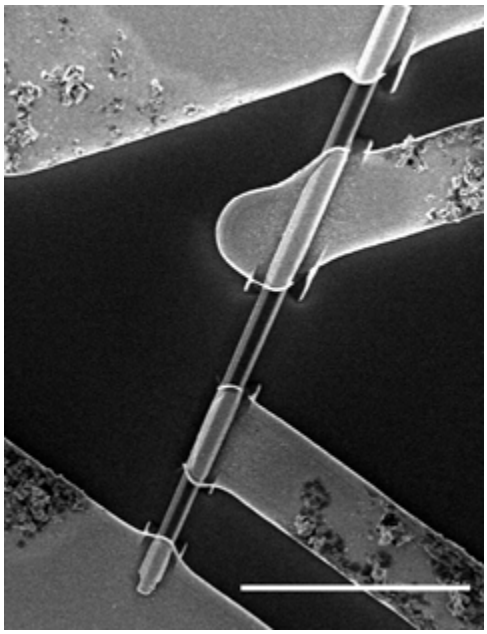


Figure 3.5: Single wire lying flat on a SiNx coated wafer, and contacted with four metal fingers. Scale bar is 20 microns.

current flow through a single wire using two point contacts. A 1.5 Volt AA battery was used as the voltage source to minimize power supply line noise. The light source was a Fianium supercontiuum laser, passed through a chopper and monochrometer. Current was measuring using a transimpedance amplifier and lock-in amplifier. A schematic of this measurement is shown in figure 3.6.

Data, shown in figure 3.7, was analyzed using a methodology similar to a Tauc plot, plotting [(photoconductivity signal/incident photon current) $\times$ photon energy]$^{1/2}$ vs. photon energy. The feature present at approximately 1.165 eV corresponds to the pump frequency in the supercontinuum laser, and causes a measurement artifact. Ignoring this, the Tauc-like plot was quite linear throughout the region around the band edge, from 1.25 eV to 1.065 eV. The extrapolated optical gaps for Si and $Si_{.9}Ge_{.1}$ correspond to 0.99eV and .94eV, respectively. The extended NIR absorption of the $Si_{.9}Ge_{.1}$ samples fits well with the expected absorption shift of approximately 40 meV given in the data tabulated by Humlicek. There are several possible sources of the approximately 100 meV systematic shift from the expected bandgaps present in both samples, including a convolution of the spectral width of the monochromated source and an ill-defined zero for the photoconductivity signal.

3.4 Conclusions and Outlook

In summary, we were able to grow patterned arrays of SiGe alloy wires using copper catalysts and chlorinated precursors with germanium content up approximately 12%. While the full range of

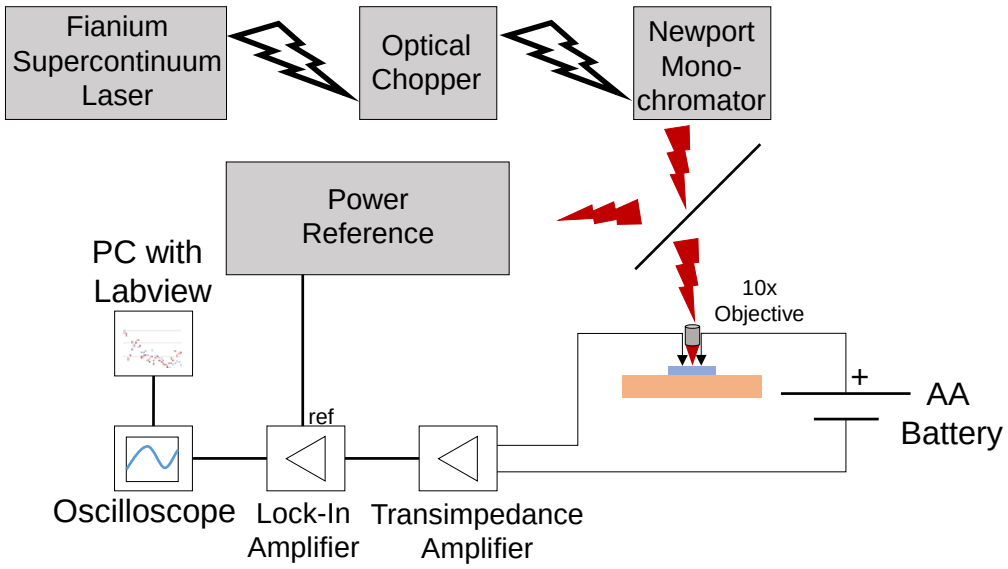


Figure 3.6: Schematic of the photoconductivity measurement used to measure absorption in SiGe wires.

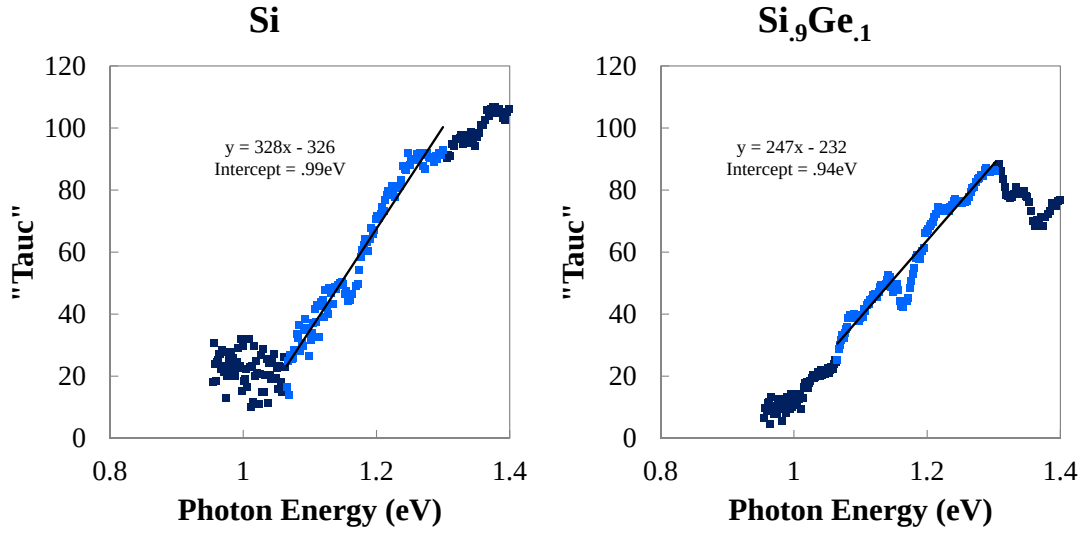


Figure 3.7: Photoconductivity data measured from single wires, plotted on a tauc-like plot. A linear fit was performed on the light blue section. "Tauc" is calculated by [(photoconductivity signal/incident photon current) $\times$ photon energy]$^{1/2}$ and normalized between samples.

concentrations was not achieved, this alloy composition is lattice and coefficient of thermal expansion matched to gallium phosphide, and should provide a high quality growth substrate for a range of III-V on silicon device applications. More work will need to be done in order to form devices, but this is a promising step towards achieving high efficiency devices with this material.

Chapter 4

High Efficiency with Microstructured Devices

4.1 Introduction

While cost is the most important driving force in widespread solar adoption, cell efficiency is leveraged in many of the module and balance of systems costs. An increase in cell efficiency has the potential to decrease total system cost by reducing the amount of glass, racking, wiring, land area, etc. needed to achieve a desired power output.

One potential strategy to improve efficiency is to drastically decrease the amount of material in a device. As discussed in section 1.2.1, the voltage of a solar cell results from the quasi-Fermi level splitting; this is a direct function of the minority carrier concentration, or injection level, in the device, and can be written as:

$$V_{OC} = \frac{kT}{q} \ln\left(\frac{(N_A + \Delta n)\Delta n}{n_i^2}\right)$$

Recall that in order to achieve high injection levels, it is necessary to have a long minority carrier effective lifetime and to absorb as much light in as small a volume as possible. The optimal device thickness for maximum efficiency therefore depends most strongly on the light trapping and achievable lifetime, which is usually dominated by surface recombination in thin devices,. Using realistic values with present technology, the efficiency peak is around 50 microns, significantly thinner than the wafers commonly used in actual devices. Indeed, recent long lifetime devices, such as the Panasonic HIT cell, have realized higher voltages, and therefore efficiencies, by moving to thinner substrates [49].

The difficulty in moving to yet thinner wafers is that conventional, planar cells have difficulty absorbing all the near-bandgap light, owing to silicon's indirect bandgap and subsequent weak absorption near its band edge. Therefore, optical design that maximizes absorption of long wavelength

light becomes increasingly important in a thin cell.

Other work on extremely thin silicon has approached moderate to high efficiencies. For example, an efficiency of 15.7% was achieved in a 10 µm silicon film with submicron inverted pyramidal texturing [50]. This device exhibited light absorption beyond the $4n^2$ limit, but exhibited poor collection efficiency at long wavelengths due to back surface recombination. Record voltages were not achieved, likely due to only moderate front surface passivation by silicon nitride — there is likely room for improvement in this area. Other recent results have shown excellent passivation of high surface area black silicon using alumina deposited by atomic layer deposition [51], resulting in un-optimized efficiencies of 22.1% on 280 µm thick wafers in an all back contract device.

Deeply microstructured, high aspect ratio silicon with very low effective thickness holds unique potential to form high efficiency devices. As shown previously, silicon wires with dimensions on the order of one micron absorb near bandgap light very strongly, in some cases even exceeding the $4n^2$ geometrical ray optics light trapping limit [11]. These high aspect ratio structures likely absorb stronger than similarly dimensioned low aspect ratio cone structures [52]. Therefore, it is possible to absorb a large portion of incident light using only a very small volume of material. As explored in the next section, light absorption beyond the $4n^2$ limit is extremely beneficial in the quest to reach very high efficiencies in thin cells.

It is also necessary to attain high lifetimes in the silicon material to realize improved voltages. As explored in Chapter 2, vapor-liquid-solid grown microwires, which use a transition metal catalyzed growth process, contain deep level traps from the growth catalyst which limit the lifetime of the resulting material. Maximum attainable efficiencies using this material are likely around 17% [14] [13]. Therefore, creating microstructures by etching high quality wafers rather than growing material was explored. The candidate process is a cryogenic deep reactive ion etching process, similar to the one used by Savin et al. to fabricate a high quality black silicon [51]. We explore the viability of this process in both creating various microstructures in silicon and maintaining high lifetimes in high quality wafers.

4.2 Limiting Efficiency Calculations

4.2.1 Method

An analytical model was used to aid in the design of a high efficiency, low equivalent planar thickness (t_{ept}) device. Input parameters considered included the thickness, light trapping path length enhancement, Shockley-Reed-Hall lifetime τ_{bulk}, and surface recombination velocity S. Additionally, the model was modified in order to include the effects present in wire arrays, namely the increased surface area and the increased light trapping. The light trapping enhancement was included by considering a factor called effective internal concentration, and multiplying the total light trapping

Table 4.1: Parameters used for limiting efficiency calculations

N_i	9.7×10^9 cm^{-3}
N_a	1×10^{15} cm^{-3}
$B_{radiative}$	4.7×10^{15} cm^3 s^{-1}
n & k	[53]

path length (such as $4n^2$) by this factor.

This model was implemented in Microsoft Excel, using VBA to iteratively solve the transcendental system of equations for steady state carrier concentration and to generate parameter sweeps. Material parameters were input and recombination rates calculated using the workbook. A full listing of the VBA code is available in appendix C, and material parameters are shown in table 4.1.

In order to calculate the limiting efficiency, generation was first calculated assuming simple Beer-Lambert absorption using the optical properties for silicon tabulated by Green at al. [53]. Next, recombination was calculated; the empirical model developed by Richter et al. was used to describe Auger recombination [54]. Surface and Shockley-Reed-Hall recombination were calculated as described in [20] using the surface recombination velocity S and bulk minority carrier lifetime τ as free parameters. Once steady state generation and recombination were calculated, the voltage was calculated from the excess minority carrier concentration, as described previously:

$$V_{OC} = \frac{kT}{q} \ln\left(\frac{(N_A + \Delta n)\Delta n}{n_i^2}\right)$$

Finally, an efficiency was extracted using the total generation as the J_{SC} and calculating a fill factor using the empirical model for a device without series resistance or shunting developed by M. A. Green:

$$FF = \frac{v_{oc} - \ln(v_{oc} + 0.72)}{v_{oc} + 1} [55].$$

This model provides an estimate for the absolute maximum achievable efficiency. It is a very simple model which neglects several common loss mechanisms, such as emitter recombination, front surface reflection, and resistances within the device. The efficiencies given are not expected to be achievable in an actual device with present technology. However, it provides value as it allows for rapid analysis on expected trends based on thickness and material and interface quality, which will have the strongest influence in device design.

4.2.2 Results

One finding was that the bulk lifetime requirements are somewhat relaxed as the equivalent planar thickness shrinks. As shown in figure 4.1, the efficiency of a three-micron-thick device with $4n^2$ light trapping is a strong function of surface recombination velocity below 1 cm s^{-1}, but only begins to

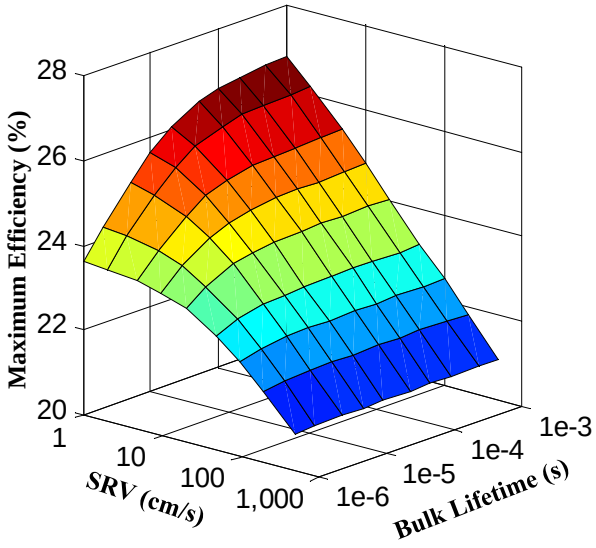


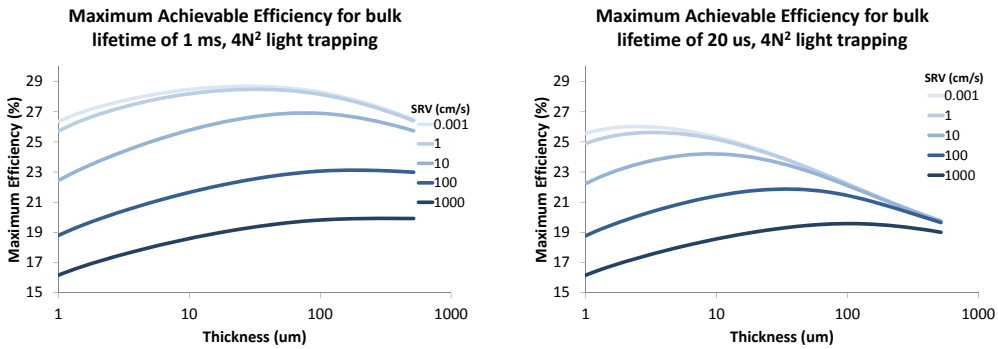
Figure 4.1: Limiting efficiency of a 3 µm thick device with $4n^2$ light trapping as a function of bulk lifetime and surface recombination velocity. Note the stronger dependence on surface recombination velocity for easily achievable bulk lifetimes, greater than 100 µs.

fall at bulk lifetimes below about 20 µs. This contrasts thick cells, which are sensitive to changes in bulk lifetimes in the ms range. The efficiency of a device with low quality bulk material is therefore more sensitive to thickness than a high material quality device, and tends towards peak efficiencies at lower thicknesses, as shown in figure 4.2.

Optimizing thickness is a tradeoff between achieving a higher voltage in a thinner cell while still collecting enough light. Therefore, light trapping beyond the $4n^2$ limit pushes the optimal thickness towards thinner devices and higher potential efficiencies. As shown in figure 4.3, given sufficient surface passivation, a light trapping enhancement factor of four results in an approximate halving of the optimal thickness and increase in the limiting efficiency by one percentage point.

Increasing the amount of surface area, quantified by the ratio of the total surface area to the planar equivalent surface [56], increases the sensitivity to the surface recombination velocity. While, as shown in figure 4.2, there is little advantage to achieving an SRV below $1\,\mathrm{cm\,s^{-1}}$ in a planar device, if the front surface area increases by a factor of 25, as in a microwire device, the device becomes sensitive to surface recombination velocities up to approximately $0.2\,\mathrm{cm\,s^{-1}}$.

While, as discussed, it has been shown to be possible to exceed the $4n^2$ light trapping limit in microstructured silicon, it is not clear what the origin of this effect is and therefore what the maximum achievable light trapping enhancement is. One likely source is wave optical effects, which have been shown to dominate in nanostructured III-V materials [57]. However, these silicon microstruc-



(a) Limiting efficiency with 1 ms bulk lifetime. (b) Limiting efficiency with 20 µs bulk lifetime.

Figure 4.2: Limiting efficiency of silicon solar cells as a function of thickness, at different surface recombination velocities and bulk lifetimes. With lower bulk lifetime, the peak efficiency is somewhat reduced, and occurs in a significantly thinner device.

tures are significantly larger, and support many more than the handful of optical modes which cause enhancement of light trapping in nanowires. Another possibility is that it is not only the index and volume of the absorber material which are relevant in calculating the limit of light trapping in these structures, but also the index and volume of the anti-reflective coating and light scattering particles. By increasing the intensity in the nearby non-absorbing material, we can effectively concentrate light on the silicon absorber as well. Therefore, the high index anti-reflective coating and scattering particles may have been critical in enhancing absorption beyond the ray optical limit in VLS grown silicon microwires.

4.2.3 Summary

In summary, there is room to achieve high efficiencies in thin devices. In some cases, these efficiencies can even exceed the efficiency of a thick, wafer based device, especially when restricted to using silicon with a low bulk lifetime. The two most important parameters in achieving very high efficiencies in thin devices are the surface recombination velocity and light trapping enhancement. Requirements on both are on the order of, but beyond, what has already been achieved and the limits must be explored in order to realize high efficiency microstructured devices.

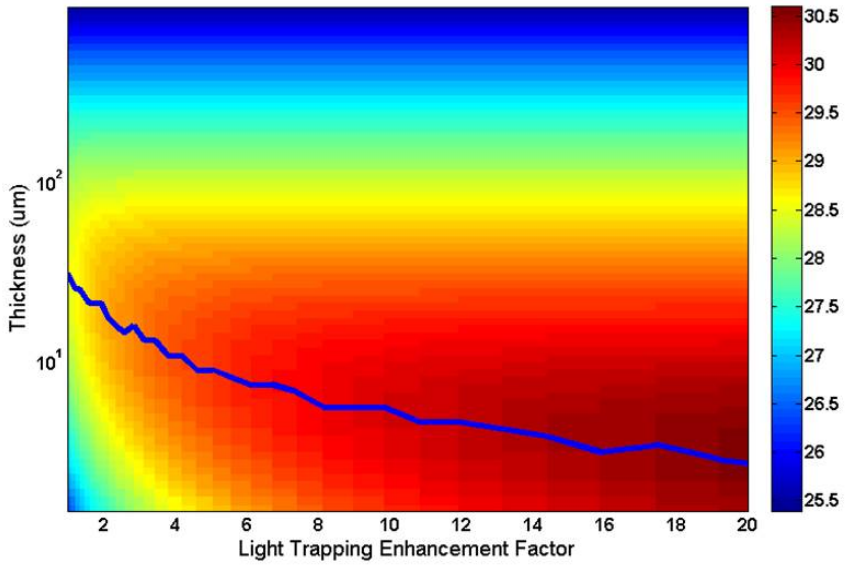


Figure 4.3: Limiting efficiency and optimal thickness for light trapping beyond the $4n^2$ limit, considering an SRV of $1\,\mathrm{cm\,s^{-1}}$ and flat surfaces.

4.3 Experimental

4.3.1 Wire Fabrication

Our approach to achieving high lifetime microstructured silicon devices was to use a cryogenic deep reactive ion etch (cryo-DRIE) process. By varying the gas flows during etching, we are able to realize a wide variety of structures, including very high aspect ratios and sharp angles. We selected this etch because it uses an inductively coupled plasma with low forward power densities, and is dominated by chemical processes, rather than physical milling. As a result, the surface is only minimally damaged during the wire forming etch, and high lifetime wafers retain their high lifetime after etching. Additionally, the resulting sidewalls are smooth, compared to the scalloped sidewalls obtained using a cycled Bosch process [58]. The extent of the surface damage was evaluated by measuring the lifetime of planar etched wafers, as described in the next section.

Due to slow cycling and high cost of both capital and consumables [59], it is not clear if the cryo-DRIE process could be scaled to a viable commercial process. Regardless, it can be considered a testbed for creating high material quality microstructured material for development of devices. A wide variety of rapid, wet chemical etching processes are currently being investigated [60] to evaluate their use in forming high quality high aspect ratio structures. Another option is template epitaxial growth, as currently explored by Solexel [61].

Etching was performed by Sisir Yalamanchili using the Oxford Plasmalab 100 ICP 380 system located in the Kavli Nanoscience Institute labs, using the method described by David Henry [58].

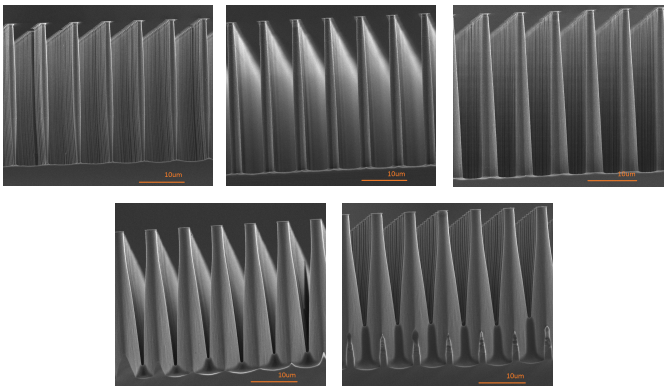


Figure 4.4: Scanning electron microscope images of wires etched by Sisir Yalamanchili using a cryo-DRIE process. The taper angle can be controlled by changing the ratio of passivation to etch gas.

Resulting high aspect ratio wire structures are shown in figure 4.4. The tapering angle is changed by varying the ratio of etch gas (SF_6) to passivation gas (O_2) during the etching process. As shown, a wide variety of structures are achievable, from undercut wires, to cylinders with near vertical sidewalls, to tapered wires. In order to achieve long wires with very pointed tips, the etch time can be increased and the gas ratio can be modified during the process.

4.3.2 Lifetime Measurements

We wished to confirm that the cryogenic deep reactive ion etching process did not damage the silicon surface so that high lifetime microstructured material could be fabricated. The extent of surface damage caused by the etching process was evaluated by measuring the lifetime of a planar silicon wafer following etching. Without a patterned alumina hard mask present, the planar geometry of the wafer is maintained. Following the dry etch, a wet etch in 30% potassium hydroxide at 70 °C was used to remove the top exposed surface. Lifetimes of wafers were measured using a Freiberg MDPspot tool, equipped with a 600 mW 980 nm diode laser. Results are shown in figure 4.5; it was found that the approximately 1 ms lifetime of the wafer could be recovered by removing the top 100-200 nm of material, implying damage induced by the cryo-DRIE process is limited to this region.

Lifetime measurements on silicon wires were performed using a home built microwave detected photoconductivity tool, as described in section 2.4.2.2. While the sensitivity of the Freiberg tool was good, the time resolution rendered the tool incapable of performing accurate measurements of lifetimes below 1-2 µs. Care was taken to enable fast measurements in the home built setup, and as a result, measurements down to 20 ns were possible, as confirmed on as-grown, unpassivated vapor-liquid-solid grown silicon wires.

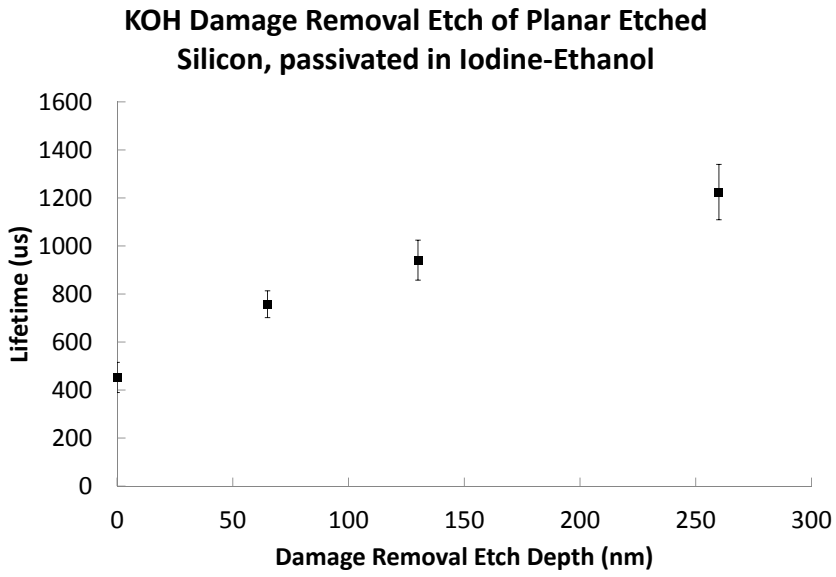


Figure 4.5: Lifetimes of planar DRIE etched wafers following potassium hydroxide damage removal etching

Etched wire samples were prepared for lifetime measurements using the following method:

1. Wires were cleaned and surfaces etched on-substrate
2. The sample was wet with ethanol
3. Wires were scraped from the surface with a razor blade, and washed with additional ethanol into a 1.5 mL centrifuge tube
4. Wires were centrifuged and excess solvent removed

An optional etch can then be performed (steps 5-8)

5. The solvent was removed by 3 successive rinse and centrifuge steps with DI water
6. A few drops (0.5 mL) of room temperature, 20% potassium hydroxide solution was added, and the wires stirred with a vortex mixer for 90 seconds.
7. To stop the etching, the tube was filled with 1:1 hydrochloric acid:DI water
8. Wires were again centrifuged to remove this salt water
9. Wires were washed as in step 5 with either DI water, ethanol, or methanol, depending on the chemical passivation. Chemical passivation was then added.

Results from lifetime measurements of wires prepared with this method are shown in table 4.2. As described in section 2.4.2.2, it is desirable to know the injection level of the lifetime measurement to determine the mechanism for recombination governing the device and how it relates to the injection regime encountered in operation. All measurements resulted in continuously increasing lifetimes as a function of intensity, indicating that we were measuring at the onset of high level injection. As in the measurements on VLS grown wires, it was observed that passivation in hydrochloric acid resulted in higher lifetimes than hydrofluoric acid. Again, this could be due to differences in surface wetting.

Transient simulations were performed with Synopsys Sentaurus TCAD in order to study how the effective lifetime varies with material parameters such as surface and bulk recombination in cylindrical and tapered structures. While simple analytical solutions relating the effective lifetime to the surface recombination velocity, bulk lifetime, and thickness exist for wafer geometries, these same expressions only exist for certain limited conditions in cylindrical geometries, and are not solved for tapered structures. More information about theses simulations, including a full code listing, is presented in appendix B.

The effective lifetimes measured under hydrochloric acid passivation fit a model which includes high bulk material lifetime of 1 ms and a surface recombination velocity of approximately $500\,\mathrm{cm\,s^{-1}}$ for both 15 µm and 3 µm diameter wires. This surface recombination velocity is significantly higher than expected; our wafer based measurements and the literature suggest that SRVs should be below $10\,\mathrm{cm\,s^{-1}}$ for all the acid [22] and iodine-ethanol [23] passivation techniques.

There are several possible explanations for these poor effective lifetimes measured. It seems likely that the defects present in this material can not be purely characterized as bulk or surface, but rather consist of a decaying density of defects within the first few nanometers of the surface. Therefore, it is not a poor surface recombination velocity in the traditional sense of dangling bonds causing recombination at the surface, but can be modeled similarly. This is likely consistent with the discrepancy between the expected and observed behavior of hydrochloric compared to hydrofluoric acid. As discussed in Chapter 2, the acids induce strong band bending at the surface which repels carriers, preventing recombination. If the hydrochloric acid causes stronger band bending which persists deeper into the material, it could result in higher lifetimes.

The remaining defects present in these wires, compared to the results obtained in planar silicon, could be due to the wide variety of facets exposed during the DRIE etch process, which will be etched at different rates by the damage removal etch. A way around this would be to use an isotropic damage removal etch, such as hydrofluoric/nitric/acetic.

Table 4.2: Lifetimes of large (15 µm) DRIE etched wires removed from the substrate and treated with a variety of chemical surface passivation treatments.

Surface Treatment	**Lifetime** (µs)
Benzoquinone in Methanol	0.183
Iodine in Ethanol	0.555
2% HF	0.441
49% HF	0.681
6M HCl	1.889

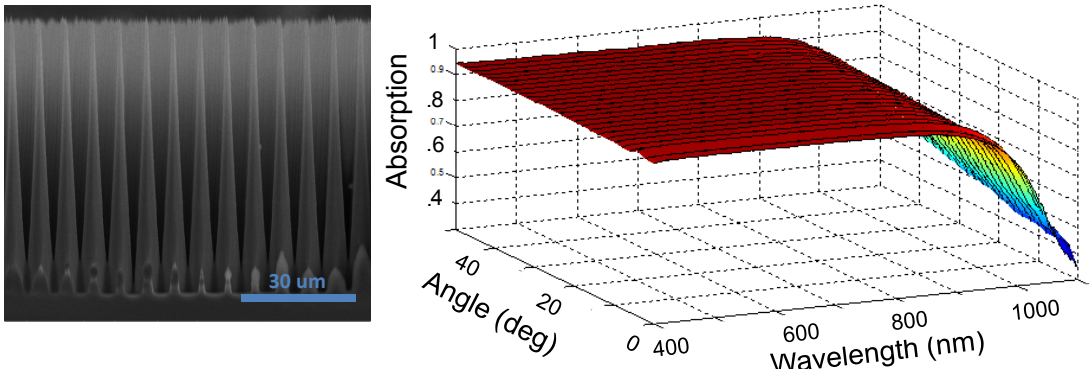


Figure 4.6: Absorption measurements of highly tapered etched wires, shown left, on substrate.

4.3.3 Absorption Measurements

Angle resolved reflection measurements were performed using a spectrophotometer equipped with an integrating sphere. The spectrophotometer instrument uses monochromated light from a Fianium supercontinuum laser and a silicon photodiode detector, as described in [62]. Measurements were performed both on wires on substrate, and peeled off wire arrays. It was important to consider absorption across the entire spectrum, although this falls into two different regimes governed by different effects. In the visible range, silicon absorbs light very strongly but also reflects due to its high refractive index. In these structures, antireflective properties are provided by the tapered shape, which provides a gradual change in refractive index, compared to the quarter-wavelength effect used in standard flat devices [63]. Absorption in the near IR, closer to the bandedge, is governed by the weak absorption of silicon. The amount of light trapping, or path length enhancement, becomes relevant at these long wavelengths.

Reflection measurements from a highly tapered structure, on substrate, are shown in figure 4.6. Reflection in the visible range is extremely low and angle independent, even without the addition of a quarter-wave antireflective coating and scattering particles, which were necessary to achieve high absorption in this wavelength range in cylindrical VLS-grown wires.

In order to measure the light trapping path length enhancement within the wire material, mea-

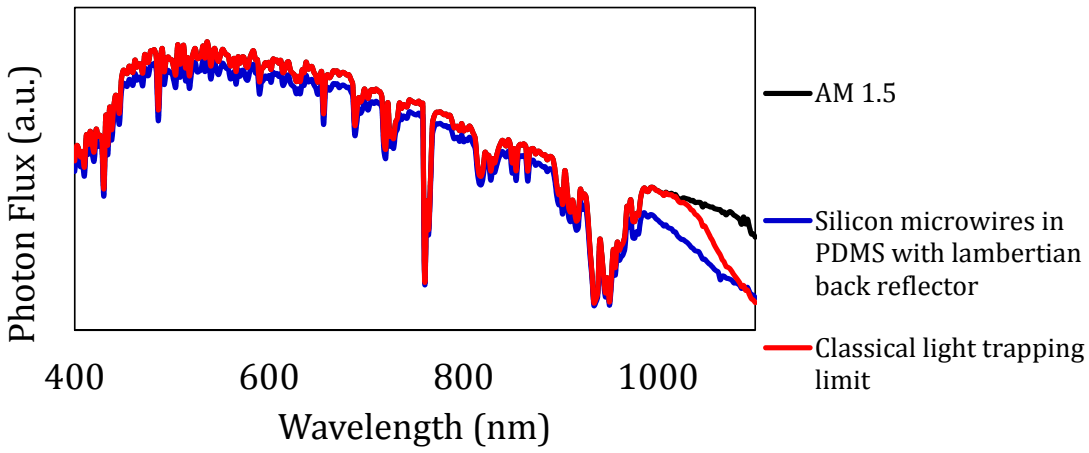


Figure 4.7: Absorption measurements of peeled off etched wires, weighted against the solar spectrum and compared to the $4n^2$ light trapping limit. The mictrostructured silicon approached the classical limit until approximately 1000 nm. This particular sample had a planar equivalent thickness of 20 µm, and there is very little room for improvement over the classical limit at this thickness.

surements were made without the presence of the substrate. Samples were embedded in PDMS and peeled off the surface, and two pass reflection, corresponding to total absorption within the wire material, was measured with a barium sulfate Lambertian back reflector. The normal incidence reflection, weighted against the solar spectrum and compared to the $4n^2$ limit, is shown in figure 4.7. The equivalent planar thickness of the films measured using this technique was approximately 20 µm; at this thickness, the $4n^2$ limit is near full absorption until very close to the band edge, leaving very little room to beat this limit. In comparison, the VLS wires which displayed light trapping beyond this limit had only 3 µm of equivalent thickness [11]. Exploring the limits of light trapping further will require fabricating even thinner microstructured material.

4.4 Conclusions and Outlook

The potential to achieve high efficiency using significantly less silicon material than a wafer was explored. Device designs rely on both the ability to absorb light very strongly and passivate surfaces extremely well. Microstructuring with a cryogenic deep reactive ion etching process was identified as a promising method for fabricating structures which absorb light very strongly while still maintaining high material quality. The resulting structures did indeed absorb light very strongly. These structures exhibit excellent broadband, angle independent, anti-reflective properties, and provided a considerable path length enhancement for infrared light. While we did not measure absorption enhancement beyond the $4n^2$ light trapping limit, these etched structures showed potential to beat

this limit by further reducing the amount of material used. Additionally, in experiments on planar silicon, this process showed potential to maintain the underlying bulk material quality. While the resulting material presented difficulty in achieving excellent surface passivation, there are several promising paths forward that would reduce near-surface defects.

Chapter 5

Silicon-Gallium Phosphide Heterojunctions

5.1 Introduction

Silicon is currently the material that makes up approximately 90% of photovoltaic installed capacity [64]. Cell efficiency is an important lever in any photovoltaic technology, allowing the reduction of module material and other balance of system costs (such as racking) per power output. Silicon heterojunctions offer improved performance due to an improved method of carrier separation and collection. They function as carrier selective contacts, not only accepting minority carriers from the base, but actively reflecting majority carriers, which minimizes recombination around the junction. This doubles to effectively passivate the top surface of the silicon. Both the current record efficiency silicon solar cell [65] and one of the highest efficiency production modules [66] rely on silicon heterojunctions.

Heterojunctions between amorphous silicon and crystalline silicon form an excellent electronic junction but have several drawbacks, limiting the maximum achievable efficiency. Amorphous silicon has a direct bandgap at around 1.8 eV, and therefore even thin layers absorb a significant amount of light. Light absorbed in heavily doped emitter layers is generally not collected at high efficiency [67], and is thus lost. Additionally, the mobility, and therefore electrical conductivity, is low compared to a crystalline semiconductor, so a transparent conductor is required in order to efficiently extract current from the device. Free carrier absorption in the transparent conductor, as well as strong absorption in the blue region of the spectrum, introduces additional parasitic absorption losses. All together, these losses add up to $2.6\,\mathrm{mA\,cm^{-2}}$, and eliminating them could result in a 5% relative efficiency gain [68].

In order to achieve efficiency gains compared to amorphous silicon, candidate materials must be both more transparent and conductive. Additionally, they must form a good electrical junction with silicon. The properties of the junction, such as the band offsets and interface defect density, will be

important in determining device behavior, but can only be measured after forming heterojunctions. While the band offsets can be theorized by Anderson's rule [69] using properties of the individual materials, the theory often fails in actual devices due to Fermi level pinning caused by defect states [70] or interface dipole charges [71]. Interface defect state density is even more difficult to theorize, and depends strongly on the growth process. We can make efforts to minimize the number of lattice defects such as dislocations and antiphase domains, but it will not be known how these physical defects will manifest electronically until characterization. Therefore, we consider light absorption and conductivity most strongly during the materials selection process, with knowledge that we must be able to measure and evaluate the relevant junction properties. Gallium phosphide was chosen as a candidate material, due to its wider, indirect bandgap of 2.26 eV [72] and higher conductivity [73] than amorphous silicon [74]. Other materials with these properties, such as GaN, SiC, and MO_3, were explored by our collaborators on this project.

In order to evaluate its suitability as a heterojunction partner with silicon, gallium phosphide was grown on silicon by group member Chris Chen, and later Dr. Rebecca Saive, on a 1×3 inch Thomas Swan Epitor II MOCVD system with a close-coupled showerhead located at the Lawrence Berkeley National Lab's Molecular Foundry. A two step growth process was used, consisting of a low temperature atomic layer deposition-like nucleation layer and high temperature growth, as developed by Grassman *et al.* [75]. High quality growths with low lattice defect densities, as measured by X-ray diffraction and transmission electron microscope, were obtained on both (112) and (001)-6° offcut silicon substrates [76].

My role in this project was to characterize electronic properties of the gallium phosphide material grown and help to characterize junctions formed between the two materials. To these ends, I performed a series of simulations to better understand and interpret measurements of the junctions and developed a substrate removal process to isolate GaP films for characterization without the influence of the silicon substrate.

5.2 Design and Simulation of Gallium Phosphide Heterojunction Devices

Synopsys Sentaurus was used to evaluate the effect of different parameters on the silicon-GaP heterojunction. Despite significant effort to grow GaP on Si by other groups, the heterojunction system has received relatively little interest previously, and as a result, most of the relevant interface parameters have not been measured. The parameters given by Wagner et al. [77] were used as a starting point. A similar device structure was used as well, consisting of a 250 µm p-type silicon base, with an oxide passivated rear side and locally diffused p+ contact regions. The front surface was a simple uniform GaP layer with an idealized front contact.

Two parameters studied were the effects of interface defects and band alignment. As discussed, these parameters are difficult to theorize but have significant implications for device performance. Additionally, their interplay was investigated, as well as the effects of doping on device performance.

5.2.1 Interface Defects

As reported by Wagner et al. [77], the simulation showed very little sensitivity to the GaP/Si interface surface recombination rate S_0. This is due to the strong band bending at the interface; as shown in the band diagram in figure 5.1a, using Anderson's rule, the band offsets at the GaP interface are sufficient to cause strong inversion within the silicon. The equation used to calculate surface recombination is:

$$R_{surf,net}^{SRH} = \frac{np - n_{i,eff}^2}{(n + n_1)/s_p + (p + p_1)/s_n}$$

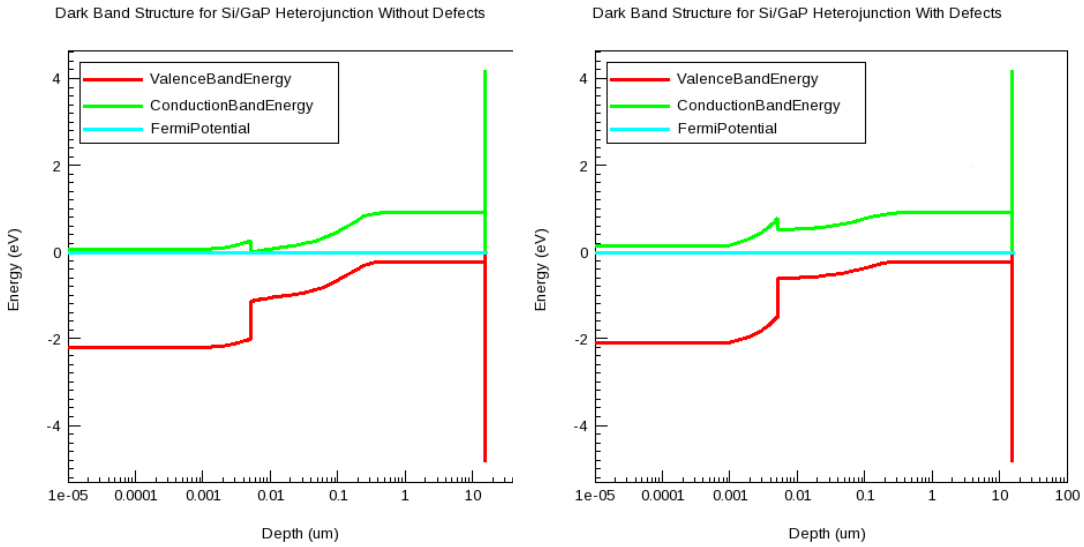
where n_1 and p_1 are trap populations, given by:

$$n_1 = n_{I,eff} \exp\left(\frac{E_{trap}}{kT}\right) \text{ and } p_1 = n_{I,eff} \exp\left(\frac{-E_{trap}}{kT}\right) \text{ [78]}$$

The intrinsic carrier concentration $n_{I,eff}$ is the effective intrinsic concentration after modifications for band gap narrowing due to the presence of defects or dopants and the populations n and p are the actual carrier concentrations at the interface. This surface recombination rate depends strongly on the pn product; while we expect a high concentration of photoexcited electrons to reach the interface in our p-type base device, strong band bending at the heterointerface suppresses the hole concentration, and subsequently, the surface recombination is suppressed at the interface. This is similar to the mechanism for suppressing recombination in a pp^+ back surface field region, where the equilibrium concentration of minority carriers is suppressed to reduce the amount of recombination [79]. The result of this is that we expect excellent performance at a heterointerface where the bands align to produce strong band bending and an inverted surface.

The simulated structure was significantly more sensitive to the concentration of defect states placed at the interface. As mentioned, few studies of the GaP/Si heterointerface exist, and it was not possible to find parameters of defects likely to be present in the literature. We therefore simulated a Gaussian distribution of states centered at midgap with $\sigma_E = 0.5$ eV, with both hole and electron capture cross sections of 10^{-13} cm^2. Without better knowledge of the nature of these defects, it is not informative to extract quantitative information from these simulations. However, the trends and recombination mechanisms revealed are independent of the defect parameters; they simply change the concentration which is needed to cause a certain amount of recombination.

These defects act to pin the Fermi level to midgap. This counteracts the strong band bending



(a) Simulated GaP/Si heterojunction without defects

(b) Simulated GaP/Si heterojunction with midgap defects at the interface

Figure 5.1: Simulated band structures of GaP/Si heterojunctions in the dark without (left) and with (right) midgap states at the interface. Note that without defects, the p-type silicon is inverted before the physical junction, but defects act to pin the Fermi level at midgap, and the silicon is never inverted.

that is expected at the heterointerface, which generally suppresses surface recombination, and allows recombination to occur. The presence of a low concentration of defects causes a drop in voltage, indicative of recombination occurring at the front surface. A large defect concentration also blocks transport across the interface, and results in a drop in current. Band diagrams comparing simulations without and with many interface states (2×10^{13} cm^{-2} using the previously described parameters) are shown in figure 5.1.

Following our measurements, which will be described in more detail in section 5.5, this is likely a more realistic picture of the action of a recombination active surface than the SRV model which incorrectly predicts a very robust interface.

5.2.2 Band Alignment

As discussed previously, it is not possible to precisely calculate the band offsets considering only the equilibrium electron affinities of the two materials in a heterojunction. However, band offset measurements can be performed early in the material screening process by measuring thin epitaxial layers with x-ray photoemission spectroscopy [80]. Additionally, it may be possible to modify the band offsets by either changing the growth conditions or adding interfacial layers [81]. It is therefore beneficial to understand the effect that band offset has on actual devices.

The traditional view is that it is most beneficial for band offsets to be situated such that they

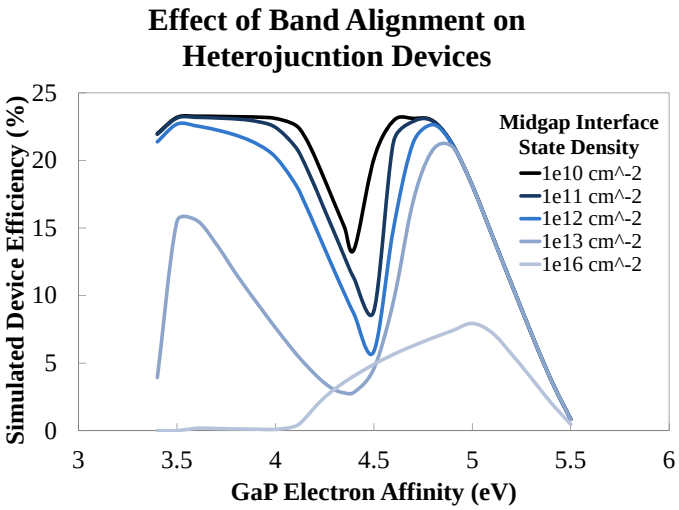
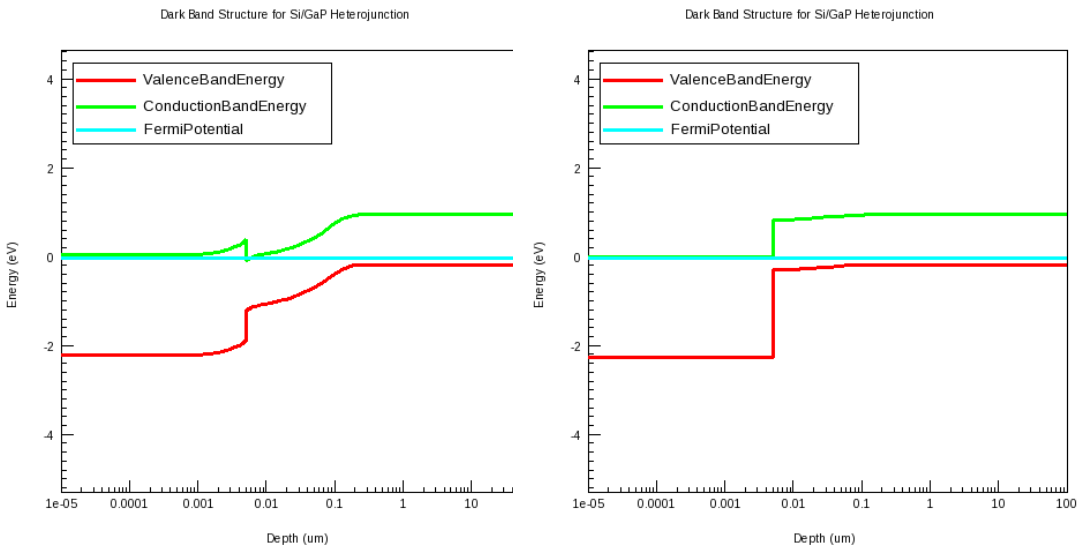


Figure 5.2: Simulated efficiency of GaP/Si heterojunction devices varying band alignment and defect concentration. Emitter doping concentration is 10^{19} cm^{-3}

allow minority carriers to be easily transported across the junction and block majority carriers. However, if a high quality interface can be achieved, absent of defects, the highest voltages are achieved when there is some barrier to minority carrier transport as well. This allows an increase in the minority carrier concentration. The ideal situation occurs when the minority carrier transport rate across the heterojunction is on the order of the recombination rate [82].

Simulations were performed with the electron affinity of the gallium phosphide layer, from which the band offsets are calculated, varied as a free parameter, from 3.4 eV to 5.5 eV. For reference, the often quoted but rarely cited value for the electron affinity of GaP in the literature is 3.8 eV [73]. Midgap interface defects as explored in the previous section were included as well. The resulting efficiency as a function of electron affinity at a variety of different interface state densities is shown in figure 5.2. Two peaks with high potential efficiency are revealed by these simulations. The first corresponds to band offsets which cause an inversion layer to be induced into the silicon side of the junction, limiting recombination. As the GaP electron affinity is raised, the induced band bending is weaker. As the silicon begins to become depleted, the Fermi level passes through mid gap, and the efficiency dips as interface recombination is more likely. Finally, the simulated efficiency rises again as the silicon bands remain straight or enter accumulation. In this case, charge separation occurs at the physical junction, rather than the induced inversion region as in the low electron affinity case. Dark band diagrams of these two scenarios are shown in figure 5.3.

As shown in figure 5.4, the effects of defects can be somewhat mitigated by increasing the emitter doping density. A highly doped emitter reduces the width of the conduction band spike, which acts as



(a) GaP/Si heterojunction with $\chi = 3.6$ eV (b) GaP/Si heterojunction with $\chi = 4.9$ eV

Figure 5.3: Simulated band structures of GaP/Si heterojunctions in the dark with electron affinities $\chi = 3.6$ eV (left) and $\chi = 4.9$ eV (right), corresponding to the approximate efficiency peaks. These simulations used a moderate interface state density (10^{11} cm^{-2}) and emitter doping density (10^{19} cm^{-3}). With a low electron affinity, charge separation occurs at the induced junction within the silicon.

a barrier to electron transport across the heterojunction. This allows carriers to tunnel through the barrier more easily, increasing the rate of transport across the barrier, and reducing the probability of recombination before collection.

5.3 Lifetime measurements of Silicon with Gallium Phosphide films

Lifetime measurements were performed in order to determine the quality of the silicon-gallium phosphide heterointerface. As explored earlier, the lifetime measurements yield a result that is influenced by both bulk and surface effects. Therefore, in order to measure the surface quality of the GaP/Si interface, the bulk lifetime must be better than the surface lifetime. Despite using float zoned, 1 ms lifetime silicon growth substrates, initial growths showed a lifetime of $<20\,\mu$s. Etching the gallium phosphide off the front surface and passivation with iodine-ethanol did not show improved lifetime, indicating that bulk contamination was the source of lifetime degradation in these samples. This effect is reported in the literature [83]. Another report found they were able to maintain silicon lifetime by slow cooling following GaP growth, but this effect was not quantified [84].

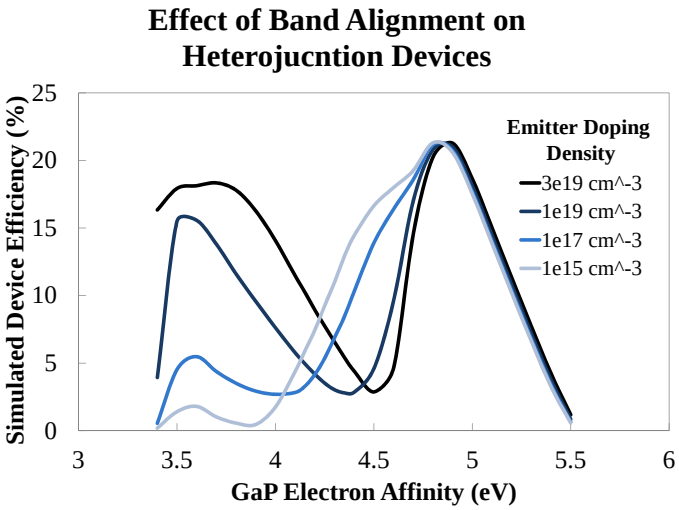


Figure 5.4: Simulated efficiency of GaP/Si heterojunction devices varying band alignment and emitter doping density at the high interface state density of 10^{13} cm^{-2}

In order to improve the bulk lifetime, care was taken to eliminate sources of contamination. A protective, and passivating, 200 nm PECVD silicon nitride film was deposited on the rear surface of the wafer. The quartzware inside the reactor was changed, and the wafer preparation beakers were changed and/or cleaned. Following these steps, lifetimes improved to the range of 45-90 µs, and were limited by the gallium phosphide surface. Bulk lifetimes measured by etching off the front surface measured in the range of 500-700 µs. Additionally, areas which appeared higher quality visually (appearing smooth and specular as opposed to cloudy) yielded higher lifetime, which indicated that high quality GaP more effectively passivated Si, and that there was likely room to further improve the passivation quality of the GaP/Si interface by improving the quality of the GaP film.

Several recent growths achieved minority carrier lifetimes up to 300 µs on intrinsic (112) and p-doped (isotype) (001) silicon, with Mg doped p-type GaP on the front surface. These lifetimes correspond to an upper bound on the GaP-Si surface recombination velocity of 100 cm s^{-1}, to our knowledge, the best so far reported. These champion devices were grown following the first attempts at silicon doping using a disilane source; however, due to a problem with the mass flow controller, the disilane flow was higher than desired for doping. It is possible that the chamber was conditioned by silicon growth on the sidewalls prior to the GaP growth, which may have been important in forming a high quality interface layer. Relatively poor (45-60 µs) lifetimes were obtained on n-type (001) substrates grown alongside high performing (112) samples. More work must be done in order to determine if this poor lifetime is a result of the band alignment causing electrical passivation in some device types but not others, or a higher level of interface states for films grown on these

particular wafers.

While we have thus far been unable to create a passivating p-n heterojunction interface, the result on isotype heterojunctions is still notable. Isotype heterojunctions hold potential for a different use in high efficiency homojunction devices as conductive window layers, passivating a silicon emitter layer. These layers could be especially useful beneath contacts to passivate a normally highly recombination active region, as most surface passivation layers are not conductive. In such a device, a material that is more transparent and passivating than gallium phosphide, such as SiO_2 or Al_2O_3, would passivate the remainder of the front surface [84].

5.4 Substrate Removed Gallium Phosphide Films

5.4.1 Motivation

As explored with simulation, it is necessary to achieve high conductivity and high doping densities to realize high efficiency devices. However, the action of dopants in the MOCVD growth process has not been well studied and must be measured in our films. Substrate removal was initially motivated by the desire to measure the electronic properties of gallium phosphide (GaP) films absent of effects caused by the silicon growth substrate. The ability to measure conductivity from the GaP film and not the silicon substrate relied on one of two assumptions: (1) that there was a p-n junction formed between the two materials, and a depletion width established in the silicon that was wide enough to prevent conduction, or (2) that the silicon was much more resistive than the GaP films.

For the films and devices grown, neither assumption was true. Current-voltage characteristics showed relatively high conduction in both directions between the silicon and GaP, revealing that there was not a wide depletion width between the silicon and GaP. Additionally, even in high performing heterojunction devices, the band offsets will cause inversion of the top layer of the silicon; the depletion width will only occur beneath this, and Hall effect measurements will still convolute the conductivity in the inverted silicon layer with the GaP conductivity [85].

Attempts to grow on insulating wafers also failed to yield meaningful measurements. While films were grown on float zoned, near-intrinsic wafers with a resistivity >4000 Ω-cm, the thickness of the film (300 nm) was much thinner than the substrate (300 µm); therefore, for the silicon to be much more resistive than the GaP films, the resistivity of the GaP film must be approximately 10,000 times less than that of the silicon, or less than 0.4 Ω-cm.

Possible solutions to the issue of the convolution of the substrate with the film while performing electrical measurements include growing on a silicon-on-insulator (SOI) substrate, including a sacrificial layer and performing epitaxial liftoff, and removing the substrate following growth. Both growth on SOI and substrate removal were attempted. The silicon layers on SOI substrates were first thinned to 20-30 nm in order to reduce the conductivity by subsequent oxidations and etches.

Reasonable resistivity measurements were obtained, but Hall effect measurements revealed conduction by the opposite carrier type expected with unrealistically high mobility. This is likely due to the high mobility silicon or interfacial inversion layer dominating the Hall effect signal.

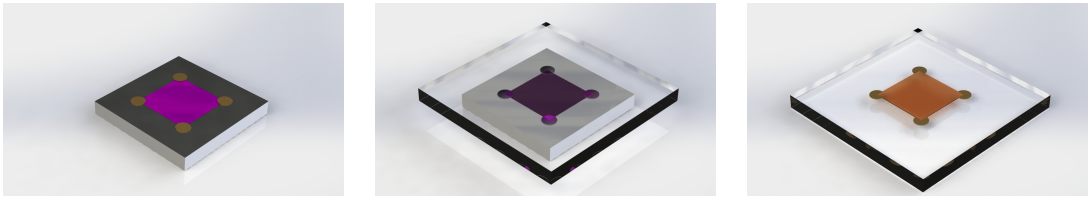
It was therefore desirable to form standalone thin films for electrical measurements. Substrate removal was chosen over epitaxial liftoff for the ability to probe the exact GaP layers we are interested in, rather than GaP grown on an intermediate layer, which may change the nature or concentration of defects. Additionally, it was preferable to perform measurements without having to develop and optimize a new growth process.

The realization of high quality free standing gallium phosphide films is also interesting due to the optical properties of GaP. Notably, GaP has a high refractive index of above 3 throughout the visible range [86]. Additionally, it is quite transparent throughout much of the visible range; absorption is extremely low below the indirect bandgap at 2.26 eV and still weak (α <3500 cm^{-1}) below the second indirect gap at 2.5-2.6 eV [86] [72] [87]. In fact, GaP has the highest bandgap of all commonly explored semiconductor materials with n >3 throughout the visible range [88]. These properties make GaP uniquely suited for many advanced optics applications implemented using high contrast gratings.

High index contrast allows strong confinement of light due to the change in amplitude of the electric field at an interface [89]. This confinement allows the use of subwavelength structures to guide and otherwise interact with light, which is necessary for the fabrication of highly integrated photonic devices [90]. The confinement within a slot waveguide, for example, is given by n_H^2/n_S^2. The systems explored by Almeida at el. are Si-air and Si-SiO_2, usable with low losses only beyond the Si band gap; in this case, the telecom wavelength 1.55 µm is discussed. Use of gallium phosphide would extend the usable wavelength for this type of device well into the visible.

Aside from waveguides, a diverse array of devices are possible by exploiting high index contrast. Metasurfaces created with high index contrast materials can affect the resulting wave with excellent control over phase and polarization [91]. Applications include both filters [92] and lenses [93] created with subwavelength flat surfaces. The transparency and high index of GaP make it ideally suited for use in these types of devices.

Another property that makes GaP interesting for optical applications is a high second-order non-linear optical coefficient [94]. Potential devices which exploit this property are parametric down-converters and frequency sum/difference generators [95]. Gallium phosphide resonant cavities which can be used to measure non-linear effects have previously been fabricated on free standing GaP membranes, grown on a sacrificial AlGaP layer [96]. The transfer of thin GaP films would allow the fabrication of larger devices and more robust devices, with a fabrication scheme that is potentially simpler and less expensive.



(a) GaP mesa patterned with photolithography and metalized through a shadow mask

(b) Metal contacts thickened and sample attached to glass with crystalbond wax

(c) Silicon substrate removed with XeF_2 etch

Figure 5.5: Schematic of GaP substrate removal process

5.4.2 Substrate Removal Process

A schematic of the substrate removal process is shown in figure 5.5. First, a mesa etch is performed on the GaP films. A 0.2 inch square or cloverleaf shape appropriate for Hall effect measurements is patterned by photolithography. Shipley 1813 resist is spun at 3000 RPM for 30 seconds, and exposed for 10 seconds using a plastic transparency mask. We develop in Microposit MF-319 developer for about 2 minutes, and hard bake at 115 °C for 5 minutes.

Several etches were explored, but most consistent results were obtained using a 5:1:1 mixture of deionized water, 97% sulfuric acid, and 30% hydrogen peroxide, as described by Barycka *et al.* for GaAs etching [97]. The etching solution must first be mixed at room temperature, then heated to 70 °C. Etch times for 300-500 nm GaP films vary from approximately 5 minutes to 30 minutes, depending on the quality of the GaP film. Completion is judged by eye and confirmed by dipping in buffered hydrofluoric acid; bare silicon will quickly become hydrophobic, while GaP will remain hydrophilic.

The mesa etch also creates a sharp edge which allows thickness measurements to be performed using a stylus contact profilometer. Thicknesses were noted and later used to extract resistivity from the measured surface resistance. Measured growth rates varied very little; all thickness measurements were within 10% of the target thickness.

Following the mesa etch, ohmic contacts are evaporated through a shadow mask onto the corners of the sample. The shadow mask was made from polyimide film and purchased from oshstencils.com, which sells stencils for PCB solder paste application for less than $10. It was then mounted on a stainless steel disc with 1 cm^2 squares cut with a water jet, shown assembled in figure 5.6. This setup was fast and extremely inexpensive to fabricate, and allowed us to rapidly mount samples with the contacts aligned to the mesa corners with excellent precision. For n-type GaP, we use a Au/Ge/Ni contact [98], formed by evaporating a six layer stack consisting of:

5 nm Ni
45 nm Au
45 nm Ge
50 nm Au

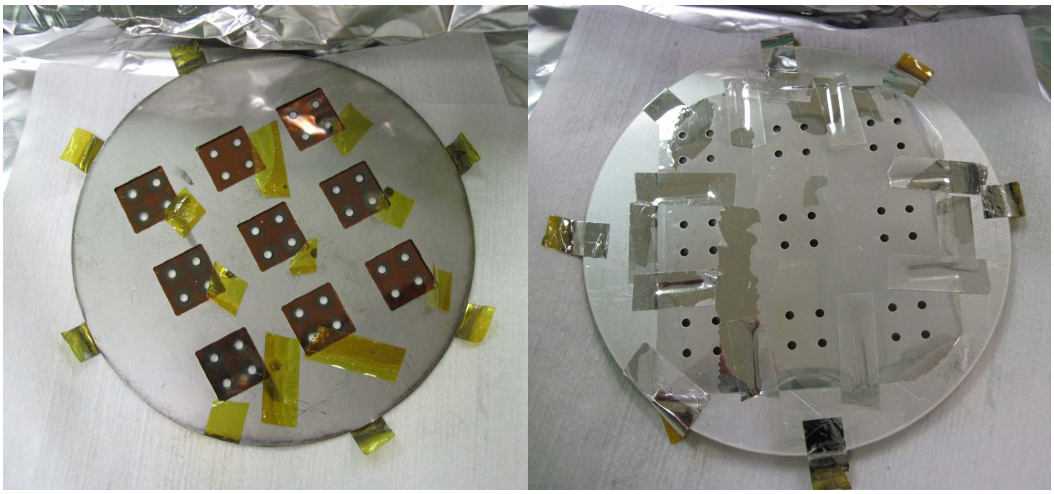


Figure 5.6: Shadow mask for deposition of Hall effect measurement contacts on 1 cm^2 substrates. Samples are mounted and taped into the slots on the rear (left), and deposition is through the front (right). Contact center to center spacing is 0.2 inches.

20 nm Ni
50 nm Au

For p-type GaP, we use a Ni/Zn/Au alloy [99] formed by a four layer stack consisting of:

5 nm Ni
45 nm Au
5 nm Zn
50 nm Au

Both contact types are annealed for three minutes at 480 °C under a forming gas (5% H_2 diluted in N_2) atmosphere. We then evaporate 300-500 nm of silver through the same shadow mask to ensure that the contacts are continuous over the edge of the film and robust to contacting.

The contacted film on substrate is then attached to a glass slide handle using Crystalbond 509 adhesive. The glass and crystalbond are placed on a hotplate set to 150 °C and the substrate with GaP film brought into contact with tweezers. The excess is then squeezed out by hand, the sample moved around to remove air bubbles, and left on the hot plate to cool slowly. The silicon wafer is then etched with a pulsed XeF_2 vapor etcher, with an etching pressure of 2000 milliTorr and pulse time of 45 seconds. It was important to purge thoroughly between pulses in order to give the sample adequate time to cool; the XeF_2 etch is quite exothermic, and the bonding waxes are susceptible to melting. This silicon dry etch was chosen for the substrate removal process due to its high selectivity for silicon over glass, most organics, and most metals [100] and generally gentle etching action. Potassium hydroxide silicon etching was attempted, but resulted in adhesion problems between the film and the substrate.

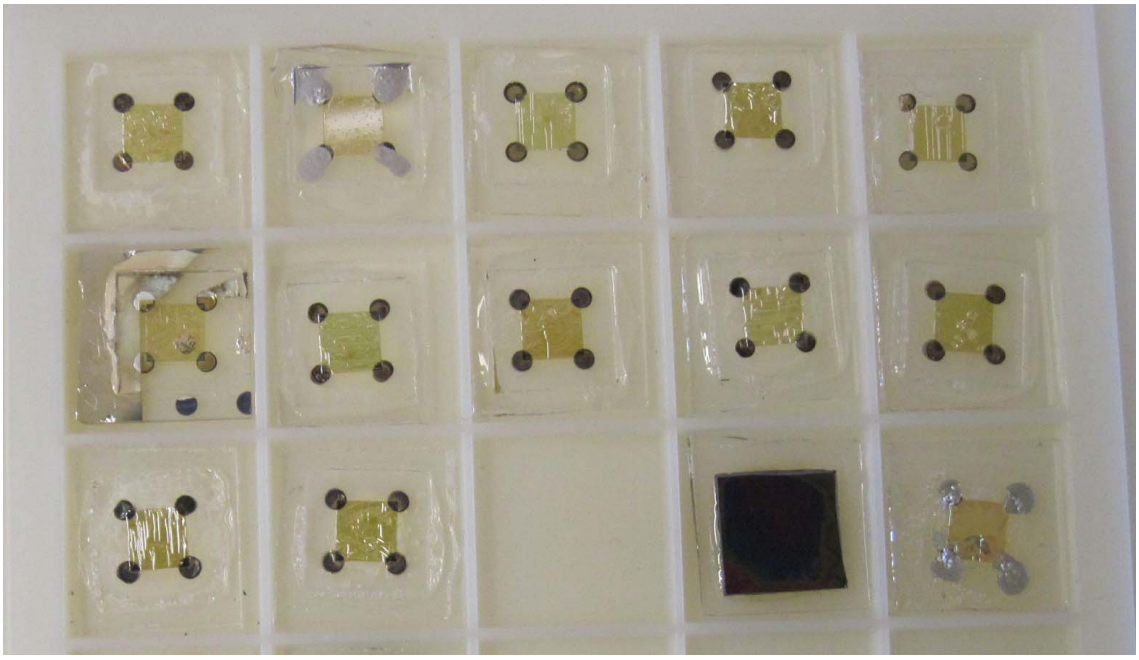


Figure 5.7: Photograph of GaP films following substrate removal with a crystalbond wax interlayer. Macroscale roughness is visible in some samples, and cracking in others. The sample second from the left in the top row exhibited neither defect. For scale, contact center to center spacing is 0.2 inches.

The result is a GaP film bound to glass with transparent wax and contacts for Hall measurements. These substrate-removed films had four continuous contacts with a yield of approximately 30-40%. Most films that remained flat cracked, while samples which exhibited buckling were more likely to be continuous. A photograph showing differences between samples is presented in figure 5.7. Samples which displayed waves or buckles had a texture several microns in height, with spacing on the order of one hundred microns. A height profile of a typical sample, measured with confocal microscopy, is shown in figure 5.8. These samples often also showed some bubbling within the crystalbond wax, and may have been a result of outgassing or localized melting and solidification. In order to mitigate outgassing issues, samples were remelted in a vacuum furnace prior to substrate removal, but this had no noticeable effect. It is also possible that internal stresses in either the film/substrate or film/wax interface prior to substrate removal caused inconsistencies between samples. One notable exception remained both flat and uncracked. This sample was processed in parallel with others, and unfortunately, it remains unknown why this sample was more successful, and how to reproduce this result.

Black wax (Apiezon Wax W) was also investigated as an interlayer. It was first dissolved in trichloroethylene and drop cast on glass. The sample was then brought into contacts and the

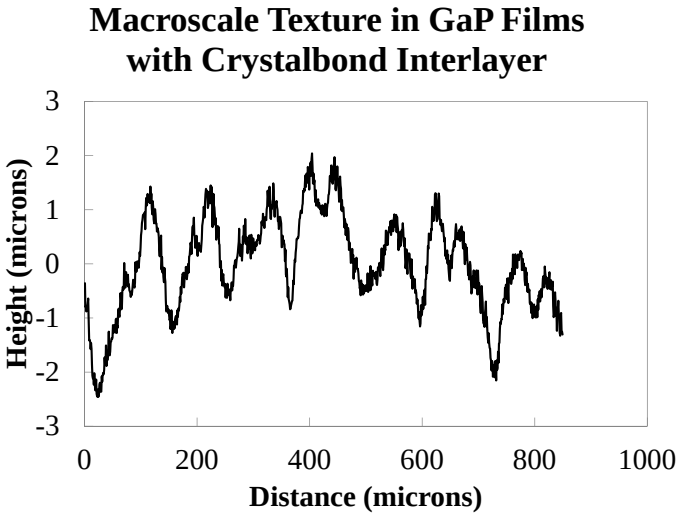


Figure 5.8: Height profile measured by confocal microscopy of typical macroscale texture GaP film with a crystalbond interlayer.

edges cleaned with additional trichloroethylene. The samples were then baked to drive off remaining solvent. Results were similar to crystalbond, and crystalbond was preferred for processing simplicity.

A second process was developed with the help of several members from the Faraon group. An SU-8 2002 (MicroChem) interlayer was used instead of the wax. The following process was used:

1. The sample and glass slide (Eagle XG 20/10, Coresix) were thoroughly cleaned with solvents and N_2, and baked at 180 °C for 5 minutes to dehydrate.

2. SU-8 2002 was spun on both the sample and the glass slide at 3000 RPM for 30 seconds. If any particles are present distorting the resist, the surface was re-cleaned and dehydrated.

3. Both the glass and sample were then soft baked for 2 minutes at 95 °C.

4. The sample was brought into contact with the glass, then baked for 30 minutes in a convection oven at 95 °C.

5. The sample was then placed in a Suss wafer bonder with 500 mbar of pressure at 95 °C.

6. the SU-8 was hardened with a 1 minute flood exposure using 365 nm light through the glass and a 20 minute hot plate bake at 180 °C.

Again, XeF_2 was used for the substrate removal etch, due to reports of adhesion problems with alkaline etches [101]. The resulting films were reliably smooth and flat, compared to the macroscale texture observed in most of the samples with a wax interlayer. Thorough cleaning is necessary to ensure a high quality wafer bond. This is easier to perform on plain GaP samples without metal

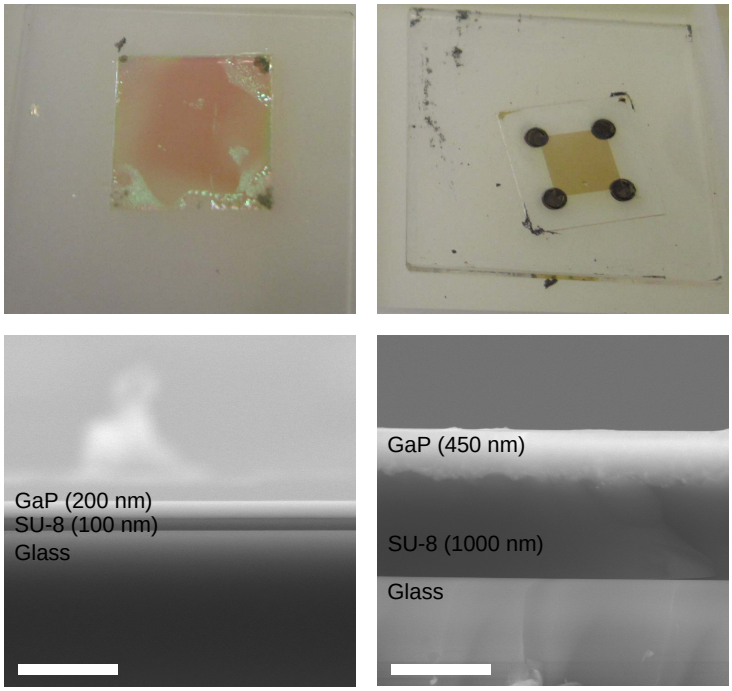


Figure 5.9: Photographs (top) and cross sectional scanning electron microscope images (bottom) of substrate removed GaP films without (left) and with (right) electrical contacts. The contacts act as spacers, increasing the thickness and improving the uniformity of the SU8 layer. The film without contacts is 1 cm wide, and the Hall sample was etched to 0.2 inch wide. The scale bars in the SEM images is 1 micron.

contacts; on the Hall effect samples, the high viscosity of SU8 2002 and resulting thick interlayer is therefore important to achieving a high quality transfer. SU8 2002 was chosen for its ability to conform to roughness or particles between the films. The thickness after spinning should be approximately 2-3 µm on each side, and following wafer bonding, the thickness was measured by Filmetrics spectral reflectance to be approximately 1.5 µm. On samples without the metal contacts, the interlayer was significantly thinner, since the metal does not act as a spacer and more SU8 can be removed during the wafer bonding process. Cross sectional scanning electron microscopy images of samples with and without contacts are shown in figure 5.9. The roughness of the contacted sample was a result of the growth process, rather than the wafer bonding and substrate removal process.

An attempt was also made to re-transfer a GaP film with a crystalbond interlayer to a glass slide, using only van der Waals attraction to bond the film. A small drop of water was placed on the sample and it was brought in contact with a glass slide. When mostly dry, the sample was submerged in acetone to remove the wax. While most of the sample flaked away, a few approximately square regions, with lengths of approximately 200 µm, remained adhered to the glass. An image of one such region is shown in figure 5.10. There is likely room to improve this process, perhaps by using solvent vapor to remove the wax to help maintain the contact between the GaP film and the glass.

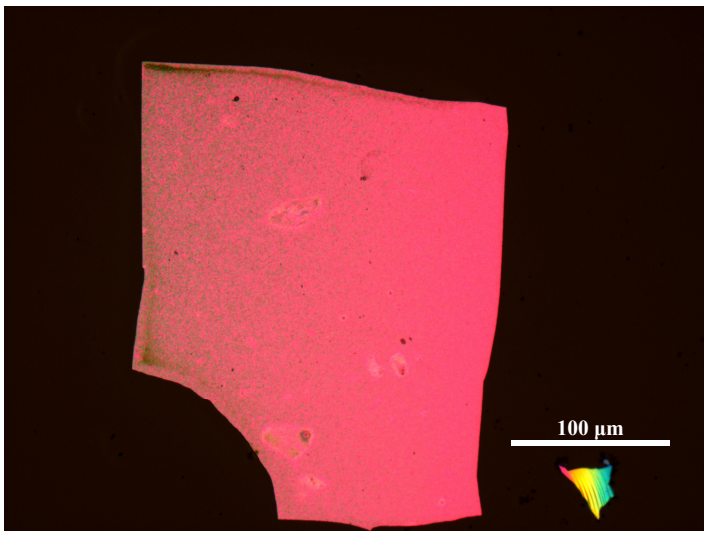


Figure 5.10: Optical image of GaP bonded directly to glass. Several regions of the same approximate dimensions transferred successfully.

5.4.3 Electrical Measurements

In order to measure doping densities and mobilities in GaP films, Hall measurements were performed on the substrate removed samples with four continuous contacts. Results are shown in table 5.1. Successful p-type doping was achieved using cyclopentadienyl-magnesium (CP_2Mg). Hole concentrations in the mid $10^{18}cm^{-3}$ range and mobilities in the range of 10-15 $cm^2\,V^{-1}\,s^{-1}$ agreed well with the results obtained by Li et al. for growth on gallium nitride [102]. Consistent with their results, continuing to increase the dopant concentration beyond that which resulted in mid 10^{18} cm^{-3} carrier concentrations resulted in an increase in resistivity, and difficulty in performing Hall effect measurements, likely due to a drop to a very small mobility. A slightly higher hole concentration of approximately 10^{19} cm^{-3} and mobilities in the range of 30-40 $cm^2\,V^{-1}\,s$ were reported by Lee at al. on window layers for AlGaInP LEDs [103], also grown my MOCVD. The highest reported values for mobility of above 60 $cm^2\,V^{-1}\,s^{-1}$ at 2×10^{19} cm^{-3} were achieved in thick films grown by horizontal sliding boat liquid phase epitaxy from a 850 °C Ga melt [104].

Due to inconsistencies between growths from different trips to Berkeley, low yield in the substrate removal process, and a limited supply of samples, more reliable trends and statistics could not be measured. Still, these samples fit well with the literature results for magnesium doping in GaP, and likely represent close to the upper limit of achievable carrier density. There is a chance that the mobility, and thus the conductivity, could be improved modestly by further reducing the defect density in the films.

Silicon, which is widely used as an n-type dopant in many III-V semiconductors, including GaInP

Table 5.1: Gallium Phosphide Hall Effect Measurements

Growth Number	Substrate Orientation	Dopant	Dopant Flow (sccm)	Sheet Resistance ($\Omega/\square$)	Resistivity (Ω-cm)	Mobility (cm^2/V-s)	Density (cm^{-3})	Carrier Type
4245	112	Mg	75	39,125	1.10	0.9	7.0e+18	Holes
4273	112	Mg	25	50,800	2.54	15.63	1.6e+17	Holes
4274	100	Mg	50	2,990	0.15	9.11	4.6e+18	Holes
4275	100	Mg	75	2,380	0.12	9.31	5.6e+18	Holes
4277	100	Mg	150	13,520	0.68	<5	?	Holes
4323	100 SOI	Mg	200	6,535	0.20	-	-	-

[105], and has been shown to be an effective dopant in GaP crystals [106], was evaluated as a dopant in MOCVD grown GaP films. Originally, silane (SiH_4) was used as a silicon precursor. While no substrate removed Hall effect samples were successfully fabricated, these samples showed some evidence of n-type doping, including showing diode-like behavior in heterojunction devices, and revealing evidence of a shift in the Fermi level by x-ray photoemission measurements performed by Rebecca Saive. It is possible that the silicon was acting as a donor, but the achievable concentrations were likely low due to its low rate of thermal decomposition at growth temperatures [107]. It is also likely that unintentionally doped MOCVD grown GaP will contain defects that act as donors [108].

In an effort to achieve higher donor concentrations, we later switched to disilane (Si_2H_6) due to its higher cracking efficiency. Growths using high flow rates of Si_2H_6 resulted in gray films which showed high Si content in X-ray photoemission spectroscopy measurements, proving incorporation in the films. However, 4-point conductivity experiments on substrate removed films with lower flow rates exhibited extremely high resistivities, in most cases unmeasurably high. It is suspected that this is caused by a compensation effect in silicon incorporation — silicon sits on both Ga and P sites, causing ineffective doping, but it is also possible that the contacts or some other process failed, or that the doping concentration is too low to measure. More work must be done to determine the cause and/or to achieve effective n-type doping. The most promising next step to achieve higher n-type doping is to add a group VI doping precursor, such as H_2Se or $Te(C_3H_3)_2$ [109].

5.4.4 Optical Measurements

Transmission measurements were performed on the GaP/wax/glass structure in the spectrophotometer equipped with an integrating sphere described in section 4.3.3. Transmission measurements were normalized to a reference spectrum consisting of wax and glass. A Tauc plot (photon energy vs $(\alpha h\nu)^{1/r}$) was generated from the normal incidence transmission data and used to extract the bandgap, as shown in figure 5.11. The features in the transmission data at photon energies below the bandgap likely result from Fresnel reflections between the GaP film, wax, and glass. Reflection data showed peaks in similar locations, but the magnitudes did not fit to fully account for all the

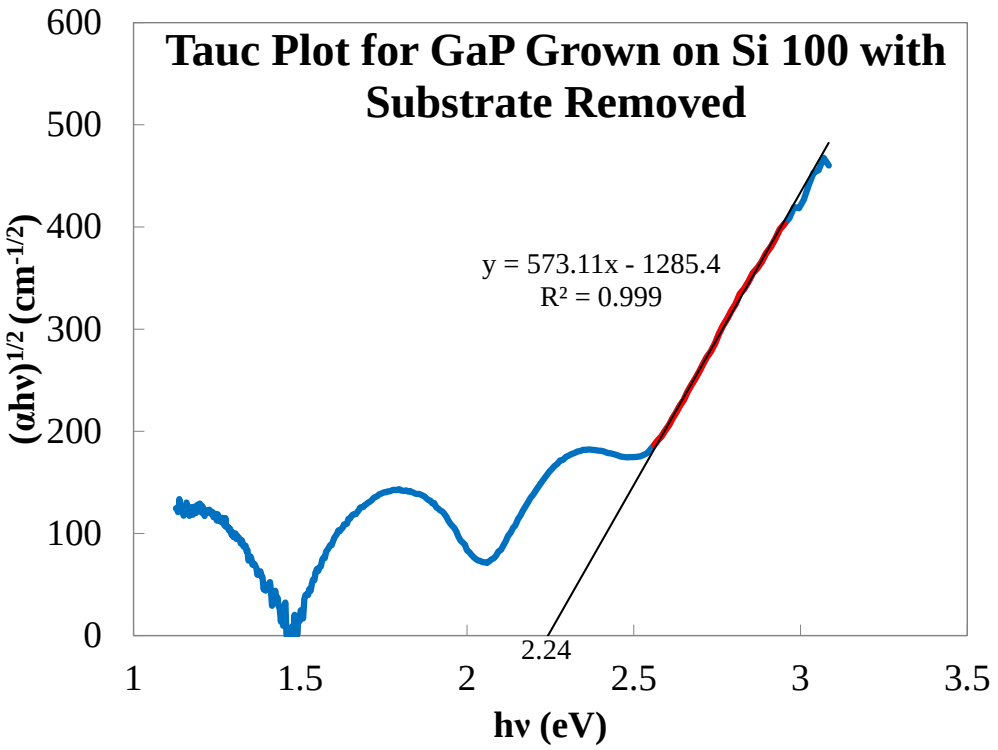


Figure 5.11: Tauc plot generated from normal incidence transmission measurements of a substrate removed GaP film. A linear fit was generated from the red data points, selected to maintain $R^2 = 0.999$, and indicates a bandgap of 2.24 eV.

losses in the transmission measurements. Discrepancies could arise from slightly different mounting angles or different spots, as the sample was not entirely flat, or from absorption within the wax. The Tauc plot is linear near the expected band edge, with a good fit to r=2, indicating an indirect bandgap. The extents of the fit were selected to maintain an R^2 value of 0.999. We can extrapolate this curve to extract a bandgap of 2.24 eV, in good agreement with the accepted value of 2.26 eV [72].

5.4.5 Time Resolved Photoluminescence

Time resolved photoluminescence (trPL) measurements were performed in the Joint Center for Artificial Photosynthesis laboratories, in collaboration with Dennis Friedrich. The source was a Coherent Libra Ti:sapphire laser, fed into an OPerA solo OPA, equipped with nonlinear optics capable of a variety of outputs. A 360 nm excitation pulse was chosen. A 364 nm long pass filter was used to block the primary beam, and a Hamamatsu C10910 streak camera was used to acquire both spectral and time resolved data. Hamamatsu's HPD-TA 9 software was used for spectral peak fitting.

We found that substrate-removed samples provided enough signal to perform measurements,

compared to on-substrate films which did not. This is to be expected; gallium phosphide has a high index of refraction of approximately 4 near its emission peaks, well matched to the silicon substrate, which absorbs strongly at these wavelengths. Therefore, luminescesed light which reaches the back surface will be transmitted to the silicon substrate and absorbed with a high probability. The front escape cone can be calculated using Snell's law:

$$\Theta_c = \sin^{-1}\left(\frac{1}{n_{GaP}}\right)$$

and considering the fraction of solid angles intercepted by this front escape cone:

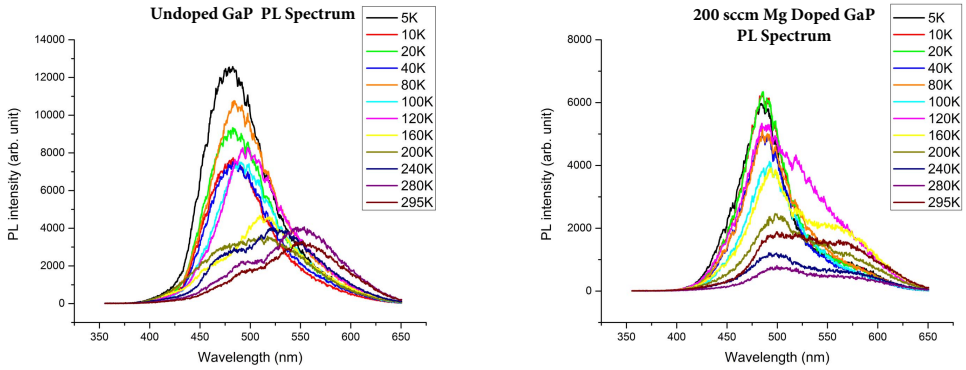
$$\frac{\Omega_{escapecone}}{4\pi} = \frac{1}{2}(1 - \cos\theta_c) = 0.016$$

We find that we expect only 1.6% of the total photoluminescence signal to escape the on-substrate sample. In contrast, light incident on the rear of the sample will not be lost in the substrate removed sample, and we expect a much higher fraction of light to escape. Additionally, these samples were easier to see, and thus resulted in better alignment. Both photoluminescence spectra and decay times were measured at different doping concentrations with the temperature varied between 5 K and room temperature.

Photoluminescence spectra of an undoped and highly doped sample are shown in figure 5.12. At low temperatures, the primary emission peak for both samples was located at approximately 480 nm. As the temperature increases towards room temperature, the undoped sample develops a second peak at approximately 550 nm, which corresponds to the primary indirect energy gap at 2.26 eV [72]. In the heavily doped sample, good fits can be generated by considering the peak either broadening from a width of 38 nm to 47 nm, or shifting to 565 nm. Regardless, we are able to observe emission to the acceptor states, and see that they are close to the band edge.

Lifetimes were extracted from the time decay information, and were very similar for all samples and independent of temperature. Lifetimes were strongly double exponential, with an initial decay of characteristic lifetime of 0.5-1.5 ns, followed by a secondary 3-5 ns decay. Lifetimes were on the shorter end for the highest doped sample, but more measurements would need to be performed to extract significance from this trend. Normalized decay profiles of this sample are shown in figure 5.13. For reference, the highest electron lifetimes reported in p-type GaP are on the order of 120 ns [110].

At room temperature, this lifetime corresponds well to the surface limited lifetime expected in our thin film. Assuming the mobility is approximately $1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, similar to the measured mobility of sample #4245 (as in table 5.1) of the same series, $\mathrm{D} = 0.026\,\mathrm{cm^2\,s^{-1}}$. We can calculate the surface limited lifetime assuming very high surface recombination velocities on an unpassivated surfaces at room temperature [111]. Using



(a) Photoluminescence spectra of undoped GaP (b) Photoluminescence spectra of Mg doped GaP

Figure 5.12: Photoluminescence spectra of undoped and heavily Mg doped GaP films between 5K and room temperature. The second peak, which appears at higher temperatures and corresponds to the indirect bandgap, red shifts in the doped sample.

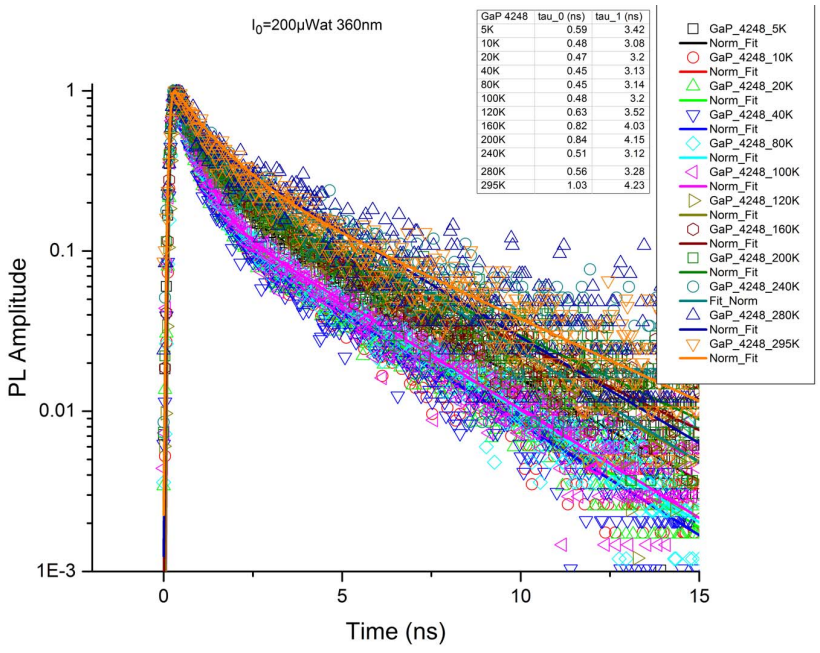


Figure 5.13: Time decay of the photoluminescence signal in the heavily doped sample, together with fits and lifetimes extracted from these fits. As discussed, the lifetime is not a strong function of temperature.

$$\tau_S \approx \frac{W}{2S} + \frac{1}{D}\left(\frac{W}{\pi}\right)^2 \text{ [112]},$$

we calculate a surface limited lifetime of 3.5 ns. We expect both the surface recombination velocity S and diffusivity D to decrease with temperature, which should cause an increase in effective lifetime if it is limited by surface recombination. However, as mentioned earlier, this effect was not observed; lifetimes were relatively constant as a function of temperature. Therefore, more measurements would be needed to fully understand the minority carrier recombination sources in our GaP films. It would be informative to measure samples with a different thickness, and from the series which exhibited higher mobilities. Unfortunately, by the time new samples were prepared, the pump laser on the trPL setup began to have problems, so this work must be left for another time.

5.4.6 Material Characterization of Substrate Removed Films

As discussed previously, aside from affording us the opportunity to characterize the gallium phosphide grown on silicon, the substrate removed films present unique opportunities for devices based on the optical properties of GaP. We therefore performed further characterization of these films to evaluate their suitability to other applications.

Crystallinity of GaP films following the substrate removal process was confirmed using X-ray diffraction, with the help of Chris Chen. Samples were measured before and after the substrate removal process, and as expected, the crystalline, oriented films maintain their crystallinity following substrate removal, as shown in figure 5.14. Similarly, samples from poor growths which resulted in non-oriented GaP films maintained their same orientation following substrate removal.

The substrate removal process with an SU-8 interlayer was performed on full 1 cm^2 samples as well. In general, the resulting films had more variation in thickness of the interlayer. Spin coating the SU-8 film on a small, square sample resulted in edge effects which were difficult to remove. Additionally, the metal contacts act to dictate the spacing between the GaP film and glass, maintaining a more constant spacing. Improvement to the process could likely be made by using round samples and proper edge bead removal techniques, or mesa isolated structures and spacers to maintain interlayer uniformity, as in the Hall effect samples. This effect was difficult to capture or quantify, but was apparent when observing the thin film interference colors caused by the interlayer.

A variety of surface defects were observed in these samples. Optical microscope images depicting these are shown in figure 5.15. Image A depicts a sample with large pinholes, surrounded by regions of high quality. These pinholes likely formed during the mesa etching process; as mentioned, some samples etch slower than others, which is enough time for the photoresist to be attacked. The features in image B appear to depict the relaxation of strain within the film. It is not clear if this strain was between the film and the growth substrate or the interlayer. Images C and D depict

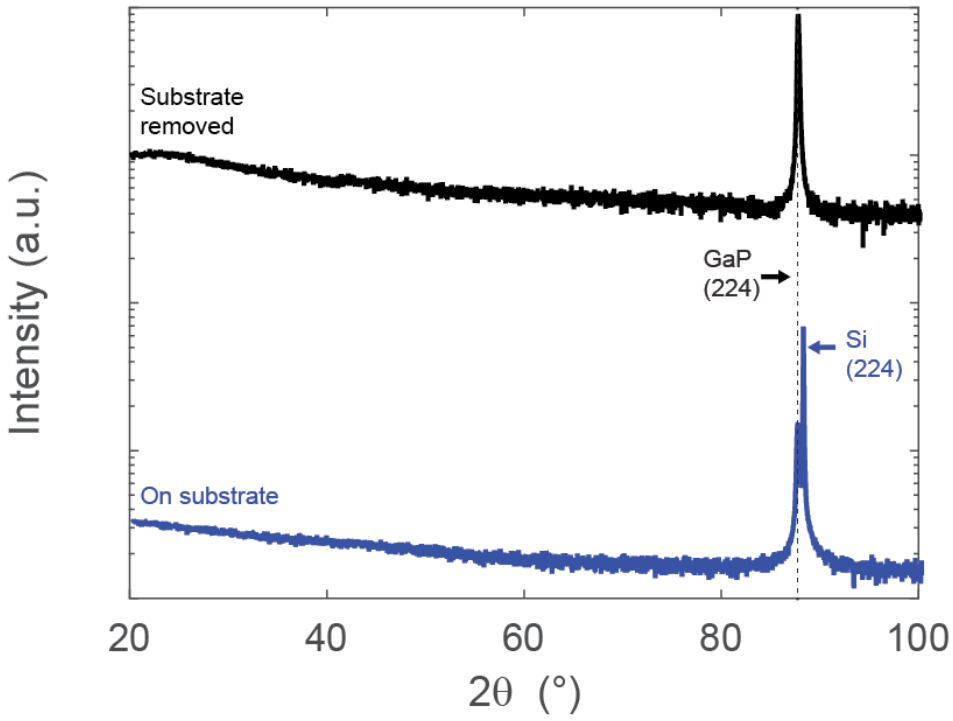


Figure 5.14: X-ray diffraction measurement of GaP film, before and after the substrate removal process. The only notable difference is the presence of the silicon peak while the substrate is present.

different microscale voids in the SU-8 interlayer. In image D, by observing the edge of the mesa, it is apparent that these voids are preset in the SU-8 layer, and not the GaP film.

5.5 Silicon-Gallium Phosphide Heterojunction Devices

Simple gallium phosphide on silicon heterojunction devices were fabricated. Edges were isolated using a mesa etch process similar to that used for Hall measurements. Instead of photolithography, a swab with acetone was used to remove the photoresist from the edges, before a hard bake and chemical etch. Ohmic contacts were then applied to the GaP by evaporation through a shadow mask. Rear ohmic contact was made to the silicon by scratching eutectic gallium-indium into the rear surface with a diamond scribe, and attaching the sample to conductive copper tape. Thicker GaP films (500 nm) were used for devices, as alloyed ohmic contacts had caused shunting in some samples with 300 nm thick films; more work must be done to mitigate this effect in actual devices.

Devices were made with both n-GaP on p-Si and p-GaP on n-Si. Based on theoretical predictions from the Anderson model, we expect a significantly smaller conduction band offset than valance band offset, which would lead us to expect better performance from p-type base devices. However, X-ray photoemission spectroscopy measurements indicated that the valence band offset is significantly

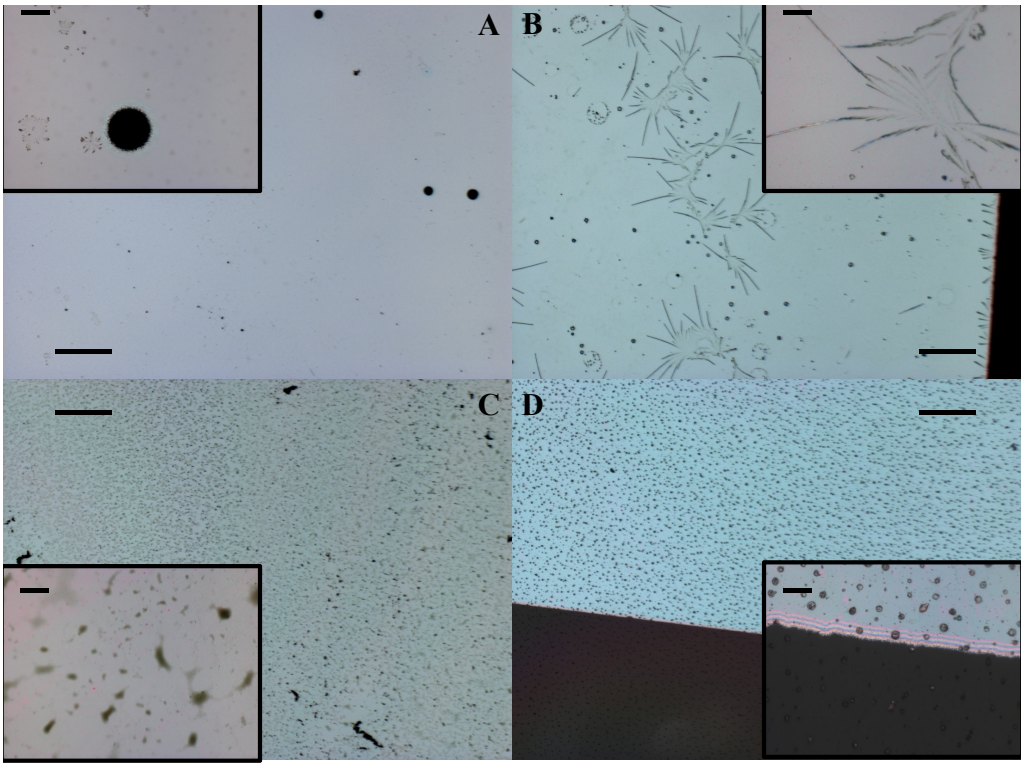


Figure 5.15: Optical microscope images depicting the surface quality of substrate removed GaP films. As shown, a variety of different surface defects were observed. Large image scale bars are 200 µm and inset scale bars are 20 µm.

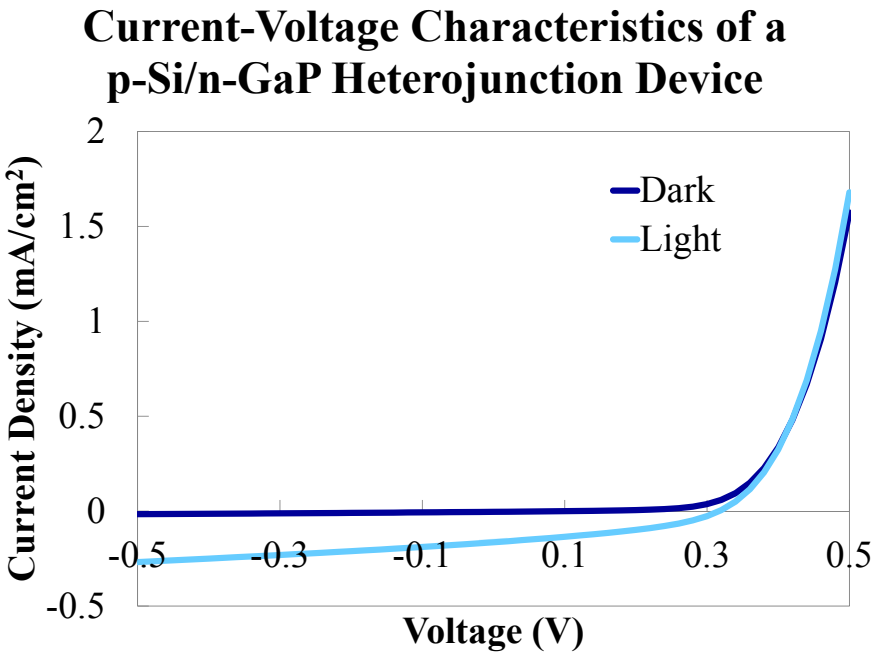


Figure 5.16: Current-voltage characteristics of an n-GaP/p-Si heterojunction device. V_{OC} = 317 mV, J_{SC} = 0.16 mA, FF = 38%.

smaller than theorized, indicating that a device with an n-type base may yield higher performance. Additionally, we were able to reach higher doping densities in p-type gallium phosphide than n-type. As simulated in section 5.2, a high emitter doping density can mitigate the effects of a defective interface or high interface barrier.

The current-voltage characteristics of a simple device with a p-type Si base and n-GaP emitter , grown with moderate silane flow, are shown in figure 5.16. As discussed in section 5.4.3, while silane was not an effective dopant, we expect unintentionally doped films to be doped lightly to moderately n-type. There are several possible explanations for the poor device performance. We confirmed that our contacts did indeed make ohmic contact as expected by measuring linearity between two similar contacts on plain Si and substrate removed GaP.

While the contact to the GaP layer was likely to be good, spectral response measurements were performed to confirm that the low current was not a result of current only being generated in the GaP emitter layer. Results are shown in figure 5.17. As evident in the figure, there were some issues with the measurement, especially around the filter crossover point at around 850 nm and near the silicon band edge. Additionally, these measurements are not quantitative; integrated spectral response in this sample yields a photocurrent higher than the measured J_{SC}. This is likely due

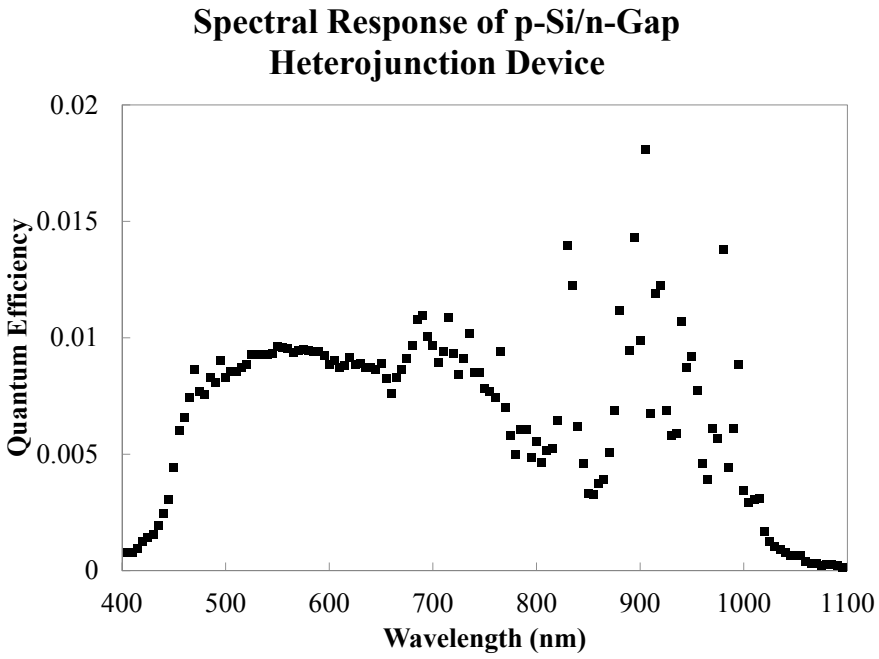


Figure 5.17: Spectral response of n-GaP/p-Si heterojunction device. Despite poor device performance and presence of several measurement artifacts, it is clear that silicon is acting as the absorber material in this device due to current response out to the silicon band edge.

to poor uniformity of the illumination spot. Measurements on a reference cell are reproducible as long as it is not moved, but after the reference is moved and replaced, the peak quantum efficiency will shift by a factor of approximately two. Regardless, current was clearly extracted uniformly throughout the visible and near IR to the silicon band edge, beyond the GaP band edge. This indicates that the current measured is in fact generated in the silicon, rather than, for example, a Schottky junction formed between the GaP and the top contact. The drop in collection efficiency in red light which is observed if averaging through the measurement noise is expected, due to the recombination active ohmic contact and absence of back surface field on the rear of the device.

Therefore, the low current in this device is likely a result of a property of the Si/Gap interface. The most likely explanation is a high barrier coupled with defects at the interface. This causes most carriers to recombine before they can be transported out of the device. The high barrier can also lead to the high series resistance/low fill factor observed, while still maintaining decent device characteristics in forward bias. While an exact match of the I-V curve was not realized in simulation, similar trends including a normal diode curve in forward bias, decent open circuit voltage, and extremely low short circuit current and fill factor were observed in simulations with a high barrier and surface defects. Additionally, X-ray photoemission measurements confirm that the

barrier is likely high, and lifetime measurements indicate a recombination active interface.

Devices formed by p-GaP emitters grown on n-type silicon bases also gave poor device performance, with a wide variety of issues. Many showed significant shunting or poor barrier formation, with extremely conduction in reverse bias. Others showed decent rectification, but with barriers in the opposite direction. Again, contacts were expected to be ohmic. More work must be done to determine the source of issues in these devices; improved reproducibility in the GaP growth process would likely make this task significantly easier.

5.6 Conclusions and Outlook

Gallium phosphide holds promise for use in heterojunction solar cells. Many steps were made towards realizing devices by growth of GaP on silicon by MOCVD. High lifetimes were measured on isotype heterojunctions, indicating that we have successfully maintained the bulk wafer lifetime by adding a silicon nitride coating to the back of the device, and that the bands at the surface are not completely pinned to midgap by defects. A substrate removal process was used which allowed us to measure the doping and photoluminescence of GaP films, and both indicate high quality p-type doping by incorporating cyclopentadienyl-magnesium in the growth process. Additionally, this substrate removal process has potential for use in a wide variety of advanced optics applications.

Despite this progress, ultimate device performance was poor, failing to reach the predicted high efficiencies. Recent results by Darnon et al. [85] show significantly better devices using GaP heterojunctions. Further work from the group [113] indicates that a high temperature annealing step is required to achieve high quality GaP growth with low interface defect density. This aligns with the hypothesis that our poor device performance is due to high interface state density. More work must be done in growing GaP on silicon with a high quality interface to realize working devices and eventually see the promised performance gains. This will likely require more careful surface cleaning and treatment prior to growth.

Chapter 6

Lateral Transport in Silicon Heterojunction Solar Cells

6.1 Introduction

Amorphous silicon/crystalline silicon heterojuction solar cells hold the potential to form high efficiency solar cells at low cost. Efficiencies above 23% have been achieved and open circuit voltages are the highest among silicon solar cells [4]. Furthermore, the a-Si:H emitter and back surface field depositions are performed at low temperatures, which has the potential to minimize processing costs.

Despite the age of the technology — the original patent was published in 1991 [114] — research groups have been slow to approach the voltage records set by Sanyo [82]. This difficulty is caused by defects at the interface. The importance of maintaining a clean interface and avoiding conditions that allow epitaxial silicon deposition is well known [115]. To fully understand the device's sensitivity to defects, the carrier transport around the heterojunction interface must be analyzed.

Transport across the heterojunction is significantly different from transport through a homojunction device. Due to band bending induced by the heterojunction, an inversion layer forms in the region just below the metallurgical junction [116]. This can be seen in the band diagram for this type of device, shown in figure 6.1 [117]. In the n-type base, p-type emitter configuration that is mostly commonly used, the c-Si/aSi heterointerface presents a valence band offset of about 0.45 eV [115]. Though charge separation occurs in the inverted region of the crystalline silicon, holes must still pass through this barrier before being extracted. Possible mechanisms include direct tunneling, hopping through band tail states, and thermionic emission across the barrier. Regardless of mechanism, there is a characteristic dwell time for carriers at the heterointerface [118]. Additionally, the high concentration of holes in the inversion layer allows for relatively high conductivity. These two parameters determine the characteristic lateral transport length of carriers in the inversion layer. Two experiments were performed in order to directly probe the carrier dynamics in the inversion layer.

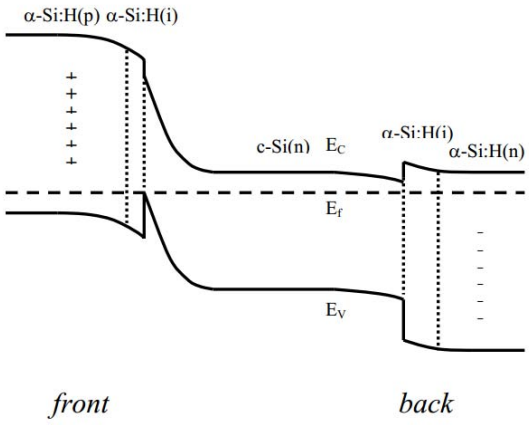


Figure 6.1: Band diagram of a crystalline silicon/amorphous silicon heterojunction device with an n-type crystalline silicon base. Note that inversion of the n-type crystalline material occurs below the physical junction. [117]

6.2 Simulation

The original inspiration for this work was a series of simulations performed by Michael Deceglie, attempting to answer the question of why the performance of silicon heterojunction cells is so sensitive to defects [119]. The simulated structure included an isolated region of defective epitaxial crystalline silicon embedded in the intrinsic amorphous silicon interfacial layer and covering 5% of the surface. The simulation revealed transport of minority carriers away from the high quality regions and towards this defect, resulting in a significant drop in voltage as the defect concentration was increased.

Following this study, we wished to confirm the results of these simulations with experiment. However, it is not possible to experimentally observe the movement of carriers within the material, as it is in a simulation. Additionally, in the aforementioned simulation the carriers are lost rather than collected. One method to probe the action of defects is to measure the effective cross section of the defect, the area around which a defect can cause recombination. A second, more direct way to probe carrier motion is to extract a current from the carriers that moved laterally. Both approaches were taken and discussed in the next section. In order to extract laterally transported current, we designed an experiment which varied the thickness of the intrinsic amorphous silicon layer in order to vary the barrier for transport across the heterojunction. This structure included two contacts directly above regions with different thicknesses of i-aSi, as shown in figure 6.3. This was simulated using Synopsys Sentaurus TCAD device physics simulator, with similar parameters as previously used [120]. The optical generation was simulated using the transfer matrix method, with the stripe

Table 6.1: Results from Current Splitting Simulation

Experiment		Lower Contact Current (mA/cm^2)	Upper Contact Current (mA/cm^2)
Uniform 1 sun	Control	16.0	16.0
	With hole	21.8	13.5
488 nm beam in center	Control	0.93	0.93
	With hole	1.14	0.72
488 nm beam over upper contact	Control	0.84	1.01
	With hole	1.05	0.81

command to provide localized generation, mimicking the LBIC measurements.

Both broad area and narrow stripes of illumination, mimicking light beam induced current (LBIC) measurements, were simulated. The current from both contacts was extracted separately and the difference considered. Trends in the current density were analyzed by visualizing the current density. As in the previous study, current tends to flow toward the junction until it reaches the inversion layer, then takes a sharp turn towards the region with the thinned intrinsic amorphous silicon (i-aSi) layer, as shown in figure 6.2. The results from several simulations are shown in table 6.1. In these particular simulations, the hole beneath the lower content had an i-aSi thickness of 2.5 nm, while the remaining device had 5 nm of i-aSi.

These simulations give some indication of experimental results that can be expected, but there are many reasons why the experiment may not match the simulation exactly. The exact mechanism for transport across the barrier at the heterointerface is not well understood. It is likely that one of the most important mechanisms for transport in this region is trap to trap hopping [118] between the many states close to the a-Si band edge present in the band tails. Sentaurus does not allow for this transport mechanism; it only considers transport between the band and a trap state and a subsequent recombination event or release of the carrier back to the band. This is likely because it is significantly more computationally difficult to consider the probability of transport between the numerous trap states, on the order of N_{Traps}^2, rather than N_{Traps}.

6.3 Experimental

The experimental structure used was a silicon heterojunction emitter, in which an intrinsic a-Si thin film was deposited between the c-Si wafer and doped a-Si emitter. All a-Si depositions were performed at EPFL using plasma enhanced chemical vapor deposition (PECVD), as described elsewhere [121]. The thickness of the intrinsic layer was varied in the experimental structure using a series of patterning steps. A schematic of the fabrication scheme is shown in figure 6.3. First, 300 nm of SiO_2 was deposited on a 4 Ω-cm n-type float zoned silicon wafer by PECVD for use as an etch stop. This was patterned to the area that would become the lower contact by photolithography. A 5 nm

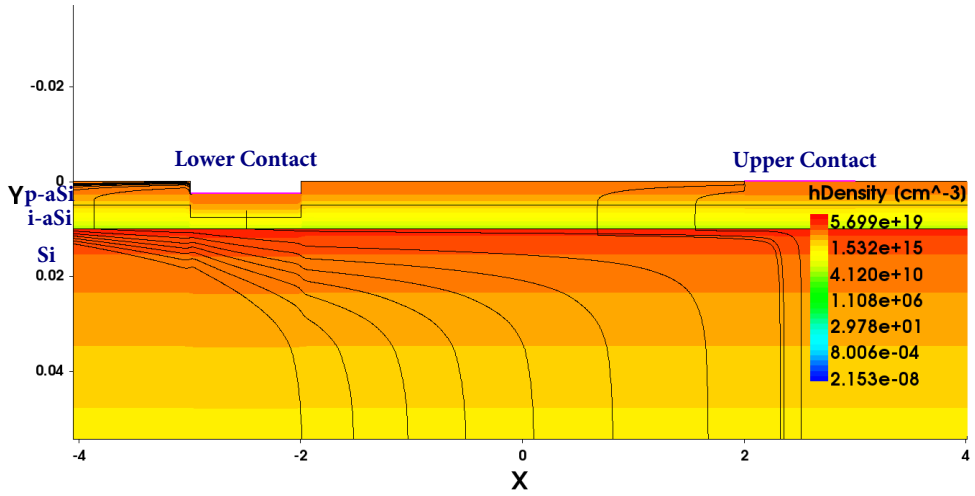


Figure 6.2: Visualized results from simulated light beam induced current experiment. The two contacts are labeled and shown in pink. The illumination source is a 488 nm beam illuminating directly over the upper contact. Current paths are traced with streamlines, and the hole density is plotted, showing the inversion layer within the silicon. Both spatial dimensions are labeled in microns.

thick initial i-aSi layer was deposited. Photolithography was again used to mask the entire sample surface except for the location of the lower contact. A XeF_2 etch was carried out for 10 s at 2000 mTorr to remove the unmasked region of i-aSi, on top of the oxide etch stop. The oxide was then removed with an HF etch and the photoresist was removed with acetone. An oxygen plasma was used to clean any remaining organics. Following a brief HF immersion, a second intrinsic aSi layer of thickness 5 nm was deposited, immediately followed by a 5 nm p-type aSi emitter and sputtered ITO top contact. A final photolithography step and HCl etch was used to remove the ITO from all regions that were not part of either contact. The resulting structures contained 80 µm wide contacts separated by varying distances above intrinsic layers of 5 and 10 nm. Control samples had the same contact geometry, but the intrinsic layer was not thinned.

6.3.1 Current Splitting Between Two Contacts

We performed a white light biased selected area illumination (WLB-SAL) experiment on the structure described above and depicted in figure 6.3. White light from a halogen lamp was used to maintain a constant photovoltage over the entire cell and a chopped 635 nm diode laser was used to locally illuminate specific areas of the sample. Both contacts were held at the same voltage as the white light bias electrically with Keithley source meters. Current from the contact under test was fed through a transimpedance amplifier with a gain of $10^5\Omega$ to a Stanford Research Systems lock-in amplifier. A schematic of this experiment is shown in figure 6.4. After recording current from both contacts, we calculated the current splitting ratio, which we define as the ratio of current collected

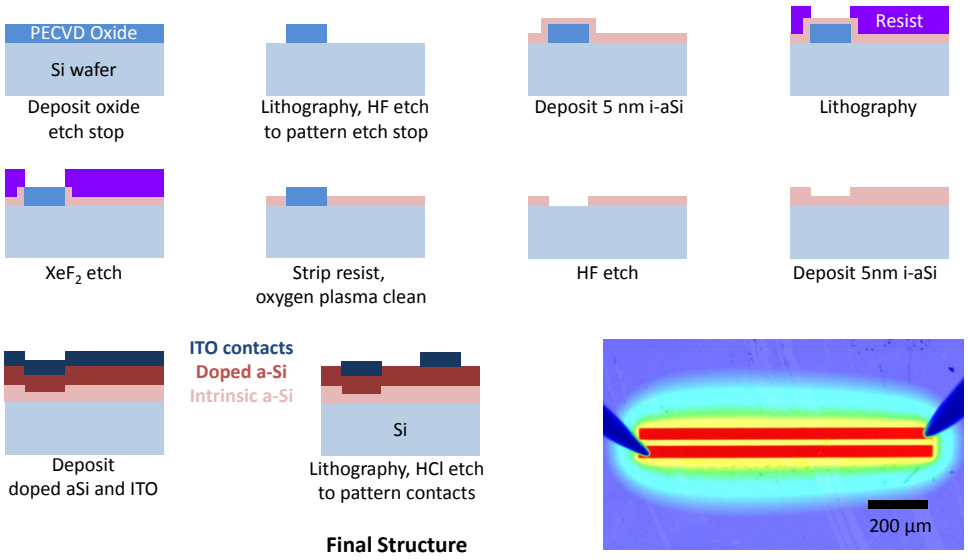


Figure 6.3: Schematic of the process used to fabricate test structure, and LBIC image (bottom right) illuminating contacts in red and showing decay of collection away from contacts

at the opposite contact to total photocurrent extracted by the local excitation.

The current splitting ratio observed when the laser is positioned directly on the upper contact is shown in figure 6.5. A significant bias dependence is observed in this measurement, with a much higher degree of current splitting at 500 mV bias than 300 mV, in both the thinned and control samples. For the closest contact pitch, more current was collected from the lower contact than the upper contact under 500 mV bias, despite the laser illumination directly above the upper contact. As the pitch is increased, this ratio decreases.

The laser wavelength was chosen so that the local excitation is absorbed adjacent to the depletion width edge, just a few microns into the material. We therefore expect carrier transport in the inversion region to be the dominant transport mechanism influencing our observations, rather than diffusion in the quasi-neutral region.

6.3.2 Lateral Transport Near a Defect

A second experiment was performed in order to probe the lateral transport length of carriers around defects. A 1 µm wide line was milled across the center of a single contact pad from the previous experiment to a depth of approximately 150 nm using a focused ion beam. This created a recombination active region in the center of the active area. This area was then probed with a light beam induced current (LBIC) measurement using a 633 nm HeNe laser source in a Zeiss scanning confocal

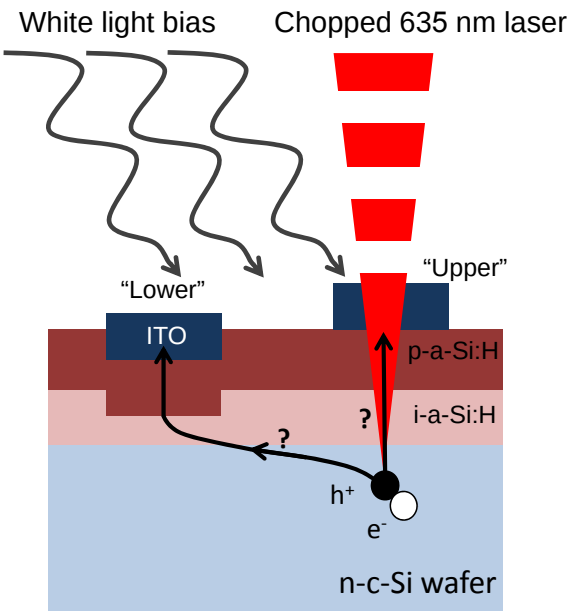


Figure 6.4: Schematic of the white light biased selected area illumination experiment with two contacts.

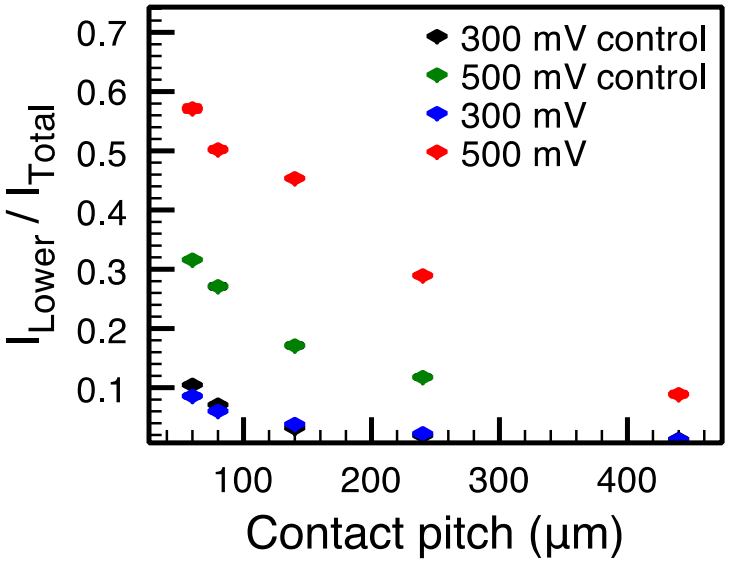


Figure 6.5: Results of white light biased, selected area illumination current splitting experiment with the upper contact illuminated. The y-axis represents the portion of the total current which traveled laterally to the lower contact. The control device had 10nm of i-a-Si:H everywhere.

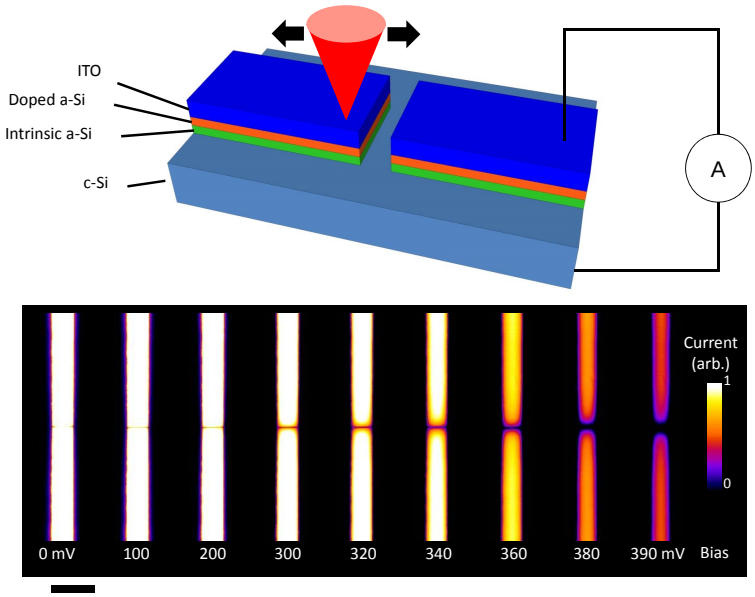


Figure 6.6: (top) Schematic of light beam induced current (LBIC) measurement around a FIB milled defect. (bottom) LBIC maps at various bias voltages. Scale bar is 50 microns.

microscope. Again, current was measured with a transimpedance amplifier and electrical bias was varied. The highest achievable bias voltage for which photocurrent was still observed was lower in this experiment, in which electrical bias was used, than in the previous because the local excitation must provide more current than the dark current from the whole cell in order to detect a signal. A schematic of this experiment and a resulting light beam induced current measurement are shown in figure 6.6.

Linescans were extracted from the LBIC maps, as in figure 6.7. The full width at half minimum was extracted from these linescans as a characteristic length, correlating with the exploration length. This varied from about 4 µm at short circuit to 31 µm at 390 mV of bias potential.

Additional measurements were performed on a sample containing whole area front contacts, rather than the isolated lines of ITO as discussed previously and shown in figure 6.6. Again, defects were induced with a focused ion beam, but this time care was taken to measure the dose of the beam. Additionally, measurements were taken with both 488 nm and 633 nm laser sources in order to vary the depth of the photogenerated carriers. A light beam induced current map and linescans extracted from these measurements are shown in figure 6.8. Here, the physical area of the defect is well known, and linescans begin at the edge of the defect and measure the decay of collected current into the non-defective area. Those decays were then fit to an exponential, corresponding to a characteristic

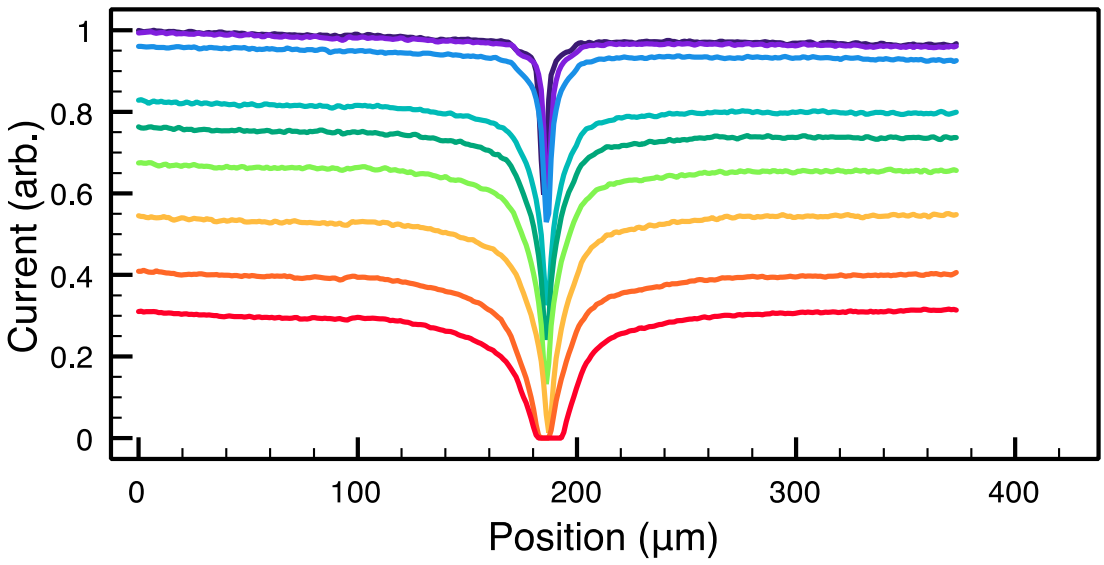


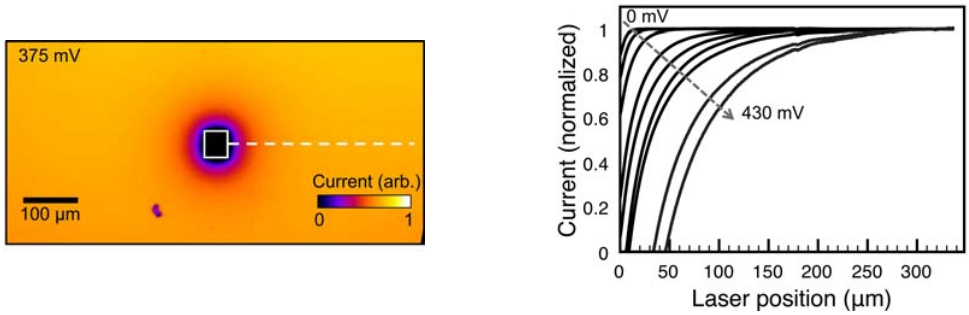
Figure 6.7: Linescans of defects showing effective cross section width

lateral transport length. Finally, the extracted lateral transport lengths were plotted as a function of bias voltage for each of the different conditions (laser wavelength and FIB dose); these results are shown in figure 6.9.

Again, lateral transport lengths were a strong function of bias voltage and approached 100 µm as the bias voltages approached operating voltages. Additionally, by varying the laser wavelength, we confirmed that the lateral transport length is independent of depth of generation, and provides additional evidence that the lateral transport is dominated by transport in the inversion layer just beneath the interface, rather than diffusion within the bulk. We expect additional bulk diffusion of approximately 2 µm to occur with the 633 nm light due to the deeper absorption in the crystalline silicon base by this same length. Aside from this slight increase in bulk diffusion, the lateral transport distance is the same, indicating that the dominant mechanism for lateral transport occurs only near the interface, regardless of where a carrier is generated.

6.4 Discussion

Both experiments provide evidence of lateral transport near the heterojunction and it is possible to describe the lateral transport with a characteristic lateral transport length. This is not a diffusion length, but instead depends on both drift and diffusion in the inversion layer. The large hole



(a) Light beam induced current map around a defect (b) Linescans extracted from the light beam inducted current measurements

Figure 6.8: Light beam induced current map of the area around a defect induced by a focused ion beam. The physical area of the defect is outlined in white, and the linescan is extracted along the dotted white line. Linescans extracted from these measurements can be fit to an exponential to measure the characteristic lateral transport length under different experimental conditions

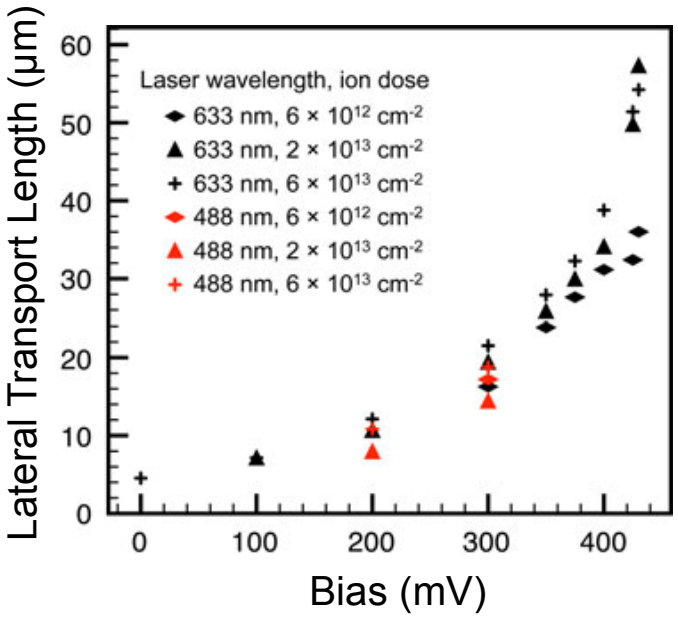


Figure 6.9: Characteristic lateral transport lengths extracted from light beam induced current linescans using different illumination wavelengths. Defects were induced by focused ion beam with the dose varied.

population at the interface is able to support high currents given a fairly small gradient in the quasi-Fermi level. The gradients in the quasi-Fermi level are provided by different sources in the two experiments and as a result, different magnitudes of lateral current are to be expected.

There are two likely explanations for the bias dependence observed in these experiments. At higher forward bias, the electric field across the intrinsic layer is reduced, which in turn reduces the driving force for transport across the intrinsic layer. It is likely that as a result of this, the dwell time in the inversion layer increases with forward bias. We saw in the first experiment that the sensitivity to intrinsic layer thickness increased in forward bias as well, as evidenced by the difference in current splitting ratios between the experimental and control samples. This supports the concept that the driving force for transport across the intrinsic layer is reduced at forward bias and the thicker intrinsic layer presents an increasingly difficult barrier to pass, resulting in a high current splitting ratio and long lateral transport lengths.

The second possible mechanism is a change in inversion layer mobility with bias. At positive forward bias it is likely that the occupation of band tail states changes, which may in turn change the hole mobility in the inversion layer. It is impossible to decouple the influences of the dwell time and mobility variation without a more complete model of transport or further experimentation.

6.5 Conclusions and Outlook

Amorphous silicon/crystalline silicon heterojuction solar cells are capable of reaching extremely high open circuit voltages, but their full potential is difficult to attain due to sensitivity to defects at the interface. In order to fully understand this sensitivity, it is necessary to gain a better understanding of carrier dynamics in the inversion layer near the heterointerface. Two experiments were performed in order to directly probe the lateral movement of charge carriers. We found that characteristic lateral transport lengths are a strong function of device bias, and are on the order of tens to hundreds of microns near practical operating voltages. The lateral transport we observe is an important mechanism in SHJ device operation and elucidates the physics underlying the sensitivity these devices show to interface quality. Continued improvements in the understanding of the physics governing interfacial transport and charge collection at the a-Si:H/c-Si interface will benefit SHJ design and optimization.

Chapter 7

Future Directions

7.1 Materials for Photovoltaics

Throughout this thesis, I have described some of the enormous changes the photovoltaics industry has witnessed over the past six years, including, most notably, the rapid fall in the costs of high quality silicon material, modules, and installed systems. The effects of the drop in cost of silicon and silicon-based devices have been widespread. There has been a massive shakeout in the industry, with more than 50 device manufacturers, large and small, declaring bankruptcy or closing between 2009 and 2014 [122].

Many of the recently failed companies were originally founded on the premise of providing a lower cost alternative to silicon wafer-based devices. Technologies included alternative materials, such as amorphous silicon and CIGS, or alternative ways to grow silicon, such as Evergreen Solar's string ribbon silicon. The common problem with most of these technologies was that alongside lower cost came lower efficiency. Amorphous silicon devices (note, this refers to devices in which the active layer is amorphous silicon, not the successful amorphous silicon-crystalline silicon heterojunction device) have record efficiencies of around 10%, with production module efficiencies significantly lower. For example, Uni-Solar, the second largest thin film device manufacturer in 2007 and bankrupt by 2012, had standard single junction device efficiencies of around 6%. While CIGS has demonstrated significantly higher efficiencies in laboratory scale, it has been difficult to scale up. For example, Honda Soltec, closed in 2013, produced CIGS modules with efficiencies of just 11.6%. Finally, alternative wafering and device maker Evergreen Solar, bankrupt in 2011, produced modules with an efficiency of around 13%.

Contrasting this list of failed companies that promised to deliver low cost devices at low efficiencies is a list of still profitable companies that entered the market with a different goal: offering high efficiency devices. Due to the decreasing cost of silicon, these companies can offer high efficiency modules — most are above 15% — at a low cost.

Silicon appears to be positioned to continue to drive the industry towards higher efficiency and

lower cost in the future. While there is no fundamental reason that another high quality material, such as GaAs, won't reach higher efficiency and lower cost, the amount of investment in silicon gives it a distinct advantage to continue developing at a rapid pace.

7.2 Device Design

The trend in device designs in the last few years has been towards devices which provide improved efficiencies, such as devices that include all back contact, locally diffused back surface fields, n-type wafers, and amorphous silicon heterojunctions. Cost is currently both the primary barrier and driving force for these additions. Currently, some of these high efficiency devices are technically difficult, but nothing fundamental stands in the way of developing low cost processes. Once low cost, high efficiency processes are developed, the overall module cost will fall compared to a lower efficiency technology. Examples of recent adoption of high efficiency device designs are widespread. The new Silevo plant in Buffalo, NY, is proposed to be one of the largest in the world, and based on high efficiency, heterojunction technology. The Chinese company Yingli Solar, previously known for its extremely inexpensive, multicrystalline silicon based modules using simple processing techniques, has recently released a high efficiency device based on n-type wafers, with ion-implanted emitters.

The current trends are likely to continue in the future. Inexpensive methods for patterning selective emitters, locally diffused back surface fields, and interdigitated back contacts will very quickly make these technologies cost-competitive. Additionally, as material quality improves and diffusion lengths increase, the size scales required for this patterning get larger, and the task easier. More generally, there is a lot of opportunity for relatively minor technological developments to have a high impact by enabling the use of higher efficiency device designs.

While the signs pointing toward higher efficiency device designs thriving are strong, the adoption of ultra-thin wafers is somewhat less certain. The fire sale of Twin Creeks, which developed a tool for creating 20 µm thick silicon wafers without saw blade kerf loss, was relatively high profile. However, there are still several companies that plan to grow ultrathin wafers directly, such as Crystal Solar and Solexel. Both have achieved high efficiency and promise low costs. Another likely path towards thinner devices is the simple evolutionary approach, my migrating to thinner wafers. This seems likely to occur, as Panasonic has already proven that higher efficiencies can be achieved using this approach. The main difficulty is that the mechanical strength of a wafer suffers, and new tools will need to focus more attention on being able to handle thinner wafers without causing breakage. Still this seems like a relatively minor hurdle that will likely be overcome.

7.3 Solar Grid Integration

A less predictable, but equally interesting, aspect of solar adoption is the question of how solar power will be integrated into the current electric grid. Will it be given special treatment because it does not emit CO_2 or other pollutants during operation, or punished because of its low capacity factor and unreliability? This is a question that will be answered by policy, rather than technology, and will likely have a different answer in different areas.

The obvious challenge in relying on solar energy is that it only produces power while the sun shines, but we want to use power regardless of the suns presence. This intermittency presents additional challenges when considering the profitability of other generating assets. For example, a natural gas fired plant in a region without significant solar energy might operate at an average of 90% of its maximum capacity; if it must shutdown during sunlight hours due to photovoltaic generation, the average output may reduce to 75% of its rated value. This increases the capital cost per unit energy output, and therefore, the total cost of electricity generated by this plant.

The question of storage is often raised when discussing adoption of solar energy, as it presents an opportunity to avoid the previously described problem associated with solar's low capacity factor. However, the viability in the near future is uncertain, as the technology and markets for storage solutions are changing at a similar pace to those of photovoltaics. While many predict that the combination of solar and a storage solution will remain too expensive for use in base load applications for a long time, very few people predicted the rapid fall in photovoltaic costs to the current level perhaps the energy storage market will witness a similar, unpredicted price plunge. Regardless of whether storage solutions will be viable in the coming years, there is still significant room to integrate additional solar generating capacity in our current grid without adversely affecting the reliability of our existing generation and transmission system. Research, and real world testbeds such as the German power grid, estimate that solar can reach approximately 8% of the total generation grid before the aforementioned problems begin to have serious consequences [123].

7.4 Conclusion

We have witnessed fantastic changes in the technology, and therefore markets, for raw silicon material and photovoltaic modules in the last several years. While the broader market for photovoltaics still faces a lot of uncertainty, with both technological and policy-based challenges relating to solar's intermittency, trends within the photovoltaic market seem clearer: the rapid drop in the cost of high quality silicon material strengthens silicon's position as a leader in photovoltaic materials. Silicon device efficiencies will continue to rise in the coming years, with many promising paths forward, including the use of heterojunctions and thinner devices.

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[122] E. Wesoff, "Rest in peace: The fallen solar companies of 2014," *Greentech Media*, 2014.

[123] N. Stodola and V. Modi, "Penetration of solar power without storage," *Energy Policy*, vol. 37, no. 11, pp. 4730 – 4736, 2009.

Appendix A

PECVD Deposition and Characterization

A.1 n^+ doped amorphous silicon in PL4

A cylinder for depositing heavily doped n-type amorphous silicon was installed and plumbed into PL4 and PL6, containing 500 ppm phosphine premixed into 5% silane diluted in helium. Helium was chosen as the diluting gas, rather than argon as used in previous premixed silane bottles, to minimize surface sputtering damage. Deposition parameters for doped a-Si were: 500 mTorr pressure, 50 sccm of SiH_4 mix gas flow and 25 sccm of H_2, and 1 W of power. Amorphous silicon films were deposited on glass through a thin stainless steel shadow mask containing square and cloverleaf patterns (shown in figure A.1 A) in order to perform electrical measurements. Indium tin oxide (ITO) contacts were then sputtered on the corners through a different shadow mask to form ohmic contact to the a-Si, followed by copper to allow wires to be soldered to the contacts. Magnet wire was then soldered to the contacts using standard lead-tin solder, and van der Pauw 4-point conductivity measurements were performed at low temperatures in a Hall measurement system. An image of a sample is shown in figure A.1 B, and results are shown in figure A.2. The conductivity and activation energy measured compare well to data in the literature [74].

A rapid method for performing thickness measurements with contact profilometry was developed. Stylus contact profilometry has many advantages — measurements are easy and fast to perform, accurate, and independent of composition and other properties of the film. However, sharp step edges are necessary to perform accurate measurements. As evident in the sample shown in figure A.1, the edge formed on the outside of the sample or near a shadow mask is particularly sharp. Furthermore, in order to prevent contamination of the chamber, we avoided using tape or some other masking technique during deposition. A simple method to form a sharp edge on a-Si samples is to place a drop of potassium hydroxide (KOH; $20\%_{w/w}$ was used) on the surface. Surface tension will hold the KOH in a droplet. Completeness can be judged by eye and the KOH washed away

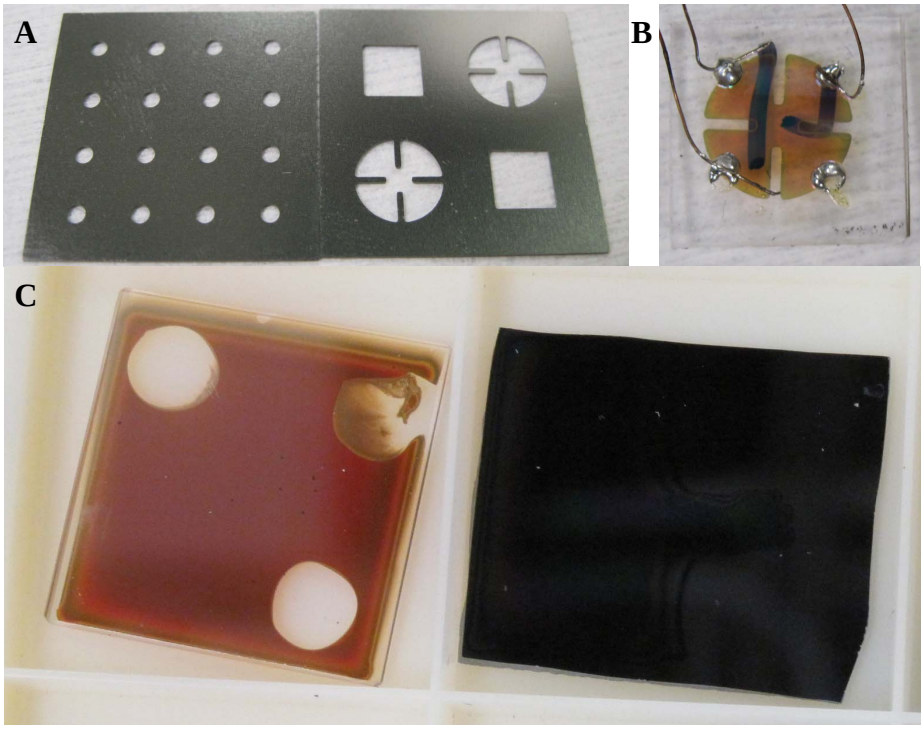

Figure A.1: A: Shadow masks for Hall effect and conductivity sample (left) and contact (right) deposition. Contact hole seperation is 0.2 inches, matching the probe spacing in the Hall effect measurement system. B: Sample prepared for low temperature Hall/conductivity measurements using the shadow masks in (A). C: Amorphous silicon (left) and silicon oxide (right) samples prepared for contact profilometry thickness measurements. Glass slide is a 0.875 inch square.

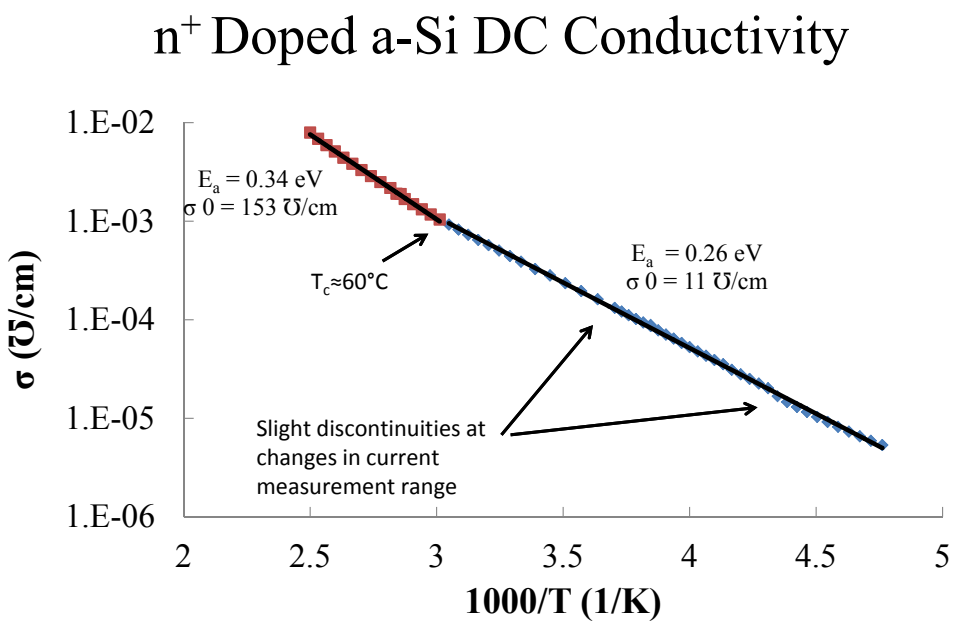

Figure A.2: DC conductivity of n^+ doped amorphous silicon

when complete. The etch rate of glass in KOH is significantly lower than silicon, so over-etching will not significantly affect the measurement. This method was attempted to measure SiO_x thickness on Si using hydrofluoric acid, but the surface was too hydrophilic; the acid did not stay in a drop. A step edge could be created by masking the etch with photoresist, but this method is generally unnecessary, as ellipsometric measurements of SiO_x on silicon were fast and accurate.

The first steps towards making a HIT-type silicon heterojunction device were performed with the heavily doped source. Simple heterojunctions on a p-type with aluminum back surface field exhibited open circuit voltages >560 mV. Indium-tin oxide was used as a front contact, which also acted as an anti-reflective coating. A champion device efficiency of 11% was achieved on a polished silicon wafer with V_{OC} = 540 mV, J_{SC} =31.7 mA cm^{-2} and FF = 64.7%. Current-voltage characteristics and spectral response are shown in figure A.3. Further optimization will be required to realize gains by adding an intrinsic interlayer and heterojunction back surface field, as in the HIT device.

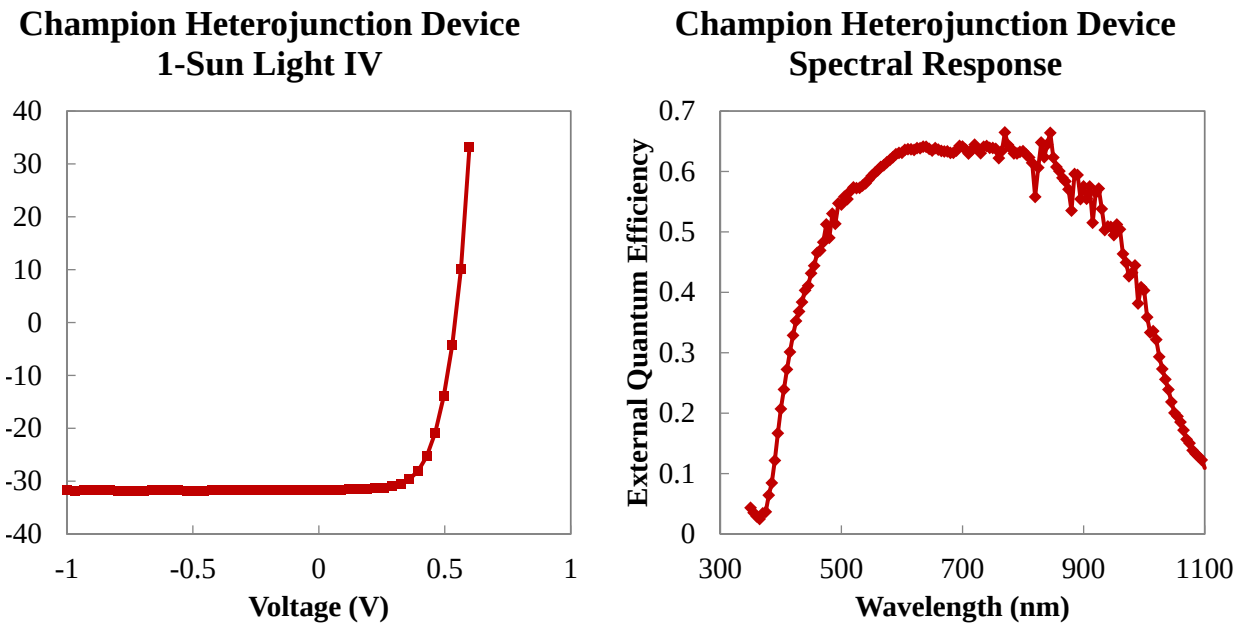

Figure A.3: Current-voltage and spectral response of simple heterojunction device. The champion device efficiency of 11% was achieved on a polished silicon wafer with V_{OC} = 540 mV, J_{SC} =31.7 mA cm^{-2} and FF = 64.7%.

A.2 Oxide in PL5

The capability to deposit SiO_x using NO_2 and 5 % SiH_4 in Ar was added not long before my arrival to the group, and very little process development had been done. Here you will find some working recipes, approaching the silicon rich suboxide regime. Recipes and growth rates are shown in table A.1 and optical data in figure A.4. Note that a heater temperature of 500 °C corresponds to a substrate temperature of approximately 350 °C.

Table A.1: Oxide/Suboxide Depositions from PL5

Growth Number	Pressure (mTorr)	Heater Temperature (°C)	RF Power (Watts)	SiH_4 Flow Rate (sccm)	N_2O Flow (sccm)	Growth Rate (nm/min)
143	750	500	3	50	50	28
145	750	500	3	50	25	26.8
146	750	500	3	50	10	19.3

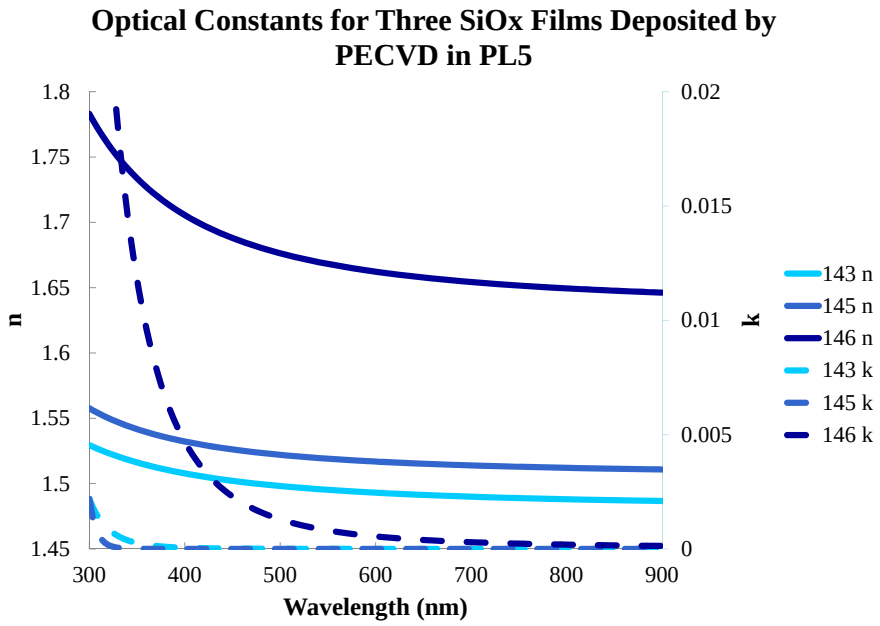

Figure A.4: Optical Constants of Oxides Deposited in PL5

Appendix B

Transient Simulations using Sentaurus TCAD

Synopsys Sentaurus TCAD was used to interpret the results of photoconductivity decay experiments. While relatively simple analytical solutions relating the effective lifetime to the surface recombination velocity, bulk lifetime, and thickness exist for wafer geometries, these same expressions only exist for certain limited conditions in cylindrical geometries, and are not solved for tapered structures. Therefore, we turn to simulations to fit likely material parameters given an effective lifetime for these geometries.

The following code was built off, and borrowed sections from the wire simulations developed by Michael Kelzenberg and adaptions made by Michael Deceglie. The general workflow follows the typical method of device simuation: first, the structure is defined and meshed in the structure editor. Next, Sentaurus Device is run once to calculate the illumination, and the illumination information is imported into the next Device simulation which calculates the carrier density. Finally Matlab is used to fit either a single or double exponential to the extracted data. An example of the output data and fit are shown in figure B.1

Listing B.1: Sentaurus Device Editor Code

```
##########################################################################################################
# Radial p-n junction solar cell structure for core depletion studies
# Sentaurus Structure Editor command file (abridged for inclusion in PhD thesis)
#
# Michael Kelzenberg, California Institute of Technology, 2010
# Modified for photoconductivity decay simulations by Hal Emmer, 2015
##########################################################################################################
#
#Global settings (project variables):
# @R@ wire radius, microns
# @L@ length of ''above substrate'' wire (note that the actual structure is 1 um longer)
# @subsdoping@ doping of the substrate, controls lifetime on the bottom surface
#
#Local settings:
#
#define BaseDoping 1E+16
# [cm-3]
#define tnitride 0.15
```

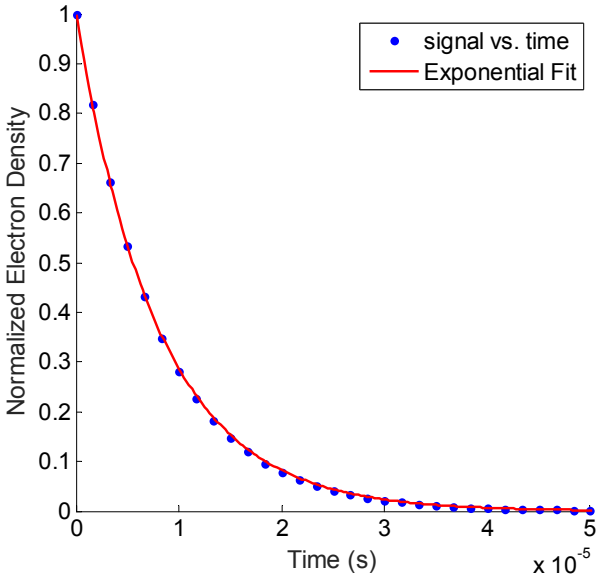

Figure B.1: Example output of a transient simulation, and exponential fit generated by Matlab.

```
# [microns] (oxide shell used to set sidewall SRV value)
#define EMinGrid 0.01
# [um] min. refinement mesh size in emitter region
#define EMaxGrid 0.2
# [um] max. refinement mesh size in emitter region
#define ERatio 1.5
# grid relaxation ratio for emitter region
#define BMinGrid 0.01
# [um] min. refinement mesh size in base region
#define BMaxGrid 0.2
# [um] max. refinement mesh size in base region
#define BRatio 1.2
# grid relaxation ratio for base region
#
##########################################################################################################
#
# Cross section of wire material for cylindrical photoconductivity decay simulations
#
##########################################################################################################
#MATERIAL
(sdegeo:create-rectangle (position 0 -tnitride 0)
        (position (+ @R@ tnitride) @L@ 0) "Nitride" "Nitride_region")
(sdegeo:create-rectangle (position 0 0 0) (position @R@ @L@ 0) "Silicon" "Base_region")
(sdegeo:create-rectangle (position 0 @L@ 0) (position @R@ (+ @L@ 1.0) 0) "Silicon" "Subs_region")

#PROFILES
(sdedr:define-constant-profile "ConstantProfileDefinition_forBase" "BoronActiveConcentration" BaseDoping)
(sdedr:define-constant-profile-region "ConstantProfilePlacement_forBase"
        "ConstantProfileDefinition_forBase" "Base_region")
(sdedr:define-constant-profile "ConstantProfileDefinition_forSubs" "BoronActiveConcentration" @subsdoping@)
(sdedr:define-constant-profile-region "ConstantProfilePlacement_forSubs"
        "ConstantProfileDefinition_forSubs" "Subs_region")



#REFINEMENTS FOR MATERIAL
(sdedr:define-refinement-size "RefinementDefinition_forSilicon" BMaxGrid BMaxGrid EMinGrid EMinGrid )
```

```
(sdedr:define-refinement-material "RefinementPlacement_forSilicon"
        "RefinementDefinition_forSilicon" "Silicon" )

#REMAINING REFINEMENTS
#POSITION
(sdedr:define-refeval-window "RefEvalWin_B_Upper" "Rectangle"
(position 0 0 0) (position @R@ (* @L@ 0.5) 0) )
(sdedr:define-refeval-window "RefEvalWin_B_Lower" "Rectangle"
(position 0 @L@ 0) (position @R@  (* @L@ 0.5) 0) )

#REFINEMENT PITCH
(sdedr:define-multibox-size "MultiboxDefinition_B_Upper"
        BMaxGrid BMaxGrid BMinGrid BMinGrid -BRatio BRatio )
(sdedr:define-multibox-size "MultiboxDefinition_B_Lower"
        BMaxGrid BMaxGrid BMinGrid BMinGrid -BRatio -BRatio )
#PLACEMENTS
(sdedr:define-multibox-placement "MultiboxPlacement_B_Upper"
        "MultiboxDefinition_B_Upper" "RefEvalWin_B_Upper" )
(sdedr:define-multibox-placement "MultiboxPlacement_B_Lower"
        "MultiboxDefinition_B_Lower" "RefEvalWin_B_Lower" )
# NITRIDE SIDEWALL
(sdedr:define-refeval-window "RefEvalWin_Nitride"
        "Rectangle" (position 0 0 0) (position (+ @R@ tnitride) @L@ 0) )
(sdedr:define-multibox-size "MultiboxDefinition_forNitride"
        BMaxGrid BMaxGrid EMinGrid EMinGrid ERatio -ERatio )
(sdedr:define-multibox-placement "MultiboxPlacement_forNitride"
        "MultiboxDefinition_forNitride" "RefEvalWin_Nitride" )
# NITRIDE TOP
(sdedr:define-refeval-window "RefEvalWin_TopNitride"
        "Rectangle" (position 0 0 0) (position (+ @R@ tnitride) -tnitride 0) )
(sdedr:define-multibox-size "MultiboxDefinition_forTopNitride"
        BMaxGrid BMaxGrid EMinGrid EMinGrid ERatio -ERatio )
(sdedr:define-multibox-placement "MultiboxPlacement_forTopNitride"
        "MultiboxDefinition_forTopNitride" "RefEvalWin_TopNitride")
# DONE. GENERATE MESH.
(sde:save-model "n@node@")
(sde:build-mesh "snmesh" "-y 1e5 --numThreads 8" "n@node@" )
```

Listing B.2: Sentaurus Device illumination code for uniform monochromatic illumination

```
# Optical Generation with Transfer Matrix Method

#setdep @node|-1:all@


#set taup 1
#set S0 1
# Required to read the parameter file. These will be modified in the device simulation
*****************************************************************************************************
* FILE
*****************************************************************************************************
File
{
        Grid                    = "n@node|-1@_msh.tdr"
        Parameters              = "@parameter@"
        plot                    = "@tdrdat@"
        current                 = "@plot@"
           OpticalGenerationOutput = "optgen_des_R@R@_L@L@_I@Power@.tdr"
}

*****************************************************************************************************
* ELECTRODES
*****************************************************************************************************


*****************************************************************************************************
* PLOT
*****************************************************************************************************
Plot {
  eCurrent/Vector hCurrent/Vector current/vector
```

```
  SpaceCharge eDensity hDensity
  Potential ElectricField
  SRH Auger TotalRecombination SurfaceRecombination
  ConductionBand ValenceBand DopingConcentration
  eQuasiFermi hQuasiFermi
  EffectiveIntrinsicDensity IntrinsicDensity
  OpticalGeneration RayTraceIntensity * RayTrees
}

*****************************************************************************************************
* PHYSICS
*****************************************************************************************************
Physics {
    Optics(
        ComplexRefractiveIndex ( WavelengthDep(real imag) )
        OpticalGeneration (
            ComputeFromMonochromaticSource
        ) * end OpticalGeneration
        Excitation (
            Window ("L1")(
             Origin = (0, 0)
             Line( Dx = @<2*@R@>@)
         )*End Window
        Wavelength = 1.064 * um, Nd:YAG laser output
        Intensity =  @Power@  * W/cm^2
        Theta = 0.       * degrees
        Phi = 30.        * degrees
        )*End Excitation

        OpticalSolver (
            TMM (
                LayerStackExtraction (
                    WindowName = "L1"
                ) * end LayerStack
            ) * end TMM
        ) * end Optical Solver
    ) *end Optics
} * end physics

*****************************************************************************************************
* MATH
*****************************************************************************************************
Math{
   Extrapolate
   Derivatives
   AvalDerivatives
   RelErrControl
   Digits=18
   RhsMin=1E-15
   ExtendedPrecision
   Iterations=300
   Notdamped=300
   ExitOnFailure
   StackSize=20000000
   Cylindrical (0.0)

}

*****************************************************************************************************
* SOLVE
*****************************************************************************************************
Solve
{
 Optics
}
```

Listing B.3: Sentaurus Device code for transient photoconductivity decay

```
#setdep @node|-1:all@
```

```
# set Nto @<@Nt@/100>@

*****************************************************************************************************
* FILE
*****************************************************************************************************
File
{
        Grid                    = "n@node|-2@_msh.tdr"
        Parameters              = "@parameter@"
        plot                    = "@tdrdat@"
        current                 = "@plot@"
        OpticalGenerationInput = "optgen_des_R@R@_L@L@_I@Power@.tdr"
}

*****************************************************************************************************
* ELECTRODES
*****************************************************************************************************
*
* No electrodes are used in the contactless photoconductivity experiment
*
*****************************************************************************************************
* PLOT
*****************************************************************************************************
Plot
{
        eCurrent/Vector hCurrent/Vector current/vector
        ElectricField/Vector eDriftVelocity/Vector hDriftVelocity/Vector
        SpaceCharge eDensity hDensity
        Potential ConductionBandEnergy ValenceBandEnergy
        SRH Auger TotalRecombination SurfaceRecombination/RegionInterface
        eGapStatesRecombination hGapStatesRecombination
        DopingConcentration OpticalGeneration
        CurrentPotential * BeamGeneration OptBeam
        NonLocal hBarrierTunneling eBarrierTunneling
}

CurrentPlot {
        SurfaceRecombination(Integrate(RegionInterface="Base_region/Nitride_region"))
        OpticalGeneration((0 , @<@L@ * @samplespot@>@)),
        eDensity(Average(Region="Base_region"))          #plot the average electron density in the base
#       eDensity((0 , @<@L@ * @samplespot@>@))          #or plot it at a specific point
}

*****************************************************************************************************
* PHYSICS
*****************************************************************************************************
Physics
{
  EffectiveIntrinsicDensity(NoBandGapNarrowing)
  Fermi
  Area=@<1e8/(2*@R@)>@
  Optics(
     OpticalGeneration(
        ReadFromFile(Scaling = 0)
        TimeDependence (
                WaveTime= (0e-4 @tlightoff@)
                WaveTsigma= 1e-6
                Scaling= 1.0     * Transient Scaling
        ) *end TimeDependence
     )
   )
}

Physics (Material="Silicon") {
   Recombination(
        SRH Auger
        Band2Band(
                Model=Schenk
        )
```

```
    )*end Recombination
    Mobility(DopingDep)
}


Physics (RegionInterface="Base_region/Nitride_region"){
     Recombination (SurfaceSRH)                    #use a surface recombination velocity defined in the
}                                                  #parameter file to be taken from the workbench




*****************************************************************************************************
* MATH
*****************************************************************************************************
Math{
    Method = ParDiSo
    Transient = Be
    Number_of_Threads = maximum
    Extrapolate
    Derivatives
    AvalDerivatives
    RelErrControl
    Digits=6
    RhsMin=1E-15
    ExtendedPrecision
    Iterations=300
    Notdamped=300
    ExitOnFailure
    StackSize=4000000
    Cylindrical (0.0)

    CurrentPlot(IntegrationUnit= cm)

}

*****************************************************************************************************
* SOLVE
*****************************************************************************************************
Solve
{

     *--First solve the dark, V=0 case (short cicuit condition)
     Coupled  { poisson }
     Coupled  { poisson electron }
     Coupled  { poisson electron hole }

     Plot( FilePrefix = "n@node@_dark_" )

     NewCurrentPrefix="light_"

     Quasistationary( InitialStep=0.1 MinStep=0.001 MaxStep=0.5
     Goal{ ModelParameter = "Optics/OpticalGeneration/ReadFromFile/Scaling" Value = 1 } )
         { Coupled  { poisson electron hole } }


     Plot( FilePrefix = "n@node@_light_" )

     NewCurrentPrefix= "Switch_"

##- from 0 to T1
         Transient (
         Initialtime= 0 Finaltime= 5e-4
                 Initialstep= 1e-7 Increment= 1.5 Decrement= 4
                 Minstep= 1e-11 Maxstep= 1e-4
         ){ Coupled{ Poisson Electron Hole }
                 CurrentPlot( Time= (                          #generate more data around the decay
                         Range= (0.0e-4 2.0e-4) intervals= 20;
                         Range= (2.0e-4 2.5e-4) intervals= 20;
                         Range= (2.5e-4 3.0e-4) intervals= 30;
                         Range= (3.0e-4 3.5e-4) intervals= 25;
```

```
                        Range= (3.5e-4 4.0e-4) intervals= 20;
                        Range= (4.0e-4 5.0e-4) intervals= 15))
        }
}
```

Listing B.4: Matlab code for fitting transient photoconductivity simulations

```
#setdep @node|-1:all@

%% Initialize variables.

starttime = @tlightoff@;

filename = './Switch_n@node|-1@_des.plt'
startRow = 11;

%% Read columns of data as strings:
% For more information, see the TEXTSCAN documentation.
formatSpec = '%26s%23s%23s%23s%s%[^\n\r]';

%% Open the text file.
fileID = fopen(filename,'r');

%% Read columns of data according to format string.
% This call is based on the structure of the file used to generate this
% code. If an error occurs for a different file, try regenerating the code
% from the Import Tool.
textscan(fileID, '%[^\n\r]', startRow-1, 'ReturnOnError', false);
dataArray = textscan(fileID, formatSpec, 'Delimiter', '', 'WhiteSpace', '', 'ReturnOnError', false);

%% Close the text file.
fclose(fileID);

%% Convert the contents of columns containing numeric strings to numbers.
% Replace non-numeric strings with NaN.
raw = repmat({''},length(dataArray{1}),length(dataArray)-1);
for col=1:length(dataArray)-1
    raw(1:length(dataArray{col}),col) = dataArray{col};
end
numericData = NaN(size(dataArray{1},1),size(dataArray,2));

for col=[1,2,3,4,5]
    % Converts strings in the input cell array to numbers. Replaced non-numeric
    % strings with NaN.
    rawData = dataArray{col};
    for row=1:size(rawData, 1);
        % Create a regular expression to detect and remove non-numeric prefixes and
        % suffixes.
        regexstr = '(?<prefix>.*?)(?<numbers>([-]*(\d+[\,]*)+[\.]{0,1}\d*[eEdD]{0,1}[-+]*\d*[i]{0,1})|([-]
------------------*(\d+[\,]*)*[\.]{1,1}\d+[eEdD]{0,1}[-+]*\d*[i]{0,1}))(?<suffix>.*)';
        try
            result = regexp(rawData{row}, regexstr, 'names');
            numbers = result.numbers;

            % Detected commas in non-thousand locations.
            invalidThousandsSeparator = false;
            if any(numbers==',');
                thousandsRegExp = '^\d+?(\,\d{3})*\.{0,1}\d*$';
                if isempty(regexp(thousandsRegExp, ',', 'once'));
                    numbers = NaN;
                    invalidThousandsSeparator = true;
                end
            end
            % Convert numeric strings to numbers.
            if ~invalidThousandsSeparator;
                numbers = textscan(strrep(numbers, ',', ''), '%f');
                numericData(row, col) = numbers{1};
                raw{row, col} = numbers{1};
            end
```

```
        catch me
        end
    end
end


%% Replace non-numeric cells with NaN
R = cellfun(@(x) ~isnumeric(x) && ~islogical(x),raw); % Find non-numeric cells
raw(R) = {NaN}; % Replace non-numeric cells

%% Allocate imported array to column variable names
Time = cell2mat(raw(:, 1));
VarName2 = cell2mat(raw(:, 2));
VarName3 = cell2mat(raw(:, 3));
VarName4 = cell2mat(raw(:, 4));
Signal = cell2mat(raw(:, 5));


for col=1:length(Time)-1

    if Time(col) >= starttime
        startindex = col;
        break;
    end
end


%% Allocate imported array to column variable names

Time = Time - starttime;
Signal = Signal / max(Signal);

%% Fit: 'Double Exponential'.
[xData, yData] = prepareCurveData( Time(startindex:end), Signal(startindex:end));

% Set up fittype and options.
ftdouble = fittype( 'exp2' );
opts2 = fitoptions( ftdouble );
opts2.Display = 'Off';
opts2.Lower = [-Inf -Inf -Inf -Inf];
opts2.Upper = [Inf Inf Inf Inf];

% Set up fittype and options.
ftsingle = fittype( 'exp1' );
opts1 = fitoptions( 'Method', 'NonlinearLeastSquares' );
opts1.Display = 'Off';

[fitresult1, gof1] = fit( xData, yData, ftsingle, opts1 );
fitresult1
gof1

% Fit model to data.
[fitresult2, gof2] = fit( xData, yData, ftdouble, opts2 );
fitresult2
gof2

if (gof1.rsquare < .9) %if we didn't get a good fit, try removing all the zeroes

        for col=1:length(yData)-1

            if yData(col) <= .0001
                startindex = col;
                break;
            end
        end

        xData = xData(1:startindex);
        yData = yData(1:startindex);

        opts1 = fitoptions( ftsingle );
        opts1.Display = 'Off';
```

```
        [fitresult1, gof1] = fit( xData, yData, ftsingle, opts1);
        fitresult1
        gof1

end

if (gof1.rsquare < .9)  %if the single exponential fit is good, output that.
    fprintf('\nDOE: R2 %.3f \nDOE: tau1 %.2f us \nDOE: tau2 %.2f us \nDOE: a %.2f \nDOE: b %.2f\n',
        gof2.rsquare, -1/fitresult2.b * 10^6, -1/fitresult2.d * 10^6, fitresult2.a, fitresult2.c);
else                            %Otherwise, output the double exponential fit
    fprintf('\nDOE: R2 %.3f \nDOE: tau1 %.2f us \nDOE: tau2 %.2f us \nDOE: a %.2f \nDOE: b %.2f\n',
        gof1.rsquare, -1/fitresult1.b * 10^6, 0, fitresult1.a, 27);
end

% Plot fit with data.
figure( 'Name', 'untitled fit 1' );
h = plot( fitresult1, xData, yData );
legend( h, 'signal vs. time', 'untitled fit 1', 'Location', 'NorthEast' );
% Label axes
xlabel( 'time' );
ylabel( 'signal' );
grid on
```

Appendix C

Excel VBA Code for Limiting Efficiency Calculations

Listing C.1: Excel VBA Solver Code

```
Dim count
Dim minerror
Dim minerrorrow
Dim startcount
Dim step

Sheet6.Activate

minerror = 5
startcount = 3
For count = startcount To startcount + 5          'generate initial seed guesses over 5 orders of magnitude
    Sheet6.Range("E" & count).Value = 0.0000001 * 10 ^ (count - startcount)
    If Sheet6.Range("N" & count).Value < minerror Then   'keep track of the closest solution
        minerror = Sheet6.Range("N" & count).Value
        minerrorrow = count
    End If
Next count


step = 10
Do While (minerror > 0.001)                       'keep generating new guesses until error < 0.001

    startcount = count
    For count = startcount To startcount + 20
        Sheet6.Range("E" & count).Value = Sheet6.Range("E" & minerrorrow).Value *
                10 ^ ((count - startcount - 10) / step)
        If Sheet6.Range("N" & count).Value < minerror Then       'keep track of the closest solution
            minerror = Sheet6.Range("N" & count).Value
            minerrorrow = count
        End If
    Next count
step = step * 10
Loop

'copy solutions to the right cells
Sheet6.Range("C22").Value = Sheet6.Range("E" & minerrorrow)
Sheet6.Range("C23").Value = Sheet6.Range("F" & minerrorrow)
Sheet6.Range("E1:N1").Value = Sheet6.Range("E" & minerrorrow & ":N" & minerrorrow).Value
Sheet6.Range("B29").Value = Sheet6.Range("C24").Value / 1000

'if wanted, solve for lifetime and voltage at max power point.
'This slows down the calculations fairly significantly, though.
'SolverOk SetCell:="$C$29", MaxMinVal:=3, ValueOf:=0,
         'ByChange:="$B$29", Engine:=1, EngineDesc:="GRG Nonlinear"
```

```
'SolverSolve True
'ActiveSheet.Range("E" & count + 1).Value = minerrorrow
'ActiveSheet.Range("E" & count + 1).NumberFormat = "General"
```

Listing C.2: VBA Code to Generate Sweeps

```
Sub Sweep()
'Sweeps thickness, and refines the calculation around the maximum efficiency thickness

Dim thickness
Dim maxefficiency

maxefficiency = 0
thickness = 1.5
Index = 3
Do While (thickness < 1000)
    Sheet1.Range("B" & Index).Value = thickness
    Sheet6.Range("C10").Value = Sheet1.Range("B" & Index).Value
    Module1.Solver

    Sheet1.Range("C" & Index).Value = Sheet6.Range("C27").Value 'efficiency
    If Sheet1.Range("C" & Index).Value > maxefficiency Then
        maxefficiency = Sheet1.Range("C" & Index).Value
        maxefficiencycell = Index
        maxefficiencythickness = thickness
    End If
    Sheet1.Range("D" & Index).Value = Sheet6.Range("C24").Value 'voc
    Sheet1.Range("E" & Index).Value = Sheet6.Range("C17").Value 'Current
    Sheet1.Range("F" & Index).Value = Sheet6.Range("C22").Value 'Effective Lifetme
    Sheet1.Range("G" & Index).Value = Sheet6.Range("C23").Value 'Carrier Concentration
    Sheet1.Range("H" & Index).Value = Sheet6.Range("B29").Value 'Voltage at MPP
    Sheet1.Range("I" & Index).Value = Sheet6.Range("B30").Value 'Carrier Concentration at MPP
    thickness = Round(thickness * 1.1, 1)
    Index = Index + 1
Loop

For thickness = Round(maxefficiencythickness, 0) - 10 To Round(maxefficiencythickness, 0) + 10
    Sheet1.Range("B" & Index).Value = thickness
    Sheet6.Range("C10").Value = Sheet1.Range("B" & Index).Value
    Module1.Solver

    Sheet1.Range("C" & Index).Value = Sheet6.Range("C27").Value 'efficiency
    If Sheet1.Range("C" & Index).Value > maxefficiency Then
        maxefficiency = Sheet1.Range("C" & Index).Value
        maxefficiencycell = Index
        maxefficiencythickness = thickness
    End If
    Sheet1.Range("D" & Index).Value = Sheet6.Range("C24").Value 'voc
    Sheet1.Range("E" & Index).Value = Sheet6.Range("C17").Value 'Current
    Sheet1.Range("F" & Index).Value = Sheet6.Range("C22").Value 'Effective Lifetme
    Sheet1.Range("G" & Index).Value = Sheet6.Range("C23").Value 'Carrier Concentration
    Sheet1.Range("H" & Index).Value = Sheet6.Range("B29").Value 'Voltage at MPP
    Sheet1.Range("I" & Index).Value = Sheet6.Range("B30").Value 'Carrier Concentration at MPP

    Index = Index + 1
Next thickness


Sheet1.Range("B1").Value = maxefficiencythickness
Sheet1.Range("C1").Value = maxefficiency
Sheet1.Activate


End Sub


Sub SweepSRV()

Dim SRV
```

```
SRV = 1.5
Index = 3
Do While (SRV < 100)
    Sheet2.Range("B" & Index).Value = SRV
    Sheet6.Range("C11").Value = Sheet2.Range("B" & Index).Value
    Module1.Solver

    Sheet2.Range("C" & Index).Value = Sheet6.Range("C27").Value 'efficiency

    Sheet2.Range("D" & Index).Value = Sheet6.Range("C24").Value 'voc
    Sheet2.Range("E" & Index).Value = Sheet6.Range("C17").Value 'Current
    SRV = Round(SRV * 1.1, 1)
    Index = Index + 1
Loop




Sheet2.Activate


End Sub

Sub SweepParams()
'generate sweeps for any parameters, as entered in the worksheet

Dim RowIndex, ColumnIndex

Dim Parameters(1 To 5) As String


For ColumnIndex = 1 To 5
    If (Sheet3.Cells(2, ColumnIndex) <> "") Then
        Select Case Sheet3.Cells(2, ColumnIndex).Value
        Case "SRH_Tau"
            Parameters(ColumnIndex) = "C7"
        Case "Na"
            Parameters(ColumnIndex) = "C9"
        Case "Thickness"
            Parameters(ColumnIndex) = "C10"
        Case "SRV"
            Parameters(ColumnIndex) = "C11"
        Case "Internal_Concentration"
            Parameters(ColumnIndex) = "C14"
        End Select
    End If
Next ColumnIndex


RowIndex = 3

Do While (Sheet3.Range("B" & RowIndex))
    For ColumnIndex = 1 To 5 'length of parameters
        Sheet6.Range(Parameters(ColumnIndex)).Value = Sheet3.Cells(RowIndex, ColumnIndex).Value
    Next ColumnIndex
    Module1.Solver
    Sheet3.Cells(RowIndex, ColumnIndex + 1).Value = Sheet6.Range("C27").Value 'efficiency
    Sheet3.Cells(RowIndex, ColumnIndex + 2).Value = Sheet6.Range("C24").Value 'voc
    Sheet3.Cells(RowIndex, ColumnIndex + 3).Value = Sheet6.Range("C17").Value 'Current

    RowIndex = RowIndex + 1
Loop

Sheet3.Activate


End Sub

Sub SweepTwoParams()
'generate sweeps for any two parameters, as entered in the worksheet
```

```
'output is a X-Y matrix suitable for generating 3D plots
Dim RowIndex, ColumnIndex

Dim Parameters(1 To 2) As String


For ColumnIndex = 1 To 2
    If (Sheet4.Cells(2, ColumnIndex) <> "") Then
        Select Case Sheet4.Cells(2, ColumnIndex).Value
        Case "SRH_Tau"
            Parameters(ColumnIndex) = "C7"
        Case "Na"
            Parameters(ColumnIndex) = "C9"
        Case "Thickness"
            Parameters(ColumnIndex) = "C10"
        Case "SRV"
            Parameters(ColumnIndex) = "C11"
        Case "Internal_Concentration"
            Parameters(ColumnIndex) = "C14"
        End Select
    End If
Next ColumnIndex


RowIndex = 3
Col2Index = 3
Do While (Sheet4.Range("B" & Col2Index))
    Sheet4.Cells(22, Col2Index + 6).Value = Sheet4.Range("B" & Col2Index).Value
    Col2Index = Col2Index + 1
Loop

Do While (Sheet4.Range("A" & RowIndex))
    Sheet6.Range(Parameters(1)).Value = Sheet4.Cells(RowIndex, 1).Value
    Sheet4.Range("H" & RowIndex + 20).Value = Sheet4.Cells(RowIndex, 1).Value
    Col2Index = 3
    Do While (Sheet4.Range("B" & Col2Index))

        Sheet6.Range(Parameters(2)).Value = Sheet4.Cells(Col2Index, 2).Value

        Module1.Solver
        Sheet4.Cells(RowIndex + 20, Col2Index + 6).Value = Sheet6.Range("C27").Value 'efficiency
        'Sheet4.Cells(RowIndex, ColumnIndex + 2).Value = Sheet6.Range("C24").Value 'voc
        'Sheet4.Cells(RowIndex, ColumnIndex + 3).Value = Sheet6.Range("C17").Value 'Current

        Col2Index = Col2Index + 1
    Loop
    RowIndex = RowIndex + 1
Loop

Sheet4.Activate


End Sub
```