Chapter

Gate-All-Around FETs: Nanowire and Nanosheet Structure

Jun-Sik Yoon, Jinsu Jeong, Seunghwan Lee, Junjong Lee and Rock-Hyun Baek

Abstract

DC/AC performances of 3-nm-node gate-all-around (GAA) FETs having different widths and the number of channels (N_{ch}) from 1 to 5 were investigated thoroughly using fully-calibrated TCAD. There are two types of GAAFETs: nanowire (NW) FETs having the same width (W_{NW}) and thickness of the channels, and nanosheet (NS) FETs having wide width (W_{NS}) but the fixed thickness of the channels as 5 nm. Compared to FinFETs, GAAFETs can maintain good short channel characteristics as the W_{NW} is smaller than 9 nm but irrespective of the W_{NS}. DC performances of the GAAFETs improve as the N_{ch} increases but at decreasing rate because of the parasitic resistances at the source/drain epi. On the other hand, gate capacitances of the GAAFETs increase constantly as the N_{ch} increases. Therefore, the GAAFETs have minimum RC delay at the N_{ch} near 3. For low power applications, NWFETs outperform FinFETs and NSFETs due to their excellent short channel characteristics by 2-D structural confinement. For standard and high performance applications, NSFETs outperform FinFETs and NWFETs by showing superior DC performances arising from larger effective widths per footprint. Overall, GAAFETs are great candidates to substitute FinFETs in the 3-nm technology node for all the applications.

Keywords: gate-all-around, nanowire, nanosheet, field-effect transistors, fin, RC delay, parasitic resistance, parasitic capacitance

1. Introduction

Gate-all-around (GAA) is a widely-using structure such as logic field-effect transistor (FET) due to its excellent short channel characteristics [1–6] or its high surface-to-volume ratio [7, 8], 3-D NAND flash memory for bit-cost scalability [9, 10], photodiode due to its waveguide effect [11, 12], and gas sensor due to its high physical fill factor or surface-to-volume ratio [13, 14]. Especially for logic applications, GAAFETs have been introduced by attaining good gate electronics and increasing current drivability under the same active area.

Currently, fin-shaped FETs (FinFETs) have been scaled down to 10-nm node [15] and further to 5-nm node [16] by forming ultra-sharp fin for high current drivability while maintaining gate-to-channel controllability. GAAFETs are possibly showing great potential to substitute FinFETs in the following technology node, and the performance comparisons between FinFETs and GAAFETs have been investigated [3–6, 17]. But more detailed analysis between FinFETs and GAAFETs

is needed to set the device guideline by considering fine TCAD calibration and middle-of-line levels.

Therefore, in this work, DC/AC performances of 3-nm-node GAAFETs were investigated using fully-calibrated TCAD platform. By changing the GAA geometries, we found optimal GAA structure to minimize the RC delay for three different applications such as low power (LP), standard performance (SP), and high performance (HP) applications.

2. Device structure and simulation methods

All the simulation works were performed using Sentaurus TCAD [18]. Drift diffusion transport equations were calculated self-consistently with Poisson and electron/hole continuity equations. Density-gradient model was adopted for the quantum confinement of carriers within the channel. Slotboom bandgap narrowing model was used to consider the doping-dependent energy bandgap. Mobility models include Lombardi for the mobility degradation at the channel/oxide interface, inversion and accumulation layer model for impurity, phonon, and surface roughness scatterings, and low-field ballistic model for quasi-ballistic effects in ultra-short gate length (L_g). Shockley-Read-Hall, Auger, and Hurkx band-to-band tunneling recombination models were adopted. Deformation potential model was used to consider the stress-induced energy bandgap, effective mass, and effective density-of-states. All these physical models were used equivalently in [19, 20].

Figure 1 shows the schematic diagrams of FinFETs and three-stacked GAAFETs. FinFETs have highly-doped punch-through-stopper (PTS) at 2×10^{18} and 4×10^{18} cm^{-3} for NFETs and PFETs, respectively, in order to prevent the sub-fin leakage currents at off state [21, 22]. GAAFETs, on the other hand, have buried oxide (BOX) layer beneath the source/drain (S/D) regions without PTS so that the bottom leakage currents are completely blocked [1, 23]. Bulk FinFETs can adopt the BOX layer according to [24], but the conventional device structure

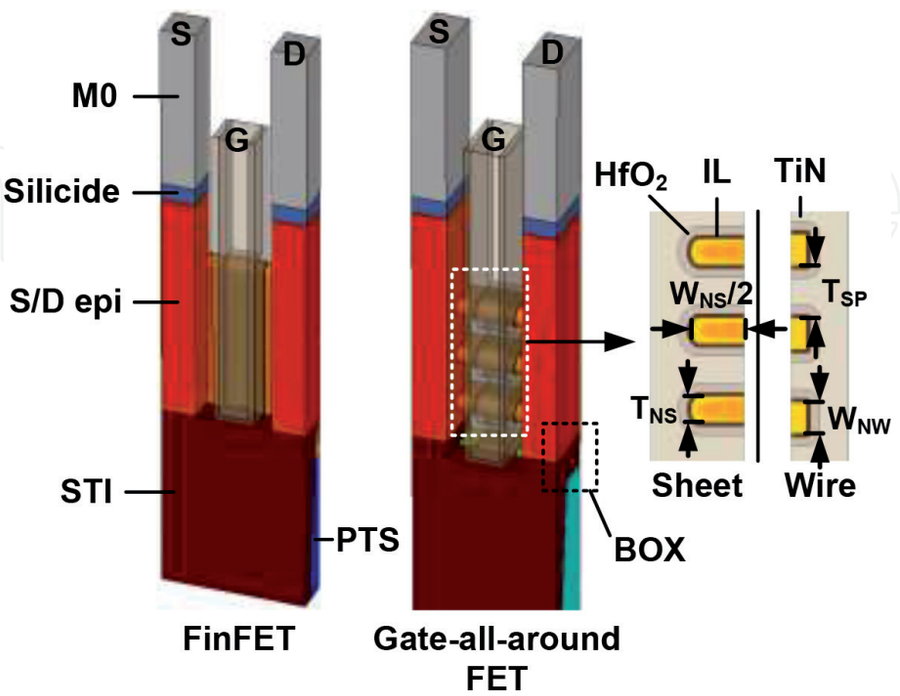

Figure 1.
Schematic diagrams of FinFETs and GAAFETs. 2-D cross-sections of nanosheet and nanowire channels were also specified to the right.

was considered in this work. S/D doping concentrations of the n-type and p-type devices are 2×10^{20} and 4×10^{20} cm^{-3}, respectively. Interfacial layer (IL), HfO_2, and low-k spacer regions have the dielectric constants of 3.9, 22.0, and 5.0, respectively. Contact resistivity at S/D and silicide interface is fixed to 10^{-9} $\Omega \cdot cm^2$ [25]. Equivalent oxide thickness (EOT) is 1.0 nm, which consists of 0.7-nm-thick IL and 1.7-nm-thick HfO_2.

Table 1 shows the geometrical parameters and values of 3-nm-node FinFETs and GAAFETs. Contacted poly pitch (CPP) and fin pitch (FP) are 42 and 21 nm, following 3-nm technology node [5]. There are two types of GAAFETs: nanowire FETs (NWFETs) having the same width and thickness as W_{NW}, and nanosheet FETs (NSFETs) having thin NS thickness (T_{NS}) of 5 nm but wide NS width (W_{NS}) as 10, 20, 30, 40, and 50 nm. The number of NW or NS channels (N_{ch}) is varied as 1, 2, 3, 4, and 5.

Figure 2 shows the schematic process flows of GAAFETs. The detailed gate-las process flows are described in [1]. After depositing $Si_{0.7}Ge_{0.3}$/Si multi-layer and etching like fin structure, poly-Si gate and low-k regions are formed. Inner-spacer is formed by etching sidewalls of $Si_{0.7}Ge_{0.3}$ regions selectively and depositing low-k regions. Followed by depositing BOX layer, selective epitaxial growth of S/D regions is performed. After removing poly-Si gate, channel release process is performed by etching $Si_{0.7}Ge_{0.3}$ regions selectively. Replacement metal gate, silicidation, and metal contact formations are done afterwards.

All the TCAD results were calibrated to Intel 10-nm node FinFETs [15]. Detailed calibration flows are as follows. Geometrical parameters such as L_g, fin width (W_{fin}), fin height (H_{fin}), CPP, and FP were referred from [15]. Subthreshold characteristics such as subthreshold swing (SS) and drain-induced barrier lowering (DIBL) were fitted by changing annealing temperature and time for proper S/D doping profiles. Saturation velocity was tuned to fit the drain current (I_{ds}) in the saturation region, whereas minimum low-field mobility and ballistic coefficient were varied to fit the I_{ds} in the linear region. Some parameters related to surface roughness scatterings were also modified to fit the I_{ds} in the strong inversion region accordingly. These calibration flows were equivalent as in [26]. After calibration, FinFETs were scaled down to the 3-nm node for comparison with GAAFETs.

Geometrical parameters		**Values**
CPP	Contacted poly pitch	42 nm
FP	Fin pitch	21 nm
NP	Nanowire/sheet pitch	W_{NW} or W_{NS} + 16 nm
L_g	Gate length	12 nm
L_{sp}	Spacer length	5 nm
W_{fin}	Fin width	5 nm
H_{fin}	Fin height	46 nm
W_{NW}	Nanowire width	5, 6, 7, 8, 9, 10 nm
W_{NS}	Nanosheet width	10, 20, 30, 40, 50 nm
T_{NS}	Nanosheet thickness	5 nm
T_{SP}	Nanowire/sheet spacing	10 nm
N_{ch}	The number of channels	1, 2, 3, 4, 5

Table 1.
Geometrical parameters and values of FinFETs and GAAFETs.

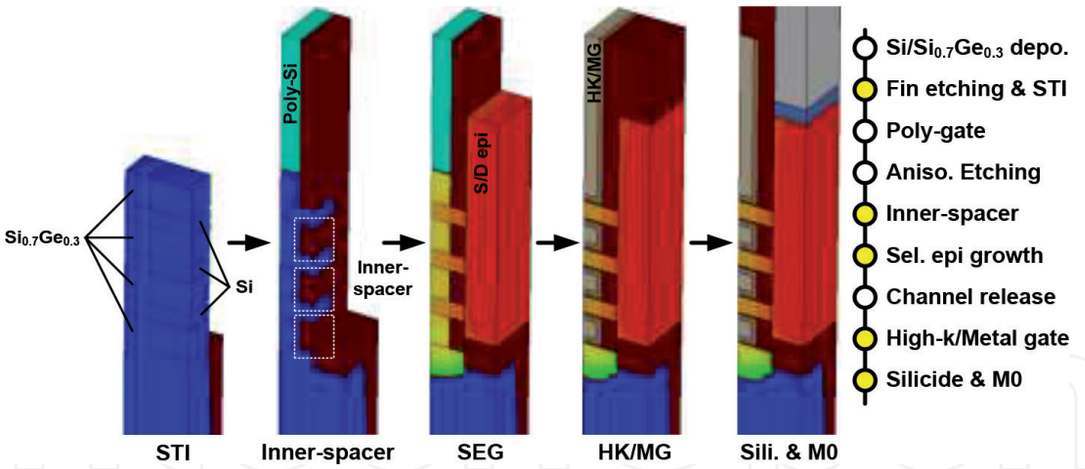

Figure 2.
Process flows of GAAFETs. Key process schemes of GAAFETs are $Si_{0.7}Ge_{0.3}$/Si multi-layer stacking, inner-spacer formation, and channel release by etching $Si_{0.7}Ge_{0.3}$ regions selectively.

3. Results and discussion

3.1 DC performances of NWFETs and NSFETs

Figure 3 shows the I_{ds} of all the GAAFETs having different W_{NW} or W_{NS} at the fixed N_{ch} of 3 at the drain voltages (V_{ds}) of 0.70 V. It is not shown in this figure, but the I_{ds} increases generally as the W_{NW} or W_{NS} increases irrespective of N_{ch}. As the W_{NW} increases, the I_{ds} shifts leftward and the gate-induced drain leakage (GIDL) increases by losing the gate-to-channel controllability [27]. P-type NWFETs have larger GIDL than n-type NWFETs due to larger S/D doping penetrations into the channel for p-type devices. On the other hand, NSFETs have small GIDL and I_{ds} shifts as thin T_{NS} of 5 nm forms 1-D structural confinement and maintains good short channel characteristics. To the following, there are three applications at different off-state currents (I_{off}): LP at the I_{off} of 100 pA/μm, SP at the I_{off} of 10 nA/μm, and HP at the I_{off} of 100 nA/μm [28]. These values were normalized to NP.

Figure 4 shows SS and DIBL of all the devices. Threshold voltages (V_{th}) and SS are extracted at the constant current of $W_{eff}/L_g \times 10^8$ A, where W_{eff} is the effective width equal to $2 \times H_{fin} + W_{fin}$ for FinFETs, $4 \times W_{NW} \times N_{ch}$ for NWFETs, and $(2 \times W_{NS} + 2 \times T_{NS}) \times N_{ch}$ for NSFETs. DIBL is calculated as the difference of the V_{th} at two different V_{ds} of 0.05 and 0.70 V for n-type (−0.05 and − 0.70 V for p-type) devices [29]. NWFETs degrade the short channel characteristics much than FinFETs as the W_{NW} is 9 and 10 nm. NSFETs, on the other hand, have smaller SS and DIBL than FinFETs even as the W_{NS} increases up to 50 nm because the gate-to-channel controllability is maintained by GAA structure and thin T_{NS} of 5 nm. But when the NWFETs have ultra-small W_{NS} of 5 or 6 nm, 2-D structural confinement decreases the SS and DIBL greatly, which would be preferable for LP applications. It is not shown in this figure, but the SS and DIBL are independent of N_{ch}.

Figure 5 summarizes the effective currents (I_{eff}) of n-type (top) and p-type (bottom) GAAFETs having different W_{NW} (or W_{NS}) and N_{ch}. I_{eff} was calculated using two I_{ds} at different V_{ds} and gate voltages (V_{gs}) as

$$I_{eff} = (I_H - I_L) / \ln\left(\frac{I_H}{I_L}\right) \quad (1)$$

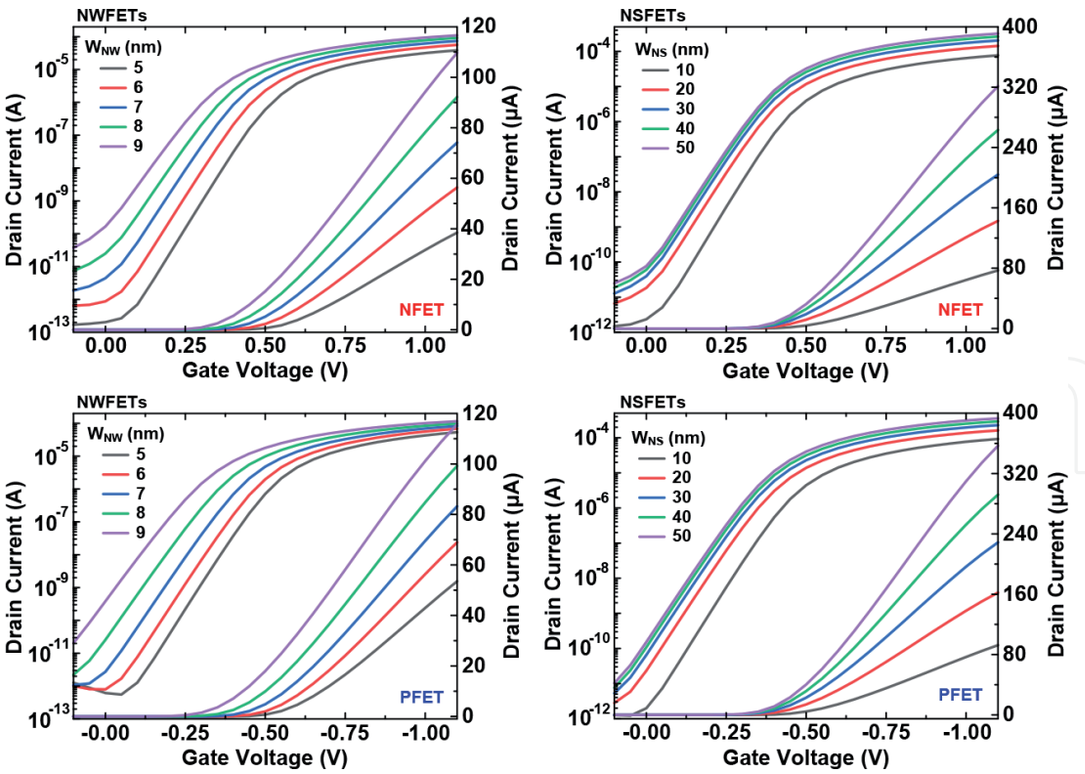

Figure 3.
I_{ds} of n-type (top) and p-type (bottom) NWFETs and NSFETs having different W_{NW} or W_{NS} at the fixed N_{ch} of 3 at the drain voltages (V_{ds}) of 0.70 V. it is not shown in this figure, but the GAAFETs have the same I_{ds} trends irrespective of N_{ch} (I_{ds} increases as the W_{NW} or W_{NS} increases).

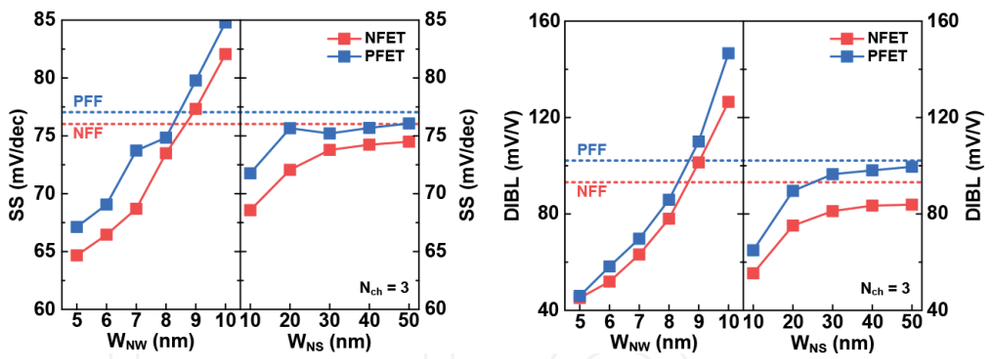

Figure 4.
SS (left) and DIBL (right) of FinFETs, NWFETs, and NSFETs having fixed N_{ch} of 3. It is not shown in this figure, but the GAAFETs have the same SS and DIBL irrespective of N_{ch}.

where $I_H = I_{ds}$ ($V_{gs} = V_{DD}$, $V_{ds} = V_{DD}/2$) and $I_L = I_{ds}$ ($V_{gs} = V_{DD}/2$, $V_{ds} = V_{DD}$) [30], and V_{DD} is the operation voltage fixed to 0.7 V. All the I_{eff} were normalized to the NP, and the I_{off} were fixed to 10 nA/μm for SP applications. GAAFETs need to have at least the N_{ch} of 3 to outperform the FinFETs. As the W_{NW} is 9 nm, both n-type and p-type NWFETs suffer from short channel effects (SCEs) and thus have smaller I_{eff} than the devices having smaller W_{NW} in spite of larger W_{eff}. NSFETs, on the other hand, have larger I_{eff} as the W_{NS} is larger as the SCEs are reduced by thin T_{NS} of 5 nm. But even though small same SS and DIBL are maintained for all the N_{ch}, the increasing rate of I_{eff} as a function of N_{ch} decreases as N_{ch} increases.

Figure 6 shows the S/D parasitic resistance (R_{sd}) of the GAAFETs having the W_{NW} or 7 nm and the W_{NS} of 30 nm as a function of N_{ch}. Other W_{NW} and W_{NS} have the same R_{sd} trends and thus are not shown in this work. R_{sd} was possibly extracted using *Y*-function method due to the linearity of *Y*-function at high V_{gs} [31]. As the

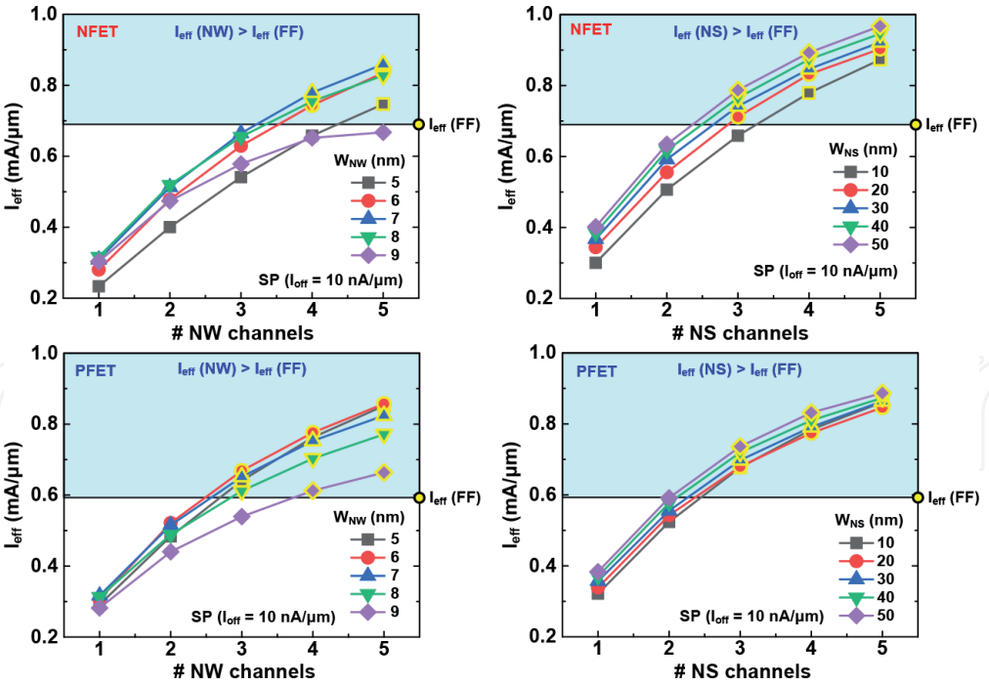

Figure 5.
I_{eff} of n-type (top) and p-type (bottom) GAAFETs having different W_{NW} (or W_{NS}) and N_{ch}. I_{eff} of n-type and p-type FinFETs are also specified as yellow symbols. Blue regions indicate that the GAAFETs have superior I_{eff} than the FinFETs.

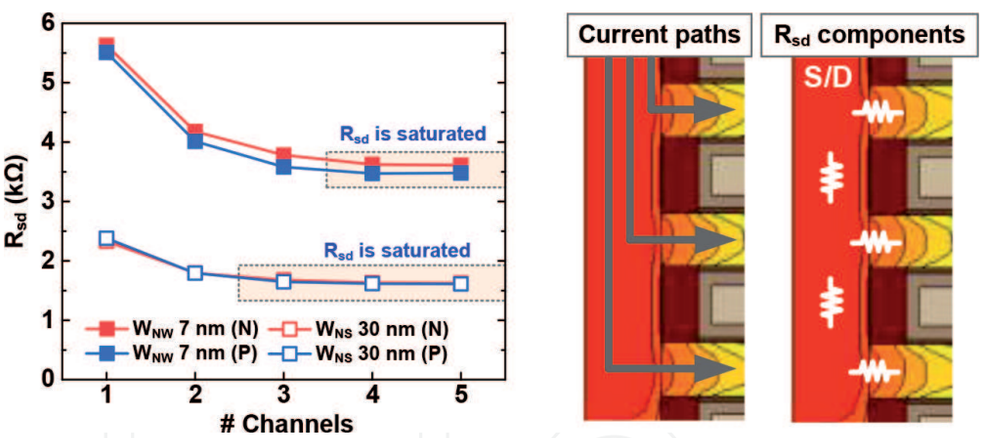

Figure 6.
R_{sd} of n-type and p-type GAAFETs having the W_{NW} of 7 nm and the W_{NS} of 30 nm as a function of N_{ch} (left) and the 2-D schematic diagram of half of the GAAFETs showing the current paths and R_{sd} components (right).

N_{ch} increases, R_{sd} of the GAAFETs decrease but at decreasing rate. Furthermore, R_{sd} becomes saturated as the N_{ch} is 3 or 4. This phenomena can be explained by 2-D schematic diagrams shown in the right of **Figure 6**. Since the S/D contacts reside at the top of the S/D epi, current paths start from the top toward the channels at the bottom. As the N_{ch} increases, longer current paths are needed to flow the bottom-side channels, facing more R_{sd} components at the S/D epi. Thus, increasing the N_{ch} beyond 3 or 4 does not help DC performance improvements greatly.

3.2 AC performances of NWFETs and NSFETs

Figure 7 summarizes the gate capacitances (C_{gg}) of all the GAAFETs. The C_{gg} is extracted at the V_{gs} and the V_{ds} of V_{DD}. Generally, C_{gg} increases as the W_{NW} (or W_{NS}) or N_{ch} increases due to the increased W_{eff}. PFETs have larger C_{gg} than NFETs due to larger S/D doping concentrations and penetrations into the channels. Different

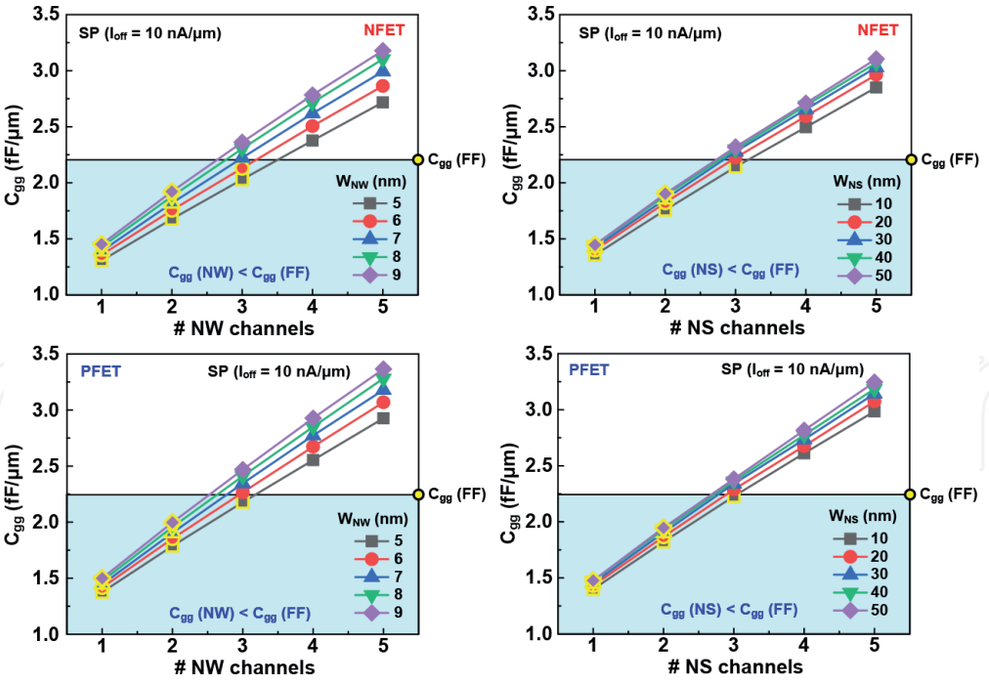

Figure 7.
C_{gg} of n-type (top) and p-type (bottom) GAAFETs having different W_{NW} (or W_{NS}) and N_{ch}. C_{gg} of n-type and p-type FinFETs are also specified as yellow symbols. Blue regions indicate that the GAAFETs have smaller C_{gg} than the FinFETs.

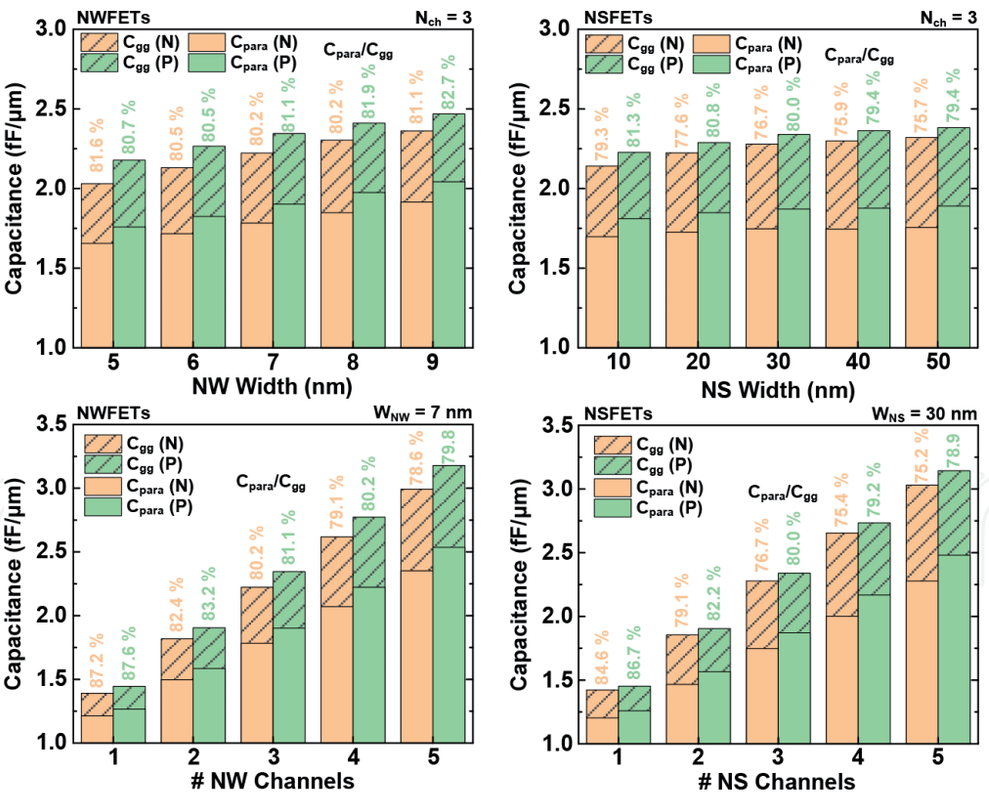

Figure 8.
C_{gg} and C_{para} of NWFETs (left) and NSFETs (right) having different W_{NW} (or W_{NS}) at the fixed N_{ch} of 3 and having different N_{ch} at the fixed W_{NW} of 7 nm (or W_{NS} of 30 nm). Percentages represent the C_{para}/C_{gg}.

from the I_{eff} trends, the GAAFETs have N_{ch} smaller than 3 to outperform the FinFETs, thus there are performance trade-offs between I_{eff} and C_{gg} as a function of N_{ch}. Furthermore, the increasing rate of C_{gg} as a function of N_{ch} is constant while the increasing rate of I_{eff} as a function of N_{ch} decreases, which would degrade the RC delay (= $I_{eff}V_{DD}/C_{gg}$) as the N_{ch} increases.

Figure 8 shows the C_{gg} and parasitic capacitances (C_{para}) of the GAAFETs varying N_{ch} and W_{NW} (or W_{NS}). C_{para} is extracted at off-state for SP applications. For all the cases, PFETs have larger C_{para} than NFETs due to larger S/D doping and penetrations into the channels [20]. At the fixed N_{ch} of 3, larger W_{NW} or W_{NS}, except for p-type NWFETs, decreases the C_{para}/C_{gg} because the proportion of the channels out of the metal gate increases. For the same reason, larger N_{ch} decreases the C_{para}/C_{gg}. Large C_{para}/C_{gg} at the W_{NW} of 9 nm for NFETs is because large SS forms on state before reaching strong inversion region.

Figure 9 shows the S/D doping profiles of NFETs (top) and PFETs (bottom) having different W_{NW} at the fixed N_{ch} of 3. In general, NFETs have larger doping concentrations in the middle of channels than PFETs because the Ge intermixing within multi-stacked $Si/Si_{0.7}Ge_{0.3}$ layers increases the Ge concentration at the channels and assists more phosphorus dopants diffusing into the channels while it segregates boron dopants [32–34]. Both NFETs and PFETs increase the doping concentrations in the middle of channels as the W_{NW} increases because the dopant segregations near the low-k spacer regions decrease [35]. But PFETs increase the doping concentrations in the middle of channels much due to smaller Ge intermixing for larger W_{NW}. This great increase of the doping concentrations in the middle of channels increases the C_{para}/C_{gg} for p-type NWFETs (as shown in **Figure 8**).

Figure 10 finalizes the RC delay of all the GAAFETs for LP, SP, and HP applications. N-type FinFETs have smaller RC delay than p-type FinFETs for all the applications due to better short channel characteristics, greater I_{eff} (as shown in **Figure 5**) and smaller C_{gg} (as shown in **Figure 8**). For LP applications, n-type GAAFETs having

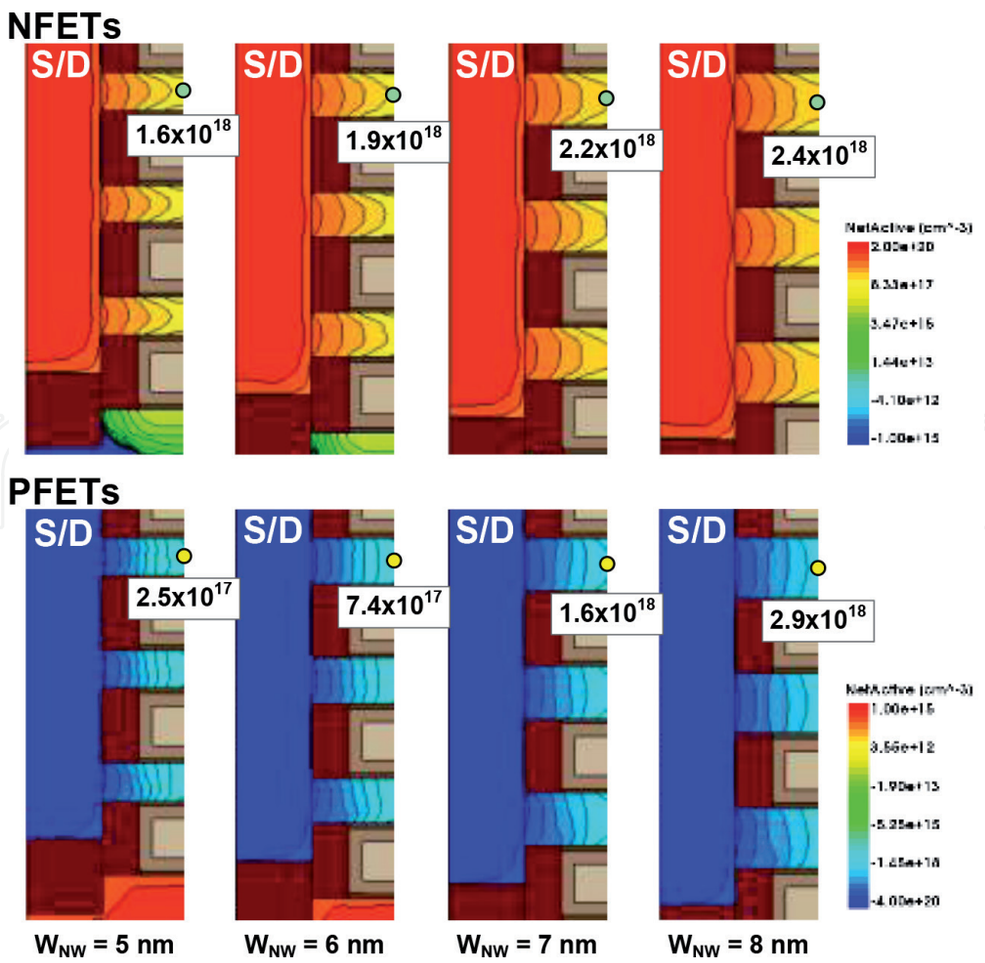

Figure 9.
S/D doping profiles of NFETs (top) and PFETs (bottom) having different W_{NW} at the fixed N_{ch} of 3. Doping concentrations in the middle of top-side channels are also specified.

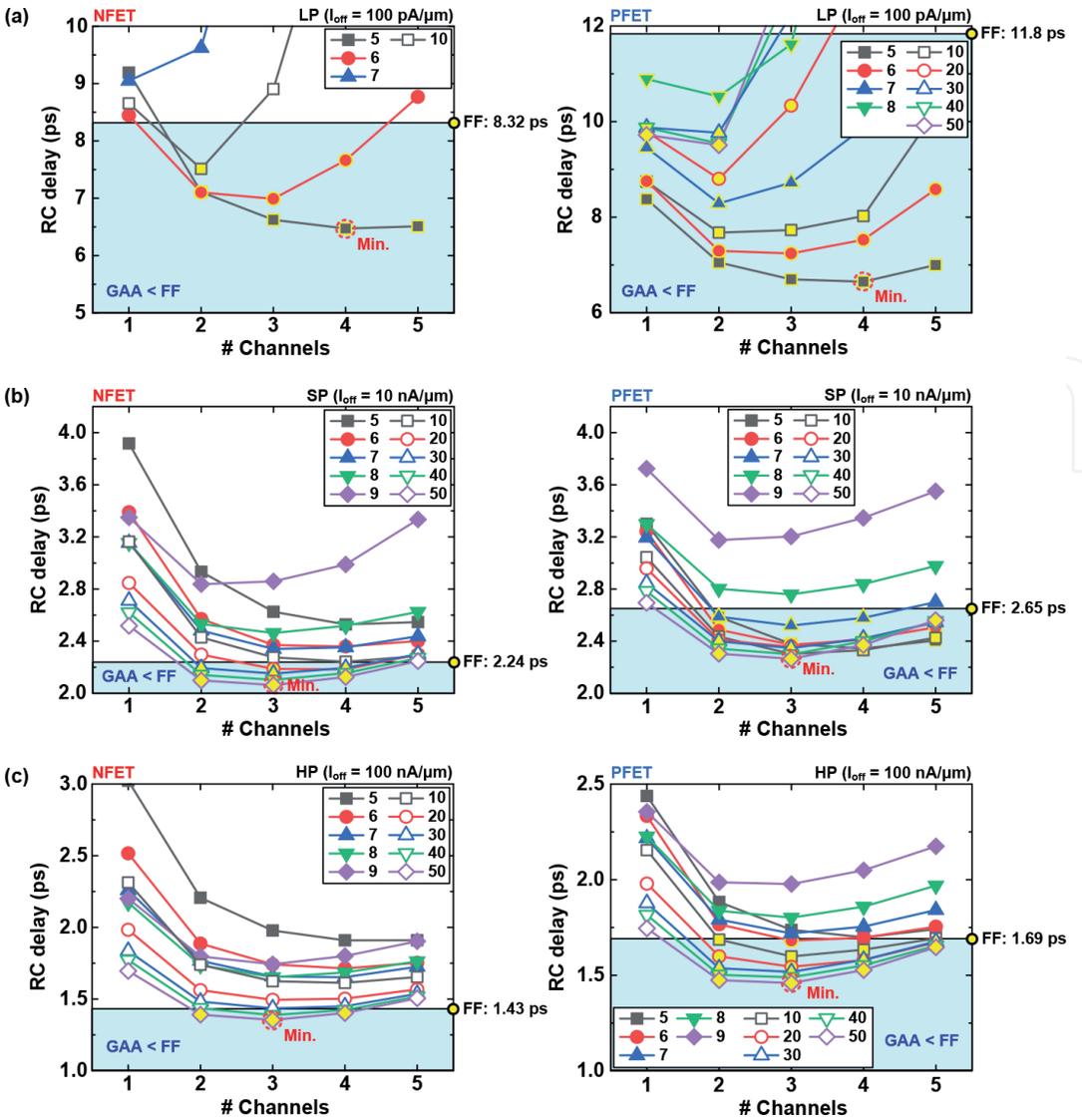

Figure 10.
RC delay of all the GAAFETs for (a) LP, (b) SP, and (c) HP applications. RC delay of FinFETs for three different applications are also specified. The devices having the RC delay smaller than FinFETs are marked as yellow.

small W_{NW} equal to 5 or 6 nm can outperform n-type FinFETs by decreasing SS and DIBL critically. But as the N_{ch} is 1 (or 5), the I_{eff} decreases greatly (or the C_{gg} increases greatly), thus degrading the RC delay. On the other hand, p-type GAAFETs have more W_{NW} or W_{NS} options to outperform p-type FinFETs because boron dopants of the GAAFETs are segregated by $Si/Si_{0.7}Ge_{0.3}$ intermixing and have more abrupt S/D doping profile than p-type FinFETs. For LP applications, both n- and p-type GAAFETs have the minimum RC delay at the W_{NW} of 5 nm and the N_{ch} of 4. For both SP and HP applications, both n- and p-type GAAFETs have the minimum RC delay at the W_{NS} of 50 nm and the N_{ch} of 3. As the W_{NS} increases beyond 50 nm, RC delay decrease but a little (as shown in **Appendix**). All these RC delay are achieved by enhancing the I_{eff} rather than the C_{gg}. To outperform the FinFETs, therefore, GAAFETs should be NWFETs, showing outstanding short channel characteristics, for LP applications and NSFETs, showing superior DC performance, for SP and HP applications.

4. Conclusion

3-nm-node GAAFETs have been analyzed by changing W_{NW} (or W_{NS}) and N_{ch} using fully-calibrated TCAD. Compared to FinFETs, GAAFETs have smaller and

SS and DIBL as the W_{NW} is smaller than 9 nm but irrespective of the W_{NS}. Both I_{eff} and C_{gg} of the GAAFETs increase as the N_{ch} increases, but the increasing rate of I_{eff} decreases due to the increase of R_{sd} at the longer S/D epi. The increasing rate of C_{gg}, on the other hand, is almost constant. Because of these phenomena, Minimum RC delay are formed at the middle N_{ch} of 3 or 4. The NWFETs having the W_{NW} of 5 or 6 nm achieve smaller RC delay than the FinFETs by achieving better gate electronics for LP applications, whereas the NSFETs having the W_{NS} of 40 or 50 nm increase the I_{eff} greatly and thus decrease the RC delay for SP and HP applications. Overall, GAAFETs are possible candidates to substitute FinFETs in the 3-nm technology node for all the applications by adopting different W_{NW} or W_{NS}.

Conflict of interest

The authors declare no conflict of interests.

Appendices and Nomenclature

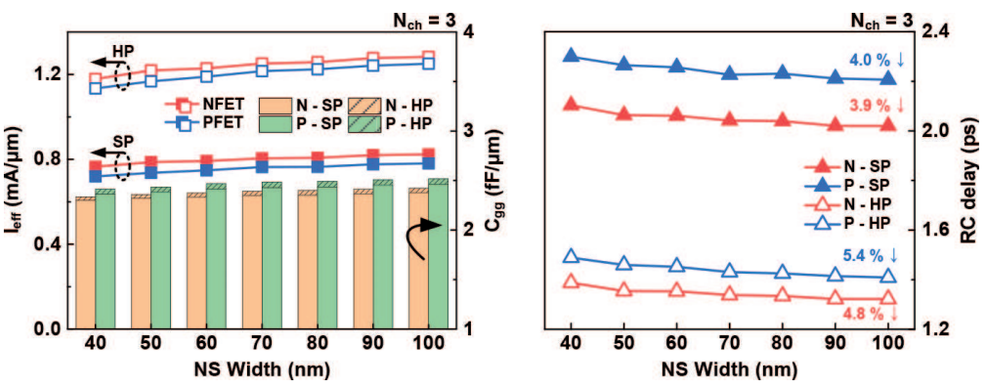

Figure A1.
I_{eff}, C_{gg}, and RC delay of the NSFETs having the W_{NS} of 40, 50, 60, 70, 80, 90, and 100 nm at the fixed N_{ch} of 3 for SP and HP applications.

Figure A1 shows the DC/AC performances of the NSFETs as the W_{NS} increases from 40 to 100 nm. Minimum RC delay are formed at the W_{NS} of 50 nm and the N_{ch} of 3 as shown in **Figure 10**, but much smaller RC delay can be attained as the W_{NS} increases to 100 nm by increasing the I_{eff} rather than the C_{gg} even though larger W_{NS} extends the device area. For the most, RC delay decrease by 5.4% for PFETs as the W_{NS} increases from 40 to 100 nm.

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