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AUTOMATIC REACTIVE POWER COMPENSATOR: AN OPEN LOOP APPROACH

A thesis submitted for the degree of Master of Philosophy

by

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ABSTRACT

Over the last few years the sudden increase of the use of non-linear loads such as personal computers and TV sets created a Power Factor (PF) problem. Although such loads consume relatively small amount of power, however the large number of these loads resulted on huge distortion in the power quality. One major element of the power quality is the PF. This thesis proposes an automatic PF correction circuit which can generate a leading as well as lagging reactive current which can be used to improve the PF. The proposed circuit consists of two semiconductor switches and two capacitors and an inductor. Such configuration is capable of generating not only variable reactive current, but also with very low distortion compared to other techniques, which usually generate a high distortion reactive current.

The proposed compensator is controlled by a microprocessor which generates the required switching pulses. The thesis also covers the protection circuits used to protect the semiconductor switches (MOSFETs) during the turn-on and turn-off times.

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List of Abbreviations

DC	Direct Current
PF	Power Factor
HVDC	High Voltage DC Transmission
TSC	Thyrister Switched Capacitor
MSC	Mechanical Switched Capacitor
PW	Pulse Width
PER	Period of the Cycle
RAM	Random Access Memory
ROM	Read Only Memory
EPROM	Erasable Programmable Read Only Memory
THD	Total Harmonic Distortion
FACTS	Flexible AC Transmission System

Chapter1

Introduction

1.1 Problem Overview

In the past, most of the loads were linear loads. A linear load is the load where the voltage across it and the current through follow the same pattern. For example if the voltage is sinusoidal the current is also sinusoidal. Calculations of power, and power factors in such loads were straight forward and most of these loads were fed from sinusoidal voltage and the power factor in these loads is simply *cos* the angle between the voltage and current. However, over the last 50 years, large non-linear loads such static power converters used in High Voltage DC transmission (HVDC) started to appear and due to the semiconductor devices used in such converters, the linear relationship between the voltage and current is not valid any more. Such large non-linear loads were identifiable and mechanisms for dealing with improving the power factor in such large non-linear loads were fully investigated. The main problem started to appear over the last 20 years where the number of 'small' non-linear loads has risen exponentially. For example a typical office building like the Howell building at Brunel University may have less than five PCs in 1985, it is now have more than 500 PCs. Such example is true for most of the buildings in the city. TV sets are another example of such 'small' non-linear loads, and it hardly to find a home now without at least two TV sets. This huge increase of 'small' non-linear loads comes with a price. The price is a very poor Power Factor (PF) and a much distorted current and voltage waveforms, in another word a very poor power quality. While 'large' non-linear loads are identifiable and correction devices can be installed to compensate for a predictable poor power factor, 'small' non-linear loads are widely spread and compensation mechanisms which are suitable for 'large' non-linear loads cannot be implemented for 'small' non-linear loads [2, 3].

This thesis investigates and proposes a compensator circuits which can be used to improve the power factor in both small linear and non-linear loads. The proposed compensators can be connected in shunt for 'retrofit application'. The advantages of this compensator are the ability to generate leading as well as lagging reactive powers and also the compactness of the design which make it more attractive and convenient in small size loads [11].

1.2 Aims and Objectives

The main aim of this research work is to design an automatic power factor compensation circuit which can be used to generate a variable leading as well as lagging reactive power for linear and non-linear loads. In order to achieve this main aim the following objectives were set:

- Investigate fully the PF problem in linear and non-linear loads.
- Proposing a compensator circuit.
- Finding a mathematical formula for the proposed circuit.
- Simulating the proposed compensator using PSPICE software.
- Investigating the control circuit and designing the protection for the semiconductor switches used in the compensator.
- Building and testing the proposed circuit.

1.3 Thesis Layout

This thesis is divided into six chapters. This chapter is introduction to the problems of feeding non-linear loads and also it gives a brief idea about compensation as basic solution for improving power factor in power system area.

The second chapter deals with the definition of power factor in linear and non-linear loads. The need for power factor correction was also summarised together with the costing analysis for power factor compensation. A numerical example to illustrate the need for a constantly variable capacitor for a changeable load was introduced. Two well known techniques (MSC and TSC) were briefly summarised. The TSC compensator was analysed in order to see the harmonic contents of such compensator. In some cases, and due to high current harmonics, such compensator will have negative effect on the power factor compensation.

The proposed automatic compensator is introduced in chapter three. The compensator is fully analysed for the possibility of generating leading as well as lagging power factors. The effective value of the capacitance of the compensator $C_{ceff\text{-}total}$ is evaluated by calculation, simulation and a comparison between the two sets of curves is introduced. The practical results of the automatic compensator are

also introduced showing the ability of the compensator to generate a variable amount of reactive current at different switching pattern. Such performance will require several banks of capacitors if ordinary fixed capacitors are used as a reactive power compensator.

In chapter four the automatic compensator is tested for improving the power factor in both linear and non-linear loads. Simulation and practical results are introduced to illustrate how the automatic compensator can improve the power factor in passive inductive loads as well as in a.c. voltage controllers (as an example of non-linear loads).

The power factor in such non-linear load decreases as the triggering angle of the thyristor increases. Obviously such circuits are used to control the output voltage applied to a load and this is achieved through the variation of the triggering angle. This means that the power factor is likely to be very poor in such applications.

In chapter five, the control of the compensator is discussed. The use of the microprocessor to produce the switching pattern for controlling the MOSFET switches is also investigated. The microprocessor was mainly set to generate the main control pulses and then a hardware circuit was used to generate the required overlapping pulses. The protection of the MOSFETs used in the compensator is fully investigated in the same chapter.

Chapter six contains the conclusions and the future work of this thesis. All relevant work which is essential but could interrupt the flow of the thesis are given in the appendices.

Chapter Two

Literature Review of Power Factor Compensator

2.1 Introduction

Inductive and capacitive loads create phase shift between voltage and current waveforms. The phase angle created by such loads can vary between 0 and 90 degrees. The current leads the voltage in the case of capacitive load and it lags the voltage in the case of inductive loads. This phase angle causes a poor power factor [1-3]. Also in non-linear loads such poor power factor can exist even if the load is a purely resistive. This chapter deals with problems caused by poor power factor and it also deals with methods for improving/correcting the power factor.

2.2 What is the Power Factor?

Power Factor (PF) is referred to in many literatures as the ratio of the Real Power to the Apparent Power and in the case of linear loads is '*cos'* the angle between the voltage and current [1,5,14].

$$P.F. = \frac{Real\ Power}{Apparent\ Power} = \cos \Phi \qquad 2.1$$

In non-linear loads such equation has to be derived from the beginning as follows. The supply voltage *v(t)* can be seen as a combination of several frequencies when added together they form the original voltage waveform. Similarly, the current in non-linear loads can also be seen as a combination of several frequencies when added together they form the original current waveform. Voltage and current harmonics having the same frequencies is referred to as *'n'* terms in equations 2.2 and 2.3. Voltage harmonics which do not have equivalent current harmonics is referred to as *'m'* terms in equations 2.2 and 2.3. Current harmonics which do not have equivalent voltage harmonics is referred to as *'k'* terms in equations 2.2 and 2.3.

$$v(t) = \sum^{n} \sqrt{2} V_n \sin(n\omega t + \alpha_n) + \sum^{m} \sqrt{2} V_m \sin(m\omega t + \alpha_m) \quad (2.2)$$

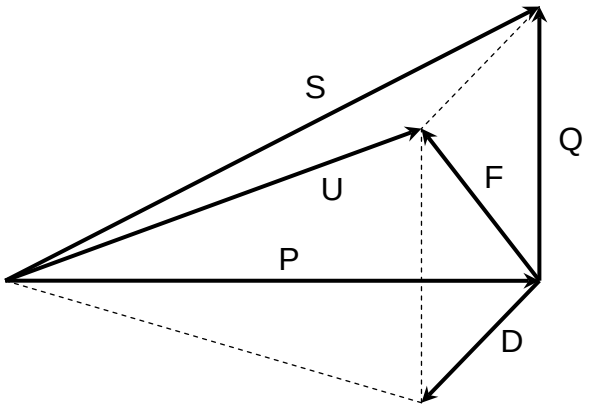
$$i(t) = \sum^{n} \sqrt{2} I_n \sin(n\omega t + \alpha_n + \phi_n) + \sum^{k} \sqrt{2} I_k \sin(k\omega t + \alpha_k) \quad (2.3)$$

$$Power\ Factor = \frac{\frac{1}{T}\int_0^T v\ i\ dt}{V\ I}$$

$$Power\ Factor = \frac{\sum^{n} V_n I_n \cos\phi_n}{\sqrt{(\sum^{n} V_n^2 + \sum^{m} V_m^2)(\sum^{n} I_n^2 + \sum^{k} I_k^2)}} \quad (2.4)$$

The power factor in such generic non-linear load can be seen as the ratio of active power (including the power consumed by other frequencies apart from the fundamental) to the apparent power [37]. The best way is to illustrate this by the diagram shown in Fig. 2.1

Fig. 2.1: "3D" Power Triangle



where:

P = Real Power

D = Distortion Power (only exists in non-linear loads)

Q = Reactive Power

F = Fictitious Power (=Reactive Power in linear loads)

S = Phasor Power (= Apparent power in linear load)

U = Apparent Power (non-linear load)

The ‘3D’ vector Apparent Power can be expressed as:

$$U = \sqrt{P^2 + Q^2 + D^2} \tag{2.5}$$

If the voltage distortion is ignored then the PF equation can be reduced to:

$$PF = \frac{V_1 I_1}{V_1 I} \cos \Phi_1 = \frac{I_1}{I} \cos \Phi_1 \tag{2.6}$$

The first term can be referred to as the distortion factor and the second tern can be referred to as the displacement factor.

Obviously if the load is linear load and there is no current harmonics, then the distortion factor is ‘1’ and the power factor equation is reduced to:

$$PF = \cos \Phi$$

The diagram in Fig. 2.2 shows the power factor triangle in linear loads.

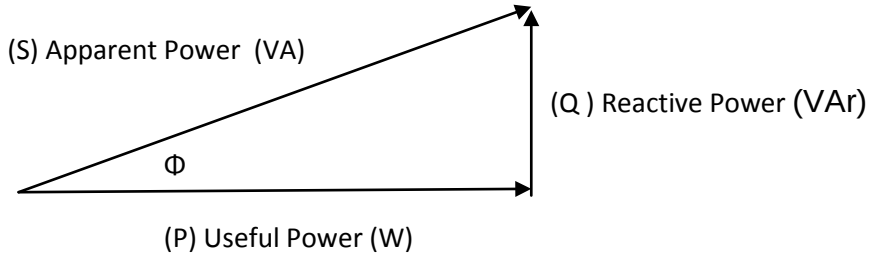


Fig. 2.2: Power Triangle in linear-loads

2.3 Power Factor Correction

As it can be seen from the previous section, at poor power factor the apparent power is much bigger than the real power. In order to generate amount of power (VA) similar or near similar to the required power (W) the power factor need to be as close as possible to unity. In non linear loads that can be achieved by passive and active filters. In linear loads that can be achieved by capacitors in parallel with the load. In either linear or non-linear loads the cost of poor power factor could be significant [1, 37, 40]. Since utility companies provide both the active and reactive

powers to meet the need for industrial consumers, they charge for KVA. That means they charge for poor power factor. The graph shown in Fig. 2.3 illustrates a typical energy charge for a small industrial customer before and after power factor correction. The details of this graph which shows the monthly billing information is given in Appendix 'A'.

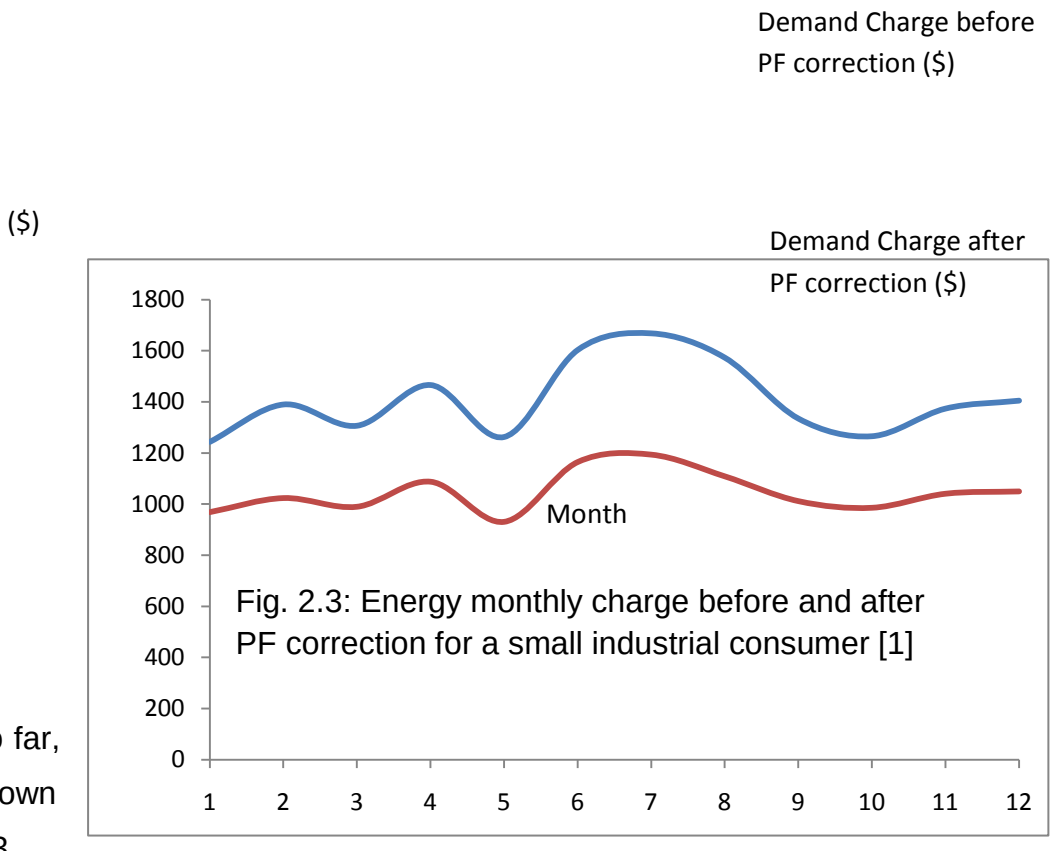


Fig. 2.3: Energy monthly charge before and after PF correction for a small industrial consumer [1]

So far, as shown in Fig. 2.3, the cost of operating at a poor PF is clearly illustrated. Those costs can be determined by understanding how the utility company calculates the electric bills. However, this is not the only cost associated with the poor PF, there are other hidden cost of poor power factor such as [1]:

- Reduces distribution system capacity
- Reduces terminal voltage equipment
- Increases heat loading in facility
- Shortens equipment life
- Creates kWh distribution losses that consumers pay for.

The following example illustrates how a poor PF reduces the capacity needed to supply additional loads:

System Capacity Released = $100 \times (1 - Pf_o / PF_f)$

Where: Pf_o = original PF

PF_f = final PF after correction

If the small industrial customer shown in Fig. 2.3 above wants to improve PF of 0.71 to 0.95:

% System Capacity Released = $100 \times (1 - 0.71 / 0.95) = 25.3\%$

That freed up capacity could allow the small industrial customer to add equipment, use smaller less expensive conductors, or avoid a costly capacity expansion project.

Improvement of power factor in linear loads using a fixed capacitor is well documented. However, a numerical example is introduced in this chapter as it will be taken as a case for a comparison when an automatic power factor correction is applied.

Numerical Example:

An inductive load has a resistance of 20 Ω and an inductance of 50 mH (connected in series) is supplied from 240 V, 50 Hz supply. Calculate the value of the shunt capacitor which can improve the power factor to 0.95 lagging.

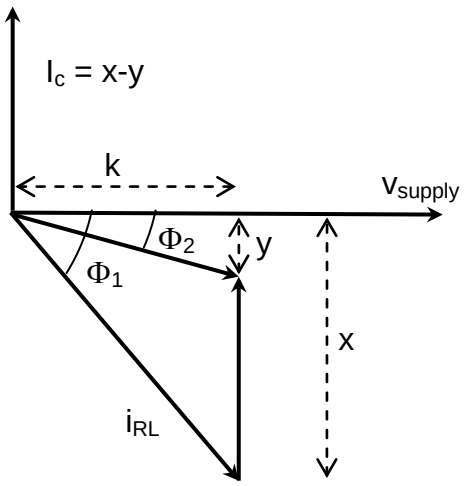


Fig. 2.4: Numerical example diagram

Referring to Fig. 2.4:

$X_L = 2 \times \pi \times f \times L = 15.7\ \Omega$

$Z = \sqrt{(20^2 + 15.7^2)} = 25.43\ \Omega$

$i_{RL} = 240 / 25.43 = 9.44$ A

$\Phi_1 = \tan^{-1} (X_L/R) = 38°$

$\Phi_2 = \cos^{-1} (0.95) = 18.2°$

$\sin \Phi_1 = x / i_{RL}$

$x = \sin 38 \times 9.44 = 5.8$

$k = \sqrt{(9.44^2 - 5.8^2)} = 7.45$

$\tan \Phi_2 = y/k$

$y = k \tan \Phi_2 = 2.45$

$x - y = 7.45 - 2.45 = 5$ (i_c should equal 5 Amp)

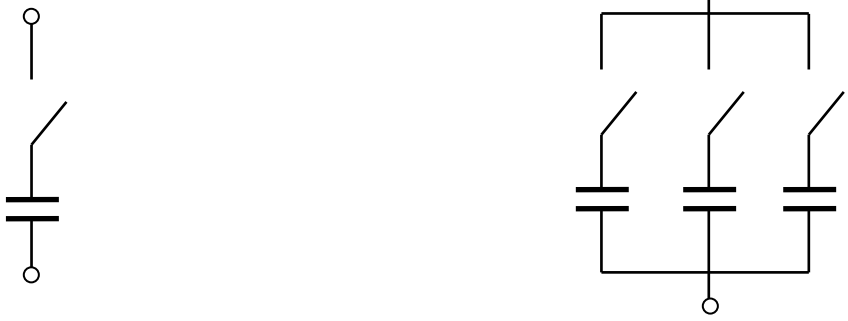
$X_c = V/i_c = 240 / 5 = 48\ \Omega$

$C = 1 / (2\ \pi\ f\ X_c) = 66\ \mu F$ (This is the value of the capacitor which will improve the power factor to 0.95.

It can be seen from the above example that if either the resistance or the inductance of the load varies, a different value of a compensating capacitor has to be re-evaluated. Also the supply frequency will affect the value of the required compensating capacitor. This can be a problem in some linear loads where the nature of the load requires continuous variation of the values of 'R' and 'L'. One solution is to use Thyristor-Switched Reactor (TSR) or Thyristor-Switched Capacitor (TSC). TSR is usually used for correcting the PF from a leading to a lagging. TSC is used for correcting the PF from a lagging to a leading. Since the proposed technique is used for lagging power factor correction, only the TSC is reviewed briefly below [8, 10].

2.4 Mechanically-Switched Capacitor (MSC)

In this technique capacitor is switched by circuit-breaker. Usually the MSC is switched only when needed. It could be a single capacitor with a single circuit-breaker or multi capacitors with multi circuit breakers in order to give variety of capacitances as shown in Fig. 2.5.



Single switch single circuit-breaker

Multi switch multi circuit-breaker

Fig. 2.5 MSC Compensator

2.5 Thyristor-Switched Capacitor (TSC)

In this technique, as shown in Fig. 2.6, the capacitor is connected in series with either two thyristors back to back or with a Triac. The thyristors (or the Triac) are either in zero or full conduction (α = 0° or α = 180°). The equivalent capacitive reactance in this circuit can be varied in stepwise manner. Although such technique can be effective in some applications, however the triggering of the thyristors in either zero or full conduction can cause the generation of huge amount of current harmonics. So although the displacement factor component in the power factor is improved, the distortion factor (due to the current harmonics) is significantly reduced. Fig. 2.7 illustrates the voltage and current waveforms as well as the frequency spectra of the current waveforms. It is very clear in this figure that the

current harmonics are having almost the same amplitude which is approximately 50% of the fundamental component of the current waveform [2, 20].

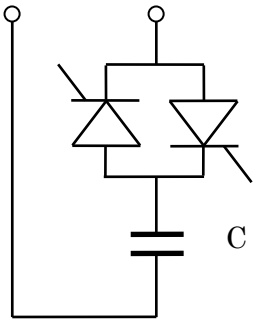
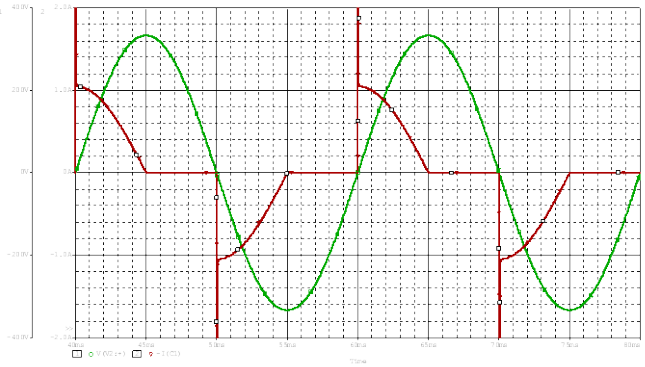
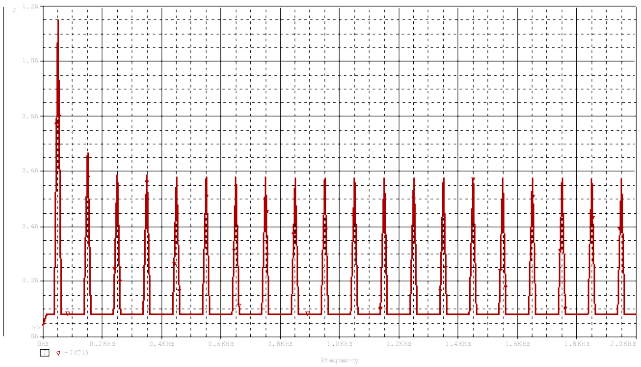


Fig. 2.6: TSC Compensator



Supply voltage (green) and compensator current (red) in the TSC circuit



Spectra of the current harmonics in the TSC circuit

Fig. 2.7: Waveforms in TSC circuit

2.6 Summary

In this chapter definition of power factor in linear and non-linear loads have been introduced. The need of power factor correction was also summarised together with the costing analysis for power factor compensation. A numerical example to illustrate the need for a constantly variable capacitor for a changeable load was introduced. Two well known techniques (MSC and TSC) were briefly summarised. The TSC compensator was analysed in order to see the harmonic contents of such

compensator. In some cases and due to high current harmonics, such compensator will have negative effect on the power factor compensation.

In the next chapter a more sophisticated technique for power factor compensation with low harmonic contents is introduced.

Chapter 3

Proposed Compensator

3.1 Introduction

In this chapter an automatic capacitor compensator circuit is introduced. The compensator is then analysed, simulated and practically verified. Harmonic analysis of the compensator is carried out and the same numerical example shown in the previous chapter is re-introduced again but using the automatic compensator in order to compare the effectiveness of the proposed technique. In general the main purpose of this chapter is to show how the effective capacitance of an automatic capacitor circuit can be varied by simply varying the timing of the on-off switching.

3.2 The Automatic Compensator

The compensator is constructed from two fixed capacitors and two semiconductor switches. The choice of the semiconductor switches is discussed in details in chapter 5. However, in this chapter the switch can be seen as an ideal bidirectional switch where it can be switched on or off at any time and allow the current to flow in any direction as well as it can operate at relatively high frequency (less than 10kHz). The compensator consists of a semiconductor switch S_1 which is connected in series with a fixed capacitor C_1 and S_2 is similarly connected in series with C_2. The two branches are then connected in parallel and the whole combination is connected in series with an inductor L as shown in Fig. 3.1. The resistor shown in the figure only represents the resistance of the inductor, switches, capacitors, and the wires. The reason the resistor is used so that it can cause the circuit to reach the steady state in the simulation, and there is no actual resistance added in the practical setup [7, 17].

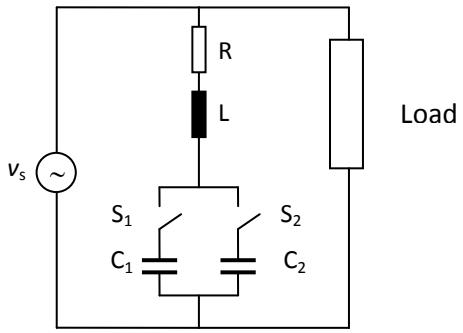


Fig. 3.1: The automatic compensator circuit

The two switches operate in anti-phase manor so that when S_1 is closed, S_2 is open and vice versa. The control pulses used for the control of the switches can be illustrated in Fig. 3.2

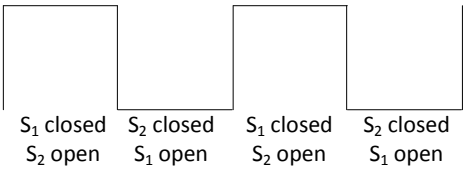


Fig. 3.2: Operation of S_1 and S_2

The 'on' time of the switch can be controlled so that the 'on'/('on'+'off'') ratio can be varied from '0' to '1'. This ratio is referred to as the switch duty cycle 'λ'. If 'λ' is '0' for S_1, it will be '1' for S_2 and vice versa. For convenience the symbol 'λ' is used in conjunction with S_1 throughout the rest of this thesis.

3.3 Calculations of the Effective Capacitance

The objective of this section is to calculate the effective capacitor value of the automatic compensator.

With reference to Fig. 3.1, the supply voltage can be expressed as:

$$V_s = L \frac{di(t)}{dt} + \frac{1}{C} f_s(t) \int_0^t f_{s1}(\tau)\, i(\tau)\, d\tau \qquad 3.1$$

The above equation is considerably simplified for only fundamental component. Following the procedure described in reference [31] the effective value of the capacitance of the two capacitors and the two switches can be written as:

$$C_{eff} = \frac{C_1}{\lambda^2 + \gamma(1-\lambda)^2} \qquad 3.2$$

where:

$$\lambda = \frac{T_{on}}{T_{on} + T_{off}} \qquad 3.3$$

$$\gamma = \frac{C_1}{C_2} \qquad 3.4$$

The equivalent capacitive reactance of C_{eff} can be written as:

$$X_{Ceff} = \frac{1}{2\pi f C_{eff}} \qquad 3.5$$

Similarly, the effective impedance (Z_{eff}) of the compensator can be written as:

$$Z_{eff} = \sqrt{R^2 + (\mathrm{X_{ceff}} - \mathrm{X_L})^2} \qquad 3.6$$

where:

$$X_L = 2\pi f L \qquad 3.7$$

R is the resistance of the inductor, switches, capacitors, and the wires as explained in section 3.2 above and therefore is very small.

If the value of the inductor is chosen to so that X_L is smaller than X_{ceff} for all value of λ, and R is very small then Z_{eff} will have the effect of a capacitor and the whole compensator circuit is a capacitive equivalent circuit. Therefore Z_{eff} can be referred to as $X_{ceff\text{-}total}$ and the equivalent capacitance of the compensator in this case will be $C_{ceff\text{-}total}$.

An Excel program was used to calculate the variable value of $C_{ceff\text{-}total}$ against the duty cycle (λ). Fig 3.3 illustrated this relationship and it can be seen from the figure that $C_{ceff\text{-}total}$ equal 124μF at λ=0 and 12.6 μF at λ=1. The maximum $C_{ceff\text{-}total}$ occurs at λ=0.1 and has the value of 140μF. Also it is clear from the graph that by selecting the appropriate duty cycle $C_{ceff\text{-}total}$ can be varied from 12.6 μF to 140μF. The range of $C_{ceff\text{-}total}$ in this case is:

140μF – 10.2 μF = 129.8 μF. The ratio of the value of this range to the maximum value of $C_{ceff\text{-}total}$ (denoted as ξ) will be the following. The general Equation to ξ:

$$\xi = \frac{129.9\ \mu F}{140\ \mu F} = 0.927\ \ (Say\ 93\%)$$

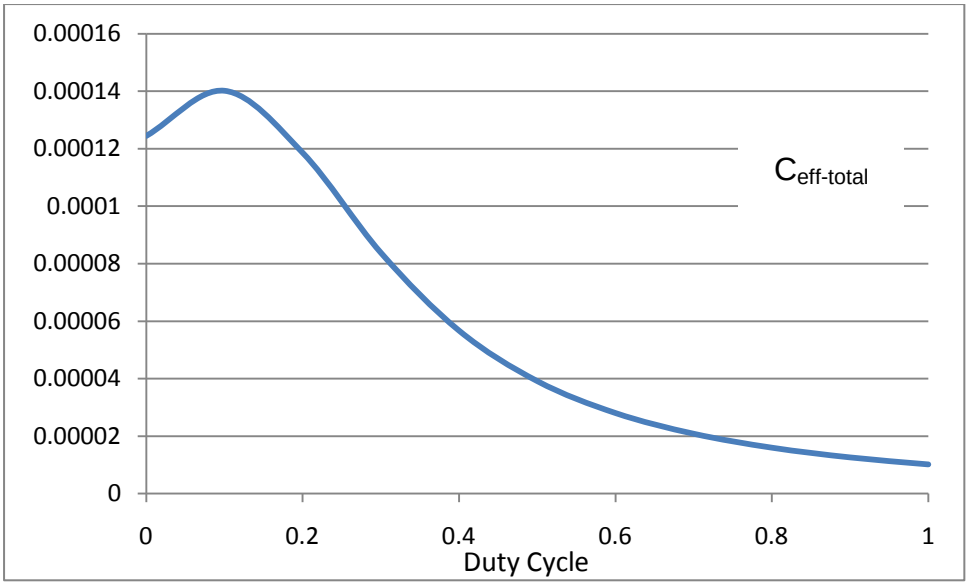


Fig. 3.3: The effective value of the capacitor as a function of the duty cycle λ. (C_1=10uf, C_2=100uf, L= 5mH, R = 1Ω)

If the value of the two fixed capacitors are equal, say $C_1 = C_2 = 100\mu F$, the peak value of $C_{ceff\text{-}total}$ will be shifted to 0.5 duty cycle as shown in Fig.3.4. $C_{ceff\text{-}total}$ at 0.1 duty cycle ($\lambda = 0.1$) in this case is the same as $C_{ceff\text{-}total}$ at 0.9 duty cycle ($\lambda = 0.9$) and is equal to 124 μF. The peak value of $C_{ceff\text{-}total}$ at $\lambda = 0.5$ in this case equals to 329 μF. The value of ξ with reference to Fig. 3.4 in this case will be:

$$\xi = \frac{329\ \mu F - 124\ \mu F}{329\ \mu F} = 0.623\ \ (Say\ 62\%)$$

It is obvious that a large value of ξ is desirable, this is mainly because a wide range of $C_{ceff\text{-}total}$ will allow a wide range of compensation. However, as it will be seen later in the simulation section that a large value of ξ comes on the expense of a large harmonic distortion.

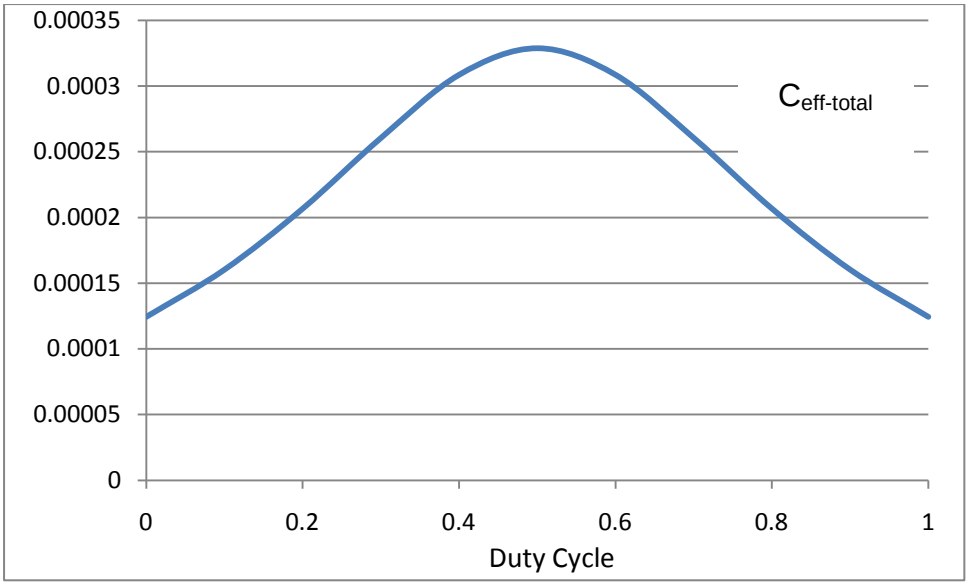


Fig. 3.4: The effective value of the capacitor as a function of the duty cycle λ (C_1=100uf, C_2=100uf, L= 5mH, R = 1Ω)

The above two cases (Figs. 3.3 and 3.4) are the two extreme cases, where the value of ξ is either minimum (≈ 0.62) or maximum (≈ 0.93). The graphs shown in Fig. 3.5 illustrate how the value of $C_{ceff\text{-}total}$ respond to different duty cycles as well as to different ratios of C_1 / C_2. This figure can help the designer in selecting the suitable fixed values for C_1 and C_2 for a particular $C_{ceff\text{-}total}$, however such choice is also determined by the harmonic contents of the compensating current as will be discussed in section 3.5. Fig. 3.6 shows the relation between ξ to γ. It can be seen from this figure that γ has an inversely proportional relationship with ξ. It is important to mention that the values of $C_{ceff\text{-}total}$, shown in Fig. 3.5 did not take into consideration any harmonic contents in the compensating current. The graphs in this figure are only based on the calculation of the fundamental component. In the simulation and practical sections which will follow, the values of $C_{ceff\text{-}total}$, will be re-presented but without ignoring any harmonic distortion. A comparison of the calculated, simulated and practical results will show that the calculated results presented in Fig. 3.5 gives an accurate envelop of $C_{ceff\text{-}total}$.

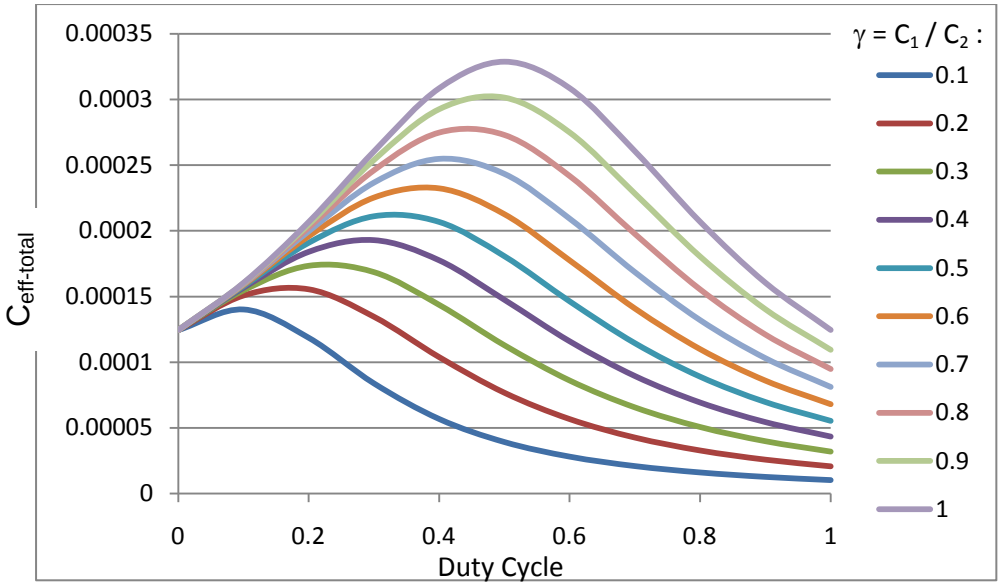


Fig. 3.5: The effective value of the capacitor as a function of the duty cycle (λ) at different value of capacitor ratios (γ)

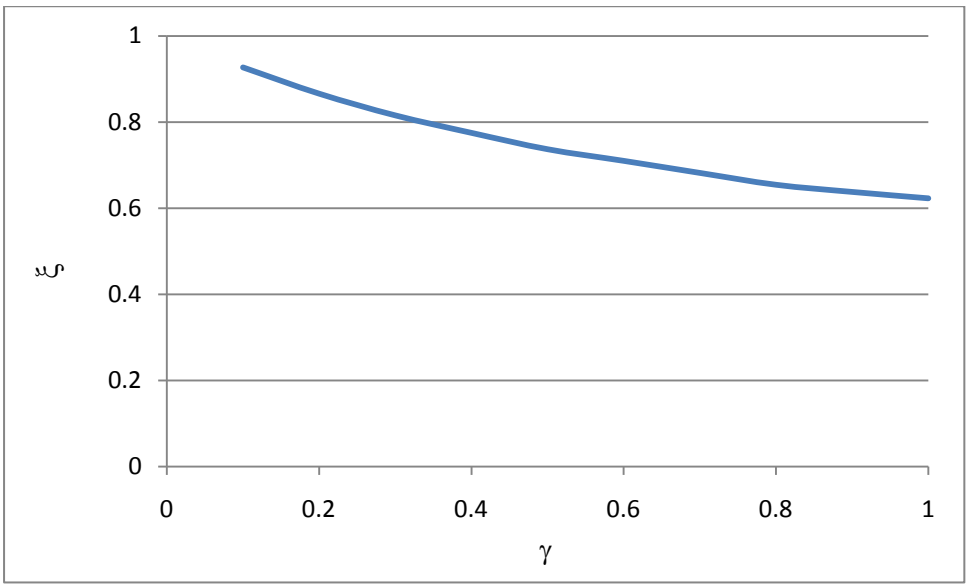


Fig. 3.6: Calculated Relationship between ξ and γ

Appendix B contains the calculated values of $C_{ceff\text{-}total}$ for different values of 'λ' and 'γ'.

3.4 Simulation of the Effective Capacitance

In order to verify the calculated results in section 3.3, the compensator circuit has been simulated using PSPICE software. The switches used in the simulation were ideal switches (Sbreak), and this is mainly to see the overall characteristics of the compensator. In chapter 5 the ideal switches are replaced by semiconductor switches (MOSFETs) in order to study the detail behaviour of the compensator (losses, etc.). The ideal switches are controlled by applying 'Vpulse', The parameters used in 'Vpulse' are shown in Fig. 3.7, where the value of 'λ' is 'PW/PER'. The switching frequency can be selected through 'PER' (f_s = 1/PER).

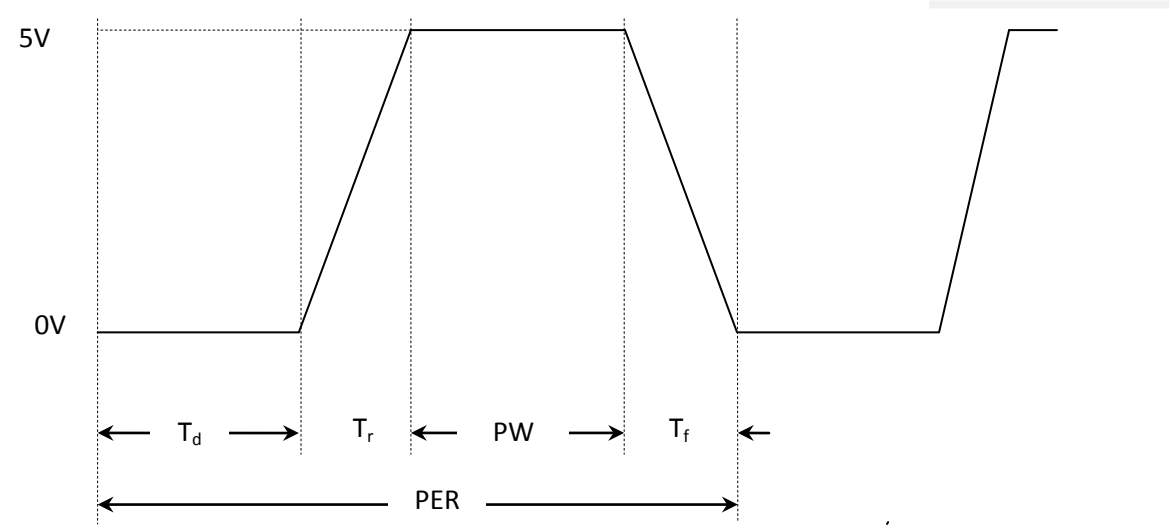


Fig. 3.7: Details of Vpulse

where T_d is delay time and T_r is rising time. Fig. 3.8 illustrates the circuit used in the simulation. The supply current and the compensator current are shown in Fig, 3.9. It is very clear from Fig. 3.9 that circuit current leads the supply voltage by 90°. This indicates that the compensator performs like a capacitor. The value of the compensator current can vary in magnitude simply by varying the duty cycle 'λ' of the switches, however the current at all values of 'λ' remains reactive current (i.e. leads the supply voltage by 90°.). This is illustrated in the current waveforms shown in Fig. 3.10 where 'λ' is 0.5 in one case and equals 0.25 in the other case. It is

noticeable that at 'λ' = 0.25, the compensator current contains some harmonic distortion. This distortion analysis is covered in details in section 3.6.

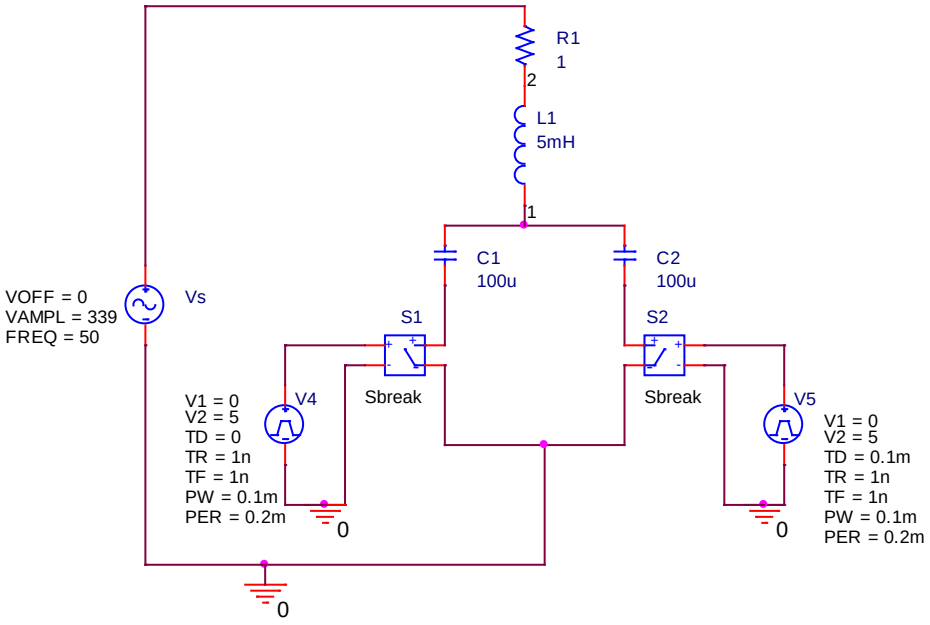


Fig. 3.8: The automatic compensator circuit used in PSPICE

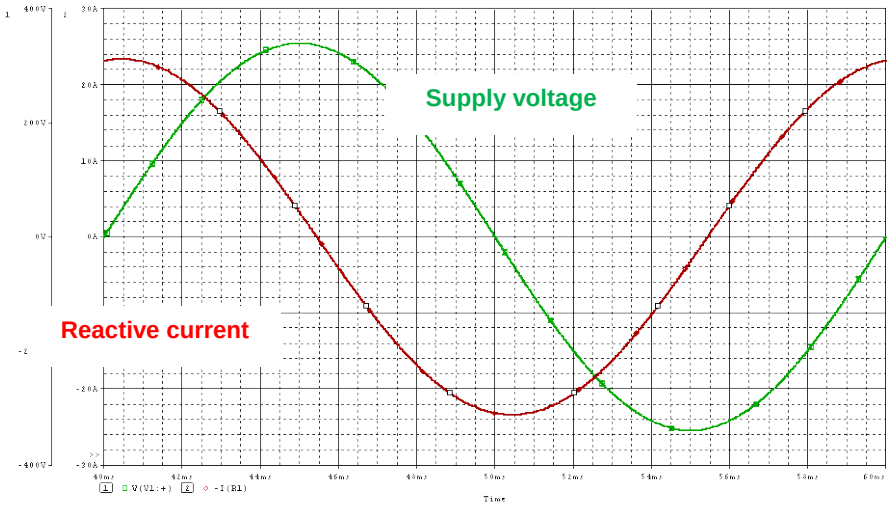


Fig. 3.9: Supply voltage and reactive current of the circuit in Fig. 3.7 (50Hz)

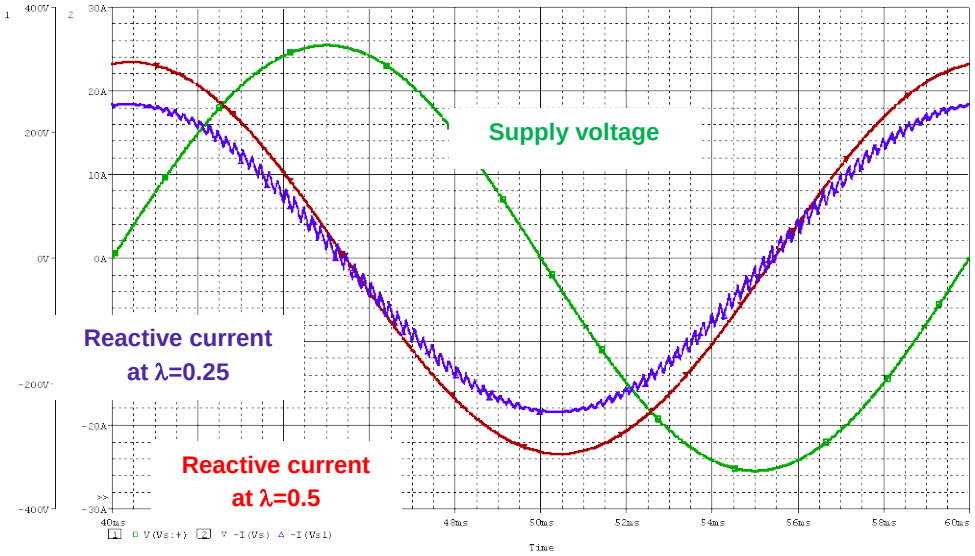


Fig. 3.10: Supply voltage and reactive currents at different duty cycles (λ). (50Hz).

The simulated result for $C_{ceff\text{-}total}$ when C_1 is 0.1 C_2 is shown in Fig. 3.11. It can be seen from that figure that $C_{ceff\text{-}total}$ can be varied from ≈14μF to ≈160μF through the selection of the appropriate duty cycle 'λ'. The shapes of Figs 3.3 and 3.11 are almost identical; however there is a difference in the values of $C_{ceff\text{-}total}$ in both cases. This difference is investigated in section 3.5.

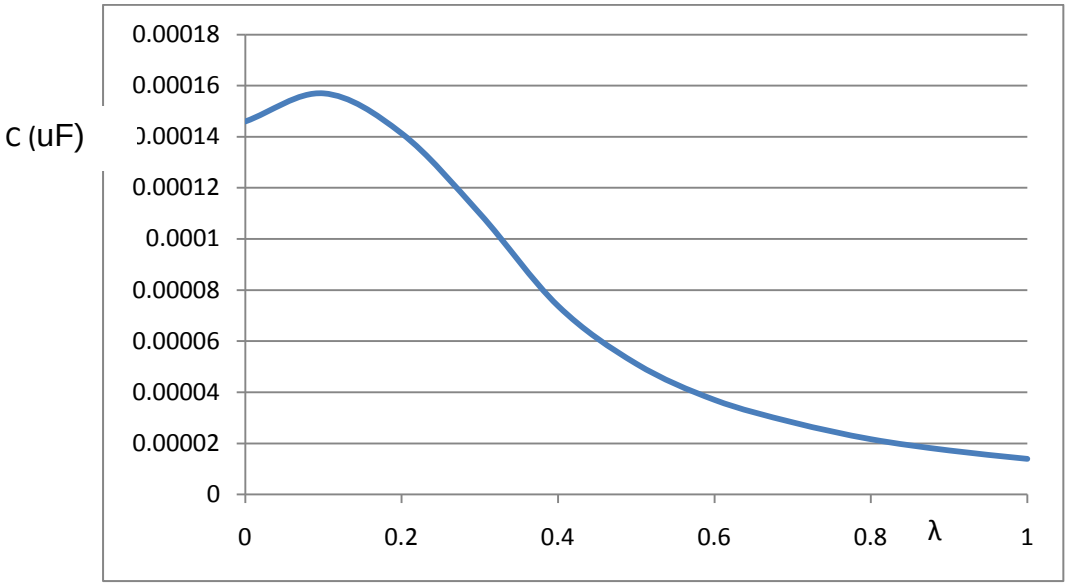


Fig. 3.11: The simulated effective value of the capacitor as a function of the duty cycle λ. (C_1=10uf, C_2=100uf, L= 5mH, R = 1Ω)

The graph at $C_1 = C_2 = 100uF$ is shown in Fig. 3.12 and it has the same envelop as the calculated graph at the same values (shown Fig. 3.4). It can also be concluded from Figs 3.11 and 3.12 that γ has an inversely proportional relationship with ξ. This can be shown in Fig. 3.13 where both the calculated graph (shown in Fig. 3.6) and the simulated graph are illustrated together for a comparison. The difference between the two graphs is discussed in section 3.5.

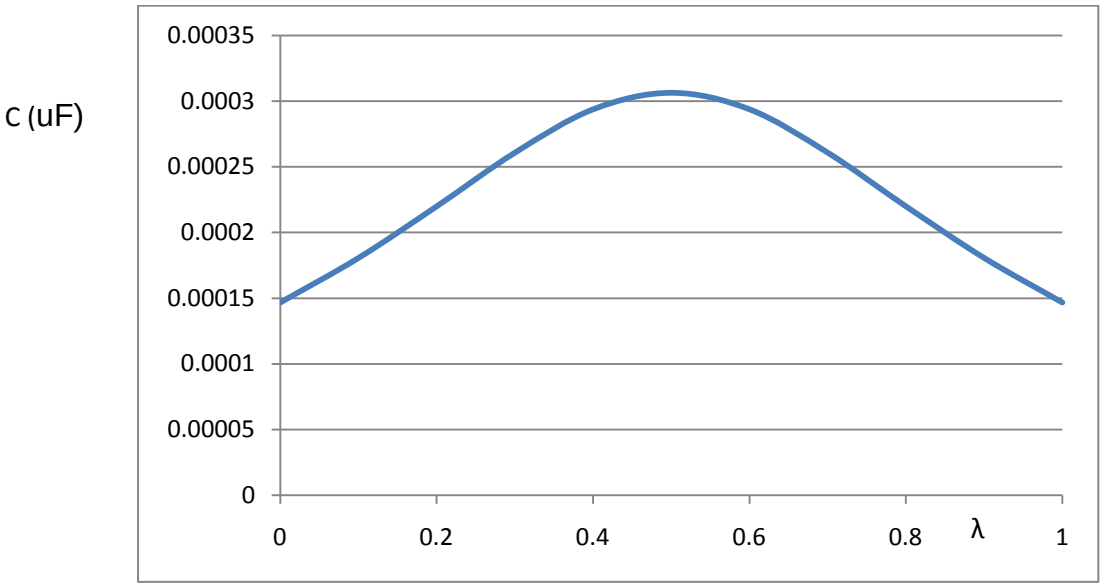


Fig. 3.12: The simulated effective value of the capacitor as a function of the duty cycle λ. ($C_1 = C_2 = 100uf$, L= 5mH, R = 1Ω)

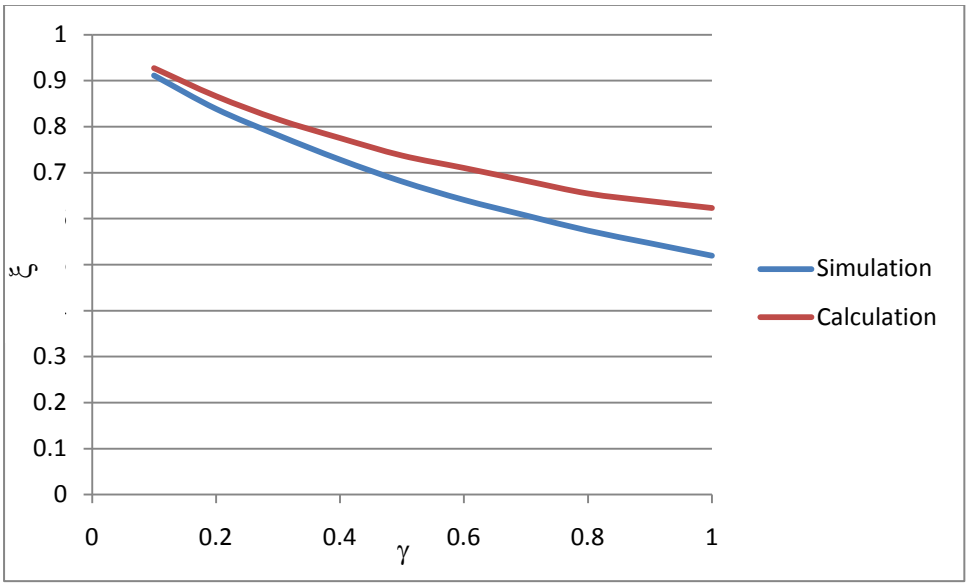


Fig. 3.13: Simulated and Calculated Relationship between ξ and γ

3.5 Comparison between Simulation and Calculated Results

In the calculation results presented in section 3.1, it has been assumed that the total compensator current is free from any harmonics and hence the calculation of $C_{ceff\text{-}total}$ was based on this assumption. If the harmonic in the current waveform is to be taken into consideration then the calculation would have been very complicated. Also by looking at the reactive compensator current (shown in Fig. 3.10), where the reactive current waveform is very close to a sinusoidal waveform, such assumption (ignoring current harmonics) can be justified. However, at some duty cycles and also at some values of 'γ', the harmonic distortion could be large.

As for the simulation results presented in the previous section (3.4), there was no need to make such assumption as the value of the current taken in the calculation of $C_{ceff\text{-}total}$ was the total current and not just the fundamental as in the case of the calculated results. Therefore, the simulation curves are more accurate compared to the calculated curves. However it has to be noticed that both calculated and simulated curves have very similar envelops.

It should also be noticed that there are several levels of simulations depending of the packages used. For example a simulation based on MATLAB is very likely to give results very close to the calculated results, however a simulation based on PSpice is more likely to give results closer to the practical setting. This is mainly because in PSpice details of the circuit parameters are considered in the simulation and most of the practical devices (capacitors, inductors, switches, etc.) have PSpice library available which gives very close simulation performance like the practical ones.

In order to see the effect of the assumption of ignoring the harmonics in the compensated current, values of $C_{ceff\text{-}total}$ for calculated and simulated results are put together for different values of 'γ' and for different duty cycle 'λ', as shown in Fig. 3.14. [see Appendix C]

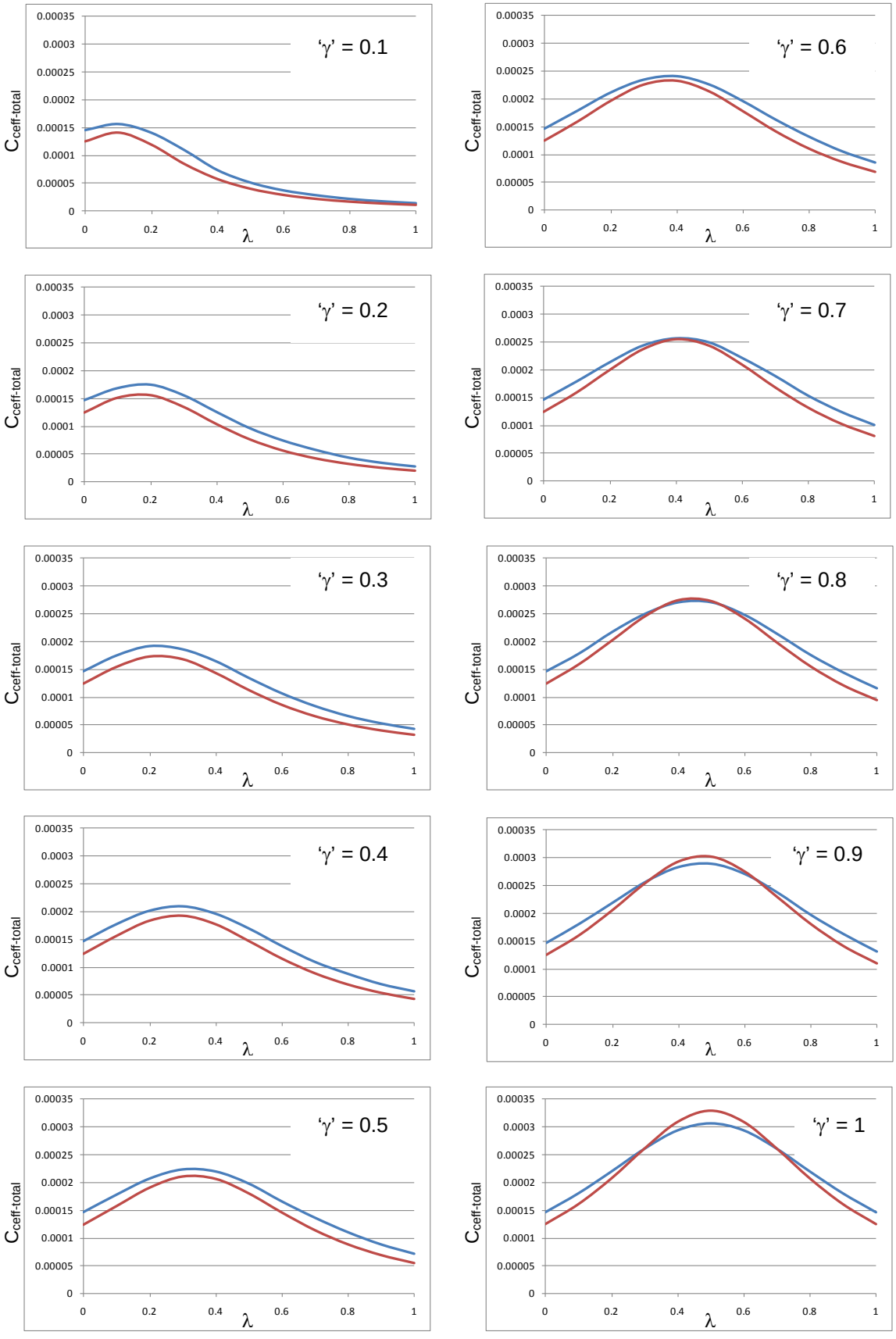


Fig. 3.14: Calculated and simulated $C_{ceff\text{-}total}$ at different values of 'γ' against duty cycles (λ) . ___ Simulation, ___ Calculation

3.6 Distortion Analysis

In this section the harmonics generated by the automatic compensator are investigated. One of the ways to measure the harmonic contents (voltage or current) is the Total Harmonic Distortion (THD). THD is the measure of how pure is the wave form. A zero THD means a pure sinusoidal waveform while a unity THD means that the total harmonics present in the system are equal to the fundamental component. THD can be expressed by the following equation:

$$THD = \frac{i_h}{i_1}$$

where: $i_h = \sum_{n=1}^{\infty} {i_n}^2$, and i_1 $is\ the\ 50Hz\ fundamental\ component$

As can be seen, it very difficult to calculate the harmonic terms up to ∞. Therefore, the THD is calculate by subtracting the fundamental component from the total current:

$$i_h = \sqrt[2]{i_t^2 - i_1^2}$$

So the THD can be expressed as:

$$THD = \frac{\sqrt[2]{i_t^2 - i_1^2}}{i_1}$$

The THD for all values of the capacitor ratios 'γ' and all values of the duty cycle 'λ' have been calculated using PSpice (for evaluating the fundamental and the total current harmonics). The spread sheet shown in Appendix E illustrates these values. It can be seen from these values that the maximum THD is: 0.282321425. The average THD in all cases is 0.119731625 (about 12%). Such THD may appear to be high; however considering that the THD in some non-linear loads (such as TV sets and computer power supplies) can easily exceeds 500% [15,18], the THD caused by the compensator could be acceptable.

3.7 Practical Results

In order to show that the automatic compensator is able to generate variable reactive currents at different duty cycles, the automatic compensator circuit was built and controlled using a microprocessor (details of the practical set up and control circuit are shown in Chapter 5). Figs. 3.15 and 3.16 illustrate the wave forms of the control switching pulses applied to S_1, the supply voltage and the compensator reactive current for two different cases. It is obvious that the compensator current is leading the supply voltage by 90°. Hence it shows the ability of the compensator to generate a variable reactive current at different duty cycles. Appendix F contains more practical results.

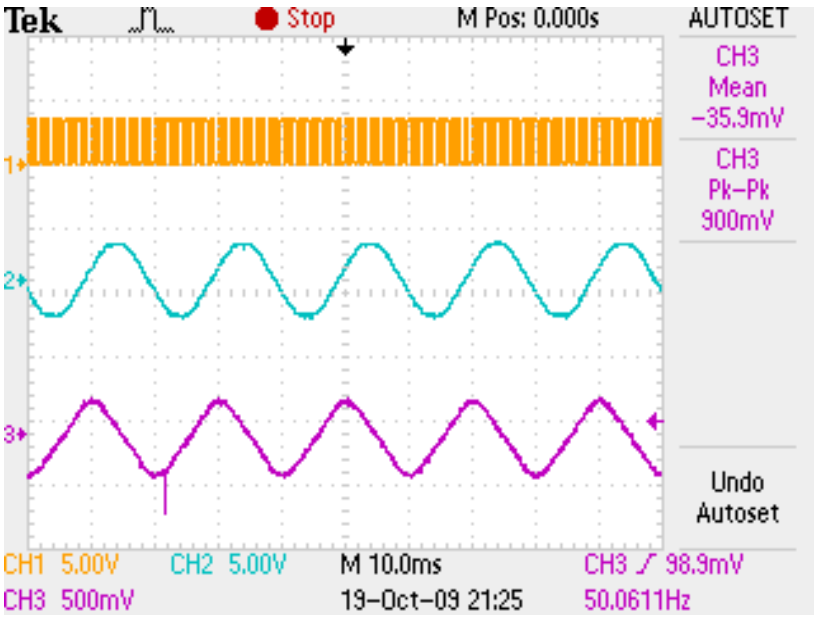


Fig. 3.15: Control pulses, supply voltage and reactive current waveforms (γ = 0.9, λ = 0.5)

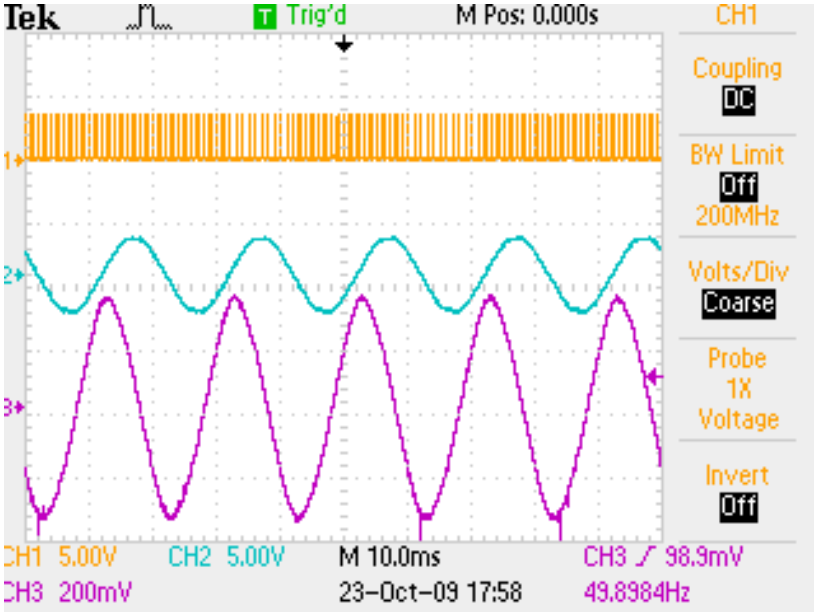


Fig. 3.16: Control pulses, supply voltage and reactive current waveforms ($\gamma = 1$, $\lambda = 0.2$)

3.8 Summary

In this chapter the proposed automatic compensator is introduced showing that the generated current leads the supply voltage by 90° and hence it is a reactive component. The effective value of the capacitance of the compensator $C_{ceff\text{-}total}$ is evaluated by calculation, simulation and a comparison between the two sets of curves is introduced. The practical results of the automatic compensator are also introduced showing the ability of the compensator to generate a variable amount of reactive current at different switching pattern. Such performance will require several banks of capacitors if ordinary fixed capacitors are used as a reactive power compensator.

In the following chapter the automatic compensator is applied in order to improve the power factor in both linear and non-linear loads.

Chapter 4

Implementation of the Automatic Compensator In Linear and Non-Linear Loads

4.1 Introduction

In the previous chapter the automatic compensator was analysed, simulated and practically tested to show how it can generates a variable reactive current which can be used to improve the power factor. In this chapter the automatic compensator is tested for improving the power factor in both linear and non-linear loads. Simulation and practical results are introduced to illustrate how the automatic compensator can improve the power factor in passive inductive loads as well as in a.c. voltage controllers (as an example of non-linear loads).

4.2 Power Factor in Linear Loads

Considering the simple R-L circuit shown in Fig. 4.1, where the power factor of the circuit can be easily calculated using the simple equation:

$$P.F. = \cos\left(\tan^{-1}\left(\frac{X_L}{R}\right)\right)$$

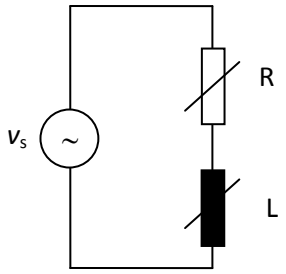


Fig. 4.1: Linear inductive circuit

The P.F. is calculated by fixing the value of L and varying R and also by fixing the value of R and varying L. The power factor is plotted in both cases as shown in Figs. 4.2 and 4.3. It can be seen from this figures that the PF is high at low value of (X_L/R) and it declines as the value of L is increased. The ratio of X_L/R in both figures was taken so that the PF angle varies from 'almost' zero to 38° [Appendix D].

PF

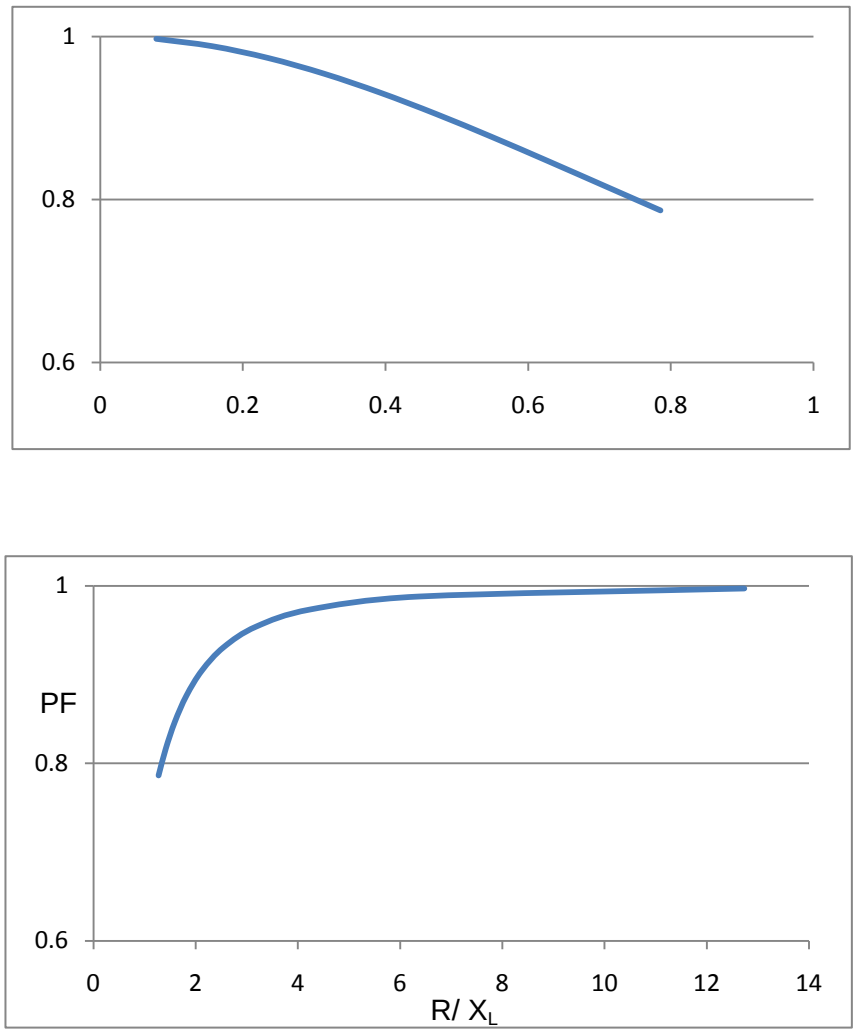


Fig. 4.3: PF as a function of R/ X_L

In order to improve the PF in such linear load a shunt capacitor is connected across R-L and the value of the capacitor is calculated (as was illustrated in the numerical example in section 2.3). Fig. 4.4 shows the calculated value of the capacitor for every combination of X_L/R in order to improve the PF to unity.

Fig. 4.5 shows the PSpice simulation for the RL circuit before and after the capacitor compensation.

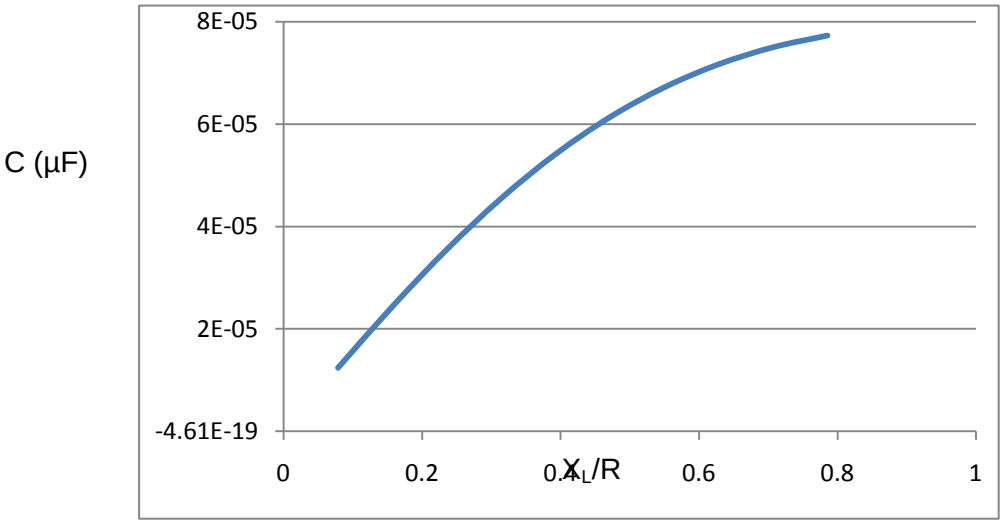


Fig. 4.4: Calculated shunt capacitance as a function of X_L/R for unity PF

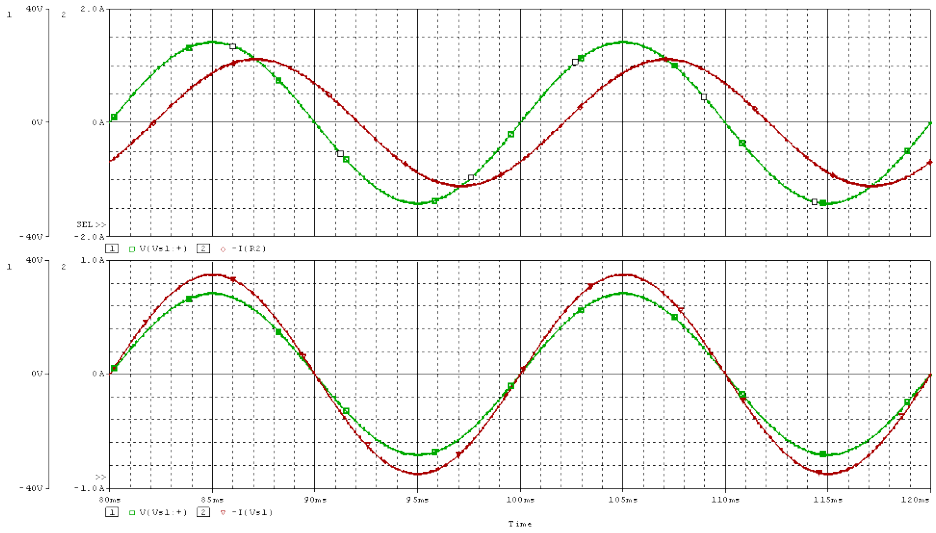


Fig. 4.5: PSPICE simulation for the RL circuit before (top graph) and after (bottom graph) the capacitor compensation ___ (supply voltage), ___ (supply current),

Obviously, it is not practical to keep changing the value of C for every RL combination. Therefore the automatic compensator circuit will now be tested for such linear load. However in order to do that, $C_{ceff\text{-}total}$ should be evaluated for every RL combination and then the duty cycle 'λ' is evaluated in order to generate this particular value of $C_{ceff\text{-}total}$.

4.3 Power Factor in Non-Linear Loads

Non–linear loads are very common nowadays. Computer power supplies, ac voltage controllers and adjustable speed drives are some examples of such non–linear loads. As was explained in Chapter 2, the PF in non-linear loads is made (at least mathematically) of two components: distortion factor and displacement factor. Distortion factor can be improved by using passive or/and active filters; this is outside the scope of this thesis. However, the displacement factor which is defined as 'cos' the angle between the fundamental components of the current and voltage waveforms can be improved through the use of fixed capacitor or, for flexibility, through the use of the proposed automatic compensator as will be discussed in the following section.

A typical non-linear load is an ac voltage controller like the one shown in Fig. 4.6. In this circuit the two thyristors (connected back-to-back) are triggered in order to control the power supplied to the load. The effect of the triggering pulses is that the voltage and hence the current waveforms are chopped in a way so that the desired power is delivered to the load [2, 8, 20]. Such chopped waveform causes not only distortion to the input current wave form but also causes the fundamental component of the current to be displaced away from the supply voltage waveform as shown in Fig. 4.7.

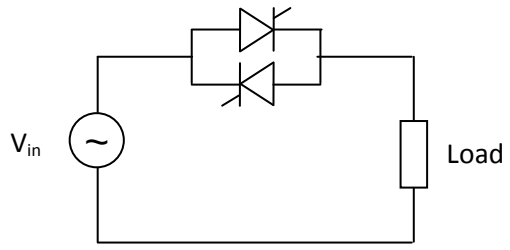


Fig. 4.6: AC voltage controller as an example of a typical non-linear load

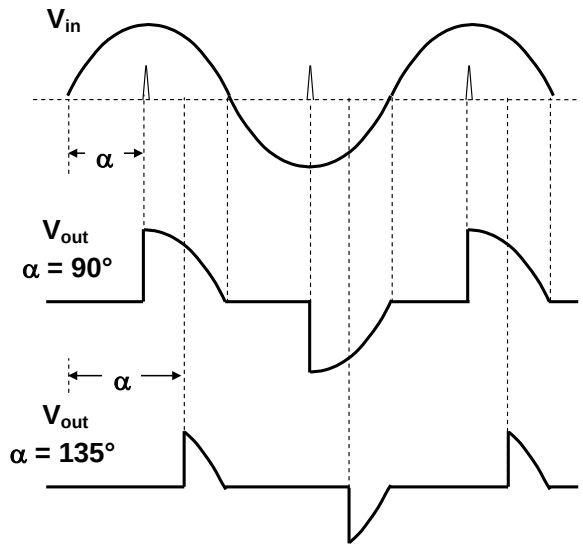


Fig. 4.7: Output voltage waveforms at different triggering angles

The distortion, displacement and power factors are now investigated in this non-linear circuit in order to calculate the optimum value of the power factor correction capacitor [7,13, 41].

The r.m.s. of the output voltage across the load can be expressed by the following equation:

$$V_{out\,(rms)} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\pi} V_{max}^2\, sin^2\,\theta d\theta} \qquad 4.1$$

$$V_{out\,(rms)} = \sqrt{\frac{V_{max}^2}{\pi}\int_{\alpha}^{\pi} \frac{1}{2}(1 - cos2\theta)\, d\theta} \qquad 4.2$$

$$V_{out\,(rms)} = \frac{V_{max}}{\sqrt{2}}\sqrt{\frac{1}{\pi}[\theta - \frac{sin\,2\theta}{2}]_{\alpha}^{\pi}} \qquad 4.3$$

$$V_{out\,(rms)} = \frac{V_{max}}{\sqrt{2}}\sqrt{\frac{1}{\pi}\left[\pi - \alpha + \frac{sin\,2\alpha}{2}\right]} \qquad 4.4$$

$$V_{out\,(rms)} = \frac{V_{max}}{\sqrt{2}}\sqrt{\frac{1}{\pi}\left[\pi - \alpha + \frac{sin\,2\alpha}{2}\right]} \qquad 4.5$$

$$V_{out\,(rms)} = V_{in\,(rms)}\sqrt{1 - \frac{\alpha}{\pi} + \frac{sin\,2\alpha}{2\pi}} \qquad 4.6$$

Since the load is assumed to be resistive, the RM. of the current waveform (the input and output current is the same in this circuit) can be expressed as:

$$I_{rms} = \frac{V_{out\ (rms)}}{R} \qquad 4.7$$

The load power (Real Power) can be expressed as:

$$P_{out} = I^2 R \quad \text{(W)} \qquad 4.8$$

And the Apparent Power is defined as the total RMS of the input voltage × the RMS current:

$$S = V_{in\ (rms)}\ \ I_{rms} \quad \text{(VA)} \qquad 4.9$$

$$\text{Power Factor (PF)} = \frac{P_{out}}{VA} \qquad 4.10$$

In order to evaluate the distortion and displacement factors, the harmonic analysis of the voltage and current waveforms are evaluated as follows:

The average thyristor current $I_{SCR(avg)} = \frac{1}{2\pi R}\sqrt{2}\int_{\alpha}^{\pi} V_{in(rms)}\sin\theta d\theta$

$$I_{SCR(avg)} = \frac{\sqrt{2}\,V_{in\,(rms)}}{2\pi R}(\cos\alpha + 1)$$

The rms value of the thyristor current :

$$I_{SCR(avg)} = \sqrt{\frac{1}{2\pi R^2}\int_{\alpha}^{\pi} V_{in}^2\ sin^2\,\theta d\theta} \qquad = \sqrt[2]{\frac{2V_{in}^2}{4\pi R^2}\int_{\alpha}^{\pi}(1 - cos2\theta)\,d\theta}$$

$$I_{SCR(rms)} = \frac{V_{in}}{\sqrt{2}R}\sqrt[2]{1 - \frac{\alpha}{\pi} + \frac{sin\,2\alpha}{2\pi}}$$

V_{out} (t) $= V_{dc} + \sum_{n=1,2,\ldots}^{\infty} a_n \cos\theta + \sum_{n=1,2,\ldots}^{\infty} b_n \sin\theta$

$V_{dc} = \frac{1}{2\pi}\int_{\alpha}^{2\pi} V_{max}\ \sin\theta \mathrm{d}\theta = 0$

$a_n = \frac{1}{2\pi}\left[\int_{\alpha}^{\pi}(V_{max}\ sin\theta)cosn\theta d\theta + \int_{\pi+\alpha}^{2\pi}(V_{max}\ sin\,\theta)cosn\theta d\theta\right]$

$a_n = 0\ \ (for\ n = 2,\ 4,\ 6$

$$a_1 = \frac{V_m}{2\pi}\ \ (cos2\alpha - 1) \qquad (for\quad n = 1) \qquad 4.11$$

$$a_n = \frac{V_m}{2\pi}\left[\frac{2}{1+n}\ (\cos(1+n)\,\alpha - 1) + \frac{2}{1-n}\ (\cos(1-n)\,\alpha - 1)\right]$$

$$(for\quad n = 3,\ 5,\ \ldots) \qquad 4.12$$

$$b_n = \frac{1}{2\pi}\left[\int_{\alpha}^{\pi}(V_{max}\ sin\theta)sinn\theta d\theta\ + \int_{\pi+\alpha}^{2\pi}(V_{max}\ sin\theta)sinn\theta d\theta\right]$$

$$b_n\ =\ 0\ (for\ n = 2, 4, 6, \dots)$$

$$b_1 = \frac{V_m}{2\pi}\ \ [\sin 2\alpha + 2\ (\pi - \alpha)] \quad (for\ n = 1) \qquad 4.13$$

$$b_n = \frac{V_m}{2\pi}\ \left[\frac{2}{1+n}\ (\sin((1+n)\alpha)) - \frac{2}{1-n}\ (\sin((1-n)\alpha))\right]$$

$$(\ for\ \ \ n = 3,\ 5,\ \dots) \qquad 4.14$$

The maximum and rms values of the voltage and current waveforms for individual harmonics can be expressed as:

$$V_{n(max)} = \sqrt{a_n^2 + b_n^2} \qquad 4.15$$

$$V_{n(rms)} = \frac{\sqrt{a_n^2 + b_n^2}}{\sqrt{2}} \qquad 4.16$$

$$I_{n(max)} = \frac{V_{n(max)}}{R} \qquad 4.17$$

$$I_{n(rms)} = \frac{V_{n(rms)}}{R} \qquad 4.18$$

The power factor of such non-linear load (as the one shown in Fig. 4.6) can be plotted against the triggering angle α using equations 4.6 to 4.10. As it is shown in Fig. 4.8, the power factor decreases as the triggering angle of the thyristor increases. Obviously such circuits are used to control the output voltage applied to a load and this is achieved through the variation of the triggering angle. This mean that the power factor is likely to be very poor in such applications.

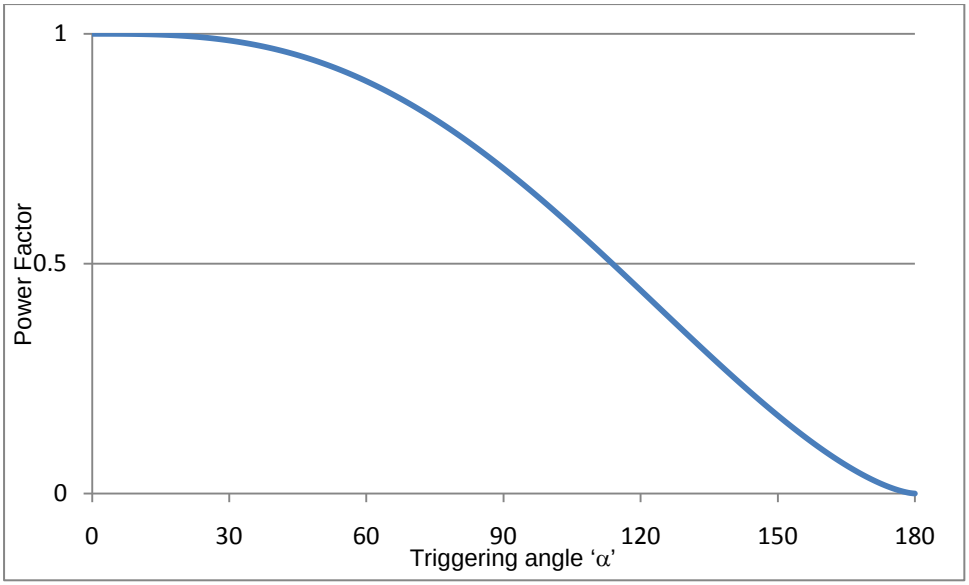


Fig. 4.8: Power factor at different triggering angles in ac voltage controller

The automatic power factor compensation can be used to improve the PF in such non-linear load. However, it is important to reemphasise the definition of the PF in non-linear loads as was explained in details in Chapter 2, equation 1.6. In that section the power factor in non-linear load was defined the as the product of the distortion factor and the displacement factor. The automatic PF compensation can improve the displacement factor which is '*cos'* the angle between the fundamental component of the voltage and current waveforms. This displacement factor is created because of the triggering effect of the thyristors [2, 6, 7, 20]. However the distortion part of the PF cannot be improved with the automatic compensation. This component can be improved through the use of passive or active filters, which is outside the scope of this thesis. Fig. 4.9 illustrates the improvement in the displacement factor after using the automatic PF compensator. The compensator generates a variable reactive current to match the displacement angle between the fundamental current and voltage components, i.e for each triggering angle the automatic compensator (through the control of the switching duty cycle) generates the appropriate reactive current.

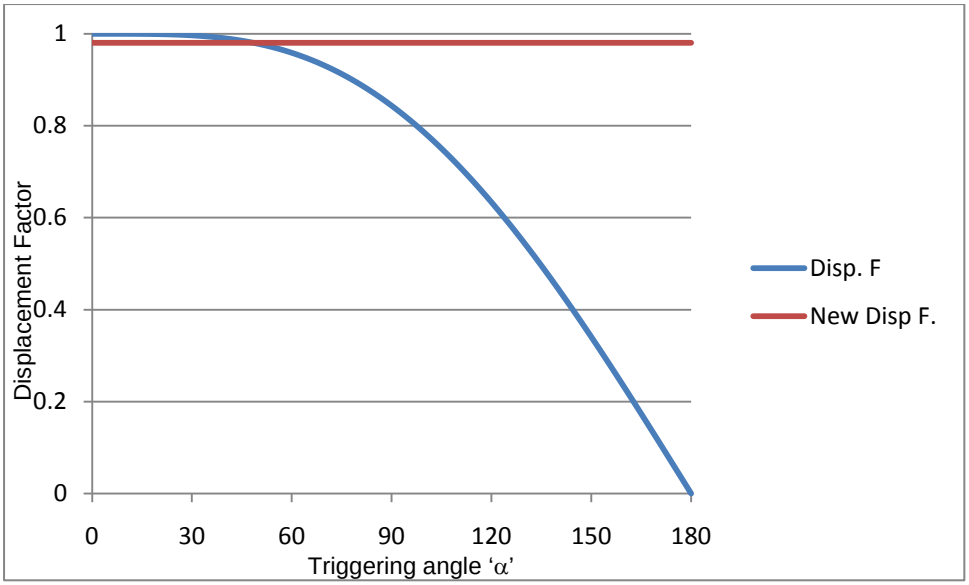


Fig. 4.9: Displacement factor before and after the use of the automatic PF compensation

The total PF after the improvement in the displacement factor is re- calculated using equations 4.6 to 4.10. The improvement in the PF is illustrated in Fig. 4.10.

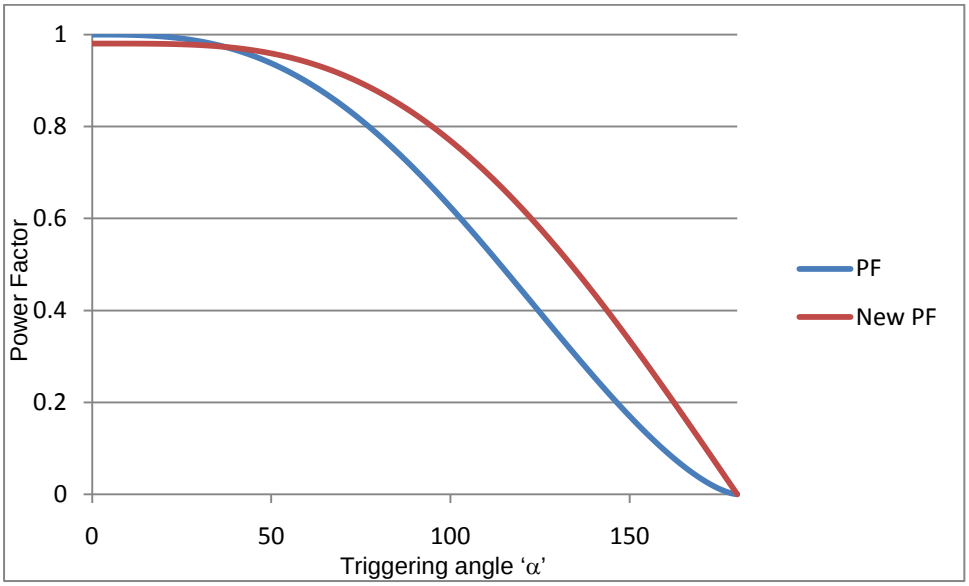


Fig. 4.10: Power Factor before and after the use of the automatic PF compensation

Obviously the PF can be improved further through the use of passive/active filters as mentioned before, but the main objective of this work is to focus on the displacement improvement.

For each triggering angle the value of the capacitor is worked to find out the optimum improvement in the displacement factor. The value of the compensated capacitor is worked as follow:

1) The Fourier coefficients of the fundamental current component (a_1 and b_1) are worked out from equations 4.11 and 4.13 for each triggering angle.

2) The phase angle of the fundamental component is worked out from the Fourier coefficients.

3) The value of the compensating capacitor current, i_c, is calculated based on the graph shown in Fig. 4.11

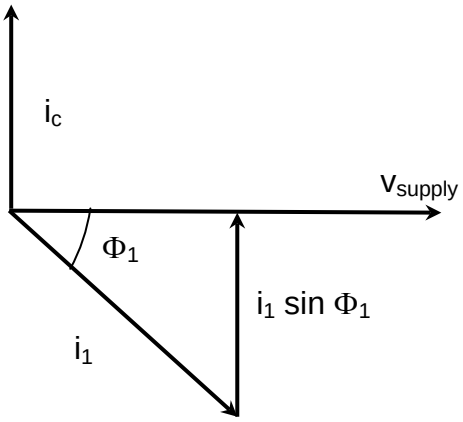


Fig. 4.11: Phasor diagram of the fundamental and compensated currents with respect to the supply voltage.

4) The value of 'C' is evaluated from the following equations

$X_c = v_{supply} / i_c$

$C = 1 / (2 \pi f X_c)$

The above steps is carried out for each triggering angle (steps of 1°) and the graph show in Fig. 4.12, illustrates the variation of the required compensated capacitor for each triggering angles [6]. It can be seen from this graph that the maximum capacitance required for the optimum compensation occurs at 90°. Such variable

capacitance is generated from the automatic compensator circuit as was described in Chapter 3.

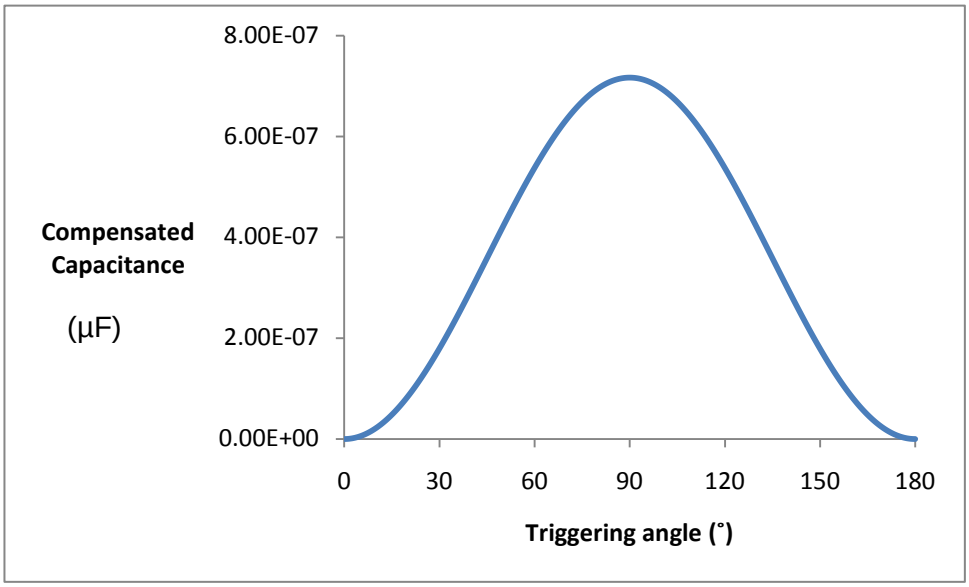


Fig. 4.12: Compensated capacitor values vs triggering angle in A.C voltage controller.

Figs. 4.13, 4.14, and 4.15 shows the improvement achieved in the power factor at three different angles (45°, 90°, and 135°) of the ac voltage controller. The value of the compensated capacitor is worked out for each of the three triggering angles and implemented in PSpice in order to see the improvement on the power factor. The figures show the transient and the steady state behaviour of the circuit, however the improvement should only be considered at the steady state; i.e. towards the end of the graph.

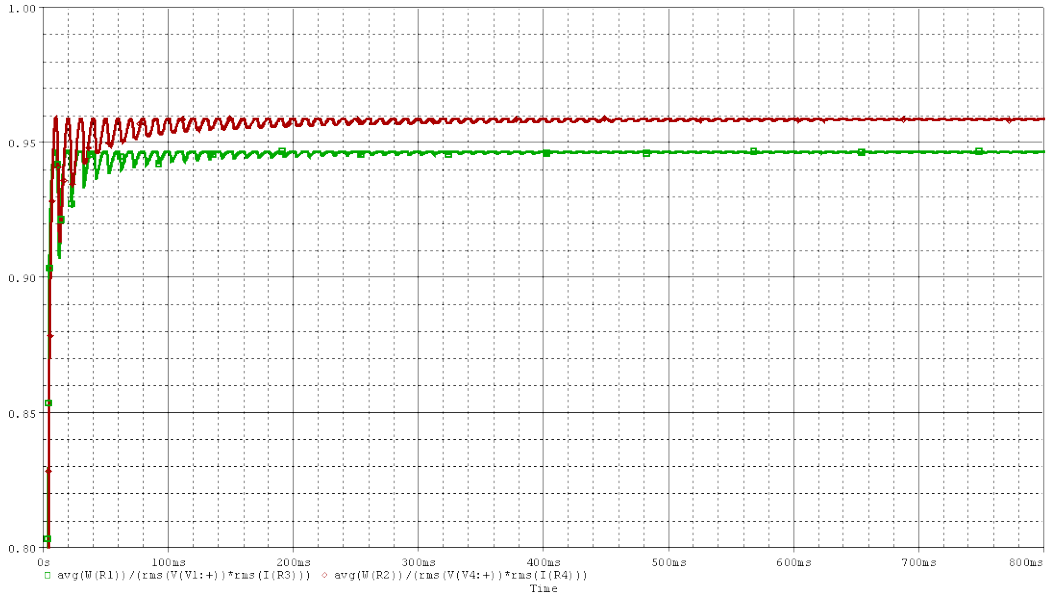


Fig. 4.13: Power Factor at α= 45°

___ Without correction capacitor

___ With correction capacitor (0.36μF)

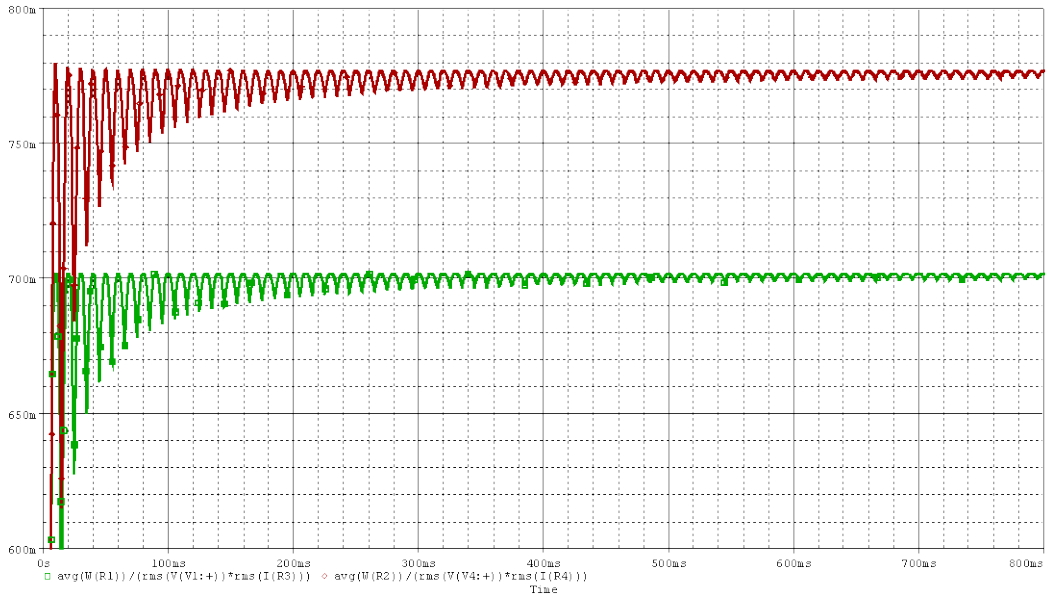


Fig. 4.14: Power Factor at α= 90°

___ Without correction capacitor

___ With correction capacitor (0.72μF)

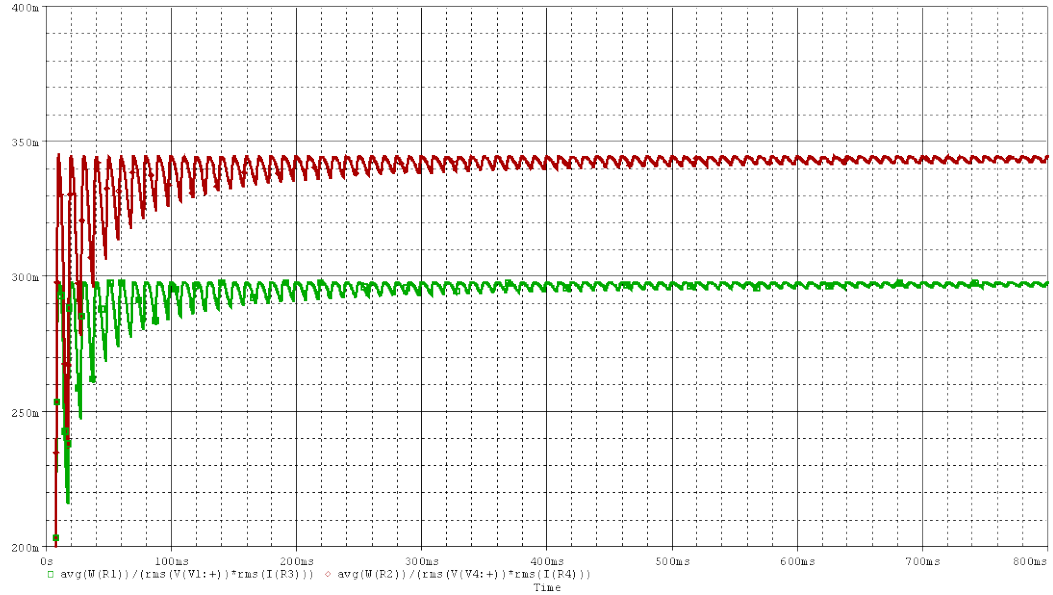


Fig. 4.15: Power Factor at α= 135°

Without correction capacitor

With correction capacitor (0.36μF)

The supply current before and after compensation for α=135° is shown in Fig. 4.16. It can be seen from this figure the effect of the capacitor in the waveshape of the input current waveform.

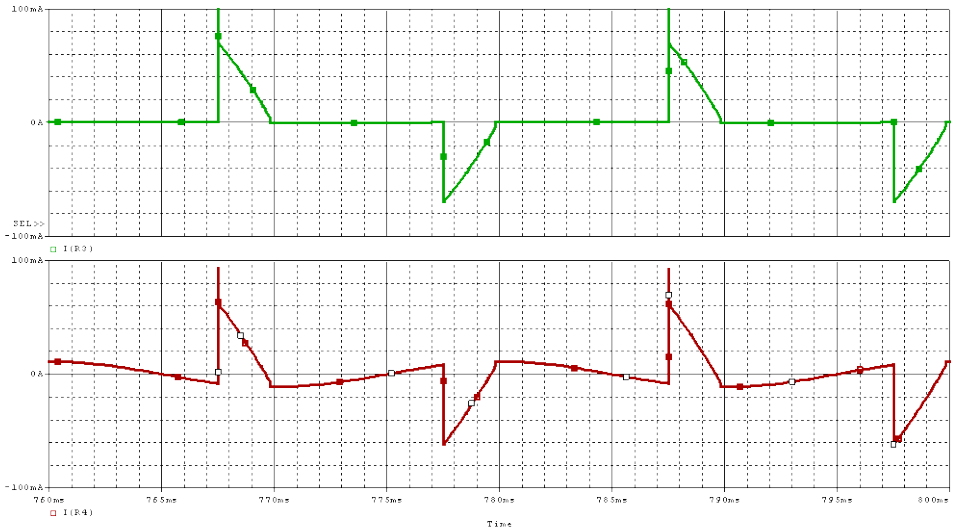


Fig. 4.16: Input current waveform α= 135°

Without correction capacitor

With correction capacitor (0.36μF)

4.4 Summary

In this chapter the power factor in linear and non-linear loads was investigated and the automatic power factor correction circuits was implemented in order to improve the power factor. In linear loads the automatic compensator circuit was successfully used in achieving a unity power factor, since there is no distortion factor component in linear loads. However, in non-linear loads although the displacement factor was improved to unity, but the total power factor was not improved to unity and that is due to the fact that the automatic compensator circuit only compensates the angle of the fundamental component. The control, driver and snubber circuits used are discussed in details in the next chapter.

Chapter 5

Control and Protection of the Proposed Compensator

5.1 Introduction

In chapter 3 and 4 the theory and implementation of the proposed compensator were introduced. Topics like the control strategy, drive circuits and devices protection were not covered in order to focus on the concept of the proposed compensator.

This chapter is mainly divided into two parts. The first one deals with use of microprocessor to control proposed compensator circuit, and experimental result involved in this work.

The second part deals with power losses in the proposed compensator circuit and the overall efficiency.

5.2 Control Circuit

The rapid growth in the microprocessor technology, lower prices and their flexibility make microprocessors ideal for many power electronic application circuits. In particular the flexibility required in controlling the power factor compensator can be achieved by storing the appropriate switching pattern in the microprocessor memory. A microprocessor in general is an integrated – circuit computer, a computer on a chip, and it represent an advanced kind of integrated circuit available. Microprocessors are essentially computer central processing units (CPUs), included an arithmetic unit, several registers, hardware stack implementation, on-chip memories (both RAM and ROM), and analogue input/output (I/O). Not all microprocessor include memory and I/O some have been optimised for computational speed and elegance, where others have been designed for simple applications where a minimum of ‘support chips’ is desirable.

Microprocessor can control the pattern required for the PF compensator by offering the suitable triggering pulses which depends on the frequency and the duty cycle (λ). This is achieved through a fast, accurate and above all a flexible programme [3, 21, 24].

5.3 Software Design

The triggering pulses depend on the switching angles and they are evaluated for each triggering angle and then stored in suitable addresses in the microprocessor EPROM. When the value of triggering angle is entered through the keyboard, the program searches for the corresponding switching angles and waits until the zero crossing pulse arrive through the interrupt (which indicates the beginning of the repetitive cycle of the program). The program is then executed and the required control pulses are transmitted to the drive circuits through the output port. The flowchart illustrated in Fig.5.1 shows the procedure used for generating the switching pulses.

The calculated switching angles are stored in the microprocessor memory and the pulses are then generated from the output port as two anti-phase signals. These two signals are practically the input signals to the driving circuits. Each switch has its own driving circuit, which is mainly to isolate the MOSFET sources from each others. The semiconductor switches used have a finite rising and falling times. If the two switches in the compensator circuit are overlapped, that will cause a circulating current between the two capacitors with nothing limiting this current except the internal resistance of the switches and capacitors. This can lead to a very high dv/dt across the switches and hence damaging them. If a dead-period is generated between the two switches in order to eliminate such problem, that will result on the inductor current being open circuit and that will equally damage on of the two switches due to a very high di/dt [20]. In order to avoid such high dv/dt or high di/dt a third branch consists of a semiconductor switch and a resistor is introduced in order to smooth the transfer between the two main switches. The pattern for the 3rd branch could be generated from the microprocessor however for more efficient and accurate control, the microprocessor is only used to generate the main switching pattern and a separate analog circuit is used to generate the related switching patterns as shown in Fig. 5.3.

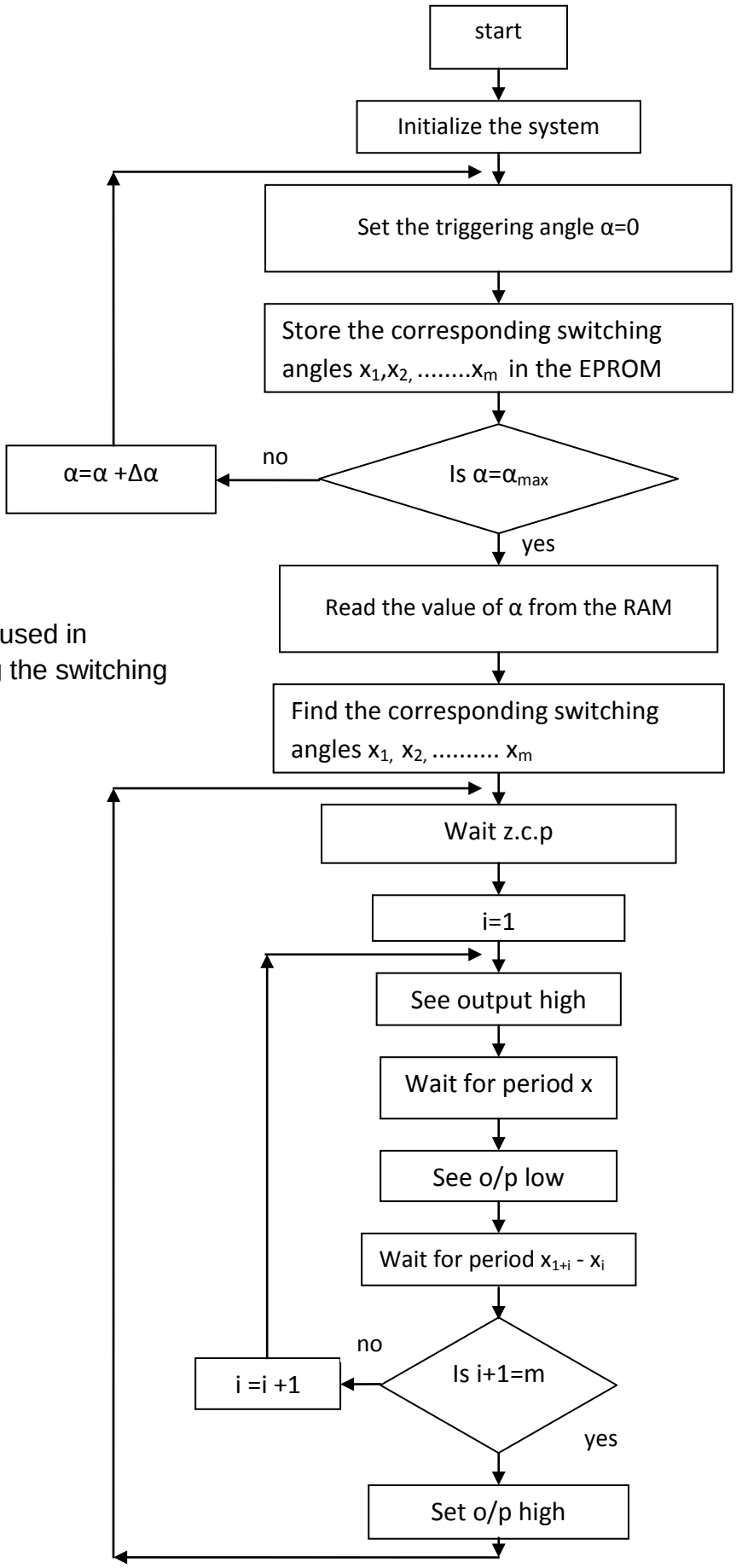


Fig. 5.1: Flowchart used in generating the switching pulses

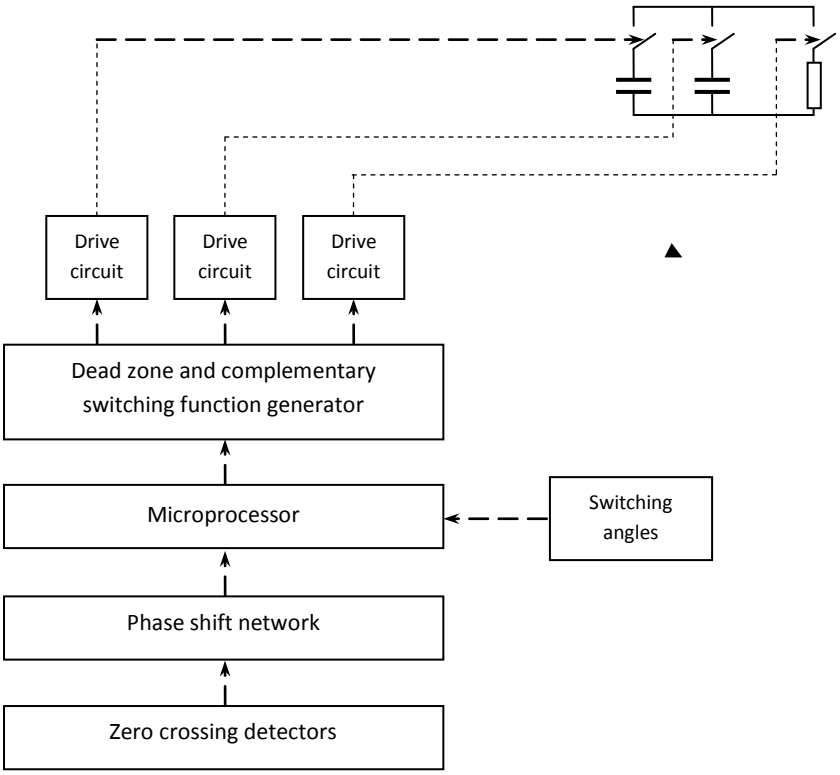


Fig. 5.2: Block diagram of the experimental setup

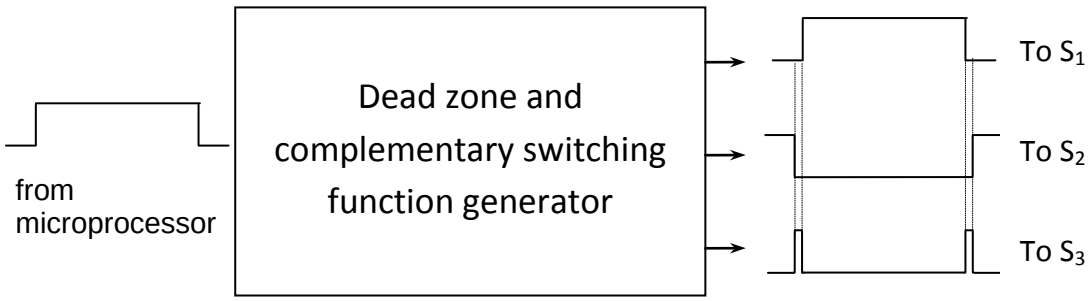


Fig. 5.3: Practical implementation of the dead zone and complementary switching function generator

5.4 Zero Crossing Detector

A zero crossing detector or a phase locked loop is essential to synchronize the generated switching pattern with the supply voltage. The control pulses can be shifted through the software program stored in the EPROM of the microprocessor. This is required in order to operate the circuit in a closed loop mode. As for open loop mode the phase angle of the switching pattern can be controlled through shifting the zero crossing pluses which controls the beginning of the program.

The switching pattern for each value of convertor triggering angle ‘α’ is evaluated and stored in the EPROM and the required switching pattern is set via the keyboard.

The microprocessor is capable of generating switching pulses for all three switches. The main pulses is generated to control s_1, complementary switching pulses is generated for s_2, and overlap pulses for s_3 on individual bases. However, it is more efficient if the microprocessor is used to generate switching pulses only for s_1 and a logic circuit convert these switching pulses to complementary and overlap pulses for s_2 and s_3 as shown in Fig. 5.3.

5.5 Drive Circuits

Although MOSFETs are voltage driven devices, and they can be easily controlled from the output of the microprocessor, however, it is recommended to use appropriate drive circuits for the following reasons:

- The MOSFET switches are in the power circuit and they handles high voltage (mains) and they also carry the main reactive current. This could be very risky situation as if something goes wrong with the MOSFETs that may affect the expensive microprocessor circuit which is mainly a low power low voltage circuit.
- Each MOSFET switch is controlled through applying pulses between the gate and the source of this MOSFET. If the pulses are coming straight from the microprocessor that means that they will all be sharing the same ground. This is not acceptable as each MOSFET should have its own ground connected to separate sources.

For the above two reasons a drive circuit is required to act as a buffer between the microprocessor and the MOSFETs and also to drive the MOSFETs into hard saturation so that the voltage across them is almost zero when they are fully on and the current is almost zero when they are fully off. There are so many drive circuits which can be used for such applications. The circuit shown in Fig. 5.4 is the one used in the practical setup. It consists of an opt-isolator chip (6N137) and driver chip (ICL7667). The reason for the opt-isolator is to isolate the microprocessor from the MOSFETs and also to create different grounds for each MOSFET.

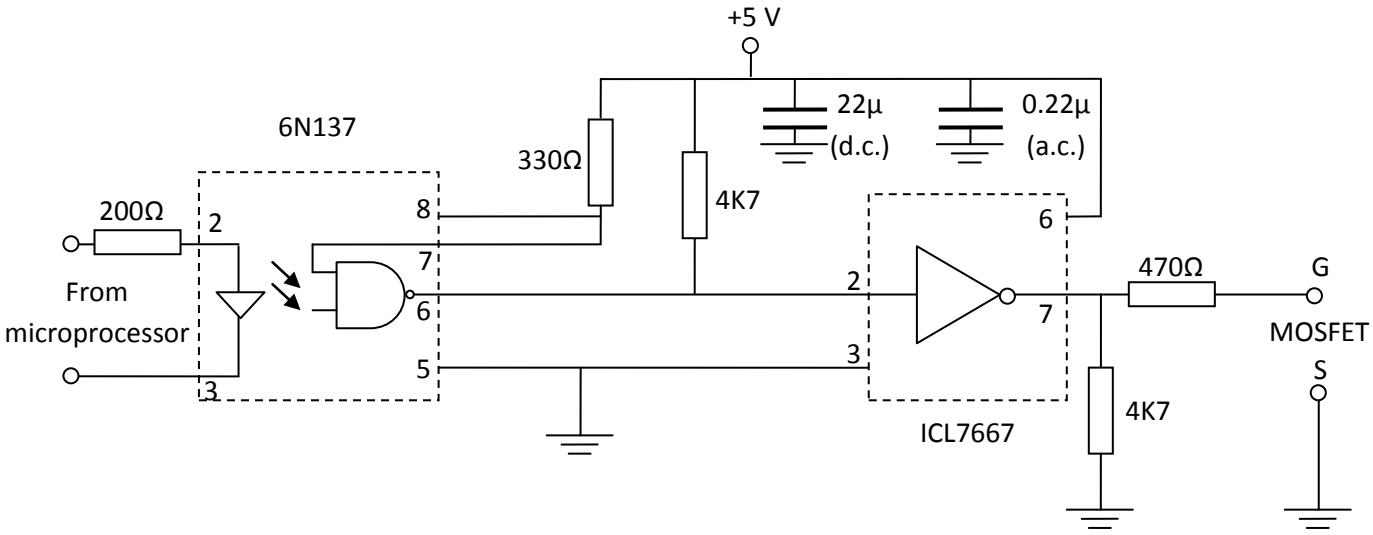


Fig. 5.4: Schematic Diagram of the MOSFET Driver Circuit

5.6 MOSFET Protection

MOSFETs used in the proposed circuit are subjected to high di/dt and high dv/dt. In order to remove or at least to reduce the stress from the MOSFETs, a snubber circuits are used to divert the power loss from the MOSFETs into an external resistor. Snubber are small network of parts in the power switching circuits whose function is to control the effects of reactances, enhance the performance of the switching circuits and resulting in higher reliability and efficiency. However, the main

intent of a snubber is to absorb energy from the reactive element in the circuit and to release stress from the semiconductor switch [2, 6, 20].

When a snubber is properly designed and implemented, the switch will have lower average power dissipative, lower operating voltage and current and this consider valuable technique to reduce the device's switching loss by modifying the switching waveform through adding passive component to the load circuit.

In order to understand the operation of the snubber circuit the voltage $v_s(t)$ and current $i_s(t)$ across and through the switch are plotted in function of time as shown in Fig. 5.5-a. They can also be plotted against each other as locus diagram as shown in Fig. 5.5-b. In common with the waveform from which it is derived, the shape of the locus depends on both the switching device and the load circuit. The switching-locus representation is useful because by using the same axes two other plots can be drawn. Since power is defined by 'p=vi ', every point on the v_s-i_s plane has a power associated with it. Curves joining points of equal power p_s may be ploted. The higher the power, the farther the curve lies from the origin. Zero power is dissipated at points lying on the axes $v_s=0$ and $i_s=0$. In order to minimise the switching loss, the switching locus should lie as close to the axes as possible. Moreover, as *t* change, the points tracing out the locus should pass as quickly as possible through the higher-power regions of the v_s-i_s plane.

Every semiconductor switching device has ratings which must not be exceeded-voltage, current, power, etc. The rating may be plotted on the v_s-i_s plane to enclose what is known as the 'the safe operating area' (SOA) of the device, as shown in Fig. 5.5-c. It is important that the switching locus lies within the SOA or the switching device will be overstressed and may fail.

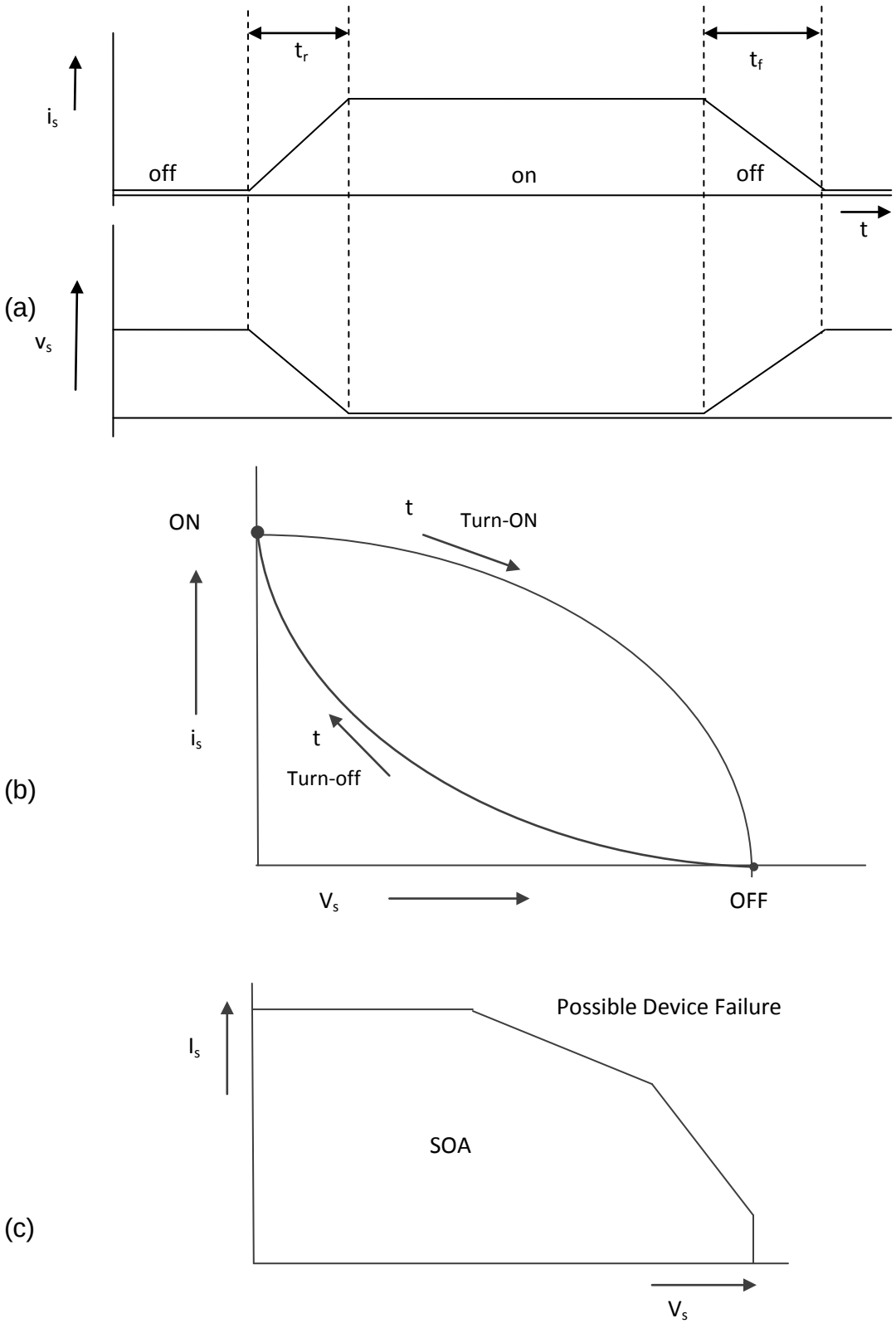


Fig. 5.5: (a) Switching waveform; (b) Switching locus; (c) Safe operating area (SOA).

5.6.1 Switching Resistive Load

With a purely resistive load fed from a voltage V, Fig.5.6 , the switch current and voltage are related by ohm's law. The switching locus is

$i_s(v_s) = (v_s)(i_s) / R$

Which is simply a straight line between the ON point (0, I), where I=V/R, and the OFF point (V,0). It is convenient to assume that the semiconductor switch causes it to change linearly during the switching interval t_r and t_f. The switching locus for a resistive load is then traversed at a constant speed.

By integrating $v_s(t) . i_s(t)$ over the interval t_r and t_f it can found that the energy dissipated during tune-on as 1/6 VIt_r and during turn-off as 1/6 VIt_f . Thus the total switching loss is

$P_s(sw) = VI (t_r+t_f) / 6T$

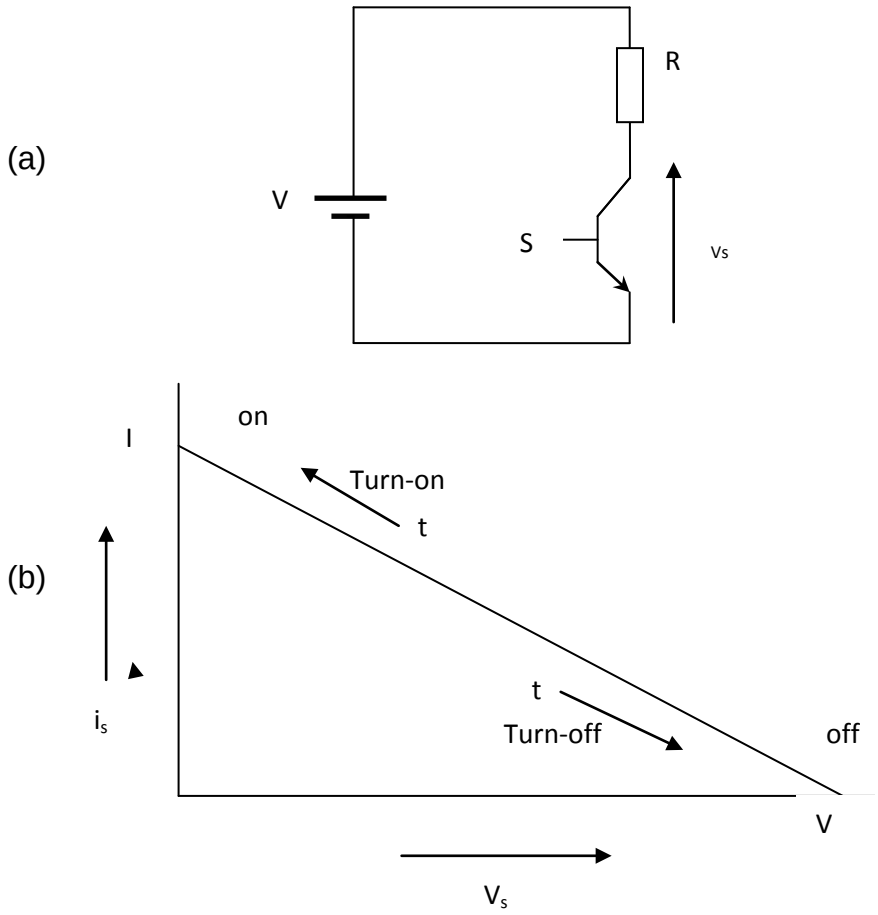


Fig. 5.6: Switching a resistive load. (a) circuit diagram; (b) Switching locus

5.6.2 Switching Inductive Load

The important case of a highly inductive load as shown in Fig. 5.7 The inductive is so large that it maintains virtually constant current 'I' throughout the switching cycle. Usually there will be a diode to provide a path for 'I' when the switch is open. The voltage across a diode must remain at zero as long as any current is flowing through it. So during t_r and t_f, the switch and the diode are each carrying part of the current 'I', with S having to support the whole of V. For this case the switching loss may be found as

$$P_s(sw) = VI (t_r + t_f) / 2T$$

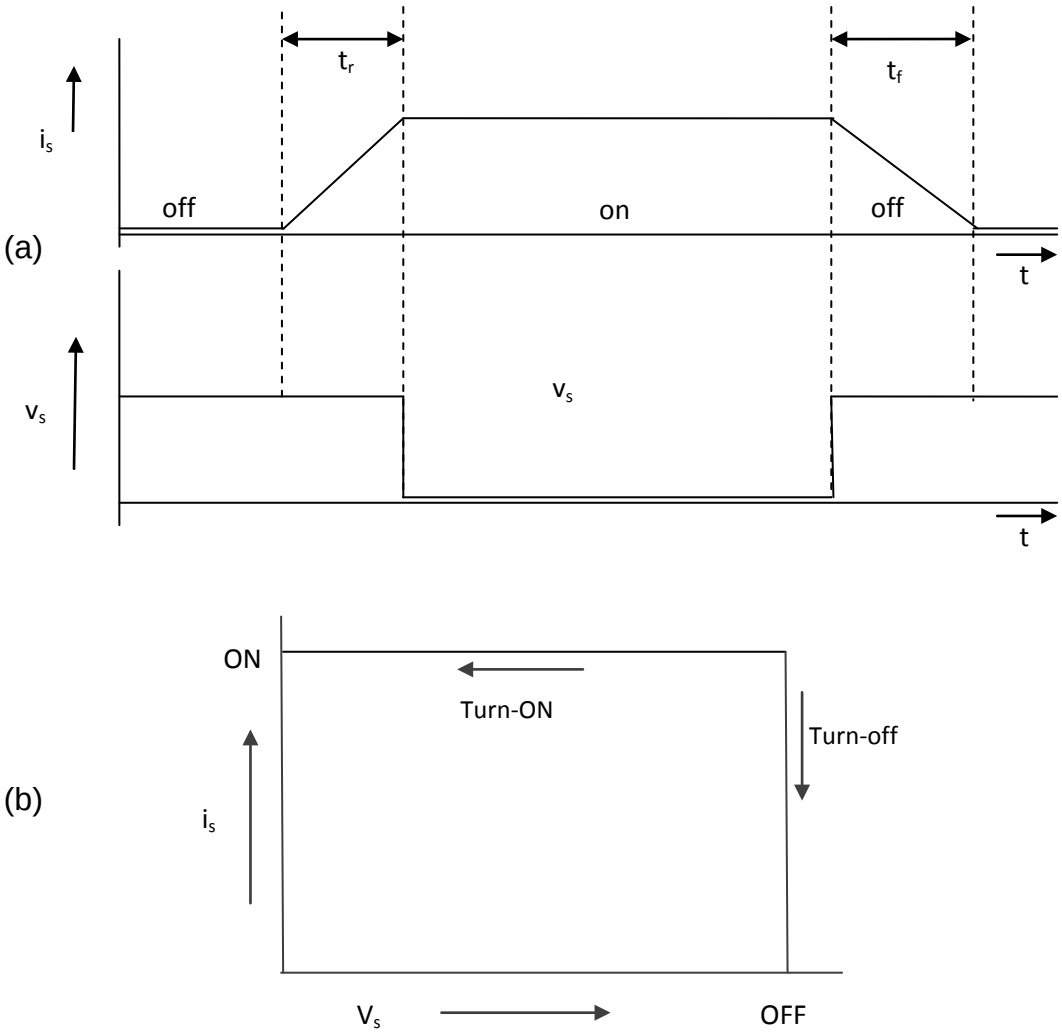


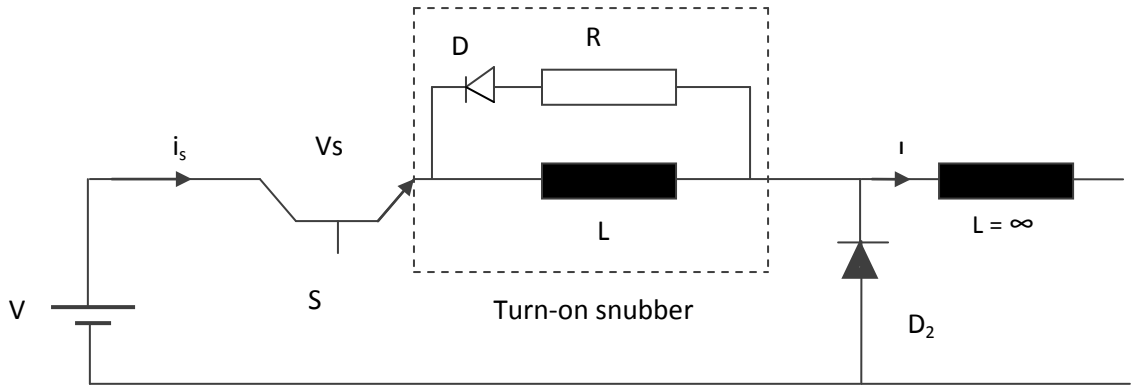
Fig. 5.7: Switching an inductive load. (a) Voltage and current waveforms; (b) Switching locus

5.6.3 Dissipative Snubber for Inductive Loads

The simplest form of snubber is dissipative. They contain resistors and therefore inefficient. Typically the snubber may dissipate power in the order of 5% of the converter's throughout. Often such inefficiency is tolerated because, in effect, heat is transferred from delicate switching devices to the rugged snubber resistors, improving the reliability and decreasing the cost of the circuit as a whole [6, 7].

5.6.4 Turn-on Snubber

The turn-on snubber of Fig. 5.8 Operates as follows. Initially no current flows in 'S' and the small snubber inductance L. As the current through 'S' rises during t_r a voltage $V_L=Ldi_s/dt$ is developed across 'L'. Assuming again that i_s increases linearly with t, $v_L=LI/tr$ can be found. If L is chosen so that v_L = v, there will be zero voltage developed across the switch 'S' during t_r, giving zero turn on loss in the switching device. The switching locus for this network is shown in Fig. 5.9.



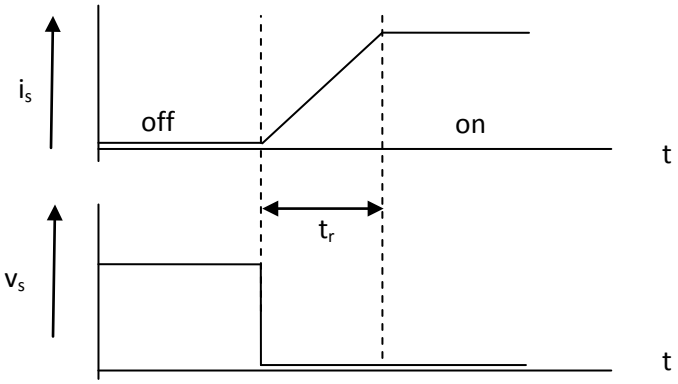


Fig. 5.8: Turn-on snubber network for an inductive load. (a) Circuit diagram; (b) Voltage and current waveforms

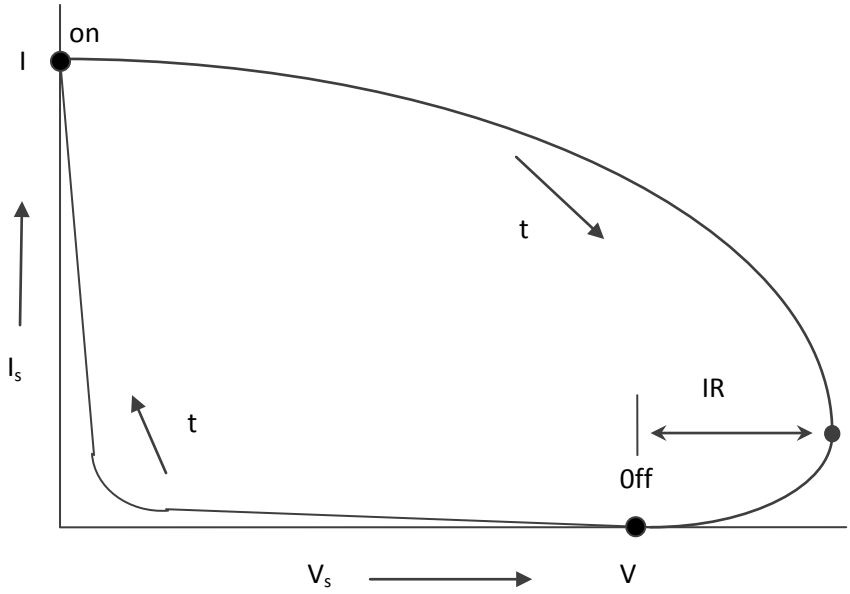


Fig. 5.9: The switching locus for turn-on snubber

Energy of 1/2 LI^2 is stored in L and must be removed (during t_{off}) so that the snubber is reset by the start of the next cycle. The simplest way to do this is to add a blocking diode D_1 and a resistor R, which dissipates the energy as heat. The current in L decays exponentially when the switch is open. The value of R is not critical, but two factors restrict it:

The time-constant L/ R must be short enough that the current can decay sufficiently during t_{off}. If 3 time-constants are allowed, the current will have decayed to I/20, and hence the stored energy will have decayed to a negligible 1/400 of its initial value.

Immediately after S has opened it sees a voltage V + IR across it, greater than the unsnubbed voltage, V. The voltage rating of 'S' must therefore be increased relative to the unsnubbed case.

The power dissipated in S during t_r is ideally $P_s(r) = 0$. The power dissipated in R is simply the stored energy multiplied by the switching frequency 1/T, i.e.

$$P_{s(r)} + P_R = P_{out} = VIt_r / 2T \qquad 5.1$$

Note that this is independent of the value of R.

If L is smaller than its optimum value some power will be dissipated in S but correspondingly less will be dissipated in R. The total loss $P_s(r)$ +PR remains the same. On the other hand if L is larger than its optimum value, the power dissipated in S stays at zero while the dissipation in R increases. These relationships are shown

in Fig. 5.10, where P_0 is the unsnubbed turn-on loss. The optimum value $L_{opt}= Vt_r / I$ ensures that all of the turn-on loss is transferred from the switching device to the snubber resistor, with no extra loss incurred. For $L \leq L_{opt}$,

$P_S + P_R = P_o = VIt_r / 2T$

This circuit is often known as an *RLD* snubber, after the components used.

5.6.5 Turn-off Snubber

The turn-off snubber of Fig. 5.10 operates as follows. Initially current *'I'* is flowing in *S* and the small snubber capacitance *C* is uncharged. As the current through *S* decreases, *C* and D_1, provides an alternative path for balance of *I*, and D_2 remains reverse-biased. Assuming that I_S falls linearly during T_f we have $i_{s(t)}=I(1-t/t_f)$, where the time origin has been taken at the start of turn-off. The current flowing into C therefore increases linearly according to $i_c=I\ t/t_f$. Putting this into the capacitance equation "i=Cdv/dt"and integrating , the capacitor voltage waveforms can be expressed as:

$$V_c(t)=\frac{1}{C}\int_0^t I\frac{t}{t_f}\,dt+V_c(0) = I\frac{t^2}{2Ct_f} \qquad 5.2$$

Thus V_C**,** and hence V_S rises parabolically from V_C (0) = 0 to $v_c(t_f) = It_f / 2C$ the end of turn-off. (Assumed that C is large enough that $v_C(t_f) < V$; if not, the above analysis must be modified.) The energy dissipated in S during turn-off can be found by integrating $P_s(t) = v_s(t) . i_s(t)$ over the interval t_f. Since D_1 is conducting, $v_S = v_c$ and we have

$$W=\int_0^{t_r} I\frac{t_r^2}{2Ct_f} . I\{1-\frac{t}{t_f}\}\,dt = \frac{I^2}{24C}t_f^2 \qquad 5.3$$

Subsequently C is charged at the full choke current I until V_C reach V, at which point D_2 becomes forward-biased and conducts the whole of I.

Energy of ½ CV^2 is stored in C and must be removed (during t_{on}). The simplest way to do this is to add D_1 and R to the snubber. The voltage across C decays exponentially when the switch is closed. The value of R is not critical but two factors restrict it:

- The time-constant CR must be short enough that V_C can decay to a negligible value during T_{on}. Once again 3 time-constants will be sufficient.
- Immediately after the switch closes, it passes a current of I + V/R, greater than the unsnubbed current, I. The current rating of S must therefore be increased relative to the unsnubbed case.

The turn-off loss in S is found by multiplying W of eq. ... by the switching frequency:

$$P_{S(f)} = \frac{I^2}{24C} t_f^2 \qquad 5.4$$

The power dissipated in R is the stored energy multiplied by the switching frequency, and again, this is independent of R:

$$P_R = CV^2/2T \qquad 5.5$$

If a full analysis of the turn-off snubber is carried out, it will be found that the total turn-off loss $Ps_{(f)} + P_R$ follows a curve as shown in Fig. 5.11. Here $P_0 = VIt_f/2T$, the unsnubbed turn-off loss. The choice of an optimum snubber capacitance C_{opt} is not as obvious the choice of L_{opt} was, but two possibilities are:

- Choose C_{opt} to minimise the total turn-off loss: $C_{opt\,(1)} = 0.22\, I\, t_f/V$. Then P $P_{s(f)}=0.33P_0$ and $P_R=0.22P_0$ (With this rather small value of capacitance, V_C, rises to V at $0.67t_f$ and stays there during the remainder of the turn-off interval; the analysis above is invalid since it was assumed that $V_C\,(t_f) < V$).
- Choose C_{opt} to minimise the loss in S without increasing the total loss above P_0 :$C_{opt(2)}$ $=0.91I/_{tf}$ *Then* $P_{s(f)} =0.09P_0$ and $P_R=0.91P_0$. With this choice V_C rises to =0.55V at t_f .

This circuit is often known as RCD snubber, and is frequently met within power electronic switching circuits.

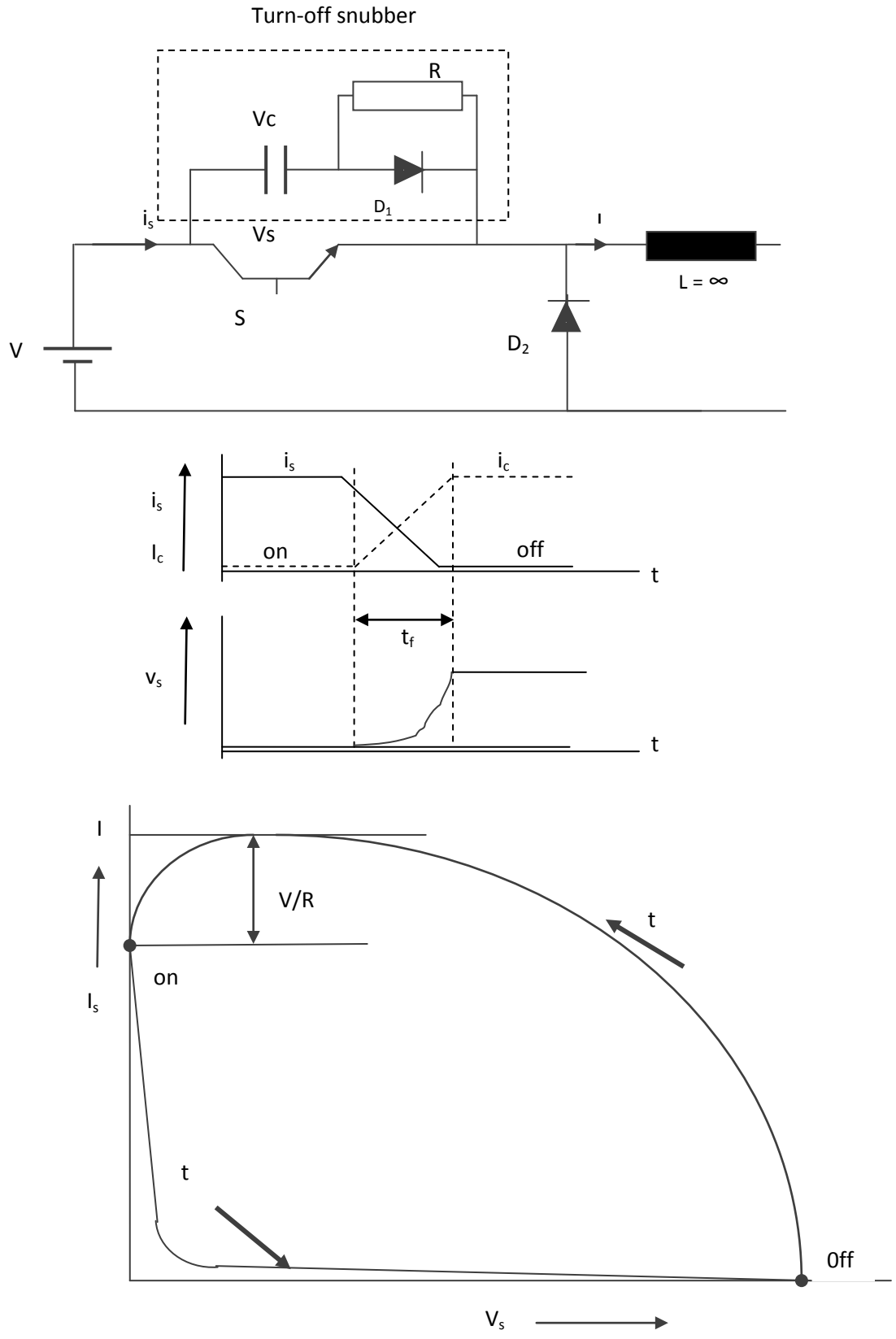


Fig. 5.10: Turn-off snubber network for an inductive load

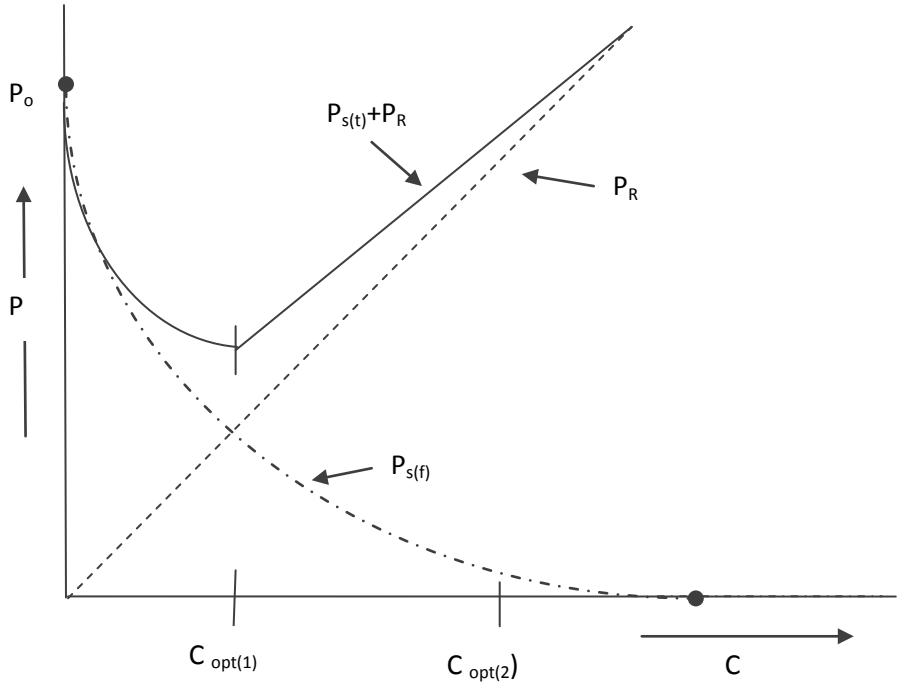


Fig. 5.11: Turn-off switching losses as a function of the snubber capacitance.

5.6.6 Turn-off / Turn-on Snubber

To snub both turn-on and turn-off, both of the above circuits can be incorporated or the combined snubber can be used. The values of C and L are determined as before. R must now be able to dissipate the sum of the turn-on PR and the turn-off PR. The value of R must be chosen with care as it forms part of both the turn-on and turn-off snubbers.

In practice, snubber design is an exercise in compromise.

The values of L and C may be chosen either on loss considerations as above, or to shape the switching locus to keep it within the SOA of the switching device. In the latter case the values of L and C might tend to be larger than the ‘’optimum’’ values indicated above.

In most applications the load current I is usually not fixed but can vary over a wide range. The supply voltage V can also vary. Since both V an I appear in the formulae for L and C, the ‘’optimum’’ snubber components depend on the circuit conditions. In

practice the snubbers are often designed for nominal operating conditions (e.g., full rated output) then adjusted empirically to obtain satisfactory performance over the whole operating range.

When designing the turn-on snubber for an inductive load, charge storage in the freewheel diode should be taken into account. An important effect of the snubber inductance is to limit the reverse recovery current of the diode.

In a transformer-coupled converter it may be necessary to have snubber components on the primary side (associated with the switch) and an RC damping network on the secondary side (associated with the rectifiers). The two networks will interact their values may have to be adjusted empirically. There may be no need for a turn-on snubber though, because the transformer will often possess enough leakage inductance to have some snubbing effect.

There is a good proportion of art as well as some science in the design of snubber networks!

5.7 Summary

In this chapter, the control of the compensator is discussed. The use of the microprocessor to produce the switching patter for controlling the MOSFET switches is discussed. The microprocessor was mainly set to generate the main control pulses and then a hardware circuit was used to generate the required overlapping pulses.

In order to operate the MOSFETs safely and efficiently, drive circuits have been designed and used as a buffer between the microprocessor and the MOSFET switches. A separate driver circuit was used for each MOSFET in order to ensure a complete isolation between the switches.

The control signals have to be synchronised with the mains in order to make sure that the compensator is generating the correct reactive current at the correct instant. This is achieved through the use of a zero crossing detector.

Finally in order to protect the MOSFET switches and in order to remove the stress caused to the switch during the turning on and turning off, a snubber circuits were designed to divert the losses from the MOSFETs to an external resistor. The design

and analysis of the turn-on and turn-off snubber circuits are covered in details in this chapter.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The main aim of this thesis is to develop an automatic power factor compensation which can be used in any types of linear and non-linear loads. Such compensator is needed especially with large number of low power non-linear loads. The proposed compensator can be used in shunt in conjunction with all types of loads. In principle there is no power limit for the proposed compensator, and the same idea can be applied for any power range. However, the compensator uses relatively fast semiconductor switches (MOSFETs) and the voltage and current ratings for such devices is still limited to low power applications. Gate Turn Off Thyristors (GTOs) can be used for high power applications and such devices will be used in the same configuration exactly the same way as the MOSFETs that are used in the proposed compensator [2,8,14,].

The compensator circuits are analysed, simulated and practically constructed, controlled and tested. The compensator generates the required reactive power which is needed to improve the power factor for any type of loads. The simulation package used to simulate the proposed compensator is PSpice. The reason of using this software is that it simulates at 'low level', i.e. as close to the practical setting as possible. For example, when MOSFET is used in the simulation, the characteristics of the simulated MOSFET are almost identical to the characteristics of the actual one.

The main advantage of the compensator is its ability to generate a smooth leading as well as lagging reactive power using only two capacitors and two switches. This is achieved through controlling the duty cycle of the semiconductor switches [6, 16,17]. The duty cycle is controlled via an 8085 microprocessor which gives flexibility as well as the speed of control. The implementation of the proposed circuit has to be considered carefully, for example issues like driving and protecting the MOSFETs has to be fully investigated before the practical work. The investigation, design, and implementation of such circuits are fully covered in the thesis.

6.2 Future Work

In fact the research work which was introduced in this thesis has in turn created more future research work compared to the original one which was intended to cover. However this is the nature of research. The following future research points which spun from this work and needs to be investigated further could be summarised in the following points:

- The compensator should be tested on high power loads, that could means the use of high power devices such as forced commutated thyristors of Gate Turn-Off Thyristors (GTOs). Obviously the design of the protection circuit has to be worked out as the dv/dt and di/dt will be much higher in this case. Also issue like Electromagnetic Compatibility (EMC) has to be fully investigated.

- Although the resonance phenomena has been briefly investigated when the compensator was designed, a more in-depth investigation is required particularly if the compensated capacitor (effective value) resonates with the supply impedance at the switching frequency.

- The proposed compensator focused mainly for improving the displacement component of the power factor. The distortion component was outside the scope of this research work. Future work could develop the compensator so that it contains an element of active filter which can be used to compensate for both the displacement as well as the distortion components of the power factor.

- So far the controller used was an external controller. The use of a single chip controller could be investigated further in such application. In that case the controller could be integrated within the compensator and the whole circuit would be wholly compatible.

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APPENDIX A

Saving due to PF Improvement in small industrial customer [1]

The table below shows typical monthly billing information which is used to calculate the penalty imposed by the utility and the cost analysis of improving the site power factor to 0.95.

Table A.1

Month	Power Factor	Actual KW Demand	KVAR Required	KW Billing Demand		Demand Charge		Demand Saving ($)
				Before Correction	After Correction	Before Correction($)	After Correction($)	
Jan	0.74	228	132	293	228	1244	969	275
Feb	0.7	241	167	327	241	1390	1024	366
Mar	0.72	233	148	307	233	1307	990	316
Apr	0.71	256	170	343	265	1466	1088	368
May	0.7	219	151	297	219	1263	931	332
Jun	0.69	274	197	377	274	1603	1165	439
July	0.68	281	211	393	281	1668	1194	474
Aug	0.67	261	203	370	261	1573	1109	464
Sep	0.72	238	151	314	238	1335	1012	323
Oct	0.74	232	136	298	232	1266	986	280
Nov	0.72	245	156	323	245	1374	1041	333
Dec	0.71	247	164	330	247	1405	1050	355
Total		16,883		12,559				

APPENDIX B

Result of Calculations of C_{eff} against λ

CALCULATION

Depending on the following equation which expresses the relationship between capacitor value (C_{eff}) and C1 & C2 and lambda (λ).

$C_{eff}=C1/\{(\lambda*\lambda)+(x*x)k\}$

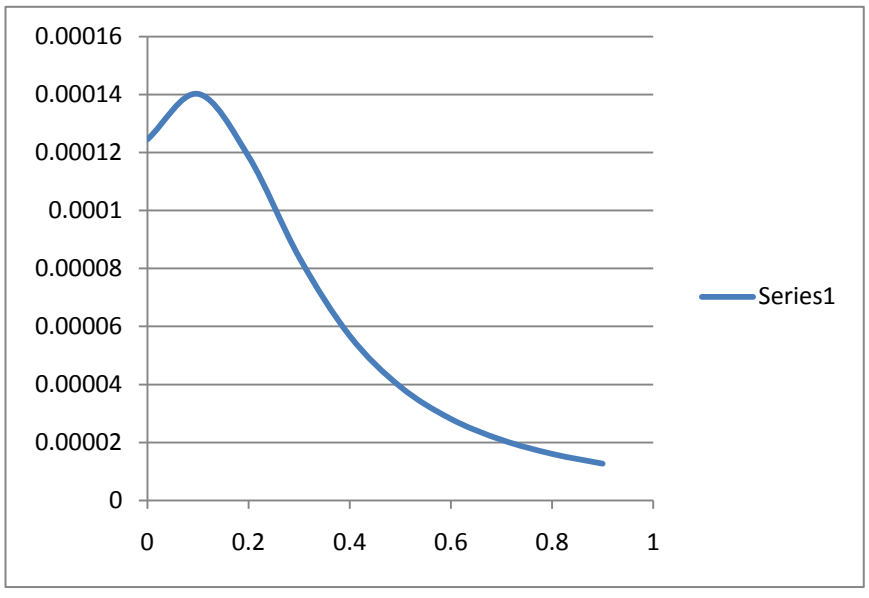
, where $x=1-\lambda$ and $k=C1/C2$

By using the Excel program, we can calculate the values of the effective capacitor. As it is clear from table below, we also, could find the capacitive impedance and to get more accurate values, we included the values of series circuit (R-L) in our calculation, like inductive impedance (Xl) and the resistance(R) and in our case we consider:

L=5mh, R=1Ω , then C1 has been increased by 10uf up to 100uf as shown at following tables:

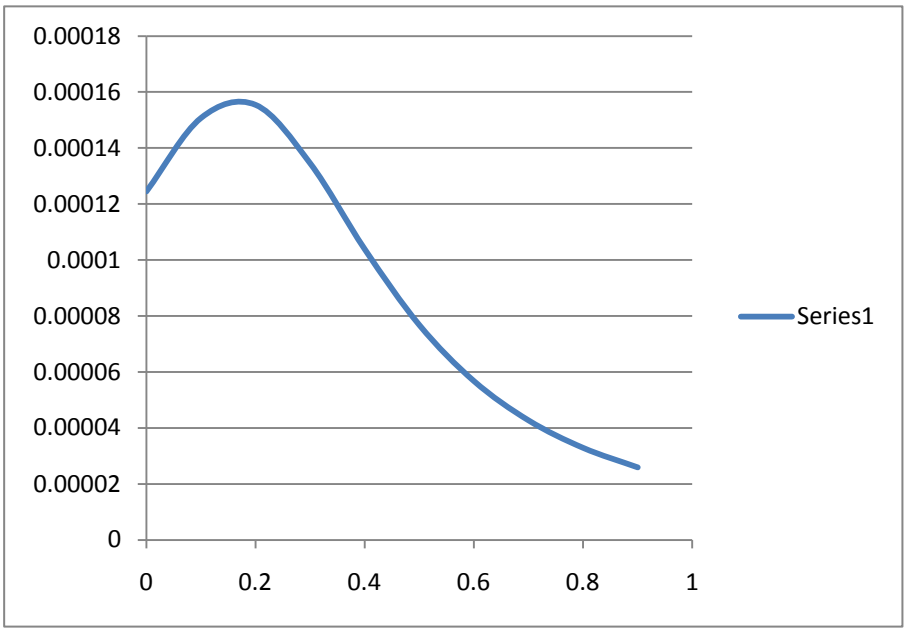
calculation at C1=10uf

Lambda(λ)	C1	λ*λ	x=1-λ	x*x	(x*x)*0.1	(λ*λ)+(x*x)*0.1	C	Xc	Xl	Xeff	Ceff
0	0.00001	0	1	1	0.1	0.1	0.0001	31.83102	6.28318	25.5674	0.000124
0.1	0.00001	0.01	0.9	0.81	0.081	0.091	0.00011	28.96622	6.28318	22.70508	0.00014
0.2	0.00001	0.04	0.8	0.64	0.064	0.104	9.62E-05	33.10426	6.28318	26.83971	0.000119
0.3	0.00001	0.09	0.7	0.49	0.049	0.139	7.19E-05	44.24511	6.28318	37.9751	8.38E-05
0.4	0.00001	0.16	0.6	0.36	0.036	0.196	5.1E-05	62.38879	6.28318	56.11452	5.67E-05
0.5	0.00001	0.25	0.5	0.25	0.025	0.275	3.64E-05	87.53529	6.28318	81.25827	3.92E-05
0.6	0.00001	0.36	0.4	0.16	0.016	0.376	2.66E-05	119.6846	6.28318	113.4058	2.81E-05
0.7	0.00001	0.49	0.3	0.09	0.009	0.499	2E-05	158.8368	6.28318	152.5569	2.09E-05
0.8	0.00001	0.64	0.2	0.04	0.004	0.644	1.55E-05	204.9917	6.28318	198.7111	1.6E-05
0.9	0.00001	0.81	0.1	0.01	0.001	0.811	1.23E-05	258.1495	6.28318	251.8683	1.26E-05



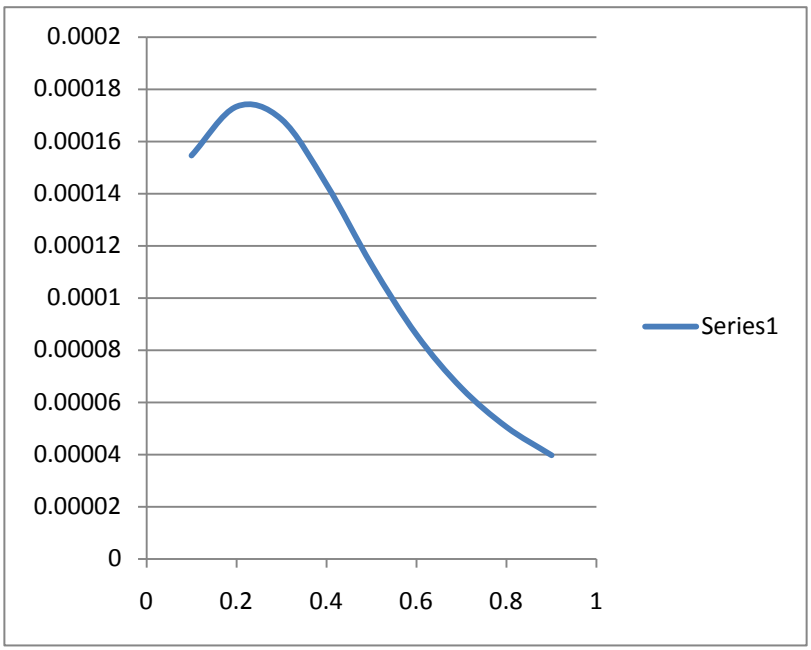
calculation at C1=20uf

lambda	C1	y*y	x=1-y	x*x	(x*x)*0.1	(y*y)+(x*x)*0.1	C	Xc	Xl	Xeff	Ceff
0	0.00002	0	1	1	0.2	0.2	0.0001	31.83102	6.28318	25.5674	0.000124499
0.1	0.00002	0.01	0.9	0.81	0.162	0.172	0.000116	27.37467	6.28318	21.11519	0.00015075
0.2	0.00002	0.04	0.8	0.64	0.128	0.168	0.000119	26.73805	6.28318	20.4793	0.000155431
0.3	0.00002	0.09	0.7	0.49	0.098	0.188	0.000106	29.92115	6.28318	23.65912	0.000134541
0.4	0.00002	0.16	0.6	0.36	0.072	0.232	8.62E-05	36.92398	6.28318	30.65711	0.000103829
0.5	0.00002	0.25	0.5	0.25	0.05	0.3	6.67E-05	47.74652	6.28318	41.4754	7.6747E-05
0.6	0.00002	0.36	0.4	0.16	0.032	0.392	5.1E-05	62.38879	6.28318	56.11452	5.67253E-05
0.7	0.00002	0.49	0.3	0.09	0.018	0.508	3.94E-05	80.85078	6.28318	74.5743	4.26838E-05
0.8	0.00002	0.64	0.2	0.04	0.008	0.648	3.09E-05	103.1325	6.28318	96.85447	3.28649E-05
0.9	0.00002	0.81	0.1	0.01	0.002	0.812	2.46E-05	129.2339	6.28318	122.9548	2.58885E-05



calculation atC1=30uf

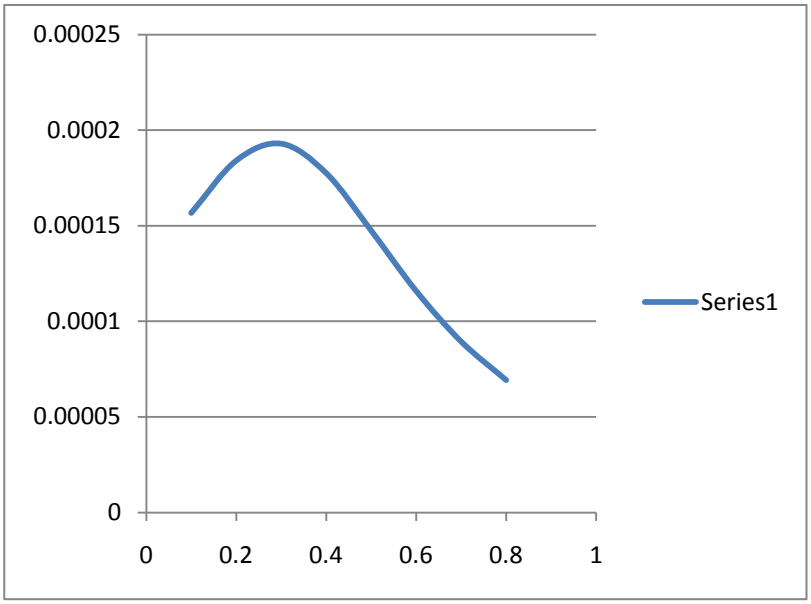
lambda	C1	y*y	x=1-y	x*x	(x*x)*0.1	(y*y)+(x*x)*0.1	C	Xc	Xl	Xeff	Ceff
0	0.00003	0	1	1	0.3	0.3	0.0001	31.831	6.28318	25.5674	0.000124
0.1	0.00003	0	0.9	0.8	0.243	0.253	0.0001	26.844	6.28318	20.58528	0.000155
0.2	0.00003	0	0.8	0.6	0.192	0.232	0.0001	24.616	6.28318	18.36006	0.000173
0.3	0.00003	0.1	0.7	0.5	0.147	0.237	0.0001	25.147	6.28318	18.88981	0.000169
0.4	0.00003	0.2	0.6	0.4	0.108	0.268	0.0001	28.436	6.28318	22.17509	0.000144
0.5	0.00003	0.3	0.5	0.3	0.075	0.325	9E-05	34.484	6.28318	28.21814	0.000113
0.6	0.00003	0.4	0.4	0.2	0.048	0.408	7E-05	43.29	6.28318	37.02051	8.6E-05
0.7	0.00003	0.5	0.3	0.1	0.027	0.517	6E-05	54.855	6.28318	48.58256	6.55E-05
0.8	0.00003	0.6	0.2	0	0.012	0.652	5E-05	69.179	6.28318	62.90418	5.06E-05
0.9	0.00003	0.8	0.1	0	0.003	0.813	4E-05	86.262	6.28318	79.98512	3.98E-05



Calculaton at
C1=40uf

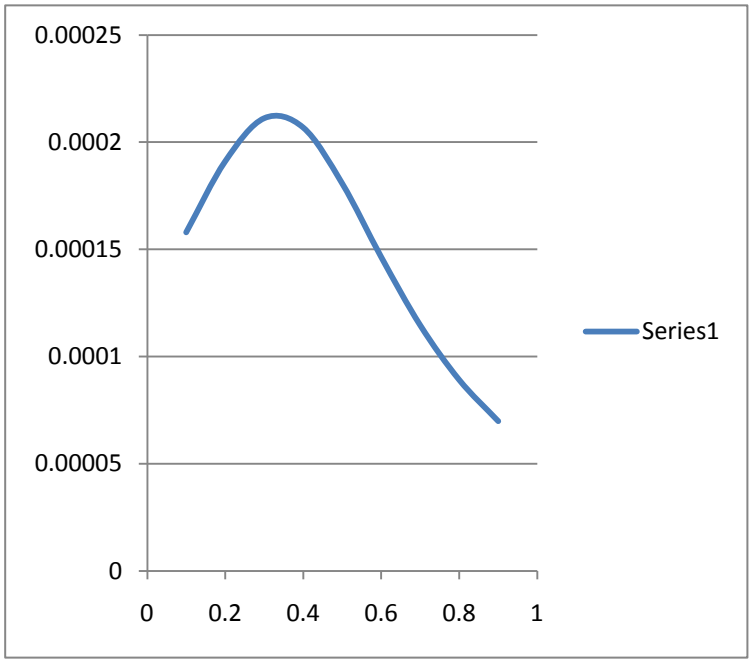
L=20mh

lambda	C1		x=1-y	x*x	(x*x)*0.1	(y*y)+(x*x)*0.1	C	Xc	Xl	Xeff	Ceff
0.1	0.00004	0.01	0.9	0.81	0.324	0.334	0.00012	26.5789	6.28318	20.3203	0.000157
0.2	0.00004	0.04	0.8	0.64	0.256	0.296	0.00014	23.555	6.28318	17.3007	0.000184
0.3	0.00004	0.09	0.7	0.49	0.196	0.286	0.00014	22.7592	6.28318	16.5063	0.000193
0.4	0.00004	0.16	0.6	0.36	0.144	0.304	0.00013	24.1916	6.28318	17.9363	0.000177
0.5	0.00004	0.25	0.5	0.25	0.1	0.35	0.00011	27.8521	6.28318	21.5921	0.000147
0.6	0.00004	0.36	0.4	0.16	0.064	0.424	9.4E-05	33.7409	6.28318	27.4759	0.000116
0.7	0.00004	0.49	0.3	0.09	0.036	0.526	7.6E-05	41.8578	6.28318	35.5887	8.94E-05
0.8	0.00004	0.64	0.2	0.04	0.016	0.656	6.1E-05	52.2029	6.28318	45.9306	6.93E-05
0.9	0.00004	0.81	0.1	0.01	0.004	0.814	4.9E-05	64.7761	6.28318	58.5015	5.44E-05



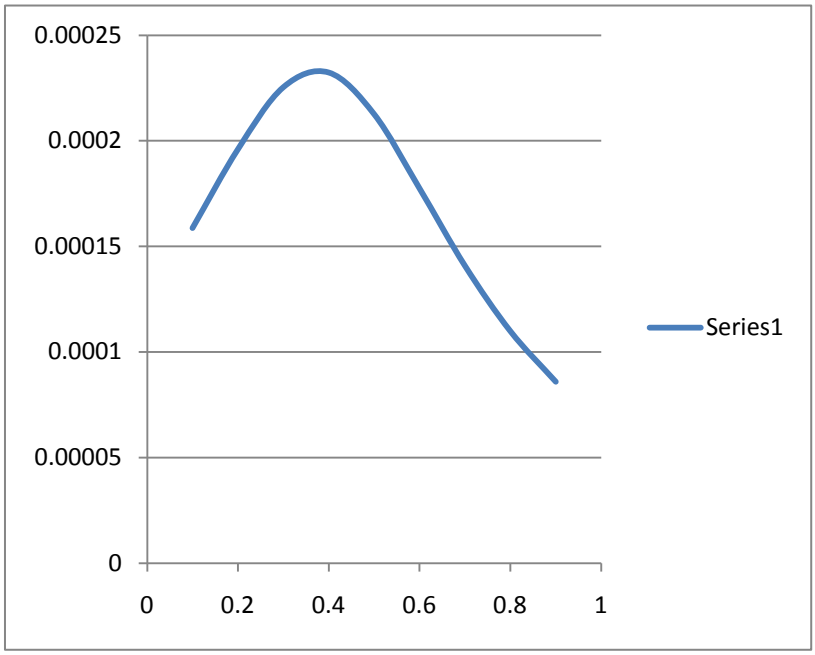
calculation atC1=50uf

(y)lambda	C1	y*y	x=1-y	x*x	(x*x)*0.1	(y*y)+(x*x)*0.1	C	Xc	Xl	Xeff	Ceff
0	0.00005	0	1	1	0.5	0.5	0.0001	31.831	6.283	25.5674	0.000124
0.1	0.00005	0.01	0.9	0.81	0.405	0.415	0.0001	26.42	6.283	20.16138	0.000158
0.2	0.00005	0.04	0.8	0.64	0.32	0.36	0.0001	22.918	6.283	16.66518	0.000191
0.3	0.00005	0.09	0.7	0.49	0.245	0.335	0.0001	21.327	6.283	15.0768	0.000211
0.4	0.00005	0.16	0.6	0.36	0.18	0.34	0.0001	21.645	6.283	15.39442	0.000207
0.5	0.00005	0.25	0.5	0.25	0.125	0.375	0.0001	23.873	6.283	17.61848	0.000181
0.6	0.00005	0.36	0.4	0.16	0.08	0.44	0.0001	28.011	6.283	21.75111	0.000146
0.7	0.00005	0.49	0.3	0.09	0.045	0.535	9E-05	34.059	6.283	27.794	0.000115
0.8	0.00005	0.64	0.2	0.04	0.02	0.66	8E-05	42.017	6.283	35.74775	8.9E-05
0.9	0.00005	0.81	0.1	0.01	0.005	0.815	6E-05	51.885	6.283	45.61234	6.98E-05



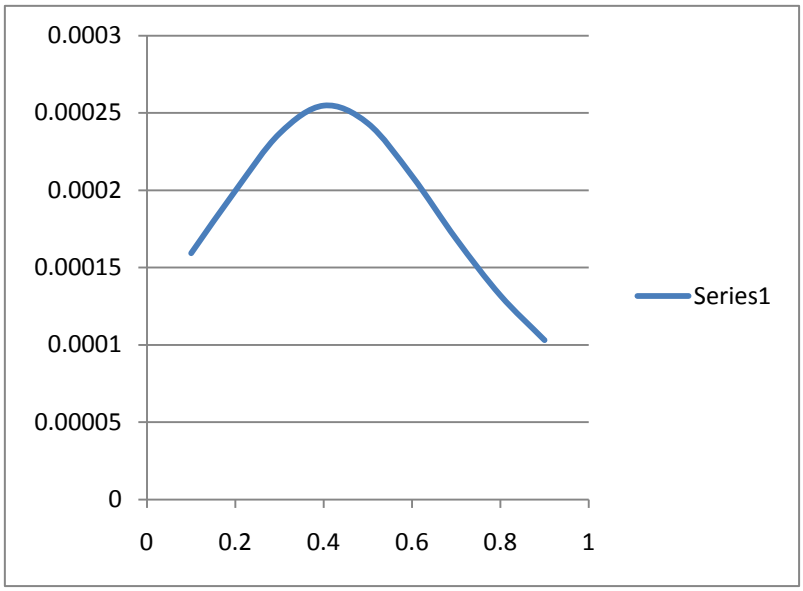
calculation at C1=60uf

lambda	C1	λ*λ	x=1-λ	x*x	(x*x)*0.1	(y*y)+(x*x)*0.1	C	Xc	Xl	Xeff	Ceff
0.1	0.00006	0	0.9	0.8	0.486	0.496	0.0001	26.314	6.28318	20.05541	0.000159
0.2	0.00006	0	0.8	0.6	0.384	0.424	0.0001	22.494	6.28318	16.24155	0.000196
0.3	0.00006	0.1	0.7	0.5	0.294	0.384	0.0002	20.372	6.28318	14.12411	0.000225
0.4	0.00006	0.2	0.6	0.4	0.216	0.376	0.0002	19.947	6.28318	13.7008	0.000232
0.5	0.00006	0.3	0.5	0.3	0.15	0.4	0.0002	21.221	6.28318	14.97093	0.000213
0.6	0.00006	0.4	0.4	0.2	0.096	0.456	0.0001	24.192	6.28318	17.93629	0.000177
0.7	0.00006	0.5	0.3	0.1	0.054	0.544	0.0001	28.86	6.28318	22.59908	0.000141
0.8	0.00006	0.6	0.2	0	0.024	0.664	9E-05	35.226	6.28318	28.96041	0.00011
0.9	0.00006	0.8	0.1	0	0.006	0.816	7E-05	43.29	6.28318	37.02051	8.6E-05



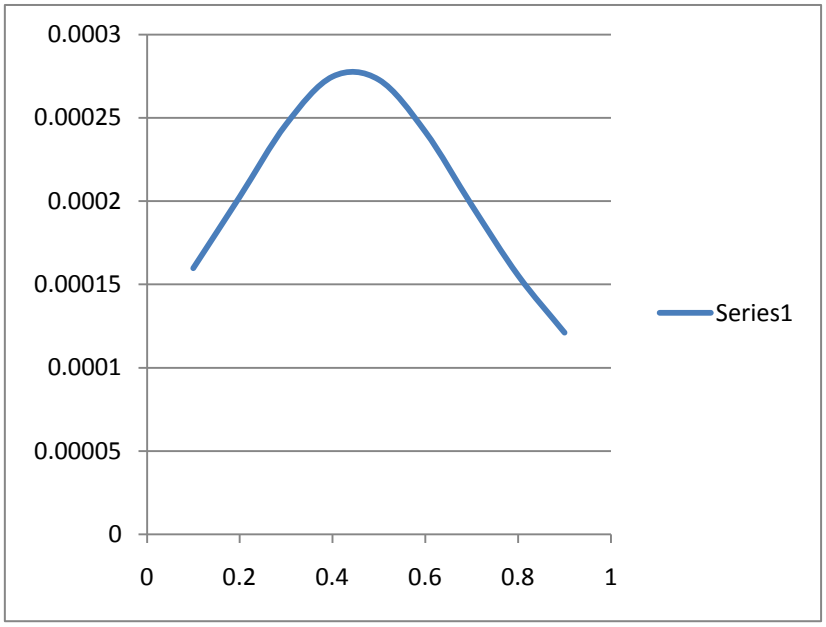
calculation at C=70uf

0.1	0.00007	0.01	0.9	0.81	0.567	0.577	0.0001	26.23785	6.28318	19.97971	0.000159
0.2	0.00007	0.04	0.8	0.64	0.448	0.488	0.0001	22.19077	6.28318	15.93899	0.0002
0.3	0.00007	0.09	0.7	0.49	0.343	0.433	0.0002	19.68976	6.28318	13.44382	0.000237
0.4	0.00007	0.16	0.6	0.36	0.252	0.412	0.0002	18.73483	6.28318	12.49174	0.000255
0.5	0.00007	0.25	0.5	0.25	0.175	0.425	0.0002	19.32597	6.28318	13.08107	0.000243
0.6	0.00007	0.36	0.4	0.16	0.112	0.472	0.0001	21.4632	6.28318	15.21292	0.000209
0.7	0.00007	0.49	0.3	0.09	0.063	0.553	0.0001	25.1465	6.28318	18.88981	0.000169
0.8	0.00007	0.64	0.2	0.04	0.028	0.668	0.0001	30.37588	6.28318	24.11345	0.000132
0.9	0.00007	0.81	0.1	0.01	0.007	0.817	9E-05	37.15134	6.28318	30.88436	0.000103



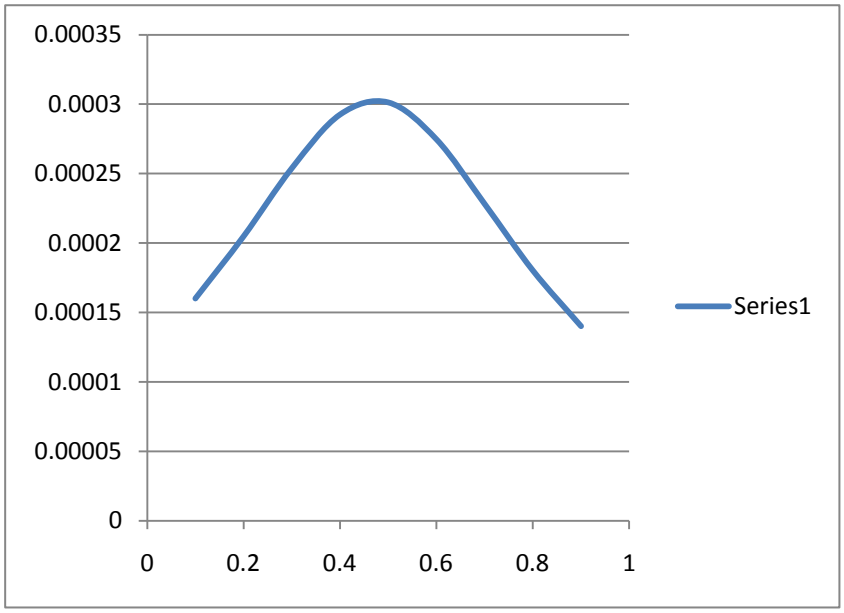
calculation at C1=80uf

0.1	0.00008	0.01	0.9	0.81	0.648	0.658	0.00012	26.18101	6.28318	19.92294	0.00016
0.2	0.00008	0.04	0.8	0.64	0.512	0.552	0.00014	21.9634	6.28318	15.71208	0.000203
0.3	0.00008	0.09	0.7	0.49	0.392	0.482	0.00017	19.17819	6.28318	12.93372	0.000246
0.4	0.00008	0.16	0.6	0.36	0.288	0.448	0.00018	17.82537	6.28318	11.58543	0.000275
0.5	0.00008	0.25	0.5	0.25	0.2	0.45	0.00018	17.90495	6.28318	11.66471	0.000273
0.6	0.00008	0.36	0.4	0.16	0.128	0.488	0.00016	19.41692	6.28318	13.17175	0.000242
0.7	0.00008	0.49	0.3	0.09	0.072	0.562	0.00014	22.36129	6.28318	16.10918	0.000198
0.8	0.00008	0.64	0.2	0.04	0.032	0.672	0.00012	26.73805	6.28318	20.4793	0.000155
0.9	0.00008	0.81	0.1	0.01	0.008	0.818	9.8E-05	32.54721	6.28318	26.28306	0.000121



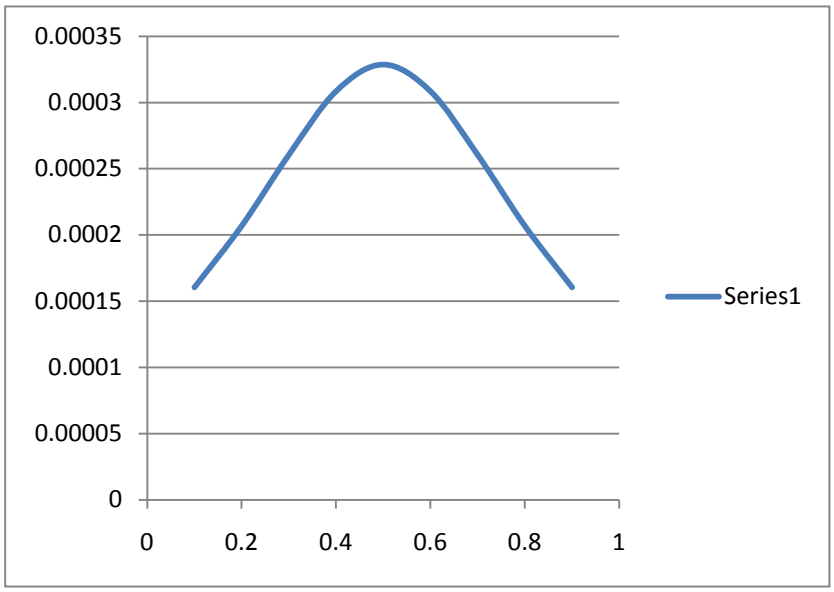
C1=90uf

0.1	0.00009	0.01	0.9	0.81	0.729	0.739	0.000122	26.1368	6.28318	19.87879	0.00016013
0.2	0.00009	0.04	0.8	0.64	0.576	0.616	0.000146	21.78656	6.28318	15.5356	0.00020489
0.3	0.00009	0.09	0.7	0.49	0.441	0.531	0.000169	18.7803	6.28318	12.53706	0.0002539
0.4	0.00009	0.16	0.6	0.36	0.324	0.484	0.000186	17.11801	6.28318	10.88088	0.00029254
0.5	0.00009	0.25	0.5	0.25	0.225	0.475	0.000189	16.7997	6.28318	10.56396	0.00030132
0.6	0.00009	0.36	0.4	0.16	0.144	0.504	0.000179	17.82537	6.28318	11.58543	0.00027475
0.7	0.00009	0.49	0.3	0.09	0.081	0.571	0.000158	20.19501	6.28318	13.94773	0.00022822
0.8	0.00009	0.64	0.2	0.04	0.036	0.676	0.000133	23.90863	6.28318	17.65379	0.00018031
0.9	0.00009	0.81	0.1	0.01	0.009	0.819	0.00011	28.96622	6.28318	22.70508	0.00014019



calculation at
C1=C2=100uf

0.1	0.0001	0.01	0.9	0.81	0.81	0.82	0.000122	26.10143	6.28318	19.84347	0.00016
0.2	0.0001	0.04	0.8	0.64	0.64	0.68	0.000147	21.64509	6.28318	15.39442	0.000207
0.3	0.0001	0.09	0.7	0.49	0.49	0.58	0.000172	18.46199	6.28318	12.21979	0.00026
0.4	0.0001	0.16	0.6	0.36	0.36	0.52	0.000192	16.55213	6.28318	10.31752	0.000309
0.5	0.0001	0.25	0.5	0.25	0.25	0.5	0.0002	15.91551	6.28318	9.684097	0.000329
0.6	0.0001	0.36	0.4	0.16	0.16	0.52	0.000192	16.55213	6.28318	10.31752	0.000309
0.7	0.0001	0.49	0.3	0.09	0.09	0.58	0.000172	18.46199	6.28318	12.21979	0.00026
0.8	0.0001	0.64	0.2	0.04	0.04	0.68	0.000147	21.64509	6.28318	15.39442	0.000207
0.9	0.0001	0.81	0.1	0.01	0.01	0.82	0.000122	26.10143	6.28318	19.84347	0.00016

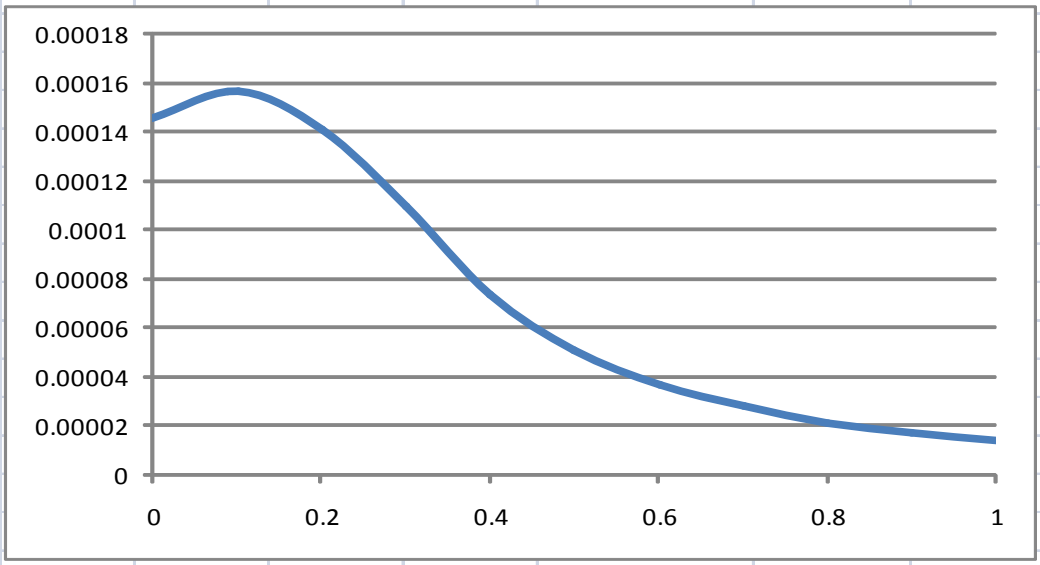


Total saving =4,324

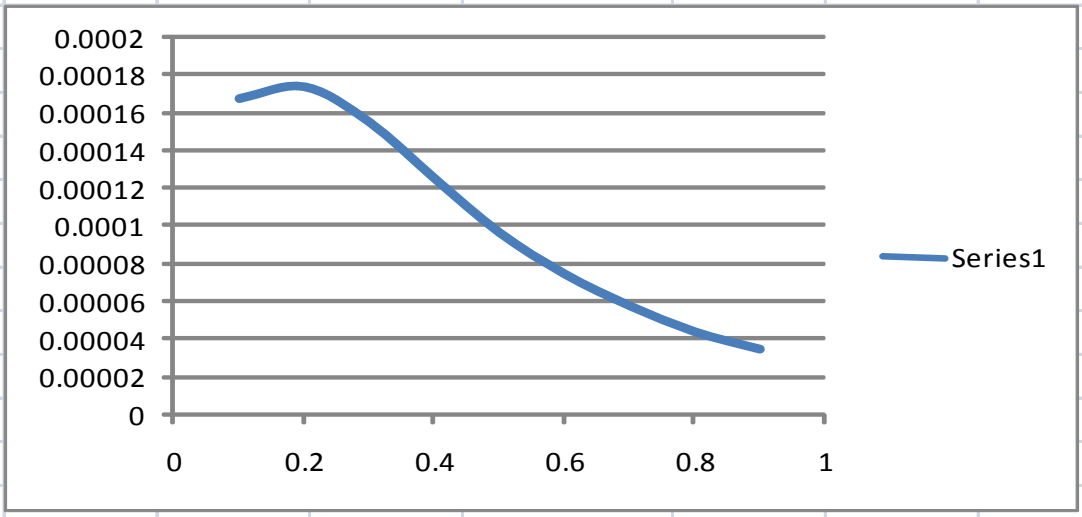
APPENDIX C

Simulation Results of C_{eff} against λ

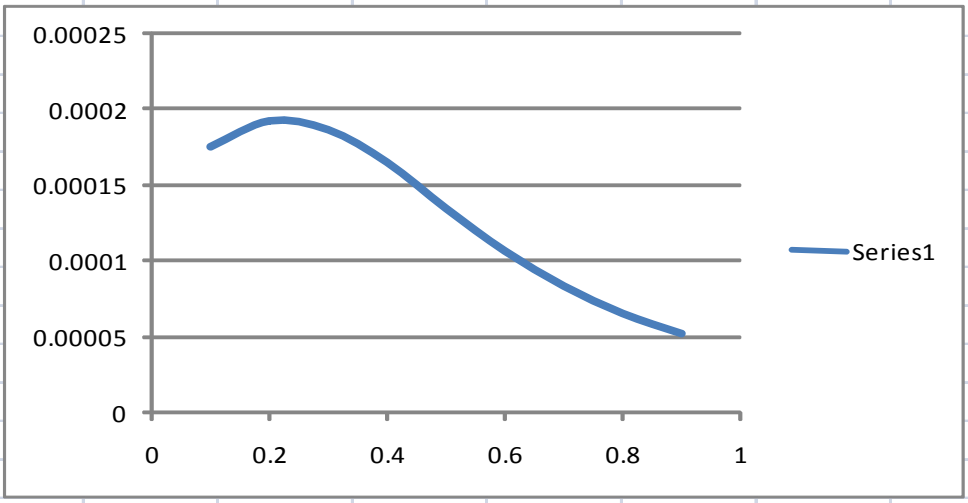
			C1=10uf			
	lambda	Ic	Xc	multiplication	c	
	0	0.93	21.80645	6847.225806	0.00014604	
	0.1	1	20.28	6367.92	0.00015704	
	0.2	0.9	22.53333	7075.466667	0.00014133	
	0.3	0.7	28.97143	9097.028571	0.00010993	
	0.4	0.47	43.14894	13548.76596	7.3807E-05	
	0.5	0.326	62.20859	19533.49693	5.1194E-05	
	0.6	0.236	85.9322	26982.71186	3.7061E-05	
	0.7	0.18	112.6667	35377.33333	2.8267E-05	
	0.8	0.138	146.9565	46144.34783	2.1671E-05	
	0.9	0.11	184.3636	57890.18182	1.7274E-05	
	1	0.089	227.8652	71549.66292	1.3976E-05	



		at C=20um					
	lambda	Ic	Xc	multiplication	c		
	0	0.934	21.71306	6817.901499	0.000147		
	0.1	1.07	18.95327	5951.327103	0.000168		
	0.2	1.11	18.27027	5736.864865	0.000174		
	0.3	0.99	20.48485	6432.242424	0.000155		
	0.4	0.799	25.38173	7969.862328	0.000125		
	0.5	0.615	32.97561	10354.34146	9.66E-05		
	0.6	0.475	42.69474	13406.14737	7.46E-05		
	0.7	0.367	55.25886	17351.28065	5.76E-05		
	0.8	0.279	72.68817	22824.08602	4.38E-05		
	0.9	0.22	92.18182	28945.09091	3.45E-05		
	1	0.179	113.2961	35574.97207	2.81E-05		
Vs=28.28							
C1=20uF							
C2=100uF							
L=5mH							
R=1							

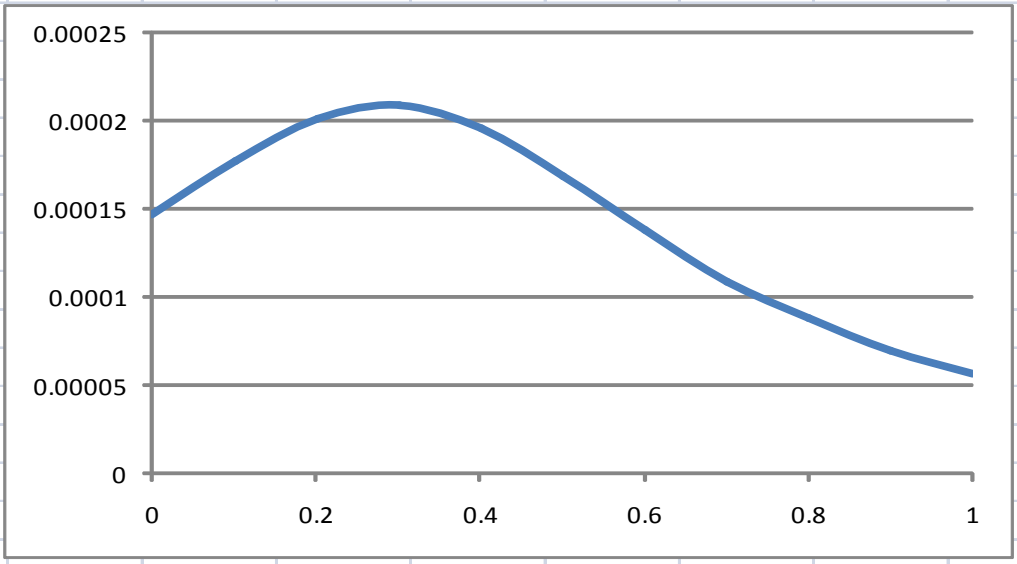


			at C1=30uf					
		lambda	Ic	Xc	multiplica	c		
		0	0.934	21.71306	6817.901	0.000147		
		0.1	1.115	18.18834	5711.139	0.000175		
		0.2	1.223	16.58217	5206.803	0.000192		
		0.3	1.186	17.09949	5369.241	0.000186		
		0.4	1.0496	19.32165	6066.997	0.000165		
		0.5	0.857	23.66394	7430.478	0.000135		
		0.6	0.679	29.86745	9378.38	0.000107		
		0.7	0.533	38.04878	11947.32	8.37E-05		
		0.8	0.418	48.51675	15234.26	6.56E-05		
		0.9	0.334	60.71856	19065.63	5.25E-05		
		1	0.27	75.11111	23584.89	4.24E-05		
Vs=28.28								
C1=30uF								
C2=100uF								
L=5mH								
R=1								

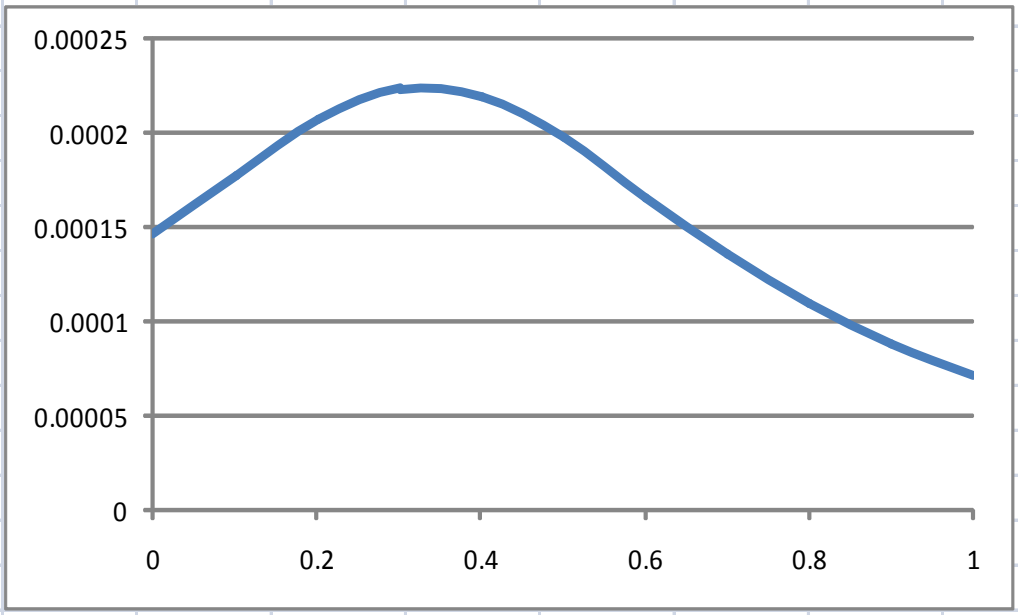


				at C1=40uf				
			lambda	Ic	Xc	multiplica	c	
			0	0.934	21.71306	6817.901	0.000147	
			0.1	1.127	17.99468	5650.328	0.000177	
			0.2	1.28	15.84375	4974.938	0.000201	
			0.3	1.33	15.24812	4787.91	0.000209	
			0.4	1.245	16.28916	5114.795	0.000196	
			0.5	1.078	18.81262	5907.161	0.000169	
			0.6	0.878	23.09795	7252.756	0.000138	
			0.7	0.697	29.09613	9136.184	0.000109	
			0.8	0.561	36.14973	11351.02	8.81E-05	
			0.9	0.444	45.67568	14342.16	6.97E-05	
			1	0.362	56.0221	17590.94	5.68E-05	

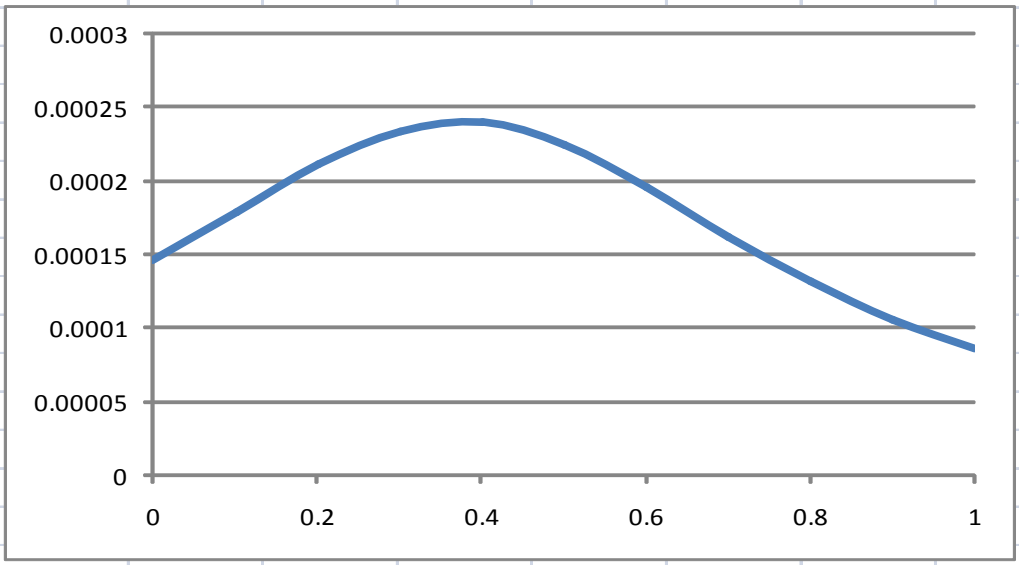
Vs=28.28
C1=40uF
C2=100uF
L=5mH
R=1



			at C1=50uf					
		lambda	Ic	Xc	multiplica	c		
		0	0.934	21.71306	6817.901	0.000147		
		0.1	1.134	17.8836	5615.45	0.000178		
		0.2	1.319	15.37528	4827.839	0.000207		
		0.3	1.424	14.24157	4471.854	0.000224		
		0.4	1.4	14.48571	4548.514	0.00022		
		0.5	1.261	16.08247	5049.897	0.000198		
		0.6	1.056	19.20455	6030.227	0.000166		
		0.7	0.869	23.33717	7327.871	0.000136		
		0.8	0.702	28.88889	9071.111	0.00011		
		0.9	0.562	36.08541	11330.82	8.83E-05		
		1	0.455	44.57143	13995.43	7.15E-05		
Vs=28.28								
C1=50uF								
C2=100uF								
L=5mH								
R=1								



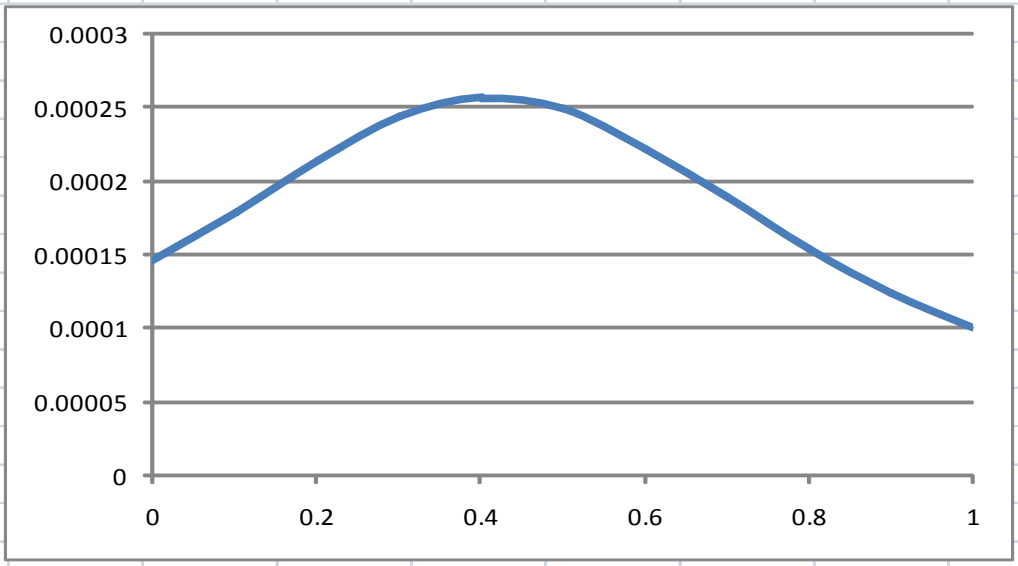
				at C1=60uf				
		lambda	Ic	Xc	multiplica	c		
		0	0.934	21.71306	6817.901	0.000147		
		0.1	1.138	17.82074	5595.712	0.000179		
		0.2	1.344	15.08929	4738.036	0.000211		
		0.3	1.49	13.61074	4273.772	0.000234		
		0.4	1.53	13.2549	4162.039	0.00024		
		0.5	1.433	14.15213	4443.768	0.000225		
		0.6	1.247	16.26303	5106.592	0.000196		
		0.7	1.035	19.5942	6152.58	0.000163		
		0.8	0.843	24.05694	7553.879	0.000132		
		0.9	0.677	29.95569	9406.086	0.000106		
		1	0.549	36.93989	11599.13	8.62E-05		



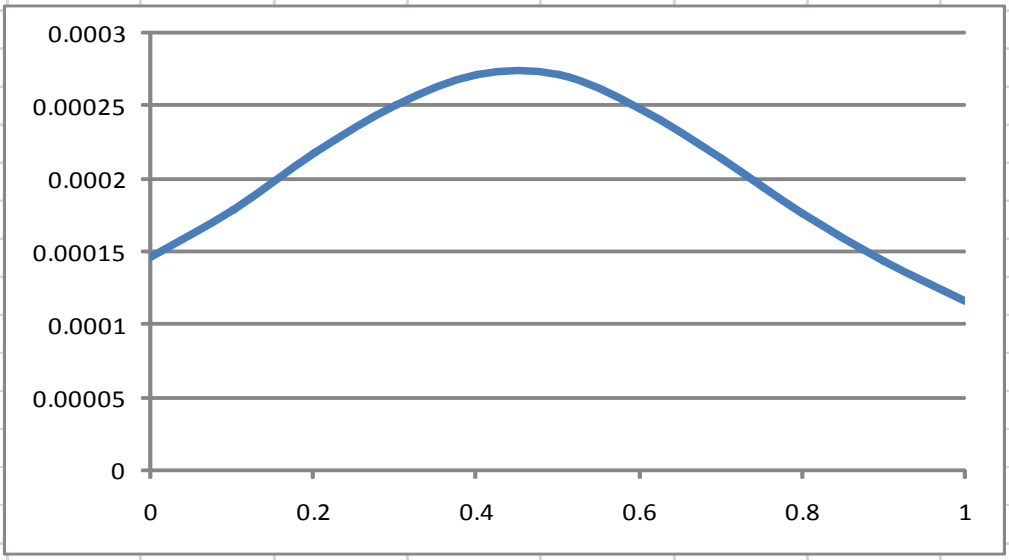
Vs=28.27
C1=60uF
C2=100uF
L=5mH
R=0

				at C1=70uf				
		lambda	Ic	Xc	multiplica	c		
		0	0.943	21.50583	6752.831	0.000147		
		0.1	1.142	17.75832	5576.112	0.000179		
		0.2	1.361	14.90081	4678.854	0.000214		
		0.3	1.552	13.06701	4103.041	0.000244		
		0.4	1.635	12.40367	3894.752	0.000257		
		0.5	1.589	12.76274	4007.502	0.00025		
		0.6	1.411	14.37279	4513.055	0.000222		
		0.7	1.205	16.82988	5284.581	0.000189		
		0.8	0.979	20.71502	6504.515	0.000154		
		0.9	0.794	25.54156	8020.05	0.000125		
		1	0.644	31.49068	9888.075	0.000101		

Vs=28.28
C1=70uF
C2=100uF
L=5mH
R=1



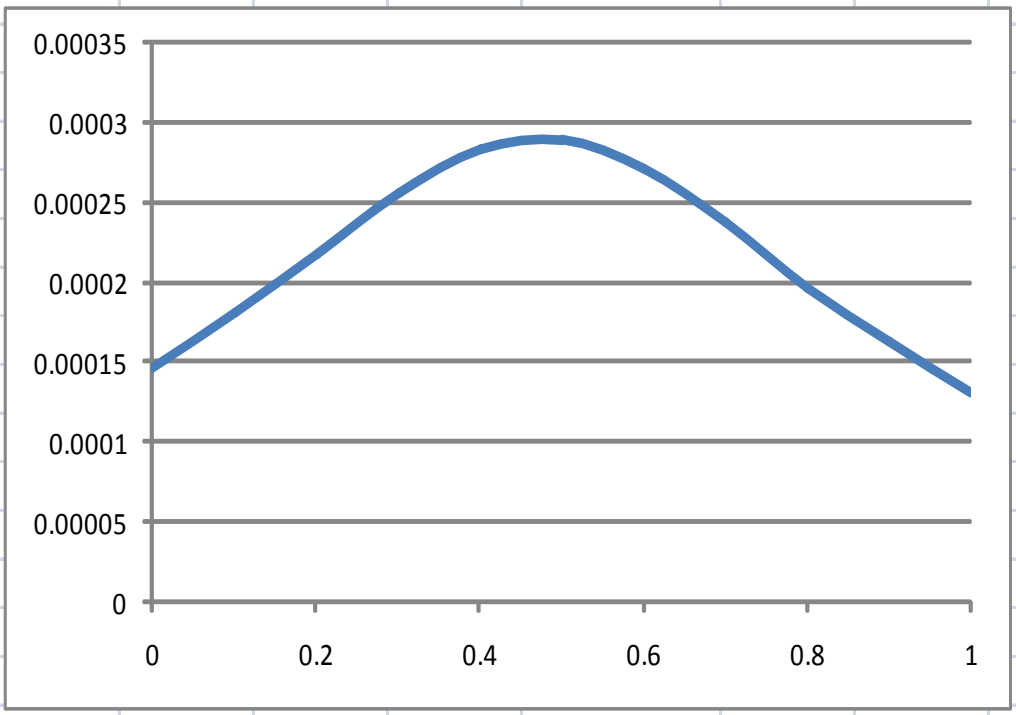
				at C1=80uf				
		lambda	Ic	Xc	multiplica	c		
		0	0.934	21.71306	6817.901	0.000147		
		0.1	1.14	17.78947	5585.895	0.000179		
		0.2	1.387	14.62149	4591.146	0.000218		
		0.3	1.596	12.70677	3989.925	0.000251		
		0.4	1.727	11.74291	3687.273	0.000271		
		0.5	1.727	11.74291	3687.273	0.000271		
		0.6	1.583	12.81112	4022.691	0.000249		
		0.7	1.361	14.90081	4678.854	0.000214		
		0.8	1.122	18.07487	5675.508	0.000176		
		0.9	0.918	22.0915	6936.732	0.000144		
		1	0.74	27.40541	8605.297	0.000116		
Vs=28.28								
C1=80uF								
C2=100uF								
L=5mH								
R=1								



at C1=90uf

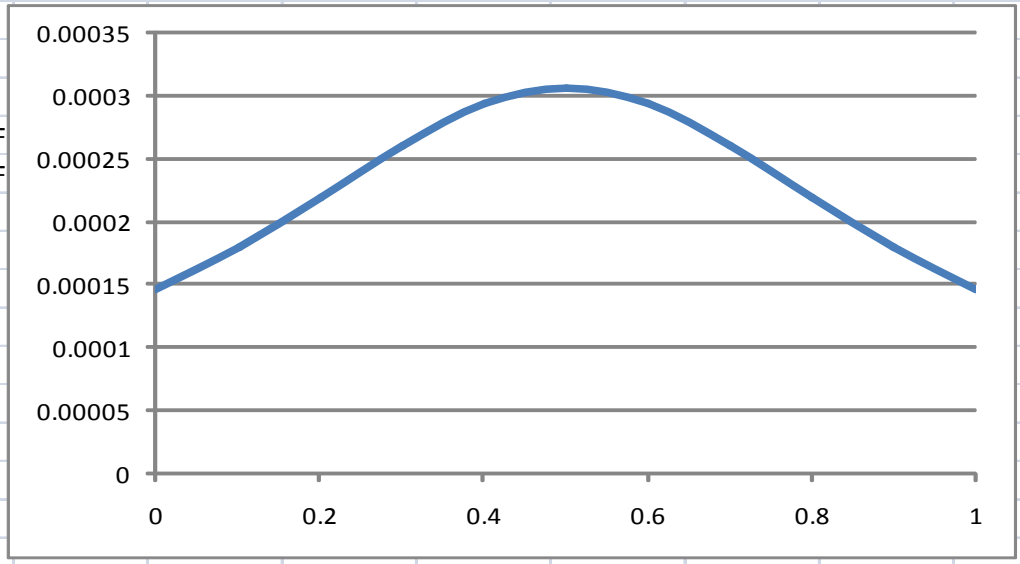
lambda	Ic	Xc	multiplication	c
0	0.934	21.71306	6817.901499	0.000147
0.1	1.153	17.5889	5522.914137	0.000181
0.2	1.393	14.55851	4571.371141	0.000219
0.3	1.633	12.41886	3899.522352	0.000256
0.4	1.804	11.24169	3529.889135	0.000283
0.5	1.842	11.00977	3457.068404	0.000289
0.6	1.726	11.74971	3689.409038	0.000271
0.7	1.511	13.42158	4214.374586	0.000237
0.8	1.257	16.13365	5065.966587	0.000197
0.9	1.035	19.5942	6152.57971	0.000163
1	0.836	24.25837	7617.129187	0.000131

Vs=28.28
C1=90uF
C2=100uF
L=5mH
R=1

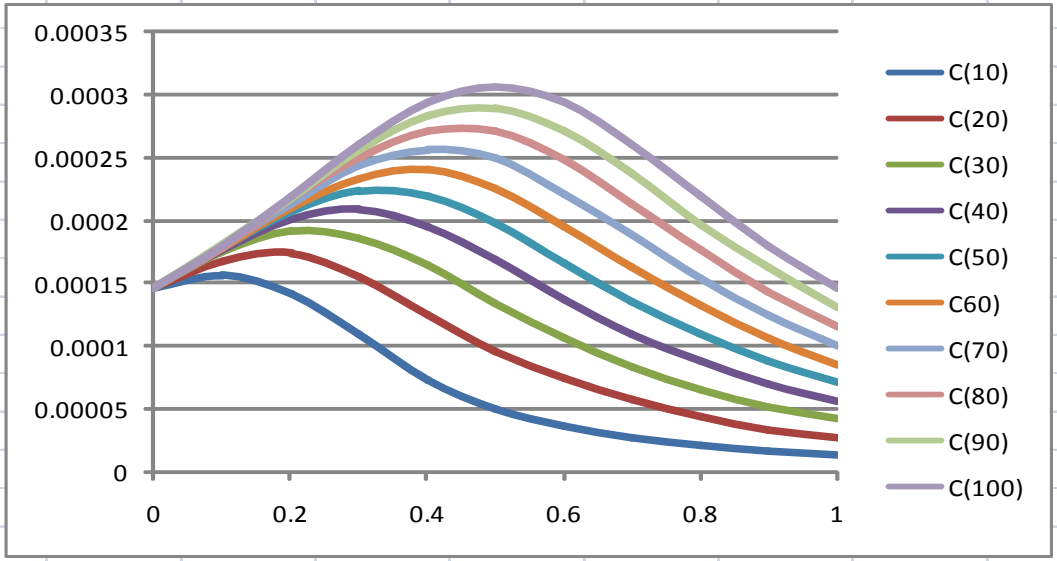


				at C1=C2=100uf				
		lambda	Ic	Xc	multiplica	c		
		0	0.934	21.71306	6817.901	0.000147		
		0.1	1.15	17.63478	5537.322	0.000181		
		0.2	1.4	14.48571	4548.514	0.00022		
		0.3	1.66	12.21687	3836.096	0.000261		
		0.4	1.87	10.84492	3405.305	0.000294		
		0.5	1.95	10.4	3265.6	0.000306		
		0.6	1.87	10.84492	3405.305	0.000294		
		0.7	1.66	12.21687	3836.096	0.000261		
		0.8	1.4	14.48571	4548.514	0.00022		
		0.9	1.15	17.63478	5537.322	0.000181		
		1	0.934	21.71306	6817.901	0.000147		

Vs=28.28
C1=100uF
C2=100uF
L=5mH
R=1



					simulation					
	C(10)	C(20)	C(30)	C(40)	C(50)	C60)	C(70)	C(80)	C(90)	C(100)
0	0.000146	0.000147	0.000147	0.000147	0.000147	0.000147	0.000147	0.000147	0.000147	0.000146673
0.1	0.000157	0.000168	0.000175	0.000177	0.000178	0.000179	0.000179	0.000179	0.000181	0.000180593
0.2	0.000141	0.000174	0.000192	0.000201	0.000207	0.000211	0.000214	0.000218	0.000219	0.000219852
0.3	0.00011	0.000155	0.000186	0.000209	0.000224	0.000234	0.000244	0.000251	0.000256	0.000260682
0.4	7.38E-05	0.000125	0.000165	0.000196	0.00022	0.00024	0.000257	0.000271	0.000283	0.000293659
0.5	5.12E-05	9.66E-05	0.000135	0.000169	0.000198	0.000225	0.00025	0.000271	0.000289	0.000306222
0.6	3.71E-05	7.46E-05	0.000107	0.000138	0.000166	0.000196	0.000222	0.000249	0.000271	0.000293659
0.7	2.83E-05	5.76E-05	8.37E-05	0.000109	0.000136	0.000163	0.000189	0.000214	0.000237	0.000260682
0.8	2.17E-05	4.38E-05	6.56E-05	8.81E-05	0.00011	0.000132	0.000154	0.000176	0.000197	0.000219852
0.9	1.73E-05	3.45E-05	5.25E-05	6.97E-05	8.83E-05	0.000106	0.000125	0.000144	0.000163	0.000180593
1	1.4E-05	2.81E-05	4.24E-05	5.68E-05	7.15E-05	8.62E-05	0.000101	0.000116	0.000131	0.000146673



APPENDIX D

Change in Power Factor as a Function of R/L

Xl/R	R	L	XL	Fai	I(RL)	Ic	Xc	C	R/XL	angle	pf		C
0.07854	20	0.005	1.570795	0.078379	0.99693	0.078058	256.2189	1.24E-05	12.73241	4.490778	0.99693		1.24E-05
0.15708	20	0.01	3.14159	0.155806	0.987887	0.153297	130.4657	2.44E-05	6.366203	8.927047	0.987887		2.44E-05
0.235619	20	0.015	4.712385	0.231399	0.973347	0.223227	89.59509	3.55E-05	4.244135	13.25817	0.973347		3.55E-05
0.314159	20	0.02	6.28318	0.304396	0.954028	0.285938	69.94521	4.55E-05	3.183102	17.44058	0.954028		4.55E-05
0.392699	20	0.025	7.853975	0.374196	0.930802	0.340231	58.7836	5.42E-05	2.546481	21.43987	0.930802		5.42E-05
0.471239	20	0.03	9.42477	0.440375	0.904592	0.385608	51.86612	6.14E-05	2.122068	25.23162	0.904592		6.14E-05
0.549778	20	0.035	10.99557	0.502673	0.876298	0.422174	47.37387	6.72E-05	1.818915	28.80104	0.876298		6.72E-05
0.628318	20	0.04	12.56636	0.560982	0.846733	0.450477	44.39738	7.17E-05	1.591551	32.14189	0.846733		7.17E-05
0.706858	20	0.045	14.13716	0.615314	0.816592	0.471349	42.43139	7.5E-05	1.414712	35.25488	0.816592		7.5E-05
0.785398	20	0.05	15.70795	0.665773	0.786439	0.485758	41.17276	7.73E-05	1.273241	38.146	0.786439		7.73E-05

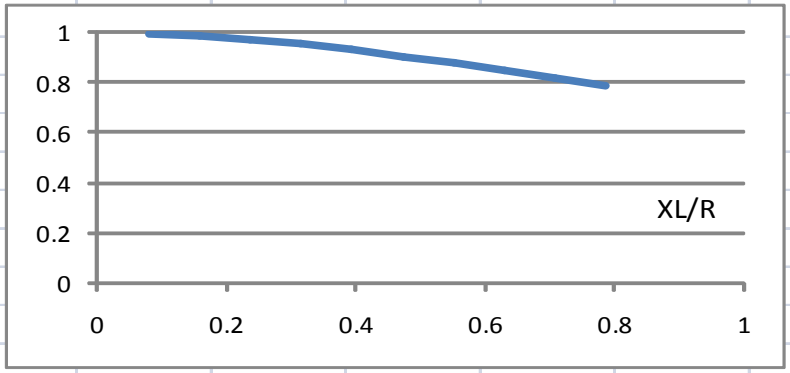


Fig. power Factor versus XL/R when L is changing

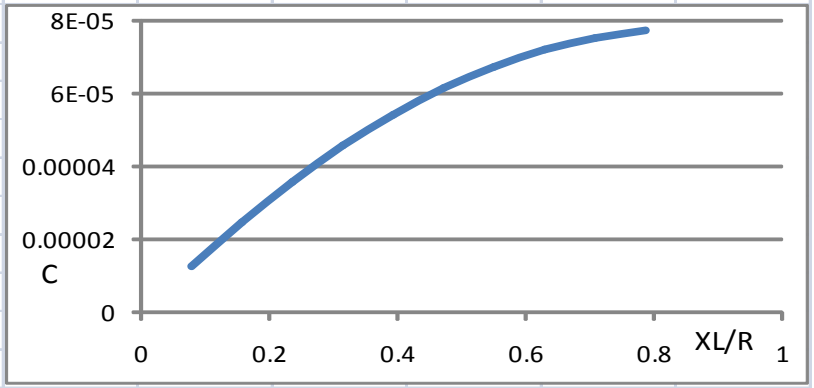


Fig. Capactor versus XL/R when L is changing

R/XL	R	L	XL	Fai	I(RL)	Ic	Xc	C	angle	pf	XL/R	C
0.127324	2	0.05	15.70795	1.444154	1.263044	1.252929	15.9626	0.000199	82.75	0.13	7.853975	0.000199
0.254648	4	0.05	15.70795	1.321448	1.233864	1.195704	16.72654	0.00019	75.7	0.25	3.926988	0.00019
0.381972	6	0.05	15.70795	1.205927	1.189424	1.111124	17.99978	0.000177	69	0.36	2.617992	0.000177
0.509296	8	0.05	15.70795	1.099739	1.134571	1.011004	19.78232	0.000161	63	0.45	1.963494	0.000161
0.63662	10	0.05	15.70795	1.003884	1.074059	0.906037	22.07415	0.000144	57.5	0.54	1.570795	0.000144
0.763944	12	0.05	15.70795	0.91843	1.01178	0.804011	24.87528	0.000128	52.6	0.6	1.308996	0.000128
0.891268	14	0.05	15.70795	0.842826	0.950508	0.709579	28.18571	0.000113	48.3	0.66	1.121996	0.000113
1.018592	16	0.05	15.70795	0.776188	0.891987	0.624894	32.00543	9.95E-05	44.45	0.71	0.981747	9.95E-05
1.145917	18	0.05	15.70795	0.717505	0.837165	0.550442	36.33445	8.76E-05	41.1	0.75	0.872664	8.76E-05
1.273241	20	0.05	15.70795	0.665773	0.786439	0.485758	41.17276	7.73E-05	38.13	0.78	0.785398	7.73E-05

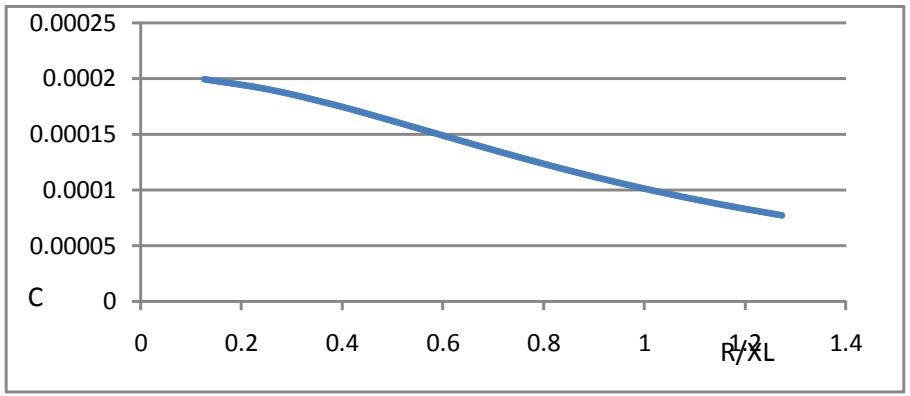


Fig. Capacitor versus R/XL when R is changing

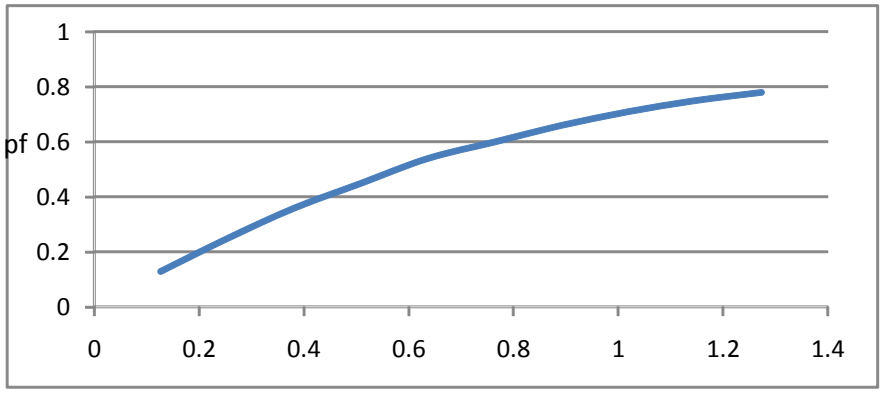


Fig. power Factor versus R/XL when R is changing

APPENDIX E

Total Harmonic Distortion as a Function of λ

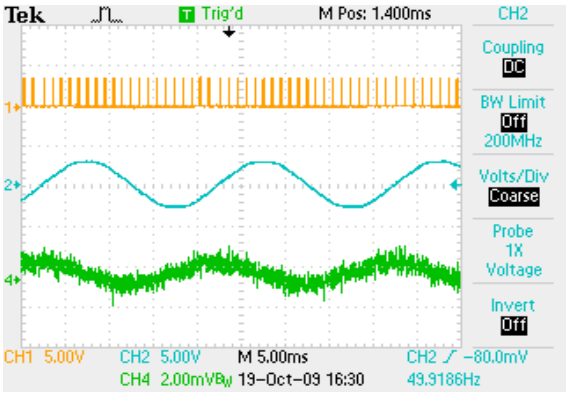
		lambda	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1	
		0	0	0	0	0	0	0	0	0	0	0	
		0.1	0.094827	0.091032	0.187452	0.106163	0.114774	0.131916	0.122603	0.117884	0.13423	0.138658	
		0.2	0.097177	0.132743	0.107476	0.119816	0.118709	0.125639	0.148662	0.148825	0.131119	0.145387	
		0.3	0.130206	0.119532	0.167351	0.205153	0.126676	0.180144	0.14923	0.233769	0.197272	0.148297	
		0.4	0.259577	0.094813	0.098827	0.101752	0.127146	0.136686	0.145147	0.15145	0.150526	0.146633	
		0.5	0.274235	0.088298	0.242874	0.133777	0.196533	0.124641	0.173801	0.04469	0.159424	0.157562	
		0.6	0.176774	0.053266	0.271484	0.206111	0.136268	0.120853	0.133861	0.089181	0.141774	0.138993	
		0.7	0.282321	0.15173	0.234094	0.176049	0.171422	0.180611	0.113399	0.145792	0.134198	0.146212	
		0.8	0.239855	0.115626	0.055189	0.136818	0.171522	0.114194	0.274674	0.132995	0.160537	0.132177	
		0.9	0.10443	0.117333	0.079758	0.164094	0.125742	0.111138	0.122245	0.14282	0.146447	0.137374	
		1	0	0	0	0	0	0	0	0	0	0	
		Max:	0.282321	0.15173	0.271484	0.206111	0.196533	0.180611	0.274674	0.233769	0.197272	0.157562	
Max THD	0.282321												
Min THD	0.15173												
AVG THD	0.119732												

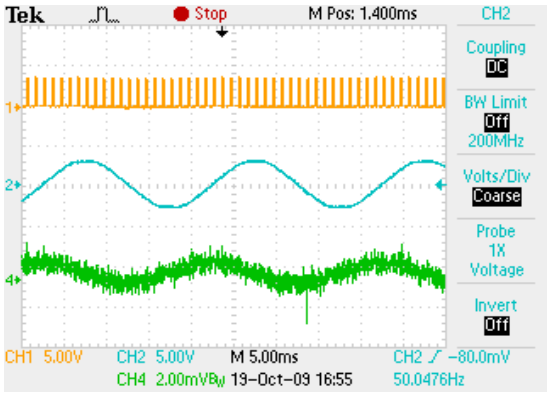
APPENDIX F

Practical Results of The Compensated Reactive Currents and the Equivalent Switching Patterns

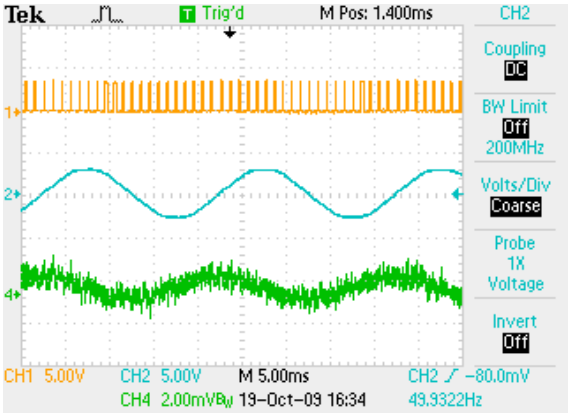
Λ (duty cycle) Gama($\gamma = (C1/C2)$ (0.1) Gama(γ) (0.2)

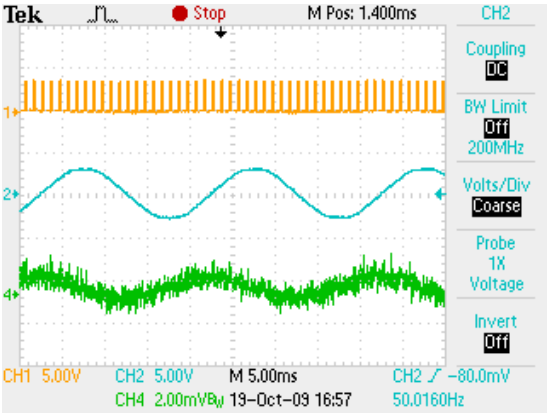
0.1



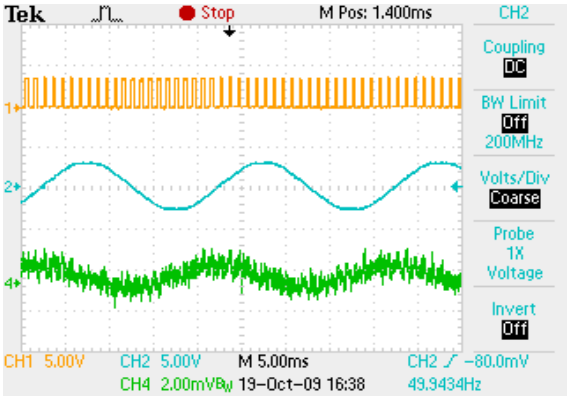


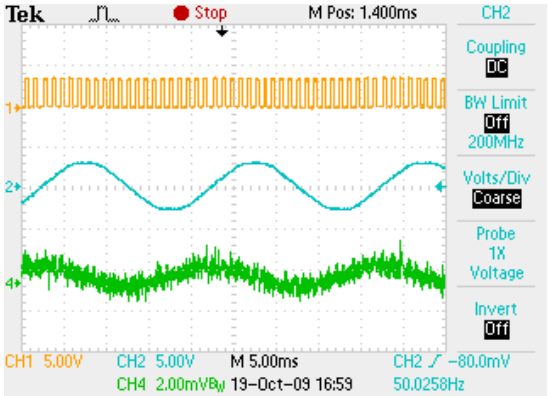
0.2



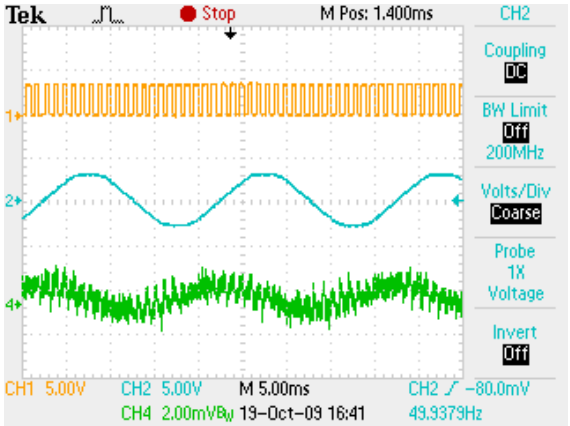


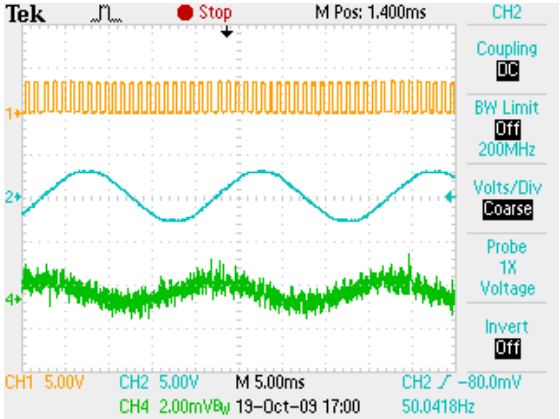
0.3



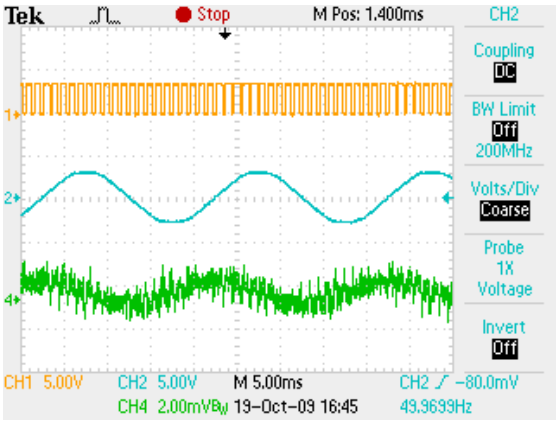


0.4





0.5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DC
BW Limit
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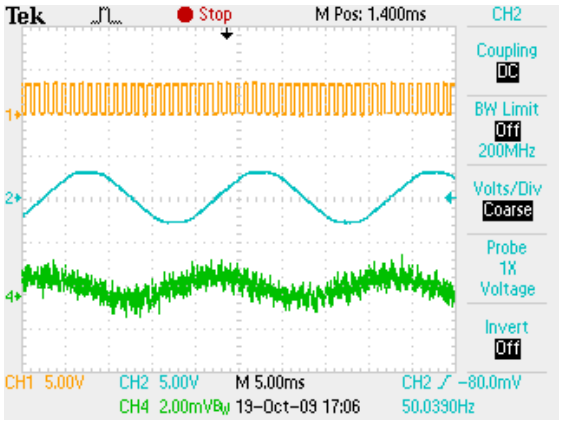
Volts/Div
Coarse
Probe
1X
Voltage
Invert
Off
CH1 5.00V
CH2 5.00V
M 5.00ms
CH2 ∕ −80.0mV
CH4 2.00mVBW 19-Oct-09 16:45
49.9699Hz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DC
BW Limit
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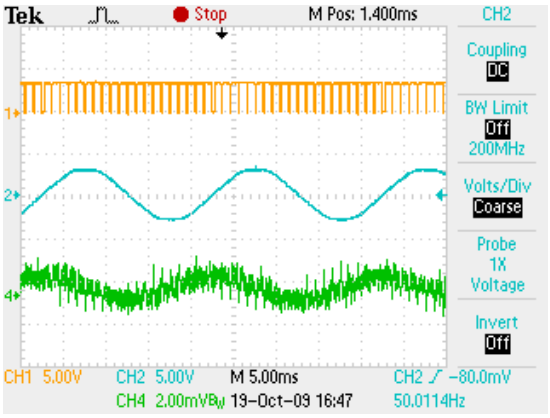
200MHz
Volts/Div
Coarse
Probe
1X
Voltage
Invert
Off
CH1 5.00V
CH2 5.00V
M 5.00ms
CH2 ∕ −80.0mV
CH4 2.00mVBW 19-Oct-09 17:06
50.0390Hz

0.6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DC
BW Limit
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200MHz
Volts/Div
Coarse
Probe
1X
Voltage
Invert
Off
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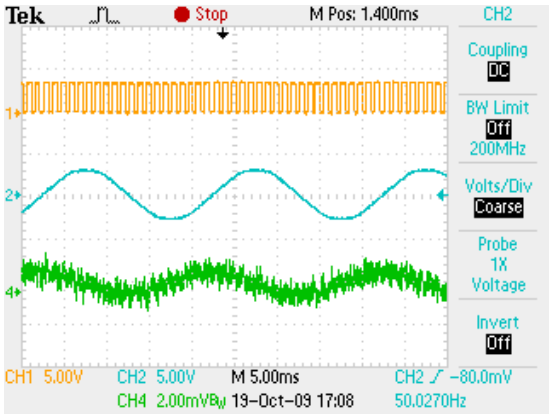
M 5.00ms
CH2 ∕ −80.0mV
CH4 2.00mVBW 19-Oct-09 16:47
50.0114Hz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DC
BW Limit
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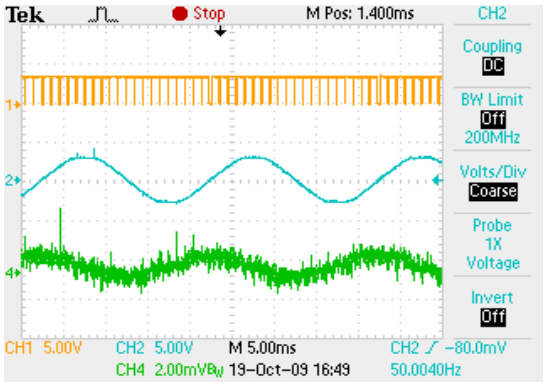
200MHz
Volts/Div
Coarse
Probe
1X
Voltage
Invert
Off
CH1 5.00V
CH2 5.00V
M 5.00ms
CH2 ∕ −80.0mV
CH4 2.00mVBW 19-Oct-09 17:08
50.0270Hz

0.7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BW Limit
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200MHz
Volts/Div
Coarse
Probe
1X
Voltage
Invert
Off
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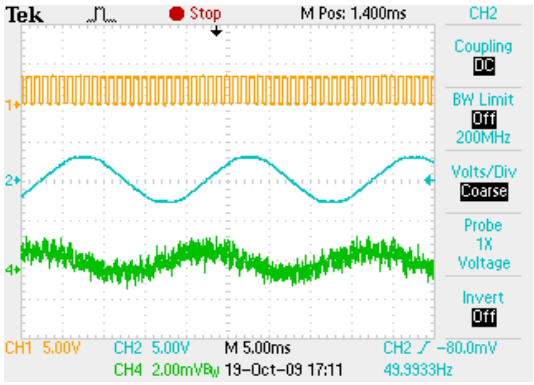
CH2 5.00V
M 5.00ms
CH2 ∕ −80.0mV
CH4 2.00mVBW 19-Oct-09 16:49
50.0040Hz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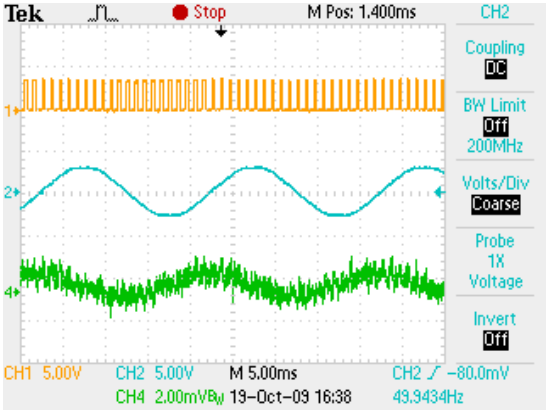
200MHz
Volts/Div
Coarse
Probe
1X
Voltage
Invert
Off
CH1 5.00V
CH2 5.00V
M 5.00ms
CH2 ∕ −80.0mV
CH4 2.00mVBW 19-Oct-09 17:11
49.9933Hz

0.8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Volts/Div
Coarse
Probe
1X
Voltage
Invert
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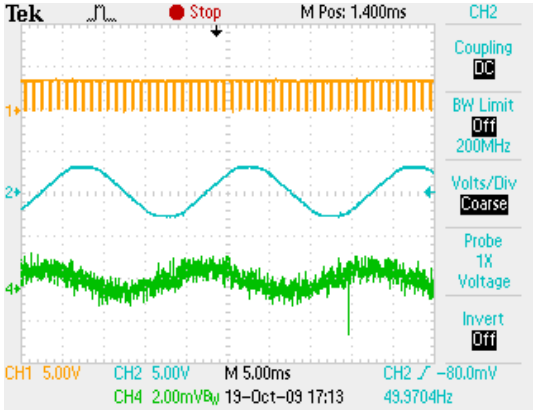
M 5.00ms
CH2 ∕ −80.0mV
CH4 2.00mVBW 19-Oct-09 16:38
49.9434Hz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Volts/Div
Coarse
Probe
1X
Voltage
Invert
Off
CH1 5.00V
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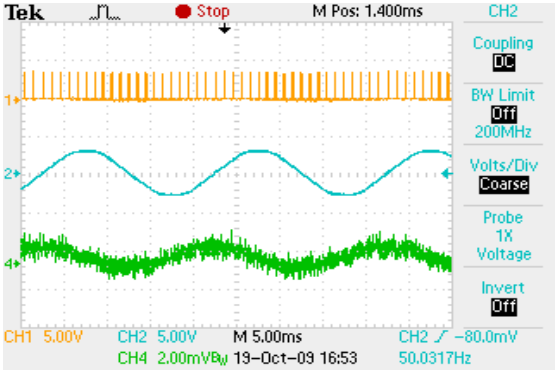
M 5.00ms
CH2 ∕ −80.0mV
CH4 2.00mVBW 19-Oct-09 17:13
49.9704Hz

0.9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200MHz
Volts/Div
Coarse
Probe
1X
Voltage
Invert
Off
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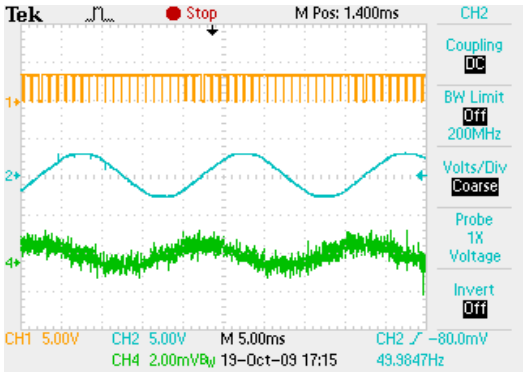
M 5.00ms
CH2 ∕ −80.0mV
CH4 2.00mVBW
19-Oct-09 16:53
50.0317Hz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DC
BW Limit
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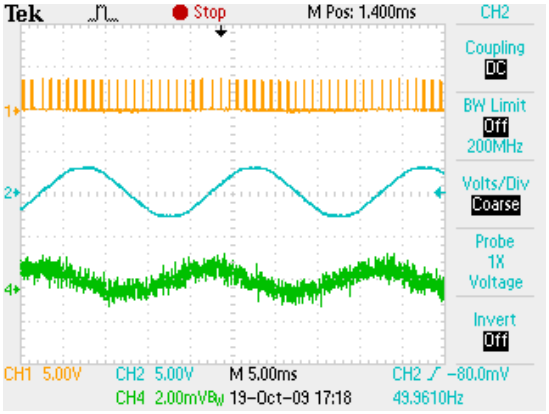
200MHz
Volts/Div
Coarse
Probe
1X
Voltage
Invert
Off
CH1 5.00V
CH2 5.00V
M 5.00ms
CH2 ∕ −80.0mV
CH4 2.00mVBW
19-Oct-09 17:15
49.9847Hz

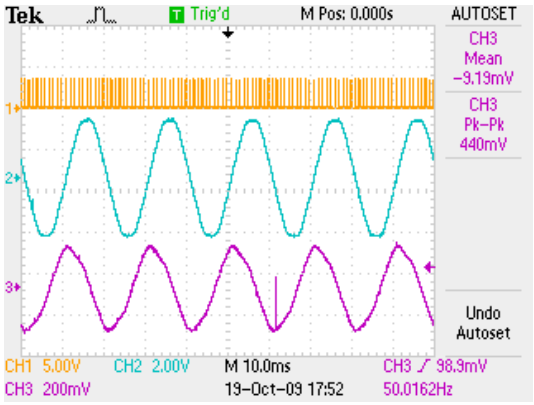
λ

Gama(γ) (0.3)

Gama(γ) (0.4)

0.1





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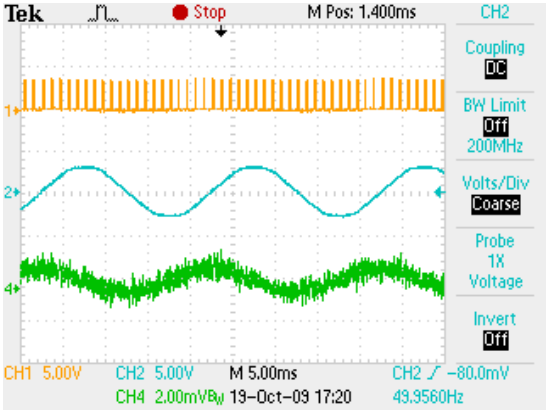

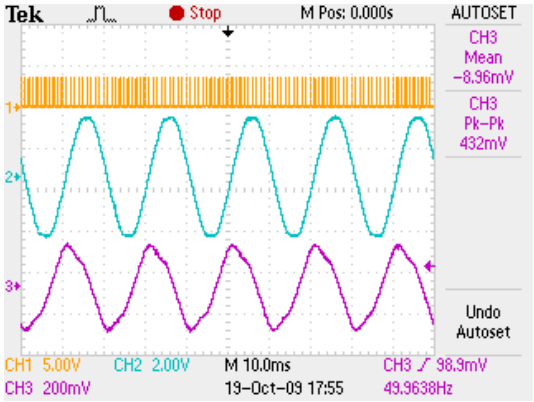

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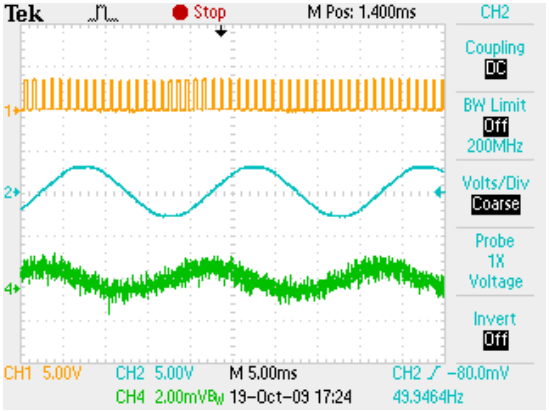

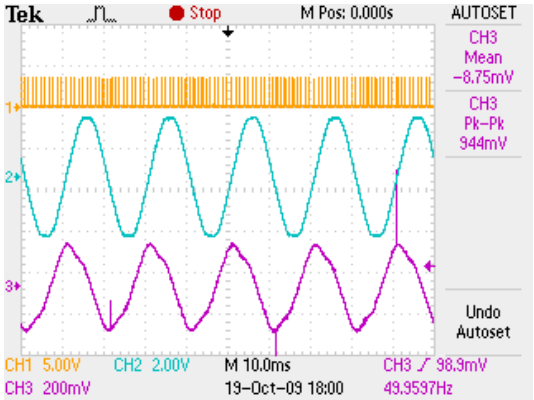

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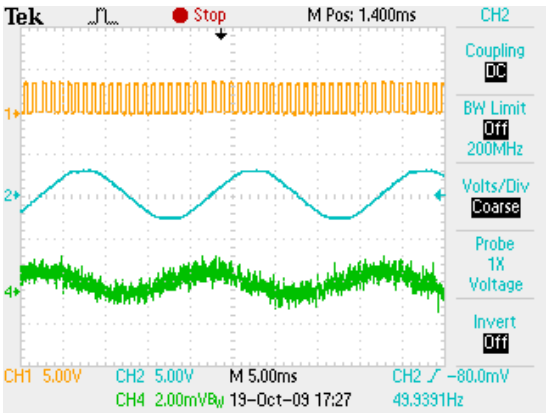
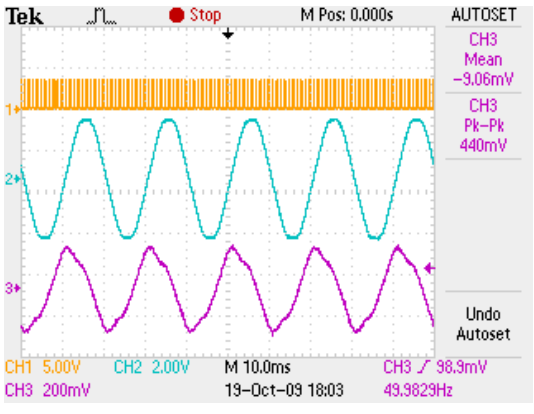
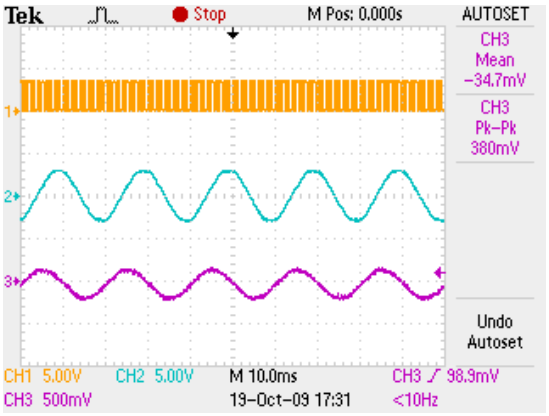




0.5


Tek
Stop
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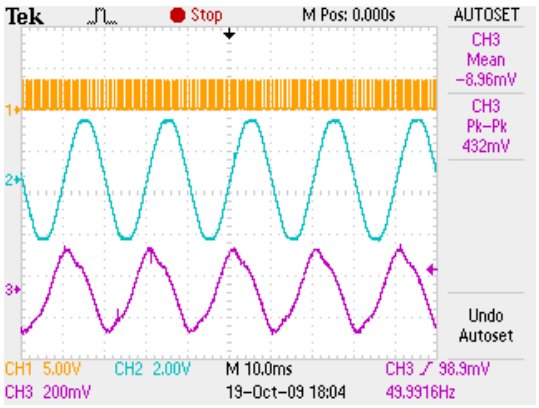
AUTOSET
CH3
Mean
−34.7mV
CH3
Pk−Pk
380mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 500mV
19−Oct−09 17:31
<10Hz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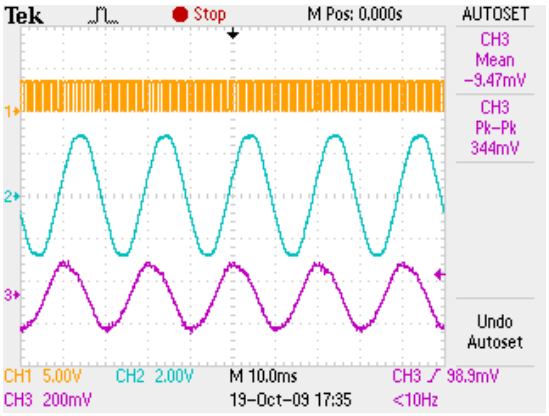
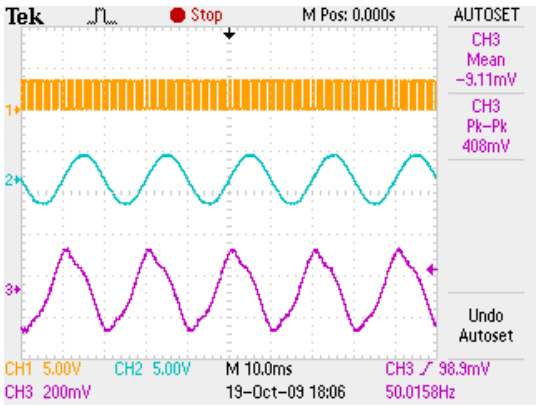
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−8.96mV
CH3
Pk−Pk
432mV
Undo
Autoset
CH1 5.00V
CH2 2.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 200mV
19−Oct−09 18:04
49.3916Hz

0.6


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−9.47mV
CH3
Pk−Pk
344mV
Undo
Autoset
CH1 5.00V
CH2 2.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 200mV
19−Oct−09 17:35
<10Hz


Tek
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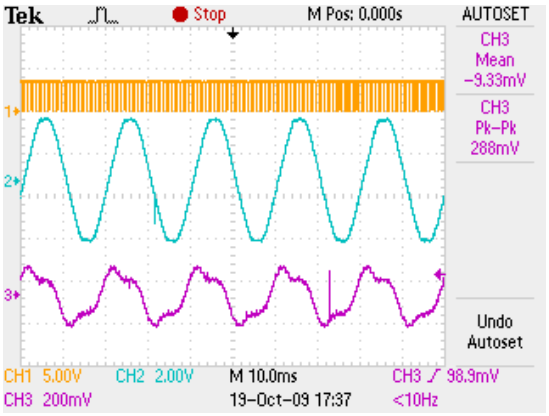
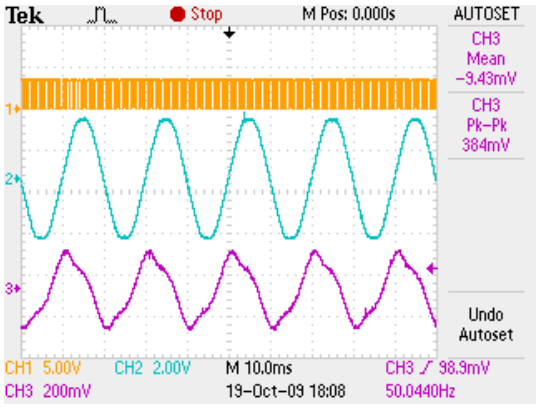
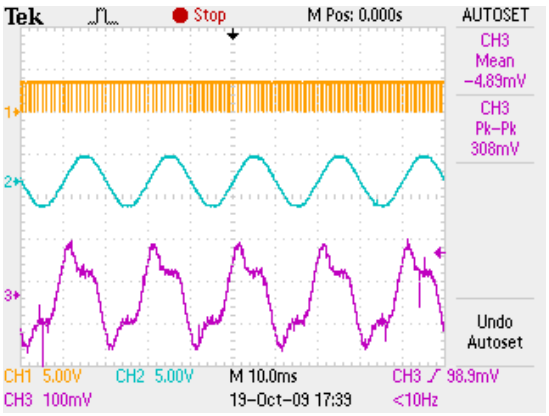
M Pos: 0.000s
AUTOSET
CH3
Mean
−9.11mV
CH3
Pk−Pk
408mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 200mV
19−Oct−09 18:06
50.0158Hz

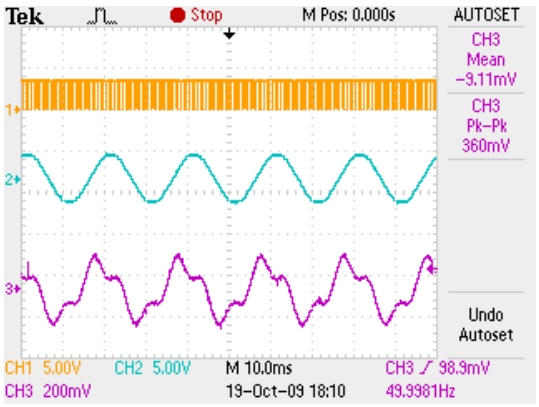
0.7


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−9.33mV
CH3
Pk−Pk
288mV
Undo
Autoset
CH1 5.00V
CH2 2.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 200mV
19−Oct−09 17:37
<10Hz

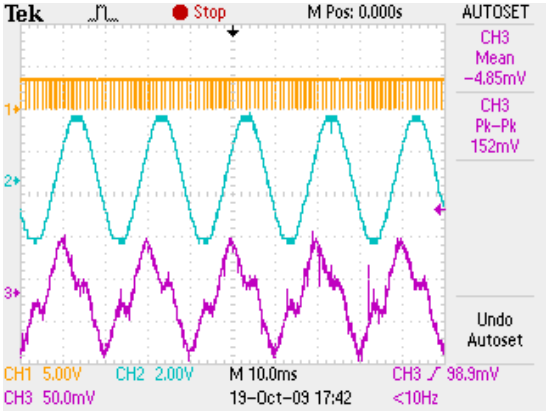

Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−9.43mV
CH3
Pk−Pk
384mV
Undo
Autoset
CH1 5.00V
CH2 2.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 200mV
19−Oct−09 18:08
50.0440Hz

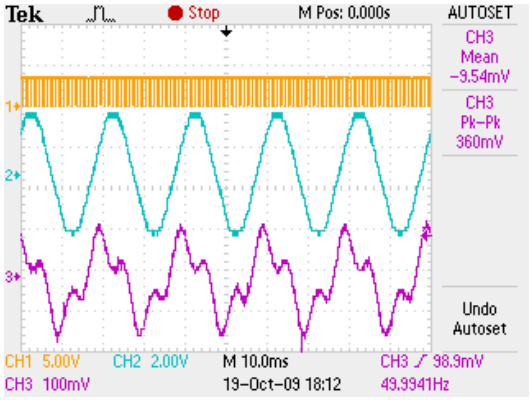
0.8

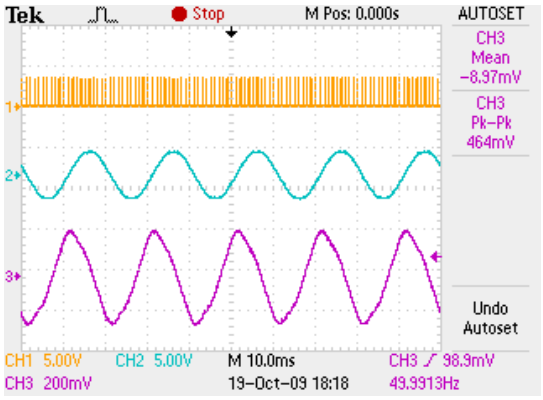
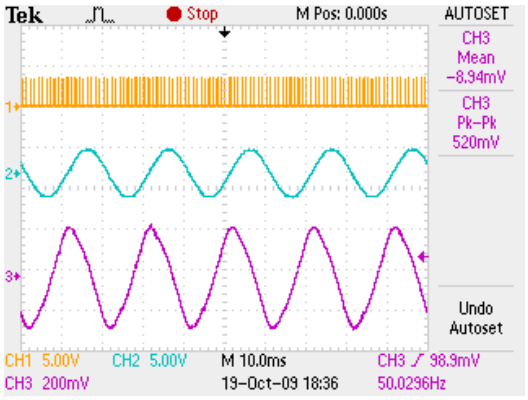
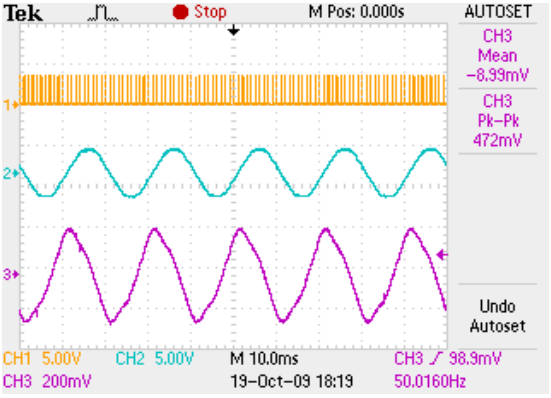
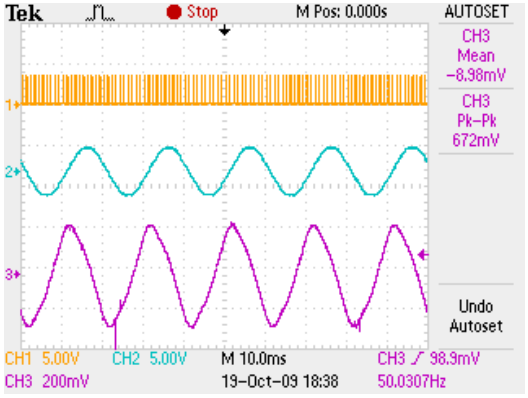
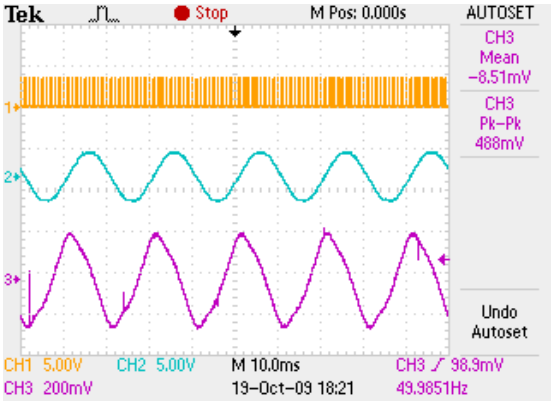
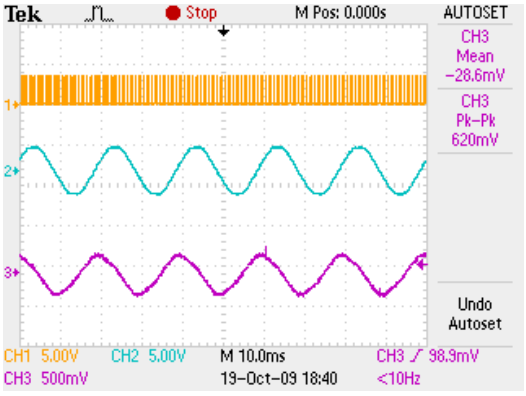
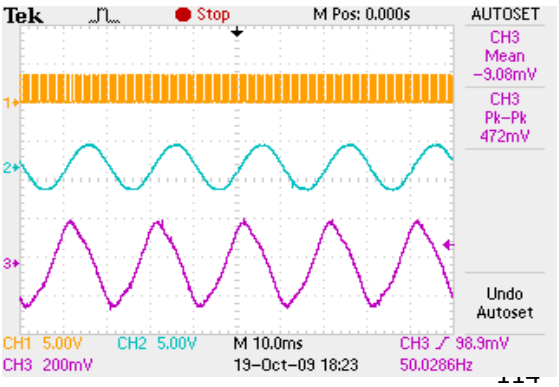
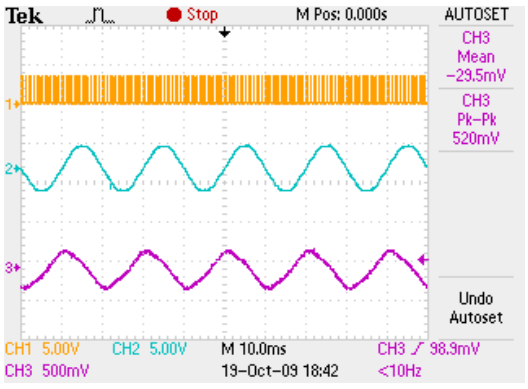

Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−4.89mV
CH3
Pk−Pk
308mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 100mV
19−Oct−09 17:39
<10Hz


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−9.11mV
CH3
Pk−Pk
360mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 200mV
19−Oct−09 18:10
49.9381Hz

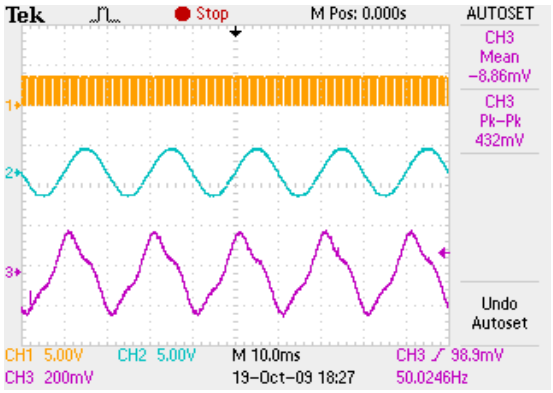
0.9

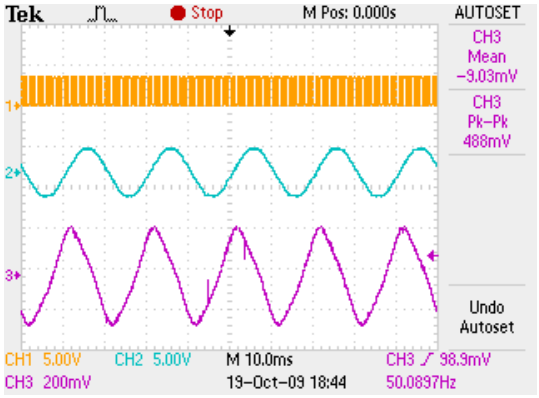

Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−4.85mV
CH3
Pk−Pk
152mV
Undo
Autoset
CH1 5.00V
CH2 2.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 50.0mV
19−Oct−09 17:42
<10Hz


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−9.54mV
CH3
Pk−Pk
360mV
Undo
Autoset
CH1 5.00V
CH2 2.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 100mV
19−Oct−09 18:12
49.9941Hz

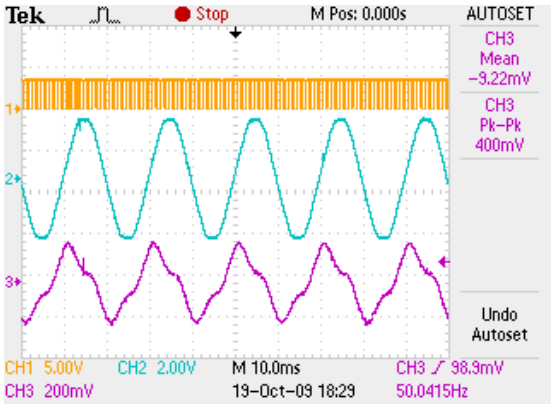
λ	Gama($\gamma = (C1/C2)$ (0.5)	Gama($\gamma = 0.6$
0.1		
0.2		
0.3		
0.4		

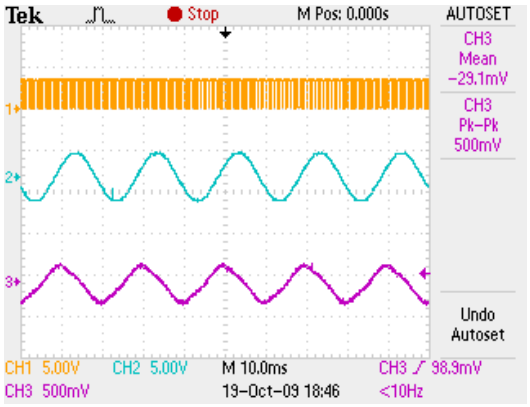
0.5


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−8.86mV
CH3
Pk−Pk
432mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 200mV
19−Oct−09 18:27
50.0246Hz

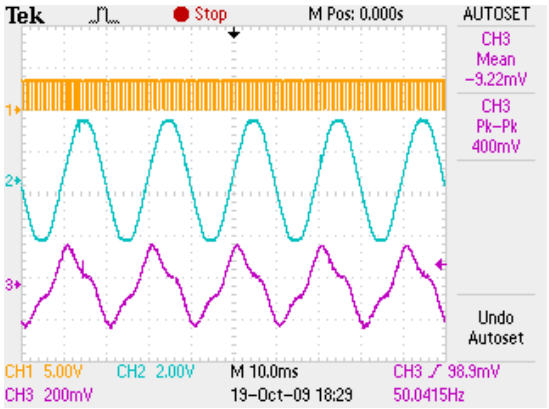

Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−9.03mV
CH3
Pk−Pk
488mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 200mV
19−Oct−09 18:44
50.0897Hz

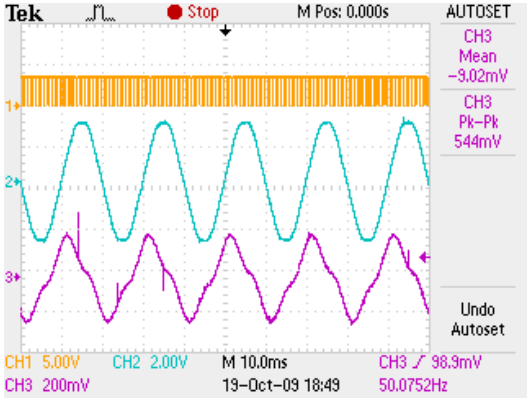
0.6


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−9.22mV
CH3
Pk−Pk
400mV
Undo
Autoset
CH1 5.00V
CH2 2.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 200mV
19−Oct−09 18:29
50.0415Hz

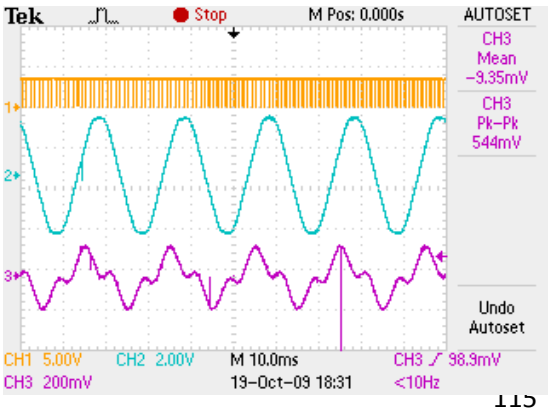

Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−29.1mV
CH3
Pk−Pk
500mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 500mV
19−Oct−09 18:46
<10Hz

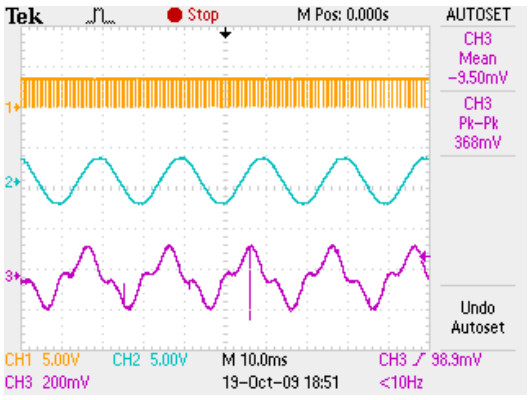
0.7


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−9.22mV
CH3
Pk−Pk
400mV
Undo
Autoset
CH1 5.00V
CH2 2.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 200mV
19−Oct−09 18:29
50.0415Hz

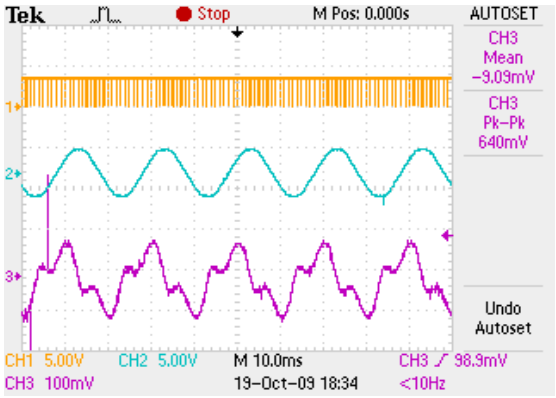

Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−9.02mV
CH3
Pk−Pk
544mV
Undo
Autoset
CH1 5.00V
CH2 2.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 200mV
19−Oct−09 18:49
50.0752Hz

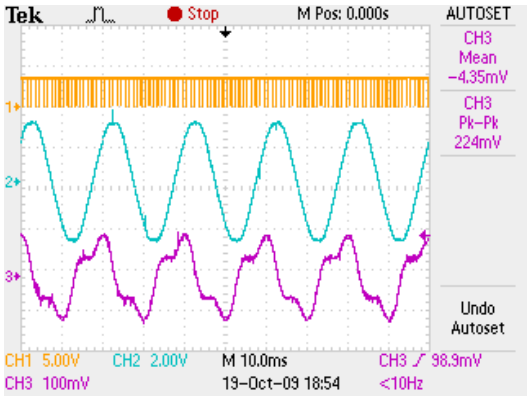
0.8

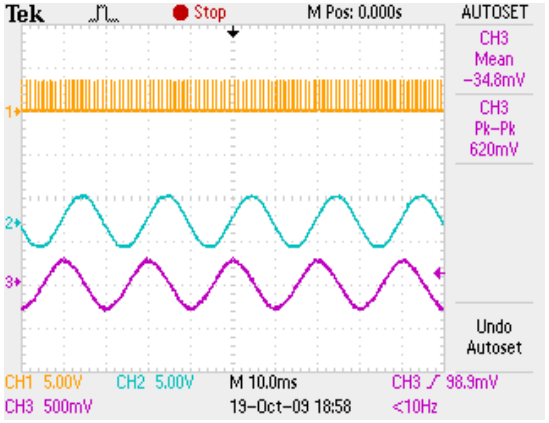
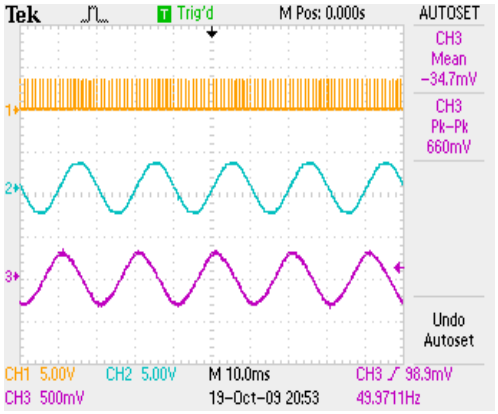
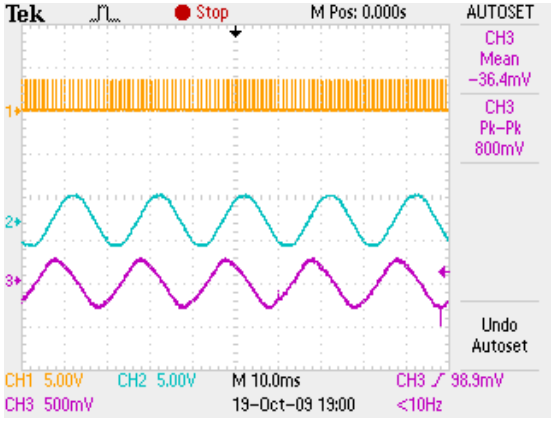
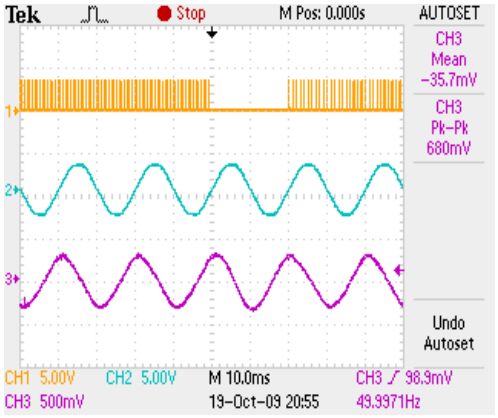
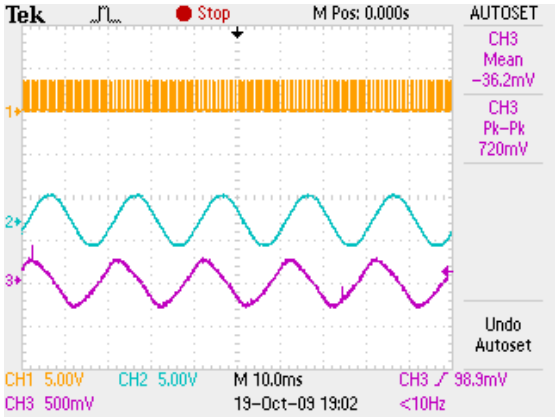
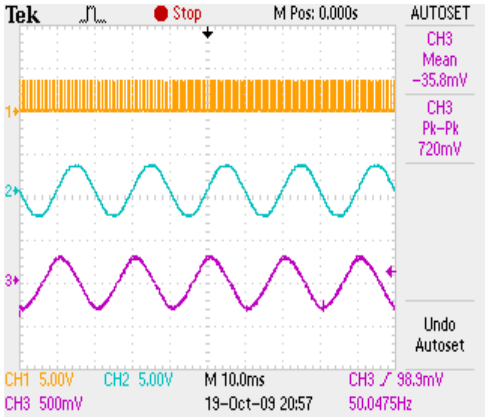
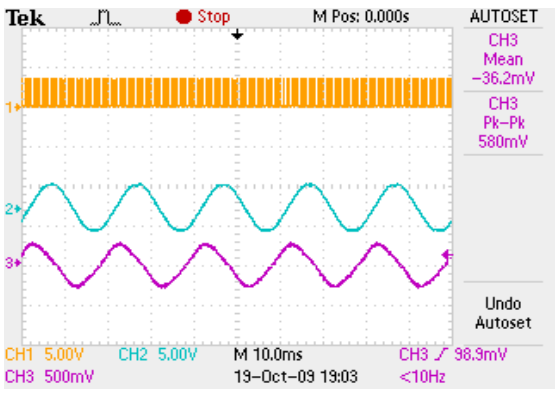
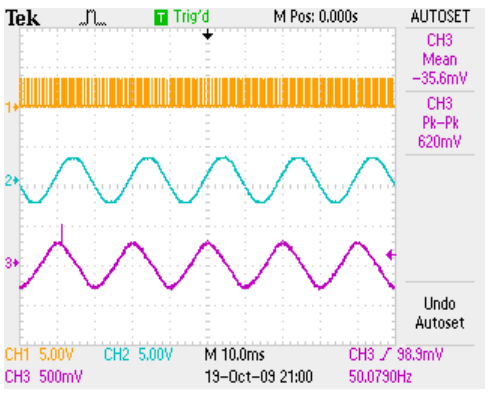

Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−9.35mV
CH3
Pk−Pk
544mV
Undo
Autoset
CH1 5.00V
CH2 2.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 200mV
19−Oct−09 18:31
<10Hz


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−9.50mV
CH3
Pk−Pk
368mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 200mV
19−Oct−09 18:51
<10Hz

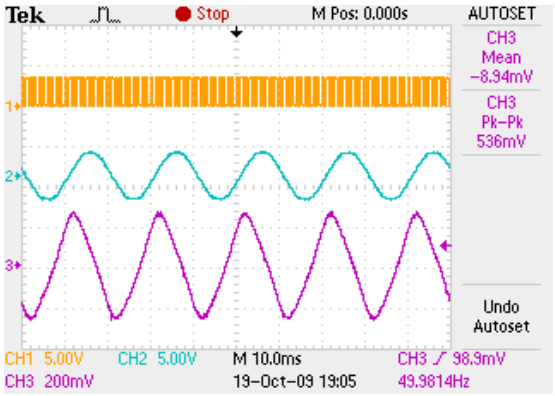
0.9

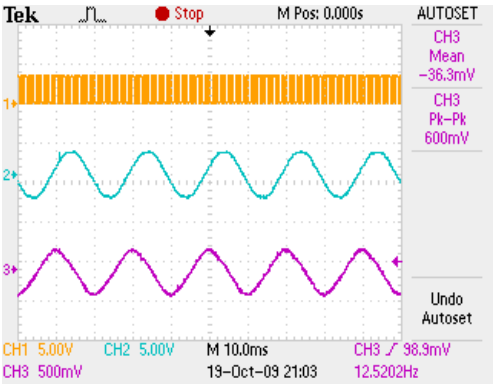

Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−9.09mV
CH3
Pk−Pk
640mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 100mV
19−Oct−09 18:34
<10Hz


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−4.35mV
CH3
Pk−Pk
224mV
Undo
Autoset
CH1 5.00V
CH2 2.00V
M 10.0ms
CH3 ⁄ 98.9mV
CH3 100mV
19−Oct−09 18:54
<10Hz

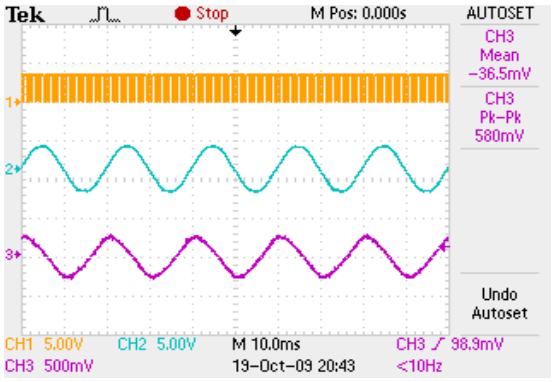
λ	Gama(γ) (0.7)	Gama(γ) (0.8)
0.1		
0.2		
0.3		
0.4		

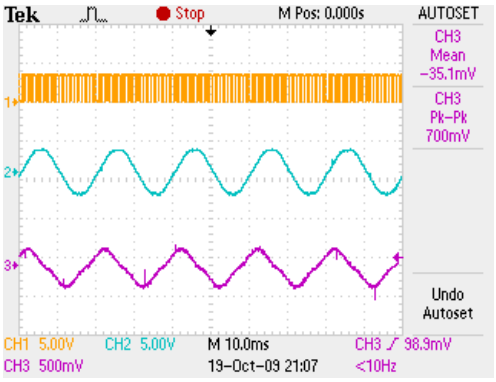
0.5


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−8.94mV
CH3
Pk-Pk
536mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 200mV
19-Oct-09 19:05
49.9814Hz

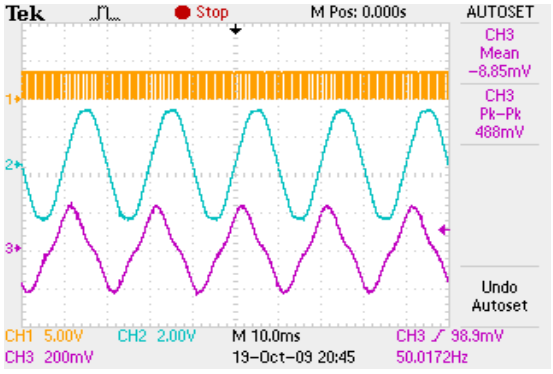

Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−36.3mV
CH3
Pk-Pk
600mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 500mV
19-Oct-09 21:03
12.5202Hz

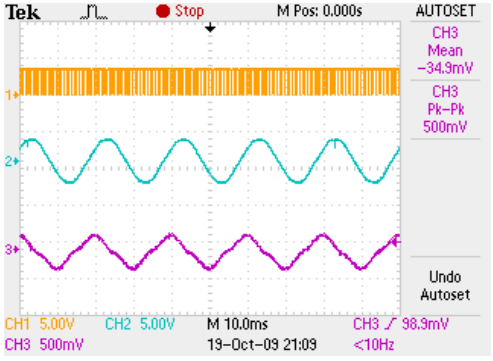
0.6


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−36.5mV
CH3
Pk-Pk
580mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 500mV
19-Oct-09 20:43
<10Hz

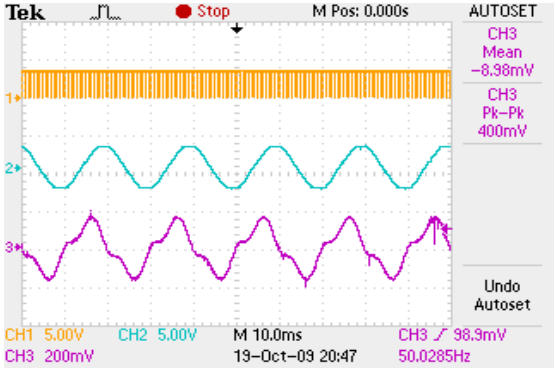

Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−35.1mV
CH3
Pk-Pk
700mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 500mV
19-Oct-09 21:07
<10Hz

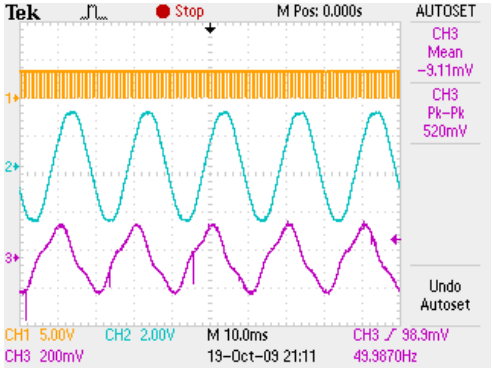
0.7


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−8.85mV
CH3
Pk-Pk
488mV
Undo
Autoset
CH1 5.00V
CH2 2.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 200mV
19-Oct-09 20:45
50.0172Hz

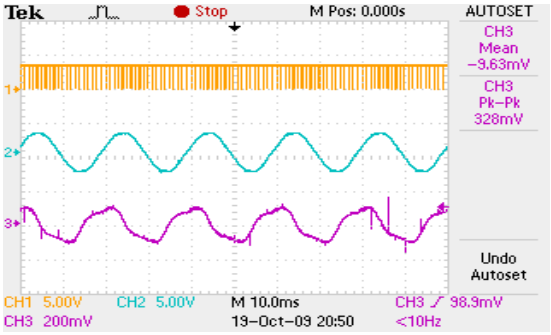

Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−34.9mV
CH3
Pk-Pk
500mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 500mV
19-Oct-09 21:09
<10Hz

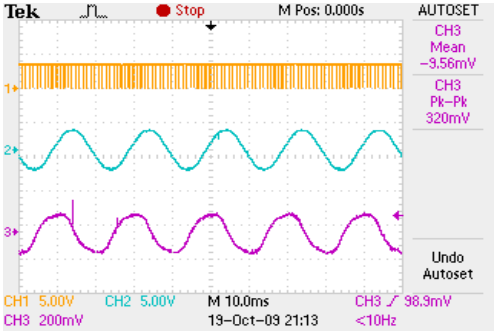
0.8


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−8.98mV
CH3
Pk-Pk
400mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 200mV
19-Oct-09 20:47
50.0285Hz


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−9.11mV
CH3
Pk-Pk
520mV
Undo
Autoset
CH1 5.00V
CH2 2.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 200mV
19-Oct-09 21:11
49.9870Hz

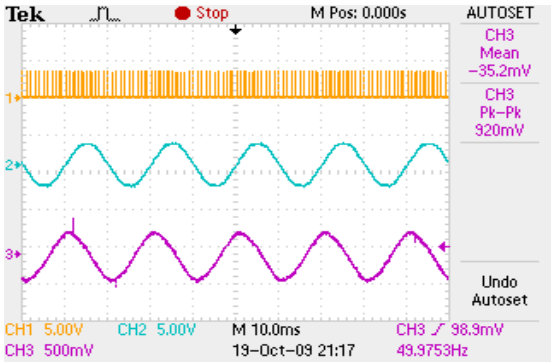
0.9

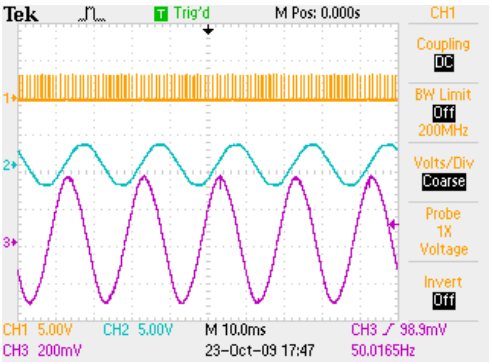

Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−3.63mV
CH3
Pk−Pk
328mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 200mV
19−Oct−09 20:50
<10Hz


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−9.56mV
CH3
Pk−Pk
320mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 200mV
19−Oct−09 21:13
<10Hz

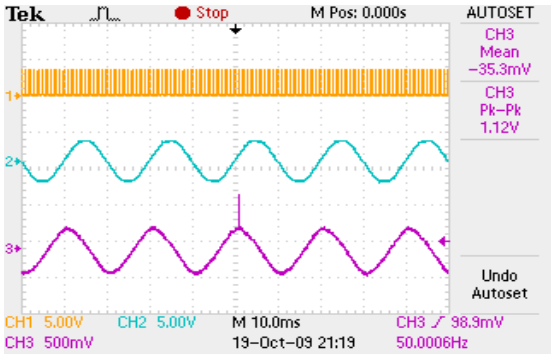
λ Gama(γ) (0.9) Gama(γ) (1)

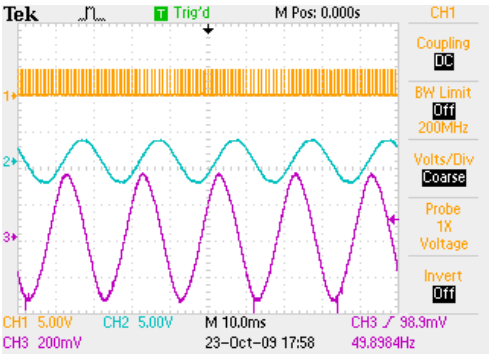
0.1



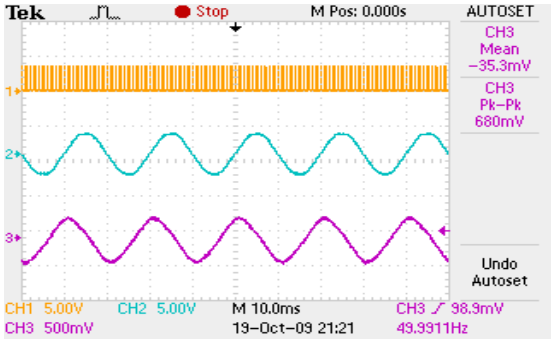


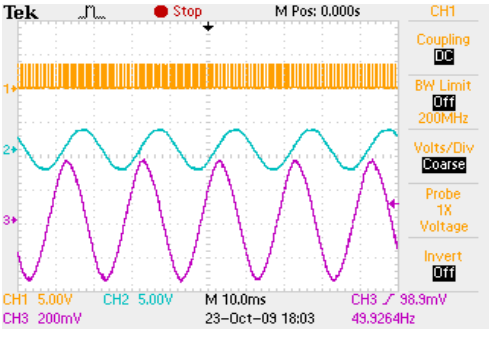
0.2



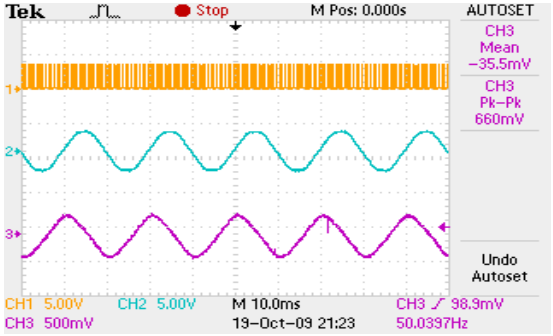


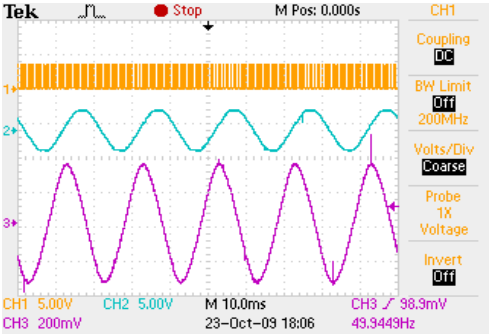
0.3



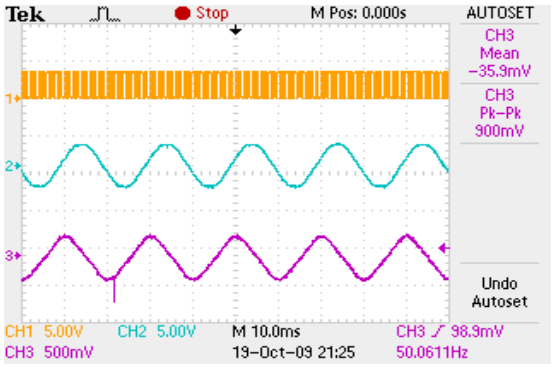


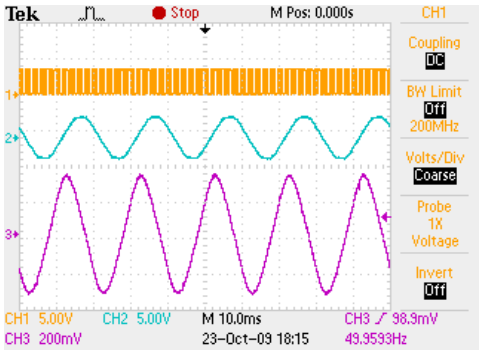
0.4



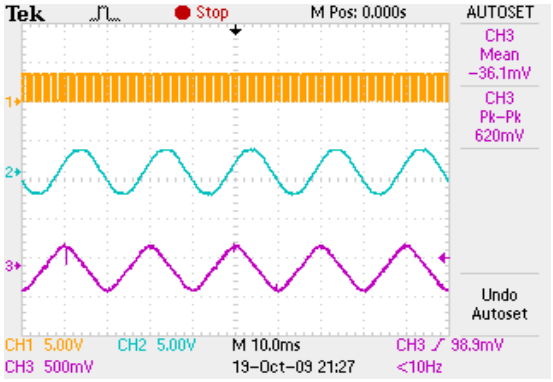


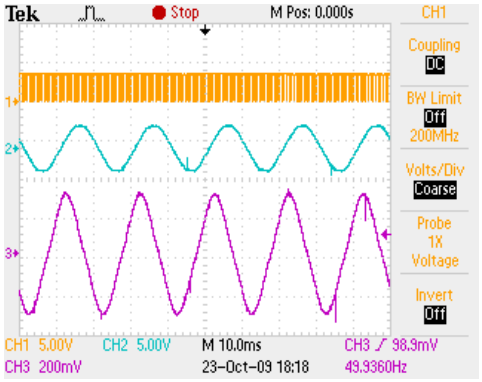
0.5


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−35.9mV
CH3
Pk-Pk
900mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 500mV
19-Oct-09 21:25
50.0611Hz

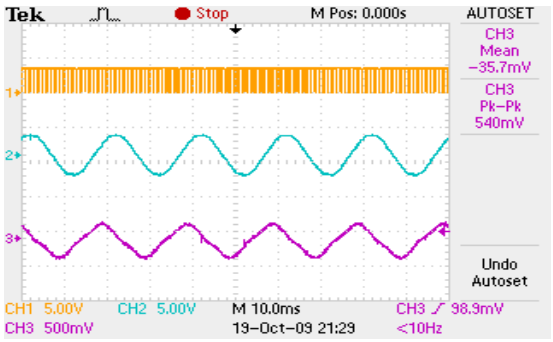

Tek
Stop
M Pos: 0.000s
CH1
Coupling
DC
BW Limit
Off
200MHz
Volts/Div
Coarse
Probe
1X
Voltage
Invert
Off
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 200mV
23-Oct-09 18:15
49.9593Hz

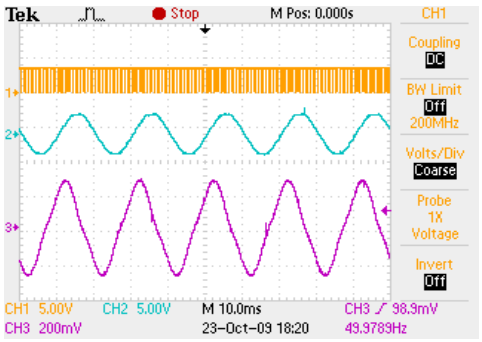
0.6


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−36.1mV
CH3
Pk-Pk
620mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 500mV
19-Oct-09 21:27
<10Hz

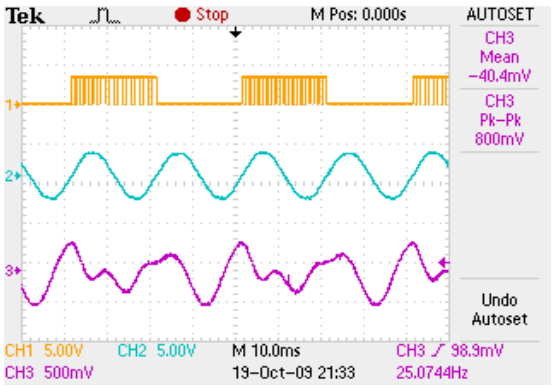

Tek
Stop
M Pos: 0.000s
CH1
Coupling
DC
BW Limit
Off
200MHz
Volts/Div
Coarse
Probe
1X
Voltage
Invert
Off
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 200mV
23-Oct-09 18:18
49.9360Hz

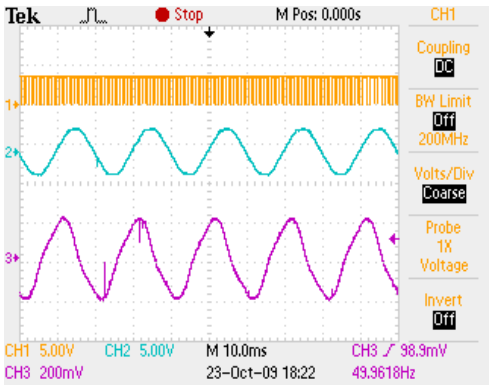
0.7


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−35.7mV
CH3
Pk-Pk
540mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 500mV
19-Oct-09 21:29
<10Hz

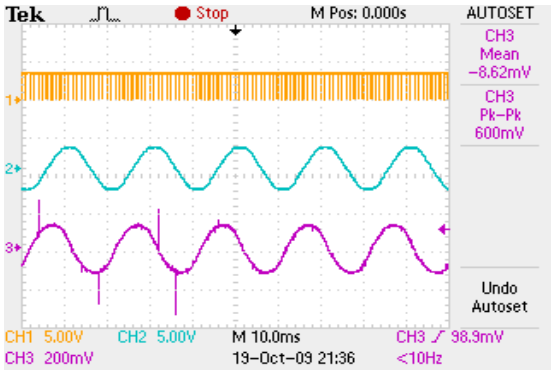

Tek
Stop
M Pos: 0.000s
CH1
Coupling
DC
BW Limit
Off
200MHz
Volts/Div
Coarse
Probe
1X
Voltage
Invert
Off
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 200mV
23-Oct-09 18:20
49.9789Hz

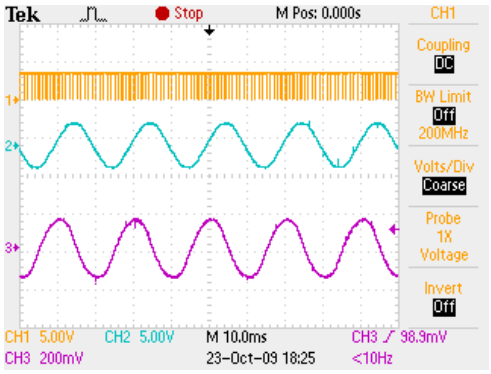
0.8


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−40.4mV
CH3
Pk-Pk
800mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 500mV
19-Oct-09 21:33
25.0744Hz


Tek
Stop
M Pos: 0.000s
CH1
Coupling
DC
BW Limit
Off
200MHz
Volts/Div
Coarse
Probe
1X
Voltage
Invert
Off
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 200mV
23-Oct-09 18:22
49.9618Hz

0.9


Tek
Stop
M Pos: 0.000s
AUTOSET
CH3
Mean
−8.62mV
CH3
Pk−Pk
600mV
Undo
Autoset
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 200mV
19−Oct−09 21:36
<10Hz


Tek
Stop
M Pos: 0.000s
CH1
Coupling
DC
BW Limit
Off
200MHz
Volts/Div
Coarse
Probe
1X
Voltage
Invert
Off
CH1 5.00V
CH2 5.00V
M 10.0ms
CH3 ⁄ 38.9mV
CH3 200mV
23−Oct−09 18:25
<10Hz