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High Total Ionizing Dose and Temperature Effects on Micro- and Nano-Electronic Devices

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***Abstract*—This paper investigates the vulnerability of several micro- and nano-electronic technologies to a mixed harsh environment involving high total ionizing dose at MGy levels and high temperature. Such operating conditions emerge today for several applications like new security systems in existing or future nuclear power plants, fusion experiments, or deep space missions. In this work, the competing effects of ionizing radiations and temperature are characterized in elementary devices made of MOS transistors from several technologies. First, devices are irradiated using a radiation laboratory X-ray source up to MGy dose levels at room temperature. Devices are either grounded or biased during irradiation to simulate two major circuit cases: a circuit which waits for a wake up signal, representing most of the lifetime of an integrated circuit operating in a harsh environment, and a nominal circuit function. Devices are then annealed at several temperatures to discuss the post-irradiation behavior and to determine whether an elevated temperature is an issue or not for circuit function in mixed harsh environments.**

***Index Terms*—Annealing, bulk silicon, fully depleted (FD), high temperature, MGy irradiation, partially depleted (PD), silicon on insulator (SOI), total ionizing dose (TID).**

I. Introduction

ELECTRONIC systems designed for harsh environments are used in various applications, such as high energy physics instruments, fusion reactors or space missions. Since recent events which occur in Fukushima Daichii, they have been pointed out as critical issues for safety systems in nuclear facilities, when used to monitor parameters such as ionizing radiation level, temperature or pressure levels either in the nuclear core or in the spent-fuel pools of nuclear power plants [1]. Radiation tolerant electronic components dedicated to other applications like space exist [2], [3]. They are designed to meet the specifications required for the targeted environment, which commonly implies lower Total Ionizing Dose (TID) levels than those encountered by electronic components in the case of an accident in nuclear power plant. For instance, most space missions consider that devices and Integrated Circuits (ICs) have to withstand less than 1 kGy while electronic systems in nuclear power plants have to be hardened up to several MGy ionizing doses. Specific studies should thus be performed to identify technologies which may present enough hardening potential to meet such requirements. Only few papers have been dedicated to high TID effects in electronic devices [4], [5], [6], [7]. Most of them discussed the hardening level of either bulk or SOI technologies in the frame of the Large Hadron Collider using dedicated test structures. More recently, a review of the MGy dose effects induced in a wide range of modern and innovative technologies including bulk, Partially Depleted (PD) Silicon On Insulator (SOI), Fully Depleted (FD) SOI and FinFET structures has been presented [8].

This paper being more focused on nuclear facilities, it considers both high TID and high temperatures occurring in nominal and accidental conditions. Few papers have already addressed such mixed temperature and irradiation issues but considering ionizing doses of about few Mrads [9], [10], [11], two orders of magnitude lower than recent requirements specified for nuclear power plants particularly in accidental conditions. To the authors' knowledge, the combination of MGy irradiation and elevated temperature is considered as the most constraining scenario for accidental conditions. Test standards [12], [13] to qualify equipments designed for such an environment thus recommend performing a two-step experimental procedure, the first one being devoted to irradiations up to MGy doses, followed by a thermodynamic test. The main issue discussed in this paper is to determine how the temperature affects the TID response of elementary test structures fabricated in various technologies.

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II. Experimental Details

A. Devices

Three different technologies are studied in this paper to estimate their relative strengths and weaknesses in high TID and temperature environments:

— 0.18 μm*conventional bulk* I/O technology featuring Metal-Oxide-Semiconductor (MOS) transistors designed either with a standard Open Layout (OLT) or an Enclosed

TABLE I
NOMINAL VOLTAGE VS TECHNOLOGY

Technology	I/O Bulk 0.18 µm	PDSOI 0.13 µm	FDSOI 20 nm
Nominal Voltage	3.3V	1.2 V	0.9 V

Layout (ELT). The nominal voltage of the technology is 3.3 V.

— *130 nm PDSOI* technology featuring MOS transistors processed on a SOI substrate with two designs: standard Floating Body (FB) and Body Contacted (BC) devices. The silicon film thickness is enough to prevent coupling effects [14] occurring in the following FDSOI technology. The nominal voltage of the technology is 1.2 V.

— 20 nm *FDSOI* technology featuring open layout transistors. One characteristic of this technology is that devices and ICs can be processed on different base SOI substrates. The silicon film thickness, the front-end and the back-end of line processes are similar in all cases, but such ICs can be fabricated on SOI substrates with various Buried OXide (BOX) thicknesses T_{BOX} = 145 nm, 25 nm or 11 nm. This may affect the FDSOI device response to MGy dose levels since it was already demonstrated to significantly modify the TID response of such integrated devices at 10kGy [15].

Table I summarizes the nominal voltages used for each technology.

All devices are mounted in standard Dual-In Line packages for both irradiation and temperature experiments.

B. Irradiation and Annealing Tests Description

First, devices are irradiated using a 10 keV X-ray laboratory source at a constant dose rate of 50 Gy/s. The TID is deposited in several steps up to a maximum of 1 MGy. Electrical measurements are performed at each TID step. Static drain-current I_D vs gate-voltage V_{GS} electrical characteristics are measured with a HP 4145 parametric analyzer through a Keithley 707 switching matrix. All parameter extractions presented in this paper come from these static measurements including the threshold voltage V_{TH}, the subthreshold slope S^{-1}, the transconductance g_m, the drive current I_{ON} (I_D at $V_{GS} = V_{DS} = V_{DD}$) and the leakage current I_{OFF} (I_D at $V_{GS} = 0$ V and $V_{DS} = V_{DD}$).

Devices are either grounded or biased during irradiation. In the following, these two bias configurations are referred as the NULL-case and OFF-case respectively. In the NULL-case, all terminals are grounded. The device can thus be considered in a stand-by mode signal. In contrast, it is in its nominal bias configuration when the device is biased during irradiation such as in the OFF-state. In this bias case, only the drain electrode is biased to the nominal voltage of the technology $V_D = V_{DD}$ when other terminals are grounded. These two configurations aim at representing most of the device functions to simulate the main profile of use of electronic devices in such harsh operating conditions, especially in accidental conditions, for which an IC is most of the time in a stand-by mode.

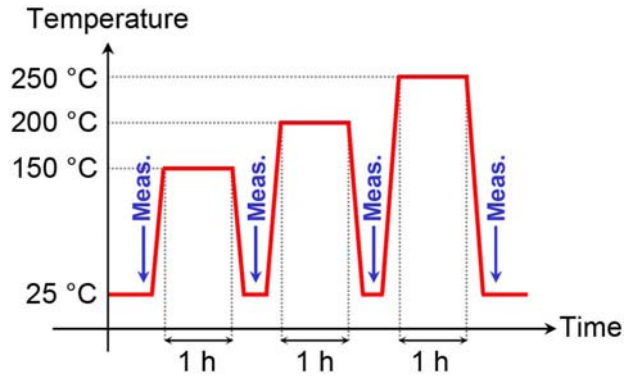

Fig. 1. Schematic of annealing steps performed during experiments. Electrical measurements are performed at room temperature between each temperature step.

Then, isochronal annealing experiments are performed using a dedicated setup to investigate the effect of temperature. Three annealing steps are done at 150°C, 200°C and 250°C, each of them during 1 hour. Electrical measurements are always performed at room temperature. A simple schematic of the annealing steps is plotted in Fig. 1. The experimental setup is optimized to reduce to only few minutes the rise time and the fall time between each temperature steps.

The first annealing step (1 hour, 150°C) is done to be consistent with requirements described in standards for test of in-containment instrumentation in accidental conditions [12], [13]. The two others are performed to get additional insights on temperature effects induced in highly irradiated silicon-based devices and to discuss the phenomena at stake in a wider range of operations.

III. MGY DOSE SENSITIVITY OF SI-BASED TECHNOLOGIES

Two major TID induced effects in MOS devices are reported in the literature [16], [17], [18]: on the one hand the trapping of radiation-induced generated charges in the oxide bulk, and on the other hand the generation of interface traps at silicon-dielectric interfaces. Physical mechanisms leading to oxide-charge trapping and interface traps generation are widely studied since it is needed to mitigate their effects on electronic device characteristics. Their respective contributions are usually estimated using the charge separation technique described in [19] which allows to attribute a voltage, either V_{OT} or V_{IT}, and then a density N_{OT} or N_{IT} for oxide-trapped charge and interface traps respectively.

In most cases, radiation-induced trapped charges are positive in MOS devices. It leads to the modification of electrical characteristics of electronic devices and ICs depending on their technology, architecture, fabrication process and geometry. This may shift the electrical characteristics I-V of MOS transistors when the total amount of trapped charge is enough to change the electrostatic potential in the active silicon layer. All main electrical parameters (V_{TH}, I_{ON} and I_{OFF}) can thus be modified due to ionizing radiation. Furthermore, oxide-trapped charges can also trigger uncontrolled parasitic conduction paths such as parasitic lateral transistors due to trapping in field oxides [20], enhanced narrow channel effects [7], [21] or parasitic back transistors in SOI technologies [22]. This could also shift the main

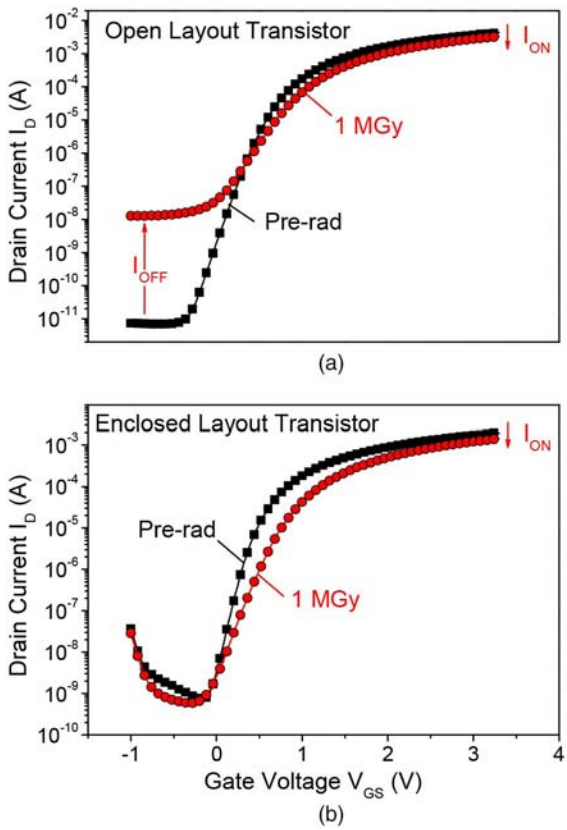

Fig. 2. Drain current I_D vs gate voltage V_{GS} characteristics of two bulk NMOS transistors: an Open Layout Transistor (OLT, top, a) and an Enclosed Layout Transistor (ELT, bottom, b) before irradiation (black squares) and after 1 MGy (red circles). Transistors are grounded during irradiation.

electrical characteristics of FDSOI devices due to both charge trapping into the BOX and coupling effects inherent to this specific SOI technology [14], [15], [23], [24], [25].

In contrast, interface traps are either negative or positive in NMOS or PMOS transistors respectively. In both cases, they degrade the subthreshold slope S^{-1} of I-V characteristics.

A. Bulk Technology

The TID behavior of I/O transistors fabricated using a standard 0.18 μm bulk technology is investigated as in [21]. Fig. 2 shows the $I_D - V_{GS}$ characteristics obtained on a standard Open Layout Transistor (OLT) with a wide design (transistor width $W = 10$ μm and gate length $L_G = 0.34$ μm) from pre-rad (black squares) up to 1 MGy (red circles). It highlights the most relevant parameters which will be used in the following of this study.

The open layout transistor (Fig. 2(a)) exhibits a significant increase of the leakage current I_{OFF}; this is due to the buildup of oxide-trapped charge in field oxides which triggers the parasitic lateral conduction [20]. By contrast and as expected, no significant shift of the threshold voltage ΔV_{TH} is observed, meaning that Radiation-Induced Narrow Channel Effect (RINCE) [7], [21] does not occur in the wide OLT (Fig. 2(a)). Even so, radiation-induced effects occur at MGy dose levels despite the fact that devices are grounded during irradiation. The device response is less impacted than when devices are biased during

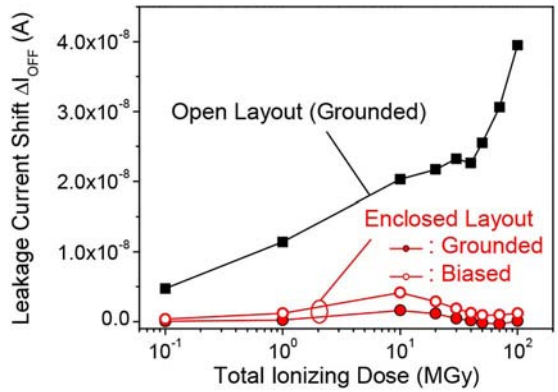

Fig. 3. Leakage current shifts ΔI_{OFF} vs TID in Open Layout Transistors (OLT, black squares) and Enclosed Layout Transistors either grounded (ELT, filled red circles) or biased (ELT, open red circles) during irradiation.

irradiation [8] but the effect remains significant. Using an enclosed geometry [7] in the transistors' design (ELT, Fig. 2(b)) strongly mitigates these effects since oxide-charge trapping only occurs in the thin gate oxide. In that case, $I_D - V_{GS}$ characteristics are mostly changed due to the buildup of interface traps, which only degrades the subthreshold slope and then the drive current I_{ON}.

Fig. 3 summarizes the leakage current increase with TID measured on bulk devices. As expected, the ELT (red circles) presents high TID tolerance with very limited modifications of its electrical characteristics; devices being grounded (filled red circles) or biased (open red circles) during irradiation. This geometry features no interface between active silicon and thick field oxides which intrinsically removes the parasitic lateral conduction leading to the observed I_{OFF} increase on the OLT (black squares). Using ELT also mitigates the RINCE which can occur in narrow transistors.

In the same time, Fig. 2 shows that the drive current I_{ON} decreases by about 30% at 1 MGy in both the OLT and the ELT. This significant lowering of the drive-current with TID must be considered in the circuit design to get margins enough to prevent circuit failure due to the lowest drivability obtained after irradiation. Actually, the circuit won't be able to operate in nominal conditions: a slower speed than the nominal one should be used to ensure reliable circuit functions.

From the circuit design's standpoint, the main drawback remains the significant area penalty induced by this hardening by design technique for both PMOS and NMOS transistors.

B. Partially Depleted SOI Technology

PDSOI technologies have already demonstrated their capabilities to withstand MGy dose irradiations. In the late eighties, pioneering works performed by Leray *et al.* [4], [5], [6] demonstrated the hardening potential of SOI technologies to MGy dose levels for Large Hadron Collider applications. More recently, PDSOI devices designed with external body contacts exhibited a very promising tolerance to MGy dose [8] either grounded or biased during irradiation. In such devices, the buildup of oxide-trapped charge in the BOX induces a parasitic back conduction which increases the leakage current I_{OFF} for devices biased during irradiation. By contrast, it was demonstrated that

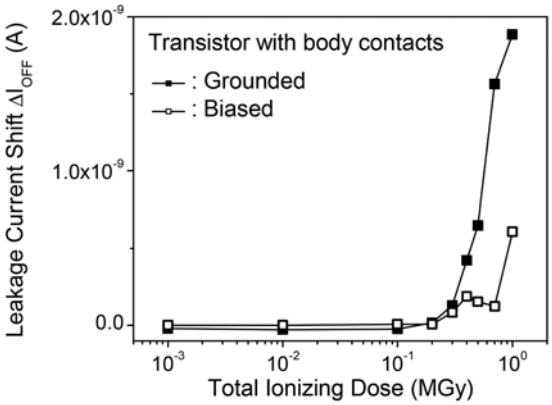

Fig. 4. Leakage current I_{OFF} shifts induced after 1 MGy on a Body Contacted transistor either grounded (filled squares) or biased (open squares) during irradiation.

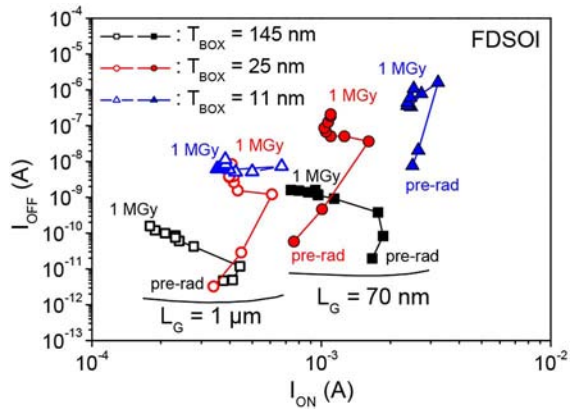

Fig. 5. $I_{ON} - I_{OFF}$ characteristics as a function of TID on FDSOI transistors processed on SOI substrates with a BOX thickness $T_{BOX} = 145$ nm (black squares), $T_{BOX} = 25$ nm (red circles) and $T_{BOX} = 11$ nm (blue triangles). Transistors with both a short gate length ($L_G = 70$ nm, filled symbols) and a long gate length ($L_G = 1\ \mu$m, open symbols) are plotted for each SOI substrate option. Devices are grounded during irradiation.

when devices are grounded during irradiation, the amount of trapped charge in the BOX is not enough to modify the electrical characteristics even after 3 MGy. This is confirmed by the parameter extractions plotted in Fig. 4 for body contacted devices only. Actually, all other electrical parameters are almost unaffected by TID.

The I_{OFF} current slightly increases from 0.3 MGy for devices grounded (filled squares) or biased (open squares). The leakage current shifts reach less than 2 nA at 1 MGy which stays within very low leakage current range. In this particular case, ΔI_{OFF} is larger when the device is grounded during irradiation than when it is OFF-biased. Actually, the OFF-case does not seem to be the worst case for such a device. Indeed, larger modifications have been presented in [8] for similar devices biased in the ON-state during irradiation (gate biased to the nominal voltage, other terminals grounded). However, one should note that the ΔI_{OFF} presented in Fig. 4 are still small despite the high TID value. Such a technology appears highly tolerant to TID all the more because the drive current I_{ON} stays within the same value (less than 2% change, not shown here, see Fig. 7 in Section III-D for more details) even after a 1 MGy irradiation.

By contrast, PDSOI transistors with a standard design without external body contacts, named as floating body transistors, behave in a different manner which will be close to the one of bulk transistors studied in the previous section. Floating body transistors feature interfaces between the active silicon and field isolations contrary to body contacted devices. Such devices then suffer from the inherent parasitic lateral conduction due to buildup of oxide-trapped charge in field oxides leading to potential additional I_{OFF} increase.

C. Fully Depleted SOI Technology

Finally, the FDSOI technology offers better scalability for nanometer scale era than both bulk and PDSOI technologies. This technology provides high performances, low power consumption and improved process variability [26], [27] which are all key issues for highly integrated technologies intended for commercial market. However, its TID sensitivity is strongly governed by oxide-charge trapping in the BOX which modifies the main electrical characteristics due to electrostatic coupling effects inherent to the FDSOI structure [14]. Some papers [15], [23], [24], [25] show that the TID sensitivity of FDSOI technologies is mainly driven by the body doping level, designed with or without body contacts, the gate length and above all the buried oxide thickness. All studies previously published were dedicated to TID below 10 kGy, so the following investigations will focus on the TID behavior of FDSOI transistors fabricated on various SOI substrates, i.e. various BOX thicknesses, at MGy dose levels. All devices were fabricated using a similar process leading to the same active silicon thickness, gate stack and doping levels. Their TID responses can thus be directly compared.

Fig. 5 summarizes the $I_{ON} - I_{OFF}$ characteristics of FDSOI devices on three different SOI substrates: $T_{BOX} = 145$ nm (black squares), $T_{BOX} = 25$ nm (red circles) and $T_{BOX} = 11$ nm (blue triangles). Results for transistors with both a short gate (filled symbols) and a long gate (open symbols) are displayed.

Short gate transistors all exhibit significant modifications of their electrical performances with TID. The drive currents I_{OFF} increase by several decades when I_{ON} almost decreases with TID, especially on the device with $T_{BOX} = 145$ nm (filled black squares). Decreasing the BOX thickness down to the thinnest value $T_{BOX} = 11$ nm enhances the TID tolerance by reducing the shifts reported both on I_{ON} and I_{OFF} compared to the other SOI substrate options. This is even more obvious on transistors with a long gate length ($L_G = 1\ \mu$m, open blue triangles). Only the drive current I_{ON} exhibits variations but with a leakage current I_{OFF} which stays within the same order of magnitude. Furthermore, results obtained on devices processed with Ultra-Thin BOX (UTB) substrates ($T_{BOX} = 25$ nm and 11 nm) are characteristic of their overall TID behavior since it was previously demonstrated that this behavior does not change with bias configuration during irradiation [15]. These promising results indicate that FDSOI devices may withstand high TID levels with appropriate substrate and design options, both if grounded or biased during irradiation. Obviously, standard thick BOX ($T_{BOX} = 145$ nm) devices do not present such characteristic, the NULL case being the one presenting

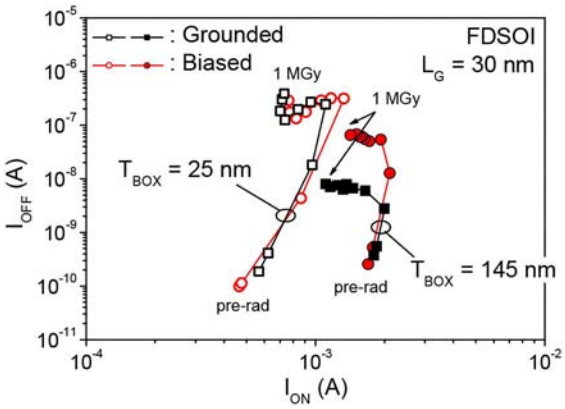

Fig. 6. $I_{ON} - I_{OFF}$ characteristics as a function of TID on FDSOI transistors processed on SOI substrates with a BOX thickness $T_{BOX} = 145$ nm (filled symbols) and $T_{BOX} = 25$ nm (open symbols), grounded (squares) or biased (circles) during irradiation. Transistors have an extremely short gate length $L_G = 30$ nm.

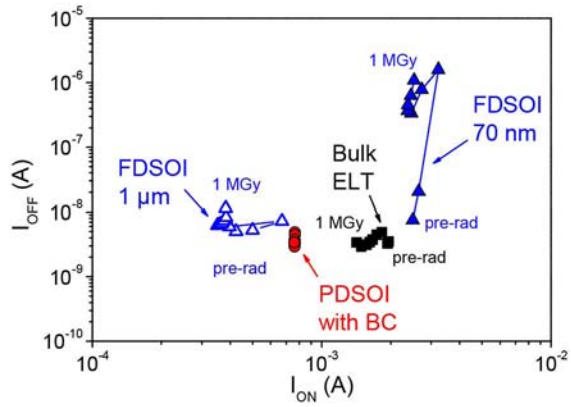

Fig. 7. $I_{ON} - I_{OFF}$ characteristics as a function of TID on FDSOI transistors for bulk (black squares), PDSOI (red circles) and FDSOI (blue triangles) technologies. Devices are grounded during irradiation.

the weakest TID induced modifications. So, the TID response of nanometer-scaled transistors with $L_G = 30$ nm either grounded (black squares) or biased (red circles) during irradiation processed on two different SOI substrates is presented in Fig. 6 within an I_{ON}vsI_{OFF} plot. Devices are fabricated on substrates with a BOX thickness of either $T_{BOX} = 145$ nm (filled symbols) or $T_{BOX} = 25$ nm (open symbols).

Fig. 6 clearly highlights the bias dependence of the FDSOI devices' TID response at MGy dose levels. Thick BOX devices (filled symbols) exhibit a clear bias dependence of their TID responses when the one of thin BOX devices (open symbols) is not anymore governed by the bias configuration during irradiation as already observed at lower TID in [15]. $I_{ON} - I_{OFF}$ characteristics of thick BOX devices ($T_{BOX} = 145$ nm) are clearly separated when measurements performed on transistors processed on the SOI substrate with $T_{BOX} = 25$ nm (open symbols) are nearly superimposed. Thin BOX devices present a significant increase of the leakage current I_{OFF} with TID, but their functionality do not suffer from any drive-current I_{ON} degradation. Fig. 6 basically shows the opposite behavior with an improvement of I_{ON} with TID which can be attributed to both the radiation-induced shift of the electrical characteristics and the stronger coupling effects with BOX thinning. This specific property may be beneficial to enhance the FDSOI devices' TID tolerance at MGy levels since the transistor drivability is not degraded contrary to what is observed on thick BOX devices. If the requirements needed by the final application can manage increase of the leakage current, thus of the power consumption, such technology may present interesting properties to operate in harsh environment with a reduced cost related to the design hardening.

D. Discussion on the Hardness Potential of Modern Technologies Submitted to High TID

All investigated technologies show TID behaviors directly linked to their architecture, fabrication process, design and geometry. However, using the appropriate design options allows enhancing their TID tolerance. Fig. 7 summarizes the $I_{ON} - I_{OFF}$ plots obtained on the most TID tolerant device for each studied technology: bulk (black squares), PDSOI (red circles) and FDSOI (blue triangles).

As a main conclusion, results presented in Fig. 7 show that all devices are still functional after a 1 MGy irradiation. Their electrical characteristics change with TID but in all cases they could be managed using the appropriate margins in the circuit design. The entire $I_{ON} - I_{OFF}$ characteristics must be considered, and not only the pre- and post-irradiation results, which do not necessarily give the largest TID-induced modifications. In the case of an accident in a nuclear facility, the choice of a technology will probably be driven by the circuit function and reliability rather than by its power consumption. Indeed, one may consider that in such environment, the power consumption of a stand alone circuit will not be the first critical parameter compared to its functionality and reliability. The requirements on the drive current stability with TID would be a greater issue than the one of the leakage current.

IV. Impact of Elevated Temperature on MGy Dose Sensitivity

The experiments should represent the real environment as much as possible. Elevated temperatures have thus to be considered in addition to ionizing radiations for security systems in nuclear facilities. Standards for tests in such conditions recommend to anneal irradiated devices for one hour at 150°C to qualify equipments submitted to mixed harsh environments [12], [13]. Such tests have been performed on all irradiated devices presented previously but they are also completed with additional experiments performed up to 250°C in order to discuss the annealing behavior of electronic devices in a wider range of operations.

Elevated temperatures in MOS devices usually induce recovery of radiation-induced effects [16]. Radiation-induced oxide-trap charges could be detrapped when point defects responsible for interface traps may anneal. So, elevated temperature may be an efficient way to recover electrical characteristics of pristine integrated circuits. However, using elevated temperatures is also a way to perform dynamic "life tests" which speeds up the ageing of electronic components. Irradiated devices may apparently recover electrical characteristics close to their initial ones but they could also suffer

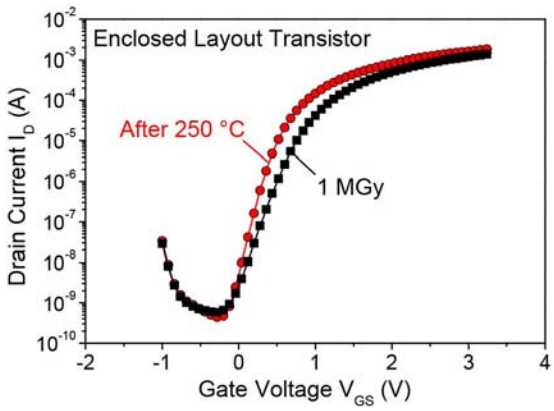

Fig. 8. $I_D - V_{GS}$ characteristics of the bulk ELT transistor after a 1 MGy irradiation (black squares) and after the 250°C annealing step (red circles). The transistor is grounded both during irradiation and annealing.

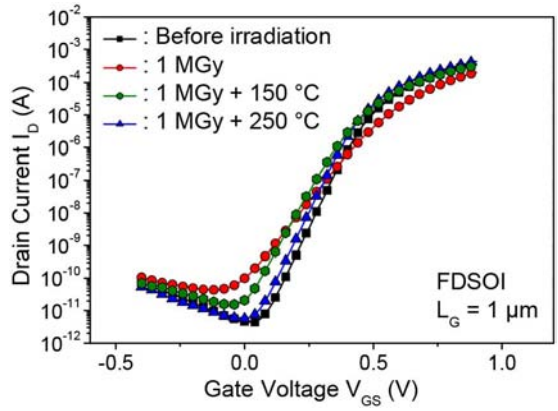

Fig. 9. $I_D - V_{GS}$ characteristics of a long gate FDSOI transistor before irradiation (black squares), after 1 MGy (red circles), after 1 MGy + 150°C (green hexagons) and after 1 MGy + 250°C (blue triangles) The transistor is grounded both during irradiation and annealing.

from a degraded reliability and thus a strongly lower remaining lifetime than at room temperature.

Fig. 8 presents the typical recovery observed on irradiated MOS transistors after annealing experiments at elevated temperatures: the subthreshold slope retrieves its initial value, meaning that most interface traps are annealed after 250°C (red circles) in this transistor. The $I_D - V_{GS}$ characteristics of the ELT annealed at 250°C superimposed the characteristic measured on this transistor before irradiation (not shown for the sake of clarity) meaning that the major part of radiation-induced degradation are annealed. Such plot cannot be presented for the PDSOI transistor since no reliable parameter extractions can be done due to the weak impact of ionizing radiations induced on electrical characteristics of these transistors. Actually, no significant oxide charge and interface traps buildup occurs in the tested PDSOI devices.

FDSOI devices exhibit I-V characteristics which retrieve their initial shape after annealing in Fig. 9. It highlights that the I-V curve of the device that experienced a 1 MGy irradiation followed by 250°C annealing (blue triangles) is closely shaped like the pristine one (black squares). It means that a strong annealing of both the oxide-trap charge and the interface traps occurs in the gate oxide and in the buried oxide and at each silicon-oxide interfaces respectively. These phenomena are enough to recover electrical characteristics close to the pristine one after the 150°C annealing step (green hexagons). These results are very promising since the elevated temperature mostly counterbalances the ionizing dose effects reported in FDSOI devices even in the nominal qualification test conditions.

Elevated temperatures strongly reduce the influence of TID on the interface traps buildup in MOS devices even at MGy dose levels. This is summarized in Fig. 10 where the $I_{ON} - I_{OFF}$ characteristics obtained on the three tested technologies are plotted. All $I_{ON} - I_{OFF}$ characteristics retrieve values close to their initial ones for all tested devices.

However, one should consider the entire "story" of the devices characteristics' instead of only looking at the pre-irradiation, post-irradiation and post-annealing results. If so, most of the information on the TID and annealing behaviors would have been lost. This may lead to take circuit design margins which do

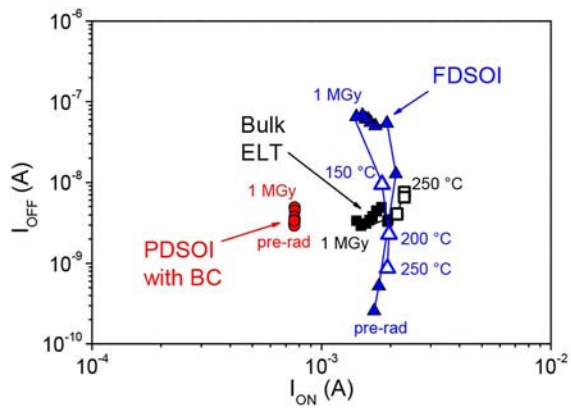

Fig. 10. $I_{ON} - I_{OFF}$ characteristics as a function of TID on FDSOI transistors for bulk (black squares), PDSOI (red circles) and FDSOI (blue triangles) technologies. Annealing results are presented for each technology with open symbols for 150°C,200°C and 250°C. Devices are grounded during irradiation and annealing experiments.

not include the largest modifications induced by TID and temperature on the electrical characteristics.

Furthermore, elevated temperatures may degrade the intrinsic reliability of electronic devices and then reduce their lifetime by several years. This should be quantified by additional dedicated tests to foresee the failure probability of security systems and their replacement periodicity.

Finally, the test procedure presented in this paper only involves "irradiation then temperature" tests. It never takes into account the effect of ionizing radiation with temperature at the same time which represents the more realistic test case compared to real accidental conditions. However, it was demonstrated recently by Girard *et al.* [28] that it may strongly affect the radiation response of optical fibers which show higher TID induced degradation of their optical propagation properties contrary to what is usually assumed. It should then be checked using dedicated experiments in electronic devices as well to ensure that "*irradiation THEN temperature*" tests are still relevant than their "*irradiation AND temperature*" counterparts for modern and innovative technologies. Finally, these first results obtained using 10 keV x-rays on modern technologies should be by to

gamma radiation experiments which are more representative to the real environment.

V. Conclusion

This paper reviews the TID behavior of several micro- and nano-electronic devices at MGy dose levels combined with elevated temperatures. The experimental results show that design rules specific to each technology are required to ensure device functionality at MGy dose levels under elevated temperature. This paper also highlights that one has to take the entire electrical characteristics shifts' induced by ionizing radiations and elevated temperatures to take margins enough to prevent any circuit function failure instead of taking only the pre- and post-TID/temperature test results. At first glance, elevated temperatures lower MGy ionizing dose-induced effects but their impacts on the intrinsic reliability and lifetime of electronic devices have to be quantified to properly qualify electronic systems designed for mixed harsh environments. Furthermore, dedicated studies should be performed to ensure that usual test procedures to qualify electronic devices operating in a mixed environment involving ionizing radiation and high temperature are still relevant for innovative and technologies.

References

[1] D. Fleetwood, "How to protect nuclear reactor electronics," *IEEE Spectrum Tech Talk*, 2011 [Online]. Available: http://spectrum.ieee.org/tech-talk/semiconductors/design/radiationhardening-101

[2] A. H. Johnston, "Space radiation effects and reliability considerations for micro- and optoelectronic devices," *IEEE Trans. Device Mater. Reliab.*, vol. 10, p. 449, 2010.

[3] R. Lacoe, "Designing radiation hardened CMOS microelectronic components at commercial foundries: Space and terrestrial environments and device and circuit techniques to mitigate radiation effects," in *Proc. IEEE Int. Integrated Reliab. Workshop Final Report*, 2005, p. 143.

[4] J. L. Leray, "Activation energies of oxide charge recovery in SOS or SOI structures after an ionizing pulse," *IEEE Trans. Nucl. Sci.*, vol. 32, no. 6, pp. 3921–3928, 1985.

[5] J. L. Leray, E. Dupont-Nivet, J. F. Pere, O. Musseau, P. Lalande, and A. Umbert, "Limiting factors for SOI VLSI high-level hardness : Modeling and improving," in *Proc SOS/SOI Technol. Conf.*, 1989, pp. 114–115.

[6] J. L. Leray, E. Dupont-Nivet, J. F. Pere, Y. M. Coïc, M. Raffaelli, A. J. Auberton-Hervé, M. Bruel, B. Giffard, and J. Margail, "CMOS/SOI hardening at 100 Mrad(SiO2)," *IEEE Trans. Nucl. Sci.*, vol. 37, no. 6, pp. 2013–2019, 1990.

[7] F. Faccio and G. Cervelli, "Radiation-induced edge effects in deep submicron CMOS transistors," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, p. 2413, 2005.

[8] M. Gaillardin, S. Girard, P. Paillet, J. L. Leray, V. Goiffon, P. Magnan, C. Marcandella, M. Martinez, M. Raine, O. Duhamel, N. Richard, F. Andrieu, S. Barraud, and O. Faynot, "Investigations on the vulnerability of advanced CMOS technologies to MGy dose environments," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 4, pp. 2590–2597, 2013.

[9] D. M. Fleetwood, F. V. Thome, S. S. Tsao, P. V. Dressendorfer, V. J. Dandini, and J. R. Schwank, "High temperature silicon-on-insulator electronics for space nuclear power systems: Requirements and feasibility," *IEEE Trans. Nucl. Sci.*, vol. 35, no. 5, pp. 1099–1113, 1988.

[10] M. R. Shaneyfelt, J. R. Schwank, D. M. Fleetwood, and P. S. Winokur, "Effects of irradiation temperature on MOS radiation response," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 3, pp. 1372–1378, 1998.

[11] D. M. Fleetwood, P. S. Winokur, M. R. Shaneyfelt, L. C. Riewe, O. Flament, P. Paillet, and J. L. Leray, "Effects of isochronal annealing and irradiation temperature on radiation-induced trapped charge," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 2366–2374, 1998.

[12] IAEA-TECDOC-118, Assessment and management of ageing of major nuclear power plant components important to safety : In containment instrumentation and control cables, 2000.

[13] NF M64-001, Procédure de qualification des matériels électriques installés dans l'enceinte de confinement des réacteurs à eau sous pression et soumis aux conditions accidentelles, 1991.

[14] H. K. Lim and J. G. Fossum, "Threshold voltage of thin film silicon-on-insulator (SOI) MOSFET's," *IEEE Trans. Electron Dev.*, vol. ED-30, no. 10, p. 1244, 1983.

[15] M. Gaillardin, M. Martinez, P. Paillet, F. Andrieu, S. Girard, M. Raine, C. Marcandella, O. Duhamel, N. Richard, and O. Faynot, "Impact of SOI substrate on the radiation response of ultra-thin transistors down to the 20 nm node," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 4, p. 2583, 2013.

[16] J. R. Schwank, "Total dose effects in MOS devices," *NSREC Short Course*, 2002.

[17] T. R. Oldham and F. B. McLean, "Total ionizing dose effects in MOS oxides and devices," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, p. 483, 2003.

[18] T. P. Ma and P. V. Dressendorfer, *Ionizing radiation effects in MOS devices and circuits*. New York, NY, USA: Wiley-Interscience, 1989.

[19] P. J. McWhorter and P. S. Winokur, "Simple technique for separating the effects of interface traps and trapped-oxide charge in metal-oxide-semiconductor transistors," *Appl. Phys. Lett.*, vol. 48, no. 2, p. 133, 1986.

[20] M. R. Shaneyfelt, P. E. Dodd, B. L. Draper, and R. S. Flores, "Challenges in hardening technologies using shallow trench isolations," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, p. 2584, 1998.

[21] M. Gaillardin, V. Goiffon, S. Girard, M. Martinez, P. Magnan, and P. Paillet, "Enhanced radiation induced narrow channel effects in a commercial 0.18 μm bulk technology," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, p. 2807, 2011.

[22] J. R. Schwank, V. Ferlet-Cavrois, M. R. Shaneyfelt, P. Paillet, and P. E. Dodd, "Radiation effects in SOI technologies," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, p. 522, 2003.

[23] W. C. Jenkins and S. T. Liu, "Radiation response of fully-depleted MOS transistors fabricated in SIMOX," *IEEE Trans. Nucl. Sci.*, vol. 41, no. 6, p. 2317, 1994.

[24] J. R. Schwank, M. R. Shaneyfelt, P. E. Dodd, J. A. Burns, C. L. Keast, and P. W. Wyatt, "New insights into fully-depleted SOI transistor response after total-dose irradiation," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 3, p. 604, 2000.

[25] P. Paillet, M. Gaillardin, V. Ferlet-Cavrois, A. Torres, O. Faynot, C. Jahan, L. Tosti, and S. Cristoloveanu, "Total ionizing dose effects on deca-nanometer fully depleted SOI devices," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, p. 2345, 2005.

[26] C. Fenouillet-Beranger, P. Perreau, S. Denorme, L. Tosti, F. Andrieu, O. Weber, S. Barnola, C. Arvet, Y. Campidelli, S. Haendler, R. Beneyton, C. Perrot, C. de Buttet, P. Gros, L. Pharn-Nguyen, F. Leverd, P. Gouraud, F. Abbate, F. Baron, A. Torres, C. Laviron, L. Pinzelli, J. Vetier, C. Borowiak, A. Margain, D. Delprat, F. Boedt, K. Bourdelle, B.-Y. Nguyen, O. Faynot, and T. Skotnicki, "Impact of a 10-nm ultra-thin box (UTBOX) and ground plane on FDSOI devices for 32 nm and below," in *Proc. ESSDERC*, 2009.

[27] L. Brunet, X. Garros, M. Cassé, O. Weber, F. Andrieu, C. Fenouillet-Béranger, P. Perreau, F. Martin, M. Charbonnier, D. Lafond, C. Gaumer, S. Lhostis, V. Vidal, L. Brévard, L. Tosti, S. Denorme, S. Barnola, J. F. Damlencourt, V. Loup, G. Reimbold, F. Boulanger, O. Faynot, and A. Bravaix, "New insights on Vt stability of HK/MG stacks with scaling in 30 nm FDSOI technology," in *Proc Symp. VLSI Technology Dig. Technical Papers*, 2010, p. 29.

[28] S. Girard, C. Marcandella, A. Morana, J. Perisse, D. Di Francesca, P. Paillet, J.-R. Macé, A. Boukenter, M. Léon-Pichel, M. Gaillardin, N. Richard, M. Raine, S. Agnello, M. Cannas, and Y. Ouerdane, "Combined high dose and temperature effects on multimode silica-based optical fibers," in *Proc. IEEE Nuclear and Space Radiation Effects Conf.*, San Francisco, CA, USA, Jul. 2013.