Speed Analysis in Pinned Photodiode CMOS Image Sensors based on a Pulsed Storage-Gate Method

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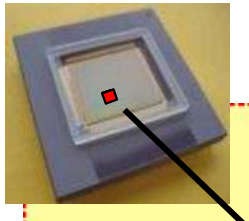
CMOS Image sensors

- **CMOS Image sensors (CIS): main technology for commercial imaging applications:**
  - Driven by massive development of consumer electronics (smart-phones, tablet ..)
    - *Multibillion $ market*
  - Technological breakthroughs announced every year
- **Scientific imaging applications:**
  - XX_{st} century: mainly Charge Coupled Devices (CCDs)
  - Thanks to the introduction of the Pinned Photodiode (PPD) technology, CIS now compete with CCDs in terms of:
    - *Sensitivity*
    - *Low noise*
  - With all the advantages of CIS technology:
    - *Lower cost, smart functions integration, random access capabilities …*

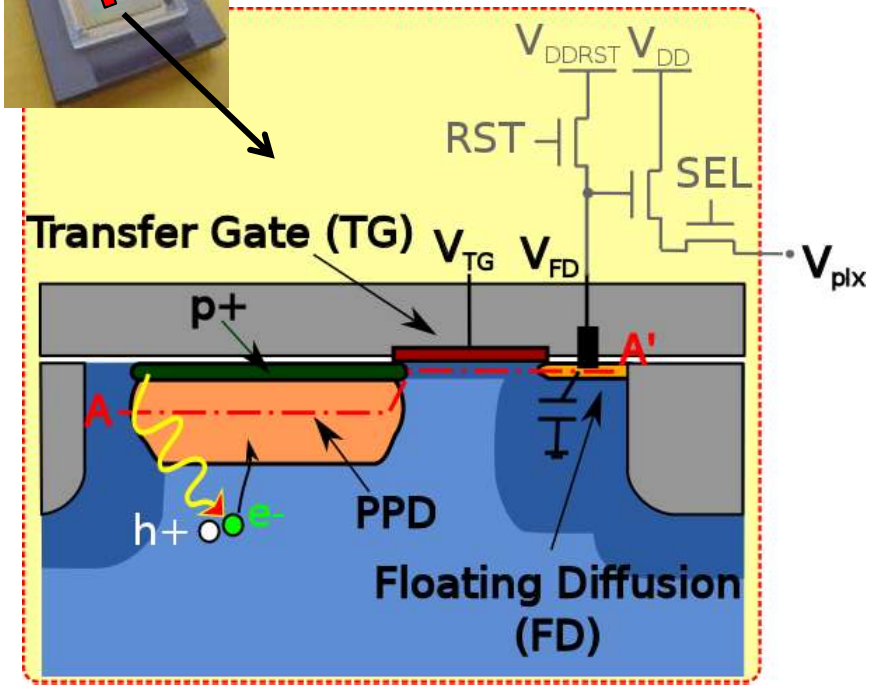
Sentinel 2 (www.esa.int)

Structure and operation principle

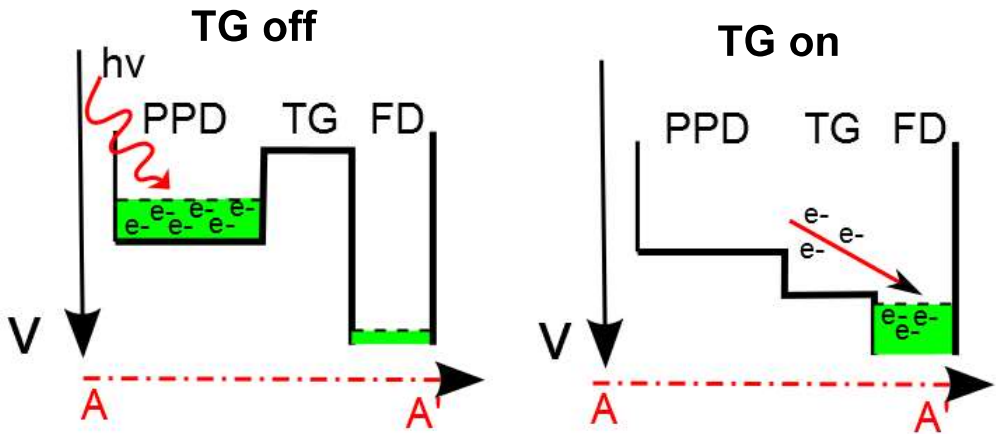
Full Image Sensor



Cross-section of a PPD pixel



- **Based on a transfer of charge:**

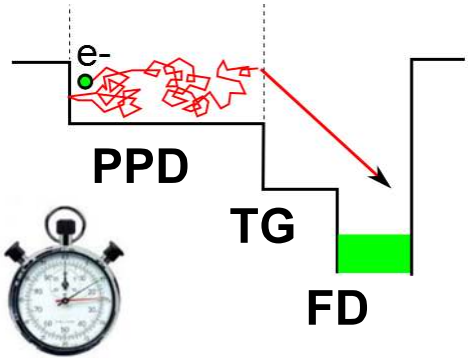


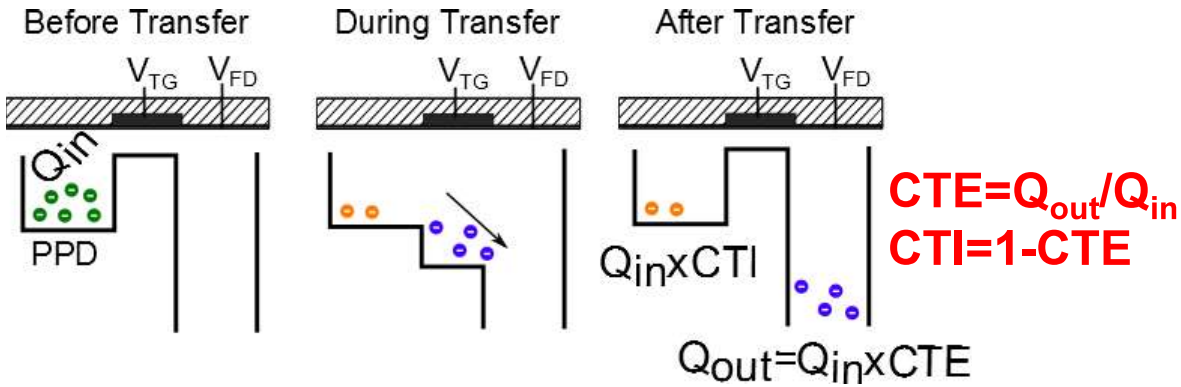
- **Low dark current, good sensitivity**
- **Enables correlated double sampling**
  - Very good SNR performances

- **Good candidate for high temporal resolution applications (such as Time of Flight applications)**
- **Requirements of high resolution applications:**
  - Fast sampling of the incoming light waveform →SPEED
  - Readout of extremely low signal levels → VERY GOOD SNR

Temporal resolution in PPD CIS

- **Limiting temporal resolution = time to transfer electrons from PPD to FD**
- **Charge Transfer Inefficiency (CTI):**
  - measures the ability of transferring the collected charge in a given time

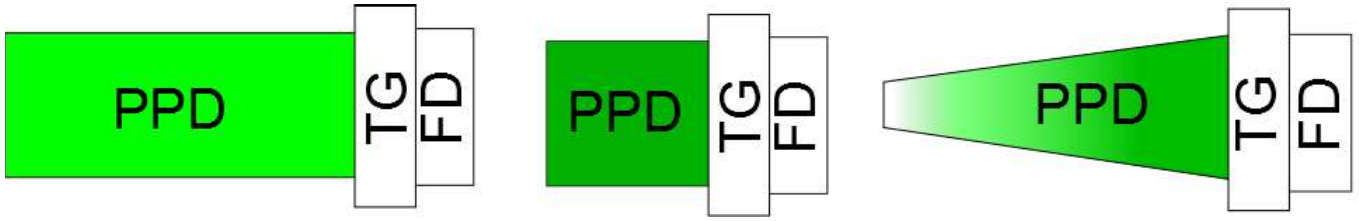




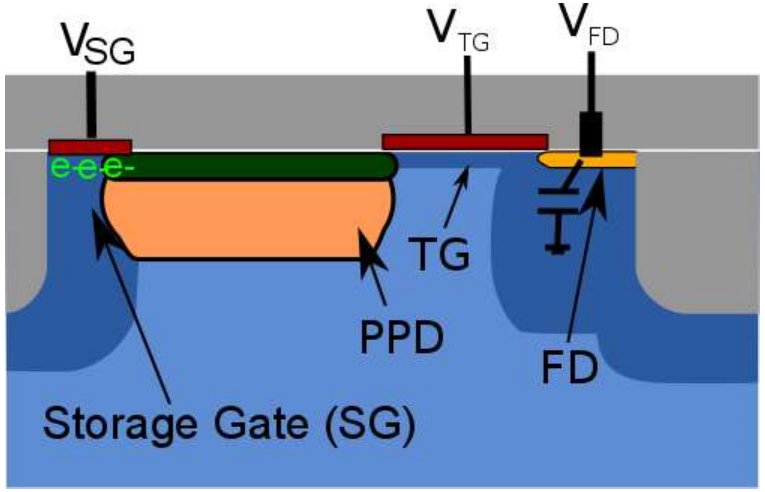
- **<u>Main Question</u>: Which design/operation parameters affect the CTI?**
- **<u>Road-map:</u>**
  - Modeling and simulation of main charge transport mechanisms in PPD CIS
  - Experimental measurements on dedicated Pulsed Storage-Gate pixels
  - Identification of bottle-neck in terms of CTI by comparing the effect of different parameters on data and simulations
- **<u>Goal of this study</u>: Provide tools to users and designers to find optimum trade-off between parameters to reach good CTI**

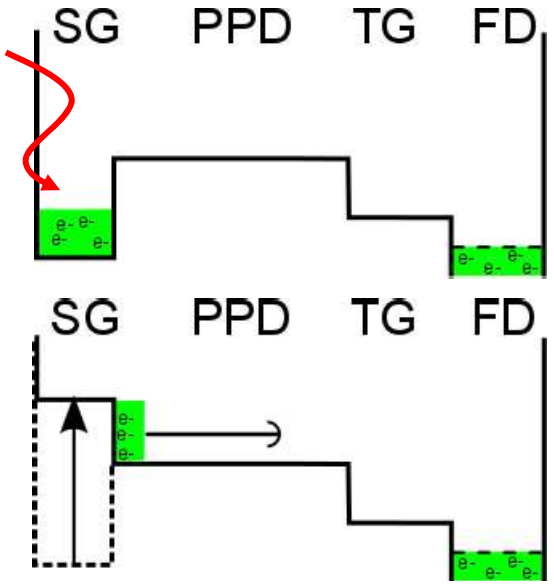
How to fairly compare CTI?

- **Hard to compare CTI in pixels with different size and geometries**
  - Different charge level and initial charge distribution



- **Pulsed Storage-Gate pixels enable comparison:**
  - With same charge level and same initial charge distribution
  - Reproducing a worst case transfer condition

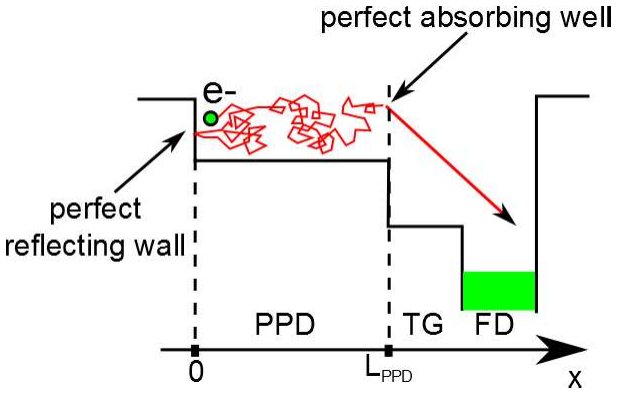




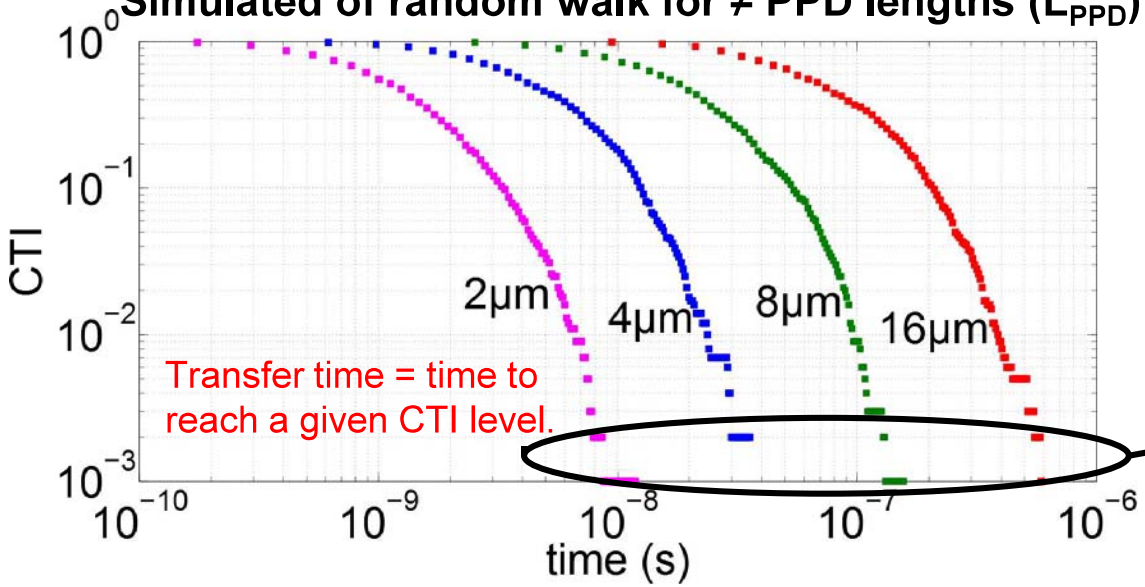
Simulations: Charge Diffusion

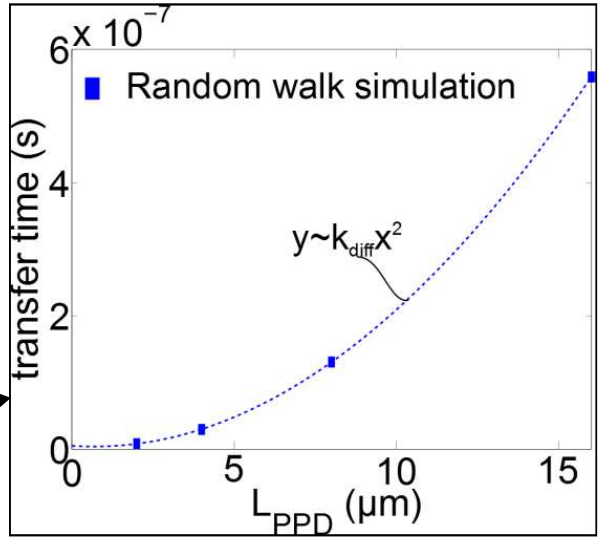
- **PPD Potential is mainly flat:**
  - Diffusion = main transport mechanism
- **Model: Montecarlo simulation of the random walk of single carriers.**
- **The arrival time of electrons is not deterministic**
  - Transfer time = time to reach a given CTI

- **Boundary conditions:**



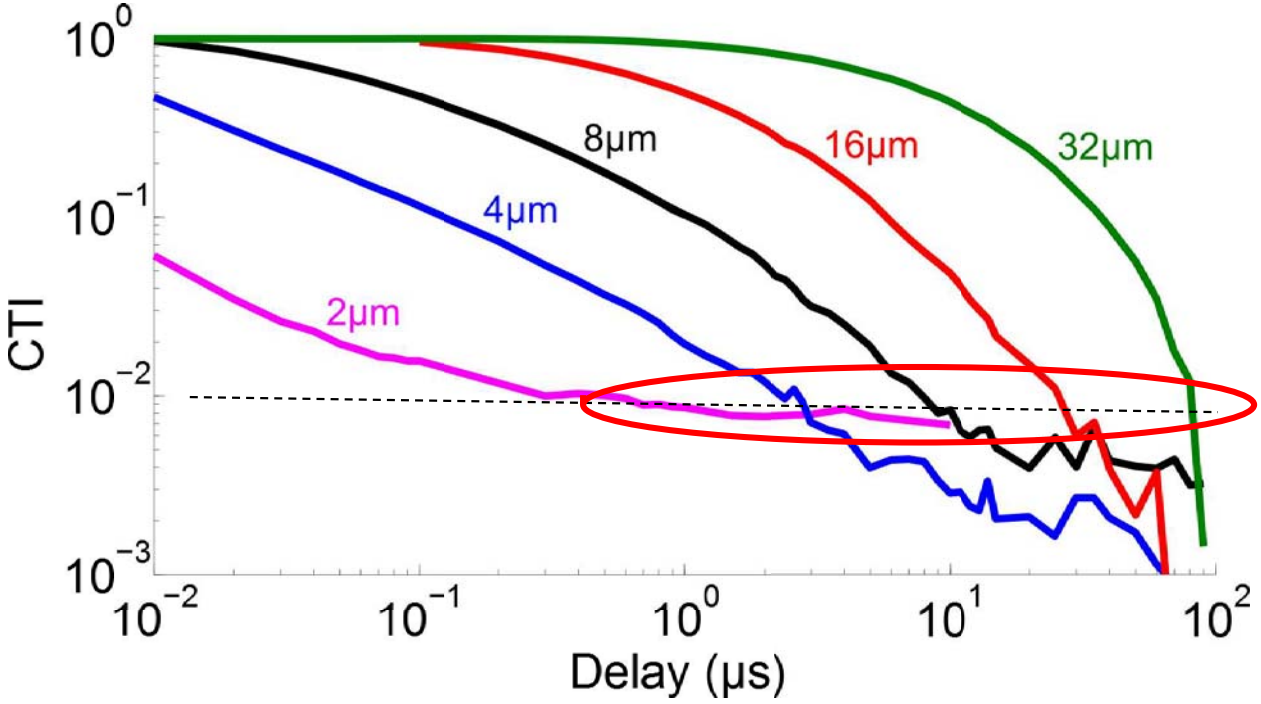
Simulated of random walk for ≠ PPD lengths (L_{PPD})

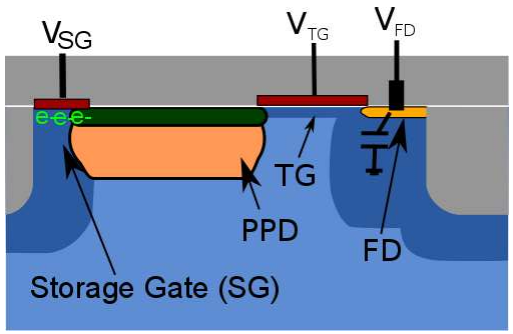




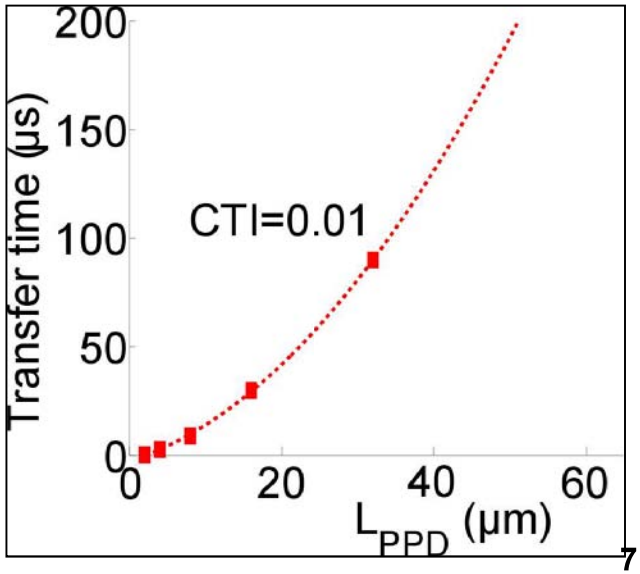
- **Transfer time increases L_{PPD}^2.**

Experimental results: effect of L_{PPD}



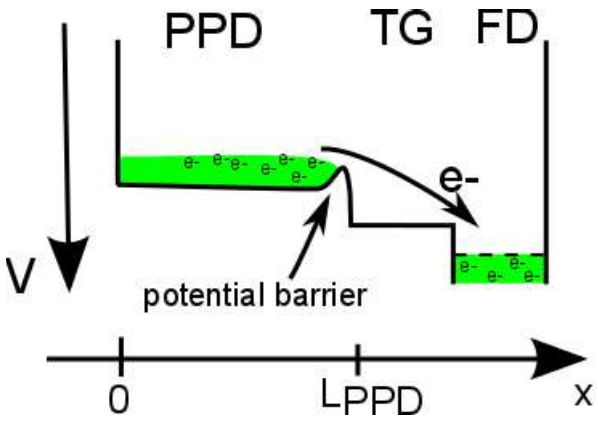


- **With respect to simulations:**
  - Same behavior (increases with L_{PPD}^2)
  - Almost 2 orders of magnitude larger than what predicted without design traps

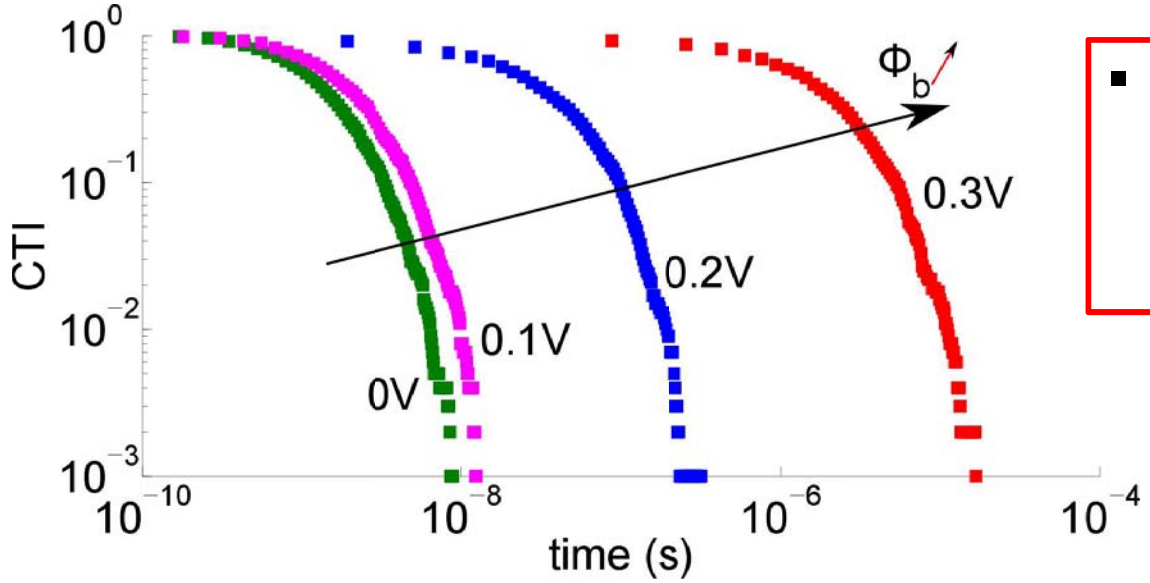


Simulation: Design traps

- **There can be ''design traps'' along the charge transfer path (potential barrier/pocket)**
  - Usually located at the PPD-TG interface
  - Electrons can
    - *"cross" the barrier by* ***thermionic emission***
    - *or " bounce" on the barrier*
  - The probability of crossing is an exponential function of the barrier height (Φ_b)



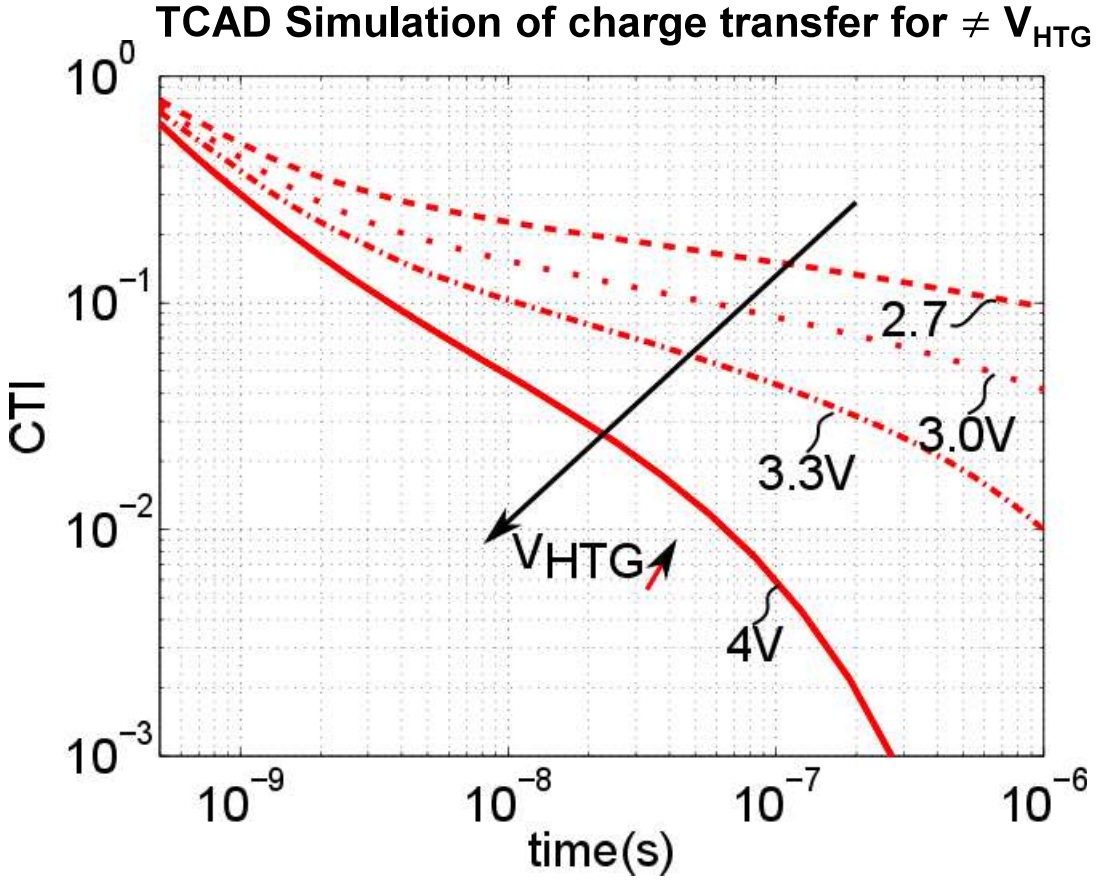
Simulation of random walk with ≠ Φ_b

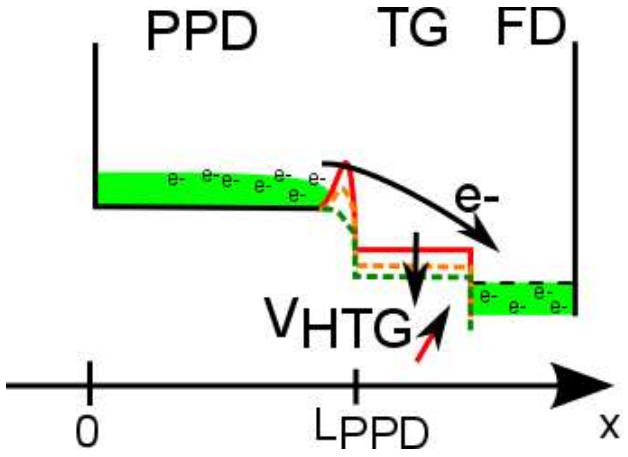


- **Design traps significantly affect the transfer time**
  - Worsening of several orders of magnitude

Simulation: reducing effect of design traps with TG biasing potentia (V_{HTG})l

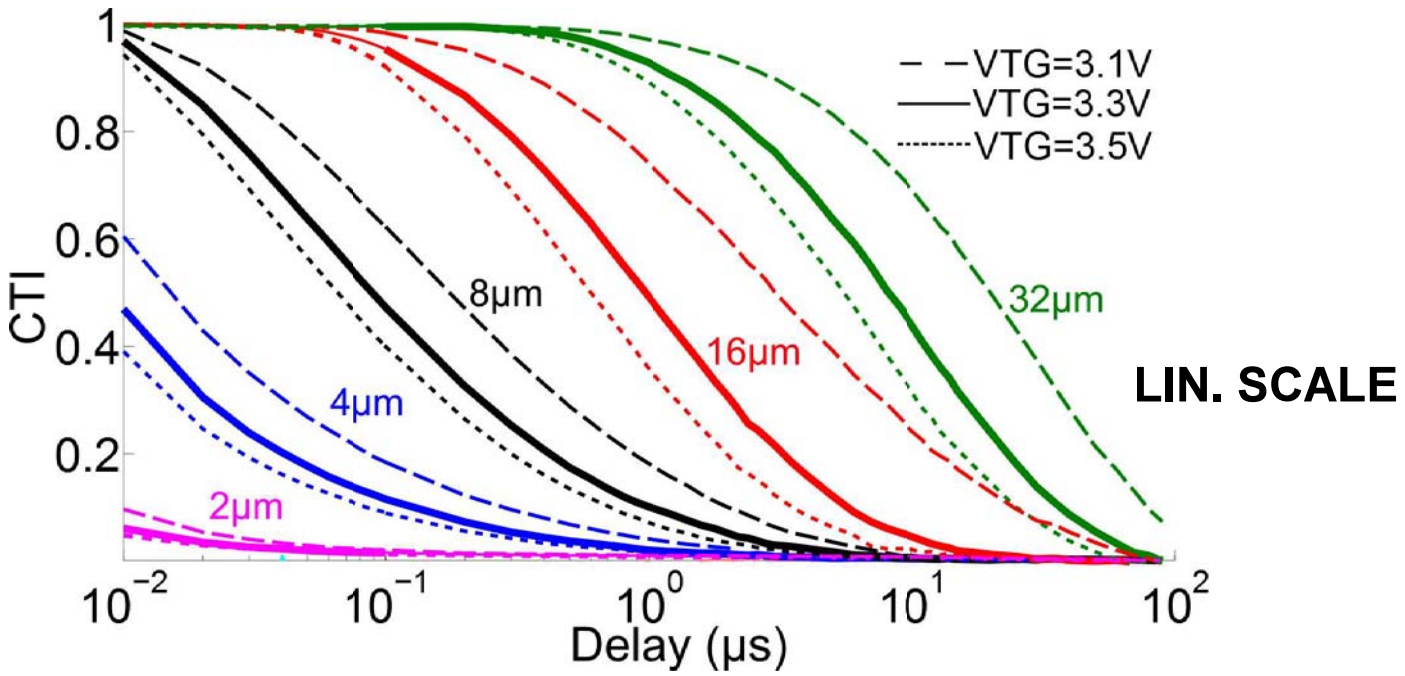
- Φ_b can be reduced by increasing the TG biasing voltage during transfer (V_{HTG})





- But..a too high V_{HTG} can result in a degradation of CTI due to charge partition phenomena
  - Trade-off

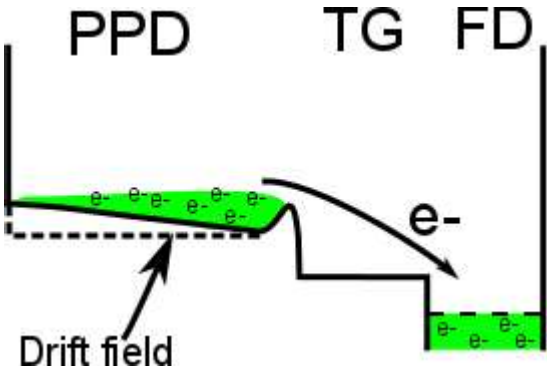
Experimental results: effect of V_{HTG}



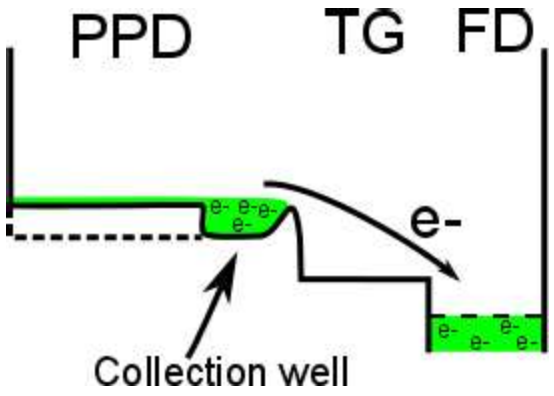
- **CTI is significantly affected by VHTG**
  - even at typical biasing levels (V_{TG}=3,3V)
- **These results have been confirmed by other measurements which also indicated that CTI is limited by a potential barrier at the PPD-TG interface**

Conclusion and Outlook

- **Charge transfer mechanisms have been studied based on Montecarlo simulations and TCAD simulations**
- **Experimental measurements on dedicated pulsed storage-gate structure**
  - Enable fair CTI comparisons (on PPD lengths up to 32µm)
- **This study showed that for this commercial technology CTI is limited by design traps even for long PPDs.**
- **This same approach can be used to identify the CTI bottleneck on other technologies**
- **Solutions to improve transfer time:**
  - Increasing V_{TG} during transfer
  - Increasing probability of crossing barrier by keeping electrons close to the TG
    - **By introducing a drift field**



    - **With a collection well**



Thank you for your attention!
Any questions?