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Pixel Level Characterization of Pinned Photodiode and Transfer Gate Physical Parameters in CMOS Image Sensors

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ABSTRACT A method to extract the pinned photodiode (PPD) physical parameters inside a CMOS image sensor pixel array is presented. The proposed technique is based on the Tan *et al.* pinning voltage characteristic. This pixel device characterization can be performed directly at the solid-state circuit output without the need of any external test structure. The presented study analyzes the different injection mechanisms involved in the different regimes of the characteristic. It is demonstrated that in addition to the pinning voltage, this fast measurement can be used to retrieve the PPD capacitance, the pixel equilibrium full well capacity, and both the transfer gate threshold voltage and its channel potential at a given gate voltage. An alternative approach is also proposed to extract an objective pinning voltage value from this measurement.

INDEX TERMS CMOS image sensor, CIS, pinned photodiode, PPD, pinning voltage, pinch-off voltage, transfer gate, TG, threshold voltage, characterization, full well capacity, FWC, EFWC, channel potential, capacitance, active pixel sensor, APS, integrated circuit, solid-state image sensor.

I. INTRODUCTION

Pinned Photodiode CMOS Image Sensors (PPD CIS)[1] represent today the main solid-state optical sensor technology[2] for imaging applications ranging from mass market smartphones to high-end scientific instruments. The PPD device has been known for more than thirty years now [1], [2] and this unique structure associated to a Transfer Gate (TG), initially developed for Charge Couple Devices (CCD), has been used in CMOS Image Sensors since about two decades [3], [4]. Despite the fact this photodetector is widely used today, defining, measuring and modeling its physical parameters is still not straightforward. One of the main reasons for that is the difficulty to reach the physical parameters of the PPD embedded inside a CIS Integrated Circuit (IC). An

alternative solution to access these physical parameters is the use of isolated test structures (see for example [5] for a pinning voltage (V_{pin}) test structure and [6] for channel potential measurement test structures). Such structures generally differ strongly from the real PPD that can be found in a pixel array, because the physical dimensions are very different, because the environment is not the same (e.g., this is the case when one directly biases a PPD without using a TG) or because the PPD readout mode does not correspond to the dynamic PPD operation in a standard imager. Some physical parameters are sometimes simply almost impossible to obtain on a test structure[3] or test structures may simply be unavailable on the studied sensor (this is most often the case during radiation test campaign for instance).

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1. Sometimes called 4T CIS when only 4 transistors are used inside the pixel.
2. in terms of volume.

3. e.g., a direct PPD capacitance measurement technique that does not modify the PPD structure by adding significant parasitic capacitances is not straightforward.
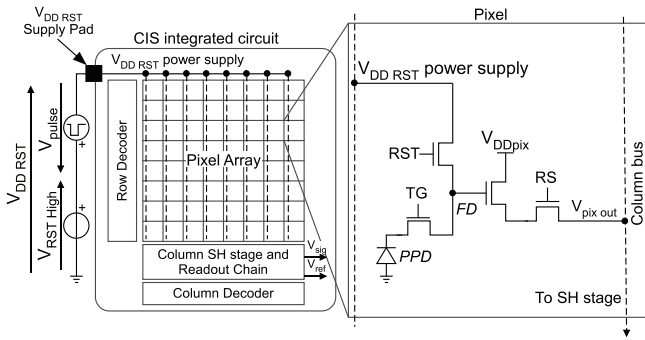
FIGURE 1. Test setup illustration. A pulse is applied on the V_{DDRST} power supply pad to inject charges in the PPD through the RST and TG MOSFETs. Only one pixel is represented for clarity purpose but the V_{DDRST} power supply is connected to all the pixels of the tested image sensor.

FIGURE 2. Simplified timing diagram that presents the measurement principle. The charges are injected into the PPD at the end of the integration phase (injection phase) by lowering V_{DDRST} to V_{inj} and pulsing TG on.

On the other hand, these unreachable physical parameters can be very useful to properly characterize a PPD CIS pixel in order to adjust a manufacturing process or a pixel design. They can also be used to improve or create PPD physical models and to monitor the health of the PPD-TG structure when exposed to various stresses (e.g., electrical stress, hot electrons, thermal stress, ionizing radiation [7], displacement damages...).

Tan, Büttgen and Theuwissen have recently proposed a measurement technique that can be applied to a standard PPD CIS to evaluate its pinning voltage without the need of an associated test structure [8].

In this work, we propose to analyze the benefit of this V_{pin} extraction method for the characterization of CIS solid-state circuits. We demonstrate that, in addition to the pinning voltage estimation, this characteristic can be used to evaluate the pinned photodiode capacitance, the Equilibrium Full Well Capacity [9] (EFWC), and in some cases, to extract the channel potential evolution with TG voltage and thus, its threshold voltage. Secondary information can be inferred from these main physical parameters such as the doping concentration, the relative importance of the peripheral capacitance compared to the area capacitance, or the existence (or not) of a significant potential barrier between the PPD and the TG.

After the detailed description of the tested device (second section) and the description of the existing technique (third section), the proposed physical parameter extraction principles are given in the fourth part. The fifth section presents the parasitic effects that can influence the extracted parameter values. Finally, in a last part before the conclusion, an objective method to determine the pinning voltage on the characteristic is proposed.

II. TESTED DEVICE DETAILS

A CMOS image sensor constituted of 256×256 7-μm-pitch-4T-pixels has been designed and manufactured using a widely used, commercially available, 180 nm CIS process from an Asian foundry. This device is different from the one used in early work [10] (different design, different pixel
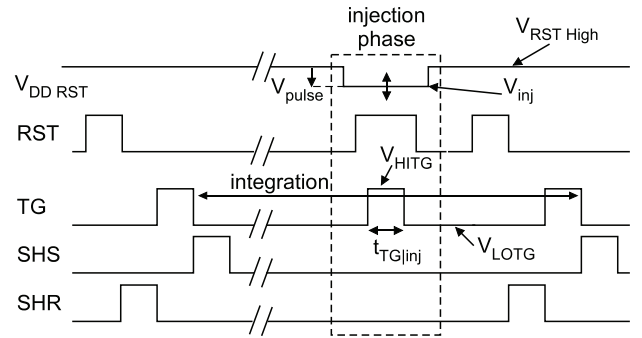
pitch). An overview of the studied solid-state circuit and the test setup is presented in Fig. 1.

The pixel array is divided in several sub-arrays of 64×64 pixels, each sub-array has a different PPD/TG design. All the pixels embed a PPD, a TG, and the three additional transistors needed for resetting the pixel, amplifying the signal and for selecting the pixel. The reference pixel studied in this paper has a square PPD of 2.5×2.5 μm^2 with a long TG on one side. The average conversion factor (CVF) on this sub-array is about 20 μV/e$^-$. The sensor is operated in the electronic rolling shutter mode with correlated double sampling (CDS). If not stated otherwise, the presented results were obtained at 22°C on this reference pixel sub-array.

III. PINNING VOLTAGE CHARACTERISTIC OVERVIEW

A. EXPERIMENT SETUP

The measurement principle that is proposed in [8] and further described here is based on the modification of the floating diffusion (FD) potential during an injection phase as shown in Fig. 2. We performed this operation thanks to the test setup shown in Fig. 1. By using an arbitrary waveform generator, the sensor V_{DDRST} power supply is lowered to V_{inj} during the injection phase. Then, the RST and TG MOSFETs of the currently selected row are turned ON to apply directly V_{inj} to the PPD channel through the FD. The injection phase of the currently selected row occurs right before the row is readout, without deselecting the row (i.e., the RS MOSFET remains ON). It means that the time between the end of the injection phase and the readout phase is very short (a few microseconds) and it ensures that parasitic currents, such as dark current (and even moderate photocurrents), do not change significantly the signal value injected in the PPD.

To ensure that the V_{inj} level is well established in the PPD and to limit the coupling effects:

- a long injection phase duration was chosen (about 45 μs)
- all the decoupling capacitances on the V_{DDRST} power supply have been removed from the test board dedicated to this measurement
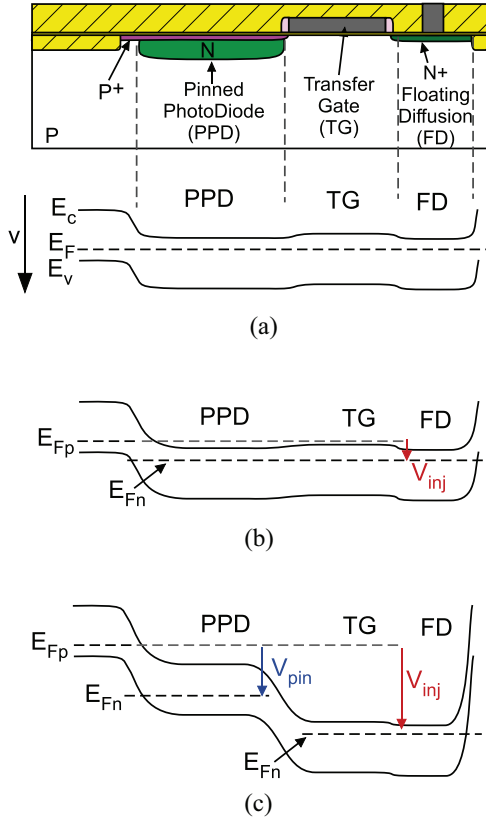
(a)

(b)

(c)

FIGURE 3. Simplified band diagram used to clarify the selected notations and illustrate the simplifying assumptions. (a) V_{inj} = 0V and TG ON. (b) $0 < V_{inj} < V_{pin}$ and TG ON. (c) $V_{inj} < V_{pin} < \phi_{TG|inv}$ and TG ON.

- the TG pulse (with a duration $t_{TG|inj}$ of about 35 μs) is enclosed by the RST pulse which is itself enclosed by the pulse on V_{DDRST} (as illustrated in Fig. 2).

During the readout phase (i.e., outside the injection phase), all the pulses (TG, RST, SHS and SHR pulses) last 1 μs. It should be mentioned that the high and low TG voltage levels (V_{HITG} and V_{LOTG} respectively) are the same during the injection phase and during the readout phase.

To obtain the V_{pin} characteristic, the injection voltage V_{inj} is stepped from 3.3 V to −1 V and for each V_{inj} value, 100 frames are acquired in the dark and averaged over time and over the area of interest (the reference pixel sub-array) to obtain one average signal value per step.

B. DEFINITIONS AND CHARACTERISTIC DESCRIPTION

As in [11], the channel potential (of the PPD or TG) is defined as the potential difference between the electron and hole quasi-Fermi levels (E_{Fn} and E_{Fp} respectively). The pinning voltage V_{pin} corresponds to the maximum PPD channel potential (i.e., the maximum difference between the hole and electron quasi-Fermi levels in the PPD [12]). The TG channel potential at which the strong inversion condition is reached is noted $\phi_{TG|inv}$ in the following.

Fig. 3 presents the band diagram of the PPD-TG-FD structure for three V_{inj} values and with the TG turned ON.
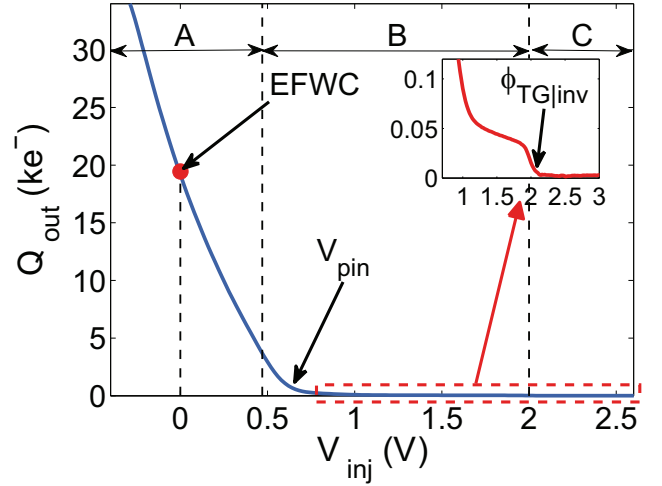

FIGURE 4. Pinning voltage characteristic measured on the reference pixel sub-array with the nominal conditions defined in Section III-A. The three main regions (A: direct injection, B: charge partition/thermionic emission, and C: no injection) and some physical parameters that can be extracted (pinning voltage V_{pin}, the equilibrium full well capacity (EFWC), and the injection voltage at which the TG channel is inverted $\phi_{TG|inv}$) are indicated.

When the injection voltage is below $\phi_{TG|inv}$ (cases (a), (b) and (c) in Fig. 3), an inversion channel is formed under the TG and its electron quasi-Fermi level is the same as the one in the FD region. As a consequence, the TG channel potential is directly equal to V_{inj} when $V_{inj} < \phi_{TG|inv}$. The same phenomenon occurs in the PPD when $V_{inj} < V_{pin}$ (cases (a) and (b)): the PPD electron quasi-Fermi level is the same as the one in the TG and FD regions and thus, the PPD channel potential is equal to V_{inj} when $V_{inj} < V_{pin}$.

The characteristic achieved with the experimental setup previously described is presented in Fig. 4. Fig. 5 presents the simplified potential diagrams that illustrate the different injection mechanisms involved in this experiment. When the injection voltage V_{inj} is higher than the TG inversion channel potential $\phi_{TG|inv}$ [Fig. 5(a) and region C in Fig. 4], there is no signal at the sensor output (no charge $Q_{out} = V_{out}/CVF$) because no charge is injected in the PPD. This case corresponds to the classical charge transfer configuration that occurs during a standard readout phase where the signal carriers (if any) are transferred from the PPD to the FD.

On the other hand, the output signal rises rapidly with decreasing V_{inj} when the injection potential is well below V_{pin} [Fig. 3(a) and (b), region A in Fig. 4 and Fig. 5(d)]. In this case, the charges are injected by direct biasing of the PPD itself (since the PPD channel potential is equal to V_{inj} in this case) and the charge injected in the PPD can be approximated by:

$$Q_{out}\left(V_{inj}\right) = \int_{V_{pin}}^{V_{inj}} C_{PPD}\left(V\right) dV, \tag{1}$$
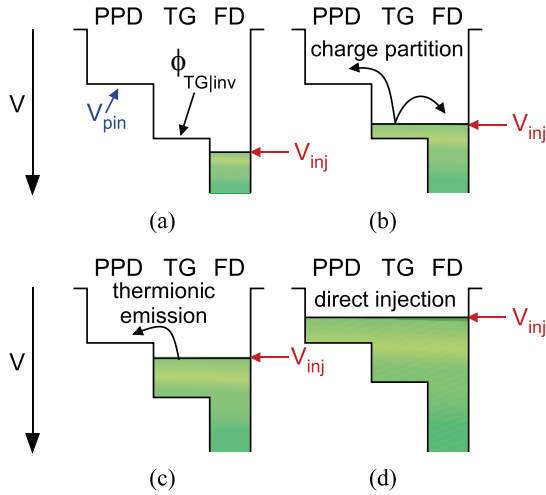
FIGURE 5. Simplified electrostatic potential diagram of the PPD, TG, and FD for several injection bias conditions. (a) When $V_{inj} > \phi_{TG|inv}$: no injection. When $V_{pin} < V_{inj} < \phi_{TG|inv}$: partial injection due to (b) charge partition or (c) thermionic emission (when V_{inj} is close enough to V_{pin}). (d) When $V_{inj} < V_{pin}$: direct injection of charges into the PPD.

with $C_{PPD}(V)$ the PPD capacitance that depends on the PPD reverse bias voltage (equal to V_{inj} in this direct injection mode).

Between these two regimes [Fig. 3(c) and region B in Fig. 4], a plateau appears on the characteristic. This plateau has not been reported in [8] and is attributed to charge partition [13], [14] between the PPD and the FD when the TG is turned OFF. This phenomenon is also sometimes referred to as a spill back effect [15] and it only occurs when an inversion channel exists before the TG is turned OFF. Therefore, it can be inferred that the steep transition between the C and B region for $V_{inj} \approx 2$ V in Fig. 4 corresponds to the particular case where $V_{inj} = \phi_{TG|inv}$.

Another process is likely to occur on the left hand side of the B region in Fig. 4: thermionic emission [16]. Such phenomenon starts to dominate the injection process when the injection potential is close enough to V_{pin} as illustrated in Fig. 5(c) [to be compared to Fig. 5(b)]. By using the simple isothermal thermionic emission theory [16] and assuming that every electron that jumps over the barrier stays in the PPD until the end of the injection phase, the thermionic injection current can be expressed:

$$I_{th} = KT^2 \exp\left(-q\frac{V_{inj} - V_{pin}}{kT}\right) \quad (2)$$

where K is a physical constant that depends on the material and on the dimensions of the structure. As a first approximation, the charge injected in the PPD through thermionic injection could be approximated by:

$$|Q_{th}| = KT^2 \exp\left(-q\frac{V_{inj} - V_{pin}}{kT}\right) \times t_{TG|inj} \quad (3)$$

where $t_{TG|inj}$ is the time duration of the TG injection pulse. This hypothesis is in good agreement with the exponential

increase with decreasing V_{inj} that can be observed for $V_{inj} \approx 1$ V in the inset of Fig. 4.

IV. IDEAL PARAMETER EXTRACTION TECHNIQUES

A. PINNING VOLTAGE

The pinning voltage of a PPD represents the bottom of the photodetector potential well and it is directly related to the pixel Full Well Capacity (FWC). Knowing its value allows to tune properly the TG and FD voltages to optimize the FWC and the charge transfer efficiency while preventing spill-back. It is also useful for sizing properly the pixel conversion factor.

The main techniques that can be found in literature to estimate V_{pin} are based on test structures [5]. As discussed in the introduction, these structures are not necessarily representative of the in-pixel PPD and in most of the cases, such structures are simply not available on the studied device.

An alternative solution is to determine this particular voltage by using the characteristic studied here [8]. According to the discussion of the previous section, when the injection voltage V_{inj} is above V_{pin}, the thermionic emission regime dominates [Fig. 5(c)] whereas the direct injection occurs when V_{inj} is below V_{pin} [Fig. 5(d)]. It means that V_{pin} is close to V_{inj} at the boundary between regions A and B (Fig. 4). That's the reason why the pinning voltage is described in [8] as the V_{inj} value that corresponds to the knee in the characteristic. It is interesting to notice that the knee position depends on the magnification used to observe the characteristic, as can be seen in Fig. 4 by comparing the inset to the whole characteristic. In the inset, the knee occurs for $V_{inj} \approx 1$ V whereas a value of ≈ 0.5 V would be inferred with the scale used for displaying the full characteristic. This is mainly due to the smooth transition from the thermionic injection case [Fig. 5(c)] to the direct injection case [Fig. 5(d)]. After discussing all the parasitic effects that can distort this characteristic, an objective pinning voltage extraction method, that does not depend on the plot scale, is proposed in Section VI.

B. EQUILIBRIUM FULL WELL CAPACITY

The FWC is the maximum charge that can be handled by a PPD. Its value depends on the illumination condition as illustrated in Fig. 6. One can see in this plot that the saturation level reached without illumination is lower than the saturation level reached under illumination. It is demonstrated in [9] that the FWC value rises logarithmically with the photon flux. The particular FWC value achieved in dark condition has recently been emphasized in [9] and will be referred to as the Equilibrium Full Well Capacity (EFWC) here. It corresponds to the amount of electrons stored in the PPD under equilibrium condition (i.e., when the PPD is full and with no illumination). This parameter is of primary importance because it is the only FWC value directly linked to the intrinsic PPD parameters: the pinning voltage and the
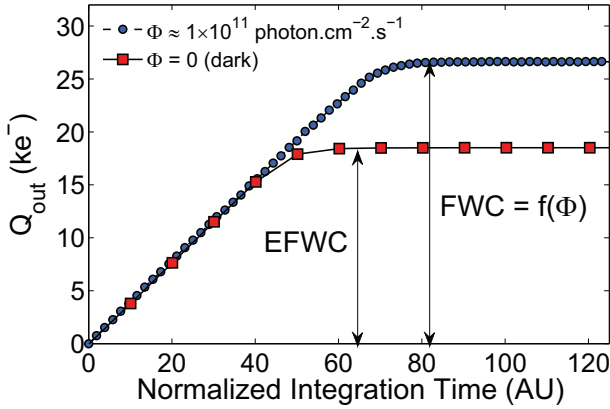
FIGURE 6. Mean sensor output charge as a function of normalized integration time for two conditions: under illumination and in the dark.

FIGURE 7. Comparison between the FWC measured in the dark (i.e., the EFWC) and the EFWC value extracted from the V_{pin} characteristic. The FWC in the dark has been measured at $40°C$ to speed up the measurement. The EFWC value extracted on the V pin characteristic corresponds to the Q_{out} value achieved for $V_{inj} = 0$.

PPD capacitance. Indeed, the EFWC can be defined as:

$$\text{EFWC} = Q_{\text{out}}\left(V_{\text{inj}} = 0\right) = \int_{V_{\text{pin}}}^{0} C_{\text{PPD}}\left(V\right) dV. \quad (4)$$

A direct measurement of the EFWC value at room temperature on state of the art CIS is very time consuming: it can take several hours of integration to get a single frame with a dark current in the e^-/s range and an EFWC value in the 10–100 ke^- range.

By definition, the EFWC is the PPD stored charge when the PPD channel potential is null. This particular value can directly be extracted from the V_{pin} characteristic by taking the Q_{out} value for $V_{inj} = 0$ V (i.e., the Y-intercept). Knowing that a V_{pin} characteristic can be measured in a few seconds or minutes, this presents a significant benefit for the fast evaluation of the EFWC value.

In order to validate the assumption that the Y-intercept of the V_{pin} curve gives the EFWC, its value has been extracted on a different PPD-CIS manufactured using a different foundry with several process variations. For each process variation, the two methods have been used to estimate the EFWC value. The first method is to increase the integration time in the dark until reaching the saturation level (equal to EFWC) as in Fig. 6. The other method is the direct determination on the V_{pin} graph (Fig. 4). The result of this comparison is presented in Fig. 7. It shows that the two methods are in pretty good agreement (less than 10% of standard deviation).

This important result confirms the previous hypothesis (that EFWC = $Q_{\text{out}}\left(V_{\text{inj}} = 0\right)$), it also strengthens the validity of the EFWC concept (and the validity of (4)) and demonstrates that the absolute value of the injected charge measured with the studied technique is pretty accurate.

C. PPD CAPACITANCE
The buried photodiode capacitance C_{PPD} is an important parameter since is provides useful information on the PPD structure (e.g., its doping profile) or the charge handling capacity per unit area. It can also be used to verify if a TCAD
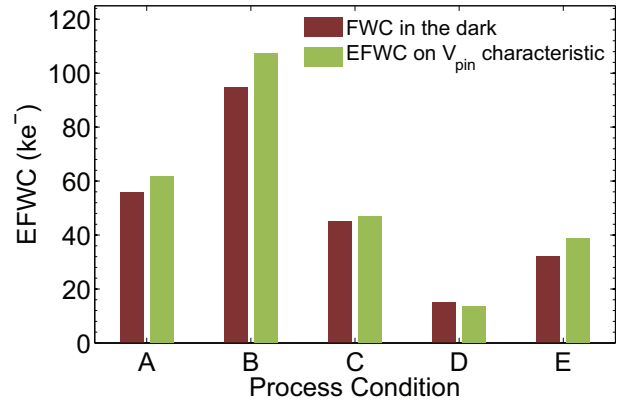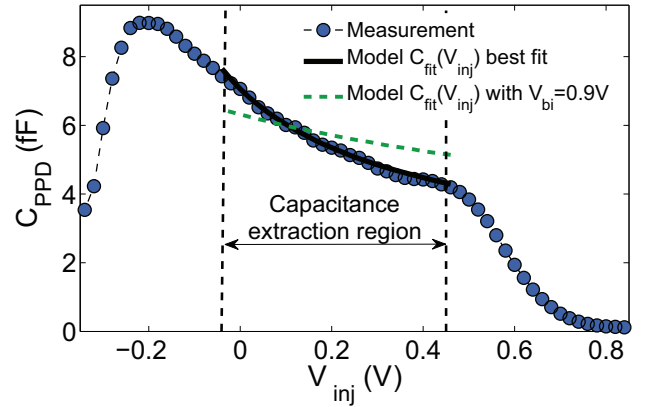

FIGURE 8. PPD capacitance extracted from Fig. 4 by computing the first order derivative. The capacitance extraction region is the region where the achieved capacitance value is supposed to be valid.

model of a PPD pixel corresponds well to the simulated manufacturing process.

However, this parameter is very difficult to reach in a CIS pixel array. In the following, we demonstrate that the PPD capacitance value can be extracted from the V pin characteristic. Indeed, differentiating (1) in region A of Fig. 4 gives:

$$C_{\text{PPD}}(V_{\text{inj}}) = \left|\frac{dQ_{\text{out}}}{dV_{\text{inj}}}\right|. \quad (5)$$

Hence, C_{PPD} can be plotted, as a function of the PPD channel potential (V_{inj} here), by computing the slope of the V_{pin} characteristic in region A. The result is presented in Fig. 8.

It appears that these assumptions are valid only in a limited region. When V_{inj} is too close to V_{pin}, thermionic injection contributes too much to the injected charge for (1) to be valid. On the other hand, when V_{inj} becomes too negative, the charge injected in the PPD is larger than the EFWC and the PN junction forward current discharge quickly the photodiode. It leads to increasing uncertainties on C_{PPD}
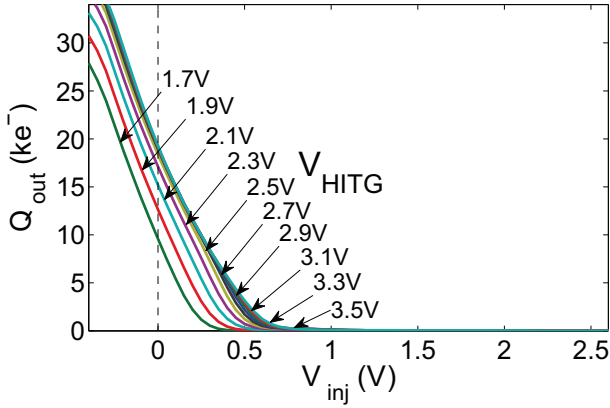
FIGURE 9. Pinning voltage characteristic measured for several V_{HITG} values.

FIGURE 10. Magnification of Fig. 9 to highlight the effect of V_{HITG} on the charge partition regime.

when V_{inj} is decreased below 0 V. Another phenomenon that leads to erroneous capacitance values is the saturation of the injected charge at negative V_{inj} values. It can be due to the readout chain saturation or to a too high forward current preventing further charge injection. This parasitic effect occurs around -0.2 V in Fig. 8. For this device, it leads to a valid capacitance extraction range of about -50 mV to $+450$ mV.

In this voltage region, the estimated capacitance value has been fitted by an analytical model. As a first approach, the ideal 1-D P-N junction model gives [17]:

$$C_{fit} = A_{PPD} \times \sqrt{\frac{q\epsilon_{Si}N_{PPD}}{2(V_{bi} + V_{inj})}} \qquad (6)$$

The two free parameters that can be adjusted are N_{PPD} and V_{bi}. The best fit is achieved with $N_{PPD} = 4 \times 10^{16}$ cm^{-3} and $V_{bi} = 0.27$ V and the result is presented in Fig. 8. The analytical model describes very well the evolution observed in the validity range. However, despite the fact that the N_{PPD} and V_{bi} values are in the right order of magnitude, they are far from the expected values. These discrepancies are most likely due to the limitations of this ideal 1-D P-N junction model to describe a complex and narrow 3-D pinned photodiode capacitance with non-uniform doping profiles. Using a more realistic 3-D model would most likely yield much better results and this approach will be studied in future work.

It is interesting to notice that by forcing V_{bi} to a more realistic value ($V_{bi} = 0.9$ V), the achieved N_{PPD} is about 10^{17} cm^{-3}, which corresponds fairly well to the expected range of doping concentration. However, with such V_{bi} the overall fit is pretty poor (as shown in Fig. 8). In the following, (6) will be used with the best fit values ($N_{PPD} = 4 \times 10^{16}$ cm^{-3} and $V_{bi} = 0.27$ V) since the overall trend of the model is in good agreement with the data.

D. TG THRESHOLD VOLTAGE AND CHANNEL DOPING
The TG-FD structure behaves as a gated diode: a MOS capacitor in which an N+ region is adjacent to the gated P-type region. In such a device, the gate voltage $V_{HITG|inv}$

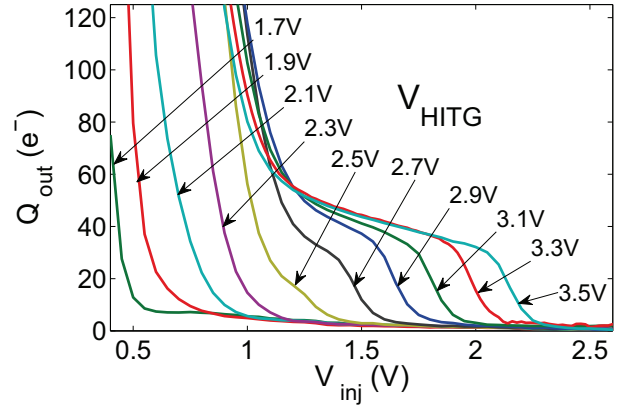required to reach the strong inversion regime is given by (Eq. 21 in [18]):

$$V_{HITG|inv} - V_{FB} = V_{inj} + 2\phi_B$$
$$+ \frac{\sqrt{2q\epsilon_{Si}N_a\left(V_{inj} + 2\phi_B\right)}}{C_{ox}} \qquad (7)$$

where V_{FB} is the flatband voltage and can be expressed as [17] $V_{FB} \approx \phi_{MS} = -0.56 - \phi_B$ in volts, if the interface state charge is neglected. The Fermi potential ϕ_B is given by [17] $\phi_B = \frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right)$.

According to the definition given in Section III-B, at the strong inversion threshold the injection voltage V_{inj} is equal to the TG channel potential $\phi_{TG|inv}$. Hence, (7) can be rewritten as a function of $\phi_{TG|inv}$:

$$V_{HITG|inv} - V_{FB} = \phi_{TG|inv} + 2\phi_B$$
$$+ \frac{\sqrt{2q\epsilon_{Si}N_a\left(\phi_{TG|inv} + 2\phi_B\right)}}{C_{ox}} \qquad (8)$$

From this formula, it is possible to express the TG threshold voltage, V_{th}, as a function of the TG channel potential at inversion:

$$V_{th} = V_{FB} + 2\phi_B + \frac{\sqrt{2q\epsilon_{Si}N_a\left(\phi_{TG|inv} + 2\phi_B\right)}}{C_{ox}}, \qquad (9)$$

by taking

$$V_{th} = V_{GS|inv} = V_{HITG|inv} - \phi_{TG|inv}. \qquad (10)$$

If we keep in mind that the TG channel potential is equal to the FD potential, this equation corresponds to the well-known definition (3.44 in [17]) of the threshold voltage in a MOSFET when a non-zero substrate bias is applied (i.e., with body effect).

We have seen in Section III-B and in Fig. 4 that the TG channel potential at inversion $\phi_{TG|inv}$ can be extracted from the pinning voltage characteristic. Therefore, measuring the V_{pin} characteristic for several V_{HITG} values should allow to plot (9) and retrieve the TG threshold voltage.
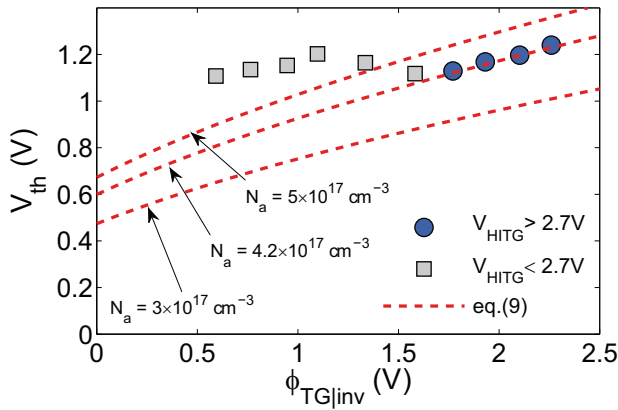
FIGURE 11. TG threshold voltage as a function of the TG inversion channel potential. $\phi_{TG|inv}$ is extracted from Fig. 10 by taking the V_{inj} value at which the charge partition step is observed. Threshold voltage data are obtained by using $V_{th} = V_{HITG|inv} - \phi_{TG|inv}$ with $V_{HITG|inv}$ the V_{HITG} value at which $\phi_{TG|inv}$ is measured. Data measured for $V_{HITG} > 2.7$ V are considered valid. Data measured for $V_{HITG} < 2.7$ V are not supposed to be reliable because the overall characteristic is distorted by the TG voltage in this regime.

The result of such measurement is presented in Fig. 9. For the highest V_{HITG} (2.7 V and above), there is no noticeable change. Below 2.7 V, the characteristic starts to slightly shift to the left. Further insight into this phenomenon is provided by the magnification presented in Fig. 10. It appears that for V_{HITG} above 2.7 V, the charge partition plateau can be observed whereas it vanishes for lower V_{HITG}. It means that when $V_{HITG} > 2.7$ V the TG channel potential at inversion $\phi_{TG|inv}$ is larger than the voltage at which the thermionic injection dominates. On the other hand, when $V_{HITG} < 2.7$ V, the TG inversion channel potential $\phi_{TG|inv}$ is so low that as soon as the inversion channel is created (i.e., when $V_{inj} \approx \phi_{TG|inv}$), thermionic injection dominates and the small charge partition contribution is not visible anymore. For even lower V_{HITG}, $\phi_{TG|inv}$ starts to have an influence on the whole V_{pin} curve by shifting it to the left leading to unreliable parameter extractions. This parasitic effect will be discussed more in details in Section V-C.

The data of Fig. 10 are compared to the ideal expression (9) in Fig. 11. $\phi_{TG|inv}$ is extracted from Fig. 10 by taking the V_{inj} value at which the charge partition step appears (as discussed in Section III-B). For each V_{HITG} a $\phi_{TG|inv}$ value is extracted. The threshold voltage is then determined using (10) with $V_{HITG|inv}$ the particular V_{HITG} voltage at which $\phi_{TG|inv}$ has been measured.

The only parameter that is not known is the TG channel doping density N_a. Equation (9) is plotted for three N_a values. The theoretical expression fits very well the valid data[4] for $N_a = 4.2 \times 10^{17}$ cm^{-3} whereas a small change of the doping concentration leads to a very poor fit. With the optimum doping concentration value ($N_a = 4.2 \times 10^{17}$ cm^{-3}) we achieve a threshold voltage without body effect[5] equal to

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4. Data points measured for $V_{HITG} > 2.7$ V.

5. i.e., for a substrate bias equal to 0 V. This particular V_{th} value corresponds to the Y-intercept of the dashed line with $N_a = 4.2 \times 10^{17}$ cm^{-3} in Fig. 11.
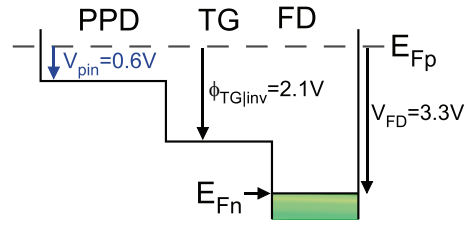

FIGURE 12. Reconstituted channel potential diagram of the studied pixel with the following conditions: the transfer gate is ON, $V_{HITG} = 3.3V$, the RST MOSFET is ON , $V_{DD\ RST} = 3.3V$ (hard reset hypothesis).
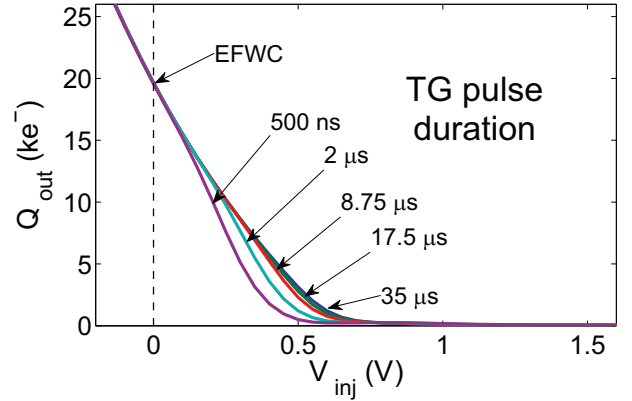

FIGURE 13. Pinning voltage characteristics measured for several TG pulse durations ($t_{TG|inj} = 35\ \mu s,\ 17.5\ \mu s,\ 8.75\ \mu s,\ 2\ \mu s$ and $0.5 \mu s$) during the injection phase.

0.6 V. It corresponds very well (less than 5% difference) to the V_{th} value given by the foundry. It shows that this measurement can directly provide the TG channel doping concentration and the threshold voltage value with a fairly good accuracy.

Thanks to the parameters extracted in this section, it is possible to reconstitute the whole potential diagram of a PPD-TG-FD structure. An example is shown in Fig. 12 for typical operating conditions ($V_{HITG} = 3.3V$, $V_{DDRST} = 3.3V$). Such diagram can be used to optimize the TG high and low bias levels without reducing the FWC or without reaching the spill-back regime that would reduce the transfer efficiency.

V. PARASITIC EFFECTS
The measurement of the pinning voltage characteristic is based on charge injection and charge readout through the TG. As a consequence, the TG performances and the way it is operated during the measurement could have an influence on the measured characteristic. Such possible parasitic effects are investigated in this section.

A. TG PULSE DURATION DURING INJECTION
Fig. 13 presents the pinning voltage characteristic measured with different TG pulse durations during injection $t_{TG|inj}$ (the readout TG pulse stays unchanged). It appears that this pulse duration affects strongly the thermionic injection region of the curve (i.e., the knee region) whereas it has no visible
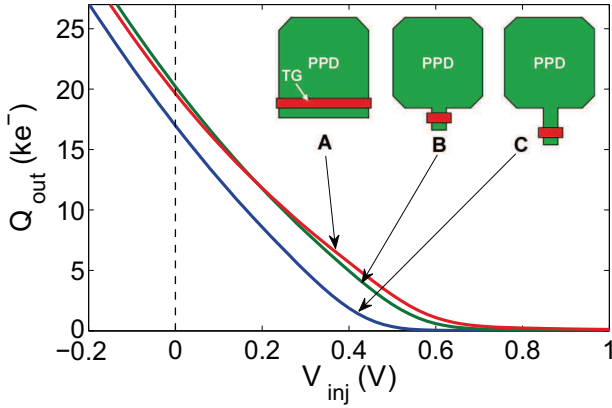
FIGURE 14. Pinning voltage measurement performed on three different pixel sub-arrays with different photodiode designs: A reference design studied here. B same as A with a bottleneck before the TG. C same as B but with a longer bottleneck.
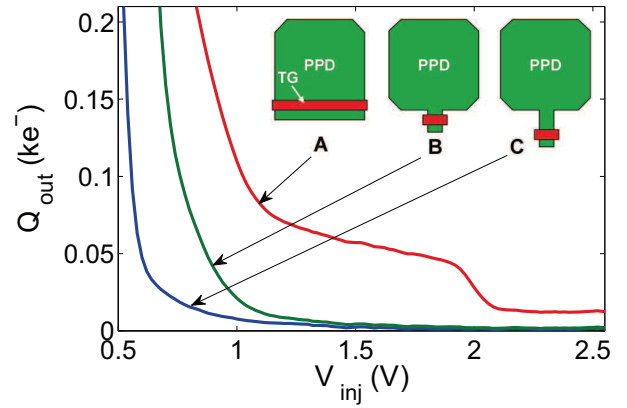

FIGURE 15. Magnification of Fig. 14 to highlight the effect of the photodiode design on the charge partition regime.

effects around the equilibrium FWC condition ($V_{inj} \approx 0$ V), where direct injection [Fig. 5(d)] dominates. This observation is in good agreement with (3) since the shorter the injection TG pulse duration, the lower the injected charge by thermionic injection. The injected charge starts to saturate for TG pulse longer than 17.5 μs leading to almost no change between the curves achieved with $t_{TG|inj} = 17.5$ μs and $t_{TG|inj} = 35$ μs.

The fact that this saturation effect is not described by (3) can possibly be due to the simplifying assumptions used previously. Indeed, to introduce (3) it has been assumed that all the electrons injected into the PPD by thermionic emission stayed in the PPD during the TG pulse duration. However, when $t_{TG|inj}$ is long enough (longer than 17.5 μs), the injected charge becomes significant and a current also flows from the PPD to the FD to empty the PPD. This current compensates the thermionic emission current from the TG to the PPD. According to the results presented in Fig. 13, an equilibrium is reached for $t_{TG|inj} > 17.5$ μs, leading to an apparent saturation of thermionic injection for long $t_{TG|inj}$.

It can be concluded that the effect of injection TG pulse duration confirms the hypothesis made on the dominant injection mechanisms that are involved in this measurement (summarized in Fig. 5). It also shows that to perform reliable and reproducible pinning voltage characteristic measurement, one should choose an TG injection pulse duration long enough to insure that the equilibrium is reached in the thermionic injection region (for TG pulse longer than ≈ 17 μs here), and thus, that the achieved characteristic does not depend on the selected $t_{TG|inj}$. It should be emphasized that, whereas the extracted PPD capacitance and pinning voltage could be affected by $t_{TG|inj}$ if not well chosen, the EFWC value is independent of this parameter.

B. CHARGE TRANSFER EFFICIENCY
The tested pixel sub-array exhibits a good charge transfer efficiency (CTE). However, it may not always be the same

and the effect of a poor charge transfer efficiency on the V_{pin} characteristic needs to be analyzed. In order to degrade the CTE, a potential barrier has been created by designing a bottleneck before the TG[6] in two other pixel sub-arrays of the same CIS, as shown in Fig. 14. Layout A corresponds to the pixel studied in the rest of this article. Pixel B has a short bottleneck and pixel C a longer one. The charge transfer inefficiency (CTI) of layout A, B and C were estimated to be respectively: $< 0.5\%$, 3% and 7% for a signal level about EFWC/2. This corresponds to the expected effect: the longer the bottleneck, the higher the potential barrier, and the higher the CTI.

The comparison of the V_{pin} measurements performed on the three pixels is presented in Fig. 14. Several differences appear between the three pixel responses despite the fact that the PPD pinning voltage is supposed to be the same. First, the EFWC of pixel B is slightly higher than the one of the reference pixel A. This small difference is due to a slightly larger PPD area in pixel B compared to pixel A. Second, the pixel B V_{pin} curve is slightly shifted to the left, suggesting a pinning voltage reduction. This effect is even more pronounced on pixel C with an apparent V_{pin} decrease of about 200 mV. It is worth noticing that this shift is so important in pixel C that it also leads to an apparent EFWC decrease of more than 10% whereas the EFWC of pixel C should be very close to the one of pixel B.

The observed V_{pin} shift that increases when the transfer efficiency drops is due to the combined effect of both:

- an incomplete charge transfer that leads to an under-estimated signal at the sensor output in pixel B and C (leading to apparent reduced full well capacity),
- and the fact that the voltage at which the direct injection regime starts is not the pinning voltage anymore but the potential of the electrostatic barrier created by the bottleneck. In other words, if a significant potential barrier exists, this pinning voltage extraction technique

6. It is well known that reducing the width of a PPD leads to a pinning voltage reduction [5], and thus to the creation of a potential barrier here.
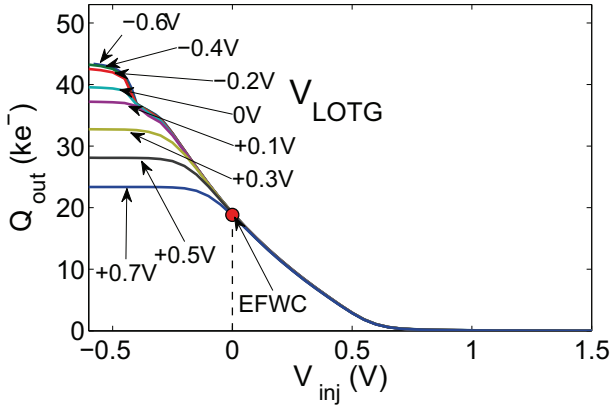
FIGURE 16. Pinning voltage characteristic for several V_{LOTG} values.

FIGURE 17. Magnification of Fig. 16 to highlight the effect of V_{LOTG} on the charge partition plateau.

provides the barrier potential instead of the pinning voltage.

Another significant effect can be seen in the magnification presented in Fig. 15. When a significant potential barrier exists (pixel B and C) the charge partition plateau completely disappears. This is in good agreement with the charge partition hypothesis since a potential barrier prevents the electrons stored in the inversion channel to flow back to the PPD. This interesting phenomenon can be used to highlight the existence of a potential barrier in a PPD-TG structure.

As a conclusion, it appears that using this characterization technique on pixels with poor CTE will lead to inaccurate parameter extraction. However, it seems that for CTI up to a few percent, the influence on the extracted value is still acceptable (below a few percent inaccuracy).

C. TG BIAS LEVELS

The effect of V_{HITG} on the pinning voltage characteristic has been previously presented in Fig. 9. As stated in Section IV-D, there is no obvious effect of the transfer gate ON voltage as far as the transfer gate channel potential at threshold $\phi_{TG|inv}$ stays well above the pinning potential. This condition is satisfied here for $V_{HITG} > 2.7$ V. This first result shows that the determination of V_{pin}, EFWC and C_{PPD} is not influenced by V_{HITG} (if higher than 2.7 V) and thus that there is no significant parasitic coupling effect due to the high value of the TG pulse voltage.

The same conclusion can be drawn on the effect of the TG OFF voltage V_{LOTG} on the extraction of these PPD physical parameters as illustrated in Fig. 16. Indeed, whatever the V_{LOTG} value, there is no change in the part of the characteristic that is used to extract V_{pin}, EFWC and C_{PPD}. Hence, it can be concluded once again that the influence of coupling effects induced by the TG pulse are insignificant. There is however, a strong effect for negative injection voltages. This expected result is explained by the fact that the maximum amount of charge that can be stored in the PPD decreases when the TG OFF increases [9], [19]. There is almost no
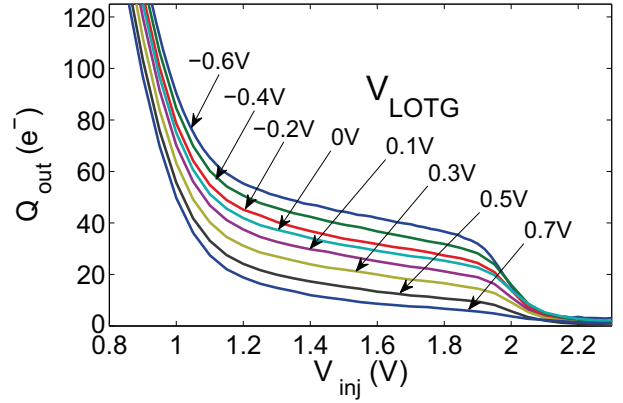
change between -0.6 V and -0.4 V because the TG channel is in the accumulation regime for both voltages and the FWC is then limited by the PPD forward current [9] which is independent of V_{LOTG}. When V_{LOTG} rises above -0.4 V, the saturation charge decreases rapidly because the FWC is in this case limited by the TG subthreshold current [9], which increases exponentially with V_{LOTG}.

Fig. 17 presents a magnification of the same measurement focused on the charge partition regime of the characteristic. It is interesting to notice that the charge partition amplitude is strongly affected by the V_{LOTG} value whereas V_{HITG} had no obvious effect on this amplitude (see Fig. 10). It means that the TG OFF voltage value determines how much charge will be injected into the PPD through the charge partition mechanism: the lower V_{LOTG} the larger the injected charge. The most probable explanation is the reduction of fall time derivative (i.e., a steepest falling edge) when V_{LOTG} is decreased[7]. It leads to a faster collapse of the electric field lines in the TG channel. This rapid disappearance of electric field reduces the number of electrons evacuated by drift to the FD, so more remaining electrons in the channel can diffuse to the PPD. This hypothesis could be easily checked by varying the fall time of the TG pulse but such feature was not available on the tested device and will be investigated in future work.

It is worth noting that to extract properly the TG threshold voltage it is better to use a sufficiently low V_{LOTG} value (or steep TG pulse falling edges) to enhance the charge partition mechanism.

VI. OBJECTIVE PINNING VOLTAGE EVALUATION

According to the previous discussions and especially the previous section, extracting the pinning voltage may not be

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7. If this hypothesis is correct, it means that V_{LOTG} has an influence on the falling edge rate whereas V_{HITG} has none. Electrical simulation were performed on the last stage that drives the TG and the results were in good agreement with the observed effects: varying V_{HITG} between 2.5 and 3.5 V had no significant effect (less than 5%) on the slope of the falling edge whereas varying V_{LOTG} from 0 V to -0.7 V led to 50% increase of the falling edge rate.

as simple as finding the knee on the curve as suggested in [8]. First, the following experimental conditions shall be met:

- the TG pulse duration $t_{TG|inj}$ must be long enough (about 17 μs here) to avoid the distortion presented in Fig. 13
- the charge transfer efficiency must be good enough (better than 99%) to avoid the apparent V_{pin} reduction presented in Fig. 14
- V_{HITG} must be high enough (higher than +2.7 V here) to insure that $\phi_{TG|inv}$ is well above V_{pin}
- V_{LOTG} must be low enough (lower than +0.7 V here) to insure that the injected charge is kept in the PPD until readout.

Second, finding the knee in the curve is not straightforward mainly because the evolution with V_{inj} in the knee region is exponential. It means that the knee voltage value depends on the scale of the plot, as can be seen in Fig. 4 by comparing the position of the knee in the inset (around 1 V) to the knee voltage in the full scale plot (around 0.5 V).

Another approach is to find a reliable point on the characteristic and to determine V_{pin} relatively to it. The most reliable point is the one corresponding to the EFWC condition (i.e., for $V_{inj} = 0$) since it has been validated by independent measurements and since it is less influenced by the parasitic effects (previously mentioned) than other parts of the curve. The most straightforward is to neglect the capacitance variations for V_{inj} between 0 and V_{pin} and to perform a linear extrapolation of the stored charge:

$$Q_{LIN}(V_{inj}) = Q_{EFWC} + \left.\frac{dQ_{out}}{dV_{inj}}\right|_{V_{inj}=0} \times V_{inj}. \quad (11)$$

In this case, the extracted pinning voltage value is $V_{pin–LIN} = V_{inj}$ when $Q_{LIN} = 0$ (i.e., the X-intercept of the Q_{lin} function).

A more rigorous approach is to use (4) by replacing C_{PPD} by the capacitance expression given by the 1-D ideal model (6). The parameters of (6) are adjusted to achieve the best capacitance fit in the direct injection regime, as discussed in Section IV-C. It is then possible to perform an integral extrapolation of (4) from $V_{inj} = 0$ to $V_{inj} = V_{pin}$:

$$Q_{INT}(V_{inj}) = Q_{EFWC} - \int_{V_{inj}}^{0} C_{fit}(V)dV \quad (12)$$

The pinning voltage estimated with this objective method is $V_{pin–INT} = V_{inj}$ when $Q_{INT} = 0$ (i.e., the X-intercept of the Q_{INT} function).

A comparison of these two methods is presented in Fig. 18. The linear extrapolation underestimate V_{pin} by more than 30% and it shows that the capacitance variation has to be taken into account to extract V_{pin} properly. As expected, the integral extrapolation leads to a very nice fit of the Q_{out} curve in the direct injection regime and allows to find an objective V_{pin} value, independent of the plot scale, near the thermionic
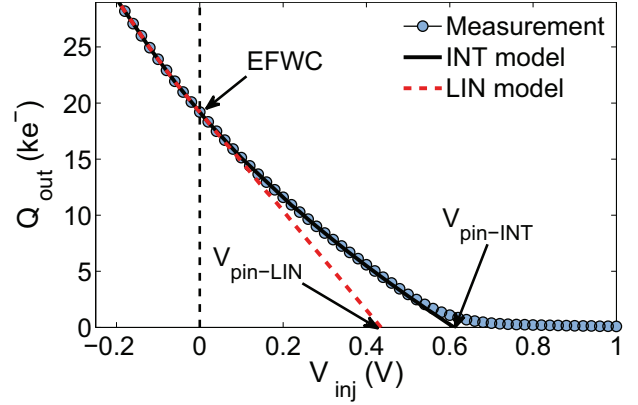

FIGURE 18. Comparison of the two proposed pinning voltage estimation techniques. $V_{pin – LIN}$ is determined thanks to a linear extrapolation from the EFWC condition (i.e., for V_{inj} = 0). $V_{pin – INT}$ is achieved by using the integral extrapolation described by (12).

emission region. Therefore, to perform objective comparison between several sensors or on a single solid-state sensor but with different experimental conditions (e.g., temperature, electrical stress...) the integral extrapolation method is highly recommended.

VII. SUMMARY AND CONCLUSION

The benefits and limitations of the pixel level pinning voltage extraction method proposed by Tan, Buttgen and Theuwissen [8] have been studied. The original purpose of this technique was to estimate the pinning voltage in a CMOS imager directly at the output of the solid-state sensor, without requiring the use of additional test structures.

In the presented study, a description of the different regimes that occur during this measurement has been proposed. It is shown that a charge partition regime appears on this characteristic and that it can be used to analyze the structure of the PPD. The presented experimental results also demonstrate that much more than the pinning voltage can be extracted from this plot:

- the PPD capacitance value (as a function of the charge stored in the PPD) can be retrieved from the slope of the curve whereas this parameter is difficult to reach otherwise
- the equilibrium full well capacity can be measured in a few minutes or seconds whereas the classical method requires the acquisition of dark frames for very long durations (up to several hours)
- the TG channel potential at a given TG voltage can be determined by detecting the beginning of the charge partition regime. This last result can be used to determine with a good accuracy the TG threshold voltage

Some limitations of the technique have been explored and it appears that:

- there is no obvious limitation due to electrical coupling induced by the TG pulse

- the TG pulse duration shall be long enough to insure a good injection (typically more than 10–20 μs)
- the technique is only accurate on CMOS pixel arrays with reasonable charge transfer efficiency (above 99%)
- the high and low value of the TG pulse must be chosen carefully to allow a good injection and a good charge handling capacity (i.e., V_{HITG} near the supply voltage and V_{LOTG} below zero if possible).

An objective V_{pin} extraction technique that is independent of the plot scale has been proposed for sensor to sensor comparisons.

The proposed PPD physical parameter extraction technique can have various applications. Its ability to reach these parameters inside a real sensor environment with a single fast measurement could be a significant benefit for:

- CIS manufacturing process developments
- CIS product and prototype characterizations
- CIS design validations
- imager health monitoring when exposed to degradation sources (hot electrons, aging, light induced degradation, temperature induced stress, high energy particles and radiation effects...)
- PPD modeling projects
- etc.

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