New Detector Technologies

for

Astronomy

A Thesis submitted for the Degree

of

Doctor of Philosophy of the University of London

by

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1997

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Abstract

This work contains a description of studies undertaken with the objective of improving the efficiency of astronomical instrumentation, particularly in terms of telescope-time usage. The primary technology discussed is the focal plane detector mosaic. A complete description of this new concept is given, covering the relevant background topics, including: image sensors; ranging from infra-red to X-ray wavebands, medium and large sized optical telescopes, imaging systems, spectrographic instruments and work in other related areas, for example; fibre-optics, medical imaging applications, remote sensing. Working prototypes of system components, embodying the new techniques developed are described. Results of tests including the system parameters: instrument noise, detector noise, detector cross-talk and detector linearity are given. A comparison of two alternative strategies for the operation of a focal plane detector mosaic is made. Software, including a novel detector control language and compiler developed specifically for the control of the system is discussed. Code portability is stressed. Collaborative work with an industrial partner (EEV Ltd.) on a unique four-side buttable imaging charge-coupled device is described. Observations on likely future developments in the field are included as part of the concluding remarks.

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Instrumentation for Astronomy: Recent Developments and Future Requirements

1.1 Introduction

Astronomy, unlike many of the sciences, is largely an observational discipline. Astronomers are not able to conduct experiments with their subjects. These two facts have had many consequences for the history of astronomy as a science and for the world in general. Astronomy is often said to be the oldest science, this seems likely as any inquisitive soul will wonder at the night sky. There are many documented cases in history of unfortunate predictions based upon astronomical observation and theory. The most profound of these theories are the bases of many religions.

The first instruments used for astronomical observation were astrometric; their purpose often being to chart the passage of time. Around the turn of the seventeenth century a fundamental addition to the techniques of astronomy was made: Galileo Galilei used the telescope to study celestial bodies. Since Galileo's time astronomical theories and instruments have developed in a symbiotic manner, theories being confirmed by instruments (for example, the discovery of the planet Neptune) and instruments being built to test theories.

Today, optical telescopes are still the workhorses of astronomical observation, but the range of the spectrum under study has expanded greatly. Information is also obtained with instruments ranging from radio telescopes to large vats containing cleaning fluid.[1] There are two main directions in which instrumentation for astronomy can be enhanced. The first of these can be broadly called sensitivity; the ability to detect fainter objects and to improve the resolution of information obtained. The second is in 'multiplexing'; to increase the number of objects about which there are data and the rate at which data are obtained. Instrumentation to cover un-observed regions of the electromagnetic spectrum has been an important area of expansion in the past. In the future, a greater amount of data will be collected by improving instrumentation for 'known' regions of the spectrum than by expanding spectral coverage—most of the useful electromagnetic spectrum has been observed at some time or other already.

This work is primarily concerned with the technology of the next generation of astronomical instruments, in particular, with the detectors which will be available and how best to utilise them. The technologies which will be discussed have applications in the optical part of the spectrum, and also the infrared, ultraviolet, X-ray and gamma ray regions of the spectrum. The emphasis is on optical uses however.

To frame this work, the rest of this Chapter is devoted to a general description of existing and planned astronomical instrumentation and detectors in widespread use in the community. The scientific purpose of much of this technology is outlined in the following section.

1.1.1 Astronomical Requirements of Instrumentation

The ultimate purpose of instrumentation built for astronomical observation is to increase our understanding of the universe. The design and specification of an instrument is largely determined by the scientific objectives of the user community for whom the instrument is intended. To illustrate this in a general sense, some of the current scientific objectives of astronomy in several fields are outlined below. Some specific examples are given. The consequent requirements, with particular regard to detectors, are then explained.

[1] The chemical used for neutrino detection is CCl_4, Carbon tetrachloride.

1.1.1.1 Some Current Scientific Objectives

Astronomical research can be considered to fall into one of four areas:

Solar System Studies of the geology, meteorology, composition and interaction of the solar system's component parts.

Interstellar Studies of the gas and dust found in the spaces between stars. Commonly known as the interstellar medium (ISM).

Stellar Studies of the formation, evolution, structure and composition of stars.

Extragalactic Studies of other galaxies, galactic clustering, the large-scale structure and origin of the universe.

These areas can all benefit from improvements in astronomical instrumentation. Several very large telescopes are now operational or under construction (see Section 1.2.3) as well as technological enhancements of existing telescopes and space observatories. Each area of astronomical study is now illustrated by example—it is beyond the scope of this work to discuss the scientific objectives of astronomy in detail.

Solar System studies are now dominated by space-based instrumentation and deep-space probes. Several missions to study the behaviour of planetary atmospheres, magnetospheres and the interaction between these systems and the Sun are planned or underway. These missions can benefit from reductions in instrument mass and power consumption, and also from improvements in instrument sensitivity.

Interstellar matter studies consider three basic types of material found in the interstellar spaces as follows[119].

Neutral diffuse matter: Optical and near infrared studies of interstellar absorption lines in the spectra of stars yield structure and composition data for neutral matter in clouds in the intervening space. Such studies can be photon limited, hence improvements in the photon collection rate by the use of larger telescopes and/or detectors will improve the understanding of this matter.

Ionized interstellar matter: This is an area of study of emission lines found in the visible to far infrared regions of the electromagnetic spectrum. Such subjects as the physical

and chemical composition of H II regions, planetary nebulae and supernova remnants are addressed. Lequeux[119] cites the faint [O III] 4363 line as the main temperature indicator for H II regions. High spatial resolution is important for study of the fine detail in such subjects. Another area benefiting from high resolution is the study of the kinematics of gas in galaxies, undertaken by obtaining velocity measurements based on Hα 6563 or other lines. These studies also require imaging spectroscopy (see Section 1.3.3).

Molecular clouds and dust: This area is often associated with studies of star formation. Most of the data on this subject are obtained by infrared observation, because such regions are opaque at optical wavelengths. The main interests are in the study of motions and shock waves in such clouds, molecular components and the nature of interstellar dust. These studies again benefit from imaging spectroscopy.

Stellar studies overlap with interstellar studies in the area of star formation. So called *protostars* are found embedded in dust and gas clouds and are observed in the infrared, millimetre and radio regions of the spectrum[131]. Optical studies of the pre-main-sequence phase of low-mass stars (mainly T Tauri type) require high-resolution spectroscopy, and, as such require the maximum possible light gathering power.

One of the most important techniques in stellar astrophysics is the study of open star clusters. All the members of such clusters lie at approximately the same distance and the light from them experiences a similar interstellar extinction. These features make an almost direct comparison of the stars' light possible. Such studies can benefit from an improvement in the limiting magnitude of observation[35] as more stars in the cluster can be investigated.

The field of **extragalactic** study is a wide one, which intrinsically concerns the most distant and faint objects observable. Much work is done on the subject of quasi-stellar objects or *quasars,* so called due to their star-like appearance on photographic plates. The light from quasars has travelled such a great distance that studies of the narrow absorption lines superimposed on their spectra by the intervening gas form an important part of the study of galaxies. The lines can be caused by either absorption in the halo of the quasar, by interposed galaxies or by intergalactic hydrogen—once the effect of the intra-galactic ISM is removed. Determination of the width of the absorption lines is difficult, requiring high-resolution spectroscopy[182]. Another study requiring high-

resolution spectroscopy is the search for the 'missing mass'. To estimate accurately the mass of a galaxy the velocities of subcomponents, assumed to be part of the galaxy, are measured. Such work is vital to map the the distribution of matter in large clusters.

When studying objects at the largest distances, the light is strongly redshifted, thus infrared observation becomes increasingly useful. Oke[136] noted the importance of charge-coupled device (CCD, see Section 1.4.2 for a description of these image sensors) for surveys of clusters of galaxies. These surveys can be undertaken with existing four-metre-class telescopes, but, for greatest efficiency, would benefit from increased detector pixel count.

1.1.1.2 Implications of Scientific Objectives for Detectors

Much of the scientific work mentioned above stands to be enhanced by the new very large telescopes. These telescopes give an improvement in resolving power and limiting magnitude as compared to the previous telescopes. To optimise the very large telescopes it is desirable to be able to use as much of the light in the unvignetted field as possible. One technique is the *serendipity* mode of observation where several of the instruments attached to a telescope are simultaneously used to observe field(s) around the target object; for example, one high-resolution spectrograph at the coudé focus and an imaging camera at another focus. An example of this technique is the Cardiff Hitchhiker camera for the William Herschel Telescope (WHT)[150]. The Hitchhiker is an off-axis CCD camera which is operated simultaneously with other instrumentation which use the light passing along the axis.

The main requirement for maximum utilisation of very large telescopes is imaging sensors with a high pixel count (total number of pixels in the detector). Detector technologies are discussed in Section 1.4; the main problem is that the most sensitive detectors do not have a sufficient pixel count to maximise the use even of four-metre class telescopes. Manufacturing detectors with arbitrary size and shape is the primary subject of this thesis.

Another area which is problematic is the size of available gratings. Spectrographs (see Section 1.3.2) for very large telescopes may require gratings larger than any which are manufactured at present. One solution is the use of mosaics of existing types of grat-

ings, a method which is becoming common at other levels in the design of astronomical instrumentation.

1.1.2 Instrumentation for Optical Astronomy

The technologies described in this work are, in the first instance, for optical and near-optical astronomy. A general tool for optical astronomy consists of five parts:

- Telescope: the principal optical component of the system.
- Instrument: normally sited at one of the foci of the telescope, the instrument processes the light beam produced by the principal optics to produce some information.
- Detector: part or all of the instrument itself, transducer of light into another form, usually an electrical signal.
- Interpreter: converts the electrical signal from the detector into a form which may be archived; normally digital data.
- Display: often a computer graphics terminal or print out, perhaps merely a table of numbers.

The distinction between these five parts is a real one; a change in one part can enhance the performance of the whole system. It is often possible to modify, for example, the detector part of an 'instrument' to achieve such an improvement, *without any other change.* Many observatories regularly interchange these parts to suit particular observing requirements, for example, moving an instrument to a different telescope, using different detectors for different astronomical objects and so on.

The remainder of this Chapter is devoted to a review of the first three parts of such a tool: the telescope, the instrument and the detector.

1.2 Telescopes

Modern telescopes are the result of years of planning and push mechanical and optical design to their limits. Earlier telescopes were, in their time, also the state-of-the-art.

This Section briefly reviews the development of the telescope and some of the variations on the basic concept.

1.2.1 A Short History of Telescopes for Astronomy[130]

The principle of the telescope is usually credited to Hans Lippershey[2], a Dutch spectacle maker, in 1608. Galileo was the first to use the new discovery to look at the skies. Galileo's instrument was a refracting telescope with an objective lens of about 2.5-cm diameter. For about sixty years refractors were used widely, making many discoveries, for example, the four largest moons of Jupiter and the rings of Saturn. The seventeenth-century refractors used single-element object lenses which were subject to chromatic aberration. To minimise this effect, lenses of enormous focal length were used. Hevelius' finest instrument, with which he produced the first chart of the Moon, was over forty-five metres in length!

Isaac Newton was the first to realise the use of a mirror to focus the light from a celestial object. His reflecting telescope, which had a 2.5-cm primary mirror made from speculum metal, was presented to the Royal Society in London in 1672. By the use of mirrors instead of lenses, the effect of chromatic aberration was completely removed.

Telescope construction remained unspectacular for more than a century after Newton's first efforts. In 1758 the instrument maker John Dollond began to manufacture lenses corrected for chromatic aberration. It was not long after that Herschel began to manufacture reflecting telescopes for his own use. Herschel's meticulous methods led him to the discovery of the planet Uranus and some fame, as well as the patronage of the King, George III. Herschel was the first to undertake the construction of large telescopes. Within ten years of his discovery of Uranus he had built a colossal telescope with a 1.2-m primary mirror, made of speculum metal. The telescope was built on a revolving platform, the main tube being supported at the top end by ropes slung from supporting ladders.

During the late eighteenth and early nineteenth centuries the two great telescope makers were Herschel and the German, Fraunhofer. Herschel was able to manufacture and sell

[2]Some research has suggested that the principle of the telescope was first discovered by two Englishmen named Digges around 1570.

reflectors, including four to the King for 600 guineas. Fraunhofer's finest instrument was the 24-cm Dorpat refractor which came into use in 1824. This telescope was also revolutionary in that it was motorised to track the motion of the sky.

Telescopic technology developed steadily during the nineteenth century. The use of photography from the mid-eighteen hundreds revolutionised astronomy itself.

At the turn of the twentieth century the largest telescopes were the one-metre Yerkes refractor, still the largest of its type, and the 1.83-m Rosse reflector. The Rosse reflector was the work of a wealthy landowner, the third Earl of Rosse, for his own scientific pursuits; as such it was not the best telescope of its time and was unused after his death in 1867, later being dismantled. The Yerkes refractor was the first ambitious project of George Ellery Hale. Hale gained the support of Yerkes, who was immensely rich, for the construction of the telescope. Hale was a visionary whose projects later led to the 2.54-m Hooker reflector on Mount Wilson, and the 5.08-m Hale Telescope on Mount Palomar, for many years the world's finest telescope. The 5.08-m telescope mirror weighs 20 tons and required more than a year to cool before it could be ground[146]. The Hale Telescope was first used in 1948, since when several telescopes of similar size have been built. The largest telescope in the world has, until quite recently, been the Soviet 6-m reflector. The late 1970s saw plans for telescopes of larger size emerge. The Keck Telescope being the first to become operational. Several projects to construct so-called 'very large telescopes' are under way. The telescopes range in size from the an eight-metre primary mirror up to a sixteen-metre equivalent. These, and other developments, such as the Space Telescope, infrared and millimetre-wave telescopes are discussed below.

Although not the primary subject of this work, it is important to note other telescope technologies. One of the most significant contributors to the astronomical data pool is radio astronomy. Radio telescopes and interferometric arrays of radio telescopes have proved useful for studying the centre of the galaxy as well as discovering pulsars and shedding light on the large scale structure of galaxies.

1.2.2 Four-Metre-Class Telescopes

With the advent of the so-called very large telescopes, existing large telescopes have been generally characterised as being of 'four-metre class'. The size of telescopes' primary

Telescope/observatory	Diameter/m	Primary Focal Ratio	Type
Bol'shoi Teleskop Azimutal'nyi Mount Pastukhov (USSR)	6.05	f/4.0	Altazimuth
George Ellery Hale Telescope Mount Palomar, California (USA)	5.08	f/3.3	Equatorial
Multiple Mirror Telescope Mount Hopkins, Arizona (USA) [3]	4.60	f/2.7	Altazimuth
William Herschel Telescope Roque des los Muchachos, Canary Islands (UK, NL, Spain)	4.20	f/2.0	Altazimuth
Cerro Tololo Interamerican Observatory Cerro Tololo, Chile (USA)	4.01	f/2.8	Equatorial
Anglo-Australian Telescope Siding Spring, NSW (UK, Australia)	3.88	f/3.3	Equatorial
Nicholas Mayall Telescope Kitt Peak, Arizona (USA)	3.80	f/2.8	Equatorial
Canada-France-Hawaii Telescope Mauna Kea, Hawaii (Can, Fr, USA)	3.60	f/3.8	Equatorial
European Southern Observatory Cerro La Silla, Chile (ESO)	3.57	f/3.0	Equatorial
New Technology Telescope European Southern Observatory Cerro La Silla, Chile (ESO)	3.50	f/2.2	Altazimuth

Table 1.1: Four-metre-class and large telescopes.[124][194]

mirrors covered by this term ranges from about 3.5-m to 4.5-m. The exceptions, *i.e.*, the existing very large telescopes, being the Hale five metre and the six-metre Soviet Bolshoi Alt-azimuth Telescope (BAT). These telescopes are listed in Table 1.1.

It is interesting to note the trend for smaller telescopes after the completion of the Hale reflector. These four-metre-class telescopes have, until relatively recently, used the

traditional equatorial mount.

Since the second world war, most of the developments in observing equipment for optical astronomy have been in the field of detectors and instrumentation. The advent of CCD and photon-counting-based instrumentation has now pushed four-metre-class telescopes to their limit, leading astronomers to propose new, larger telescopes. The main improvements gained by the use of larger telescopes are improved resolution and increased light-gathering power.

1.2.3 Very Large Telescopes

At the time of writing several groups are engaged in projects to build large telescopes. The work is at varying stages of progress. Currently the 10-m W. M. Keck II Telescope is under construction on Mauna Kea, Hawaii. This telescope is a 'twin' of the revolutionary Keck I which uses a segmented primary mirror. First light on the Keck I Telescope was in December 1990 when only nine of the thirty-six segments of the primary mirror were in place. The telescope has since been completed and is fully operational. Current very large telescope projects are summarised in Table 1.2.

It should be noted that the improvement in resolution which the construction of very large telescopes may offer can only be realised by the use of adaptive optics. Atmospheric motions cause the image of a star to be spread out, this effect is independent of the size of the telescope and generally limits the best resolution achievable to about a half of one arcsecond. This effect was one of the reasons for the construction of the 2.4-m Hubble Space Telescope (HST) which can achieve a 0.06 arcsecond resolution (see Section 1.2.4). Over the last ten years, advances, particularly in computer control technology have made the possibility of optics to compensate for atmospheric distortion a real one. It should be possible to achieve 0.1 arcsecond resolution from ground based telescopes using adaptive optics in the near future. The main contribution to the *seeing limit* is the motion of air within the telescope dome and structure, such effects are carefully considered at the design stage of modern telescopes.

The European Southern Observatory (ESO) VLT project uses four 8.2-m unit telescopes with the option of forming a 16-m equivalent mirror at a combined focus. This choice of configuration makes the step up in size from the existing four-metre class smaller than in

Telescope/Organisation	Equiv. Diam./m	Mirror type	Status
W. M. Keck I/CARA	10.0	segmented	operational
W. M. Keck II/CARA	10.0	segmented	construction
Multiple Mirror/Univ. Arizona	6.5	honeycomb	figuring
Japanese Nat. Large Telescope (Subaru)/Gov. Japan	7.5	meniscus	construction
German Large Telescope/ Gov. Germany	12.0?	meniscus/ segmented?	?
Spectroscopic Survey Telescope/ Univ. Pennsylvania, Univ. Texas	8.0	segmented	construction
Very Large Telescope (VLT)/ European Southern Observatory	16.0	meniscus	casting/ site preparation
Gemini (2)/NOAO, Gov. UK, Gov. Canada/Minor parties	8.0	meniscus	construction
Binocular Telescope/Gov. Italy, Univ. Ohio, Univ. Arizona,	11.9	honeycomb	design
Magellan/Canegie Institute, Univ. Arizona.	6.5	honeycomb	construction

Table 1.2: Very Large Telescope Projects.

the case of the Keck Telescopes which are a whole new technology. The ESO system will also be able to attempt interferometry, a technique for combining the images from two (or more) telescopes to approximate the resolving power of a single mirror of diameter equal to the distance between the two. Indeed, one of the motivations behind the construction of Keck II is the use of the twin telescopes (sited some 85m apart on Mauna Kea) as an interferometric instrument.

Existing very large telescope projects use three mirror technologies. The Keck Telescope, as mentioned earlier, uses a segmented primary mirror. Many small (of the order of one-metre equivalent diameter) mirrors are mounted on a motorised support structure which positions these elements so that they all focus light onto a single point. The four unit telescopes of the ESO VLT have meniscus mirrors. These are single pieces of glass (or

aluminium) which are too thin to support themselves. The mirror is supported on a set of mechanical actuators which deform the mirror to the correct shape. The third mirror technology is the honeycomb. A thin reflective surface is fixed to a glass honeycomb structure which gives the mirror a stiff structure and which is light in weight because most of its volume is air. The German Large Telescope is interesting in that it is planned to consist of an eight-metre meniscus mirror surrounded by small segments to make an instrument of total equivalent diameter 12.0m.

1.2.4 Other Telescopes

This Section is a collection of examples to demonstrate the range of telescopic instrumentation not described in the previous sections.

Schmidt telescopes, named after the pioneer of the Schmidt optical configuration, provide images of very large areas of sky. Two examples of Schmidt telescopes are the 1.83-m UK Schmidt Telescope (aperture 1.24m) at Siding Spring in Australia[157] and the 1.2-m Palomar Schmidt Telescope in California. These telescopes have been used to produce a complete survey of the celestial sphere in the red (R) and blue (B) wavebands. The unvignetted field in these two telescopes covers $6.4^o \times 6.4^o$ on the sky[157].

The **Hubble Space Telescope** (HST) is a significant astronomical tool for its envisaged lifespan. The telescope is a 2.4-m reflector with a full instrument package. The HST is free of the problems of seeing—atmospheric distortions of the telescope image, and as such should be able to achieve diffraction limited performance and resolution of about 0.06 arcseconds. The problem of atmospheric extinction, which makes ultraviolet and some infrared observations impossible from the surface of the Earth, is also overcome. The HST has a huge wavelength coverage from 0.115μm in the ultraviolet to at least 10μm in the infrared. The instrument package for the HST is a 'microcosmic' model for the basic instrument package of most large telescopes:

Wide-Field Planetary Camera (WF/PC II) uses light from the centre of the telescope light beam, the remainder is available for other instruments. The instrument, as its name suggests, has two modes of operation. In wide-field mode each pixel of the four 800×800 CCDs covers an area of 0.1 arcseconds square on the sky. In planetary mode the pixels are equivalent to only 0.046 arcseconds square, about

one tenth of the size used in imaging instruments for ground-based four-metre-class telescopes. The CCDs have been coated with the phosphor lumogen to improve their ultraviolet response[25].

Space Telescope Imaging Spectrograph (STIS) covers the spectrum from the ultraviolet (1150Å) through the visible, red and the near-IR (10 000Å). The STIS has three detectors: a cesium iodide photocathode Multi-Anode Microchannel Array (MAMA) for 1150–1700Å, a cesium telluride MAMA for 1650–310Å, and a CCD for 3050–10000Å. All three detectors have a 1024×1024-pixel format. The field of view for each MAMA is 25 arcseconds square, and the field of view of the CCD is 50 arcseconds square.

Near Infrared Camera and Multi-Object Spectrometer (NICMOS) provides the capability for infrared imaging and spectroscopic observation. NICMOS detects light with wavelengths in the range 0.8–2.5μm. The HgCdTe arrays which comprise the infrared detectors in NICMOS are operated at cryogenic temperature using frozen nitrogen ice.

Faint-Object Camera (FOC) is complementary to the WF/PC. As its name suggests, this instrument is intended for faint targets. The detectors used are photon counters (Section 1.4.3) which give superior ultraviolet sensitivity to CCDs. This combined with their zero readout noise makes the instrument ideal for the very faintest objects. The pixel size can be either 0.022 arcseconds square or 0.043 arcseconds square.

Faint-Object Spectrograph (FOS) had two detector systems based on the scanning vidicon type technology. One detector optimised for the blue part of the spectrum, the other for the red. The total wavelength coverage was from about 0.115μm to 0.8μm. This instrument was removed during one of the maintainence missions to HST.

High-Resolution Spectrograph (HRS) had a higher dispersion than the FOS giving greater detail in the spectrogram, at the expense of being only suitable for brighter objects. The detectors were similar to those in the FOS. This instrument was also replaced during one of the maintainence missions to HST.

The FOC has, in addition, a means of measuring light polarization; this subject is discussed in Section 1.3.3. Unfortunately, the telescope's initial instrument collection does not include any infrared detectors as the project was planned and completed before the new infrared sensors (see Section 1.4.4) became available. The next generation of instruments for HST include an infrared camera.

During 1983 the **IRAS** mission[8] proved to be a great success. This was an infrared space telescope. The primary mirror of IRAS was 0.60m in diameter; however, the design of the optical system reduced the effective light-collecting area to only $0.2m^2$, equivalent to a 0.25-m diameter mirror. The IRAS focal-plane assembly included detectors for $12\mu m$, $25\mu m$, $60\mu m$ and $100\mu m$ bands with which it undertook a virtually complete all-sky survey at a resolution of 4–6 arcminutes. The IRAS telescope was liquid-helium cooled; when the helium supply was exhausted the thermal background from the telescope became too great for any further observation.

A successor to IRAS, the **Infrared Space Observatory (ISO)** was launched in November 1995. The optical system is essentially similar to that of IRAS; however, the instrumentation package of ISO is considerably more advanced, a representation of the great advances in infrared imaging in recent years (see Section 1.3.1.2).

One of the most successful space observatories was the IUE (**international ultraviolet explorer**)[15][16]. By placing the telescope above the atmosphere the full UV region of the electromagnetic spectrum is made available for study. The telescope consists of a 0.45-m diameter mirror (central obscuration 0.22-m diameter) in a Cassegrain configuration of focal ratio 15. The on-board instrumentation includes two spectrographs and SEC vidicon cameras. The IUE was shutdown in September 1996.

There are several **infrared telescopes**, the largest of which is the United Kingdom Infrared Telescope (UKIRT) on Mauna Kea, Hawaii. UKIRT is a 3.81-m telescope[157][181]. The telescope was originally intended to be a low cost instrument, and to this end a thin mirror was used. The mirror has a mass of only 6.5 tonnes, about one third that of a typical four-metre-class telescope. The use of a light mirror and relatively fast focal ratio (f/2.5) allowed the telescope tube to also be of a low-mass design. Because UKIRT is used for infrared astronomy (typically in the $1\mu m$ to $35\mu m$ region of the electromagnetic spectrum), the less rigid mirror construction is not a problem for the accuracy of the

optical design. One of the most successful infrared imaging cameras, IRCAM, is in extensive use at UKIRT (see Section 1.3.1.2).

The **James Clerk Maxwell Telescope (JCMT)** is a **millimetre** and **sub-millimetre telescope**[157]. Like UKIRT, the JCMT is sited on Mauna Kea, Hawaii and is operated by the Royal Observatory, Edinburgh (ROE). The telescope is of a Cassegrain configuration with 15-m primary and 75-cm secondary mirrors. The telescope is important because it is one of the first successful examples of the use of a *mosaic* technology for astronomical instrumentation. The primary mirror consists of 276 panels arranged in seven rings. Each mirror-element has an area about one-metre square. The panels are constructed from an aluminium skin overlaying an aluminium honeycomb. Each panel is mounted on hydraulics which allow the element to be positioned to an accuracy of 3μm, the whole surface of the mirror being maintained within 38μm (rms) of a parabola[157]. Like UKIRT, the secondary mirror can be 'chopped' to subtract the sky background when observing with the JCMT. The JCMT is used for observations at wavelengths longer than the 35μm to 300μm region of the electromagnetic spectrum, wavelengths to which the Earth's atmosphere is mostly opaque. Up to four receivers can be used simultaneously. In the near future several multiple-channel instruments will be commissioned for the JCMT which will improve its imaging capabilities even further[157].

1.3 Instruments

Most of the instruments in use for optical astronomy can be classified in one of two groups, namely imaging and spectroscopic. A few other types of instrument, such as polarimeters and interferometers are also important, these are described in Section 1.3.3.

1.3.1 Imaging Instruments

For centuries imaging has been the primary method by which astronomical data have been obtained. Imaging is essentially the mapping of the intensity of radiation as a function of co-ordinate in a particular wavelength band. Imaging can yield three basic types of information: morphological, the structure of the target object; astrometric, the location of the target object in a reference coordinate system; and photometric, the measurement

of the brightness of the target source against an agreed standard (these values may be time dependent).

Imaging instruments can be classified according to the wavelength band for which they are designed.

1.3.1.1 Optical Imaging Instruments

The nature of optical imaging instruments is fundamentally defined by the detector technology available. For example, for surveys and targets of large angular size, photographic plates remain the most efficient data collection medium. As mentioned in Section 1.2.4, Schmidt telescopes cover very large areas of the sky. Photographic plates approximately 35.6cm×35.6cm costing $200[171] each are used with the Schmidts, giving about 1000 times the data rate of a small-size (512×512 pixels) CCD. (This data rate is calculated as the product of the number of effective pixels and the quantum efficiency of the detector, for the case of a hypersensitised Kodak IIIa-J photographic emulsion[124].) The Schmidt/photographic emulsion is a powerful imaging system and can be used for near-infrared imaging in addition to optical work. The photographic emulsion is currently the detector of choice for such wide-field work, simply because it is the only detector of sufficient size and resolution.

Most of the imaging instruments currently in use are based upon the charge-coupled device. The CCD camera is usually placed at either the prime or Cassegrain focus of a telescope depending on the application. The prime-focus cameras have a larger field of view than the Cassegrain cameras, typically about 300 arcseconds, which is ideal for faint objects. Cassegrain cameras have a higher resolution for better sampling of the blurred seeing disk of the subject. Such cameras will include a set of filters, usually mounted in a rotating wheel, to sample different regions of the spectrum. The filter wheel is placed in front of the detector which will itself be mounted in a vacuum cryostat (the technicalities of CCD cameras are discussed in Chapter 2). CCD-based cameras are able to detect very faint objects and stretch the capabilities of the existing four-metre-class telescopes close to their theoretical limits.

1.3.1.2 Infrared Imaging Instruments

The Earth's atmosphere is not uniformly transparent to infrared radiation. For this reason, much of the work done at infrared wavelengths has been done from balloons, rockets and more recently from space observatories such as ISO (see Section 1.2.4). Fortunately some of the infrared part of the spectrum is able to penetrate the atmosphere and these 'windows' include some important astronomical features. Traditionally the infrared part of the spectrum began at a wavelength of about 0.7μm, where the visual part of the spectrum (*i.e.* that detectable by the human eye) ends. More recently that part of the spectrum considered 'visual' has been extended by the CCD which is sensitive to wavelengths up to 1.1μm.

Infrared imaging is a relatively new technique. Imaging sensors for the infrared part of the spectrum have only reached a sufficient quality for astronomical applications in the last five years. The first common-user infrared camera for astronomy was the Royal Observatory, Edinburgh (ROE) IRCAM for the infrared telescope UKIRT. IRCAM was an enormous step forward in infrared technology; previously infrared images had been constructed by scanning a single infrared detector over the sky. IRCAM has detected sources of radiation as faint as the 21st magnitude.

A full consideration of infrared detector technology is given in Section 1.4.4.

1.3.1.3 Ultraviolet Imaging

The ultraviolet (UV) part of the spectrum is normally considered to cover wavelengths shorter than about 0.35μm. The Earth's atmosphere is completely opaque to wavelengths shorter than 0.30μm. To obtain data in the ultraviolet part of the spectrum the observatory must be situated above the atmosphere. Several successful UV spectroscopic space observatories have been established, including the International Ultraviolet Explorer (IUE) and Copernicus. The Hubble Space Telescope is another example; the Wide-Field/Planetary Camera (WF/PC) and Faint-object camera (FOC) are both UV capable. The FOC has a pixel size of only 0.022 arcseconds square.

The ubiquitous CCD is the detector used in the WF/PC, however, the FOC uses a photon-counting detector similar to the IPCS (see Section 1.4.3). Photon counters have

no readout noise and have, in the past, been preferred to CCDs when the subject is very faint.

1.3.2 Spectroscopic Instruments

A spectrographic instrument can be used to measure the intensity of radiation from a source in one or more regions of the spectrum. Usually the instrumental *profile* of a spectrographic instrument will be narrow, *i.e.,* the light detected in any particular region is fairly monochromatic. This is distinct from filter photometry which is described in Section 1.3.3.

1.3.2.1 Optical and Infrared Spectroscopy

The range of spectroscopic instrumentation in use for astronomy is very large; however, most of the instruments can be classified into one of the following areas.

- Lower-resolution faint-object spectrographs.
- Intermediate-dispersion spectrographs.
- High-resolution spectrographs.
- Imaging spectrometers.
- Fourier-transform spectrometers.

Each type of of spectrograph serves a different astronomical purpose. The greater the resolution of the spectrum required, the less the intensity of light in each wavelength range. This means that the very faintest astronomical objects, often those of most interest, must be studied at lower resolution.

Faint-object spectrographs are often constructed by placing a grating in the light path in front of a detector. This gives the highest possible transmission of the meagre signal by the use of as simple an optical configuration as possible (smallest number of elements). A prism is used as a cross-dispersing element and the Schmidt camera configuration is used.

The intermediate-dispersion spectrographs are the workhorses of astronomy. These can often be quite complex instruments as they must cater for a wide variety of observational requirements. The ISIS spectrograph for the WHT is an example of such an intermediate-dispersion instrument. ISIS is a double instrument—it has two spectrographs one optimised for the blue region and one for the red region of the optical spectrum, and, in addition, it has a faint-object spectrographic camera capability.

An example of a high-resolution spectrograph is the ultra-high-resolution facility for the University College London Échelle Spectrograph (UCLES-UHRF) at the Anglo-Australian Observatory. This instrument provides resolution of spectra to the diffraction limit of the AAT.

The imaging spectrometer produces a three-dimensional data set. Essentially, the spectrum for each point within a scene is obtained. An example of this type of instrument is TAURUS, based around a Fabry-Pérot interferometer (see later in this Section).

The need for data has prompted the development of several multiple-object spectrographs. These employ fibre-optic cables to route light from the focal plane of a telescope to the entrance slit of a spectrograph where the fibres are stacked up along the slit. The older multiple-object spectrographs used focal-plane assemblies which were prepared for each target field by hand. More-modern instruments such as the Steward Observatory MX[76] and the AAT AUTOFIB[138] and 2dF systems have automated fibre-positioning systems.

There are many techniques for realising a spectrographic instrument. The primary component of the instrument is the *dispersing* element; that part which separates light of different wavelengths. The main methods used are:

Grating Spectrographs A grating which consists of many narrowly spaced lines disperses the light by diffraction. The many wave-fronts which arise interfere to produce the resulting spectrum.

Prism Spectrographs One or more prisms disperse the light by refraction.

Fabry-Pérot Interferometer In this case, the primary component of the system is the *etalon,* a cavity formed by two high-reflectivity, low absorption face-to-face plates. The plates are held parallel to a very high accuracy. By changing the separation

of the plates the transmitted wavelength is altered.

The actual method used in an instrument is dependent upon the particular application. Each configuration has its own strengths. It is beyond the scope of this work to discuss the design of spectrographs for astronomy in detail. The reader is referred to the work of Diego[50] for such a discussion.

1.3.3 Other Instruments

This Section is not intended to be an exhaustive list of optical instruments not already covered; rather, some important specialised instruments are discussed.

One of the most important classes of instrument not mentioned above is the *polarimeter.* Some of the light arriving from celestial objects exhibits a degree of polarisation, often due to magnetic fields in the region from which the light was emitted. By measuring this polarisation astronomers can gain insight into the structure of the magnetic field. Polarimetry depends on relative brightness measurements on the same source[124]. A polarising element (*polaroid* or *polarisation modulator*) is placed in the light path and measurements of the intensity of transmitted light are taken for different degrees of rotation of the element. The polarising element can be made from a material which has a crystal structure which is *birefringent, i.e.,* sensitive to the orientation of the plane of vibration of incident radiation.

There are several *CORAVEL* (COrrelation RAdial VELocities)[51] type stellar doppler-shift measurement instruments. The operation of the CORAVELs is based on the cross-correlation of an échelle stellar spectrum with a mask. The CORAVELs are useful because they enable velocities of quite faint stars to be measured with telescopes of only modest size. There are CORAVELs in use at ESO in Chile, the Observatoire Haute-Provence in France and at the University of Cambridge 0.9-m Telescope in the UK.

Ground-based *Speckle cameras* overcoming the atmospheric distortion of light have been used[124]. The image of an astronomical object is blurred by the motion of the atmosphere. By using very short exposures (the technique can only be used for bright objects) the image motion is essentially frozen. Using several of these 'snap shots' and software to combine the data from each a near-diffraction-limited-resolution image can be con-

structed. Such cameras require a high magnification to achieve the necessary spatial sampling rate of the speckle pattern to construct the image.

Photometry is the technique by which brightness and waveband-brightness relations are measured. This is an important technique as it gives both qualitative and quantitative data about the target object. The basic purpose of filter photometry is to determine some aspects of a star's spectral nature by a simpler and quicker method than obtaining the spectrum. To enable data from different instruments to be compared, standards or references have to be agreed. The most commonly used system is the UBV system defined by Johnson and Morgan in 1953[104]. The definition is quite complex, requiring particular filter types, detector and telescope, thus data referenced against this standard must allow for variations from it. The UBV system is a three filter system, each filter's wavelength pass band roughly corresponding to the ultraviolet-violet, blue/photographic and red/visual (human eye) bands respectively. The basic UBV system has been subsequently expanded to include more bands at the red end.

1.4 Detectors

Only a few types of detectors are in extensive use for optical astronomy. The three primary detectors are: photographic emulsions, charge-coupled devices and photon counters. Several detectors for the infrared part of the electromagnetic spectrum have become available, and are discussed in Section 1.4.4. The emphasis in this work is on multichannel detectors or *imagers.* Single-channel detectors are used for accurate photometric measurements; however, the excellent quality of contemporary charge-coupled-device technology makes single-channel sensors almost unnecessary. Gamma-ray, X-ray and radio observations are often made using single-channel detectors, but this is beyond the scope of this work.

1.4.1 Photographic Emulsions

Photography has been an integral part of astronomy since about 1845. Even today when the majority of work uses solid-state detectors, the photographic plate is still the most effective way of exploiting the focal area of large telescopes. Once a photographic plate

has been exposed and developed the scientific data contained therein has to be extracted by some means. Several plate-measuring machines are in constant use for this purpose, including the ROE COSMOS machine. Plate-measurement machines, in simple terms, consist of an accurate (as a function of motion) jig to carry the plate and a *densitometer* which measures the density of the developed emulsion. The information so produced is then digitised and thus made available for analysis. Plates produced by the UK Schmidt Telescope are analysed using the SuperCOSMOS machine.

The maximum detective quantum efficiency for a IIIa-J type emulsion is about 2% (at a wavelength of about 500μm). The size of the *grains* or silver halide crystals in an emulsion is about 20μm^2[127]. This suggests that a region 1cm$\times$1cm of a photographic emulsion will contain about 2.5×10^5 photosites.

1.4.2 Charge-Coupled Devices

The first sentence of the original CCD paper reads: 'A new semiconductor device concept has been devised which shows promise of having wide application[20]'. Since their invention in 1970[4][20] charge-coupled devices (CCDs) have indeed found many uses. CCDs have had a profound effect on both imaging technology and applications; many imaging systems would simply not be possible without these devices. During the late 1970s the CCD was one of several image sensors in use for astronomical purposes, the others ranging from CIDs[101] (a related technology) and vidicon-type camera tubes to photographic plates. During the 1980s the CCD came to be the detector of choice for most instruments at many observatories. Even photon-counting systems (Section 1.4.3), which had used vidicon tube technology, now use the CCD as their light-to-signal transducer.

The main benefits of CCD technology for astronomy are:

- High quantum efficiency.
- Reproducible and linear photometric performance.
- Low noise.
- Wide range of spectral response.
- Stable geometry.

Mackay[122] described some of the uses of CCDs for astronomy, highlighting the detective quantum efficiency (DQE), which is higher for CCDs than for image intensifier or for photographic-based systems.

In 1987 when Mackay's article[122] was published, CCD readout noise levels were of the order of $10\text{–}50e^-_{rms}$. Currently, readout noise of the order of $\approx 5e^-_{rms}$[98] is regularly achieved, with the possibility of sub-electron readout noise devices in the near future [36][92]. Readout noise is the main limiting factor on the usefulness of CCDs for astronomical purposes—except for their small size. The progress being made in the reduction of readout noise suggests that these devices will be used even *more* in the future.

1.4.2.1 A Functional Description of the Charge-Coupled Device

There are many existing descriptions of the principles of operation, design and use of charge-coupled devices. The best of these include: EEV's *CCD Imaging* series[27]–[33], McLean[124], Mackay[122] and Janesick[89]. A short description of the operation of CCDs is given here for completeness.

Three principles are vital to the operation of imaging CCDs, these are:

- The photo-generation of electric charge in silicon.
- The technique of charge transport, *charge coupling,* which gives the devices their name.
- The conversion of information in the form of a charge into a voltage by means of the relation $V = Q/C$, where: V is voltage (Volts), Q is charge (Coulombs), and C is the capacitance (of the detector output node) (Farads).

A simplified cross-section of a CCD column is shown in Figure 1.1. The device is made on a silicon substrate. P-type, isolating *channel stops* run vertically along the device, forming a conducting channel. This is covered by an insulating layer of silicon oxide. Semi-transparent electrodes fabricated from polycrystalline silicon (polysilicon) run perpendicularly to the channel across the device.

Each electrode is equivalent to the gate of an MOS transistor. In the case of an imaging device, signal information is stored in the form of electrons (opposite polarity devices are

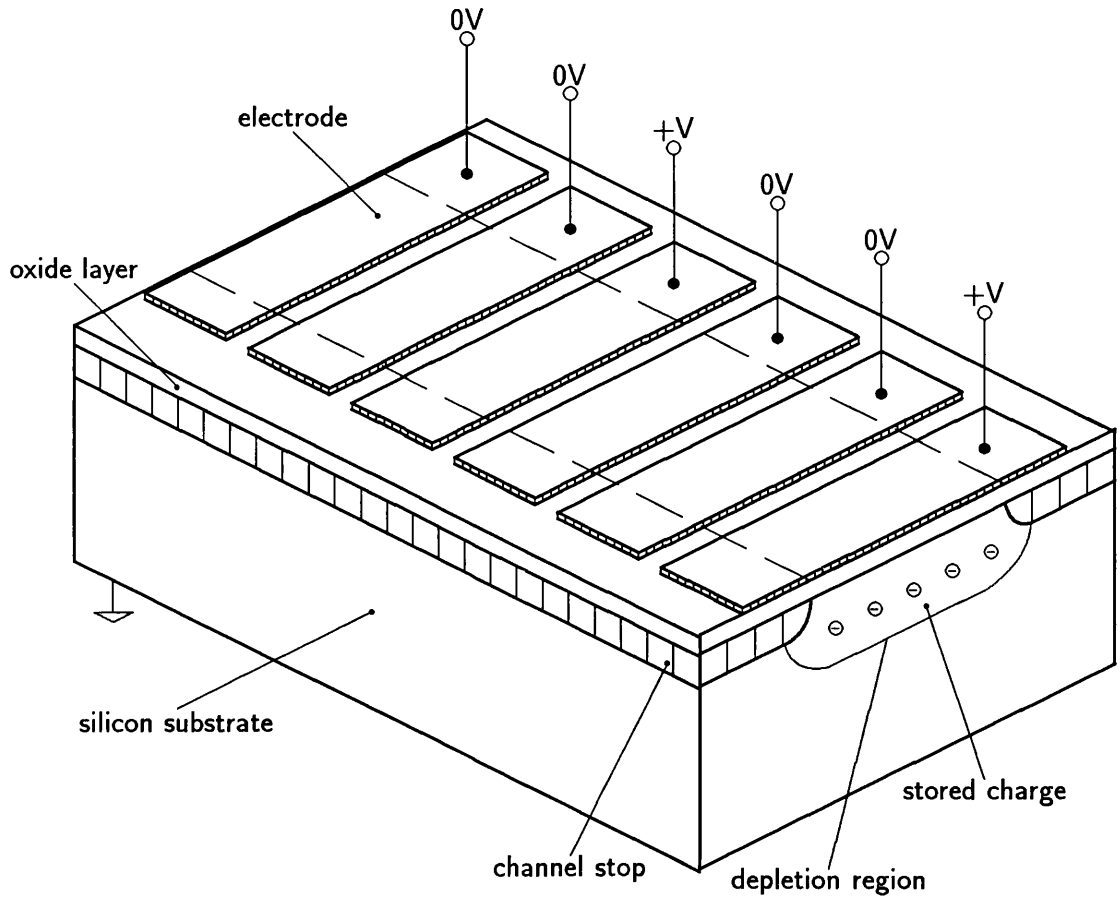

Figure 1.1: Basic structure of a charge-coupled device.[27]

also possible). Charge is localised in the substrate below the electrodes of the highest applied potential. This is because the underlying silicon is in depletion and assumes a positive potential with respect to regions below the adjacent, less potentive, electrodes.

Figure 1.2 illustrates the technique by which charge is transferred or *coupled* between adjacent electrodes. The charge is initially held beneath the electrode of the highest applied potential. The potential on one of the adjacent electrodes is raised and thus the region of the substrate in depletion is enlarged and the charge is spread over a larger volume. To complete the transfer, the potential on the first electrode is reduced and thus the signal charge moves with the depletion region to be localised beneath the second electrode. This is the technology which gives the charge-coupled device its name. Charge transfers are highly efficient, with virtually no loss or spillage of charge in modern devices.

Figure 1.3 shows schematically a 4×5 pixel two-dimensional CCD. The device consists

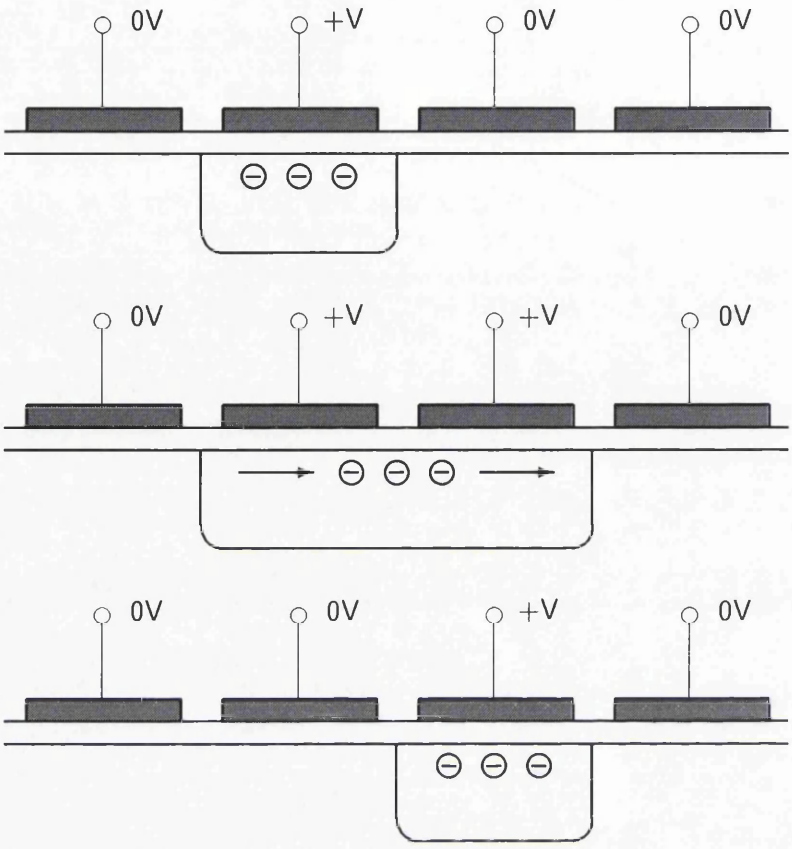

Figure 1.2: The technique of *charge coupling.*[27]

of two sets of electrodes. The first set runs horizontally across the image section of the device. The second set of electrodes run across a channel at one edge of the image section; this channel is the readout section. In both sections, each electrode is part of one of three groups arranged so that every third electrode is connected together. Such a device is known as a *three-phase CCD* because of the electrode interconnections. Devices using other architectures are common and are discussed in Section 2.2.3.

In Figure 1.3 the dashed lines mark the edge of the channel stops which restrict signal charge to the four columns of pixels, the readout section and the output node. The output amplifier is electrically shielded from the readout section by a gate marked OG, the *output gate.* The electrode groups are known as *phases,* where those for the image section are designated Iϕ, and those for the readout section Rϕ. When drive pulses are applied as illustrated in Figure 1.4 to a register, charge is moved in the directions indicated by the arrows in Figure 1.3, towards the output amplifier.

The CCD operates as follows. Light incident on the device is able to penetrate the semi-

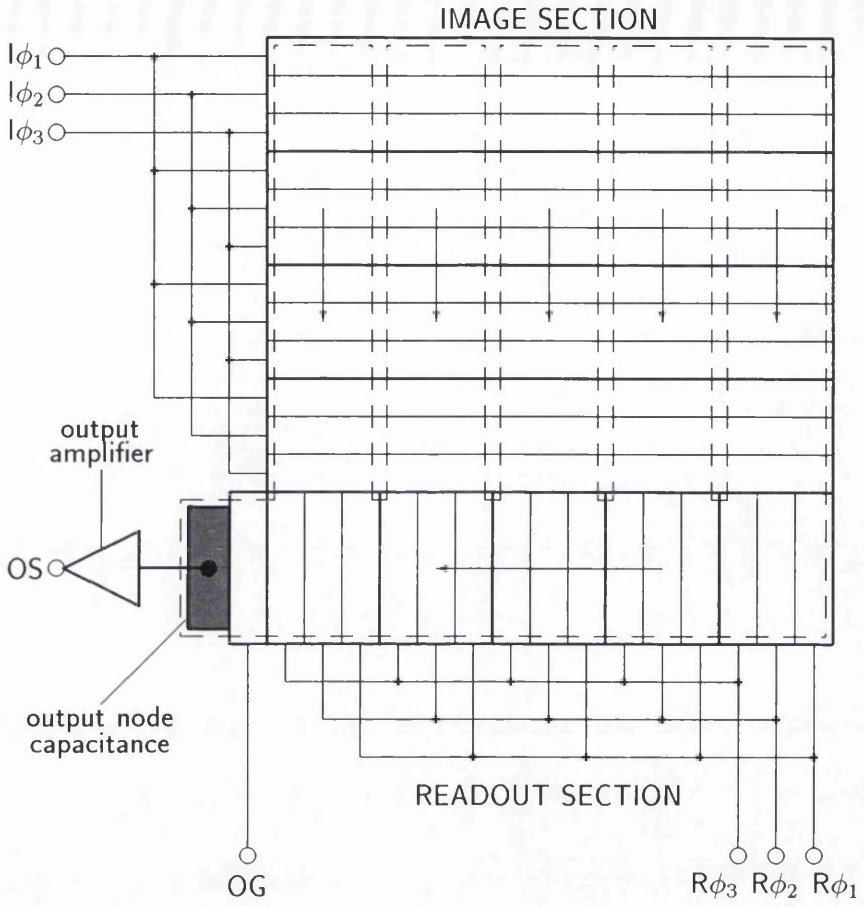

Figure 1.3: Schematic of a 4×5 pixel CCD.[27]

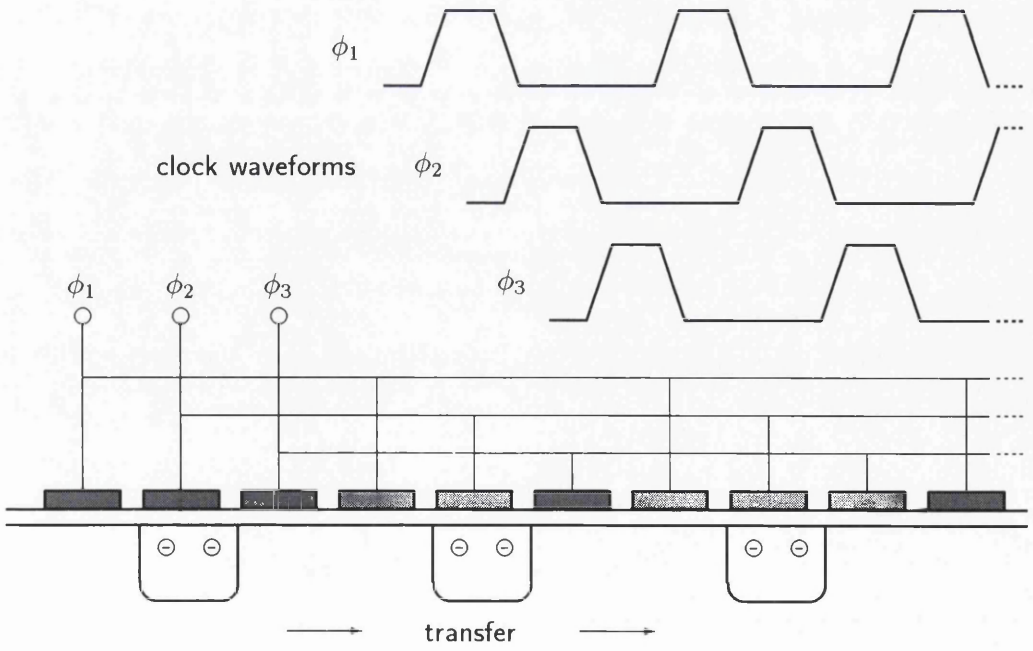

Figure 1.4: CCD drive pulses.[27]

transparent electrode structure and generate electron-hole pairs in the silicon substrate. The electrons so produced diffuse towards the nearest biased electrode where they are accumulated as a signal charge. Holes produced by incident photons diffuse away from the electrodes and are effectively lost in the substrate. The resulting charge packet is proportional in size to the intensity of incident light and the exposure or *integration* time. Because of the electrode interconnections, many electrodes are biased simultaneously. These electrodes are divided into separate charge collection sites by the channel stops. In the case of a three-phase device, every third electrode in the image section is biased. At the end of an integration the device thus contains a two-dimensional charge distribution, representative of the light incident upon the device.

If the charge has been collected under the Iϕ_2 electrodes, for example, then using one cycle of the waveforms shown in Figure 1.4 the charges are all shifted to the next Iϕ_2 electrode. Assuming the Rϕ_2 electrodes are also biased, then charge from beneath the electrode in the image section adjacent to the readout section will be transferred to reside below the Rϕ_2 electrodes. This process, which moves a complete line of charge packets from the image section to the readout section, and shifts the whole matrix one line closer to the readout section is known as a *vertical transfer*. By applying the drive waveform cycle to the readout register repeatedly, each charge packet is brought to the output amplifier in turn. In simple terms, each charge packet is dumped on to the output node capacitance (see Figure 1.3) which generates an output voltage proportional to the charge. In practice the output node is positively charged by a bias voltage applied to the device, then the voltage output is reduced slightly when the signal charge packet flows on to it. The difference between the two voltages represents the output signal. Once all the charge packets in one line have been output another vertical transfer can be made. This process continues until the whole image has been read out.

Qualitative aspects of the use of CCDs for various astronomical purposes are discussed in Section 2.2.3 and include; low-light level applications, frame-transfer devices, device size, pixel size, wavelength sensitivity range, dark current and quantum efficiency.

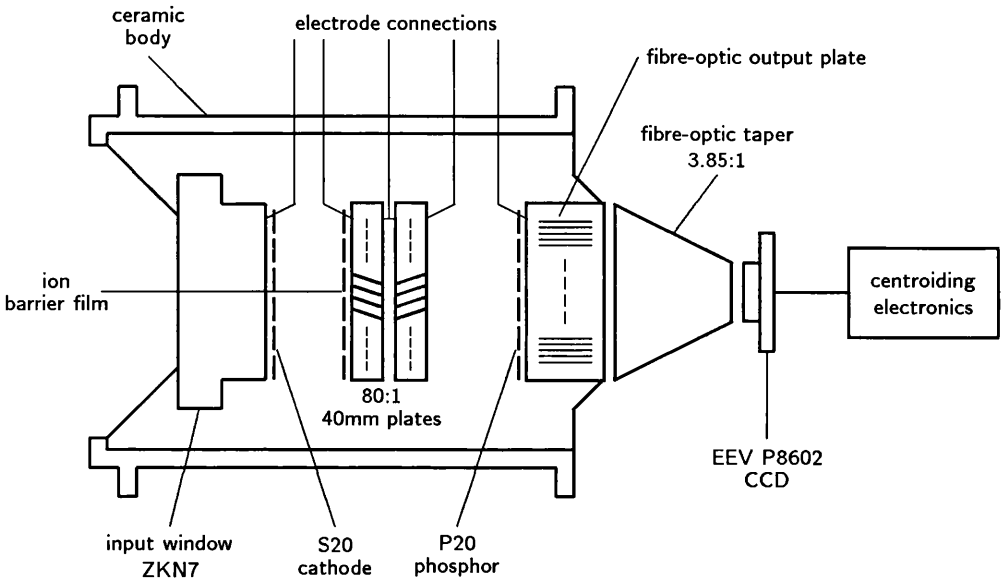

Figure 1.5: Schematic of a 40mm Micro Channel Plate intensified IPCS.
Courtesy of J. Fordham.[59]

1.4.3 Photon-Counting Systems

Photon-counting systems (PCS) detect individual photo-electrons produced by an image focussed onto the photocathode of an intensifier tube. The location of each event can be recorded or, more commonly, the events are integrated in computer memory for a time to build an image. An example of such a detector is the University College London Image Photon Counting System (IPCS)[61]. A schematic of the IPCS is shown in Figure 1.5.

An important feature of the IPCS is the special pattern processor which is placed between the CCD and the data acquisition computer. These *centroiding* electronics identify the central position of each photon event. They also allow each event to be recorded with equal weight and without system noise. Centroiding to 0.125 of a CCD pixel is achieved in the modern versions of the IPCS, providing approximately 2000×2000 channels when a standard-sized CCD is used.

Photon-counting systems are particularly useful in areas such as speckle interferometry which require a higher time resolution than that achievable with a plain CCD. They are also useful in very low-light level situations, for example, high-resolution spectroscopy of faint objects, where the photon arrival rate at some wavelengths may be very low. The principle advantage of PCS over other detectors is their zero readout noise, which makes

the detection of low-intensity signals a possibility (CCDs would be dominated by noise from dark current and cosmic-ray events). Until recently the large number of effective pixels possible with PCS has also been an advantage over CCDs. It should be noted that larger CCDs now available can be used to replace the small-format devices traditionally used as the back-end of PCS thus leading to an increase in pixel count. Common-user versions of the IPCS are in use at the Royal Greenwich Observatory (RGO) on La Palma and at the Anglo Australian Observatory (AAO) and have been used in the past at the Hale Telescope and at ESO.

1.4.4 Infrared Detector Arrays

CCDs are fabricated from silicon. The longest wavelength of light which can be absorbed by silicon is about 1.1μm. This limit is set by the band-gap energy of silicon; photons of longer wavelength do not have sufficient energy to raise electrons from the valence band. To extract information from light of wavelength greater than 1.1μm astronomers have to use different detectors. This is the realm of the *infrared.*

The infrared part of the electromagnetic spectrum may, for descriptive purposes, be divided into: the **near** infrared, 1–5μm; the **mid** infrared, 5–20μm; and the **far** infrared, which extends from 20μm to about 200μm.

Infrared radiation is less attenuated by interstellar dust than optical radiation and so such regions as the centre of the galaxy, which are hidden in the visual, can be studied. Many of the most distant objects in the universe are, according to the Hubble Law, moving away from the galaxy at velocities proportional to their distance. This motion leads to the doppler shifting of light from such objects towards the red. Spectral features which are normally found in the visual part of the spectrum are shifted into the infrared for many of the most distant objects.

Until the advent of infrared detector arrays, painstaking observations had to be made using single-cell sensors. Neugebauer and Leighton used a lead-sulphide cell for a 2μm survey of the sky[124]. The resolution of their survey was only 4 arcminutes, much less than that possible with optical telescopes.

Many researchers have attempted to manufacture infrared imagers, the main driving force being the military applications of such technology. Texas Instruments attempted

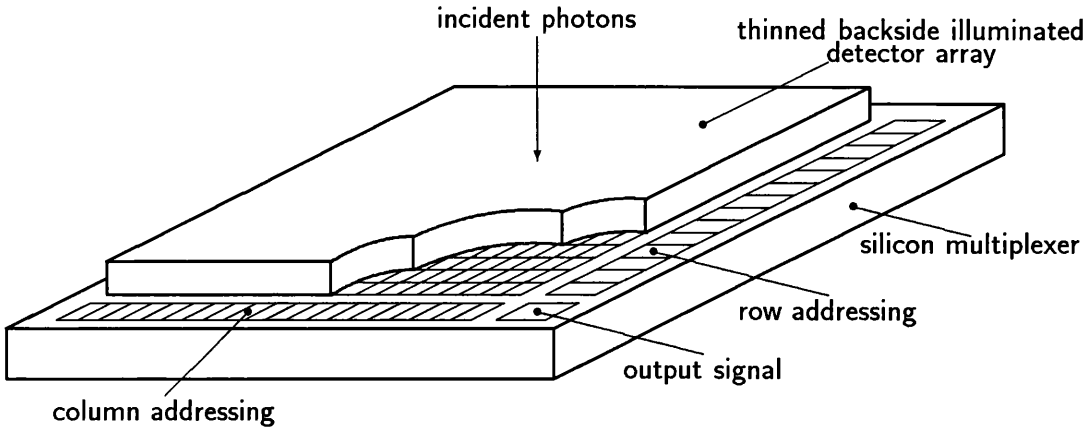

Figure 1.6: A schematic of an infrared imager.[124]

to manufacture an entire CCD based on a cadmium-mercury-telluride substrate as early as 1974, but this and other similar efforts proved fruitless, and the technology of *hybrid* devices was needed.

The hybrid imagers now developed separate the photon detection and signal multiplexing functions; the latter being done by a silicon-based CCD-type multiplexer. A schematic of a hybrid infrared imager is shown in Figure 1.6.

The figure shows how the hybrids have a sandwich-like structure, the upper part being the detector array. Several different materials can be used for the detection function: indium antimonide, the previously mentioned cadmium-mercury-telluride or a doped semiconductor. Table 1.3 shows the long-wavelength limit for several doped semiconductors.

The first astronomically used infrared imagers were developed by the Santa Barbara Research Center (SBRC), based on technology they had developed for military applications. The 62×58 pixel sensor is fabricated from an indium-antimonide infrared transducer and a silicon-based CCD. This sensor forms the heart of the IRCAM infrared camera for the UKIRT.

Several groups, including Rockwell International, are working on larger arrays using technologies both similar and different to the SBRC sensor. A Rockwell device is at the heart of the ESO SHARP camera (see Section 1.3.1.2). Larger and less noisy arrays are currently becoming available, and detectors covering the full 1μm to 200μm infrared region of the spectrum should be available for the space based observatories being built.

The mosaic technique, which is the main subject of this work is as applicable to infrared

Base material	Impurity	Long wavelength limit /μm
Germanium (Ge)	Gold (Au)	8.3
	Mercury (Hg)	13.8
	Cadmium (Cd)	20.7
	Copper (Cu)	30.2
	Zinc (Zn)	37.6
	Boron (B)	119.6
Silicon (Si)	Indium (In)	8.0
	Gallium (Ga)	17.1
	Bismuth (Bi)	17.6
	Aluminium (Al)	18.1
	Arsenic (As)	23.1
	Phosphorus (P)	27.6
	Boron (B)	28.2
	Antimony (Sb)	28.2

Table 1.3: Extrinsic semiconductors.[124]

sensors as it is to optical CCDs.

1.4.5 Other Detectors

Although CCDs are used in nearly all new instrumentation (sometimes as part of a photon-counting-camera head) many older instruments use other detectors. The immediate predecessor of the CCD in imaging applications is the vidicon-type television tube. In the vidicon, image photons are incident upon a photocathode. Photoelectrons produced are accelerated through an electrostatic field towards a thin target where they release secondary electrons thereby leaving a positive charge pattern on the target. The target is scanned from the rear in a raster pattern by electrons from an electron gun. In the vidicon the signal is derived from the change in potential on the target during the raster scan[194]. Vidicons are not used in modern instrumentation, however, they proved successful for imaging, particularly in the Voyager deep space missions.

Like most electronic detectors, the *photomultiplier* is based on the photoelectric effect[104]

(the excitation of electrons in a solid by incident photons, such electrons reaching the conduction band and being collected as a signal charge or detected as a signal current). A photoemitter is coated onto the cathode of the tube which may be held at, typically, a negative potential of 1000 volts with respect to earth. Photoelectrons produced by photons incident upon the cathode are accelerated towards subsequent *dynodes* which are held at progressively higher potentials (compared to the cathode). When the photoelectron is incident upon the first dynode it may release more than one electron thus giving rise to signal multiplication, after subsequent stages a single incident photon may give rise to a signal of 10^6 electrons. Photomultiplier tubes have been used in many astronomical instruments, particularly those for photometry (for example, the IP21 tube used by Johnson and Morgan[104]).

1.4.6 Photon Counters and Charge-Coupled Devices Compared

The previously described photon counters and CCDs are currently the dominant detectors in optical astronomy. The two technologies are complementary. CCDs have a non-zero readout noise, which is likely to remain the case for several years in practical systems. Photon-counting systems have an effective zero readout noise and are thus highly desirable in low-light-level applications where the signal-to-noise ratio (for a CCD camera) is small. Contemporary photon-counting systems can offer total detector-pixel counts much larger than monolithic CCDs by the use of the *centroiding* technique (see Section 1.4.3) and modern Micro-Channel Plate image intensifiers. Photon counters offer superior quantum efficiency when compared to (unthinned) CCDs in the violet and ultraviolet regions of the spectrum. This, when combined with their zero read noise, is highly significant for faint targets.

CCDs offer a larger dynamic range than contemporary photon-counting systems. Photon counters cannot be used for work with bright sources as the photomultiplier part will saturate. CCDs have a superior quantum efficiency to photon counters over much of the spectrum at wavelengths longer than the blue part of the optical. In addition, the existing centroiding algorithm parameters (in particular thosed used in the UCL IPCS) are intensity dependent. In practice, this means that a fixed-pattern noise is imposed upon images produced with photon-counting systems, especially when a large dynamic range is present in the image being sampled. This problem may be overcome in future

versions of the IPCS[62].

In summary: CCDs are preferable to photon counters in the majority of applications due to their superior dynamic range and quantum efficiency. Photon counters, however, remain the detector of choice for low-light-level applications, particularly in the blue and ultraviolet parts of the spectrum where the signal-to-noise ratio of CCDs is inferior due to their readout noise.

1.5 Scope of this Work

As previously mentioned, this thesis is primarily concerned with detector technologies for optical astronomy—in particular, the focal-plane mosaic. The goal of the research is to make an order of magnitude improvement in the rate of data acquisition for astronomy a real possibility. The following Chapters detail the progress of this continuing research from inception to the present day.

1.5.1 Collaborations & Contributions

The vast majority of the material described in this text is the author's own work; contributions and collaborations with others are marked where they are discussed and as follows.

- The justifications for mosaic-detector technology and its 'thumbnail' sketch as presented in Section 2.4 are partially due to D. D. Walker and A. C. Fish.
- The requirements of a mosaic detector technology described in Chapter 2 are the result of the author's reviews *and* discussions with those engaged in the research.
- The outline specification of the modular structure of the mosaic-detector hardware, presented in Chapter 3, is partially due to A. C. Fish.
- The specification of the EEV P88300UC CCD in Chapter 3 is the result of a collaboration by the research team at OSL and a team at EEV. The design of the chip carrier is due to P. J. Pool at EEV and the chip transport jig to M. Dryburgh at the OSL.

Chapter 2

A Large-Area Detector

2.1 Introduction

The rate at which astronomical data are collected has increased many fold over the last twenty-five years. This expanding base of data comes from a greater number of instruments, but the primary reason for the expansion has been advance in technology. A new generation of very large optical telescopes is becoming available to the astronomical community. Use of these will circumvent the main limitation on data collection in the optical part of the spectrum, namely, light-gathering power. The first-generation instrumentation packages for the new telescopes are now being defined and built. In many cases the full potential of the telescope will not be exploited; this is for several reasons, not the least of which is cost.

Many avenues of scientific investigation in the area of optical astronomy require, or would benefit from, improved detector technology (see Section 1.1.1). The charge-coupled device is by far the most common detector used for optical astronomy. Superior detectors will be necessary to exploit fully the very large telescopes. This Chapter describes the requirements of such detectors and outlines a practical technique for achieving these requirements. A review of the available charge-coupled devices, with particular reference to the large-area sensor is made. The important parameters of charge-coupled devices and their performance are explained. Examples of proposed and possible instruments which make use of large detectors are discussed with reference to certain existing instrumentation and techniques. The background of the research undertaken at the Optical

Science Laboratory is described.

The requirement of a large-area detector is to maximise the usage of available light collected by the largest telescopes. By utilising the full beam of very large telescopes, the rate of astronomical data aquisition can be increased, possibly by several orders of magnitude. Similarly, coverage of a wider spectral range in a single integration during spectroscopic studies can also improve observing efficiency. The operation of modern observatories is expensive, observing time being the most precious resource.

2.2 Imaging Charge-Coupled Devices

The development of charge-coupled devices and their astronomical use have been intimately linked. The majority of detector development programmes are, however, directed primarily at applications other than astronomy. The basic functionality of these devices is described in Section 1.4.2. In this section the important characteristics (for astronomical use) of charge-coupled devices are explained and discussed.

The architecture of all charge-coupled devices is basically very similar to that described in Section 1.4.2. Some devices have different electrode configurations and additional electrodes or *transfer gates* to assist the transfer of charge from the image section to the readout section. These architectural differences and the various bias voltage levels and clock signals required to operate the detectors are discussed in Section 2.2.4. The majority of the charge-coupled devices available have been manufactured with a *frame-transfer* architecture for commercial TV application. The operation of these devices is, again, similar to that described in Section 1.4.2.

2.2.1 Frame-Transfer Devices

Many charge-coupled devices are designed for use in video cameras, their basic architecture being of the frame-transfer type. An example of the frame-transfer CCD is the EEV P86000 series (See Figure 5.5 and Figure 5.4). These devices are similar to those described in Section 1.4.2, they have an additional register, the *storage* register. The storage register is masked with an opaque covering, which in some devices is an aluminium shield intrinsic to the device (Philips NXA1010 [143]), which in others is removable (EEV

P86000 series). The frame-transfer CCD is designed to be used without a mechanical shutter. The array operates as follows. An image is projected on to the device (image section), and after what is normally a short period of integration this image is transferred to the storage section of the device by the charge-coupling technique (see Section 1.4.2.1) in a *very* short period of time. As long as the transfer time is small when compared to the integration time the light collected during the transfer *(image smear)* does not degrade the image significantly. Whilst the subsequent integration is occurring the charge held in the covered storage section is read out through the readout section in the manner described in Section 1.4.2.

The storage section of a frame-transfer device is manufactured in an identical fashion to the image section. This means that it may also be used for imaging if the opaque covering is removed.

Frame-transfer devices are in widespread use for astronomy, in a full-frame mode. The pixel format and pixel size of the devices vary (see Tables 2.1–2.3). Despite their non-scientific origins excellent performance has been achieved with frame-transfer CCDs.

2.2.2 Interline Transfer Devices

Another device architecture, radically different to the common frame-transfer and full-frame devices is the *interline transfer* device. These devices have alternate light sensitive and covered columns of pixels. After an integration, the photo-generated charge is shifted horizontally by one pixel to lie beneath the covered columns. The charge is then shifted toward the readout register in the normal manner. Interline transfer devices are less suitable to astronomical applications because the covered columns of the devices represent an unavoidable loss of device response and cause aliasing of high spatial frequency information in the image.

2.2.3 Available Devices

Tables 2.1–2.3 illustrate the range of charge-coupled devices which have been and are available (up to 1995). The characteristics vary widely. Recently the trends are for: greater quantum efficiency over a wider spectral range; lower readout noise; and larger formats. These trends are discussed in Section 2.2.3.5. The information in Tables 2.1–2.3

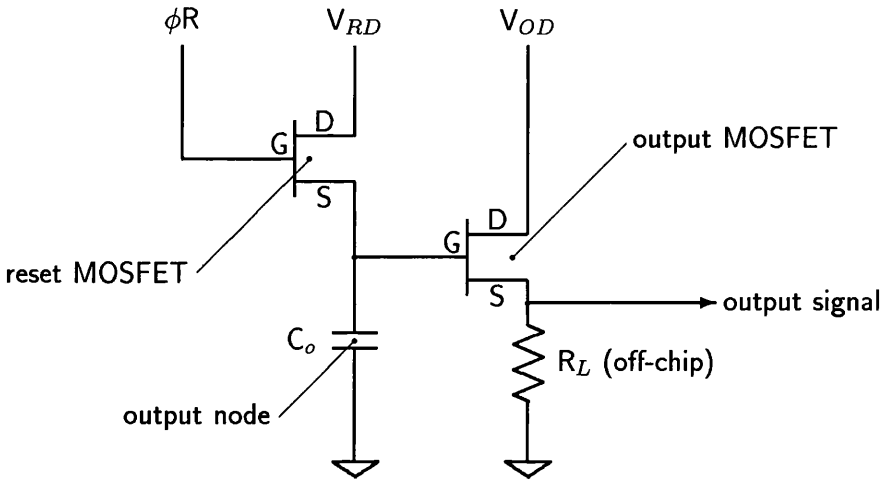

Figure 2.1: CCD on-chip output amplifier.[89]

is representative of the vast majority of the detectors which have been manufactured and covers most of those used for astronomical applications.

2.2.3.1 Readout Noise

'Readout noise usually raises the most emotion amongst users'[98] so it is discussed here first. Figure 2.1 shows a typical on-chip output circuit for a charge-coupled device.

This circuit is used in the EEV P86000 and P88000 series and the Texas Instruments three-phase 800×800 pixel device. The output circuit is a single-stage MOSFET source-follower and a reset MOSFET. The circuit is simple and gives low-noise performance. Noise generated in the output amplifier defines the ultimate readout-noise floor of a CCD. There are two basic components of noise in the output amplifier: white noise and inverse-frequency ($1/f$) noise[89]. Operating the device at cryogenic temperatures has the advantage of reducing both noise sources and, when combined with operation of the output transistor at (typically) 1mA drain-source current, the $1/f$ noise is greatly reduced[32].

The level of readout noise has steadily decreased with improvements in charge-coupled device manufacture. The highest-noise devices in Tables 2.1–2.3 are all old designs. The vast majority of modern devices achieve readout noise levels better than $10e^-_{rms}$ with performance about $5e^-_{rms}$ or better being the accepted norm for astronomical instrumen-

tation.

One method employed to improve the readout noise performance of some charge-coupled devices has been to reduce the physical size of the output amplifier. This reduces the capacitance of the output node and, by the relation $V = Q/C$, increases output gain or output transfer function (in volts-per-electron). Unfortunately, this tends to increase the white noise level and so there is an optimum size for the amplifier.

Readout noise is most significant in low-light-level applications—for signals of hundreds of electrons or more the uncertainty of the measurement is dominated by photon shot noise. In high-dispersion spectroscopic applications the number of photons incident on some pixels of the detector will be very small. This is in contrast to direct imaging where the sky background will produce some signal in all pixels of the detector. When the light is dispersed across the detector by wavelength it is possible for virtually no photons to be detected at some wavelengths, even with long integration times. These small signals may be only a few tens of electrons or less and thus a readout noise of five or more electrons is significant. Photon-counting detectors (see Section 1.4.3), which have zero readout noise, have often been used in preference to charge-coupled devices for such applications.

Manufacturer	Device	Pixel Format	Pixel Dimensions	Peak QE	Readout Noise	Notes
			μm		e^-_{rms}	
EEV	P86000	385×578	22×22	0.50	10	[98]
EEV	P88100	298×1152	22.5×22.5	≈0.50	5	[98]
EEV	P88200	770×1152	22.5×22.5	≈0.50	5	[98]
EEV	P88300	1242×1152	22.5×22.5	≈0.50	5	[98]
EEV	P88500	2186×1152	22.5×22.5	≈0.50	5	Prototype[98]
Fairchild	CCD221	380×488	18×30	0.12	30	Interline[58][98]
Ford	PM512	516×516	20×20	≈0.50	5	[21][98]
Ford	2048	2048×2048	15×15	—	—	[98]
Ford	4096	4096×4096	7.5×7.5	—	—	[98][92]
Ford	Skipper	64×256	—	—	≈1	[92]
Kodak	KAF1400	1035×1320	7×7	≈0.35	15	[98]
Kodak		2048×2048	9×9	—	—	Prototype[98]
Kodak		4096×4096	4.5×4.5?	—	—	Planned[98]
MIT/Lincoln		≈450×500	≈20×20?	≈0.35?	5	Prototype[98]
MIT/Lincoln		420×420	27×27	—	9	Buttable[24]

Table 2.1: Charge-coupled devices (continued over).

Manufacturer	Device	Pixel Format	Pixel Dimensions	Peak QE	Readout Noise	Notes
			μm		e^-_{rms}	
Philips	NXA1010	604×576	10×15.6	—	—	[143][144]
RCA	SID-501EX	320×512	30×30	0.75	60	Obsolete[98]
RCA	SID-503	640×1024	15×15	0.75[98], 0.85[183]	60[98], 51[183]	Obsolete[98]
RCA	SID-504	403×512	16×20	0.75	—	Obsolete[149]
RCA	SID-612	320×512	30×30	0.75[64], 0.85[65]	70[64], 99[65]	Obsolete[64]
Reticon	RA1200J	400×1200	27×27	0.30	5	[98]
Reticon	Thin	400×1200	27×27	0.60	5	Prototype[98]
Reticon	RA1024J	1024×1024	13×13	0.60	5	MPP[110]
Reticon	RA2000J	2048×2048	27×27	0.60	5	MPP[110]
Reticon		800×2400	13.5×13.5	0.30	5	[98]
Reticon	VNIR	64×404	52×52	0.40	30	[197]
Tektronix	TK512	512×512	27×27	0.30–0.40	5–10	[57][98][170]
Tektronix	512-thin	512×512	27×27	≈0.50	10	[98]
Tektronix	TK1024E	1024×1024	24×24	≈0.50	10	[98]
Tektronix	TK2048M	2048×2048	27×27	≈0.30	10	[98][170]
Tektronix	TK2048M-thin	2048×2048	27×27	≈0.50	10	[98]

Table 2.2: Charge-coupled devices (continued over).

Manufacturer	Device	Pixel Format	Pixel Dimensions	Peak QE	Readout Noise	Notes
			μm		e^-_{rms}	
Texas Inst.	TC211	204×165	13.75×16	—	19	Virtual Phase[79]
Texas Inst.	4849	390×584	22×22	≈0.75	11	Virtual Phase[172]
Texas Inst.		800×800	15×15	0.60	14	[98][134]
Texas Inst.		800×800	15×15	0.75	18[134], 12[12]	Virt. Ph.[12][96][134]
Texas Inst.	Thin	800×800	15×15	≈0.70	6.2–10.7	[111]
Texas Inst.	VP1M	1024×1024	18×18	0.50	30	Virtual Phase[173]
T.I. Japan	TC215	1000×1018	12×12	0.60	7	Virtual Phase[169][39]
Thomson	TH7852	208×144×2	30×19/30×28	0.50	—	[174][176]
Thomson	TH7861	384×576	23×23	0.40	23	[128][174]
Thomson	TH7882	384×576	23×23	0.40	5	[98]
Thomson	TH7883	512×512	18.5×23.5	0.45	≈5	[6]
Thomson	THX31156	1024×1024	19×19	0.40	5	[98][177]
Thomson	THX31157	400×579	23×23	0.40	5	Buttable[6][98][152]
Thomson	THX31159	512×512	23×23	0.40	5	[98]

Table 2.3: Charge-coupled devices.

2.2.3.2 Pixel Sizes and Pixel formats

The majority of the devices in Tables 2.1–2.3 are designed for CCIR- or EIA-standard compatible video applications. These devices have pixel formats of about 400×580 and smaller. The square format devices, 512×512 pixels and similar, are usually designed with scientific applications in mind. Devices of the order of 1024×1024 pixels are now widely available for scientific imaging applications. The very largest format devices are all prototypes or one-off projects.

Charge-coupled devices are manufactured in much the same way as any other integrated circuit. The devices are fabricated on a silicon wafer, usually four inches (about 10cm) in diameter or smaller. This is a current limitation of semiconductor manufacturing technology. The very largest devices available (Tektronik TK2048, Ford 4096) must be manufactured 'one to a wafer'—this is very expensive as the probability of a flaw in a die is proportional to the area of silicon occupied. There has been a trend recently, by those using the 'silicon foundry' method of device procurement, towards smaller pixels. This reduces the device size and thus increases the yield. From Tables 2.1–2.3 it can be seen that the size of pixels varies from about $10\times10\mu m^2$ to $27\times27\mu m^2$. The exceptions to this are the largest detectors, which compromise on pixel size in order to increase pixel count, and the Reticon VNIR (Visual and Near Infrared) CCD developed for the NASA Space Shuttle programme.

The significance of pixel size for astronomy can be summarised as follows. The full-well capacity of a detector, (*i.e.*, the largest number of electrons which may be held in a pixel before charge spills out of the potential well) is dependent on the physical size of the pixel. The readout noise of the detector is, however, effectively independent of the pixel size as it is determined by the structure and operation of the device's output amplifier (see Section 2.2.3.1). This means that, for a device with a particular readout noise the dynamic range of the detector is fixed by the full-well and therefore the pixel size. This is important, particularly in spectroscopic applications where some pixels of the detector may be illuminated relatively brightly compared to other pixels which may receive only a handful of photons, even in a long exposure.

From an optical design point of view, larger pixels can be of benefit in spectrographic design as they imply slower focal ratios and ease the problem of aberrations[186].

In general, astronomical applications require as many pixels in the detector as possible ('pixel count'). Whilst the recent developments in large-pixel-count detectors are of benefit for electronic photography and digital photocopying, they are made at the expense of smaller pixels and so are a compromise from an astronomical point of view.

Several of the detectors in Tables 2.1–2.3 have more than one readout amplifier. This allows the full frame to be partitioned and more than one pixel to be read out at a time. This is advantageous for the larger devices as it reduces readout time and the effect of charge transfer errors. Conversely, extra electronics are required to operate the separate amplifiers (effectively there are two or more devices to the single die) and the data from the amplifiers must be separately calibrated.

2.2.3.3 Quantum Efficiency and Spectral Response

Silicon-based charge-coupled devices are capable of responding to radiation with wavelength in the range 1–10 000 Angstroms[89]. The *quantum efficiency* (QE) of a detector is the ratio of the number of photoelectrons released to the number of incident photons absorbed by that detector[124]. The quantum efficiency of a detector is a function of the wavelength of the incident radiation. The values in Tables 2.1–2.3 are *peak* values. Figure 2.2 shows quantum efficiency versus wavelength graphs for several detectors.

From Figure 2.2 it can be seen that a device's response typically peaks at about 500–700nm and falls off in the red and blue. The trend in recent years has been towards improved response in the blue, often by the use of special coatings. Another important technique for improving blue response has been device *thinning*. The old RCA thin detectors were used all over the world: note the high QE in Figure 2.2. Thinning is used for the following reasons. Normally a CCD will be operated in a front-illuminated mode, that is, with the light incident on the surface of the device which carries the electrode structures. The polysilicon electrode structure tends to degrade the blue performance as the photons are all absorbed in the electrode layer and do not pass through to the pixel depletion regions. By (in essence) cutting away the bulk of the silicon from the back of the device and inverting the very thin device which results, the light becomes incident directly on to the epitaxial substrate of the device. This avoids the absorption effect of the electrode structure and vastly improves the blue response of the detector. The

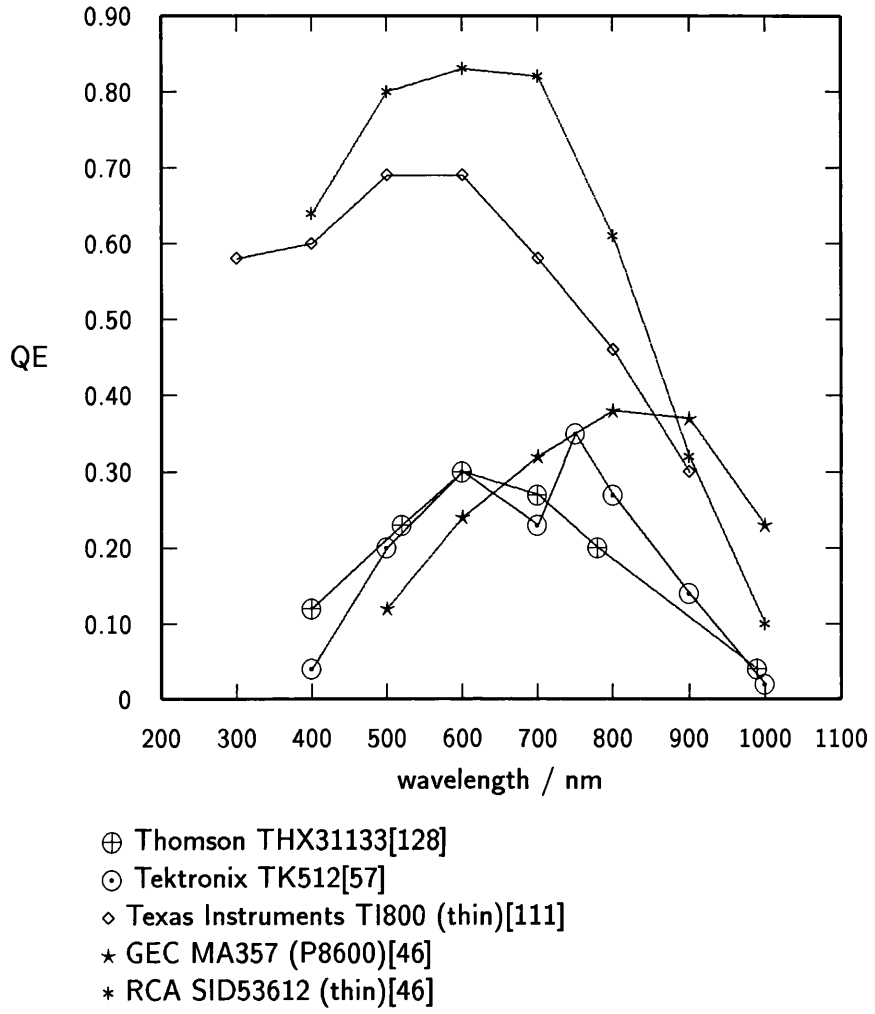

Figure 2.2: Quantum efficiency curves for various detectors.

resulting thinned device may be only 10μm thick and is supported on a glass or ceramic base.

From an astronomical point of view, the quantum efficiency should be maximised, hence shortening exposure times. Another important feature is quantum efficiency *stability*. The response of the device should be as time-independent as possible. During the development of the Texas Instruments thinned 800×800 pixel device it was found that the quantum efficiency of the thinned device changed when it had been exposed to light. This effect is termed *quantum efficiency hysteresis* (QEH)[89][90]. Fortunately, a solution to the QEH problem, which also enabled extremely high QE in the blue to be achieved, was found *eventually*—the flash gate [83][84][90][91]. In simple terms, the deposition of

a very thin layer of platinum (for example), only a few atoms thick, on the back surface of the CCD produces a negative surface charge. This charge repels photoelectrons generated near the surface of the device and the charge moves into the epitaxial layer where it is collected by a potential well. Without the flash gate the photoelectrons generated close to the surface (*i.e.*, by the highest-energy photons/those of shortest wavelength) are caught by surface trapping states, which degrades the blue and ultraviolet performance of the detector.

2.2.3.4 Other Charge-Coupled Device Parameters

Charge transfer efficiency (CTE) is the fraction of charge successfully moved from pixel to pixel in a CCD by the process of charge-coupling[124]. To enable direct comparison of the CTE for different devices it is usually quoted per pixel-to-pixel transfer, but, it is occasionally quoted per inter-electrode transfer. Except at the very lowest signal levels (10–50 electrons), CTE is excellent for modern CCDs. CTE has values typically greater than or equal to 0.999995. This high value means that CTE is negligible for the video-format CCDs and most devices up to about 1000×1000 pixels. For larger format devices, for example the Tektronix TK2048, the effect can be significant.

Full well The physical dimensions of a CCD pixel determine the maximum quantity of charge which may be held in a potential well beneath that pixel's electrodes. This maximum charge is known as the *full well.* Typically, full well is less than about $5 \times 10^5 e^-$. If the illumination of a pixel is such that the full well is reached, further photoelectrons generated will cause charge spillage into the adjacent pixels.

Dark current Because of the small gap in energy between the valence band and conduction band in silicon it is easy for electrons to be excited into the conduction band. The kinetic energy of electrons in silicon at room temperature is large enough to generate a significant number of conduction band electrons. This charge is known as *dark current* because it is not due to incident photons. At room temperature, the amount of charge generated per second for an average CCD pixel is of the order of 10^5 electrons. Such a signal would saturate most detectors in only a few seconds. Fortunately, as the rate of charge generation is related to temperature, the effect

can be reduced by device cooling.

Equation 2.1[124] relates the dark signal N_D to

$$N_D = \frac{I_0}{e} d^2 \exp\{-(T_0 - T)/9.96\} \quad e^- \tag{2.1}$$

I_0 the dark current in amps per square centimetre at room temperature (T_0), d the pixel size in square centimetres, T the temperature of operation of the device in Kelvin and e the electronic charge.

By cooling a device to cryogenic temperatures, dark current can be made very small, allowing the long integration times required for detection of very faint astronomical sources. In practice this is achieved by the use of a liquid-nitrogen cryostat. The CCD chamber is evacuated to prevent condensation damage to the device. Electric heat pumps (peltier devices) are sometimes used as an alternative.

Recent developments in device manufacture, including device thinning, have helped to reduce the level of dark current, which should enable charge-coupled devices to be operated at higher temperatures in the future.

Cosmic-ray susceptibility Older charge-coupled devices were highly prone to spurious signals generated by cosmic rays incident upon them. The use of thinned devices and epitaxial substrate devices reduces this effect because the volume of silicon from which charge is collected is less. Charge-coupled devices are also susceptible to terrestrial radiation, which can generate spurious signals in a similar way to the cosmic rays, and for this reason even low-level radioactive materials are avoided in the design and construction of astronomical CCD cameras.

Response non-uniformity Non-uniformity of device construction leads to significant pixel-to-pixel variation in the sensitivity of charge-coupled devices. CCDs are, however, highly linear in their response and so it is possible to calibrate the relative response of the pixels in a detector and completely remove the non-uniformity. This technique is known as *flat fielding* as a completely uniform or *flat* illumination is required for the calibration.

Parameter	1990	1995 (projected)
Pixel format	512×512 or 385×576	1024×1024
Pixel size	20×20μm	15×15μm
Peak QE	0.40 (thick), 0.70 (thin)	0.70 (thick)/0.80 (thin)[99]
Readout noise	$5e^-_{rms}$	$2e^-_{rms}$
Operating temperature	150K	180K
Cosmetic quality	No column defects, a few ($\leq$ 10) traps	No column defects, one or two traps
Cost	\$3–4K/\$1–2K[99]	\$14K/\$3K[99]

Table 2.4: The standard CCD, 1990 and 1995, after Jorden[98][99].

2.2.3.5 Future Developments in Charge-Coupled Devices

Jorden[98][99] reviewed charge-coupled-device technology, with particular reference to likely trends in future device performance. For comparison the parameters of his 'standard' CCDs of 1990 and (his projection to) 1995 are shown in Table 2.4. It seems likely that the steady improvement in device parameters such as readout noise and quantum efficiency will continue, especially as much of the experimental work on CCD design has yet to filter down to the 'standard' device level. Larger detectors may be possible, eight-inch (20-cm) silicon wafers have recently been fabricated[124]. It is interesting to note the revision by Jorden (in his second review) of his projections[99] of peak QE upwards and device price downwards.

The *multi-phase pinned* (MPP)[154] mode of operation has enabled the slow-scan operation of CCDs at room temperature. The technique reduces dark current. The structure of each row of pixels is altered by the addition of implants. Originally the implants were intended to improve vertical transfer efficiency, but had the added benefit that they prevented charge spread when all the vertical clocks were dropped to the same level. If the vertical clocks are held at a sufficiently low level the surface layer becomes inverted and thermally generated electrons from the surface of the device are unable to reach the active volume of the CCD.

The readout noise of laboratory tested devices continues to fall; also, the non-destructive

readout amplifier or *Skipper* has enabled sub-electron readout noise to be achieved for the first time[92].

The most promising development in charge-coupled-device development and procurement for astronomy is the *silicon foundry* idea. There are several groups who have designed their own devices, including 2048×2048 pixel devices with skipper amplifiers[154] and the work of the Danish CCD group coordinated by Johannes Andersen[49]. Most of the construction work has been undertaken by Ford Aerospace, now called *Loral.* Unfortunately, such devices have to be thinned elsewhere and thus the procurement of the very best devices is a complex process.

Astronomical instrumentation has historically used the state-of-the-art in detectors, and this can be expected to continue. Is is important for instrument builders to be able to take advantage of new developments as rapidly as possible. It is therefore necessary to review detector operation requirements and look for future trends in this area.

2.2.4 Requirements for Operation of any CCD

Tables 2.5–2.7 show the nature of the architectures of the devices discussed in Section 2.2.3 where available.

The registers of the CCDs vary from four-phase to uni-phase architecture. There does not appear to be a trend in the number of phases of detectors, and different manufacturers have retained their original system; for example, Thomson use a four-phase architecture and EEV use three-phase. A significant development has been the *virtual phase* architecture used by Texas Instruments. The need for only one clocking signal simplifies the drive electronics. The potential wells in a virtual phase (or two-phase) device have a stepped structure which allows charge to flow in only one direction: towards the output of the device. The potential-well profile is manufactured by diffusing an implant into the substrate below one side of the electrode(s). The diffusion increases the depletion beneath it, giving rise to the stepped structure. In a virtual phase device, a special implant is made between each electrode to generate the step in the depletion region; this is called the virtual phase. The potential on the single phase, when raised, collects charge beneath the electrodes. When the potential is decreased the region beneath the electrodes goes out of depletion and the charge flows from under the electrodes to the virtual phase.

Some devices have *transfer gates* situated between image and readout sections and/or the readout section and the output amplifier. These gates may be clocked or held at a fixed potential.

All devices require fixed level or *bias* voltages for their operation, the number required depends on the output amplifier design for that particular device. The number is typically about five, including the substrate, from which other applied voltages are referenced.

An important consideration for the operation of charge-coupled devices is the relationship between readout rate, device size and clock current. Astronomical CCD cameras operate the devices in *slow-scan* mode. The name of this technique arises because the pixel rate is much slower than that used in television cameras. The pixel readout rate for astronomical applications is typically in the range 10^4–10^5 pixels per second in order to facilitate the use of output processing techniques (see Section 2.2.4.1). This means that larger detectors take longer to read out. The electrodes of a CCD act as capacitances; this becomes significant, particularly in the image section, where the capacitances can be quite large. For example, the Tektronix TK2048 CCD image section has a capacitance of 0.4μF[170], compared with a 25nF capacitance for the same register of the TK512 and only 200pF in the readout register of the TK512. Using the relation

$$\overline{I} = C\frac{\Delta V}{\Delta t} \quad \text{Amps} \tag{2.2}$$

where $\overline{I}$ is the mean current flowing through an electrode phase; ΔV is the voltage difference between the low and high levels of the clock signal; and Δt is the time for a transition from high to low voltage (or vice versa), the current source/sink capability of the driving electronics can be calculated. If, as may be the case, the only change from the TK512 CCD to the TK2048 CCD is the electrode capacitance, a drive circuit with sixteen times the current handling capability is required. A system which caters for fast charge transfers in the image section of the very large detectors may have an un-necessarily high power consumption. Conversely, a system designed for moderate-rate charge transfers in the image section may have a limiting maximum readout rate below 10^5 pixels per second.

Manufacturer	Device	Vertical Clocks	Horizontal Clocks	Bias Voltages	Clock Amplitudes Volts	Bias voltage range Volts	Other Clocks	Notes
EEV	P86000	3	3	5	−10–+5	0–+24	1	
EEV	P88100	3	3	5	−10–+5	0–+24	1	
EEV	P88200	3	3	5	−10–+5	0–+24	1	
EEV	P88300	3	3	5	−10–+5	0–+24	1	
EEV	P88500	3	3	5	−10–+5	0–+24	1	
Fairchild	CCD221	2	2	4	0–+12	0–+16.5	3	[58]
Ford	PM512	4	4	?	?	?	?	[21]
Ford	2048	?	?	?	?	?	?	
Ford	4096	3	3	4	?	?	3	[92]
Ford	Skipper	3	3	3	?	?	5	[92]
Kodak	KAF1400	?	?	?	?	?	?	
Kodak		?	?	?	?	?	?	
Kodak		?	?	?	?	?	?	
MIT/Lincoln		?	?	?	?	?	?	
MIT/Lincoln		3	3	4	?	?	1	[24]

Table 2.5: Charge-coupled devices—requirements (continued over).

Manufacturer	Device	Vertical Clocks	Horizontal Clocks	Bias Voltages	Clock Amplitudes Volts	Bias voltage range Volts	Other Clocks	Notes
Philips	NXA1010	4	4	4	0–+12	0–+22	5	[143][144]
RCA	SID-501EX	3	1	6	−7–+8	0–+20	1	[148]
RCA	SID-503	?	?	?	?	?	?	
RCA	SID-504	3	1	6	−12–+8	0–+20	1	[149]
RCA	SID-612	?	?	?	?	?	?	
Reticon		?	?	?	?	?	?	
Reticon		?	?	?	?	?	?	
Reticon	Thin	?	?	?	?	?	?	
Reticon	VNIR	4	4	4	?	?	2	[197]
Tektronix	TK512	3	3	4	0–+15	0–+20	3	[170]
Tektronix	512-thin	3	3	4	0–+15	0–+20	3	[170]
Tektronix	TK1024	3	3	4	0–+15	0–+20	3	[170]
Tektronix	TK2048	3	3	4	0–+15	0–+20	3	[170]
Tektronix	TK2048-thin	3	3	4	0–+15	0–+20	3	[170]

Table 2.6: Charge-coupled devices—requirements (continued over).

Manufacturer	Device	Vertical Clocks	Horizontal Clocks	Bias Voltages	Clock Amplitudes Volts	Bias voltage range Volts	Other Clocks	Notes
Texas Inst.	TC211	1	1	?	?	?	?	[79]
Texas Inst.	4849	1	1	3	−10–0	0–+16	1	[172]
Texas Inst.	800VP	1	1	4	−15–0	?	2	[13][96]
Texas Inst.	800	3	3	4	−7–+11	0–+32	2	[13][111]
Texas Inst.	800 Thin	3	3	4	−7–+11	0–+32	2	[13][111]
Texas Inst.	VP1M	1	1	5	−12–0	0–+24	3	[173]
TI. Japan	TC–215	1	1	3	?	?	2	[169][39]
Thomson	TH7852	2	2	4	0–+12	0–+21	1	[174][176]
Thomson	TH7861	4	4	4	0–+12	0–+21	1	[174][175]
Thomson	TH7882	4	4	3	0–+12	0–+21	1	[6][174]
Thomson	TH7883	4	2	3	0–+12	0–+21	1	[174]
Thomson	THX31156	4	4	3	0–+12	0–+15	1	[6][177]
Thomson	THX31157	?	?	?	?	?	?	[152]
Thomson	THX31159	?	?	?	?	?	?	

Table 2.7: Charge-coupled devices—requirements.

The remaining consideration for operation of any device is the range of clocking signal voltages required. Typical clock amplitudes in tables 2.5–2.7 are about ten volts, the bias voltages required by the detectors' output amplifiers are all *higher* than the substrate bias and less than about +25 volts relative to the substrate. Detectors running in *inversion mode*, *i.e.,* with the clock levels either partially or completely less than substrate may require transfer gate bias voltages which are also less than substrate.

The following sources should be sufficient to drive *any* known device and allow for future developments.

- Sixteen bi-polar voltage sources, range −12–+12V.
- Eight uni-polar voltage sources, range 0–+25V.

The practicalities of detector operation are discussed in detail in Section 3.5. The operational requirements of a large-area sensor are discussed in Section 2.4.

2.2.4.1 Output Processing

Equally as important as the drive electronics, the charge-coupled device output train is now discussed. Figure 2.1 shows a typical CCD output circuit, the operation of this circuit proceeds as follows[29]. Prior to charge output from the readout section of the device a reset pulse, ϕR, is applied to the first transistor. The high level of this pulse turns the transistor on, *i.e.* conducting, and the output node capacitance, C_o, is charged to the potential of the reset drain, V_{RD}. As the reset pulse goes low the transistor turns off, leaving the capacitance charged to the drain potential. By cycling the clocks of the readout register, charge is transferred into the output node. This partially discharges the output node capacitance causing the potential across it to drop. The change in output potential is proportional to the charge transferred out of the CCD by the relation: $\Delta V = Q/C_o$ where Q is the charge transferred. The second output transistor operates as a source follower to buffer the signal from the output node to subsequent circuitry. The next ϕR pulse will reset the output capacitance and the process is repeated until the whole CCD is read out.

Due to thermal noise generated in the reset transistor the voltage to which the output capacitor is reset fluctuates randomly. The random fluctuations are superimposed on the

exponential charging curve. When the reset pulse ends there will be some uncertainty in the value of the potential on the output node. This noise is known as *reset noise*. The reset noise in electrons, n_{reset}, at temperature T Kelvin is given by

$$n_{reset} = \frac{\sqrt{kTC}}{e} \quad e^- \tag{2.3}$$

where: C is the output node capacitance, e is the electronic charge and
k is Boltzmann's constant (1.38×10^{-23}J/K)[124].

Reset noise can be eliminated by sampling the voltage on the output node after reset (but before charge transfer) and comparing this to the signal value. Because the reset MOSFET has a very high impedance when it is 'off' the voltage on the output node is fixed, only the small signal charge which is dumped on to the output node can alter it. The most common method employed to remove the reset noise is correlated double sampling (CDS). The difference between the reset voltage and final signal output voltage is found using this technique. The CDS system usually also integrates the output-node voltages to further reduce noise[202]. At a temperature of 120K the reset noise for the EEV P8*000 series CCDs is $\approx 80e^-$[124], this compares to a processed readout noise of only $5e^-_{rms}$; hence, the CDS technique is of vital importance.

The last element in the signal train for a charge-coupled device is usually an analogue to digital converter (ADC) which produces a digital representation of the output signal from the device.

2.3 Instruments Requiring a Large-Area Detector

In this section a few examples of instruments which would benefit from large-area image sensors are discussed. These examples are practical in that all of them have been at least proposed, though not necessarily funded. Existing instrumentation which utilises large-area detectors is also briefly described; a more technical description of parts of these instruments is presented in Chapter 3.

2.3.1 The INT Wide-Field Camera

In response to the September 1990 Announcement of Opportunity for Instrumentation for the ING Telescopes, a wide-field camera for the Isaac Newton Telescope (INT) was proposed[34]. The instrument would be a prime-focus CCD *mosaic*. The full field (40 arcminutes diameter) of the 2.5-m telescope would be utilised. This instrument would use either four of the EEV P88500 large-format CCDs or twelve of the P88300UC devices, (see Section 3.4) the latter giving a better coverage of the available image area. The instrument would provide a deep-sky survey and represent a significant step forward from the Palomar/Siding-Spring Schmidt Telescope surveys. It was suggested at the time[188] that the detector assembly should be designed with a replacement of the prime focus corrector for the INT in mind. Such a replacement would give a field up to two degrees in diameter. At the time of writing there are no monolithic detectors of sufficient size to replace the focal-plane mosaic in this instrument.

2.3.2 Columbia University Wide-Field Spectroscopic Telescope

Many spectra can be obtained simultaneously using optical fibres to guide the light from target objects into the slit of a single spectrograph (see Section 1.3.2). In 1988 an ambitious design was studied at the Optical Science Laboratory by D. D. Walker[187]. The proposed instrument, a multiple-object, high-resolution spectrograph was intended to produce spectra of a quality similar or better than that of contemporary single-object high-resolution spectrographs at a lower cost per spectral element. The instrument consisted of six spectrographs; two optimised for ultraviolet, two for the blue region of the visible, and two for the red. The instrument was designed to acquire high-resolution spectra of one thousand objects in one integration. To cover the free spectral range of each spectrum of all the target objects simultaneously required a 3×36 mosaic of 'notional' detectors of 1024×1024 pixels of size $27\times27\mu m^2$ in each spectrograph. The specification required that the gaps between detectors be small both to minimise light loss in those gaps and to produce the minimum possible obstruction size in the Schmidt-configuration cameras of the spectrographs. Like the INT Wide-Field Camera, this instrument could not be realised without the use of detector mosaics, even assuming an order of magnitude increase in the size of monolithic detectors. It is interesting to note that the instrument

design also required the use of grating mosaics.

2.3.3 Cameras for the UCLES Family of Spectrographs

In response to the 1990 AO for the ING Telescopes a short camera for the UES was proposed[190]. UCLES at the AAO was also designed with such a camera in mind and the proposal included the likelihood of a large overlap in the design of the two cameras. UCLES was originally to have included a short camera; however, the potential use of large-area CCDs (in particular, the then-emerging Tektronik TK2048) as the detector in such a camera led to postponement of the construction pending the availability of large-area detectors. The proposal suggested that the possible use of a Tektronik device as the detector in an unfolded Schmidt Camera may be less efficient than an equivalent mosaic of detectors with superior detection-area-to-package-area ratio. It would also be possible to use a mixture of blue- and red-optimised sensors to maximise the efficiency of the instrument. Any small detector butting gaps could be arranged to be parallel to the dispersion in the spectrum and fall between orders.

2.3.4 Cameras for the HROS spectrograph

The design for the High Resolution Optical Spectrograph (HROS) for the Gemini I telescope includes two cameras. Both camera designs envisage the use of mosaics of 2000×4000 pixel CCDs. The long camera will use a three-CCD mosaic whilst the short camera will use a two-CCD mosaic.

2.3.5 Existing Instrumentation

There are several imaging cameras which use 'large-area' detectors. These employ several CCDs, either in a focal-plane mosaic or in separate dewars. Applications of this technology are not limited to astronomy, but include medical imaging, high-energy and particle physics and remote sensing.

2.3.5.1 The Four Shooter

The Four Shooter is an imaging camera for the Hale Telescope[70]. The name of the instrument arises due to its use of four Texas Instruments 800×800 CCDs. The concept of the Four Shooter developed from a previous instrument: the Prime Focus Universal Extragalactic Instrument (PFUEI). The main features of the Four Shooter are:

- 0.336 arcsecond pixel^{-1} image scale.
- ≈1570×1570 pixel (8.8 arcminutes square) image size.
- Integral faint-object spectrograph.
- Optics: Maximum 1.5% loss in transmissive elements, 1% in reflecting elements for the wavelength range 400–1100nm.

In operation, light passes from the Cassegrain focus of the telescope into the instrument. Apart from a protective window, the first optical element met is a four-faceted pyramid-shaped mirror. This mirror reflects quarters of the total image onto four independent cameras; each a CCD in its own dewar. The angles of the pyramid faces are sufficiently small that there is only a little light-loss at the edges of the facets. The control system of the Four Shooter is quite complex: the instrument has the capability to use the *drift scanning* technique[122] to reduce flat-fielding errors.

In their descriptive paper, Gunn *et al*[70] note that a single Tektronix TK2048 CCD would out-perform the four shooter for imaging. It is also noted that the Hale Telescope/Tektronix TK2048 would represent almost the best possible instrument for imaging *without* using a larger telescope—which would require a larger detector for optimum performance.

2.3.5.2 HST Wide Field/Planetary Camera

Another example of the use of a faceted mirror to split the field of view is in the Space Telescope Wide Field/Planetary Camera[201]. The WF/PC is conceptually very similar to the Four Shooter. The camera again uses four Texas Instruments 800×800-pixel CCDs, in this case cooled to operate at about 180K with thermoelectric coolers.

2.3.5.3 ESO Mosaic CCD

A group at the European Southern Observatory (ESO) have a continuing project to produce $2\times n$ mosaics of CCDs for astronomy. Their work is in collaboration with Thomson who have developed a three-side buttable CCD specifically for the project (THX 31157, see Section 2.2.3). The main features of the ESO mosaic system are:

- Component detector: 579×400 pixels $23\times23\mu m^2$.
- Inter-detector gaps: ≈200nm and ≈400nm.
- Readout noise $\approx 4.3 e^-_{rms}$.
- Precise (0.1 pixel) inter-detector alignment.

This system has been proven in the laboratory and at the La Silla Observatory.

2.3.5.4 MOSAIC—Mosaicked Optical Self-scanned Array Imaging Camera

The MOSAIC system was a complex photon-counting machine[203]. The back-end of the micro-channel plate (MCP) intensifier consisted of a 3×3 array of Texas Instruments 800×800-pixel CCDs. The system was intended for use in space-borne instruments. Important considerations in the design were *modularity* and *extensibility.* The most significant part of the design from the point of view of this study is the use of a fibre-optic taper to couple the MCP to each CCD.

2.3.5.5 MIT/Lincoln 840×840 Pixel CCD Mosaic

A custom designed CCD (see Section 2.2.3) was fabricated by the MIT group specifically to investigate focal-plane-mosaic assembly techniques[24]. The detector has a two-side buttable architecture so that 2×2 mosaics are easily constructed. The system had a high co-planarity and pixel alignment requirement as the completed mosaic was to be cemented to an optically flat fibre-optic bundle. The target seam loss was two pixels, which proved to be a problem as the saw for cutting the device wafers was prone to chip the edges of the CCDs. These devices are planned to be used in the Advanced X-ray Astrophysics Facility (AXAF)[85].

2.3.5.6 Craine *et al*

The work of Craine *et al*[43] was targeted at medical imaging applications. It was claimed in this work that the techniques developed could be used to manufacture 'arbitrarily large mosaics of arrays of CCD detectors'. This is true; however, the method used to expand the mosaic was replication of the image by partial reflection, leading to a huge decrease in instrument efficiency. The work of Craine included a 2×2 CCD prototype.

2.3.5.7 Luppino *at al*

Luppino is involved in several projects using few-device mosaics of CCDs[121][45] ranging up to the 8k×8k-pixel camera at the CFHT and University of Hawaii 2.2-m telescope. The detectors used are two-side buttable, the objective being to produce detectors four times the size of the individual detectors.

2.4 Specifications of a Large-Area Detector System

For the foreseeable future it is unlikely that detectors of a significantly larger size than those now available will appear. A method for constructing larger detectors—the focal-plane mosaic, has been used successfully on a small scale. The goal of the present investigation is to develop techniques for constructing mosaics of arbitrary dimensions. The astronomical application of these mosaics and the philosophy of adaptability, which is central to the OSL mosaic CCD system, are here used to define the goals of the research in greater detail:

- Whilst cross-device pixel alignment may not be essential, the mosaic must conform well to the depth-of-focus requirements of astronomical instrumentation. This means that the detectors must be coplanar (for a flat focal-plane) to only a few tens of microns.

- The technologies developed should be as conducive to induction as possible—it should be conceptually as simple to design and build a mosaic of hundreds of detectors as a mosaic of a few.

- The architecture of the system should be as simple as possible without compromising flexibility (a compromise between these design goals may be required).
- The noise performance and dynamic range of the large-area sensor should be at least as good as existing single-CCD systems.
- The readout time should be independent of mosaic dimensions, *i.e.*, there must be parallel processing of the CCD output signals. This is essential if time bottlenecks are to be avoided.
- The system should be designed to operate with any of the existing detectors and those likely to appear in the future.
- A particular instrument should be able to contain devices of different types, sizes, specifications and operation requirements.
- Each device in the mosaic should be individually performance-optimised.
- Any inter-device cross-talk should be insignificant from an astronomical point of view. In practice, zero cross-talk will therefore be required.
- The focal-plane assembly of detectors should be easy to maintain, *i.e.*, it should be possible to replace or upgrade a detector in the array without affecting the neighbouring devices.
- The system should include a degree of automatic self-calibration and optimisation. This is essential to avoid the potentially large instrument-optimisation time for many detectors.
- The component parts of the system should be as simple as possible, in terms of circuit complexity.
- Instrument overheads, such as power consumption, should have as flat a relationship to detector count as possible.
- The physical size of the system should be small.
- As far as possible, existing technical support at an observatory should be able to handle the maintenance of a mosaic detector instrument.

- The software required for detector control should be as portable and simple as possible. It should be easy to integrate new detectors. Some degree of protection against accidental damage to the detectors by human error should provided. The control software should integrate with existing instrumentation seamlessly.
- The parts of the system should have the minimum cost.

2.4.1 Research into Mosaics of Detectors at the Optical Science Laboratory

In December 1986 a proposal was made to the Science and Engineering Research Council to conduct research into detector mosaics for astronomy. The proposal was made by the Optical Science Laboratory of University College London, a group which evolved from the successful AAT UCLES project team. The proposal was granted, at a slightly reduced funding level. A second application was made in February 1987 for funding for a CASE studentship in the mosaic detector project (at that time labelled 'matrix detector project'). It was through this application that the author became involved in the project.

Originally, it had been intended to purchase CCDs in the die state (not housed in the traditional DIL packages) and attach them to a common substrate at Photonic Science Limited of Robertsbridge, Sussex. For several reasons (see Section 3.4) this collaboration did not occur. Instead, a custom designed, low dead-space package for one of EEV's existing CCDs was designed. The original grant application also requested funding for the construction of preamplifiers and data acquisition from all four devices in a 2×2 CCD prototype of the mosaic detector system. Funding for data acquisition from only one detector was granted. This remained the case throughout the progress of the project, to the present day.

A second grant application, to continue research into mosaic detectors at OSL was made in February 1989. This was funded, with the main objective being the completion of the 2×2 CCD camera head; however, funds for the upgrade of computing facilities were not granted.

At the time of writing the status of the development of the system is as follows: The architecture of the controller has been proven in laboratory use and is now ready for second-generation prototyping (see Section 3.7) and practical use. Control software to

support the next generation of controllers is in use (see Section 4.8) and fully tested. The architecture of the analogue drivers has been functionally proven and is ready for second-generation prototyping. A sound design for the output processing and correlated double sampling has been used. This can be enhanced by modernisation (see Section 3.6). A camera head for the 2×2 CCD prototype has been constructed and is in use. The concept of an indefinitely expansible detector mosaic has been realised in prototype.

Chapter 3

Mosaic Detector System: Design Philosophy

3.1 Introduction—the Mosaic Technique

The background of optical-detector technology for astronomy has been detailed in previous Chapters. The need for larger detectors has been explained. The nature of existing detectors and likely future technologies have been discussed. In this Chapter a practical philosophy for the construction of indefinitely expansible mosaic detectors is described. The design of the system components is discussed, with reference to previous work in the field. The constraints and requirements of the system at a technical level are also discussed.

One simple method of building as large an area of sensor as required is to replicate a single CCD system many times. There are practicalities which limit the effectiveness of such systems. In the future, it may be possible to produce monolithic sensors larger than those available today, but there are practical reasons for avoiding these designs as well.

The primary technology which enables practical large-area sensors of arbitrary dimensions to be constructed is the sensor *mosaic.* The mosaic technique is becoming common in many astronomical-instrumentation architectures and is a real boon when used to optimal effect. The mosaic has a subtlety which the replication of a single-element system lacks, namely that each element is designed to be a sub-part of a complete system and is

optimised for that purpose. The mosaic also has advantages over monolithic architectures when the sub-parts are designed with adaptability or portability in mind.

It should be noted that a mosaic architecture is effectively the same as a *parallel* one. This means that many parts of the system act simultaneously but in a coordinated manner to achieve expeditiously a goal. The design of such a highly parallel system should avoid *bottlenecks.* This means that points in the architecture at which the data (analogue or digital) may be multiplexed should be carefully optimised. Fortunately astronomical mosaic detector systems are not prone to the main gremlin of parallel computing architectures—deadlock[1]. The significance of parallel and evolutionary architectures for data processing should be borne in mind as this forms part of the over-all detector system discussed here.

3.1.1 A Few Examples of Mosaics at Work

The most celebrated example of mosaic technology around in optical astronomy at the current time is the CARA W. M. Keck 10-metre telescope (see Section 1.2.3). The instrument uses thirty-six independent mirrors to focus the light from the sky into a single image. The mirrors are the parallel elements of the system, and they act to multiplex the light into the single image.

Charge-coupled devices themselves use the parallel-multiplex system too. The integration of light occurs in parallel, the data then being multiplexed through a single on-chip amplifier.

It has been suggested[187][192] that mosaics of prisms and gratings may be a useful technique in the construction of spectrographs for very large telescopes. The Keck HIRES spectrograph does indeed use a mosaic échelle grating.

3.1.2 Mosaics Compared to Monolithic Detectors

An image sensor constructed using a mosaic architecture would have the following advantages over an equivalent detector of monolithic design (one of the same pixel count

[1]Deadlock is a condition which may occur in a parallel system where all the elements of the system are waiting to complete communication operations but none of them are able to complete. The situation may arise for many different reasons.

and over-all image area dimensions):

- Charge-transfer efficiency (CTE) problems are reduced as each signal charge packet has a smaller number of transfers to make to reach the device output amplifier. A mosaic architecture has a fixed charge-transfer noise for any size of mosaic.
- Each of the component detectors of a mosaic should be sufficiently flat for most instrument designs and a mosaic may be built to a similar degree of flatness (see Section 3.4.2).
- A mosaic system has a fixed readout time, dependent upon the largest element in the mosaic, regardless of mosaic dimensions.
- The elements of a mosaic system may be operated independently to give different integration times. (An effective increase in the dynamic range of an observation.) Conversely, if only a part of the mosaic is in use, the bandwidth of the output train is higher and a greater time resolution in observation is possible.
- There is some evidence of thermal cycling leading to cracking of larger devices[186]. This is not a problem with existing smaller devices.

A flexible mosaic architecture has the following additional advantages:

- A mosaic can be indefinitely large. The geometry of a mosaic has greater flexibility than a monolithic architecture—this can ease design constraints of the optics of the overall system. Mosaic elements could be positioned to produce a *curved* focal plane.
- Mosaic technologies can be immediately applied to state-of-the-art detectors as they become available. Much of the technology can be applied to infrared detector arrays as well as optical CCDs. The induction of small, high-performance detectors into mosaics creates the opportunity for astronomers quickly to achieve optimal use of new technologies regardless of the pixel format of the devices.
- The elements of a mosaic are fairly independent. Failure of one detector does not preclude continued use of the remaining parts of the instrument. The cost of replacing one *element* will be less than that of an entire monolithic device.

- The range of spectral coverage and response of a monolithic detector is likely to be less than that possible by mixing devices of optimised spectral response. This can be advantageous for spectrograph design—UV/blue- and red/infrared-sensitive devices can be positioned in the appropriate areas of the focal plane.

Conversely, monolithic architectures have the following advantages over mosaics:

- The electronic architecture of a monolithic sensor system is simpler than that for a mosaic.
- There are no inter-element gaps to be considered in a monolith. The gaps in a mosaic must be overcome by optical means or data processing must be used to transform the separate elements into a single image.
- The physical size of monolith (area) should be less than that of an equivalent mosaic as there is no dead space. This might be an important consideration, particularly for Schmidt-camera-type faint-object spectrographs.

Large monolithic sensors are the outcome of many years of design iteration—this is certainly the case for the Tektronix TK2048 device. The adoption of a monolithic sensor would mean that a degree of inflexibility had been built into an instrument—to upgrade the system it would basically have to be replaced completely. Astronomers require the state-of-the-art in instrumentation and to achieve this mosaic and modular architectures are preferred both due to their shorter lead time and their relative cost-effectiveness (smaller development cost compared to large monoliths).

3.2 Outline Technical Specifications of the Mosaic Detector System

These specifications should be regarded along with those given in Section 2.4. These are requirements for a real instrument rather than laboratory testing.

Instrument noise $\approx 1 e^-_{rms}$. This is the initial goal, so that detector readout noise or photon shot noise set the noise floor of any measurement.

Maximum readout time of ≈60 seconds. This is to ensure that as much of the available telescope time as possible is spent on integration rather than waiting for detector readout.

Local frame buffer for image data. The amount of data produced by a mosaic detector instrument could in principle be very large, hence local memory is needed to eliminate data-flow bottlenecks. Ideally the local memory should be sufficient to store *two* images from the system so as to maximise the data-acquisition rate.

Fibre-optic data transmission. To eliminate one source of introduction of electronic noise into the system and provide a (mechanically) reliable link from the instrument control computer to data processing.

Software controlled timing and voltages. To enable the system to be used to operate mixed devices and fast changeover between operational modes.

Very few chip count controller. To minimise cost, maintenance overheads, system size and power consumption and maximise reliability.

Compact device-drive module. As for the previous item.

3.3 Mosaic-Detector System Overview

To discuss the detailed design philosophy of the OSL Mosaic-Detector System it is necessary to begin 'in the middle' of the system architecture—at the focal-plane assembly. It is necessary to do this as the input and output requirements of the focal-plane assembly determine the design limitations for other system components. An overview of the architecture is given here first to clarify how the components fit into the system profile.

3.3.1 System Architecture

An expandable system must be modular in design, thus an arbitrary detector mosaic has to be divided into suitable units for replication. The dividing lines between modules are reasonably self-evident. Figure 3.1 shows how the components listed below fit together to form an instrument.

The parts of the system are:

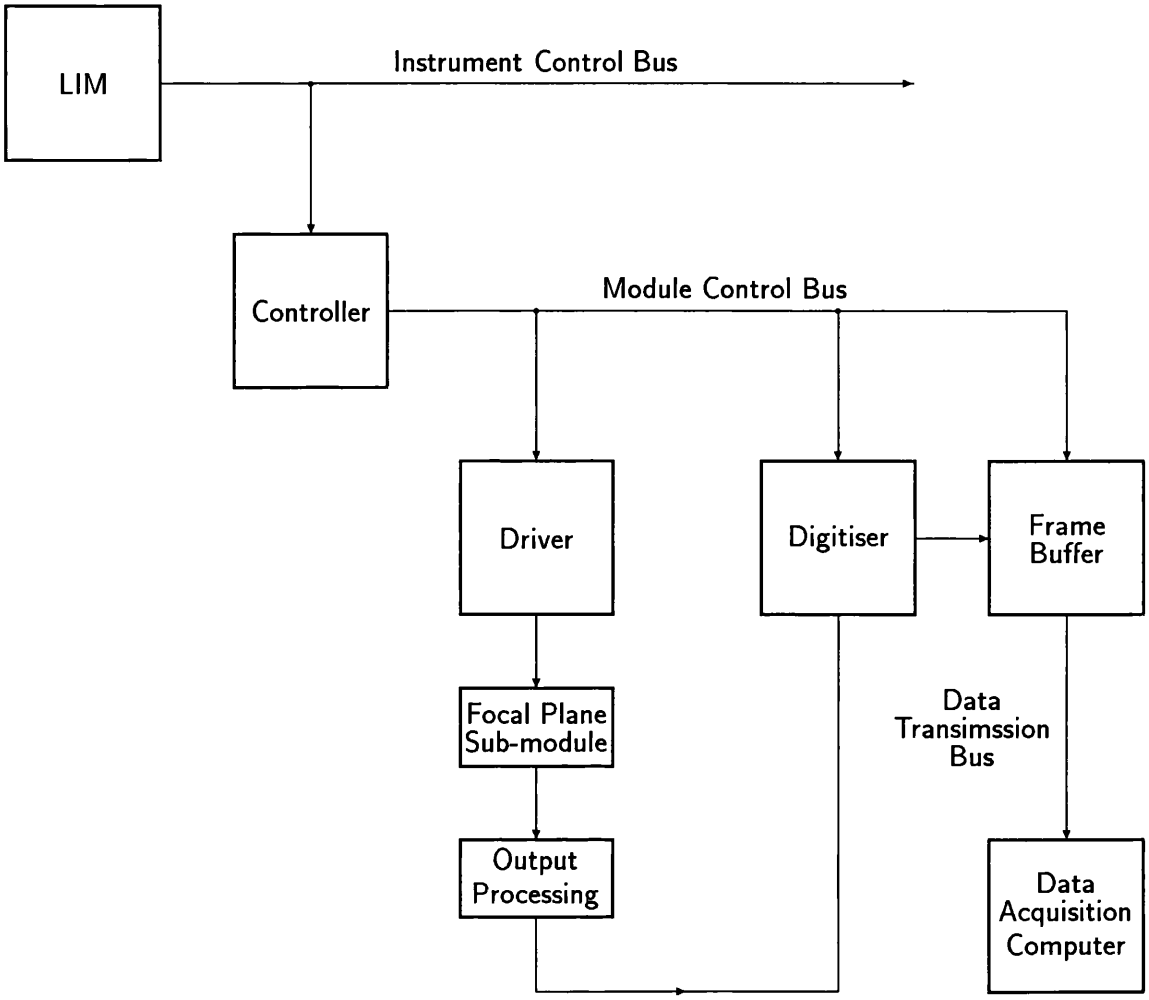

Figure 3.1: Schematic of OSL mosaic-detector system.

Local Instrument Microcomputer (LIM). A computer dedicated to generating the data needed to set voltages and define clock waveforms in the system. This would be situated at the telescope.

Instrument Control Bus (ICB). Communications bus for transmission of information from the LIM to the component modules of the system.

Controller Module. Sequences the electronic events needed to operate the detector mosaic. This is a purely digital component.

Module Control Bus (MCB). The internal control bus for a single focal-plane submodule. This is accessible only via the Controller Module and not directly from the LIM.

Driver Module. Produces analogue bias voltages and translates digital sequences to analogue drive waveforms required to operate detector mosaic. A digital-to-analogue component.

Focal-Plane Sub-module. A group of individual image sensors arranged to form what is, from an optical point of view, a single detector or part of a larger detector.

Output Processor Array. A set of output amplifiers and correlated double samplers, one for each detector in the focal-plane sub-module.

Digitiser Module. Converts detector output to digital information. An analogue-to-digital component.

Frame Buffer. Instrument-local storage for the digital data from the Digitiser Module.

Data Transmission Bus. Communications sub-system for transport of image data from the instrument to processing computer and archival media.

Data Acquisition Computer. The target destination of the acquired image data.

These components are designed in such a manner that they may be assembled into a Mosaic-Detector System with a focal-plane detector array of any dimensions. The majority of the modules have a fixed design, merely having to be replicated in the requisite quantity. The focal-plane assembly is the most instrument-dependent part of the system, along with the cabling between the detector mosaic and driving and processing electronics. These instrument dependencies are identified in Section 3.4.

The design of each of the modules is now discussed.

3.4 Focal Plane Array

There are three overlapping design considerations for the assembly of the focal plane array of sensors: optical, mechanical, and electrical. Of these, the optical requirements are of the greatest importance, otherwise the instrument simply won't achieve its purpose. In this work consideration of the mechanical and electrical problems is made, with some consideration of the optical design included for completeness (the optical design is the subject of other work at OSL).

A current problem with mosaics of common sensor devices is the size of inter-sensing area dead spaces. These represent a loss of data or observing efficiency. For some applications it may be possible to accept the loss of light in these gaps, but for a general mosaic-detector technology to be complete it is necessary to have a method for overcoming them. A related problem is that of device alignment. There are several techniques for overcoming inter-device gaps: the use of mirrors, multiple lenses or fibre-optic tapers for example. The most flexible and efficient technique appears to be the use of lenses. A study of the practicalities of design for the lenses has been made by A. Radley of OSL[147]. For almost all applications of mosaic-detector techniques there will be some pre-detector optics *apart* from the re-focus lenses required to mate the detector to the remainder of the instrument. If a detector is intended to be dedicated to a particular instrument then the functions of refocus and mating may possibly be combined into a single optical element or array (parallel array) of elements. This will lead to improved efficiency. For imaging systems in particular, when a camera may move from one telescope to another, or one focus to another, it will probably be necessary to separate the refocus and mating stages, otherwise an expensive multiple-lens refocus assembly would be needed for each possible detector site. The conclusion of Radley's initial studies is that refocus lenses are a feasible and effective solution to the inter-device gaps.

Closely related to the problem of inter-sensing-area dead spaces is that of device alignment. The modern, fast optical telescopes, especially the new eight-metre class telescopes; require that the component devices of a detector mosaic conform very closely to the intended focal plane. A conformity to better than 50μm across an entire focal plane would be typical. This constraint on device position cannot be relaxed. The position within the plane of the devices is a different consideration however. There are two approaches to this problem: accurate physical alignment of the pixels from one device with those of other devices or software calibration of a rough-aligned mosaic to remove alignment errors.

Several groups have attempted accurate device alignment. The most recent work has been done by the Optical Instrumentation Group at ESO[152]. A device-to-device alignment of about 3-μm accuracy was achieved. However, this was for a 2×2 prototype only. An accuracy of about one tenth of a pixel is required if the pixel size and optics are correctly matched (lens optical distortions would be an effect of similar magnitude).

Thus for pixels of 25-μm dimension the accuracy achieved is acceptable. For the more modern CCDs, which have pixel sizes down to only 7.5μm (see Section 2.2.3.2) a better alignment would be needed. Achieving such an alignment across a larger array, possibly one of very large dimensions, would be a difficult assembly task and may require very careful consideration of differential thermal expansion effects. Initially, the OSL system will use software calibration of any alignment errors in preference to attempting accurate physical alignment. The long-term strategy for data alignment was developed as follows.

3.4.1 Partially Buttable Detectors

At the outset of the OSL project to investigate mosaic-detector technologies it was envisaged that die-state CCDs would be assembled, probably by epoxy bonding, on to a common, probably ceramic, substrate. In practice this is undesirable for several reasons, the most significant of which is the maintainability of such an assembly. It would be quite difficult to replace a faulty or damaged device in the middle of a mosaic without damaging adjacent devices. Another problem was that potential suppliers of the die-state devices would not be able to test the devices beyond the basic probe test (for device functionality) before the wafers are cut. This is because they are not equipped to test unpackaged devices at cryogenic temperatures. The potential therefore existed to construct an expensive mosaic which would have effectively permanent cosmetic faults and no maintainability. After discussion with designers at EEV a different approach was adopted. Each device would be mounted on its own carrier, the packages being assembled by EEV and the devices tested at the OSL. This approach was appealing for several reasons. Firstly, the special carriers could be made with very little dead space (see Figure 5.4) which is a requirement for the refocus lens system to be feasible. Secondly, the carriers could be manufactured from a multi-layer ceramic sandwich carrying some surface-mount electronics, for example a constant current source for the device output and temperature-control diode-resistor pairs. Thirdly, as each device is individually packaged it is easy to replace any which are faulty.

Prototype carriers were designed by P. Pool of EEV and a set of five devices plus several empty packages for evaluation were delivered to the OSL in February 1991. The internal connections made on the carriers reduced the number of connection pins to only 14 (from 44 for the normal package for that device)—an additional bonus for PCB design.

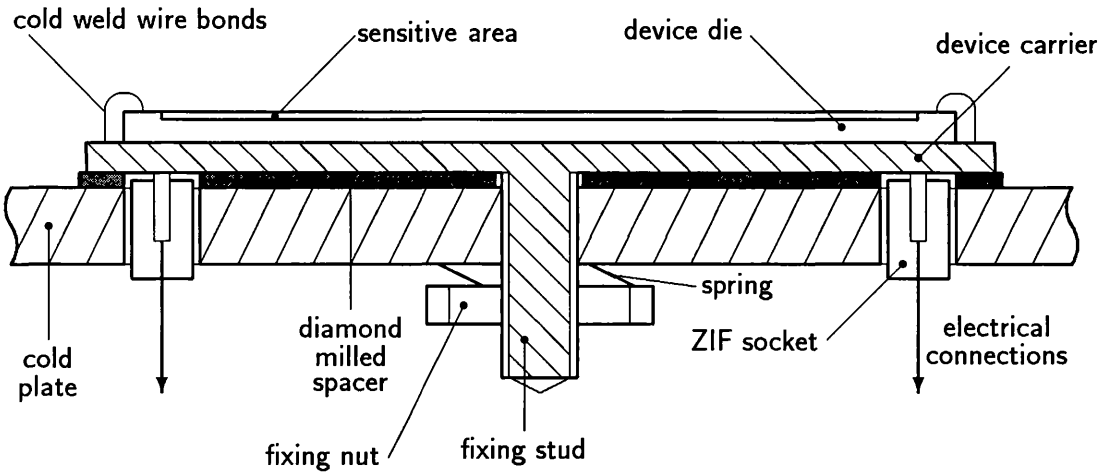

Figure 3.2: Mounting for single CCD.

The purpose of these devices is to demonstrate the mosaic control electronics and the implementation of some of the focal-plane assembly ideas.

In the longer term, the use of silicon foundry services would be combined with custom designed carriers to create the focal-plane elements. This would allow the mixing of optimised devices and the *user definition* of the devices, as well as using available sensors as best as possible.

3.4.2 Focal-Plane Optical Flatness

The EEV-manufactured special-packaged CCDs are intended to be assembled in a non-flat, non-aligned mosaic for demonstration of the electronics and investigation of system performance. The empty packages also supplied are for the investigation of mosaic assembly techniques. Figure 3.2 shows schematically how a single device on its carrier is mounted to be part of a mosaic focal-plane. A threaded stud is attached to the rear of the supplied package to fix the device to the cryogenic 'cold slab'. The heights of the corners of each device are measured using a short-focal-depth optical microscope. A diamond-milled copper spacer is then prepared to compensate for errors in the device's front-surface position relative to the rear surface of the chip carrier. The spacer is then placed behind the device, bringing its front face into the focal plane. This process is repeated for each device in the mosaic. This system allows a single device to be removed from the mosaic and replaced. The required optical flatness can be achieved.

This simple assembly technique successfully achieves the project's primary goal of an accurate conformity to the required focal plane. In the medium term, the use of an *active* support technique may be more desirable. Very accurate position adjustments can be made by the use of *piezoelectric* devices. These devices exhibit small and reproducible dimension changes when voltages are applied to them. If each device in a mosaic is mounted on a piezoelectrically positioned carrier then it should be possible to not only create the required focal plane but also maintain a device-to-device pixel alignment to a high accuracy. Two uses of this method are: as part of the detector assembly for an actively flexure compensated spectrograph for a large telescope; and in space-borne actively-positioned optical systems, where thermal cycling effects can be significant.

3.4.3 Electrical Considerations and Wire Routing

In both the existing device-mounting method and any active system the electrical connections would be made via zero-insertion-force sockets which would float freely in holes through the cold slab (see Figure 3.2). The wiring is effectively routed away from the focal plane using the depth of the vacuum enclosure.

3.5 Analogue Drive Waveform Generation

Traditionally, optimisation of the analogue driving part of a CCD system has spared no expense of size or circuit complexity. In a mosaic, especially a large system, this cannot be the case. The performance required of mosaic drive circuitry remains the same, however.

In a practical system it may well be necessary to site the analogue part of the drive electronics *within* the cryostat. Previous systems have differed widely in the amount of electronic circuitry positioned within the vacuum space, from the system of Wright & Mackay[204] which had no electronics except the CCD within the cryostat, to systems with heavy filtering of the input signals and output amplifier circuits at the camera head[191]. The problem with an indefinitely expandable mosaic is that the number of lead-out wires from the evacuated space is, to first approximation, directly proportional to the number of detectors. By placing the analogue clock drivers and bias-voltage sources within the cryostat, the number of lead-outs can be greatly reduced. Either the

module-control buses or perhaps even the instrument-control bus, plus power supplies and outputs would be the only lines to pass through the cryostat jacket.

For minimisation of mechanical design and monetary cost, if the system is sufficiently small (of the order of about two hundred leads to the head assembly needed), positioning of driver electronics outside the cryostat may be selected. This would ease the thermal constraints on the camera head and facilitate the use of simple intra-cryostat systems.

The generalised mosaic technology must offer an analogue driver module with the following characteristics:

- Low power consumption.
- Small physical size.
- Safe for low-pressure use.
- Minimum cross-talk.
- Ease of maintenance.
- Low cost.

In addition to these general design requirements a driver must also be able to provide the signals required to operate a wide range of detectors past, present, and future. There are two types of signals needed: static bias voltages and time-varying clock voltages. These are now discussed in turn.

3.5.1 Bias Voltages

The bias voltages required by CCDs can be generated by simple analogue circuits. The voltages must be controllable to allow device optimisation and operation of a range of devices under a range of conditions. To achieve low-noise performance in the detectors it is necessary to have a high degree of stability in the bias voltages. This is especially true for the output drain of CCD output amplifiers as any noise on the drain voltage is directly coupled to the output signal. The bias voltage requirements of most CCDs can be met (see Section 2.2.4) by sources with output in the range 0V to +25V. Setting of bias voltages to 0.1V accuracy is sufficient for device optimisation. This requires a

resolution of about 1 in 250 or eight bits digital. Eight-bit digital to analogue conversion is therefore acceptable.

3.5.2 Clock Voltages

The nature of the clock voltages required by most operation modes of CCDs is quite simple. During each clock cycle, the voltage will move from one value to another and back again, or, remain steady (during binning). This gives the waveforms a basically rectangular form, although for correct operation of the charge-coupling process a slight slope to the edges is required. As described in Section 1.4.2, charge coupling occurs when the voltage on one electrode is raised and then the voltage on the electrode which had previously held the charge is lowered. Normally the two voltage transitions overlap; this keeps the ground (substrate) clean as transient currents in the device are, to a first approximation, equal and opposite. The shape of the edges is not important[30] as long as they are smooth and the *overlap occurs at the 50% of peak-to-peak height or above* [30]. For this reason software control of transition-edge shape is not necessary as long as the edge shape is cleanly defined in hardware. Software control of the edge timing is needed, however. For operation of CCDs at slow-scan rates an edge transition time of about 1μS is required, this allows the device to be operated at pixel rates up to 100kHz.

Typically, the peak-to-peak range required of the clock voltages is less than 15V. As discussed in Section 2.2.4, an output voltage range of about 25V is sufficient and matches well with the bias level driver specification.

3.5.3 Buffer Design

The analogue-buffer design selected to meet these specifications incorporates a DAC buffered with an op-amp and output filtering. The gain in the op-amp stage sets the full-scale voltage range and the R-C output filter sets the clock edge transition time. The circuit for one buffer is shown in schematic in Figure 3.3. The circuit is replicated as many times as required for the system. Typically, this would be 64 times for a single driver module. The 64 buffers are split into two groups, one for bias levels and one for clock signals. The two groups output offsets being set by separate offset sources, in the case of the bias levels from the ground.

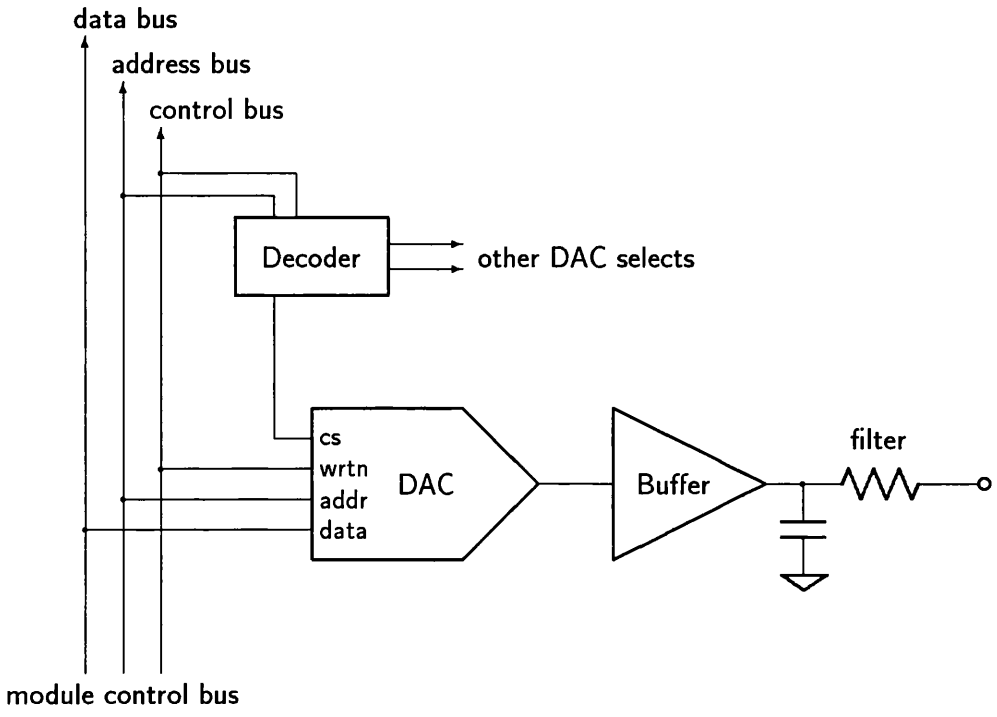

Figure 3.3: Single channel driver circuit schematic.

A second clock driver design has also been selected, the two designs being evaluated in laboratory tests. This design (Figure 3.4) uses two DACs to supply the high- and low-level voltages required to drive a single clock register of a detector.

These simple designs facilitate compact circuits. Multiple unit packages, for example octal DAC and quad op-amp packages, have been selected to further facilitate a small physical size for the driver.

3.5.4 Component Selection

Octal eight-bit DACs are marketed by at least two manufacturers. These are Brooktree (type Bt110) and Analogue Devices (AD7228). The Bt110 device is a current output circuit. Several ancillary components such as output-range adjustment resistors are required. The AD7228 is a voltage output device, with its own internal output buffers. This device does not require as many extra parts as the Bt110 but does require an external voltage reference (the Bt110 is internal). Of the two devices the AD7228 is smaller

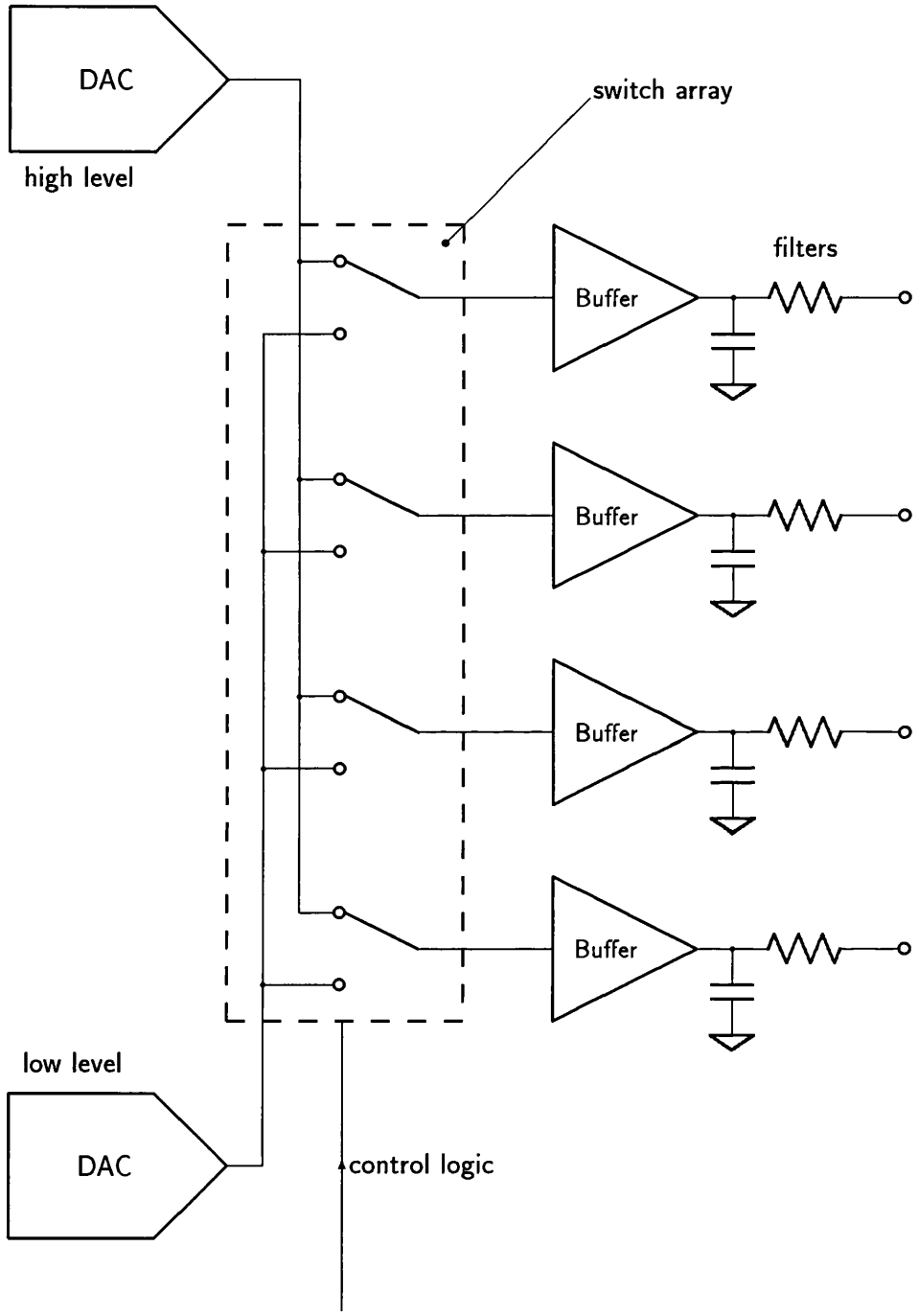

Figure 3.4: Single register driver circuit schematic.

(in both DIL and surface-mount packages) due to its fewer number of pins. Both devices have similar digital interfaces and exhibit 100nS digital cycle times. The most significant performance differences between the devices are: the Bt110 has an output settling time of 100nS compared to 5μS for the AD7228; and the Bt110 has an output compliance

limit from −1.0V–+1.2V whereas the AD7228 can operate up to +10V. These differences mean that the AD7728 is not sufficiently fast to drive CCD clock voltages directly and that the output from the Bt110 must be passed through a gain stage of about ×25 to generate the required swing. Because both devices are octal packages and available in surface mount versions, highly compact circuits can be made.

For the buffer stages of both designs quad op-amps have been selected. A standard pin configuration (both for DIL and surface mount packages) exists for quad-packaged op-amps making possible direct component upgrade in the designs. A wide range of quad op-amps is available; the fastest currently available is the Motorola MC35085 with an output slew rate quoted at 55V/μS, which is more than sufficient for CCD drive requirements.

The selected op-amps for the prototypes are the PMI OP-471GP, which is a low-noise amplifier device and the Motorola MC33074 which is a uni-polar device. These are used for the clock lines and bias levels respectively.

These particular components have been selected because they meet the performance requirements; because they represent a high level of integration; and because they are available in surface mount versions. The system is intended to be progressed through three design stages: first, wire-wrapped prototypes; second, traditional printed circuit boards (PCB); and finally, a production version surface mount PCB. Using the selected components a 64-source driver module (enough to drive four CCDs) would occupy at most only 100 cubic centimetres.

3.6 Signal Train

As discussed in Section 1.4.2.1, the output from a CCD is typically a small time-varying signal superimposed upon a relatively large static voltage. To achieve low-noise performance this bias pedestal must be removed and the remaining signal sampled.

The output transfer function for modern CCDs is of the order of 1μV per electron (see Table 5.1). Most analogue-to-digital converters have maximum resolutions of the order of 100μV, and thus a significant gain is required to achieve a useful resolution. The gain will depend on the mode of operation and dominant noise source in the system. In

general the noise floor (usually the detector noise floor) will be arranged to produce a signal of a couple of ADUs so that the noise signal is reasonably sampled. Thus for a detector with output noise of $4e^-_{rms}$ an output voltage gain of the order of $\times 50$ to $\times 60$ will be required.

To achieve such a signal gain an integrator is often employed. The basic technique used for low-noise astronomical CCD-based cameras is *correlated double sampling.* This method removes noise in the bias pedestal (reset noise).

3.6.1 Correlated Double Sampling

The technique of correlated double sampling for noise reduction in CCD output circuits was first documented by White[202]. For example (see Figure 5.28), the output signal from the CCD is high-pass filtered (AC coupled) to remove the DC component. This DC component is most of the reset voltage of the CCD output amplifier; which is subject to an uncertainty known as reset noise for each output pixel (see Section 2.2.4.1). Because the signal is always relative to the actual reset voltage it is possible to remove the effect of reset fluctuations by accurately measuring the output voltage *before* the output of charge from a pixel and then finding the difference between this value and that after charge output. This is achieved by the use of a two-phase sampling process. First, after output node reset, the output voltage is integrated for some period of time, t_s, before charge output. A signal charge is then moved to the CCD output node by charge coupling. This reduces the voltage on the output node slightly. The resulting signal is then sampled *with precisely the opposite gain* to the first sample on to the same integrating capacitance for the same time t_s. This reduces the voltage on the integrating capacitor, until some small positive voltage which is proportional to the CCD output charge remains. This signal can then be digitised.

Correlated double sampling and the similar technique of 'clamp and sample' are used highly successfully in many CCD systems. This is the most practical system for acquisition of data from detector mosaics. Unfortunately, the output signal from a detector must always be connected to its sampler during the two integration stages. To minimise system noise the proportion of readout time spent on integration as a fraction of pixel readout time should be maximised. This implies that one correlated double sampler is

needed for each detector. Fortunately, the design of these circuits is now highly refined and noise performance of the order of equivalent $1e^-_{rms}$ is routinely achieved. The main requirements for mosaic-detector systems will be:

- Identical noise performance for multiple-device systems as for single-device.
- No significant cross-talk between detector output channels.
- Minimum circuit size and power consumption.
- Minimum unit cost.

These requirements are common to the whole system. The design and implementation of a surface mount or hybridised output processor is recommended by the author for mosaic-detector systems. Unfortunately, at the time of writing, funds were not available for such work to be undertaken. Thus, for the purposes of the current research; the preamplifier-correlated double sampler used for the UCL SAAO CCD system has been used. This is described in Section 5.9.1. Later in the research programme some funds were allocated for the construction of two signal processors based on the Leach preamplifier/correlated double sampler. This is described in Section 5.9.2.

3.6.2 Digitisation

In a single-detector system the signal from the output processor is fed directly to a single analogue-to-digital converter (ADC). To optimise the size and cost of a mosaic system the signals from several detectors should be multiplexed to each ADC. To achieve this, a fast ADC is required and the output from each of the detectors must be phase shifted so that they do not all appear at the same time. The RGO[100] system used for the WHT ISIS spectrograph detector includes a similar multiplex technique. In that case, however, the detectors are operated in parallel and thus the signals from the devices arrive simultaneously at the digitiser. This is a potential source of noise due to voltage droop on the integrator outputs. Some cross-talk was detected in that system when large signals were adjacent to small signals. This can be overcome, first by preventing the input buffer of the ADC from becoming saturated, and secondly, by clamping the input to ground between each pixel digitisation. Channel-to-channel cross talk can be minimised by using individual analogue switches for each signal channel.

3.6.2.1 Analogic AM40016 ADC Module

If a pixel readout time of 50μS for each detector in a mosaic is specified then if, for example, eight detectors are used a conversion time of, at most, about 6μS is needed. To achieve this the Analogic AM40016 Sampling ADC module has been selected. At the beginning of the mosaic-detector project at OSL this was the fastest module available. The integral sampling circuit and simple trigger and output buffer circuits make this an ideal selection. The module has a maximum signal acquisition and conversion time of 2μS making the digitisation of signals from eight devices, and perhaps more, possible.

3.7 Controller Module

The architecture of CCD controllers for astronomical cameras has progressed greatly from the early designs. There have been three 'ages' of controller design which have developed in accordance with the available semiconductor technology. The function of the controller is to define the waveforms and logic pulses required to operate the detector(s) and to sequence these events appropriately.

3.7.1 CCD Controllers—Existing Technologies

The earliest controllers were of a *hardwired* design. This means that the function of the circuit is defined in hardware and requires a circuit modification to alter the programme. Examples of this architecture are the Cambridge CCD system[204] and the Palomar Observatory system[72]. CCD systems for astronomy usually have to be flexible to cater for a wide range of operational modes. This means that newer systems are rarely built with hardwired controllers. It is, however, possible to construct an extremely compact camera system using a hardwired design.

The fixed readout pattern of hardwired systems has now been replaced by controllers with a programmable architecture. Among the earliest of the programmable designs is the Kitt Peak National Observatory (KPNO) system[68]. The KPNO system uses a bit-slice microprocessor (type 2901) and programmable read-only memories (PROM) to store the the programme for the microprocessor. To change the operating mode of the camera the PROMs must be replaced or reprogrammed.

In truly programmable systems the memory devices used are random access (RAM). An example of this type of system is the RGO system; which was originally developed to operate CIDs[101]. The programme for the controller is stored at the LIM and down-loaded to the system when the power is activated. To alter the operating mode a new programme is down-loaded. Many different operation mode programmes can be stored at the LIM and thus fast mode-changing is possible. Another advantage of the programmable design is its flexibility—the same architecture can be used to operate many different detectors simply by altering the programme.

The most recent camera control systems have even greater flexibility than the bit-slice processor based systems. There are at least four of these contemporary controller designs. The design philosophy of these controllers is dominated by the operational requirements of large-area detectors. The architectures of these systems are based on micro-processors: the *digital signal processor* (DSP) and the *Transputer.*

The DSP is a *reduced instruction set* processor which means that most of its instructions are completed in a single clock cycle. This is useful where accurate timing is required. The Transputer is a parallel computing architecture element—it is designed for use in such systems. Transputers are excellent at communication functions and require little 'glue' logic for their operation and networking.

The first of the modern systems is the DSP-based 'multiple readout CCD controller' designed by Leach and Beale[113][114][115]. The DSP used is the Motorola DSP56001. The processor runs at an instruction rate of 10MHz. The system is designed to operate up to eight simultaneous CCD readouts and is particularly aimed at 2×2 mosaics of 2048-square class devices. The controller deals with all communications between the system and LIM as well as co-ordinating the focal-plane readout. Section 3.5 explains how digitally controlled waveforms and control voltages are generated in such systems. It is primarily by means of such digital control that this system advances in its flexibility over previous controllers. The hardware is compact (single board, $9.9\times22.9\text{cm}^2$) as well as controlling many readouts.

The second of the modern systems is based around the Inmos T222 Transputer. This system was developed at the RGO by Waltham and Van Breda[23][195]. The processor is operated at 20MHz; however, the architecture of the system means that the maximum

waveform-update rate is 5MHz. This system is designed to be as compact as possible, it is intended for the operation of single-detector cameras at the RGO. However, the controller should be able to operate several detectors in parallel. The communication functions in a system based on this controller are handled by a separate 'personality' card. This controller is again very compact having only about a dozen IC components.

The third contemporary controller is that for the ESO buttable-CCD mosaic. This system was developed by Reiß, D'Odorico *et al*[152]. The heart of the system is an Analog Devices ADSP-1401 Word-slice Programme Sequencer. The system clock in this case is 10MHz. This system is designed for operation of mosaics, the structure of the bus used is sufficient for sixteen readouts per controller. Communications are handled by other circuitry.

The last of the four systems is that developed by Smith at CTIO[162][163]. This system is Transputer based, with a waveform update rate of, at most, 20MHz. The controller is only designed to generate 48 waveform timing signals for the subsequent electronics; thus this controller may operate up to four readouts in parallel. A second Transputer is dedicated to host communications.

The software required to operate these systems is discussed in Section 3.8—the complexity is related to both the number of detectors or readouts in the system and the architecture of the controller.

3.7.2 What is to be Controlled?

The driver-module architectures discussed in Section 3.5 provide the bias-voltage levels and clock signals required for the operation of the focal-plane mosaic. The bus backbone of the driver allows huge flexibility in the actual voltage signals which may be generated. The system is capable of producing all manner of waveforms most of which are not required to operate detectors. In fact, the operational requirements of even a large array include only a small sub-set of the range of the driver. This matter is discussed in Section 3.8 where the software model of the system is constructed.

The controller's function is to read out the detector mosaic. The readout of detectors can have several subtleties such as binning or the use of the drift-scanning technique. In terms of the driver module these appear as similar actions—series of voltage-change

events. The readout of the detectors always necessitates the cyclic repetition of certain series of events. Typically these events are of two types: those associated with the parallel (or vertical) movement of image signal and those associated with serial (or horizontal) movement of signal to device output nodes. A complete readout will consist of the product of these cycles.

In a mosaic we may require that all the component detectors of a mosaic be read simultaneously. This, again, appears to the driver as a series of voltage-change events. These events can be multiplexed into memory at the controller. Repeated patterns can be stored with counters and memory pointers (addressing registers) used to cycle around these data as required to generate the stream of data which must be sent to the driver to produce the readout desired.

Such a simple architecture is all that is needed for the operation of the detector mosaic. The architecture remains flexible as most of the variation in readout modes exists within the data stored in memory. These data are undefined by the controller and must be provided from elsewhere—software.

3.7.3 Programmable Logic Device Technology

The early astronomical CCD cameras used hardwired logic. For example, the controller for the UCL SAAO CCD system developed at UCL consisted of over one hundred TTL logic family integrated circuits. Each TTL device has a fixed logical purpose. In the late 1980s large programmable logic devices became available. These devices allow engineers to electrically programme standard, off-the-shelf logic elements to meet the specific needs of their applications. There are several types of programmable logic device: programmable logic arrays (PLA) and programmable logic devices (PLD) are the most commonly used. PLDs are based upon CMOS EPROM technology. The largest range of PLD and erasable programmable logic devices is manufactured by the Altera Corporation of San Jose, California, USA[3]. Altera devices are used throughout the mosaic-detector project prototypes. Altera PLDs of up to 20 000 gates with 200 pins (EPM7000 series) are now available. A single EPM7256 device is the equivalent of 200 or more standard TTL devices.

The internal architecture of the PLD is based around a single internal interconnection

array. In the EPM7256, 256 *macrocells* are arranged into *logic array blocks* (LAB) which are all accessible from the interconnection array. A macrocell is an array of EPROM cells which can be used to produce combinatorial logic functions based on the macrocell's inputs. Each macrocell has a single OR and XOR function and configurable output register. Most logic functions can be implemented in single macrocells, however each LAB has a pool of additional product terms (logical ANDs) which can be routed into the LABs component macrocells as required by the design. This architecture leads to *predictable* gate delays and logic timing. The first generation EPM7256 can operate at clock speeds of over 80MHz[3].

To implement logic functions in programmable logic several CAD tools are available. The proprietary Altera package (MAX+plus) has been used in the mosaic-detector project. Figure 3.5 shows the MAX+plus design cycle. The user creates a logic design using TTL component emulations and other *macrofunctions*, basically assembling a schematic of the logic design as if it were to be implemented in discrete components. The Altera compiler then optimises and fits the logic to the internal architecture of the target PLD. A compiled design can be tested in software (by a simulator) and logic delays can be predicted and examined by this means.

Because of the potential complexity of the internal logic of a single device the schematic capture software uses an *hierarchical* system to enable the designer to structure the design in a block fashion.

The programmable logic device offers a real alternative to microprocessor (Transputer, DSP or otherwise) based CCD controllers.

3.7.4 Architecture of the OSL Mosaic-Detector Controller

The existing astronomical CCD controllers (see Section 3.7.1) illustrate the use of DSP and Transputer technologies to this application. In the previous generation of controllers *bit-slice* microprocessors were used, these designs have been abandoned due to the ease of use (electrical), speed and ease of programming of the more modern devices. The architecture of the modern designs is quite simple, as is illustrated in Figure 3.6.

The two major components of such a controller are the processor and the memory cache. The main functions of the controller are simple input and output to both the system

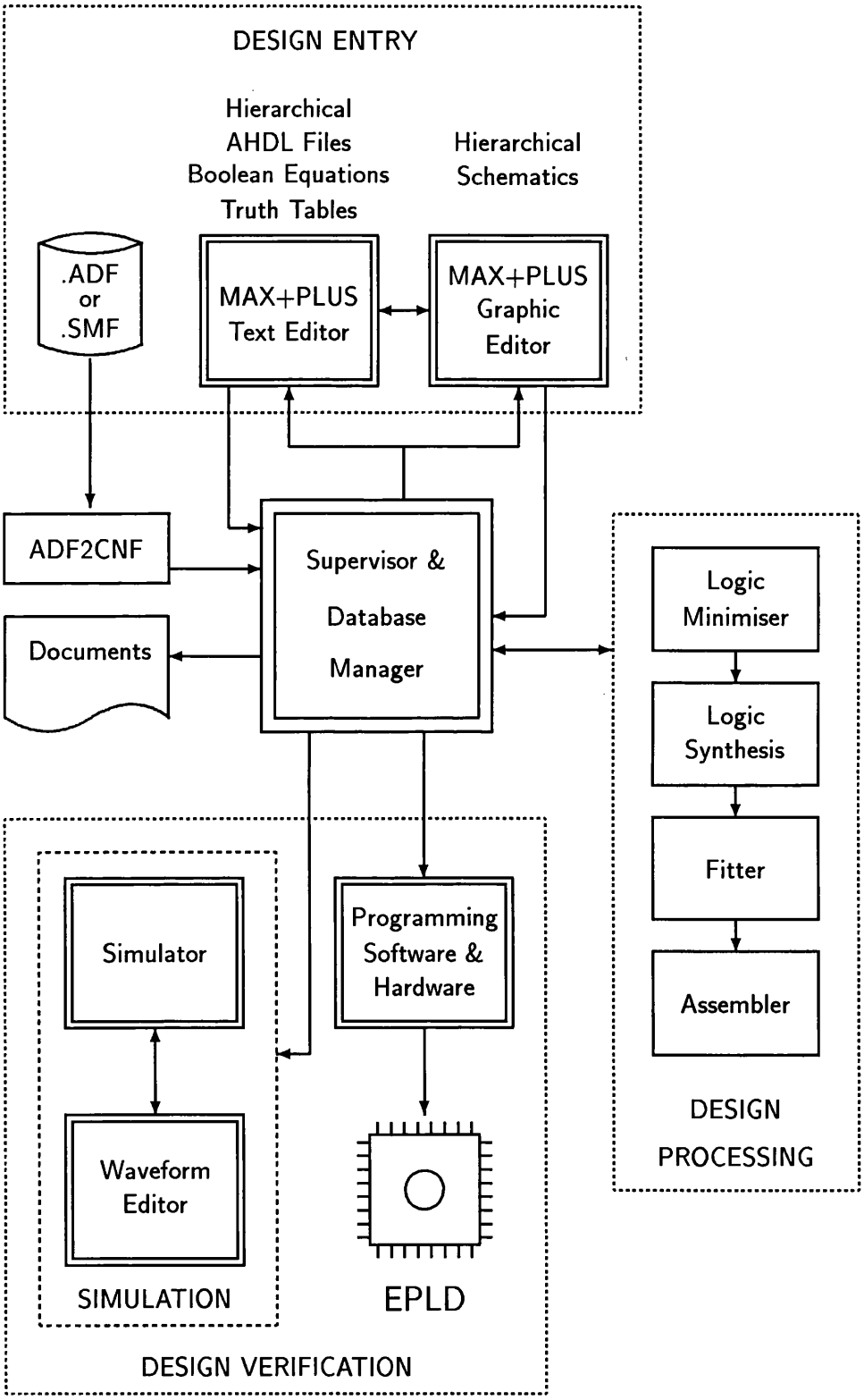

Figure 3.5: MAX+plus design cycle. Courtesy W. Han.

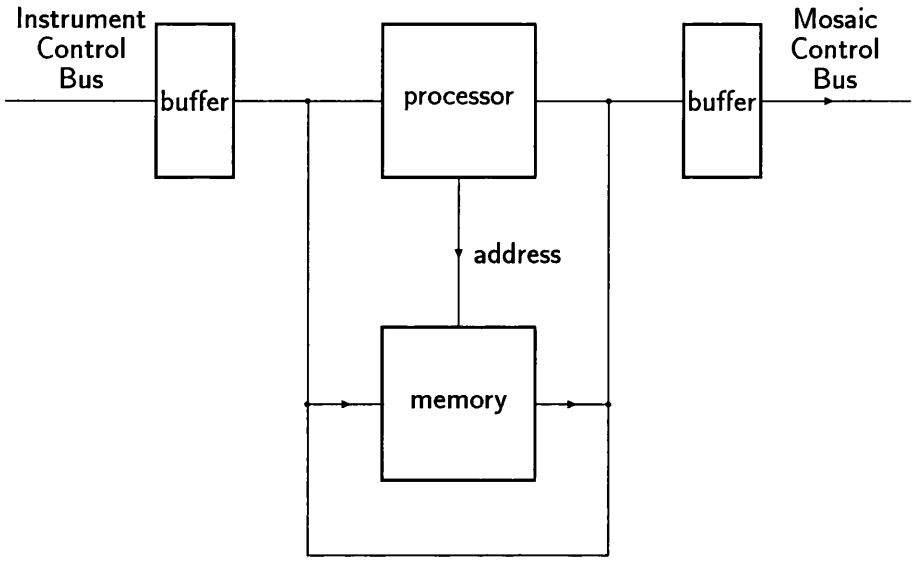

Figure 3.6: Architecture of contemporary CCD controller.

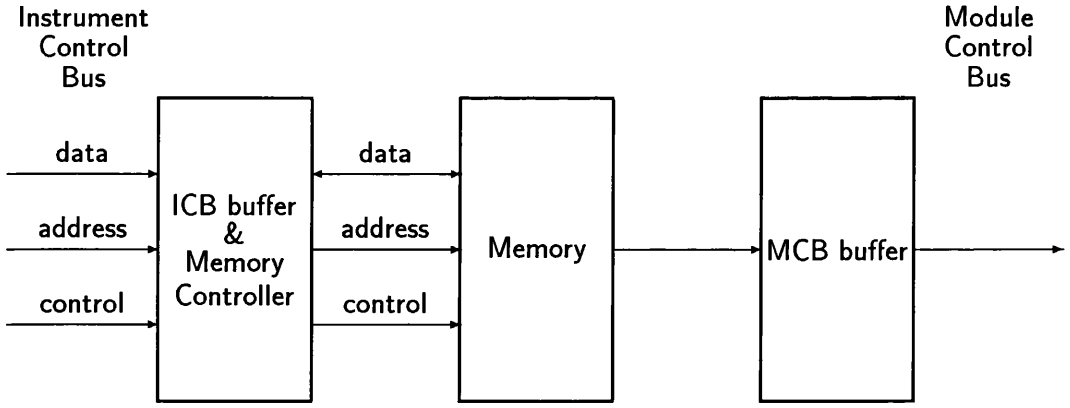

Figure 3.7: Architecture of OSL CCD controller.

hardware and the system-control computer. Functions such as looping are also needed to generate the repeated waveform patterns necessary for the operation of the detector array.

The OSL controller architecture is conceptually identical to these systems, however, the local processor function is split between two PLDs (see Figure 3.7). One PLD deals with communication with the system-control computer and the highly reduced controller command set. The second PLD deals with communication with the system hardware.

This architecture has several advantages over other systems:

- In principle, a multiple detector controller can be implemented in only four ICs (two PLDs, one memory, one clock).
- The clock speed for PLDs has been about four times that of contemporary microprocessors for about the last four years (although the speeds of both have increased). For example, the fastest clock rate used in the existing designs is that of the CTIO controller at 20MHz, this compares with the 80MHz clock rate for the EPM7256. This is particularly important for the operation of multiple infrared detectors where the readout rate is higher than for CCDs, and for any faster-readout mode CCD system, for example in a wave-front sensor.
- A PLD-based architecture can be simulated in software and potential timing errors removed. Timing delays in the final design are completely predictable as the PLD is not subject to any I/O or interrupt overheads.
- The instruction set for the PLD can be made exactly as large as is needed for operation of a mosaic of detectors. This greatly simplifies programming of the controller as effectively *no* software runs on the controller; rather, the programme is implemented in hardware. Such a design does not lack the flexibility of microprocessor-based systems as it is easy to add additional functions to the internal logic of the PLD and simply replace the device on the controller. A carefully designed system will be able to carry out all of the functions needed for a mosaic-detector system.

The hardware specification of the OSL mosaic controller module is as follows.

- Controller-internal clock rate: 40MHz.
- System bus maximum data rate: 40MHz.
- 32 bits per 'event' in memory as follows:
  - 16-bits system-bus address,
  - 8-bits system-bus data/action,
  - 8-bits controller instruction.

The 16-bit module-address bus allows for up to 65 536 independent waveforms or functions to be accessed by a single controller. Although 8 bits are reserved for controller instruction, only a small number of a possible 256 instructions are likely to be used.

- Minimum memory configuration: 65 536 bits (corresponds to one op-mode for 16 CCDs).
- Maximum memory: 2 097 152 bits (corresponds to 16 op-modes/ancillary programmes for at least 16 1024×1024 pixel class CCDs).
- 2×16-bit pixel counters. This allows for waveform repetitions up to 65 535 times, sufficient for all existing devices.
- Memory controller as follows:
  - 4-bit programme page address latch; this selects from up to sixteen system-operation programmes which can be stored in the controller internal memory cache. Only one programme is active at any one time.
  - 16-bit memory address counter/latch; this generates the address of controller internal memory which is to be accessed, *not* the module bus address which comes from the memory itself.
- Minimum ('reduced') instruction set—each instruction executed or instigated in one controller clock cycle (25nS).
- Software reset: the controller hardware can be 'warm booted' from the instrument control computer.
- Software interrupt: the currently executing controller programme can be halted by the instrument control computer.

3.7.4.1 System Module Internal Control Bus

As mentioned in Section 3.7.4, the internal bus of a system module consists of eight data bits and sixteen address bits plus control lines. This specification was chosen on the basis that a single CCD might require 32 addresses for drive waveforms and bias levels

plus output processing. (This compares with 13 for a GEC P88000-class device with one output in use: 7 clocks, 5 bias levels and one address for output processing.) Thus a mosaic sub-module of 16 CCDs might require 512 addresses for basic operation. The provision of a vastly larger address space than necessary allows for the operation of ancillary functions such as shutter operation, bias lights, filter wheels and other mechanical functions. Although the data bus is only 8 bits wide it is easy to transmit larger words in a serial fashion, and again the large address space allows plenty of headroom for such a development.

The data rate on the bus is 40MHz, which is much faster than the update rate required of a single CCD driver or even of a single DAC (see Section 3.5). Driver and digitiser modules which are operated by the controller therefore have to modify the information from the bus to suit their own capabilities. No acknowledgement is required from the slave drivers and digitisers which reside on the module internal bus; conversely this means that, from a hardware point of view, no error checking is made. It is assumed that the compiler software for module-operation programmes will prevent the user from accessing two addresses in the same driver if this contravenes the driver's own capabilities (see Section 3.8).

3.8 Control Software

Software is the most nefarious part of any instrument. Most astronomical instruments have their own unique software, often only understood by a very small group of people. Fortunately, the advent of global networking, and the standards appearing due to Starlink and other astronomical networks, are unifying forces. Several new software techniques have come to light in the few years that the OSL mosaic-detector project has been underway. The most significant of these are *object orientated programming,* parallel data-processing and user-interface standardisation. To varying degrees these ideas are incorporated in the control software of the OSL system.

Most of the existing detector-control systems require some low-level programming of their sequencer or controller modules. Such programming is orientated toward the code itself and not the *detectors.* The mosaic control software will have to be more closely related to the detectors themselves rather than the control code simply due to the potential

amount of code needed. For this reason, an application-oriented compiler—essentially a command language for the description of mosaics of detectors and their operational requirements—is needed.

The compiler will require some ability to group information, in a manner analogous to the directory-file structure used in many operating systems. Such an *hierarchical* structure is needed to keep the operation code for the system at an acceptable level of complexity and avoid large lists of information. The modular nature of the code which will result also aids in code reusability and maintainability.

Considering the controller architecture described in Section 3.7, and a typical operation mode, an estimate of the amount of data required to operate a single focal-plane sub-module (*i.e.,* the size of the controller code) can be made. For example, if the pixel readout rate from the sub-module is 10kHz and assuming a vertical transfer time of 100μS, a single controller programme is of size about 32kbytes. When a mosaic is composed of many sub-modules this programme size can become significant if the data rate on the instrument control bus is slow (for example, limited by serial communications). The control software must not worsen this problem by adding a time overhead during programme down-load, for this reason module-operation programmes should be available in a binary form to be directly down-loaded to the system when the mosaic is being used.

One possible danger of the highly flexible hardware specification outlined above is that of damage to the component devices of a mosaic by applying voltages out of specification. The wide range of voltages which may be produced by the driver module means this is a real danger. The mosaic-control software must be able to recognise and apply the manufacturers' device voltage limitation rules. In practice this will mean simulating the operation of each module's operation programme in software to ensure that the rules are not broken at any time.

Once the mosaic-detector system has been proven in prototype form (see Chapter 5 and 6) it will become necessary to be able automatically to perform as much device optimisation and characterisation as possible. The software should contain tools to enable these functions.

3.9 Communications

There are two important data paths in the mosaic-detector system: the LIM to instrument control bus path (input) and the frame buffer to data acquisition computer path (output). The data rate on the output path is, of course, much greater than on the input path. In practice, the required data rates will be approximately in proportion to the size of the whole mosaic and the readout rate of the detectors. Modern astronomical instrumentation has adopted the use of *fibre optics* to link instrument-control and data-acquisition computers to the main instrument racks. Fibre optics have the dual advantages of preventing the transmission of noise in digital circuitry to the instrument and immunity to electrical noise in the environment of the observatory. For these reasons, fibre-optic communications should be adopted.

A particularly effective solution for both input and output data-paths is the use of high-speed serial communication links, for example, the Advanced Micro Devices Am7968/-Am7969 combination[2]. These convert an eight-bit input word into a serial data stream. The maximum data transmission rate for these devices (known as TAXI for Transparent Asynchronous Transmitter/Receiver Interface) is quoted as 100Mbit per second. A single TAXI link can carry data from about 600 detectors operating at a 10kHz pixel readout rate. Using a single TAXI/fibre link for LIM to ICB communications is sufficient for control of extremely large detector arrays. Detector arrays up to about 100 devices will not use the full bandwidth of a second TAXI/fibre link for data output. For larger arrays the output TAXI/fibre link can be duplicated.

In summary: communication between the instrument control computer, system and data acquisition computers can be effectively implemented for mosaics for hundreds of CCDs using TAXI/fibre links.

3.10 Processing and Archival of Mosaic Image Data

As discussed in the previous Section, the transport of the data from a mosaic-detector instrument is a soluble problem. More significant problems from an astronomer's point of view are: the computing power needed to reduce the data; the time take to reduce the data; the time taken to store data in an archivable (effectively permanent) form; and the

physical size of the data. The detailed solution of these problems is beyond the scope of this work, however, the techniques which are likely to be used are described here for completeness.

All of these problems are now solvable, if perhaps at large expense. One of the primary solutions to the data-processing problem is the use of parallel computing and software architectures. In the simplest terms this means that more than one datum is processed at each instant during the data-reduction process. Improvements in semi-conductor-fabrication technologies are likely to lead to affordable massively parallel hardware in the near future. These systems will have direct application in the reduction of mosaic-detector data as well as in the data reduction for existing instrumentation which produces large data sets (TAURUS for example).

There exists no fixed standard for the archiving of astronomical data. The commonly used FITS standard[199][200] has limitations: it is primarily intended for the storage of image data and is not suitable for the storage of all astronomical data. The largest problem relating to archival is, however, that of the storage medium. The extensive use of magnetic tapes such as Exabyte 8mm video tape is being reviewed in the face of the large data sets from several contemporary instruments, let alone future mosaic instrumentation. Several technologies offer possible solutions; among these are optical disks, writable compact disks (CD-ROM) and WORM disks. Consideration needs to be made of what data should be archived—should the raw data all be stored?

Regardless of which storage medium or media are selected it seems likely that some form of *data compression* will be used to enhance the efficiency of the archival process. The two commonest types of data compression are Lempel-Ziv algorithm and run-length encoding. These methods would, for image data, best be applied to the actual bit planes in the data rather than to the data in a word-wise format. The reason for this is that not all the planes contain useful information. For example, typically the least significant two bits in an astronomical image might be noise, bits of increasing significance will have larger and larger structures, eventually the most significant bits may be either present or absent in the whole image—a high level of data redundancy.

The various methods of data reduction are interesting in that they might also be used in a mosaic instrument to reduce the bandwidth required in the data output path. Lempel-

Ziv and run-length encoding techniques can be implemented in hardware and thus be applied directly to data from the instruments' image-frame buffers.

Chapter 4

System Control Software

4.1 Introduction

A vital part of a mosaic-detector instrument is the control software. Generating programmes for the controllers and drivers is a complex task, especially for large numbers of detectors. The techniques used to meet the specification for the control software outlined in Chapter 3 are here described. The code which has been written is for the operation of a detector mosaic and data acquisition. Particular attention has been paid to code portability and reusability. The software will produce FITS (Flexible Image Transport System)[199][200] compatible data files. Simple statistical facilities for characterisation of detectors have been included. However, data analysis and processing are not considered to be primary goals for this project. Many extensive data-reduction and analysis packages already exist and are maintained to a high standard.

4.1.1 Scope of Software Control

The degree of software controllability of a mosaic-detector instrument is dependent upon the hardware architecture. In the system developed at UCL all of the electronic signals required to operate a mosaic are generated by digital-to-analogue converters (DACs). This naturally facilitates software control; all the DACs are directly addressable from the control programme. Software control gives enormous flexibility in the control and operation of a mosaic instrument at the expense of a requirement for careful software

design and testing. In a practical instrument the fully software-controlled mosaic is both more flexible and more reliable than any partially manually controlled system; in addition, a degree of human error can be removed by careful laboratory testing of the code.

To facilitate the operation of mosaics of arbitrary dimensions the control software includes a pseudo-compiler using a mosaic hardware description and waveform-definition language, which has a simple and logical structure.

To understand the design of the software and its methods of use, it is first necessary to refer to the hardware architecture and the modes of operation required of the mosaic-detector system.

4.2 Hardware Considerations for Software Control of A Mosaic

In this discussion the term *module* refers to a group of CCDs (or other detectors) driven by one controller and one driver. A module can contain any number of devices up to a hardware dependent limit—typically eight or sixteen devices. A mosaic may be composed of any number of modules. A mosaic-operation programme is composed of many parallel programmes, one for each module in the mosaic. Correct operation of each module can be verified independently of the others; this is a hardware characteristic. Once all the modules of a mosaic are functioning correctly, their programmes can be grouped together into a single mosaic-operation programme. The software is able to deal with modules composed of any number of devices until the host computer memory is used up; this would be in the order of hundreds of devices on even a small PC.

The architecture of the mosaic-detector system is such that component devices of a module can be read out independently one after the other, or in *phase-shifted parallel.* When operated in parallel the devices cannot produce synchronous output because only one signal can be digitised at any particular instant—hence the phase shifting. It should be noted that the system architecture limits the programmability of a module in only two ways:

- Only one *event* (a change of one of the control voltages at the detectors or logic

signals at the output processing array) is allowed at any particular time. Successive events must be separated by, at least, a hardware-dependent time; this the limiting resolution of control waveforms. In the prototype system this time is 200nS. (See Section 5.6.)

- Only one signal may be digitised at any particular time. The time separation of successive signal outputs must be at least the conversion time of the digitiser module *plus* the time taken to store the data produced.

The specification of the mosaic-detector system requires that the component devices of each module be operated in an integrating, full-frame mode. This method of operation has three stages:

- Device purge—removal of the residual signal charge due to previous exposure, thermal or cosmic-ray effects.
- Integration—maintenance of a set of static voltage levels at the device throughout an accurately timed exposure (the exposure time is the measured time of the shutter being open).
- Device readout—sequential movement of the signal charge stored in the device to the output node, amplification and digitisation of each pixel's signal.

The procedure would then be repeated for each subsequent exposure. Typically for a particular mosaic the first operation, *purging,* will always require identical bias-voltage and clock-signal sequencing regardless of the mode of operation of the *readout.* Integration times will obviously differ for varied subjects, but this is trivial to control and measure. The readout operation may be completely different for a set of applications of one mosaic, for example, partial readout of the mosaic (not all modules, perhaps only one device in the whole mosaic, or even a section of one device), pixel binning, different system gains (a different gain leads to a different dynamic range). The software is, therefore, designed to be able to cope with different operation modes of the mosaic, in the form of completely revised waveforms and bias voltages as required by those different modes.

To actually read out the mosaic requires two waveform sets for each detector in the mosaic: one to move a line of the signal from the image register into the readout register

of each device, one to move the readout register contents one pixel toward the readout node and amplifier of the device (purging is a special case of readout and is considered so from now on). These two waveform sets or *look-up tables* are hereafter referred to as the *vertical pixel* and *horizontal pixel* respectively. The horizontal pixel look-up table not only contains the clock signal information to shift the readout register, it also controls the sequencing of the readout amplifier clock(s) and the mosaic's analogue output processing (dual-slope integrators). Readout of a single device of format y lines of x pixels each is achieved by correct sequencing of the vertical and horizontal pixel operations as:

> "Repeat y times: one vertical pixel operation followed by x horizontal pixel operations."

The sequencing is done by the controller, the control software supplying the values of x and y.

To read out a module composed of devices of varied formats the programmer must use the largest values of x and y found in each module, hence, smaller devices are over-read producing redundant data. No data are lost, however. Figure 4.1 shows this for three devices, of sizes 30×50, 40×40 and 60×20 pixels. The largest x value is 60 pixels, and the largest y, 50 lines. The over-reading of the second detector by 10 lines and by 20 pixels is also shown.

The architecture of the mosaic-detector hardware is such that the DACs of each driver are addressed in the same way by their controller, regardless of whether they are bias voltages, vertical-pixel clocks or horizontal-pixel clocks. For this reason, there is no need to distinguish between the waveform look-up tables when they are under preparation; only when they are grouped into a module programme are they identified as the vertical-pixel and horizontal-pixel look-up tables. The requirements then for a particular operation mode are:

- Number of vertical pixels (y).
- Number of horizontal pixels (x).
- One vertical-pixel look-up table.
- One horizontal-pixel look-up table.

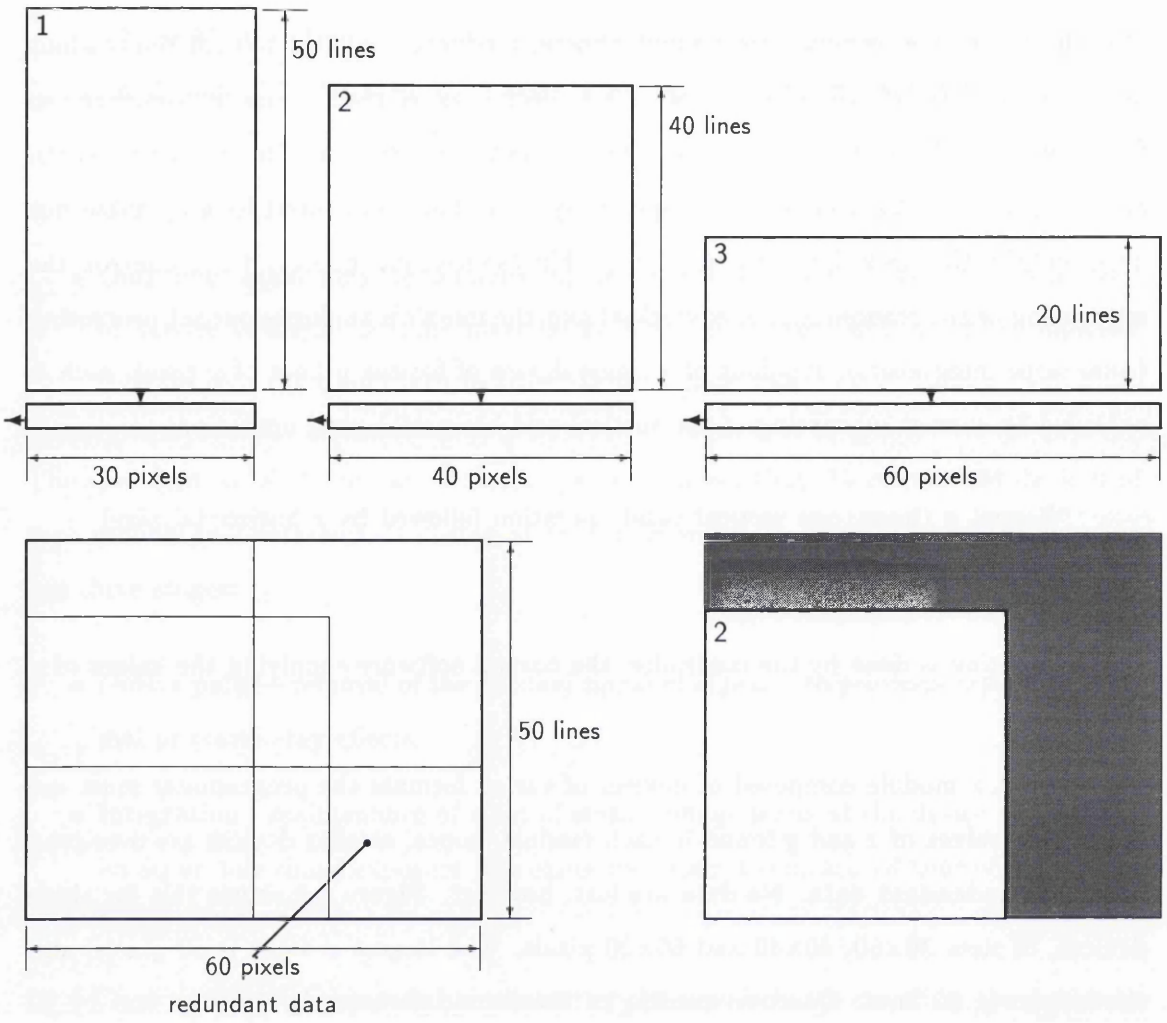

Figure 4.1: Over-reading of small detectors in a mosaic.

- One bias-voltage look-up table.

These five items are required for *each* module in the mosaic and there may be distinct differences between the modules and hence, between their programmes.

The software is able to programme into the look-up tables the correct phase information so that each detector in a module is operated in an optimum manner. It is possible to refer (in the software) to individual devices of the mosaic without affecting the operation of the other devices. To achieve this, each voltage source at the drivers is individually addressable.

In summary: the software is able both to group information (devices into modules, modules into a mosaic) and to refer to the components of the groups without affecting

the integrity of the readout programme.

4.3 Overview of Hardware and Operation Mode Definition

The mosaic-detector-control software is called `DMAP`—a contraction of *data map.* `DMAP` is designed to generate the look-up tables required and to group them into module operation programmes. These programmes can then be logically linked into mosaic-operation programmes. The whole problem is given an *hierarchical* structure, allowing the user to work at module, device and mosaic levels of the system as required. `DMAP` operates at the module level by default; optimised programmes for operation of each module can then be compiled for subsequent grouping into a mosaic programme.

4.3.1 Hardware Description

`DMAP` contains an internal representation of the system hardware for which programmes are being written. This hardware description can be freely edited—for example, when the specification of a driver changes. The description follows a tree structure, similar to the directory structure of many operating systems. A user would first define the component detectors of the module. Subsequently, the analogue circuitry required to drive these detectors is declared, with logical links being made between devices and the buffers which supply the signals required. The buffers reside one level below the devices in the hierarchical representation of the hardware. This means that a particular signal (for example, the reset pulse of a particular device, here called `CCD1`) would be referred to with a name similar to `CCD1.RESET`. The actual hardware producing this signal—a DAC with op-amp buffered output—will, of course, have a limited range of output voltage. A table of the voltage sources available from the driver is maintained by `DMAP`. Each voltage source is described by three parameters: a timing delay, an intercept and a slope. These represent the real-time difference between an event in controller memory and at the focal plane assembly, the output for zero digital-number assignment and the output voltage change for one digital-number change in the value sent to the DAC respectively. As the data sent to a DAC is eight-bit, the software is able to check any voltage assignment made to ensure that it can be produced by that buffer. It is assumed that the DAC response has a linear volts per digital-number character. If the user attempts to assign a

value to the buffer output voltage which is out of the eight-bit range as determined from the parametric description of that buffer, the software responds with an error signal and does not make the assignment.

The user is able to define voltage levels or states for a buffer and symbolise them with a name. For example `CCD1.RESET.HI` might be assigned the value ten volts. Voltage symbols reside one level below the buffers in the hierarchical representation of the hardware. By this means, the user builds up a set of symbols which stand for particular states of the various clock signals required by the detectors. Once the programme has a complete description of the component devices of the module and of the driver's buffers, logical links can be made between the two. It should be noted that the definition of the system hardware and voltage states will maintain its integrity for any change. For example, if an attempt is made to change the definition of a buffer for which any voltage states are assigned, the command will only be accepted if all those voltage states can be produced by a buffer which has the new characteristics. Consider the following example which illustrates these points: a buffer, `CCD1.RESET`, has been declared to have intercept 0 volts and slope 0.1 volts per digital number. This buffer can therefore produce output in the range 0 volts to +25.5 volts as it is based around an eight-bit DAC. If a voltage symbol `CCD1.RESET.HI` is assigned the value 15 volts it will be accepted. An attempt to modify the buffer declaration so that the slope of the buffer profile is 0.05 volts per digital number will fail as the maximum voltage output from such a buffer is only +12.25 volts and this is inconsistent with the existing definition of `CCD1.RESET.HI`. Similarly, an attempt to set up a voltage symbol `CCD1.RESET.LO` of value −3 volts would fail as this is beyond the current buffer definition's possible voltage output range.

Control signals for the mosaic output processing array are treated in a similar fashion to the voltages required by the detectors. Each bit required by a detector can be assigned a name; for example `CCD1.RESET_INT`.

4.3.2 Creating Module Level Programmes

As described in the previous section, each voltage or signal required at the detector mosaic is assigned a name or *symbol.*

DMAP allows the user to group symbols into look-up tables. The software treats bias-voltage look-up tables differently to waveform look-up tables. A bias-voltage look-up table *must* contain a symbol for every declared voltage buffer—the programme for a module will not compile if its bias-voltage look-up table is incomplete. This prevents the user from failing to define the initial state of all of the signals required by the module. Waveform look-up tables need not contain any symbols—usually, however, each waveform look-up table will define either a vertical- or a horizontal-pixel operation.

The procedure for creating a waveform look-up table is as follows:

1. Declare the waveform look-up table; this involves giving it a name and allocating it a length in microseconds.

2. Set *events* in the table at appropriate points—each event being represented by a voltage symbol, logic-data symbol, or logic-state symbol.

3. repeat 2. until a complete sequence is set up.

4. Move events to optimise the performance of the system, changing the voltages represented by symbols if needed.

The size of the waveform look-up table is its repeat period. For example, if a readout rate from a single device of 10kHz is required, this corresponds to a period of 100μS; a horizontal-pixel look-up table of size 100μS would thus be required. The *events* are simply the voltages symbolised by the user (*e.g.*, `CCD1.RESET.HI`). When an event is set it is declared that that voltage is to be set up at that time during the execution of the waveform look-up table content. For example, if `CCD1.RESET.HI` is ten volts and is set at 10μS from the start of the look-up table, then the reset clock of the device `CCD1` will be biased to ten volts 10μS after the start of each horizontal-pixel operation. By placing the voltage symbols in the appropriate time sequence the device-readout waveform can be built up. Because the voltages are referred to by *name*, not value, it is simple to change the clock voltages whilst retaining the same timing sequence.

Each device can be addressed uniquely; this means that the waveform look-up tables needed to operate a device can be created without having to view the mass of events for all the devices of a module. It should be noted that only one event can be placed in each

memory location of the controller memory—DMAP ensures that this is the case by refusing to overwrite existing events in a look-up table; rather, they must be explicitly unset if that time slice is to be re-allocated. The user may even work with the look-up table at the level of a single buffer—viewing only those events for one clock of one device.

In a similar manner to the voltage change events, logic bits required by the output processing array can be set or unset at the appropriate points in a waveform look-up table. Logic states are referred to by name, for example `CCD1.RESET_INT.ON`.

4.3.2.1 Error Checking

When a module programme is complete it can be compiled. Before compilation, the programme is checked for any events or voltage assignments which might contravene the voltage limiting rules declared with the devices' buffer requirements.

When the buffers for a device are declared, limiting rules for the voltages at those buffers are required. The module-programme compiler simulates running of the module through one vertical-, two horizontal- and one further vertical-pixel operations, which is sufficient to cover all changes of state at the detectors. During the simulation the voltages at all of the buffers are cross referenced to ensure that their relative values will not exceed the conditions declared. Absolute value checking is possible (*i.e.* relative to the local ground level rather than to another source for the device itself). Normally the voltages at the buffers of a device would be cross checked against either the substrate voltage or another buffer voltage. The substrate voltage is then 'absolute value' checked, for completeness—in fact only the *relative* voltages of the pins of each device can affect damage to the device.

In summary: the programmer has a high degree of flexibility in programming method and in the way module-level programmes are viewed and developed.

4.3.3 Grouping of Module Level Programmes into Mosaic Programmes

Once each detector in a module has been optimised, the waveform look-up tables for that programme can be compiled into a single file. Each operation mode will thus consist of a text file—and the code for the look-up tables in the DMAP language and a binary file—

the actual data which would be down-loaded to the appropriate module. At the mosaic level, programmes consist of a set of pointers to the compiled module programmes. If a module does not have a programme attached to it in a particular mosaic programme it will simply not be operated. It is preferable to maintain mosaic-level programmes in this semi-compiled form to minimise the down-load time. For mosaics of more than a few CCDs the quantity of data required to define the look-up tables will be large and should be available in the rawest form possible, *i.e.* compiled. More than one mosaic-level programme may make use of a single module-level programme if necessary.

The module-level programme code need not be kept on the LIM once the programme has been optimised. It is, however, needed to update the compiled module-level programmes as there is no decompiler available.

4.3.4 Programmes and Files

`DMAP` has the ability to read commands from text files or from the terminal. The user can use any text editor available on the host computer to create the programme files. The commands entered by the user can also be written out to a file from `DMAP`, which gives the user a record of the status of interactive programming. The user can edit this log file and read it back with enhancements so made. For the purposes of clarity, module-level programmes are composed of files in a manner which echoes the hierarchical structure of the programme; one file for the buffers driving each detector, and one file for each waveform look-up table. A module programme file thus consists of calls to other files as required, plus the 'glue' code to complete a module-operation programme.

4.4 Operating the System and Data Acquisition

In practical use the control software (`DMAP` or otherwise) is embedded in an extensive user environment. Except during testing, the user hardly ever needs to access the CCD control system beyond simply down-loading binary data to the system hardware.

In the laboratory system, several batch or command-procedure files are available which set up the system hardware for testing and experimentation.

Data acquisition and analysis are system dependent; for example, on the laboratory

PC-based system a suite of statistical-analysis and image-display programmes has been written. It is intended that available data-acquisition systems on other hardware platforms should be used in preference to porting this package to such systems.

4.5 Mosaic Control Programme DMAP

4.5.1 Introduction to DMAP

As previously mentioned DMAP is short for 'data map', a reference to the nature of the information stored in the memory of the controllers of the mosaic-detector system. DMAP is a *pseudo-compiler,* meaning that it builds a representation of the mosaic system in memory, only converting (*i.e.* compiling) when the data is either sent to the system or if the user requests that the information be archived in compiled form.

For instruments with more than one module it is necessary to maintain programmes in compiled form. This is for two reasons: first the compilation procedure takes about a second for a complex DMAP programme; secondly the down-loading time for even a single-module programme is also about one second. To minimise the combined effect of these features, the compilation can be done before the instrument is in use, thus reducing the set-up time. Down-load time can only be reduced by improving the hardware.

DMAP recognises files of two types. The first consists of instructions regarding either the hardware configuration of the system or the operation mode required of the system. The second file type is the compiled DMAP programme, which is stored in a binary format. The text files can be ported from one machine to another, but, the programme files may not be portable, depending on the underlying architecture of the host machine.

4.5.2 Portability and Porting of the Code

The C programming language[102] is used for all the proprietary software of the Mosaic-Detector Project. C compilers are available for most computer hardware, and quickly become available for new processors when they appear on the market. The American National Standards Institute has ratified a standard version of C which should be a subset of the language implemented by any particular compiler. Because of the extensive use of ANSI C[103], and the ease of use of the language for hardware control, it is an ideal

vehicle for the source code of mosaic control software. Use of a standardised language does not in itself ensure that the software has maximum portability; careful structuring of the code is also required.

The software is written to the ANSI standard as far as possible. The code also adheres to the STARLINK C programming standard[133][184]. Machine- and compiler-dependent parts of the code are grouped together into either a pre-processor #include'd file (an *header*) or a separate object file. An example of this is the non-ANSI date and time functions of the PDOS C compiler[141]. Code to mimic the standard date and time functions is compiled into a machine-specific object file, making the portable section of the code link correctly without any change. The hardware description, *i.e.* the system-rack address-map, is included in the header file `dmapspec`, as this is very much machine-dependent.

In practice it has proven to be a simple task to port the code originally developed on the VME system to compile in Digital UNIX (DU), MS-DOS and VMS operating-system environments. The VMS and DU versions of the programme are not interfaced to hardware (part of machine specifics), the port being undertaken with the intention of checking code portability. The user-interface and file-access parts of the software are available so that `DMAP` mosaic control programmes can be developed and checked on these computers.

Despite the supposedly standard nature of ANSI C, several changes to the portable part of the code were made in the light of problems uncovered when compiling on different hardware. The modifications take the form of changes to the code, but maintain the use of the ANSI standard. The most significant problem found was that when using the Microsoft C5.0 compiler the amount of memory which may be used for global variables is limited to 64kbytes. The problem arises for historical reasons, the architecture of the MS-DOS operating system being based on the original 8086 processor. Several large arrays which have to be of global scope, *i.e.* visible to all functions in the programme, are used. The code has been modified so that data compression is used, reducing the amount of memory allocated to global variables. The modification reduces memory usage by 40%—a benefit on any hardware. Even with the modifications made to reduce the extent of global variables, under MS-DOS several of the arrays have to be reduced in size to fit the 64kbyte limit.

4.5.3 DMAP User Interface

Ideally, a graphical user interface (GUI) would be available as part of the mosaic-detector-control software. To achieve the high portability specification of the code, this would require either that the GUI be written in-house using ANSI C, or that a similar standard format or language for GUI be adopted. At the time of writing no such standard exists. The X-Windows[67][158] GUI is not easily implemented on small computers, and no other GUI is even remotely a 'standard'. In the future it may be useful to produce an X-Windows version of DMAP, but this represents a significant amount of effort and as such is a secondary objective for the system software. The C language does not contain any constructs for graphics programming. Even for the simplest action of plotting points on the display, a machine-specific function must be written. For this reason, and the lack of any portable standard, no GUI is included in the code.

The interface used is a normal 'line input' interpretive one. The user types commands to which the programme responds. DMAP is not case sensitive, all commands being converted to upper case before parsing, except strings enclosed within pairs of double quotation marks '"'. The set of commands available has been kept as small as possible without loss of flexibility. The command-line interpreter is able to accept multiple commands on a single line, each separated by a semicolon ';'. There is a degree of programmability in the user interface. A command (DEFINE) may be used to substitute a shorthand or familiar string (a *macro*) for a single command or series of commands. The macro can accept parameters. Using this feature it is a simple exercise to make the user interface appear similar to other detector-operation software. Commands can be passed directly to the host-computer operating system so that file management need not be part of the C code; rather, it is written in the language of the control software to mimic the user's preferred operating system.

Different applications for mosaic detectors will require different user interfaces. For example: one for mosaic and detector characterisation tests, and another for actual operation of the mosaic by the end user. By making programmability a feature of the control-software user interface it is possible to tailor the command set to suit each application. When the control software is invoked a base file may be loaded which can include any command that might be entered interactively. The base file is intended to contain the custom def-

initions required for the particular application. This technique is similar to the format and base files used by the TEX[107] and METAFONT[106] typesetting programmes—when different format files are used; the language understood by the programme changes.

If a programmable graphics environment is available on any host computer, it is possible to set up a GUI front end for the system. Information can then be piped between the command-line interpreter and the user in a seamless design, for example a version of DMAP has been linked which runs under Microsoft Windows.

4.5.4 DMAP Source Code

The source code of the mosaic-detector-control software is contained in about fifty files. All of the files are quite small, their sizes ranging from about fifty lines to two thousand lines. Any parts of the ANSI-standard C libraries not available on the host machine which are required by the software are coded in a separate file and linked into the executable. For example, on the OSL PDOS system no equivalent of the ANSI-standard library time functions was available. Look-alike functions were coded and linked with the rest of DMAP. By splitting the code into many small files, each DMAP object or action is clearly delineated. This makes maintenance and improvement of the code quick and easy. The DU and MS-DOS versions of DMAP include a 'make' file to build and maintain the executable. The VMS version is maintained by a code-description file and the VMS Module Management System (MMS) which is functionally similar to 'make'. The PDOS version is maintained by command-procedure files.

DMAP hardware dependencies are gathered into the file `dmapspec.h`, this file is adjusted for each implementation.

4.5.5 DMAP Command Language

DMAP has a fairly complex command set to give the user maximum flexibility. Operating system commands can be accessed. Complex or repeated sets of commands can be stored in procedure files (or *scripts*) and then accessed like any other command. Similarly, command macros (or *aliases*) can be defined.

Appendix B gives a summary of the DMAP command set. Appendix C contains a real

example of the code in use.

4.6 Laboratory Versions of DMAP

DMAP exists in two laboratory versions. The first of these is version 0.85, running on the old 68000-based VME system. The second is the up-to-date version 0.95, running on the laboratory IBM PC and under the DU and VAX/VMS operating systems. The actual syntax of the two versions is entirely different, reflecting the faster development cycle on the PC. The VME-based software is now out of date with respect to the general development of DMAP, but will not be upgraded for reasons discussed in Section 4.7.

4.6.1 Operating Systems

As part of the functional testing and development programme for DMAP, the code has been ported to several operating systems. Originally, the programme ran on the laboratory 68000-based microcomputer under the PDOS operating system. To test the code portability, a port to VAX/VMS was undertaken, leading to a rationalisation of system dependencies within the code.

When the second SERC grant for CCD development became available an IBM PC clone was purchased, representing a considerable improvement in computing power over the 68000. DMAP was ported to the new operating system (MS-DOS) and further developments of the system were undertaken in this environment.

When the local STARLINK node acquired a UNIX workstation (DECstation 5000) DMAP was ported to the new environment as a further test of the code.

4.6.1.1 PDOS Real-Time Operating System[140]

PDOS is a real-time, multi-tasking operating system developed by the Eyring Research Institute for the Motorola 68000 family of microprocessors. The version in use on the laboratory VME system is PDOS 2.6. The user interface consists of a command-line interpreter and a set of about forty two-letter commands. Unlike most operating systems, the directory structure of PDOS 2.6 is not hierarchically arranged; rather, the directory boundaries are 'soft', *i.e.* one may access files in other directories which reside at the same

level. In use the system exhibits a susceptibility to VME bus errors, *i.e.* the operating system would crash or lose its memory-allocation table, leading to an inevitable reboot.

4.6.2 Handling of Mosaic Data in the Laboratory System

As explained in Chapter 3, the data produced by the digitisers are intended to be stored initially in a local frame-buffer memory. The data can then be transferred to a data-processing computer for reduction, analysis, and archiving. The transfer of data can take place at any time when data are not being written to the memory. By default, `DMAP` does not contain any constructs for handling the data produced by a mosaic instrument.

In the laboratory prototype there is no local frame-buffer memory, the data being stored directly in the LIM memory. FITS-compatible data files can be produced. The code for writing out the FITS files was originally ported from the CCD-IPCS IDRIS software (written by R. N. Hook) and used in the UCL SAAO CCD[191] laboratory data acquisition system. The host for that system was the same VME-based 68000 machine now in use as the one of the Mosaic CCD system LIM. The data acquisition sub-system on the VME system is a short 68000 assembly language routine. The routine strobes the hardware status and reads data when an end-of-conversion (EOC) pulse from the digitiser is detected.

The IBM-PC based data-acquisition system uses a Lotus-Intel-Microsoft Expanded Memory Manager Standard[80] compliant device driver to access extra on-board memory. The data-acquisition sub-system functions in a manner analogous to the VME system and is written in 80386 assembly language. Data are paged into the expanded memory. This system can acquire up to 32Mb of data (at the time of writing only 4Mb of memory are fitted in the PC LIM.)

Simple stand-alone utilities for the manipulation of image data have been coded. These include utilities for selecting regions of images for statistical analysis and the calibration of the system (see Chapter 6). These utilities are seamlessly incorporated into the `DMAP` environment using the standard `DMAP` command `SPAWN` (see Appendix B).

4.6.3 Image Displays and Image Display Software

Three image displays have been used for data obtained with the mosaic CCD. These are: an IO Research PLUTO graphics engine; a Transtech Harlequin Transputer graphics card for a PC and standard PC video graphics array (VGA) display.

Most of the routines for image display and manipulation on the PLUTO engine (interfaced to the VME 68000 system, see Section 5.3.1) were written by R. Hook, D. Bone and C. Hirst for previous projects. The existing code has been updated and incorporated into the new project. Typically, these routines allow manipulation of the image display and colour look-up table as well as line-graph and axes drawing.

As part of the port of the existing software to an IBM PC platform the graphics display software was modified and upgraded to support both the PC standard VGA display and the Transputer graphics card. New features were added including image binning in software, display of floating-point data sets, image masking, multiple image display, regional pan and zoom. This hardware configuration uses the Lotus-Intel-Microsoft Expanded Memory Specification[80] for data storage and thus required almost complete revision. The Inmos Transputer Development System was used to modify the source code (Inmos B007 graphics utilities) for high-speed communication between between the host PC and the Transputer board. For example, using the supplied programme a single line of a CCD image of 220 pixels (440 pixels binned factor 2) would require a total of 6160 bytes to pass between the PC and the graphics board. Using the new routine the same line can be displayed with only 240 bytes passing between the two systems. A typical image is scaled and displayed in about six seconds.

4.6.4 Other Software

The control software for one of the OSL prototype controllers was written by W. Han[73]. The code was written in Microsoft QuickBASIC. Simple functions such as detector purge and readout are supported. Interactive modification of the readout mode of the detector mosaic is not possible, requiring a re-compilation of the software. `DMAP_0.95` supports programming of this controller and thus the BASIC software was not required by the author for laboratory experiments.

Several simple communications test programmes were produced for debugging the interfaces to the CCD control rack. A simple programme for calibrating the buffered DACs of the Driver module (see Section 5.7.3) was also written and used for system analysis.

4.7 Debugging and testing of Software

Many problems arose during the development of the mosaic-detector-control software. The single largest problem was the archaic nature of the PDOS operating system and the C compiler available on the 68000 system. The final PDOS version of `DMAP` (0.85) takes some two hours for a complete compilation and link cycle on the 68000 system. Such a development cycle time is unacceptably large, especially during debugging. For comparison, the more extensive `DMAP_0.95` code can be compiled and linked under MS-DOS in about six minutes. Unfortunately, the compilation time under the PDOS C compiler has not been the only problem during programme development. Several errors in the source code for the Standard C library have been located and had to be circumvented.

Once an MS-DOS operating system IBM PC was acquired for the project all software development was moved this platform. It soon became apparent that porting of code from the PC to the VME system was highly inefficient, hence the VME-based system has not been significantly upgraded beyond the simplest system-control, data-acquisition and image-display package needed for system-noise and cross-talk evaluation.

The more recent versions of the software (*i.e.* those coded and debugged under MS-DOS) have had significant design improvements. The STARLINK-standard use of inherited status on function call has been adopted. The `DMAP` command language has been made more robust and virtually all user input is dealt with in a logical fashion. The internal variables of the software have been moved into a single object-orientated structure, removing almost all global variables. Functions dealing with each class of object have been grouped into a single file thus achieving a degree of encapsulation.

The `DMAP` compiler has been tested by down-loading the resulting code to the mosaic system hardware and checking the resulting waveforms with a logic analyser. The binary data have also been hand checked.

4.8 Future Developments

The current version of DMAP has sufficient capabilities to support the development of the next generation of mosaic-detector controllers and the operation of multiple controllers. The system does not therefore, require significant improvement from the hardware point of view. The user interface for the software could be upgraded to a GUI and/or menu-based system, but this is not currently part of the project schedule. Support of simple control flow statements and user calculations is the next requirement for the system. Such capabilities will allow the user to perform automated calibration and optimisation of detectors in a mosaic instrument. These abilities, combined with an enhanced command-macro definition facility and the ability to use command procedures/scripts which accept parameters will make the DMAP compiler into an operating system for detector control systems.

Chapter 5

Prototype Hardware & Functional Testing

5.1 Introduction

In this Chapter the electronics built to demonstrate and evaluate the mosaic concepts from earlier chapters are described. The laboratory equipment, computer hardware and general technical specifications are given. Tests made to prove the functionality and to characterise the prototypes are described, with results.

5.1.1 Overview of Laboratory System

Laboratory testing of the mosaic-detector system hardware has been done in several modes, reflecting the different detector drive architectures being evaluated.

Figure 5.1 shows the configuration of the system when both data acquisition and hardware control are via a single custom-built interface. For simplicity, the schematic shows only one CCD detector.

The system consists of three primary sections: the local microcomputer, in this case a 68000-based VME computer; the system electronics rack; and the cryogenic enclosure for the camera head. The LIM is connected to the system rack by a 32-way twisted pair cable. The signals passing through the cable are opto-isolated so that there is no electrical connection between the two racks. The LIM runs the mosaic control and data-aquisition

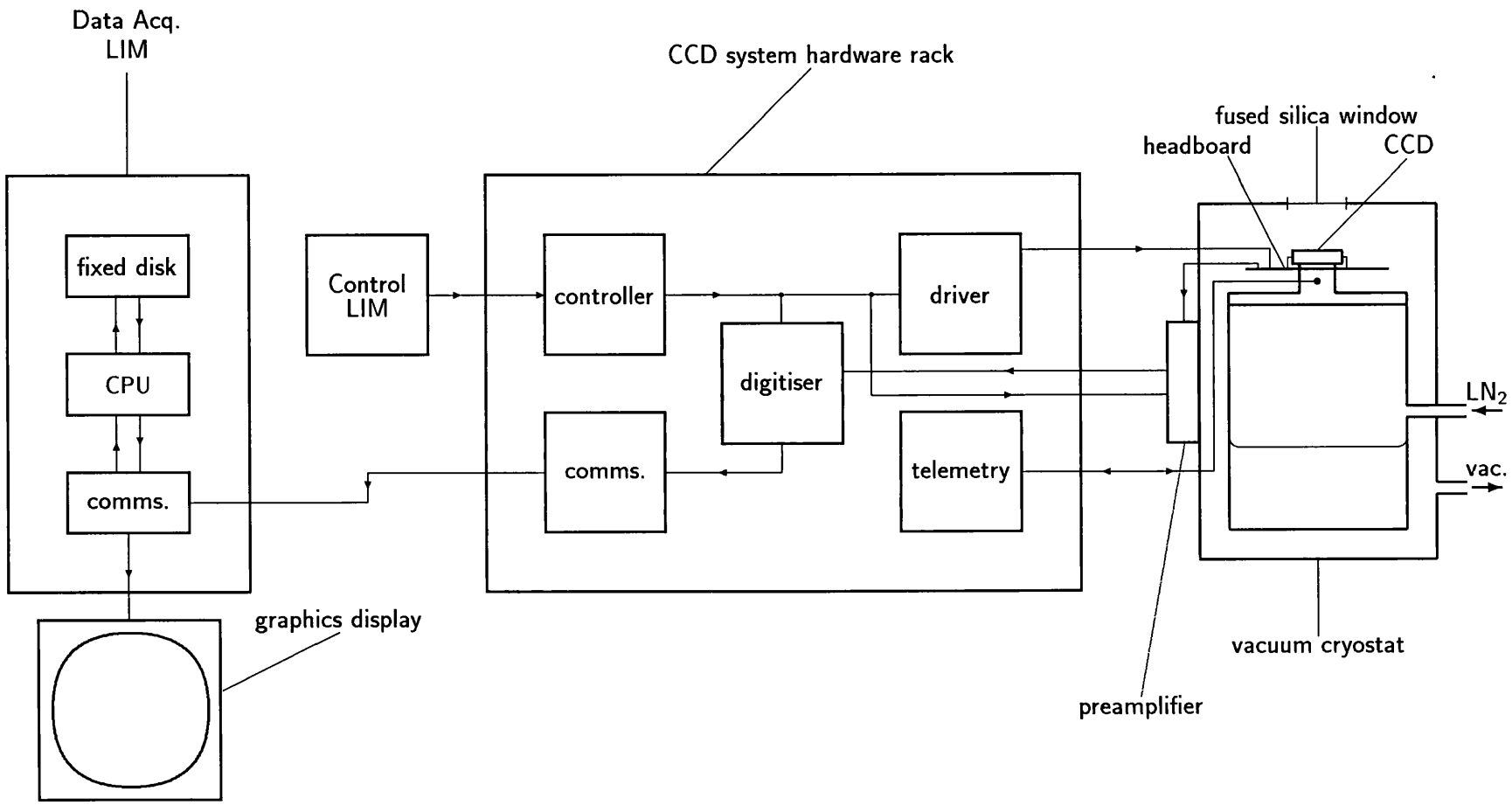

Figure 5.1: Laboratory mosaic detector system.

programme DMAP_ 0.85. There are five boards in the electronics crate. The link to the LIM is controlled by the communications card which also generates the system reset on power-up. DMAP communicates with the single controller module in the rack. A driver module sufficiently populated to drive up to four CCDs is programmed by the controller. The analogue signal from the detectors is processed by the digitiser connected to the rack backplane; thus making the image data available to the LIM. The detector assembly is positioned at the front of the cryostat, close to the fused silica window. The detectors are cooled by liquid nitrogen via a 'cold finger'. The headboard carries filter capacitors for the detector bias levels[1]. A signal diode and resistor are embedded in the cold finger to enable monitoring of the temperature of the detectors and stabilisation of that temperature.

Figure 5.2 shows the configuration of the system when the hardware is controlled via one interface whilst the data acquisition is made via a second interface. In this mode, the controller and driver are changed, the alternative boards representing a different CCD control technique. The controller is no longer accessed via the communications card; instead, it is directly interfaced to the PC LIM. The system is essentially similar to the single-interface system excepting that the PC runs a simple bitmap-generation and system-control programme written in BASIC (see Section 4.6.4).

In the third mode of operation, which is functionally the same as the first, both hardware control and data acquisition are carried out from a single IBM PC clone (see Section 5.3.2). The connection between the CCD rack and the computer is through a 50-way ribbon connector. Opto-isolators are used on the communications card at the CCD rack to electrically isolate the system from the computer. In this case the LIM runs DMAP_0.95, which is a considerably more advanced and flexible version of the control software than that available on the 68000 system.

Figure 5.3 shows the main part of the electronics of the mosaic-detector system prototype and test-bed.

[1] An earlier headboard carried constant-current sources for the four detectors' output signals, no longer needed with the contemporary preamplifier.

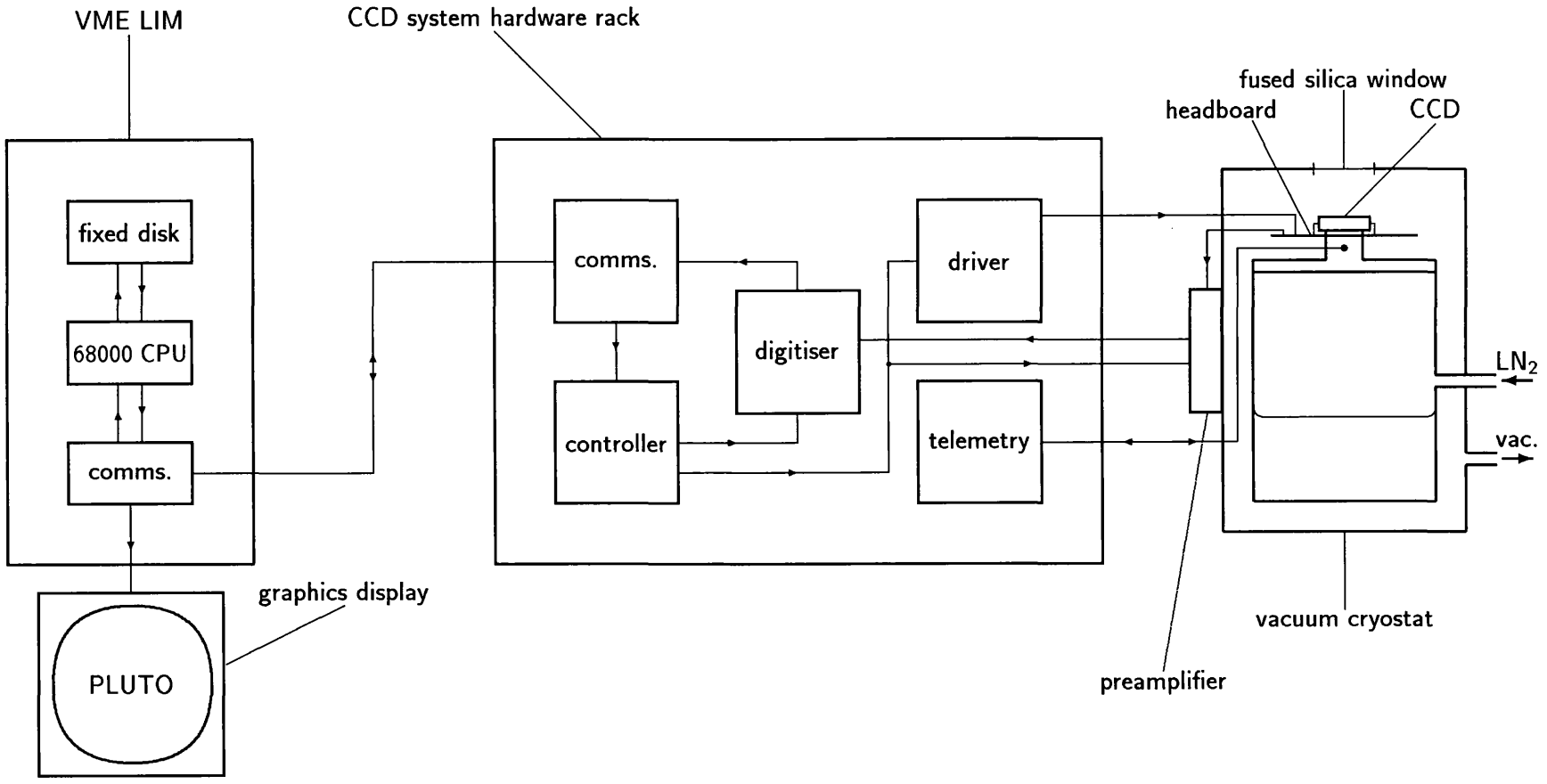

Figure 5.2: Laboratory mosaic detector system—split interface.

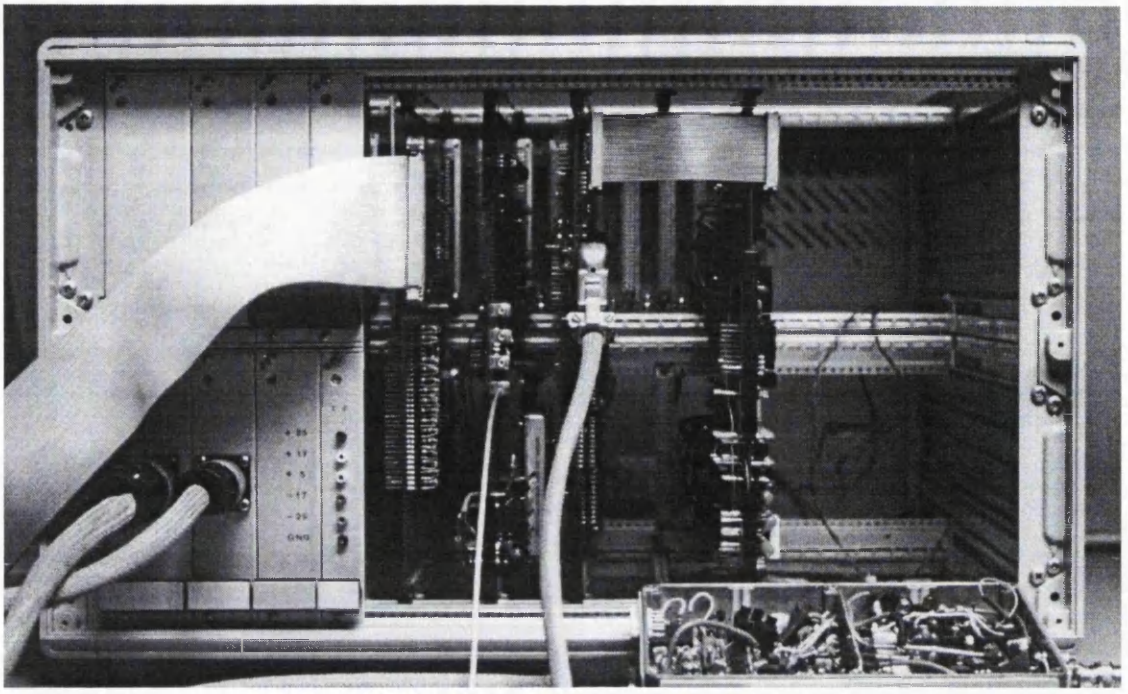

Figure 5.3: Prototype electronics rack.

5.2 Detectors Used During System Development

Three CCDs have been used during the development of mosaic detector instrument hardware. Two of the detectors are based on the successful P8600 CCD manufactured by EEV Ltd. of Chelmsford, England. The third detector forms an integral part of the project, and is a special reduced package-size version of the EEV P88300 CCD. The P88300UC is 78.7% imaging area as opposed to the 36.8% of the standard P88300. These three CCDs are shown in Figure 5.4 with a standard P88300 for comparison.

5.2.1 P86235

A schematic of an EEV P86000 series CCD is shown in Figure 5.5, EEV have produced many variants on this basic structure. The P86235 is designed for frame-transfer operation, principally in black-and-white 625-line video cameras. Six of these devices were supplied by EEV, with performance test results including cosmetic-defect details. This information can be found in Table 5.1. The P86235 provides an imaging area of 8.5mm×12.6mm when operated in full-frame mode. This consists of 385×578 22μm-

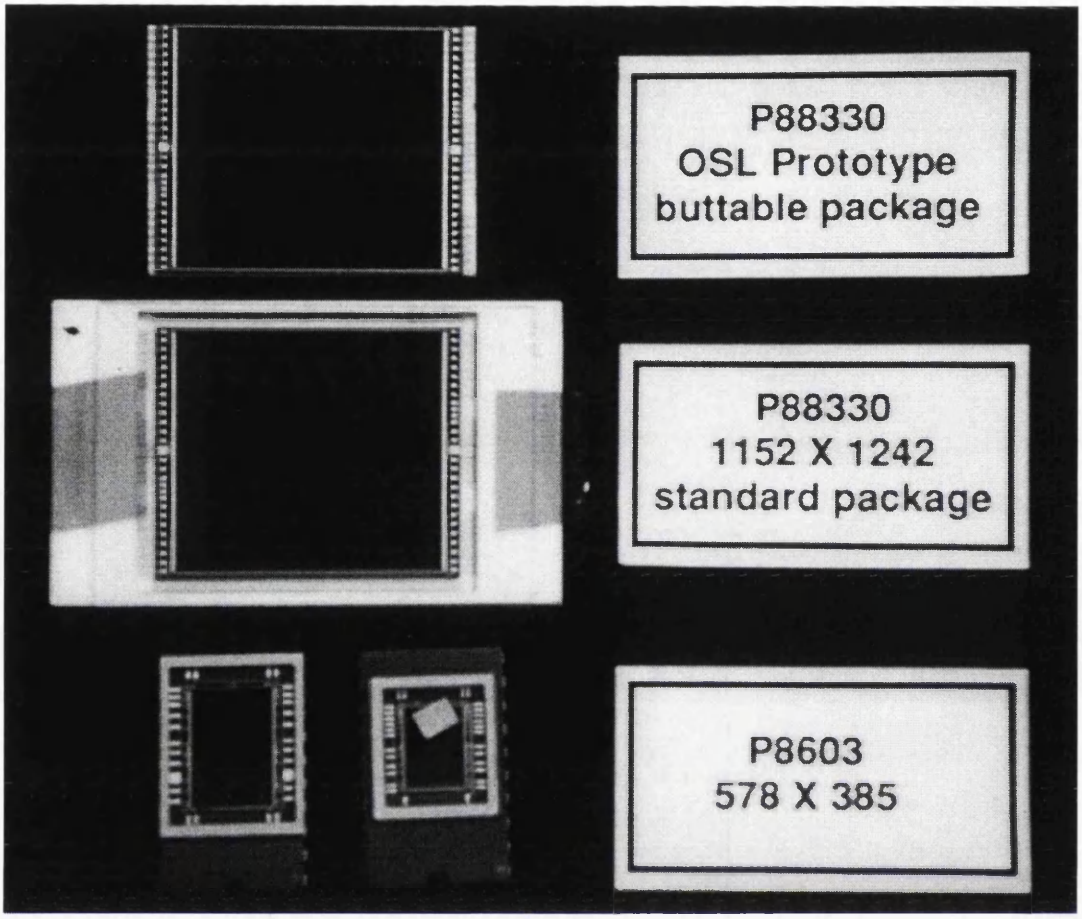

Figure 5.4: CCDs used in laboratory experiments. Top is the P88300UC, middle the standard P88300, bottom two P8600 series CCDs.

square pixels. The principal purpose of these devices was to test the functionality of the system drive electronics and to look for cross-talk between devices. Their operating requirements are generally similar to the P88300.

5.2.2 P86420

A single device of this type was supplied by EEV. This was a functional reject device specifically for testing drive electronics. The P86420 is pin compatible with the P86235 and is ideal for such testing. Despite its reject nature this device was used to obtain the first image from the mosaic CCD system, the rather noisy Figure 5.6.

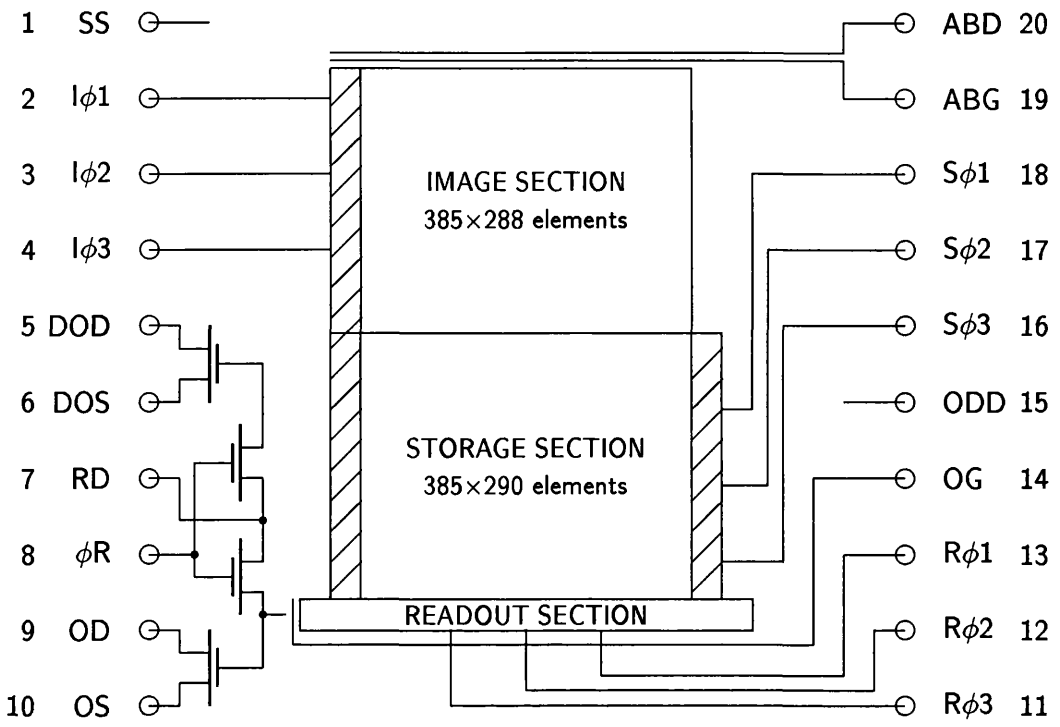

Figure 5.5: P86000 series EEV CCD schematic. [27]

Serial No.	Noise/e^-_{rms}	O/P Capacitance/pF	O/P Voltage Gain
8432-09-35	6.2±0.32	0.108±0.006	0.65
8432-09-37	6.3±0.28	0.109±0.005	0.65
9112-08-09	7.0±0.38	0.140±0.006	0.65
9112-08-33	6.5±0.31	0.826±0.040	0.65
9112-08-42	6.9±0.37	0.104±0.006	0.75
9112-08-44	6.9±0.36	0.104±0.005	0.75

Table 5.1: EEV Test data for P86235 CCDs used in the laboratory.

5.2.3 P88300UC

This CCD consists of 1242×1152 imaging pixels, each 22.5μm square, giving a total area of 28mm×26mm. The device is of the 1024-pixel-square class described in Section 2.2.3.2. The device was fabricated using EEV's CCD05 mask set. In collaboration with EEV, a special package for the CCD05 has been developed. Special-packaged and standard-

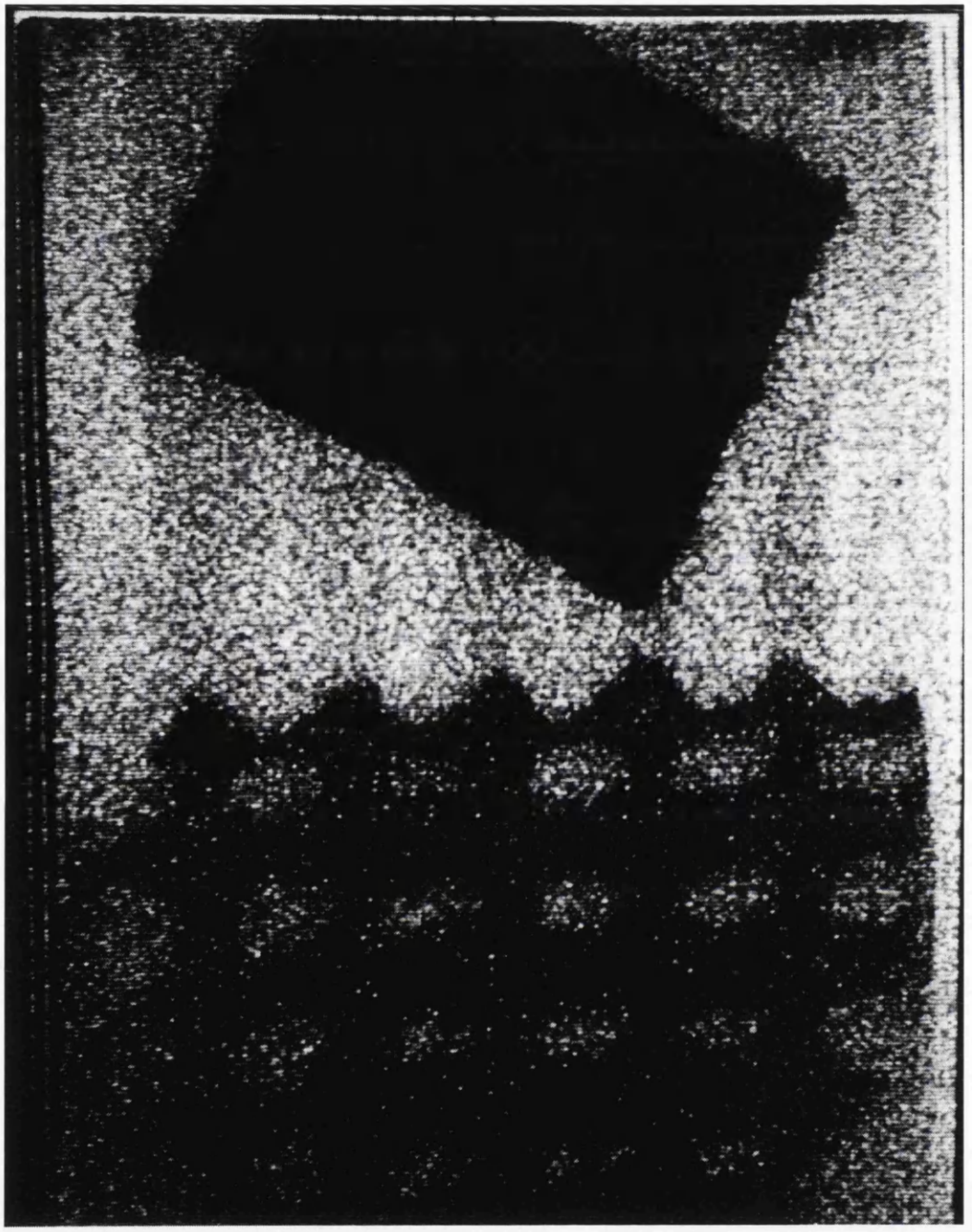

Figure 5.6: The first image obtained with the system.

packaged P88300-type CCD are shown in Figure 5.4. As mentioned earlier, the special package has a much higher filling factor than the standard device. The special package also has a much reduced pin count, as multiple connections to the image section are made internally to the package and only one of the four available readout amplifiers is connected to the pins. Schematics of the P88300UC and of the standard device are

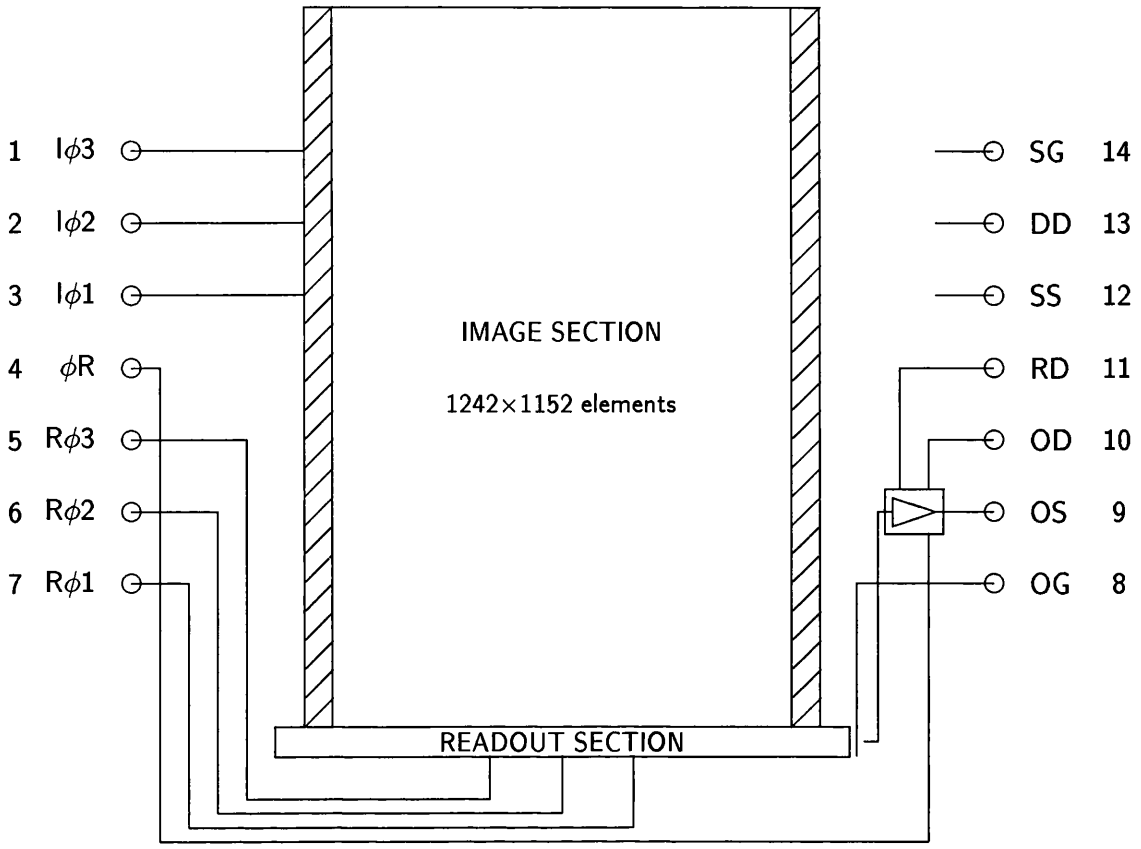

Figure 5.7: P88300UC EEV CCD schematic.

shown in Figures 5.7 and 5.8 respectively. The decrease in connection complexity is quite important from the point of view of the design of intra-cryostat electronics. The P88300UC has a special transport jig for handling of the device. A device held in the transport jig is shown in Figure 5.9.

5.3 Instrument Control Computer

As mentioned in Section 5.1.1, the mosaic-detector system can be operated in three modes, reflecting the different architectures under evaluation. The primary subject of this work is the first and third modes of operation. The second mode is described in detail elsewhere[73]. It should be noted that the `DMAP` mosaic-control software is ported to both MS-DOS and PDOS operating systems and thus both systems appear the same to the user (except for newer features of `DMAP_0.95`).

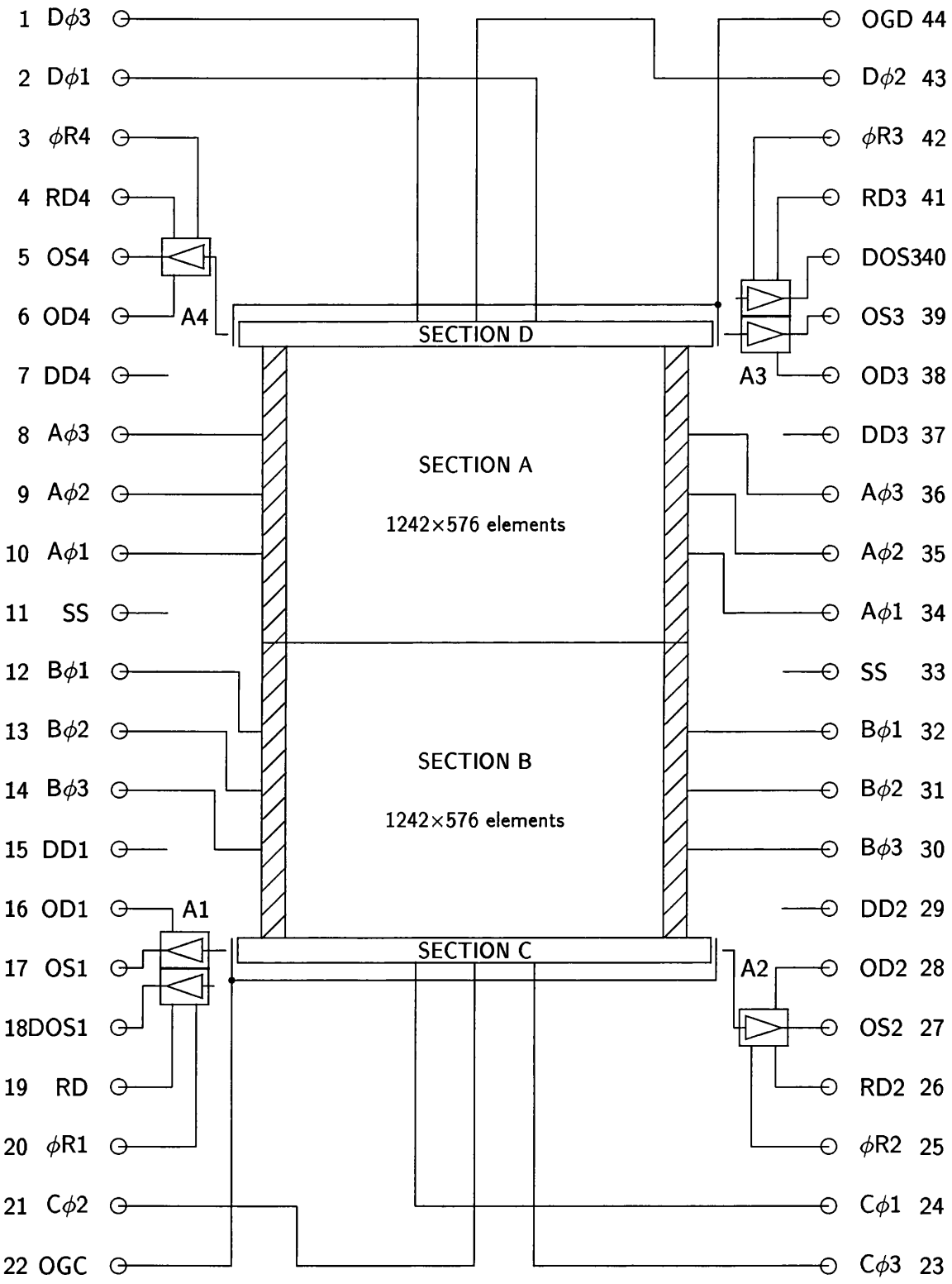

Figure 5.8: EEV P88000 series, standard CCD schematic.

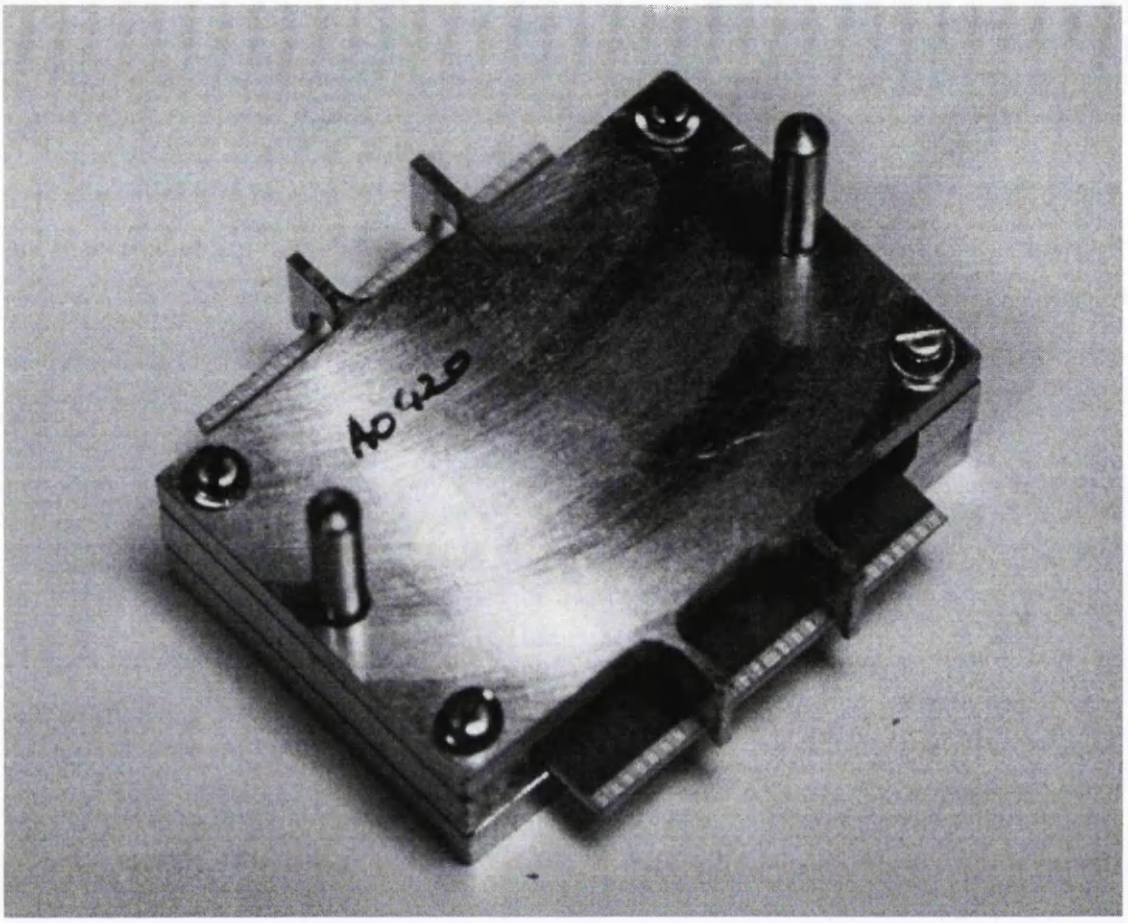

Figure 5.9: P88300UC transport jig.

5.3.1 68000 VME System

One of the data-acquisition computers for the mosaic CCD prototype is a VME-based 68000 CPU system. The system was manufactured by Force Computers Incorporated of California, USA. This system was originally procured for the UCL SAAO CCD system development in 1985[191]. The basic system components are:

- Force SYS68K/CPU-2F board. 10MHz CPU with one megabyte of RAM.
- Parallel interface board PIO-1.
- Serial board SIO-1. Six RS-232 compatible serial ports.
- WFC-1 disk controller.
- 20Mbyte fixed disk.

- 1Mbyte removable disk.
- Power supplies.

The system runs the PDOS real-time operating system[140] which is described in Section 4.6.1. The 68000 is interfaced to the mosaic control rack and a graphics display via a custom-built board described in Section 5.5. Control and data-acquisition software are described in Chapter 4.

5.3.1.1 PLUTO Graphics Engine

The graphics display used with the 68000 is an IO Research PLUTO colour graphics engine. The system, like the VME system, was originally purchased for the UCL SAAO CCD system development. The PLUTO provides for images up to 576×640 pixels in size. One byte is available per pixel, thus giving a possible 256 on-screen colours. The PLUTO is based around an 8088 CPU with ROM-based firmware which handles high-level graphics instructions like line and arc drawing. Programming of the PLUTO is described in Section 4.6.3. The display used is a Cotron Sword type F6. The interface to the PLUTO is described in Section 5.5.

5.3.2 Dell System 316

The IBM-PC clone used for the evaluation tests is a Dell system 316. The characteristics of this system are:

- MS-DOS 3.3 operating system.
- 16MHz 80386 CPU.
- 80387 mathematics coprocessor.
- 1MByte RAM.
- 4MByte Expanded/extended RAM.
- VGA compatible (320×200 pixels) graphics.
- 105Mbyte fixed disk.

- 1.2Mbyte removable disk.

Similarly to the 68000 system, the Dell is interfaced to the mosaic control rack via a custom-built board described in Section 5.5. However, at the LIM end of the link a simple parallel-communications card is used (Blue Chip PIO-48). The Dell runs the MS-DOS (3.3) operating system. Graphics display is achieved by either the use of the VGA display or by the Transputer graphics card described in the next section.

5.3.2.1 Harlequin Transputer Graphics Card

The PC-based data-acquisition system uses an Harlequin Graphics Board (TSB07) manufactured by Transtech Devices Limited. This card was originally acquired as part of the DTI Transputer Initiative as part of the research work of David Mills into the processing of large astronomical data sets.

The board has two 512×512-pixel image buffers, so that fast toggling between two images is possible. Eight bits per pixel are available, giving 256 on-screen colours. The on-board processor is a 25MHz Inmos T800 Transputer. The PC appears at the end of one of the serial links (Link 0) from the Transputer. Software at the PC end emulates Transputer communications and downloads the boot code for the graphics board. Programming of the board is described in Section 4.6.3. The image display used is an NEC Multisync type II monitor.

5.3.3 Connection to other Computers

One of the serial ports on the 68000 system is configured to allow the system to be connected to a DECserver which is party to the departmental thin-wire Ethernet. This allows slow-rate transfer of data to and from the local STARLINK cluster and remote control of the system.

A second port is available for remote control of the 68000 from a local microcomputer, typically an IBM-PC. This allows the remote user to control the mosaic detector hardware from their local system, whilst seamlessly co-ordinating the data acquisition and display at the 68000.

5.4 Power Supplies & System Rack

The power supplies for the mosaic detector system are mounted on a base plate to fit into a 19″-wide rack. The unit has a front-panel-mounted on/off switch and mains inlet with filter. The rack houses five linear power supplies, manufactured by Lambda Electronics. Two pairs of supplies are arranged to give complementary power rails at ±26.5V (type LOS-W-24V) and ±17V (type LOS-W-20V). The fifth supply (type LOS-W-5V) provides the +5V digital rail. The linear returns of the five supplies are connected at a single 'star point' in this rack. Separate returns for digital and linear supplies are provided for the main system rack.

The power supplies are passed to the system rack through a cable connected at a 19-way Trident connector.

The prototype hardware circuit boards are mounted in a BICC VERO KM6-II rack, size 84HP by 6U height. A BICC-VERO J1 nine-slot VME motherboard forms the upper part of the rack backplane. The rack and the main boards are shown in Figure 5.3

5.5 Communications

5.5.1 VME 68000 Based Communications

The CCD electronics rack is mapped in to the address space of the 68000 by an interface board. The rack appears as 128 single-byte addresses, which may be written and read just like any of the memory on the CPU-2F board. The circuit board of the communications link at the CCD rack is shown in Figures 5.10 and 5.11. IC U7 is a reset generator, type TL7705ACP, which provides a hardware reset on power-up. This signal is made available at the backplane. The board base address is set at the VME rack which generates select, read and write control signals for the CCD rack. These control signals, along with the VME address bus bits 1 to 7, are sent to the CCD rack communication cards. The cable linking the two racks is a 5-metre 32-way twisted-pair cable. Signals are passed to the cable by quad differential line drivers, type AM26LS31CN. Signals are received from the cable by dual opto-isolators, type HP2630, the cable being terminated appropriately.

The eight-bit data pathway is opened as appropriate for the particular communication

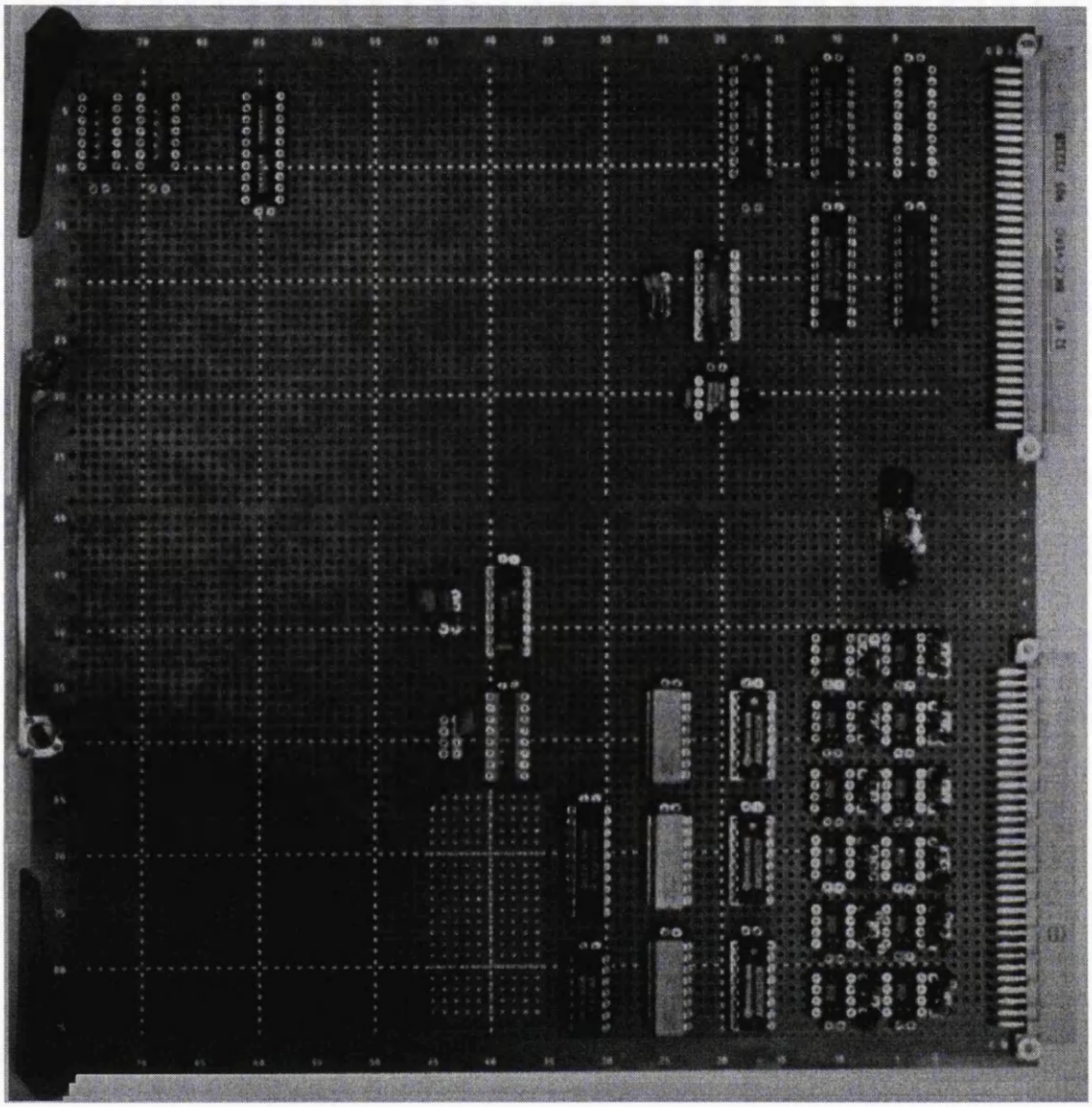

Figure 5.10: VME to CCD rack communications card.

being made. For VME to CCD rack write cycles, the data are supplied to the CCD rack by differential line drivers at the VME rack. Separate lines in the 5-metre cable are provided for the return of data from the CCD rack during read cycles, and these are again buffered to the cable by differential line drivers. At the CCD rack the backplane data bus is connected to the communications link as appropriate for the cycle by buffers U2 and U4.

ICs U6, U8 and U9 are dual monostable multivibrators, used to generate suitable buffer control signals for the CCD-rack backplane. The DTACK signal from the VME rack is

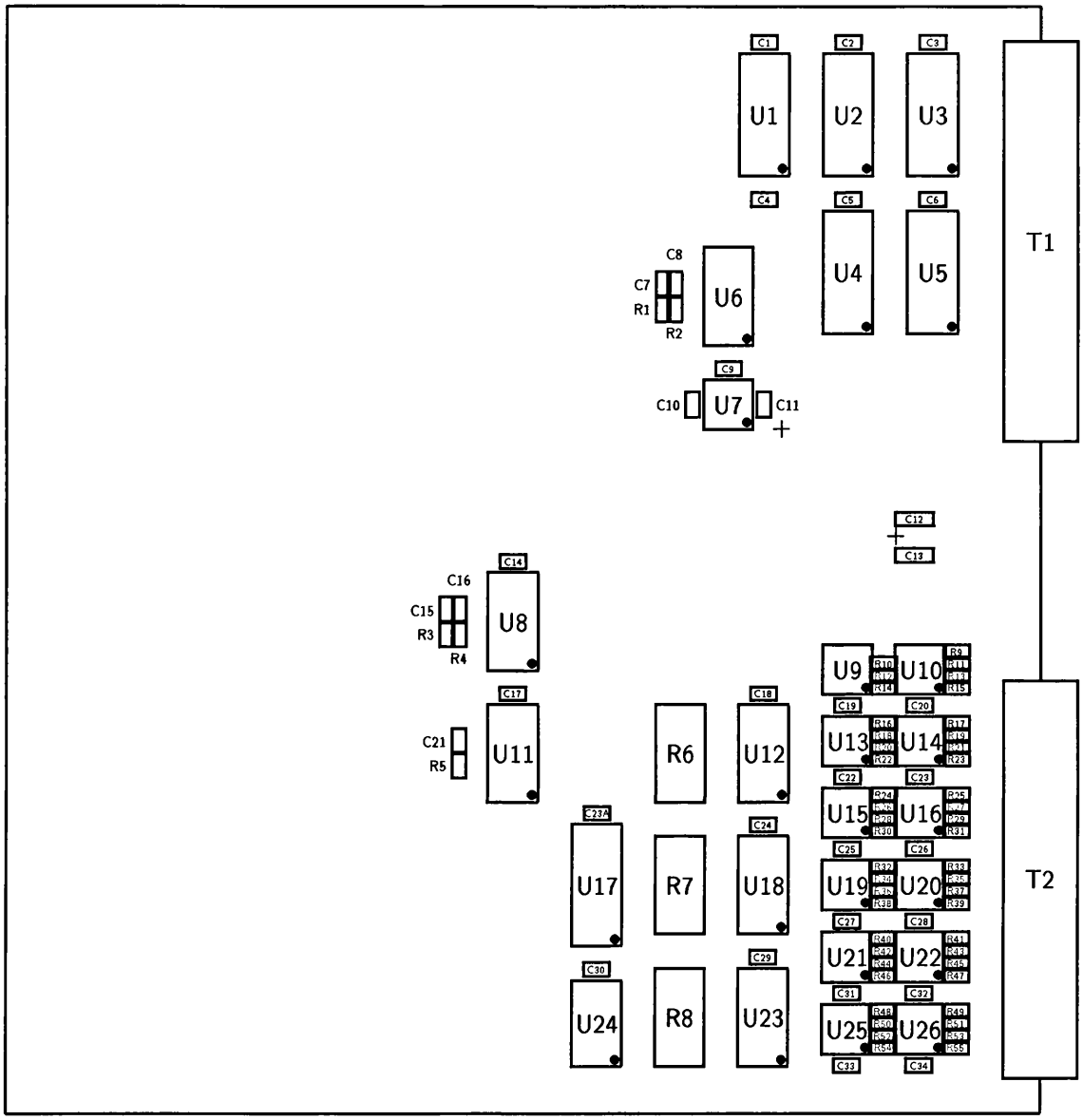

Figure 5.11: VME to CCD rack communications card layout.

passed down the 5-metre cable and delayed by U9 before being returned to the VME rack. This allows for the small delay in propagation of control signals within the CCD rack, and, because the signal is passed through the cable, the delay introduced by it is removed.

The timing diagrams for CCD-rack read and write cycles are shown in Figures 5.12 and 5.13. Read and write cycle timing data are given in tables 5.2 and 5.3 respectively.

during voltage level assignment cycles.

When the VME system is in use for data acquisition only (see Section 5.1.1) the CCD

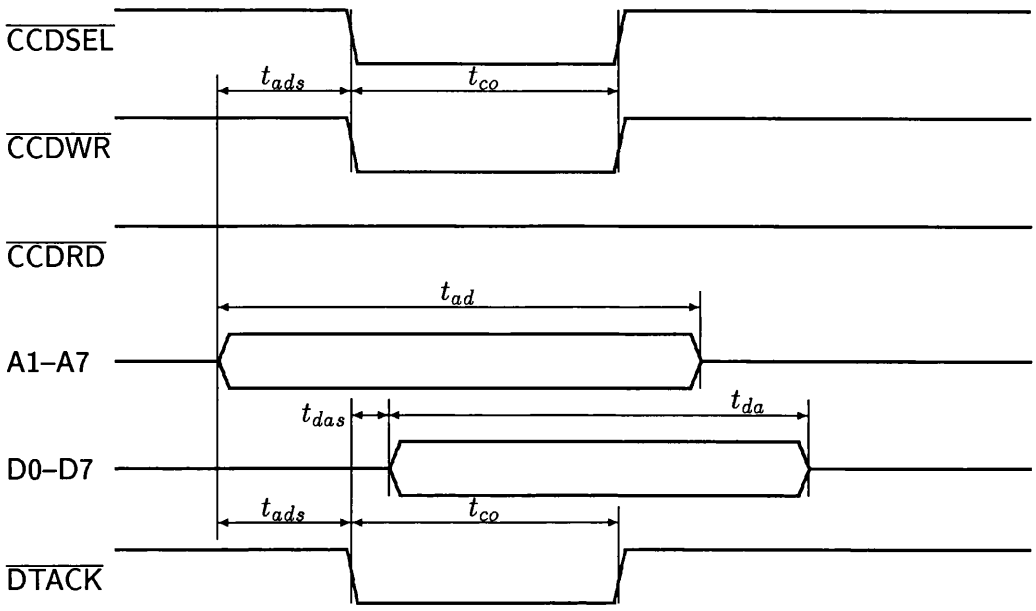

Figure 5.12: VME from CCD rack data write cycle.

Symbol	Parameter	Value/nS
t_{ads}	Address set-up time	250
t_{co}	Control signal hold time	500
t_{ad}	Address hold time	880
t_{das}	Data set-up time	70
t_{da}	Data hold time	760

Table 5.2: VME to CCD rack data write cycle timing.

Symbol	Parameter	Value/nS
t_{co}	Control signal hold time	500
t_{ads}	Address set-up time	260
t_{ad}	Address hold time	1880
t_{das}	Data set-up time	100
t_{da}	Data hold time	920
t_{dap}	Data propagation time	660

Table 5.3: VME from CCD rack data read cycle timing.

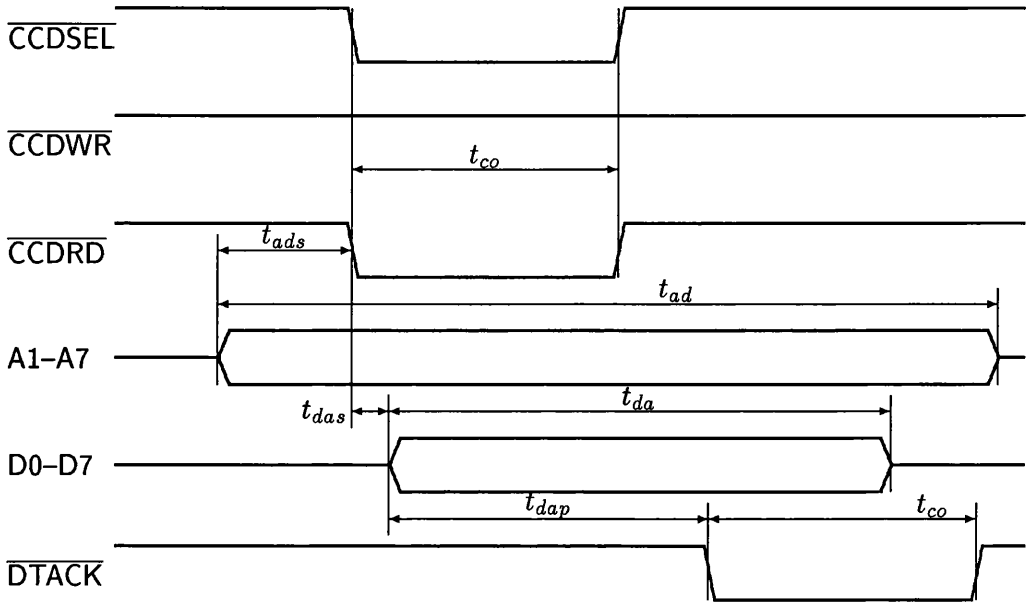

Figure 5.13: VME from CCD rack data read cycle.

rack communications card must be disabled, except during mosaic readout. The buffer U17 accepts a signal from the backplane which is provided by the PC controller, which disables the board at such times as are necessary. The three IC sockets at the top left corner of the board were used to mount a buffer and two hexadecimal digital-display LEDs. These were used for debugging the interface.

The VME communications card (designed and constructed by A. C. Fish) serves a dual purpose, linking the 68000 to the CCD-rack hardware and to the PLUTO graphics engine. The board is similar to the CCD-rack communications card, except that it also has channels for the link to the PLUTO and for address decoding from the VME backplane. A 68172 VME bus controller is used to arbitrate with the backplane. The base address of each of the two 'daughter' systems is set on this board by wire-wrap fields fed to address comparitors. Opto-isolators are used in all return lines from the CCD rack, giving complete electrical isolation of the two racks. The PLUTO link is, however, not opto-isolated—line driver/receiver combinations are used.

The PLUTO occupies only two addresses in the 68000 memory space, a data port and a status port. Communication through these addresses is controlled by routines prepared for the CCD-IPCS IDRIS image display system, which use the PLUTO command language. These routines have been linked with the `DMAP` system.

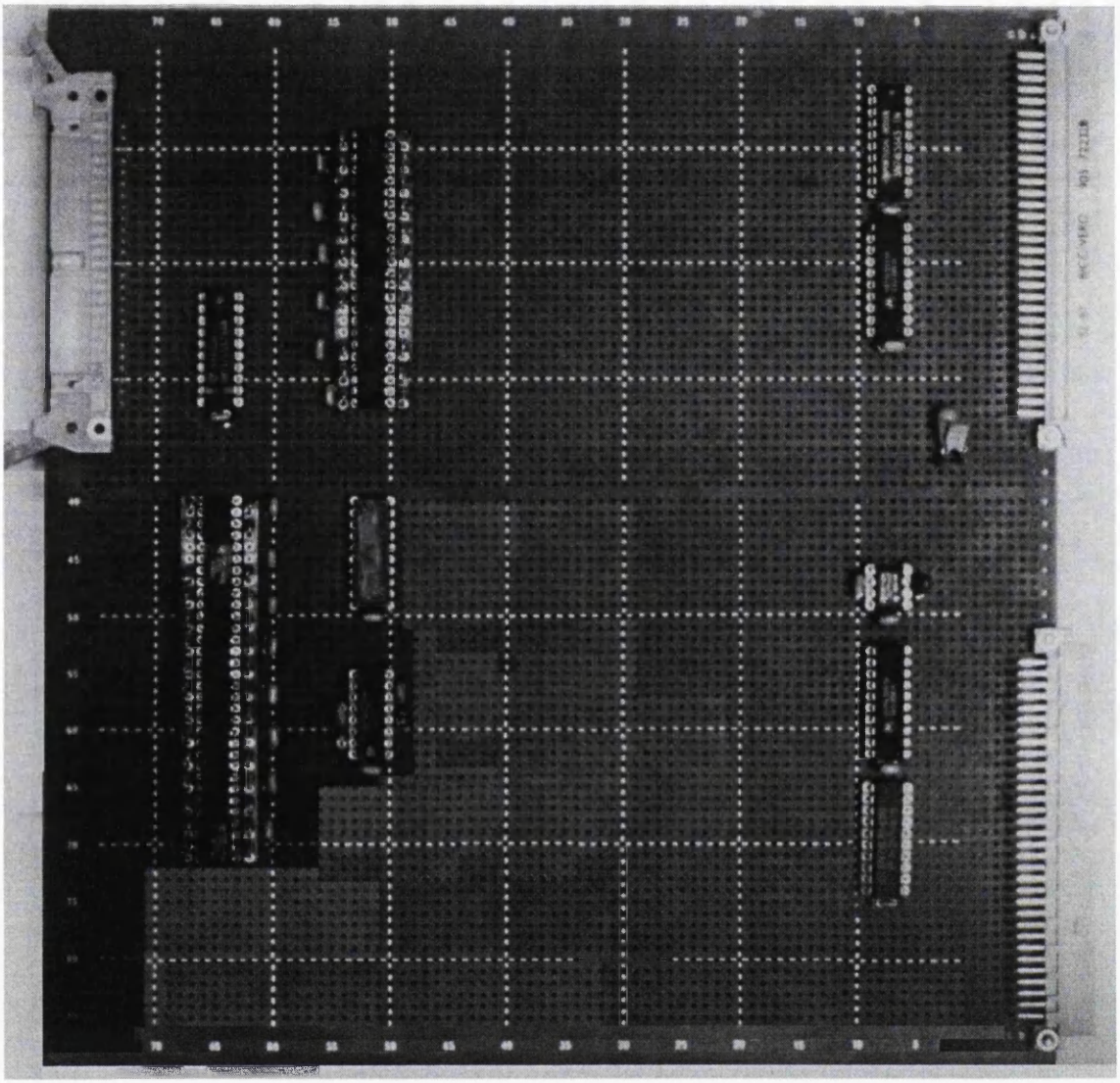

Figure 5.14: PC to CCD rack communications card.

5.5.2 PC Based Communications

When the Dell PC is used as the LIM the interface functions in a different manner. The Dell contains a parallel IO card with six eight-bit channels. This is connected to an interface card at the CCD control rack via a 50-way ribbon cable. The interface card is shown in Figures 5.14 and 5.15. The card carries opto-isolators for all digital lines from and to the PC. The digital power supplies from the PC are carried to the card via the ribbon cable. At the board the PLD E1 and dual monostable U16 generate suitable timing signals for the CCD-rack backplane (emulating the CCDWR, CCDRD

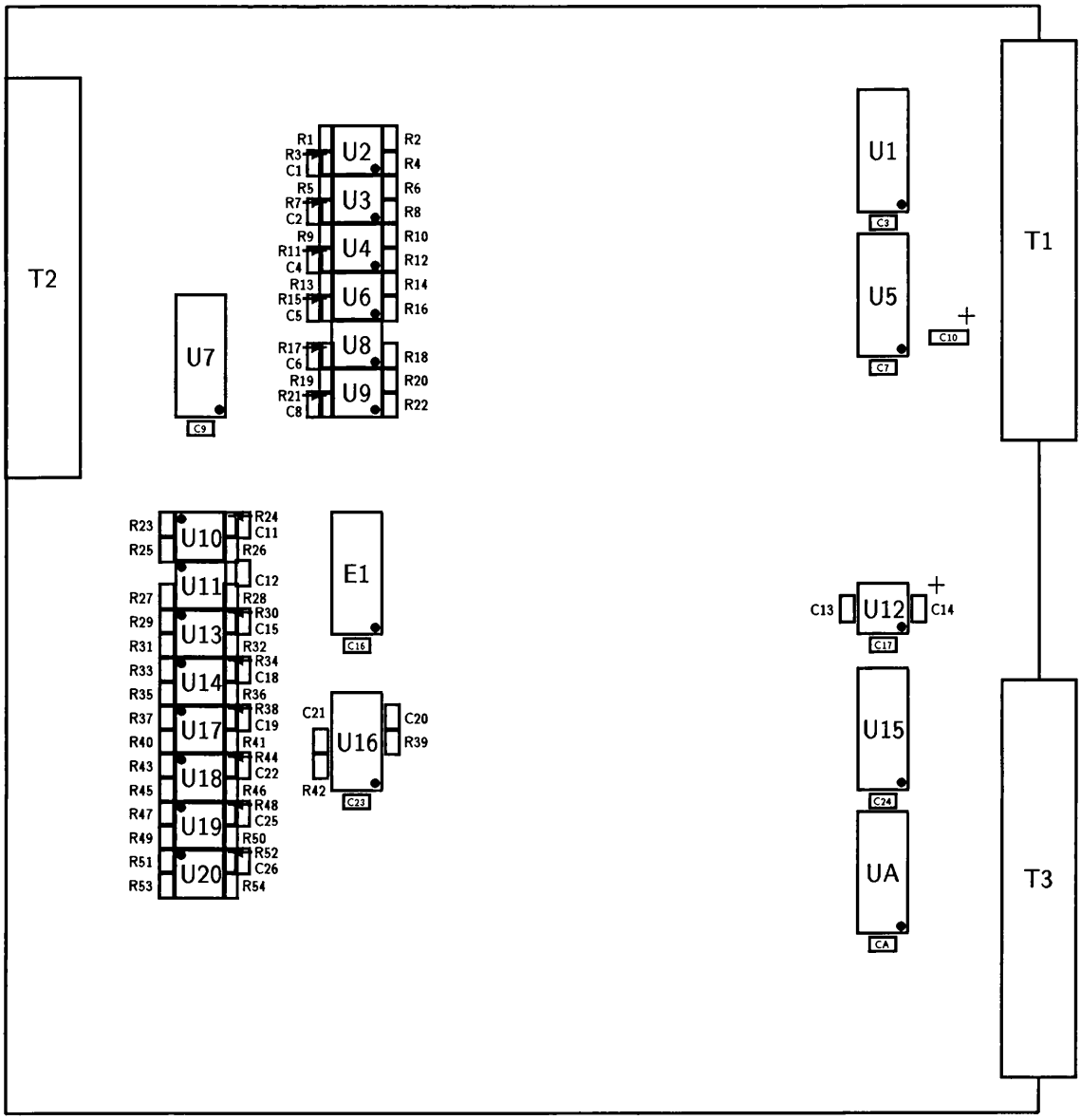

Figure 5.15: PC-to-CCD rack communications card layout.

and CCDSEL of the VME system). These signals are buffered to the backplane via U15 with address lines via U5, both 74LS541 buffers.

Section D.1 contains the software routine used for communication via this interface. The write cycle proceeds as follows. The data to be written are placed in the output latch of one of the channels of the PIO card. These data are buffered directly on to the CCD rack backplane. The address to be written is then placed in the output latch of a second channel of the PIO card and so made available on the CCD-rack backplane. The action of loading this second output latch strobes a single bit in a third output channel of the

PIO card and this triggers the CCD-rack backplane control signal sequence. The data are then used as required by the subsequent circuitry.

The read cycle operates in the reverse fashion. The address output latch of the PIO card is loaded first and this causes information from the CCD rack data bus to be latched in U7. This data byte is then read through a single input channel of the PIO card.

The power-up reset signal for the CCD rack is generated by U12.

Unlike in the VME-based system no data strobe (DTACK) type signal is passed back to the PC during a communications cycle. In practice this is not a problem as the communications action time plus the cable transmission delay is much less than the MS-DOS input/output operation time.

Buffer UA provides for switching between this board and the controller driving the rack backplane during dual-interface-controlled mode operation.

5.6 Controller Submodules

To demonstrate the sequencer concept described in Chapter 3, and to test prototypes of the driver submodule also described there, two working prototypes were constructed.

The first prototype (here described in detail) uses Altera's 'traditional' PLDs, the logic being shared between several ICs. The second is very similar in functional design, but uses the newer, denser logic of the MAX family of PLDs. The second prototype is described in detail elsewhere[73].

5.6.1 Controller Prototype Specification

The prototype constructed represents the minimum sub-set of the general sequencer specification described in Section 3.7. The controller consists of:

- One line counter—maximum count 4095.
- One pixel counter—maximum count 4095.
- One memory-access controller—maximum memory size 4kwords.
- Twenty-four-bit by 4kword memory cache—access time $\leq$ 100nS.

- Controller clock—5MHz (200nS period).
- Non-transparent latched output.

This specification allows for only one set of waveforms and pixel counts to be stored in the controller memory at a time. To change the operation mode, for example to pixel bin, new information must be downloaded from the LIM. In the laboratory this is not a serious limitation. In a production system the available memory would be expanded to hold mutliple programmes. The pixel and line counters are sufficiently large to operate all but the very largest detectors[92] in full-frame mode.

A further reduction in the design specification is the removal of all controller commands except those absolutely necessary for demonstration and test purposes. The commands implemented are:

- Set line count.
- Set pixel count.
- Set vertical pixel pointer.
- Set horizontal pixel pointer.
- Access controller memory from LIM.
- Step controller memory address.
- Start detector mosaic readout.

The controller occupies several addresses in the LIM processor's memory space. Normal memory access cycles are used to execute the above commands and to read or write access the controller memory cache. Only one address of the controller memory cache is visible to the LIM at any particular time, so the LIM must send a 'step controller memory address' command to move through the cache memory by one step. The various counts and pointers are stored in the PLDs in latches, in contrast to the general specification where the counts are stored in the high addresses of each page of memory. Making this change simplifies the memory-access controller, making the logic compact enough to occupy only one of the EP1800 PLDs. The 24-bit sequencing data output from the controller

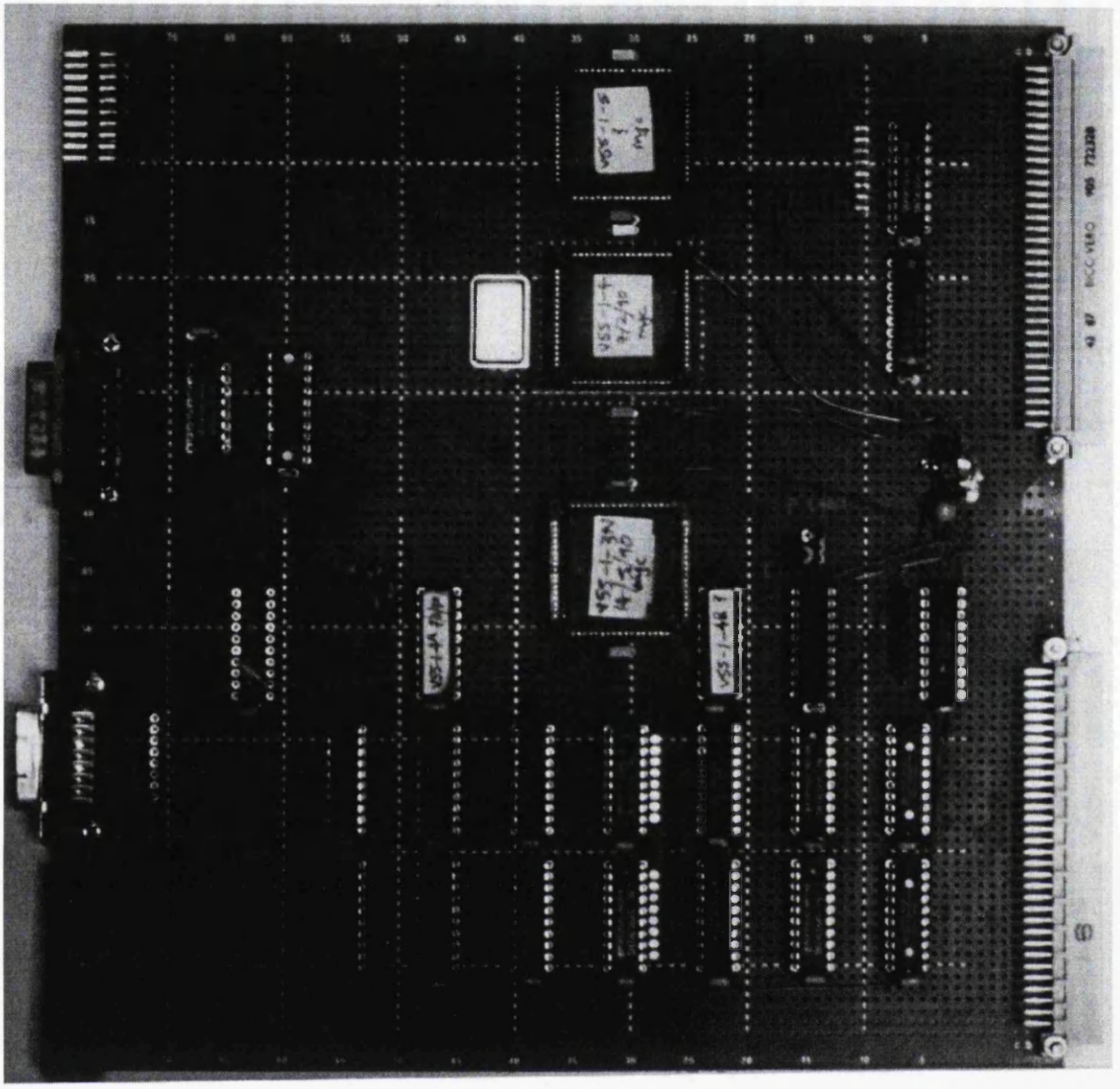

Figure 5.16: Prototype controller module.

memory cache is non-transparently latched at the controller submodule to ensure that clean, synchronous data are available to be used by the other system submodules.

5.6.2 Controller Hardware Description

The prototype controller module is shown in Figures 5.16 and 5.17. The prototype is wire-wrapped on a single-sided, double-height eurocard. It consists of twenty-five ICs: five PLDs, six memory chips, twelve TTL buffers, one differential line driver and one IC crystal.

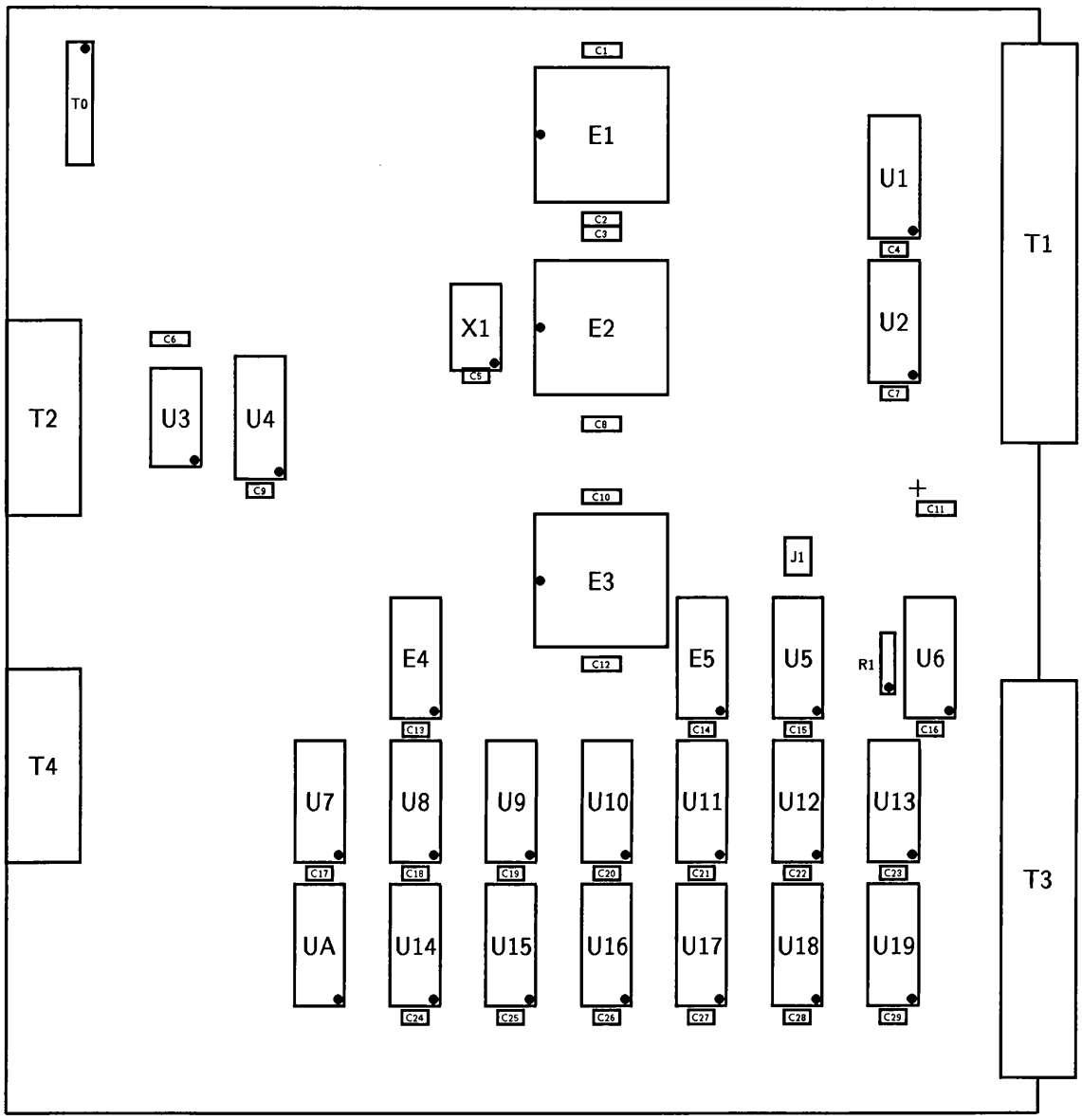

Figure 5.17: Prototype controller module layout.

The three larger PLDs (type EP1800) each contain one counter and ancillary logic. E1 is the line counter, E2 is the pixel counter and E3 is the memory access controller. During tests, it was found that the timing of logic signals passing between the devices was a problem, with 'logic races' between PLD-internal and signals from other PLDs. This was only manifest for clock rates $\geq$6MHz, the symptom being counter over-run: gates in the counter clock signal path were controlled by signals from other PLDs—at higher clock rates the delay in the gate-control signals was sufficient for extra clock edges to pass along the signal path *internal* to the PLD before the gate was closed. The PLDs would

then be left in a state of deadlock, each waiting for a signal from one of the others. This problem was solved by adding logic to synchronize the gate-control signal to the clock signal for each PLD. Due to the limited logic capacity of the EP1800, two further PLDs (E4 and E5, both type EP320) were needed to implement this logic—one being a buffer between the pixel counter and the line counter, the other between the memory-access controller and the pixel counter.

U5 and U6 sequence the data-path control signals from the LIM correctly at the controller. These ensure that data-bus interconnection buffers are enabled before and after the address and control signals of a cycle, thus allowing for any slight timing differences between the two.

Six memory ICs, Hitachi type HM6168HLP-45, are used. Their access time is 45nS, well within the specification. These static RAM devices have a very simple control timing requirement, which enabled the memory-access control logic to be fitted into one EP1800 PLD. Each memory IC is of size 4knibbles (4k addresses of 4 bits each), giving the requisite 24-bit by 4kword cache. The memory ICs are in three pairs, each pair appearing as a single eight-bit address to the LIM. The address lines of the memory ICs are all connected to a common controller-internal address bus. During controller operation (mosaic readout) the TTL latches U4, U8 and U14 non-transparently latch the data appearing at the outputs of the memory on rising edges of the system clock. This makes available clean signals, valid for virtually the full 200nS cycle time. Jitter effects during the 45nS memory access time are thus eliminated.

Of the 24 bits output from the memory, three are buffered by U3, a quad differential line driver, type AM26LS31CN, to match the specification of the existing UCL SAAO preamplifier; two bits are made available at the backplane (connector T1, pins 24b and 15b) for use as the ADC trigger pulse and device select; and sixteen bits plus data strobe and bus control logic are relayed to the driver submodule via T0. In addition, five bits and control signals are relayed to the OSL preamplifier via T4. Conversion between operation modes for the UCL SAAO and OSL preamplifiers is achieved by altering the code in the controller memory and is entirely handled by `DMAP`.

The jumper J1 allows the ADC trigger pulse to be sent directly from the LIM rather than from the controller submodule for test purposes.

5.6.3 Prototype Verification

Correct operation of the prototype has been confirmed using a logic analyser (Gould type K50/Thandar TA2000), and tests on memory loading and counter cycling have proved successful. When connected to the preamplifier, sequencing of the three timing signals as set in control software has been observed. When connected to a driver submodule prototype, further tests verified that the link to that submodule is functionally correct.

Adjustments to the waveforms downloaded from the LIM showed excellent controllability of the signal spacing, as expected.

An intermittent problem with controller triggering (*i.e.* mosaic readout) was diagnosed as caused by the PC-based communications cycle being faster than the original VME system. The problem was removed by adjusting the control-signal timing of the communications cycle to match that in the VME system (see Figures 5.12 and 5.13). The command decoder used in the system prototype (within a PLD) will be modified in subsequent revisions of the controller so that communications timing is non-critical.

5.7 Driver Submodules

Like the controller module, two prototypes of the driver module were built. Both designs are based on available octal DAC ICs (see Section 3.5.4). One design is a simple array of DACs, all on a common data/address/control bus, buffered to the detector array. This design is described here in detail. The second prototype uses an array of FET switches to select between voltage levels generated by the DACs, these 'switchable' levels then being buffered to the detector array. A detailed description of the second prototype is given elsewhere[73], its design is described here in outline only.

Experimentation with these prototypes is described below, leading to a design for a production version of the driver module.

5.7.1 Driver Prototype Specification

The specification of these modules is essentially the same as for the production version described in Section 3.5. The main difference is that these prototypes are designed to

operate only four devices of a general specification. For the 'common bus' type driver module the specification is:

- Thirty-two clock signal sources—output voltage range −12V to +12V.
- Thirty-two bias voltage sources—output voltage range 0V to +24V.

To simplify the prototypes further a total of only sixteen bias-voltage sources has been provided, sufficient to operate four of the P88300UC devices.

The 'switchable'-type driver has identical bias-voltage requirements, however the clock signal specification is different:

- Two sets of four switches between two levels (for driving image and readout registers) per device.
- One switch between two levels (for driving the readout amplifier reset pulse) per device.

The levels in this specification are each generated by a single DAC. A production implementation might require some extra sources of the reset-pulse type to drive transfer gates, if devices of that type are present in the detector mosaic.

A standard interconnection scheme for controller to driver and driver to cryostat links was chosen, so that the various controller and driver modules could be interchanged easily for comparative experiments.

5.7.2 Hardware Description

5.7.2.1 Common Bus Type

The prototype of this driver module is shown in Figures 5.18 and 5.19. The prototype consists of thirty-seven ICs: eleven quad operational amplifiers (four uni-polar, seven bi-polar); six j-lead SMT-packaged Bt110 octal DACs; one TTL buffer; one unity-gain buffer; one voltage reference; one dual relay driver; one decoder; and one PLD.

The six octal DACs are on the common data/address/control bus, with chip selects generated by U1, which decodes the A4–A6 address lines. Board selection is achieved by

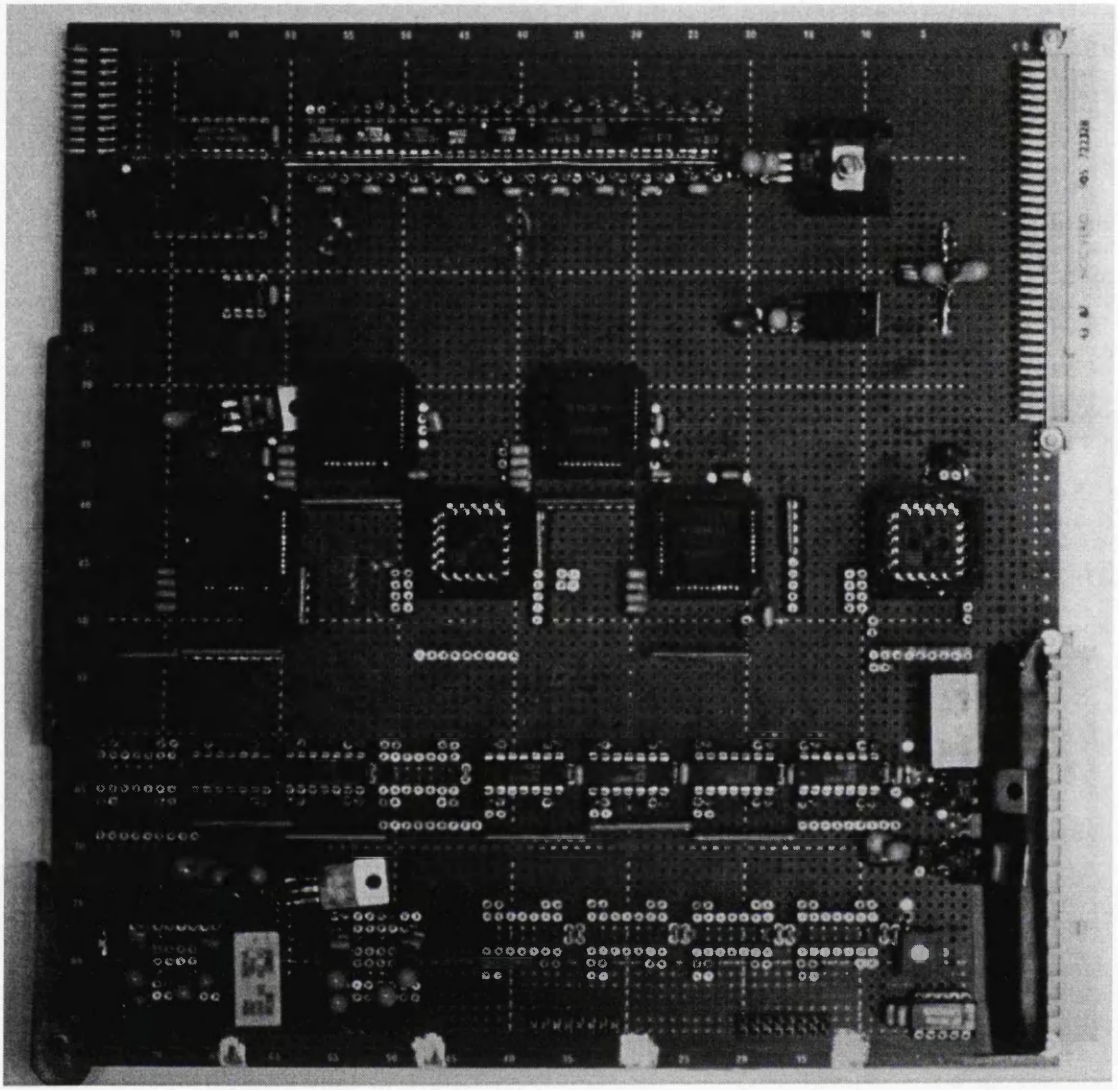

Figure 5.18: Prototype driver module.

setting A7 high. This module thus occupies the upper half of the 128 addresses available on the module-control bus, and each DAC appears to the controller as a single address. The Bt110 octal DACs require a large number of passive components in attendance for correct operation, they are current sourcing devices, hence a transresistance configuration is required to convert the output to a particular voltage range. Passive-component values were chosen to give a maximum 1mA current output into a 1kΩ resistor, *i.e.*, a 0V to +1V output range. Each of the 1V FSR is amplified by a simple ×25 configured op-amp to give the full 25V swing required at a resolution of about 0.1V. The bi-polar sources for clock signals are achieved by offsetting the 25V swing by −12.5V; this is done using

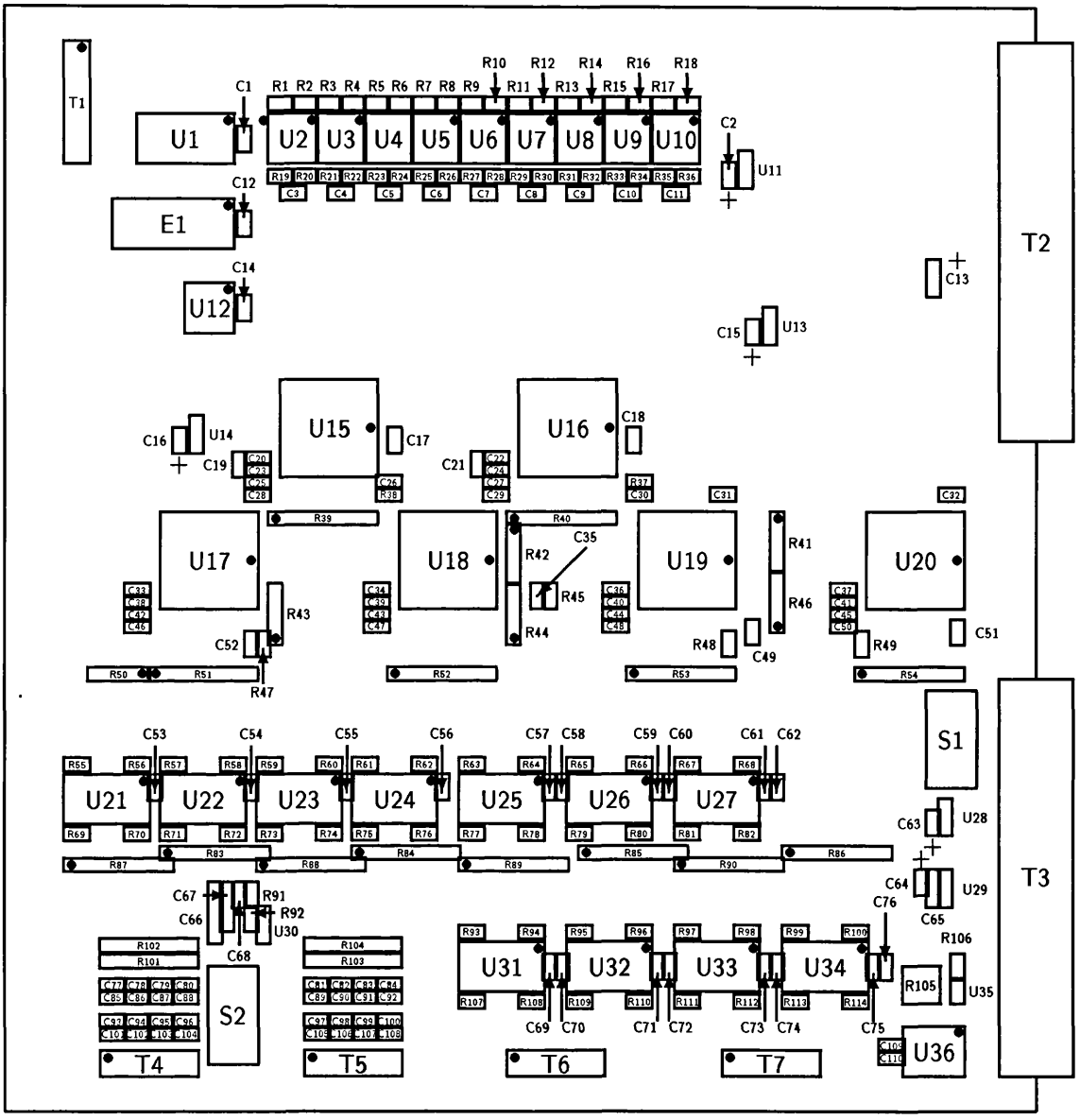

Figure 5.19: Prototype driver module layout.

a reference voltage of approximately 0.5V generated by U35 and U36 and fed to the inverting inputs of the bi-polar op-amps.

The power supplies to the op-amps are switched by the relays S1 and S2. These relays are software controlled and power up to an open (op-amp power supplies off) state. The EP320 PLD, E1 decodes relay control logic from the backplane bus. The relays appear to the controller at one of the spare addresses in the driver board DAC array, (*i.e.*, as one of the DACs not required to operate EEV CCDs). During the power-up sequence, a program to initialise the outputs of the DACs and then switch on the relays is down-

loaded from the LIM to the controller. This programme is executed and the component devices of the focal-plane array are thus powered-up in the correct bias-voltage state.

5.7.2.2 Switchable Type

A full description of this prototype can be found elsewhere[73]. Attention is drawn to the differences between the common bus driver and this second type. The switchable voltage sources are generated by Octal DACs, in this case the Analogue Devices AD7228. The AD7228 is a 28-pin DIL packaged device, a *voltage* sourcing device which requires no attendant passive components and thus has a double-size advantage over the DIL packaged Bt110. The AD7228, however, can only source 5mA, which is much less than the 25mA required to drive the detectors in the mosaic. Also, the AD7228 has an output settling time of 5μS , which is too slow for use in the common-bus type driver.

The bias levels required are generated by buffering the DAC outputs with op-amps as in the common bus driver. Pairs of DAC outputs are used as sources for arrays of switches. One DAC in a pair is the source for the clock 'high' level, the other is the clock 'low' level. The output from each switch is op-amp buffered to the devices to give the correct voltage range.

The DACs in this case are again common bussed and sit in the MCB memory space, with voltage levels (bias and clock high and low levels) set directly by the controller. An array of latches whose state is set by the controller is built into a PLD at the driver module; these set the state of the clocks at the devices in the mosaic. The op-amps are on a separate power supply (from the DACs) so that they can be activated after the initial voltage states have been sent by the controller, again by software-controlled relays.

5.7.3 Prototype Verification

At first, the common bus driver prototype had dual control from the LIM and from the controller module. When complete, it was found that some significant digital cross-talk was occurring. The voltage output from DACs which were not being accessed was observed to change. Testing identified the problem as short glitches in the address information from the LIM. Address information was subsequently latched at the driver module. The use of a non-transparent latch eliminated the problem.

The Bt110 has a latch-read capability, making it possible to read the data stored in the internal latches of the device back to the control computer. A simple programme to check for digital cross-talk and correct latching was designed and run for extensive periods (representing tens of millions of latch operations) to confirm the reliability of the driver-board logic. A mechanical problem (poor seating) with U2 was found by this means.

When connected to the controller, correct operation was found, with the requisite waveforms for operating the detector mosaic being generated. Tests of the driver module loaded with capacitor networks designed to simulate the loading by a CCD showed that the circuit was easily able to meet the required edge-speed and overlap-control specifications. The edges observed are exponential in shape, taking 2.6μS for 90% of the swing from 0V to +10V when loaded by an EEV P8603. Satisfactory edge overlap and charge-transfer efficiency was achieved by adjustment of the waveform look-up tables in the controller memory cache.

Once the basic functionality of the board was acceptable, the interface to the rack backplane was removed to reduce digital noise feed-through to the sensitive analogue parts of the board.

During over-all system noise characterisation (see Chapter 6) it was found that the major noise source was digital switching being fed through the clock buffers. To reduce the effect the large $\times 25$ voltage gain was reduced. This was achieved by modifying the DAC output buffering to utilise the full 2.2V (-1V to +1.2V) output compliance of the Bt110. This has the dual benefits of reducing the gain required to $\times 10$ and removing the need for the 0.5V offset input to the op-amp buffers. Instead, a -1.2V offset is generated by a heavily filtered potentiometer and U36. These changes effectively reduced the digital feedthrough to a level which does not degrade over-all noise performance. An unexpected benefit of the modifications made was an improvement in edge time to $\approx 1.0\mu$S. This is discussed in more detail in Section 6.2.3.

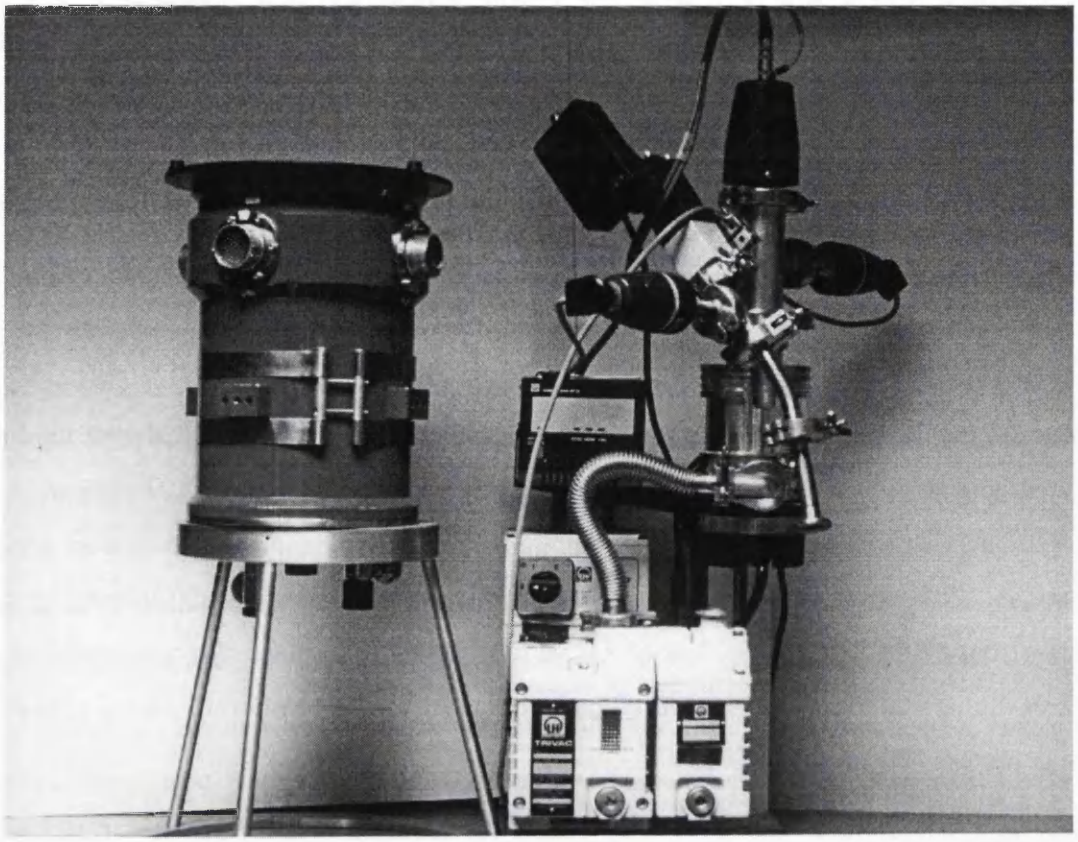

Figure 5.20: Cryostat and vacuum system.

5.8 Cryostat, Vacuum system & Head Electronics

5.8.1 Oxford Instruments Cryostat

An Oxford Instruments liquid-nitrogen cryostat, type MN1815INV, was purchased for testing of CCD detectors and drive electronics. The cryostat can be seen in Figure 5.20 with the vacuum-pumping system. A schematic cross-section of the cryostat is shown in Figure 5.21. The cryostat was supplied with 4 radial ports, each with 55-way Amphenol type connectors. A sorbtion pump to improve vacuum hold time was included. The window of the vacuum chamber is 80mm diameter×4mm thick, fashioned from fused silica. Re-entrant tubing to allow inverted operation of the cryostat was supplied. Test data provided by Oxford Instruments are summarised in Table 5.4.

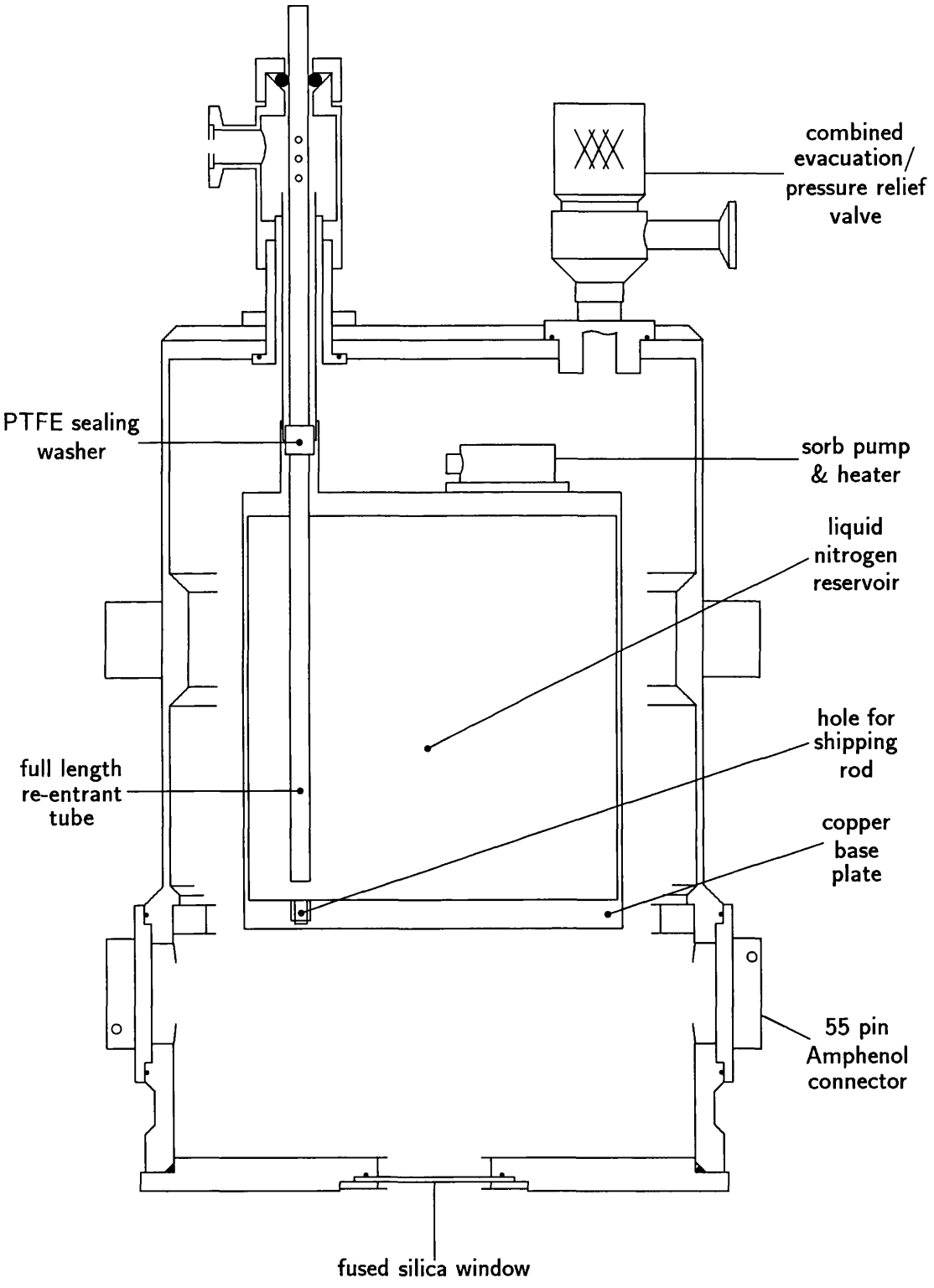

Figure 5.21: Vertical section through MN1815INV cryostat.[137]

Parameter	Value	Unit
LN_2 capacity	1.5	litres
Hold time (upright)	34	hours
Hold time (inverted)	29	hours
Resistance of sorb heater	155	ohms

Table 5.4: Test data for cryostat, serial number 31459.

5.8.2 Leybold Hyraeus vacuum system

To evacuate the liquid-nitrogen cryostat, a vacuum-pumping system was acquired. This replaced a diffusion/backing pump combination which had been in laboratory use for several years. The pumps can be seen in Figure 5.20 with the cryostat. Figure 5.22 shows the pumping arrangement in schematic form. The two pumps are a rotary pump and a turbomolecular pump. The rotary pump is used for achieving a rough vacuum in the cryostat and for backing the turbomolecular pump. The rotary pump will evacuate the cryostat to a pressure of about 10^{-6} bar. The turbomolecular pump can operate down to about 10^{-9} bar, which is more than sufficient for the operation of the detector mosaic at temperatures of the order of 100K to 150K. The system has three gauge heads connected to a single moving-coil meter with appropriate shunting electronics. The gauges marked T in Figure 5.22 are thermal-conductivity gauges which can measure pressures from atmospheric down to 10^{-7} bar. The P gauge head is of the Penning type, for measurement of pressures down to 10^{-12} bar. The electromagnetic valve isolates the vacuum system from the cryostat when power to the pump stand is removed or fails. This prevents damage to the blades of the turbomolecular pump. Once the cryostat has been evacuated it can be decoupled from the vacuum system at the seal crossed by a dashed line in Figure 5.22.

5.8.3 Camera-Head Electronics

Figure 5.23 shows the headboard and four P86000 class CCDs in the cryostat. The board and assembly were designed and built by W. Han, for electronic, system noise and linearity testing only. The head circuit for one CCD is shown in Figure 5.24. The circuit

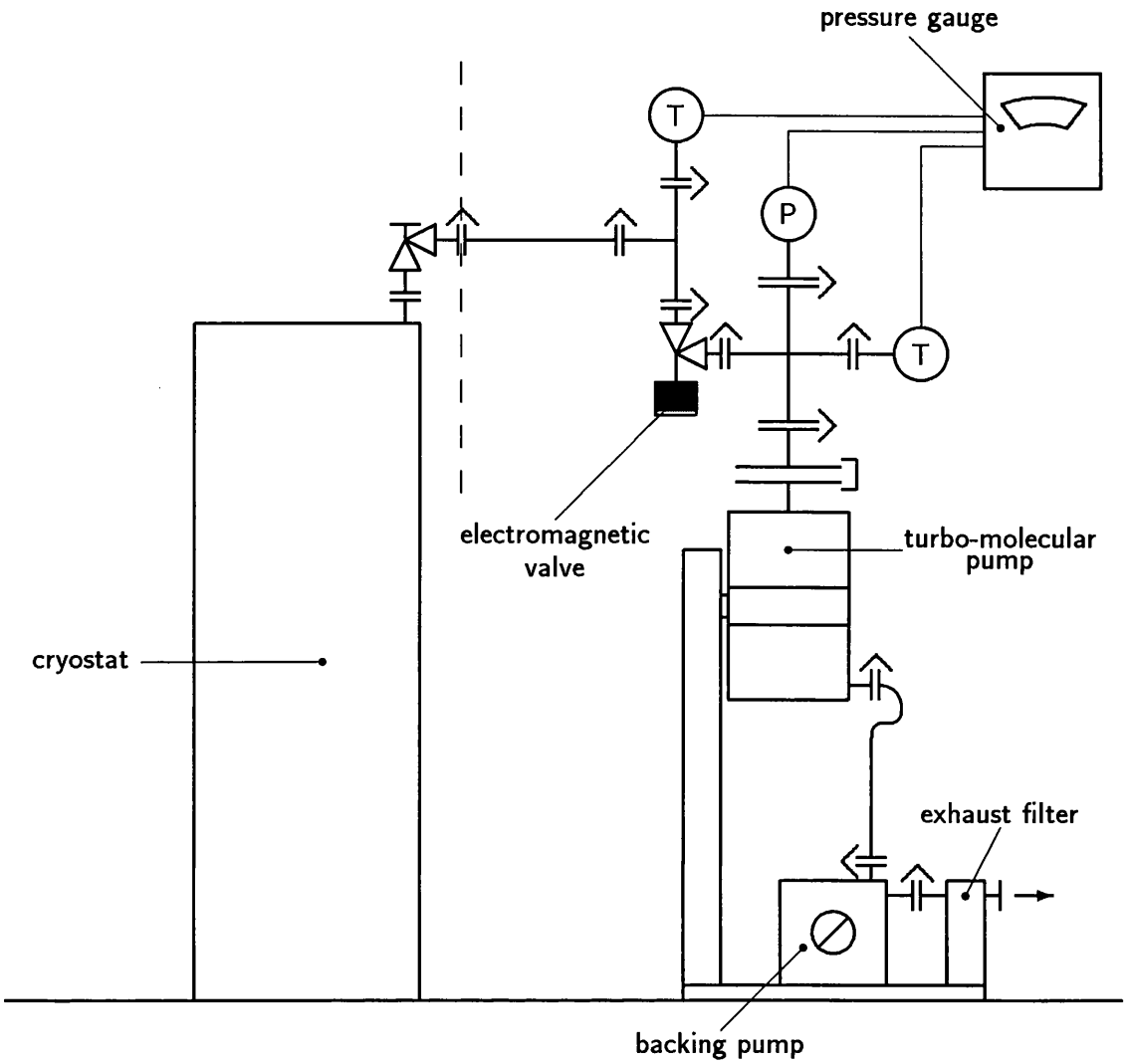

Figure 5.22: Leybold Hyraeus vacuum system in schematic.

is replicated four times, once for each device. All of the signals required by the detectors are passed directly from outside the cryostat to the mosaic. A constant-current source to drive the output coaxial cable is provided on the headboard (×4), this being the only intra-cryostat circuitry apart from the CCDs themselves, the temperature telemetry and the sorbtion-pump heater.[2]

Figure 5.25 shows the assembly for four of the P88300UC devices dismounted from the cryostat. A schematic of the assembly in the cryostat is shown in Figure 5.26. This assembly was designed by H. O. Jamshidi. The four devices are mounted in ZIF sockets

[2]This headboard was subsequently replaced with a ground-plane board for two-device testing (in particular for device-to-device cross talk measurement). The newer board supports capacitive filtering of bias voltages for the devices and does not carry any constant current sources.

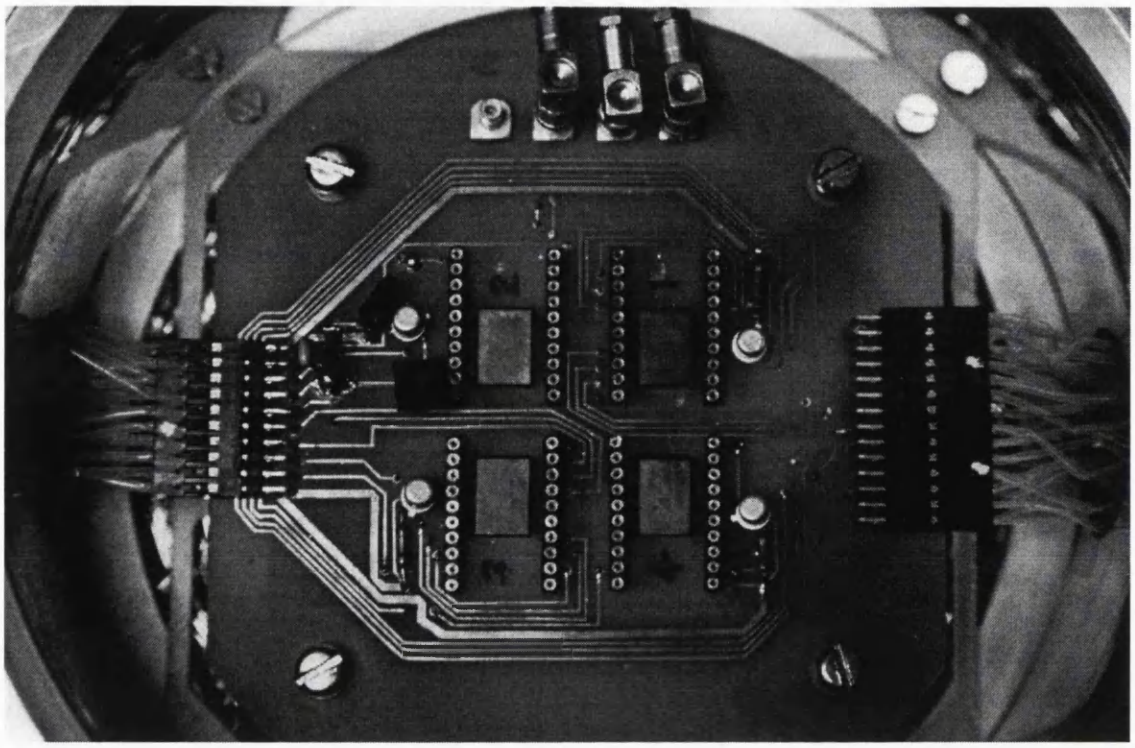

Figure 5.23: P86000 series CCD camera head.

which are in turn mounted on a simple PCB which routes the output lines to two half size DIN41642 connectors. These connect to a second PCB carrying the head circuit.

5.9 Preamplifier and Signal Processor

Two preamplifier and signal processing circuits have be used during the course of the Mosaic Detector Project; one constructed for earlier work at the OSL, the other based on the Janesick/JPL preamplifier and Leach/SDSU signal processor.

5.9.1 Single-CCD Testing

The preamplifier used for single-CCD noise tests was originally constructed for laboratory evaluation of the UCL SAAO CCD system[191]. Figure 5.27 shows the preamplifier box with its perforated lid removed. The circuitry is divided into two parts: the power-TTL section and the preamplifier section.

The power-TTL section regulates the power rails ($\pm$15V, +5V) for the preamplifier sec-

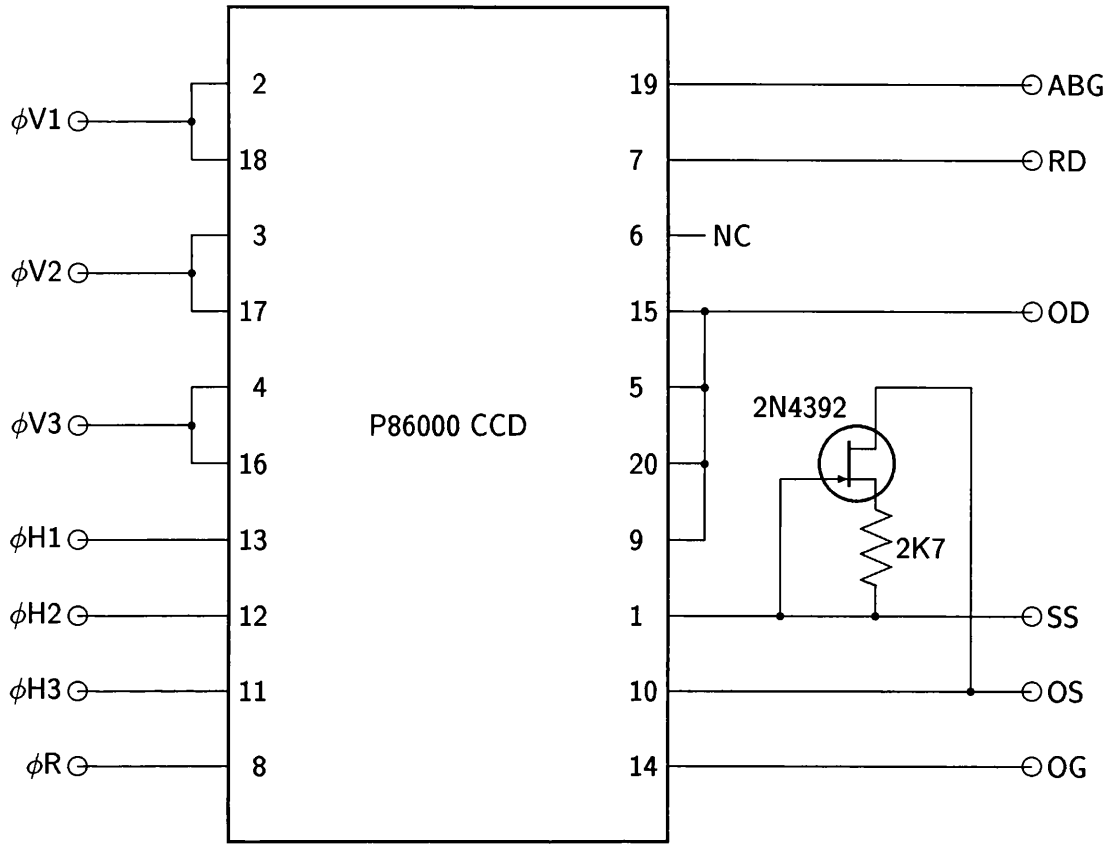

Figure 5.24: Head circuit for one CCD.

tion. In the UCL SAAO system this circuit also provided the bias voltages for the CCD; only the video reference level is used in the current system. TTL control signals from the controller module are opto-isolated in this section and passed to the preamplifier section through short coaxial cables.

Figure 5.28 shows the circuit of the preamplifier and dual-slope integrator. The circuit has essentially three sections: the input stage, inverter and integrator, and output buffer. The input stage is based around a low-noise NE5534AN op-amp. In the UCL SAAO system, the large DC pedestal of the CCD output signal was largely removed by a differential amplifier on the CCD headboard. This is no longer the case in the mosaic detector system, where the CCD output signal is presented directly to the preamplifier input stage. To remove the large DC component of the signal the input stage has been slightly modified, an AC couple being added. Only the small AC component of the CCD output, the actual signal, is passed through to the first stage of the preamplifier. The input

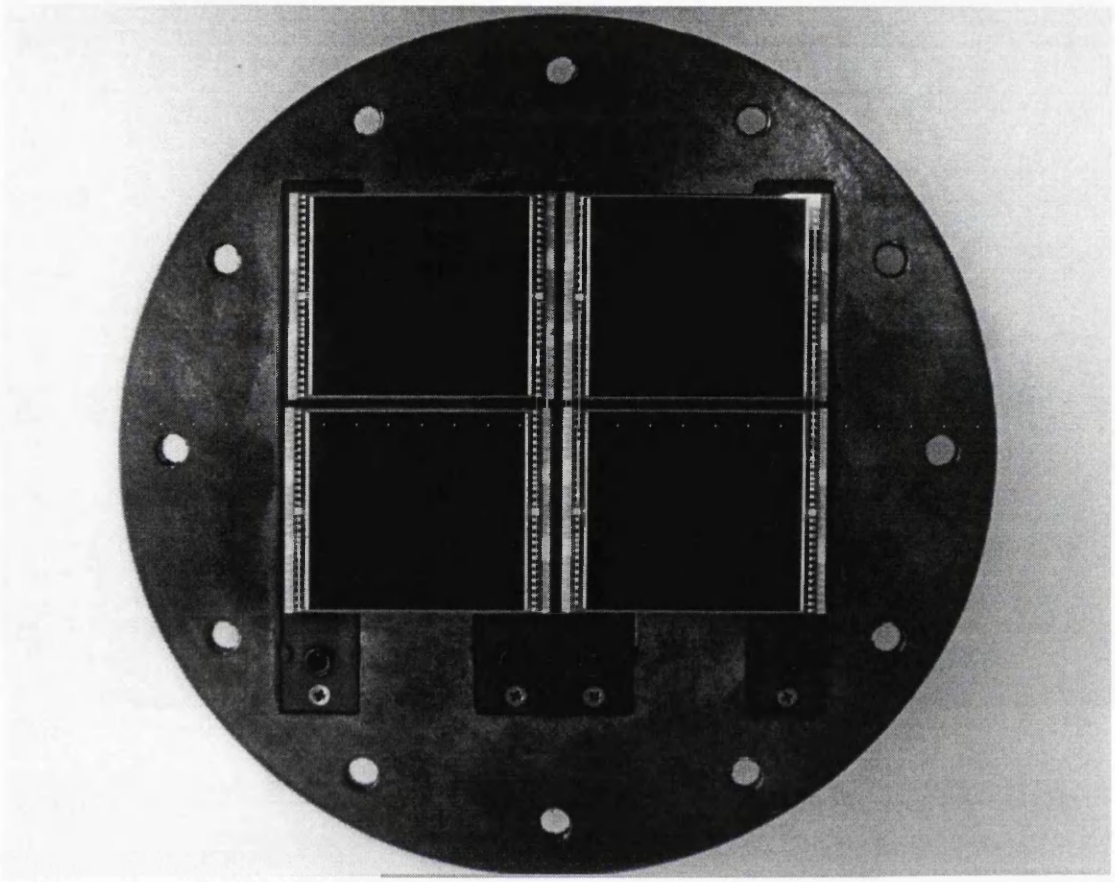

Figure 5.25: P88000 series CCD camera head.

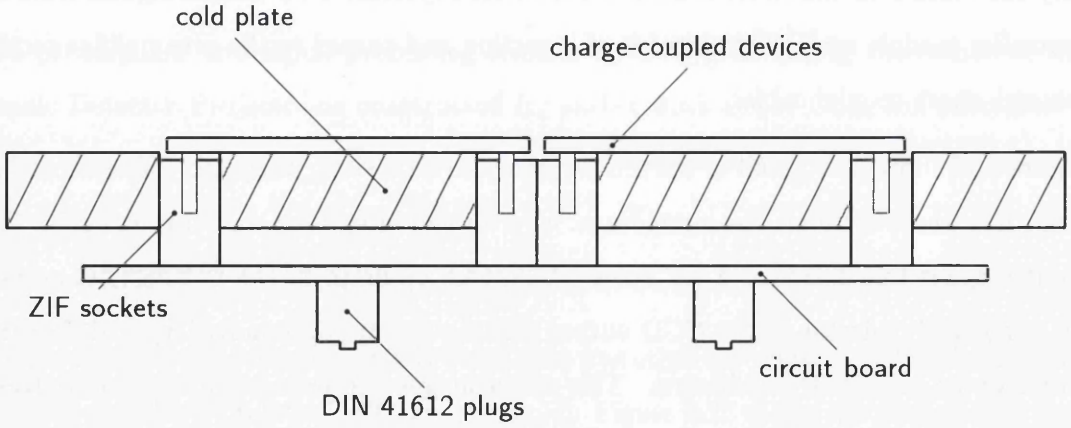

Figure 5.26: Schematic of buttable CCD head assembly.

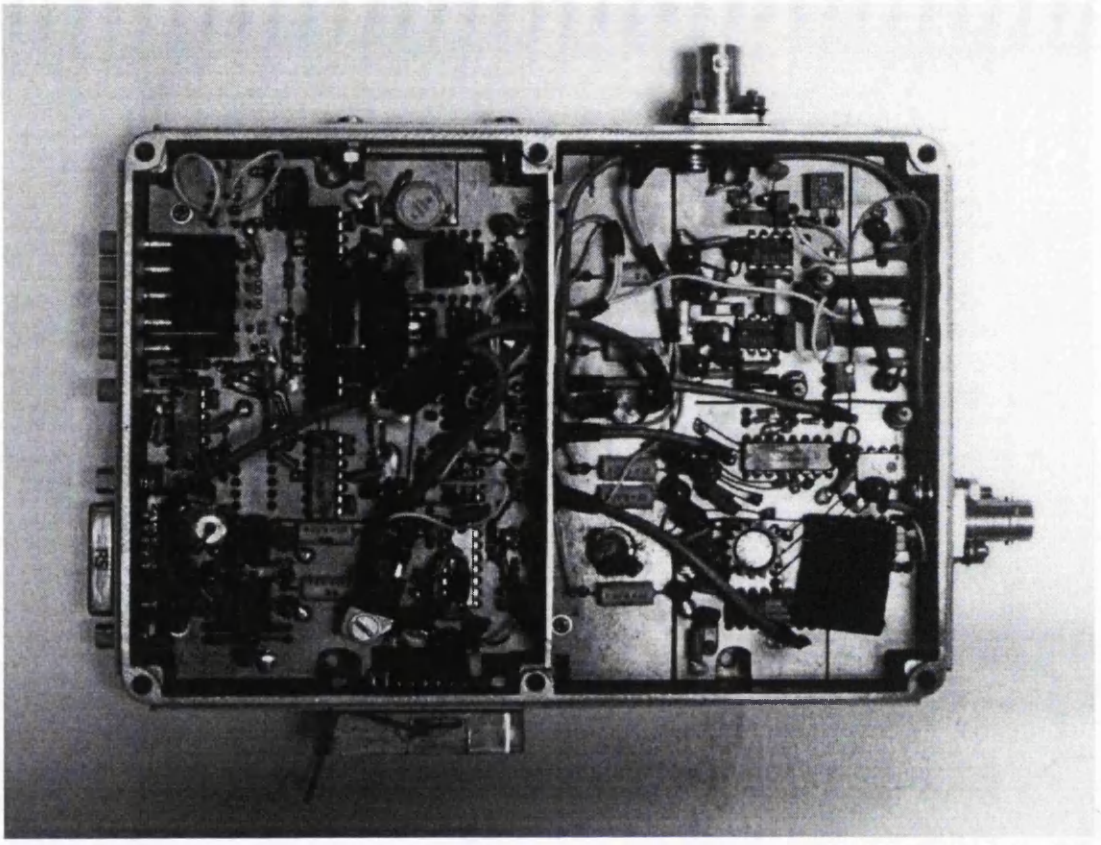

Figure 5.27: UCL SAAO preamplifier module.

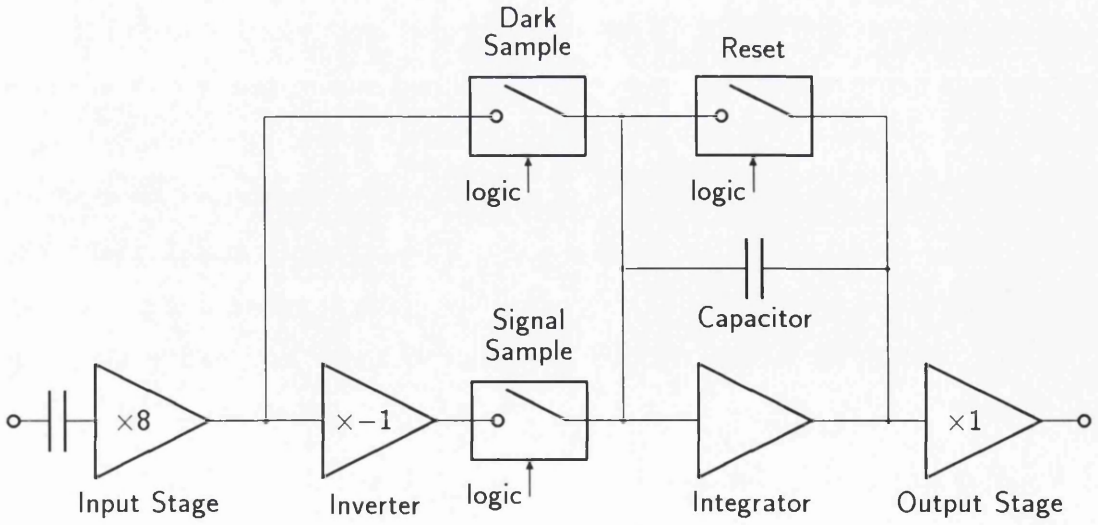

Figure 5.28: UCL SAAO preamplifier circuit schematic. Courtesy W. Han.

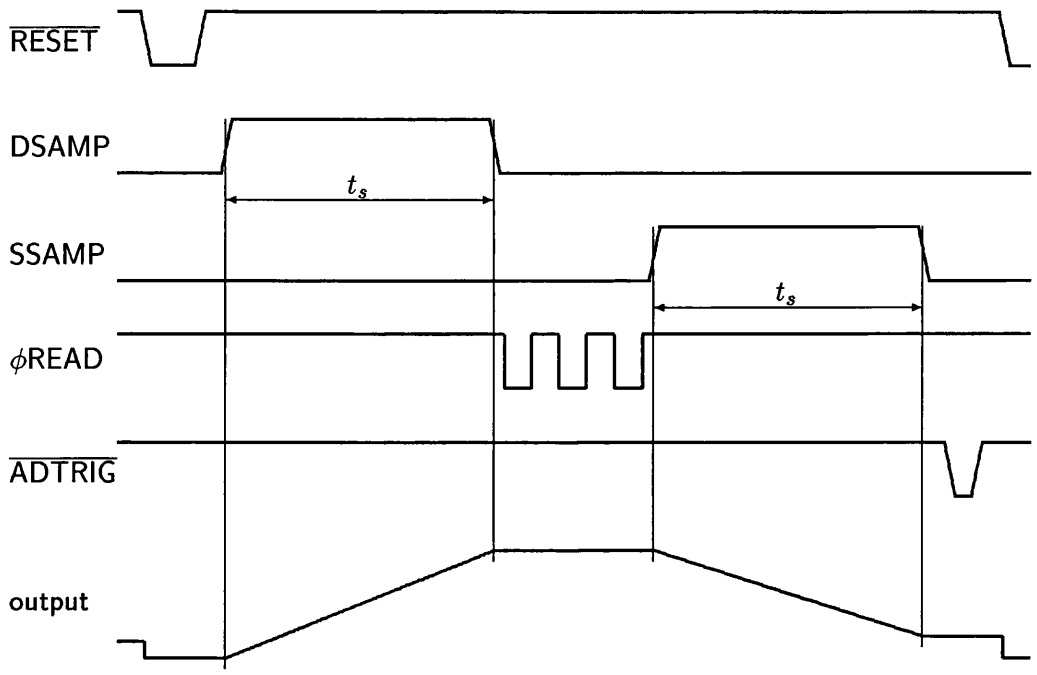

Figure 5.29: Preamplifier control timing.

stage is supplied with a reference bias voltage from the TTL-power section (the video reference) which is used to set the integrator ramp height. The gain of the input stage is typically $\times 4$, but can be altered by replacing the feedback resistor of the NE5534AN.

The input stage feeds two circuit paths, one of which contains an inverting, unity-gain buffer. The input and feedback resistors of this buffer form a matched pair to accurately fix the gain at -1 in this path. A second bias voltage, divided from the video reference is supplied to the input of the inverter, and is used to set the output voltage level for a zero-light signal. The complementary normal and inverted signals from the input stage of the circuit are fed to the integrator through the two halves of a dual-channel analogue switch, Intersil type IH5143CPE. A second dual analogue switch provides a reset to discharge the integrated signal from the integrating capacitor, and one switching channel is unused.

The output from the integrator is buffered via an LH0002 IC and fed through a coaxial cable to the digitiser module. A 39Ω resistor is put in the signal path to correctly terminate the cable at the amplifier end.

Figure 5.29 shows the sequence of the control signals for operating the integrator. The

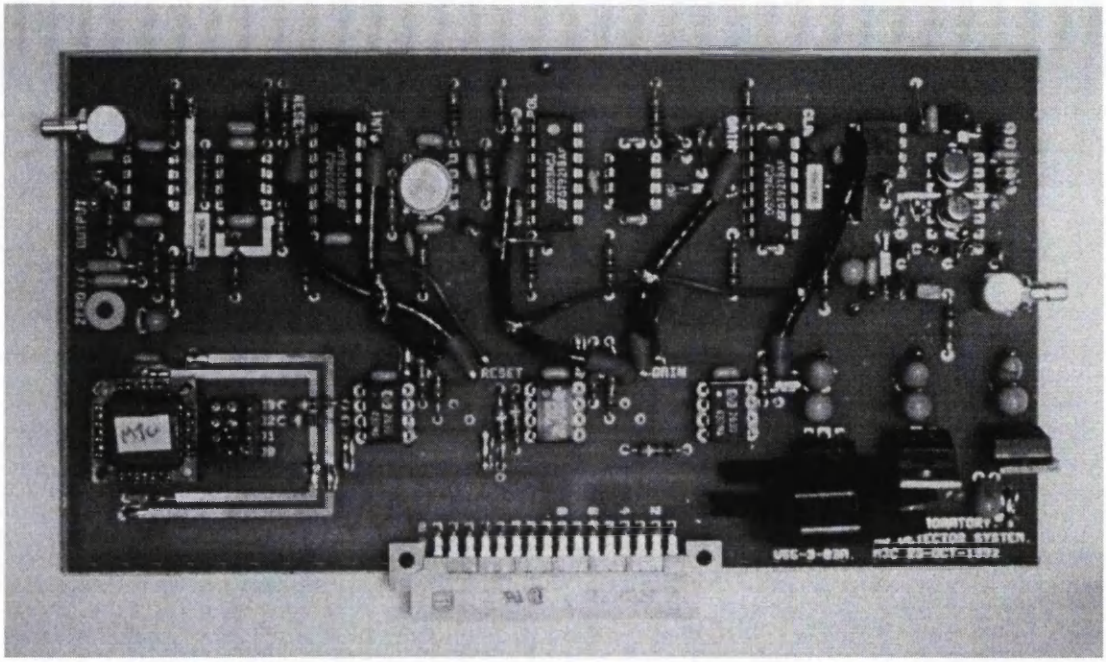

Figure 5.30: OSL preamplifier module.

sequence runs as follows. The integrating capacitor is discharged by the RESET signal. For a time t_s the voltage at the output node of the CCD is sampled with a gain of $+1$. This is triggered by the DSAMP signal. The CCD readout register is then cycled once to move a signal charge packet on to the output node. The voltage is again sampled, this time with a gain of -1 triggered by the SSAMP signal. Once this sequence has completed the preamplifier output carries a voltage proportional to the CCD signal. The digitiser is then triggered and the sequence can then be repeated.

5.9.2 Multiple CCD Testing

A completely new preamplifier/sampling circuit design was developed, based upon the Leach SDSU board. Figure 5.30 shows one of the completed boards. Two such boards were constructed to allow data acquisition from two detectors operating in parallel. Figure 5.31 shows boards connected to their common logic and power supply bus. The input signal arrives at the gold-coloured miniature BNC connector at the right in the figure. The detector load is a 20kΩ resistor and the signal is AC coupled to a version of the Janesick/JPL preamplifier. The signal is then progressively amplified and correlated double sampled. The output appears from the second BNC connector at the left in the

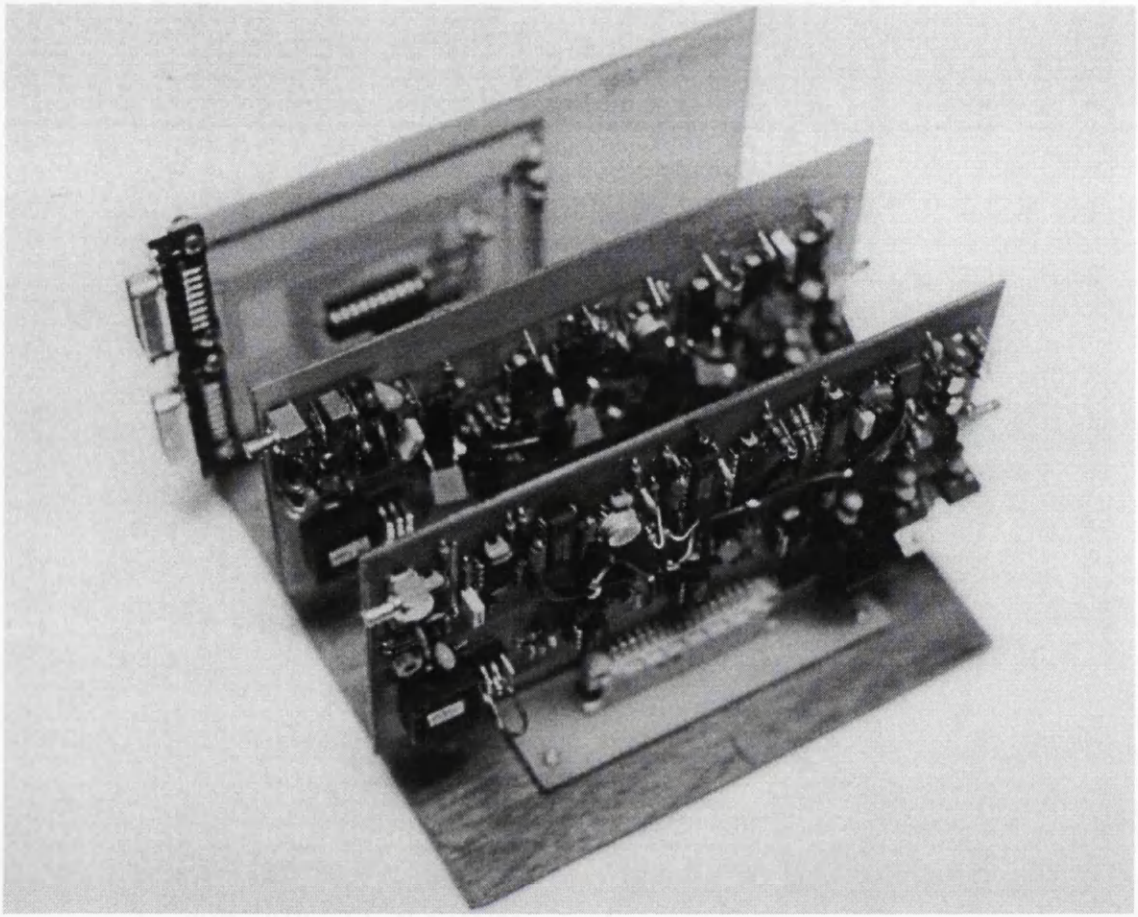

Figure 5.31: Preamplifier modules on their backplane.

figure. The lower part of the board is occupied by power-supply regulators, logic control (a single EP5032 PLD) and opto-isolators. A single half-length DIN41612 connector is used for power supply and logic signal input.

A simple multiple-preamplifier backplane was built to support up to four of these modules, though only two are currently used.

Figure 5.32 shows the circuit of the preamplifier and dual-slope integrator. The circuit has five sections: the input stage (preamplifier), selectable gain stage, polarity reversal buffer, integrator, and output buffer. The input stage is the Janesick/JPL preamplifier (McLean[124] p. 156). The detector output signal is AC-coupled to the preamplifier. When this circuit was adopted the constant current source head circuit previously described was no longer used. Instead a simple load resistor situated at the preamplifier board is used. The preamplifier gives a $\times 10$ gain to the AC component of the input

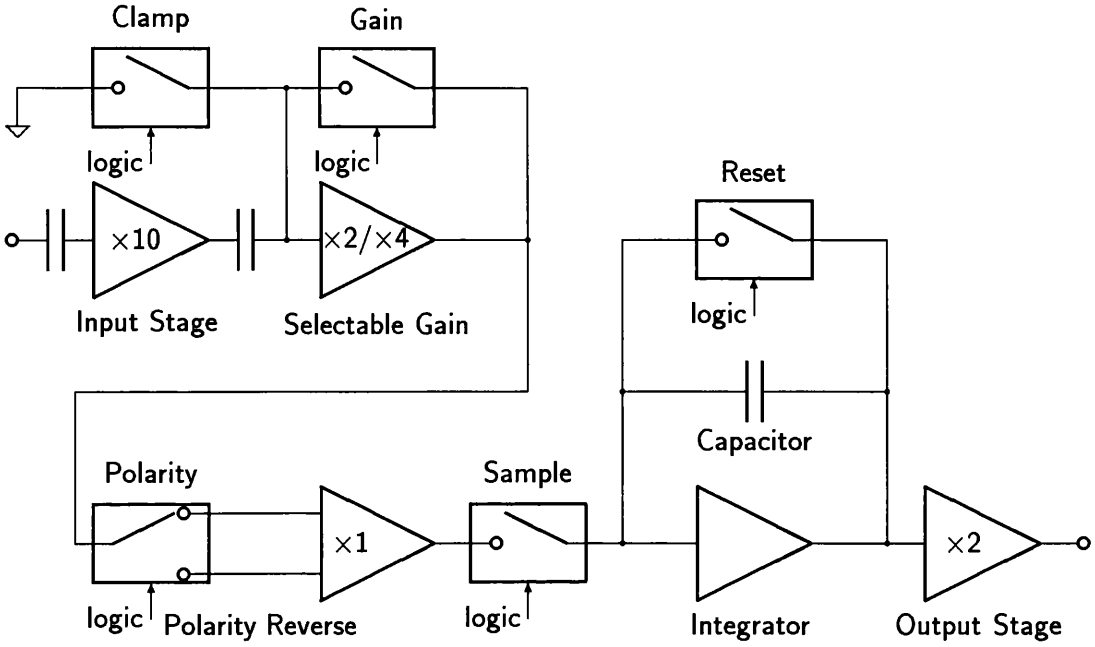

Figure 5.32: OSL preamplifier circuit schematic.

signal which is again coupled to the subsequent circuitry.

The signal passes through a simple op-amplifier buffer giving a selectable gain of either $\times 2$ or $\times 4$. The gain can be set by the controller programme or wire-wrapped to fix either state in hardware. A zero clamp is used at the input of this stage to keep the signal close to ground by referencing to ground prior to each double sample.

The polarity-reversal buffer allows the signal to pass through a unity gain or unity gain-inverting buffer by reversing the signal connections to a single op-amplifier. A standard integrator with a reset switch is used to achieve correlated double sampling. The integration time is set by the 'sample' logic signal. Finally, the signal is buffered to a digitiser by the output stage which gives a gain of $\times 2$.

The sequence of control signals required to operate this preamplifier is essentially similar to that for the UCL SAAO preamplifier. The minor differences are: that the RESET signal is also routed to the zero clamp (in practice two bits of controller memory containing identical information are used); and that the DSAMP and SSAMP signals are replaced by the polarity and sample signals—the polarity selects between the two sample modes, the

sample sets the time of integration. A more significant operational difference between the designs is the addition of a board base address as set by wire-wrapped inputs to on-board PLD. These control signals are sent from controller memory and allow for up to 16 such preamplifiers to be operated together.

5.9.3 Functional Testing

Both preamplifiers were found to perform correctly after minor modifications to the timing data supplied by the controller. The polarity of the DSAMP and SSAMP signals of the UCL SAAO version were originally found to be wrong, giving rise to a an output signal which had the correct shape (as in Figure 5.29) but was of the wrong polarity, *i.e.*, the signal was least for greatest signal from the detector. This problem was located by a systematic investigation of the amplifier in use. The circuit of the OSL preamplifier had to be modified slightly when it was found that the switches selected had to be operated from split power supplies rather than the single supply adopted to simplify the design. Noise testing and linearity data for both preamplifier designs can be found in Section 6.2.2.

5.10 Digitiser Submodule

This section describes the prototype digitising submodule. The submodule handles data from only two detectors; however, the design is very similar to the general specification given in Section 3.6.

The heart of this part of the system is an Analogic AM40016 Sampling ADC (see Section 3.6.2).

5.10.1 Prototype Specification

The prototype digitiser is designed not only for image data aquisition, but also to be useful for several performance tests of the Mosaic CCD System.

The prototype is designed to achieve the following specification:

- Fast aquisition time, sufficient for eight CCDs running at individual pixel readout

rates of 50kHz.

- No contribution to system noise beyond quantisation noise.
- Cycle trigger either from module controller or from LIM.

The major part of the general specification not implemented in the prototype is the multiplex of signals from more than two output-processing submodules. Data may only be acquired from at most two detectors at a time.

5.10.2 Hardware Description

The prototype digitiser module is shown in Figures 5.33 and 5.34. The board is mostly constructed by wire-wrap, although many of the power-supply components have been soldered in to place to achieve better noise rejection (by use of lower impedance wiring). The main component on the board is the AM40016 sampling analogue-to-digital converter. The module (M1) has a maximum sampling time of 2μS and accepts unipolar input in the range 0V to +10V.

The board has twenty-seven ICs: 10 TTL, 9 Opto-couplers, 3 analogue switches, one PLD, and 4 Power supply regulators. The four power supplies required by the AM40016 (+15V, +5V, −6V, −15V) are all generated on board by integrated-circuit power-supply regulators (U18–U21). Apart from decoupling capacitors, the ADC is the only component on the board-generated power supply rails. Digital connections to the ADC are made via the 7 type-2630 dual opto-couplers (U11–U17). U5 and U6 are monostable multivibrator ICs type-74121. U5 generates a pulse suitable for correct triggering of the ADC (the trigger pulse must be between 150nS and 200nS in duration), from external ADC trigger pulses. The ADC trigger pulse is carried by the IRQ7 pin of the VME backplane (Connector T1, pin 24b). U6 expands the 175nS 'Transfer' or EOC pulse from the ADC to a sufficient duration that the LIM can detect each datum.

The PLD E1 is used to control the analogue switch timing. The switch control signals are buffered though the remaining two opto-isolators (U22 and U23). Of the four miniature BNC connectors one is not used, one is used for single-detector data acquisition and the other two for dual-detector data acquisition. The three switches S1–S3 are of type DG200A which are dual SPST CMOS analogue switches. Two of these are used to

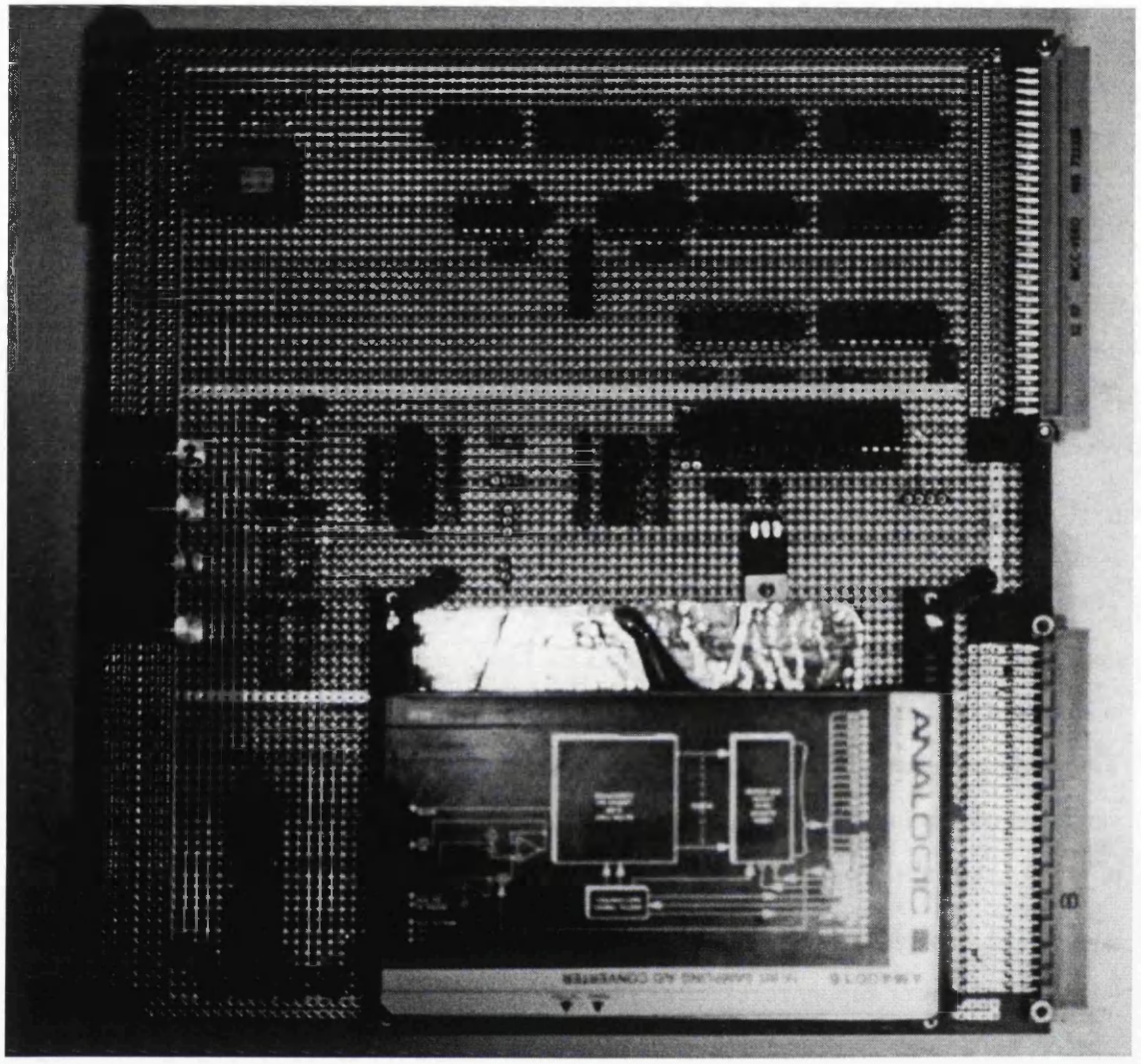

Figure 5.33: Prototype digitiser module.

switch the detector output signals and references, while the third is used to clamp the ADC module input buffer to ground between each input datum. When the system is configured for data acquisition from only a single detector the analogue switching circuit is disabled. Figure 5.35 shows the control signal sequencing for dual-detector data acquisition. Two inputs from the controller, CHANNEL and TRIG, are used by the PLD to generate the analogue switch sequencing, in combination with the system clock at backplane pin 16b. The length of the switching pulses for S1 and S3 t_s and that of the ADC trigger pulse delay t_d are set by wire-wrapped jumper fields J1 and J2 on the board.

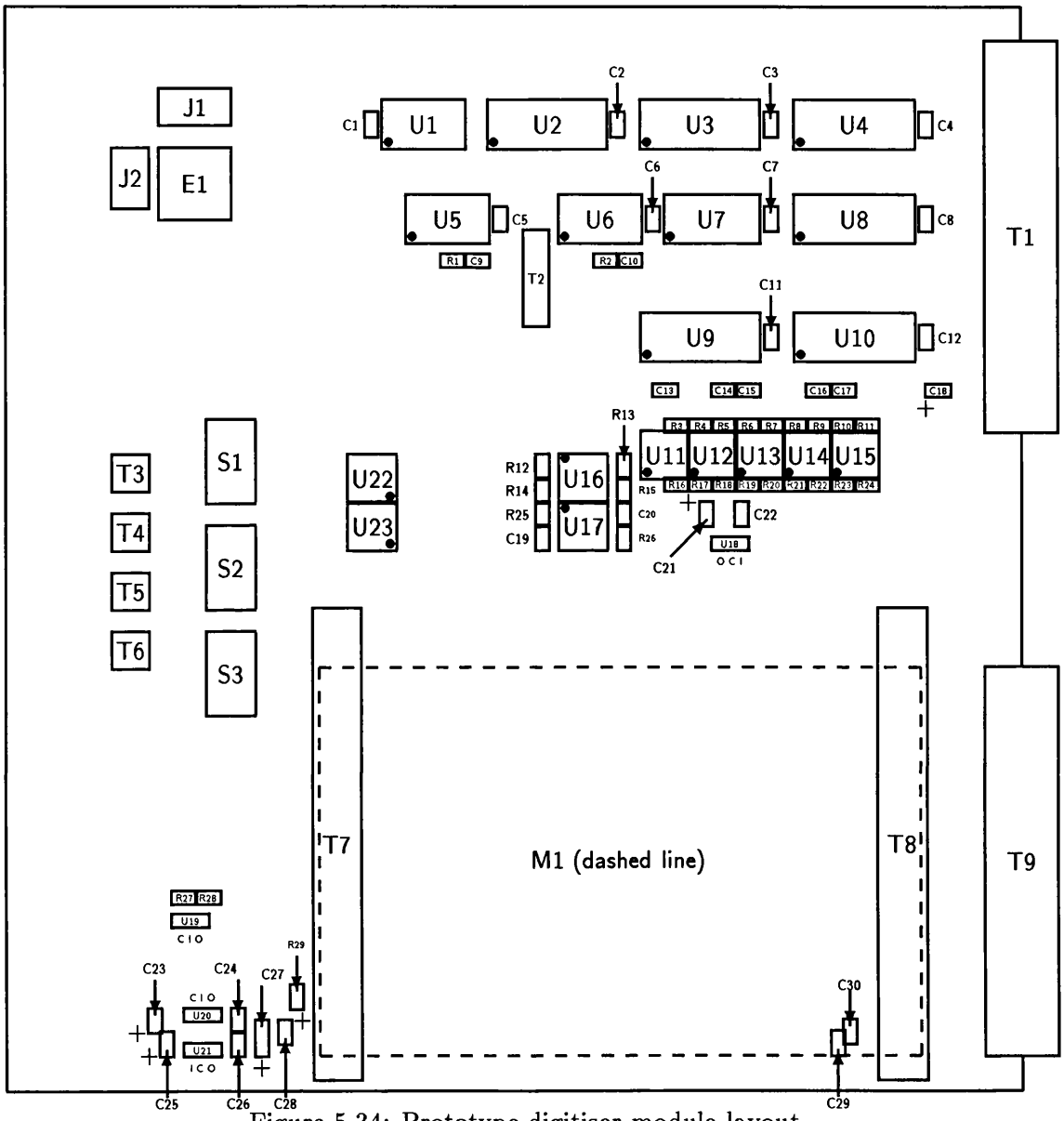

Figure 5.34: Prototype digitiser module layout.

The sample time t_s is set to be sufficient to allow for the approximately 1μS switch-on time of the DG200A plus the maximum 2μS conversion time of the AM40016. The ADC delay t_d is set to allow for the switch-on time of the analogue switches.

The remaining ICs deal with buffering of digital information to and from the rack backplane, board selection and address decoding.

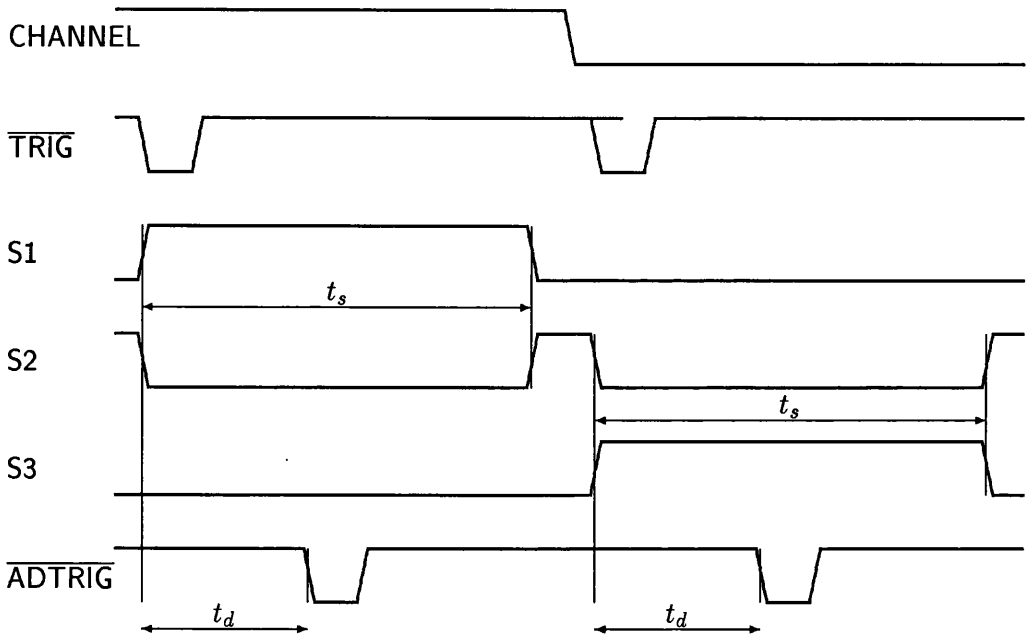

Figure 5.35: Analogue switch control timing.

5.10.3 Prototype Verification

Simple operational testing of the digitiser by connecting the input to a variable voltage source proved successful, *i.e.*, the mean digital number for each input was in close agreement with the expected value. The ADC full scale of 0V–10V at the resolution of 16 bits means that each bit represents about 152μV at the input. With no connection to the digitiser (the ADC input is effectively grounded through the cable-termination resistor R29) a standard deviation on the input signal of $\approx$0.6DN was observed. This is in good agreement with the expected value due to quantization noise only.

Chapter 6

System Performance: Evaluation Methods and Results

6.1 Introduction

The most important parameter of the Mosaic Imaging Detector System to be measured and optimised is instrument read noise—one of the system design goals being that dynamic range and noise performance should not be compromised by the presence of many detectors operating together. Another important aspect of the system to investigate is detector-to-detector cross-talk, the ultimate goal in this case being zero cross-talk.

The measurement of noise and cross-talk, and the achievement of acceptable performance levels in both cases are vital to proving the technology developed. In this Chapter results of system-performance tests are described along with experimental techniques and system improvements made during the experimental phase of the project.

6.2 Noise Testing

When the first fully assembled prototype of the MIDS modules was assembled, the initial noise level found was of the order of $180e^-_{rms}$. A significant amount of effort was expended on improving many aspects of the analogue design of the circuitry, particularly in respect of the CCD bias levels. Grounding and shielding strategies throughout the system were carefully investigated, and sources of noise systematically removed from the design.

The initial tests of the system involved simply grounding the input of the digitiser module to obtain a flat, zero-volt signal from the ADC. It was quickly established that the grounding strategy here had to be improved as a system noise of several ADU was discovered. An effective quantization-level noise of ≈ 0.6 ADU was obtained after implementing simple modifications.

6.2.1 ADC Code Probability

During investigation of the digitiser board and its noise pick-up it was found that occasionally an abnormally low spread of values was obtained. For example, a CCD frame-sized sample might give a standard deviation of about 0.5 ADU. Further investigation revealed that this was often related to particular mean levels in the ADC output signal. To check the general probability of bit combinations in the output of the digitiser the following simple test was performed. A reasonably "noisy" DC voltage was connected at the input of the ADC and a set of 1 million samples of the voltage taken. A histogram plot of code-occurrence versus code was then made. A fairly smooth Gaussian distribution is expected, with small fluctuations and no systematic patterns.

In fact a departure from a Gaussian distribution was found, with code probability either side of a bit-4 change-over being altered. The effect being that the lower code probability is slightly augmented whilst the higher code value is diminished by an amount roughly equal to the "missing" values in the lower code. The effect is estimated to be that the codes are about 5% more (or less) probable than they should be for this type of experiment. Figure 6.1 illustrates the results of one of these investigations.

In practice, this discrepancy does not effect the statistical tests required for device noise measurement to a significant extent. As long as the noise value to be measured is significantly greater than 2 ADUs there is not a problem. Indeed, the effect was only just noticeable even for a grounded input to the digitiser board.

The likely cause of the code probability problem is a damaged ADC module. An accidental insertion of the module with incorrect polarity in its ZIF socket effectively disabled the ADC; however, with careful "surgery", parts from an earlier (completely unrecoverably damaged) module were transplanted into the faulty module and function restored. The imperfect tuning of the module to the replaced part (digital buffer and interface logic) is

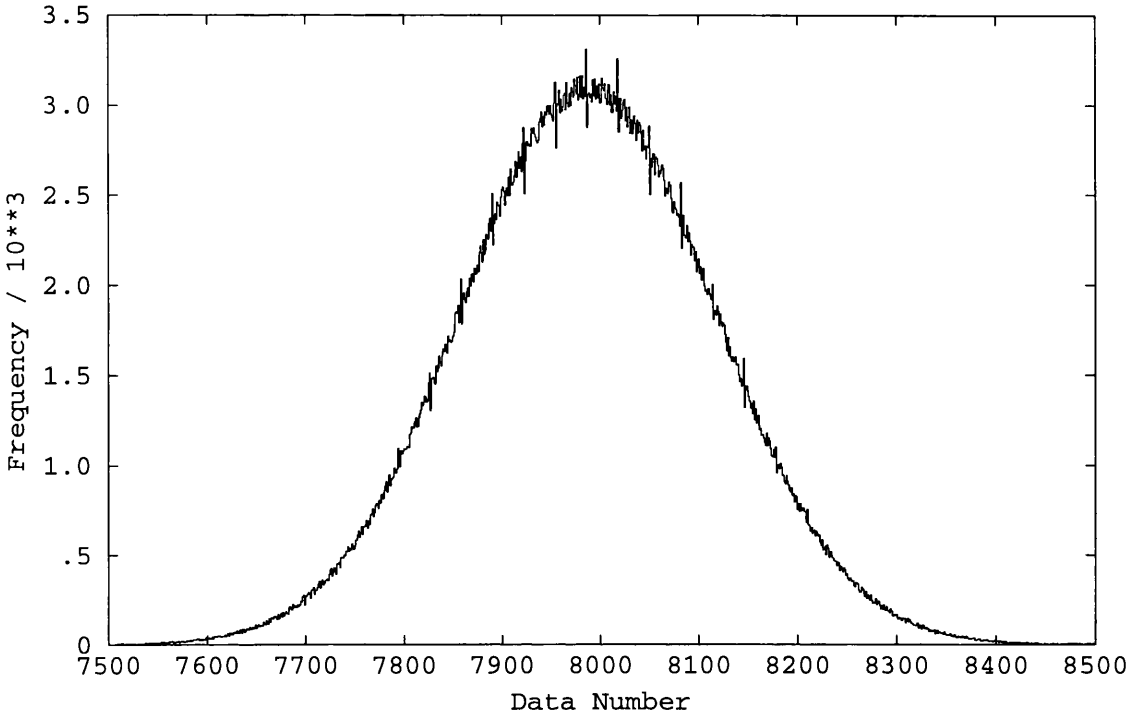

Figure 6.1: Typical ADC output statistic.

the probable cause of the code probability variation.

6.2.2 Preamplifier Characteristics

The next stage in testing was to ground the input to the preamplifier and correlated double sampler and obtain frame-equivalent datasets. The UCL SAAO preamplifier exhibited a roll-on level shift lasting for perhaps a quarter of a second. This was a known effect from the original system, in that case overcome by inhibiting the first vertical transfer of a readout for about half a second. This delay allows the output level to stabilise. The effect was present in both the DC- and AC-coupled versions of the amplifier. In the expected gain configuration, giving a transfer function of ≈ 1.0 electron per ADU, the measured noise of this amplifier was 8–9e^-_{rms}. This compares to the measured noise of the laboratory UCL SAAO system of 6–7e^-_{rms}. The difference probably arises due to the differences in the system designs—the amplifier was not optimised for an AC-coupled connection; also the unused bias-level supplies remained present, parts of the circuit being required for operation of the amplifier itself.

The new preamplifier design (see Section 5.9.2) performed better. Initially, in the same

gain configuration as the UCL SAAO module, a similar noise level was observed. Careful uncoupling of the circuit components traced the noise source to a single operational amplifier. The guilty component was replaced with a similar-specification part with a metal case. The effect on observed noise performance was dramatic, with signal noise dropping to $\leq$3 ADU. This translates to the equivalent of $3e^-_{rms}$ at the CCD output node. Although this level of noise performance is acceptable for the CCDs available to the project (intrinsic device output node noise $\approx 7e^-_{rms}$) it is higher than hoped, indeed it is higher than the original implementation of the circuit in the San Diego State University System[113]. The likely reasons for this discrepancy are discussed later (see Section 6.2.5).

The method used to measure the gain in the preamplifiers was to use a single-slope integration of a stable, measured voltage at the input node. This uses the simple equation

$$V_{out} = \frac{V_{in} \times t_{int}}{C_{int} \times R_{int}} \tag{6.1}$$

to relate the output voltage measured by the digitiser, V_{out}, to the input voltage, V_{in}. The approximate values of the integrator input resistance, R_{int}, and integrator capacitance, C_{int}, are known. By measuring the output voltage a simple check can be made that the expected gain is being obtained.

6.2.3 Analogue Driver Board Noise Sources

As described in Section 5.7.3, one of the major noise sources located was digital feed-through from the analogue clock waveform sources. This noise source was located after applying simple tests to measure noise levels in the bias sources. Each of the static bias levels used to operate the CCD was in turn channeled into the preamplifier input. During these tests the CCDs themselves were the only components of the system absent, the connection being made at the device socket in the cryostat.

The original test design did not incorporate any bias-level filtering. This was quickly revealed as a major noise source. Applying a range of capacitors to each bias-voltage source to give a wide frequency range of filtering effectively eliminated the noise as detected from this source. Typical system noise measured in this configuration was $\approx$5–$6e^-_{rms}$ equivalent. This level of noise in the bias levels reflects the inherent problems of constructing a four-CCD driver module by wire-wrap techniques. Achieving an adequate

ground connection throughout the board proved to be the main requirement for reducing this effect.

Experiments investigating the effect on bias level noise measurements with and without the CCD clock waveforms running revealed no significant cross-talk between clock signals and bias levels, whether intra-device or between devices.

Once the amplifier and digitiser noise levels and bias-level signals had been optimised the next stage in testing was to investigate possible noise sources in the system CCD clocks. This represents more of a challenge than filtering the bias levels as a wider frequency pass-band is required to achieve adequate clock rise and fall times and shapes. In practice, a higher level of signal noise in the register clocks (than in the bias levels) is acceptable as the level of feed-through from clocks to the output node is much less than for bias levels. Uncertainty in the reset pulse level is effectively removed by the correlated double sampler. However, as this clock runs physically closest to the output node within the device, careful investigation of the general noise level was carried out. Initially, the signal from a reset clock circuit was fed into the preamplifier module, as in the case of bias levels, the voltage level produced was held at a stable voltage. This revealed a high, though probably acceptable, detected noise level equivalent to $\approx 40 e^-_{rms}$. In practice this will lead to only a small effect in the CCD output noise as the feedthrough from the clocks is of the order of one part in 500[7]. Nevertheless, filtering circuitry was introduced to limit the frequency pass band at the high end for the clocks. Filtering (particularly of the reset clock) was applied at increasing levels of capacitance until just before a degradation of clock transition-edge quality could be see on an oscilloscope. For the vertical clocks the large capacitance of the CCD itself acts as a very effective filter (this being one reason why the noise feedthrough is so small). Some extra filtering was added to the horizontal clock signals.

The next step in system testing was to assemble the complete system and perform accurate system-noise measurements.

6.2.4 The Photon-Transfer Technique

This is a well-documented method for calibrating the transfer function of a photon-detection system. In general terms, the photon statistics of the incident light (and their

appearance in the output signal) are used to determine the relationship between the output signal in digital numbers (DN)[1] and the CCD output signal in electrons. The technique also gives a measure of the overall system noise.

There are several detailed descriptions of the photon-transfer technique[89][124][126]. The method is also known as the *mean-variance test.*

The data recorded on the LIM is in the form of a two-dimensional data frame, each pixel in the CCD Mosaic being represented by a two-byte unsigned number (*i.e.,* in the range 0–65535). This represents the output voltage from the ADC for each pixel. The ADC output is essentially linear to a fraction of a DN and there is a small zero-offset so that zero volts input to the ADC will produce a small positive integer output (typically 50–200 ADU).

The recorded signal S_o (in DN) is related to the charge detected N_e (in electrons) by the equation

$$S_o = G \times N_e + b \tag{6.2}$$

where G is the system transfer function or gain and b is the bias signal for zero detected charge, part of which is the ADC offset described above.

The transfer function can be determined in two ways. The first method is to calculate G using a detailed knowledge of the amplifier circuit design and measurements of the CCD output-node capacitance. In practice, this method only serves as a guideline estimate of system gain as the precise values of circuit components will be different from their catalogue values. The second technique is to collect a series of observations of a uniformly illuminated scene with different mean signal levels and to study the photon statistics of these observations.

In practice a series of observations is collected, each of a different light level. The individual observations are flat-fielded and bias subtracted. The bias level was estimated by over-scanning the CCDs, selecting a region in the over-scan and taking its median value as the bias. The size and shape of the over-scan region and the region within the detector imaging area were carefully matched. A 'clean', *i.e.* blemish-free, region of the detector was selected for the experiments. Flat-fielding was achieved by using the

[1]DN are variously known as data numbers, digital numbers and analogue-to-digital units (ADU), all are equivalent in meaning.

mean, dark-subtracted signal at each light level. The mean signal for each observation was taken as the average of the two exposures at that light level. The standard statistical techniques applied to the data to arrive at the mean, S_m, and variance, V_m, values were

$$S_m = \sum X_i/n \tag{6.3}$$

and

$$V_m = \sum (X_i - S_m)^2/(n-1) \tag{6.4}$$

where the summation is over all n pixels in the selected image region.

The observations should contain two noise sources: the readout noise from the CCD output amplifier and attendant processing electronics, R; and the photon 'shot' statistical noise of the signal photoelectrons, p. It is worth noting that the effect of signal from non-photon sources; for example dark current, is included in the shot noise.

The two noise sources add in quadrature to the total noise, n_e

$$n_e^2 = p^2 + R^2 \tag{6.5}$$

The units of this equation are numbers (of electrons). By multiplying equation 6.5 by G^2 on both sides we obtain

$$(G \times n_e)^2 = (G \times p)^2 + (G \times R)^2 \tag{6.6}$$

Using the Poisson photon-noise rule

$$p = \sqrt{S_m/G} \tag{6.7}$$

as the photoelectron signal count uncertainty is simply the square root of the photoelectron count, which is the mean signal in DN divided by the photon-transfer function G. Rewriting equation 6.6 with the left hand side equated to the signal variance (it is simply the product of the system transfer function and the total noise, squared)

$$V_m = G \times S_m + (G \times R)^2 \tag{6.8}$$

This is a linear equation in S_m and V_m with gradient G and intercept $(G \times R)^2$. The quantities S_m and V_m are the observed means and variances of the experiment. The equation shows that the variance of a signal is proportional to the signal level. In practice

this is why measurements at a series of signal levels are taken. A graph of means versus variances of this series of observations will give a direct measure of the gain (gradient) and subsequently of the system readout noise, R as this can be calculated from the intercept of the graph $(G \times R)^2$. This graph gives the experiment its "mean-variance test" name.

6.2.4.1 Implementation Details of the Photon-Transfer Test

To achieve an even illuminated field an approximate point source was used, in practice, an ordinary LED with a pin-hole mask. By positioning the point source a sufficient distance from the CCD an effectively flat-field is achieved. During these experiments the distance used was of the order of two meters, giving a flat-field of less than 0.1% non-uniformity. The stability of the light output level from the LED was not investigated. In practice it was found that repeated exposures for the same time period produced signal level variations due to statistical effects as expected, *i.e.*, the effect of uncertainty in flux level is not any greater than other sources of uncertainty in the experiment. This is due to the nature of the test.

The exposure time was controlled by the LIM. The internal operating system clock was used. This gives the time (in the software implementation used) to an accuracy of about 32ms. To minimise errors in the exposure time, intervals greater than 5 seconds were usually employed, giving an uncertainty of 0.6%, improving as the exposure time increases. The actual exposure control was implemented by switching on and off the LED rather than using a shutter. This method does have some disadvantages in that the CCD remains exposed to any stray light between exposures. To minimise these effects great care was taken to ensure that the darkroom used for the experiments was thoroughly light-tight. In addition, a simple cardboard tube, painted with matt-black paint was used as a baffle in front of the cryostat window. This limits considerably the solid angle through which the detector is exposed to stray light. Some longer "dark frames" (*i.e.* longer than the exposure times used) were taken in this configuration to ensure that any light leaks were not detectable.

A `DMAP` command procedure based around several `DMAP` macros was created to manage the exposures in an automated fashion. Each complete experiment would be run from the command procedure which would contain of a list of exposure times. The macros

then manage the acquisition of frame pairs and the calculation of mean values as well as flat-fielding and bias subtraction. At the end of a run a simple unweighted least-squares fit algorithm is used to obtain values for the system transfer function and noise. These figures, along with the individual exposure details are tabulated and written to a text file for later analysis.

Prior to a run the experimenter selects two regions of a test image to be used as the data and bias sets. The analysis software consists of a small suite of programmes, each stand-alone, which interact via simple text messages written in one-line disk files. Available utilities include a region and dataset based image calculator allowing for scalar add and multiply as well as image add, subtract, multiply and divide. When a region of an acquired data frame is selected for analysis the data are converted from 16-bit unsigned to double precision floating point prior to any processing.

In the laboratory, the image display device was placed outside the darkroom to monitor the progress of an experiment. Each image was displayed with image and overscan statistical data.

6.2.5 Device Output Processor Transfer Function & Readout Noise

Table 6.1 shows the output from a typical run of the transfer-function procedure. The first column is the exposure time in seconds. The second to fifth columns refer to the first exposure (A) of a pair. These figures are: the mean level in the selected region of the image, the standard deviation in that region, the mean level in the selected region of the overscan and the standard deviation in that region. The sixth to ninth columns refer to the second exposure of a pair (B), with the columns ordered as for exposure A. The tenth column is the mean bias-subtracted field value. The final column is the variance of the difference of the A and B images, when subtracted on a pixel-by-pixel basis, this value is further divided by two, reflecting the quadrature addition of signal noise in the two images.

The fit data given at the bottom of the table is for an unweighted linear least-squares fit to the mean (x) and variance (y) data. The method used was

$$m = \frac{N\sum x_i y_i - \sum x_i \sum y_i}{N\sum x_i^2 - \left(\sum x_i\right)^2} \tag{6.9}$$

Optical Science Laboratory. Mosaic Detector Project.

DMAP Automated Photon Transfer Test. File: mv.log.

Test carried out by: W. HAN.

Test date: Mon Dec 14 17:43:13.370 1992.

Exposure Data:

Time	A				B				Mean	$\sigma^2/2$
/S	Image	σ	OS	σ	Image	σ	OS	σ	(x)	(y)
2.0	784.6	17.3	380.5	8.4	776.3	17.2	380.4	8.3	400.0	231.06
4.0	1116.1	25.0	380.2	8.6	1115.0	24.9	380.4	8.4	735.2	374.39
6.0	1465.7	33.3	379.8	8.7	1462.4	32.8	379.8	8.6	1084.3	557.85
8.0	1795.8	40.7	380.7	8.8	1793.6	41.4	380.4	8.4	1414.2	767.14
10.0	2135.4	47.9	380.8	8.4	2129.4	47.7	380.4	8.4	1751.8	826.90
12.0	2480.0	56.8	380.0	8.7	2487.3	57.3	380.6	8.9	2103.4	1012.91
14.0	2824.1	64.8	380.9	8.7	2818.6	64.1	380.9	8.8	2440.5	1086.43
16.0	3164.8	72.7	381.4	8.4	3166.1	72.4	380.6	8.5	2784.4	1304.53
18.0	3508.3	79.2	381.5	8.3	3505.7	81.3	381.0	8.5	3125.8	1504.81
20.0	3833.5	89.9	382.3	8.6	3835.4	90.1	382.7	8.6	3452.0	1755.46
22.0	4177.5	96.4	383.2	8.6	4181.5	96.4	382.8	8.4	3796.5	1795.26
24.0	4536.6	104.3	382.1	8.6	4523.7	104.8	383.1	8.3	4147.6	1926.59
26.0	4881.8	113.0	382.6	8.5	4871.9	113.2	383.0	8.5	4494.1	2221.11
28.0	5208.6	119.7	383.0	8.4	5213.1	119.0	383.4	8.6	4827.7	2241.69
30.0	5562.6	126.4	383.2	8.5	5552.5	128.4	383.0	8.8	5174.5	2410.75

Unweighted least squares fit data:

Solution to y = mx + c is c=45.85 ($\sqrt{c}$=6.77) m=0.46, correlation=0.997.

Referred to the CCD output node:

System transfer function: 2.16 electrons/ADU.

System noise: 14.618 electrons.

Table 6.1: Typical photon-transfer test result.

where N is the total number of exposure pairs and

$$c = \frac{\sum x_i^2 \sum y_i - \sum x_i \sum x_i y_i}{N \sum x_i^2 - (\sum x_i)^2} \tag{6.10}$$

in the equation for the best fit line

$$y = mx + c \tag{6.11}$$

The correlation figure quoted is a measure of the goodness of fit. This figure ranges from $+1$ to -1, more positive values suggesting direct correlation, negative values inverse correlation. Values close to zero suggest poor correlation between the two variables. This correlation figure is calculated by

$$corr = \frac{N \sum x_i y_i - \sum x_i \sum y_i}{\sqrt{N \sum x_i^2 - (\sum x_i)^2} \times \sqrt{N \sum y_i^2 - (\sum y_i)^2}} \tag{6.12}$$

At the time of writing the quoted noise figure of $\approx 15 e^-_{rms}$ is close to the best figure achieved in any photon-transfer test run with this system. Each module of the system has been evaluated as a possible noise source and carefully investigated. The figure remains poor compared to the manufacturers measured noise level of $\approx 7 e^-_{rms}$, reflecting several problems which remain in the prototype system.

The largest single noise source remaining is likely to be the data acquisition link to the LIM. During system debugging it was noted that when observing the preamplifier output (with an oscilloscope) and **not** acquiring data the trace appeared distinctly 'cleaner'. This suggests that the extra digital activity during data acquisition is feeding into the detector output at some point. This observed extra noise is most likely due to a varying phase relationship between the digital timing of the acquisition system and the controller module. In the development system the EOC pulse from the ADC is detected in software by polling the appropriate address of the digitiser module. This means that the timing of acquisition of a particular datum is not locked to the EOC but can vary depending on the relationship between the software loop time and the pixel time of the controller. Indeed, at the best noise-performance level a modulation pattern of frequency 1890 Hz was visible in some dark images at an estimated peak-to-peak level of 5–10 ADU. Subjective assessment of the acquisition data link—via an unshielded ribbon cable driven by opto isolators—suggests that this is not the best implementation of the data acquisition system.

It seems likely that the presence of this digital feedthrough is also an important source of the excess noise found in the preamplifier (over that expected for the design). It is hard to estimate its contribution to the total noise, simply because the data acquisition system has to be active to measure the noise level.

The majority of transfer-function measurements were made with only a single detector present and active in the cryostat. Dual-detector tests were undertaken to confirm that multiple devices can be run without any detectable noise-performance cost.

6.3 Cross-talk Between Detector Channels

To assess the level of inter-device signal cross-talk a simple experiment was performed. A dual-device set-up was assembled with one device masked to prevent illumination. The second device was partially illuminated using a mask with a (roughly) square hole. Data from the covered device only were acquired. Data from a region on the first device corresponding to the mask area on the second device with a suitable reference area (in practice a border around the mask region) were successively acquired and images added using the image arithmetic software available.

For a non-saturated signal from the second device, effectively no cross-talk signal was seen. A pattern, probably resulting from light-leakage and/or dark-current fixed pattern was observed to develop in the summed data. However, the pattern did not correspond in any way with the mask on the second device and was at a level to be expected from sensitivity variations in the CCD.

As the second device signal saturated the preamplifier/digitiser combination it became immediately apparent that a significant cross-talk effect *was* occurring. This experiment was conducted *without* using the switches on the digitiser board to ground-clamp the ADC input between successive conversions. Investigation showed that the saturation of one channel was causing a change in the current draw from the ground plane, leading to an effective voltage shift which the other device output channel was also seeing. Implementation of ADC input clamp-to-ground will assist in cross-talk rejection by ensuring that the input stage of the ADC is set to the same reference point before each conversion. The observed interference between pre-amplifier circuits which occupy the same ground

plane and are located in close proximity to each other is a more serious design flaw. One possible solution may be to implement a clamp switched by a comparator as part of the correlated double sampler to prevent the circuit going into saturation for large signal levels. This would effectively limit the signal level to be between the limits of each op-amp's output slew, leading to a prevention of the ground current problem.

6.4 Combining Images from Adjacent Devices

The current data acquisition implementation results in a device-multiplexed data stream to the LIM. This means that in the case of a dual-CCD system each alternate data point arrives from a different device. To retain compatibility with the existing software, both for image display and data acquisition, a post-acquisition demultiplex programme was written. This simple code reads the message file written by `DMAP` and then demultiplexes the acquisition system output which is written to a file at the end of a mosaic readout. After this process, the individual images can be displayed or, if desired, shifted on the display to correspond to their relative physical positions. In the laboratory system this display-mosaic feature was not needed. In practice a side-by-side display of output from two of the detectors in the cryostat is a useful tool for system testing, however, there was no need to align the displays as the images were often independent and also the inter-device gaps were larger than the devices' sensitive areas.

Chapter 7

Discussion & Conclusions

7.1 Introduction

A programme of research to fulfil aims described in Chapters 1 and 2 has been attempted. Many of the ideas proposed in Chapter 3 have been investigated, developed and proven. In this Chapter the extent to which the research goals of the project have been completed and the results obtained are discussed. The overall architecture of the system is reviewed in the light of these studies and proposals for continuation of the work are made.

7.2 Project Achievements

7.2.1 Project Targets

The original grant proposal for the Mosaic Imaging Detector System (MIDS) research project requested funding to construct a 2×2 CCD mosaic using television-format devices, the intention being to acquire a four-device image. Funding for data acquisition from only one device has been obtained. Summarising from Sections 2.4 and 3.2, the main project targets with the funding granted were:

- Devise a modular detector architecture, generalised for any application.
- Investigate solutions to the problem of assembling multiple devices in coplanar arrays.

- Investigate methods for overcoming inter-device gaps.
- Develop architecture for operating multiple devices in vacuo.
- Develop logic electronic architecture for control of a mosaic.
- Develop analogue electronic circuitry for operation of a mosaic.
- Investigate data-acquisition methods for large mosaics.
- Develop software for operation and characterisation of mosaics.
- Construct a demonstration system.
- Evaluate the demonstration system.

The extent to which each of these goals was achieved is now discussed. Other unexpected developments are also mentioned.

7.2.2 System Architecture

Extensive investigation of the requirements of, and available materials for, detector mosaics has led to an outline system architecture described in Chapter 3. Over the duration of the project these specifications required little alteration in the light of technological advance. Some new technologies and devices have allowed the easing of certain design constraints, however, for a generalised architecture such a relaxation is not possible.

7.2.3 Detector Coplanarity

The proposed use of diamond-turned spacers to correct for errors in the flatness of individual devices within a mosaic has not yet been investigated. It is expected that this will prove a simple part of the system development once use of the OSL diamond turning machine becomes possible. Currently, a new computer-control system of this machine is being constructed.

Alternative mounting strategies, for example using piezoelectric devices, have also been considered. For most applications this active element is unnecessary. However, for lightweight, space-based systems or as part of a system which has an overall active design, such

a mounting may be very useful. These devices have been used in numerous applications requiring high positional resolution and reproducibility.

7.2.4 Inter-Device Gaps

Alan Radley's work in the OSL[147] has proved the basic feasibility of refocus optics to overcome inter-device gaps within a mosaic. Further work is needed to optimise the throughput of the lenses, particularly in the areas closest to the device edges where the current design has a poor throughput.

7.2.5 Cryogenic System Design

The primary problem of lead-out wire routing for multiple devices within a single cryostat has been discussed earlier. This can be solved by using surface-mount modules to drive the focal-plane array. These surface-mount modules are housed within the cryostat physically underneath (or behind) the focal-plane array. The number of lead-outs can be reduced by orders of magnitude using this method. These drive modules will be placed in good thermal contact with the cryostat outer jacket to provide a sink for the heat they generate. This should limit the sources of heat load of the liquid nitrogen to that of heat conduction through connections to the array plus normal levels of radiative and convective heating. It is possible that demountable fibre-optic couplings could be used for all digital communication to and from the intra-cryostat electronics. This would reduce the heat load on the liquid nitrogen by cutting the number of good thermal conductors passing through the cryostat jacket. Developments such as the multi-phase pinned detector[154] may lead to higher operating temperatures for focal-plane arrays of CCDs becoming the norm in the future.

The mechanical design of the cryogenic chamber for large-area detectors is a problem beyond the scope of the research undertaken. Here, custom-built systems would probably be best for an astronomical application. There should be no problems in scaling designs for larger detector areas up to the sizes required for eight-meter-class telescopes.

7.2.6 Controller Design

The original PLD-based controller concept has proven highly successful. Two generations of controller architecture have been developed and proven in the laboratory. The design is compact, requiring only about eight components to construct a circuit to control between eight and sixteen detectors (the actual limiting number is determined by detector format and required readout modes). This design could be implemented in a surface-mounted PCB to achieve minimum size.

As discussed in Chapter 3, the PLD-based design is potentially faster than microprocessor-controlled designs as it uses the inherently simple PLD chip.

With a few enhancements, the basic controller design could be made generally useful for many control applications; *e.g.,* a project to use this controller architecture as part of a wavefront sensor is underway in the OSL. An earlier OSL project for control of an active mirror polishing lap which utilised a complex microprocessor-based controller has also benefitted directly from the bit-map approach.

An important aspect of optimising the use of these circuits is the use of the MIDS control programme `DMAP` which makes programming of the controller both simple and flexible, as well as scalable for large systems. No external dependence on compilers as for microprocessor-based systems is present in this design.

7.2.7 Analogue Driver Design

In practice the idea of a multiple-detector drive module has proved difficult to realise. The primary reason for this is the large number of components with many lead-outs being assembled in one wire-wrap or PCB circuit. The architecture of the mosaic imaging detector system lends itself to modulisation of the analogue circuitry on a per-detector basis. This has several advantages: in a real system the analogue electronics would be located within the cryostat and close to the focal plane array; a design with one analogue board per device is easier to assemble and maintain; the design of the circuit for one device is conceptually easier than that for n (this proved the main problem in circuit design and construction); and because each channel is on its own board an extra degree of inter-channel isolation is achieved. Unlike the controller design, no component-

count reduction is possible by controlling many detectors from one circuit board. Hence, in the analogue side of the design, integration of multiple-device driving circuitry is unnecessary. In practice there is only a very small saving in overhead (typically one piece of decoding logic per CCD integrated) when multiple detectors are driven from a single circuit analogue-circuit board.

From a different perspective the analogue design has been a success. CCDs have been driven with a compact and simple circuit design which is also inexpensive and contains few components. The prototype design utilises integrated circuits which are available in surface-mount packages and so the existing circuits could be very easily reconfigured for a per-detector, highly integrated surface-mount analogue-driver module.

7.2.8 Data Acquisition techniques

As in the analogue drive circuitry, there is no effective way to integrate the output processing systems for many detectors. One correlated double sampler is required for each detector. The laboratory prototype has proved reasonably successful. Again as for the analogue-driver module, the existing architecture is probably not ideal—the channels of separate devices are in close proximity at precisely the point where the signal is at its weakest and most sensitive to cross-talk. An architecture where the output processing circuitry is closely integrated with the analogue drive electronics, in particular the bias-level sources, and where each channel is realised on its own surface-mount circuit board would be preferable. The existing design can be optimised for surface-mount and constructed in a circuit small enough to be mounted behind a single typical 1000×1000-pixel detector within the cryostat jacket. This seems to be the most logical approach to the problem.

In the existing prototype a very fast ADC module has been employed. Signals from several devices (in the prototype only two) are multiplexed into this module. This has proven successful; however, careful attention has been paid to clamping the input to the digitiser between conversions and avoiding saturation of its input. In a practical system it may be less expensive to provide a single, slower digitiser for each detector channel. Such an architecture has the advantage that one detector can reach output-channel saturation without affecting adjacent channels. In practice it may be useful to be able to operate

only one or two detectors from the focal-plane array (per digitiser) at a faster readout rate, for example for a time-resolved observation. The single fast digitiser per n detectors is the preferred architecture in that case.

7.2.9 System Control Software

A very successful aspect of the project has been the control software. The high level of system-control flexibility and abstraction originally hoped for has been fully achieved. Unlike other multiple-detector control systems this one is programmed in a detector- and control-waveform-oriented manner, rather than in hexadecimal or machine language.

The control software has proven vastly useful in system testing and characterisation, where experiments such as operating the detectors with vertical or horizontal registers running backwards in response to "what if?" type queries has been routinely realised and with ease. This proved particularly useful during noise-source characterisation experiments.

The early specification of a portable control programme has been met; the pseudo-compiler parts of `DMAP` having been successfully ported to several operating systems (MS-DOS, VAX/VMS, Ultrix, OSF/1, P-DOS). This bodes well for the programme being used in a future upgraded development system.

7.3 Other Work in the Field

In recent years several groups have undertaken development projects for CCD detector mosaics. The most important of these projects have been directly associated with very-large-telescope projects; for example, the development of a 4k×2k pixel three-side buttable detector for use in Keck Observatory instrumentation[167] and ESO development of modular control electronics for VLT instrumentation[151]. Most of the work done has concentrated on specific areas of the technology: the detectors or the control electronics, rather than developing a generalised technology as in this work. Several of the papers describing mosaic projects acknowledge the necessity of multiple-CCD instruments to realise the full potential of the new telescopes.

7.3.1 Buttable Detectors

Several groups have used silicon foundries to manufacture custom-design CCDs specifically for the purpose of building close-packed detector mosaics. An important consideration in this case is the device yield. Luppino *et al* [120] have selected 2048×4096-pixel dimensions for the component CCDs (pixel size 15×15μm square) on the basis that this is the largest size of silicon area which will give a reasonable device yield at this time. Their design is based on a close-packed buttable detector mosaic with gaps of less than or about 1mm between individual CCDs.

At the time of writing most current work in mosaic detectors is focussed quite closely on the new generation of optical instruments being built now, rather than on a generalised mosaic-construction technology.

7.4 Design Changes & Future Objectives

7.4.1 Design Changes

In the light of the results obtained and considering the changes in available computing and detector technologies over the duration of this project, several modifications leading to improvements in the modular mosaic technology have become apparent.

The most important of these is the modularity or 'granularity' of the system. Originally it was envisaged that several detectors would be driven from a single analogue-driver module, and in turn perhaps several analogue-driver modules would be driven by each digital-controller module. On reflection, it seems likely that individual analogue channels are superior for several reasons:

- The design of each module is simplified—routing the connections between the components for two channels on a single board leads to about a factor 1.5 increase in the complexity of board layout. Use of multilayer PCBs would alleviate the problem for 'few'-detector cases. However, ultimately the same layout difficulties will be met, even for perhaps as few as sixteen detectors. This defeats the goal of controlling many detectors from a single analogue circuit.

- The maintenance of the system is simplified—a failure in one board affects only

one channel and is at least conceptually easier to debug and/or replace. This may also reduce replacement-parts costs.

- A level of channel isolation is inherent in the system. In the existing prototype system an acceptable level of inter-device cross talk in the analogue drive electronics has been achieved. This part of the system may prove difficult to scale without exceeding the noise budget. If each channel resides in its own analogue 'domain' then cross-talk can be more easily limited.

- The mechanical design of the system is simplified. As each detector is driven by a single analogue board these boards can be placed in close proximity to the detector focal plane and short connection leads used. The number of connections to each board is also reduced leading to a reduction in the complexity of the system.

- Fast, cheap analogue-to-digital converters are now available. For many slow-scan-mode detector arrays it will be as effective and economic to use one converter per detector. This also gives effective channel isolation and allows for close proximity to the detector.

From these points an architecture in which a single surface-mount device flexible PCB is used to operate the analogue aspects of a single mosaic element detector can be envisaged. This architecture has the great advantage of a smaller number of analogue interconnections per module which leads to improved reliability and a reduction in the total length of interconnections—with subsequent improvement in noise immunity.

It should be possible to make available the analogue outputs from each (or several) individual correlated double sampler(s) to a single ultra-fast analogue-to-digital conversion module if a faster device-operation mode was required. This fast-read mode could be implemented in a subset of the mosaic—for example, in the centre of an imaging field.

The second architectural change is in the area of data acquisition. Rather than siting memory devices in the system rack; *i.e.,* instrument-local memory, the memory of the LIM could be used. This enhancement is due to improvements in communications technology in recent years. The advantage gained is that the complexity of the instrument design is reduced and the memory is available for other instruments and/or applications to use. Also, the image data are immediately present in memory accessible by a proces-

sor which can compress the data to reduce data archival time; which can be significant compared to the exposure times used in practice.

An additional enhancement to the system is in the available output formats of the data acquisition software. Although FITS format is generally acceptable for image data it has inherent limitations. Many of these are overcome if an hierarchical data storage format is used. A practical system might use the Starlink Extensible N-Dimensional Data Format (NDF)[198] which is based on an hierarchical format (HDS)[47]. This would be a useful facility for UK-based astronomers. In practice, use of Starlink NDF would require the data acquisition software to be available on a platform running a Starlink supported operating system. Such standardisation is generally desirable from the point of view of maintenance costs at an observatory.

The addition of NDF as an output format should *not* be instead of FITS, as the majority of the world astronomical community will prefer FITS format—the UK community may well prefer NDF, though.

7.4.2 Future Objectives

At present the prototype system is available as a laboratory tool in the OSL. Limited funding is required to upgrade the laboratory system, whilst simultaneously investigating the revised architecture; for example, by constructing single detector drive electronics on surface-mounted boards.

If sufficient funds can be found to construct the four channels required, the OSL 4-detector camera head can be completed and made available for laboratory use. A relaxed requirement for instrument-local memory would greatly reduce the cost of completing this system.

Parts of the mosaic detector technology, notably the controller, are being developed as a byproduct of other OSL projects. An example of this is the use of the controller architecture discussed here in a fast-readout CCD controller for wavefront sensing.

The author has been extensively involved in the development of the new control system software for the UCL IPCS II—many of the ideas from the `DMAP` command line interface have been included in the IPCS command interface. The software represents a considerable improvement over the Transputer graphics display used during the core years of

this project and can be easily integrated with DMAP and the data-acquisition system of the mosaic detector system.

Using these threads to progress the modules of the control system it is hoped that a mature, modular detector-control system can be made available in the future. The ultimate objective must be to utilise the developments in a practical, common-user instrument at one of the major observatories. At the present time the main limiting factor is the expense of a large-area CCD detector. In practice the detectors could well account for more than 50% of the total cost of the system. For this reason it seems likely that future development will have to continue in-house for the present, as and when funds are available.

Appendix A

MIDS paper published in Proc. SPIE Vol. 2198

A versatile mosaic CCD controller design

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ABSTRACT

Current astronomical CCDs (Charge-coupled devices) are limited in size. However, there are increasing demands for larger devices for spectroscopic and direct imaging use. A comparison of the areas of a direct Schmidt-survey plate, and the largest CCD likely to be available in the foreseeable future, serves to illustrate limitations of current electronic technology. Similarly, modern spectrographs can serve *either* high spectral resolution *or* multi-object capability, but not both. One could conceive of an updated analogue of a classical coudé spectrograph, which would provide both simultaneously, were the enormous detector areas required available. It is with these two long-term applications in view that we consider the prospects for large-scale CCD mosaics. Spectroscopy in particular would benefit from mixed devices in the same mosaic e.g. blue and red-optimised, IR

devices etc. We address how optimally to provide the drive waveforms with i) minimum interconnections and complexity, ii) the ability to mix CCDs, iii) the ability to tune the individual CCD waveforms for optimum low-light level performance, and iv) to conceive an architecture which is indefinitely expansible. Our solution is to multiplex the drive waveforms *to* the CCDs as well as the signals *from* them. Minimum chip-count in the sequencing electronics is ensured by using high-density PLD technology (Programmable Logic Device), which enables a module of sixteen or more CCDs to be sequenced from one PLD plus memory. We describe a laboratory prototype, and describe how this could be developed into a system with all the drive electronics for large numbers of CCDs immediately behind the focal plane array. We also summarise our software system for efficiently generating and editing the bitmaps which define the CCD waveforms.

1. INTRODUCTION

Current CCDs used widely in astronomy have the limitation of a relatively small sensing area compared to conventional detectors. However, there are increasing demands for larger devices to cover wide sensing areas; in particular wide-field direct imaging on large telescopes, and two-dimensional spectroscopy. The existing technology of a single large area CCD does not fully support such requirements. Parallel driving of multiple CCDs is another prospect, however, this rules out the possibility of individual tuning of CCDs. Such optimisation is very important when the ultimate low-light level performance is required, particularly for new, or mixed devices. The latter could be important for echelle spectroscopy, where we may envisage blue, red and IR sensors covering the echellogram.

In this work, a new concept is explored representing an entirely novel approach, where the drive waveforms are multiplexed and interleaved. This reduces the number of leadout connections from the vacuum enclosure, simplifying the system and improving reliability.

The overall goal, towards which we have taken significant steps, is a mosaic technology which is indefinitely expansible. Since the number of CCDs and hence connections goes up with the square of the field diameter, whereas the total edge-length of the mosaic available for connections goes only linearly, there is a potential problem in bringing out the connections for large systems. Therefore, we envisage the ultimate solution being to mount the drive electronics behind the CCDs. This drives the design to the minimum

possible chip-count, which has been a key issue in this work. Such a system would require only optical-fibre connections for input commands and output data, plus power and ground.

2. DESIGN CONSIDERATIONS

In recent years, several groups have been attempting to implement the mosaic CCD concept with various approaches[6,7,10]. Some groups utilise buttable CCDs in a mosaic focal plane to minimise the gaps between the devices. Buttable devices are already available from some manufacturers[8,11]. The pixel format of such devices is roughly of the order of 1000×1000 at the present time, but 2000×2000 formats have been developed[11]. In the electronics, most groups adopt a microprocessor based controller to deal with multiple readout operations[6,10]. It is difficult to generalise as to which approach is the more efficient when dealing with such a mosaic, because the technical requirements of a system can differ according to the specific purpose of the observation. Some general design requirements of the system that we have taken into account are briefly summarised as follows:

A.2.3 Expansibility with minimum gaps between CCDs

The ability to cope with an indefinite number of CCDs with little or no modification is actually the key feature of our mosaic approach. In the focal plane, using buttable sensors is a reasonable approach, with the possibility of future expansibility. Of course, buttable sensors have been primarily developed to minimise inter-CCD gaps in a mosaic focal plane. Three side buttable devices can easily cover a '2×N' detector format[10].

A.2.4 Flexibility

It is most desirable for the hardware to handle any number of (different) CCDs in any format without modification. Most of the system parameters have to be easily adjustable to optimise operating conditions, such as readout time, timing of drive waveforms and voltage levels. The most efficient way to accomplish this is by software control.

A.2.5 Simplicity and compactness

Simple design with minimum chip count increases reliability, reduces cost and heat dissipation, and opens the way to install the electronics behind the CCDs. There is a penalty in software complexity. Recent developments of surface mount device technology provide a wider choice of compact electronic components to achieve such system requirements.

A.2.6 Low system noise and cross-talk

The system noise of a CCD imaging system is one of its most important parameters, particularly for low-light level applications such as astronomy. Lower noise devices are being developed, which impacts on the design of the electronics operate them. Careful attention has also to be paid to cross-talk between the outputs of the CCDs. Lower-noise CCDs imply a tighter tolerance on cross-talk.

A.2.7 Short readout time: multiplexed readout versus parallel and separate

The total readout time of all the frames from the devices in a mosaic is also important. Ideally, the readout time of a system should be independent of the number of CCDs employed. This also implies that multiple readout (or parallel readout) of the frames should be implemented. Two solutions are normally used: i) connect all the CCDs in parallel, or ii) replicate all the drive electronics for each CCD. The latter of course requires many more leadouts in a mosaic system.

Our novel solution is slightly to phase-shift the readouts of successive CCDs in the mosaic so that they are read out in an interleaved fashion. This gives the possibility of i) using different drive waveforms for each CCD, and ii) multiplexing the waveforms en-route to the CCDs. This is the heart of the system architecture we have developed.

3. CONTROLLER DESIGN USING PLD

In controlling multiple CCDs, one of the most important tasks is how we can organise the multiple drive waveforms easily and efficiently for each device. Many other systems have adopted microprocessors for this purpose[6,10]. In this work, a controller design for multiple

CCDs has been investigated using the considerable advantages of PLD technology. This is a unique approach in the design of mosaic imaging systems. There are no major functional differences with a microprocessor based design. Indeed, the PLD system retains the flexibility of microprocessor based controllers. The PLD design has advantages such as predictable timing-delays without any low-level language programming, and low design chip-count. Therefore, flexibility and compactness of the system are achieved as well as design simplicity. The PLD can in some ways be considered a custom microprocessor. The programming of a PLD is a relatively simple task for an electronics engineer equipped with commercial CAD and digital simulation software.

Some advantages of using PLD CAD software in the design of a mosaic CCD system are summarised as follows.

- Compactness: Up to 20,000 logic gates can be integrated in a single PLD. All the logic functions of a multi-CCD sequencer can easily be contained in one PLD. The data which defines the CCD sequencing is contained in a RAM chip, which is loaded from a host computer. Therefore, the heart of a multi-CCD sequencer is contained in just two chips.
- Flexibility: Modification or upgrade of a design, e.g. for a completely different CCD architecture, is possible by editing the PLD logic-definition file and re-programming the device off-line. For all normal optimisation of devices, new sequencing data is simply down-loaded to the RAM.
- Simple system control software: Due to its simple hardware architecture, the system control software for multiple CCDs is also simple.
- Low cost and easy handling: The approach described should prove to be more economic than using microprocessors with their support chips.
- Timing delays of the design are predictable since the PLD is not subject to any instruction or interrupt time overhead as with microprocessors, and does not require any low-level language programming. Total digital performance can be simulated in advance of 'blowing' the PLD.

In principle, a total of two digital devices (one PLD, one memory chip) plus a system clock and buffers can produce all the required logic to control multiple CCDs. A digital

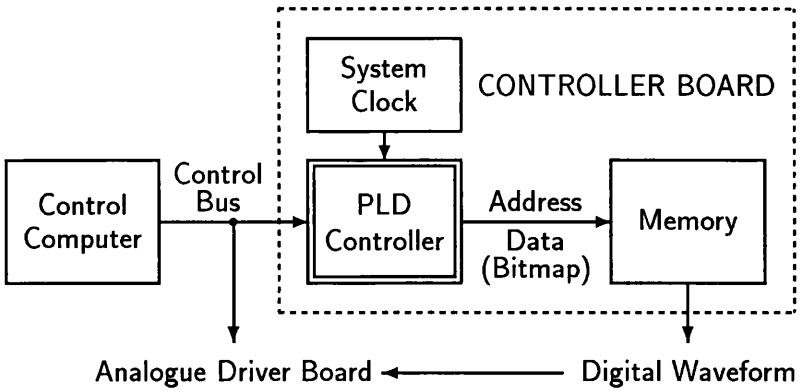

Figure A.1: The block diagram of the PLD controller design concept.

controller has been designed by CAD, and integrated into a single PLD chip, to control the memory device and supervise sequencing (Figure 1). Multiple drive waveforms can be defined as a digital bit-pattern (hereafter bitmap) with CCD addresses, stored in the memory device. After the host computer downloads the bitmap to the memory, cycling through the memory generates the digital waveforms for the CCDs directly. The bitmap is composed of series of logical 0's and 1's that represent logical high and low in binary numbers of 16 or 24 bits width. Each of these 16 or 24 separate bits represents a particular CCD clock or related signal. Note that the width of the data word does *not* increase with the number of CCDs because the CCDs are phase-shifted and the signals multiplexed. This is why 16–24 bits is still adequate for all the clocks for 16 CCDs, with flexibility retained to optimise individual device performance.

Hence the width of the data word represents the number of clocks etc. for one CCD, multiplexed to serve several CCDs. Generally the length of the bitmap (the number of words long) depends on the number of resolution elements into which one pixel-time is subdivided. The main task of the PLD is then to roll through the stored data words at the appropriate clock rate, until the end of a pixel. It then has to repeat the procedure for the length of the horizontal register, and instigate the appropriate vertical equivalents until the end of the readout.

This approach allows great flexibility. Clock waveform changes are simply made by downloading new data to the memory, as are mode changes such as binning, fast transfers etc.

Digital signals are converted to analogue by octal DACs. These allow great flexibility in compact packages and provide many voltage sources efficiently. We have explored two methods of using them. The first is to load the DACs from the host-computer, producing pairs of static voltages from which CCD clock high and low levels are derived. FET analogue switches clocked from the PLD-memory sequencer then switch between the static voltages. The other method is to clock the DACs in real time, generating the waveforms directly. In both cases, amplification and level shifting is required to provide CCD drive signals. Both techniques have proved effective in the operation of multiple CCDs. Bias voltages are similarly programmed direct from software into DACs.

4. SOFTWARE

The controllability of a mosaic imaging system mainly depends on hardware architecture and its associated software. The software has to be written for the specific hardware requirements. System control parameters include repeat patterns for clocking waveforms according to the bitmap, DAC control information and controller initialise parameters. Such information is given from a file or from a terminal together with some commands that supply trigger signals for system operation. In terms of PLD controller structure, four groups of digital information are required from the software to operate the system, as summarised below:

- DAC Control: The DACs in the analogue driver circuit should be programmed to their proper state of high or low by the software. All DACs are directly addressable from software. This allows the user a wide choice of combinations of clock voltage levels and bias levels for optimum low-light level performance. This information is stored in internal digital latches of the DACs.

- Controller Initialise Parameters: The initial system control parameters have to be set before any operation. These include pixel and line numbers of a CCD, and *one pixel readout time* in units of time resolution (e.g. 200nS in our prototypes), for both horizontal and vertical clock waveforms. This information is stored in the internal latches of the PLD to set the operation mode of the system. A user may select any combination of these parameters for his own purpose.

- Bitmap: The software has to provide the bitmap. It consists of 16 (or 24) bit

digital words, including CCD multiplex addresses, video processing signals as well as clock information and shutter commands. The information is stored in RAM and cycling around the memory generates digital clocks directly. The user can tailor drive waveforms by modifying the bitmap source file.

- System Control Commands: Some command signals are necessary to control the system such as 'start readout' or 'select RAM write mode'. Command signals from the computer generate an associated pulse in the controller, to trigger the required operation. Most of these signals are stored in some internal latches of the PLD until operation terminates, and are cleared immediately after the operation for future commands.

The combination of these control parameters by software allows individual tuning of waveforms and bias levels for optimum low-light level performance. When operating devices of different formats in one mosaic, the user provides the largest values of pixel

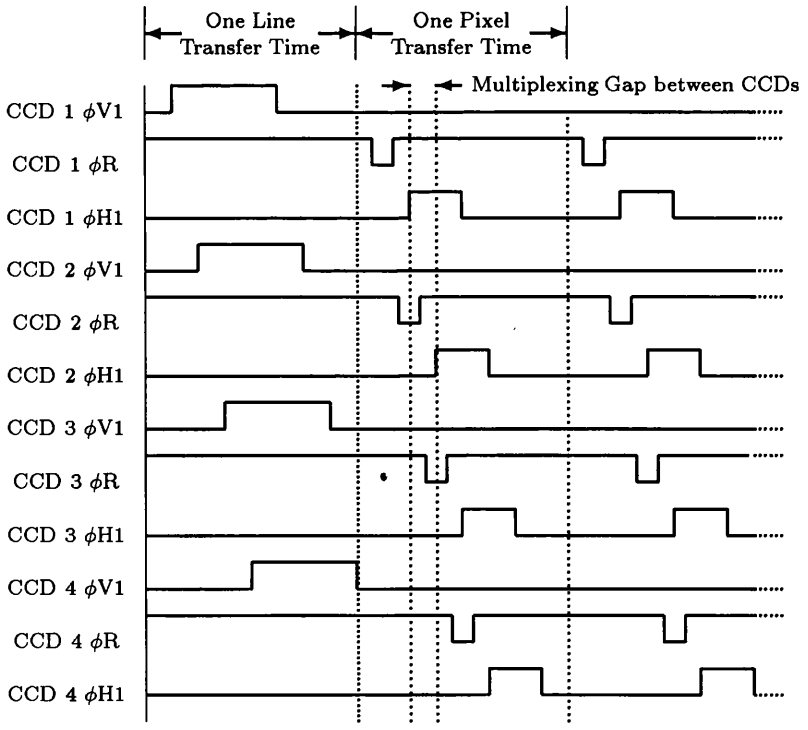

Figure A.2: Part of the timing diagram of the *multiplexing* concept showing bitmap arrangements. The drive waveforms for each CCD can be slightly shifted within one pixel readout time.

and line numbers. Hence, smaller devices are over-scanned producing redundant data.

The multiplexing of multiple CCDs is a fundamental feature of our approach. Its implementation is achieved by including information to specify CCDs by an address in the bitmap, with corresponding events in separate devices *slightly phase shifted* (see Figure 2). These then can be distributed to each CCD by subsequent de-multiplexing logic.

However this multiplexed approach has a limiting condition. In one bit in the bitmap word (say clock $\phi H1$), there is only one opportunity to define a digital state in each time-resolution period of the sequence. To which CCD a given 1 or 0 is applied, is defined by the CCD address selected. Once the level has been defined, it is then held by a digital latch in the appropriate DAC, while the CCD address, and the succeeding bitmap data update another CCD. This introduces a potential coincidence problem, analogous to the coincidences in photon-counting systems. In particular no two events on the same clock on different CCDs can occupy the same time-resolution period. This ultimately limits the number of CCDs and/or the speed of clocking which is possible. With current PLDs, sixteen CCDs controlled from one multiplexed bitmap is in general feasible for normal 'slow-scan' readout. We have operated our prototypes at 5MHz, PLDs available now will run at up to 50MHz giving a possible waveform time resolution of 20nS. This will improve as faster PLDs become available.

5. LABORATORY PROTOTYPE

We have undertaken practical work with four cryogenically-cooled EEV P86320 devices with a pixel-format of 385×578, for initial experiments. Particular attention has been paid throughout this work to 'compatibility and expansibility' to deal with different CCDs (possibly much larger format) and to increase the number of CCDs for future applications.

Using four EEV P88330 devices (format of 1152×1242), a prototype focal plane is being developed. To minimise the inter-CCD gaps, special buttable packaged versions of the EEV P88320 have been developed in collaboration with EEV. The mosaic has a total size of 35mm×28mm with 75% sensing area compared with only 35% for the standard package. The total dead space between sensing areas of adjacent CCDs in a mosaic is 1.6mm on the side and 6.7mm on the end. Figure 3 shows these arrangements schemati-

cally. Further development to minimise butting gaps, *jigsaw* buttable sensors is feasible, pending funding. This would give 1.1mm and 2.5mm butting gaps respectively. Optical methods to overcome butting gaps between the CCDs have also been developed. A. Radley[9] developed the optical design of focal reducer lenses for a large-scale CCD mosaic focal-plane, using ray tracing software. The design, comprising demagnification lenses, allows avoidance of gaps between the CCDs with minimum aberrations.

Prototype versions of the digital controller and analogue driver circuits have been wire-wrapped and tested functionally. The digital design of these controllers have been made with the PLD CAD software provided by Altera[1]. The designs were programmed into a single PLD. The overall design of the PLD has been organised into several subsystems in an hierarchical configuration. The basic structure of the circuit is based on a cascaded 36-bit counter which is the heart of the sequencer. The PLD circuit also includes interface logic, clocking logic and some other control signals such as buffer or system control signals. The design has been thoroughly simulated and tested using the CAD facility. As well as the PLD, the controller board consists of a 10MHz master clock (divided by two), two memory chips, and some buffers. The analogue circuitry uses octal DACs (eight DACs in a single package) as already described. The demultiplexer logic has also been designed by CAD and integrated into a single PLD in the analogue driver board. This distributes digital waveforms to each CCD analogue circuit, according to the addresses from the bitmap.

The system control software consists of several subroutines according to their main functions they deal with, as described in the earlier section. In system control, speed of the host computer is not a great issue since it has only to issue commands and down-load bitmap data off-line. Data acquisition software has been developed by Clayton[2] for multiple CCDs including some statistical subroutines. The software is written almost entirely in ANSI 'C', except for time-critical data acquisition. The code has been successfully ported to VMS, UNIX, and MS-DOS hosts. The system control computer is an IBM PC clone equipped with an Intel 8255 based interface board. This is interfaced via Ethernet to a Sequent computer which acts as file-server to 6GBytes of disk storage.

The system has been integrated for functional and performance tests of the current experimental wire-wrapped version. The system has been optimised with a wide range of operational conditions. Two video processors, including correlated double sampling

circuits, were constructed as modules, based on the circuit designed by Leach[5]. Only one digitiser (500kHz) was employed, by multiplexing the video signals from the CCDs with analogue switches. The multiplexing logic for the video processor and digitiser were also designed using CAD and integrated into PLDs.

The bitmap sequencer, multiplexing analogue-driving and data acquisition systems have all proved to operate exactly as anticipated from the computer simulation function by CAD software. Cross-talk between CCDs has been measured to be minimal, unless one of the CCDs is saturated. It is intended to implement signal clamping to overcome this.

6. SUGGESTED SYSTEM CONFIGURATION

For the foreseeable future it is unlikely that detectors of significantly larger size than those now available will appear. A method for constructing larger detectors—that of the mosaic, has been used successfully on a small scale. The goal of this investigation is to develop techniques for constructing mosaics of arbitrary dimensions. The astronomical application of these mosaics, and the philosophy of adaptability which is central to our philosophy are here used to define the goals.

- Expandable, modular system architecture. At least 16 detectors (100mm×100mm imaging area with EEV88300) can be supported with the simplest configuration of the system. Larger mosaics can be created by modular expansion.
- Flexible design supporting all available detectors and mixed-detector mosaics.
- Support for many mosaic operation modes such as pixel binning, each detector can be independently binned.
- Compact electronic design. The drive electronics for the detectors can ultimately be fitted behind the mosaic.
- Individual and independent optimisation of each detector in a mosaic.
- Text and graphical software user interfaces for definition and tailoring of mosaic operation modes. FITS and TIFF output file formats.
- Minimal data loss in gaps. Use of 'lean' detector packages in hand with re-focus optics and alignment software can produce an effectively monolithic imager.

- Pixel format: 1152×1242 × 4. Pixel Size: 22μm.
- Scale: Approx. 1:1, Actual Size.

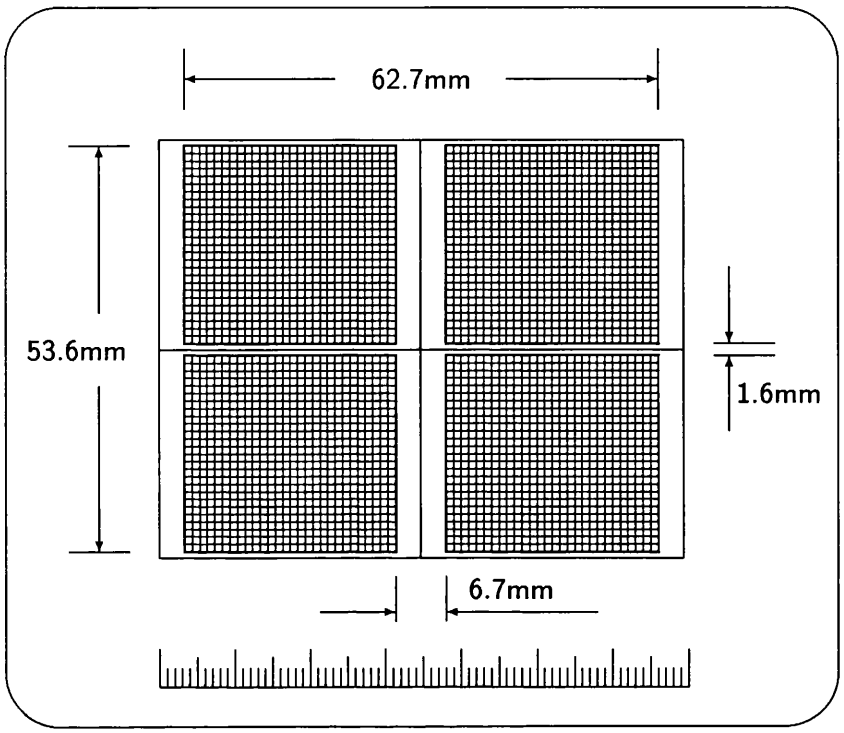

Figure A.3: Assembled prototype of the mosaic array using 4 EEV/OSL CCDs (EEV P88300 variant).

- Readout time of the whole mosaic is only that of the largest detector used. Typically this might be 60 seconds.

This system definition is mainly based on a common-user instrument as an initial development, rather than an instrument oriented for a specific purpose. This implies that some items are suggested to meet the needs of as many research programmes as possible. The system design and performance of a mosaic imaging detector system can be tailored according to specific applications, such as direct imaging or spectroscopy. The system configuration can be individually optimised and customised to achieve the best performance for each application taking into account observational efficiency and other

circumstances such as project funding.

7. CONCLUSION

We have developed a new concept for driving many CCDs in a mosaic. This is to phase-shift each line signal as it is applied to successive CCDs. This permits multiplexing of the signals whilst retaining the ability individually to tune the CCDs. The PLD implementation reduces chip count in the sequencing logic to two devices—one PLD plus memory—plus a few buffers required. Prototypes of both the analogue and digital parts of a system have been built and operated. These ideas are particularly applicable to very large mosaics of detectors.

8. ACKNOWLEDGEMENTS

This project was supported by several SERC grants. We are grateful to Dr. H. Jamshidi for offering his wide experience in electronics and being kind enough to afford constructive suggestions to tackle many problems. Dr. A. Fish has also given valuable advice. Our particular gratitude goes to E. E. Kim for his help in experiments, and A. Radley for his optical study. The private communication with Dr. R. Leach is also deeply appreciated.

9. REFERENCES

1. Altera Corporation, *Altera PLD Data Book*, 1993.

2. M. J. Clayton, *New Detector Technologies for Astronomy,* Ph. D. thesis, University College, University of London, in preparation.

3. A. C. Fish, *Advanced Detector and Control Systems for Optical Astronomy,* Ph. D. thesis, University College, University of London, 1990.

4. W. Y. Han, *New Development for Mosaic CCDs*, Ph. D. thesis, University College, University of London, 1993.

5. R. W. Leach, Private Communication, 1992.

6. R. W. Leach and F. L. Beale, "Design and operation of a multiple readout CCD camera controller" *Instrumentation in Astronomy VII, Proc. SPIE*, **1235**, 284, 1990.

7. G. A. Luppino and K. R. Miller, "A modular dewar design and detector mounting strategy for large-format, astronomical CCD mosaics", *Pub. A. S. P.*, **104**, 215, 1992.

8. Optical Science Lab., "OSL Documentation for Mosaic CCD project", OSL, Dept. Physics and Astronomy, University College, University of London, 1993.

9. A. S. Radley, *An investigation into some aspects of the development of a large scale CCD mosaic imaging system for use in space applications,* M. Sc. dissertation, University College, University of London. 1991.

10. R. Reiß, H. Bauer, S. Deiries, S. D'Odorico, and A. Longinotti, "Buttable optical CCD mosaics: concept and first results at the European Southern Observatory", *New Technologies for Astronomy, Proc. SPIE*, **1130**, 152, 1989.

11. Thomson Composant Militaires et Spatiaux, Data Sheet for TH7897M, 1992.

Appendix B

DMAP Command Language

A detailed description of the DMAP command language can be found elsewhere[40] (this Appendix is extracted from the documentation of DMAP). A summary of the commands and their usage is given here to illustrate the capabilities of the software and for reference purposes.

Each command is described with any possible alternative syntax. Where commands or parameters may be abbreviated, the non-critical part of the command is enclosed in square brackets, *e.g.*,

Syntax: `ASS[IGN]`

In this case only the first three letters ASS are required.

Required parameters are enclosed in triangle brackets (or 'greater than', 'less than' signs) thus:

Syntax: `ASS[IGN] <voltage_buffer> <address>`

Both `voltage_buffer` and `address` **must** be given.

Where there is a choice of parameter, the alternatives are separated by a vertical bar character thus:

Syntax: `CAL[CULATE] AD[D] <value>|IM[AGE]`

In this case the choice is between a scalar `value` and the addition of `IM[AGE]`s.

Optional parameters are enclosed between vertical bars thus:

Syntax: `SET <symbol> <location> |<waveform_look-up_table>|`

In this case the `waveform_look-up_table` may possibly be omitted.

B.1 ASSIGN: Form logical links between hardware and virtual buffers

Syntax: `ASS[IGN] <voltage_buffer> <address>`

`ASS[IGN] <logic_buffer> <bit>`

The `ASSIGN` command makes logical links between real hardware and the notional hardware declared as part of the system description. The actual circuitry which generates a voltage (*e.g.*, `CCD1.RESET`) is then associated with that virtual buffer. The specified `address` is used in compilation and/or down-loading.

Alternatively, the controller memory bit which specifies the particular logic state (for example `CCD1.RESET_INT`) is linked with the logic bit buffer. The selected `bit` is used in compilation and/or down-loading.

This command allows different focal plane assemblies and driving hardware to be 'glued' together into a single system. It also allows a portable focal plane description to be made.

B.2 TBOX: Select area of image data set for analysis or zoom

Syntax: `TBOX`

An interactively positioned and sized box is placed on the image display. The region specified by the box is then selected for analysis. (See related commands: `CALC, ISTAT, TZOOM`).

B.3 CALCULATE: Perform data manipulation and analysis

Syntax: `CAL[CULATE] AD[D] <value>|IM[AGE]`

`CAL[CULATE] CO[PY] RE[SULT]|TE[MPORARY]`

`CAL[CULATE] DIS[PLAY] RE[SULT]|TE[MPORARY] <minimum> <maximum>`

`CAL[CULATE] DIV[IDE] <value>|IM[AGE]`

`CAL[CULATE] LO[AD] RE[SULT]|TE[MPORARY] <file_name>`

`CAL[CULATE] MO[VE] RE[SULT]|TE[MPORARY]`

`CAL[CULATE] MUL[TIPLY] <value>`

`CAL[CULATE] SA[VE] RE[SULT]|TE[MPORARY] <file_name>`

`CAL[CULATE] ST[ATISTICS] RE[SULT]|TE[MPORARY]`

`CAL[CULATE] SU[BTRACT] <value>|IM[AGE]`

`CAL[CULATE] SW[AP]`

The `CALCULATE` command is used for simple analysis of image data acquired from the mosaic detector system. The `BOX` or `AREA` commands must be used to select a region of the image data set to process before any calculation is attempted.

Two double-precision buffers for calculation are available (`RESULT` and `TEMPORARY`). The selected data must be moved to one or both of these buffers using the `MOVE` sub-command. All access to the buffers is through the sub-command set of `CALCULATE`. The result of a calculation is sent to the standard output or stored in the `RESULT` buffer.

The actions which may be performed on the data are (respective with the syntax list above):

Addition A constant value is added to each pixel in the result buffer, or, the two buffers are added pixel-by-pixel. The outcome is stored in the result buffer.

Copy The specified buffer is replicated, pixel-by-pixel to the other buffer.

Display The chosen buffer is scaled and displayed on the image display device.

Divide Each pixel in the result buffer is divided by a constant value, or, pixel-by-pixel divided by the content of the temporary buffer. The outcome is stored in the result buffer.

Load The specified buffer is loaded with data from the named file. The file must have been created with the `SAVE` sub-command.

Move The selected region of the `DMAP` image buffer is moved to the specified calculation buffer.

Multiply Each pixel in the result buffer is multiplied by a constant value. The outcome is placed in the result buffer.

Save The specified buffer is written to the named file.

Statistics The mean and standard deviation of the chosen buffer's pixel values is calculated. The minimum, maximum and buffer dimensions are also found. The outcome is written to standard output.

Subtract A constant value is subtracted from each pixel in the result buffer, or, the temporary buffer is subtracted from the result buffer pixel-by-pixel. The outcome is stored in the result buffer.

Swap The contents of the result and temporary buffers are exchanged.

Commands which involve both buffers will not be carried out if the dimensions of the two buffers are not identical.

B.4 CHECK: Scan and simulate a module programme for voltage rule errors

Syntax: `CHECK <programme>`

The chosen programme is checked and simulated for the following possible errors:

Incomplete initialisation definition The bias voltage look-up table and initial state of logic bit buffers for the selected program must be complete.

Driver hardware capability violation A selected hardware address or bit does not exist or cannot produce a required voltage or state.

Controller hardware capability violation The length of the waveform look-up tables or number of pixels in the readout program are out of the range of the module controller.

Device voltage limit violation A particular set of logic or voltage states at the focal plane assembly would violate protection rules defined in one of the device description files for the module. (This prevents reverse bias of device output transistors for example.)

B.5 COMPILE: Translate DMAP structures into a binary file for download to hardware

Syntax: `COM[PILE] <programme> <file_name>`

The selected **programme** is checked (see `CHECK` command) and compiled into binary data if no errors are found. **file_name** can be: the `TERM[INAL]` in which case the data is written to the standard output as a table of binary, hexadecimal and decimal numbers; a file, in which case a binary data file is created; or `SYS[TEM]` in which case the data is down-loaded directly to hardware.

B.6 CREATE: Create user's command macro

Syntax: `CRE[ATE] MAC[RO] <macro> {macro_text}`

`CREATE` is used to create command macros. A command macro is 'short hand' for a more complex command, for example:

```
CRE MACRO TEST {REPEAT #1 {SYSRUN; WAIT INACTIVE}}
```

This sets up the macro `TEST` which accepts a single parameter (replaceable parameters in the macro definition are signified by the # character preceding the number of the parameter). The macro triggers system hardware and waits for the controller module to stop before re-triggering. The process will be repeated as many times as the user requires.

Macro definitions can be nested and can accept up to ten parameters.

B.7 DEASSIGN: End logical links between hardware and virtual buffers

Syntax: DEASS[IGN] <voltage_buffer>|<logic_buffer>

The logical link previously created with the ASSIGN command for either voltage_buffer or logic_buffer is removed and the assignment state is set to UNASSIGNED in DMAP internal structures.

B.8 DEFINE: Declare and/or define DMAP objects

```
DEF[INE] CONT[ROLLER] <name> <base_address>
DEF[INE] CONT[ROLLER] [MEM]ORYWIDTH <width>
DEF[INE] CONT[ROLLER] [VOLTAGEA]DDRESS <start_bit> <end_bit>
DEF[INE] CONT[ROLLER] [VOLTAGEE]VENTMARK <bit>
DEF[INE] CONT[ROLLER] [VOLTAGED]ATA <start_bit> <end_bit>
DEF[INE] CONT[ROLLER] [LOGICS]TATE <bit>
DEF[INE] CONT[ROLLER] [LOGICA]DDRESS <start_bit> <end_bit>
DEF[INE] CONT[ROLLER] [DEV]ICEADDRESS <start_bit> <end_bit>
DEF[INE] CONT[ROLLER] [LOGICE]VENTMARK <bit>
DEF[INE] MOD[ULE] <name> <addresses>
DEF[INE] ADDR[ESS] <address> <type> |<intercept> <slope>|

DEF[INE] PROG[RAM] <prog> <bias> <horizontal> <vertical>
DEF[INE] WAV[ETABLE] <waveform_look-up_table> <table_size>
DEF[INE] BIAS[TABLE] <bias_voltage_look-up_table>
DEF[INE] SYM[BOL] <voltage_symbol> <voltage>
DEF[INE] STA[TESYMBOL] <logic_state_symbol> <state>
DEF[INE] DEV[ICE] <device> <device_type>
DEF[INE] BUF[FER] <voltage_buffer> <min_eqn> <max_eqn>
DEF[INE] BIT[BUFFER] <logic_buffer>
```

The DEFINE command has two main functions. The first of these is the description of system hardware. Hardware parameters such as the voltage output profile of the device

driver buffer circuits and position of control bits in the sequencer/controller memory are defined.

Hardware description commands in the above list have the following purposes:

Controller name the controller part of the focal plane module. Define the base address for this module on the system bus.

Controller memorywidth Define width of the controller memory cache in bits, typically 24 or 32.

Controller voltageaddress Which bits in the controller memory cache are to contain the address of the buffer selected.

Controller voltageeventmark Which bit in the controller memory is used to mark an event to be sent to the voltage buffers.

Controller voltagedata Which bits in the controller memory are to hold the data which defines the voltage to be sent.

Controller logicstate Bit to hold logic state to be set.

Controller logicaddress Bits to hold address of logic bit buffer for selected device.

Controller deviceaddress Bits to hold the number (address) of the device to be accessed.

Controller logiceventmark Bit to be used to mark logic events in the controller memory cache.

Module Set the name of the voltage buffer (driver) part of the module and the number of addresses in that driver which may be accessed.

Address Describe the response of the DAC at a particular address. The response is assumed to be linear and is described by an intercept and slope. Addresses in the controller bus used for switching or not used can also be defined.

The second function of the `DEFINE` command is for the description of the operation mode programme of the mosaic and the operation requirements of the component detectors.

Mode definintion commands in syntax list above are (respectively) for the declaration of:

Module programmes Complete details of one operation mode for a single module.

Drive waveform look-up tables List of events and timing for either a vertical or horizontal pixel operation.

Bias voltage look-up tables List of initial voltages and logic levels for the electronic hardware of a module.

Voltage level symbols A tag for a particular voltage level or event at a particular pin of a device in the focal plane array.

Logic State symbols A tag for a particular logic state or event in the system hardware.

Member devices One of the component detectors of a module focal plane array.

Voltage buffers Hardware circuits which produce a varying voltage dependent upon the input digital data, for example DACs.

Logic bit buffers Hardware circuits which are driven by simple binary logic (*i.e.*, 'on' or 'off').

The `DEFINE` command can thus be used to build both a complete hardware description and description of the mode of operation of the mosaic.

B.9 DELETE: Remove a command macro definition

Syntax: `DEL[ETE] <macro>`

The previously created `macro` is removed from the command macro list.

B.10 DREAD: Get data from system hardware and scale

Syntax: `DREA[D] <address> |<dig_max>| |<float_max> <unit> <label>|`

The chosen `address` is read. If formatting options (`float_max, unit, label`) are given an output line of the form:

```
label = (value / dig_max * float_max) unit
```

is written to the standard output, where **value** is the digital data read from hardware. Otherwise a hexadecimal and decimal representation of the **value** obtained is written. An 8 or 16 bit read is performed, depending on the value of **dig_max**.

B.11 DWRITE: Put data to system hardware

Syntax: `DWRI[TE] <address> <value>`

The selected **value** is written to the hardware **address**. A sixteen bit write is performed if the **value** exceeds 255 decimal.

B.12 EDIT: Alter DMAP objects

Syntax: `ED[IT] AD[DRESS] <address> <intercept> <slope>`
`ED[IT] WAVE[TABLE] <wavetable> <position> <delta_time>`
`ED[IT] SYM[BOL] <voltage_symbol> <delta_voltage>`
`ED[IT] BUF[FER] <voltage_buffer> MIN[IMUM]|MAX[IMUM] <lim_eqn>`

The **EDIT** command allows the **DMAP** user to alter some of the objects stored in the programme internal structures. In version 1.00 of the software this will be useful for automated optimisation and diagnostic testing of mosaic performance (in the current version (0.93) no arithmetic or programme control-flow operations are available). The commands are useful for interactive adjustment of device operation, error correction and hardware testing.

The above commands have the following uses:

Address Allows the user to calibrate the voltage output of a hardware buffer by altering the **DMAP** internal equation for the buffer.

Wavetable Allows the user to cut or add time from a waveform look-up table. If new time is added it is initialised to contain no events.

Symbol Can be used to alter the voltage symbolised, for example, to change the value of a clock voltage.

Buffer Can be used to alter the voltage limit rules for a virtual buffer. (This command should never be used.)

B.13 ECHO: Put text to standard output stream

Syntax: `EC[HO] {echo_text}`

The `echo_text` is written to the standard output.

B.14 EXIT: Leave DMAP

Syntax: `EX[IT] |<return_value>|`

The `DMAP` environment is exited. Control is returned to the calling shell. By default the programme returns zero (0), otherwise the `return_value` is returned.

B.15 HELP: Interactive help facility

Syntax: `H[ELP] |<subject>| |<subject>...|`

The interactive help facility is invoked. The help facility will attempt to access data for the chosen subject and sub-subjects specified on the command line. The facility is functionally similar to the VMS on-line help facility.

B.16 READ: Execute DMAP commands from text file

Syntax: `REA[D] <file_name>`

The commands in the text file `file_name` are executed until and end-of-file character is met. Control is returned to the stream in which the `READ` command was made.

B.17 RENAME: Change the tag of a DMAP object

Syntax: `REN[AME] <object_tag> <new_object_tag>`

The specified object is renamed. The data associated with the object is unchanged. References to the object by tag are not altered (for example in command macros).

B.18 REPEAT: Carry out command several times

Syntax: `REP[EAT] <repeat_count> {repeat_text}`

The `repeat_text` is repeated `repeat_count` times or until an error is detected. The `repeat_text` can be any series of macros or `DMAP` commands. Recursive `REPEAT` loops are possible. The level of recursion possible is dependent upon the amount of memory available.

B.19 SEND: Down-load module programme to hardware

Syntax: `SEND PROG[RAM] <programme>`

`SEND FILE <file_name>`

Either: The selected `programme` from `DMAP` internal structures is compiled and down-loaded to system hardware with no device voltage limit violation checking or simulations.

Or: The selected `file_name`, which should be a binary file created by the `DMAP COMPILE` command is read and sent to system hardware.

B.20 SET: Position events or set DMAP flags

Syntax: `SET <symbol> <location> |<waveform_look-up_table>|`

`SET <symbol> |<bias_voltage_look-up_table>|`

`SET <programme> H[ORIZONTAL]|V[ERTICAL] CO[UNT] <count>`

`SET <symbol> VOLT[AGE] <voltage>`

`SET MA[SK] <object_mask>`

`SET PROM[PT] <prompt_string>`

`SET <flag>`

The `SET` command is used to build up look-up tables. Events or bias voltages are defined with this command. The dimensions of the image are also set with `SET`.

`SET` can also be used to set the voltage represented by a symbol.

SET has three ancillary functions: selection of the default edit mask; the setting/resetting of DMAP internal flags (for example SET NOSHOW turns off verbose command output); and the setting of the command input prompt.

B.20.1 Setting events and edit masks

The command SET CCD1.RESET.HI 10.4 PIXEL sets the event CCD1.RESET.HI 10.4μS into the PIXEL waveform look-up table. If a command SET MASK PIXEL has previously been issued then the former command may be abbreviated to SET CCD1.RESET.HI 10.4 the waveform look-up table is implied by the current value of MASK. If the MASK is set to also include the current device by SET MASK CCD1 then the command can be further abbreviated to SET RESET.HI 10.4. It is also possible to mask at the buffer level.

Voltages for initialisation (Bias voltage look-up tables) are set in a similar fashion: SET CCD1.RESET.LO STARTUP. Here STARTUP is the name of the bias voltage look-up table.

B.20.2 DMAP internal flags

The following flags may be set or reset with the SET command:

- [NO]BREAK determines whether user interrupt of WAIT states is allowed. (Default: allowed.)
- [NO]CHANGEPROMPT determines whether the SET MASK command sets the command input prompt to reflect the current edit mask. (Default: prompt is changed to reflect edit mask.)
- [NO]CHECK determines whether data is read back from the controller memory to verify correct down-load. (Default: data is verified.)
- [NO]SHOW determines whether verbose output (informational messages) are written. (Default: verbose output.)
- [NO]VERIFY determines whether the user is prompted to verify programme exit. (Default: exit verify not required.)

B.21 SHOW: Display DMAP objects

Syntax: `SHO[W] <object>`

`SHO[W] <object_class>`

`SHO[W] <table_contents>`

`SHO[W] MACRO[S]`

`SHO[W] <flag>`

The `SHOW` command is used to display information about `DMAP` objects or to list all the objects of a particular class. The command is also used to display the events set in a waveform look-up table.

The command has two ancillary uses: the listing of command macros; and the display of `DMAP` internal flags.

B.22 SPAWN: Create new (operating system) command shell

Syntax: `SPAWN`

`SPAWN <task>`

`SPAWN {task_text}`

A sub-shell is started. If no command line arguments are given, control is passed to the sub-shell and the method of return (`LOGOUT` for example) is given. Alternatively, a single string command `task` may be specified on the command line (`task` must contain no spaces), or a multiple string command `task_text` may be given. The command(s) given are passed to the sub-shell for execution.

B.23 SYSRUN: Trigger hardware and acquire data

Syntax: `SYSR[UN] |RE[AD]|`

The appropriate data to execute a controller programme is sent to hardware. If the `READ` option is specified, the data acquisition sub-system is called and this handles hardware triggering and collection of image data from the digitiser to the `DMAP` image buffer.

B.24 UNSET: Remove events or unset DMAP flags

Syntax: `UNSET <event> |<bias_table>|`

`UNSET <time> |<waveform_look-up_table>|`

This command is used to remove events form bias voltage and waveform look-up tables. The command is sensitive to the current edit mask.

B.25 WAIT: Wait for absolute or delta time or particular hardware state

Syntax: `WAIT UNT[IL] <absolute_time>`

`WAIT FOR <delta_time>`

`WAIT ACT[IVE]`

`WAIT INACT[IVE]`

Real time delays can be introduced with the **WAIT** command. **DMAP** will suspend command execution until the specified time or hardware condition has occurred. The wait-state can be terminated by an user escape **ESC**.

Appendix C

DMAP Programming Examples

The following example of DMAP code has been used for test purposes in the laboratory at UCL. The code defines a four-CCD mosaic of which only one device is in use.

The first file is a 'base file' which should be loaded when DMAP is started up:

```
%
%headline
%
echo; echo {DMAP initialisation file for MS-DOS 3.3. 9-NOV-1992.}
%
%read in macros
%
read macros.dm
%
%set up for four CCDs
%
def dev ccd1 p8603; set ccd1 active
def dev ccd2 p8603; set ccd2 active
def dev ccd3 p8603; set ccd3 inact
def dev ccd4 p8603; set ccd4 inact
def dev ancil default; set ancil inact
%
```

```
%set up bias table
%
def bias start
set mask start
set mask ccd1; read p8603b.dm
set mask ccd2; read p8603b.dm
set mask ccd3; read p8603b.dm
set mask ccd4; read p8603b.dm
set ancil.power.on
set ancil.power.off 1
set mask 00
%
%
%define control hardware
%
read system.hdf
%
%assign buffers
%
read assign.dm
%
%read in wavetables
%
read pixel.dm
read line.dm
%read rline.dm
%read rpixel.dm
%read ppixel.dm
%read pline.dm
%read nstart.dm
%
%empty wavetable
```

```
%
%def wave null 3.0
%
%system programmes
%
def prog run start pixel line
set run horiz cou 440
set run vert cou 578
%
%def prog rrun start pixel rline
%set rrun horiz cou 440
%set rrun vert cou 578
%
%def prog brun start rpixel rline
%set brun horiz cou 440
%set brun vert cou 578
%
%def prog prun start ppixel pline
%set prun horiz cou 440
%set prun vert cou 578
%
%def prog sysset start null nstart
%set sysset horizontal count 1
%set sysset vertical count 1
%
echo; echo {Initialisation complete.}
%
%End of file
%
```

The base file reads a set of macro definitions from `macros.dm`, for housekeeping operations such as directory listing and displaying text files. Command abbreviations are also given. The base file performs all the set-up operations required for the test facility. Files which

define the look-up tables and assign hardware are all called as necessary. Several external commands, such as `iacq` (image acquisition) are also defined as macros:

```
%
%default macros for DMAP
%
def mac dir {spawn {dir #1 #2 #3}}
def mac copy {spawn {copy #1 #2 #3 #4}}
def mac del {spawn {del #1 #2 #3 #4}}
def mac cls {spawn cls}
def mac ty {spawn {type #1}}
def mac qc {spawn {qc #1 #2 #3}}
def mac kermit {spawn kermit; echo}
def mac vaxlink {spawn vaxlink; cls}
def mac isr? {wait inactive}
def mac go {iacq; istat}
def mac test {repeat #1 {sysrun; isr?}}
def mac upd {send #1 noinit}
def mac ampon {read ampon.dm; send run}
def mac ampoff {read ampoff.dm; send run}
def mac ccdoff {read linoff.dm; read pixoff.dm; send run}
def mac ccdon {read linon.dm; read pixon.dm; send run}
def mac id {set run h coun #1; set run v coun #2}
def mac td {cd e:\v55-8\test}
def mac th {cd e:\v55-8\harl}
def mac cd {spawn {cd #1}}
def mac sd {spawn {cd #1}}
def mac block {spawn {block #1 #2 #3 #4 #5 #6 #7 #8 #9}}
def mac box {spawn {tbox #1 #2 #3 #4 #5 #6 #7 #8 #9}}
def mac calc {spawn {dmcalc #1 #2 #3 #4 #5 #6 #7 #8 #9}}
def mac demux {spawn {demux #1 #2 #3 #4 #5 #6 #7 #8 #9}}
def mac disp {spawn {tdisp #1 #2 #3 #4 #5 #6 #7 #8 #9}}
def mac iacq {spawn {iacq #1 #2 #3 #4 #5 #6 #7 #8 #9}}
```

```
def mac ihead {spawn {ihead #1 #2 #3 #4 #5 #6 #7 #8 #9}}
def mac istat {spawn {istat #1 #2 #3 #4 #5 #6 #7 #8 #9}}
def mac tinit {spawn {tinit #1 #2 #3 #4}}
def mac itest {repeat #1 {iacq /s; istat /s}}
def mac ltest {echo {System test running: do not touch keyboard!};\
  repeat #1 {spawn {dmtime >> ltest.log};\
  repeat #2 {spawn {iacq /s >> ltest.log};\
     spawn {istat /s >> ltest.log}}}}
def mac tclear {spawn {tco 10 0>nul}}
def mac setr {spawn {setrain #1}}
def mac setg {spawn {setgrey #1}}
def mac boxswap {spawn {copy message.bx0 zx.zx>nul};\
  spawn {copy message.bx1 message.bx0>nul};\
  spawn {copy zx.zx message.bx1>nul};\
  spawn {del zx.zx>nul}}
def mac ob {boxswap; istat}
def mac lampon {dwrite 1 11}
def mac lampoff {dwrite 0 11}
def mac exp {test 2; lampon; wait for #1; lampoff; wait for 1; go}
def mac vset {set #1 voltage #2}
def mac meanvar {read meanvar.dm}
%
%End-of-file
%
```

The next file, which is read four times is the file `p8603.ddf`. The `define device` command reads the file:

```
%
% EEV CCD P8603: device description file.
% Martin Clayton 30th November 1991.
%
% voltage buffers & default symbols
```

```
%
%                minimum maximum  hardware delay
%                  limit limit    |                    symbol
%      buffer    equation equation |         symbol       value
%          |           | |        |            |          |
%          |           | |        |            |          |
%          v           v v        v            v          v
define buf reset vss-15.0 vss+15.0 0; define sym reset.hi  10.0;
      define sym reset.lo   0.0;
define buf h_1   vss-15.0 vss+15.0 0; define sym h_1.hi    10.0;
      define sym h_1.lo     0.0;
define buf h_2   vss-15.0 vss+15.0 0; define sym h_2.hi    10.0;
      define sym h_2.lo     0.0;
define buf h_3   vss-15.0 vss+15.0 0; define sym h_3.hi    10.0;
      define sym h_3.lo     0.0;
define buf v_1   vss-15.0 vss+15.0 0; define sym v_1.hi    10.0;
      define sym v_1.lo     0.0;
define buf v_2   vss-15.0 vss+15.0 0; define sym v_2.hi    10.0;
      define sym v_2.lo     0.0;
define buf v_3   vss-15.0 vss+15.0 0; define sym v_3.hi    10.0;
      define sym v_3.lo     0.0;
define buf vss        0.0     20.0 0; define sym vss.init   0.0;
define buf vog   vss       vss+5.0 0; define sym vog.init   3.0;
define buf vrd   vss      vss+23.0 0; define sym vrd.init  22.0;
define buf vod   vss      vss+23.0 0; define sym vod.init  15.0;
define buf abg   vss       vss+1.0 0; define sym abg.init   0.5;
%
% logic bit buffers & default symbols
%
%                                logic                  logic
%   logic bit buffer             state    symbol        state     symbol
%          |                     symbol    value        symbol     value
```

```
%          |   hardware delay     |          |          |           |
%          |        |             |          |          |           |
%          v        v             v          v          v           v
def logicb zero_int 0;   def stat zero_int.on 1; def stat zero_int.off 0;
def logicb pre_samp 0;   def stat pre_samp.on 1; def stat pre_samp.off 0;
def logicb sig_samp 0;   def stat sig_samp.on 1; def stat sig_samp.off 0;
def logicb adc_trig 0.8; def stat adc_trig.on 1; def stat adc_trig.off 0;
%
% End of file
%
```

The file contains buffer description and default values for the bias voltages and clock levels. The file also defines the logic control bits required.

The next file read in is `p8603b.dm` which simply sets up the default bias voltage table. `DMAP` next reads in the system hardware defintion file `system.hdf`:

```
%
% system.hdf : hardware description.  Martin Clayton 20th January 1992.
%
% controller definition
%
define controller seq ff0801;
%
define controller memorywidth 24;
define controller voltageaddress 0 5;
define controller voltageeventmark 6;
define controller voltagedata 8 15;
define controller logicstate 16;
define controller logicbit 17 19;
define controller logicaddress 20 22;
define controller logiceventmark 23;
%
% driver definition
```

```
%
define module driver 64;
%
%           address   intercept  slope
%              |             |    |
%              |             |    |
%              v             v    v
define address 0 analogue 0.081 0.0962;
define address 1 analogue 0.081 0.0962;
define address 2 analogue 0.081 0.0962;
define address 3 analogue 0.081 0.0962;
define address 4 analogue 0.081 0.0962;
define address 5 analogue 0.081 0.0962;
define address 6 analogue 0.081 0.0962;
define address 7 analogue 0.081 0.0962;
define address 8 analogue 0.081 0.0962;
define address 9 analogue 0.081 0.0962;
define address 10 analogue 0.081 0.0962;
define address 11 analogue 0.081 0.0962;
define address 12 analogue 0.081 0.0962;
define address 13 analogue 0.081 0.0962;
define address 14 analogue 0.081 0.0962;
define address 15 analogue 0.081 0.0962;
define address 16 analogue -12.5 0.0968;
define address 17 analogue -12.5 0.0968;
define address 18 analogue -12.5 0.0968;
define address 19 analogue -12.5 0.0968;
define address 20 analogue -12.5 0.0968;
define address 21 analogue -12.5 0.0968;
define address 22 analogue -12.5 0.0968;
define address 23 analogue -12.5 0.0968;
define address 24 analogue -12.5 0.0968;
```

```
define address 25 analogue -12.5 0.0968;
define address 26 analogue -12.5 0.0968;
define address 27 analogue -12.5 0.0968;
define address 28 analogue -12.5 0.0968;
define address 29 analogue -12.5 0.0968;
define address 30 analogue -12.5 0.0968;
define address 31 analogue -12.5 0.0968;
define address 32 analogue -12.5 0.0968;
define address 33 analogue -12.5 0.0968;
define address 34 analogue -12.5 0.0968;
define address 35 analogue -12.5 0.0968;
define address 36 analogue -12.5 0.0968;
define address 37 analogue -12.5 0.0968;
define address 38 analogue -12.5 0.0968;
define address 39 analogue -12.5 0.0968;
define address 41 analogue -12.5 0.0968;
define address 42 analogue -12.5 0.0968;
define address 43 analogue -12.5 0.0968;
define address 44 analogue -12.5 0.0968;
define address 45 analogue -12.5 0.0968;
define address 46 analogue -12.5 0.0968;
define address 47 analogue -12.5 0.0968;

define address 48 analogue -12.5 0.0968;
define address 49 analogue -12.5 0.0968;
define address 50 analogue -12.5 0.0968;
define address 51 analogue -12.5 0.0968;

define address 40 analogue 0.000 0.1;
%
% End of file
%
```

This file contains a complete definition of the system sequencer and analogue electronics. DMAP now reads `assign.dm` which makes logical links between the actual driving hardware and the requirements of the detectors:

```
%
% assign.dm: set-up logical links.  Martin Clayotn 20th Jabuary 1992.
%
% first device
%
set mask ccd1;
%
%    voltage
%     buffer address
%          | |
%          | |
%          v v
assign reset 47;
assign h_1   23;
assign h_2   31;
assign h_3   39;
assign v_1   19;
assign v_2   27;
assign v_3   35;
assign vss   48;
assign abg    3;
assign vod   15;
assign vrd    7;
assign vog   11;
%
%         logic
%        buffer bit
%             | |
%             | |
```

```
%            v v
assign zero_int 0;
assign pre_samp 1;
assign sig_samp 2;
assign adc_trig 3;
%
% second device
%
set mask ccd2;
%
%    voltage
%     buffer address
%          | |
%          | |
%          v v
assign reset 46;
assign h_1   22;
assign h_2   30;
assign h_3   38;
assign v_1   18;
assign v_2   26;
assign v_3   34;
assign vss   49;
assign abg    2;
assign vod   14;
assign vrd    6;
assign vog   10;
%
%         logic
%        buffer bit
%             | |
%             | |
```

```
%            v v
assign zero_int 0;
assign pre_samp 1;
assign sig_samp 2;
assign adc_trig 3;
%
% third device
%
set mask ccd3;
%
%    voltage
%     buffer address
%          | |
%          | |
%          v v
assign reset 44;
assign h_1   20;
assign h_2   28;
assign h_3   36;
assign v_1   16;
assign v_2   24;
assign v_3   32;
assign vss   50;
assign abg    0;
assign vod   12;
assign vrd    4;
assign vog    8;
%
%         logic
%        buffer bit
%             | |
%             | |
```

```
%             v v
assign zero_int 0;
assign pre_samp 1;
assign sig_samp 2;
assign adc_trig 3;
%
% fourth device
%
set mask ccd4;
%
%    voltage
%     buffer address
%          | |
%          | |
%          v v
assign reset 45;
assign h_1   21;
assign h_2   29;
assign h_3   37;
assign v_1   17;
assign v_2   25;
assign v_3   33;
assign vss   51;
assign abg    1;
assign vod   13;
assign vrd    5;
assign vog    9;
%
%         logic
%        buffer bit
%             | |
%             | |
```

```
%             v v
assign zero_int 0;
assign pre_samp 1;
assign sig_samp 2;
assign adc_trig 3;
%
% reset edit mask
%
set mask 00;
%
% End of file
%
```

Next DMAP reads the look-up table files `pixel.dm`, `line.dm`, `null.dm` and `nstart.dm`, `pixel.dm` is shown here as an example:

```
%
% horizontal pixel waveform look-up table.
% this is for CCD1 active only.
%
define wave pixel 54.8;
%
set mask pixel; set mask ccd1;
%
%    event  location (microsec)
%      |           |
%      |           |
%      v           v
set reset.hi      4.0;
set reset.lo      8.0;
set zero_int.on   0.0;
set zero_int.off 12.0;
set pre_samp.on  13.6;
```

```
set pre_samp.off 23.6;
set h_3.hi       26.8;
set h_2.lo       28.2;
set h_1.hi       33.2;
set h_3.lo       43.6;
set h_2.hi       39.6;
set h_1.lo       41.0;
set sig_samp.on  43.0;
set sig_samp.off 53.0;
set adc_trig.on  53.8;
set adc_trig.off 54.0;
%
% End of file
%
```

The remaining lines of the base file define various module programmes used for purging and device testing.

Appendix D

Software for Hardware Control and Testing

This Appendix contains several routines and functions used for the control and testing of the mosaic system hardware.

D.1 PC to CCD Rack Communication Function

The following file `contcomm.c` defines communication functions for `DMAP_` 0.92 when used with the laboratory Dell PC and Blue Chip PIO-48 card.

```
/*
 * Mosaic CCD project.
 * Controller programme create/edit facility 'DMAP'.
 * Version: 0.92.
 * File: CONTCOMM.C.  Hardware communication Functions.
 * Date: 10th April 1992.
 * Written by: Martin Clayton.
 */

/*Standard header files.
 */
```

```
#include <stdio.h>
#include <math.h>
#include <time.h>

/*System specifics.
 */
#include "dmapspec.h"

/*DMAP parameters and code substitutions.
 */
#include "dmapdefs.h"

/*Global variables and function declarations.
 */
#include "dmapvars.h"



/*
 * cont_com : transfer of data between host and controller
 * ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
 */
int cont_com( addr, value, dirn )

/*Required arguments:
 */
int addr;                       /* Relative address to be accessed.    */
int value;                      /* Data to be sent, if any.            */
int dirn;                       /* Flag, read or write the address.    */

{
/*No local variables.
 */
```

```
/*First case, read data from the control rack.
 */
    if ( dirn == READ ) {

/*    Set-up the address and control lines,
 *    this loads the data output latch (U7)
 *    on the communications board.
 */
        outp( BASEADDR + ADDRADDR, addr );

/*    Read the data latch into the local variable.
 */
        value = inp( BASEADDR + DATA__IN );

/*Second case, send eight-bit data to the rack.
 */
    } else if ( dirn == WRITE ) {

/*    Put the on the PIO card output latch.
 */
        outp( BASEADDR + DATA_OUT, value );

/*    Strobe the address and control lines in the
 *    CCD rack, so the data is picked up.
 */
        outp( BASEADDR + ADDRADDR, addr + 128 );
    }

/*Return the value sent, or, the value read.
 */
return ( value );
```

```
}

/*End-of-file.
 */
```

D.2 DMAP Photon Transfer Curve Tools

The following two DMAP files are examples of those used for collecting the data for calibrating the system noise and photon transfer function of a detector.

The first file `mvtools.dm` defines DMAP macros needed to carry out the experiment.

```
create macro setup {lampoff; powon; send run; test 2}
create macro mvinit {spawn {mvinit #1 > mv.log}}
create macro mvend  {spawn {mvend >> mv.log}}
create macro iaql {spawn {iacq -s >> mv.log}}
create macro istl {spawn {istat -s>> mv.log}}
create macro mexp {test 2; lampon; wait for #1; lampoff; iaql; istl}
create macro tore {boxswap; istl; spawn {calc mo re}; boxswap}
create macro tote {boxswap; istl; spawn {calc mo te}; boxswap}
create macro sigsq {spawn {calc sub im};\
                                spawn {calc stat re -s >> mv.log}}
create macro explog {spawn {echo Exposure time=#1 >> mv.log}}
create macro idisp {spawn {tdisp 2900 35000}}
create macro mvpt {spawn {tstring 300 300 255 Exposure_Time=#1};\
       explog #1; mexp #1; tote; idisp; mexp #1; tore; idisp; sigsq}
```

The second file `meanvar.dm` is read as part of the meanvar macro defined in the file `plain.dm` (see AppendixC).

```
read mvtools.dm % define mean-variance test tools
set show
spawn {tstring 300 300 255 "Initialising"}
setup
```

```
echo {"Creating result file MV.LOG"}
mvinit MJC
spawn {tstring 300 300 255 "Starting_Run"}
mvpt 5
mvpt 10
mvpt 20
mvpt 40
mvpt 80
spawn {tstring 300 300 255 "Mean-Variance_Run_Complete"}
mvend
```

Thus to perform a mean-variance measurement:

1. DMAP is activated with the macros from `plain.dm` loaded.
2. The power supply rack is manually switched on.
3. The computer controlled light source is positioned appropriately.
4. A dark enviroment for the test is established.
5. The user retires from the dark room after typing a command similar to `$ wait for 30; meanvar` which gives time to leave the room.

Glossary

AAO	Anglo-Australian Observatory
ADAM	Astronomical Data Acquistion Monitor
AAT	Anglo-Australian Telescope
ADC	Analogue to Digital Converter
AXAF	Advanced X-ray Astrophysics Facility
BAT	Bolshoi Alt-azimuth Telescope *(Bol'shoi Teleskop Azimutal'nyi)*
CARA	California Association for Research in Astronomy
CCD	Charge-Coupled Device
CDS	Correlated Double Sampling
CFHT	Canada France Hawaii Telescope
CID	Charge Injection Device
CMOS	Complimentary Metal Oxide Semiconductor
CORAVEL	Correlation Radial Velocities
CTE	Charge Transfer Efficiency
CTIO	Cerro Tololo Inter-American Observatory
DAC	Digital to Analogue Converter
DIL	Dual In Line
DN	Digital Number/Data Number
DSP	Digital Signal Processor
DQE	Detective Quantum Efficiency
EPLD	Erasable Programmable Logic Device
EPROM	Erasable Programmable Read Only Memory
EOC	End of Conversion
ESO	European Southern Observatory
FOC	Faint-object Camera

FOS	Faint-object Spectrograph
FSR	Full Scale Range
HDS	(Starlink) Hierarchical Data Format
HROS	High-resolution Optical Spectrograph
HRS	High-resolution Spectrograph
HSP	High-speed Photometer/polarimeter
HST	Hubble Space Telescope
IC	Integrated Circuit
ING	Isaac Newton Group (of telescopes)
INT	Isaac Newton Telescope
IPCS	Image Photon Counting System
IRAS	Infrared Astronomical Satellite
ISO	Infrared Space Observatory
IUE	International Ultraviolet Explorer
JCMT	James Clerk Maxwell Telescope
KPNO	Kitt Peak National Observatory
LED	Light Emitting Diode
LIM	Local Instrument Microcomputer
MCP	Micro-Channel Plate
MIDS	Mosaic Imaging Detector System
MMS	Module Management System
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MPP	Multi-Phase Pinned
NDF	(Starlink) N-Dimensional Data Format
NTT	New Technology Telescope
OSL	Optical Science Laboratory
PCB	Printed Circuit Board
PFUEI	Prime Focus Universal Extragalactic Instrument
PLD	Programmable Logic Device
PROM	Programmable Read Only Memory
QE	Quantum Efficiency
QEH	Quantum Efficiency Hysteresis

RAM	Random Access Memory
RGO	Royal Greenwich Observatory
ROE	Royal Observatory, Edinburgh
ROM	Read Only Memory
SAAO	South African Astronomical Observatory
SBRC	Santa Barbara Research Center
SMT	Surface Mount Technology
UCLES	University College London Échelle Spectrograph
UES	Utrecht Échelle Spectrograph
UKIRT	United Kingdom Infrared Telescope
UKIRT	United Kingdom Infrared Telescope
VGA	Video Graphics Array
VLT	Very Large Telescope
WF/PC	Wide-field/Planetary Camera
WHT	William Herschel Telescope
WORM	Write Once Read Many
ZIF	Zero Insertion Force (Socket)

Acknowledgements

Adrian Fish, Alice Evans, Allie Lane, Andrea Cresswell, Andrew Squire, Andy Charalambous, Andy Cook, Anne Mette Udsholt, Anthony James, Baron Kwantreng, Bella McEwen, Bill Sterland, Bill Towlson, Brett Stewart, Charlie Tomlinson, Chas Warlow, Chris Hartley, Chris Hirst, Chris Holland, Chris Scully, Chris Skinner, Clifford Chiča, Cordula Robinson, Dave Bone, Dave Brooks, Dave Fletcher, Dave Mills, Dave Rees, Dave Rooks, Dave Walker, Dave Webb, Debbie Skidmore, Derrick Attree, Donald Knuth, Elizabeth Mayer, Ee-Eul Kim, Emma Foxhall, Emma Longley, Emma Russell, Faith Hanstater, Francisco Diego, Gareth Thomas, Geraint Jones, Gil Nixon, Helen Heyward, Heshmat Jamshidi, Ian Crawford, Ian Griffin, Ian Howarth, ℑ IMIMIX, John Bellis, John Deacon, John Deer, John Fordham, John Peet, Juliet Walshe, Karen Murphy, Kathy Dallas, Kemal Ahkter, Leslie Lamport, Lesley Wilson, Louise E. Hird, Lulu Angorita, Mark Dryburgh, Mark Evans, Mark Lilgie, Martin Cullum, Matthew Low, Max Wilde, METAFONT, Mike Barlow, Mike Cresswell, Mike Oldfield, Nazarene Zafar, Nick Perry, Nick Storey, Patrick Watkinson, Paul Grist, Paul Jorden, Paul Plater, Pete Bull, Pete Rae, Peter Pool, Peter Sanford, Phil Smith, Print Spot, Robert Leach, Roger McMinn, Sam Flynn, Sarah Dallas, Simon Holt, Siobhan Leary, Starlink, Steve MacAulay, Steve Murphy, Steve Wilkins, Sug-Whan Kim, Sunil Chopra, The Brewery České Budějovice, Tim Lewsley/Redgrove, UK.AC.TEX, Won-Yong Han, Yung-Soo Kim,

Bibliography

[1] J. M. Achtermann,
Using DSPs to Build Modular Data-Acquisition and Instrument Control Systems: Shifting Functionality from Hardware to Software,
Pub. A. S. P. Vol. 106, pp. 173–181, February 1994.

[2] *Product Description, Am7968/Am7969 TAXIchip devices,*
Advanced Micro Devices Inc., California, USA, 1987.

[3] *Data book,*
Altera Corporation, California USA, 1991.

[4] G. F. Amelio, M. F. Tompsett and G. E. Smith,
Experimental verification of charge-coupled device concept,
Bell Syst. Tech. J. Vol. 49, pp. 593–600, 1970.

[5] J. R. P. Angel,
Matching very large telescopes with CCDs for imaging and spectroscopy,
Steward Observatory Preprint, No. 262, 1979.

[6] G. Béal, G. Boucharlat, J. Chabbal, J. P. Dupin, B. Fort and Y. Mellier,
Thomson-CSF frame-transfer charge-coupled device imagers: design and evaluation at very low flux level,
Opt. Eng. Vol. 26 No. 9, pp. 902–910, September 1987.

[7] F. Beale and R. W. Leach,
Video processor and clock driver circuitry for CCD cameras,
Proceedings of the CCDs in Astronomy Conference, A. S. P. Conference Series, No. 8, pp. 180–187, 1990.

[8] C. A. Beichman, G. Neugebauer, H. J. Habing, P. E. Clegg and T. J. Chester (Eds.),
Infrared Astronomical Satellite (IRAS) catalogs and atlases,
Vol. 1, *Explanatory supplement,* NASA RP–1190, 1988.

[9] P. R. Bevington,
Data Reduction and error analysis for the physical sciences,
McGraw-Hill, 1969.

[10] M. M. Blouke, B. Corrie, D. L. Heidtmann, F. H. Yang, M. Wizenread, M. L. Lust, H. H. Marsh IV and J. R. Janesick,
Large format, high resolution image sensors,
Opt. Eng. Vol. 26 No. 9, pp. 837–845, September 1987.

[11] M. M. Blouke, D. L. Heidtmann, B. Corrie, M. L. Lust and J. R. Janesick,
Large area CCD image sensors for scientific applications,
Solid State Imagers and their Applications, Proc. SPIE Vol. 591, pp. 117–122.

[12] M. M. Blouke, J. R. Janesick, J. E. Hall, M. W. Cowens and P. J. May,
800×800 charge-coupled device image sensor,
Opt. Eng. Vol. 22 No. 5, pp. 607–614, September/October 1983.

[13] M. M. Blouke, J. R. Janesick, S. T. Elliott, J. E. Hall, M. W. Cowens and P. J. May,
Current status of the 800×800 charge-coupled device image sensor,
Opt. Eng. Vol. 26 No. 9, pp. 864–874, September 1987.

[14] M. M. Blouke, F. H. Yang, D. L. Heidtmann and J. R. Janesick,
Traps and deferred charge in CCDs,
Instrumentation for Ground-Based Optical Astronomy, Proc. Ninth Santa Cruz Summer Workshop in Astronomy and Astrophysics, Lick Observatory, pp. 462–485, July 13–24, 1987.

[15] A. Boggess, F. A. Carr, D. C. Evans, D. Fischel, H. R. Freeman, C. F. Fuechsel, D. A. Klinglesmith, V. L. Krueger, G. W. Longanecker, J. V. Moore, E. J. Pyle, F. Rebar, K. O. Sizemore, W. Sparks, A. B. Underhill, H. D. Vitagliano, D. K. West, F. Macchetto, B. Fitton, P. J. Barker, E. Dunford, P. M. Gondhalekar, J. E. Hall, V. A. W. Harrison, M. B. Oliver, M. C. W. Sandford, P. A. Vaughan, A. K. Ward,

B. E. Anderson, A. Boksenberg, C. I. Coleman, M. A. J. Snijders and R. Wilson,
The IUE spacecraft and instrumentation,
Nature, No. 275, pp. 372–376, 1978.

[16] A. Boggess, R. C. Bohlin, D. C. Evans, H. R. Freeman, T. R. Gull, S. R. Heap, D. A. Klinglesmith, G. R. Longanecker, W. Sparks, D. K. West, A. V. Holm, P. M. Perry, F. H. Schiffer, B. E. Turnrose, C. C. Wu, A. L. Lane, J. L. Linsky, B. D. Savage, P. Benvenuti, A. Cassatella, J. Clavel, A. Heck, F. Macchetto, M. V. Penston, P. L. Selvelli, E. Dunford, P. Gondhalekar, M. B. Oliver, M. C. W. Sandford, D. Stickland, A. Boksenberg, C. I. Coleman, M. A. J. Snijders and R. Wilson,
In-flight performance of the IUE,
Nature, No. 275, pp. 377–385, 1978.

[17] G. D. Boreman,
Fourier spectrum techniques for characterization of spatial noise in imaging arrays,
Opt. Eng. Vol. 26 No. 10, pp. 985–991, October 1987.

[18] F. Bortoletto and M. D'Alessandro,
Universal CCD-controller system,
Rev. Sci. Instrum. Vol. 57 No. 2, pp. 253–258, February 1986.

[19] A. Bouere, J. Cretolle, B. Fort, R. Jouan, M. Gorisse, A. Lecomte, Y. Rio and L. Vigroux,
Description and performance of a charge-coupled device (CCD) camera,
Solid State Imagers for Astronomy, Proc. SPIE Vol. 290, pp. 142–143, 1981.

[20] W. S. Boyle and G. E. Smith,
Charge-coupled semiconductor devices,
Bell Syst. Tech. J. Vol. 49, pp. 587–593, 1970.

[21] R. A. Bredthauer, C. E. Chandler, J. R. Janesick, T. W. McCurnin and G. R. Sims,
Recent CCD technology developments,
Instrumentation for Ground-Based Optical Astronomy, Proc. Ninth Santa Cruz Summer Workshop in Astronomy and Astrophysics, Lick Observatory, pp. 486–492, July 13–24, 1987.

[22] J. D. Bregman and A. Doorduin,
New design concepts for compact CCD controllers,
Instrumentation in Astronomy VI, Proc. SPIE Vol. 627, pp. 616–623, 1986.

[23] J. D. Bregman and N. R. Waltham,
Basic design of compact CCD controllers for the William Herschel Telescope,
ESO-OHP Workshop on the Optimization of the use of CCD detectors in Astronomy Proceedings, ESO Conference and Workshop Proceedings No. 25, pp. 127–136, December 1986.

[24] B. E. Burke, R. W. Mountain, P. J. Daniels and D. C. Harrison,
420×420 Charge-coupled device imager and four-chip hybrid focal plane,
Opt. Eng. Vol. 26 No. 9, pp. 890–896, September 1987.

[25] C. J. Burrows (Ed.),
Wide Field and Planetary Camera 2 Instrument Handbook,
STScI publication (May 1994).

[26] G. S. Burley, S. Chapman, G. A. H. Walker and A. Parameswaran,
A Precisely Aligned CCD Mosaic,
Pub. A. S. P. Vol. 108, pp. 1024–1996, November 1996.

[27] D. Burt and J. Morcom,
Basic operation of a CCD frame transfer array, in
CCD Imaging (publication of EEV Ltd.), Technical Note 1, Issue 1, March 1982.

[28] D. Burt and J. Morcom,
CCD Type P8600 : 385×576 element area image sensor, in
CCD Imaging (publication of EEV Ltd.), Technical Note 2, Issue 2, August 1981.

[29] D. Burt and J. Morcom,
P8600 : Operation of output circuit, in
CCD Imaging (publication of EEV Ltd.), Technical Note 3, Issue 1, June 1982.

[30] D. Burt and J. Morcom,
P8600 Drive pulse buffers, in
CCD Imaging (publication of EEV Ltd.), Technical Note 4, Issue 1, August 1982.

[31] D. Burt and J. Morcom,
A guide to operation of the P8600, in
CCD Imaging (publication of EEV Ltd.), Technical Note 5, Issue 1, August 1982.

[32] D. Burt and J. Morcom,
P8600: Slow-scan operation, in
CCD Imaging (publication of EEV Ltd.), Technical Note 6, Issue 1, September 1982.

[33] D. Burt and J. Morcom,
P8600 : Epitaxial substrate version, in
CCD Imaging (publication of EEV Ltd.), Technical Note 7, Issue 1, July 1982.

[34] D. Carter, M. Irwin, R. McMahon, R. Terlevich,
A wide field CCD camera for the INT,
Response to Announcement of Opportunity, August 1990.

[35] V. Castellani,
Very large telescopes and stellar astrophysics,
Very Large Telescopes, their Instrumentation and Programs, Proc. IAU Colloquium No. 79, pp. 695–702, Garching, April 9–12, 1984.

[36] C. E. Chandler, R. A. Bredthauer, J. R. Janesick, J. A. Westphal and J. E. Gunn,
Sub-electron noise charge-coupled devices,
Charge-Coupled Devices and Solid State Optical Sensors, Proc. SPIE Vol. 1242, pp. 238–251, 1990.

[37] N. C. Chang,
Mosaic focal plane for star sensors,
Mosaic Focal Plane Methodologies, Proc. SPIE Vol. 244, pp. 32–45, 1980.

[38] P. C. Chen and J. Novello,
A General purpose CCD controller,
Pub. A. S. P. Vol. 101, pp. 940–946, October 1989.

[39] C. F. Claver, M. E. Cornell and C. B. Opal,
Evaluation of Texas Instruments TC215-32 CCD for astronomical imaging,
Instrumentation in Astronomy VII, Proc. SPIE Vol. 1235, pp. 253–262, 1990.

[40] M. J. Clayton,
Mosaic Imaging Detector System: Detector Control Language **DMAP**,
Documentation, Optical Science Laboratory, University College, University of London.

[41] L. Colquitt Jr., N. Bluzer and R. McKee,
Charge partition noise in charge-coupled devices,
Opt. Eng. Vol. 26 No. 10, pp. 992–998, October 1987.

[42] F. J. Cook and H. M. Luther,
Fibre-optic coupled solid state focal plane mosaic,
Mosaic Focal Plane Methodologies, Proc. SPIE Vol. 244, pp. 126–131, 1980.

[43] E. R. Craine, S. Forbes and J. S. Scott,
Very high resolution fast image digitization,
Medicine XIV/PACS IV, Proc. SPIE Vol. 626, pp. 386–391, 1986.

[44] P. Crane, A. Rose and P. Schabel,
The European Southern Observatory (ESO) charge-coupled device (CCD) camera system,
Solid State Imagers for Astronomy, Proc. SPIE Vol. 290, pp. 120–123, 1981.

[45] J.-C. Cuillandre, Y. Mellier, J.-P. Dupin, P. Tilloles, R. Murowinski, D. Crampton, R. Wooff and G. A. Luppino,
Wide-Field CCD Imaging at CFHT: The MOCAM Example,
Pub. A. S. P. Vol. 108, pp. 1120–1128, December 1996.

[46] M. Cullum, S. Deiries, S. D'Odorico and R. Reiß,
Spectroscopy to the atmospheric transmission limit with a coated GEC CCD,
L1–3, Astron. Astrophys., No. 153, 1985.

[47] M. J. Currie, P. T. Wallace and R. F. Warren-smith, *Starlink Standard Data Structures,*
Starlink General Paper 38.2, Starlink Project, January 1989.

[48] T. Daud, J. R. Janesick, K. Evans and S. T. Elliott,
Charge-coupled-device response to electron beam energies of less than 1keV up to

20keV,

Opt. Eng. Vol. 26 No. 8, pp. 686–691, August 1987.

[49] S. D'Odorico, T. Ducros, O. Iwert and R. Reiß,

Mini-workshop on large-size CCDs at ESO,

ESO Messenger, No. 65, pp. 43–45, September 1991.

[50] F. Diego,

Optical design of the University College London Échelle Spectrograph (UCLES),

Ph. D. thesis, University College, University of London, 1988.

[51] F. Diego, R. F. Griffin, J. Echevarría, R. G. Bingham and D. D. Walker,

CORAVEL,

Instrumentation in Astronomy VII, Proc. SPIE Vol. 1235, pp. 662–672, 1990.

[52] F. Diego and D. D. Walker,

On the possibility of increasing the throughput of astronomical spectrographs by overfilling the dispersing element,

Mon. Not. R.astr. Soc., Vol. 217, pp. 347–354, 1985.

[53] J. P. Doty, G. A. Luppino and G. R. Ricker,

Design of low noise, high performance x-ray charge-coupled device cameras,

Opt. Eng. Vol. 26 No. 10, pp. 1055–1060, October 1987.

[54] E. W. Dunham, R. L. Baron, J. L. Elliot, J. V. Vallerga, J. P. Dotty and G. R. Ricker,

A high-speed, dual-CCD imaging photometer,

Pub. A. S. P. Vol. 97, pp. 1196–1204, December 1985.

[55] M. E. Dunham and P. G. Sanchez,

Ultimate sensitivity and resolution of phosphor/fiber/charge-coupled device systems,

Opt. Eng. Vol. 26 No. 10, pp. 1035–1042, October 1987.

[56] A. Eckart, R. Hofmann, P. Duhoux, R. Genzel, S. Drapatz,

First results from SHARP at the NTT,

ESO Messenger, No. 65, pp. 1–2, September 1991.

[57] P. M. Epperson, J. V. Sweedler, M. Bonner Denton, G. R. Sims, T. W. McCurnin and R. S. Aikens,
Electro-optical characterization of the Tektronix TK512M-011 charge-coupled device,
Opt. Eng. Vol. 26 No. 8, pp. 715–724, August 1987.

[58] Fairchild CCD221 Preliminary data sheet, March 1979.

[59] A. C. Fish,
Advanced Detector and Control Systems for Optical Astronomy,
Ph. D. thesis, University College, University of London, 1990.

[60] A. C. Fish,
The control system for the UCL coudé échelle spectrograph,
Instrumentation for Ground-Based Optical Astronomy, Proc. Ninth Santa Cruz Summer Workshop in Astronomy and Astrophysics, pp. 628–637, Lick Observatory, July 13–24, 1987.

[61] J. L. A. Fordham, D. A. Bone and A. R. Jorden,
The UCL CCD-based image photon counting system,
Instrumentation in Astronomy VI, Proc. SPIE Vol. 627, pp. 206–212, 1986.

[62] J. L. A. Fordham,
Private communication, 1994.

[63] E. R. Fossum,
Architectures for focal plane image processing,
Opt. Eng. Vol. 28 No. 8, pp. 865–871, August 1987.

[64] A. Fowler, P. Waddell and L. Mortara,
Evaluation of the RCA 512×320 charge-coupled device (CCD) imager for astronomical use,
Solid State Imagers for Astronomy, Proc. SPIE Vol. 290, pp. 34–44, 1981.

[65] J. C. Geary and S. M. Kent,
Imaging characteristics of the RCA 512×320 charge-coupled device (CCD),
Solid State Imagers for Astronomy, Proc. SPIE Vol. 290, pp. 51–57, 1981.

[66] J. C. Geary, L. B. Robinson, G. R. Sims and R. A. Bredthauer,
Development of a 2048 × 2048 imager for scientific applications,
Charge-Coupled Devices and Solid State Optical Sensors, Proc. SPIE Vol. 1242, pp. 38–46, 1990.

[67] J. Gettys, R. Newman and R. Schleifler,
The Xlib C language X Interface,
Massachusetts Institute of Technology, 1987.

[68] L. E. Goad and W. F. Ball,
Charge-coupled device (CCD) detector utilization and development at Kitt Peak National Observatory (KPNO),
Solid State Imagers for Astronomy, Proc. SPIE Vol. 290, pp. 130–136, 1981.

[69] A. B. Grafinger and G. J. Michon,
Review of charge injection device (CID) technology,
Mosaic focal plane methodologies, Proc. SPIE Vol. 244, pp. 26–31, 1980.

[70] J. E. Gunn, M. Carr, G. E. Danielson, E. O. Lorenz, R. Lucinio, V. E. Nenow, J. Devere Smith, J. A. Westphal, D. P. Schneider and B. A. Zimmerman,
Four-shooter: a large format charge-coupled device camera for the Hale Telescope,
Opt. Eng. Vol. 26 No. 8, pp. 779–787, August 1987.

[71] J. E. Gunn, E. B. Emory, F. H. Harris and J. B. Oke,
The Palomar Observatory CCD camera,
Pub. A. S. P. Vol. 99, pp. 518–534, June 1987.

[72] J. E. Gunn and J. A. Westphal,
Care, feeding and use of charge-coupled device (CCD) imagers at Palomar Observatory,
Solid State Imagers for Astronomy, Proc. SPIE Vol. 291, pp. 16–23, 1981.

[73] W. Han,
New developments in mosaic CCDs,
Ph. D. thesis, University College, University of London, 1993.

[74] D. C. Harrison and B. E. Burke,
Large area focal plane comprising charge-coupled devices and fibre optics,
p897, Opt. Eng. Vol. 26 No. 9, September 1987.

[75] R. Hayes and D. L. Heidtmann,
Dual-channel charge-coupled device for high speed signal acquisition,
Opt. Eng. Vol. 26 No. 9, pp. 829–836, September 1987.

[76] J. M. Hill and M. P. Lesser,
Deployment of the MX spectrometer,
Instrumentation in Astronomy VI, Proc. SPIE Vol. 627, pp. 303–320, 1986.

[77] C. J. Hirst, D. D. Walker, F. Diego, A. C. Fish and A. Charalambous,
General philosophy for the control and data reduction for the Anglo-Australian and William Herschel Telescopes' échelle spectrographs,
Instrumentation in Astronomy VI, Proc. SPIE Vol. 627, pp. 721-729, 1986.

[78] P. Horowitz and W. Hill,
The art of electronics,
Cambridge University Press, 1980.

[79] S. M. Hsieh and H. H. Hosack,
Low light level imaging with commercial charge-coupled devices,
Opt. Eng. Vol. 26 No. 9, pp. 884–889, September 1987.

[80] *Lotus-Intel-Microsoft Expanded Memory Standard,*
Intel Corporation, part number 300275-004, August 1987.

[81] J. R. Janesick,
Charge-Coupled-Device Manufacture and Application,
(Editorial), Opt. Eng. Vol. 26 No. 9, pp. 827–828, September 1987.

[82] J. R. Janesick,
Charge-Coupled-Device and Charge-Injection-Device Theory and Application,
(Editorial), Opt. Eng. Vol. 26 No. 10, pp. 963–964, October 1987.

[83] J. R. Janesick and D. Campbell,
Quantum Efficiency model for the CCD flash gate,
Preprint, IEEE IEDM, 1986.

[84] J. R. Janesick, D. Campbell, S. T. Elliott and T. Daud,
Flash technology for charge-coupled-device imaging in the ultraviolet,
Opt. Eng. Vol. 29 No. 9, pp. 852–863, September 1987.

[85] J. R. Janesick and S. T. Elliott,
History and advancement of large area array scientific CCD imagers,
Proceedings of A. S. P. Conference, A. S. P. Conference Series, 1991. (Preprint).

[86] J. R. Janesick, S. T. Elliott, R. A. Bredthauer, C. E. Chandler and B. Burke,
Fano-noise-limited CCDs,
X-ray Instrumentation in Astronomy II, Proc. SPIE Vol. 982, pp. 71–95, 1988.

[87] J. R. Janesick, S. T. Elliott, R. A. Bredthauer, J. Cover, R. Schaefer and R. Varian,
Recent developments in large area scientific CCD image sensors,
Optical Sensors and Electronic Photography, Proc. SPIE Vol. 1071, pp. 115–133, 1989.

[88] J. R. Janesick, S. T. Elliott, S. A. Collins, T. Daud, D. Campbell and A. Dingizian,
CCD advances for X-ray scientific measurements in 1985,
X-ray instrumentation for astronomy, Proc. SPIE 1985. (Preprint).

[89] J. R. Janesick, S. T. Elliott, S. A. Collins, H. H. Marsh, M. M. Blouke and J. Freeman,
The future scientific CCD,
State of the Art Imaging Arrays and their Applications, Proc. SPIE Vol. 501, pp. 2–31, 1984.

[90] J. R. Janesick, S. T. Elliott, T. Daud and D. Campbell,
The CCD flash gate,
Instrumentation in astronomy VI, Proc. SPIE Vol. 627, pp. 543–582, 1986.

[91] J. R. Janesick, S. T. Elliott, T. Daud, J. McCarthy and M. M. Blouke,
Backside charging of the CCD,
Solid State Imaging Arrays, Proc. SPIE Vol. 570, pp. 46–79, 1985.

[92] J. R. Janesick, S. T. Elliott, A. Dingizian, R. A. Bredthauer, C. E. Chandler, J. A. Westphal and J. E. Gunn,
New advancements in charge-coupled device technology—sub-electron noise and 4096 × 4096 pixel CCDs,
Charge-Coupled Devices and Solid State Optical Sensors, Proc. SPIE Vol. 1242, pp. 223–237, 1990.

[93] J. R. Janesick, S. T. Elliott, G. Fraschetti, S. A. Collins, M. M. Blouke and B. Corrie,
Charge-coupled device pinning technologies,
Optical Sensors and Electronic Photography, Proc. SPIE Vol. 1071, pp. 153–169, 1989.

[94] J. R. Janesick, S. T. Elliott, J. McCarthy, H. H. Marsh, S. A. Collins and M. M. Blouke,
Present and future CCDs for UV and X-ray scientific measurements,
X-ray instrumentation for astronomy, Proc. SPIE 1985. (Preprint).

[95] J. R. Janesick, S. T. Elliott and F. Pool,
Radiation damage in scientific charge-coupled devices,
IEEE 1988 nuclear science symposium. (Preprint).

[96] J. R. Janesick, J. Hynecek and M. M. Blouke,
Virtual phase imager for Galileo,
Solid State Imagers for Astronomy, Proc. SPIE Vol. 290, pp. 165–173, 1981.

[97] J. R. Janesick, K. Klaasen and S. T. Elliott,
Charge-coupled-device charge-collection efficiency and the photon transfer technique,
Opt. Eng. Vol. 26 No. 10, pp. 972–980, October 1987.

[98] P. R. Jorden,
CCDs Past, Present and Future,
Gemini, The Newsletter of the Royal Greenwich Observatory, No. 27, pp. 20–23, March 1990.

[99] P. R. Jorden,
CCDs for the 1990s,
New Windows to the Universe, pp. 465–481, Ed. F. Sanchey, Cambridge University Press, 1990.

[100] P. R. Jorden,
An EEV large-format CCD camera on the WHT ISIS spectrograph,
Instrumentation in Astronomy VII, Proc. SPIE Vol. 1235, pp. 790–798, 1990.

[101] P. R. Jorden and I. G. Van Breda,
The Royal Greenwich Observatory (RGO) charge injection device camera system,
Solid State Imagers for Astronomy, Proc. SPIE Vol. 290, pp. 113–119, 1981.

[102] B. W. Kernigan and D. M. Richie,
The C Programming Language,
Prentice Hall, 1978.

[103] B. W. Kernigan and D. M. Richie,
The C Programming Language,
Second Edition, Prentice Hall, 1988.

[104] C. R. Kitchin,
Astrophysical Techniques,
Adam Hilger, 1984.

[105] D. E. Knuth,
Computer Modern Typefaces,
American Mathematical Society and Addison Wesley, 1986.

[106] D. E. Knuth,
The METAFONT*book,*
American Mathematical Society and Addison Wesley, 1986.

[107] D. E. Knuth,
The TEXbook,
American Mathematical Society and Addison Wesley, 1984.

[108] F. Lacombe, D. Rouan, D. Stefanovitch, B. Talureau, J. Berezné, G. Epstein, S. Pau, D. Phan Van, Y. Zéau,
Qualifying a mosaic of detectors for infrared astronomy,
Very Large Telescopes, their Instrumentation and Programs, Proc. IAU Colloquium No. 79, pp. 603–606, Garching, April 9–12, 1984.

[109] L. Lamport,
LaTeX: A document preparation system,
Addison Wesley, 1986.

[110] EG&G Reticon Advertising,
p81, *Laser Focus World,* Vol. 27, No. 11 November 1991.

[111] R. W. Leach,
Characteristics of four thinned TI 800×800 CCDs,
Pub. A. S. P. Vol. 100, pp. 853–858, July 1988.

[112] R. W. Leach,
Low-light-level performance of a TI 800×800 CCD,
Pub. A. S. P. Vol. 100, pp. 1162–1168, September 1988.

[113] R. W. Leach,
Design of a CCD controller optimized for mosaics,
Pub. A. S. P. Vol. 100, pp. 1287–1295, October 1988.

[114] R. W. Leach,
Operating a digital signal processor CCD camera under UNIX,
Proceedings of the CCDs in Astronomy Conference, A. S. P. Conference Series, No. 8, pp. 171–179, 1990.

[115] R. W. Leach and F. L. Beale,
Design and operation of a multiple readout CCD camera controller,
Instrumentation in Astronomy VII, Proc. SPIE Vol. 1235, pp. 284–293, 1990.

[116] R. W. Leach and H. Gursky,
The cosmic ray background in charge-coupled devices,
Harvard Smithsonian Center for Astrophysics Preprint series, No. 1196, September 1979.

[117] R. Lee and J. A. Tyson,
A Large Area CCD Imaging System,
Instrumentation for Ground-Based Optical Astronomy, Proc. Ninth Santa Cruz Summer Workshop in Astronomy and Astrophysics, pp. 742–748, Lick Observatory, July 13–24, 1987.

[118] M. Lesser,
Antireflection coatings for silicon charge-coupled devices,
Opt. Eng. Vol. 26 No. 9, pp. 911–915, September 1987.

[119] J. Lequeux,
Interstellar matter with very large telescopes,
Very Large Telescopes, their Instrumentation and Programs, Proc. IAU Colloquium No. 79, pp. 675–678, Garching, April 9–12, 1984.

[120] G. A. Luppino, R. A. Bredthauer and J. C. Geary,
Design of an 8192 × 8192 pixel CCD mosaic,
Instrumentation in Astronomy VIII, Proc. SPIE Vol. 2198, pp. 810–820, 1994.

[121] G. A. Luppino and K. R. Miller,
A Modular Dewar Design and Detector Mounting Strategy for Large-Format, Astronomical CCD Mosaics,
Pub. A. S. P. Vol. 104, pp. 215–222, March 1992.

[122] C. D. Mackay,
Charge-coupled devices in astronomy,
Ann. Rev. Astron. Astrophys. Vol. 24, pp. 255–283, 1986.

[123] C. D. Mackay,
The British General Electric Company charge-coupled device (CCD) development program,
Solid State Imagers for Astronomy, Proc. SPIE Vol. 290, p159, 1981.

[124] I. S. McLean,
Electronic and Computer-Aided Astronomy,
Ellis Horwood Ltd., 1989.

[125] I. S. McLean, W. A. Cormack, J. T. Herd and C. Aspin,
The Royal Observatory Edinburgh (ROE) charge-coupled device (CCD) camera system,
Solid State Imagers for Astronomy, Proc. SPIE Vol. 290, pp. 155–158, 1981.

[126] S. Marcus, R. Nelson, R. Lynds,
Preliminary evaluation of a Fairchild CCD-211 and a new camera system,
Instrumentation in Astronomy III, Proc. SPIE Vol. 172, pp. 207–236, 1979.

[127] J. Meaburn,
Detection and Spectrometry of Faint Light,
D. Reidel, Dordrecht, Holland, 1976.

[128] Y. Mellier, M. Cailloux, J. P. Dupin, B. Fort, C. Lours, J. P. Picat and P. Tilloles,
Evaluation of the performance of the 576 384 Thomson CCD for astronomical use,
Astron. Astrophys. Vol. 157, pp. 96–100, 1986.

[129] D. G. Monet,
The USNOFS CCD array sensor,
Proceedings of the CCDs in Astronomy Conference, A. S. P. Conference Series, No. 8, pp. 11–17, 1990.

[130] P. Moore,
The story of astronomy,
Fifth edition, Macdonald and Jane, 1977.

[131] A. F. M. Moorwood,
Star formation,
Very Large Telescopes, their Instrumentation and Programs, Proc. IAU Colloquium No. 79, pp. 679–693, Garching, April 9–12, 1984.

[132] L. Mortara and A. Fowler,
Evaluations of charge-coupled device (CCD) performance for astronomical use,
Solid State Imagers for Astronomy, Proc. SPIE Vol. 290, pp. 28–33, 1981.

[133] J. Murray,
Starlink C Programming Standard,
Starlink General Paper 4, May 1991.

[134] D. D. Norris, M. M. Blouke, J. R. Janesick, P. J. May and D. McGrath,
Progress in 800×800 charge-coupled device (CCD) imager development and applications,
Mosaic Focal Plane Methodologies II, Proc. SPIE Vol. 311, pp. 42–45, 1981.

[135] J. B. Oke,
Low and moderate resolution spectroscopy with an RCA charge-coupled device (CCD),
Solid State Imagers for Astronomy, Proc. SPIE Vol. 290, pp. 45–50, 1981.

[136] J. B. Oke,
The nature of galaxies and clusters of galaxies at very large distances,
Very Large Telescopes, their Instrumentation and Programs, Proc. IAU Colloquium No. 79, pp. 713–719, Garching, April 9–12, 1984.

[137] *Instruction Manual, Infrared Detector Cryostat MN1815INV,*
Oxford Instruments Limited, July 1984.

[138] I. R. Parry and P. M. Gray,
An automated multiobject fibre optic coupler for the Anglo-Australian Telescope,
Instrumentation in Astronomy VI, Proc. SPIE Vol. 627, pp. 118–122, 1986.

[139] M. A. C. Perryman, C. L. Foden and A. Peacock,
Optical Photon counting using superconducting tunnel junctions,
Nuclear Instruments and Methods in Physics Research, pp. 319–325, A325, 1993.

[140] *PDOS Programmer's Reference Manual,*
First edition, Force Computers Inc., June 1984.

[141] *PDOS C 68000 Programmer's Reference Manual,*
Eyring Research Institute, Inc., 1984.

[142] S. W. Petrick,
Generalized approach to cooling charge-coupled devices using thermoelectric coolers,
Opt. Eng. Vol. 26 No. 10, pp. 965–971, October 1987.

[143] Philips technical publication 150,
The frame transfer sensor.

[144] Philips technical publication 211,
The frame transfer sensor,
(Update of T. P. 150), April 1986.

[145] P. J. Pool, W. A. F. Suske, J. E. U. Ashton and S. R. Browning,
Design aspects and characterisation of EEV large area CCDs for scientific and medical applications,
Charge-Coupled Devices and Solid State Optical Sensors, Proc. SPIE Vol. 1242, pp. 17–25, 1990.

[146] C. S. Powell,
Mirroring the cosmos,
Scientific American, Vol. 265, No. 5, pp. 80–89, 1991.

[147] A. S. Radley,
An investigation into some aspects of the development of a large scale CCD mosaic imaging system for use in space applications,
M. Sc. dissertation, University College, University of London, 1991.

[148] RCA SID-006EX preliminary data sheet.

[149] RCA SID-504 Solid State Image Sensor, Data sheet, RCA, Lancaster, Pennsylvania, USA, September 1984.

[150] N. Rees, C. Mackay and M. Disney,
Parallel observing—how to get unlimited observing time on a large optical telescope,
Instrumentation in Astronomy VII, Proc. SPIE Vol. 1235, pp. 459–465, 1990.

[151] R. Reiß,
Array Control Electronics (ACE) ESO's next generation of CCD Controllers for the Very Large Telescope,
Instrumentation in Astronomy VIII, Proc. SPIE Vol. 2198, pp. 895–906, 1994.

[152] R. Reiß, H. Bauer, S. Deiries, S. D'Odorico and A. Longinotti,
Buttable optical CCD mosaics: concept and first results at the European Southern Observatory, New Technologies for Astronomy, Proc. SPIE Vol. 1130, pp. 152–165, 1989.

[153] L. B. Robinson,
The Lick Observatory charge-coupled device (CCD) and controller,
Solid State Imagers for Astronomy, Proc. SPIE Vol. 290, pp. 124–129, 1981.

[154] L. B. Robinson, W. E. Brown, D. K. Gilmore, R. J. Stover, M.-Z. Wei and J. C. Geary,
Characteristics of large Ford and Reticon CCDs,
Instrumentation in Astronomy VII, Proc. SPIE Vol. 1235, pp. 315–325, 1990.

[155] L. B. Robinson, R. J. Stover, J. Osborne, J. S. Miller, S. S. Vogt and S. L. Allen,
Lick Observatory charge-coupled device data acquisition system,
Opt. Eng. Vol. 26 No. 8, pp. 795–805, August 1987.

[156] A. W. Rodgers, J. Van Harmelen, D. King, P. Conroy and P. Harding,
Large-format photon counting arrays,
Pub. A. S. P. Vol. 100, pp. 841–852, July 1988.

[157] *Royal Observatory Edinburgh, research and facilities handbook 1989,*
Royal Observatory, Edinburgh, 1989.

[158] R. Schleifler and R. Newman,
The X Window System Protocol,
Massachusetts Institute of Technology, 1987.

[159] P. Seige and G. Ress,
Application of Texas Instruments TC-104 linear charge-coupled device arrays in spaceborne camera systems,
Opt. Eng. Vol. 26 No. 10, pp. 1029–1034, October 1987.

[160] M. Sekiguchi, H. Iwashita, M. Doi, N. Kashikawa and S. Okamura,
Development of a 2000×8144-Pixel Mosaic CCD Camera,
Pub. A. S. P. Vol. 104, pp. 744–751, September 1992.

[161] C. J. Skinner,
Infrared spectroscopy and circumstellar matter,
Ph. D. thesis, University College, University of London, 1987.

[162] R. M. Smith,
CCD controller technology for 1990,
Proceedings of the CCDs in Astronomy Conference, A. S. P. Conference Series, No. 8, pp. 153–164, 1990.

[163] R. M. Smith,
CTIO Array Controller Preliminary Data,
NOAO, Tuscon, USA, June 1990.

[164] R. A. Stern, R. C. Catura, P. Kimble, A. F. Davidsen, M. Wizenread, M. M. Blouke, R. Hayes, D. M. Walton and J. L. Culhane,
Ultraviolet and extreme ultraviolet response of charge-coupled device detectors,
Opt. Eng. Vol. 26 No. 9, pp. 875–883, September 1987.

[165] R. A. Stern, K. Liewer and J. R. Janesick,
Evaluation of a virtual phase charge-coupled device as an imaging x-ray spectrometer,
Rev. Sci. Instrum. Vol. 54 No. 2, pp. 198–205, February 1983.

[166] R. J. Stover and S. L. Allen,
A high-speed CCD photometer,
p877, Pub. A. S. P. Vol. 99, August 1987.

[167] R. J. Stover, W. E. Brown, D. K. Gilmore and M. Wei,
Characterization of a 4Kx2K Three-Side Buttable CCD,
Instrumentation in Astronomy VIII, Proc. SPIE Vol. 2198, pp. 803–809, 1994.

[168] H. J. Strasler,
Modular high density focal plane concepts,
Mosaic Focal Plane Methodologies, Proc. SPIE Vol. 244, pp. 68–74, 1980.

[169] N. Takato, T. Aoki, S. Ichikawa and M. Iye,
Performance of Japan TI CCD housed in a microminiature refrigerator,
Instrumentation in Astronomy VII, Proc. SPIE Vol. 1235, pp. 242–252, 1990.

[170] Tektronix preliminary data sheet, July 1985.

[171] R. Terlevich,
Outline proposal for INT prime focus quantitative survey instrument,
private communication, 1990.

[172] Texas Instruments data sheet for 4849 CCD imager, November 1984.

[173] Texas Instruments data sheet for VP1M imager, April 1985.

[174] Thomson-CSF data sheet DTE 119 A,
Dispositifs photosensibles matriciels à transfert de charge (DTC),
Area array charge-coupled device (CCD) image sensors.

[175] Thomson-CSF data sheet for TH7861, TEV 3502, July 1983.

[176] Thomson-CSF data sheet for TH7852, TEV 3513, October 1983.

[177] Thomson-CSF data sheet for THX 31156, October 1989.

[178] M. L. Tincknell, S. I. Chase, T. Dinh, J. W. Harris and L. Teitelbaum,
Fast megapixel charge-coupled device image acquisition and analysis system for high energy nuclear physics,
Opt. Eng. Vol. 26 No. 10, pp. 1067–1076, October 1987.

[179] J. A. Tyson,
Low-light-level charge-coupled device imaging in astronomy,
J. Opt. Soc. Am. A. Vol. 3 No. 12, pp. 2131–2138, December 1986.

[180] J. A. Tyson,
The shift-and-stare technique and a large area CCD mosaic,
Proceedings of the CCDs in Astronomy Conference, A. S. P. Conference Series, No. 8, pp. 1–10, 1990.

[181] *United Kingdom Infrared Telescope, Annual Report 1990*
Royal Observatory, Edinburgh, 1990.

[182] M.-H. Ulrich,
Uses of very large telescopes for galaxy research,

Very Large Telescopes, their Instrumentation and Programs, Proc. IAU Colloquium No. 79, pp. 703–711, Garching, April 9–12, 1984.

[183] P. Waddell and C. Christian,
Evaluation of the RCA 640×1024 charge-coupled-device imager for astronomical use,
Opt. Eng. Vol. 26 No. 8, pp. 734–741, August 1987.

[184] P. T. Wallace,
Starlink Application Programming Standard, Starlink General Paper 16, June 1990.

[185] A. R. Walker,
TODE, the CCD data acquisition program,
UCL SAAO documentation, December 1982.

[186] D. D. Walker,
Advances in building a matrix of CCDs and in the readout architecture for economic large-area imagers, case for support,
Application for SERC research grant, December 1986.

[187] D. D. Walker,
Preliminary design study of the spectrograph for the Columbia University Wide Field Spectrographic Telescope,
Study report commissioned by the University of Columbia, 1989.

[188] D. D. Walker,
Private communication, 1991.

[189] D. Walker, F. Diego, M. Barlow and I. Crawford,
The ultra-high resolution facility for the UES—a design study,
Response to ING AO, April 1991.

[190] D. Walker, F. Diego and S. Unger,
The short camera for the UES—a design study,
Response to ING AO, April 1991.

[191] D. Walker, P. Sandford, A. Lyons, D. Bone, A. Walker and A. Bokesenberg,
The UCL charge-coupled device camera at the South African Astronomical Observatory,
Advances in electronics and electron physics, Vol. 64A, pp. 185–192, 1985.

[192] D. Walker, R. G. Bingham and F. Diego,
Échelle spectrographs for 8m-class telescopes,
Instrumentation in Astronomy VII, Proc. SPIE Vol. 1235, pp. 535–549, 1990.

[193] D. D. Walker, F. Diego, A. Charalambous, C. J. Hirst and A. C. Fish,
High resolution échelle spectrographs for the Anglo-Australian Telescope coudé focus and William Herschel Telescope Nasmyth focus,
Instrumentation in Astronomy VI, Proc. SPIE Vol. 627, pp. 291–302, 1986.

[194] G. A. H. Walker,
Astronomical observations, an optical perspective,
Cambridge University Press, 1987.

[195] N. R. Waltham, I. G. Van Breda and G. M. Newton,
A simple Transputer-based CCD camera controller,
Instrumentation in Astronomy VII, Proc. SPIE Vol. 1235, pp. 328–337, 1990.

[196] E. J. Wampler,
Thoughts about Very Large Telescopes,
Very Large Telescopes, their Instrumentation and Programs, Proc. IAU Colloquium No. 79, pp. 3–8, Garching, April 9–12, 1984.

[197] W.-L. Wang, L. R. Hudson and H.-F. Tseng,
High performance visible and near-infrared charge-coupled device array for spectroscopy applications,
Opt. Eng. Vol. 26 No. 9, pp. 844–851, September 1987.

[198] R. F. Warren-Smith,
NDF Routines for Accessing the Extensible N-Dimensional Data Format,
Starlink User Note 33.3, Starlink Project, December 1991.

[199] D. C. Wells and E. W. Greisen,
FITS: A Flexible Image Transport System,

Proceedings of International Workshop on Image Processing in Astronomy, Trieste, Italy, 1979.

[200] D. C. Wells, E. W. Greisen and R. H. Harten,
FITS: A Flexible Image Transport System,
Astron. Astrophys. Suppl. Ser. Vol. 44, pp. 363–370, 1981.

[201] J. A. Westphal and the WF/PC Investigation Definition Team,
The wide field/planetary camera,
The Space Telescope Observatory, NASA Publication CP-2244, pp. 28–39, 1982.

[202] M. H. White, D. R. Lampe, F. C. Blaha and I. A. Mack,
Characterisation of surface channel CCD image arrays at low light levels,
IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 1, February 1974.

[203] J. T. Williams and D. Weistrop,
MOSAIC (Mosaicked Optical Self-scanned Array Imaging Camera),
Proc. SPIE Vol. 290, pp. 204–211, 1981.

[204] J. F. Wright and C. D. Mackay,
The Cambridge charge-coupled device (CCD) System,
Solid State Imagers for Astronomy, Proc. SPIE Vol. 290, pp. 160–164, 1981.