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Built-in Reliability Design of Highly Integrated Solid-State Power Switches With Metal Bump Interconnects

Jianfeng Li, Alberto Castellazzi, *Member, IEEE*, Tianxiang Dai, Martin Corfield, Adane Kassa Solomon, and Christopher Mark Johnson, *Member, IEEE*

***Abstract*—A stacked substrate–chip–bump–chip–substrate assembly has been demonstrated in the construction of power switch modules with high power density and good electrical performance. In this paper, special effort has been devoted to material selection and geometric shape of the bumps in the design for improving the thermomechanical reliability of a highly integrated bidirectional switch. Results from 3-D finite-element simulation indicate that for all design cases the maximum von Mises stresses and creep strain accumulations occur in the solder joints used to join bumps on IGBTs during a realistic mission profile, but occur in the solder joints used to join bumps on DBC substrates during accelerated thermal cycling. The results from both the simulation and the accelerated thermal cycling experiments reveal that selection of Cu/Mo/Cu composite brick bumps in the stacked assembly can significantly improve the thermomechanical reliability of both the solder joints and the DBC substrates when compared to Cu cylinder bumps and Cu hollow cylinder bumps reported in previous work. Such results can be attributed to the effective reduction in the extent of mismatch of coefficients of thermal expansion between the different components in the assembly.**

***Index Terms*—Cu/Mo/Cu composite, finite-element (FE) method, integration, thermal cycling, wirebond-less packaging.**

I. Introduction

WIRE-BOND interconnect technology is the standard method that has widely been used to achieve the electrical interconnects on the front side of power devices in power modules. However, wire bonds have limited ability to dissipate heat and have relatively high parasitic inductance, which often restricts the thermal and electrical performance of the power modules. To overcome this problem, several replacements of wire bonds, such as ribbon bond [1], dimple array [2], embedded chip technology [3]–[5], silicon interposer [6], solder bump [7], metal bump [8]–[12], and press-pack bus-bar-like interconnects [13] have been proposed and investigated over the past years. Of them, metal bump interconnects, also called solid interconnect posts, have been demonstrated not only to obtain dramatic improvement in the thermal and electromagnetic performance, but also allow advanced integration schemes, e.g., stacked devices, for the optimization of basic power switch topologies, e.g., half bridge switch and bidirectional switch [14]–[16]. However, further investigation of reliability and manufacturability for the implementation of this technology is still needed for wider acceptance and generalization.

Manuscript received April 1, 2014; revised July 28, 2014; accepted September 2, 2014. Date of publication September 11, 2014; date of current version December 23, 2014. This work was supported by Innovative Electronics Manufacturing Research Centre (IeMRC) funded by the U.K. Engineering and Physical Sciences Research Council (EPSRC) through research Grant EP/H03014X/1. Recommended for publication by Associate Editor M. Saeedifard.

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Digital Object Identifier 10.1109/TPEL.2014.2357334

Metal bumps (or posts) may be formed using double etching and electroplating and joined using bonding technology [8]–[12]. Haque *et al.* [8] used Cu brick posts and soldering technology to develop a metal posts interconnected parallel structure power module. Their results demonstrated the improved electrical performance of the developed power module when compared to corresponding Al wire bonded power modules. Johnson *et al.* [9] created Cu posts on direct bond copper substrates using a double etching process. The posts were created to make contact on the top side of power devices for assembling a sandwich structure power module with low parasitic inductances. Zeanh *et al.* [10] investigated the thermomechanical reliability of an insulated gate bipolar transistor (IGBT) module constructed with Cu cylinder bumps and soldering technology, and identified the solder joints used to bond the bumps as thermomechanically weak points. Menager *et al.* [11] deposited brick-like Cu microposts on the top sides of power diodes, and achieved good electrical connection for a 3-D packaging of power modules. Lee *et al.* [12] prepared deposited cylindrical Cu bumps and microstud structure on Si wafers for Cu–Cu 3-D packaging, and then, used electroless Ni plating to compensate for the bump height variation. Solomon *et al.* [14]–[16] used Cu brick and Cu hollow cylinder bumps to develop highly integrated bidirectional switch and half bridge switch modules, and obtained dramatic improvements in the thermal and electromagnetic performance.

This paper is concerned with the thermomechanical reliability of a stacked substrate–chip–bump–chip–substrate assembly that has been constructed with soldering technology for implementation of a highly integrated bidirectional power switch. In a previous preliminary study [17], such a stacked assembly was designed based on a surface soldered Cu bump approach. The 3-D finite-element (FE) modeling had been employed to simulate the thermomechanical response of the designed assembly under a realistic mission profile, with considerations of two types of bumps, solid and hollow cylinder Cu bumps, and three types of substrates, Al_2O_3, Si_3N_4, and AlN-based substrates. The simulation results indicated that the effect of the two types of bumps

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on the thermal performance is negligible, while the AlN-based substrates offered the best thermal performance when compared to Si_3N_4 and Al_2O_3-based substrates, respectively. However, the solder joints for bonding the bumps on the IGBTs are the thermomechanical weak points with the maximum creep strain accumulation. The combination of Si_3N_4-based substrates with hollow cylinder bumps can slightly reduce the creep strain accumulation in the critical solder joints when compared to the other combinations of Al_2O_3 and AlN-based substrates with both the solid and hollow cylinder bumps.

This paper presents an extended and more comprehensive FE modeling approach to optimize the thermomechanical performance of the stacked bidirectional power switch assembly. First, both pure Cu and Cu/Mo composite were selected as the bump materials, with brick, cylinder, and hollow cylinder (with different wall thickness), for the geometric bump shapes. Then, 3-D FE modeling will be used to simulate and compare the thermomechanical response of the stacked assemblies designed using the different bumps under not only a mission profile but also an accelerated thermal cycling test between -55 and $+150$ °C. In addition, the FE simulation results will be evaluated against the accelerated thermal cycling test from two stacked assembly samples constructed with hollow cylinder Cu bumps and brick Cu/Mo/Cu composite bumps.

The main objectives of this paper are: 1) to summarize the FE simulation results that may be used for optimization of the thermomechanical performance of power modules; 2) to compare the different thermomechanical response of the stacked assemblies under the mission profile and accelerated thermal cycling tests; 3) to demonstrate the equivalent importance of both geometric bump shape and selection of material for achieving improved thermomechanical reliability of stacked assemblies; and 4) to evaluate the FE simulation results with those of the thermal cycling experiments.

II. Design Consideration

A. Overall Design

As reported in the previous preliminary study [17], the stacked assembly of substrate–chip–bump–chip–substrate has been designed for implementing a bidirectional switch constructed with 70-μm-thin IGBTs and diodes, rated at 200 A–600 V, as shown in Fig. 1, in which their front metallization has been treated with a NiP/Pd finish to aid solderability. The footprint of one IGBT is $10 \times 9.5 \times 0.07$ mm, and that of one diode is $9.5 \times 5.5 \times 0.07$ mm. In the designed assembly as shown in Fig. 2, the front side (with conductor circuit tracks) of both the top and bottom substrates are used for attaching one IGBT and one diode and provide terminals for gate and emitter contact for the IGBT attached on the opposite substrate. With this assembly, the backside of both substrates can function as primary cooling surfaces for achieving double-sided cooling. AlN-based substrates are selected for both the top and bottom substrates, which consist of 0.3-mm-thick direct bonded Cu (DBC) on 1-mm-thick AlN ceramic tiles. The bumps A (as shown in Fig. 2) are used to provide the electrical interconnects between the IGBTs and the opposite diodes. The bumps B are used to provide the electrical interconnects between the IGBTs and the opposite substrates. The bumps C are used to connect the gate signals of the IGBTs from the opposite substrates. In addition, the bumps D are used to achieve all inputs, outputs, and signals of the switch to be terminated on one substrate, and provide additional mechanical support to the assembly.

B. AlN-Based Substrates

As mentioned previously, AlN-based substrates offer better thermal performance when compared to Si_3N_4 and Al_2O_3-based substrates in a stacked assembly under the same mission profile [17]. For example, provided that other conditions are identical, the highest maximum temperature in the assembly during the mission profile for 1-mm-thick AlN ceramic tiles (used in DBC substrates) are approximately 12 °C and 22 °C lower than those for 0.3-mm-thick Si_3N_4 ceramic tiles and 0.4-mm-thick Al_2O_3 ceramic tiles, respectively. Furthermore, as presented later, two soldering steps have been used to assemble the present samples. The 1-mm-thick AlN tiles used in the substrates can reduce the bending deformation of the substrates down to lower than 20 μm after the first soldering step, while 0.3-mm-thick Si_3N_4 ceramic tiles and 0.4-mm-thick Al_2O_3 ceramic tiles used in the substrates lead to corresponding bending deformation higher than 100 μm. Therefore, AlN-based substrates are more suitable for manufacturing the designed switch module, and are hence, selected for both the top and bottom substrates.

C. Bump Shapes and Selection of Materials

Five types of bumps consisting of pure Cu or Cu/Mo composite as shown in Fig. 3 have been considered to investigate the effects of bump shapes and selection of materials on the thermal performance and the thermomechanical reliability of the stacked assemblies. In Fig. 3, L is length, W is width, H is height, ϕ is diameter, and t is thickness. Furthermore, several ratios of t to ϕ or t to H for the Cu hollow cylinder bump, the Cu/Mo shell/core composite cylinder bump and the Cu/Mo/Cu composite brick bump have also been taken into account. The dimensons of the bumps A, B, C, and D shown in Fig. 2 for all the considerations of bump shapes and selection of materials are listed in Table I. For each of the design cases listed in Table I, the ratio of t to ϕ or t to H for all bumps A, B, C, and D has remained a constant. These dimensions have been selected to ensure both sufficient insulating distance between the electrodes of the IGBTs and diodes in the assemblies and relative convenience for manufacturing. For example, commercially available or custom prepared Cu rods, tubes, and plates can be used to cut or machine into Cu cylinders, Cu hollow cylinders, and Cu brick bumps, respectively. The shell/core Cu/Mo rods can be formed using metal wire drawing technology, and then, cut into Cu/Mo composite cylinder bumps. The Cu/Mo/Cu plates can be produced using combined rolling and diffusion bonding process, and then, stamped into the Cu/Mo/Cu composite brick bumps.

D. Solder Joints

All the IGBT and diode attachments and bump interconnects are made with Sn-3.5Ag solder joints, and therefore,

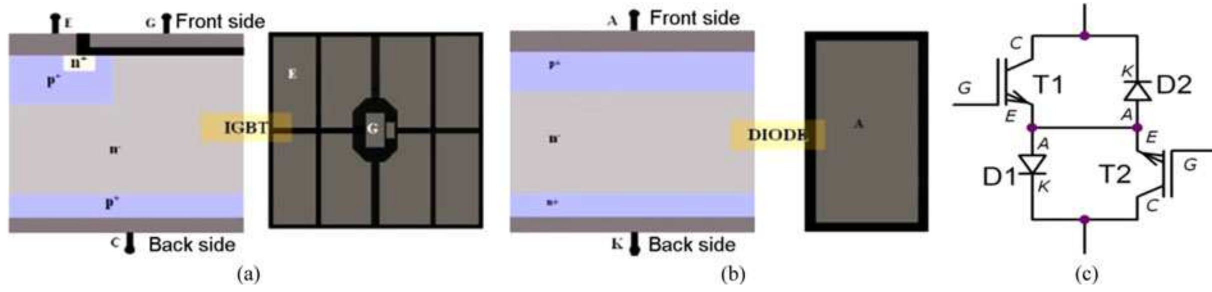

Fig. 1. Photographs of the 70-μm thin: (a) IGBT and (b) diode chips; and (c) the schematic of the bidirectional power switch designed with two IGBTs and two diodes.

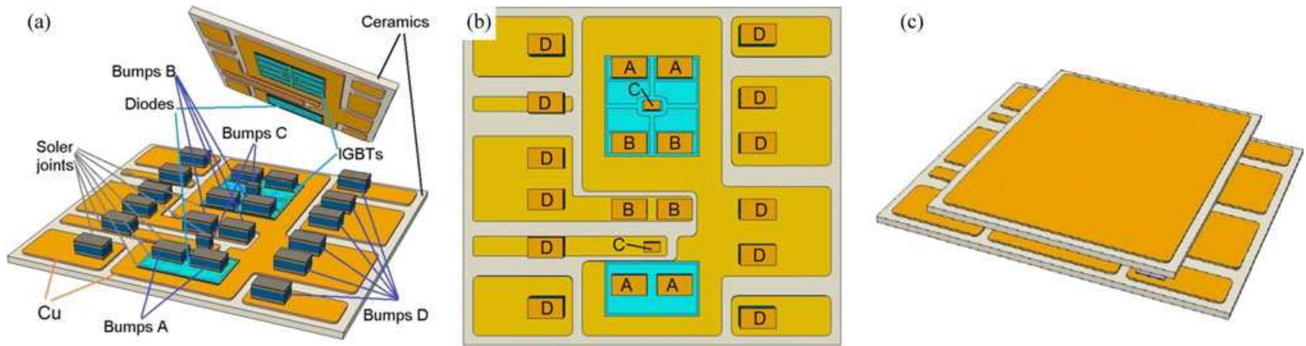

Fig. 2. Stacked assembly of substrate–chip–bump–chip–substrate for the bidirectional switch: (a) open view of the assembly with Cu/Mo/Cu composite brick; (b) top view of part of the assembly showing the layout of bumps A, B, C, and D; and (c) closed view showing one entire assembly.

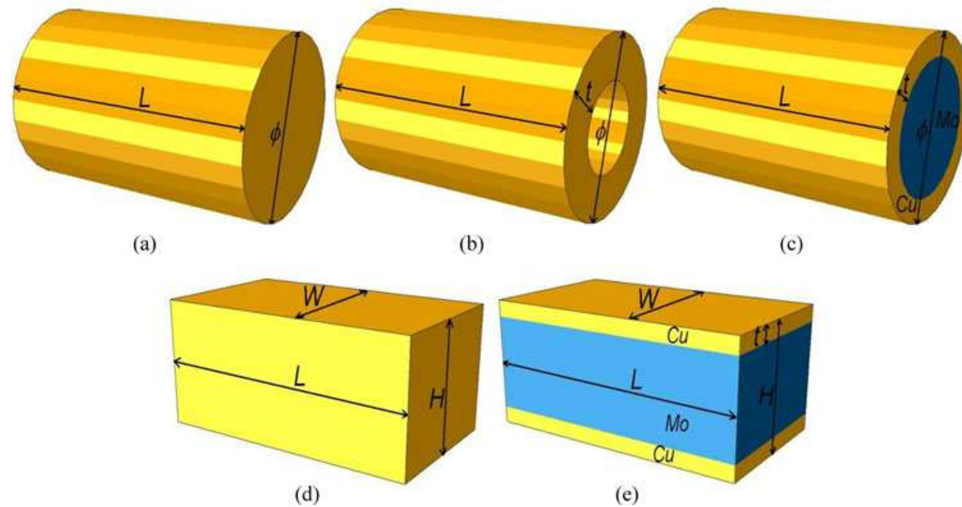

Fig. 3. Three-dimensional schematic diagrams of the five types of bumps considered in this paper: (a) Cu cylinder bump; (b) Cu hollow cylinder bump; (c) Cu/Mo shell/core composite cylinder bump; (d) Cu brick bump; and (e) Cu/Mo/Cu composite brick bump.

eliminate the need for standard wire bond packaging technology. For attaching the IGBTs and diodes on the substrates, the Sn-3.5Ag solder joints have been designed to be 0.1 mm in thickness. For joining the bumps to the chips and/or to the substrates, the Sn-3.5Ag solder joints follow the shapes of the bumps, with a minimum thickness of 0.1 mm. It should be pointed out that the shapes of the solder joints shown in Fig. 2 are ideal approximations for subsequent FE modeling and simulation, and those of the actually reflowed solder joints may vary somewhat.

E. Assembling Process

With automatic machines and/or suitable jigs for positioning the devices and bumps, the stacked substrate–chip–bump–chip–substrate assembly may be assembled using a single soldering

TABLE I
TYPES, DIMENSIONS AND THE CORRESPONDING CODES FOR THE BUMP SHAPES AND SELECTION OF MATERIALS CONSIDERED IN THE DESIGN OF THE STACKED SUBSTRATE–CHIP–BUMP–CHIP–SUBSTRATE ASSEMBLY

	Design case	Bump type	$L \times W \times H$ or $L \times \phi$ in mm				t/ϕ or t/H
			Bump A	Bump B	Bump C	Bump D	
a	CC	Cu cylinder	3×1.8	3×2.1	1.5×2.1	3×2.1	
	CHC25	Cu hollow cylinder	3×1.8	3×2.1	1.5×2.1	3×2.1	0.25
b	CHC13	Cu hollow cylinder	3×1.8	3×2.1	1.5×2.1	3×2.1	0.13
	CHC07	Cu hollow cylinder	3×1.8	3×2.1	1.5×2.1	3×2.1	0.07
c	CMC13	Cu/Mo cylinder	3×1.8	3×2.1	1.5×2.1	3×2.1	0.13
	CMC07	Cu/Mo cylinder	3×1.8	3×2.1	1.5×2.1	3×2.1	0.07
d	CB	Cu brick	$3.5 \times 2 \times 1.5$	$3.5 \times 2 \times 1.7$	$1.6 \times 0.9 \times 1.7$	$3.5 \times 2 \times 1.7$	
e	CMB13	Cu/Mo/Cu brick	$3.5 \times 2 \times 1.5$	$3.5 \times 2 \times 1.7$	$1.6 \times 0.9 \times 1.7$	$3.5 \times 2 \times 1.7$	0.13
	CMB07	Cu/Mo/Cu brick	$3.5 \times 2 \times 1.5$	$3.5 \times 2 \times 1.7$	$1.6 \times 0.9 \times 1.7$	$3.5 \times 2 \times 1.7$	0.07

step. In this paper, the samples for the thermal cycling test have been manually prepared using two soldering steps, where eutectic Sn-3.5Ag solder paste has been used in both steps. In the first soldering step, after applying solder paste on both substrates using stencil printing, one IGBT, one diode, two bumps B, and all bumps D are placed on the bottom DBC substrate, and one IGBT and one diode placed on the top DBC substrate. Next, (after dispensing solder paste on one end of bumps A and C) two bumps of A and one bump of C are placed on the bond pads of the IGBT already placed on the bottom DBC substrate, and two bumps of A and one bump of C on the bond pads of the IGBT already placed on the top DBC substrate. Then, the bottom and top substrates (both with devices, bumps and solder paste) are placed into a reflow oven for soldering. Reflow soldering was accomplished using a temperature profile consisting of first heating up to 200 °C within 3 min, holding at 200 °C for 3 min, heating up to 250 °C within 2 min, holding at 250 °C for 3 min before being cooled down to room temperature within 6 min. In the second soldering step, solder paste was first applied to the other end of all the bumps already soldered on the substrates and the IGBTs. The top substrate was then placed and aligned on the bottom substrate through the use of an alignment jig. Finally, the whole assembly was placed in the reflow oven to finish the second soldering step, using a reflowing temperature profile identical to that used in the first soldering step.

III. THERMOMECHANICAL MODELING

A. Meshing System

The thermomechanical modeling and simulation has been done using commercial available FE analysis software Abaqus 6.11-3 and its graphic user interface CAE. Fig. 4 presents two representative meshing systems consisting of 162440 and 156294 elements (C3D8 linear brick elements and DC3D6 linear triangular prism elements) to discretize the design cases CHC25 and CMB13. In both cases, the largest element is $1\,\text{mm} \times 1\,\text{mm} \times 0.45\,\text{mm}$, and the smallest element is $0.5\,\text{mm} \times 0.25\,\text{mm} \times 0.025\,\text{mm}$. In all the design cases listed in Table I, the elements used in the critical domains all have the same dimensions. For example, the sizes of the brick elements used to discretize the critical solder joints whose maximum von Mises stress and creep strain accumulation will be used to assess the thermomechanical reliability are all $0.5\,\text{mm} \times 0.25\,\text{mm} \times 0.025$ mm in size. This is necessary because longer computing times would be required if meshing size-independent solutions were implemented for the present 3-D model with a much finer meshing system used. Therefore, relatively coarse meshing systems with the same size of elements (in the critical domains for all the design cases) have been employed to achieve an acceptable computing time.

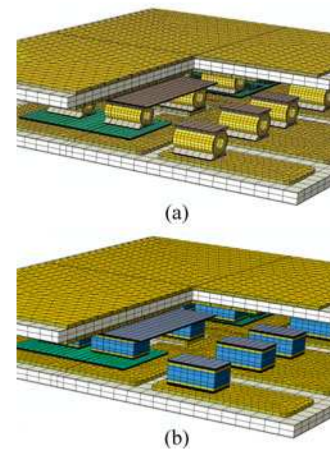

Fig. 4. Cut views of two representative meshing systems to discretize the stacked assembly for: (a) design case CHC25; and (b) design case CMB 13.

In addition, S4 shell elements of $0.5\,\text{mm} \times 0.5\,\text{mm}$ or $0.5\,\text{mm} \times 0.25\,\text{mm}$ in size were also used to discretize the NiP finish on the surfaces of the substrates and the Al metallization on both sides of the chips. This is because there is a layer of $\sim$5-μm-thick electroless NiP finish existing on all surfaces of the Cu metallization on both sides of the commercially available AlN-based DBC substrates. There were also 3.2-μm/500-nm/300-nm-thick AlSiCu/NiP/Pd metallization on the top side,

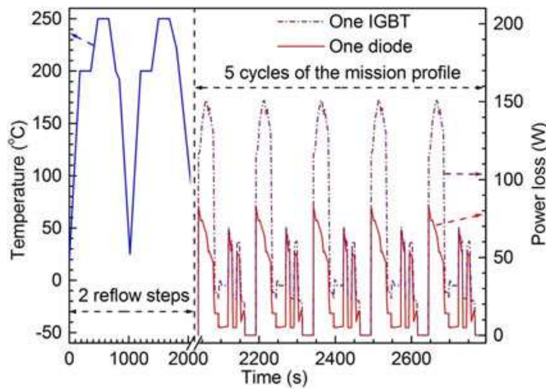

Fig. 5. Thermal history of predefined temperature profile of the two soldering steps followed by five cycles of mission profiles with heat generated by power losses of IGBTs and diodes.

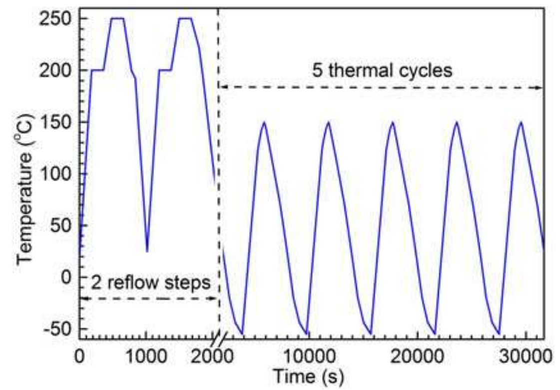

Fig. 6. Thermal history of predefined temperature profile of the two soldering steps followed by five thermal cycles between −55 and 150 °C.

and 1-μm/300-nm/300-nm-thick AlTi/Ni/Ag metallization on the backside of all the as-received IGBTs and diodes. They were assumed as a layer of 3.2-μm-thick Al on the top side and a layer of 1-μm-thick Al on the backside of the chips in the present model. This is justified and based on the fact that most of the NiP/Pd and Ni/Ag layers react with liquid Sn-3.5Ag solder to form intermetallic compounds (IMCs) embedded within the matrix of the solder during the reflow process, and as such (the IMCs) have been neglected.

It should be pointed out that a more accurate 3-D model for analyzing the thermomechanical performance of the stacked assembly should include the IMCs formed at the solder/contact metallization interfaces and their subsequent evolution during any thermal history. However, it is still a formidable task to solve such a 3-D thermomechanical problem because the IMCs are extremely thin when compared to other materials and parts in the model, and would require extremely fine elements to discretize them. Therefore, the formation and growth of the IMCs in this model have been ignored.

B. Thermal History and Boundary Conditions

The assembly was first subjected to a predefined temperature profile to simulate the stress and strain developments during the two-step reflow soldering process. During both soldering steps, the corresponding solder joints were deactivated without the development of stress and strain when they were in the form of either solder paste or molten solder. They were activated when they solidified from the molten solder. Both the solder paste and the solid solder joints are molten at the melting point of 221 °C, and the solidification of the molten solder occurs at a supercooling temperature of 192 °C for Sn-3.5Ag solder alloys [18].

Then, the thermomechanical response of the assembly associated with five cycles of a realistic mission profile and five cycles of thermal cycling between −55 and +150 °C, as shown in Figs. 5 and 6, were further simulated independently. In the mission profile, the power losses of the IGBTs and diodes were taken as uniform surface heating sources. This may be somewhat different from the actual distribution of heating source in the devices [19], but can offer a relatively simple way to assess the thermal performance of the different design cases as listed in Table I. The heat exchange boundary condition as described in Fig. 7 were applied to both the top and bottom cooling surfaces of the assembly, where the heat exchange coefficient of 5000 W · m^{-2} · k^{-1} is typical for a water-based cooler in power electronics [20]. The temperature field obtained from the thermal simulation was used as inputs to simulate further stress and strain development in the assembly during the mission profile. For the thermal cycling, a predefined uniform temperature field in the entire assembly (following the temperature profile) was directly applied to simulate further stress and strain developments. Thermal cycling between −55 and +150 °C has been selected because the reliability of the assembly samples for the design cases CHC25 and CMB13 had been experimentally tested under this thermal cycling condition.

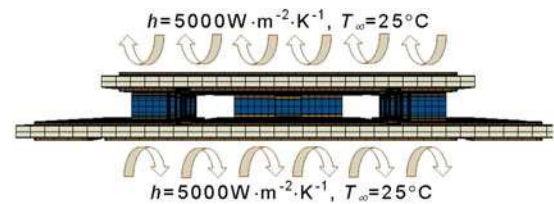

Fig. 7. Boundary condition of heat exchange applied in the thermal simulation during the mission profile.

For the aforementioned thermomechanical simulations, all the parts in the assembly (for all the design cases) have been assumed to have a zero stress and strain state at the beginning of the first soldering step, and the model is referred to as full model. To investigate the effect of different initial stress and strain states in the DBC substrates, all the parts in the assembly for the design cases CHC25 and CMB13 have also been assumed to have zero stress and strain state until the moment when the solidification of the molten solder occurred, during the second soldering step, and the model is referred to as simple model. In other words, the full model has taken into account the stress and strain developments in the assembly during all heating up and cooling down stages of the two soldering steps, while the

TABLE II
THERMAL AND MECHANICAL PROPERTIES OF PART OF THE COMPONENT MATERIALS USED DURING THE THERMOMECHANICAL SIMULATIONS

	Si	AlN	Mo	NiP
Thermal conductivity (W/(K · m))	146	175	138	5
Specific heat (J/(kg · °C)	750	740	250	540
Density (kg/cm^3)	2.33	3.30	10.22	8.10
Coefficient of thermal expansion (10^{-6}/K)	2.5	4.6	4.8	16.4
Young's modulus (GPa)	130	331	317	60
Poisson ratio	0.22	0.22	0.32	0.3

simple model has only taken into account the stress and strain developments in the assembly during the cooling stage of the second soldering step.

C. Properties of Materials

The thermal and mechanical properties of the Si, AlN ceramic, Mo, and the NiP finish on the substrates for the thermomechanical simulation are listed in Table II [10], [21], and [22]. For the rest of the materials in the assembly, Chaboche's plastic model was used to describe the mechanical properties of the Cu and Al, and Anand's creep model was used to describe the mechanical property of the Sn-3.5Ag solder alloy. All the mechanical and thermal properties for the Cu, Al, and Sn-3.5Ag were taken from [10] and [21], and are therefore, not repeated here.

In real applications, the stacked assembly will be filled with a soft dielectric encapsulant and integrated with a double-sided water-based cooler. These have been ignored because silicone gel, which is commonly used as the encapsulating gel, has extremely low thermal conductivity and Young's modulus compared to the other components and parts in the assembly. Also using the backsides of the two DBC substrates as the primary cooling surfaces the mechanical constraint caused by installation of the double-sided water-based cooler will be limited. Therefore, the effect of ignoring the encapsulant and water-based cooler on the simulation results to be used for the optimization of the thermomechanical design should be negligible.

D. Simulation Criteria for Thermomechanical Performance

The effects of the bump shapes and materials on the maximum juncture temperature in the Si chips and on the thermomechanical reliability of the Sn-3.5Ag solder joints and DBC substrates have been considered. Regarding the possibility of thermomechanical failure of the solder joints, the maximum creep strain accumulation is adopted for qualitative comparison with the simulated creep strain fields for the different design cases [10], [23]–[26]. Thermomechanical failure of the DBC substrates is closely associated with the plastic strain development in the Cu metallization [27], [28]. However, brittle cracking of the AlN tiles is the dominant failure mode and is mainly controlled by tensile stresses [10], [21], [29], [30]. Thus, the maximum tensile principal stress is employed for qualitative comparison with the simulated stress fields for the different design cases.

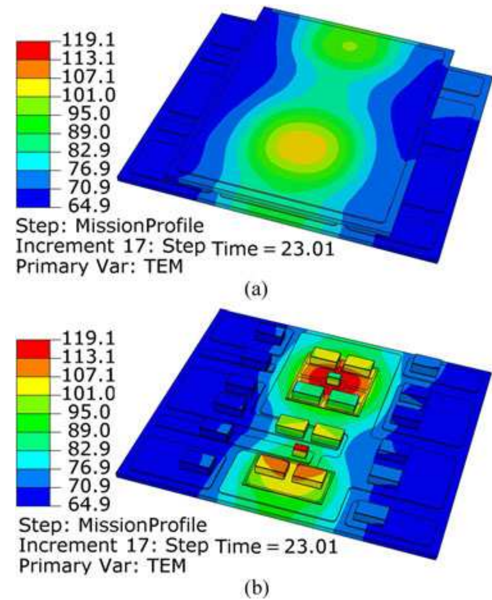

Fig. 8. Simulated temperature field with unit in °C for design case CMB13 at 23.01 s during one cycle of the mission profile: (a) overall view and (b) open view.

It should be noted that these criteria are only regarded as indicators of the sequence and location of possible crack initiation, and are viewed as sufficient to provide insight and guidance for subsequent thermomechanical design and optimization. A more accurate prediction of the thermomechanical lifetime of the assembly would require a finer numerical model and a full description of the stress–strain behavior and response of all the materials in the assembly under the relevant thermal history.

E. Simulation Cases

All the nine design cases listed in Table I have been simulated using the full model and subjected to the two types of thermal history associated with the mission profile and thermal cycling (as shown in Figs. 5 and 6). The design cases CHC25 and CMB13 have also been simulated using the simple model and subjected to the thermal history associated with the mission profile. In total 20 simulation cases have been executed on a PC computer with Intel[R] Core[TM] i7-3820 CPU at 3.60-GHz processor and 32-GB RAM. The running times were 30–36 h for all cases.

IV. SIMULATION RESULTS AND DISCUSSION

A. Thermal Performance

Fig. 8 presents the simulated temperature distribution field for the design case CMB13 at 23.01 s during the mission profile, where in the open view, the top substrate of the assembly is removed for better observation. For all design cases listed in Table I, the maximum temperature can be observed on either the IGBT or diode attached to the top DBC substrate, during the mission profile. At any instantaneous time, the maximum temperature on the IGBT and diode attached on the bottom

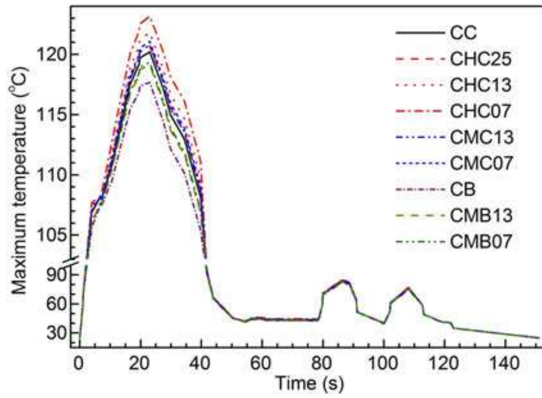

Fig. 9. Evolution of the simulated maximum temperature in the assembly for all the nine design cases listed in Table I during one cycle of the mission profile.

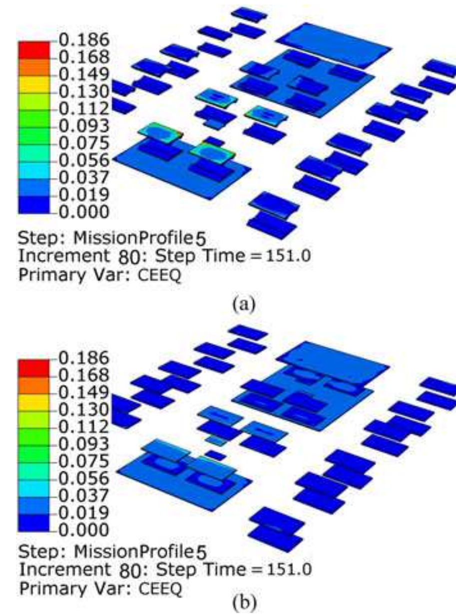

Fig. 10. Distributions of the creep strain accumulation in most solder joints after five cycles of the mission profile for the design cases: (a) CHC25 and (b) CMB13.

DBC substrate is 0.1–0.2 °C lower than the corresponding devices attached on the top substrate. This is readily understood because the cooling surface (area) of the top substrate is slightly smaller than the bottom substrate, while the bumps used (for joining) are similar in size and material.

Fig. 9 compares the evolution of the simulated maximum temperature in the assembly for all the nine design cases listed in Table I during one cycle of the mission profile. For all the design cases, the highest maximum temperature is observed at 23.01 s during the mission profile. Compared with Cu solid cylinder bumps (CC), which will be used as a reference, the Cu brick bumps (CB) can reduce the highest maximum temperature in the assembly by 2.5 °C. This can be attributed to the fact that, in addition to the slight difference in size, the average thickness of the Sn-3.5 solder joints used to join the cylinder bumps is thicker than the average thickness of the Sn-3.5 solder joints used to join the brick bumps. In contrast, in comparison with the Cu solid cylinder bumps, the Cu hollow cylinder bumps (CHC25, CHC13, CHC07) with different wall thicknesses increase the highest maximum temperature in the assembly by 0.5–3 °C. This again can be easily understood because the air gap in the hollow bumps reduces the cross-sectional area for the heat transfer. In agreement, the Cu/Mo composite cylinder bumps (CMC13, CMC07) also increase the highest maximum temperature in the assembly by 0.6–0.9 °C when compared to the Cu solid cylinder bumps. The highest maximum temperatures in the assembly with the Cu/Mo/Cu brick bumps (CMB13, CMB07) are between those of the Cu brick bumps and the Cu solid cylinder bumps, which can be ascribed to the Mo in the bumps, which has a lower thermal conductivity than Cu, but higher thermal conductivity than Sn-3.3Ag solder alloy [22].

B. Thermomechanical Stresses and Strains

1) Effect of Initial Stress and Strain State in DBC Substrates: From the simulation results of design cases CHC25 and CMB13, it was observed that the stress and strain developments in all the solder joints during five cycles of the mission profile are almost independent of the use of either the full model or the simple model as described in Section III-B. In other words, they are independent of the initial stress and strain state in the DBC substrates before the mission profile. Fig. 10 shows the distributions of the creep strain accumulation in most solder joints in both design cases after five cycles of the mission profile, where Fig. 11 compares the evolutions of the maximum creep strain accumulation. It can be seen that almost identical simulation results have been obtained using either the full model or the simple model.

In contrast, the stresses and strains in the DBC substrates simulated using the full model are all higher than those simulated using the simple model. Therefore, for a more accurate prediction of the thermomechanical lifetimes of the DBC substrates, it is important to know the initial stress and strain states [21], [31]. However, if the relative profiles of the simulation results between the design cases CHC25 and CMB13 are compared, both the full model and the simple model predict the same or similar evolutions during five cycles of the mission profile, for all the maximum von Mises stress and plastic strain in the Cu metallization, and the maximum maximum-principal stresses in the AlN tiles of the DBC substrates. Figs. 12 and 13 compare the distribution and evolutions of the maximum-principal stress in the AlN tiles of the DBC substrates, simulated using the two types of models. These results are readily understood because the stress and strain developments in the different materials are controlled by the mismatches of coefficients of thermal expansion (CTEs) between the materials and the accumulations of plastic and/or creep strains in the Cu and solder alloy [10], [21]. The inclusions of plastic strain developments in the Cu metallization of the DBC substrates during the early soldering stage lead to higher stresses and strains in the DBC substrates simulated using the full models than those simulated using the simple model during five cycles of the mission profile.

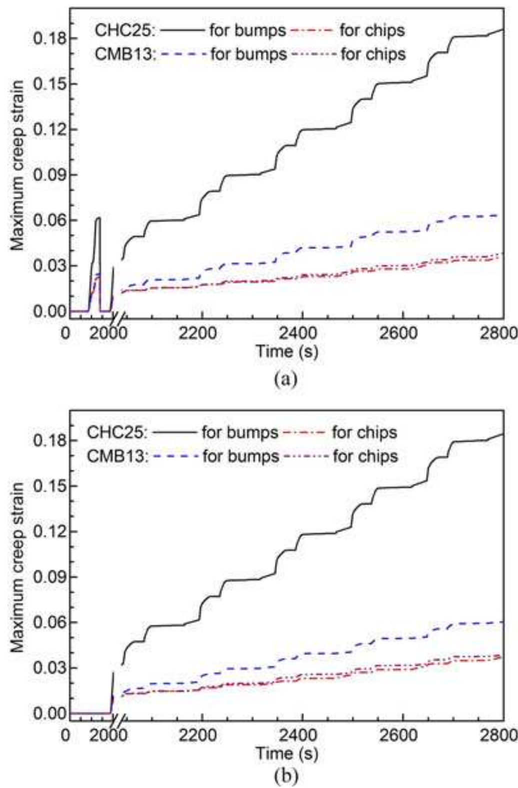

Fig. 11. Evolutions of the maximum creep strain accumulations in all solder joints in the design cases CHC 25 and CMB13 during five cycles of the mission profile, simulated using: (a) full model and (b) simple model.

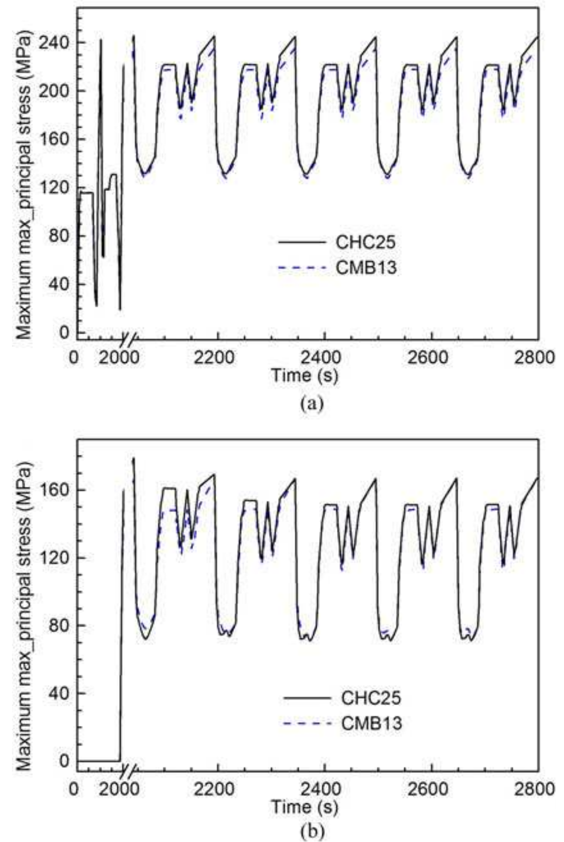

Fig. 13. Evolutions of the maximum maximum-principal stresses in the AlN tiles of the DBC substrates in the design cases CHC 25 and CMB13 during five cycles of the mission profile, simulated using: (a) full model; and (b) simple model.

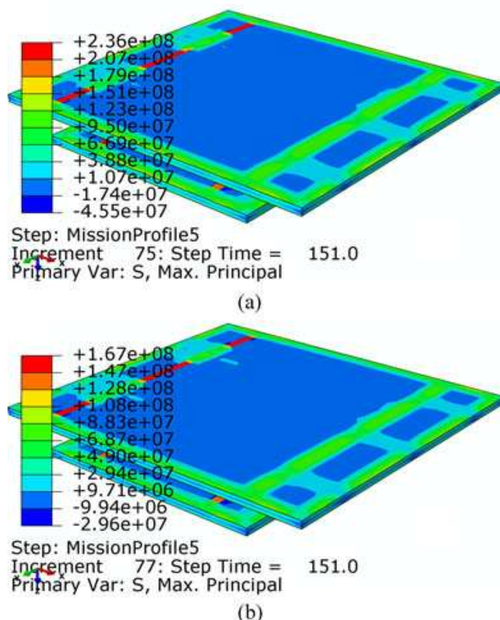

Fig. 12. Distributions of the maximum-principal stress with unit in Pa in the AlN tiles of the DBC substrates in the design case CMB13 after five cycles of the mission profile, simulated using: (a) full model and (b) simple model.

Different amounts of mismatches in the CTE between the materials in the different design cases dominate the relative sizes of the stress and strain developments in the DBC substrates, no matter whether they are simulated using the full model or the simple model. Therefore, for the purpose of optimization of the thermomechanical design, the present FE simulation results can provide useful comparisons between the different design cases even if the initial stress and strain state in the as-received DBC substrates might not be known. The simulation results presented below will now all be presented from the full model.

2) Effect of Thermal History: The assembly has been subjected to relatively high temperatures for longer durations during the five thermal cycles than the five cycles of the mission profile. Relatively high temperatures (at longer duration) would promote creep strain accumulation, which would somewhat lead to the release of stress. Therefore, it is not surprising that the mission profile and thermal cycling histories have significantly different effects on the stress and strain development in the parts/components of the assembly. For all the design cases listed in Table I, the relevant maximum stresses and strains in the different parts/components have all been observed at the corners and/or edges of the interfaces between the different materials, irrespective of the applied profile (mission or thermal). This can be understood because the stress and strain developments

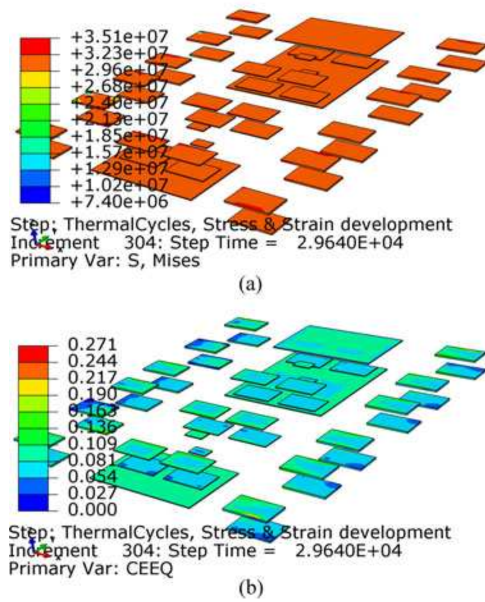

Fig. 14. Distributions of: (a) von Mises stress with unit in Pa; and (b) creep strain in most solder joints in the design CMB13 after five thermal cycles.

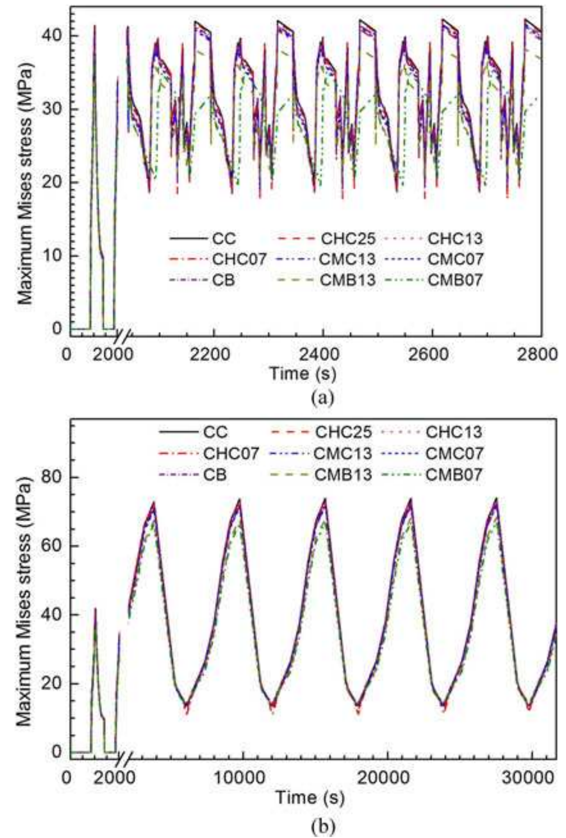

Fig. 15. Comparison of the evolutions of the maximum von Mises stresses in the solder joints in all the design cases during: (a) five cycles of the mission profile and (b) five thermal cycles.

are caused by the mismatches in the CTEs of the different materials in the assembly. It should be pointed out that for all solder joints, the maximum von Mises stresses and creep strain accumulations occur in the solder joints between the bumps and IGBTs during the mission profile (see Fig. 10). However, they occur in the solder joints between the bumps and DBC substrates during the thermal cycles (see Fig. 14). This can be attributed to the relatively high temperatures in the solder joints (used to join bumps) on Si chips when compared to those in the solder joints (used to join bumps) on the DBC substrates during the mission profile, compared to the uniform distribution of temperatures during thermal cycling. The solder joints with the maximum creep strain accumulations are in general identified as the thermomechanically weak point [23]. Therefore, as stated in previous work [32], care must be taken when the results of thermal cycling are used to predict the failure and lifetimes of assemblies during realistic mission profiles.

Figs. 15–17 compare the evolutions of the relevant maximum stresses and creep strain accumulations in all the solder joints and the AlN tiles of the DBC substrates for all the design cases during five cycles of the mission profile and five thermal cycles. During the mission profile, the maximum von Mises stresses in all the solder joints and the maximum maximum-principal stresses in the AlN tiles of the DBC substrates both basically increase with decreasing maximum temperature in the assembly (see Fig. 9). During the thermal cycling, the highest maximum von Mises stresses in all the solder joints and the highest maximum-principal stress in the AlN tiles of the DBC substrates also occur at the moment when the assembly is subjected to the lowest temperature (see Fig. 6). Conversely, the lowest maximum von Mises stresses in all the solder joints occurs at the moment when the assembly is subjected to the highest temperature. The lowest maximum-principal stresses in the AlN tiles of the DBC substrates occur during cooling down of the thermal cycling from the highest temperature to the lower temperature. During both the mission profile and thermal cycling, the increase in rate for the maximum creep strain accumulation in all the solder joints is higher for higher maximum temperatures in the assembly (see Figs. 6, 9 and 16). The latter can be attributed to the fact that the Sn-3.5Ag solder alloy is prone to creep at relatively high temperatures [10], [24].

3) Effects of Bump Shapes and Materials: From Figs. 15–17, it can further be seen that between the Cu cylinder bumps and Cu brick bumps (design cases CC and CB), the effects of these two types of bump shapes on the maximum von Mises stresses and creep strain accumulations in all the solder joints and the maximum maximum-principal stresses in the AlN tiles of the DBC substrates are all negligible during both the mission profile and the thermal cycling. This may be due to the fact that the solder joints with a higher CTE directly contact and withstand the different thermal expansion/contraction developments of the DBC substrates, Si chips, and Cu bumps with relatively low CTEs. On the one hand, the individual solder joints for joining the cylinder bumps are thicker (on average), and may contribute more to the relevant stress and strain developments at the interfaces between them and the DBC substrates, Si chips and Cu bumps. On the other hand, the individual solder joints for joining the brick bumps are thinner in average thicknesses,

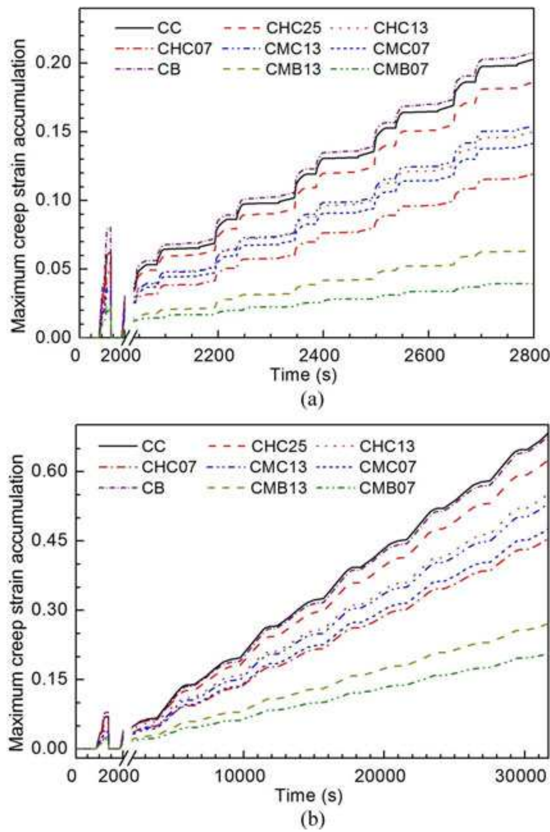

Fig. 16. Comparison of the evolutions of the maximum creep strain accumulations in the solder joints in all the design cases during: (a) 5 cycles of the mission profile and (b) five thermal cycles.

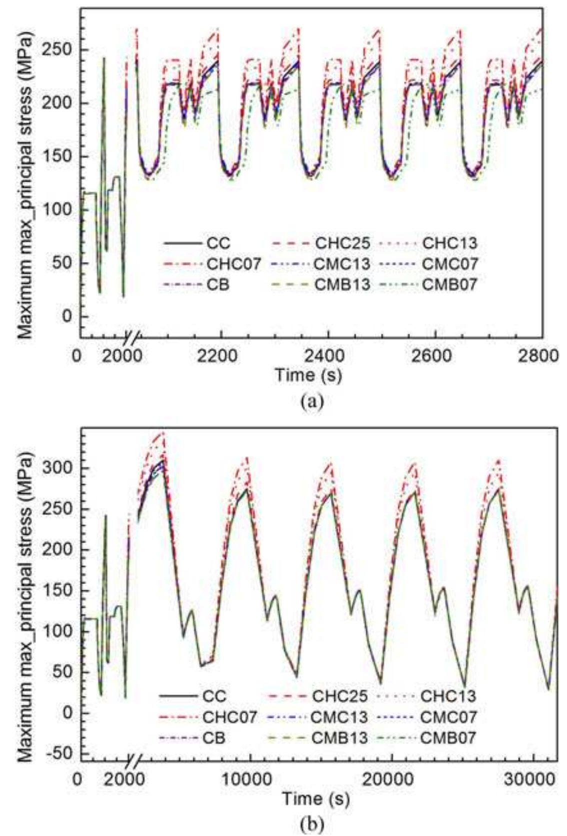

Fig. 17. Comparison of the evolutions of the maximum maximum-principal in the AlN tiles of the DBC substrates in all the design cases during: (a) five cycles of the mission profile and (b) five thermal cycles.

and may transfer more relevant stresses and strains between the two opposite interfaces of the corresponding solder joints. These two effects may counteract the effects of the two types of bump shapes on the relevant stress and strain developments in all the solder joints and the DBC substrates.

Using relatively compliant Cu hollow cylinder bumps (design cases CHC25, CHC13, and CHC07), the maximum von Mises stresses and creep strain accumulations in all the solder joints can be reduced to some extent during both the mission profile and the thermal cycling. However, this somewhat increases the maximum maximum-principal stresses in the AlN tiles of the DBC substrates during both the mission profile and thermal cycling. These results may be associated with the fact that the compliant hollow bumps could absorb a certain amount of deformation energy from the solder joints, and transfer some to the AlN tiles of the DBC substrates. This is because a flexible PCB was reported to absorb some deformation energy of a flip chip assembly, and thus, slow the growth of cracks and improve the thermal fatigue lifetime of the corresponding solder joints subjected to thermal cycling [33].

By contrast, using the Cu/Mo shell/core composite cylinder bumps (design cases CMC13 and CMC07), the relevant maximum stresses and strain accumulations in all the solder joints and the AlN tiles of the DBC substrates are all lower than or similar to those using the Cu cylinder bumps and Cu brick bumps, during both the mission profile and the thermal cycling. This result can simply be attributed to the fact that the Mo core with much lower CTE constrains the thermal expansion and contraction of the Cu/Mo shell/core composite cylinder bumps, and thus, reduces the extent of mismatch of CTEs between the bumps, Si chips, and DBC substrates.

More effectively, using the Cu/Mo/Cu composite brick bumps (design cases CMB13 and CMB07), the maximum von Mises stresses and creep strains in all the solder joints can further be reduced when compared with those using Cu/Mo shell/core composite cylinder bumps during both the mission profile and the thermal cycling. The relevant maximum stresses in the AlN tiles of the DBC substrates are also slightly lower than or similar to those using the Cu/Mo shell/core composite cylinder bumps. This can be ascribed to the fact that the Cu/Mo/Cu composite brick bumps can more effectively reduce the extent of mismatch of CTEs between the bumps, Si chips, and DBC substrates than the Cu/Mo shell/core composite cylinder bumps.

V. Experimental Evaluation

The aforementioned thermomechanical stresses and strains simulated using the FE numerical model are evaluated by comparison with the experimental results for the reliability of the design cases CHC25 and CMB13 subjected to thermal cycling between −55 and +150 °C as shown in Fig. 6. These two

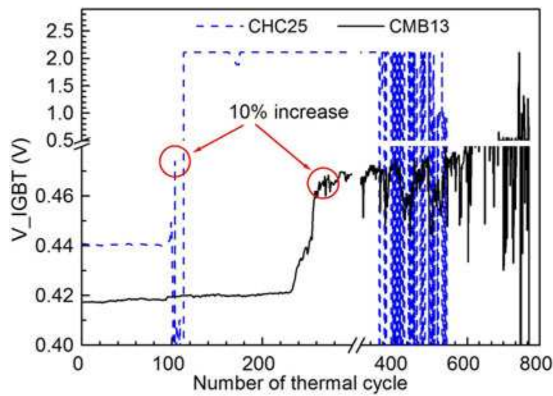

Fig. 18. Evolutions of on-state voltage drops, V_IGBTs, across the IGBTs in the samples CHC and CMB13 at 90 °C, with respect to number of thermal cycle between −55 and 150 °C.

design cases have been tested because the simulated thermomechanical stresses and strains are easy to compare (showing a marked difference in values) and the corresponding bump materials are commercially available. The samples were prepared using two soldering steps as detailed previously. The reliability of the assembled samples during the thermal cycling test was continuously monitored by recording the on-state voltage drop across the Si chips under a fixed bias current of 200 mA. The related experimental procedures for this real-time monitoring and recording have been described in detail in a previous paper [34], and thus, are not repeated here.

Fig. 18 presents the evolutions of the on-state voltage drop recorded at 90 °C, V_IGBTs, across the IGBTs in the samples CHC and CMB13, with respect to number of thermal cycles between −55 and +150 °C. Note that the recorded on-state voltage drop included the contributions from both the IGBTs themselves and the electronic interconnects such as the bumps, solder joints, and the Cu tracks on the DBC substrates. Therefore, any significant change in the recorded voltage drop should be associated with failure in the corresponding conductive path. As can be seen from Fig. 18, a 10% increase in the V_IGBT was recorded after 100 thermal cycles for the sample CHC25 and after 265 thermal cycles for the sample CMB13. Such a 10% increase in V_IGBT can be used as an indicator of the failure of the solder joints in the conductive path, due to the formation and initial rapid growth of fatigue cracks. This is because no appreciable degradation of the DBC substrates could contribute a 10% increase in V_IGBTs, while all the Si chips in the assemblies were intact.

The thermal cycling test of the sample CHC25 was stopped after 550 cycles. Complete debonding of several bumps D from both the top and bottom DBC substrates and complete delamination of several Cu tracks from the AlN tiles of both the top and the bottom DBC substrates were observed. Fig. 19 shows some representative scanning electronic microscopy (SEM) images (backscattered) taken from the tested sample CHC25. The solder residual on the bottom DBC substrate as shown in Fig. 19(a) is due to formation and growth of fatigue cracks within the solder joint used to join bumps D. The complete delamination of the two Cu tracks from both the top and the bottom DBC substrates shown in Fig. 19(b) was due to the formation and growth of fatigue cracks within the AlN tiles. The enlarged view shown in Fig. 19(c) confirmed the existence and growth of fatigue cracks within the solder joints prior to their fracture.

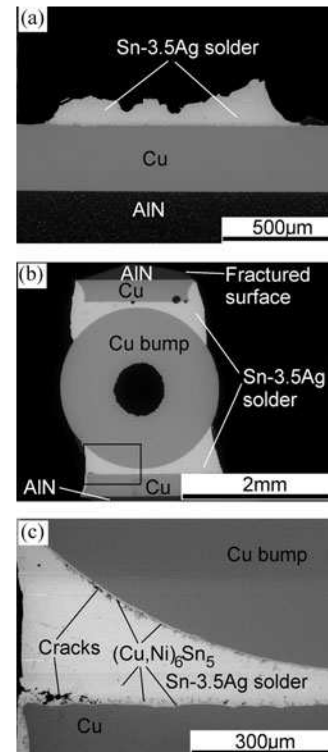

Fig. 19. SEM images taken from the sample CHC25 after 550 thermal cycles: (a) solder residual on the bottom DBC; (b) one bump D between two Cu tracks completely delaminated from both the top and the bottom DBC substrates; and (c) enlarged view of the box at the bottom left side of (b).

After 550 thermal cycles, no noticeable debonding of the soldered bumps and delamination of the DBC substrates could be observed in the sample CMB13. The thermal cycling test of this sample lasted until 770 cycles, where partial delamination of the Cu tracks from the AlN tiles of the DBC substrates was observed. Fig. 20 shows typical fatigue cracks formed within the AlN tiles and the solder joints used to join bumps D between the two (top and bottom) DBC substrates in the sample CMB13. Unlike sample CHC25, where some Cu tracks of the DBC substrates and some bumps D had been separated from the sample after 550 thermal cycles, all the Cu tracks and bumps still remained in the sample CMB13 after 770 thermal cycles. Therefore, it may be concluded that the two DBC substrates in sample CMB13 were more reliable than the two DBC substrates in sample CHC25 though exact lifetimes for them cannot be given in the present thermal cycling experiment.

Thermomechanical fatigue lifetimes of soft solder joints, such as the present Sn-3.5Ag solder joints can be described with prediction models based on the plastic strain development, creep strain development, and inelastic energy density per thermal cycle [10], [23]–[26]. In the present FE simulation, the mechanical property of the Sn3.5Ag solder joints was described by the

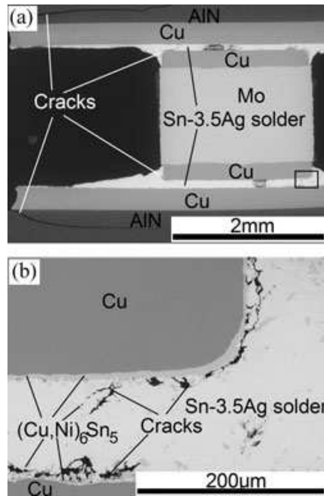

Fig. 20. SEM images taken from the sample CMB13 after 770 thermal cycles: (a) one bumps D between two Cu tracks on the AlN tiles of the top and the bottom DBC substrates, showing the fatigue cracks within the AlN tiles and (b) enlarged view of the box at the bottom right side of (a), showing $(Cu,Ni)_6Sn_5$ IMC and fatigue- cracks within the solder joint.

Anand viscoplastic model, and the simulated creep strains include both the creep and plastic deformation developments in the solder joints subjected to thermal cycling. Combining the experimental lifetimes of 100 cycles and 256 cycles for the critical solder joints in the samples CHC25 and CMB13 with the simulated creep strain accumulations presented in Fig. 16(b), the following equation can be applied through data fitting [23]:

$$N_f = \frac{1}{C\Delta\varepsilon_{cr}} \tag{1}$$

where N_f is the experimental fatigue lifetime in thermal cycles, $\Delta\varepsilon_{cr}$ the simulated creep strain accumulation per thermal cycle, C is the inverse of the creep ductility. With the $\Delta\varepsilon_{cr}$ of 0.132 and 0.056 for the samples CHC25 and CMB13, the present $C = 0.0683$ is obtained. Such a value is comparable with but somewhat higher than the $C = 0.045$ for the SnAgCu solder alloy reported in the existing literature [23]. This may be attributed to the fact that the present Sn-3.5Ag solder joints had been saturated with Cu during the reflow process, as evident from the formation of $(Cu,Ni)_6Sn_5$ IMC within the solder joints as shown in Figs. 19(c) and 20(b). However, the present temperature range of thermal cycling from −55 to 150 °C is wider than those from −40 to 125 °C, −55 to 125 °C, and 0 to 100 °C that were used in [23].

Using (1) with the obtained $C = 0.0683$ and the $\Delta\varepsilon_{cr}$ determined from Fig. 16, the fatigue lifetimes of the weakest solder joints in all the simulation cases are predicted and plotted in Fig. 21. It should be pointed out the lifetimes of the solder joints under the mission profile condition should be longer than these predictions. This is because (1) has been derived from the experimental results of the two samples CHC25 and CMB13 under harsh thermal cycling condition, where the solder joints were more seriously suffering from damaging due to lower ductility at higher stress and low temperature. Under the mission profile, the solder joints would be more ductile at lower stresses.

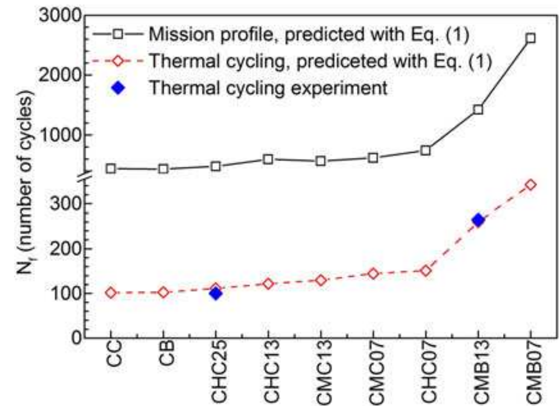

Fig. 21. Experimental lifetimes and those predicted from the creep strain accumulations per thermal cycle or per cycle of the mission profile, $\Delta\varepsilon_{cr}$, simulated with the FE model.

As reported in [23], the SnAgCu solder joints in a variety of package type are about three times more ductile at lower stress and the strains are more damaging due to lower ductility at high stresses and low temperatures. Nevertheless, from Fig. 21, it can be seen that the Cu/Mo/Cu composite brick bumps CMB13 and CMB07 can significantly improve the thermomechanical reliability of the solder joints under both the thermal cycling and mission profile conditions.

There are two types of fatigue lifetime models, which have been developed to predict the lifetimes of DBC substrates. One of them is based on the plastic strain development within the Cu metallization, either in the form of the Coffin–Manson law or in more complicated form [27], [28]. The other one is based on the maximum-principal stress within the ceramic tiles, including the fracture mechanics modeling the propagation rate of crack and the weakest-link theory capturing the material's probabilistic behavior [21], [29]. From the present experimental result that the DBC substrates in the sample CMB13 was more reliable than those in sample CHC25, the simulated maximum-principal stress within the AlN tiles should be more applicable to compare the lifetimes for optimization of design. This is because the simulated maximum plastic strains within the Cu metallization of the DBC substrates in the two samples were found to be almost the same as each other, but the simulated maximum-principal stress within the AlN tiles of the DBC substrates in the sample CHC25 is somewhat higher than for that in sample CMB13 (see Fig. 17).

Both the 3-D FE simulation results and the resultant thermal cycling experiment verify that the selection of Cu/Mo/Cu composite brick bumps in the designed power module can significantly improve the thermomechanical reliability of both the solder joints and the DBC substrates. As reflected by the simulation results shown in Figs. 15–17, both the shape and selection of material for the bumps are important to improve the thermomechanical reliability of all the solder joints, DBC substrates and Si chips in a stacked substrate–chip–bump–chip–substrate assembly. The optimized reliability can be achieved by selecting the Cu/Mo/Cu composite brick bumps with the lowest thickness ratio of Cu to Mo.

VI. Conclusion

Based on the aforementioned results of the FE simulation and experimental evaluation for the thermomechanical reliability of the stacked substrate–chip–bump–chip–substrate assembly used to construct a highly integrated bidirectional power switch, the following conclusions are drawn.

Of the nine design cases, the Cu brick bumps have the best thermal performance, and the Cu hollow cylinder bumps with the thinnest thickness have the worst thermal performance. The Cu/Mo/Cu composite brick bumps showing optimized thermomechanical reliability of the assembly have thermal performance between the Cu brick bumps and the Cu hollow cylinder bumps, with a maximum temperature 1.5 °C higher than that in the assembly with the Cu brick bumps.

The initial stress and strain states in the DBC substrates have negligible effect on the stress and strain developments in the Sn-3.5Ag solder joints, but have a marked effect on the stress and strain developments in the DBC substrates. However, the different initial stress and strain states in the DBC substrates give similar relative results.

During both the mission profile and thermal cycling, the relevant maximum stress and creep strain developments reflecting the thermomechanical reliability of the Sn-3.5Ag solder joints and DBC substrates have the same or similar order when comparing the different bumps in the assembly. However, the maximum von Mises stresses and creep strain accumulations occur in solder joints used to join bumps on IGBTs during the mission profile, but occur in solder joints used to join bumps on DBC substrates during the thermal cycling tests.

The FE simulation results in combination with the accelerated thermal cycling experiment reveal that the thermomechanical reliability of the Sn-3.5Ag solder joints in the assembly samples with the Cu hollow cylinder bumps and the Cu\Mo\Cu composite brick bumps is inversely proportional to the creep strain accumulation per thermal cycle, and the thermomechanical reliability of the DBC substrate is more likely to be dominated by the maximum-principal stress development within the AlN tiles.

The results from the accelerated thermal cycling experiment verifies that selection of the Cu/Mo/Cu composite brick bumps in the stacked substrate–chip–bump–chip–substrate assembly can significantly improve the thermomechanical reliability of both the solder joints and the DBC substrates when compared to Cu cylinder bumps and Cu hollow cylinder bumps reported in previous work.

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