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UNIVERSITY OF NOTTINGHAM

# Single-Ended Traveling Wave Fault Location on Radial Distribution Lines

A thesis submitted in partial fulfillment for the
degree of Doctor of Philosophy

in the
Faculty of Engineering
Department of Electrical And Electronic Engineering

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# *Abstract*

In this thesis a single-ended traveling wave fault location algorithm is developed for autonomously locating short circuit faults on a radial distribution line using the high frequency traveling wave transients. The traveling wave pattern observed at the substation is correlated with the traveling wave pattern predicted using time tree analysis for different fault locations and fault resistance. Genetic search techniques are used to evolve an initial population of possible fault locations to determine the most likely fault location. It is shown through extensive EMTP simulations that the scheme is capable of finding the location of three phase faults, inter-phase faults and single-phase faults for fault resistances ranging from 0 - 1000 ohm on a radial distribution line with five sub-feeders.

A new high speed FPGA based data acquisition system is developed suitable for capturing traveling wave fault data from a radial distribution line with the necessary fidelity for the proposed fault location algorithm. The data acquisition system is deployed on a Medium Voltage distribution line in the Santa Caterina region of Brazil.

A branched communication network is constructed out of RG-58 coaxial cable and a Time Domain Reflectometry device is used to capture the reflection pattern under different fault conditions. The fault location algorithm is adapted to work with TDR as opposed to fault generated traveling waves. The location algorithm is capable of locating faults with resistance between 0 and 75 ohm up to three zones away from the injection point.

# *Publications*

The work in thesis has been published or is under consideration in several publications which are as follows

1. D. Coggins, D. W. P. Thomas, Y. Zhu, and B. R. Hayes-Gill, 'An FPGA Based Travelling Wave Fault Locator' International Conference on Field-Programmable Technology 2007 December 12th-14th, 2007 The Kitakyushu International Conference Center Kokurakita, Kitakyushu, JAPAN

2. D. Coggins, D. W. P. Thomas, Y. Zhu, and B. R. Hayes-Gill, 'A New High Speed FPGA Based Traveling Wave Fault Recorder for MV distribution Systems' The 9th International Conference on Developments in Power System Protection 2008 March 17th-20th, 2008 The Crowne Plaza Hotel, Glasgow, UK

3. D. P. Coggins, D. W. P. Thomas, B. R. Hayes-Gill, Y. Zhu, E. T. Pereira, and S. H. L. Cabral 'Initial Experiences with a new FPGA based traveling wave fault recorder installed on a MV distribution network', POWERCON2008 & 2008 IEEE Power India Conference Accepted for oral presentation

4. D. P. Coggins, D. W. P. Thomas, M. Sumner, 'Fault Location on a Branched Network using Time Domain Reflectometry' Submitted to the IEEE Journal on Industrial Electronics

5. D. P. Coggins, D. W. P. Thomas, 'Single-Ended Traveling Wave Fault Location on a Radial Distribution Line' Submitted to the IEEE Journal on Power Delivery

# *Acknowledgements*

I would like to express my sincere thanks to my supervisor Dr. Thomas who has provided advise and encouragement. Thanks also go to Dr. Zhu and Dr. Hayes-Gill for their guidance with the design of the fault recorder hardware. I would like to thank Dr. Pereira and Dr. Cabral at FURB university in Brazil for their hospitality and assistance. I would also like to pay thanks to CELESC power company for allowing access to their distribution network. I would like to express a special thanks to Hoang Nyugen who was involved in the design of the fault recorder hardware and has been a good friend over the past four years. Finally I would like to thank my family and friends who have encouraged me and helped me through some difficult times.

# Contents

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# Abbreviations

| **Acronym** | **What (it) Stands For** |
|---|---|
| **AC** | Alternating Current |
| **ADC** | Analogue to Digital Converter |
| **ANN** | Artifical Neural Network |
| **ATP** | Alternative Transient Program |
| **AWG** | Arbitary Waveform Generator |
| **CT** | Current Transformer |
| **DAC** | Digital to Analogue Converter |
| **DC** | Direct Current |
| **DNO** | Distribution Network Operator |
| **EHV** | Extra High Voltage |
| **EMTP** | Electro Magnetic Transient Program |
| **EMTDC** | ElectroMagnetic Transients including DC |
| **ENOB** | Effective Number Of Bits |
| **DCM** | Digital Clock Manager |
| **DLL** | Digital Lock Loop |
| **DSP** | Digital Signal Processor |
| **EDK** | Embedded Development Kit |
| **FIFO** | First In First Out |
| **FPGA** | Field Programmable Gate Array |
| **GA** | Genetic Algorithm |
| **GPS** | Global Positioning System |
| **JTAG** | Joint Test Action Group |
| **MSPS** | Mega Samples Per Second |
| **MV** | Medium Voltage |

| | |
|---|---|
| **OPB** | **O**nboard **P**eripheral **B**us |
| **PC** | **P**ersonal **C**omputer |
| **pps** | **p**ulse **p**er **s**econd |
| **PROM** | **P**rogrammable **R**ead **O**nly **M**emory |
| **QDR** | **Q**uad **D**ata **R**ate |
| **SINAD** | **S**ignal **I**n **N**oise **A**nd **D**istortion |
| **SPI** | **S**erial **P**rogramming **I**nterface |
| **TWFL** | **T**raveling **W**ave **F**ault **L**ocator |
| **USB** | **U**niversial **S**erial **B**us |
| **UTC** | **C**oordinated **U**niversal **T**ime |
| **VHDL** | **V**ery high speed integrated circuit **H**ardware **D**escription **L**anguage |
| **VT** | **V**oltage **T**ransformer |

# Physical Constants

Speed of Light $c = 2.997\,924\,58 \times 10^{8}\ \mathrm{ms}^{-\mathrm{S}}$

Electric Permittivity $\epsilon_0 = 8.854\,187\,817 \times 10^{-12}\ \mathrm{Fm}^{-1}$

Magnetic Permeability $\mu_0 = 4\pi \times 10^{-7}\ \mathrm{NA}^{-2}$

# Symbols

| | | |
|---|---|---|
| $C$ | capacitance | F |
| $L$ | inductance | H |
| $R$ | resistance | $\Omega$ |
| $\rho$ | reflection coefficient | |
| $T$ | transmission coefficient | |
| $\omega$ | angular frequency | $\mathrm{rads}^{-1}$ |
| $\gamma$ | propagation constant | |
| $\alpha$ | attenuation constant | |
| $\beta$ | phase constant | |
| $[S]$ | modal voltage transform matrix | |
| $[Q]$ | modal current transform matrix | |
| $[Y]$ | admittance matrix | |
| $[Z_s]$ | surge impedance matrix | |
| $[V]$ | voltage matrix | |
| $[I]$ | current matrix | |
| $[U]$ | unit matrix | |

*In memory of Dad. . .*

# Chapter 1

# Introduction

## 1.1 Introduction to Thesis

The ability to successfully locate faults on power distribution systems has a significant impact on the reliability, safety, quality and economic performance of the network. There has been considerable investment in the power transmission system over the past two decades to develop a variety of different techniques to accurately and reliably locate faults. Transmission systems have been the main target for investment because of the widespread impact a fault can have on the performance of the network as well as the amount of time that is required to physically check the long transmission line lengths. In recent years however there has been increased interest and investment in applying fault location techniques to distribution networks.

Approximately 75 percent of all customer hours lost on the traditional power delivery system are as a result of faults that occur on the distribution network [1]. Since the introduction of deregulated market conditions and the emphasis on Distribution Network Operators (DNOs) to improve performance and promote efficiency, the importance of accurate fault location has increased.

Migrating the online fault location techniques developed for transmission networks to the distribution network is not a trivial task. There are many additional complexities introduced at the distribution level which must be accounted for if fault location methods are to be successful. These include, but are not limited to, the topologies of the network, the shorter lengths of the distribution lines, the loads connected to the network and the required accuracy. These factors must also be balanced with the financial investment required by the network operators.

Fault location techniques can be broadly classified into impedance based methods, traveling wave based methods and knowledge based methods. The work in this thesis investigates the transition of traveling wave based methods from transmission lines to branched radial distribution lines. When a short circuit fault occurs their is a sudden collapse of voltage at the fault location. The abrupt change in operating conditions causes high frequency traveling waves to be generated which propagate in both directions away from the fault. The location of the fault can be estimated by capturing the fault generated transient and making synchronised measurements at two or more locations on the transmission line and comparing the differences in the arrival times of the initial waves or by analysing the traveling wave pattern at one location and identify the time between the initial wave and the reflected wave from the fault location. Double ended methods have proven to be reliable on Extra High Voltage(EHV) transmission lines [2–5] but a consistently reliable single-ended scheme is more favourable because there is no need for a communication channel to exist between remote ends and there is also no need for accurate time synchronisation. The problem with existing single-ended fault location schemes is that it is difficult to always correctly identify the reflected wave from the fault location from other reflected waves.

On a distribution line the problem of identifying the wave reflected from the fault location is made more difficult by the additional points of reflection resulting from sub-feeders that branch off the main line. For fault generated transients, reflections from sub-feeder junctions tend to dominate over the reflection from the fault location [6]. There have been a number of proposals of how to perform single ended traveling wave fault location on radial distribution lines [7–9]. Most schemes still involve analysis of the fault waveform (or the features extracted from the fault waveform) by a skilled engineer.

The majority of fault location schemes that have been proposed for branched distribution lines have only been applied to simulated data. There are very few examples of traveling wave fault location schemes which have been applied to real distribution line fault data [10]. Commercially available traveling wave fault recorders were originally designed to be operated on transmission systems [11] and as such are not suited to the shorter lengths of distribution lines and the added complexities their topologies introduce. A higher sampling frequency and higher bit resolution is required to capture the traveling wave data at sufficient fidelity.

## 1.2 Objective of Thesis

It has already been established [9] that a technique called time tree analysis gives a good approximation to the traveling wave pattern simulated for a fault at a given location on a radial distribution line. Time tree analysis uses the principle of the Bewley lattice diagram which is a visual representation of wave propagations and points of reflection in a network. Time tree analysis uses a computer program to keep track of all the waves on a network following a disturbance. The key advantages of time tree analysis is the speed at which the traveling wave pattern can be calculated and the ease at which the network can be reconfigured to represent different fault conditions. A thorough investigation into the performance of time tree analysis will be conducted for the most common types of faults and fault resistances to establish the maximum size and complexity of radial distribution line that time tree analysis can successfully represent.

Impedance based fault location schemes which use optimisation techniques such as genetic algorithms have been proposed for transmission networks [12, 13] but so far have not been applied to traveling wave data. One of the main reasons for this is the long computation time that is required for traveling wave simulations. In this thesis the fast calculation and reconfigurability of time tree analysis will be exploited by using a genetic search optimisation algorithm to provide an autonomous fault location scheme for single ended traveling wave data on a radial distribution line. Initially this will be evaluated against simulated network data.

A new high speed fault recorder will be designed and constructed, capable of recording traveling wave fault data from distribution lines. The fault recorder will be deployed on a radial distribution line operated by CELESC power company. CELESC own and operate the distribution network in the Santa Caterina region of Brazil. They are currently involved in research activities with the Universidade Regional de Blumenau (FURB) to develop traveling wave based fault location schemes. They have kindly given access to part of their network.

It is proposed to evaluate the time tree genetic search algorithm with real fault data captured by the fault recorder installed in Brazil. To provide an alternative, if the recorder fails to record any fault data from the distribution line, a radial communication line will be used to evaluate the performance of the time tree genetic search algorithm. It will be shown that the time tree genetic search algorithm has numerous areas of applications other than power distribution lines.

The main objectives for the thesis are summarised below:

- Develop a genetic search algorithm based on the concept of time tree analysis to provide an automated single ended fault location scheme for branched distribution lines.
- Develop a new traveling wave fault recorder design for radial distribution systems capable of recording high fidelity traveling wave data suitable for single ended fault location as well as providing accurate time tagging of data so that double ended fault location (where relative time is important) can also be applied.
- Evaluate the performance of the time tree genetic search algorithm against simulated and recorded data.

## 1.3 Outline of Thesis

The rest of this thesis is structured as follows.

Chapter 2 provides a comprehensive review of the existing techniques used for fault location on power systems as well as emerging schemes and technologies which have been proposed. An overview of the distribution network including typical network topologies, the types of faults that can occur and the most common methods of fault location are presented.

Chapter 3 looks at how traveling waves behave on a three phase power system and provides some examples of typical fault conditions.

Chapter 4 presents the proposed fault location method which combines the concept of time tree analysis with a genetic search algorithm to provide an autonomous method of estimating fault locations.

Chapter 5 gives an in depth description of the hardware design and FPGA/VHDL design of the new traveling wave fault recorder.

Chapter 6 presents the results and lessons learn from the deployment of the fault recorder on the distribution line in Brazil. The genetic algorithm is evaluated against a radial communication network which was constructed at the University of Nottingham.

Chapter 7 provides a summary of the work and the conclusions drawn. Areas for further work are identified.

# Chapter 2

# Fault Location

## 2.1 Introduction

This chapter reviews existing fault location methods and draws particular attention to the complications that the distribution network introduces. Fault location is one component of what is referred to as fault management, which includes fault protection, fault identification and system restoration. Although many of the analysis techniques described in this chapter have also been applied to fault protection, identification and to a limit extent restoration, their focus has been different. For example, fault protection is a real time technique in which the speed of operation is of primary concern. In contrast, fault location is an off-line analysis technique in which the speed of operation is not as crucial but accuracy is more important and time can be spent performing more complex calculations to improve the accuracy.

The traditional power delivery system consists of power generation, transmission, distribution, and consumption. Transmission networks deliver the energy generated at power stations over long distances to substations. The distribution network then delivers the power from the substation to the point of consumption. The distribution network differs from the transmission network in a number of key attributes [14]. The topology of transmission networks are normally point-to-point or mesh topologies connected through substation whereas the distribution network consist of many radial lines which are interconnected with each other. The topology of distribution networks are also more frequently subject to reconfiguration. The typical line lengths on transmission networks are of the order of hundreds of kilometres whereas on distribution networks, lengths are typically of the order of tens of kilometres. Sub-feeders that branch off the main distribution line are typically of the order of a kilometre or less. Unlike transmission networks, distribution networks have loads tapped off the main line at various points along its length. A more recent development has been the introduction of distributed generation to the distribution network. All of these differences introduce complications to the fault location at the distribution level. If the fault location schemes developed for the transmission network are to be adopted on the distribution network they must first be adapted to account for the additional complications. Further details of fault location techniques can be found in [15–17].

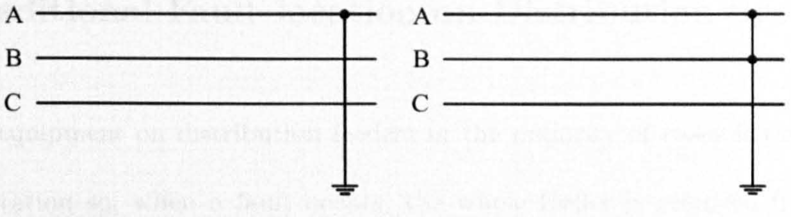
## 2.2 Short Circuit Faults

The causes of short circuit faults on a power network can vary largely. The frequency of certain types of faults depend on the geographical location of the network and the climate. For example, in tropical countries, a large proportion of faults are caused by lightning strikes. Power networks which are constructed from overhead lines are more susceptible to fault events. In most cases the cause of faults fall under one of the following categories [1]:

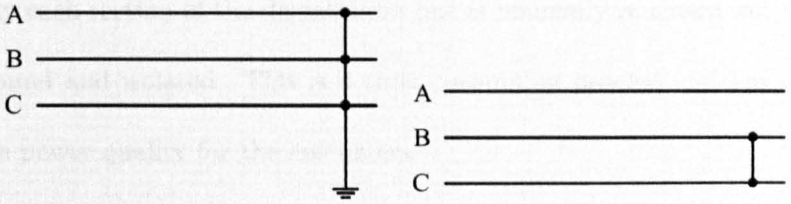
- Lightning
- Insulation failure
- Human Accident or Vandalism
- Vegetation or animals contacting the electrical circuits

Faults on an MV network can be either transient or permanent in nature. Transient faults are the most common type of faults and can be cleared by simply de-energizing the line for a short amount of time. Typically when a fault is detected on a network circuit breakers at the ends of the line operate to de-energize the line. After a short period of time an attempt is made to re-energize the line. If after a number of attempts, the circuit breakers still trip, the fault is assumed to be permanent and the line remains de-energized until the fault is located and repaired. Permanent faults require the fault location method to be as accurate as possible so that the fault can be identified, repaired and power restored in the shortest possible time.

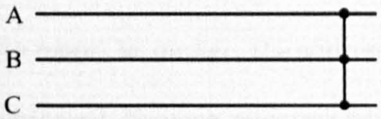
For three phase power systems, faults can be classified as one of the following:



(a) Single phase to earth fault (b) Double phase to earth fault



(c) Three phase to earth fault (d) Phase to phase fault



(e) Three phase fault

FIGURE 2.1: Types of Faults

- Single phase to earth fault. This can be either phase-A to earth, phase-B to earth or phase-C to earth. A phase-A to earth fault is shown in Fig. 2.1(a).
- Double phase to earth fault. This can be either phase-A to phase-B to earth, phase-A to phase-C to earth or phase-B to phase-C to earth fault. A phase-A to phase-B to earth fault is shown in Fig. 2.1(b).
- Three phase to earth fault. This is phase-A to phase-B to phase-C to earth and is shown in Fig. 2.1(c).
- Double phase fault. This can be either phase-A to phase-B, phase-A to phase-C or phase-B to phase-C. A phase-B to phase-C fault is shown in Fig. 2.1(d).
- Three phase fault. This is phase-A to phase-B to phase-C fault and is shown in Fig. 2.1(e).

## 2.3 Traditional Fault location on Distribution Systems

Protection equipment on distribution feeders in the majority of cases is only installed at the substation so, when a fault occurs, the whole feeder is removed from service. Traditionally each section of the distribution line is manually re-closed until the faulted section is found and isolated. This is a time consuming process and has a significant effect on the power quality for the customers.

Another method of fault location is to use the power outage reports from customers. When a customer phones up to report an outage, the address of the customer is recorded. This is then used by an experienced dispatch engineer who has detailed knowledge of the distribution network topology and can isolate and deploy ground crew to the most likely faulted section.

In both methods the location of the fault can only be resolved to the section of distribution line where the fault is located. This could represent a few kilometres of line length, depending on the network configuration, which would have to be manually patrolled to find the exact fault location. When a transient fault occurs, the dispatch engineer will not receive any outage reports as to when and where the fault occurred [14]. Transient faults may lead to permanent faults. Accurate information about transient faults can help DNO's take preventive action before the transient fault potentially becomes a permanent fault.

## 2.4 Methods of Fault Location

Fault Location methods can be broadly classified into impedance based methods, traveling wave based methods and knowledge based methods as shown in Fig. 2.2. Impedance and traveling wave based methods can be further classified into single-ended and double-ended techniques. Double-ended methods require data to be recorded at two locations on the transmission or distribution line (typically at the line ends) and single-ended methods require data from one location only (typically at a substation).

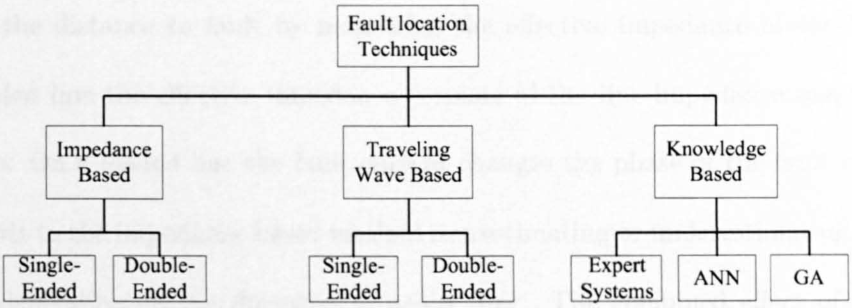


FIGURE 2.2: Classification of fault location methods

### 2.4.1 Impedance Based Methods

Impedance based methods are concerned with measuring the power frequency phase voltages and currents to calculate the line impedance. The fault location is estimated by expressing the distance from substation to fault as a function of impedance. This can be achieved by single-ended or double-ended methods.

There are a number of examples proposed in the literature of both single-ended [18, 19] and double-ended [20, 21] fault location schemes. Impedance based methods are particularly attractive to DNOs because the phasor voltage and current measurements do not require expensive specialist measuring equipment.

The distribution network introduces complications to the impedance based methods in a number of ways [14, 15, 22]. Since most distribution lines have a radial or interconnected topology, a distance to the fault from the substation as a function of impedance can relate to more than one geographical location. Distribution lines that consist of both underground and overhead lines do not have the same impedance along their length so there is not a simple linear relationship between distance and impedance. Distribution lines which have loads connected along their length contribute to the fault current and it is very difficult to predict their contributions in advance. Impedance based methods estimate the distance to fault by measuring the effective impedance of the line. On an unloaded line the effective impedance consists of the line impedance and the fault resistance. On a loaded line the fault current changes the phase of the fault resistance which leads to the impedance based method overestimating or underestimating the fault location depending on the direction of power flow. The combined effect of the fault resistance and load current is known as the reactance effect. A distribution system can either be solidly grounded, ungrounded or Peterson's coil / resistance grounded. Single phase faults that occur on the ungrounded and resistance grounded systems result in a much smaller fault current when compared with a solidly grounded distribution systems making it difficult to detect the fault.

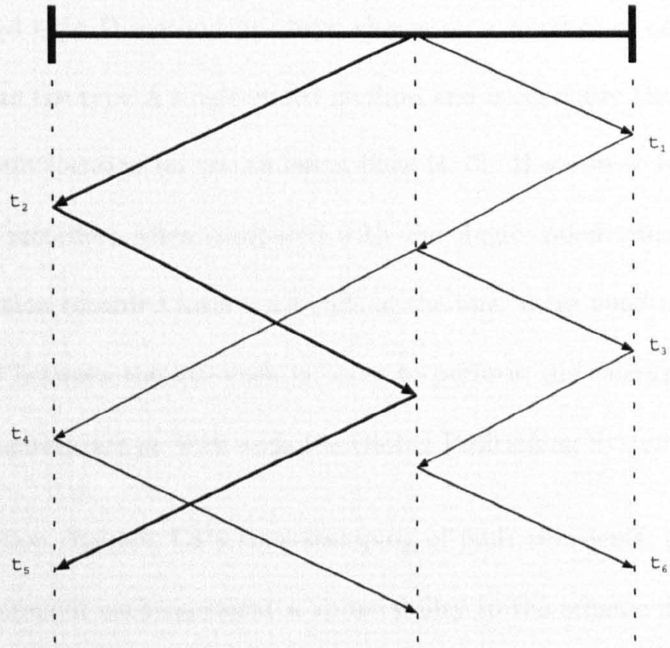
Further details of impedance based fault location techniques which have been improved to cope with the additional complexities distribution lines present can be found in [23–25].

### 2.4.2 Traveling Wave Based Methods

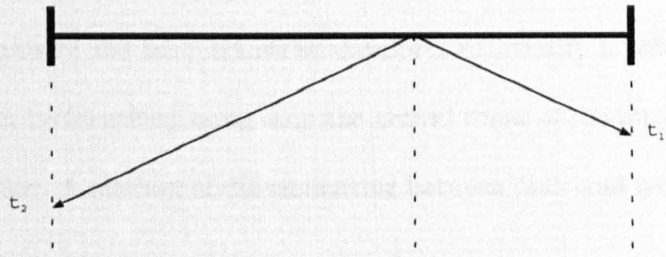
Traveling wave fault location is a well known and established technique for accurately locating faults on E.H.V transmission lines [2–5, 26, 27]. There have been a number of schemes proposed for High Voltage Direct Current (HVDC) systems [28–30], underground power cables [31–33] and for radial distribution lines [6, 9, 34]. When a short circuit fault occurs on a transmission line or distribution line there is a sudden collapse in voltage at the fault location. The abrupt change in operation conditions causes high frequency traveling waves, super imposed on the power frequency signal, to propagate in both directions away from the fault position. The traveling waves propagate at a velocity dictated by the electric permittivity and magnetic permeability of the surrounding medium. For overhead transmission lines, where the surrounding medium is air, the velocity of propagation is close to the speed of light. For underground cables the velocity of propagation is of the order of 2/3 the speed of light.

Traveling wave fault location is classified into types A, B, C, D and E modes of operation [35]. Their modes of operation are depicted in Fig. 2.3. Type A is a single-ended method which measures the fault generated transients at one location only and relies on identifying the second incident pulse reflected from the fault location. Type B and D are double-ended methods that require measurements from both ends of the line. In the type B method a timer is started when a traveling wave reaches the end of the transmission line nearest the fault. Traveling waves reaching the other end of the transmission line trigger a transmitter which sends a stop signal to the timer. The time delay can be used to calculate the distance to the fault. In the type D method the fault location is calculated using the absolute arrival times of the initial wave fronts at each end of the line. This is acheived by syncronising the recorders at each end using GPS timing. Type C method uses pulse generating equipment to inject a signal and can therefore only be used when the line is de-energised. Type E method uses the traveling waves generated from a circuit breaker re-closure when an attempt is made to re-energise the transmission line [27, 36]. Both methods work by measuring the time difference between the injection of a signal into the line at one end and subsequent reflection from the fault point.

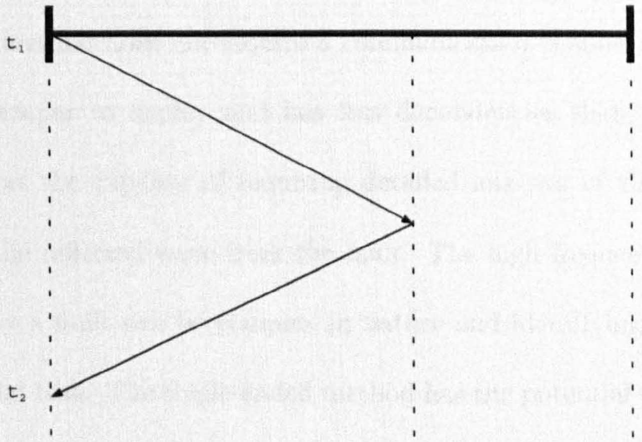
The on-line methods are preferred to the off-line methods because they do not require special pulse generating equipment and can be used whilst the line is in operation.



(a) Type A fault location



(b) Type B and D fault location



(c) Type C and E fault location

FIGURE 2.3: Types of traveling wave fault location

On-line techniques are also able to identify transient faults.

The double-ended type D method has been shown on a number of deployments to be more reliable than the type A single-ended method and is currently the preferred implementation for fault location on transmission lines [4, 5]. However it requires twice the amount of fault recorders when compared with the single-ended scheme, and, since it requires information recorded from both ends of the line, there must also be a communication channel between the line ends in order to perform the calculation. To provide syncronised measurements at both ends the Global Positioning System (GPS) is used.

The communication channel, GPS time-stamping of fault transients, and multiple sets of recording equipment each represent a vulnerability to the scheme if any were to fail to operate as expected. The key advantage of the double-ended scheme is that is does not require analysis of the fault transient waveform to identify a reflected wave. The fault location can be identified using only the arrival times of the initial wave fronts at each end of the line. A method of discriminating between fault and non-fault transients is also necessary.

The single-ended method does not require a communication channel or accurate time-stamping so is cheaper to deploy and has less dependencies than the double-ended scheme. This is at the expense of requiring detailed analysis of the recorded waveform to identify the reflected wave from the fault. The high frequency traveling wave patterns caused by a fault can be complex in nature and identifying the correct wave front is not a trivial task. The single-ended method has the potential to provide greater accuracy than the double-ended method because it is not limited by the accuracy of the GPS time-stamping (typically +/- 100 ns) but is instead limited by the sampling frequency of the recorder and the bandwidth of the transducers used to capture the traveling waves. The closer a fault is to the fault recorder, the more difficult it is to identify the correct fault location using the single-ended scheme because the amount of time between the initial wave and the reflected wave is reduced.

In both the double-ended scheme and single-ended scheme, faults that occur close to zero inception angle are difficult to detect because the traveling waves which are produced are small. The advantages of traveling wave fault location over impedance based methods is the potential accuracy that is achievable. Typically impedance based methods at best can achieve an accuracy of between 2-5% of the line length [15], Traveling wave fault location has achieved accuracy to within 500m [4].

The accuracy of impedance based methods are affected by loads connected directly to the line because they contribute to the fault current and alter the effective impedance measured. Since most loads are inductive they appear as a large impedance at high frequencies so have little effect on the traveling waves propagating down the transmission line [37]. The same can be said for distributed generation that may be connected to the line [37].

A Bewley lattice diagram [38] of a fault that has occurred on a transmission line is shown in Fig. 2.4. A fault has occurred a distance $x$ from substation A. Traveling waves propagate in both directions towards substation A and substation B. Fig. 2.5 shows the traveling wave pattern observed at substation A for a fault that has occured 1km from substation A. The total length of the transmission line is 3km. The signal has been high pass filtered to remove the power frequency component.

If the double-ended scheme is being used then the fault location can be estimated using equation (2.1):

$$x = \frac{(t_2 - t_1)u}{2} + \frac{L}{2} \tag{2.1}$$

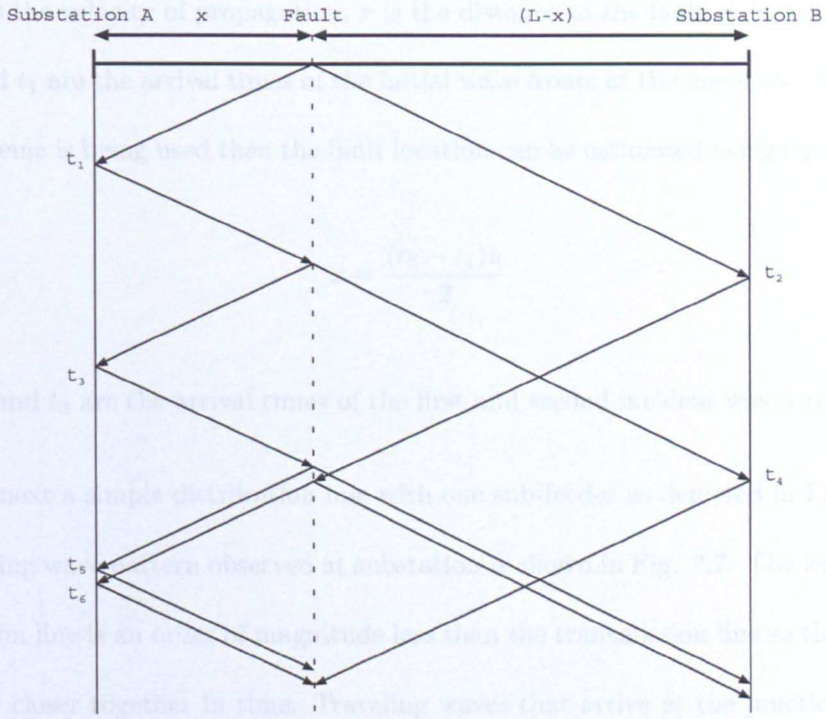


FIGURE 2.4: A Bewley Lattice diagram depicting a fault that has occurred between substation A and substation B

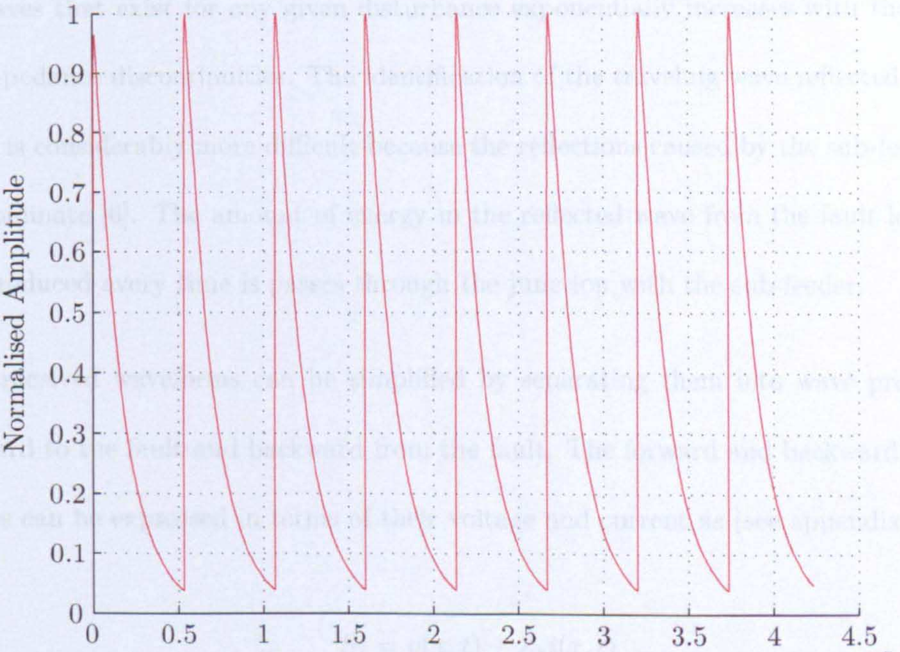


FIGURE 2.5: Traveling wave pattern observed at substation A for a fault 1 km from substation A

where $u$ is the velocity of propagation, $x$ is the distance to the fault, $L$ is the line length and $t_2$ and $t_1$ are the arrival times of the initial wave fronts at the line ends. If the single ended scheme is being used then the fault location can be estimated using equation (2.2)

$$x = \frac{(t_3 - t_1)u}{2} \tag{2.2}$$

where $t_1$ and $t_3$ are the arrival times of the first and second incident waves respectivley.

Consider next a simple distribution line with one sub-feeder as depicted in Fig. 2.6 and the traveling wave pattern observed at substation A shown in Fig. 2.7. The length of the distribution line is an order of magnitude less than the transmission line so the traveling waves are closer together in time. Traveling waves that arrive at the junction between the sub-feeder and main line experience a discontinuity in the characteristic impedance. This causes both reflected and transmitted traveling waves to be generated. The number of waves that exist for any given disturbance exponentially increases with the number of impedance discontinuities. The identification of the traveling wave reflected from the fault is considerably more difficult because the reflections caused by the sub-feeder tend to dominate [6]. The amount of energy in the reflected wave from the fault location is also reduced every time is passes through the junction with the sub-feeder.

The received waveforms can be simplified by separating them into wave propagating forward to the fault and backward from the fault. The forward and backward traveling waves can be expressed in terms of their voltage and current as (see appendix A):

$$S_1 = v(x,t) + Z_s i(x,t) \tag{2.3}$$

$$S_2 = v(x,t) - Z_s i(x,t) \tag{2.4}$$

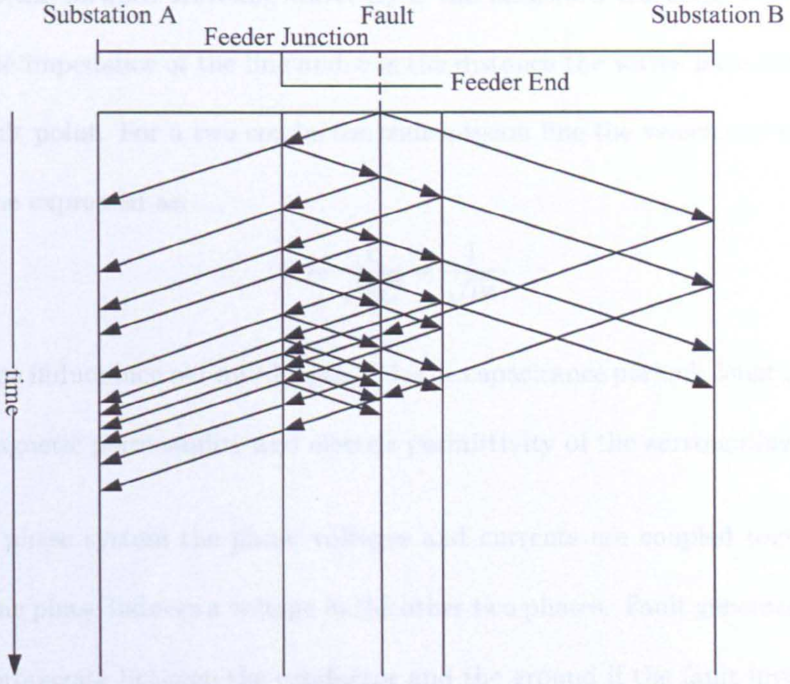


FIGURE 2.6: Bewley lattice diagram for a fault that has occurred on a distribution line with one sub feeder

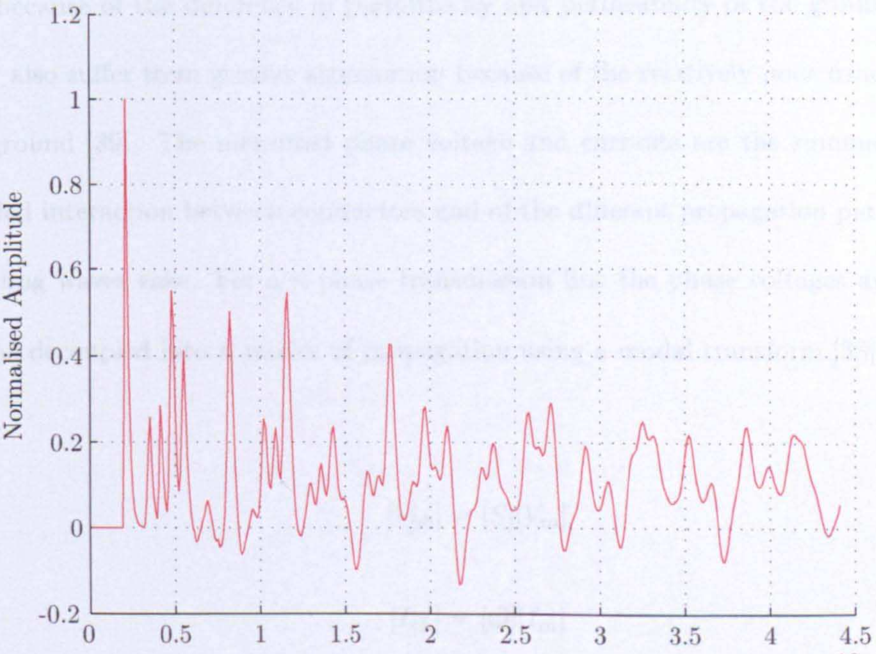


FIGURE 2.7: Transient waveform observed at substation A for a fault that has occurred on a distribution line with one sub feeder

Where $S_1$ is the forward traveling wave, $S_2$ is the backward traveling wave, $Z_0$ is the characteristic impedance of the line and $x$ is the distance the waves have traveled away from the fault point. For a two conductor transmission line the velocity of wave propagation can be expressed as:

$$u = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{\mu\epsilon}} \tag{2.5}$$

where $L$ is the inductance per unit length, $C$ is the capacitance per unit length, and $\mu$ and $\epsilon$ are the magnetic permeability and electric permittivity of the surrounding medium.

On a three phase system the phase voltages and currents are coupled together i.e. a current in one phase induces a voltage in the other two phases. Fault generated traveling waves can propagate between the conductor and the ground if the fault involves a conduction path to ground. Traveling waves that propagate in the ground have a velocity of propagation much lower than traveling waves that propagate just between the conductors because of the difference in permittivity and permeability of the ground medium. They also suffer from greater attenuation because of the relatively poor conductivity of the ground [39]. The measured phase voltage and currents are the summation of the coupled interaction between conductors and of the different propagation paths that the traveling waves take. For a $n$ phase transmission line the phase voltages and currents can be decoupled into $n$ modes of propagation using a modal transform [38] such that:

$$[V_{ph}] = [S][V_m] \tag{2.6}$$

$$[I_{ph}] = [Q][I_m] \tag{2.7}$$

where $[V_m]$ are the modal voltages, $[I_m]$ are the modal currents, $[V_{ph}]$ are the phase voltages, $[I_{ph}]$ are the phase curres, $[S]$ is the modal voltage to phase voltage transform matrix and $[Q]$ is the modal current to phase current transform matrix. For a balanced three phase system, mode 0 (commonly known as ground mode), contains signals which have propagated through the ground. For a fully transposed line this is equivalent to the zero sequence component. Modes 1 and 2 (commonly known as aerial modes) contain signals which have traveled only between the conductors.

The characteristic impedance can be expressed in terms of the transmission lines inductance and capacitance per unit length as:

$$Z_s = \sqrt{\frac{L}{C}} \tag{2.8}$$

When a traveling wave reaches a discontinuity in the characteristic impedance of the line, such as at a busbar at a substation, a junction with a sub feeder, or the fault location itself, two waves are formed; one which is reflected and one that continues past the discontinuity. The amount of energy in the reflected and refracted wave is related to the ratio of the characteristic impedances at the discontinuity as (see appendix A):

$$\rho_v = -\rho_i = \frac{Z_b - Z_a}{Z_b + Z_a} \tag{2.9}$$

where $\rho_v$ is the voltage reflection coefficient, $\rho_i$ is the current reflection coefficient, $Z_a$ is the impedance of the line containing the incident wave and $Z_b$ is the impedance seen looking into the discontinuity. The transmission coefficient is defined as (see appendix A):

$$T_v = 1 + \rho_v \tag{2.10}$$

where $T_v$ is the voltage transmission coefficient and $T_i$ is the current transmission coefficient. The propagation, reflection and refraction of traveling waves continues until the energy has been dispersed and a new steady state is reached.

#### 2.4.2.1 Correlation Techniques

Correlation is a popular technique used in single-ended fault location on transmission lines to identify the reflected wave from the fault location. Correlation is used to measure the similarity between two signals. The cross-correlation function of two signals, $x(t)$ and $y(t)$ is defined as:

$$r_{xy}(\tau) = \frac{1}{T_0}\int_0^{T_0} x(t)y(t+\tau)dt \tag{2.11}$$

The auto correlation of a signal is defined similarly to the cross-correlation but instead measures the similarity between a signal and a time shifted version of itself.

$$r_{xx}(\tau) = \frac{1}{T_0}\int_0^{T_0} x(t)x(t+\tau)dt \tag{2.12}$$

Correlation can either be performed as an auto-correlation of the initial traveling wave or by separating the traveling waves into forward and backward components and cross-correlating the initial backward traveling wave with all other forward traveling waves [40]. In both techniques a peak in the cross-correlation function occurs at a time $\tau$ which is equal to the round trip time of the traveling wave from the fault location.

To obtain the forward and backward traveling waves, $S_1$ and $S_2$ in equations 2.3 and 2.4 requires both the high frequency voltage and high frequency current signals. Measuring the current is a relatively simple task that can be achieved by measuring the current in the secondary of an existing current transformer and using a suitable current probe to extract the high frequency components [6] because conventional CTs have a bandwidth wide enough to include the traveling wave components. However, extracting the high frequency voltage using conventional CVTs is not so straight forward because CVTs are tunned to the power frequency bandwidth. They have a very poor high frequency response and filter out the high frequency traveling waves [41].

In [2] a method was proposed for inferring the high frequency voltage transients by estimating the instantaneous impedance of the busbar to which the transmission line is connected to. This is achieved by simultaneously measuring the current in at least two other transmission lines that are connected to the same busbar. Using the estimated bus bar impedance, the high frequency voltage signals can be inferred.

Both the auto correlation and cross correlation methods work well for a low impedance fault on a single transmission line but are less reliable for high impedance faults where the reflection from the fault location is small or when the transmission line is connected to other lines as part of a larger network. Under these circumstances it is harder to differentiate the peak in the cross correlation function relating to the fault from other points of reflection.

#### 2.4.2.2 Time Tree Analysis

It has been shown that correlating simulated data with recorded fault data produces very high degrees of correlation under a variety of fault conditions including single phase faults [42]. The downside of such an approach is the long simulation times required to accurately simulate different fault locations and fault conditions. Distribution networks are subject to reconfiguration on a regular basis so the exact layout of the network must be known at the time of the fault and the simulation model changed accordingly.

Time Tree Analysis was first proposed by [4] as a method of fault location. The technique works by keeping a record of the amplitude and path traveled by each wave, starting at the fault point, and propagating throughout the network. An observation point on the network is specified and a pulse array is generated representing the time and amplitude of every pulse that arrived at the observation point. The pulses can then be shaped to estimate the wave shaping caused by the network.

In [9], time tree analysis was applied to single-ended traveling wave analysis on a radial distribution line. It was shown that time tree analysis showed very strong correlation with EMTP simulations of the same network. The advantage of time tree analysis is the short computation time and the speed at which the time tree can be reconfigured to represent a new fault condition when compared with traditional simulation programs. Using the time tree technique over a hundred fault scenarios can be predicted in under a second for a typical network configuration. EMTP simulations in contrasts require manual reconfiguration of the network topology to insert a fault and recalculation of the affected transmission line sections. Time tree analysis is therefore an ideal candidate to form the basis of an automatic search algorithm which is recognised by [4] but so far has not been implemented.

#### 2.4.2.3 Wavelet Analysis

In both the double-ended and single-ended schemes the precise identification of the beginning of the traveling wave fronts is crucial to accurate fault location. As a wave propagates along a transmission line it suffers from attenuation and distortion which changes the shape of the wave front. The wavelet transform is a signal processing technique which has been widely adopted as a method of identifying the exact arrival times of traveling waves for both double-ended [7, 43] and single-ended schemes [34, 44]. Wavelet analysis allows a signal to be analysed whilst being localised in both frequency and time which makes it ideally suited to the analysis of transient signals which only exist for a short period [44]. Wavelets are mathematical functions that analyse the input signal at different frequencies. The shape of the wavelet changes with frequency so that is most suited to the analysis at each particular frequency scale. A whole family of wavelets is derived by scaling and translating a mother wavelet. Narrow wavelets are used for the analysis of high frequency components and broad wavelets are used for the analysis of low frequency components. Wavelet analysis can either be performed as a Continuous Wavelet Transform (CWT) [45] or as a Discrete Wavelet Transform (DWT). A CWT considers all possible scaling values to produce a continuous time-scale domain analysis of the signal. As a result, CWT is computationally intensive. A DWT considers only a discrete number of scales and can be implemented efficiently as a series of cascading band pass filters. There are also examples of where wavelet analysis has been used to de-noise traveling wave signals [46].

#### 2.4.2.4 Application to Distribution Lines

The implication of a radial network topology is that the traditional single-ended correlation technique, which calculates the distance to fault, can correspond to more than one fault location. Further analysis of other wavefronts is necessary to discriminate the most likely fault location. Since there are many more sets of traveling waves reverberating around the network when a disturbance occurs, at certain positions in the network waves can either constructively or destructively interfere with each other. This further adds to the difficulty in identifying the origins of the wavefronts.

If a fault occurs on a sub feeder the double ended method (that uses relative arrival times) can only resolve the position of the fault to the point where the sub-feeder joins the main line. In [8] and [7] schemes are proposed that place fault recorders at the end of each sub-feeder to provide total coverage of the distribution line but this is very costly and there may also not be suitable places to install all the recorders. In [6] a method is proposed where single-ended methods are combined with double-ended methods to correctly identify a fault that has occurred on a sub-feeder. First the faulty feeder is identified using the double-ended method and the fault distance along the feeder is estimated using the single ended method.

In [47] a scheme for identifying the faulted section of the distribution line is proposed by analysing the sums of squares of the wavelet transform coefficients. It is shown that the lower scale wavelet coefficients which correspond to the high frequency traveling wave data exhibit distinguishable responses depending on which section of the distribution line the fault is located. Using this method the exact location along the faulted section cannot be estimated and the author suggests the use of more conventional impedance based approach once the faulted section has been identified. The idea of using wavelet analysis as a feature extraction method is developed further in [48] for fault location on a rural inefficiently grounded distribution line. The faulted section is first identified by comparing the energy in the wavelet coefficients and then type C traveling fault location is performed to inject a short duration high voltage pulse into the distribution line. The reflected wave from the fault is identified with knowledge of the faulted section to estimate the fault location.

### 2.4.3 Knowledge Based Methods

Knowledge based methods are those that take a heuristic approach to arrive at a solution as opposed to an algorithmic approach. Heuristic approaches are particularly suited to complex problems where it would otherwise be too difficult or impossible to formulate the problem deterministically.

#### 2.4.3.1 Expert Systems

An expert system is a software system that attempts to provide the same service as a human expert or group of human experts would on a particular subject. This is achieved by creating a knowledge base and a rule base relating the knowledge. The expert system is interrogated by posing questions and using an inference engine it is able to deduce information through logical reasoning. There are a number of examples in the literature of expert systems being used to locate faults on distribution systems[49, 50]. In [49] an expert system is used to emulate the behavior of an experienced dispatcher in diagnosing distribution system faults. The expert system consists of a database containing information about feeder circuit configuration and geographical maps of feeder locations. When a fault occurs on the network phone calls from interrupted customers are received. The addresses of the interrupted customers are fed into the expert system which then deduces the most likely locations of the fault.

#### 2.4.3.2 Artificial Neural Networks

An artificial neural network is a computational model based on biological networks similar to those that exist in nature and was inspired by research on the central nervous system. The network consists of a large number of node elements which are connected through a series of weighted connections. The nodes and connections are organised into layers such that nodes only have connections with preceding node layers. The first layer represents the input and the final layer represents the output with one or more hidden layers existing in between. The network is trained with given input patterns to produce desired output patterns which are obtained by altering the weighting on the connections between nodes. The great advantage of the neural network approach is that through a period of training the network learns by its self rather than having to be programmed. It does not have to be told s specific set of rules like expert systems but instead establishes its own set of rules based on the data it is trained with. However, it is noted [51] that the ability to learn means that the ANN cannot explain to the user how it arrived at its conclusions. Another important point raised by [51] is that whilst ANNs are very good at interpolating data they are poor at extrapolation which means that the training data must be chosen very carefully and comprehensively to include all of the solution space. There are a number of examples in the literature [52, 53]that show that once sufficient training has been performed neural networks can make accurate predictions of fault locations under a variety of fault conditions and fault resistances.

#### 2.4.3.3 Genetic Algorithms

A genetic algorithm is a search technique used to optimise a problem using the mechanics of natural selection. Each solution parameter is encoded, usually as a numerical string, in such a way that for each possible solution a unique numerical gene exists. An initial population is created, usually at random, of genes representing possible solutions. For each gene a value of fitness is calculated which is a measure of its worth to the problem being optimised. Genes are selected to form the next generation of population based on their fitness value. Genes with a higher fitness value on average tend to survive whilst genes with lower fitness values do not. Genes that are selected for the next generation undergo a process of "cross-over" which is a method of combining two genes to produce a new gene containing components of both its parents and a process of mutation which introduces random genetic variation. This process of selection, cross-over, and mutation continues over a number of generations until the algorithm converges on an optimum solution. In [54] and [55] genetic algorithms are used as an optimisation technique for waveform matching the power frequency phasor measurement of fault events on transmission lines. In [55] the technique is applied to situations where only sparsely recorded data is available. Genetic algorithms have so far not be applied to waveform matching of traveling wave data. One of the main reasons for this is the long computation times that traveling wave simulations require and the time it takes to reconfigure the simulation model to represent a different fault condition. However using time tree analysis these problems have been resolved.

## 2.5 Summary

In this chapter a review of the different techniques used for fault locating on both transmission and distribution lines has been presented. There is no single technique that performs well under all circumstances; the impedance based methods are heavily influenced by real time operating parameters whereas the traveling wave based methods struggle with close up faults and close to zero incident fault angles.

The use of knowledge based systems such as artificial neural networks and expert systems allows multidimensional relations between data to be established that would have otherwise been difficult to identify. Genetic algorithms have proven to be particularly effective at rapidly searching a large solution space to find the optimum maximum.

The potential accuracy of traveling wave fault location and its relatively low susceptibility to system operating parameters when compared with impedance based methods makes it attractive as a fault location scheme and is one of the main reasons why its was chosen for this research project. Although the waveforms produced are far more complex than those on transmission lines it has been demonstrated [9] that using the time tree analysis, a waveform closely representing that predicted by simulation can be produced, in a very short computation time. Instead of trying to identify a single reflected wave, the entire fault signature is considered. An absolute location can be specified instead of just a distance to fault which addresses the problem of multiple fault locations on a radial topology.

A genetic search algorithm which exploits the speed of time tree analysis will be developed to efficiently search the fault solution space of a radial distribution line to find the most likely fault location autonomously without the need for interpretation of a complex waveform by a specialised engineer.

# Chapter 3

# Typical Fault Events

## 3.1 Introduction

In this chapter the traveling wave patterns produced for the most common types of faults are presented for an idealised transmission line. The faults considered are three phase to ground faults, phase to phase faults and single phase faults. For each fault condition considered, both the phase measurements and modal components are presented and discussed.

## 3.2 Fault Events on Three Phase Systems

On a three phase system the surge impedance for each phase is made up of not only the self impedance of the conductor but also by the mutual impedance that exists between neighbouring conductors. The surge impedance is expressed in matrix form to relate the phase voltages and phase currents to the self impedance and mutual impedance that exist between each phase. For a single propagating three phase voltage and current wave the three phase voltages are related to the three phase currents as:

$$[V] = \pm[Z_s][I] \tag{3.1}$$

Where $Z_s$ equals:

$$[Z_s] = \begin{pmatrix} Z_{aa} & Z_{ab} & Z_{ac} \\ Z_{ba} & Z_{bb} & Z_{bc} \\ Z_{ca} & Z_{cb} & Z_{cc} \end{pmatrix} \tag{3.2}$$

and the sign depends on the direction of propagation. Definition of symbols can be found in appendix A. Similarly the fault resistance can be express in matrix form by using the fault conductance matrix developed by [56] which allows every combination of short circuit fault condition to be expressed. The fault conductance matrix, $[Y_f]$ is defined as:

$$[Y_f] = \begin{pmatrix} \frac{1}{R_{aa}} + \frac{1}{R_{ab}} + \frac{1}{R_{ac}} & -\frac{1}{R_{ab}} & -\frac{1}{R_{ac}} \\ -\frac{1}{R_{ab}} & \frac{1}{R_{bb}} + \frac{1}{R_{ab}} + \frac{1}{Rbc} & -\frac{1}{R_{cb}} \\ -\frac{1}{R_{ac}} & -\frac{1}{R_{cb}} & \frac{1}{Rcc} + \frac{1}{R_{ac}} + \frac{1}{R_{bc}} \end{pmatrix} \tag{3.3}$$

Fig. 3.1 shows a graphical interpretation of the fault conductance matrix.

Expressions for the initial voltage and current traveling waves can be derived in similar manner to the single phase transmission line in Appendix A. Equation (A.27) can be written in matrix form by substituting the conductance matrix for the fault resistance

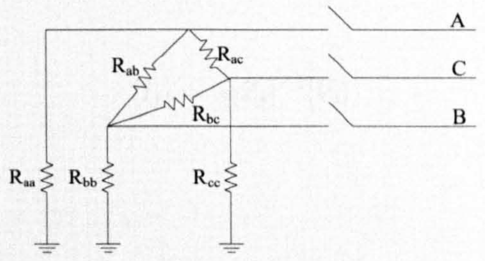


FIGURE 3.1: Representation of the fault conductance matrix

and the impedance matrix for the line surge impedance using the notation used in Appendix A.

The total voltage across the fault is:

$$[V_1] = -[V_f] + [Y_f]^{-1}[I_f] \tag{3.4}$$

The total fault current, $[I_f]$ is given by:

$$[I_f] = 2[I_1] \tag{3.5}$$

$$[I_f] = 2[Z_s]^{-1}[V_1] \tag{3.6}$$

Substituting for $[I_f]$ in equation (3.4) gives:

$$[V_1] = -[2[U] + [Z_s][Y_f]]^{-1}[Z_s][Y_f][V_f] \tag{3.7}$$

where $[U]$ is the unit matrix.

Similarly, the initial current wave $[I_1]$ is given by:

$$[I_1] = -[Z_s]^{-1}[V_1] \tag{3.8}$$

$$[I_1] = [Z_s]^{-1}[2[U] + [Z_s][Y_f]]^{-1}[Z_s][Y_f][V_f] \tag{3.9}$$

### 3.2.1 Reflections at Impedance Discontinuities

The analysis that is performed in Appendix A for reflections at impedance discontinuities on a single phase system is repeated using matrix notation to represent the impedance matrix of the transmission lines. The incident and reflected voltages and current at an impedance discontinuity are related as:

$$[V_t] = [V_i] + [V_r] \tag{3.10}$$

$$[I_t] = [I_i] + [I_r] \tag{3.11}$$

The currents are related to the voltages as:

$$[I_t] = [Z_b]^{-1}[V_t] \tag{3.12}$$

$$[I_r] = -[Z_a]^{-1}[V_r] \tag{3.13}$$

$$[I_i] = [Z_a]^{-1}[V_i] \tag{3.14}$$

Substituting into equation (3.11) and rearranging gives:

$$[V_r] = [[Z_b]^{-1} + [Z_a]^{-1}]^{-1}[[Z_a]^{-1} - [Z_b]^{-1}][V_i] \tag{3.15}$$

where the voltage reflection coefficient is

$$[\rho_v] = -[\rho_i] = [[Z_b]^{-1} + [Z_a]^{-1}]^{-1}[[Z_a]^{-1} - [Z_b]^{-1}] \tag{3.16}$$

### 3.2.2 Reflections at Fault Locations

By substituting for $Z_b$ in equation (3.15) for the parallel combination of the fault conductance matrix and the line surge impedance matrix and rearranging gives:

$$[V_r] = -[2[U] + [Z_s][Y_f]]^{-1}[Z_s][Y_f][V_i] \tag{3.17}$$

or

$$[V_r] = [T_f][V_i] \tag{3.18}$$

where the voltage reflection coefficient $T_f$ is given by:

$$[T_f] = -[2[U] + [Z_s][Y_f]]^{-1}[Z_f][Y_f] \tag{3.19}$$

### 3.2.3 Modal Mixing

The modal voltage reflection matrix $[\rho_{vm}]$ and modal current reflection matrix $[\rho_{im}]$ can be expressed in terms of the phase reflection matrices as:

$$[\rho_{vm}] = [S]^{-1}[\rho_{vp}][S] \tag{3.20}$$

$$[\rho_{im}] = [Q]^{-1}[\rho_{ip}][Q] \tag{3.21}$$

It can be shown [57] that for single phase faults, all reflected aerial waves at the fault location depend on the total incident wave on the faulted phase. Put another way, ground mode components that arrive at the fault location reflect as both aerial and ground mode and vice versa for aerial mode components arriving at the fault. One of the implications of this is that it is impossible to completely decouple the aerial and ground mode components of a single phase fault because they mix at the fault location.

## 3.3 Simulation of different types of faults

In the following examples an idealised transmission line of 100 km is simulated where a fault has occurred 60 km from the source. To keep the examples simple, the far end of the transmission line is left open circuit and the source is considered ideal. At the open circuit termination of the transmission line fault current traveling waves will be reflected with a coefficient of -1 and at the ideal source they will be reflected with a coefficient of 1. The point of observation where the high frequency current is measured is the source. The high frequency waves are extracted by applying a high pass Butterworth filter with a cut off frequency of 1 kHz to remove the power frequency components and a low pass anti aliasing filter with a cut off frequency of 500 kHz . A sampling frequency of 1.25 MHz is used which is the same as what is used in commercially available traveling wave fault recorders. The simulation is run until steady state conditions have been met before the fault is applied. A one-line diagram of the simulation is shown in Fig. 3.2.

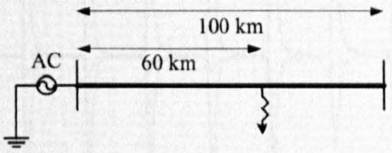


FIGURE 3.2: One-line diagram of simple transmission line

### 3.3.1 Balanced three phase and balanced three phase to ground fault

An example of the traveling wave pattern produced for a three phase fault is shown in Fig. 3.3 which shows the measured phase currents for each phase. During a three phase fault significant traveling waves are produced on each of the phases. The amplitude of the initial traveling waves can be determined by equation (A.28).

Since the transmission line under consideration is an ideally transposed transmission line, the modal components can be calculated using Clark's Transform matrix. The modal components of the phase currents are shown in Fig. 3.4. There is no significant mode 0 or ground mode component because the three phase fault is balanced and the ground mode currents sum to zero.

The waveform is therefore very easy to follow; a traveling wave is setup which periodically travels between the source and the fault location. The amplitude of the wave gradually decreases as a result of the attenuation of the line.

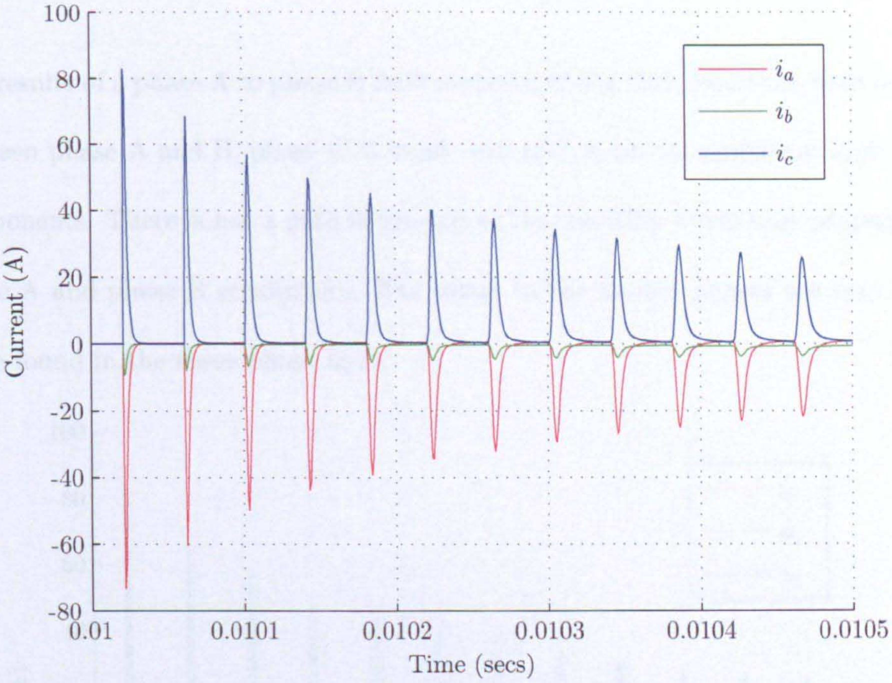


FIGURE 3.3: Phase currents of three phase fault

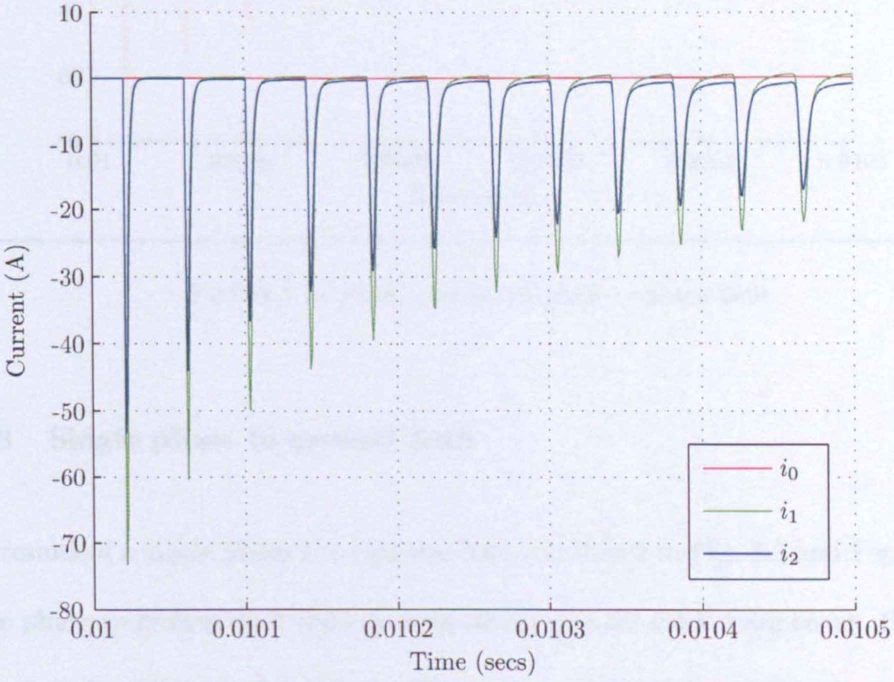


FIGURE 3.4: Modal components of three phase fault

### 3.3.2 Phase to phase fault

The results of a phase A to phase B fault is shown in Fig. 3.5. Since the fault only occurs between phase A and B, phase C is unaffected and shows no significant high frequency components. There is not a path to ground so the traveling waves only propagate in the phase A and phase B conductors. The waves in the faulted phases are very similar to those found in the three phase fault.

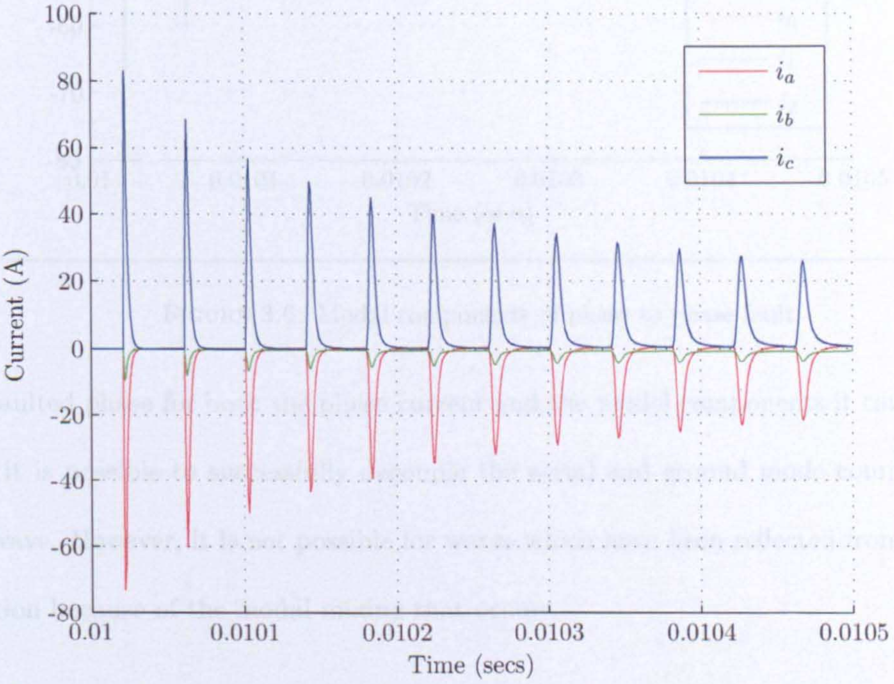


FIGURE 3.5: Phase currents of phase to phase fault

### 3.3.3 Single phase to ground fault

The results of a single phase C to ground fault are shown in Fig. 3.7 and Fig. 3.8. In a single phase to ground fault there is a significant ground mode component. Recall that waves traveling through the ground suffer greater attenuation and distortion as a result of the higher impedance of the ground conductor. Comparing the initial wave front of

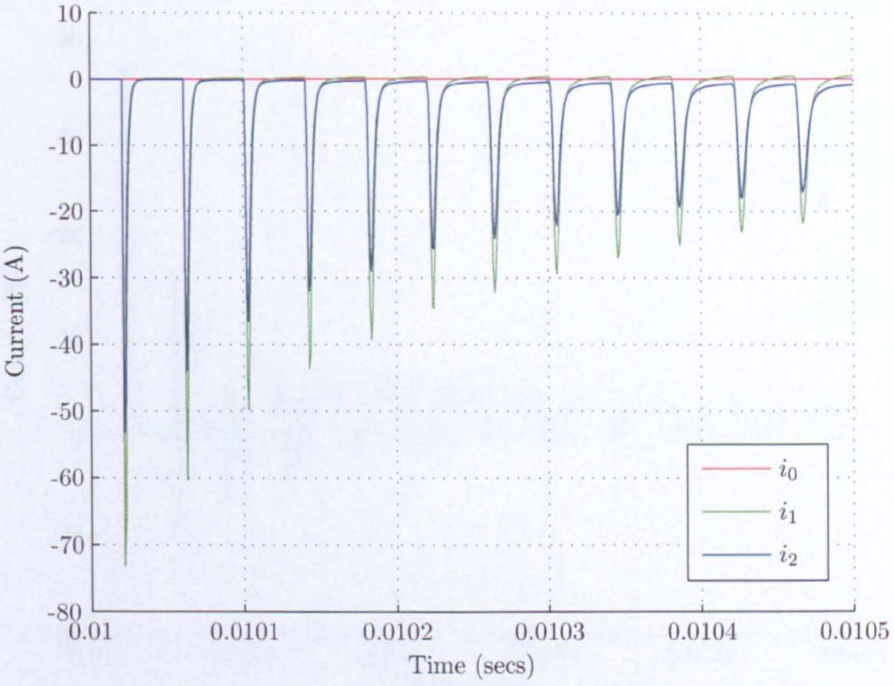


FIGURE 3.6: Modal components of phase to phase fault

the faulted phase for both the phase current and the model components it can bee seen that it is possible to successfully decouple the aerial and ground mode components of the wave. However, it is not possible for waves which have been reflected from the fault location because of the modal mixing that occurs.

## 3.4 summary

In this chapter consideration was given to fault events on a three phase transmission line. Simulation results for different types of fault on and idealised transmission line were presented and it was shown that single phase to ground faults have a significant ground mode component that suffers greater attenuation and distortion than the aerial mode components. Modal mixing should be taken into consideration when ground mode

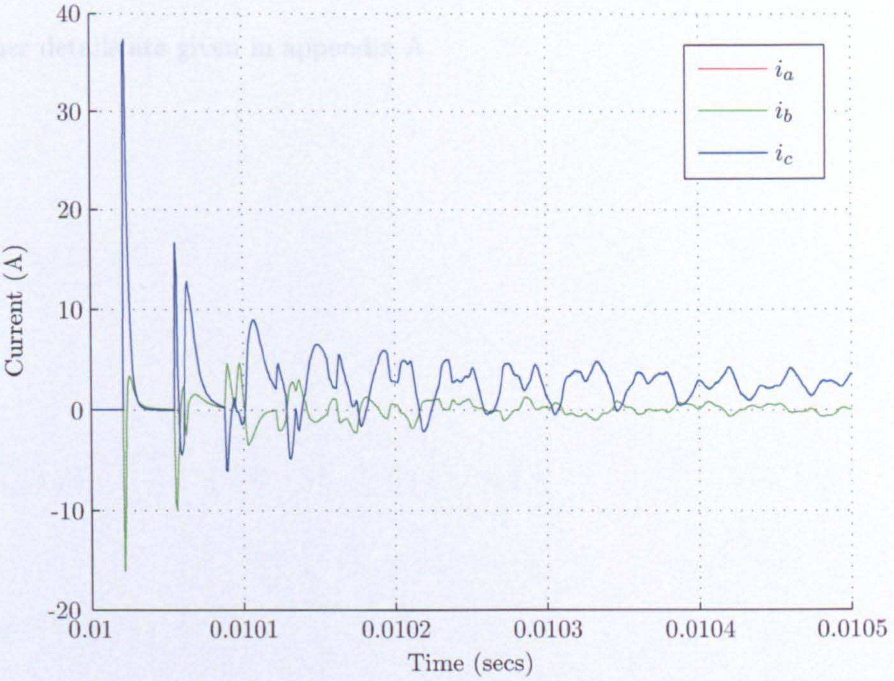


FIGURE 3.7: Phase currents of single phase fault (phase a and phase b are overlayed on each other)

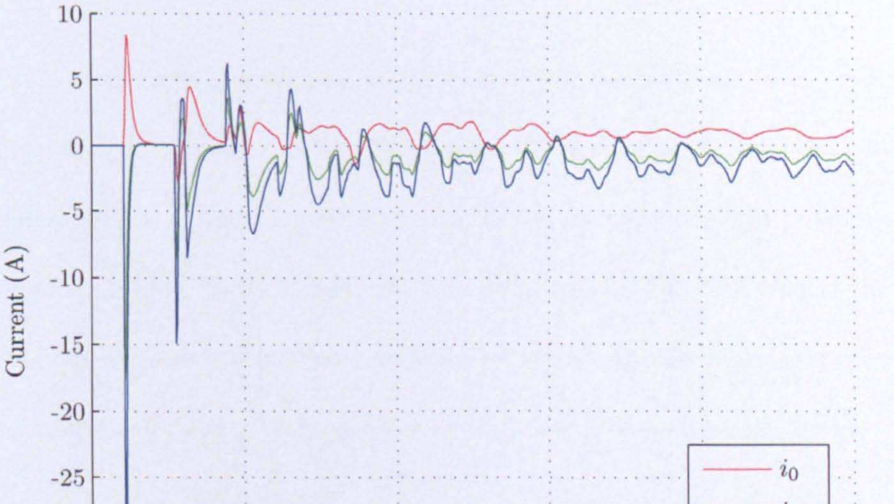


FIGURE 3.8: Modal components of single phase fault

propagation are present because all reflections at the fault location are dependent on it. Further details are given in appendix A.

# Chapter 4

# Time Tree Analysis of Power Networks

## 4.1 Introduction

Time tree analysis is a simulation method based on keeping track of all traveling waves that exist on a network following a disturbance. It uses the principle of the Bewley lattice diagram which is a visual representation of wave propagations and points of reflection in the network [38]. Lattice diagrams can be drawn by hand for simple networks but soon become impractical for more complex network configurations. Time tree analysis uses a computer program to keep track of the wave propagations.

In recent years there has been an increased interest in applying optimisation techniques, such as genetic algorithms, to power systems [12, 55]. Genetic search algorithms are capable of quickly finding the optimal solution to a problem within a multi-dimensional solution space. So far genetic search algorithms have not been applied to traveling wave fault location. This is partly due to the relatively long computation times of traveling wave simulations.

In this chapter time tree analysis is combined with a genetic search algorithm to efficiently identify the most likely location of a fault on a branched distribution line as simulated using the ATP/EMTP simulation software for a variety of fault conditions.

## 4.2 ATP/EMTP simulation software

ATP/EMTP [58] is a popular simulation software used for accurately simulating high frequency transient events. It is capable of modeling the frequency dependent distributed nature of transmission lines and multi modal propagations. Transmission lines can either be modeled as lumped parameter pi sections or as distributed parameter models. The JMARTI [58] distributed parameter transmission line was used in this study to model the transmission line sections which calculates the line parameters based on the geometry of the line and the surrounding medium. It uses a constant modal transform matrix calculated at a frequency representative of traveling waves. The simulation model was created using ATPDraw [59], a graphical preprocessor to the ATP simulation engine. ATPDraw allows the user to create network configurations by dragging and dropping network components together. It then creates the relevant ATP input files for the ATP simulation engine. The output files of the ATP simulation were first processed using the PlotXY program which converts the data into a format suitable for Matlab. All further signal processing was performed in Matlab.

## 4.3 Time Tree Concept

The lattice diagram was first introduced by Bewley as a method of keeping track of surges following a lightning strike on a transmission line [38]. The diagrams soon become too complicated to follow when the number of branches in the network is increased. Time trees are a formal way of representing the waves that propagate on a lattice diagram. Originally time trees were proposed as a method of simulating surge events such as lightning strikes [60, 61]. As computing power increased, time tree techniques were abandoned for more sophisticated methods which took into account such phenomena as modal propagation and the frequency dependent nature of attenuation. In a large number of situations, the results of time tree simulations show a high degree of correlation with the simulation results of more sophisticated simulation packages. This was recognised by [4], who proposed using time trees to locate faults based on traveling wave data on transmission networks and subsequently [9] on distribution lines.

The main advantage of time tree analysis over other simulation methods is the speed at which the simulation can be executed and the ease at which the network can be reconfigured to represent a different fault condition. These two factors have led to the idea of combining time tree analysis with a genetic search algorithm to autonomously seek out the correct fault location.

There are a number of different ways time tree analysis can be implemented [4, 60, 61]. The method used in this work and presented in this chapter is based on [61]. Consider the very simple example network shown in Fig. 4.1 which shows a distribution line with an ideal source, one sub feeder, and open circuit terminations at nodes N2 and N3. A fault has occurred 20m along branch B2.

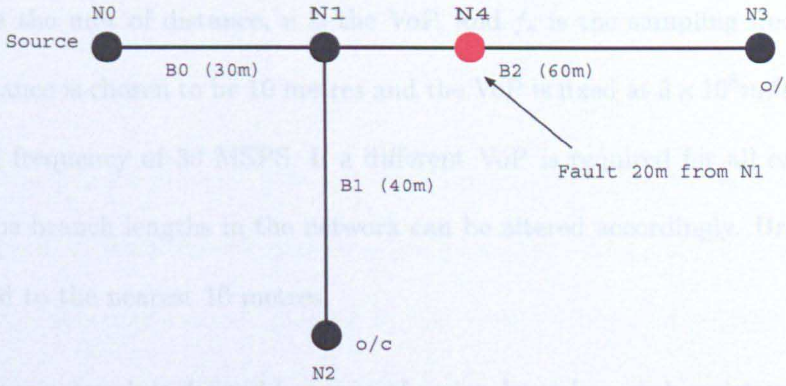


FIGURE 4.1: Diagram of simple distribution line (branch lengths are shown in metres)

It will be assumed that the network represents a single phase distribution line and that the impedances of each section of transmission line are all the same. The fault induces an e.m.f at the fault location, equal and opposite to the pre fault steady state voltage and in series with the fault resistance at the moment the fault occurs. The sudden application of an equivalent e.m.f at the fault location causes traveling waves to propagate away from the fault location. When the propagating transients meet impedance discontinuities at line terminations or junctions, reflected and transmitted waves are created as the transient propagates through them.

To implement this scenario as a computer program, a distance-branch array is created, similar to the one shown in Fig. 4.2. The distance branch array keeps a record of all the traveling waves propagating on the network. Each column of the distance branch array represents one unit of distance. The branch lengths for the example in Fig. 4.1 where chosen to be very short so that it was possible to show a good proportion of the distance-branch array on one page. The unit of distance is related to the sampling frequency of the time tree analysis and the velocity of wave propagation (VoP) as:

$$\delta d = \frac{v}{f_s} \tag{4.1}$$

where $\delta d$ is the unit of distance, $v$ is the VoP, and $f_s$ is the sampling frequency. The unit of distance is chosen to be 10 metres and the VoP is fixed at $3 \times 10^8 m/s$ which gives a sampling frequency of 30 MSPS. If a different VoP is required for all or part of the network, the branch lengths in the network can be altered accordingly. Branch lengths are rounded to the nearest 10 metres.

The time tree network is defined in terms of nodes, branches, stub resistances and node pairs. A node is defined as any point in the network where there is a termination or intersection of transmission line or discontinuity in surge impedance, such as at the fault location. Each node has a node ID and node name associated with it.

A branch is defined as a length of transmission line with no junction or change in surge impedance along its length. Each branch has a branch ID, branch length, impedance and Node IDs associated with it. The node IDs at either end of the branch are referred to as node 1 and node 2.

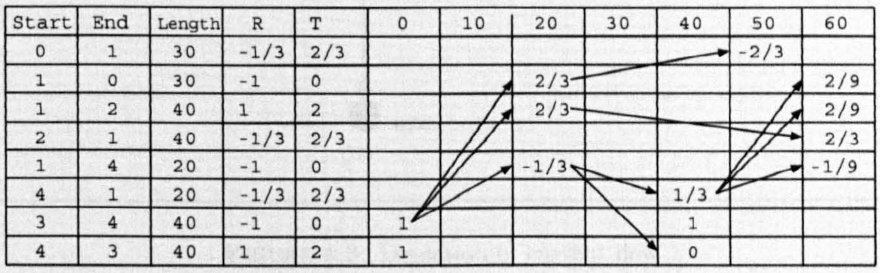
A stub resistance is defined in terms of the node ID where it is located and a resistance. A stub resistance can be added to any node in the network. The stub resistance represents a shunt resistor to ground.

Node pairs are used to describe a particular direction of propagation along a branch. The node pair has associated with it a start node, an end node, a branch length and a reflection coefficient. The start node and end node dictate the direction of propagation and the reflection coefficient determines how a wave is reflected once it has reached the end node. The reflection coefficient for each node pair is calculated based on the other branches or stub resistances connected to the end node.

To represent a fault on the network, the branch containing the fault is effectively split into two branches which are connected via a common node called the fault node. When a fault is imposed on a network the node pair objects are updated to reflect the new network configuration.

For each branch in the network, two rows (node pairs) are added to the distance-branch array representing both directions a wave can propagate. The distance-branch array is initialised by inserting a pulse, created by the fault, in the first column on the rows where the start node is equal to the fault location (i.e. fault node).

Now that the branch array has been initialised, each element in the array can be processed, starting at row 0, column 0. Further action need only be taken if an array element has a non-zero value. Additional pulses are entered into the distance-branch array on the rows which have the same start node as the end node of the current row being evaluated. The column in which the pulse is entered is determined by the current column plus the length of the branch being evaluated. Multiple pulses that are entered into the same array element are added together.



| Start | End | Length | R | T | 0 | 10 | 20 | 30 | 40 | 50 | 60 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 30 | -1/3 | 2/3 | | | | | | -2/3 | |
| 1 | 0 | 30 | -1 | 0 | | | 2/3 | | | | 2/9 |
| 1 | 2 | 40 | 1 | 2 | | | 2/3 | | | | 2/9 |
| 2 | 1 | 40 | -1/3 | 2/3 | | | | | | | 2/3 |
| 1 | 4 | 20 | -1 | 0 | | | -1/3 | | | | -1/9 |
| 4 | 1 | 20 | -1/3 | 2/3 | | | | | 1/3 | | |
| 3 | 4 | 40 | -1 | 0 | 1 | | | | 1 | | |
| 4 | 3 | 40 | 1 | 2 | 1 | | | | 0 | | |

FIGURE 4.2: Distance Branch Array Voltages

The distance-branch array for the example in Fig. 4.1 is shown in Fig. 4.2. The fault node is node 4. The first non-zero values are in column 0 which represent the initial pulse generated by the fault event. The initial pulse travels towards the open circuit termination of branch B2 and towards the junction of branches B0, B1 and B2. The pulse that arrives at the open circuit termination is reflected with a value of +1 while the pulse that arrives at the junction generates a reflected wave with an amplitude of

-1/3 and transmitted waves with an amplitude of 2/3. The reflected waves travel back towards the fault location while the transmitted waves travel towards the source N0 and open circuit termination N2. The process of wave reflection and transmission repeats until all the energy in the wave is dissipated to a negligible level or the total simulation time is achieved

The voltage pulse pattern at a particular observation point can be extracted from the distance branch array by summing together all the pulses at the observation node for each unit of distance. The current pulse pattern can be extracted by summing the pulses entering and leaving the observation point for each unit of distance. The positive direction for current flow is defined as leaving a node as shown in Fig. 4.3.

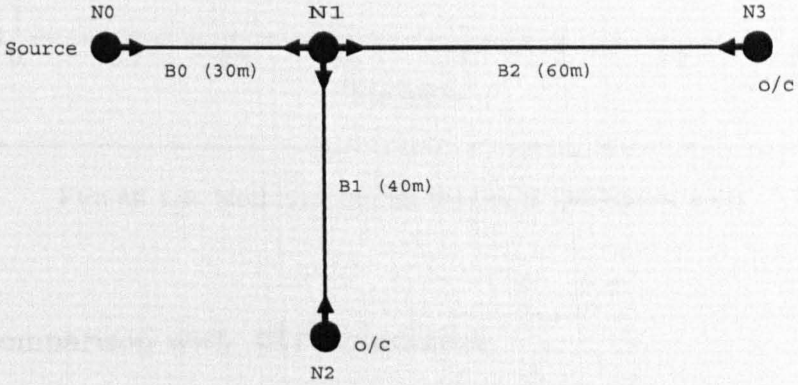


FIGURE 4.3: Depiction of current flow

To extract the voltage pulse pattern only an observation node needs to be specified. However, to extract the current pulse pattern, an observation branch must also be specified because the observation node may have more than one branch connected to it such as node 1 in the previous example. In either case, the resulting pulse pattern is the ideal fault impulse response of the network. The impulses represent the wavefronts or the impulse response to a step voltage change therefore the total voltage or current at the observation point can be obtained by integrating the fault impulse response. The ideal fault current impulse response is shown in Fig. 4.4 and the cumulative integral of the current impulse response at the observation point is shown in Fig. 4.5.

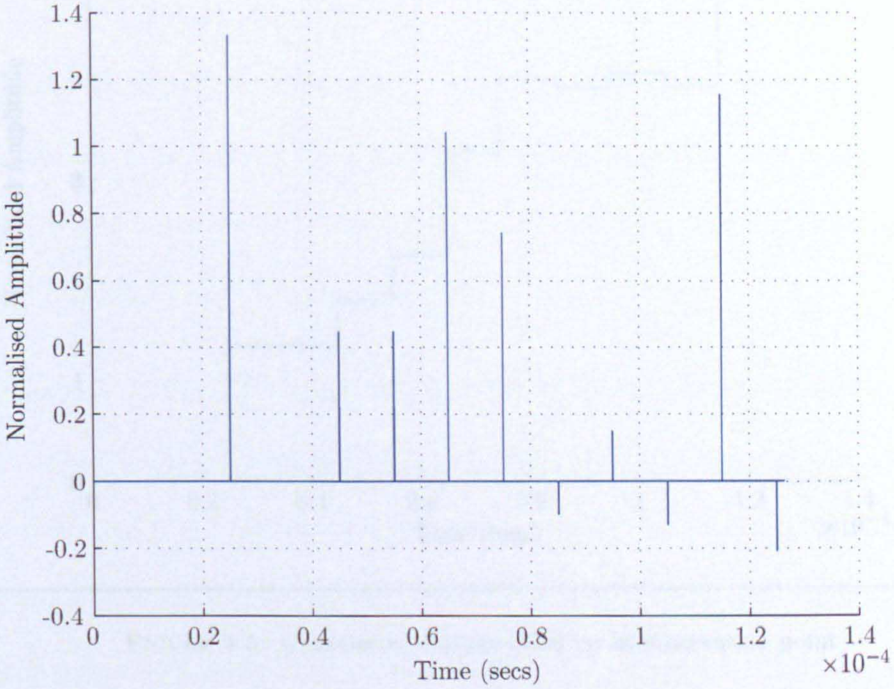


FIGURE 4.4: Ideal fault current impulse at observation point

### 4.3.1 Comparison with ATP simulation

The network in Fig. 4.1 was simulated in ATP using the JMARTI distributed parameter model for the transmission lines. The branch lengths were increased so that B0 was 3 km, B1 was 4 km and B2 was 6km. A sampling frequency of 1 MSPS was used to simulate the network. The current observed at the source was exported to Matlab where it was high pass filtered using a single pole Butterworth filter with a cut off frequency of 100 kHz to extract the traveling wave data from the power frequency. The data could also be low pass filtered or filtered with a more sophisticated filter response to model the transfer function of the transducer used to extract the traveling wave data on a real system. The filtered data was re-sampled at the same sampling frequency as the time

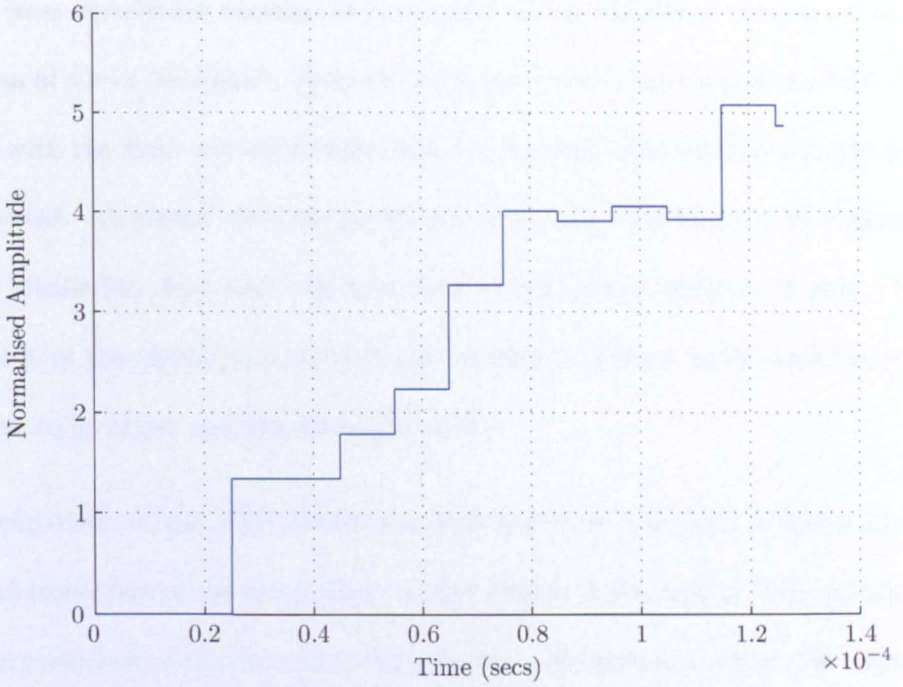


FIGURE 4.5: Cumulative current build up at observation point

tree program (30 MSPS) so that direct correlation could be made between the ATP simulation data and the time tree simulation data.

The time tree response was created by performing a sample and hold on the ideal fault impulse response, to obtain the current at the observation point, and high pass filtered with the same 100 kHz Butterworth filter. The result was then low pass filtered with a cutoff frequency of half the original sampling frequency of the ATP simulation (500 kHz).

To measure the similarity between the two signals a cross correlation was used. Recall from chapter 2 that the cross correlation function of two signals, $x(t)$ and $y(t)$ is defined as:

$$r_{xy}(\tau) = \frac{1}{T_0} \int_0^{T_0} x(t)y(t+\tau)dt \tag{4.2}$$

The cross correlation function is a measure of the similarity between a time lagged version of one of the signals. However, for the purpose of correlating the ATP simulation data with the time tree simulation data, we are only interested in a single correlation coefficient, calculated when the initial pulses in each waveform are in alignment. The ATP simulation data and time tree data is normalised between -1 and +1 and the location of the initial pulse in both sets of data is defined as the location of the first sample to go above and absolute value of 0.2.

A comparison of the ATP simulation data and time tree data is shown in Fig. 4.6. Visual inspection of the waves shows a high degree of correlation. The calculated correlation coefficient of the two sets of data was for a correlation window of 60 microseconds. The main difference between the ATP simulation and the time tree simulation is that the attenuation and phase shift of the traveling waves caused by the transmission line parameters was not taken into consideration in the time tree model. Attenuation and dispersion could be included in the time tree model but would significantly add to the overall computation time. The main objective of the time tree model was to produce an approximation of the traveling wave response which is 'good enough' to allow discrimination of different fault locations with minimum computation. A short computation time means many fault conditions can be evaluated in quick succession making the time tree analysis suitable for use with a genetic search algorithm.

## 4.4 Genetic Search Algorithm

A genetic algorithm is a search technique used to seek out the optimum solution to a problem using the mechanics of natural selection. Each parameter of the solution is encoded as a binary string, in such a way that for each possible solution, a unique

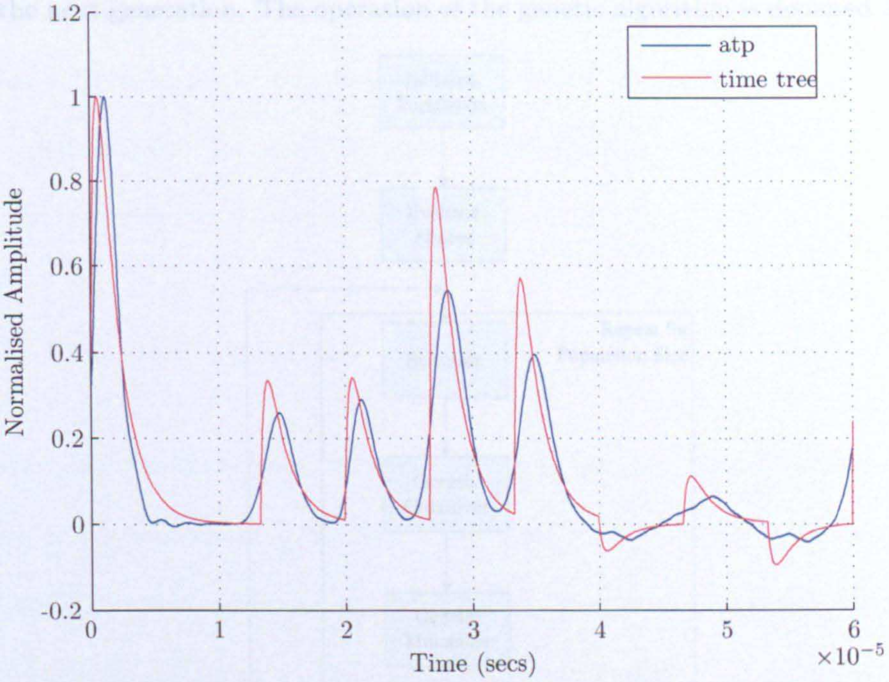


FIGURE 4.6: Comparison of time tree simulation and ATP simulation for a three phase fault

numerical gene exists. An initial population is created, usually at random, of genes representing possible solutions. For each gene, a value of fitness is calculated which is a measure of how well a particular solution satisfies the problem being optimised. The fitness function is chosen such that the fitness values lie in the range 0 - 1, where 1 represents a perfect solution. Genes are selected to form the next generation of population based on their fitness values. Genes with a higher fitness value, on average, tend to survive whilst genes with lower fitness values do not. Genes that are selected for the next generation undergo a process of 'cross-over', which is a method of combining two genes to produce a new gene containing components of both its parents, and a process of mutation which introduces random genetic variation. The selection, cross-over, and mutation of genes continues over a number of generations until the algorithm converges on an optimum solution. A technique which can improve the performance of a genetic algorithm, called elitism, ensures that the best solution from each generation is passed onto the next generation. The operation of the genetic algorithm is depicted in Fig. 4.7

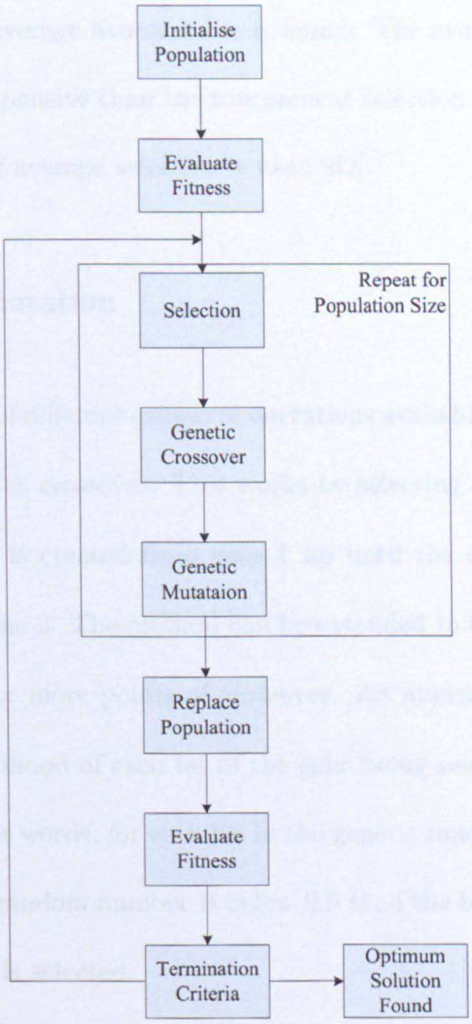


FIGURE 4.7: Diagram depicting operation of genetic algorithm

### 4.4.1 Selection

There are a number of methods that can be used to select genes from the current population. Two popular methods are tournament selection and average selection. In tournament selection, two population members are chosen at random and the one with the highest fitness value is selected. In the average selection method, a population member is chosen at random but is only selected for the next generation if it is above the average fitness value for the population. If it is below the average fitness of the population then another member is chosen at random. The process continues until a member with an above average fitness value is found. The average selection method is more computationally expensive than the tournament selection method but populations tend to converge faster if average selection is used [62].

### 4.4.2 Crossover Operation

There are also a number of different crossover operations available. The simplest crossover method is called one-point crossover. This works by selecting one point in the gene at random. The new gene is created from gene 1 up until the crossover point at which point it is made up of gene 2. The method can be extended to the multi-point crossover method which has two or more points of crossover. An alternative method is uniform crossover where the likelihood of each bit of the gene being selected for the new gene is equally as likely. In other words, for each bit in the gene, a random number is generated between 0 and 1. If the random number is below 0.5 then the bit from gene 1 is selected else the bit from gene 2 is selected.

### 4.4.3 Mutation

The mutation operator introduces random genetic variation into members of the population. It is implemented by randomly changing bits in a gene from 0 to 1 or vice versa. This introduces new genetic material which was not necessarily in the original initial population allowing more of the solution space to be explored. Mutation has a negative effect on the ability of a population to converge and therefore should only occur at a relatively low probability of the order of between 1 - 10 % [62].

### 4.4.4 Application to Traveling Waves

To apply genetic search techniques to traveling wave fault location, the fault location and fault resistance must be encoded in the gene used for the genetic algorithm. The fault location is encoded using the faulted branch ID and the distance from node 1 of the faulted branch to the fault location. The fault reflection coefficient is encoded, instead of the fault resistance, so that the genetic algorithm covers all possible short circuit fault resistances regardless of transmission line impedance. The fault resistance for a specific transmission line impedance can be calculated from the fault reflection coefficient using equation (A.30). The structure of the gene looks like:

$$\text{Gene} = [\text{Fault Branch ID}][\text{Fault Distance}][\text{Fault Reflection Coefficient}]$$

The number of bits used to represent the fault reflection coefficient determines the resolution to which the fault resistance can be predicted. The same is true for the fault distance but the resolution is also limited by the effective sampling frequency of the time tree program.

A genetic algorithm is linked to the specific problem being optimsed by the fitness function. In this case the fitness function is the cross correlation of the ATP simulation result and the time tree simulation results as described in section 4.3.1. The correlation coefficient has a range between -1 and 1 where 1 represents a perfect positive correlation, -1 represents a perfect negative correlation and 0 represents no correlation at all. The genetic algorithm requires the fitness value to lie in the range 0 - 1 so the absolute value of the correlation coefficient is used for the fitness value. When the time tree simulation fault impulse response is produced for the correct fault condition there will be a maximum correlation with the ATP simulation impulse response.

Two correlation lengths were investigated. The first was a variable length correlation window, set to twice the distance from the observation point to the fault location (enough to include the wave reflected from the fault location) and the second, was a fixed length correlation window, set to twice the maximum possible fault distance from the observation point. In other words, twice the distance to the furthest point on the network from the observation point. It was found that both schemes gave a global maximum corresponding to the fault location but, the variable length correlation window, introduced many more local maxima at other locations in the solution space. The fixed correlation length window was chosen for the genetic algorithm because there was less likelihood of the genetic algorithm mistaking a local maxima as the optimum solution.

### 4.4.5 Choice of parameters

There are a number of parameters and methods that must be chosen for a genetic algorithm including population size, mutation factor, gene selection method and gene cross-over method. There are no set rules for choosing these parameters and in many cases there is a trade off between computation time and performance. The parameter which has the most influence on the performance of the genetic algorithm is the choice of population size. If the population size is too small then it could converge on a local maximum as opposed to the global maximum. If the population size is too large then the computation time will become excessive. Larger population sizes take more generations to converge, further increasing the computation time.

## 4.5 CELESC distribution line

To evaluate the algorithm a relatively simple distribution system was chosen. Network schematics for a simple distribution line were made available by the CELESC power company. CELESC operate all the distribution networks in the Santa Catarina region of Brazil. A one-line diagram of the distribution line is shown in Fig. 4.8. Detail of the branch lengths are given in Table 4.1. The distribution line runs along a beach providing power for residential customers and a few small businesses. The length of the distribution line is relatively short, especially the lengths of some of the sub-feeders. However, the topology of the network, is similar to what would be found for a large number of rural distribution lines. Tests were successfully performed using long sub feeders but the results are not shown here. The ability to perform accurate single-ended fault location on rural distribution lines can significantly reduce the amount of time and money spent dispatching repair crews in what can be difficult terrain to access. Rural distribution lines often only serve a few customers so it is hard to justify the financial investment of a multi-ended fault location scheme that would require a communication channel. Radial network topologies are particularly vulnerable to disruption from permanent faults because there is no alternative route from which power can be supplied. A fault close to the start of the distribution line results in the majority of customers being left without power until the fault is located and repaired.

Four fault locations are marked in Fig. 4.8 which are used to evaluate the performance of the time tree analysis and genetic search algorithm. The fault locations were chosen to test close up (fault 1) and far end faults (fault 4) as well as faults on sub feeders (fault 2) and faults near the middle of the distribution line (fault 3). Faults 2 and 3 were chosen to be close together in distance from the observation point to see how easy it was for

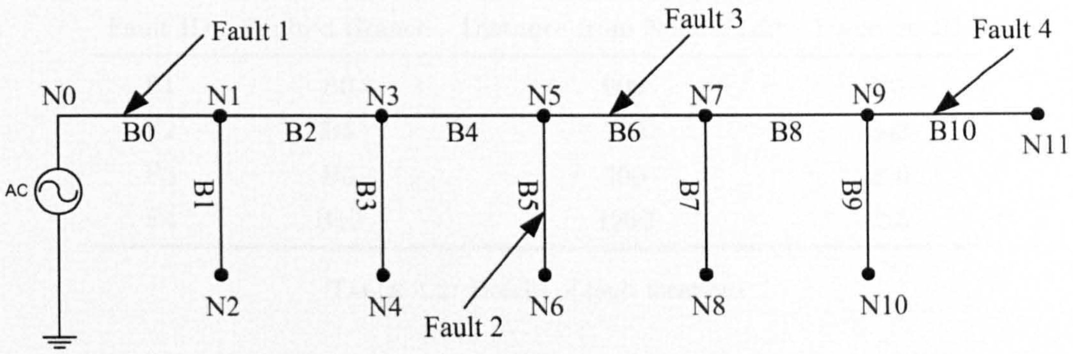


FIGURE 4.8: One line diagram of rural CELESEC distribution line

the genetic algorithm to differentiate between them. Details about the location of the faults along the branches are given in Table 4.2. The branch lengths in the time tree simulation are rounded to the closet 10 metres because this is the distance resolution of the time tree program.

| Branch ID | Actual Length (m) | Time Tree Length (m) | Node 1 | Node 2 |
|---|---|---|---|---|
| B0 | 1335 | 1340 | 0 | 1 |
| B1 | 197 | 200 | 1 | 2 |
| B2 | 743 | 740 | 1 | 3 |
| B3 | 617 | 620 | 3 | 4 |
| B4 | 487 | 490 | 3 | 5 |
| B5 | 172 | 170 | 5 | 6 |
| B6 | 643 | 640 | 5 | 7 |
| B7 | 63 | 60 | 7 | 8 |
| B8 | 589 | 590 | 7 | 9 |
| B9 | 295 | 300 | 9 | 10 |
| b10 | 2345 | 2350 | 9 | 11 |

TABLE 4.1: Details of branch lengths

For each of the fault locations, three phase to ground, inter phase and single phase faults were simulated. Simulations were performed for 0, 100, 500 and 1000 ohm fault resistances. The effect of a fault inception angle close to zero is a well known limitation to traveling wave fault location because the fault transient signals generated are very

| Fault ID | Faulted Branch | Distance from Node 1 (m) | Location ID |
|---|---|---|---|
| F1 | B0 | 800 | 80 |
| F2 | B5 | 100 | 343 |
| F3 | B6 | 200 | 370 |
| F4 | B10 | 1200 | 625 |

TABLE 4.2: Details of fault locations

small and difficult to detect. An alternative approach would be necessary for identifying near zero inception angle faults. However, for the time tree scheme to be a viable fault location scheme, reasonable coverage of fault inception angles must be provided and it must be able to cope with fault inception angles that are less than half the angle that produces the maximum fault transient. A fault inception angle of 30 degrees was chosen for each fault condition.

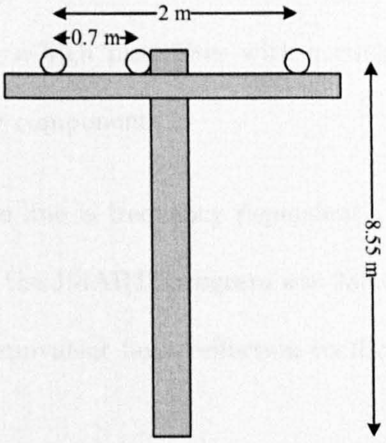


FIGURE 4.9: Tower configuration for CELESC distribution lines

Fig. 4.9 shows the tower configuration for the distribution line. The parameters for the tower configuration were input into ATP and the JMARTI program was used to generate the line parameters. Field measurements made in Brazil found that the earth resistivity was approximately 100 ohm metres. The time tree simulation has an effective sampling frequency of 30 MSPS. Therefore a simulation time step of $2 \times 10^{-7} secs$ was chosen for the ATP simulation which is equivalent to a sampling frequency of 60 MSPS to ensure that the performance of the genetic algorithm was not limited by the resolution of the ATP simulation.

The correlation method used to compare the ATP and time tree simulation data was the same as that described in section 4.3.1. The time tree program produces only one traveling wave response, so for each fault condition, one of the faulted phases is chosen for comparison with the time tree simulation.

The ATP simulation results were first low-pass filtered, to prevent aliasing, and then re-sampled at the same sampling frequency as the time tree simulation. The low-pass filter has a cut-off frequency of 10 MHz which is typical of next generation Rogowski coils which can measure the current directly on the high voltage side. The traveling waves were extracted using a high pass filter with a cut-off frequency of 100 kHz to remove the power frequency components.

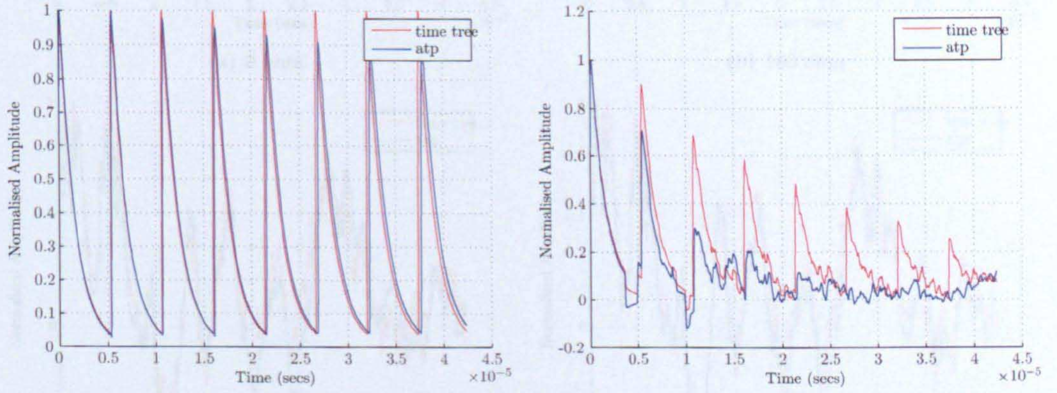
The surge impedance of the line is frequency dependent. The transmission line surge impedance as calculated by the JMARTI program was 933 ohms at 500 kHz. This value was used to calculate the equivalent fault reflection coefficient values which are shown in Table 4.3.

| Fault Resistance | Fault Reflection Coefficient |
|---|---|
| 0 | -1 |
| 100 | -0.82 |
| 500 | -0.48 |
| 1000 | -0.32 |

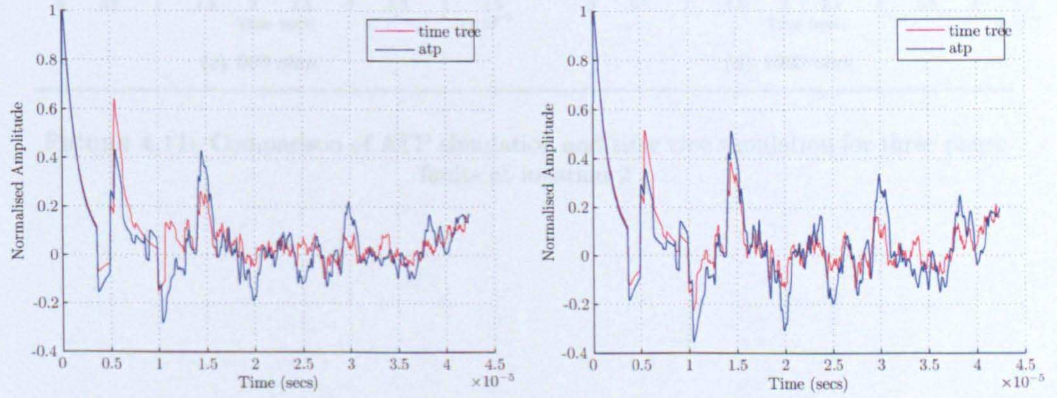
TABLE 4.3: Fault reflection coefficients

### 4.5.1 Three phase faults

Three phase faults are the simplest faults to analyse because all waves travel as aerial mode components. Ground mode components are generated on each phase but, because the fault is balanced, they cancel each other out. For the same reason no modal mixing occurs at the fault location. Any one of the three phases can be chosen for comparison with the time tree prediction. Fig. 4.10 shows both the ATP simulation results and time tree simulation results for a three phase fault at location 1 for all fault resistances. Similarly, Fig. 4.11 shows the results for location 2, Fig. 4.12 shows the results for location 3, and Fig. 4.13 shows the results for location 4. A summary of the correlation coefficients is given in Table 4.4.

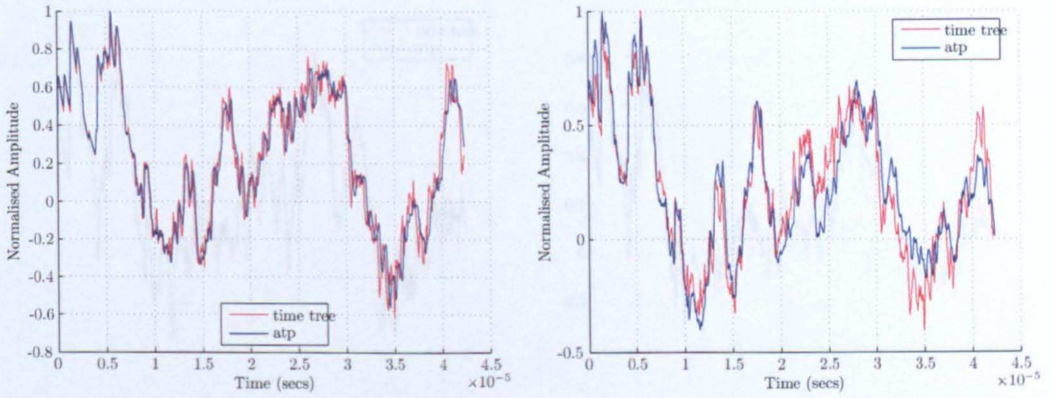


(a) 0 ohm (b) 100 ohm



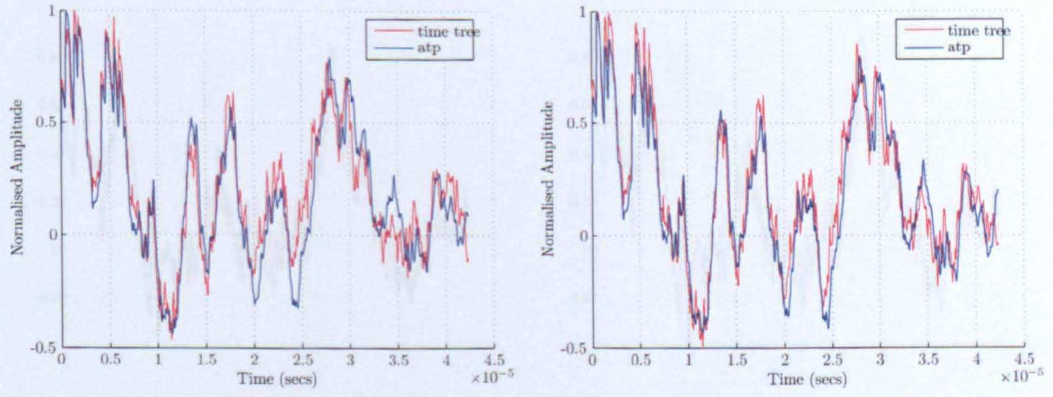
(c) 500 ohm (d) 1000 ohm

FIGURE 4.10: Comparison of ATP simulation and time tree simulation for three phase faults at location 1



(a) 0 ohm

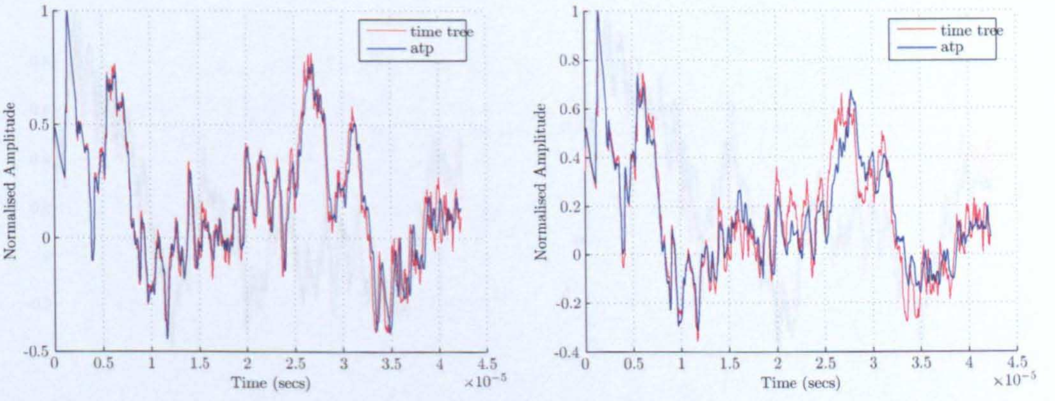
(b) 100 ohm



(c) 500 ohm

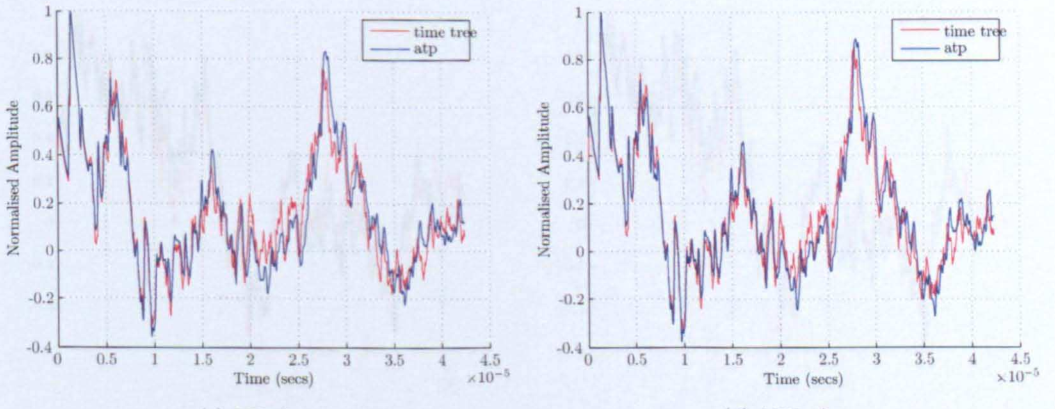
(d) 1000 ohm

FIGURE 4.11: Comparison of ATP simulation and time tree simulation for three phase faults at location 2



(a) 0 ohm

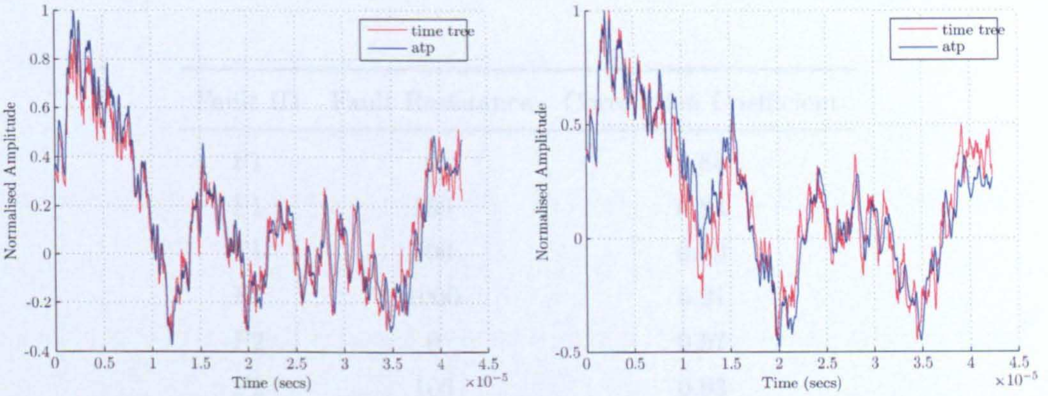
(b) 100 ohm



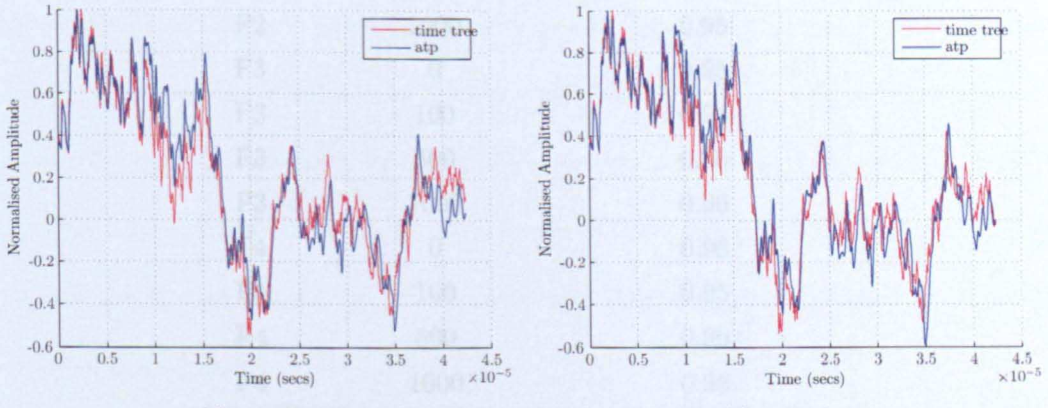
(c) 500 ohm

(d) 1000 ohm

FIGURE 4.12: Comparison of ATP simulation and time tree simulation for three phase faults at location 3



(a) 0 ohm (b) 100 ohm



(c) 500 ohm (d) 1000 ohm

FIGURE 4.13: Comparison of ATP simulation and time tree simulation for three phase faults at location 4

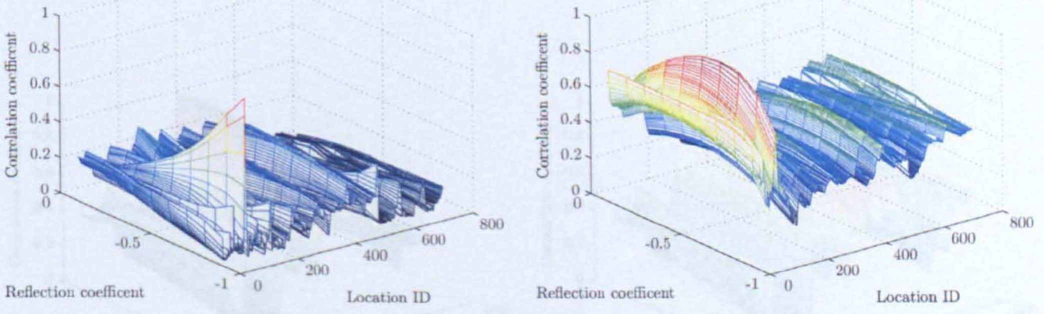
| Fault ID | Fault Resistance | Correlation Coefficient |
|---|---|---|
| F1 | 0 | 0.83 |
| F1 | 100 | 0.84 |
| F1 | 500 | 0.89 |
| F1 | 1000 | 0.91 |
| F2 | 0 | 0.97 |
| F2 | 100 | 0.93 |
| F2 | 500 | 0.93 |
| F2 | 1000 | 0.95 |
| F3 | 0 | 0.95 |
| F3 | 100 | 0.94 |
| F3 | 500 | 0.95 |
| F3 | 1000 | 0.96 |
| F4 | 0 | 0.96 |
| F4 | 100 | 0.95 |
| F4 | 500 | 0.96 |
| F4 | 1000 | 0.96 |

TABLE 4.4: Correlation coefficients for 3 phase faults

Visual inspection of all the graphs show a high degree of correlation between the ATP simulation and time tree simulation. The difference between the ATP simulation and time tree simulation becomes greater the further away the fault is from the observation point because line attenuation and dispersion are not modeled in the time tree simulation. This does not severely impact on the correlation coefficient with the majority of cases having a correlation coefficient above 0.90. The solution space for each of the fault locations and fault resistances is shown in Fig. 4.14, Fig. 4.15, Fig. 4.16 and Fig. 4.17. The graphs depict the correlation of the ATP fault transient with every possible fault scenario predicted using time tree analysis. Each location on the network was given a unique ID so that it was possible to plot the whole solution space on one graph. The relationship between each branch in the network and the location ID is shown in Table 4.5 and the specific location ID for each of the four faults is shown in Table 4.2. The y axis shows the ID of each location on the network. The x axis represents the reflection coefficient at the fault location which has a range from 0 to -1. The z axis is the absolute value of the correlation coefficient of the fault traveling wave pattern produced in ATP with the time tree prediction at that particular fault condition. The absolute value of the correlation coefficient is the fitness value used for the genetic algorithm and has the range between 0 and 1.

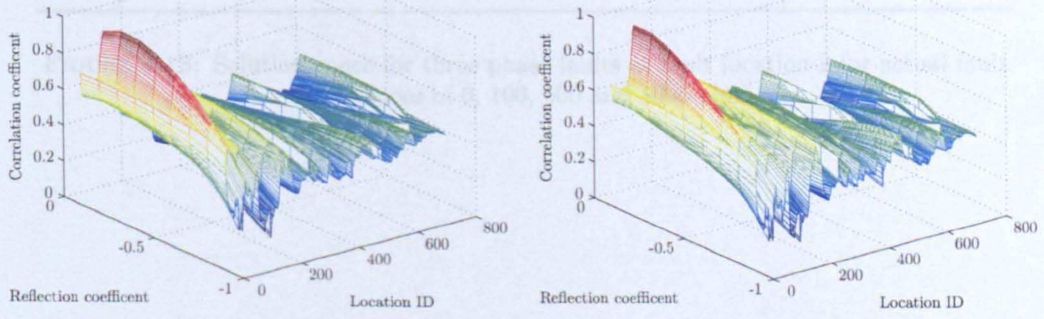
| Branch | Location ID range |
|---|---|
| B0 | 0 - 132 |
| B1 | 133 - 151 |
| B2 | 152 - 224 |
| B3 | 225 - 285 |
| B4 | 286 - 333 |
| B5 | 334 - 350 |
| B6 | 351 - 413 |
| B7 | 414 - 418 |
| B8 | 419 - 476 |
| B9 | 477 - 505 |
| B10 | 506 - 739 |

TABLE 4.5: Location ID for each branch in CELESC network



(a) 0 ohm

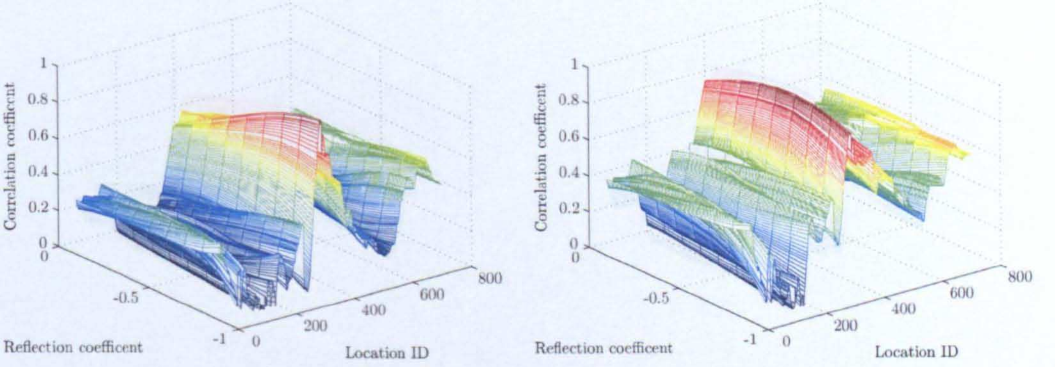
(b) 100 ohm



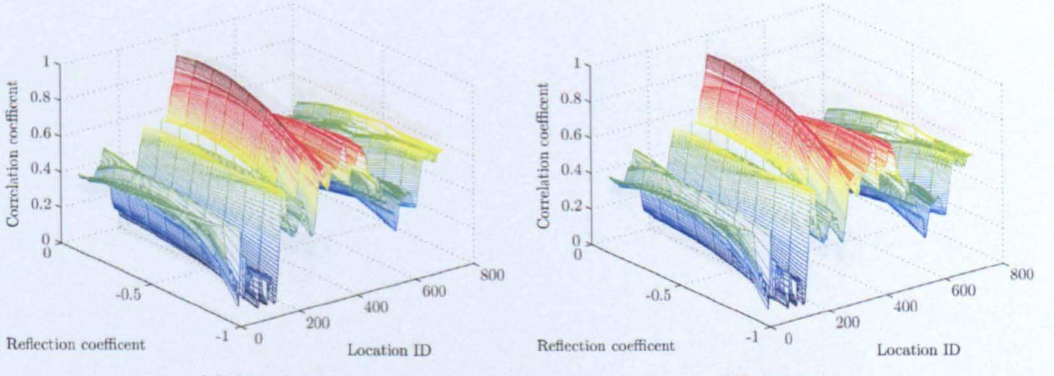
(c) 500 ohm

(d) 1000 ohm

FIGURE 4.14: Solution space for three phase faults at fault location 1 for actual fault resistances of 0, 100, 500 and 1000 ohm

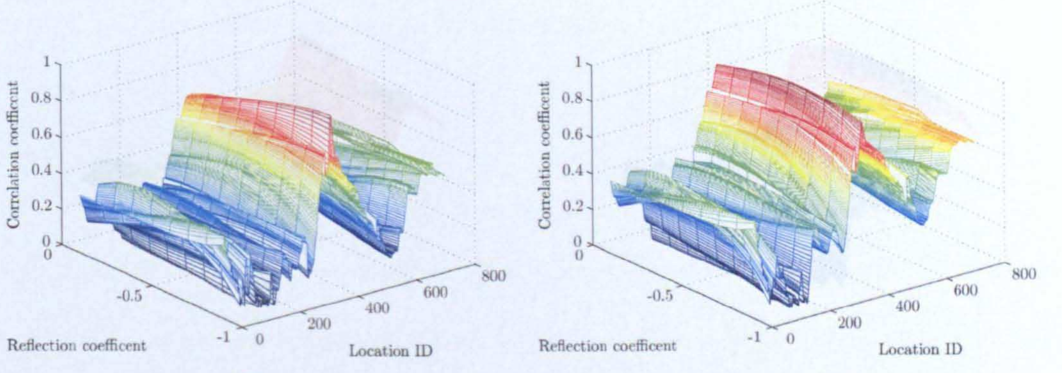


(a) 0 ohm (b) 100 ohm

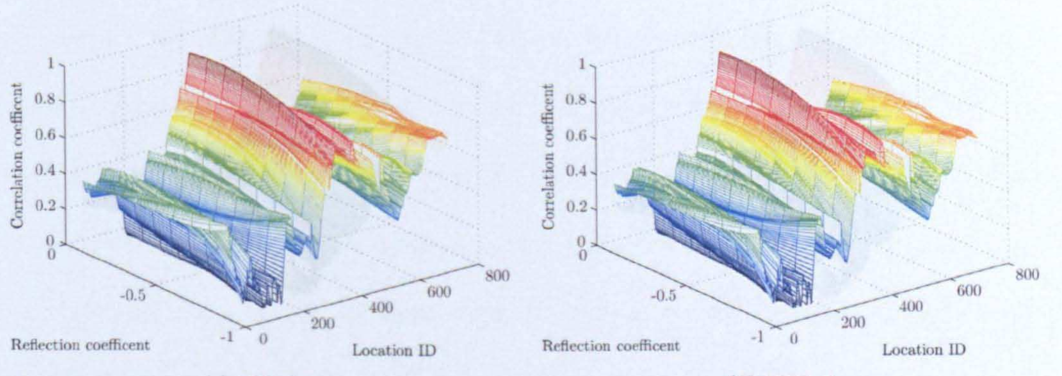


(c) 500 ohm (d) 1000 ohm

FIGURE 4.15: Solution space for three phase faults at fault location 2 for actual fault resistances of 0, 100, 500 and 1000 ohm

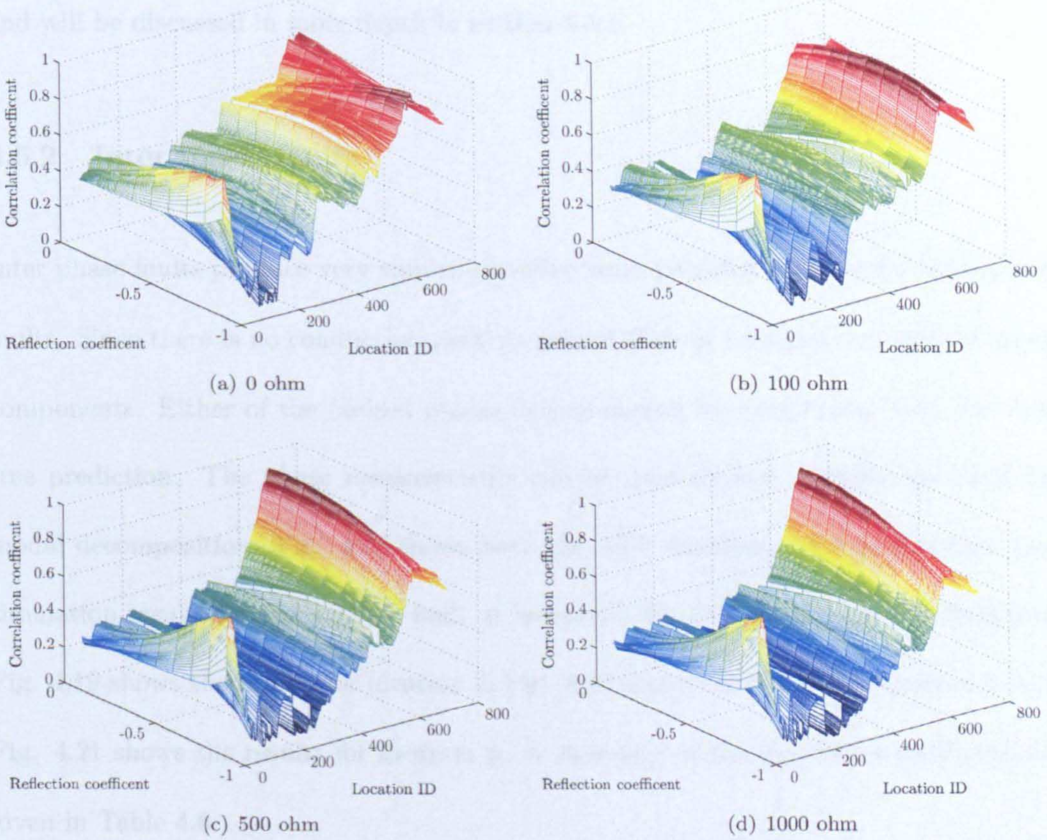


(a) 0 ohm (b) 100 ohm



(c) 500 ohm (d) 1000 ohm

FIGURE 4.16: Solution space for three phase faults at fault location 3 for actual fault resistances of 0, 100, 500 and 1000 ohm



(a) 0 ohm

(b) 100 ohm

(c) 500 ohm

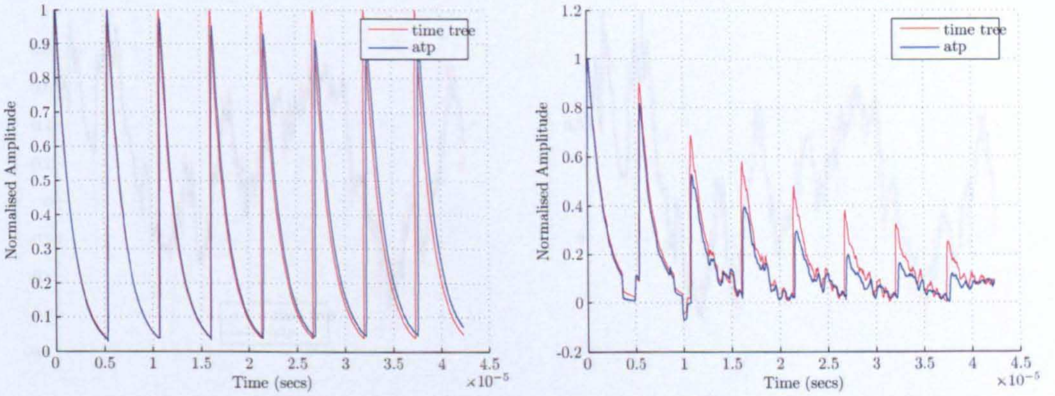
(d) 1000 ohm

FIGURE 4.17: Solution space for three phase faults at fault location 4 for actual fault resistances of 0, 100, 500 and 1000 ohm

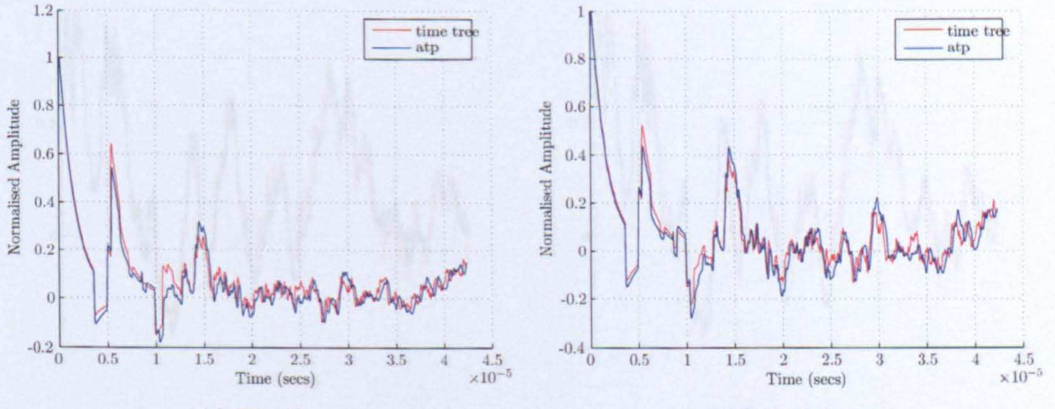
For each of the four fault locations, the maximum ridge in the solution corresponds to the correct location ID. Faults that occur at location 1 result in a ridge which is very sharp with fault locations either side of the ridge having comparatively low correlation values. For all other fault conditions, the ridge in the solution space corresponding to the correct fault location has a more gradual roll off. The sharp ridge characteristic of faults at location 1 can have implications on the performance of the genetic algorithm and will be discussed in more depth in section 4.5.4.

### 4.5.2 Inter phase faults

Inter phase faults produce very similar traveling wave patterns to balanced three phase faults. Since there is no conduction path to ground there is no significant ground mode components. Either of the faulted phases can be chosen for comparison with the time tree prediction. The phase measurements can be used directly without the need for modal decomposition. Fig. 4.18 shows both the ATP simulation results and time tree simulation results for three phase fault at location 1 for all fault resistances. Similarly, Fig. 4.19 shows the results for location 2, Fig. 4.20 shows the results for location 3, and Fig. 4.21 shows the results for location 4. A summary of the correlation coefficients is given in Table 4.6.

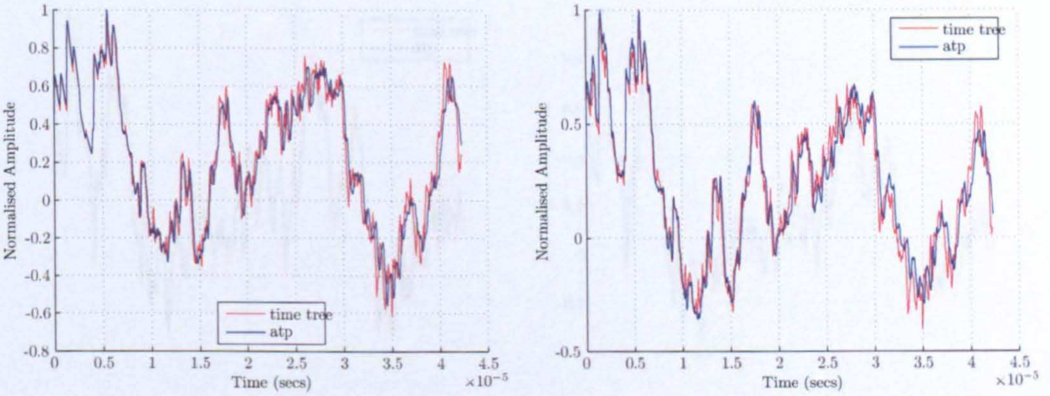


(a) 0 ohm (b) 100 ohm

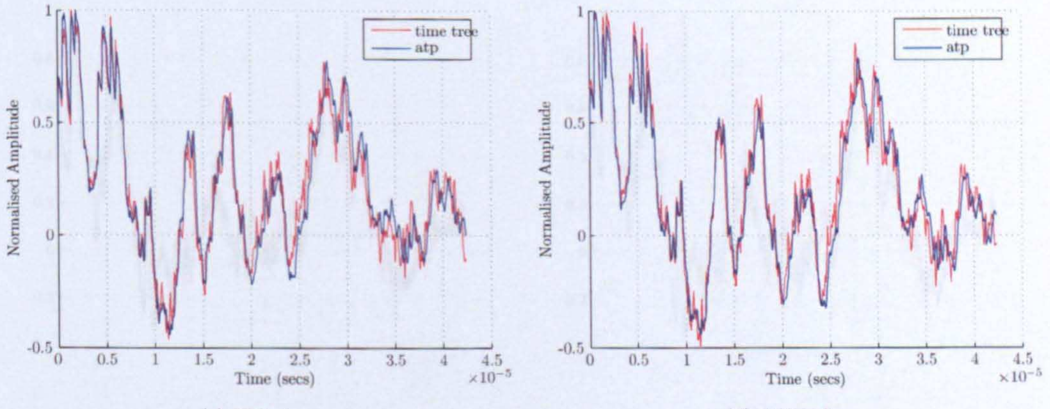


(c) 500 ohm (d) 1000 ohm

FIGURE 4.18: Comparison of ATP simulation and time tree simulation for inter phase faults at location 1

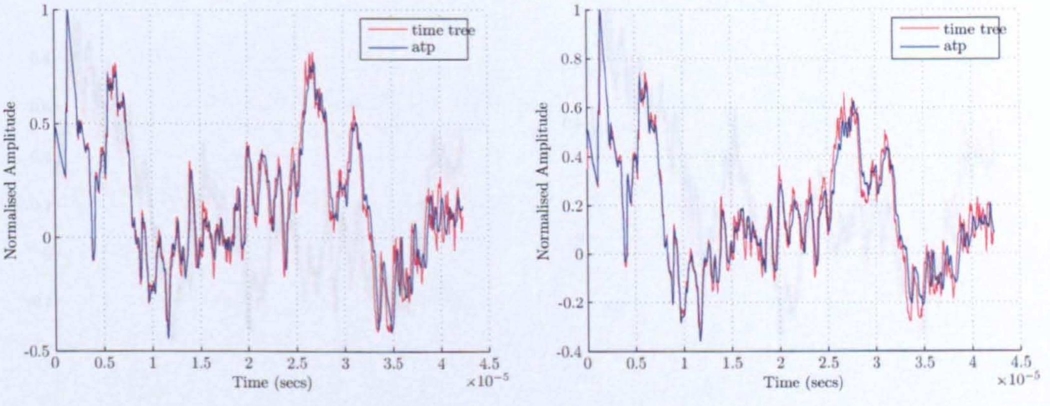


(a) 0 ohm (b) 100 ohm



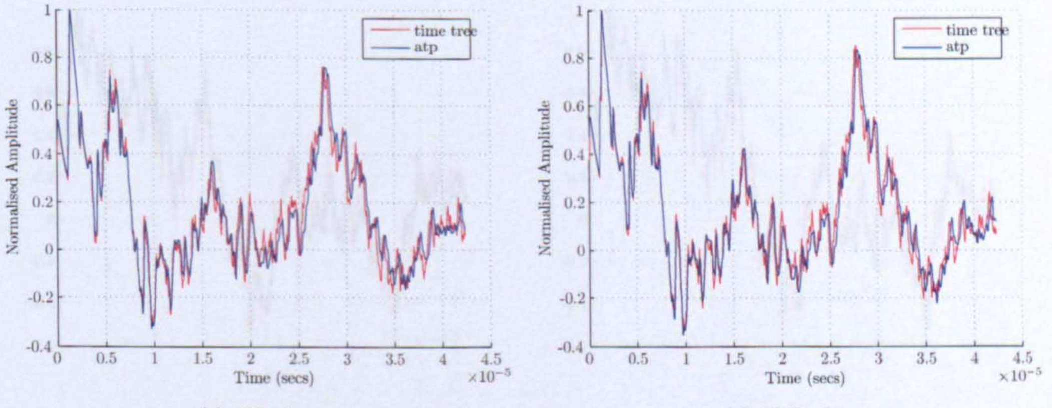
(c) 500 ohm (d) 1000 ohm

FIGURE 4.19: Comparison of ATP simulation and time tree simulation for inter phase faults at location 2



(a) 0 ohm

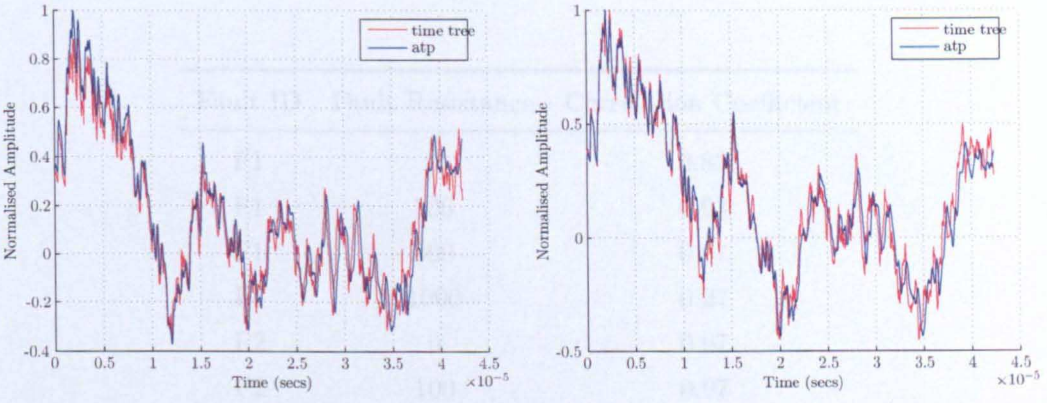
(b) 100 ohm



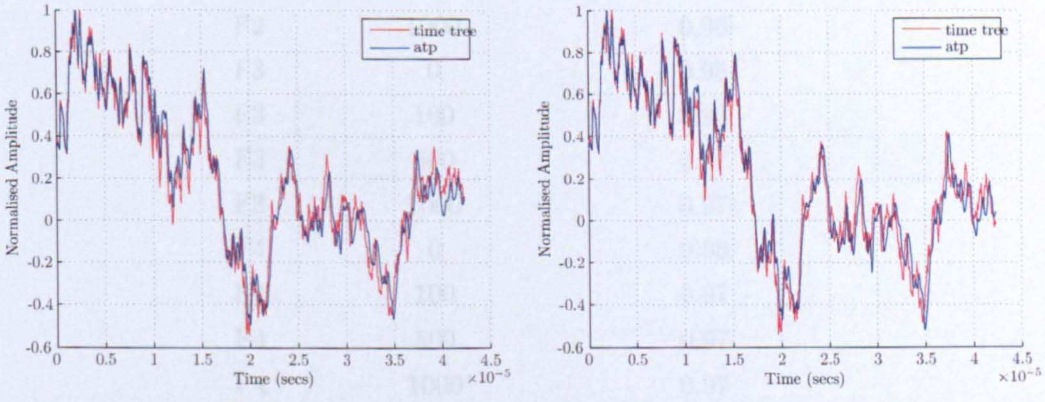
(c) 500 ohm

(d) 1000 ohm

FIGURE 4.20: Comparison of ATP simulation and time tree simulation for inter phase faults at location 3



(a) 0 ohm (b) 100 ohm



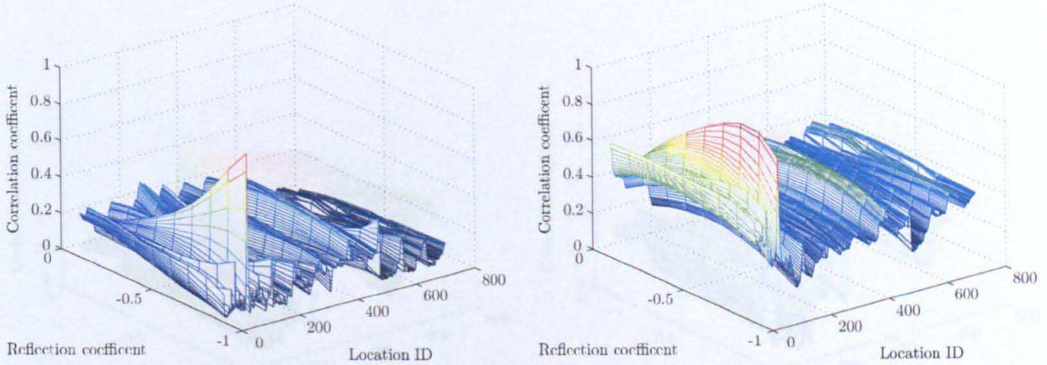
(c) 500 ohm (d) 1000 ohm

FIGURE 4.21: Comparison of ATP simulation and time tree simulation for inter phase faults at location 3

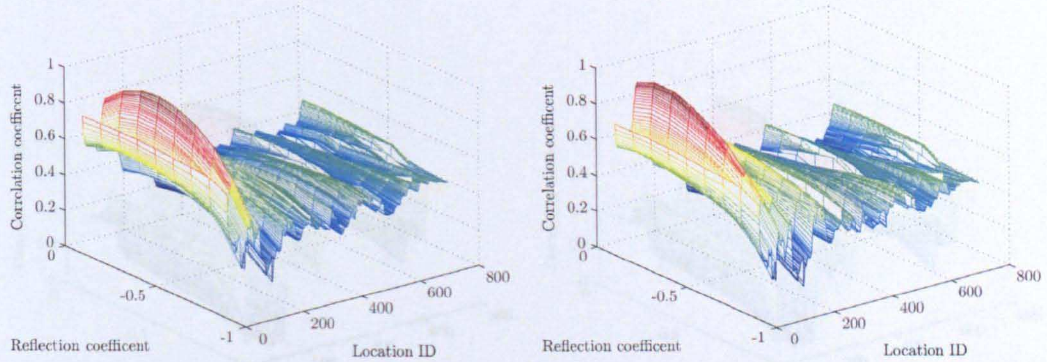
| Fault ID | Fault Resistance | Correlation Coefficient |
|---|---|---|
| F1 | 0 | 0.83 |
| F1 | 100 | 0.93 |
| F1 | 500 | 0.97 |
| F1 | 1000 | 0.97 |
| F2 | 0 | 0.97 |
| F2 | 100 | 0.97 |
| F2 | 500 | 0.96 |
| F2 | 1000 | 0.96 |
| F3 | 0 | 0.95 |
| F3 | 100 | 0.96 |
| F3 | 500 | 0.97 |
| F3 | 1000 | 0.97 |
| F4 | 0 | 0.96 |
| F4 | 100 | 0.97 |
| F4 | 500 | 0.97 |
| F4 | 1000 | 0.97 |

TABLE 4.6: Correlation coefficients for inter phase faults

Visual inspection of all the graphs show almost identical performance as with the three phase case. The differences between the ATP simulation and the time tree simulation can be accounted for by the line attenuation as explained for three phase faults. The solution space for each of the fault conditions is shown in Fig. 4.22, Fig. 4.23, Fig. 4.24 and Fig. 4.25.

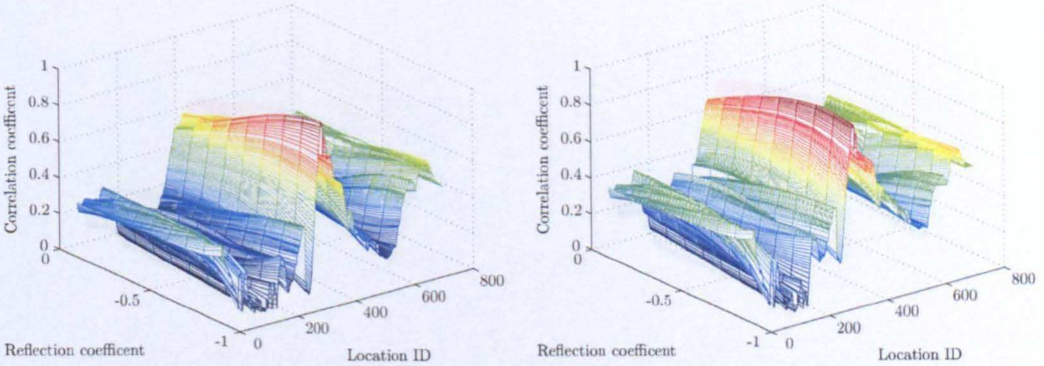


(a) 0 ohm (b) 100 ohm



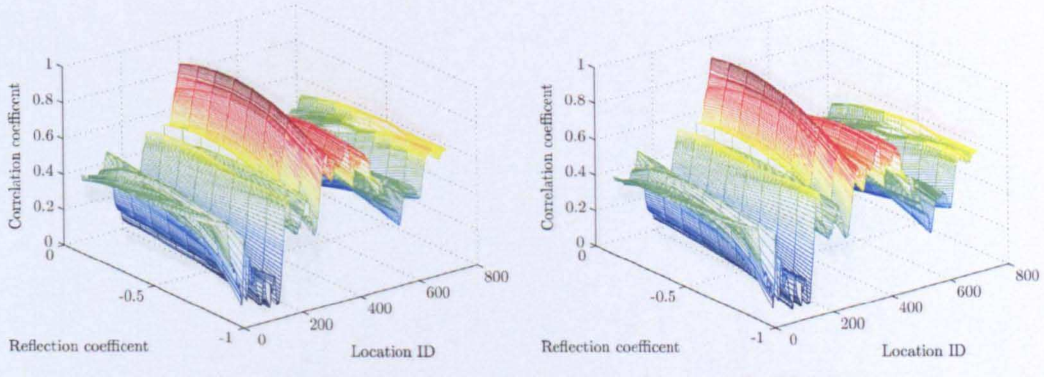
(c) 500 ohm (d) 1000 ohm

FIGURE 4.22: Solution space for inter phase faults at fault location 1 for actual fault resistances of 0, 100, 500 and 1000 ohm



(a) 0 ohm

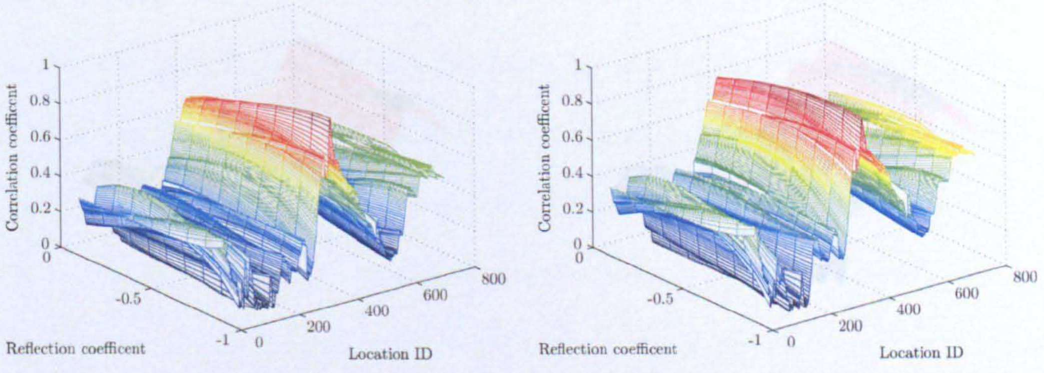
(b) 100 ohm



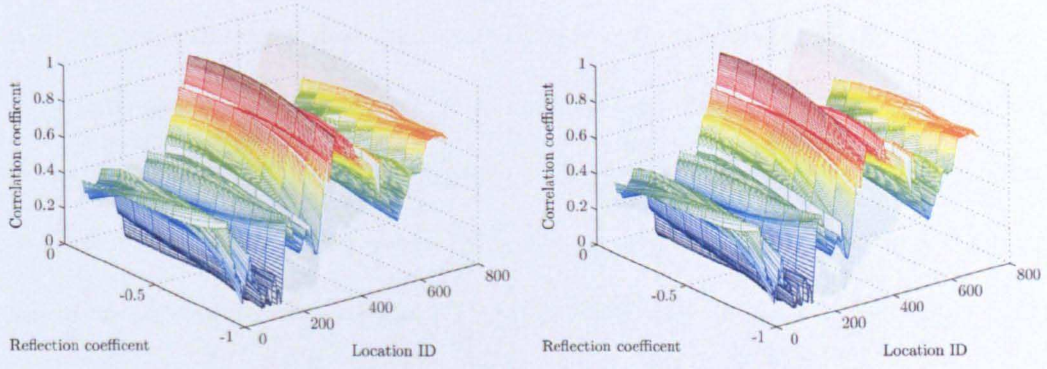
(c) 500 ohm

(d) 1000 ohm

FIGURE 4.23: Solution space for inter phase faults at fault location 2 for actual fault resistances of 0, 100, 500 and 1000 ohm

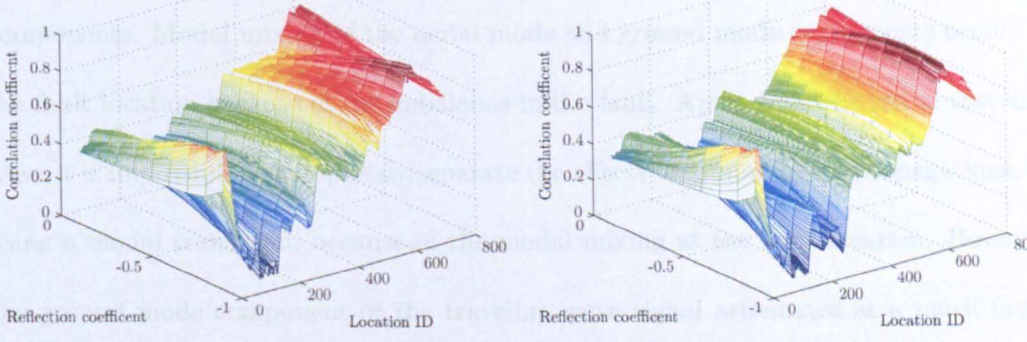


(a) 0 ohm (b) 100 ohm

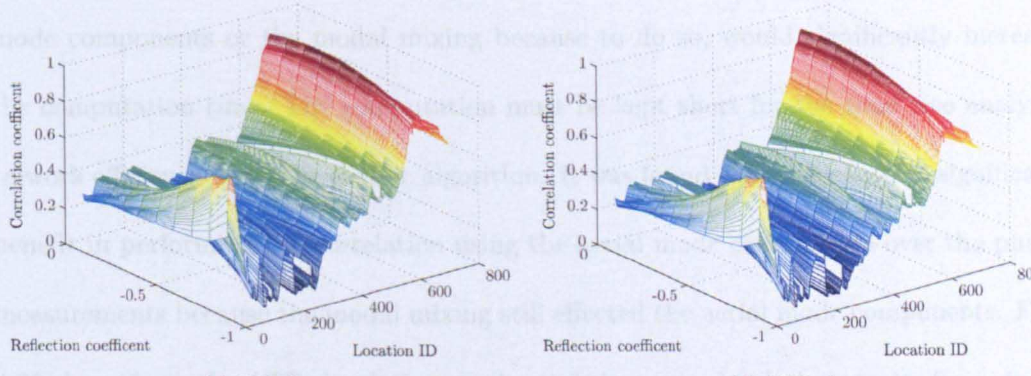


(c) 500 ohm (d) 1000 ohm

FIGURE 4.24: Solution space for inter phase faults at fault location 3 for actual fault resistances of 0, 100, 500 and 1000 ohm



(a) 0 ohm (b) 100 ohm



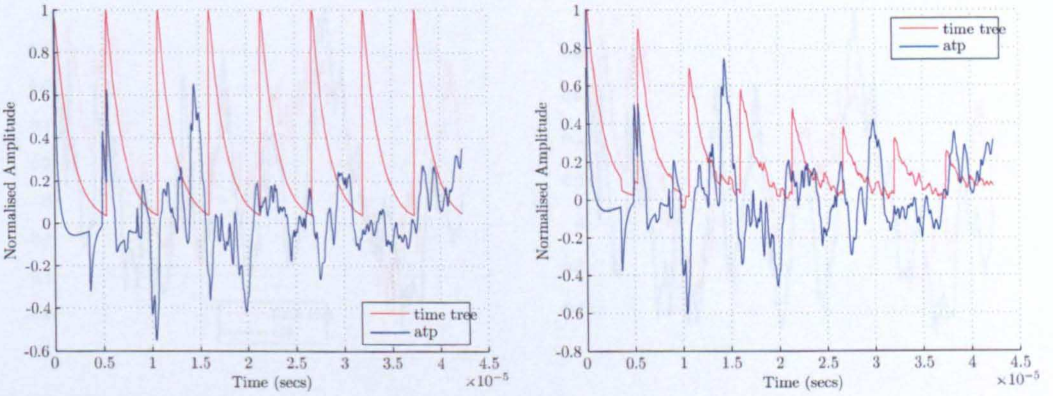
(c) 500 ohm (d) 1000 ohm

FIGURE 4.25: Solution space for inter phase faults at fault location 4 for actual fault resistances of 0, 100, 500 and 1000 ohm

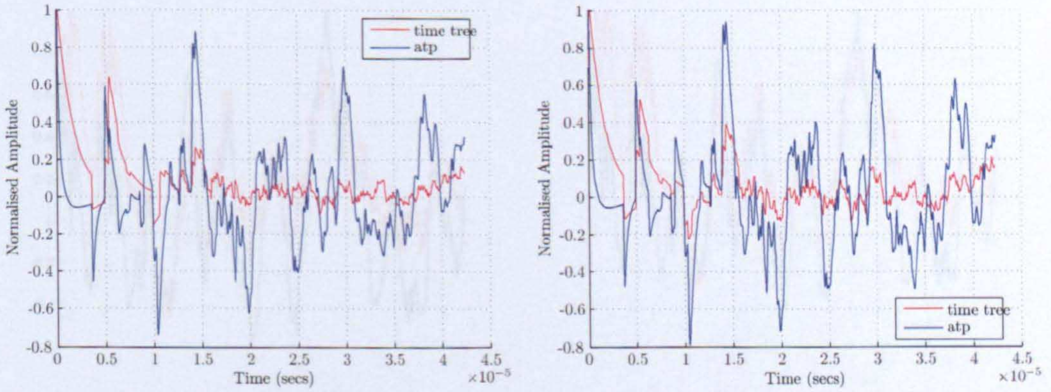
The solution spaces are almost identical to the three phase fault case, as would be expected, and the same conclusions can be drawn.

### 4.5.3 Single phase faults

The analysis of single phase faults is more complex than the analysis of balanced faults and inter phase faults because the traveling wave fault signature contains ground mode components. Modal mixing of the aerial mode and ground mode components occurs at the fault location because of the imbalance in the fault. Apart from the initial traveling wave it is impossible to completely separate the effects of ground mode propagations, by using a modal transform, because of the modal mixing at the fault location. However, the ground mode component of the traveling wave signal attenuates at a much faster rate than the aerial mode component. The time tree program does not model the ground mode components or the modal mixing because to do so, would significantly increase the computation time. The computation must be kept short for the time tree analysis to work efficiently with the genetic algorithm. It was found that there was no significant benefit in performing the correlation using the aerial mode components over the phase measurements because the modal mixing still effected the aerial mode components. Fig. 4.26 shows both the ATP simulation results and time tree simulation results for a single phase fault at location 1 for all fault resistances. Similarly, Fig. 4.27 shows the results for location 2, Fig. 4.28 shows the results for location 3, and Fig. 4.29 shows the results for location 4. A summary of the correlation coefficients is given in Table 4.7.

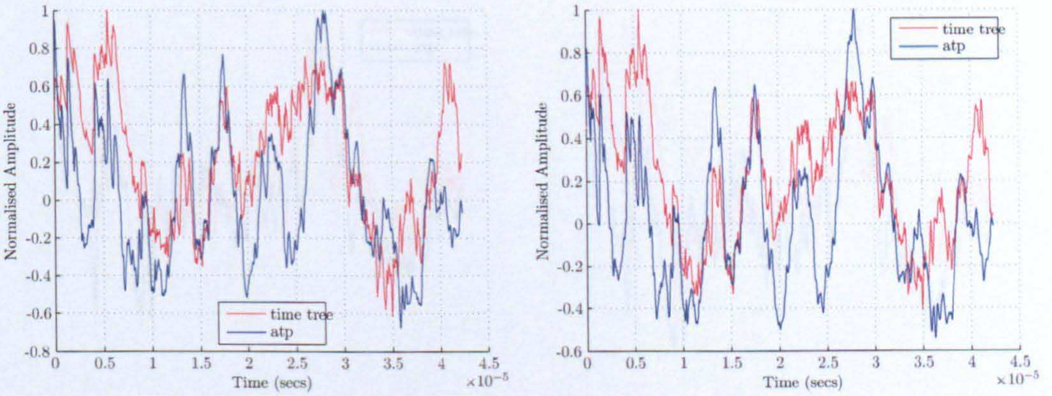


(a) 0 ohm (b) 100 ohm

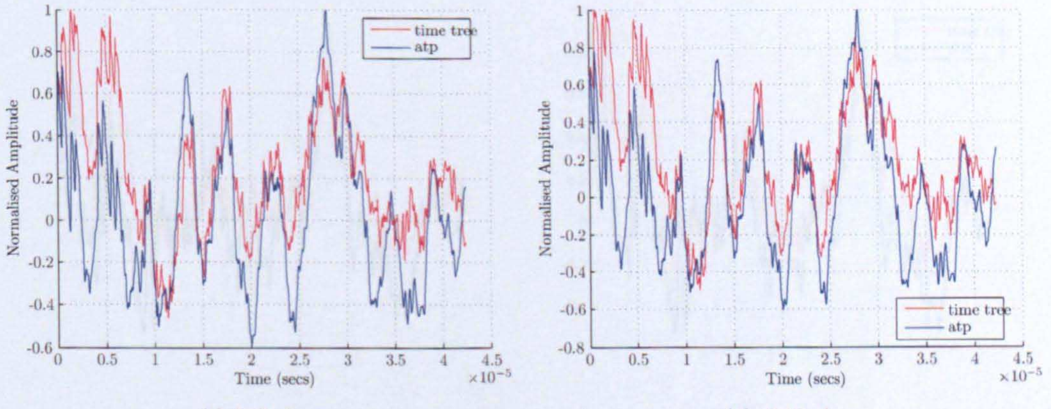


(c) 500 ohm (d) 1000 ohm

FIGURE 4.26: Comparison of ATP simulation and time tree simulation for single phase faults at location 1

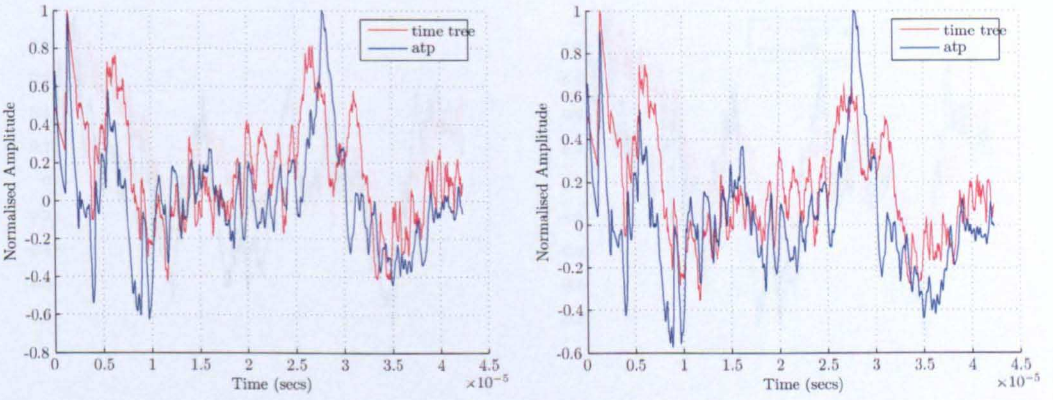


(a) 0 ohm (b) 100 ohm



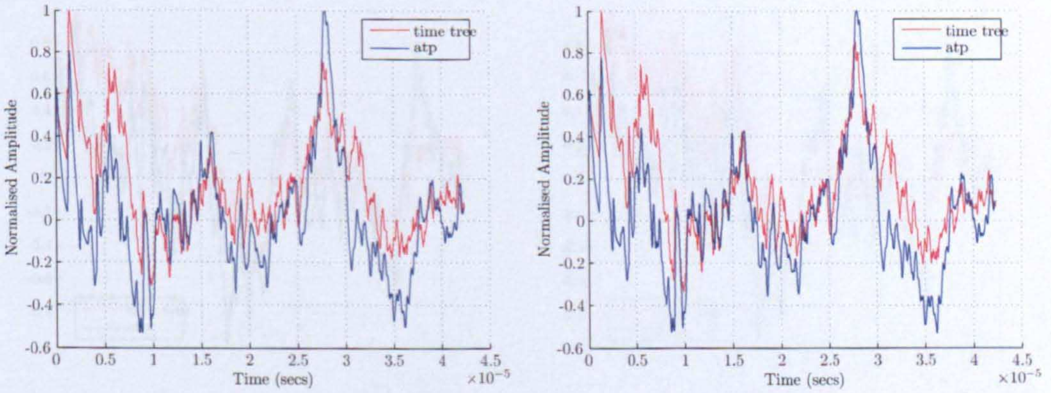
(c) 500 ohm (d) 1000 ohm

FIGURE 4.27: Comparison of ATP simulation and time tree simulation for single phase faults at location 2



(a) 0 ohm

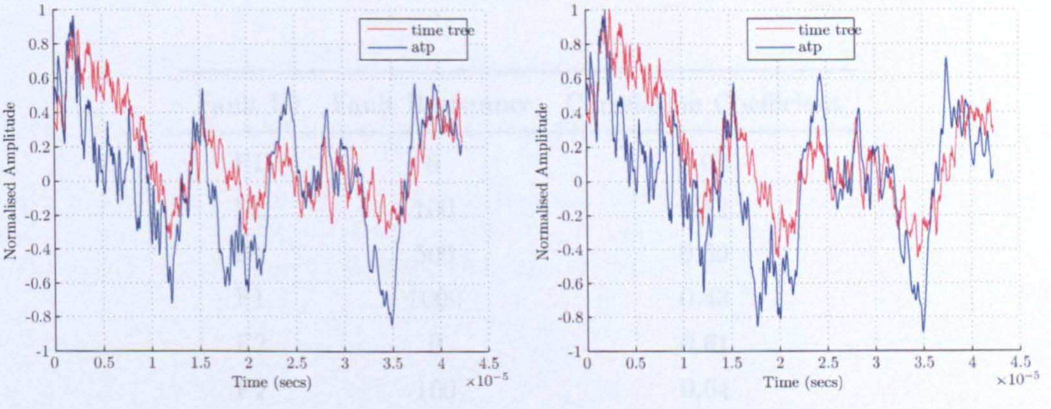
(b) 100 ohm



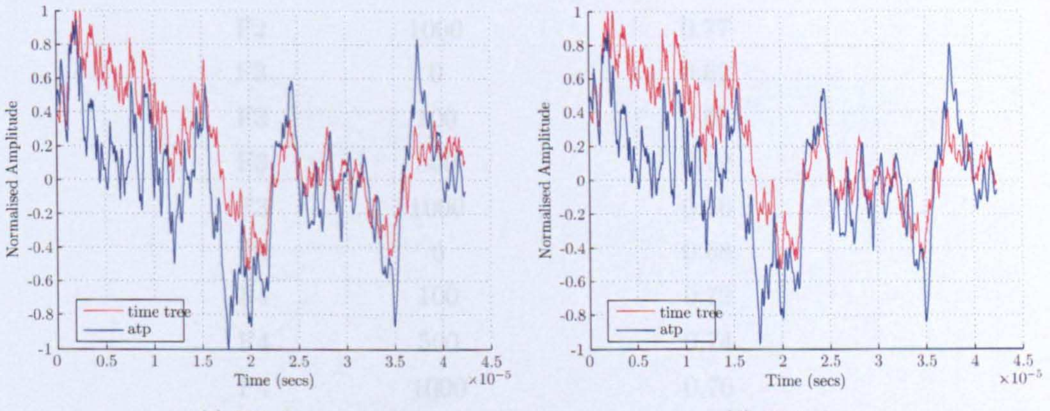
(c) 500 ohm

(d) 1000 ohm

FIGURE 4.28: Comparison of ATP simulation and time tree simulation for single phase faults at location 3



(a) 0 ohm (b) 100 ohm



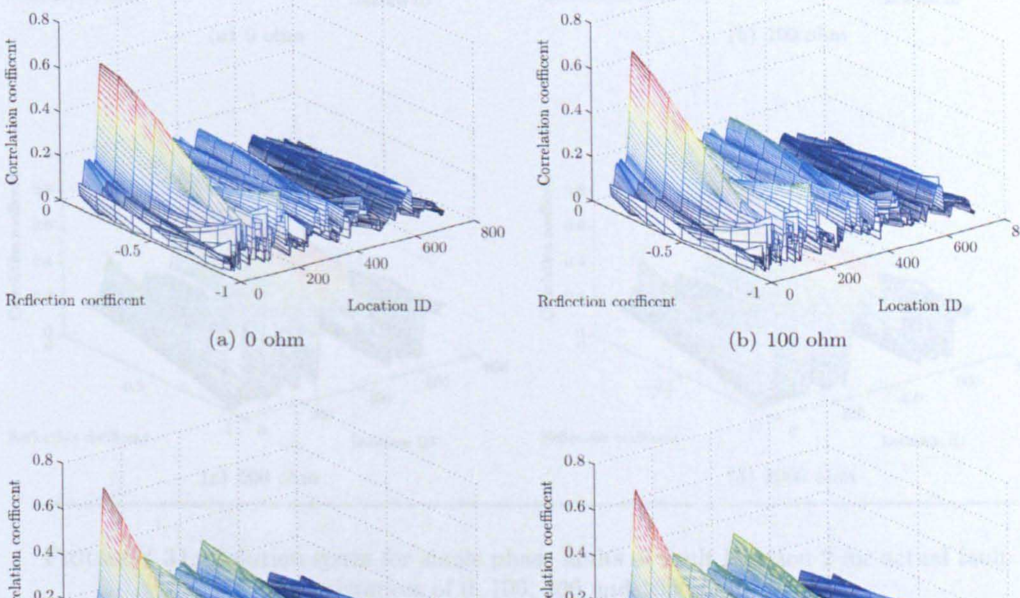
(c) 500 ohm (d) 1000 ohm

FIGURE 4.29: Comparison of ATP simulation and time tree simulation for single phase faults at location 3

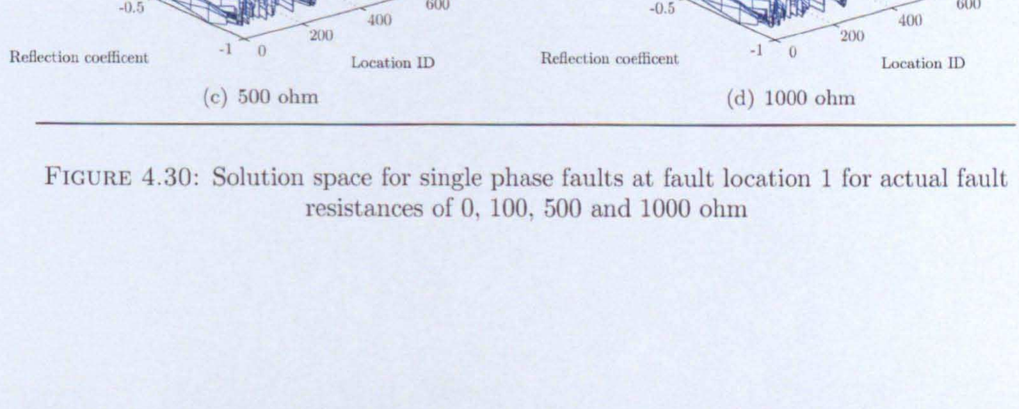
| Fault ID | Fault Resistance | Correlation Coefficient |
|---|---|---|
| F1 | 0 | 0.08 |
| F1 | 100 | 0.12 |
| F1 | 500 | 0.30 |
| F1 | 1000 | 0.43 |
| F2 | 0 | 0.61 |
| F2 | 100 | 0.64 |
| F2 | 500 | 0.73 |
| F2 | 1000 | 0.77 |
| F3 | 0 | 0.62 |
| F3 | 100 | 0.65 |
| F3 | 500 | 0.72 |
| F3 | 1000 | 0.76 |
| F4 | 0 | 0.68 |
| F4 | 100 | 0.72 |
| F4 | 500 | 0.74 |
| F4 | 1000 | 0.76 |

TABLE 4.7: Correlation coefficients for single phase faults

Visual inspection of the waves reveals more differences when compared with the 3 phase or inter phase case especially for close up faults. The situation becomes clearer when the whole solution space is considered. The solution space for each of the fault conditions is shown in Fig. 4.30, Fig. 4.31, Fig. 4.32 and Fig. 4.33. The solution space still has a ridge corresponding to the correct fault location but the maximum in the solution space occurs at a higher fault resistance. The impact of the ground mode components can be crudely modeled by an additional resistance in series with the fault resistance. The most important result is that the maximum in the solution space occurs on the ridge relating to the correct fault location. Accurately locating the fault is the most important goal of the genetic search algorithm, the exact fault resistance is of far less importance.

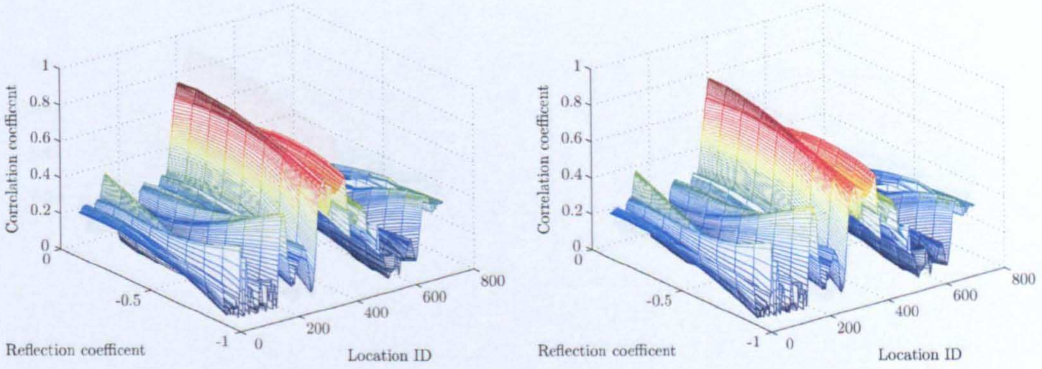


(a) 0 ohm (b) 100 ohm



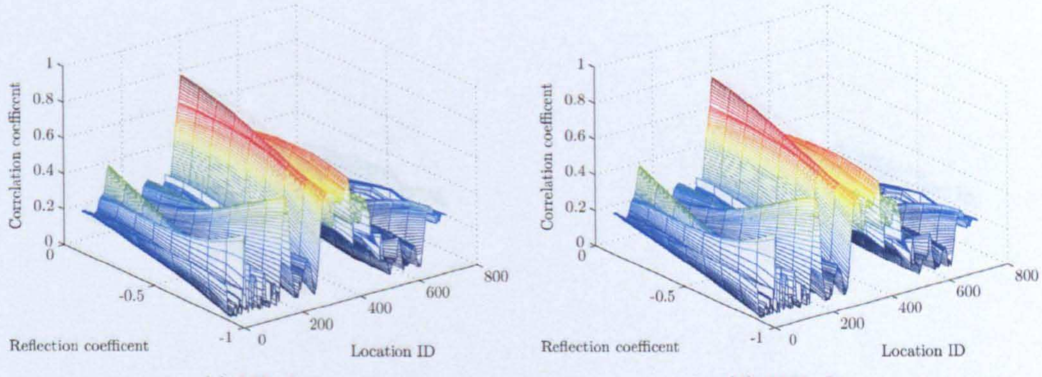
(c) 500 ohm (d) 1000 ohm

FIGURE 4.30: Solution space for single phase faults at fault location 1 for actual fault resistances of 0, 100, 500 and 1000 ohm



(a) 0 ohm

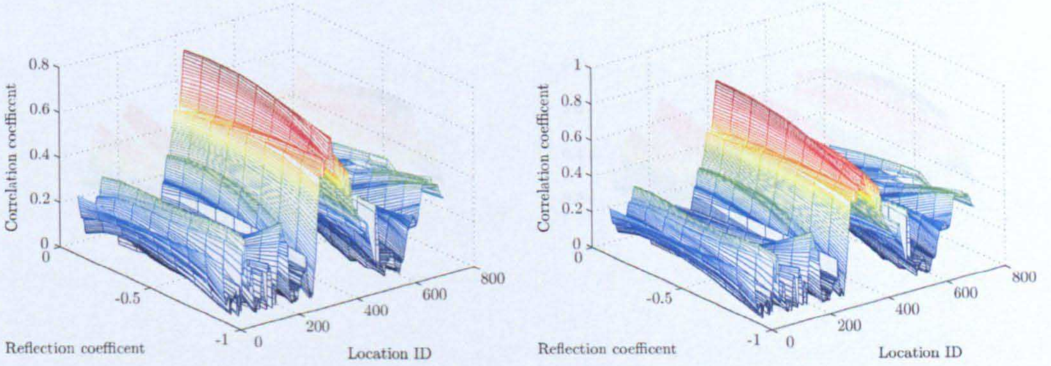
(b) 100 ohm



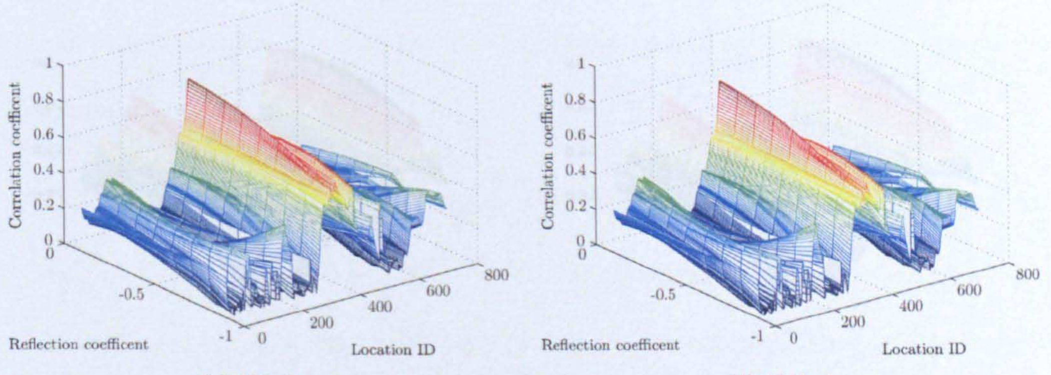
(c) 500 ohm

(d) 1000 ohm

FIGURE 4.31: Solution space for single phase faults at fault location 2 for actual fault resistances of 0, 100, 500 and 1000 ohm

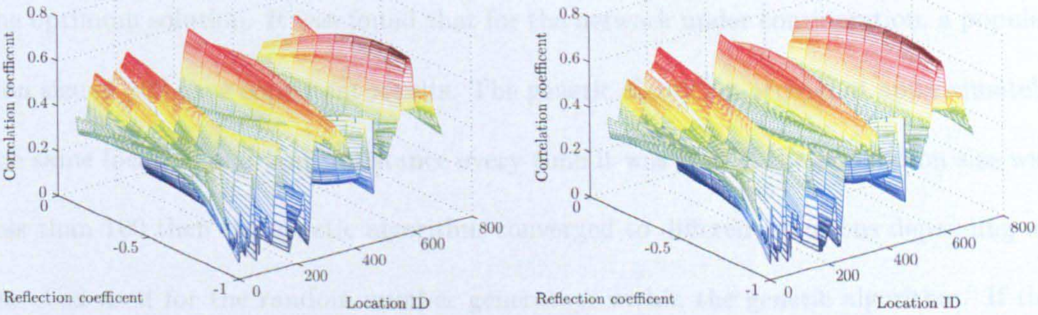


(a) 0 ohm (b) 100 ohm

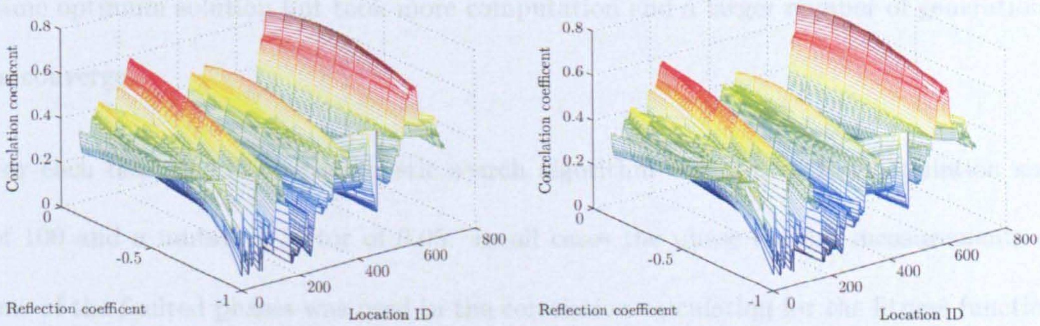


(c) 500 ohm (d) 1000 ohm

FIGURE 4.32: Solution space for single phase faults at fault location 3 for actual fault resistances of 0, 100, 500 and 1000 ohm



(a) 0 ohm (b) 100 ohm



(c) 500 ohm (d) 1000 ohm

FIGURE 4.33: Solution space for single phase faults at fault location 4 for actual fault resistances of 0, 100, 500 and 1000 ohm

### 4.5.4 Performance of Genetic Algorithm

Extensive testing of different combinations of genetic algorithm parameters was performed. As stated in section 4.4.5, the choice of population size has the greatest impact on the performance of the genetic algorithm. If the population size is too small then the genetic algorithm can fail to find the optimum solution, if the population size is too large then excessive computation time is required and the population is slower to converge on the optimum solution. It was found that for the network under consideration, a population size of 100 gave consistent results. The genetic algorithm arrived at approximately the same location and fault resistance every time it was run. If the population size was less than 100 then the genetic algorithm converged to different solutions depending on the seed used for the random number generation within the genetic algorithm. If the population size was made greater than 100, the genetic algorithm still converged to the same optimum solution but took more computation and a larger number of generations to converge.

For each fault condition the genetic search algorithm was run with a population size of 100 and a mutation factor of 0.05. In all cases the phase current measurements of one of the faulted phases was used in the correlation calculation for the fitness function of the genetic algorithm as opposed to one of the aerial mode components. Uniform crossover was used for the genetic crossover operator and to ensure the best solution for each generation was passed down to the next (elitism). The resolution of fault location was encoded to the nearest 10 metres and the fault reflection coefficient had a resolution of 0.01. Fault resistance resolution is not a requirement for correct fault location and the end experience has shown a lower resolution could be used.

The performance of the genetic algorithm was evaluated at a number of levels. The first measure of success was whether the genetic algorithm managed to correctly identify the branch on which the fault occurred. Secondly the error between the predicted location and the actual location was calculated as:

$$\text{location error} = \frac{d_e - d_a}{d_a} \times 100 \qquad (4.3)$$

Where $d_e$ is the estimated distance from observation point to fault location and $d_a$ is the actual distance from observation point to fault location. Thirdly, the error in the fault reflection coefficient and hence fault resistance was calculated as:

$$\text{reflection error} = (\text{estimated reflection} - \text{actual reflection}) \times 100 \qquad (4.4)$$

Table 4.8, Table 4.9 and Table 4.10 show the performance of the genetic algorithm for three phase faults, inter phase fault and single phase fault respectively. The tables show the fault location and fault resistance predicted by the genetic algorithm. For all fault conditions the genetic algorithm identified the correct branch containing the fault. The location of the fault along the branch was estimated in the majority of cases to within 0.5 % of the line length or better which translates to an accuracy of 30 metres. The error in the fault reflection coefficent is approximtaley an order of magnitude greater than the error in the fault location. The reason for this is that the reflection coeffiecient is determined by the amplitude of the reflected wave and since attenuation has not been modeled in the time tree simulation, there is a difference between the amplitude in the ATP simulation and the time tree simulation.

The results show that there was one occasion when the genetic algorithm struggled to locate the correct fault location. This occurred for a single phase 1000 ohm fault at location 1. Recall that the ridge in the solution space for this particular fault condition is very sharp; neighbouring fault locations have comparatively low correlation coefficients. This makes it difficult for the genetic algorithm to 'climb' the ridge to find the optimum solution.

The error in the fault reflection coefficient for single phase fault was very large, 92 % in one case. The cause of this was the ground mode component of the fault which is strongest for low resistance faults. Altough ground mode propagation was not included in the time tree model, there is still a clear ridge in the solution space corresponding to the correct fault location and the results of the genetic algorithm show that it is able to correctly locate the fault.

| Fault | Resistance | Estimated Branch | Estimated Location | Estimated Reflection | Fitness | Error (%) | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Branch | Distance | Reflection |
| F1 | 0 | 0 | 810 | -0.95 | 0.944992 | pass | 1.23 | 5 |
| F1 | 100 | 0 | 820 | -0.60 | 0.952007 | pass | 2.43 | 24 |
| F1 | 500 | 0 | 800 | -0.24 | 0.975457 | pass | 0.0 | 24 |
| F1 | 1000 | 0 | 790 | -0.16 | 0.967841 | pass | 1.23 | 16 |
| F2 | 0 | 5 | 130 | -0.91 | 0.965654 | pass | 1.12 | 9 |
| F2 | 100 | 5 | 110 | -0.56 | 0.960325 | pass | 0.37 | 26 |
| F2 | 500 | 5 | 90 | -0.28 | 0.969515 | pass | 0.37 | 20 |
| F2 | 1000 | 5 | 90 | -0.16 | 0.967245 | pass | 0.37 | 16 |
| F3 | 0 | 6 | 190 | -0.91 | 0.926776 | pass | 0.36 | 9 |
| F3 | 100 | 6 | 200 | -0.60 | 0.972848 | pass | 0.0 | 22 |
| F3 | 500 | 6 | 180 | -0.28 | 0.976636 | pass | 0.72 | 20 |
| F3 | 1000 | 6 | 180 | -0.19 | 0.974409 | pass | 0.72 | 13 |
| F4 | 0 | 10 | 1220 | -0.95 | 0.971117 | pass | 0.40 | 5 |
| F4 | 100 | 10 | 1190 | -0.58 | 0.976409 | pass | 0.20 | 24 |
| F4 | 500 | 10 | 1190 | -0.23 | 0.980826 | pass | 0.20 | 9 |
| F4 | 1000 | 10 | 1180 | -0.14 | 0.979176 | pass | 0.40 | 18 |

TABLE 4.8: Performance of Genetic Algorithm for three phase faults

| Fault | Resistance | Estimated Branch | Estimated Location | Estimated Reflection | Fitness | Error (%) | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Branch | Distance | Reflection |
| F1 | 0 | 0 | 810 | -0.95 | 0.944436 | pass | 0.16 | 5 |
| F1 | 100 | 0 | 810 | -0.70 | 0.976701 | pass | 0.16 | 10 |
| F1 | 500 | 0 | 800 | -0.38 | 0.982305 | pass | 0.0 | 10 |
| F1 | 1000 | 0 | 800 | -0.24 | 0.975442 | pass | 0.0 | 8 |
| F2 | 0 | 5 | 130 | -0.91 | 0.965618 | pass | 1.13 | 9 |
| F2 | 100 | 5 | 110 | -0.79 | 0.963767 | pass | 0.38 | 3 |
| F2 | 500 | 5 | 90 | -0.4 | 0.969055 | pass | 0.38 | 8 |
| F2 | 1000 | 5 | 90 | -0.4 | 0.955132 | pass | 0.38 | 8 |
| F3 | 0 | 6 | 210 | -0.9 | 0.973393 | pass | 0.36 | 10 |
| F3 | 100 | 6 | 210 | -0.75 | 0.976048 | pass | 0.36 | 7 |
| F3 | 500 | 6 | 180 | -0.31 | 0.974093 | pass | 0.72 | 17 |
| F3 | 1000 | 6 | 180 | -0.27 | 0.976613 | pass | 0.72 | 5 |
| F4 | 0 | 10 | 1220 | -0.95 | 0.971108 | pass | 0.40 | 5 |
| F4 | 100 | 10 | 1200 | -0.73 | 0.973601 | pass | 0.0 | 9 |
| F4 | 500 | 10 | 1190 | -0.37 | 0.981166 | pass | 0.20 | 11 |
| F4 | 1000 | 10 | 1190 | -0.24 | 0.980819 | pass | 0.20 | 8 |

TABLE 4.9: Performance of Genetic Algorithm for inter phase faults

| Fault | Resistance | Estimated Branch | Estimated Location | Estimated Reflection | Fitness | Error (%) | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Branch | Distance | Reflection |
| F1 | 0 | 0 | 790 | -0.08 | 0.628906 | pass | 0.16 | 92 |
| F1 | 100 | 0 | 800 | -0.03 | 0.6934 | pass | 0.0 | 79 |
| F1 | 500 | 0 | 800 | -0.0 | 0.754002 | pass | 0.0 | 48 |
| F1 | 1000 | 0 | 960 | -0.0 | 0.478818 | pass | 2.52 | 32 |
| F2 | 0 | 5 | 130 | -0.2 | 0.822597 | pass | 1.13 | 80 |
| F2 | 100 | 5 | 90 | -0.11 | 0.837941 | pass | 0.38 | 71 |
| F2 | 500 | 5 | 100 | -0.06 | 0.846202 | pass | 0.0 | 42 |
| F2 | 1000 | 5 | 100 | -0.01 | 0.842841 | pass | 0.0 | 31 |
| F3 | 0 | 6 | 190 | -0.28 | 0.793649 | pass | 0.37 | 72 |
| F3 | 100 | 6 | 190 | -0.07 | 0.80954 | pass | 0.37 | 75 |
| F3 | 500 | 6 | 190 | -0.04 | 0.8147 | pass | 0.37 | 44 |
| F3 | 1000 | 6 | 190 | -0.0 | 0.811332 | pass | 0.37 | 32 |
| F4 | 0 | 10 | 1200 | -0.79 | 0.733774 | pass | 0.0 | 21 |
| F4 | 100 | 10 | 1190 | -0.65 | 0.738121 | pass | 0.20 | 17 |
| F4 | 500 | 10 | 1180 | -0.43 | 0.74874 | pass | 0.40 | 5 |
| F4 | 1000 | 10 | 1180 | -0.36 | 0.75665 | pass | 0.40 | 4 |

TABLE 4.10: Performance of Genetic Algorithm for single phase faults

## 4.6 Limitations

In the previous section it was shown that the time tree and genetic search algorithm approach to fault location works well for a radial distribution system for a variety of fault conditions. There is, however, a limit to the size of the network for which the technique is successful. The lengths of the branches, although responsible for attenuating and distorting the traveling waves have far less of an impact on the amplitude of the traveling waves when compared with the number of branches in the network. Every time a traveling wave is transmitted through the junction of three similar transmission lines the resulting wave is reduced to 2/3 of the original amplitude. During simulation it was found that is was difficult to identify a fault that was more that 6 junctions away from the observation point (Initial wave attenuated to less than 1/10). On a real system this maybe less because of the resolution of the transducer used to measure the traveling waves. The inception angle of the fault also impacts the performance because the fault angle determines the amplitude of the initial traveling wave at the fault location.

One possible solution to this problem would be to incorporate fault recorders at numerous locations along the distribution line. However, this would negate the advantages of single-ended fault location in terms of requiring the minimum amount of equipment to install and maintain and also non-dependence on communication between multiple points along the distribution line. For major urban distribution lines there may still be the financial justification for such an approach but for rural distribution lines which serve a small number of customer this is unlikely to be the case.

For networks that have less than six junctions between the furthest fault location and observation point the single-ended time tree fault location method is a viable scheme. For larger networks, measurements from more than one location can be combined to give complete coverage. Since a communication channel would exist, a hybrid fault location technique could be used. The double-ended fault location scheme can identify faults that have occurred on the main feeder, by measuring the arrival time of the initial traveling waves at each of the fault recorders. The single-ended time tree approach can be used to locate faults that have occurred on sub feeders using the fault traveling wave pattern from the closet fault recorder, the closet fault recorder being determined from the double-ended scheme.

Another drawback to the single ended time tree approach occurs if there is symmetry in the network topology. For example, consider the network depicted in Fig. 4.34. If a fault occurred at either one of the fault locations marked they would produce identical traveling wave patterns. There would be two high amplitude ridges in the solution space which the genetic algorithm is equally as likely to identify as the correct fault location. The ambiguity can be resolved if the traveling waves are measured at more than one location, however this would lose the advantages of single ended fault location as outlined above.

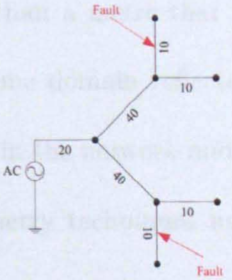


FIGURE 4.34: Diagram of symmetric network

## 4.7 Application to other types of network

The time tree and genetic algorithm technique is not limited to radial power distribution lines. For example, it could be applied to transmission networks which have an interconnected mesh network topology. The single ended time tree fault location scheme could provide a backup to the double-ended scheme or it could be used in situations where only sparse recordings are available [55].

The dimensions of the network to which the time tree analysis can be applied is limited only by the bandwidth of the transducers and sampling frequency of the recording device used to capture the fault traveling wave pattern. The technique could equally by applied to the majority of wiring (either power or communication lines) found on marine vessels and aircraft where the lengths of wire are of the order of tens of metres. Fault location on aircraft, particularly intermittent faults that only occur during flight, is currently a very active area of research. The majority of techniques that have been proposed for locating faults on aircraft wiring are based on reflectometry methods [63] because of the high accuracy to within less than a metre that is required. The most commonly used reflectometry technique is time domain reflectometry which involves injecting a high frequency pulse at one point in the network and measuring the reflected response. However, recently other reflectometry techniques have been developed which can be used to provide continuous monitoring of the aircraft wiring whilst it is in operation [64, 65]. With slight modification, the time tree program can reproduce the response created from a TDR device. This idea is explored in more detail in chapter 6 where time domain reflectometry is applied to a branched communication network.

## 4.8 Summary

In this chapter a fault location scheme has been developed based on a genetic search algorithm that uses time tree analysis to estimate the fault location. The time tree analysis technique allows the traveling wave pattern at a particular fault location and fault resistance to be produced in a very short computation time. It is also very easy to reconfigure the time tree network to predict a different fault location and fault resistance. The fast computation time and reconfigurability has allowed the time tree technique to be used efficiently with a genetic search algorithm. The genetic search algorithm can rapidly evaluate a number of different fault conditions and, by using the mechanics of natural selection, arrive in the majority of cases to a solution within approximately 30 metres of the actual location. The exception to this are when the optimum solution is located on a very sharp ridge in the solution space. In the network evaluated a sharp ridge in the solution space only occurred for close up faults on the first branch of the network.

The performance of the genetic algorithm was similar for 3 phase, inter phase and single phase faults. It was capable of correctly locating the fault location to within approximately 0.5 % of the line length for faults ranging from 0 ohm to 1000 ohm. The accuracy of the fault resistance identified was much less, between 10 and 20 % of the actual fault resistance. This was primarly because the time tree model did not take into account line attenuation but also due to errors in the estimation of the fault reflection coefficient. The actual value of a fault resistance is of far less importance to a dispatch engineer compared with the correct fault location. It was found that accurate fault location was achieved by using the phase current measurements directly without the need to decouple the measurements into their modal components.

# Chapter 5

# Fault Recorder Hardware Design

## 5.1 Introduction

Current commercially available traveling wave fault recorders [11] were originally designed for use on transmission lines. They record the high frequency current traveling waves with a sampling frequency of 1.25 MHz and with an ADC resolution of 8 bits. This is considered adequate for transmission lines [27] because the network topology is relatively straight forward and the lengths of the lines are long. Distribution lines in contrast, typically have a number of sub-feeders which create more points of reflection in the network [6]. The line lengths are also significantly shorter. The resulting traveling wave pattern is more difficult to interpret because there are more traveling wave fronts to identify and the wave fronts are closer together in time. A recorder with a greater resolution is required if single ended traveling wave fault location is to be applied to distribution networks. The required sampling frequency is dictated by the lengths of each section of transmission line in the distribution network and the desired accuracy. The sampling frequency must be sufficient so that important wave fronts are not missed. In this chapter a new high speed, FPGA based, data acquisition unit is developed suitable for recording traveling wave fault data on a variety of distribution systems [66, 67].

## 5.2 System Requirements

In section 2.4.2.4 the challenges of applying traveling wave fault location to power distribution networks was discussed. Sub-feeders that branch off the main distribution line create many more points of reflection in the network, significantly increasing the number of traveling waves for a given disturbance. The length of distribution lines are far less (of the order of km's) when compared with transmission lines (of the order of tens or hundreds of km's) resulting in the traveling wave fronts being much closer together and harder to distinguish.

The resolution of +/- 250m provided by existing fault recorders [11] is considered an adequate resolution for transmission lines because the resolution is comparable to the distance between two supporting towers. For distribution systems, where the poles are closer together, a resolution to the nearest pole (approximately 40m) would be more favorable.

The aim of the new traveling wave fault recorder is to record traveling wave patterns produced from real fault events to further evaluate the performance of the single-ended search algorithm developed in chapter 4. It is also important that the recorder is capable of accurately time tagging fault events so that the double-ended scheme can be used to verify the single ended fault location algorithm and so that data from other traveling wave recorders monitoring the same line can be compared directly. The system requirements for the fault recorder are summarised below:

- The ability to monitor up to six channels simultaneously, allowing the high frequency current in two distribution lines to be monitored or both the high frequency voltage and high frequency current in one distribution line to be monitored.
- Record the input signals at a sampling frequency of at least 10 MHz giving a theoretical maximum resolution of 30 m per sample.
- Provide Global Positioning System (GPS) time tagging of fault events.
- Provide variable gain amplification of input signals.
- Provide secondary storage for recorded transients and a high speed link with a host PC

## 5.3 Hardware Design

A number of design solutions were considered at the early stages of the project including micro controller, Digital Signal Processor (DSP) and Field Programmable Gate Array (FPGA) based solutions. The final choice of an FPGA solution was influenced predominantly by the large I/O requirements of the system, particularly by the need to support six high speed Analogue to Digital Converters (ADC), and the high data throughput rates that it entails

FPGA devices consist of a piece of silicon populated with an array of logic gates and interconnects. By electronically programming the device it is possible to create the desired logic circuit by including or excluding the interconnect between logic circuits. The parallel, concurrent nature of an FPGA solution enables large amounts of data to be handled with a relatively low system clock frequency. Since each separate logic controller of the design effectively works independently from any other, it is possible to be recording a transient event, receiving a GPS time stamp and sending data to a host PC all at the same time - something that would be difficult using a micro controller or DSP unless a very high system clock frequency was used.

Modern FPGA design now facilitates embedding micro controllers in the FPGA logic allowing the benefits of using a micro controller for the control and communication and using the FPGA logic for the high speed, high data rate, time critical part of the design.

### 5.3.1 Overview of Hardware Component

The design of a bespoke FPGA solution requires beyond a single man year of development time so it was decided to develop the fault recorder in collaboration with members of the applied optics group at the University of Nottingham who required a high speed data acquisition board for capturing and processing data from a CMOS camera chip [68] . A high level block diagram of the hardware components in the fault recorder system is shown in Fig. 5.1. The fault recorder consists of a main PCB Board and a number of daughter cards. The main PCB board contains the FPGA device, Quad Data Rate (QDR) memory, Programmable Read Only Memory (PROM), SD-Card and GPS receiver. The main board also has 8 LEDs, 4 push buttons and 8 switches. The ADCs, USB and front-end board are separate daughter cards which plug into the main board. The layout and testing of the main FPGA board was done by Hoang Nyguen[69] and the layout of the ADC and USB board was done by Dr. Yiqun Zhu [70].

Schematic diagrams for the main board can be found in Appendix B. A detail description of the design and layout of the main board, including details of the power requirements, can be found in [69]. A photograph of the final populated main board with and without daughter cards are shown in Fig. 5.2 and Fig. 5.3.

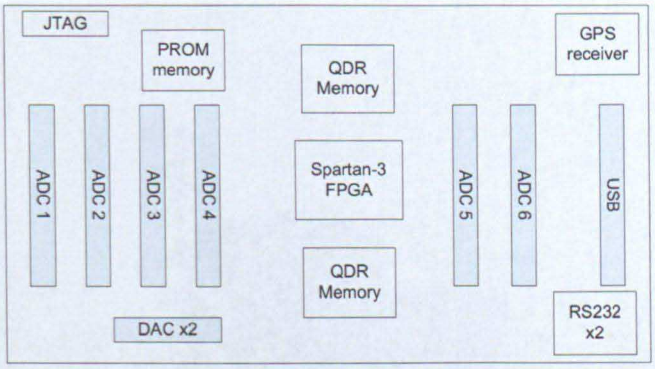


FIGURE 5.1: High level block diagram of FPGA system

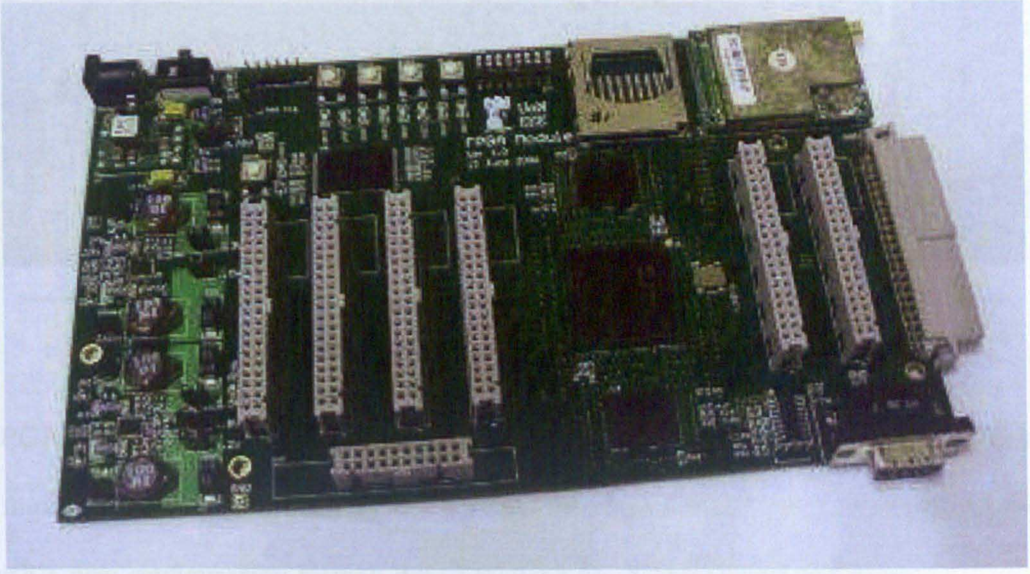


FIGURE 5.2: Photograph of main FPGA board without daughter cards

### 5.3.1.1 FPGA Device and PROM Memory

The FPGA device on the main board is a Xilinx Spartan 3 FPGA [71], chosen predominately for its low cost and large number of I/O pins. The fault recorder supports the Spartan-3 1500K and 4000K gates devices which both have 676 I/O pins.

The Programmable Read Only Memory (PROM) is used to hold the bitmap data file containing the configuration data for the FPGA design. When the power to the board is switched on, the bitmap file is read from the PROM memory and used to configure the

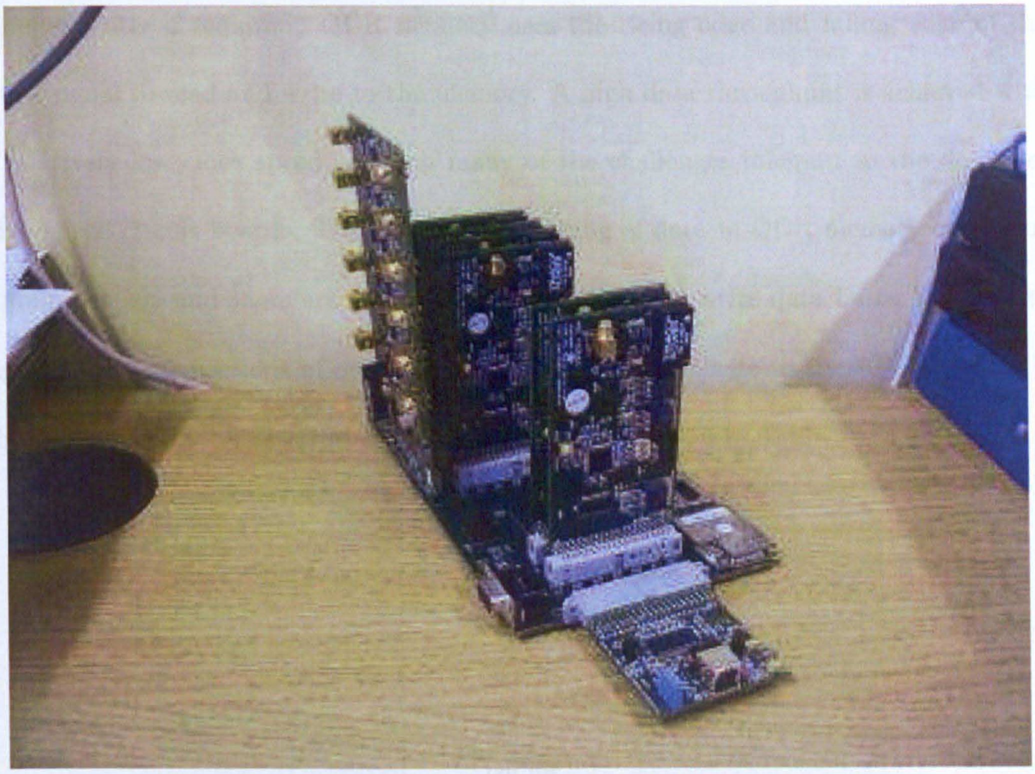


FIGURE 5.3: Photograph of main FPGA board with daughter cards

FPGA. The PROM memory used on the main board is a XCF16PV048C chip made by Xilinx [72]. The PROM memory has a JTAG interface so that it can be reprogrammed with a new configuration bitmap data file using the Xilinx impact software.

Alternatively, the FPGA can be configured in boundary scan mode. The bitmap data is sent from the host PC to the FPGA configuration ports through the JTAG interface. The PROM memory is placed first in the JTAG chain so that on power up the FPGA first loads any bitmap configuration data stored in the PROM memory.

#### 5.3.1.2 QDR Memory

On the main board there are two CY7C1303AV25 QDR SRAM [73] devices made by Cypress. The memory is connected to the FPGA so that both QDR devices can be used independently if required. QDR memory uses the rising edge and falling edge of the clock signal to read and write to the memory. A high data throughput is achieved with a relatively low clock speed avoiding many of the challenges inherent to the design of high speed circuit boards. The reading and writing of data in QDR memory can occur simultaneously and there are therefore separate read and write data buses and control signals. The connections of one of the QDR memory elements to the FPGA device is shown in Fig. 5.4. A description of the connections is given in Table 5.1.

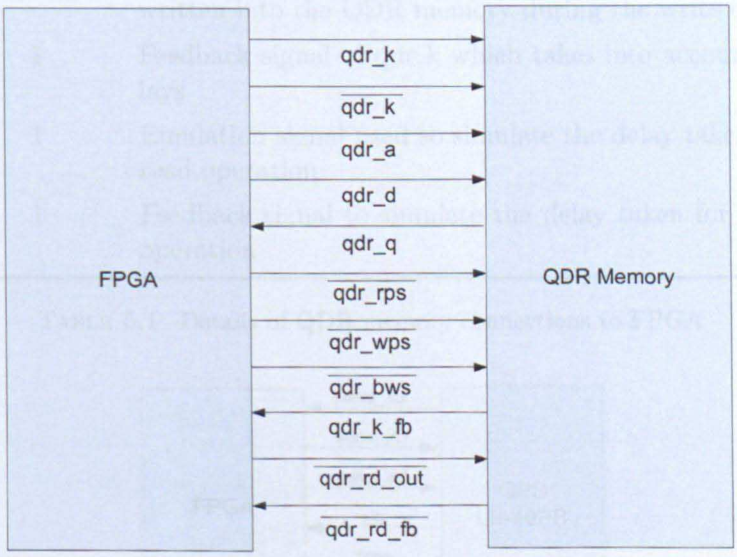


FIGURE 5.4: Connections between FPGA and QDR memory

#### 5.3.1.3 GPS Receiver

The GPS receiver on the fault recorder is an LS-40EB device [74]. This is a fast acquisition enhanced sensitivity 12 channel GPS with a small form factor. It has two RS232 communication channels to read and control the settings of the GPS and provides a 1 pulse per second (1 pps) signal for accurate time synchronisation to within 100 ns. The connections of the GPS receiver to the FPGA device is shown in Fig. 5.5 and a description of the connections is given in Table 5.2

| Name | Width | Description |
|---|---|---|
| qdr_k | 1 | Positive clock input |
| qdr_k_bar | 1 | Negative clock input |
| qdr_a | 19 | Address bus |
| qdr_d | 18 | Input data bus |
| qdr_q | 18 | Output data bus |
| qdr_rps | 1 | Read port select, active low, used to initiate a read operation |
| qdr_wps | 1 | Write port select, active low, used to initiate a write operation |
| qdr_bws | 3 | Byte write select, active low, used to select which byte is written into the QDR memory during the write operation |
| qdr_k_fb | 1 | Feedback signal of qdr_k which takes into account gate delays |
| qdr_rd_out | 1 | Emulation signal used so simulate the delay taken for QDR read operation |
| qdr_rd_fb | 1 | Feedback signal to simulate the delay taken for QDR read operation |

TABLE 5.1: Details of QDR memory connections to FPGA

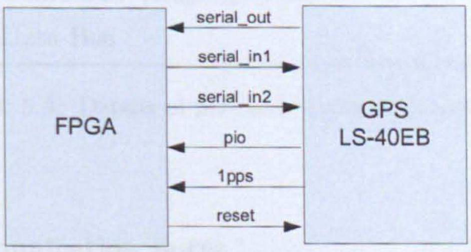


FIGURE 5.5: Connections between FPGA and GPS Receiver

| Name | Width | Description |
|---|---|---|
| serial_out | 1 | Serial data sent from GPS, used to output NMEA sentences |
| serial_in1 | 1 | First serial input to GPS, used to send commands to GPS |
| serial_in2 | 1 | Second serial input to GPS |
| pio | 1 | Pulse indicator signal, indicates to the user when lock signal has been obtained |
| 1pps | 1 | 1 pulse per second signal, used for accurate time tagging of events |
| reset | 1 | GPS reset, active low |

TABLE 5.2: Details of GPS connections to FPGA

#### 5.3.1.4 SD Card Reader

The fault recorder is fitted with a SD-card socket which accepts SanDisk SD cards from 16MB to 2GB and supports SD bus and SPI modes of read write operations [75]. The connections of the SD-card socket and the FPGA device is shown in Fig. 5.6. A description of the connections is given in Table. 5.3

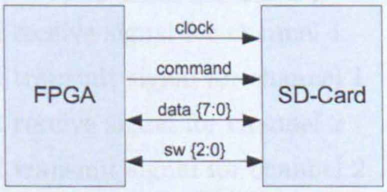


FIGURE 5.6: Connections between FPGA and SD-card reader

| Name | Width | Description |
|---|---|---|
| clock | 1 | Clock Input |
| command | 1 | Command/Response Line |
| data | 4 | Data Bus |

TABLE 5.3: Details of SD-card connections to FPGA

#### 5.3.1.5 RS232 communication ports

There are two RS232 communication channels on the fault recorder board provided by an ICL232 2 channel RS232 transceiver. One of the channels is connected to a DB9 socket and the other connects via a three pin header. The connections of the RS232 ports to the FPGA device is shown in Fig. 5.7. A description of the connections is given in Table. 5.4

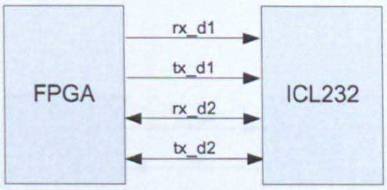


FIGURE 5.7: Connections between FPGA and RS232 transceiver

| Name | Width | Description |
|---|---|---|
| rx_d1 | 1 | Serial receive signal for channel 1 |
| tx_d1 | 1 | Serial transmit signal for channel 1 |
| rx_d2 | 1 | Serial receive signal for channel 2 |
| tx_d2 | 1 | Serial transmit signal for channel 2 |

TABLE 5.4: Details of RS232 connections to FPGA

#### 5.3.1.6 USB Daughter Card

The USB daughter card was developed as part of another research project at the University of Nottingham [70]. It is based around a Cypress EZ-USB FX2 USB Micro controller high-speed peripheral controller [76] which is a single chip integrated USB 2.0 Transceiver and 8051 Microprocessor. The Microprocessor is connected to the FPGA via a 16 bit data bus. Data is transferred from the FPGA to the USB controller into an on-board 4 kB FIFO. The maximum frequency that data can be clocked into or out of the USB controller is 40 MHz. The connections between the USB daughter card and the FPGA device is shown in Fig. 5.8. A description of the connections is given in Table. 5.5.

A picture of the USB daughter card is shown in Fig. 5.9.

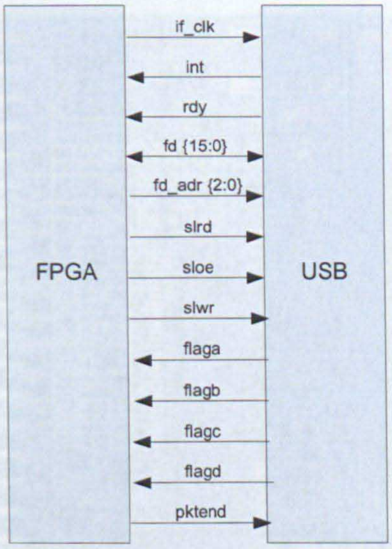


FIGURE 5.8: Connections between FPGA and USB daughter card

| Name | Width | Description |
|---|---|---|
| if_clk | 1 | Interface clock used for clocking data into or out of FIFO |
| int | 1 | USB interrupt signal |
| rdy | 1 | USB ready signal |
| fd | 16 | FIFO data bus |
| fd_addr | 3 | FIFO address bus |
| slrd | 1 | Read word from USB FIFO, active low |
| sloe | 1 | Output enable, active low, sets the direction of data bus |
| slwr | 1 | Write word to USB FIFO, active low |
| flaga | 1 | FIFO status flag (half empty) |
| flagb | 1 | FIFO status flag (empty) |
| flagc | 1 | FIFO status flag (full) |
| pktend | 1 | End current package, asserted to end current package (normally 256) |

TABLE 5.5: Details of usb connections to FPGA

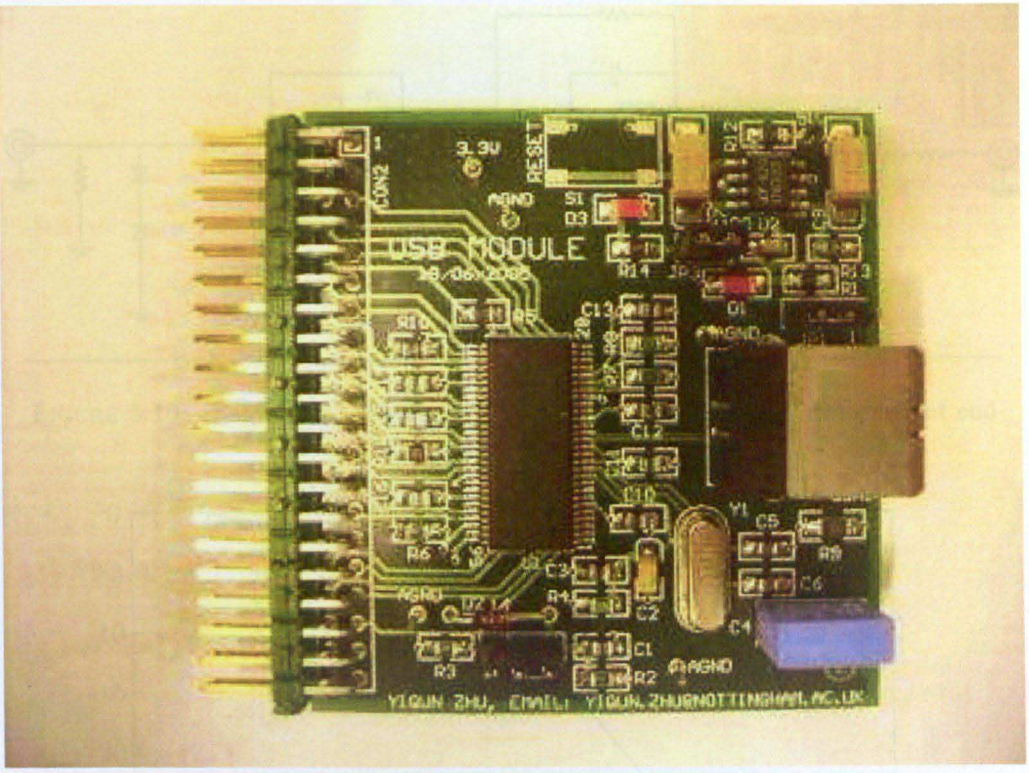


FIGURE 5.9: Picture of USB daughter card

#### 5.3.1.7 Front End Board

The front end PCB consists of anti aliasing filters, to remove high frequency components from the input signals before they are sampled by the ADCs, and variable gain amplification of the input signals, so that the full range of the ADCs can be utilised. A schematic diagram for the entire front end board is shown in Appendix B. Fig 5.10 shows the anti-aliasing filter and variable gain amplifier for one channel.

The input signals to the front-end board are past through a 4 pole butter-worth low pass filter implemented in a two stage Sallen-Key circuit. This removes any frequency components above the cutoff frequency of 5 MHz. Fig. 5.11 shows the measured magnitude frequency response for the anti-aliasing filter.

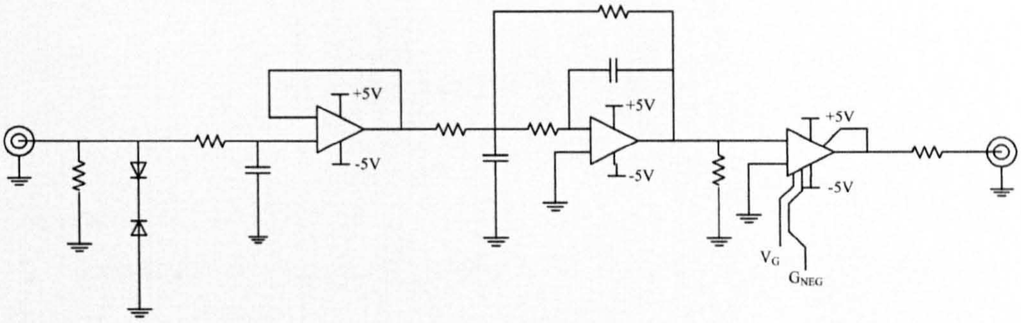


FIGURE 5.10: Diagram of anti aliasing filter and variable gain amplifier on front end board

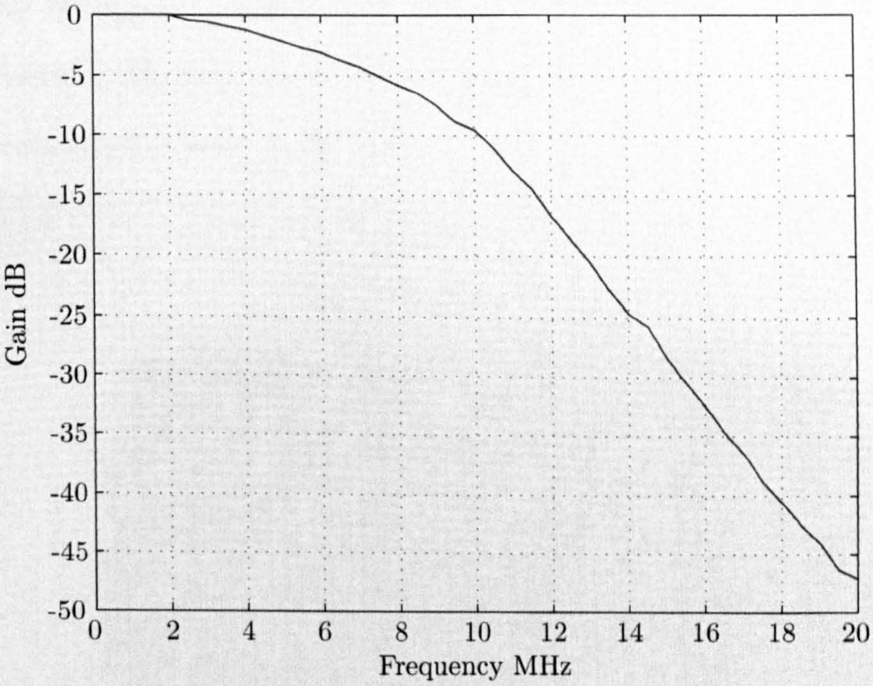


FIGURE 5.11: Measured frequency response of anti-aliasing filter

The output of the filters for each channel are connected to the inputs of AD603 variable gain amplifiers [77] that provide amplification between -11 dB and +35 dB. The gain for the amplifiers is controlled by the analogue voltage $V_G$ which is produced by AD7801 Digital to Analogue Converters (DAC) [78] on the front-end board. There are two DACs on the front end board, each responsible for controlling the gain of three input signals.

The interface between the DACs on the front end board and the FPGA is shown in

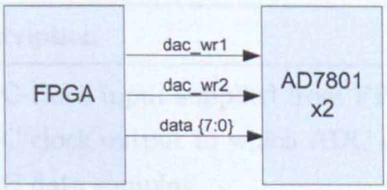


FIGURE 5.12: Connections between FPGA and DACs on front-end board

Fig. 5.12. The DACs have an 8 bit resolution which translates to a gain resolution of 0.16dB per bit. Both DACs share the same 8 bit data bus but have separate write signals. Writing to the DACs is achieved by sending the appropriate DAC write signal (**dac_wr1** or **dac_wr2**) low for one clock cycle. A photograph of the final populated front end board is shown in Fig. 5.13

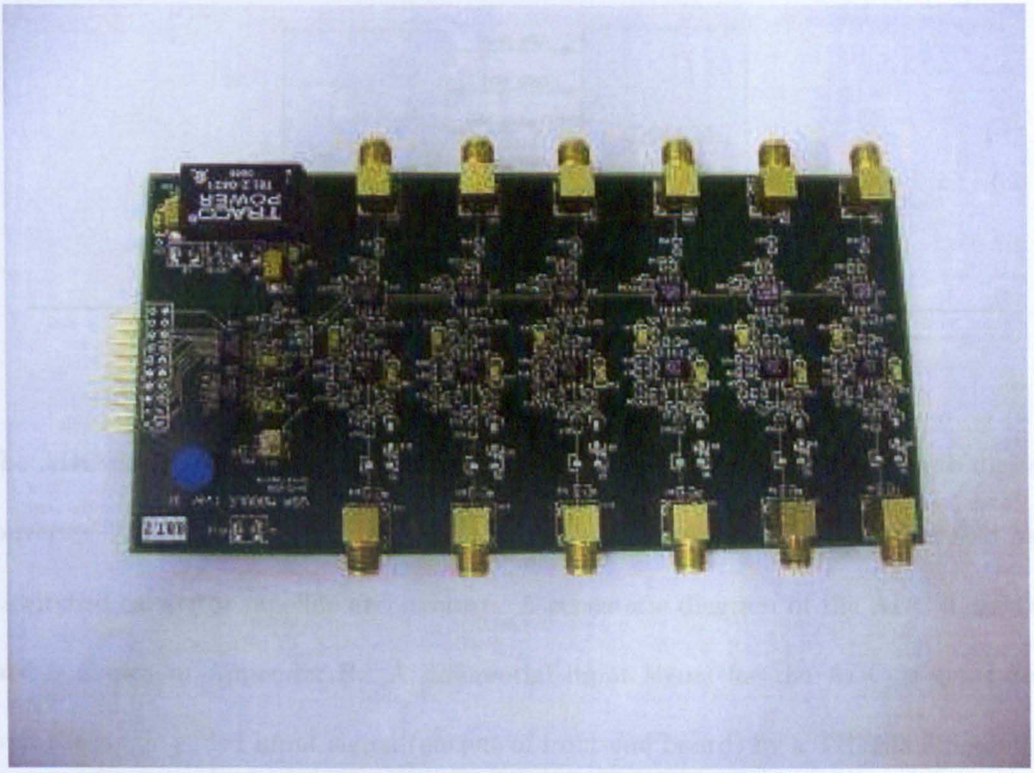


FIGURE 5.13: Photograph of populated front end board

| Name | Width | Description |
|---|---|---|
| adc_clki | 1 | ADC clock input supplied from FPGA |
| adc_clko | 1 | ADC clock output to which ADC data is syncronised |
| adc_data | 14 | ADC data samples |
| adc_sclk | 1 | ADC serial programming clock |
| adc_sen | 1 | ADC serial programming enable |
| adc_sdata | 1 | ADC serial programming data |

TABLE 5.6: Details of ADC connections to FPGA

#### 5.3.1.8 ADC Daughter Card

The connections between one ADC daughter card and the FPGA is shown in Fig. 5.14. A description of the connections is given in Tables 5.6

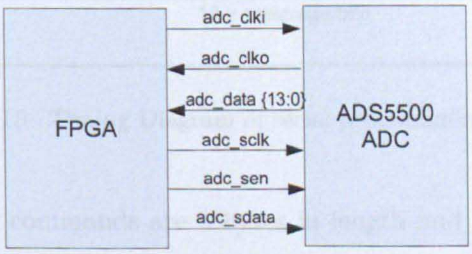


FIGURE 5.14: Connections between FPGA and one ADC socket

The ADC daughter card is based on a Texas Instruments ADS5500 analogue to digital converter [79]. The ADS5500 is a 14 bit, 125 MSPS analogue to digital converter that has a switched capacitor pipeline architecture. A schematic diagram of the ADC daughter card is shown in Appendix B. A differential input signal for the ADC is generated from the single-ended input signal (output of front-end board) by a TH4503 differential amplifier [80]. The ADC input voltage range is 2.3 Vpp. The pipeline architecture of the ADC introduces a 16.5 clock cycle delay latency to the data. Data is presented at the output of the ADC as a 14 bit parallel word and syncronised to a separate output clock.

The operation of the ADC is controlled via a three-wire serial programming interface. The ADC can be put into various test configurations or be powered down via the serial programming interface. The ADC requires the use of an on-board Digital Lock Loop (DLL) for sampling frequencies above 50 MSPS. In the default configuration, the DLL is turned on and so when using lower sampling frequencies (i.e. 40 MSPS) it is necessary to first turn off the DLL. The timing diagram for the serial programming interface is shown in Fig. 5.15.

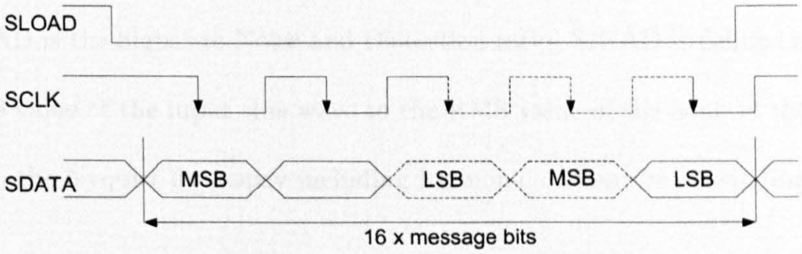


FIGURE 5.15: Timing Diagram of serial programming interface

The serial programming commands are 2 bytes in length and are sent MSB first. The first 4 bits relate to the address and the remaining 12 bits are data as shown in Fig. 5.16.

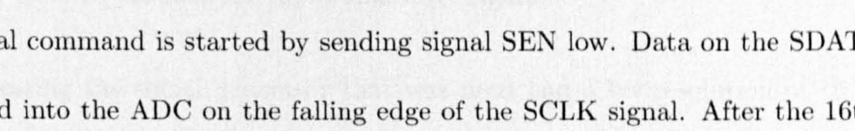


FIGURE 5.16: Format of ADC serial programming message

The serial command is started by sending signal SEN low. Data on the SDATA signal is latched into the ADC on the falling edge of the SCLK signal. After the 16th SCLK falling edge the data is loaded on the ADC. Details of all the commands available can be found in the ADS5500 data sheet [79].

To quantify the performance of the ADC a measure known as the Effective Number of Bits (ENOB) was obtained across the frequency range of interest. The effective number of bits for a sine wave input at a given input frequency is calculated from the Signal-to-Noise and Distortion ratio as [79]:

$$ENOB = \frac{(SINAD - 1.76)}{6.02} \tag{5.1}$$

where SINAD is the Signal-to Noise and Distortion ratio. SINAD is defined as the ratio of the RMS value of the input sine wave to the RMS value of the noise of the converter from DC to the Nyquist frequency including harmonic content but excluding DC.

$$SINAD = 20\log_{10}\frac{Input(V_s)}{(\text{Noise} + \text{Harmonics})} \tag{5.2}$$

Fig. 5.17 shows the ADC daughter card ENOB performance against frequency. The data sheet for the ADC gives a typical value for the ENOB of 11.3 bits for input frequency of 70 MHz sampling at a rate of 125 MSPS. This is less than was achieved on the ADC daughter card but drawing a direct comparison is difficult because the data sheet does not provide a typical value for the ENOB when sampling at a lower rate with the DLL turned off. The performance of the ADC is also dictated by the quality of the signal generator used to produce the input sine wave signal.

During testing the signal generator that was used had a bit resolution of 16 bits and a SINAD value of 60 dB at 10 MHz which gives and ENOB value of 9.67 bits. Under these conditions the ADC daughter card performed close to the theoretical maximum achievable with the signal generator available.

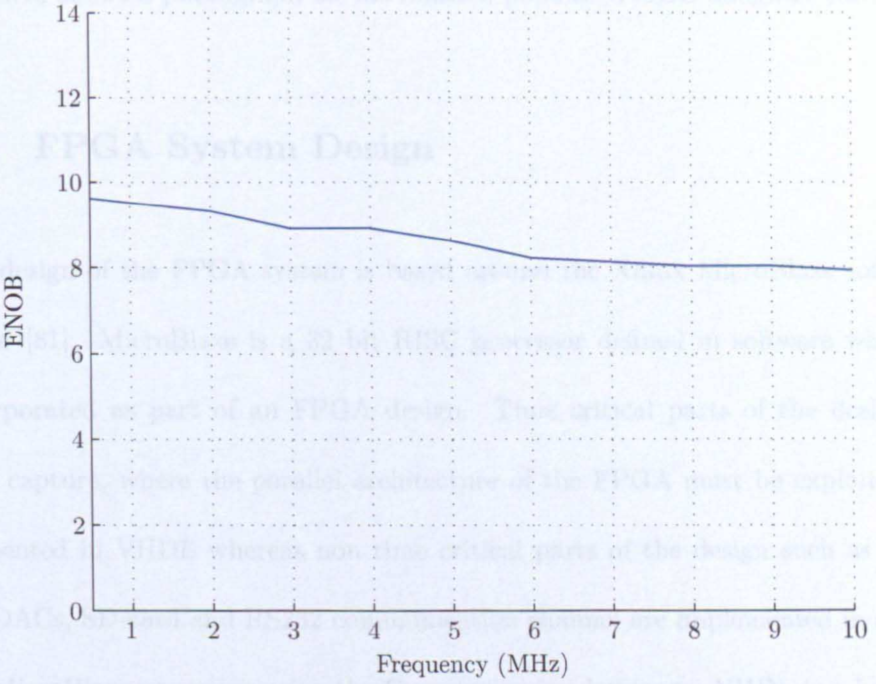


FIGURE 5.17: ADC daugther card ENOB performance against frequency

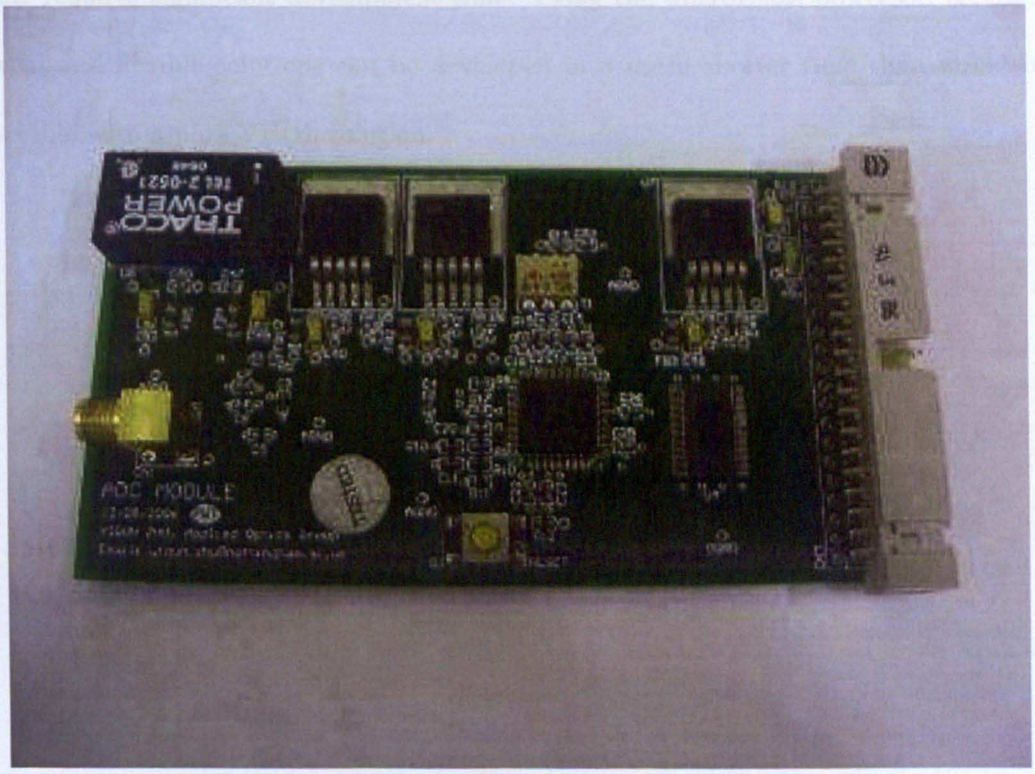


FIGURE 5.18: Photograph of populated ADC daughter card

Fig. 5.18 shows a photograph on the finished populated ADC daughter card.

## 5.4 FPGA System Design

The design of the FPGA system is based around the Xilinx MicroBlaze soft core processor [81]. MicroBlaze is a 32 bit RISC processor defined in software which can be incorporated as part of an FPGA design. Time critical parts of the design such as data capture, where the parallel architecture of the FPGA must be exploited, are implemented in VHDL whereas non time critical parts of the design such as controlling the DACs, SD-card and RS232 communication channel are implemented in software on the MicroBlaze processor using the C programming language. VHDL is a hardware description language used to describe synthesizable logic circuits. It is a low level language that requires significant development time. Using the MicroBlaze processor, sophisticated and flexible solutions can be developed in a much shorter time than would be possible with a pure VHDL solution.

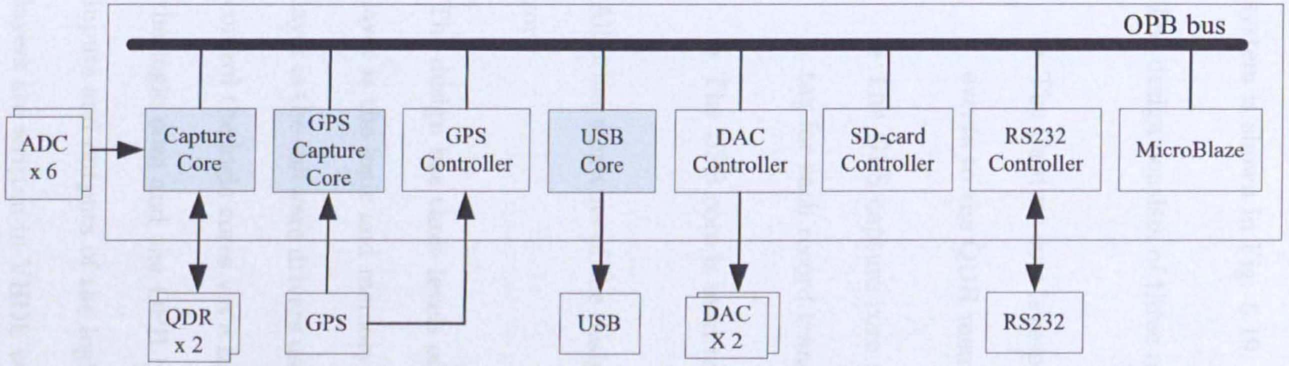


FIGURE 5.19: Top level diagram of FPGA system

### 5.4.1 Overview of system

The system consists of a number of VHDL logic cores connected to the MicroBlaze processor via the On-board Peripheral Bus (OPB). The top level diagram of the FPGA system is shown in Fig. 5.19.

The design consists of three main VHDL cores:

- The Capture core is responsible for capturing ADC data and writing fault transient events to the QDR memory.
- The GPS capture core provides the MicroBlaze processor with an accurate time tag for each record transient event.
- The USB core is used to transmit recorded events to the host PC.

All other elements of the design are implemented in software on the MicroBlaze processor.

The design has three levels of abstraction which are shown in Fig 5.20. At the bottom layer is the logic and memory elements the make up the VHDL logic cores. At the top layer is the software drivers used by the program running on the MicroBlaze processor to control the logic cores via a register interface. The second layer is the interface between the logic core and the OPB bus of the MicroBlaze processor. This layer connects the inputs and outputs of the logic core to registers and to the OPB bus. The bottom two layers are written in VHDL whereas the top layer is written in C.

The design of the cores has taken advantage of some VHDL primitives which are specific to Xilinx FPGAs. An explanation of the primitives used are given in Table 5.7.

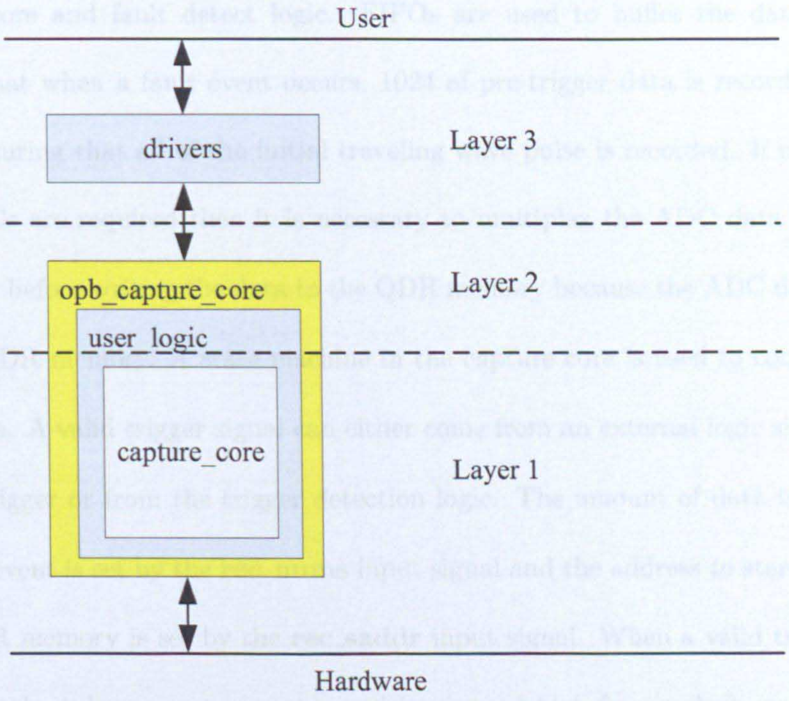


FIGURE 5.20: Levels of abstraction in FPGA design

| Name | Description |
|---|---|
| OBUF | Output buffer used to isolate a signal leaving the FPGA chip from the internal logic circuit and provide the correct amount of drive current to the external circuitry. |
| IBUF | Input buffer used to isolate a signal entering the FPGA chip from the internal logic circuit. |
| BUFG | special type of buffer used to buffer global clock signals. |
| DCM | Digital Clock Manager used to generate the different clock frequencies and phase shift clock signals within the design. |

TABLE 5.7: Details of Xilinx VHDL primitives

### 5.4.2 Capture Core

The Capture Core monitors the data from the ADCs for a possible fault event and records the data to QDR memory when an event is detected. A diagram of the capture core is shown in Fig. 5.21 and a description of the control parameters and input/output signals is given in Table. 5.8. The core consists of the ADC controller core, the memory controller core and fault detect logic. FIFOs are used to buffer the data from the ADCs so that when a fault event occurs, 1024 of pre-trigger data is recorded for each channel ensuring that all of the initial traveling wave pulse is recorded. If more than 4 of the ADCs are required then it is necessary to multiplex the ADC data using a 3:2 multiplexer before writing the data to the QDR memory because the ADC data is wider than the QDR memory. A state machine in the capture core is used to coordinate the flow of data. A valid trigger signal can either come from an external logic signal, a user initiated trigger or from the trigger detection logic. The amount of data to record for each fault event is set by the **rec_nums** input signal and the address to starting writing in the QDR memory is set by the **rec_saddr** input signal. When a valid trigger signal is received, the **trigger_out** output signal is asserted high for on clock cycle and data from the FIFOs is recorded to the QDR memory for the desired number of samples. The **trigger_out** output signal is used to trigger an interrupt on the MicroBlaze processor and to capture the current counter value in the GPS capture core. Whilst the data is being written to the QDR memory, the **rec_ doing** output signal is held high. Once the data has been written to the QDR memory the **rec_ done** output signal is asserted high for one clock cycle and the capture core returns to monitoring for a valid trigger event. The management of the QDR memory in terms of the number of samples to record and where to write in memory is implemented in software on the MicroBlaze processor and is described in more detail in section 5.4.5.

#### 5.4.2.1 ADC Core

The ADC Core is used to capture data from the ADS5500 ADCs and to configure them in the correct mode of operation via the serial programming interface. A diagram of the

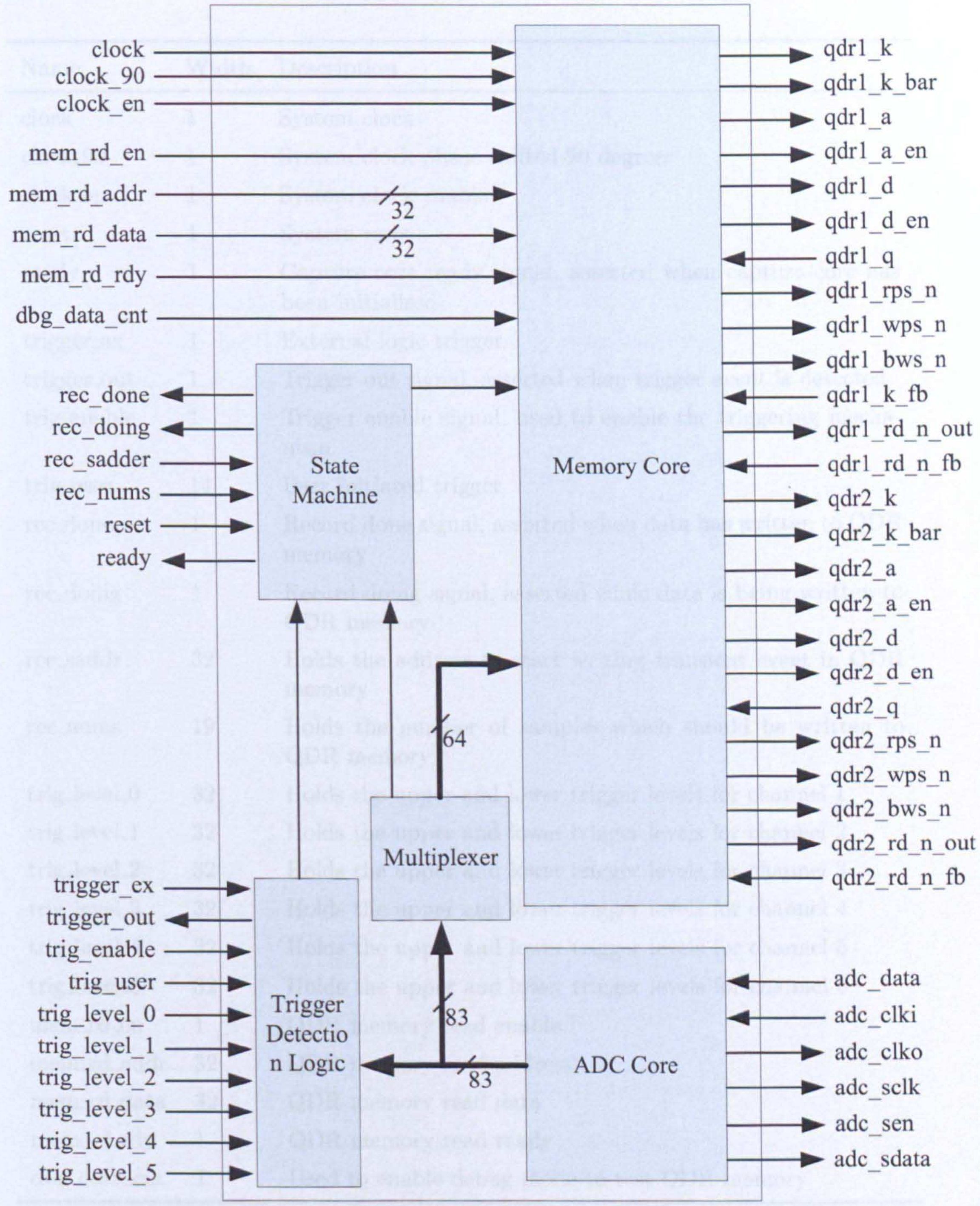


FIGURE 5.21: Diagram of capture core

| Name | Width | Description |
|---|---|---|
| clock | 1 | System clock |
| clock_90 | 1 | System clock phase shifted 90 degrees |
| clock_en | 1 | System clock enable |
| reset | 1 | System reset |
| ready | 1 | Capture core ready signal, asserted when capture core has been initialised |
| trigger_ex | 1 | External logic trigger |
| trigger_out | 1 | Trigger out signal, asserted when trigger event is detected |
| trig_enable | 1 | Trigger enable signal, used to enable the triggering mechanism |
| trig_user | 14 | User initiated trigger |
| rec_done | 1 | Record done signal, asserted when data has written to QDR memory |
| rec_doing | 1 | Record doing signal, asserted while data is being written to QDR memory |
| rec_saddr | 32 | Holds the address to start writing transient event in QDR memory |
| rec_nums | 19 | Holds the number of samples which should be written to QDR memory |
| trig_level_0 | 32 | Holds the upper and lower trigger levels for channel 1 |
| trig_level_1 | 32 | Holds the upper and lower trigger levels for channel 2 |
| trig_level_2 | 32 | Holds the upper and lower trigger levels for channel 3 |
| trig_level_3 | 32 | Holds the upper and lower trigger levels for channel 4 |
| trig_level_4 | 32 | Holds the upper and lower trigger levels for channel 5 |
| trig_level_5 | 32 | Holds the upper and lower trigger levels for channel 6 |
| mem_rd_en | 1 | QDR memory read enable |
| mem_rd_addr | 32 | QDR memory read address |
| mem_rd_data | 32 | QDR memory read data |
| mem_rd_rdy | 1 | QDR memory read ready |
| dbg_data_cnt | 1 | Used to enable debug mode to test QDR memory |

TABLE 5.8: Details of capture core input and output signals

| Name | Type | Description |
|---|---|---|
| C_DLL_ON | boolean | Used to turn the internal DLL on ADCs on or off |
| C_NUM_CHANNEL | integer | Number of ADC channels used on FPGA main board |
| C_SEL_CLKO | integer | Selects the ADC channel from which the output clock is used for reference |
| C_CAP_DELAY | integer | Emulate the ADSS500 pipeline delay plus internal FPGA delay |
| C_ADC_CLK_DIV | integer | Used to decimate ADC data to achieve lower sampling frequencies |

TABLE 5.9: Details of ADC core generic parameters

| Name | Width | Description |
|---|---|---|
| clock | 1 | System clock |
| reset | 1 | System reset |
| cfg_done | 1 | Asserted when ADC configuration has completed |
| data_out_en | 1 | Asserted when ADC data is valid |
| data_out | 84 | Data from six ADCs |

TABLE 5.10: Details of ADC core input and output signals

ADC controller core is shown in Fig. 5.22 and a description of the control parameters and input output signals is given in Table. 5.10 and 5.9 respectively.

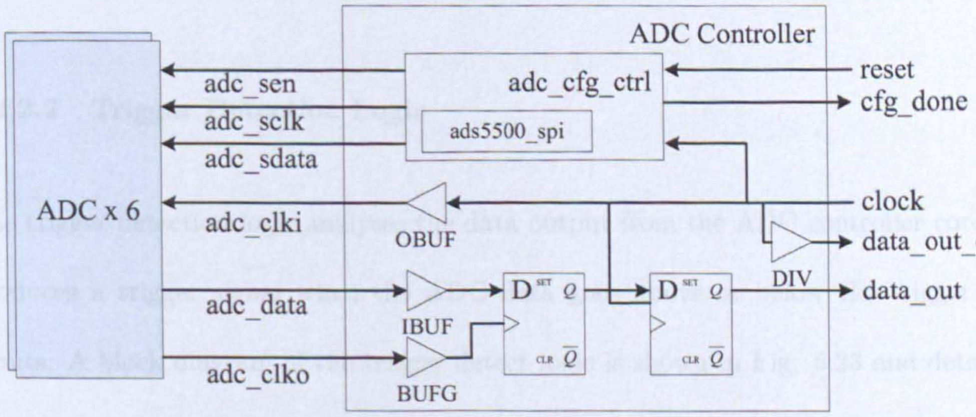


FIGURE 5.22: Diagram of ADC controller core

When the FPGA first powers up or whenever there is global reset signal the ADC configuration routine is performed. The configuration routine configures the DLL on each ADC depending on whether the ADC is operating in high sampling frequency mode or low sampling frequency mode. The configuration routine is implemented in a state machine which produces the three relevant serial programming interface signals for each ADC. The SPI interface signals adhere to the timing diagram in Fig. 5.15.

The ADC controller core provides each ADC with a valid clock signal from the FPGA clock which is buffered through a OBUF primitive. Each ADC has an output clock signal to which the data is synchronised. One of the ADC output clock signals is chosen via the **C_SEL_CLK_O** control parameter to be the clock source for the FDC latches used to capture the ADC data from all the ADCs connect to the FPGA. The selected ADC clock source is buffered using a BUFG primitive. ADC data is clocked out of the second FDC latch using the FPGA clock ensuring that data is synchronised to the FPGA clock. Any differences in the alignment of ADC data as a result of different track lengths between the FPGA and the ADCs is eliminated. The data enable signal can be used to decimate the ADC sampling frequency. The amount of decimation is determined by the **C_ADC_CLK_DIV** control parameter.

#### 5.4.2.2 Trigger Detection Logic

The trigger detection logic analyses the data output from the ADC controller core and produces a trigger signal when the ADC data goes above or below the trigger level inputs. A block diagram of the trigger detect logic is shown in Fig. 5.23 and details of the input and output signals are given in Table. 5.11.

The trigger detection logic monitors the data relating to one ADC channel. The logic is generated for each of the ADCs in the system. If the input data from the ADC core goes

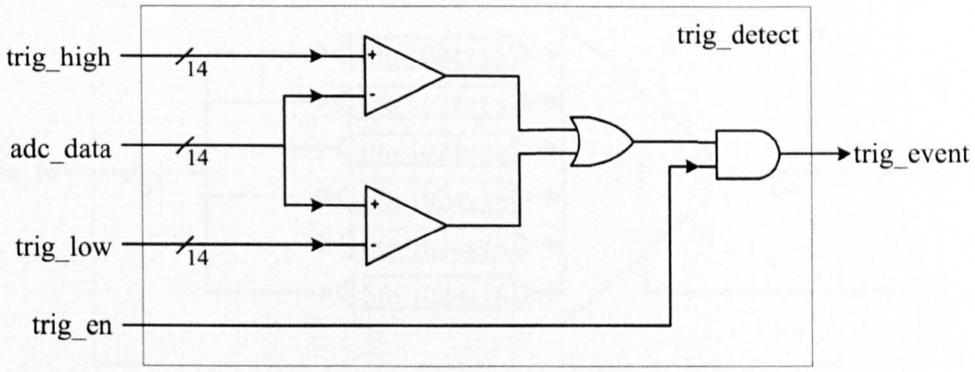


FIGURE 5.23: Diagram of Trigger Detect Core

| Name | Width | Description |
|---|---|---|
| clock | 1 | System clock |
| reset | 1 | System reset |
| data_in | 14 | Data in from one ADC channel |
| trig_high | 14 | Holds upper trigger level value |
| trig_low | 14 | Holds lower trigger level value |
| trig_en | 1 | Enables trigger detection logic |
| trig_event | 1 | Asserted when a trigger event is detected |

TABLE 5.11: Details of trigger detection input and output signals

above or below the upper or lower trigger levels then a trigger signal is generated. The trigger output signals from each of the trigger detection logic blocks are ORed together to produce one data trigger signal. The data trigger signal is ORed with the external trigger input and the user trigger input. The result of this operation is ANDed with the trigger enable input to produce the trigger signal for the state machine in the capture core. This is depicted in Fig. 5.21.

### 5.4.2.3 Multiplexer Controller

The Multiplexer Controller consists of six FIFO memory elements and a multiplexer as shown in Fig. 5.24. Details of the input and output signals are shown in Table 5.12.

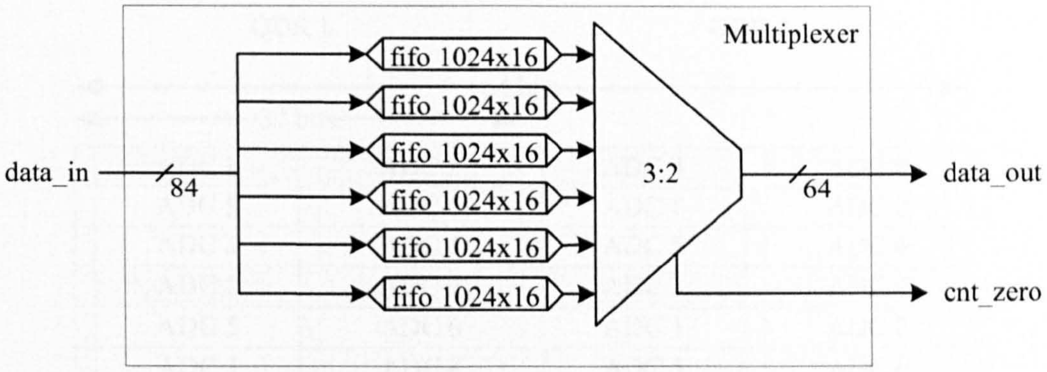
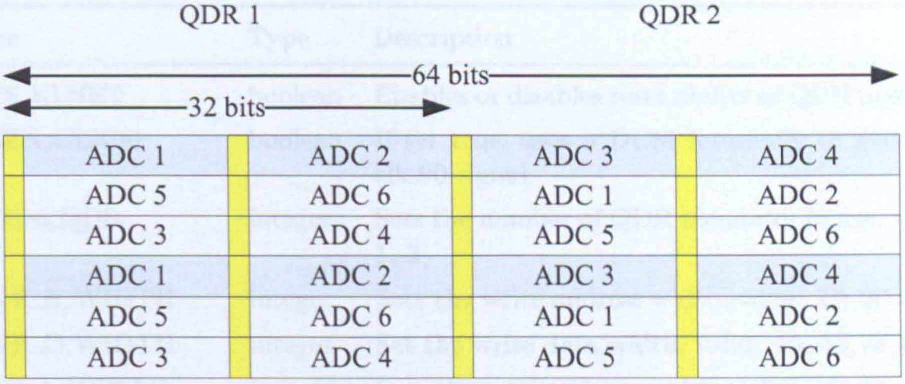


FIGURE 5.24: Diagram of Multiplexer core

| Name | Width | Description |
|---|---|---|
| reset | 1 | System Reset |
| in_clk | 1 | System clock |
| in_data | 96 | ADC data input from six ADCs which have been made 16 bits wide for each channel |
| in_data_en | 1 | Asserted when in_data is valid |
| out_clk | 1 | Memory clock (1.5 times system clock) |
| out_data | 64 | Multiplexed data formatted for QDR memory |
| out_data_en | 1 | Asserted when out_data is valid |
| out_cnt_zero | 1 | Asserted when out_data consists of data from ADCs 1-4 |

TABLE 5.12: Details of multiplexer controller input and output signals

Multiplexing of the input signals is necessary when more than 4 ADCs are in use because the data width from the ADCs is wider than the maximum width of the QDR memory. If six ADCs are being used, the output signal from the ADCs is 84 bits wide (6 x 14 bits) but the maximum width that the QDR memory can be configured to is 64 bits. A 3:2 multiplexer is used to format the data to a 64 bit width. The outputs of the FIFOs must be read at least 1.5 times the speed of the ADC clock frequency. A DCM is used to generate the higher clock frequency which is also used to operate the QDR memory. Fig. 5.25 shows a diagram of how the ADC data is mapped into the QDR memory if the multiplexer is used.



| | | | |
|---|---|---|---|
| ADC 1 | ADC 2 | ADC 3 | ADC 4 |
| ADC 5 | ADC 6 | ADC 1 | ADC 2 |
| ADC 3 | ADC 4 | ADC 5 | ADC 6 |
| ADC 1 | ADC 2 | ADC 3 | ADC 4 |
| ADC 5 | ADC 6 | ADC 1 | ADC 2 |
| ADC 3 | ADC 4 | ADC 5 | ADC 6 |

FIGURE 5.25: Diagram showing how ADC data is stored in QDR memory

The signal **mux_cnt_zero** is asserted whenever the multiplexer output consists of ADC channels 1-4. The **mux_cnt_zero** is used by the capture core state machine to ensure that when the data is read out from the QDR memory, the data from each of the ADC channels is aligned in the same place in memory each time. If up to 4 ADC channels are being used then the multiplexer controller is replaced with just the FIFO memory elements.

#### 5.4.2.4 Memory Core

The Memory core controls the two QDR memory devices connected to the FPGA. It was design as part of another related project [69] at the University of Nottingham. The memory core is depicted in Fig. 5.26 and a description of the control parameters and input output signals are given in Table 5.13 and 5.14 respectively. The core can be configured to use either one or both of the QDR memory devices and the memory read and write data buses can be independently set to 16, 32 or 64 bit widths.

For the fault recorder both QDR devices are required and are configured with a write data bus of 64 bits. The read data bus is configured to 32 bits to make it compatible with the 32 bit OPB bus of the MicroBlaze processor.

| Name | Type | Description |
|---|---|---|
| C_EN_RESET | boolean | Enables or disables reset ability of QDR memory |
| C_GEN_CLK90 | boolean | If set true, uses a DCM internally to generate clk_90 signal |
| C_NUM_QDR | integer | Sets the number of QDR memories to use, valid: 1, 2 |
| C_WR_A_WIDTH | integer | Sets the write address width, valid: 19, 20 or 21 |
| C_WR_D_WIDTH | integer | Set the write data width, valid: 16, 32, or 64 |
| C_RD_A_WIDTH | integer | Sets the read address width, valid: 19, 20 or 21 |
| C_RD_D_WIDTH | integer | Set the read data width, valid: 16, 32, or 64 |
| C_PHASE_SHIFT | integer | Sets the phase shift of the clock used to capture QDR data |
| C_FB_CLK_SOURCE | integer | Sets the QDR feedback clock source. 0 = DCM 1 = clk_0 2 = clk_90 3 = clk_180 4 = clk_270 |

TABLE 5.13: Details of memory core generic parameters

| Name | Width | Description |
|---|---|---|
| clk_in | 1 | Clock input |
| clk_in_90 | 1 | 90 degree phase shifted clock input. Valid if C_GEN_CLK90 is false |
| clk_in_en | 1 | Asserted if clock inputs are valid. Valid if C_GEN_CLK90 is false |
| clk_out | 1 | Clock output, equal to clk_in if C_GEN_CLK90 is false |
| clk_out_90 | 1 | 90 degree phase shifted clock output. Valid if C_GEN_CLK90 is true |
| clk_out_en | 1 | Asserted if clock output signals are valid. Valid if C_GEN_CLK90 is true |
| reset | 1 | System reset |
| ready | 1 | Asserted if QDR memory is initialised |
| mem_wr_addr | 19 | QDR memory write address bus |
| mem_wr_data | 64 | QDR memory write data bus |
| mem_wr_en | 1 | QDR memory write enable |
| mem_rd_addr | 20 | QDR memory read address bus |
| mem_rd_data | 32 | QDR memory read data bus |
| mem_rd_en | 1 | QDR memory read enable |
| mem_rd_rdy | 1 | QDR memory read ready signal, asserted when memory is ready to be read after read enable signal |

TABLE 5.14: Details of memory core input and output signals

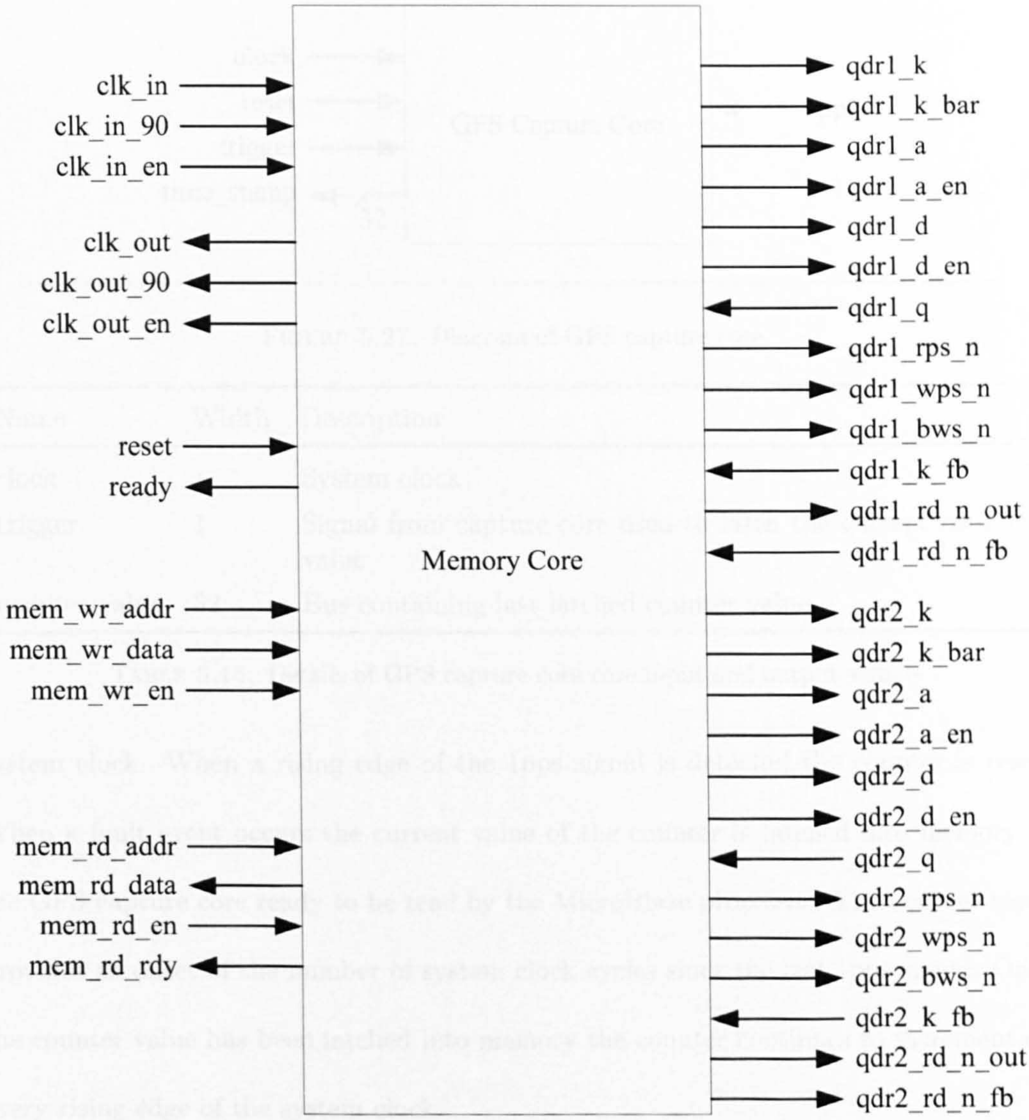


FIGURE 5.26: Diagram of Memory Controller

### 5.4.3 GPS Capture Core

The GPS capture core uses the 1pps output of the GPS device, which is accurate to 100 ns, in conjunction with the FPGA system clock to provide an accurate time stamp. The GPS capture core interface signals are shown in Fig. 5.27 and a description of the control parameters and input/output signals is given in Table. 5.15

Within the GPS capture core is a counter which increments on every rising edge of the

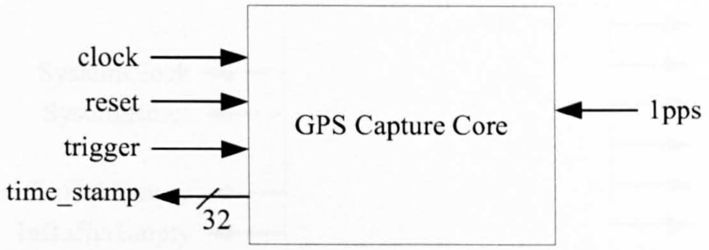


FIGURE 5.27: Diagram of GPS capture core

| Name | Width | Description |
|---|---|---|
| clock | 1 | System clock |
| trigger | 1 | Signal from capture core used to latch the current counter value |
| counter_value | 32 | Bus containing last latched counter value |

TABLE 5.15: Details of GPS capture core core input and output signals

system clock. When a rising edge of the 1pps signal is detected the counter is reset. When a fault event occurs the current value of the counter is latched into memory in the GPS capture core ready to be read by the MicroBlaze processor. The counter value provides an offset of the number of system clock cycles since the last 1pps signal. Once the counter value has been latched into memory the counter continues to increment on every rising edge of the system clock.

### 5.4.4 USB Core

The USB core controls the operation of the USB daughter card. The core was originally designed for [70] and was subsequently modified in [69] so that it could be interfaced to the OPB bus and operated by the program running on the MicroBlaze processor. The USB core interface signals are shown in Fig. 5.28 and a description of the input/output signals is given in Table 5.16.

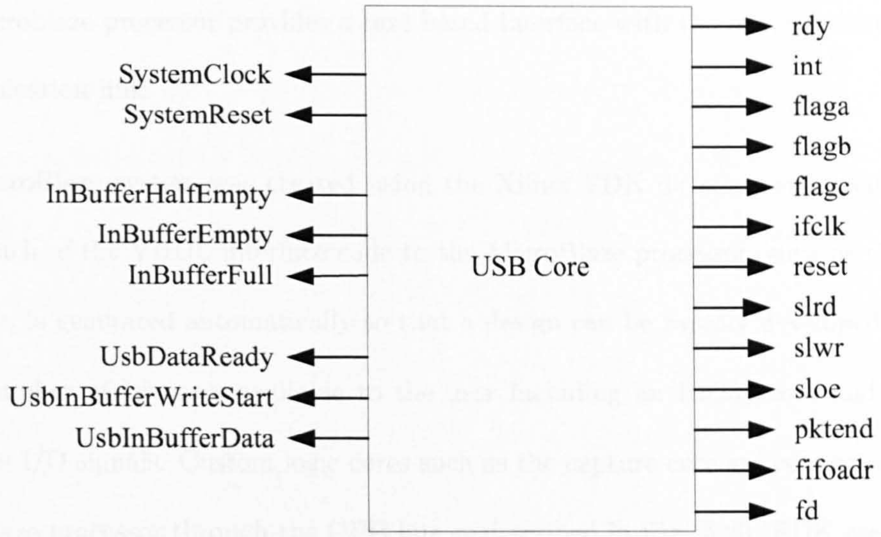


FIGURE 5.28: Diagram of USB core

| Name | Width | Description |
|---|---|---|
| SystemClock | 1 | System clock |
| SystemReset | 1 | System reset |
| InBufferHalfEmpty | 1 | Asserted if the memory buffer on the USB board is half full |
| InBufferEmpty | 1 | Asserted if the memory buffer on the USB board is empty |
| InBufferFull | 1 | Asserted if the memory buffer on the USB board is full |
| UsbDataReady | 1 | Asserted if the USB board is ready to send or receive data |
| UsbInBufferWriteStart | 1 | Used to start sending each packet of USB data |
| UsbInBufferData | 16 | USB data |

TABLE 5.16: Details of GPS capture core core input and output signals

### 5.4.5 MicroBlaze Processor

The MicroBlaze processor forms the heart of the fault recorder system. All the logic cores in the design connect to the MicroBlaze processor via the OPB bus and the processor is responsible for the coordination of the logic cores as well as the control of other low speed devices, such as the SD-card and the DACs, to provide a complete solution.

The Microblaze processor provides a text based interface with the user over the RS232 communication link.

The MicroBlaze system was created using the Xilinx EDK development environment [82]. Much of the VHDL interface code to the MicroBlaze processor, such as the OPB interface, is generated automatically so that a design can be rapidly developed. There are a number of IP cores available to the user including an RS232 core and general purposes I/O signals. Custom logic cores such as the capture core are connected to the Microblaze processor through the OPB bus as described in Fig. 5.20. EDK creates the OPB interface based on the number of registers required by the user, leaving the user to connect the custom logic core to the corresponding registers.

#### 5.4.5.1 Theory of Operation

When the FPGA is powered on, the configuration data for the system is read from the PROM memory and programmed into the FPGA. After a global reset signal the Microblaze program initialises the system. Configuration information regarding the trigger levels for each channel and the amount of samples to record for each transient are stored on the SD-Card. MicroBlaze reads the configuration data and configures the logic cores with the correct parameters before enabling the system. This ensures that in the event of power lost, the FPGA can automatically reconfigure itself once power is restored.

Once the system is enabled, the capture core begins to monitor the ADC data for a transient or for an external trigger event. When an event occurs the capture core writes data to the QDR memory and issues a trigger event signal. The trigger event signal causes the GPS capture core to latch the current time stamp and interrupts the

MicroBlaze processor. When the Microblaze processor receives an interrupt signal it disables the capture core to prevent any further triggering whilst it updates the QDR start address in the capture core with where to start recording the next transient event. The capture core is re-enabled so that it returns to monitoring for the next fault event. When the **rec_done** signal is asserted the MicroBlaze processor reads the transient stored in the QDR memory and records it to the SD-Card. The processor also records the latched time stamp from the GPS capture core to the SD-Card.

The system can also receive inputs from the user via the RS232 communication channel. The system has three modes of operation. When the fault recorder is in test mode, recorded transient events are immediately sent from the QDR memory to the host PC via USB cable link. When the fault recorder is in operational mode (default mode), fault data is recorded to the on-board SD-card so that a host PC is not required to be present. When the system is in retrieve mode the recorded data is read from the SD-card and sent via USB to the host PC. The fault recorder is checked at intervals once installed in the substation or remote location. The system is taken out of operational mode when configuration data needs to be changed or when downloading data from the SD-card via USB to the host PC.

## 5.5 Testing

Behavioral simulation models were performed for each of the logic cores in the design and can be found in Appendix C. All cores simulated with the correct response.

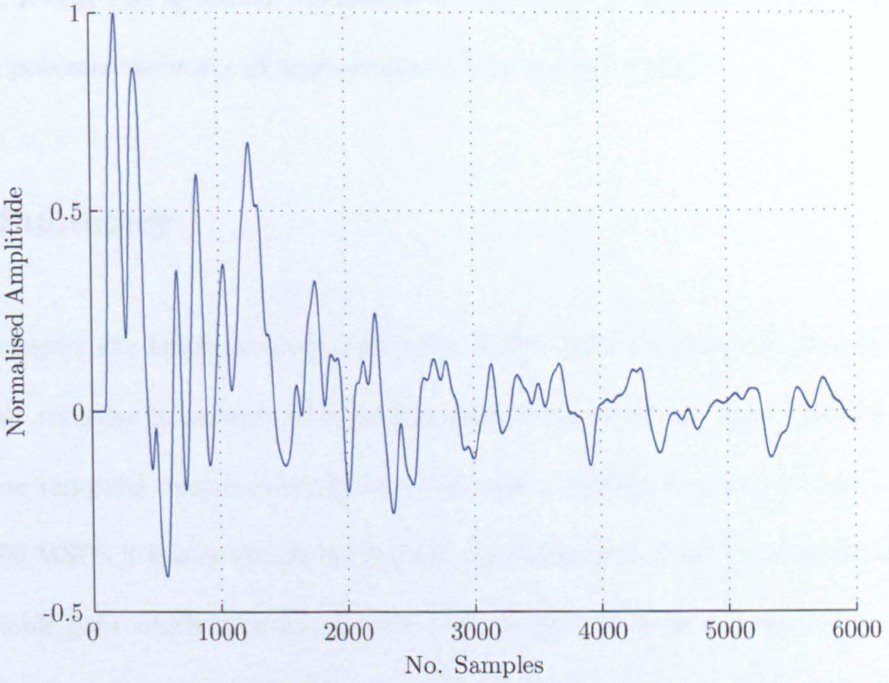
The design was synthesised for both the spartan-3 1500 gate and 4M gate devices. It was found that there was a limit to the maximum sampling frequency that the ADCs could be run at if more than 4 ADCs were included in the design. If five or six ADCs are required then the QDR memory must be run at 1.5 times the clock frequency used for the ADC sampling and both of the QDR memory devices are required. Under these conditions the place and route algorithm was not able to meet all timing requirements. This was partly due to the layout of the QDR memory on the FPGA device which could not be changed. Much effort was made using manual placement methods to try an reduce the clock delay but was unsuccessful. If six ADCs are to be used then the maximum sampling frequency achievable is 26.66 MSPS. If four ADCs are being used then the design meets all timing requirements and the maximum ADC sampling frequency is 40 MSPS.

To test how the system performed to likely fault transient signals an Arbitrary Waveform Generator (AWG) was used to generate an analogue signal based on fault transients from the simulation model of the power network in chapter 4. An example of the simulated and recorded data is shown in Fig.. 5.29.

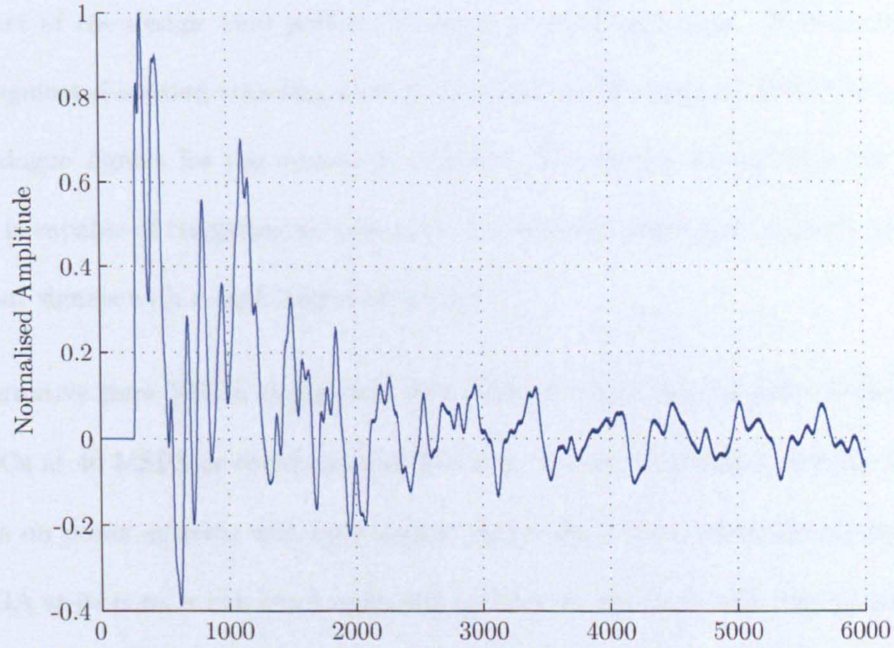
Visual inspection of Fig. 5.29 shows a very high degree of correlation. Similar results were observed for different fault transients. It can be concluded that the FPGA system is capable of faithfully recording the signals from the ADC inputs.

## 5.6 Other Implementations

The reduced sampling frequency of the ADCs which was as a result of an excessive delay on one of the clock signals in the design is avoided if the Microblaze processor is removed from the design. An alternative pure VHDL solution was therefore developed which was able to run all six ADCs at 40 MSPS. The structure of the design was very similar to the Microblaze design in that each of the cores were connected via a 32 bit data bus. However there was no microprocessor in the design so less functionality was achieved.



(a) AWG result



(b) AWG result

FIGURE 5.29: Comparison of simulated data reproduced by an AWG and recorded by FPGA system for a three phase 100 ohm fault at location 2

The SD-card was removed from the design and recorded events were sent directly to the host PC. If only two ADCs are required in the design then they can be run at 80 MSPS giving a potential accuracy of approximately 4 metres per sample.

## 5.7 Summary

In this chapter the hardware design of a new FGPA fault recorder has been described. The fault recorder is capable of recording data from up to six input channels. The maximum sampling frequency of the input signals is 40 MHz for up to 4 input channels and 26.66 MSPS if five or six input channels are being used. Each set of three channels has variable gain which is programmable via the FPGA. Data recorded can either be sent via USB to a host PC or written to SD-card. Behavioural simulation models for each part of the design were perform to ensure correct operation. The recorder was tested against simulated traveling wave fault transients by using an AWG to reproduce the analogue signals for the system to capture. The results showed that the FPGA system is capable of triggering on typical fault transient events and faithfully recording the input signals with a high degree of accuracy.

At alternative pure VHDL design was also realised which was capable of running all six ADCs at 40 MSPS or could run two ADCs at 80 MSPS making it suitable for fault location on power systems with even shorter distribution lines. Since the hardware has an FPGA at its core, it can be reconfigured making the hardware suitable for not only a traveling wave fault recorder, but as a generic high speed data acquisition system. The modular design of the hardware also allows different daughter cards to be designed to extend the functionality of the hardware.

The transducers used to provide signals to the ADCs will be dependent on the situation in which the recorder is deployed. For this reason the discussion of the transducers is reserved for chapter 6 which discusses the deployment of the fault recorder on the CELSEC distribution line.

Although the FPGA data acquisition system was built in collaboration with the applied optics group, the key features developed for this project by the author are as follows:

### 5.7.1 Hardware

The author was responsible for testing of the ADC daughtrer card including the identification of the correct modifications to the PCB layout to improve the ADC performance. The author was also responsible for the design and testing of the front end variable gain board including schematic capture and PCB layout.

### 5.7.2 FGPA

The author was responsible for the individual design of the capture core and GPS capture core. The author was also responsible for the design and implementation of the overall system so that each of the separate cores connected and communicated properly with each other. This included the interfacing of the 40MHz and 60MHz clock domains. The author was responsible for the design and implementation of the overall Microblaze data acquisition system and the design and implementation of the pure VHDL data acquisition system.

### 5.7.3 Software

The author was responsible for designing and implementing the software running on the Microblaze processor which provided the memory address management of the QDR memory and command line driven user interface. The author was also responsible for the design and implementation of software running on the host PC for controlling and receiving data when using the pure VHDL implementation of the data acquisition system.

The testing present in this chapter was also performed by the author. The design of the ADC core and Memory core was done by Hoang Nyguen and the design of the USB core was done by Dr. Yiqun Zhu.

# Chapter 6

# Field tests and Laboratory tests

## 6.1 Introduction

This chapter presents the experimental results used to validate the time tree genetic search fault location algorithm developed in chapter 4. The FPGA based fault recorder developed in chapter 5 was installed in the substation of a major MV distribution line, operated by CELESC, for the town of Pomerode near the city of Blumenau in the Santa Catrina region of Brazil. A number of switching events were captured by the recorder and the design of the triggering mechanism was improved based on the experience of installing the equipment in the substation. It was recognised in chapter 4 that the time tree genetic search algorithm can be applied to a whole range of networks. Therefore a communication line with several branches which represents a similar topology was constructed and a Time Domain Reflectometry (TDR) device was used to acquire the reflection pattern under different fault conditions. The time tree genetic search algorithm was modified so that it was able to locate faults on the communication line.

## 6.2 CELESC Distribution Line

The MV distribution line made available by CELESC for the installation of the fault recorder was a major 23.8 kV distribution line serving the town of Pomerode near the city of Blumenau in the Santa Catarina region of Brazil. Pomerode is a town of approximately 8000 customers and supports a number of large industrial customers. CELESC is particularly interested in developing an accurate fault location scheme for this distribution line because it is particularly vulnerable to permanent fault events due to its radial network topology. When a permanent fault occurs it has a significant impact on a large number of companies and businesses. The one-line diagram of the distribution line is shown in Fig. 6.1.

The distribution line originates at a substation approximately 20 km away from Pomerode. The distribution line is significantly more complex than the one evaluated in chapter 4. The large number of sub feeders that branch off the main line result in the traveling wave patterns becoming too weak to detect unless the fault is located to within six feeder junctions with respect to the observation point. It is not suitable for the single-ended fault location scheme if only one recorder is installed on the network. The bus bar on which the distribution line originates also has another distribution line of similar complexity connected to it. To apply the single-ended fault location scheme both of the distribution lines need to be incorporated into the time tree model because traveling waves will propagate through the bus bar and appear on both lines. It should be appreciated at this stage that urban distribution lines such as this one pose a formidable challenge to any fault location scheme.

There were two locations on the distribution line where fault locators could be installed, one at the substation and the other approximately half way along the line in the town

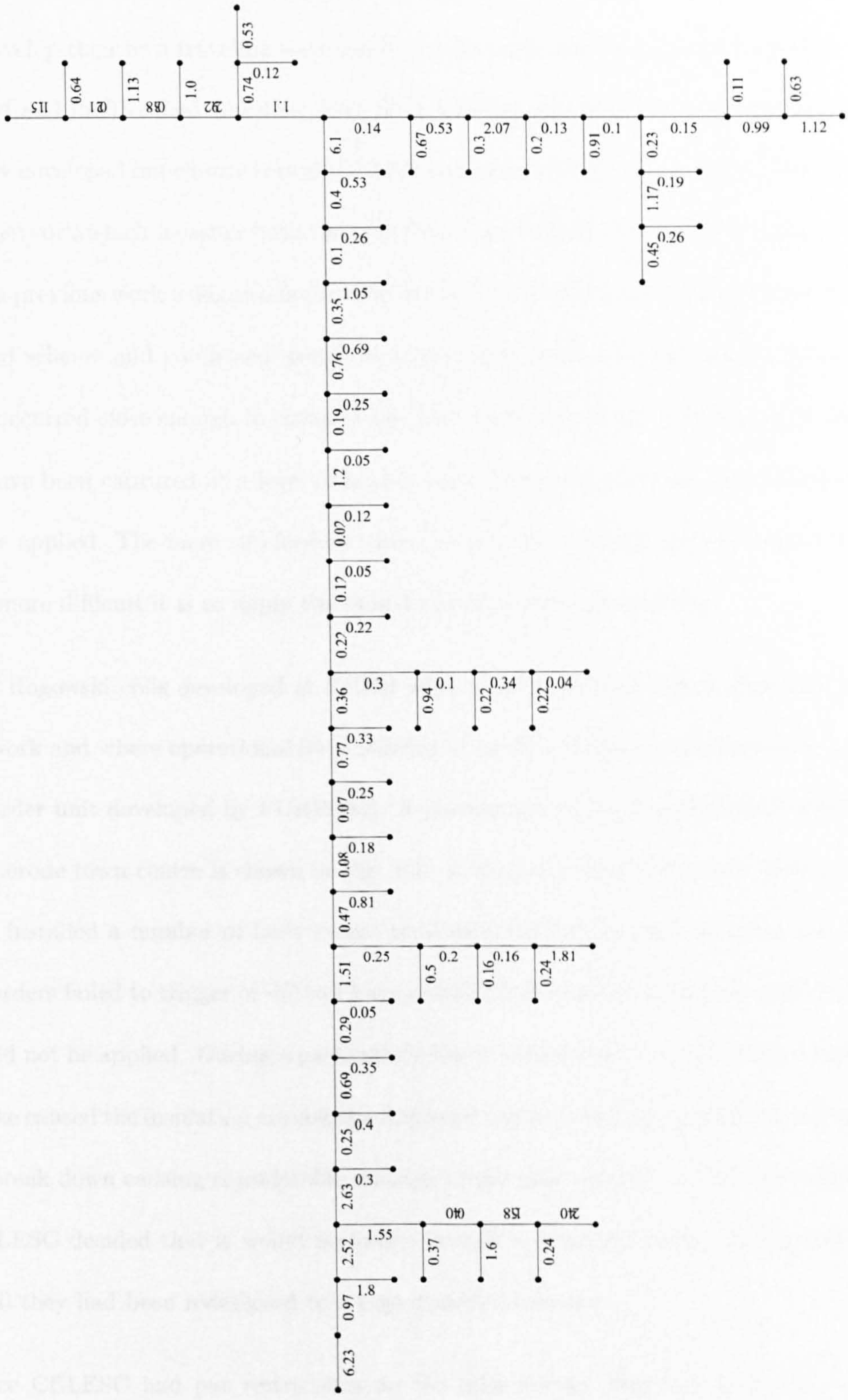


FIGURE 6.1: One-line diagram of Pomerode distribution line

centre of Pomerode. FURB university have been working in collaboration with CELESC to develop their own traveling wave fault recorder and have focused on applying double-ended and multi-ended traveling wave fault location schemes. Their scheme uses some newly developed impedance transducers [83] connected directly to the high voltage side of the network which measure both the high frequency voltage and high frequency current. From previous work using two fault recorders [34], faults can be located using the double-ended scheme and confirmed using the single-ended fault location scheme if the fault has occurred close enough to either of the fault recorders for the traveling wave pattern to have been captured at a level of fidelity high enough for the time tree fault location to be applied. The more sub-feeders there are between the fault and the fault recorder, the more difficult it is to apply the fault location scheme successfully.

The Rogowski coils developed at FURB were installed on the high voltage side of the network and where operational for a number of months. They were connected to a fault recorder unit developed by FURB [84]. A photograph of the Rogowski coil installed in Pomerode town centre is shown in Fig. 6.2. During the months that the fault recorder was installed a number of fault events were detected but on each occasion, one of the recorders failed to trigger or did not have a valid GPS signal so the double-ended scheme could not be applied. During a particularly heavy thunderstorm a surge from a lightning strike caused the insulation around the Rogowski coil installed just outside the substation to break down causing considerable damage to the fault recorder and to the substation. CELESC decided that it would no longer be safe to continue using the Rogowski coils until they had been redesigned to a higher safety standard.

Since CELESC had put restrictions on the high voltage Rogowski coils, only one of the fault recorders developed in chapter 5 was installed. It was located inside the substation with Rogowski coils connected to the secondary wiring of a instrument current

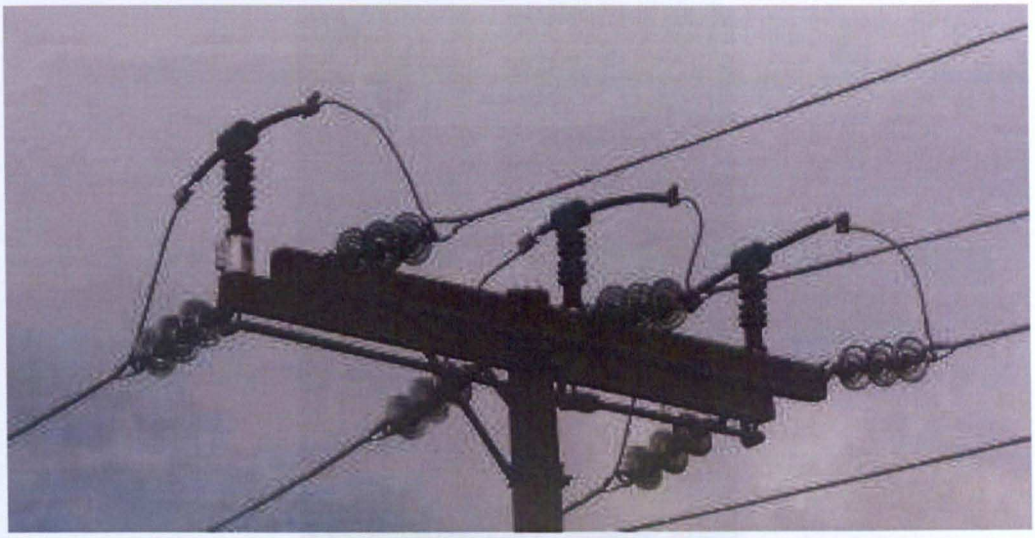


FIGURE 6.2: Photograph of Rogowski coils installed on high voltage side of MV distribution line

transformer, used to monitor the power frequency current of the distribution line. Fig. 6.3 shows a picture of the Rogowski coils connected to the secondary wiring. The Rogowski coils used were supplied by PEM Ltd and have a bandwidth of 17 MHz which is more than ample for use on the distribution line. However the fidelity of the traveling waves is limited by the bandwidth of the instrument current transformer. To establish whether the genetic algorithm was still able to estimate the fault location even when the bandwidth is severely restricted the network described in chapter 4 was evaluated again but this time the traveling wave data from the ATP simulation was low pass filter with a cut-off frequency of 500 kHz to represent the filtering effect of the instrument current transformer. The results are given in Appendix D. The results show that the genetic algorithm can still locate the fault to within an accuracy of 0.5% (30 m) with the exception of single phase faults at the far end of the distribution line where the solution space has a false ridge with a higher value than the ridge corresponding to the fault location.

Rogowski coils are ideally suited to measuring fault traveling wave signals. They have

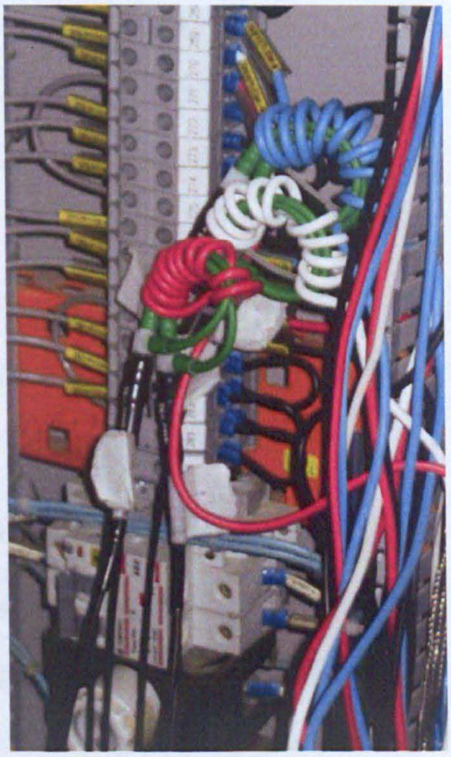


FIGURE 6.3: Photograph of Rogowski coils installed on the secondary wiring of current transformer

a high bandwidth and good linearity due to the absence of magnetic material [85]. The lack of magnetic material also results in non-saturation of the coil under fault currents. A Rogowski coil consists of closely and evenly wound coils of wire on a non-magnetic former. If the coil is a closed loop with no discontinuities then the voltage induced at the output of the coil is proportional to the derivative of the current flowing through the conductor that the Rogowski coil is connected around. It can be shown that the induced voltage is related to the differential of the current in the conductor as:

$$E = S\frac{dI}{dt} \tag{6.1}$$

where $S = 4\pi 10^{-7} NA$ is the coil sensitivity, $N$ is the number of coils and $A$ is the cross-sectional area. In many applications it is necessary to include and integrator on the output of the Rogowski coil to obtain a voltage proportional to the current in the conductor. However, since we wish to exclude the power frequency components, the derivative signal is fed directly to the FPGA and triggering circuitry. The derivative essentially acts as a high pass filter. Any sudden change in current, such as a fault or switching event, causes a large change in the derivative signal which is used to trigger the FPGA. The signal is integrated and post processed in Matlab using Butterworth filters to obtain the traveling wave signature.

The performance of the Rogowski coils and the FPGA were tested at PEM using a SDN coaxial shunt. The coaxial shunt has an impedance of 100 mohm and a bandwidth from DC to 800 MHz. The Rogowksi coil is connected around 15 coil turns of the output cable of the coaxial shunt. The shunt cable is 50 ohm terminated. Fig. 6.4 shows the response of the Rogowski coil to the current pulse. The blue trace is current pulse generated by the coaxial shunt and the yellow trace is the Rogowski coil response. It can be seen from the trace that the Rogowski coil produces a very accurate derivative signal with a very small amount of ringing and overshoot.

It was necessary to wrap the Rogowski coil 10 times around the secondary wiring because the maximum fault current in the secondary wiring was 5A but the Rogowski coil resolution was 1V/50A. The variable gain amplifiers on the front end board were also used to increase the amplitude of the transients signals so that they used the full scale of the ADCs.

The fault recorder was installed in the substation for a one month period between 24/04/2008 and 21/05/2008 [67]. During this period no fault events were registered by the fault recorder although some faults were registered by CELESC during the same period. The reason the fault recorder missed these fault events was because of a large

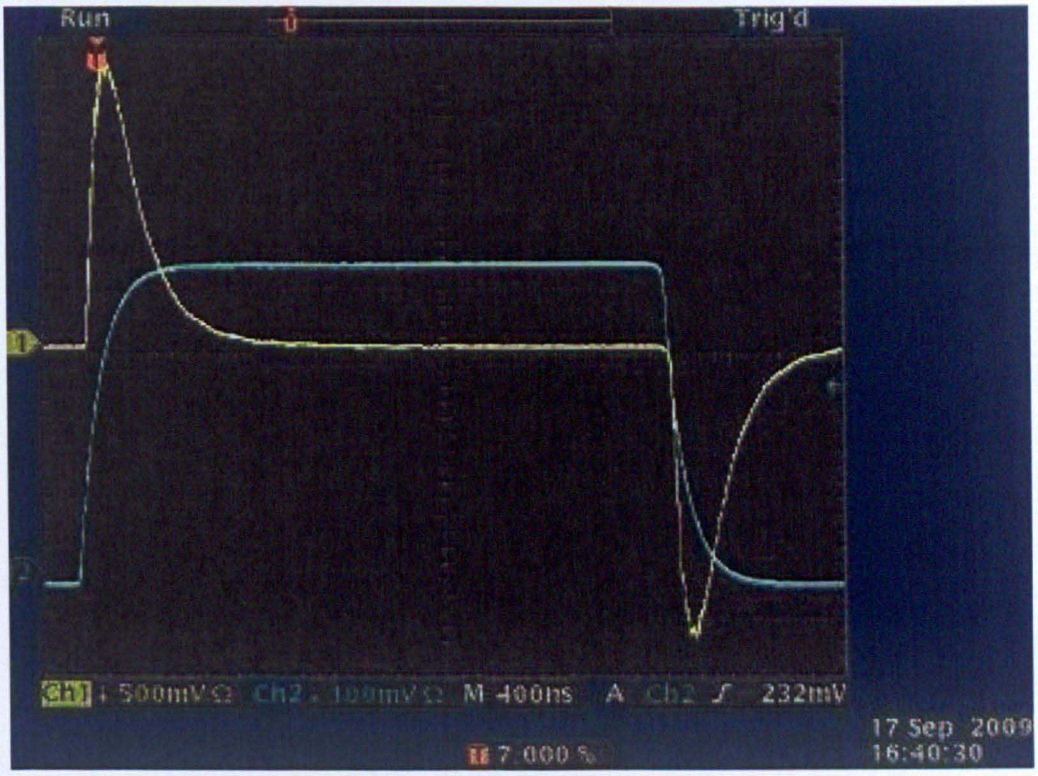
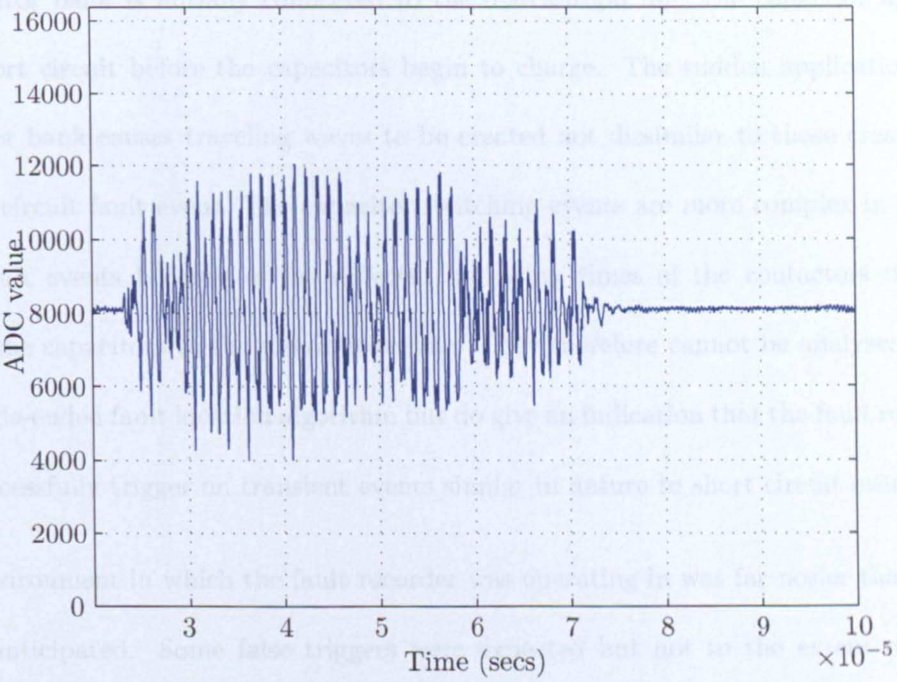


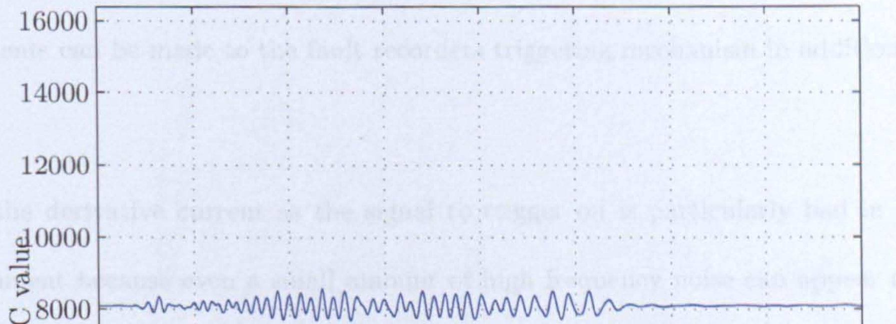
FIGURE 6.4: Response of Rogowski coils to current pulse

number of false triggers which saturated the fault recorder. The false trigger events were caused by pickup on the Rogowski coils from other equipment within the substation. An example of a typical unwanted pickup signal on the Rogowski coil, responsible for the false trigger events, is shown in Fig. 6.5. The event consists of a burst of high frequency energy most probably relating to switching events of other equipment inside the substation. Also shown in Fig. 6.5 is the same signal filtered with a 4 pole low pass Butterworth filter with a cutoff frequency of 500 kHz. The design of the fault recorder was improved to include an IIR filter on the input of the trigger logic core with the same characteristics to suppress the high frequency pickup, however this was only possible after the one month installation period.

During the installation of the fault recorder a number of capacitor switching events were captured such as the one in Fig. 6.6. Capacitor banks are located at different points



(a) Raw data



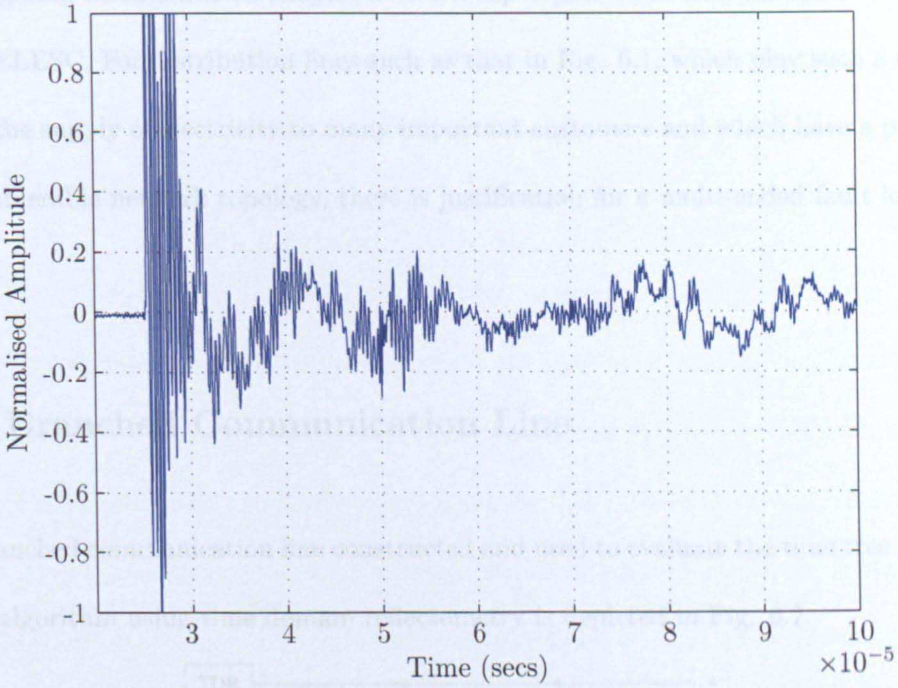
(b) Filtered data

FIGURE 6.5: Example of unwanted pickup signal on Rogowski coil responsible for causing false trigger events

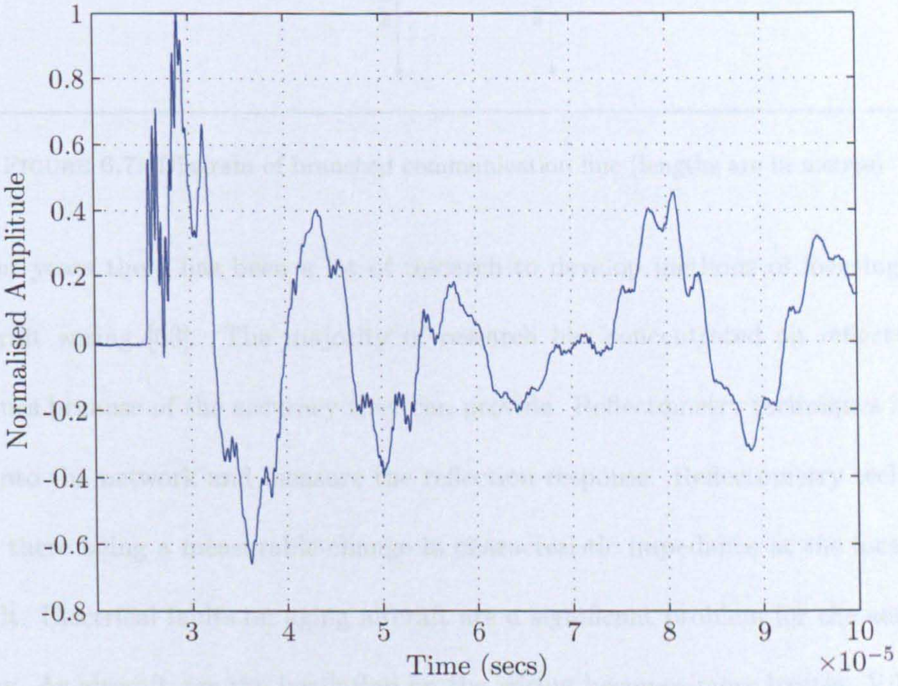
along the distribution line to compensate for reactive power on the network. When a capacitor bank is initially connected to the distribution line, the capacitor appears as a short circuit before the capacitors begin to charge. The sudden application of a capacitor bank causes traveling waves to be created not dissimilar to those created by a short circuit fault event. The capacitor switching events are more complex in nature than fault events because of the different operating times of the contactors used to attach the capacitors to the distribution line. They therefore cannot be analysed using the single-ended fault location algorithm but do give an indication that the fault recorder can successfully trigger on transient events similar in nature to short circuit events.

The environment in which the fault recorder was operating in was far nosier than originally anticipated. Some false triggers were expected but not to the extent of what was experienced. To improve the performance of the fault recorder a number of improvements can be made to the fault recorders triggering mechanism in addition to the filter.

Using the derivative current as the signal to trigger on is particularly bad in a noisy environment because even a small amount of high frequency noise can appear as large changes in the derivative signal. A better solution would be to include an integrator on the output of the Rogowski coil and bandpass filter the integrated signal to only include the frequency content of interest (i.e. 100 kHz - 500 kHz) where the majority of the energy of the traveling wave is located. The band pass filter could either be implemented as part of the FPGA using a digital filter or could be implemented as an additional analogue filter on the front end board. In either case, this signal would only be used as the trigger. The unfiltered output signals of the front-end board would still be the signals recorded by the FPGA and all post processing of the data would be done in Matlab or similar analysis program.



(a) Raw data



(b) Integrated and filtered data

FIGURE 6.6: Example of capacitor switching event captured by fault recorder

The fault recorder will continue to be used in future deployments with improvements to the triggering mechanism on simpler network topologies when they are made available from CELESC. For distribution lines such as that in Fig. 6.1, which play such a crucial role in the supply of electricity to many important customers and which have a particularly vulnerable network topology, there is justification for a multi-ended fault location scheme.

## 6.3 Branched Communication Line

The branched communication line constructed and used to evaluate the time tree genetic search algorithm using time domain reflectometry is depicted in Fig. 6.7.

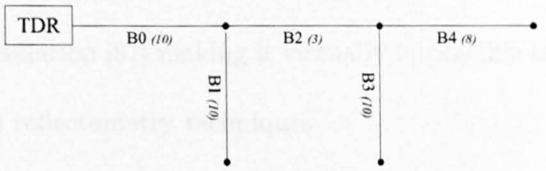


FIGURE 6.7: Diagram of branched communication line (lengths are in metres)

In recent years there has been a lot of research to develop methods of locating faults on aircraft wiring [63]. The majority of research has concentrated on reflectometry techniques because of the accuracy they can provide. Reflectometry techniques inject a signal into the network and measure the reflection response. Reflectometry techniques rely on there being a measurable change in characteristic impedance at the location of the fault. Electrical faults on aging aircraft are a significant problem for the aerospace industry. As aircraft age the insulation on the wiring becomes more brittle. Vibration during operation and the differences between atmospheric conditions during flight and on the ground increase the chance of short circuits, broken wires and frays in insulation [63]. Many of the faults that occur on the aircraft wiring are intermittent faults that only occur during flight. For example, short circuit or broken wire faults may only become apparent as a result of the operational vibration of the aircraft. Arcing faults caused by frays in the insulation may also only occur when the aircraft is under certain load or vibrational conditions. The loss of critical electrical systems or a fire resulting from an electrical fault can have devastating consequences.

Engineers that try to locate faults that have been reported during flight often conclude a no fault found condition because the fault no longer appears as a significant discontinuity in characteristic impedance. There have been a number of suggestions to improve the accuracy of reflectometry techniques so that small changes in the characteristic impedance, such as frays in insulation, can be identified [86]. However, even a slight change in the cables position can change the characteristic impedance enough to mask the reflection caused by a fray in insulation [87] making it virtually impossible to locate the fray using any of the traditional reflectometry techniques.

An alternative approach under development is the continuous monitoring of wiring whilst the aircraft is in operation. During the time in which the fault is active, i.e. before the operation of the circuit breaker, the fault location will appear as a significant impedance discontinuity which can be detected using reflectometry techniques. A number of reflectometry techniques have been proposed, which can be performed without interfering with the normal operation of the cable being monitored. Sequence Time Domain Reflectometry (STDR) [64] and Spread Spectrum Time Domain Reflectometry (SSTDR) [65] are reflectometry techniques which involve injecting a low level pseudo noise binary sequence on to the cable being monitored and correlating the transmitted sequence with the received signal. The PN-sequence is chosen so that it has an autocorrelation of 1 and zero for all other instances, including correlation with a delayed version of itself. The result of the correlation shows peaks at points relating to impedance discontinuities on the cable and represents the impulse response similar to what would be obtained if traditional time domain reflectometry were used. Other examples of online reflectometry techniques include multi carrier reflectometry [88], which involves injecting a signal made up of a selected combination of frequencies, and noise domain reflectometry [89], which is a completely passive technique that uses the self correlation of existing signals on the cable to estimate the impulse response. There are very few examples in the literature where the reflectometry techniques have been applied to branched networks [63].

Time domain reflectometry will be used to evaluate the performance of the time tree genetic algorithm fault location scheme on the branched communication network. An Agilent 54754A TDR device [90] was available for making laboratory measurements. The fault location technique could equally be applied to STDR or SSTDR measurements or any other reflectometry technique that can extract the impulse response of the network.

### 6.3.1 Experimental Setup

The network was constructed out of RG-58 coaxial cable which has a characteristic impedance of 50 ohms and a velocity of propagation equal to 2/3 the speed of light. Three fault locations were chosen to impose short circuit faults as indicated in Fig. 6.7 with fault resistances of 0 ohm, 25 ohm, 50 ohm and 75 ohm. The locations of the faults are detailed in Table 6.1.

| Fault ID | Faulted Branch | Distance from Node 1(m) | Location ID |
|---|---|---|---|
| F1 | B1 | 5 | 1499 |
| F2 | B2 | 1 | 2099 |
| F3 | B4 | 6 | 3899 |

TABLE 6.1: Details of fault locations

The time tree program was modified so that it produced the TDR impulse response instead of the fault impulse response. This was achieved by placing the initial pulse at the node where the TDR device was located instead of the placing the initial pulse at the fault location. The time tree program was modified so that it had a distance resolution of 1 cm which translates to an effective sampling frequency of 20 GSPS.

The Agilent 5475A TDR device used records the step response of the network at a sampling frequency of 1.024 GSPS. The device used was an Agilent . The impulse response was extracted by applying a high pass single pole Butterworth filter with a cut off frequency of 5 MHz in Matlab. The TDR impulse response was re-sampled in Matlab at the same sampling frequency as the time tree program (20 GSPS) so that direct correlation could be made between the recorded impulse response and the time tree impulse response.

The time tree impulse response was created by sample and hold of the ideal impulse response to obtain the step response and then band pass filtered using the same lower cutoff frequency of 5 MHz used to extract the impulse response from the measured TDR response and an upper cutoff frequency of 512 MHz which is half the original sampling frequency of the TDR device.

The TDR device has an output impedance of 50 ohm so a stub resistance of 50 ohm was included in the time tree model at node 0 which is where the TDR device was located in the actual experiment setup. The matched impedance absorbs waves arriving at the TDR device preventing further reflections. For each fault condition, the recorded TDR response was compared with the time tree response and the correlation coefficient calculated. The solution space for each of the fault conditions was calculated in a similar fashion to chapter 4. Each location on the network was given a unique ID so that it was possible to plot the whole solution space on one graph. Details of the location IDs for each branch is given in Table 6.2 and the location ID for each fault is given in Table 6.1.

| Branch ID | Branch Length (m) | Location ID range |
|---|---|---|
| B0 | 10 | 0-999 |
| B1 | 10 | 1000-1999 |
| B2 | 3 | 2000-2299 |
| B3 | 10 | 2300-3299 |
| B4 | 8 | 3300-4099 |

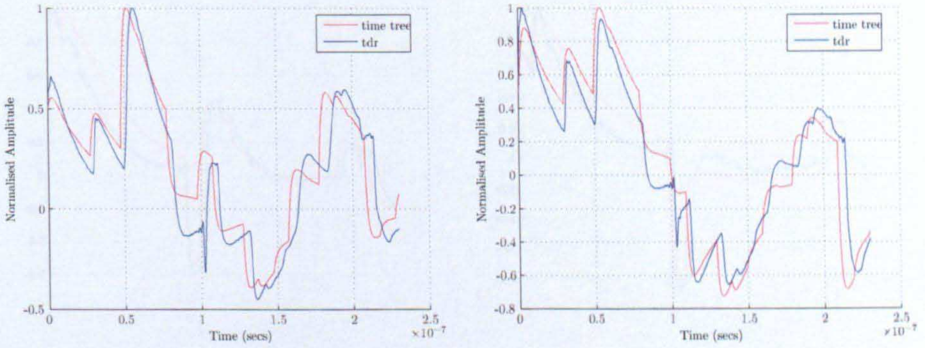
TABLE 6.2: Details of branched communication line

### 6.3.2 Results

A comparison of the TDR response for the branch network made from RG-58 coaxial cable and the time tree simulation is shown in Fig 6.8, Fig. 6.9 and Fig. 6.10 for each fault condition. A summary of the correlation coefficients are given in Table 6.3.

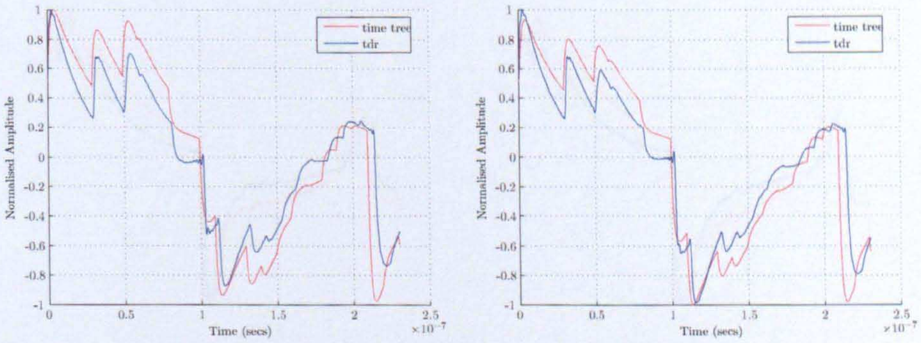
| Fault ID | Fault Resistance | Correlation Coefficient |
|---|---|---|
| F1 | 0 | 0.87 |
| F1 | 25 | 0.94 |
| F1 | 50 | 0.94 |
| F1 | 75 | 0.94 |
| F2 | 0 | 0.93 |
| F2 | 25 | 0.92 |
| F2 | 50 | 0.93 |
| F2 | 75 | 0.93 |
| F3 | 0 | 0.87 |
| F3 | 25 | 0.93 |
| F3 | 50 | 0.93 |
| F3 | 75 | 0.93 |

TABLE 6.3: Correlation coefficients for faults on RG-58 coaxial cable branched network



(a) 0 ohm

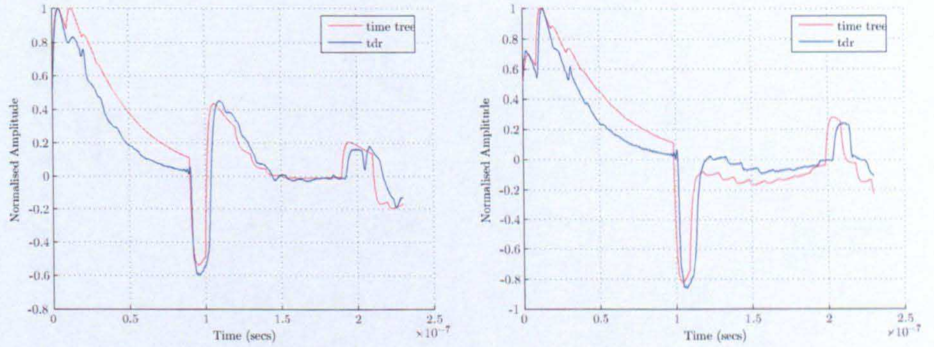
(b) 25 ohm



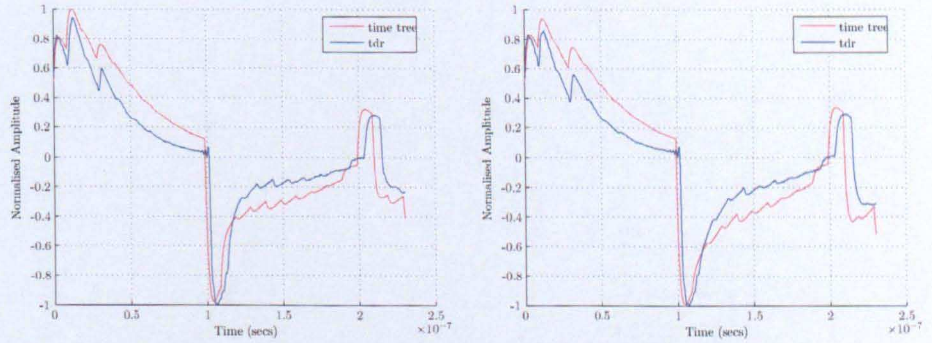
(c) 50 ohm

(d) 75 ohm

FIGURE 6.8: Comparison of measured TDR response and time tree simulation for fault location 1

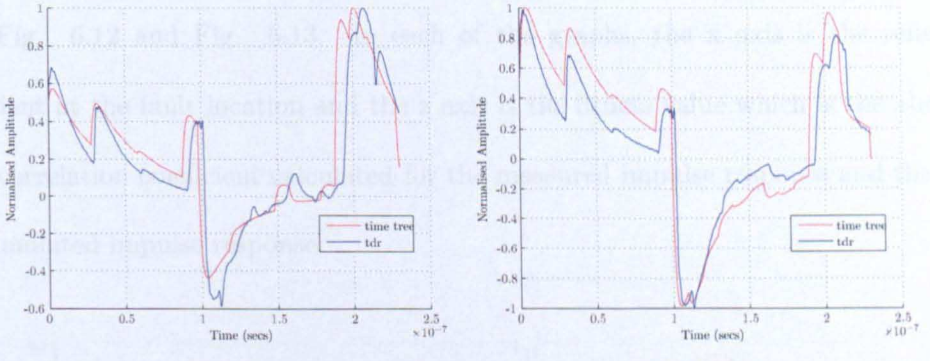


(a) 0 ohm (b) 25 ohm

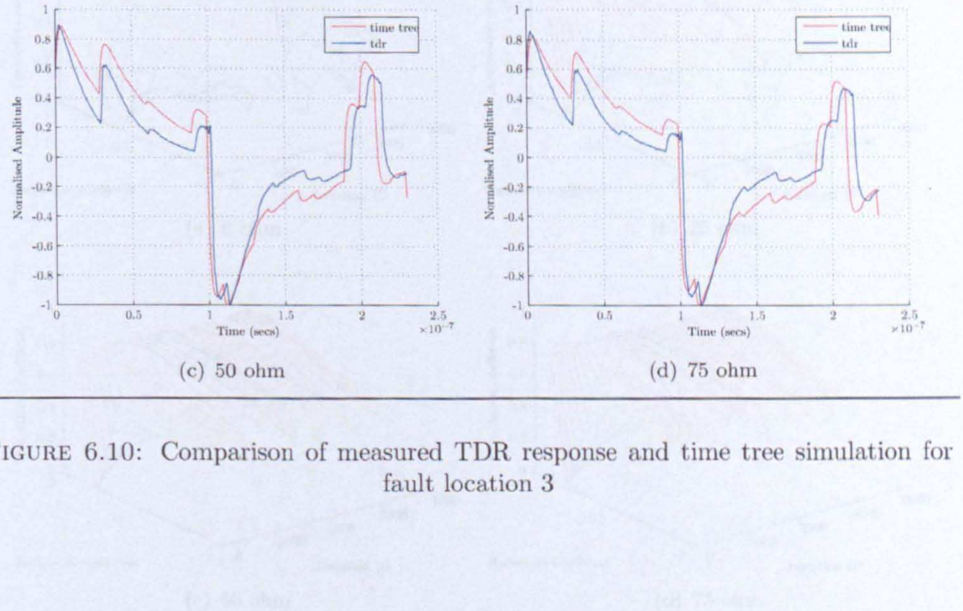


(c) 50 ohm (d) 75 ohm

FIGURE 6.9: Comparison of measured TDR response and time tree simulation for fault location 2



(a) 0 ohm (b) 25 ohm

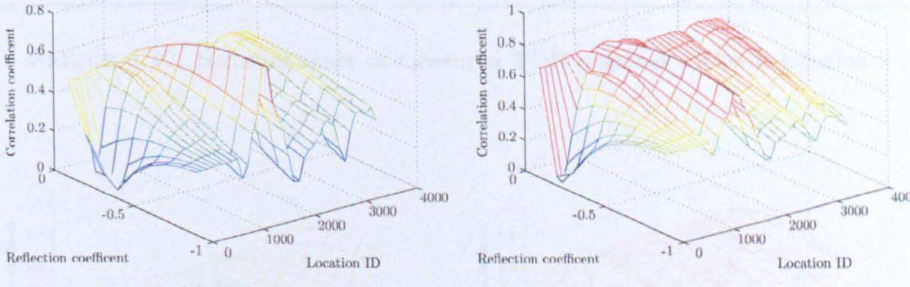


(c) 50 ohm (d) 75 ohm

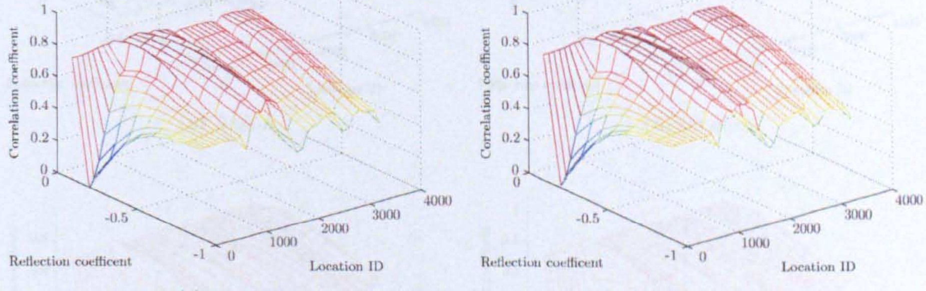
FIGURE 6.10: Comparison of measured TDR response and time tree simulation for fault location 3

From visual inspection of the graphs and the correlation coefficients in Table 6.3 it can be seen that there is a high degree of correlation between the time tree prediction and the measured TDR response for all fault conditions. The differences result from the fact that attenuation and distortion of the traveling waves are not modeled in the time tree analysis.

The solution spaces for each fault conditions on the RG-58 network are shown in Fig. 6.11, Fig. 6.12 and Fig. 6.13. In each of the graphs, the x axis is the reflection coefficient at the fault location and the z axis is the fitness value which is the absolute value correlation coefficient calculated for the measured impulse response and the time tree simulated impulse response.



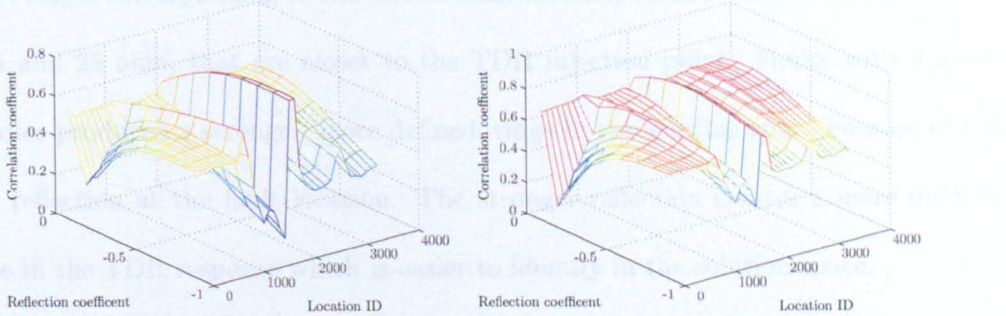
(a) 0 ohm (b) 25 ohm



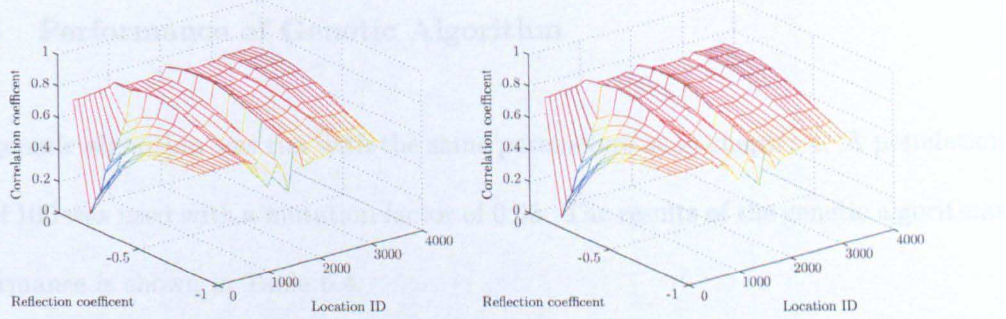
(c) 50 ohm (d) 75 ohm

FIGURE 6.11: Solution space of measured TDR response for fault location 1 for real fault resistances 0, 25, 50 and 75 ohm

Fault locations 1 and 2 are both one branch junction away from the TDR injection point and fault location 3 is two branch junctions away from the TDR injection point. The

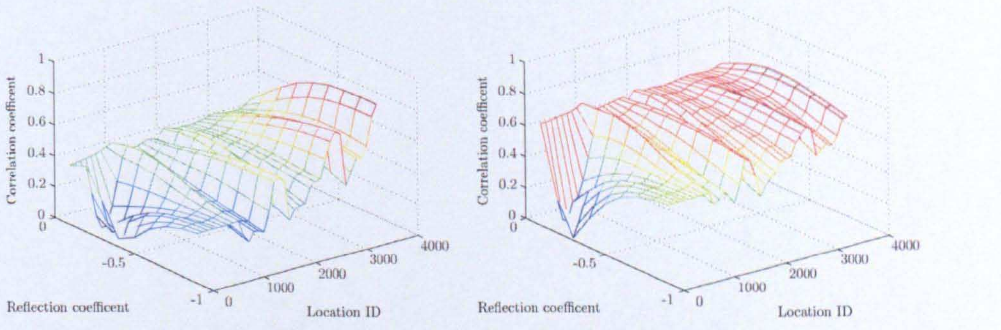


(a) 0 ohm (b) 25 ohm

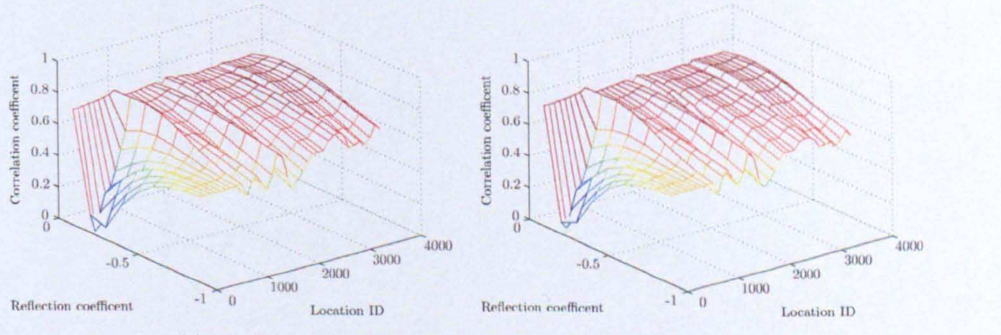


(c) 50 ohm (d) 75 ohm

FIGURE 6.12: Solution space of measured TDR response for fault location 2



(a) 0 ohm (b) 25 ohm



(c) 50 ohm (d) 75 ohm

FIGURE 6.13: Solution space of measured TDR response for fault location 3

clearest ridges corresponding to the correct fault location occur for low resistance faults, 0 ohm and 25 ohm, that are closet to the TDR injection point. Faults with a lower resistance produced a stronger, more defined, ridge in the solution space because of the larger reflection at the fault location. The stronger reflection creates a more distinct change in the TDR response which is easier to identify in the solution space.

### 6.3.3 Performance of Genetic Algorithm

The genetic algorithm was run with the same parameters as in chapter 4. A population size of 100 was used with a mutation factor of 0.05. The results of the genetic algorithms performance is shown in Table 6.4.

| Fault | Resistance | Branch | Distance (cm) | Reflection | Correlation | Branch Error | Distance Error (%) | Reflection Error (%) |
|---|---|---|---|---|---|---|---|---|
| F1 | 0 | 1 | 509 | -0.85 | 0.904707 | pass | 0.60 | 15 |
| F1 | 25 | 1 | 510 | -0.55 | 0.94317 | pass | 0.67 | 5 |
| F1 | 50 | 1 | 505 | -0.33 | 0.942322 | pass | 0.33 | 0 |
| F1 | 75 | 0 | 950 | -0.21 | 0.94282 | fail | n/a | n/a |
| F2 | 0 | 2 | 95 | -0.91 | 0.939671 | pass | 0.45 | 9 |
| F2 | 25 | 2 | 129 | -0.66 | 0.92629 | pass | 2.64 | 16 |
| F2 | 50 | 2 | 128 | -0.36 | 0.939298 | pass | 2.55 | 3 |
| F2 | 75 | 2 | 137 | -0.31 | 0.934534 | pass | 3.36 | 6 |
| F3 | 0 | 4 | 685 | -0.84 | 0.922058 | pass | 4.47 | 16 |
| F3 | 25 | 3 | 805 | -0.63 | 0.919793 | fail | n/a | n/a |
| F3 | 50 | 4 | 644 | -0.47 | 0.937243 | pass | 8.21 | 14 |
| F3 | 75 | 4 | 637 | -0.28 | 0.933987 | pass | 8.57 | 3 |

TABLE 6.4: Performance of Genetic Algorithm on Branched Network using TDR Analysis

In the large majority of cases the genetic algorithm identified the correct branch where the fault was located and found the correct location with less than 2 % error which translates to a distance of 46 cm. The occasions when it failed to find the correct location related to either high impedance faults or faults that are in the furthest zone from the injection pont. There is no clearly defined ridge in the solution space for high impedance faults so the GA is likely to converge on one of a large range of possible solutions.

### 6.3.4 Limitations

The extend to which traditional TDR responses can be used with time tree analysis to locate faults on branched wire networks is limited by the number of consecutive branches, the resistance of the fault, and the attenuation and distortion of the TDR signal caused by the cable. Recall from chapter 4 that the number of junctions that exist between the observation point and the fault location has the greatest impact on the ability to detect the individual wavefronts. Every time a traveling wave is transmitted through a junction of three similar transmission lines its amplitude is reduced by 2/3. It was found through experiment that it was difficult to detect a fault that was more than three branch junctions away from the injection point using the TDR device available in the laboratory because the waves have to travel twice this distance i.e. from the injection point to the fault and then back to the injection point. This therefore puts a limit on the complexity of the network that the time tree analysis can be applied to. Careful positioning of the TDR injection point could increase the number of consecutive branches in the network. If the injection point was chosen in the middle of the network, there could be three consecutive branches in one direction and three consecutive branches in the other direction. On a real system however it may not by possible to insert a TDR device in the middle of a network. One of the drawbacks of traditional TDR is that the steep step voltage that is injected into the network has a wide bandwidth. The higher frequency components are attenuated and dispersed more rapidly making it difficult to determine the correct arrival time of the reflected pulses. Other reflectometry techniques such as SSTDR may perform better because it has a narrower bandwidth. Alternatively the time tree program could be improved to try and approximate the attenuation and dispersion effects. When applying the time tree analysis to overhead lines the amount of attenuation and dispersion is relatively small because the surrounding medium is air and the conductors are spread far apart when compared with the diameter of the conductors. The same cannot be said for most cable configurations where conductors are bundled together and the surrounding medium is a dielectric. Under these circumstances attenuation and dispersion is more acute. The level of attenuation and distortion in coaxial cable is relatively low when compared with other non-impedance controlled cables which is why the time tree in this case has provided a reasonable approximation.

When the time tree analysis technique was applied to fault generated traveling waves in chapter 4 it was able to locate high impedance faults with a similar success rate to low impedance faults. This was because the injection point changed depending on where the fault was located which gave rise to large changes in the reflection pattern. Since correlation is performed on the whole fault signature, the location of other waves in the fault signature play a large role in determining the fault location. With TDR analysis, the injection point remains constant. Low impedance faults still cause a significant change in TDR response that can be detected but high impedance faults that are larger than the cable impedance produce less distinct responses which is why in the solution spaces in Fig. 6.11 to Fig. 6.13 high impedance faults have less of a distinct ridge at the correct fault location. The effect is exacerbated the more junctions there are between the observation point and the fault location.

## 6.4 Summary

In this chapter experimental results were obtained to test the time tree genetic search algorithm. The new high speed traveling wave fault recorder developed in chapter 5 was deployed on a MV distribution line in Brazil. The complexity of the distribution line was far beyond the fault finding capabilities of the time tree algorithm because of the number of sub-feeders that branched off the network. The fault recorder suffered from many false trigger events which flooded the memory card with unwanted data resulting in actual fault events being missed. The triggering mechanism has since been improved to reduce the amount of false triggers.

A branched communication line was constructed and a TDR device was used to evaluate the performance of the time tree search algorithm. Three fault locations were investigated with fault resistances ranging from 0 to 75 ohm. It was found in the majority of cases that the genetic algorithm identified the correct branch where the fault was located and to within less than 46 cm of the actual location.

# Chapter 7

# Conclusions

## 7.1 Introduction

Fault location methods can be categorised into impedance based, traveling wave based and knowledge based techniques. Traveling wave based techniques offer, potentially, the most accuracy. They can either be implemented as double or multi ended schemes, where syncronised measurements are taken at more than one location on the distribution line, or implemented as a single-ended scheme, were measurements are taken from one location only. The double and multi-ended schemes identify the arrival time of the initial traveling waves at two or more locations to estimate the fault location whereas the single ended scheme estimates the fault location by identifying the time between the initial traveling wave and the wave reflected from the fault.

The advantages of the single ended scheme are that it does not require syncronised measurements to be taken and does not require a communication channel. The challenge of traditional single-ended fault location is to correctly and reliably identify the wave reflected from the fault location. On a radial distribution line this is particularly difficult because there are many points of reflection resulting from sub-feeders that branch off the main line. It is very hard to differentiate between waves reflected from the fault and other reflected waves using traditional correlation techniques.

In this thesis a different approach was taken to single-ended fault location by considering the traveling wave 'fault signature' as a whole, rather than trying to identify the first individual reflected wave from the fault. It was assumed that each fault location produced a traveling wave signature that was unique enough to differentiate it self from other fault locations. The obvious exception to this assumption is if the radial network has symmetry, however, this can be considered a special case rather than the norm.

## 7.2 Time Tree Genetic Search Algorithm

The interaction of traveling waves on a distribution line that has several sub-feeders is a complex one. Since there are many routes a traveling wave can propagate along, both positive and destructive interference of the waves can occur. Analysing the relative positions of each wave in the fault signature deterministically becomes complex. Therefore a different approach based on a genetic search algorithm was used.

A genetic algorithm takes a heuristic approach to find the optimal fault location. It seeks out the optimum solution to a problem using the mechanics of natural selection. Genetic algorithms have been shown to be efficient at finding the optimum solution to complex problems.

For the genetic search algorithm to work efficiently, a method for predicting the traveling wave fault signature for many different fault locations in quick succession was required.

Time tree analysis uses the principle of the Bewley lattice diagram and points of reflection in the network to keep track of all the traveling waves following a disturbance. It was shown that time tree analysis exhibits a high degree of correlation (above 90% in the majority of cases considered) with the traveling wave pattern simulated using ATP. The advantage of time tree analysis is the speed at which the traveling wave pattern can be simulated and the ease at which the time tree can be reconfigured to represent a different fault condition.

An autonomous time tree genetic search algorithm was developed in chapter 4 and was evaluated against a branched distribution line simulated using ATP. Four fault locations were investigated to determine how well the search algorithm performed for close up faults, far end faults, faults near the half way point and faults on sub-feeders. For each location, four fault resistances ranging from 0 to 1000 ohm were investigated. Three phase faults, phase to phase faults and single phase faults were considered. The time tree simulation results and the ATP simulation results were compared with each other by calculating the correlation coefficient for a window length equal to twice the distance from the observation point to furthest location on the network. The absolute value of the correlation coefficient was used as the fitness function of the genetic search algorithm.

For each of the traveling wave fault signatures investigated the solution space of the genetic algorithm was calculated. It was shown that there was a ridge in the solution space corresponding to the correct fault location for all fault conditions considered. The genetic algorithm converged on the correct fault location to within 30 m or better which translates to just under 0.5 % of the total line length. The genetic algorithm worked consistently over all fault resistance values showing that the fault location scheme is not limited by high resistance faults.

The genetic algorithm was also able to correctly locate single phase faults on the network even though the ground mode propagation was not modeled in the time tree simulation. The effect that the ground mode propagations had on the traveling wave pattern could be crudely represented by the time tree as a large resistance in series with the fault resistance. There was a maximum in the solution space corresponding to the correct fault location and the genetic algorithm was able to find it.

## 7.3 Fault Recorder

In chapter 5 a new FPGA based high speed data acquisition board was developed suitable for capturing traveling wave data on distribution lines. The recorder is capable of capturing data from six ADCs at a maximum sampling frequency of 40 MSPS which is four times higher than the original objective. If only two ADCs are required, a sampling frequency of 80 MSPS can be achieved. The high sampling frequency and reconfigurability of the FPGA device means this generic high speed data acquisition board can be used in a variety of tasks other than capturing traveling wave data. The modular design allows other input/output cards such as DAC, LAN connection, etc. to be developed to further extend its functionality. Laboratory tests with an arbitrary waveform generator confirmed that the ADCs could faithfully recorded the analogue signals at their input.

## 7.4 CELSEC distribution Line

The FPGA based fault recorder was installed on a distribution line in Brazil operated by CELESC. The complexity of the distribution line, combined with the one month installation period, made the chance of capturing a fault event which could be analysed using the time tree genetic algorithm a very ambitious task. It is therefore not surprising that a fault event was not captured.

The original plan was to use Rogowski coils connected to the high voltage side of the distribution line to capture the traveling waves at a higher fidelity. This was not possible due to safety concerns so the traveling waves were extracted by connecting Rogowski coils to the secondary of an instrument current transformer. It was shown in Appendix D that the genetic algorithm could still locate the correct location of the fault on the example network in chapter 4 even if the traveling waves were low pass filter with a cut-off frequency of 500 kHz with the exception of single phase faults at the far end of the line. This in theory would mean that there is still sufficient fidelity in the traveling wave pattern even after the filtering effect of the current instrument transformer to perform accurate fault location.

The chance of success could have been greatly improved if a more sophisticated triggering mechanism had been implemented that was able to better discriminate false trigger events. The amount of false trigger events from electromagnetic interference within the substation was far worse than was initially anticipated and highlights the difficulties of trying to capture short high frequency events within a noisy environment. The shortcomings of the trigger mechanism have since been addressed and it is hoped that in the future that it will be possible to capture traveling wave data from a distribution line with a simpler topology.

## 7.5 Branched Communication Line

A branched communication line made from RG-58 coaxial cables was constructed and used to evaluate the performance of the time tree genetic search algorithm. Instead of using fault generated waves, a time domain reflectometry device was used to inject a high frequency pulse into the communication line and the subsequent reflection pattern was recorded. Three fault locations were evaluated with fault resistances ranging from 0 to 75 ohm. The time tree predictions showed very strong correlation with the recorded TDR response, above 90% in most cases. This goes someway to verify that the time tree analysis is a good representation of real world measurements however this must also be confirmed with fault generated traveling waves.

For each of the fault conditions investigated, the whole solution space of the genetic algorithm was calculated. The ridge in the solution space corresponding to the correct fault location was most pronounced for low resistance faults because the strong reflection at the fault location causes the most noticeable change in the reflection pattern.

When fault generated traveling waves are used to locate the fault, the injection point of the traveling waves changes depending on the fault location. When TDR analysis is being used, the injection point remains the same. The TDR response for high resistance faults above the cable impedance result in only small changes in the reflection pattern and is why the corresponding solution spaces do not have well defined ridges corresponding to the correct fault location.

## 7.6 Suggestion for Further Work

Although a considerable amount of time was spent developing a new traveling wave fault recorder to capture the fault signature at a higher fidelity it was unsuccessful in capturing any fault events. Shortcomings with the triggering mechanism have since been addressed and it is hoped in future deployments that it will be capable of capturing fault events which can be analysed using the time tree method. The time tree genetic algorithm could also be applied to transmission networks as a complement to the double-ended scheme.

Further investigation is needed into how well the time tree prediction compares to traveling waves that have propagated on underground cables. The velocity of propagation is slower on cables but more importantly, the effect of attenuation and dispersion is greater. An approximation to the attenuation and dispersion may need to be included if the distribution line consists of sections of underground cable. The time tree model could also be extended to the three phase case and represent the ground mode propagations. This will increase the computational burden and increase the time taken to estimate the fault location.

The signal analysis of traveling wave patterns in this thesis has focused on the time domain representation. This has worked well in the majority of simulated cases but the reality of working with a real distribution line has highlighted that the quality of the captured traveling wave pattern is likely to be corrupted by noise. Using analysis techniques such as wavelet analysis to extract features of the wave before applying genetic search techniques may provide improved performance in a noisy environment.

# Appendix A

# Traveling Wave Theory

## A.1 The Transmission Line Equation

The behaviour of traveling waves on transmission lines are governed by telegraphers equations [38, 91]. The voltage and current on a uniform two conductor transmission line depicted in Fig. A.1 can be expressed using the telegraphers equations as:

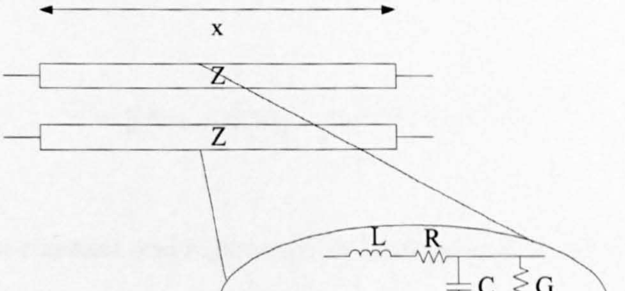


FIGURE A.1: Diagram of a loss-less uniform two conductor transmission line

$$\frac{dV}{dx} = -(R + j\omega L)I \tag{A.1}$$

$$\frac{dI}{dx} = -(G + j\omega C)V \tag{A.2}$$

where $L$, $C$, $R$ and $G$ are the transmission line inductance, capacitance, resistance and conductance per unit length. Differentiating equation (A.1) with respect to $x$ gives:

$$\frac{d^2V}{dx^2} = (R + j\omega L)(G + j\omega C)V \tag{A.3}$$

the general solution to equation(A.3) has the form:

$$V(x) = Ae^{-\gamma x} + Be^{\gamma x} \tag{A.4}$$

$V(x)$ consists of two components, one that travels in the direction $x$ and the other traveling in the opposite direction. The term $\gamma$ is known as the propagation constant and is equal to:

$$\gamma = [(R + j\omega L)(G + j\omega C)]^{\frac{1}{2}} = \alpha + j\beta \tag{A.5}$$

$\alpha$ is the attenuation constant and represents the amount of attenuation a traveling wave experiences as it propagates and $\beta$ is the phase constant and represents the amount of phase shift a traveling wave experiences as it propagates. The propagation constant on overhead lines also has a frequency dependence due to the skin effect. At higher frequencies the current only propagates on the edge of the conductor effectively reducing the cross sectional area. Higher frequency waves are attenuated more than lower frequency waves because of the difference in effective cross-sectional area. At the frequency range of traveling waves all propagation occurs on the skin of the conductor and the attenuation and dispersion are influenced more by the conductor spacing and the permittivity and permeability of the surrounding medium.

Substitution of equation(A.4) into equation (A.2) gives:

$$I(x) = Z_0^{-1}[Ae^{-\gamma x} - Be^{\gamma x}] \tag{A.6}$$

where $Z_0$ is defined as:

$$Z_0 = \sqrt{\frac{(R + j\omega L)}{G + j\omega C)}} \tag{A.7}$$

For overhead transmission lines, where the conductor spacing is much greater than the diameter of the conductor, the line resistance and leakage conduction have negligible influence on the result. The voltage and current for a loss-less transmission line can be expressed in the time domain as:

$$\frac{\partial v(x,t)}{\partial x} = -L\frac{\partial i(x,t)}{\partial t} \tag{A.8}$$

$$\frac{\partial i(x,t)}{\partial x} = -C\frac{\partial v(x,t)}{\partial t} \tag{A.9}$$

Differentiating equation (A.8) with respect to $x$ and equation (A.9) with respect to $t$ gives:

$$\frac{\partial^2 v(x,t)}{\partial x^2} = LC\frac{\partial^2 v(x,t)}{\partial t^2} \tag{A.10}$$

Differentiating equation (A.9) with respect to $x$ and equation (A.8) with respect to $t$ gives:

$$\frac{\partial^2 i(x,t)}{\partial x^2} = -LC\frac{\partial^2 i(x,t)}{\partial t^2} \tag{A.11}$$

The general solution for the loss-less wave equations in the time domain expresses $v(x,t)$ and $i(x,t)$ in terms of forward and backward traveling waves as:

$$v(x,t) = \frac{1}{2}[F_1(ut-x) + F_2(ut+x)] \tag{A.12}$$

$$i(x,t) = \frac{1}{2Z_s}[F_1(ut-x) - F_2(ut+x)] \tag{A.13}$$

where $u$ is the surge velocity of the wave and $Z_s$ is the surge impedance of the line. $F_1$ and $F_2$ represent waves that travel in opposite directions from the point of disturbance. $F_1$ and $F_2$ are arbitrary functions used to represent the traveling waves. $F_1$ travels in the same direction as the defined positive $x$ direction and $F_2$ travels in the negative $x$ direction. The surge velocity is related to the inductance and capacitance per unit length of the transmission line as [92]:

$$u = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{\mu\epsilon}} \tag{A.14}$$

The inductance and capacitance per unit length of a transmission line are a function of the diameter of the conductor and spacing between conductors [92]. The surge impedance $Z_s$ of the line increases with conductor spacing and decrease in conductor diameter [39]. It can been observed from equation (A.14) that the velocity of propagation is unaffected by the conductor geometry and depends only on the magnetic permeability and electric permittivity of the surrounding medium. For overhead transmission lines, where the surrounding medium is air, the waves propagate at approximately the speed of light.

If a constant observation point $x$ and constant propagation speed $u$ is assumed then equations (A.12) and (A.13) can be rearranged in terms of their forward and backward traveling waves as:

$$S_1(t) = v(t) + Z_s i(t) \tag{A.15}$$

$$S_2(t) = v(t) - Z_s i(t) \tag{A.16}$$

where $S_1$ describes the forward traveling waves and $S_2$ describes the backward traveling waves.

## A.2 Multi-Phase Transmission Lines

On a practical three phase system, traveling waves propagate through the conductors and through the ground if the fault has a conduction path to earth. Traveling waves which propagate through the conductors, do so at a velocity close to the speed of light. Traveling waves which propagate through the ground, do so at a speed significantly less than the speed of light because of the difference in the permittivity and permeability of the ground medium. Ground mode signals also suffer more attenuation because of the relatively poor conductivity of the ground. Unless the transmission line is ideally transposed, the amount of attenuation for each aerial mode will be different depending on which conductor the traveling wave propagated down. Telegraphers partial differential equations for a multi-phase transmission line can be written in matrix form as [39]:

$$\frac{d[V_{ph}]}{dx} = -[Z_{ph}][I_{ph}] \tag{A.17}$$

$$\frac{d[I_{ph}]}{dx} = -[Y_{ph}][V_{ph}] \tag{A.18}$$

where $[V_{ph}]$ is the phase voltages, $[I_{ph}]$ is the phase currents and $[Z_{ph}]$ and $[Y_{ph}]$ are the phase impedance and admittance matrices respectively. Differentiating equations (A.17) and (A.18) and substituting gives:

$$\frac{d^2[V_{ph}]}{dx^2} = [Z_{ph}][Y_{ph}][V_{ph}] \tag{A.19}$$

$$\frac{d^2[I_{ph}]}{dx^2} = [Y_{ph}][Z_{ph}][I_{ph}] \tag{A.20}$$

The phase voltage and phase currents can be decoupled into independent modal components using model transform matrix:

$$[V_{ph}] = [S][V_m] \tag{A.21}$$

$$[I_{ph}] = [Q][I_m] \tag{A.22}$$

where $[V_m]$ is the modal voltage matrix and $[I_m]$ is the modal current matrix. $[S]$ is the modal voltage to phase voltage transform matrix and $[Q]$ is the modal current to phase current matrix. The modal impedance matrix can also be calculated as:

$$[Z_m] = [S]^{-1}[Z_{ph}][Q] \tag{A.23}$$

Equations (A.19) and (A.20) can be expressed in terms of their modal components as:

$$\frac{d^2[V_m]}{dx^2} = [S]^{-1}[Z_{ph}][Y_{ph}][V_{ph}] = [\gamma^2][V_{ph}] \tag{A.24}$$

$$\frac{d^2[I_m]}{dx^2} = [Q]^{-1}[Y_{ph}][Z_{ph}][I_{ph}] = [\gamma^2][V_{ph}] \tag{A.25}$$

The matrices $[S]$ and $[Q]$ are chosen to diagonalize $[\gamma^2]$. For a fully transposed balanced three-phase transmission line the modal transformation is independent of frequency [93]. Under these circumstance the modal transform matrix can be reduced to the Clarke transform matrix:

$$[S] = [Q] = \frac{1}{3}\begin{pmatrix} 1 & 1 & 1 \\ 2 & -1 & -1 \\ 0 & \sqrt{3} & -\sqrt{3} \end{pmatrix} \tag{A.26}$$

The first row gives the ground mode and the other two rows defines the aerial modes. The transform matrices of an untransposed transmission line are frequency dependent and contain complex components. The transform matrices can be calculated from the line parameters by selecting a frequency representative of the traveling waves and using eigen vector analysis [94] to diagonalize $[\gamma^2]$.

It was shown in [95] that the imaginary components of the transform matrix are small when compared with the real components at the frequency range of traveling waves so a good approximation can be made using just the real components only thus simplifying the calculations involved.

## A.3 Fault Events on Single Phase Systems

For short circuit faults the initial amplitude of the traveling wave at the fault location can be found by assuming there is an e.m.f equal and opposite to the steady state voltage at the fault location had the fault not occurred [39, 40] in series with a fault resistance $R_f$. Assuming the surge impedance, $Z_s$, of the transmission line is the same either side of the fault, the voltage and current amplitudes of both the forward and backward traveling waves will be identical. This situation is depicted in Fig. A.2

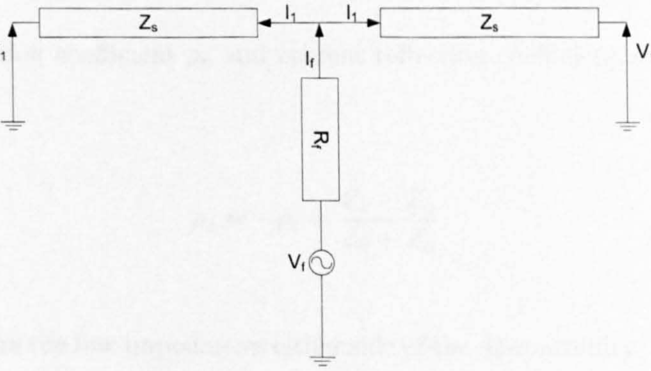


FIGURE A.2: Equivalent circuit of initial fault condition

The initial voltage wave is then:

$$V_1 = -\frac{Z_s}{Z_s + 2R_f} V_f \tag{A.27}$$

Similarly, the initial value of the current wave $I_1$ is:

$$I_1 = \frac{V_1}{Z_s} = \frac{1}{Z_s + 2R_f} V_f \tag{A.28}$$

Forward current traveling waves traveling in the positive $x$ direction will have the same sign as the forward voltage traveling waves. Backward current traveling waves will have the opposite sign to the backward voltage traveling waves.

### A.3.1 Reflections at Impedance Discontinuities

For a single propagating wave ($f_1$ or $f_2$ in equation (A.12)) the surge impedance of a transmission line is defined as the ratio of voltage over current.

$$Z_s = \frac{v(x,t)}{i(x,t)} \tag{A.29}$$

The voltage reflection coefficient $\rho_v$ and current reflection coefficient $\rho_i$ are defined as:

$$\rho_v = -\rho_i = \frac{Z_b - Z_a}{Z_b + Z_a} \tag{A.30}$$

where $Z_a$ and $Z_b$ are the line impedances either side of the discontinuity. The transmitted voltage $T_v$ and transmitted current coefficient $T_i$ are defined in a similar fashion as:

$$T_v = 1 + \rho_v = \frac{2Z_b}{(Z_b + Z_a)} V_i \tag{A.31}$$

and

$$T_i = \frac{Z_a T v}{Z_b} \tag{A.32}$$

### A.3.2 Reflections at Fault Locations

The fault location represent a significant discontinuity in characteristic impedance of the line as depicted in Fig. A.3.

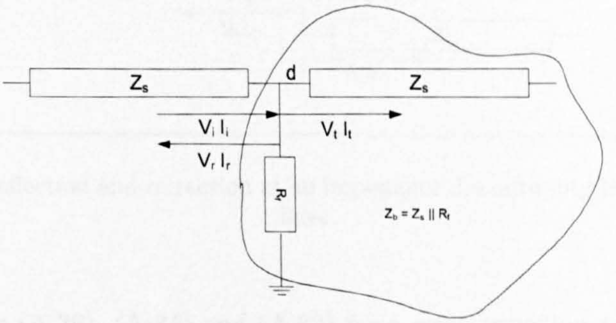


FIGURE A.3: Reflection of a traveling wave at a fault location

A traveling wave propagating towards the fault location will see an effective impedance at the fault location equal to the parallel combination of fault resistance, $R_f$, and the surge impedance the line, $Z_s$. This can be substituted into equation (A.31) to give the fault voltage reflection coefficient:

$$\rho_{vf} = -\frac{Z_s}{Z_s + 2R_f} \tag{A.33}$$

where $\rho_{vf}$ is the voltage reflection coefficient at the fault location. Similar expressions can be obtained for the voltage and current transmission coefficients.

### A.3.3 Reflections at Intersections of Multiple Lines

In some circumstances, such as at the junction between a sub-feeder and main feeder, reflection and refraction of traveling waves occur on multiple lines. Consider the situation depicted in Fig.A.4 which shows the junction of three line $a$, $b$ and $c$ with surge impedance $Z_a$, $Z_b$ and $Z_c$.

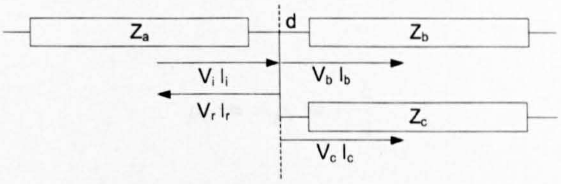


FIGURE A.4: Reflection and refraction at an impedance discontinuity between multiple lines

Applying equations (A.30), (A.31) and (A.32) for a wave traveling toward the junction along line $a$, the voltage and current reflection coefficients are given as:

$$\rho_v = -\rho_i = \frac{\frac{Z_b Z_c}{Z_b + Z_c} - Z_a}{\frac{Z_b Z_c}{Z_b + Z_c} + Z_a} \tag{A.34}$$

The voltage transmission coefficients are given as:

$$T_v = 1 + \rho_v = \frac{2\frac{Z_b Z_c}{Z_b + Z_c}}{\frac{Z_b Z_c}{Z_b + Z_c} + Z_a} \tag{A.35}$$

The current transmission coefficients are given as:

$$T_{ib} = \frac{Z_a T_v}{Z_b} \tag{A.36}$$

and

$$T_{ic} = \frac{Z_a T_v}{Z_c} \tag{A.37}$$

The same analysis can be applied to junctions of $n$ transmission lines in the same manner. In the majority of circumstances the impedance of each of the transmission lines have the same surge impedance. In the case of the junction of three lines as in Fig. A.4 the reflection and transmission coefficients reduce to:

$$\rho_v = -\rho_i = -\frac{1}{3} \tag{A.38}$$

and

$$T_v = T_i = \frac{2}{3} \tag{A.39}$$

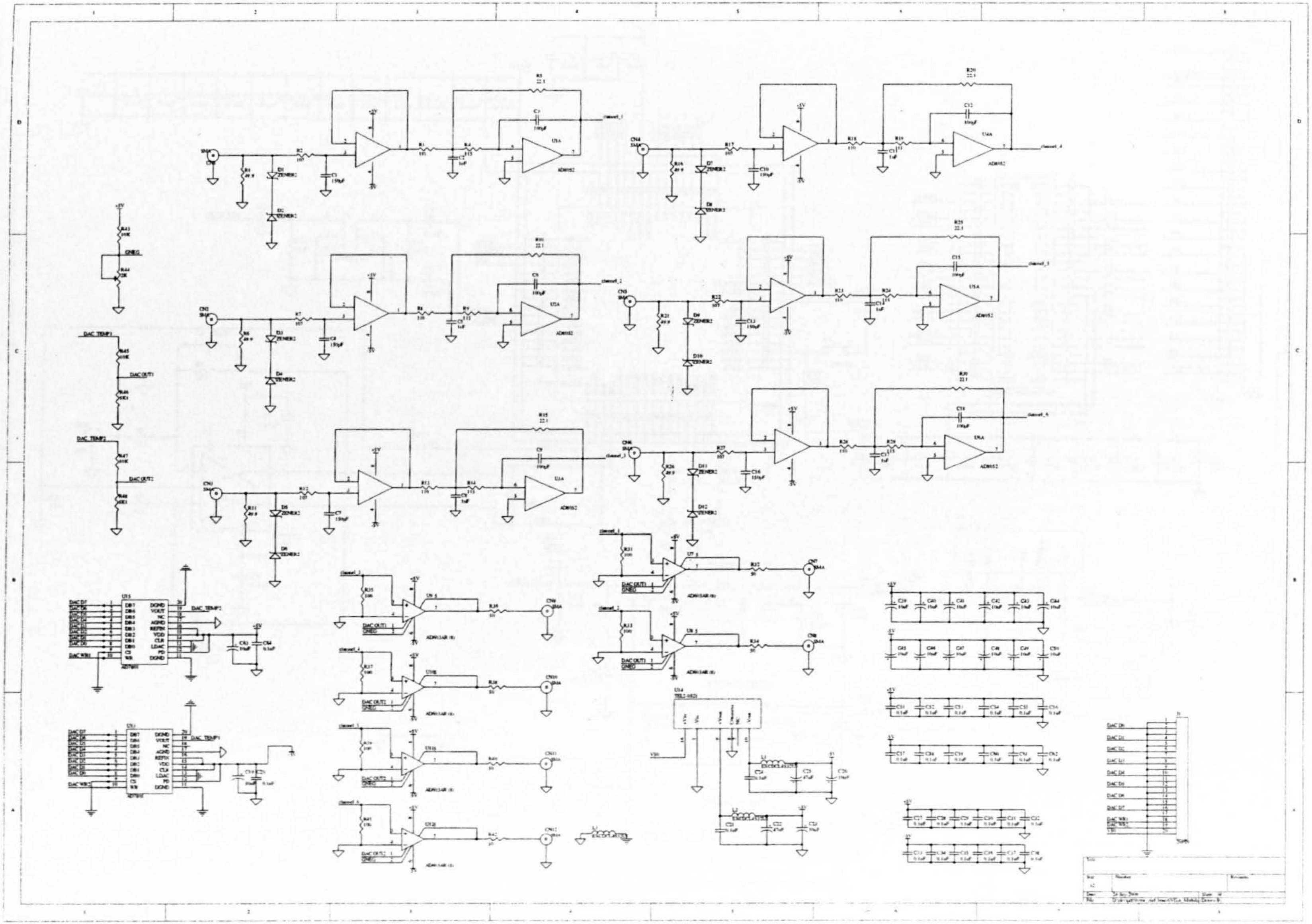
# Appendix B

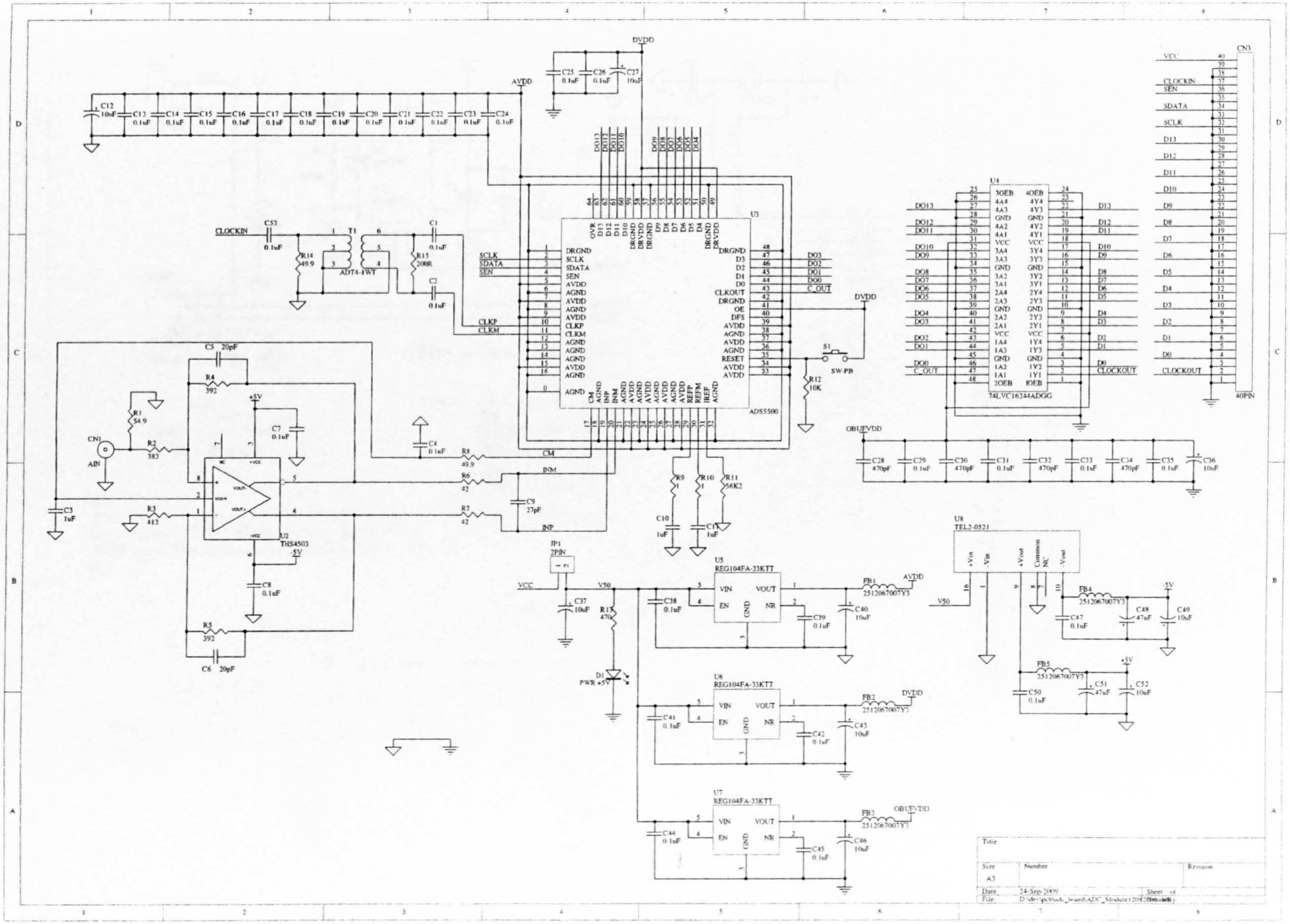
# Fault Recorder Schematics

## B.1 Description

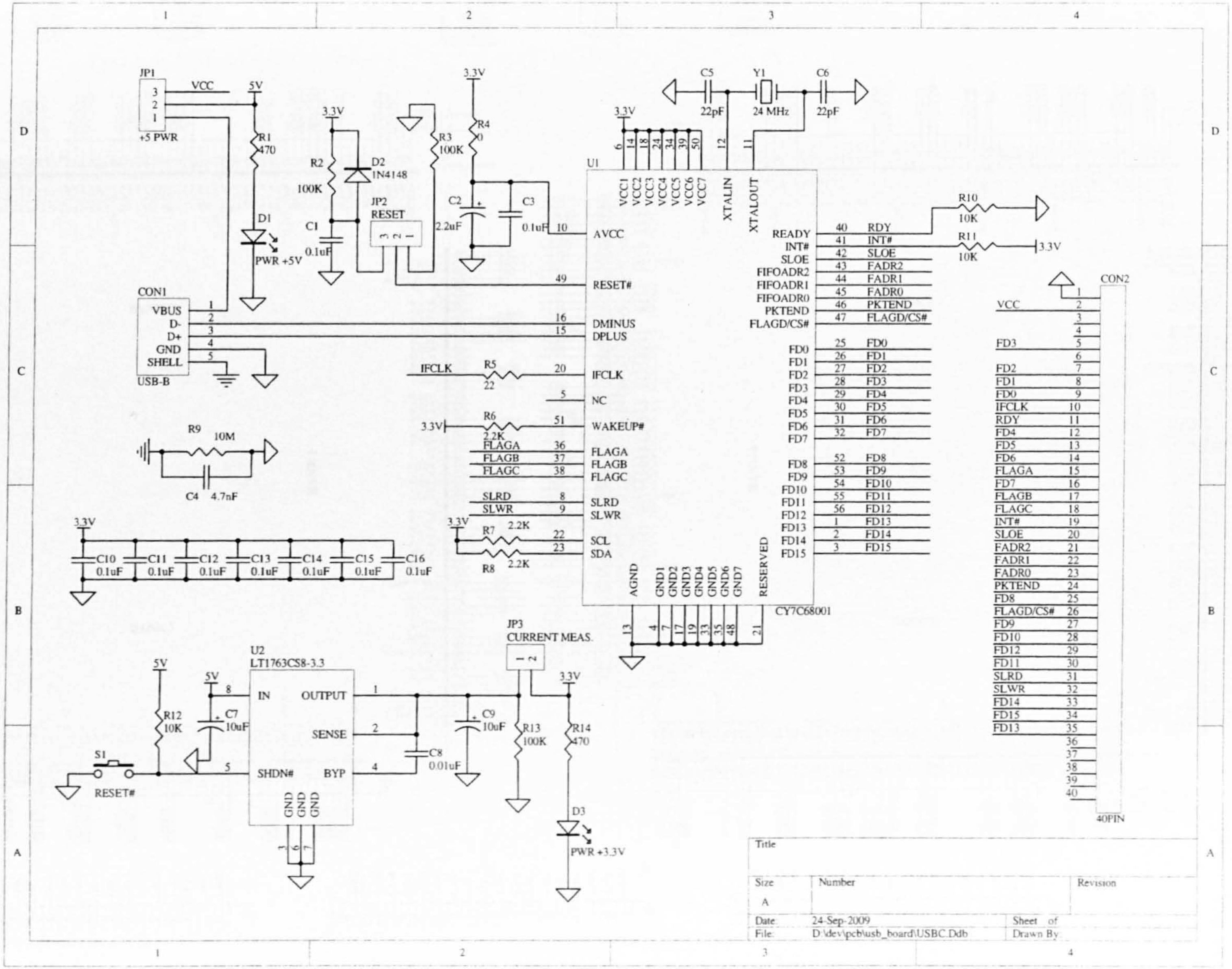
In this appendix are the schematic diagrams of the hardware on the FPGA high speed data acquisition unit presented in chapter 5. The schematic diagrams are in the following order:

- Front-end Board
- ADC Board
- USB Board [70]
- FPGA Board [69]

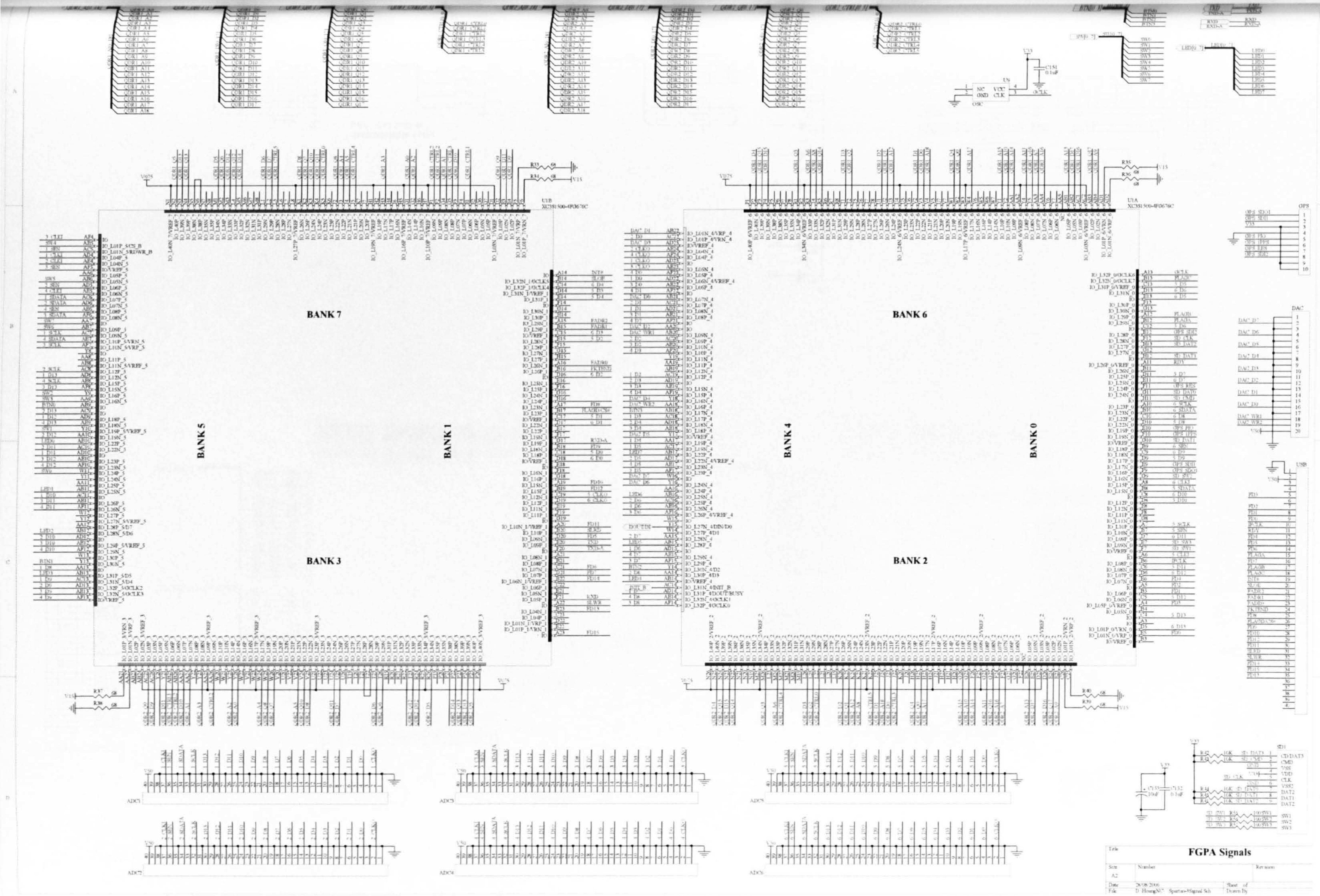




DVDD
AVDD
C12 10uF
C13 0.1uF
C14 0.1uF
C15 0.1uF
C16 0.1uF
C17 0.1uF
C18 0.1uF
C19 0.1uF
C20 0.1uF
C21 0.1uF
C22 0.1uF
C23 0.1uF
C24 0.1uF
C25 0.1uF
C26 0.1uF
C27 10uF
CLOCKIN
C53 0.1uF
R14 49.9
T1 ADT4-1WT
R15 200R
C1 0.1uF
C2 0.1uF
SCLK
SDATA
SEN
CLKP
CLKM
U3 ADS5500
DRGND
SCLK
SDATA
SEN
AVDD
AGND
CLKP
CLKM
OVR
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
CLKOUT
OE
DFS
RESET
CM
INP
INM
REFP
REFM
IREF
DRVDD
DO13
DO12
DO11
DO10
DO9
DO8
DO7
DO6
DO5
DO4
DO3
DO2
DO1
DO0
C_OUT
S1 SW-PB
R12 10K
R9 1
R10 1
R11 56K2
C10 1uF
C11 1uF
C4 0.1uF
R8 49.9
R6 42
R7 42
C9 27pF
CM
INM
INP
C5 20pF
R4 392
+5V
C7 0.1uF
R1 54.9
CN1 AIN
R2 383
C3 1uF
R3 412
U2 THS4503
-5V
C8 0.1uF
R5 392
C6 20pF
U4 74LVC16244ADGG
1OEB 2OEB 3OEB 4OEB
1A1 1A2 1A3 1A4 2A1 2A2 2A3 2A4 3A1 3A2 3A3 3A4 4A1 4A2 4A3 4A4
1Y1 1Y2 1Y3 1Y4 2Y1 2Y2 2Y3 2Y4 3Y1 3Y2 3Y3 3Y4 4Y1 4Y2 4Y3 4Y4
VCC
GND
CLOCKOUT
CN3 40PIN
VCC
OBUFVDD
C28 470pF
C29 0.1uF
C30 470pF
C31 0.1uF
C32 470pF
C33 0.1uF
C34 470pF
C35 0.1uF
C36 10uF
JP1 2PIN
VCC
V50
C37 10uF
R13 470
D1 PWR +5V
U5 REG104FA-33KTT
U6 REG104FA-33KTT
U7 REG104FA-33KTT
VIN
EN
GND
VOUT
NR
C38 0.1uF
C39 0.1uF
C40 10uF
FB1 2512067007Y3
C41 0.1uF
C42 0.1uF
C43 10uF
FB2 2512067007Y3
C44 0.1uF
C45 0.1uF
C46 10uF
FB3 2512067007Y3
U8 TEL2-0521
+Vin
-Vin
+Vout
Common
NC
-Vout
FB4 2512067007Y3
C47 0.1uF
C48 47uF
C49 10uF
FB5 2512067007Y3
C50 0.1uF
C51 47uF
C52 10uF
Title
Size A3
Number
Revision
Date 24-Sep-2009
Sheet of
File



JP1
3
2
1
+5 PWR
VCC
5V
R1
470
D1
PWR +5V
3.3V
R2
100K
D2
1N4148
C1
0.1uF
JP2
RESET
3 2 1
R3
100K
3.3V
R4
0
C2
2.2uF
C3
0.1uF
CON1
VBUS
D-
D+
GND
SHELL
USB-B
IFCLK
R5
22
3.3V
R6
2.2K
FLAGA
FLAGB
FLAGC
SLRD
SLWR
R7
2.2K
R8
2.2K
R9
10M
C4
4.7nF
3.3V
C10 0.1uF
C11 0.1uF
C12 0.1uF
C13 0.1uF
C14 0.1uF
C15 0.1uF
C16 0.1uF
C5
22pF
Y1
24 MHz
C6
22pF
U1
VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7
XTALIN
XTALOUT
AVCC
RESET#
DMINUS
DPLUS
IFCLK
NC
WAKEUP#
FLAGA
FLAGB
FLAGC
SLRD
SLWR
SCL
SDA
AGND
GND1 GND2 GND3 GND4 GND5 GND6 GND7
RESERVED
READY
INT#
SLOE
FIFOADR2
FIFOADR1
FIFOADR0
PKTEND
FLAGD/CS#
FD0 FD1 FD2 FD3 FD4 FD5 FD6 FD7
FD8 FD9 FD10 FD11 FD12 FD13 FD14 FD15
CY7C68001
RDY
INT#
SLOE
FADR2
FADR1
FADR0
PKTEND
FLAGD/CS#
R10
10K
R11
10K
3.3V
CON2
40PIN
VCC
FD3
FD2
FD1
FD0
IFCLK
RDY
FD4
FD5
FD6
FLAGA
FD7
FLAGB
FLAGC
INT#
SLOE
FADR2
FADR1
FADR0
PKTEND
FD8
FLAGD/CS#
FD9
FD10
FD12
FD11
SLRD
SLWR
FD14
FD15
FD13
JP3
CURRENT MEAS.
U2
LT1763CS8-3.3
5V
R12
10K
S1
RESET#
5V
C7
10uF
IN
OUTPUT
SENSE
SHDN#
BYP
GND GND GND
C8
0.01uF
C9
10uF
R13
100K
3.3V
R14
470
D3
PWR +3.3V
Title
Size
A
Number
Revision
Date: 24-Sep-2009
File: D:\dev\pcb\usb_board\USBC.Ddb
Sheet of
Drawn By:
1 2 3 4
A B C D


U1B
XC3S1500-4FG676C
U1A
XC3S1500-4FG676C
BANK 7
BANK 5
BANK 1
BANK 3
BANK 6
BANK 4
BANK 0
BANK 2
U5
OSC
NC
GND
VCC
CLK
C151
0.1uF
V33
OCLK
V075
V15
R33
R34
R35
R36
R37
R38
R39
R40
68
GPS
DAC
USB
SD1
ADC1
ADC2
ADC3
ADC4
ADC5
ADC6
C133
C132
10uF
0.1uF
SW1
SW2
SW3
Title
FGPA Signals
Size
A2
Number
Revision
Date
28/08/2006
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File
D:\HoangNC\...\Spartan-3Signal.Sch
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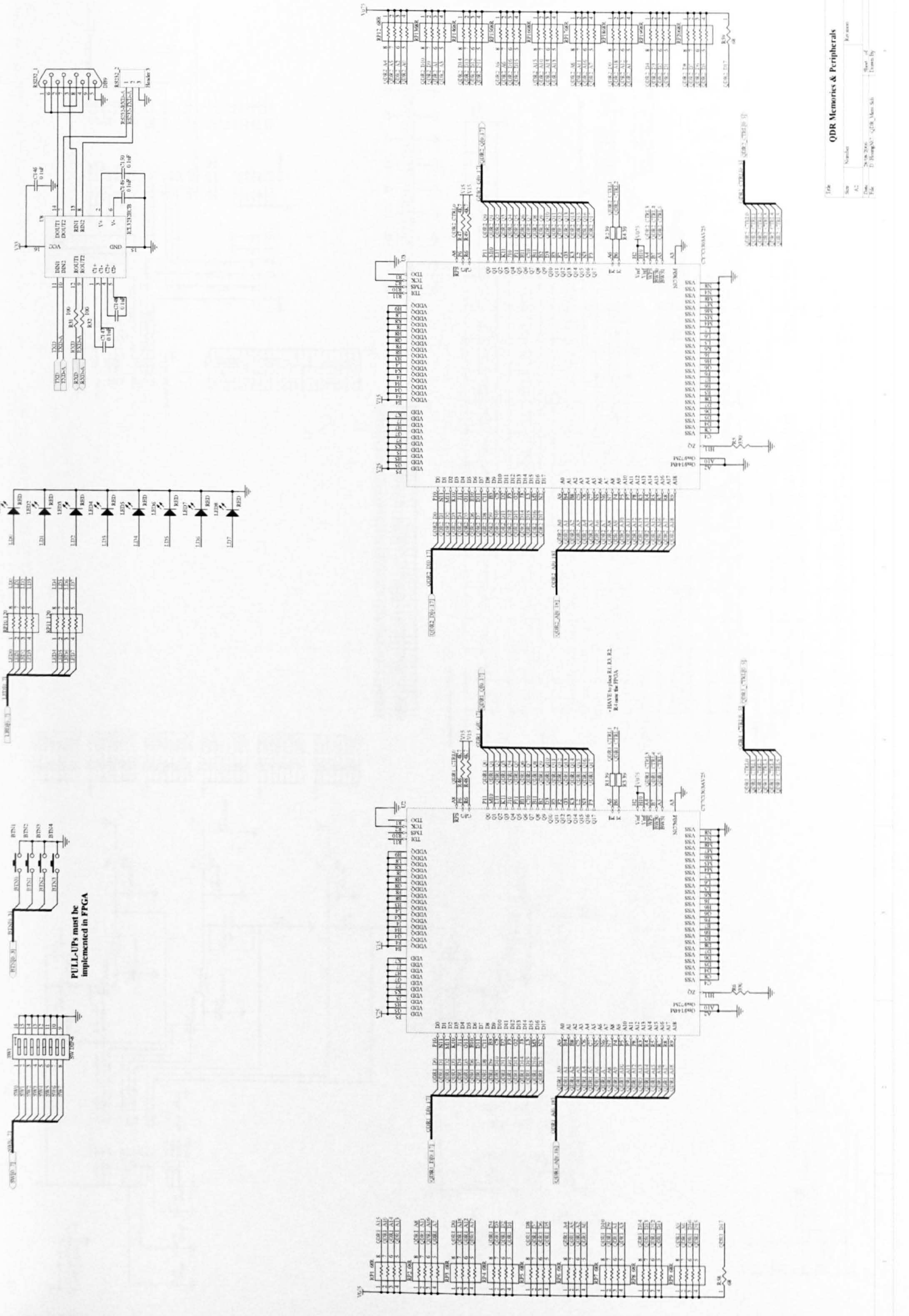
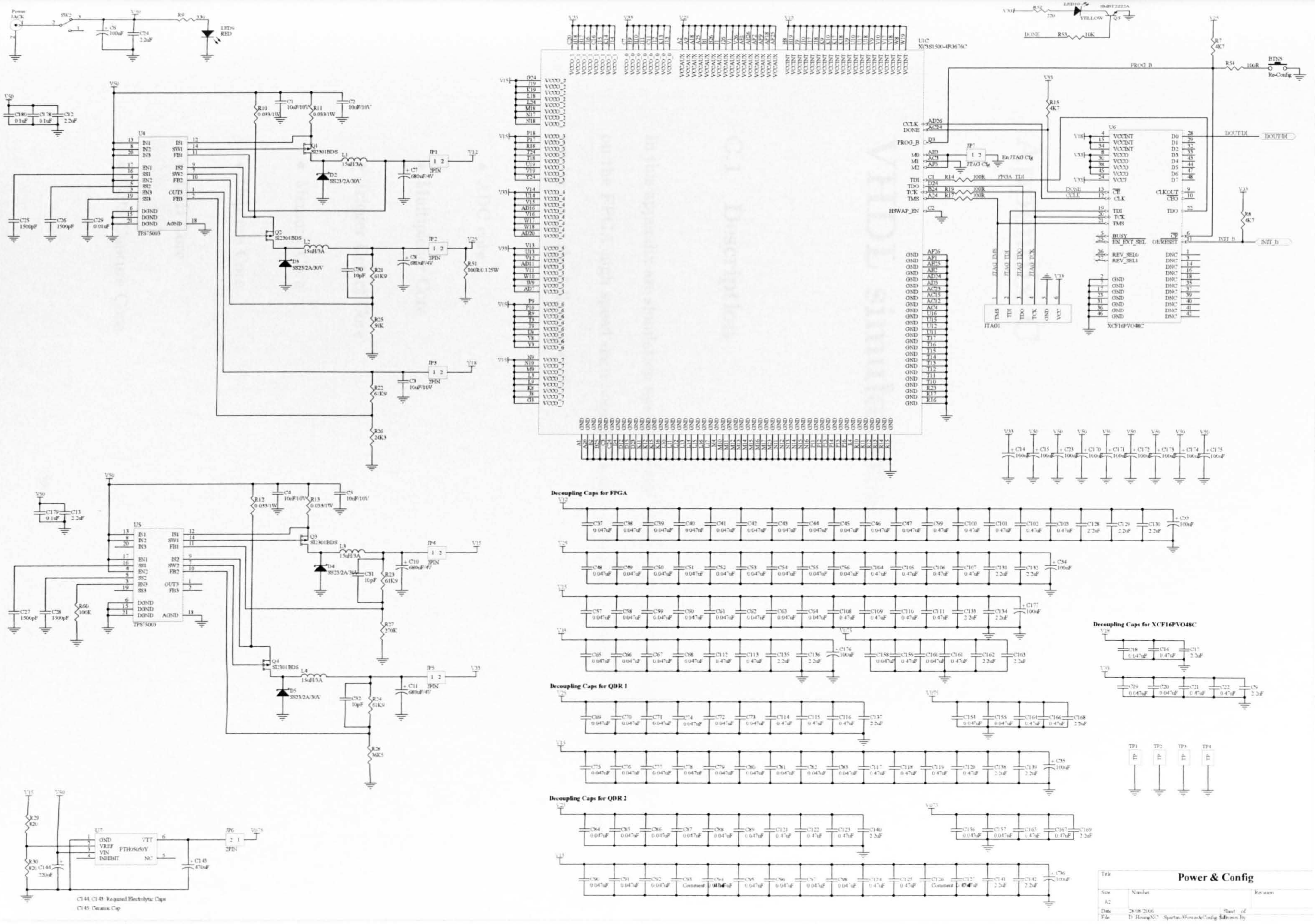

QDR Memories & Peripherals
Title
Size
A3
Number
Revision
Date
29-08-2006
File
QDR_Mem.Sch
Sheet of
Drawn By
PULL-UPs must be implemented in FPGA
SW1
SW DIP-8
BTN1
BTN2
BTN3
BTN4
LED1
LED2
LED3
LED4
LED5
LED6
LED7
LED8
RED
RP10
RP11
U8
ICL3232CBN
VCC
GND
DIN1
DIN2
ROUT1
ROUT2
DOUT1
DOUT2
RIN1
RIN2
C1+
C1-
C2+
C2-
V+
V-
C146
C147
C148
C149
C150
0.1uF
R31
R32
100
TXD
RXD
RS232_1
DB9
RS232_2
Header 3
U2
U3
CY7C1313AV25
VDD
VDDQ
VSS
TDI
TMS
TCK
TDO
ZQ
Vref
NC/36M
NC/72M
NC/144M
RPS
WPS
BWS0
BWS1
K
C
QDR1_D[0..17]
QDR1_A[0..18]
QDR1_Q[0..17]
QDR1_CTRL[0..5]
QDR2_D[0..17]
QDR2_A[0..18]
QDR2_Q[0..17]
QDR2_CTRL[0..5]
- HAVE to place R1, R3, R2, R4 near the FPGA
RP1
RP2
RP3
RP4
RP5
RP6
RP7
RP8
RP9
RP12
RP13
RP14
RP15
RP16
RP17
RP18
RP19
RP20
68R
R38
R39
V25
V15
VTT


Power JACK
SW2
C6 100uF
C24 2.2uF
R9 330
LED8 RED
U4 TPS75003
U5 TPS75003
Q1 SI2301BDS
Q2 SI2301BDS
Q3 SI2301BDS
Q4 SI2301BDS
L1 15uH/3A
D2 SS23/2A/30V
JP1 2PIN
JP2 2PIN
JP3 2PIN
JP4 2PIN
JP5 2PIN
JP6 2PIN
U7 FTH050505Y
C144, C143: Required Electrolytic Caps
C145: Ceramic Cap
U1C XC3S1500-4FG676C
CCLK
DONE
PROG_B
M0
M1
M2
TDI
TDO
TCK
TMS
HSWAP_EN
JP7 JTAG Cfg
En JTAG Cfg
FPGA_TDI
JTAG1
JTAG TMS
JTAG TDI
JTAG TDO
JTAG TCK
U6 XCF16PVO48C
DOUT/DI
INIT_B
BTN5 Re-Config
LED10 YELLOW
Q5 MMBT2222A
Decoupling Caps for FPGA
Decoupling Caps for QDR 1
Decoupling Caps for QDR 2
Decoupling Caps for XCF16PVO48C
TP1
TP2
TP3
TP4
Title
Power & Config
Size A2
Number
Revision
Date 28/08/2006
Sheet of
File D:\HoangNC\...\Spartan-3Power&Config.Sch
Drawn By

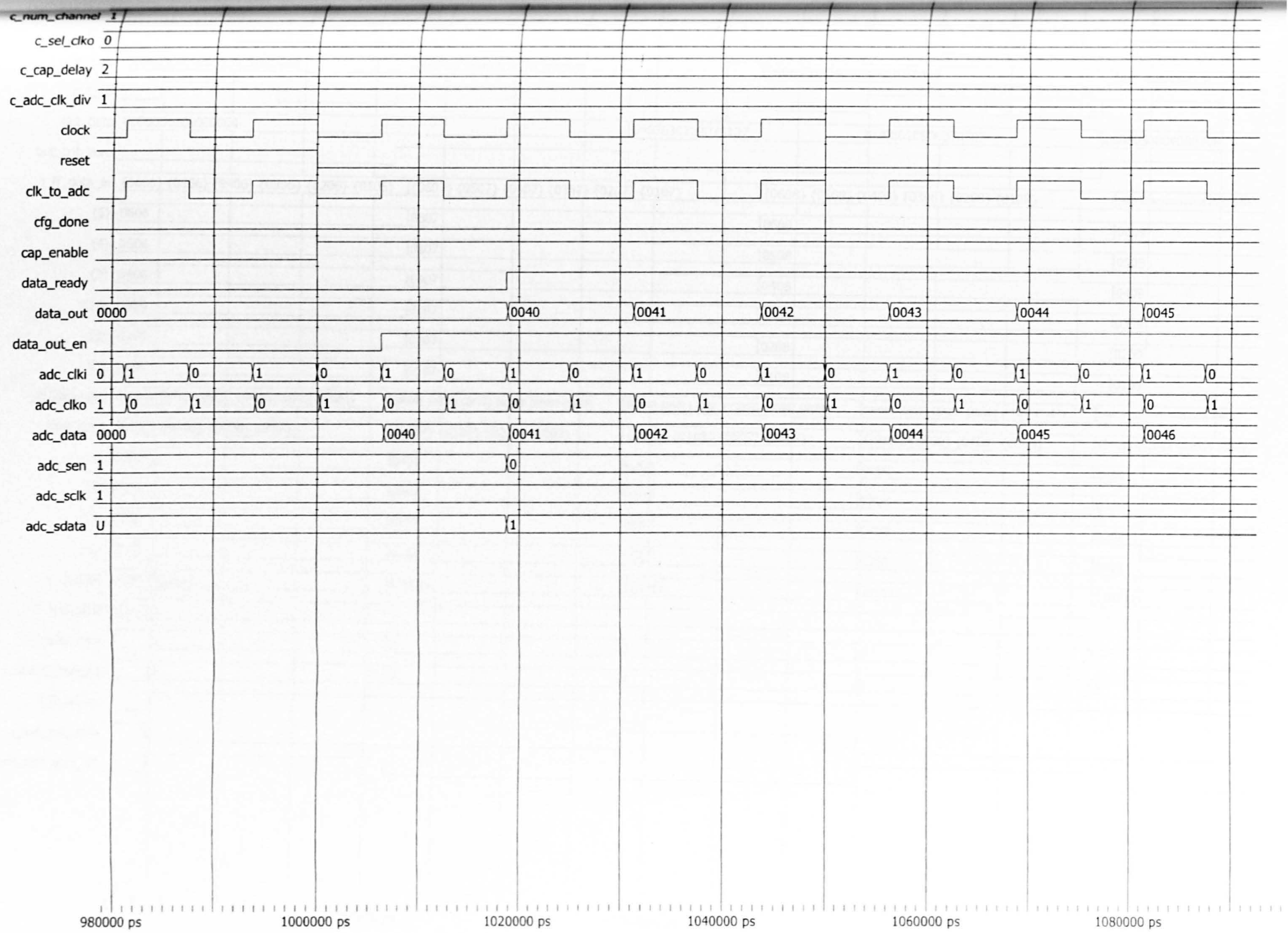
# Appendix C

# VHDL simulations

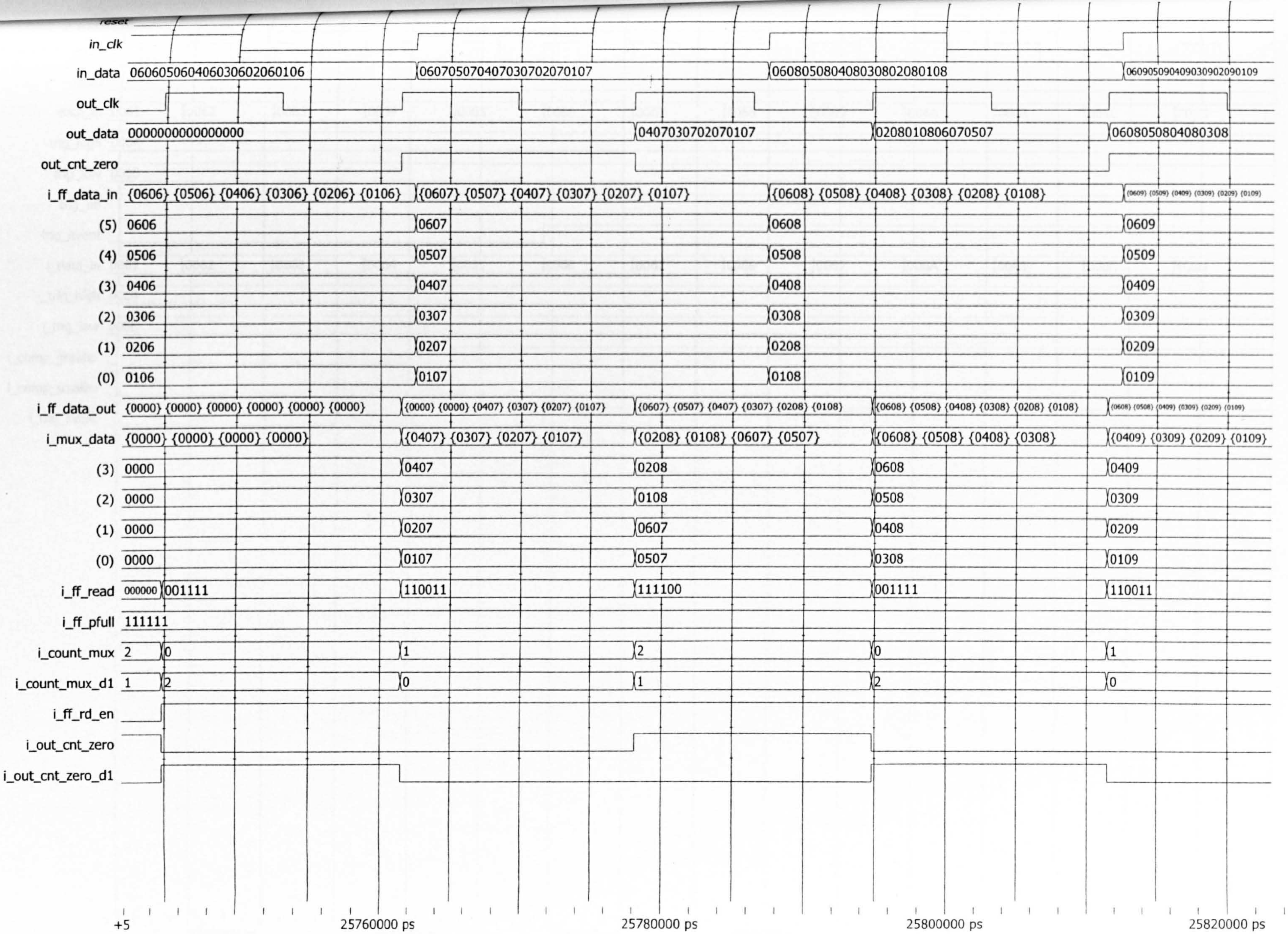
## C.1 Description

In this appendix are simulation results for the VHDL cores used to control the hardware on the FPGA high speed data acquisition unit presented in chapter 5. The simulation results are in the following order:

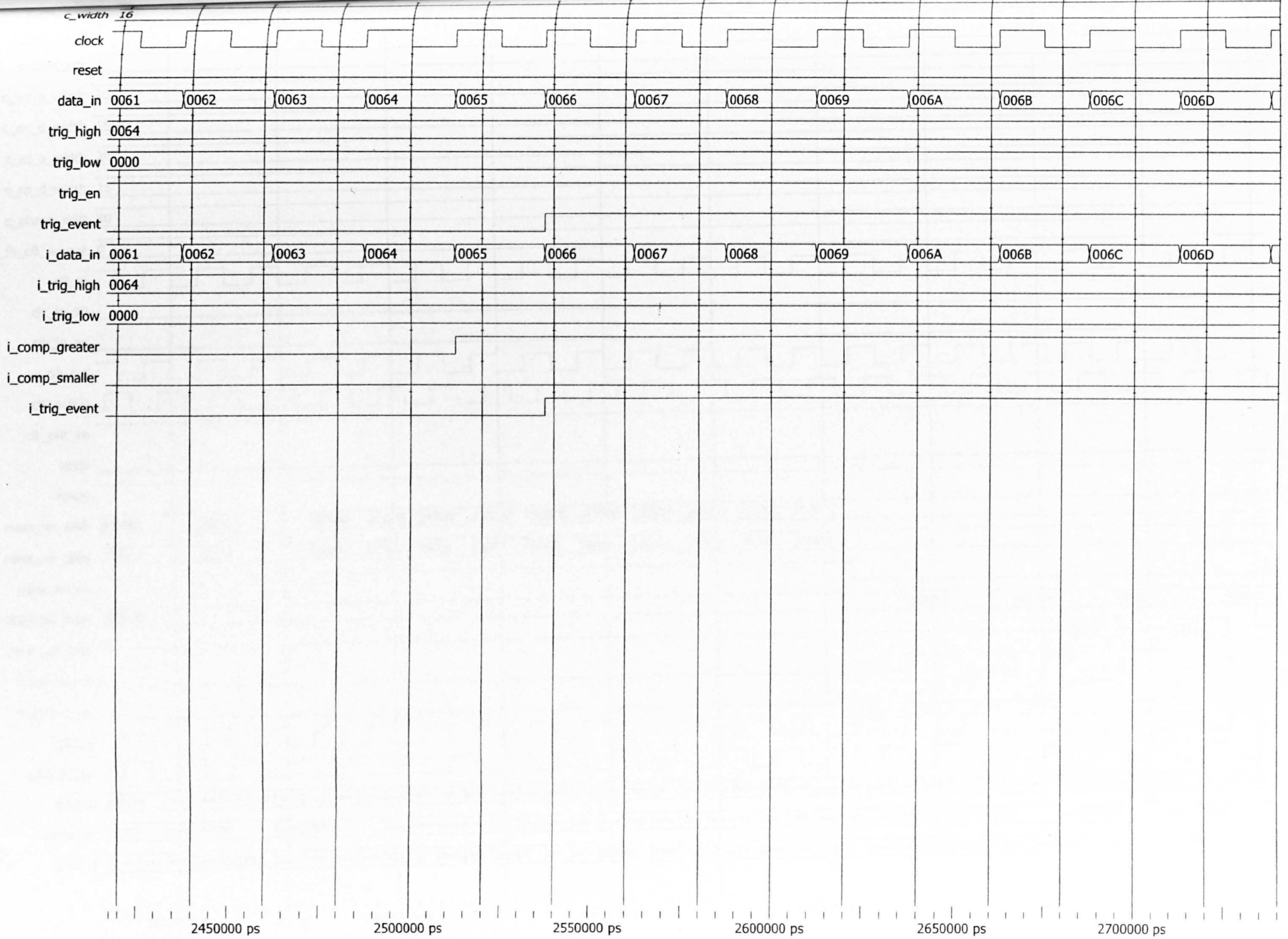
- ADC core
- Multiplexer Core
- Trigger Detect Core
- Memory Core
- Capture Core
- USB Core
- GPS Capture Core



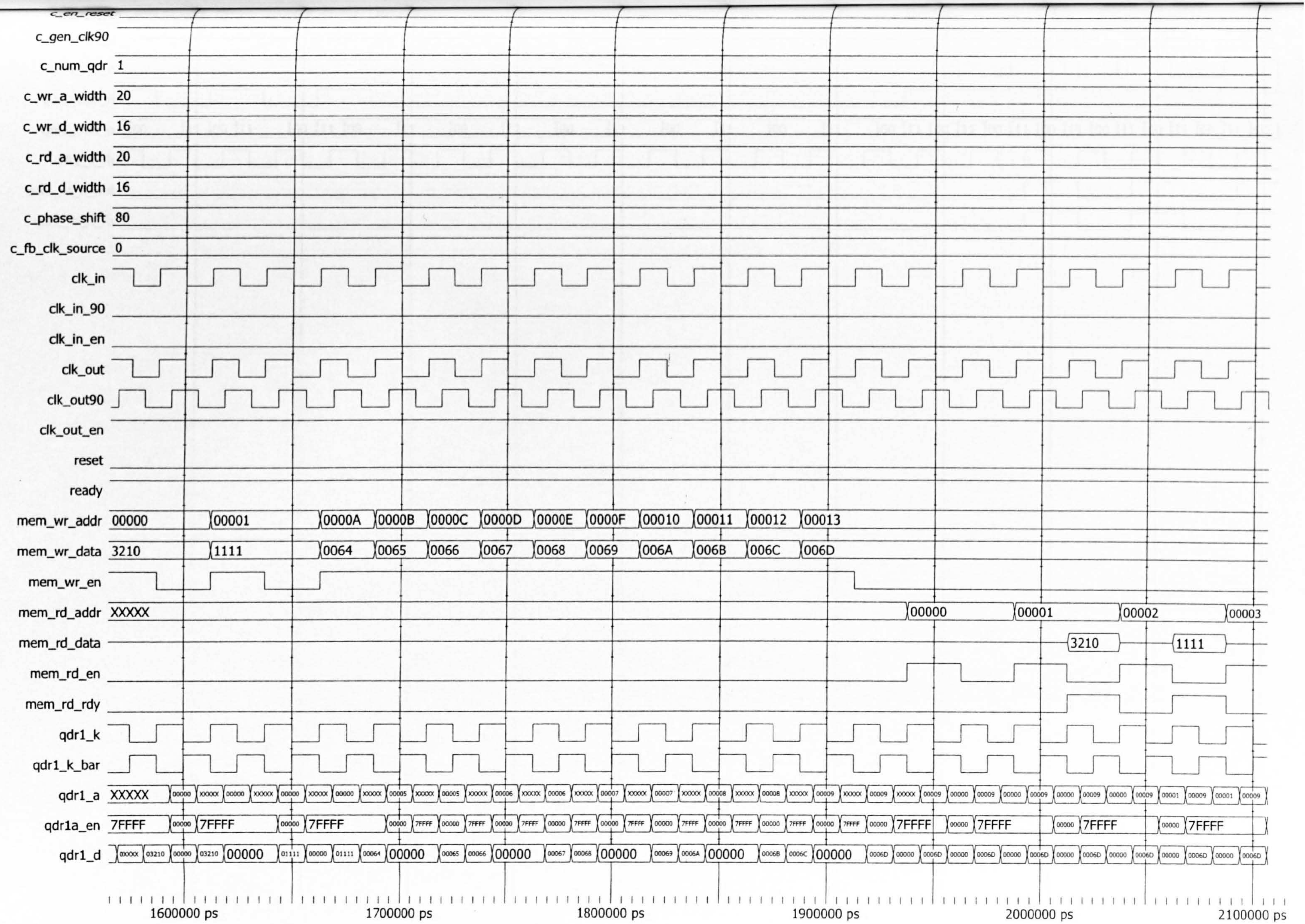
Entity:tb_adc_core Architecture:beh Date: Tue Sep 22 15:48:59 GMT Daylight Time 2009 Row: 1 Page: 1



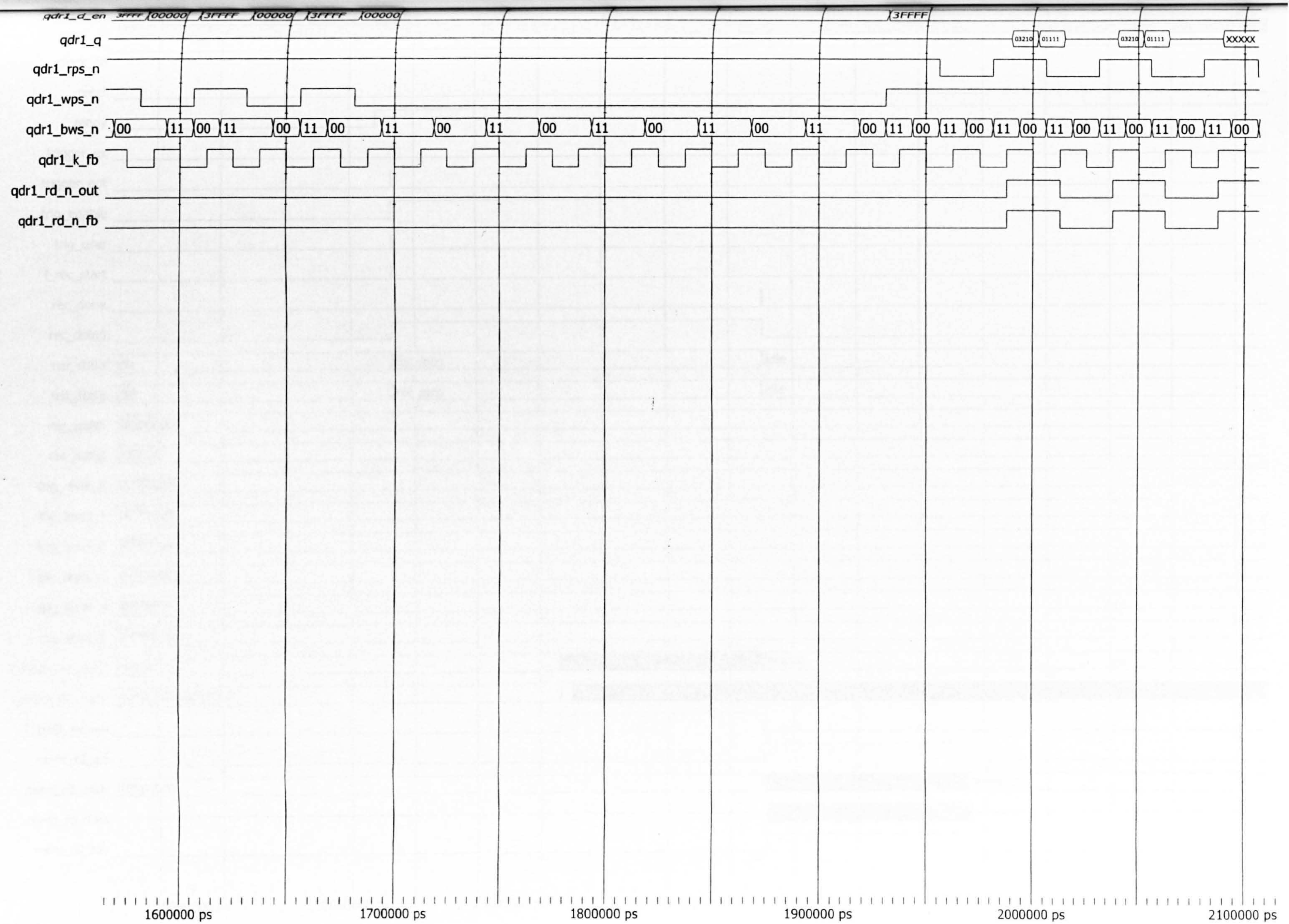
Entity:tb_adc_mux Architecture:behavior Date: Wed Sep 23 08:46:32 GMT Daylight Time 2009 Row: 1 Page: 1



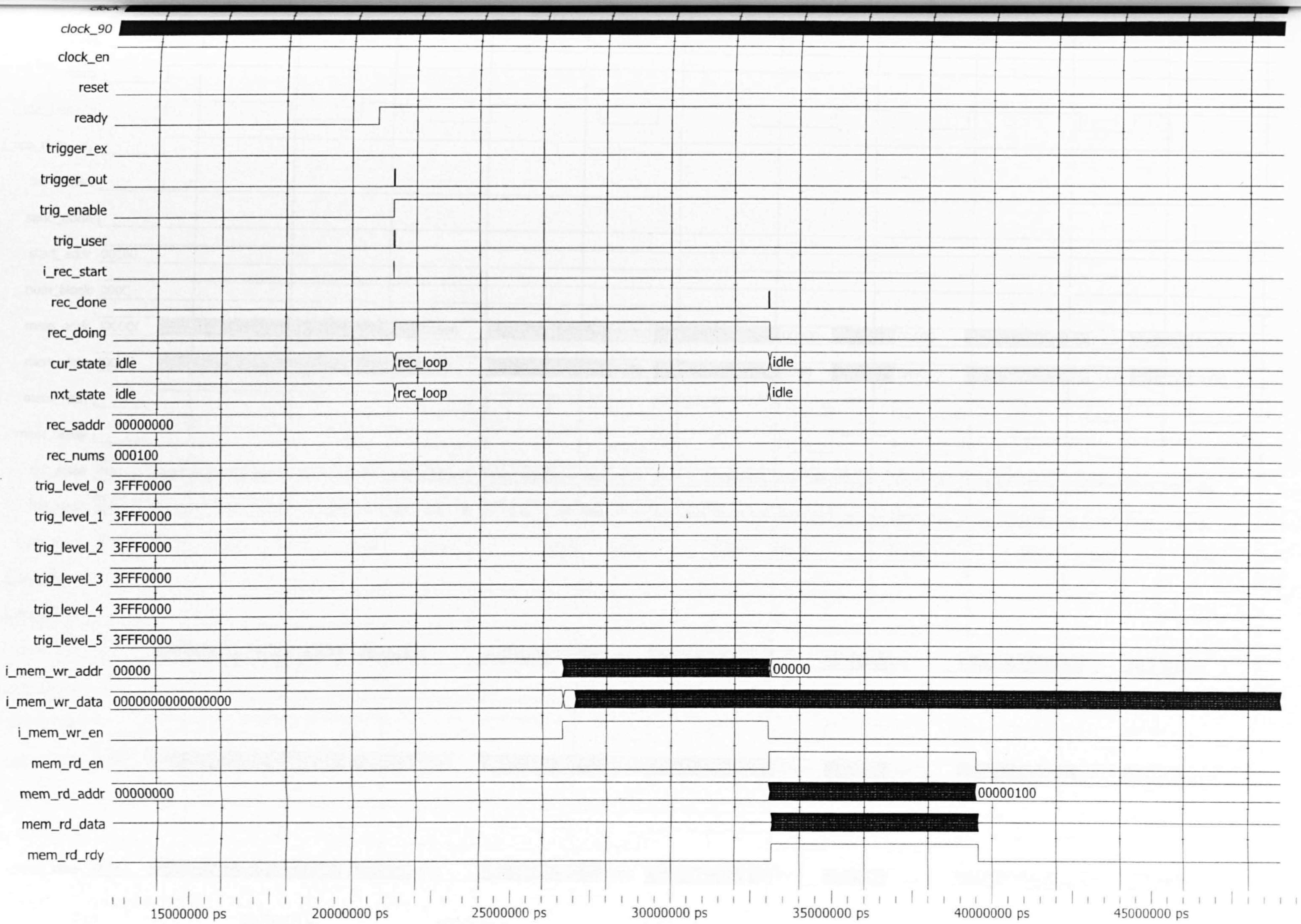
Entity:tb_trig_detect Architecture:beh Date: Wed Sep 23 09:11:27 GMT Daylight



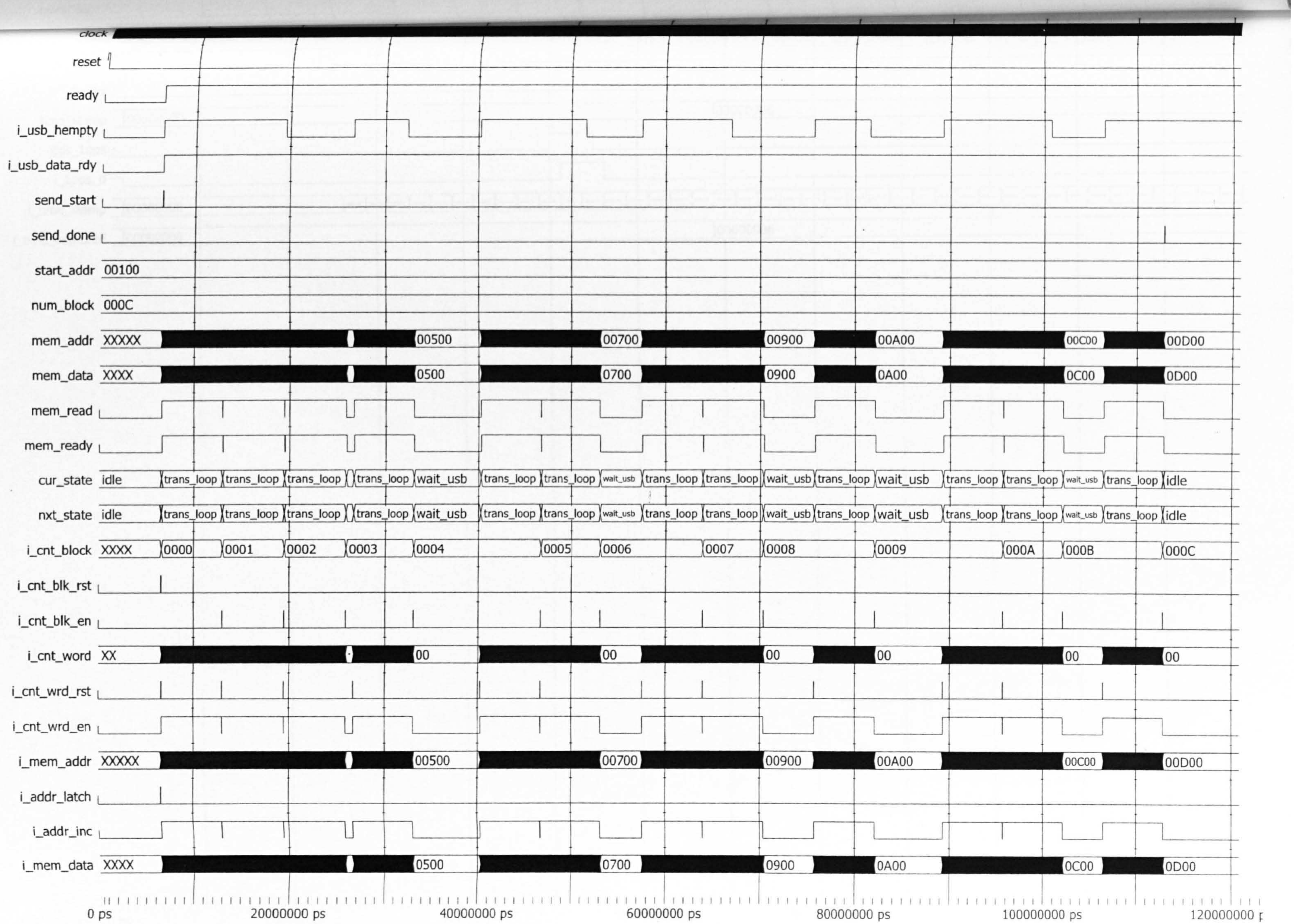
Entity:tb_mem_core_v20 Architecture:beh Date: Thu Sep 24 08:39:57 GMT Daylight Time 2009 Row: 1 Page: 1



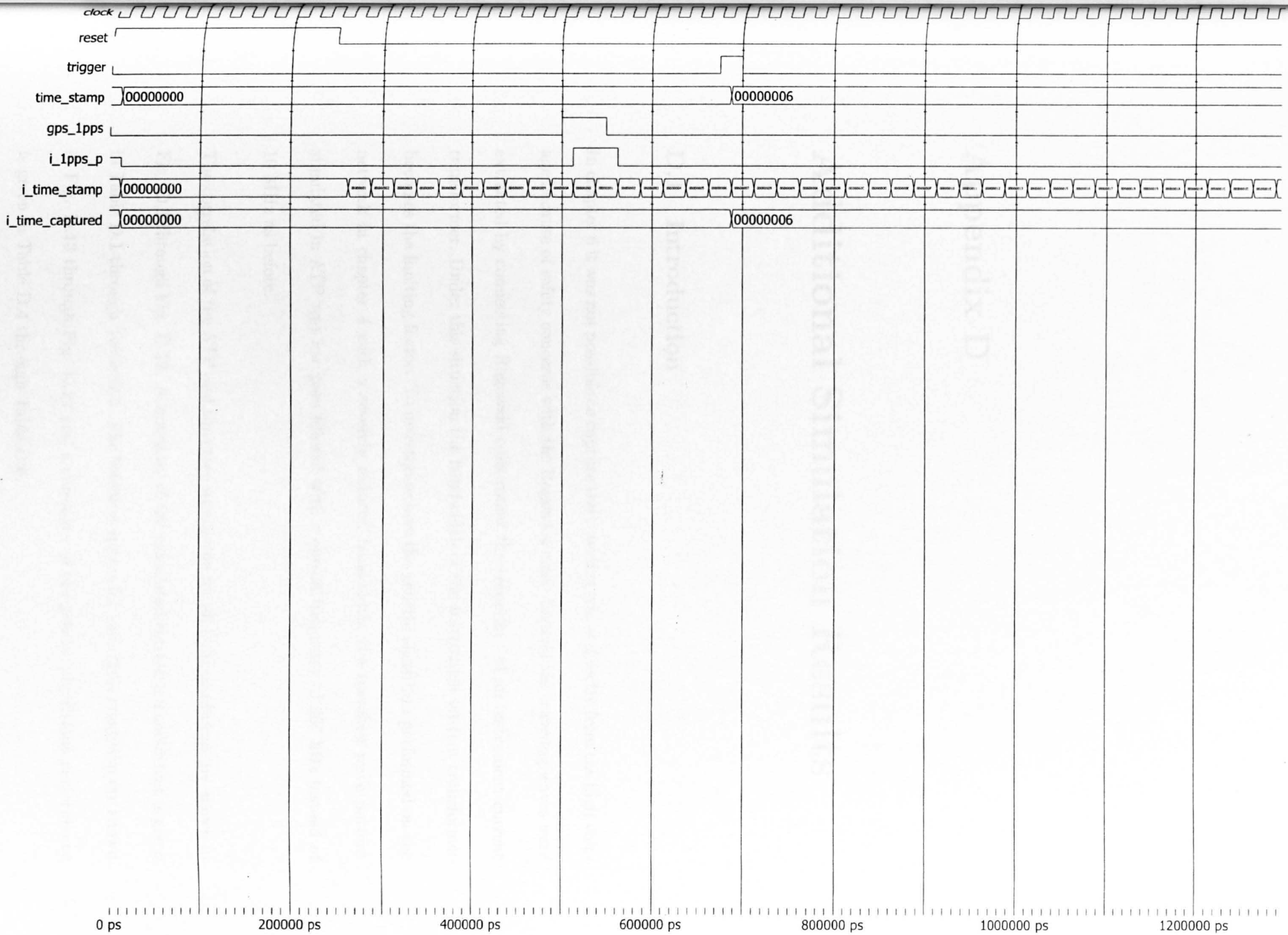
Entity:tb_mem_core_v20 Architecture:beh Date: Thu Sep 24 08:39:57 GMT Daylight Time 2009 Row: 1 Page: 2



Entity:tb_capture_core Architecture:beh Date: Wed Sep 23 16:43:10 GMT Daylight Time 2009 Row: 1 Page: 1



Entity:tb_usb_trans Architecture:beh Date: Thu Sep 24 08:51:23 GMT Daylight Time 2009 Row: 1 Page: 1



Entity:tb_gps_capture_core Architecture:beh Date: Tue Sep 22 16:15:11 GMT Daylight Time 2009 Row: 1 Page: 1

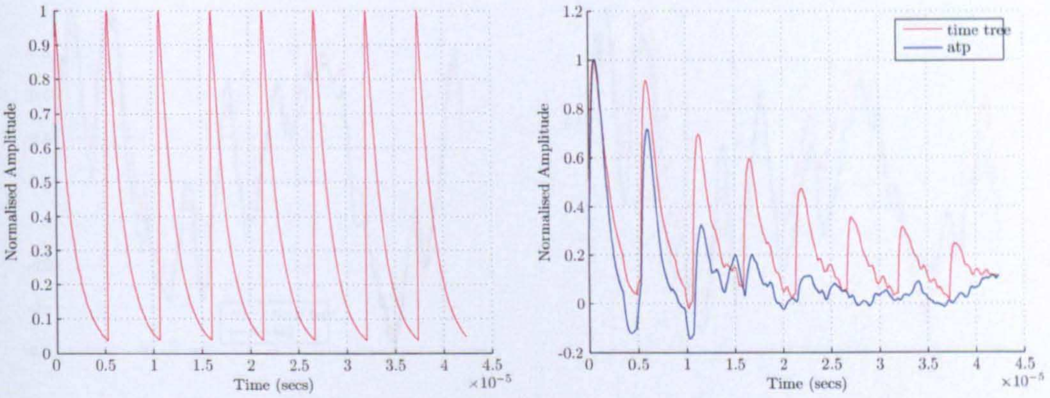
# Appendix D

# Additional Simulation Results

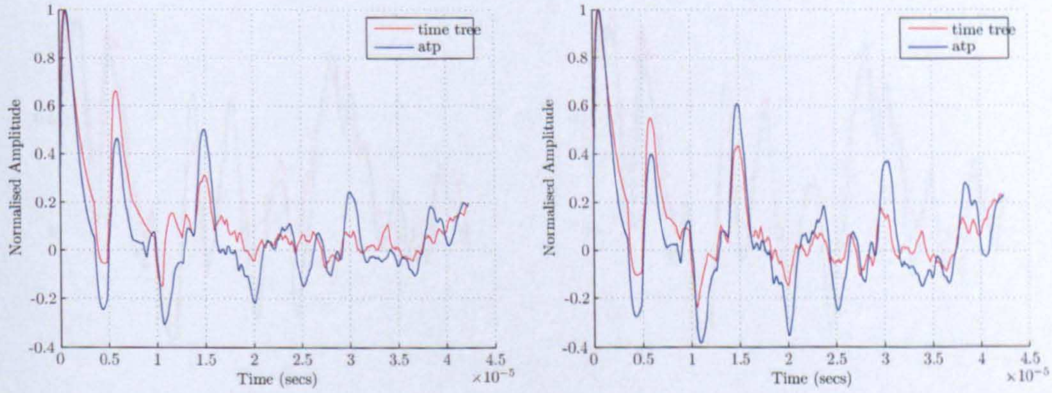
## D.1 Introduction

In chapter 6 it was not possible to capture the traveling waves directly from the high voltage because of safety concerns with the Rogowksi coils. Instead the traveling waves were extracted by connecting Rogowski coils round the secondary of an instrument current transformer. Under this situation the bandwidth of the instrument current transformer becomes the limiting factor. To investigate how the genetic algorithm performed on the network in chapter 4 with a severely reduced bandwidth, the traveling wave pattern simulated in ATP was low pass filtered with a cut-off frequency of 500 kHz instead of 10 MHz as before.

The correlation of the ATP and time tree simulation for all fault conditions are shown in Fig. D.1 through Fig. D.12. A summary of the calculated correlation coefficient is given in Table D.1 through Table D.3. The Solution spaces for each fault condition are shown in Fig. D.13 through Fig. D.24 and a summary of the genetic algorithms performance is given in Table D.4 through Table D.6.

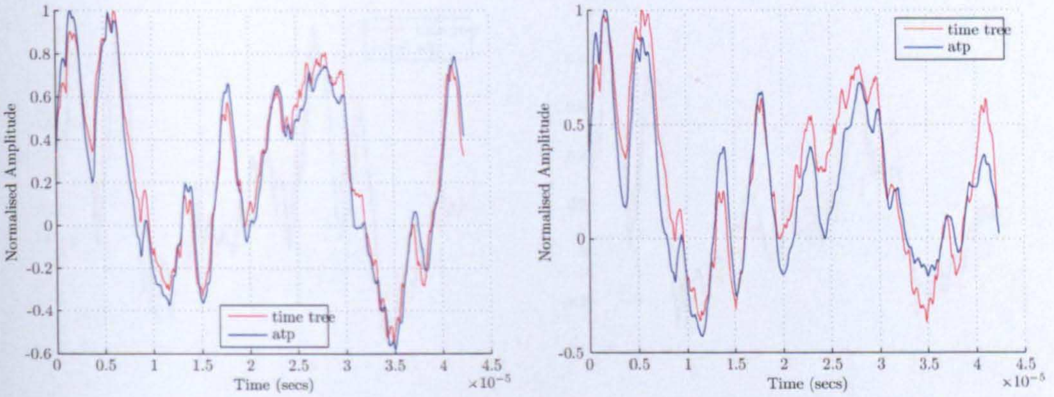


(a) 0 ohm (b) 100 ohm

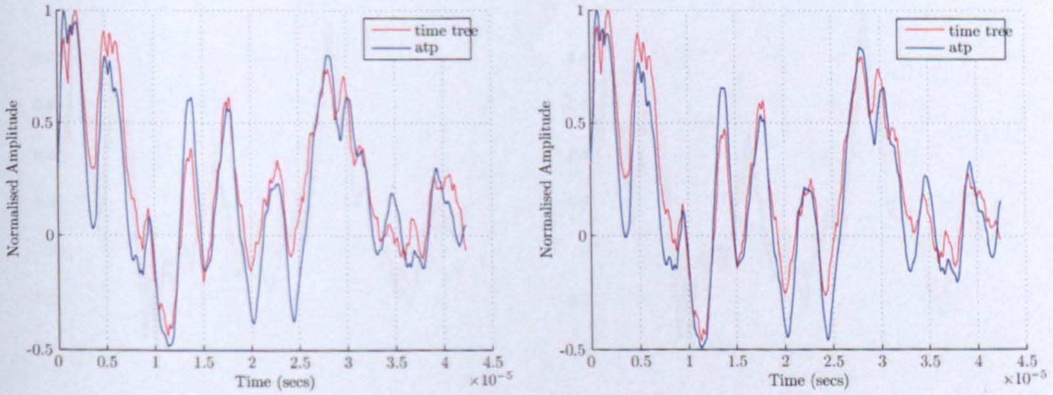


(c) 500 ohm (d) 1000 ohm

FIGURE D.1: Comparison of ATP simulation and time tree simulation for three phase faults at location 1

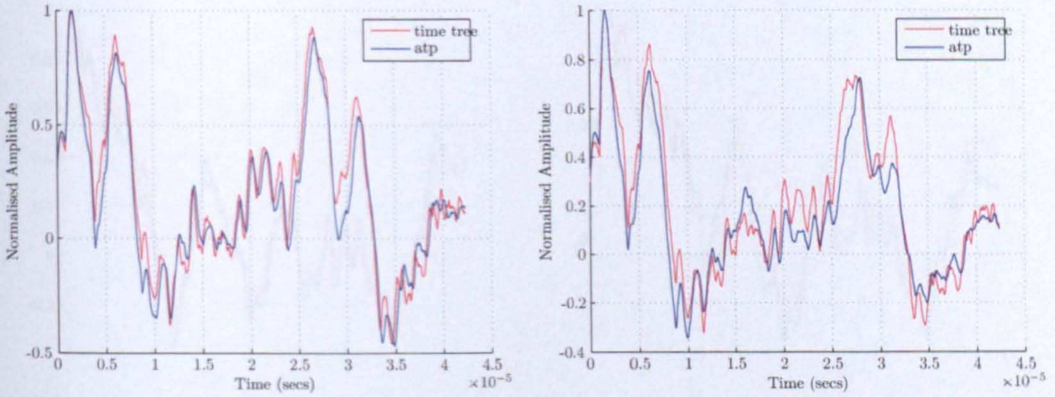


(a) 0 ohm (b) 100 ohm



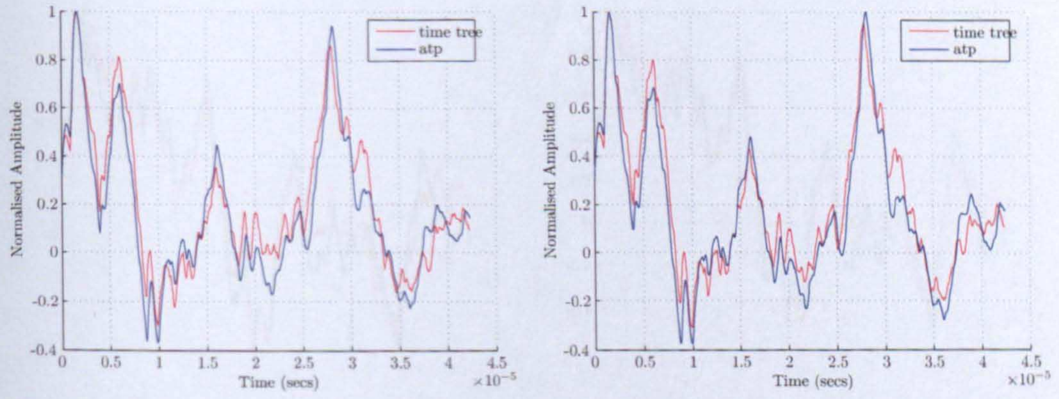
(c) 500 ohm (d) 1000 ohm

FIGURE D.2: Comparison of ATP simulation and time tree simulation for three phase faults at location 2



(a) 0 ohm

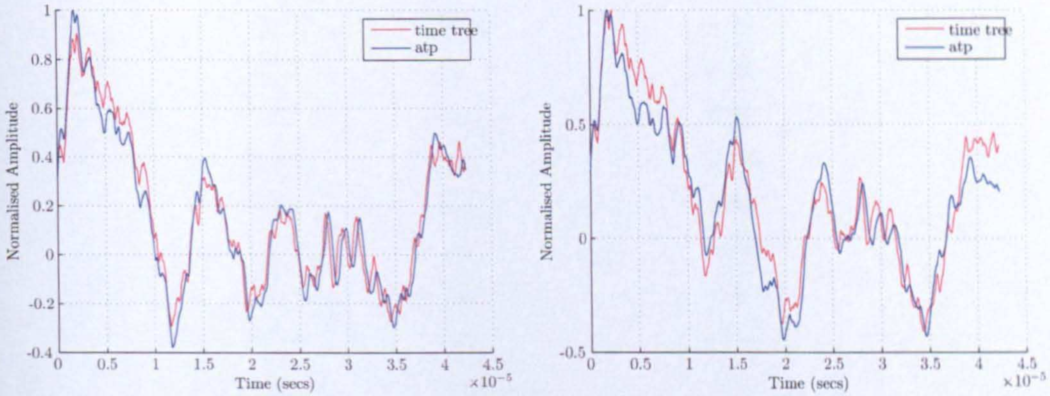
(b) 100 ohm



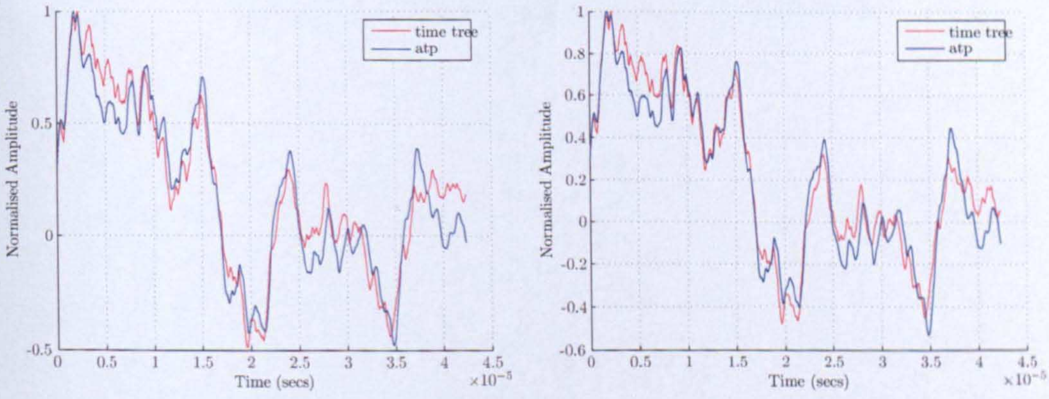
(c) 500 ohm

(d) 1000 ohm

FIGURE D.3: Comparison of ATP simulation and time tree simulation for three phase faults at location 3



(a) 0 ohm (b) 100 ohm

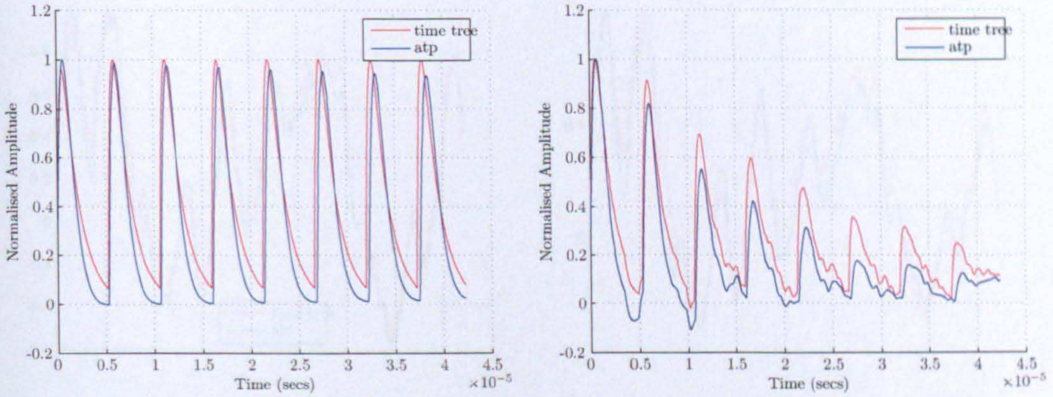


(c) 500 ohm (d) 1000 ohm

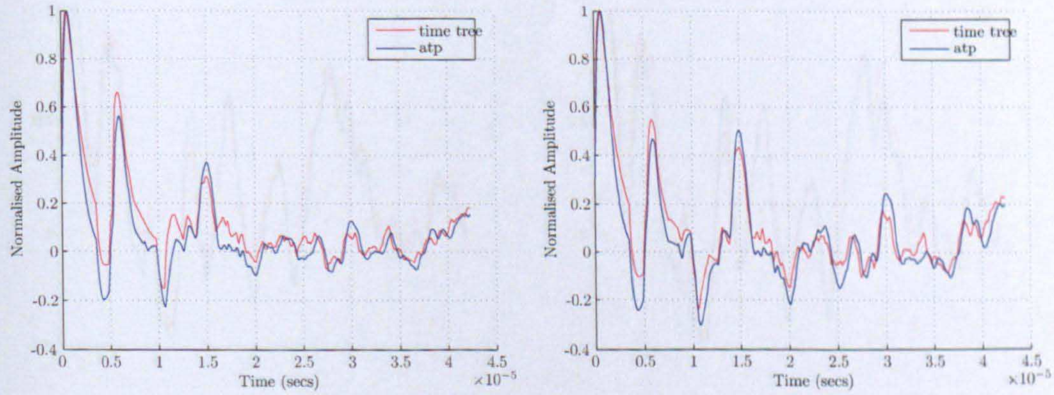
FIGURE D.4: Comparison of ATP simulation and time tree simulation for three phase faults at location 4

| Fault ID | Fault Resistance | Correlation Coefficient |
|---|---|---|
| F1 | 0 | 0.91 |
| F1 | 100 | 0.87 |
| F1 | 500 | 0.88 |
| F1 | 1000 | 0.90 |
| F2 | 0 | 0.98 |
| F2 | 100 | 0.93 |
| F2 | 500 | 0.93 |
| F2 | 1000 | 0.95 |
| F3 | 0 | 0.97 |
| F3 | 100 | 0.95 |
| F3 | 500 | 0.95 |
| F3 | 1000 | 0.96 |
| F4 | 0 | 0.98 |
| F4 | 100 | 0.96 |
| F4 | 500 | 0.96 |
| F4 | 1000 | 0.97 |

TABLE D.1: Correlation coefficients for three phase faults

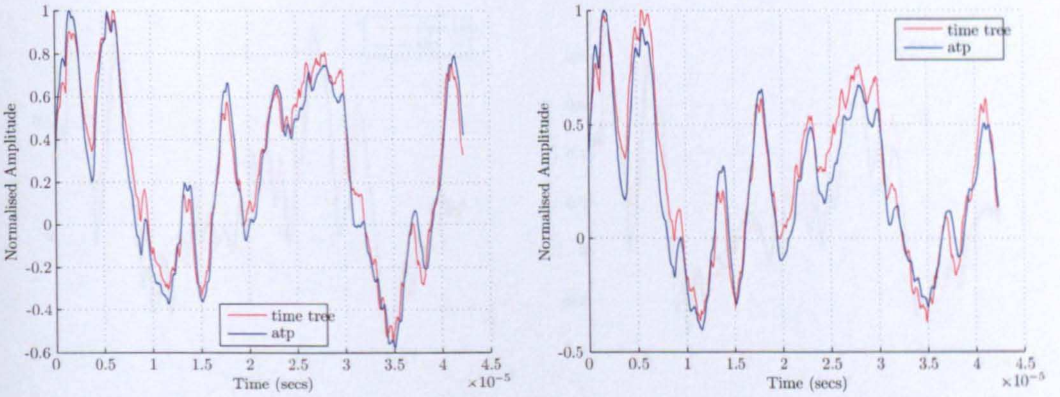


(a) 0 ohm (b) 100 ohm

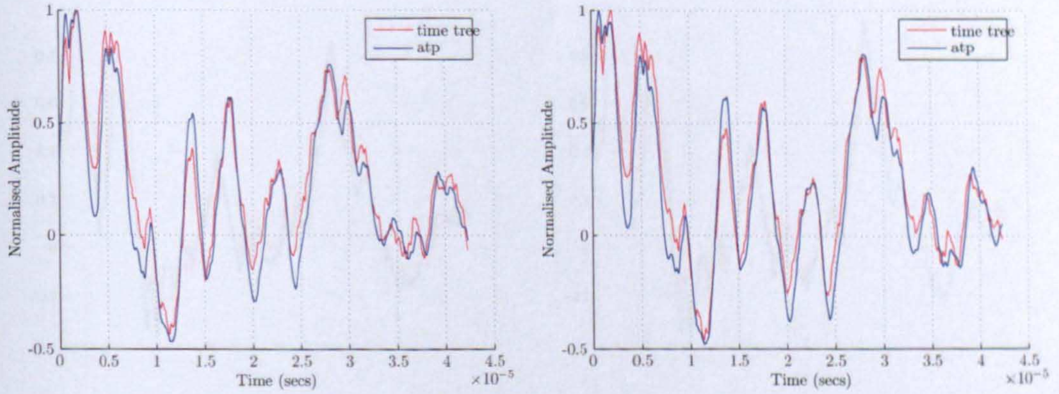


(c) 500 ohm (d) 1000 ohm

FIGURE D.5: Comparison of ATP simulation and time tree simulation for inter phase faults at location 1

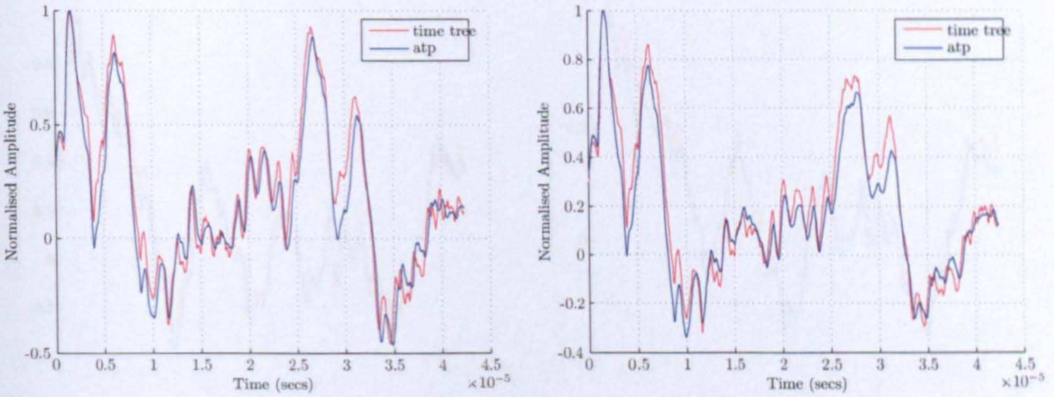


(a) 0 ohm (b) 100 ohm



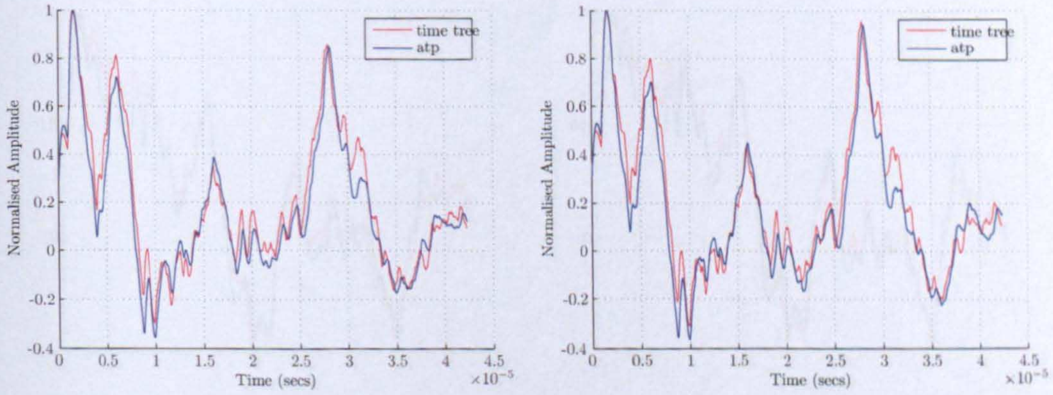
(c) 500 ohm (d) 1000 ohm

FIGURE D.6: Comparison of ATP simulation and time tree simulation for inter phase faults at location 2



(a) 0 ohm

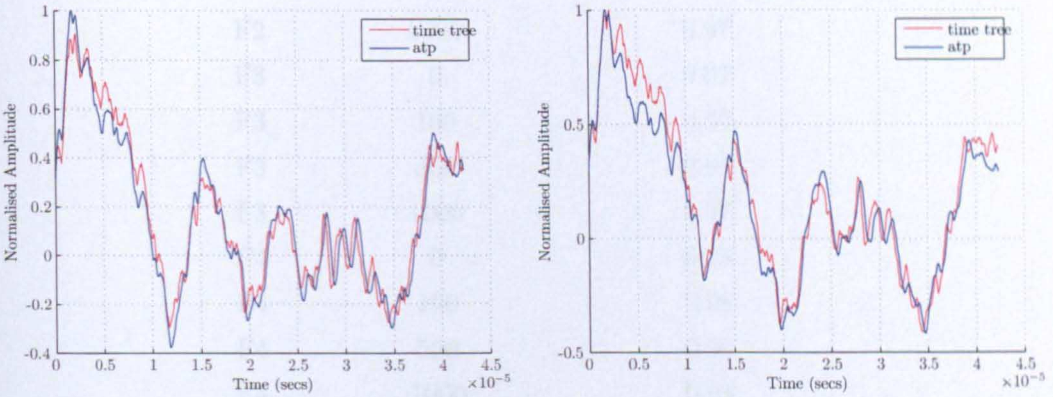
(b) 100 ohm



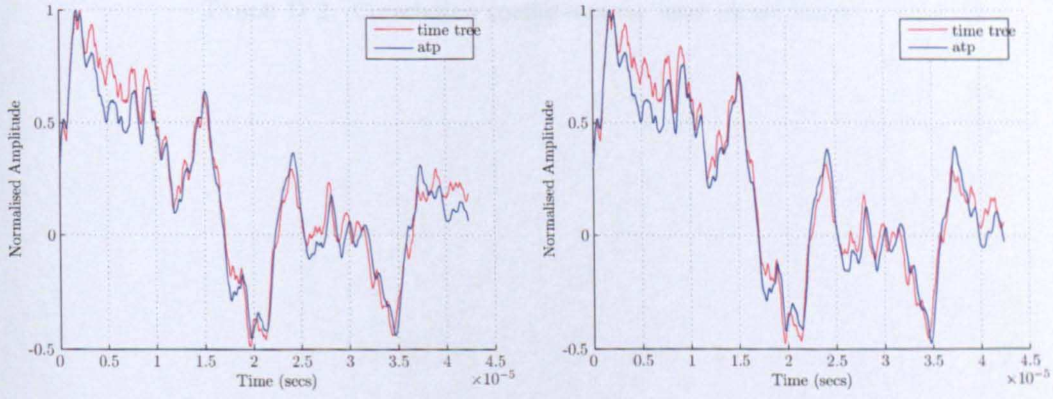
(c) 500 ohm

(d) 1000 ohm

FIGURE D.7: Comparison of ATP simulation and time tree simulation for inter phase faults at location 3



(a) 0 ohm (b) 100 ohm

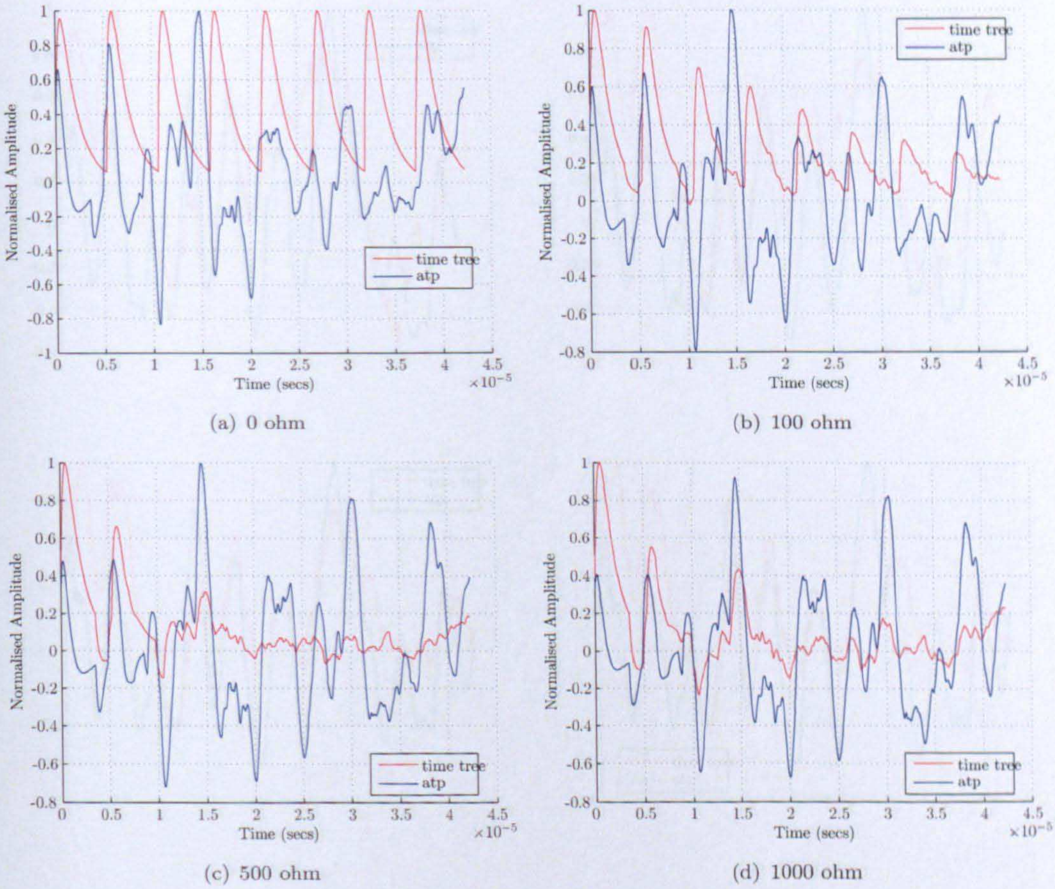


(c) 500 ohm (d) 1000 ohm

FIGURE D.8: Comparison of ATP simulation and time tree simulation for inter phase faults at location 3

| Fault ID | Fault Resistance | Correlation Coefficient |
|---|---|---|
| F1 | 0 | 0.91 |
| F1 | 100 | 0.95 |
| F1 | 500 | 0.96 |
| F1 | 1000 | 0.96 |
| F2 | 0 | 0.98 |
| F2 | 100 | 0.97 |
| F2 | 500 | 0.97 |
| F2 | 1000 | 0.97 |
| F3 | 0 | 0.97 |
| F3 | 100 | 0.97 |
| F3 | 500 | 0.98 |
| F3 | 1000 | 0.97 |
| F4 | 0 | 0.98 |
| F4 | 100 | 0.98 |
| F4 | 500 | 0.98 |
| F4 | 1000 | 0.98 |

TABLE D.2: Correlation coefficients for inter phase faults



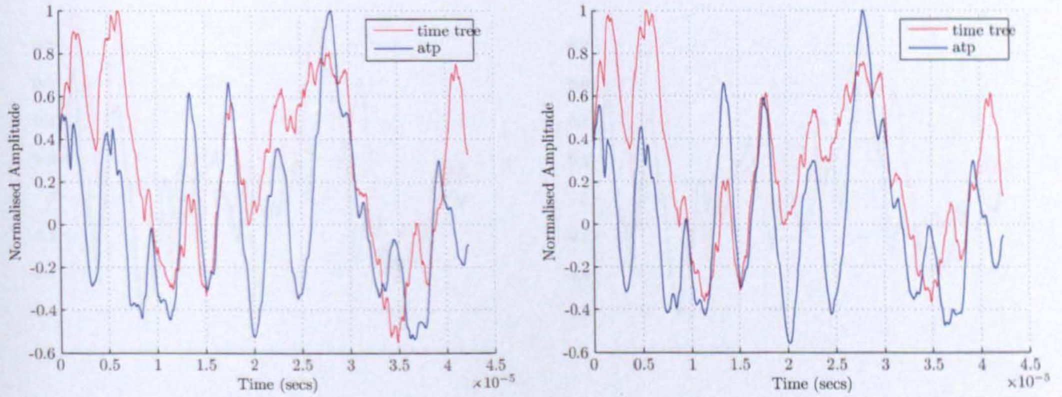
(a) 0 ohm

(b) 100 ohm

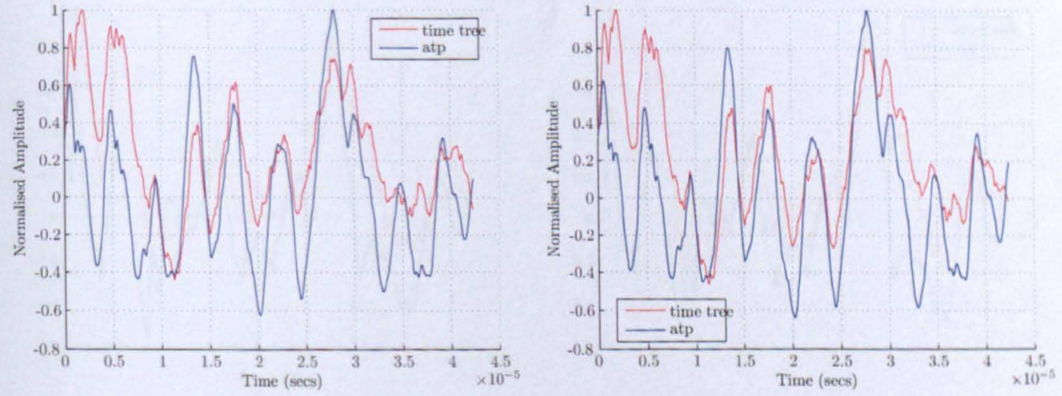
(c) 500 ohm

(d) 1000 ohm

FIGURE D.9: Comparison of ATP simulation and time tree simulation for single phase faults at location 1

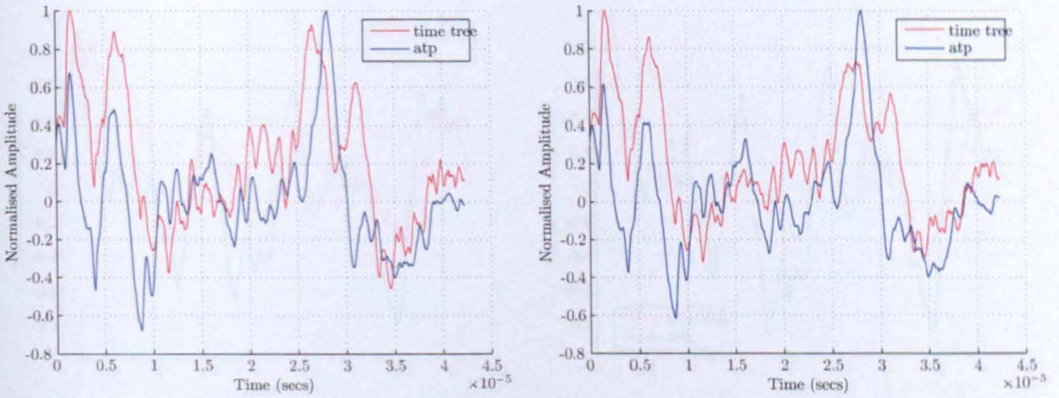


(a) 0 ohm (b) 100 ohm



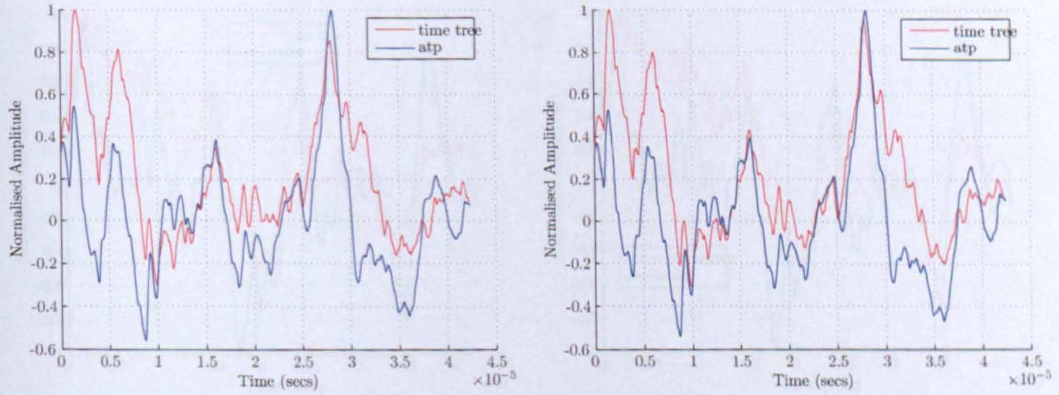
(c) 500 ohm (d) 1000 ohm

FIGURE D.10: Comparison of ATP simulation and time tree simulation for single phase faults at location 2



(a) 0 ohm

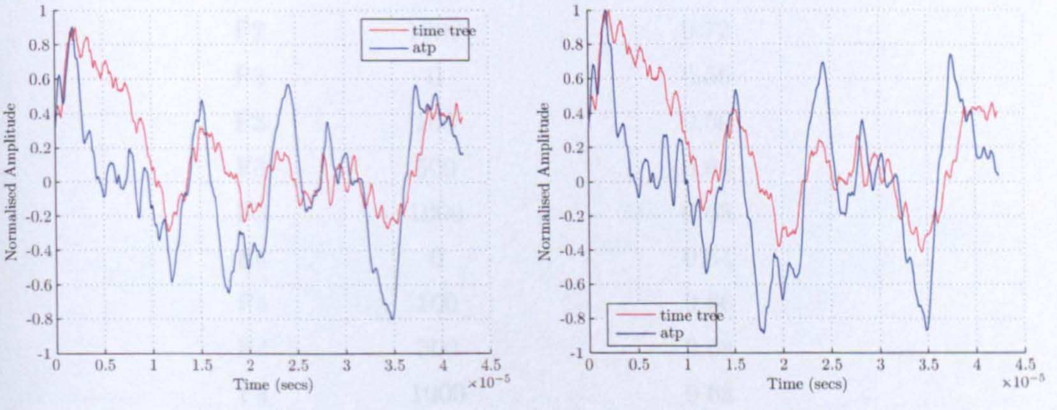
(b) 100 ohm



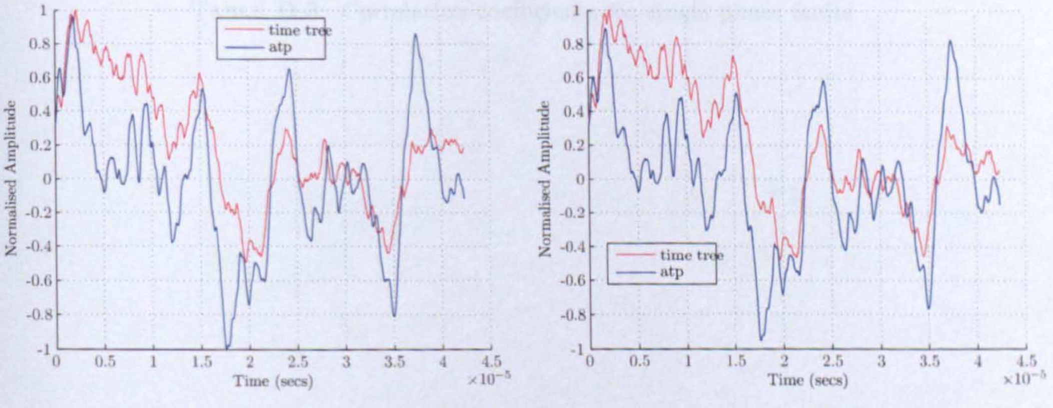
(c) 500 ohm

(d) 1000 ohm

FIGURE D.11: Comparison of ATP simulation and time tree simulation for single phase faults at location 3



(a) 0 ohm (b) 100 ohm

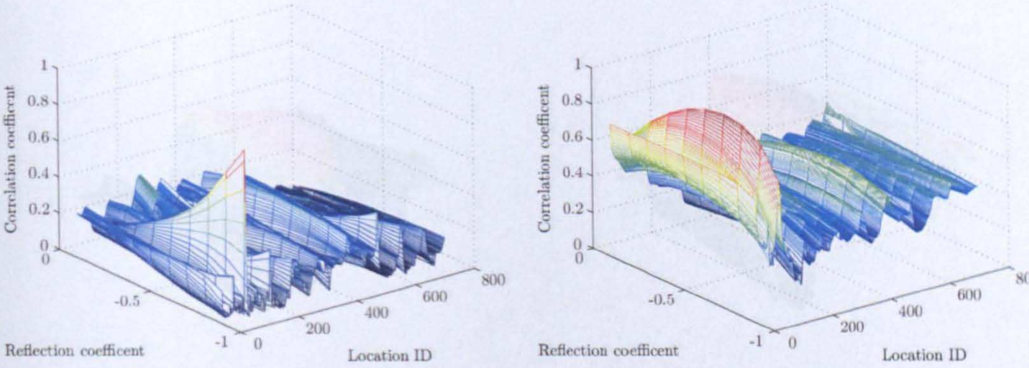


(c) 500 ohm (d) 1000 ohm

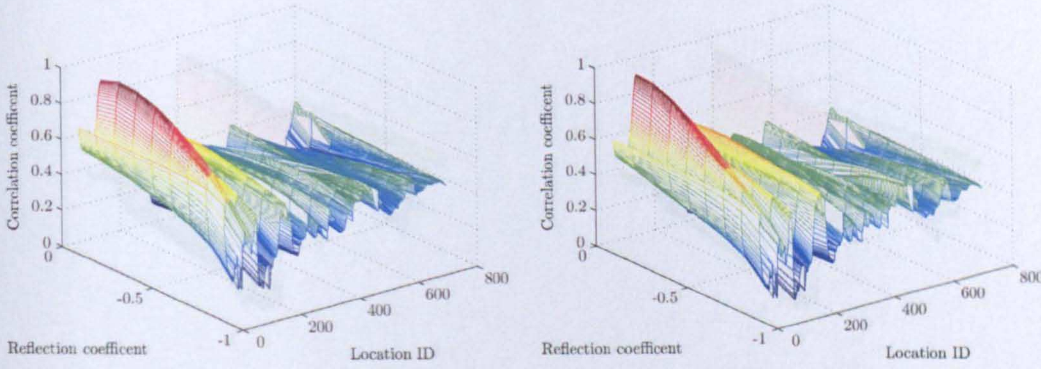
FIGURE D.12: Comparison of ATP simulation and time tree simulation for single phase faults at location 3

| Fault ID | Fault Resistance | Correlation Coefficient |
|---|---|---|
| F1 | 0 | 0.05 |
| F1 | 100 | 0.08 |
| F1 | 500 | 0.25 |
| F1 | 1000 | 0.38 |
| F2 | 0 | 0.59 |
| F2 | 100 | 0.61 |
| F2 | 500 | 0.68 |
| F2 | 1000 | 0.72 |
| F3 | 0 | 0.56 |
| F3 | 100 | 0.59 |
| F3 | 500 | 0.64 |
| F3 | 1000 | 0.68 |
| F4 | 0 | 0.64 |
| F4 | 100 | 0.66 |
| F4 | 500 | 0.68 |
| F4 | 1000 | 0.68 |

TABLE D.3: Correlation coefficients for singla phase faults

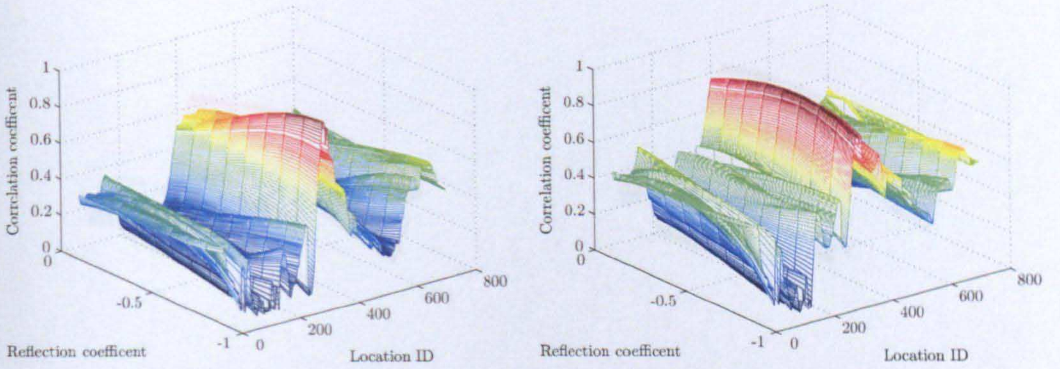


(a) 0 ohm (b) 100 ohm

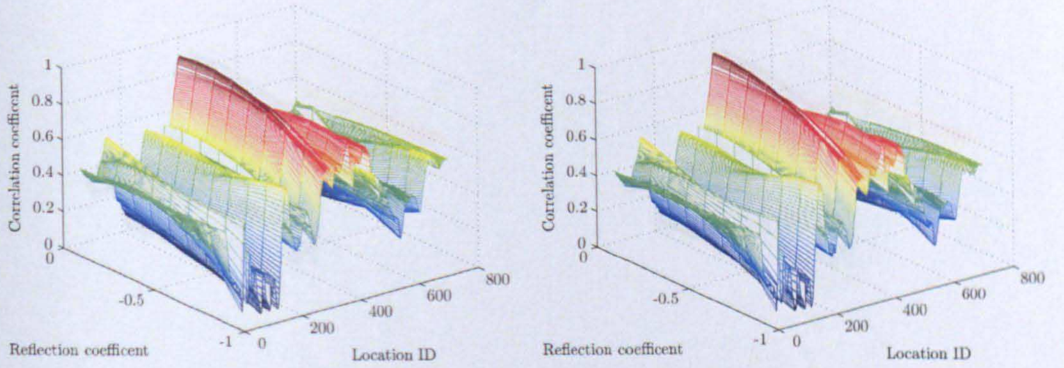


(c) 500 ohm (d) 1000 ohm

FIGURE D.13: Solution space for a three phase faults at fault location 1

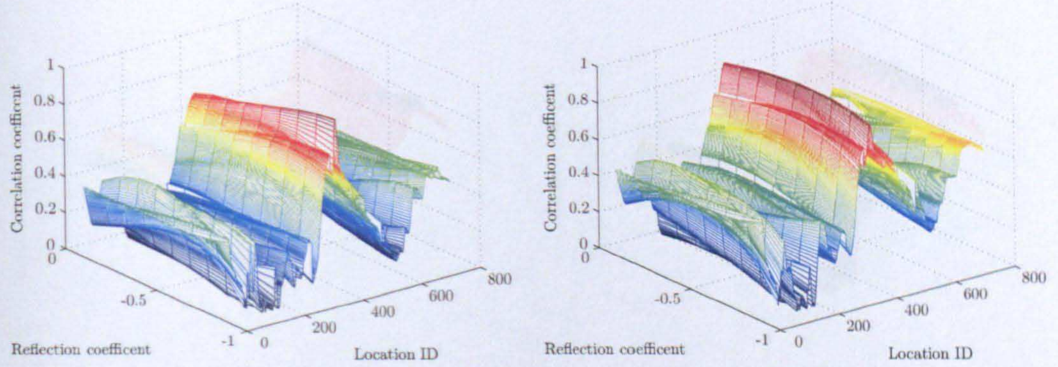


(a) 0 ohm (b) 100 ohm

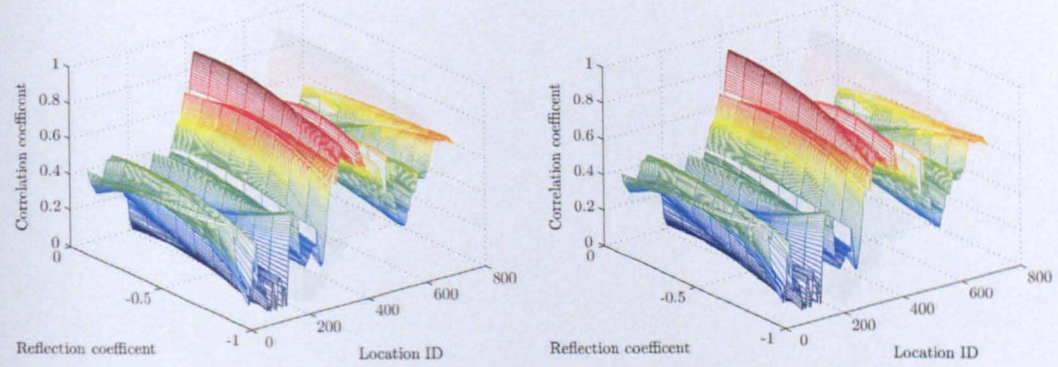


(c) 500 ohm (d) 1000 ohm

FIGURE D.14: Solution space for a three phase faults at fault location 2

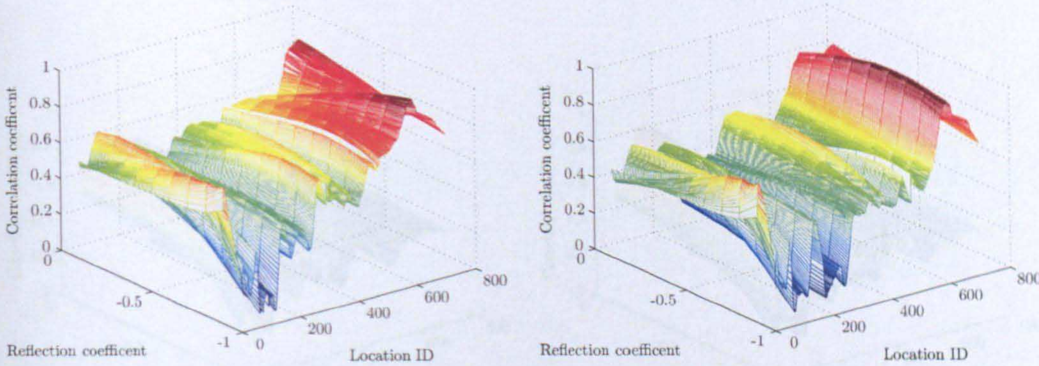


(a) 0 ohm (b) 100 ohm

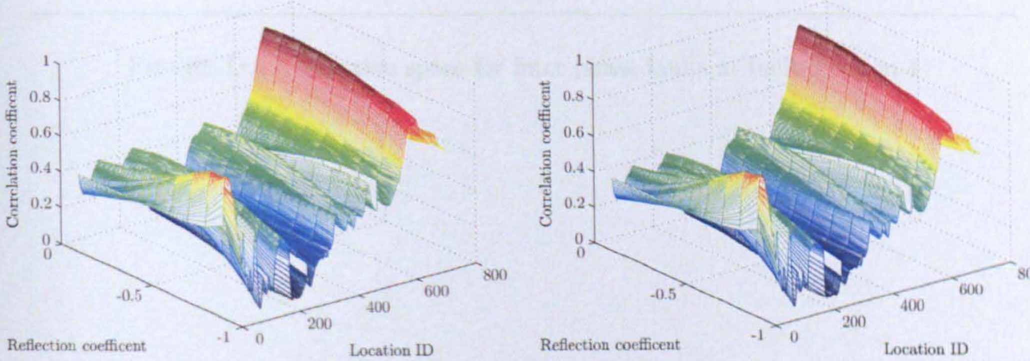


(c) 500 ohm (d) 1000 ohm

FIGURE D.15: Solution space for a three phase faults at fault location 3

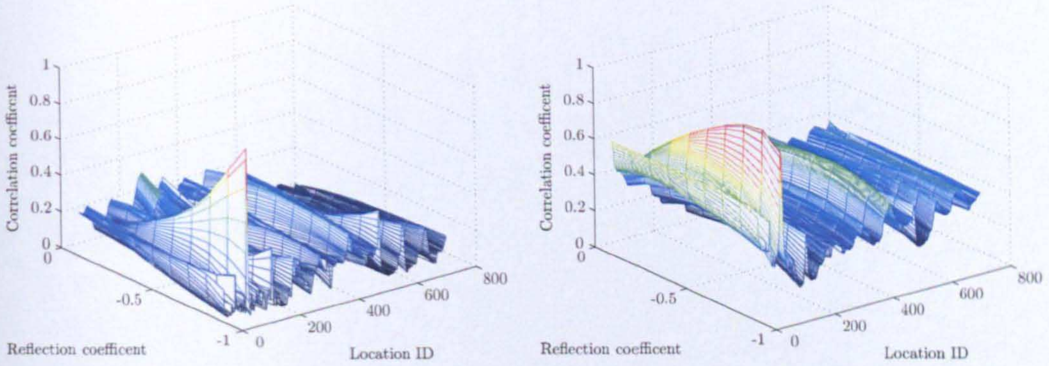


(a) 0 ohm (b) 100 ohm

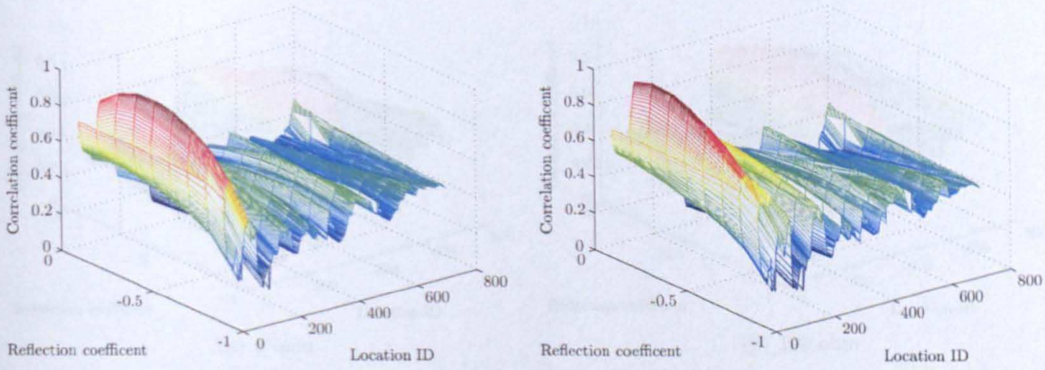


(c) 500 ohm (d) 1000 ohm

FIGURE D.16: Solution space for a three phase faults at fault location 4

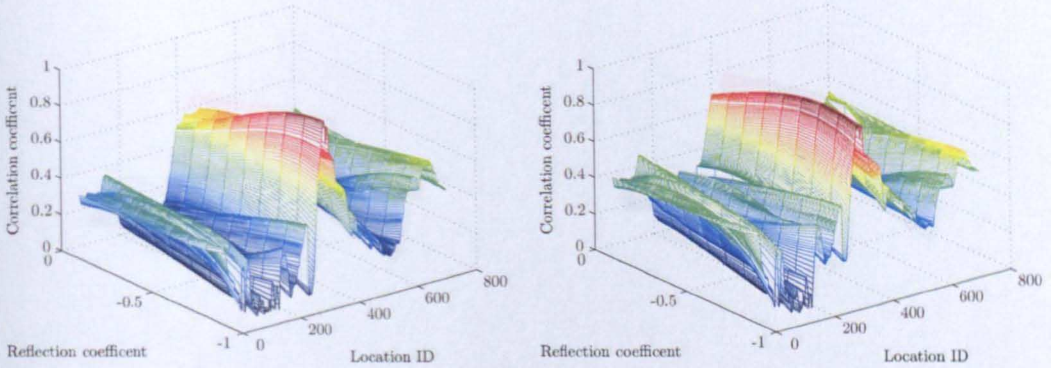


(a) 0 ohm (b) 100 ohm

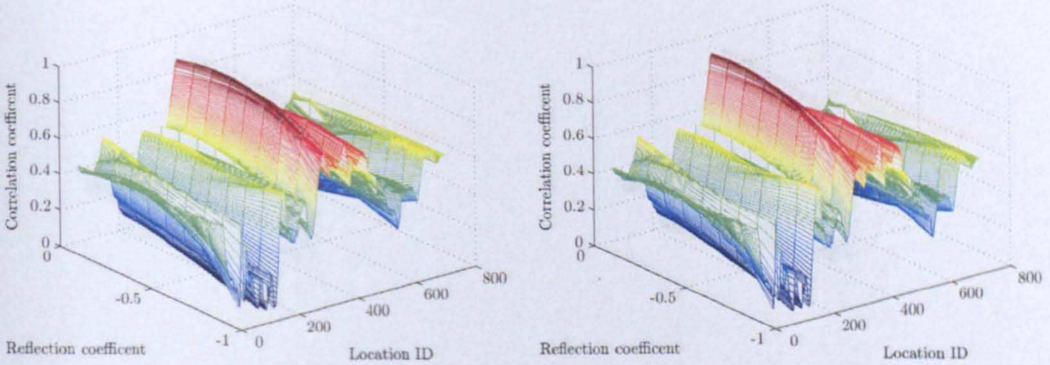


(c) 500 ohm (d) 1000 ohm

FIGURE D.17: Solution space for inter phase faults at fault location 1

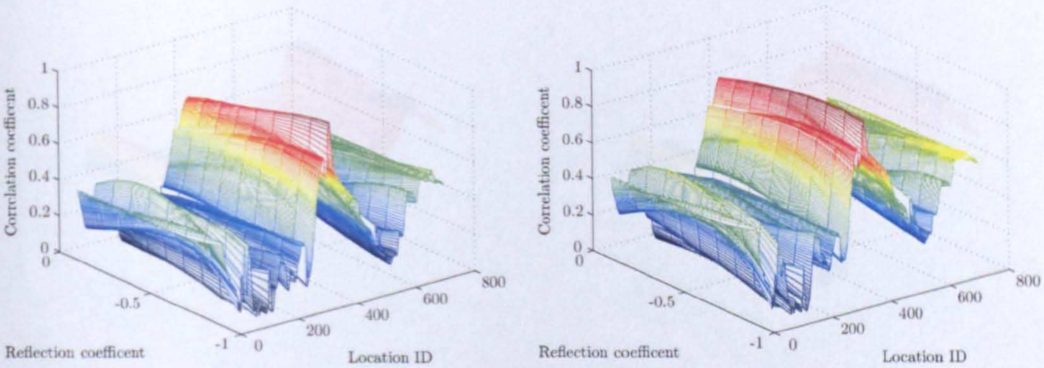


(a) 0 ohm (b) 100 ohm

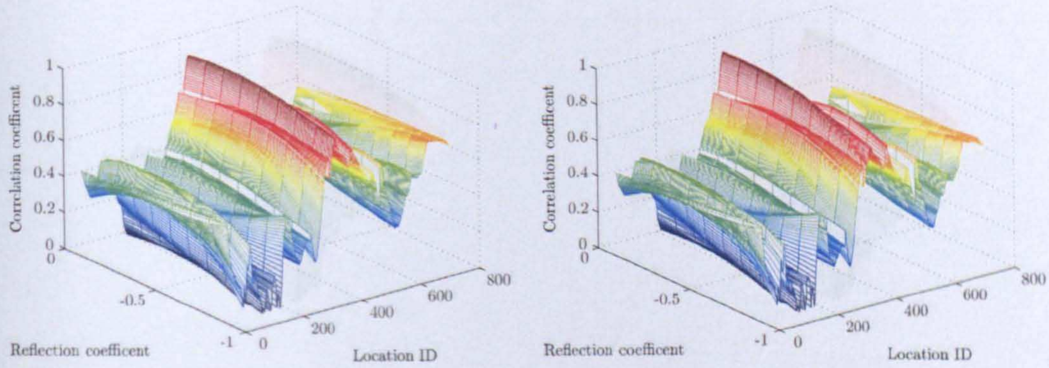


(c) 500 ohm (d) 1000 ohm

FIGURE D.18: Solution space for inter phase faults at fault location 2

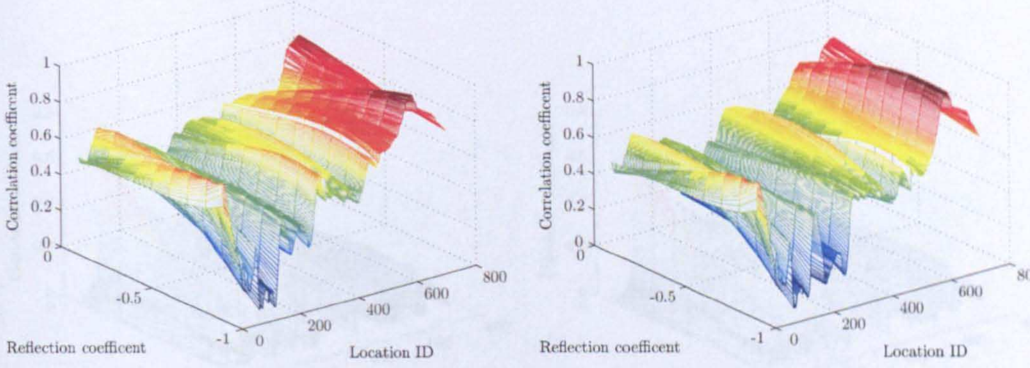


(a) 0 ohm (b) 100 ohm

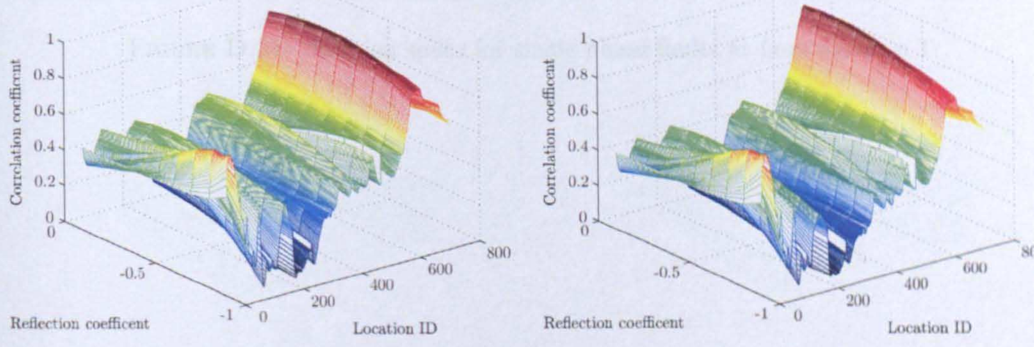


(c) 500 ohm (d) 1000 ohm

FIGURE D.19: Solution space for inter phase faults at fault location 3

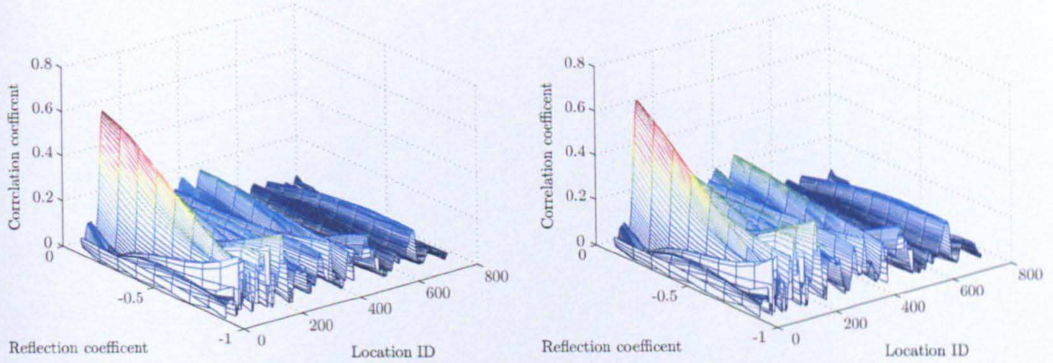


(a) 0 ohm (b) 100 ohm

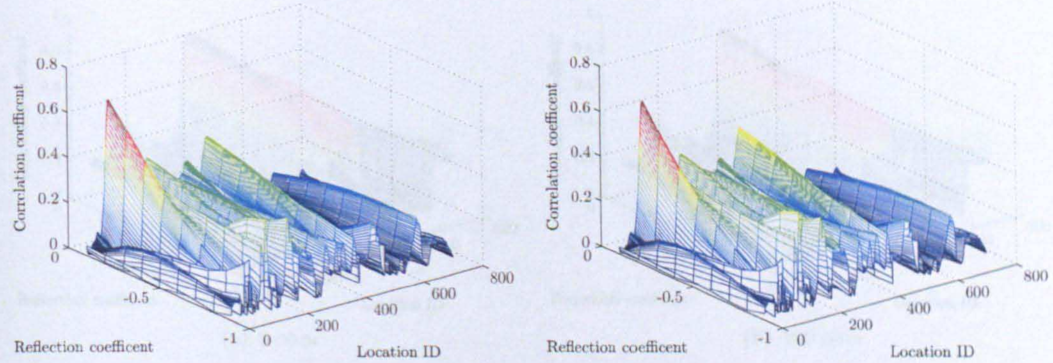


(c) 500 ohm (d) 1000 ohm

FIGURE D.20: Solution space for inter phase faults at fault location 4

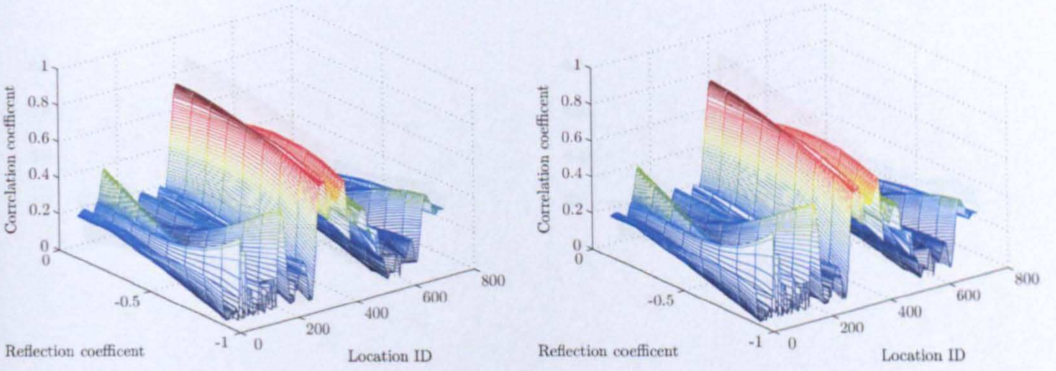


(a) 0 ohm (b) 100 ohm



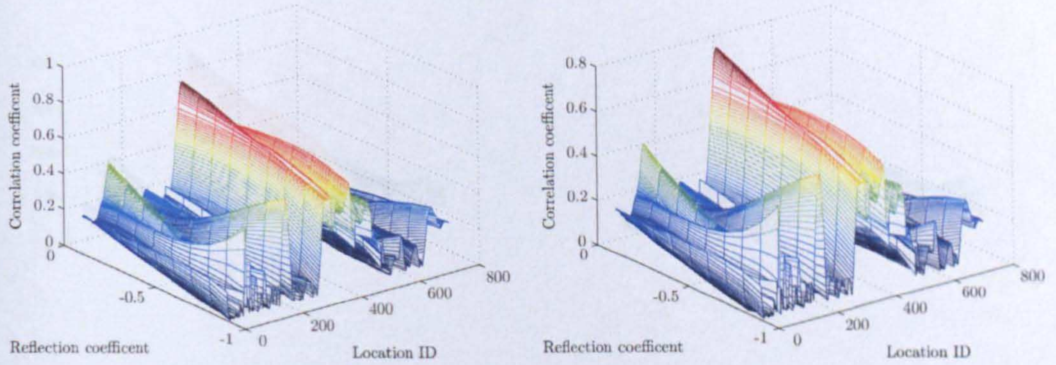
(c) 500 ohm (d) 1000 ohm

FIGURE D.21: Solution space for single phase faults at fault location 1



(a) 0 ohm

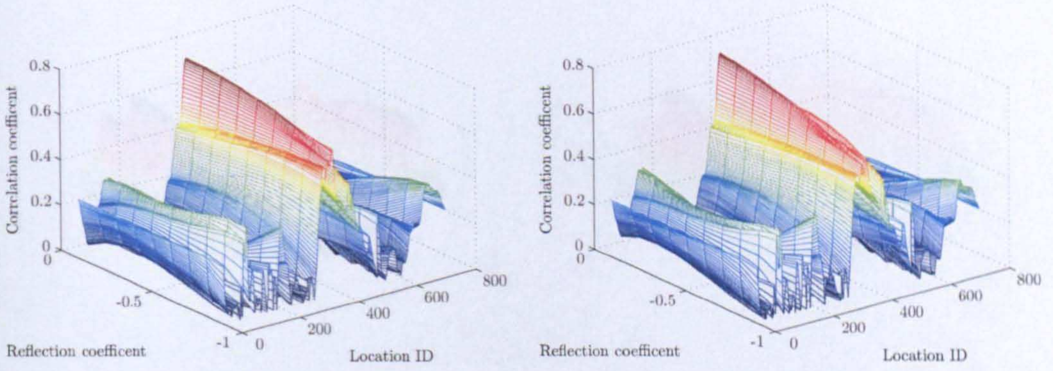
(b) 100 ohm



(c) 500 ohm

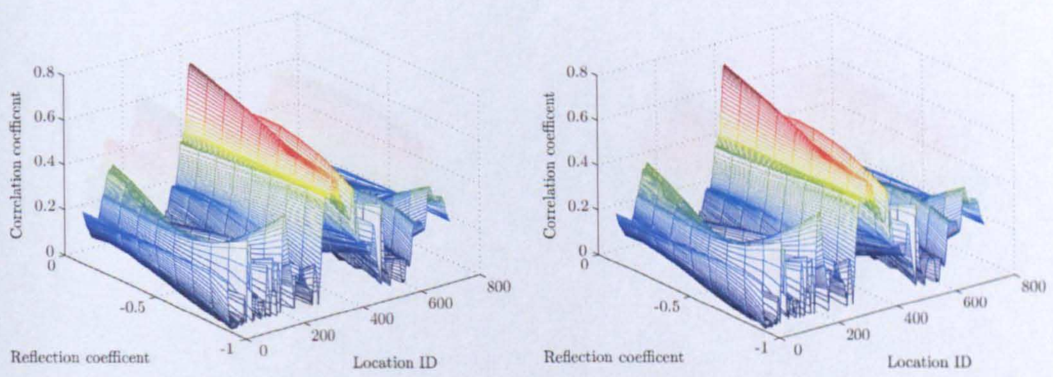
(d) 1000 ohm

FIGURE D.22: Solution space for single phase faults at fault location 2



(a) 0 ohm

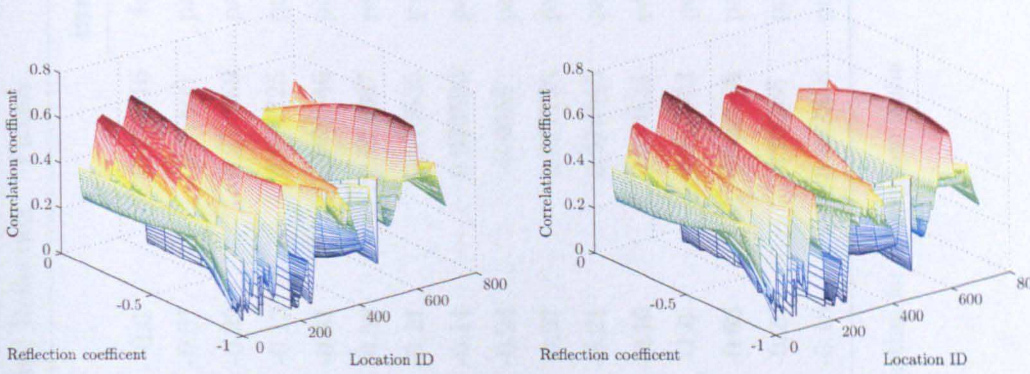
(b) 100 ohm



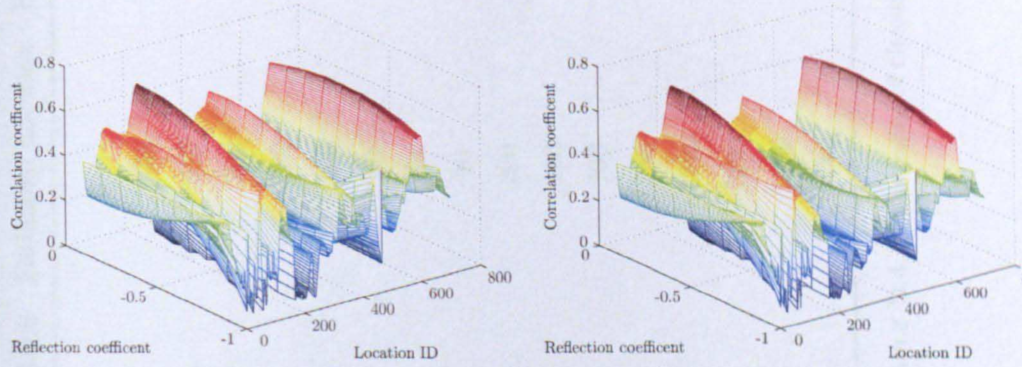
(c) 500 ohm

(d) 1000 ohm

FIGURE D.23: Solution space for single phase faults at fault location 3



(a) 0 ohm (b) 100 ohm



(c) 500 ohm (d) 1000 ohm

FIGURE D.24: Solution space for single phase faults at fault location 4

| Fault | Resistance | Estimated Branch | Estimated Location | Estimated Reflection | Fitness | Error (%) | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Branch | Distance | Reflection |
| F1 | 0 | 2 | 640 | -0.0 | 0.456416 | fail | n/a | n/a |
| F1 | 100 | 0 | 810 | -0.61 | 0.97806 | pass | 0.16 | 21 |
| F1 | 500 | 0 | 780 | -0.22 | 0.974369 | pass | 0.32 | 26 |
| F1 | 1000 | 0 | 780 | -0.13 | 0.974725 | pass | 0.32 | 19 |
| F2 | 0 | 5 | 100 | -0.91 | 0.979546 | pass | 0.0 | 9 |
| F2 | 100 | 5 | 80 | -0.58 | 0.974087 | pass | 0.75 | 24 |
| F2 | 500 | 5 | 90 | -0.21 | 0.976635 | pass | 0.38 | 27 |
| F2 | 1000 | 5 | 90 | -0.11 | 0.976593 | pass | 0.38 | 21 |
| F3 | 0 | 6 | 200 | -0.94 | 0.9658 | pass | 0.0 | 6 |
| F3 | 100 | 6 | 190 | -0.57 | 0.977736 | pass | 0.36 | 25 |
| F3 | 500 | 6 | 190 | -0.21 | 0.978946 | pass | 0.36 | 27 |
| F3 | 1000 | 6 | 200 | -0.16 | 0.974831 | pass | 0.0 | 11 |
| F4 | 0 | 10 | 1220 | -1.0 | 0.981923 | pass | 0.40 | 0 |
| F4 | 100 | 10 | 1200 | -0.63 | 0.982966 | pass | 0.0 | 19 |
| F4 | 500 | 10 | 1180 | -0.26 | 0.98288 | pass | 0.40 | 22 |
| F4 | 1000 | 10 | 1180 | -0.16 | 0.982358 | pass | 0.40 | 16 |

TABLE D.4: Performance of Genetic Algorithm for three phase faults

| Fault | Resistance | Estimated Branch | Estimated Location | Estimated Reflection | Fitness | Error (%) | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Branch | Distance | Reflection |
| F1 | 0 | 2 | 600 | -0.01 | 0.458868 | fail | n/a | n/a |
| F1 | 100 | 0 | 810 | -0.77 | 0.981975 | pass | 0.16 | 5 |
| F1 | 500 | 0 | 800 | -0.37 | 0.976043 | pass | 0.0 | 11 |
| F1 | 1000 | 0 | 780 | -0.22 | 0.974341 | pass | 0.32 | 10 |
| F2 | 0 | 5 | 130 | -0.92 | 0.969138 | pass | 1.13 | 8 |
| F2 | 100 | 5 | 100 | -0.8 | 0.971607 | pass | 0.0 | 2 |
| F2 | 500 | 5 | 90 | -0.4 | 0.976358 | pass | 0.38 | 8 |
| F2 | 1000 | 5 | 90 | -0.23 | 0.976791 | pass | 0.38 | 9 |
| F3 | 0 | 6 | 200 | -0.94 | 0.965781 | pass | 0.0 | 6 |
| F3 | 100 | 6 | 210 | -0.76 | 0.977157 | pass | 0.36 | 6 |
| F3 | 500 | 6 | 190 | -0.35 | 0.979535 | pass | 0.36 | 13 |
| F3 | 1000 | 6 | 190 | -0.21 | 0.978962 | pass | 0.36 | 11 |
| F4 | 0 | 10 | 1220 | -1.0 | 0.981946 | pass | 0.40 | 0.0 |
| F4 | 100 | 10 | 1190 | -0.77 | 0.980606 | pass | 0.20 | 5 |
| F4 | 500 | 10 | 1190 | -0.4 | 0.983172 | pass | 0.20 | 8 |
| F4 | 1000 | 10 | 1180 | -0.26 | 0.982887 | pass | 0.40 | 6 |

TABLE D.5: Performance of Genetic Algorithm for inter phase faults

| Fault | Resistance | Estimated Branch | Estimated Location | Estimated Reflection | Fitness | Error (%) | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Branch | Distance | Reflection |
| F1 | 0 | 0 | 790 | -0.04 | 0.618411 | pass | 0.16 | 96 |
| F1 | 100 | 0 | 780 | -0.0 | 0.677667 | pass | 0.32 | 82 |
| F1 | 500 | 0 | 790 | -0.08 | 0.677912 | pass | 0.16 | 40 |
| F1 | 1000 | 0 | 750 | -0.02 | 0.668118 | pass | 0.79 | 30 |
| F2 | 0 | 5 | 120 | -0.13 | 0.813531 | pass | 0.75 | 87 |
| F2 | 100 | 5 | 110 | -0.08 | 0.824174 | pass | 0.38 | 74 |
| F2 | 500 | 5 | 110 | -0.01 | 0.822961 | pass | 0.38 | 47 |
| F2 | 1000 | 5 | 110 | -0.0 | 0.817863 | pass | 0.38 | 32 |
| F3 | 0 | 6 | 220 | -0.07 | 0.756787 | pass | 0.72 | 93 |
| F3 | 100 | 6 | 190 | -0.0 | 0.774469 | pass | 0.36 | 82 |
| F3 | 500 | 6 | 220 | -0.0 | 0.783294 | pass | 0.72 | 48 |
| F3 | 1000 | 6 | 220 | -0.0 | 0.778039 | pass | 0.36 | 32 |
| F4 | 0 | 10 | 1230 | -0.8 | 0.679664 | pass | 0.60 | 20 |
| F4 | 100 | 2 | 300 | -0.05 | 0.692498 | fail | n/a | n/a |
| F4 | 500 | 2 | 320 | -0.06 | 0.695339 | fail | n/a | n/a |
| F4 | 1000 | 2 | 340 | -0.09 | 0.686838 | fail | n/a | n/a |

TABLE D.6: Performance of Genetic Algorithm for single phase faults

The performance of the genetic algorithm for 3 phase and inter phase fault is very similar to the performance when the higher cut-off frequency of 10 MHz was used. It can be concluded that there is enough information contained within the traveling wave fault signature that has been filtered at 500 kHz. The only exception is close up faults which for the zero ohm fault, failed to locate the correct branch. The reason for this is the sharp ridge that occurs in the solution space which is difficult for the genetic algorithm to climb.

The performance of the genetic algorithm for single phase faults was similar to the performance with the higher cut-off frequency of 10 MHz except for location 4. This is because of a false ridge that appears in the solution space which is higher that the ridge corresponding to the correct fault location. The genetic algorithm correctly identifies the highest ridge in the solution space but this will not give the correct fault location. The time tree could be improved to correctly model the ground mode propagation to remove the unwanted ridge from the solution space.

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