The University of Nottingham
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ELECTRICAL PROPERTIES OF III-V ANTIMONIDE/GaAs HETEROSTUCTURES GROWN BY INTERFACIAL MISFIT MOLECULAR BEAM EPITAXY TECHNIQUE

by

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ABSTRACT

Lattice mismatched heterostructures grown by Interfacial Misfit (IMF) technique, which allows the strain energy to be relieved both laterally and perpendicularly from the interfaces, are investigated. However, electrically active defects are created at the interface and away from the interface with energy levels deep in the bandgap of the host materials. These defects dramatically affect the optical and electrical properties of the devices.

In this thesis, an investigation of deep level defects is carried out on GaSb/GaAs uncompensated and Te compensated heterostructures grown by the IMF method using DLTS, Laplace DLTS, I-V, C-V, C-F and C-G-F measurements. Furthermore, the effect of thermal annealing treatments on the defect states is also studied on both types of samples. It was found that the well-known EL2 electron trap is commonly observed near to the interface of both uncompensated and Te compensated GaSb/GaAs IMF samples. However, several additional electron defects are detected in Te compensated samples.

Rapid thermal annealing performed on uncompensated samples resulted in the annihilation of the main electron trap EL2 at a temperature of 600 ^{o}C. On the other hand rapid thermal annealing and conventional furnace annealing were carried out on Te compensated samples, and it was observed that rapid thermal annealing process is more effective in terms of defects reduction.

The density of interface states is determined from C-G-F and forward bias DLTS measurements. Te compensated samples exhibit the highest density of interface states and have additional hole traps as compared to uncompensated samples.

The electrical properties of p-i-n GaInAsSb photodiodes grown on uncompensated and Te compensated GaSb/GaAs templates on GaAs substrates using special growth mode are investigated. The non-radiative defects which could have detrimental effects on the performance of these photo diodes are studied here for the first time. Both electron and hole defects are detected, and their capture cross-section measurements reveal that some of defects originate from threading dislocations. The double pulse DLTS measurements are performed and the concentration distributions of the detected defects are determined.

PUBLICATIONS

1. Electrical Characterisation of Deep Level Defects in Be-doped AlGaAs Grown on (100) and (311) A GaAs Substrates by MBE.
   Riaz H Mari, Muhammad Shafi, Mohsin Aziz, Almontaser Khatab, David Taylor, Mohamed Henini
   Nanoscale Research Letters, 6, 180 (2011)

2. Effect of Epitaxial Layer Thickness on the Deep Level Defects in MBE Grown n-Type $Al_{0.33}Ga_{0.67}As$.
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10. Effect of Substrate Orientation on the Electrical Properties of Polyaniline Grown on GaAs (311)B and (100)
Dler Jameel, Jorlandio Felix, Mohsin Aziz, Noor Saqri, David Taylor, Walter de Azevedo, Eronides da Silva, Mohamed Henini
Submitted to J. Physics: Applied Physics D

CONFERENCE PRESENTATIONS

ORAL TALK

- "Deep level transient spectroscopy (DLTS) characterisation of defects in AlGaN/Si dual-band (UV/IR) detectors grown by MBE"

  International Conference on Extended defects in semiconductors (EDS), Thessaloniki, Greece, 24-29 June, (2012)

POSTER PRESENTATIONS

- "Growth and characterization of InGaN Grown by MBE for photovoltaic"

  Sustainable Chemical and Biological Processing (SCBP) Priority Group, Nottingham, United Kingdom, 18 December, (2012).

- "Laplace Deep-level Transient Spectroscopy of Cubic-GaN Grown by MBE on SiC"

  International Conference on Semiconducting and Insulating Materials (SIMC- XVI), Stockholm, Sweden, June 20-23, (2011).

- "Deep-level Transient Spectroscopy and Conductance Measurements of Interfacial States in "Buffer-Free" p-i-n GaSb/GaAs Devices"

  International Conference on Defects Recognition, Imaging and Physics in Semiconductors, Warsaw, Poland, September 15-19, (2013).

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ACRONYMS

The following acronym will be used throughout the thesis.

DLTS	DEEP LEVEL TRANSIENT SPECTROSCOPY
Laplace DLTS	Laplace DEEP LEVEL TRANSIENT SPECTROSCOPY
I-V	Current-Voltage
C-V	Capacitance-Voltage
C-F	Capacitance-Frequency
C-G-F	Capacitance-Conductance-Frequency

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

The development of III-V compound materials started in 1930, however the interest in III-V materials such as Indium Antimonide (InSb) and Gallium Arsenide (GaAs) boosted in 1950 with the discovery that these materials have similar crystal structures as group IV semiconductors such as Si and Ge. The importance of III-V compound semiconductors increased further after the advent of non-equilibrium growth techniques such as Molecular Beam Epitaxy (MBE) in the early 1980's. This epitaxial technique offers tremendous tailoring capabilities for device fabrication by forming compound materials from these semiconductors. The other most commonly used epitaxial techniques are Metalorganic Chemical Vapor Deposition (MOCVD) and Metalorganic Vapor Phase Epitaxy (MOVPE). One of most studied III-V semiconductor material is GaAs. It is the building block of high frequency and optoelectronic devices. Due to its six time higher electron mobility at room temperature compared to conventional elemental Si substrate, it is one of the materials of choice for high speed devices operating above 200GHz [1]. Single crystal GaAs wafers are commercially available for the epitaxial growth of similar or other III-V compound semiconductors. The lattice matching to the substrate is desirable to achieve high quality epitaxial layers. Due to this constraint, there is a limited choice of materials that can be grown on GaAs.

The development of advanced processing and growth techniques enabled the creation of integrated devices. However, the integration of heterojunctions requires reliable interfaces where the interfacing materials have different crystalline properties. For example if the lattice constants of the materials forming a heterojunction are different then this results in a build-up of compressive or tensile strain. The relaxation of such strain leads to structural defects in the devices. One method employed to avoid such defects is the use of a thick buffer layer involving long growth times. This approach affects cost and also the performance of the devices.

Heterostructures are formed by making chemical bonds at the interface between two materials. Usually such heterostructures are fabricated by epitaxial growth techniques on a substrate. If the lattice constant of the two materials are the same then the interfaces are smooth. However, this is rarely the case as most materials have different lattice constants and a misfit is created between them. This lattice mismatch, F, can be calculated as

$$F = \frac{a_{sub} - a_{epi}}{a_{sub}}$$

where a_{sub} and a_{epi} are the lattice constants of substrate and epilayers, respectively. The mismatch is undesirable because of the creation of dislocations which can propagate to the active region of devices and act as short circuits resulting in large reverse currents. It is accepted that a mismatch of < 2% does not affect the operation of devices. The misfit is classified into three categories, namely low (< 2%), moderate (3-4%) and high (> 6%) [2]. Figure 1.1 shows the energy gaps and lattice constants of some of the most common semiconductors.

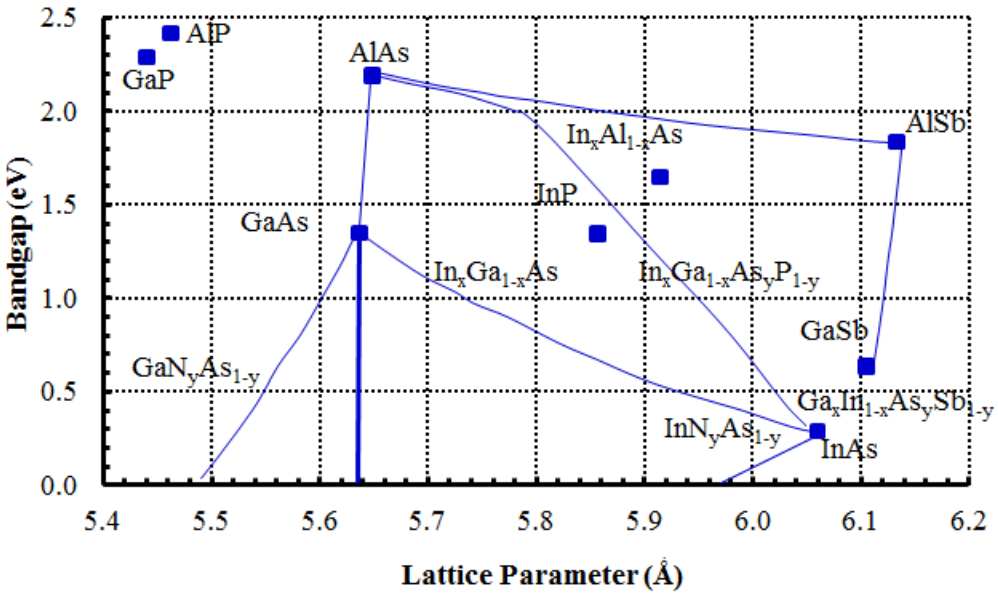

Figure 1.1: energy gaps and lattice constants of few common III-V semiconductors.

The dislocation at the interface of heterostructures takes many forms depending on the dislocation direction with respect to the alignment with interface. In order to distinguish between the different types of dislocations an angle needs to be determined with respect to their orientation. In order to specify the angle of the dislocation, two vectors are needed, namely, the Burgers vector and the dislocation vector (dislocation line). In 2D primitive square lattice, the Burgers vector can be determined by the following steps: (1) trace a closed loop around the dislocation line in 2D square lattice as shown in Figure 1.2a; (2) trace out a similar path in a perfect crystal by moving by the same number of lattice vectors along each direction as illustrated in Figure 1.2b. The loop will not complete and closer failure is called Burgers vector as shown in Figure 1.2b.

In order to define the angle a second vector, called dislocation line or dislocation vector, that describes the direction of the dislocation is required. If the dislocation is continuous in a crystal it would be symmetrical around the dislocation line. For

example, Figure 1.2a represents a sign ⊥ in which the line perpendicular to the page is the dislocation line. One can characterize the dislocation by the angle between the Burgers vector and the dislocation line. In Figure 1.2a the angle between the dislocation line and Burgers vector is 90^{o}. This dislocation, called edge dislocation, appears in two dimensional planes and does not propagate out of the planes. In other words such dislocations, which appear at the interface of heterojunctions and remain at the interface, do not propagate into the active region of devices.

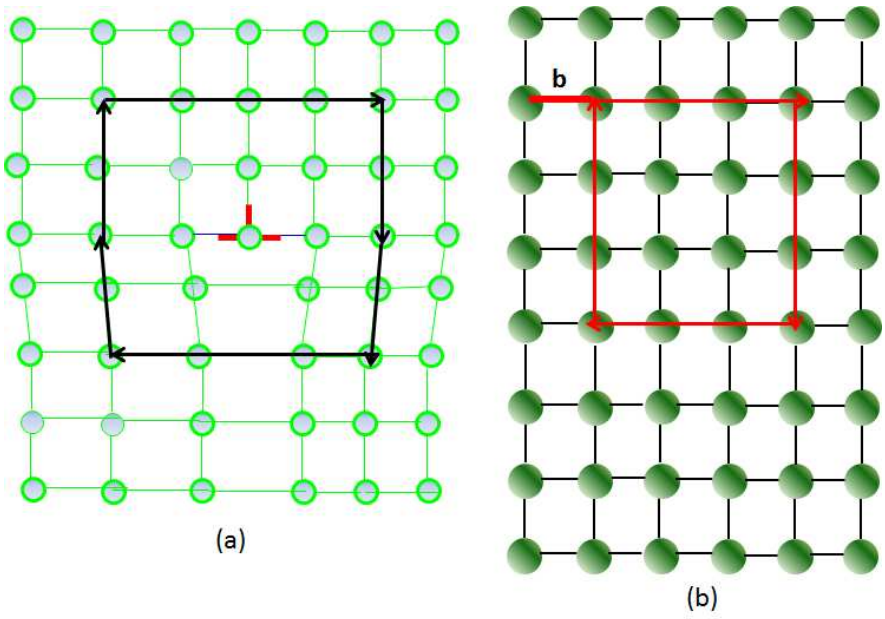

Figure 1.2 (a) The structure of a crystal with a line defect and Burgers circuit, and (b) The perfect crystal structure with Burgers vector [3].

However, for the case of screw dislocations the angle between the dislocation line and the Burgers vector is 0^{o} as shown in Figure 1.3. This type of dislocation can easily propagate towards the surface and cause serious issues. Other types of dislocation that propagate into the active region of devices include those with 30^{o} and 60^{o}. These dislocations, which decrease the recombination rates of electron

and holes and hence decrease the minority carrier life time, have detrimental effects on devices based on minority carriers such as solar cells. For example, the dislocations induced defects reduce dramatically the efficiency of solar cells [4]. Similarly the increased nonradiative recombination rates also decreases the luminescence and operational efficiencies of LEDs and lasers [5].

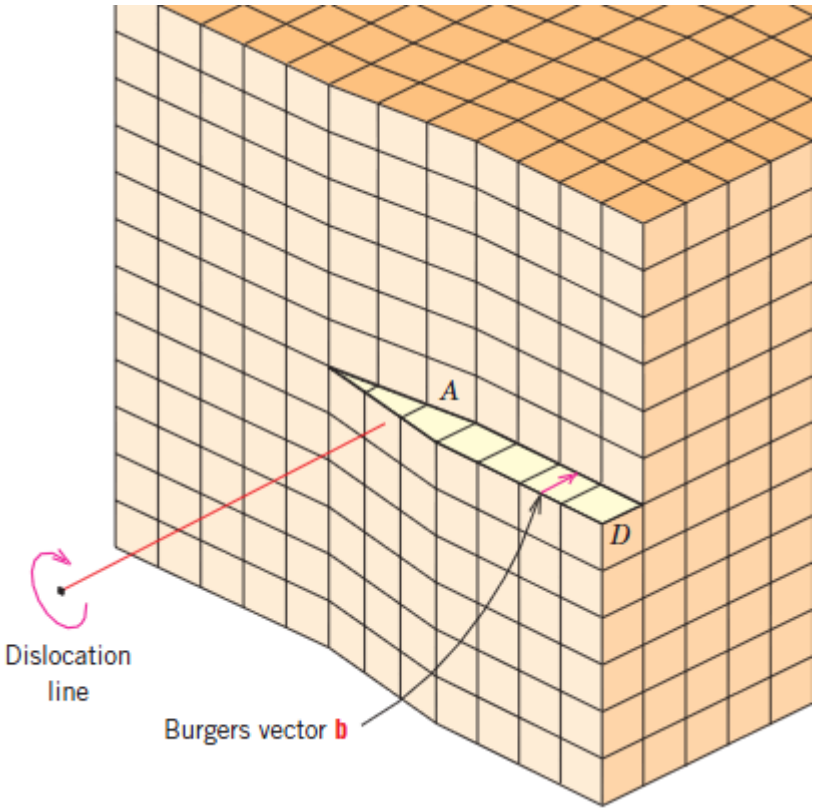

Figure 1.3: Determination of Burgers vector from screw dislocation (angle between dislocation line and Burgers vector **b** is 0^{o}) [6].

One of the difficulties of growing Sb-based optoelectronic devices is the dislocations induced during the epitaxial growth on either Si or GaAs substrates. Reliable devices rely on smooth interfaces which are not affected by edge dislocations. In this way cost effective and better efficiency Sb-based devices can

be epitaxially grown on GaAs substrates. The current method that is being investigated to avoid problems of mis-matching and achieving smooth interfaces is the creation of highly periodic edge dislocations at the interface between two materials. This periodic arrangement of dislocations, the so-called interfacial misfit array (IMF), is used to grow GaSb/GaAs heterostructures [2]. The strain energy is demonstrated to be completely relieved at the interface without creating structural defects. However, this technique is still under development although pure IMF formation is demonstrated by structural analysis of GaSb/GaAs heterostructures [7]. It has been shown that during the formation of IMF, dangling bonds are created at the interface [8]. These dangling bonds are claimed to be overcome by the introduction of delta doping at the interface. This delta doping, which is achieved with Te atoms, reduces the dangling bonds and improve the electrical performance of devices [9, 10]. However, reliable evidence can only be provided by studying interfaces with sensitive techniques capable to determine the electrical activity due to the defect states created during IMF growth. DLTS is a powerful technique to study such electrically active defects [11].

1.2 MOTIVATION

The electrically active defects play a major role in electronic and optoelectronic devices. The interface defects or interface states created during the growth of heterojunctions also have a major contribution in the poor performance of the devices. The motivation of this work is to study the electrically active defects and interface states created by novel Interfacial Misfit (IMF) growth technique by using I-V, C-V, DLTS, C-G-F and C-F methods.

The DLTS technique is applied to study defects in GaSb/GaAs IMF epitaxially grown heterostructures, namely uncompensated and Te compensated samples. C-V and I-V techniques are employed to understand interface states created at the interfaces of GaSb/GaAs. The effect of thermal annealing on the defects in the as-grown devices is also investigated by using two different approaches, namely rapid thermal annealing and furnace annealing.

Furthermore, the defects created in p-i-n photodiode GaInAsSb devices grown on IMF GaSb/GaAs are also studied by the DLTS method.

1.3 SCHEME OF THE THESIS

The scheme of the thesis is as follows: Chapter 1 introduces the background of Interfacial Misfit (IMF) growth technique and motivation of the thesis. Chapter 2 is devoted to the description of the fundamental concepts of semiconductors, crystal structure, principles of heterostructure devices, and the properties of GaAs, GaSb and GaInAsSb. The crystal defects and theoretical background of carrier kinetics are given in Chapter 3. In Chapter 4 a brief description of experimental techniques such as DLTS, Laplace DLTS, and conductance methods is given. The hardware and software required to implement these methods are also presented. The details of samples preparation and measurements set up are described in Chapter 5. Chapter 6 presents detailed results and analysis of DLTS, I-V and C-V experiments performed on uncompensated and Te compensated IMF samples. Chapter 7 discusses the effect of rapid thermal annealing (400 ^{0}C – 600 ^{0}C) on the defects in uncompensated samples, and 400 ^{o}C rapid thermal annealed and furnace annealing in Te-compensated samples. Chapter 8 reports an investigation of the density of interface states in both uncompensated and Te compensated

samples using conductance-frequency and DLTS techniques. The electrically active defects detected in p-i-n GaInAsSb photodiodes grown on IMF GaSb/GaAs studied by DLTS are presented in Chapter 9. Finally, in Chapter 10, the overall conclusions of the work reported in this thesis are summarized, and future outlook is given.

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CHAPTER 2

FUNDAMENTAL CONCEPTS AND GROWTH OF SEMICONDUCTORS

The basic concepts of semiconductors are discussed in this chapter such as doped and undoped semiconductor, energy gap, temperature dependent energy gap, direct and indirect energy gap, density of states, lattice mismatch, band alignment, electronegativity and graded gap semiconductors. Some general properties of GaAs, GaSb and InGaAsSb are also presented. In addition, two different growth modes for growing GaSb/GaAs mismatched heterostructures are also discussed.

2.1 SEMICONDUCTORS

Semiconductors are very important in our society and are used in cordless phones, wireless networks, radio-controlled toys, television broadcasts, cell phones, satellite communications, etc. In addition, these important material systems are found in transistors that are the backbone of advanced processor chips used in laptops and computers. The use of devices made from semiconductors has become so widespread that it would be impossible to list all their different applications. Semiconductors are categorised into two classes, namely elementary semiconductors such as Si and Ge, and compounds semiconductors involving two or more elements. For example, compounds semiconductors made by two elements from the periodic table are called binary compounds (e.g. GaAs and

GaSb) and those which are made by three elements are known as ternary compounds semiconductors such as InGaAs and GaAsSb.

2.1.1 UNDOPED AND DOPED SEMICONDUCTORS

Pure semiconductors made of elementary (e.g. Si) or binary compound semiconductor (e.g. GaAs) are referred to as undoped or intrinsic semiconductors. The conductivity of such semiconductors is many orders of magnitude lower than metallic conductors. For example, thermally excited electrons in Si and GaAs are 1.5×10^{10} cm^{-3} and 1.1×10^{6} cm^{-3}, respectively, at room temperature. Due to this small number of charge carriers, the electrical resistivity of intrinsic semiconductors is high, and consequently the electrical conductivity is low. Semiconductor materials have unique property to tune their electrical conductivities by introducing some foreign atoms (called impurities) into the host material, a process referred to as doping. When semiconductors are doped with other atoms, such semiconductors are called extrinsic semiconductors. This doping could be n-type (excess electrons) or p-type (excess holes). For example, when Si is doped with one of the elements from group V in the periodic table, such as arsenic (As), the process is known as n-type doping. Si has four electrons in its outermost orbit and As has five electrons in its outer electronic shell. The four electrons in Si will pair with the four electrons in As and one electron in As atom will be free for n type conduction. Similarly, p type doping in Si can be achieved by incorporating group III atoms of the periodic table. The incorporation of trivalent impurity atoms such as boron, aluminium or gallium creates deficiencies of valence electrons in Si, called holes. Such material having deficiencies of electrons are called p-type material.

2.2 CRYSTAL STRUCTURE AND PROPERTIES

The performance of semiconductors depends upon the crystal structure. The crystalline structure of semiconductors depends upon the position of the atoms in the crystal.

2.2.1 CRYSTAL STRUCTURE

The ideal crystal structure consists of a set of atoms arranged in infinite repetitive arrangements. The unit cell is the basic building block of the crystal structure. It consists of small repeating entity. There are different types of crystal structures as shown in Figure 2.1. The simplest one is the cubic lattice in which atoms are arranged at each corner of the cube. There are two other types of cubic structures, namely, face centered and body centered. In face centered cubic (fcc) lattice, the atoms are arranged at the corners of the cube and one atom at centre of each face of the cube. While in the body centered cubic (bcc) lattice each atom is arranged at the corner and one atom at the centre of the cube.

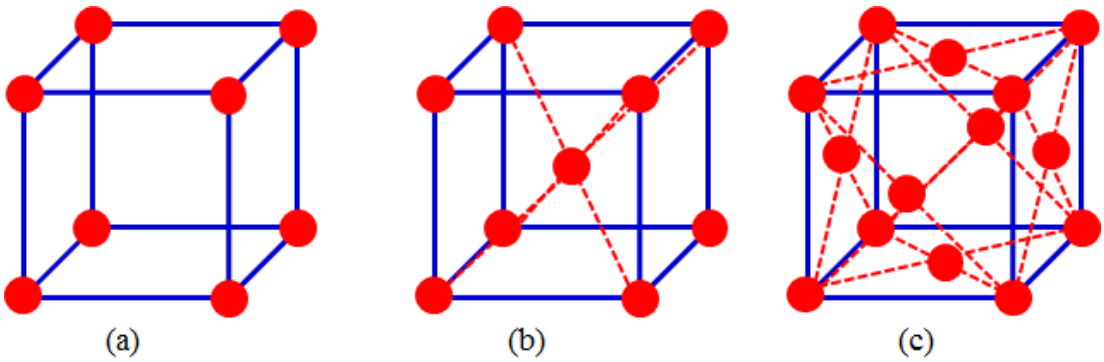

Figure 2.1: Crystal structure of (a) simple cubic (b) body centered cubic lattice and (c) face centered cubic lattice.

Most structures in semiconductors are classified into zinc blende structure and diamond structure as illustrated in Figure 2.2. In both types of structures each atom is covalently bonded to the four nearest neighbours of a regular tetrahedron. The zinc blende structure is essentially the same as the fcc structure except that the atoms at the second sub-lattice are now of different species. While in the diamond structure the same atoms are present in all lattice sites. Examples of zinc blende and diamond structures are compound (GaAs, GaSb, and InAs) and elemental (Si, Ge and C) semiconductors, respectively.

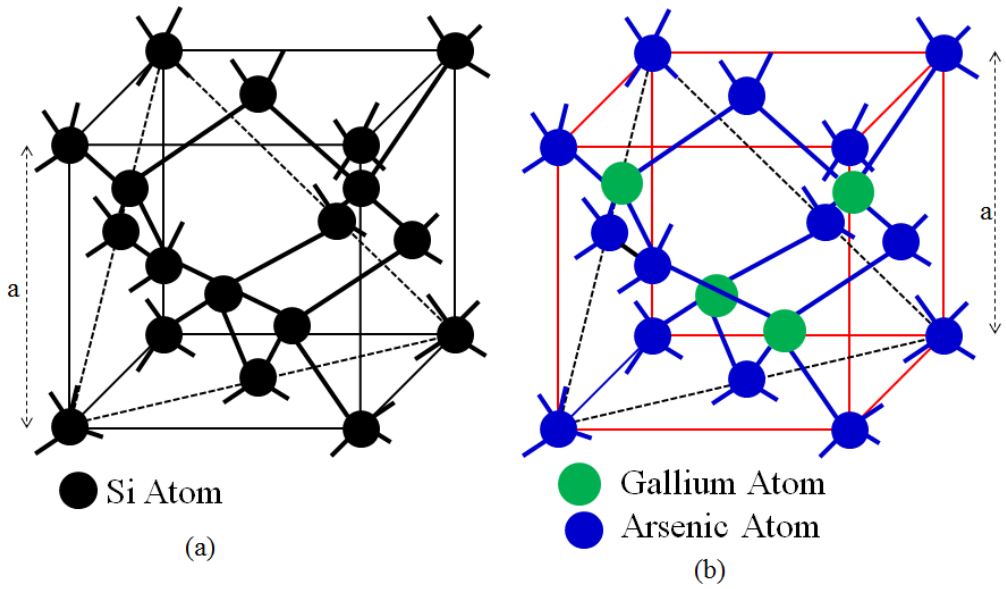

Figure 2.2: The conventional cubic unit cell of (a) diamond where both types of atomic sites are occupied by Si and (b) zinc blende structure where the sites are occupied by Ga and As atoms [1].

In semiconductor devices it is important to know a plane or set of planes in a crystal. The choice of plane on which devices are fabricated is very important since it can affect the electrical and optical properties of devices. Surface orientations may influence the device properties. This is usually done by using

Miller indices. In Miller indices first the origin is selected where all three vectors (**a**, **b**, **c**) are defined along (x, y, z) directions. Figure 2.3 shows an example of a plane with Miller indices (3, 2, 2).

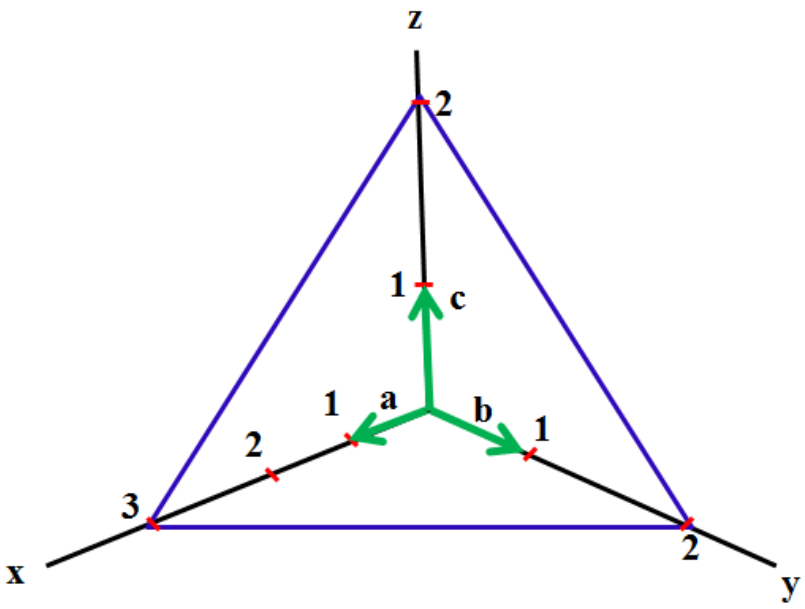

Figure 2.3: The schematic representation of plane having Miller indices of (322).

The direction of any general vector can be express in terms of set of indices h, k,l. The following symbols are used to express directions and planes of the crystals.

1) [hkl] represents a direction.
2) <hkl> represents a family of directions
3) (hkl) represents a plane
4) {hkl} represents a family of planes

In the diffraction theory the reciprocal lattice is used to get information about the crystal structure. In fact each point in the real lattice corresponds to another point in the reciprocal lattice. In this way one can represent the reciprocal lattice (G) in terms of its primitive components.

$$G = h\,A + kB + l\,C \qquad 2.1$$

where h, k and l are integers.

Three primitive basis vectors (**a, b,** and **c**) of direct lattice (R) is defined as;

$$\boldsymbol{R} = p\boldsymbol{a} + q\boldsymbol{b} + r\boldsymbol{c}$$

where p, q and r are integers. For any choice of position vector **R**, the lattice looks exactly the same. The relationship between direct lattice (**R**) and reciprocal lattice (G) is given by

$$G \cdot \mathbf{R} = 2\pi \times \text{integer} \qquad 2.2$$

The reciprocal lattice basis vectors **A, B, C** have the following relationship with the primitive vectors ***a, b*** and ***c***.

$$\mathbf{A} = 2\pi \frac{(\mathbf{b} \times \mathbf{c})}{[\mathbf{a}.(\mathbf{b} \times \mathbf{c})]}$$

$$\mathbf{B} = 2\pi \frac{(\mathbf{a} \times \mathbf{c})}{[\mathbf{a}.(\mathbf{b} \times \mathbf{c})]}$$

$$\mathbf{C} = 2\pi \frac{(\mathbf{a} \times \mathbf{b})}{[\mathbf{a}.(\mathbf{b} \times \mathbf{c})]}$$

Here $\mathbf{A}.\mathbf{a} = 2\pi$ and $\mathbf{A}.\mathbf{b} = 0$ and so on, whereas the denominators are the same because $\mathbf{a}.(\mathbf{b} \times \mathbf{c}) = \mathbf{b}.(\mathbf{c} \times \mathbf{a}) = \mathbf{c}.(\mathbf{a} \times \mathbf{b})$, and is known as the volume enclosed by the vectors (a, b, c).

2.2.2 ENERGY BANDGAP

Materials can be classified into three categories, namely insulators, metals and semiconductors. These materials can be distinguished by their energy gap. The lowest energy levels of any system, which are filled with electrons, are called valence band, and the upper available states are called conduction band. The maxima of the valence band and the minima of the conduction band are separated

by an energy gap (E_g). For insulators E_g is very high (e.g E_g > ~6 eV), for metals E_g =~0 eV and for semiconductors ~0.17 eV (InSb) < E_g < ~ 6 eV (AlN). The band gap of a semiconductor is usually represented by the energy-wave vector (E-k) relationship as shown in Figure 2.4. The maxima of valence and minima of conduction at k = 0 is approximately parabolic and their energy is given by

$$E_c = E_g + \frac{h^2 k^2}{8\pi^2 m_e}, \; E_v = -\frac{h^2 k^2}{8\pi^2 m_h} \qquad 2.3$$

where h represents Plank's constant, m_e and m_h are the mass of electron and hole, respectively.

At 0K electrons in the valence band do not have enough energy to be excited to the conduction band, and therefore a semiconductor behaves as an insulator at 0K. In this case all the electrons occupy the valence band.

2.2.3 DIRECT AND INDIRECT ENERGY BANDGAP

Semiconductors are classified into direct and indirect band gaps. In direct band gap semiconductors, the lowest available state for the electron where they can move from valence to conduction states lies at k=0 (Γ point). On the other hand in the indirect band gap semiconductors this lowest available state will be away from k=0 point. Figure 2.4 shows the E (k) relationship for GaAs and Si, the most common direct and indirect semiconductors.

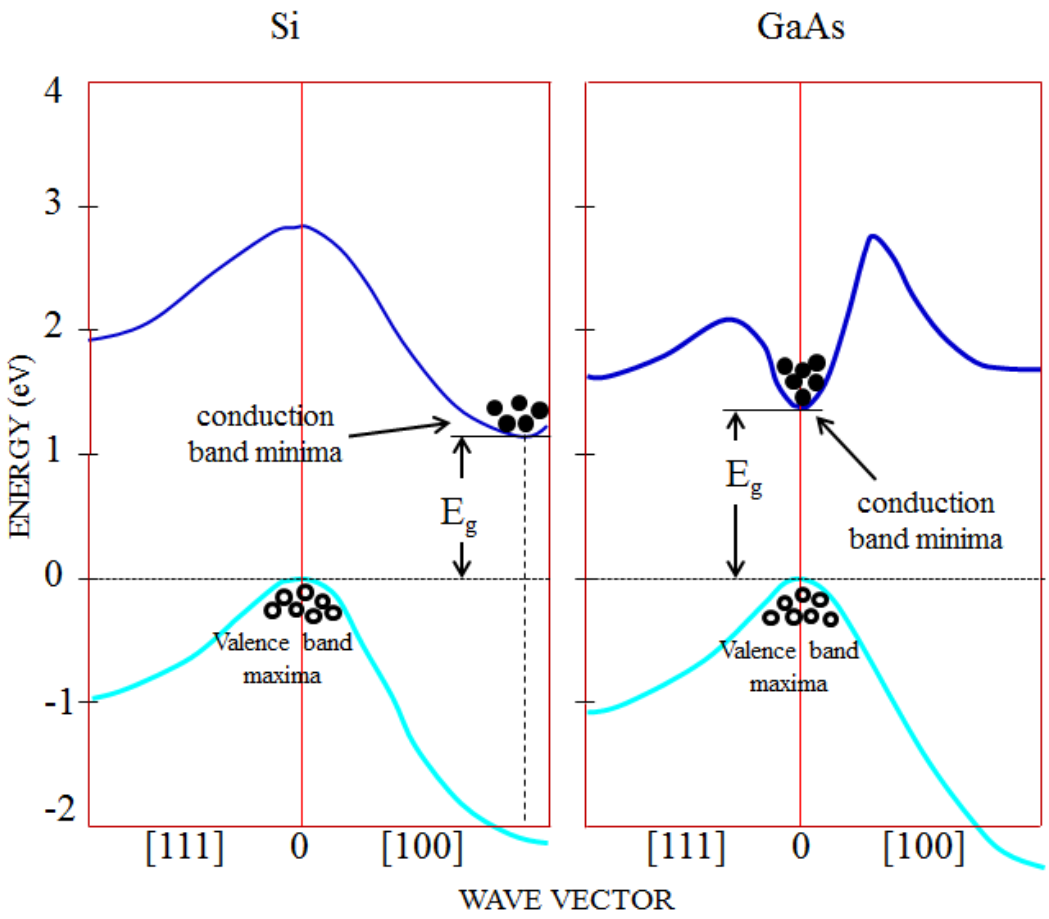

Figure 2.4: Schematic representation of Si indirect band gap semiconductor and GaAs direct band gap semiconductor.

2.2.4 TEMPERATURE DEPENDENT ENERGY BANDGAP

The energy gap of semiconductors decreases with increasing temperature. This reduction is attributed to an increase of the inter-atomic spacing which causes the potential seen by electron to decrease, and consequently the size of the energy gap is reduced.

The empirical relationship for the temperature dependence of energy band gap is given by [2]

$$E_g(T) = E_g(0) + \frac{\alpha T^2}{T+\beta} \qquad 2.4$$

Where E_g (0) is the energy gap at 0K, and α and β are the fitting parameters related to the material. For example for the case of GaAs α and β are 0.5 meV/K and 220 K, respectively [3].

2.2.5 DENSITY OF STATES

In order to determine various properties of semiconductors for example absorption, emissions and how electrons and holes distribute themselves one needs to know the number of available states. Energy bands arise from their closely spaced sublevels as electrons tend to occupy all lower energy states available to them which in turn give rise to two highest energy bands known as valence and conduction bands. In the conduction process, an excited electron from the valence band can occupy a state in the conduction band by leaving behind a local positive charge (a hole) in the valence band. The density of states of a system describes the number of states at each energy level that are available to be occupied. The confinement of charge carriers (e.g. electrons) depends upon the material structure which determines the available degree of freedoms. Semiconductor materials are categorized into four classes namely, bulk or three-dimensional (3D), two-dimensional (2D), one-dimensional (1D) and zero-dimensional (0D) material systems.

The density of states for three dimensional systems is proportional to the square root of energy. In case of two dimensional systems it follows the step like function. However, for one and zero dimensional systems the density of states is proportional to $(E)^{-1/2}$ and independent of (delta function) energy, respectively.

Figure 2.5 represents different systems to illustrate the relationship between the density of states and energy.

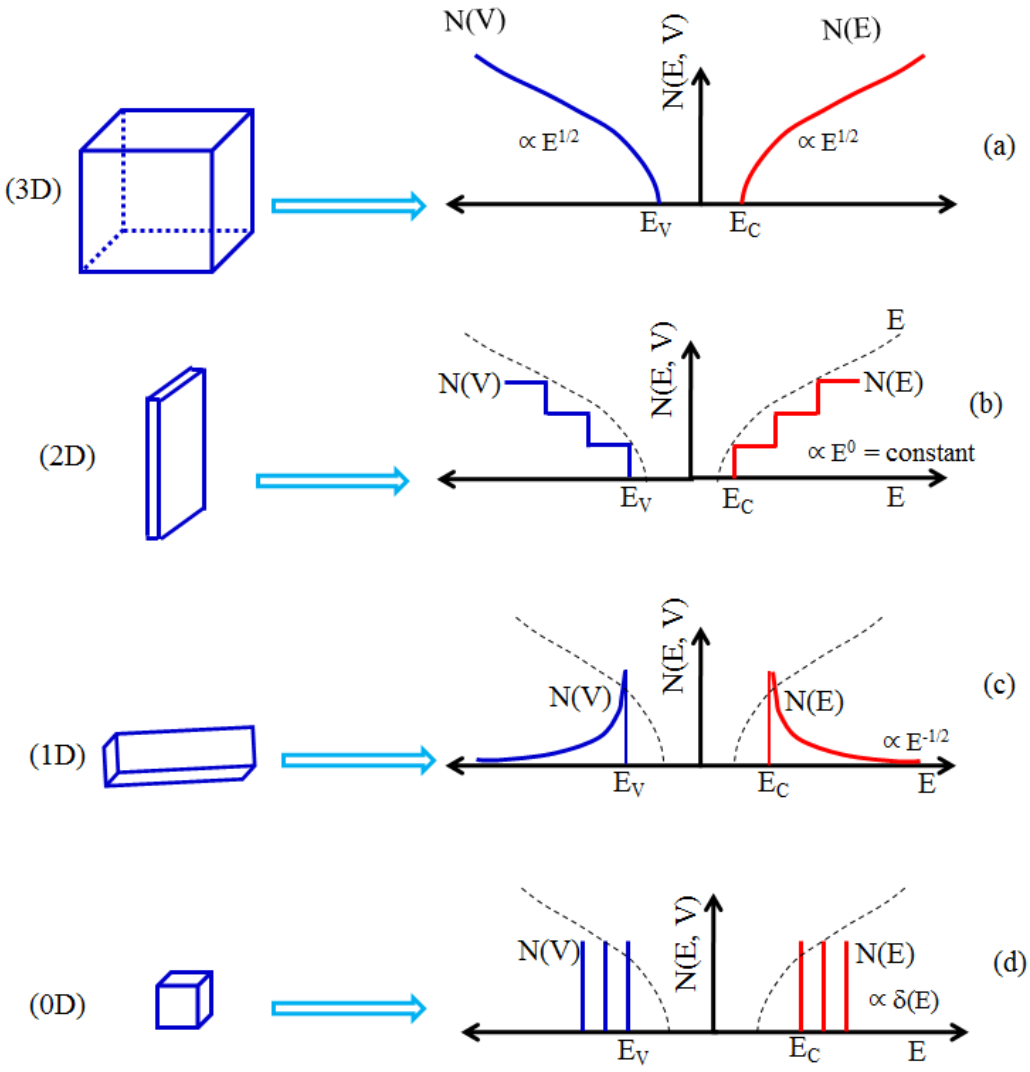

Figure 2.5: Electron and hole density of states for, 3D, 2D, 1D and 0D systems [1]

2.3 HETEROJUNCTION STRUCTURES

There are two types of structures called homojunction and heterojunction structures. Homojunction structures involve the same materials deposited on top of each other. On the other hand in heterojunction structures different materials are grown on a substrate. A heterojunction involves different materials having different properties (e.g. bandgap, electron affinity or lattice constant).

2.3.1 LATTICE MISMATCH

In a lattice matched material system, the lattice constant of the materials are exactly the same. However due to different lattice constants of the materials making a heterostructure strain at the interface occurs. The strain due to the lattice mismatch can be calculated as;

$$Lattice\ mismatch = \left(\frac{a_s - a_e}{a_s}\right) \qquad 2.5$$

a_s is lattice constant of substrate, and a_e is lattice constant of epilayer.

There are two types of strain, namely, compressive and tensile. When a semiconductor layer with larger lattice constant (called epilayer) is grown on top of a substrate (having small lattice constant), the growth will be compressive. On the other hand when smaller lattice constant material (epilayer) is grown on top of substrate (having larger lattice constant) the effective growth will be tensile. The three different types of growth, lattice match, compressive and tensile are shown in Figure 2.6.

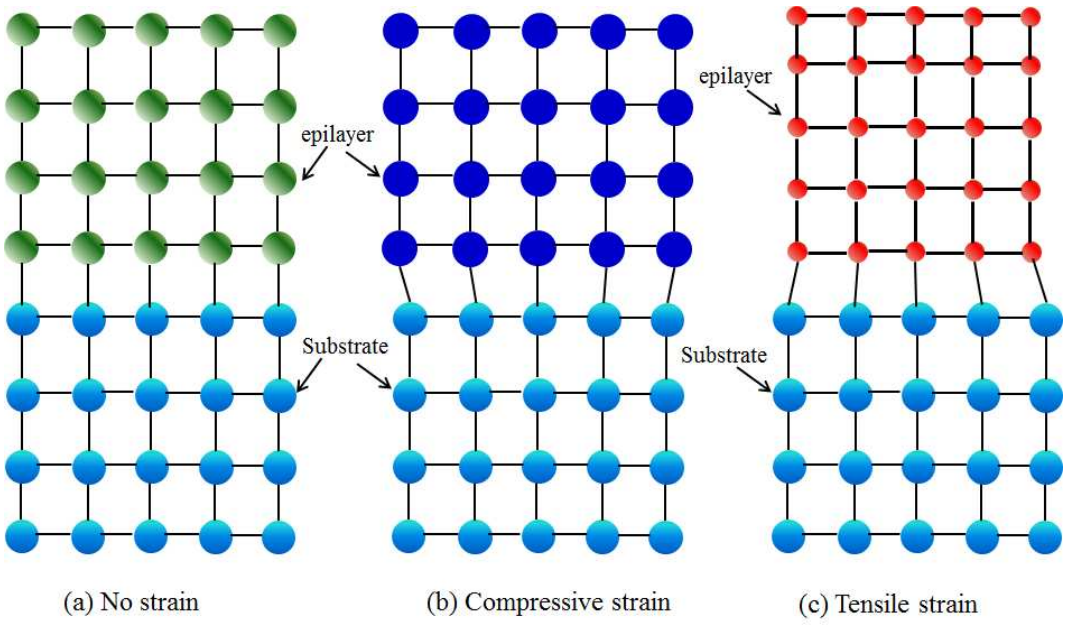

Figure 2.6: Schematic representation of lattice mismatched (a) No strain, (b) Compressive strain and (c) Tensile strain.

2.3.2 ATOM SIZE AND ELECTRONEGATIVITY

The electronegativity is the ability of an atom or molecule to attract an electron to itself in order to create a chemical bond. The electronegativity is a unitless quantity and referred to as Pauling scale after the name of Linus Pauling, who carried out the first principal study of electronegativity in 1932 [4]. If one considers two different materials X and Y to make the heterojunction, the Pauling's empirical formula for the difference in the electronegativity of these two materials can be calculated using the following equation,

$$\chi_X - \chi_Y = \left[(\mathrm{eV})^{-\frac{1}{2}}\right] \sqrt{E_D\,(XY) - \frac{[E_D(XX) + E_D(YY)]}{2}} \qquad 2.6$$

where χ_X and χ_Y is the electronegativity of X and Y, respectively, and $E_D\,(XY)$, $E_D(XX)$ and $E_D(YY)$ are the dissociation energies in eV between the atoms XY, XX and YY, respectively. The factor $\left[(\mathrm{eV})^{-\frac{1}{2}}\right]$ is used to render the value of electronegativity unitless.

2.3.3 BAND ALIGNMENT

In 1962 Anderson [5] proposed a model to construct the energy band diagram of semiconductor heterostructures. When two different semiconductor materials are brought into contact their valence and conduction bands align due to their different energy gaps and electron affinities. The three different types of band alignments, known as type-I or straddled alignment, type-II or staggered alignment and type-III or broken gap alignment, are shown in Figure 2.7. In type-I system, the conduction band of the material with smaller energy gap lies within the conduction band of the material with higher energy gap, and the valence band of the smaller energy gap material lies within the valence band of the larger

bandgap material, Typical examples of such alignment are CdSe/CdS, AlGaAs/GaAs, InGaAs/InP structures. In type II alignment, both conduction band edge and valence band edge of one material being lower than the corresponding conduction and valence band edge of the other material. In this material system electrons are confined to the one material and hole are confined in the other material. One of such example of type two alignment is GaSb/GaAs heterostructures. In heterostructures where the conduction band of one type of material lies below the valence band of the other type of material is called type III band alignment, such as GaSb/InAs structures.

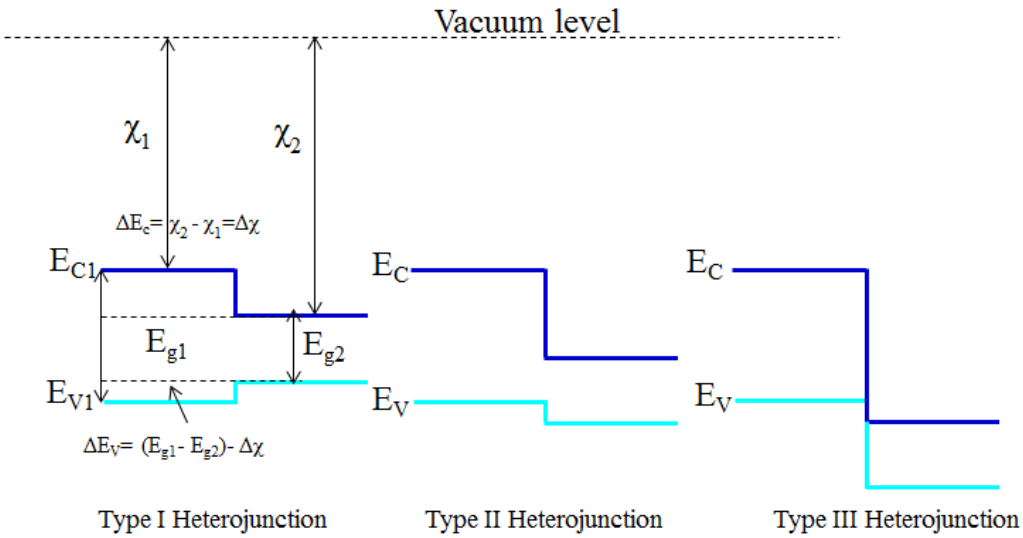

Figure 2.7: Band alignments of three types of heterostructures.

According to Anderson model [5] the difference in electron affinities of two different materials results in the offset of both conduction band (ΔE_C) and valence band (ΔE_V). These are given by

$$\chi_1 - \Delta E_C - \chi_2 = 0 \qquad 2.7$$

$$\Delta E_C = \chi_2 - \chi_1 \text{ and } \Delta E_V = \Delta E_g - \Delta\chi \qquad 2.8$$

However Anderson's model has some limitations because it does not include surface interface states, defect states and dislocations.

2.3.4 GRADED GAP SEMICONDUCTORS

The variation in the chemical compositions of the semiconductor may lead to the change in the alloy properties of graded gap semiconductors, such as change in gap energy and change in lattice constant but in most of the graded structures the lattice constant does not change appreciably.

For example, a quaternary alloy can be fabricated by three or four binary compounds: AC, AD, BC, and BD having composition $A_x B_{1-x} C_y D_{1-y}$ or AB, AC, and AD with compositions of the form $AB_x C_y D_{1-x-y}$. Thus the quaternary material parameter (Q) such as lattice constant and energy gap (Eg) can be estimated from binary parameters (B) by using following relationship

$$Q(x,y) = xyB_{AC} + x(1-y)B_{AD} + (1-x)yB_{BC} + (1-x).(1-y)B_{BD} \quad 2.9$$

Or

$$Q(x,y) = xB_{AB} + yB_{AC} + (1-x-y)B_{AD} \quad 2.10$$

where the lattice constant is known to increase linearly with the composition. The band gap of many ternary alloys can be approximated from the following quadratic equation [6]

$$E_{ABC}(x) = xE_{AC} + (1-x)E_{BC} + bx(1-x) \quad 2.11$$

Where b is referred to as bowing parameter, and for some compound semiconductors the value of the bowing coefficient is negligibly small so that the term $[b.x.(1-x)]$ in the above equation is negligible.

2.4 LATTICE-MISMATCHED GROWTH VIA TETRAGONAL DISTORTION (TD)

The strain due to lattice mismatch is pseudomorphic (irregular) due to the fact that the epilayer takes the morphology of the substrate. In this case, the epilayer growth is governed by "Tetragonal Distortion (TD)". In tetragonal distortion the strain energy between epilayer and substrate is relieved perpendicularly which results in the distortion in the epilayer. However, if growth continues the material that was once strained and distorted will come back to its original shape. By doing so, the material will be moved from a pseudomorphic phase to a metamorphic phase, where it will regain its native lattice form and lattice constant. Depending on the material properties, the crystal may take several microns to completely relax. By using this technique, the problems created by lattice mismatching between the substrate and the epilayer can be eliminated. However, metamorphic growth is restricted to optoelectronic devices because of the presence of non-radiative defects which acts as recombination centers. The lattice-mismatched growth involving metamorphic buffers will have a majority of 60° dislocations that propagate through the layers and lead to threading dislocations, and hence will cause high leakage currents in the devices that are created on top of the metamorphic buffer layers. There are other ways in which very thick buffers layer on top of substrate (often >1 μm thick) is grown in order to overcome the threading and misfit dislocations. TD approach often fails due to improper filtering of these defects from the buffer layer.

2.5 LATTICE-MISMATCHED GROWTH VIA INTERFACIAL MISFIT (IMF) DISLOCATION ARRAYS

The limitations of threading dislocations can be overcome by the use of Interfacial Misfit (IMF) growth mode. IMF growth mode is a fundamentally different growth mode that results in low defect or defect-free bulk material in which the strain energy between epilayer and substrate is relieved latterly. The limitation of metamorphic buffers can be easily overcome by using IMF growth. Once the IMF is formed, strain-free layer-by-layer growth can be achieved. The IMF arrays can be formed by using many different epilayer growth techniques such as Metal-Organic Chemical Vapour Deposition (MOCVD) [7,8] , Molecular Beam Epitaxy (MBE) [9] and Metalorganic Vapour Phase Epitaxy (MOVPE) [10].

The IMF array forms direct 90º dislocations, which are very efficient in relieving strain compared to other types of dislocations such as TD which relieves strain with 60º dislocations. Any material system with lattice mismatch ranging from 0.04% to 13% can be achieved by the IMF growth mode. All kind of lattice mismatched heterojunctions such as from group III-V and II-VI can be grown with this approach. Hence, this technique has advantages to grow defects free tuneable wavelength devices like lasers, detectors, and solar cells.

2.6 GENERAL PROPERTIES OF GALLIUM ARSENIDE (GaAs)

GaAs is one of the most important semiconductors, and is made of Gallium (Ga) of group (III) and Arsenic (As) of group (V) from the periodic table. It was

discovered in 1920 by Goldschmidt [11], however its properties remained undiscovered until 1952.

The energy band diagram shown in Figure 2.8 shows that its minima of conduction and maxima of valence band lies at K=0. Hence, when promoting an electron from the valence band to the conduction band the momentum is conserved. This makes GaAs a direct band gap semiconductor. This is very important property for the devices used in optoelectronics compared to indirect band gap (e.g Si). Furthermore, GaAs possesess high carrier mobilities compared to indirect band gap Si, which make GaAs a potential candidate for the fabrication high frequency devices.

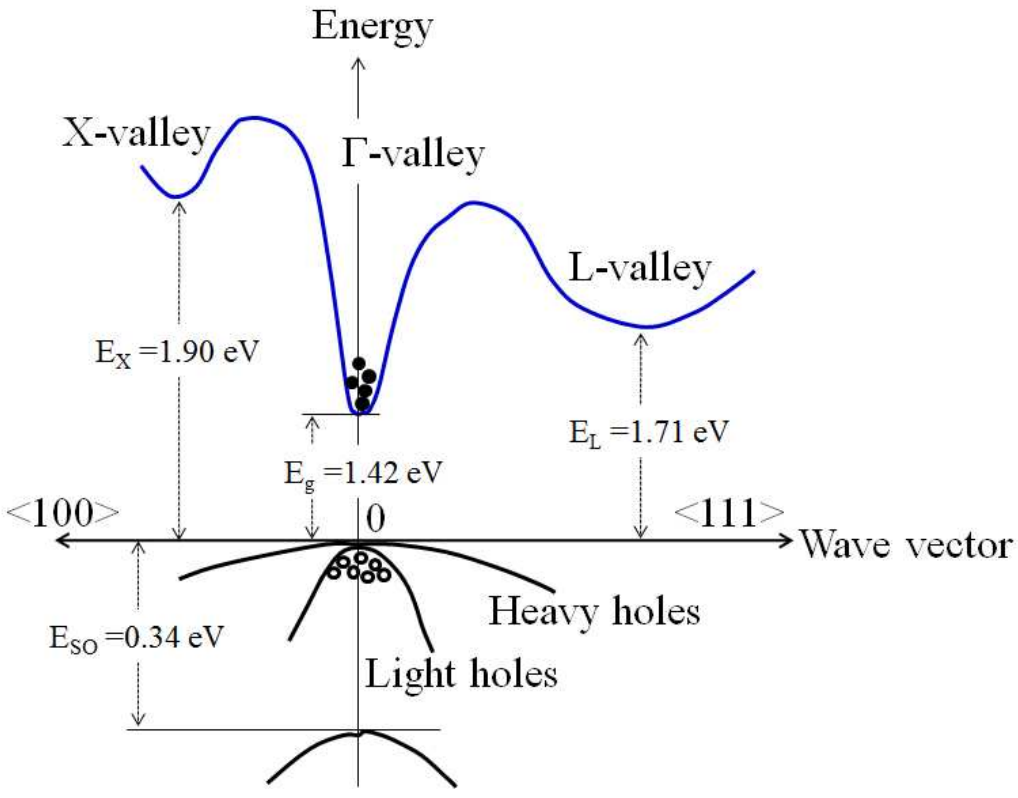

Figure 2.8: Energy band diagram of GaAs.

The resistivity of GaAs is very high ~ 10^8 Ω-cm compared to Si ~ 6.4×10^2 Ω-cm. This makes GaAs a semi-insulating substrate used in integrated circuits. In

addition, due to the fact that the energy gap of GaAs is higher than Si, the GaAs devices are more reliable to operate at higher temperatures than Si devices.

In addition to the above mentioned selected properties, some other intrinsic GaAs properties at room temperature (300K) are given in Table 2.2.

2.7 GENERAL PROPERTIES OF GALLIUM ANTIMONIDE (GaSb)

GaSb is one of the most promising candidates for devices operating in the 2-4 µm wavelength window. From the point of view devices GaSb has many applications including laser diodes with low threshold voltage, photodetectors with high quantum efficiency, superlattices with tailored optical and transport characteristics, booster cells in tandem solar cell arrangements for improved efficiency and high efficiency thermo photovoltaic (TPV) cells.

The crystal structure of GaSb is zincblende, in which face-centered cubic lattice (fcc) of Sb with Ga atoms positioned on the body diagonals. The zincblende structure of GaSb is shown in Figure 2.9.

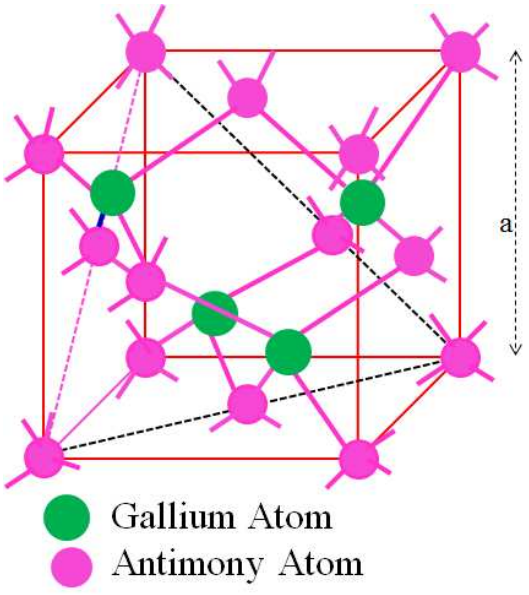

Figure 2.9: Zincblende crystal structure of GaSb.

The energy band diagram of GaSb is shown in Figure 2.10. It can be seen that the valence band maxima and conduction band minima lie at the same Γ-valley. This confirms that in order for the electrons to move from valence band to conduction band, the momentum will be conserved and therefore gap is referred to as direct.

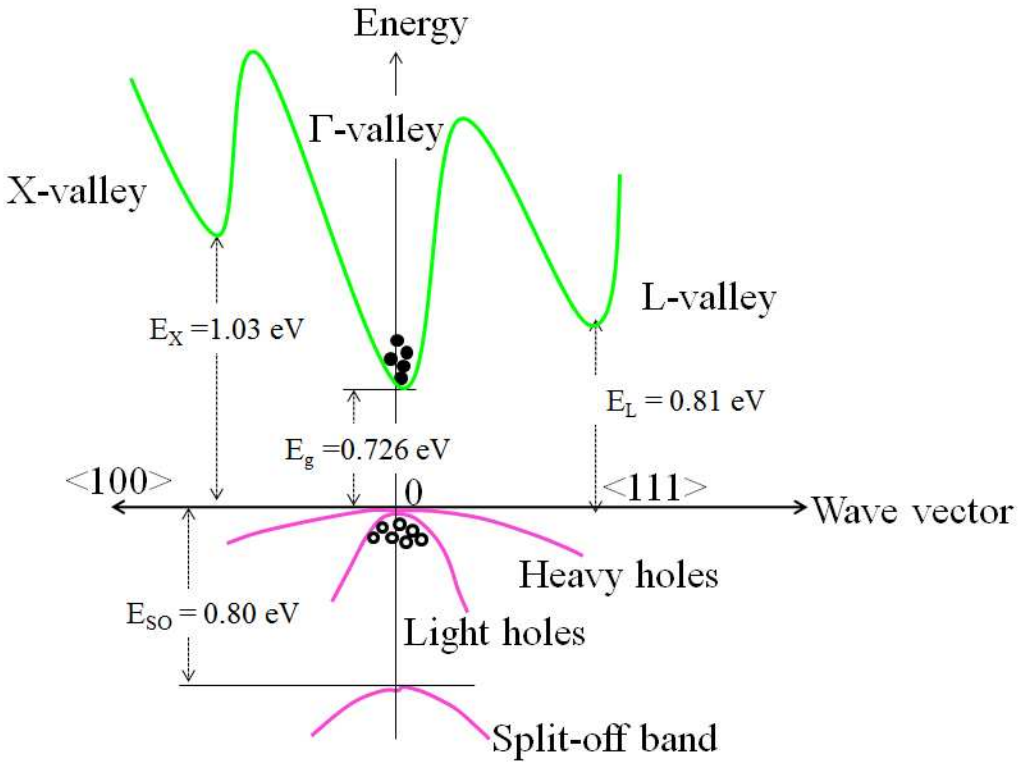

Figure 2.10: Energy band diagram of GaSb.

GaSb is particularly interesting as a substrate material whose lattice parameter matches with many ternary and quaternary III–V compounds with band gaps covering a spectral range from 0.3 to 1.58 eV [12].

For a doping of ~ 10^{17} cm^{-3} the electron mobility of GaSb is 4000-5000 $cm^2/V.s$ which is comparable to the electron mobility of GaAs. The electron mobility in thin layers of GaSb, which is as high as 2000 $cm^2/V.s$ for a doping of 10^{18} cm^3, decrease nears to the interface. Similarly the hole mobilities of GaSb are 500-600 $cm^2/V.s$ for a doping of 4 x 10^{16} cm^{-3} which are comparable to those of GaAs.

The electron and hole mobilities of GaSb are shown in Figure 2.12. These higher mobilities make GaSb an ideal candidate for the optoelectronic devices in the range of 2-4 µm wavelength window.

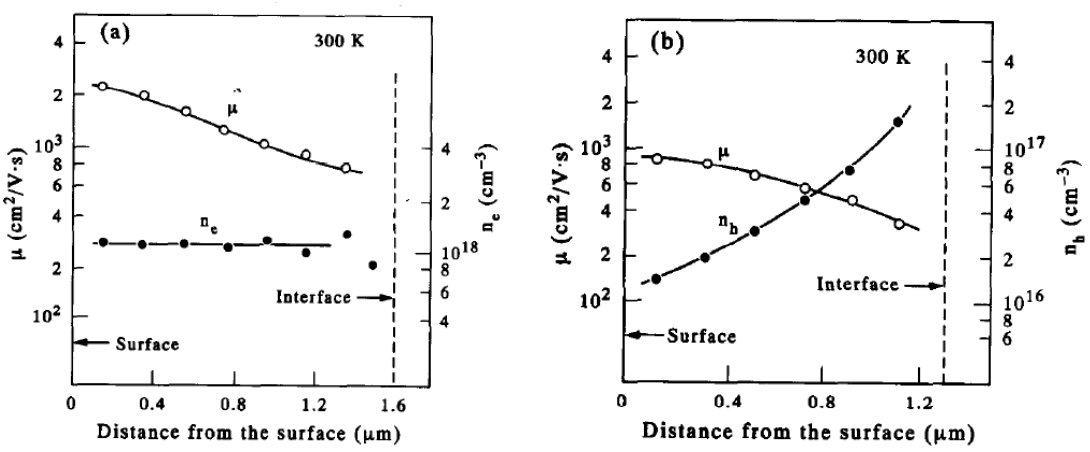

Figure 2.11: (a) The electron mobility and concentration of Te-doped 1.6 µm thick GaSb grown on GaSb substrate by MBE and (b) Hole mobility and concentration of undoped 1.2 µm GaSb at 300K [12].

Beside these selected properties, a list of other properties of GaSb is given in Table 2.2.

2.8 GENERAL PROPERTIES OF GALLIUM INDIUM ARSENIDE ANTIMONIDE (GaInAsSb)

There is a great interest in materials which have potential applications in optical fiber telecommunications. The spectral region 2-4 µm gets much attention due to the development of low-loss fluoride glass fibers in this wavelength spectrum. The quaternary compound GaInAsSb provides the basic building block of the devices that operates in this spectral region [13]

The lattice matched quaternary GaInAsSb can be grown on GaSb and InAs. The band gap energies of $Ga_{1-x}In_xAs_ySb_{1-y}$ vary from 0.30 eV to 0.71 eV (4.1 to 1.7 for 0 ≤x≤ 1 and $y = \frac{0.3835 - 0.3835x}{0.4210 + 0.216x}$, respectively [13]. The fundamental energy gap of GaInAsSb in the whole range of composition (x) has a direct nature. Figure 2.12 shows the energy gap variation of GaInAsSb as function of composition (x) calculated by different sources.

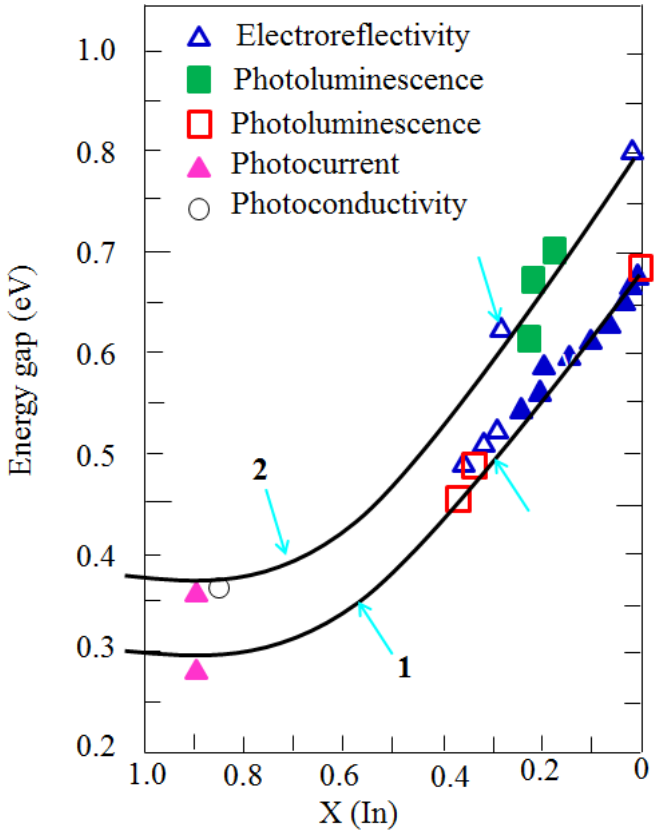

Figure 2.12: Energy gap E_g of $Ga_{1-x}In_xAs_ySb_{1-y}$ vs. x (y = 0.9x) lattice-matched to GaSb. Experimental points are taken from different sources. Arrows show region of miscibility gap. Data points are taken by different techniques as shown in the inset. Curves 1 and 2 are taken at 77K and 300K, respectively [14].

It is clear from Figure 2.13 that at low composition of x, the conduction band minima at Γ point is much lower than X and L points.

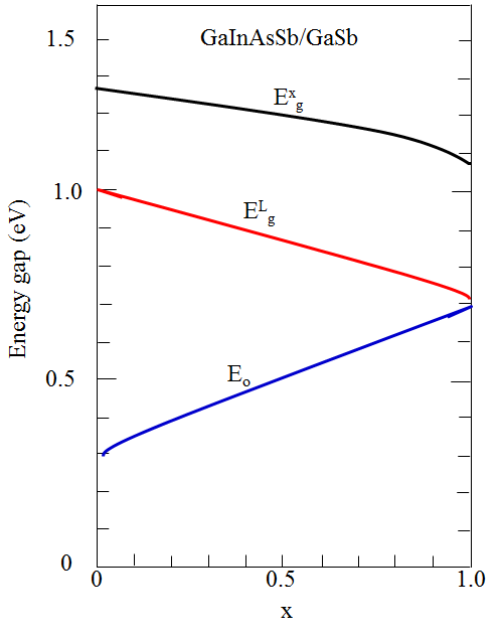

Figure 2.13: Energy band gap of $In_{1-x}Ga_xAs_ySb_{1-y}$ as function of composition x, where E_o, E^L_g and E^x_g are energy gaps at Γ, X and L valleys, respectively [13].

Table 2.1 composition dependent of energy gap and lattice constant of $Ga_xIn_{1-x}As_ySb_{1-y}$[15].

x, y	a (Å)	E_b (eV)	x, y	a (Å)	E_b (eV)	x, y	a (Å)	E_b (eV)
0.0, 0.0	6.478	0.178	0.3, 0.8	6.021	0.341	0.7, 0.5	5.992	0.483
0.0, 0.1	6.436	0.143	0.3, 0.9	5.979	0.433	0.7, 0.6	5.949	0.556
0.0, 0.2	6.394	0.119	0.3, 1.0	5.936	0.545	0.7, 0.7	5.905	0.650
0.0, 0.3	6.352	0.107	0.4, 0.0	6.325	0.297	0.7, 0.8	5.862	0.744
0.0, 0.4	6.310	0.107	0.4, 0.1	6.282	0.253	0.7, 0.9	5.818	0.854
0.0, 0.5	6.268	0.118	0.4, 0.2	6.239	0.228	0.7, 1.0	5.775	0.973
0.0, 0.6	6.226	0.141	0.4, 0.3	6.196	0.222	0.8, 0.0	6.171	0.552
0.0, 0.7	6.184	0.175	0.4, 0.4	6.153	0.234	0.8, 0.1	6.128	0.507
0.0, 0.8	6.142	0.221	0.4, 0.5	6.110	0.251	0.8, 0.2	6.084	0.484
0.0, 0.9	6.100	0.279	0.4, 0.6	6.068	0.283	0.8, 0.3	6.040	0.491
0.0, 1.0	6.051	0.350	0.4, 0.7	6.025	0.345	0.8, 0.4	5.997	0.521
0.1, 0.0	6.440	0.193	0.4, 0.8	5.982	0.424	0.8, 0.5	5.953	0.576
0.1, 0.1	6.397	0.152	0.4, 0.9	5.939	0.520	0.8, 0.6	5.909	0.653
0.1, 0.2	6.355	0.128	0.4, 1.0	5.896	0.634	0.8, 0.7	5.865	0.752
0.1, 0.3	6.313	0.116	0.5, 0.0	6.286	0.348	0.8, 0.8	5.822	0.871
0.1, 0.4	6.271	0.116	0.5, 0.1	6.243	0.304	0.8, 0.9	5.778	0.988
0.1, 0.5	6.229	0.127	0.5, 0.2	6.200	0.279	0.8, 1.0	5.734	1.111
0.1, 0.6	6.186	0.151	0.5, 0.3	6.157	0.274	0.9, 0.0	6.133	0.636
0.1, 0.7	6.144	0.187	0.5, 0.4	6.114	0.287	0.9, 0.1	6.089	0.592
0.1, 0.8	6.102	0.236	0.5, 0.5	6.071	0.319	0.9, 0.2	6.045	0.576
0.1, 0.9	6.060	0.301	0.5, 0.6	6.028	0.369	0.9, 0.3	6.001	0.585
0.1, 1.0	6.017	0.404	0.5, 0.7	5.985	0.436	0.9, 0.4	5.957	0.618
0.2, 0.0	6.401	0.219	0.5, 0.8	5.942	0.519	0.9, 0.5	5.914	0.675
0.2, 0.1	6.359	0.176	0.5, 0.9	5.899	0.619	0.9, 0.6	5.870	0.755
0.2, 0.2	6.316	0.152	0.5, 1.0	5.856	0.735	0.9, 0.7	5.826	0.859
0.2, 0.3	6.274	0.141	0.6, 0.0	6.248	0.408	0.9, 0.8	5.782	0.985
0.2, 0.4	6.232	0.141	0.6, 0.1	6.205	0.363	0.9, 0.9	5.738	1.129
0.2, 0.5	6.189	0.154	0.6, 0.2	6.161	0.339	0.9, 1.0	5.694	1.260
0.2, 0.6	6.147	0.180	0.6, 0.3	6.118	0.334	1.0, 0.0	6.095	0.728
0.2, 0.7	6.104	0.219	0.6, 0.4	6.075	0.349	1.0, 0.1	6.051	0.688
0.2, 0.8	6.062	0.273	0.6, 0.5	6.032	0.397	1.0, 0.2	6.006	0.674
0.2, 0.9	6.019	0.359	0.6, 0.6	5.988	0.466	1.0, 0.3	5.962	0.684
0.2, 1.0	5.977	0.469	0.6, 0.7	5.945	0.538	1.0, 0.4	5.918	0.718
0.3, 0.0	6.363	0.254	0.6, 0.8	5.902	0.626	1.0, 0.5	5.874	0.776
0.3, 0.1	6.320	0.210	0.6, 0.9	5.859	0.731	1.0, 0.6	5.830	0.858
0.3, 0.2	6.278	0.186	0.6, 1.0	5.815	0.848	1.0, 0.7	5.786	0.964
0.3, 0.3	6.235	0.179	0.7, 0.0	6.210	0.476	1.0, 0.8	5.742	1.094
0.3, 0.4	6.192	0.181	0.7, 0.1	6.166	0.431	1.0, 0.9	5.698	1.248
0.3, 0.5	6.150	0.196	0.7, 0.2	6.123	0.407	1.0, 1.0	5.654	1.424
0.3, 0.6	6.107	0.225	0.7, 0.3	6.079	0.404			
0.3, 0.7	6.064	0.268	0.7, 0.4	6.036	0.432			

GaInAsSb alloys have the highest electron mobilities due to their smaller electron effective mass. The reported value of room-temperature electron mobility is up to 30,000 $cm^2/(V \cdot s)$ for a carrier density of 5.7×10^{15} cm^{-3} [16]. This makes GaInAsSb an ideal candidate for high speed electronic devices such as field effect transistor (FET) and high electron mobility transistor (HEMT).

Table 2.2: Some important properties of intrinsic GaAs, GaSb and GaInAsSb at 300K; hh and lh stand for heavy hole and light hole, respectively [17, 18]

Parameter	GaAs	GaSb	$Ga_xIn_{1-x}As_ySb_{1-y}$
Crystal Structure	Zincblende	Zincblende	Zincblende
Lattice constant (Å)	5.6533	6.09	y=(0.3835-0.3835x)/(0.4210+0.216x)
Crystal density (g/cm^3)	5.360	5.61	5.360-1.6x
Energy band gap (eV)	1.42	0.725	0.725x +0.290(1-x) -0.6x(1-x)
Band type	Direct	Direct	Direct
Electron effective mass	$0.063\ m_0$	$0.0412\ m_0$	$0.022+0.03x -0.012x^2\ m_o$
Hole effective mass	$0.62m_0$ (h_h) $0.087m_0$(l_h)	$0.28m_0$ (hh) $0.05m_0$ (lh)	$0.41 +0.16x +0.023x^2\ m_o$
Dielectric constant (static)	12.85	15.69	15.3+0.4x
Specific heat(cal/gK)	0.08	0.019	0.0597
Electron affinity (eV)	4.07	4.06	(4.87 -0.81x)

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CHAPTER 3

DEFECTS IN SEMICONDUCTORS AND THEIR PROPERTIES

This chapter is based on defects due to imperfection in crystalline semiconductor materials. Different types of defects are discussed in this chapter such as point defects and defect complexes. The effect of these defects as generation recombination centres and the theory of deep level defects are also presented. Defects in GaAs, GaSb and InGaAsSb semiconductor materials are covered in detail in this chapter.

3.1 CLASSIFICATION OF DEFECTS

A perfect crystal is formed by the repetition of infinite number of unit cells along the crystal orientation. There are many types of defects ranging from point, complexes, and extended defects. In the sections below the different kind of defects will be discussed.

3.1.1 POINT DEFECTS

A point defect is formed when an atom is missing or when some foreign atom substitutes an atom from the host crystal. This is also called a zero dimensional defect. These defects which are introduced during growth can alter the electrical and optical performance of the devices. The different types of point defects are presented in the following section [1].

1 VACANCY AND SUBSTITIONAL DEFECTS

A vacancy, called Schottky defect, is created when an atom is missing from the lattice site in a crystal plane as illustrated in Figure 3.1 (a).

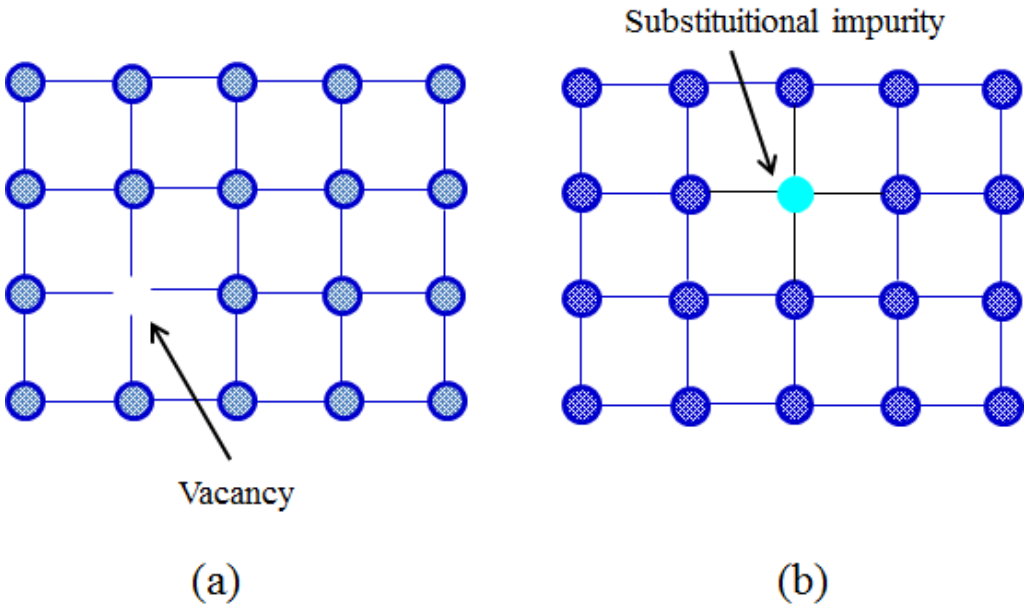

Figure 3.1: Vacancy and interstitial defects.

When a foreign atom, such as an impurity, occupies the site of a host atom from its regular position, the defect is referred to as substitional impurity as shown in Figure 3.1(b).

2 INTERSTITIAL AND ANTISITE DEFECTS

Figure 3.2(a) shows an interstitial impurity. There are two types of interstitial impurities called self-interstitial and foreign interstitial. In self-interstitial an atom from the host material occupy a site other than its regular site in the crystal. On the other hand if a foreign atom occupies an irregular site of the crystal it is called foreign interstitial as shown in Figure 3.2 (a).

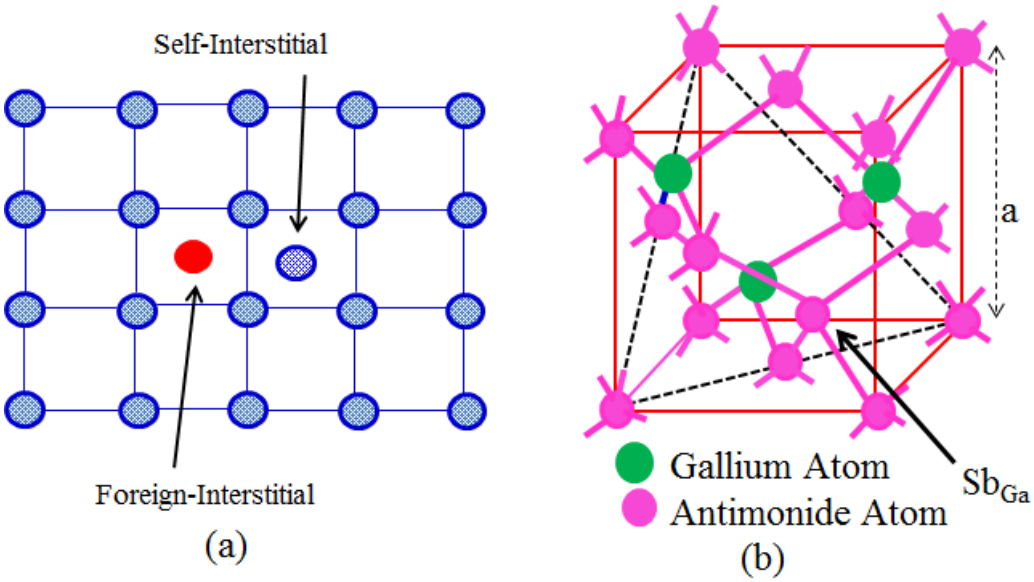

Figure 3.2: (a) Interstitial defects; (b) Antisite defect

When a host atom occupies the site of another host atom in a material, the impurity formed is called antisite. For example in GaSb material when Sb atom occupies the Ga site the resulting defect, $Sb_{Ga,}$ is called antisite (Figure 3.2(b)).

3.1.2 COMPLEXES OF POINT DEFECTS

When two or more point defects form pairs the resultant defects will be complexes. In the following selected complexes are discussed.

1 SPLIT-INTERSTITIAL AND FRENKEL DEFECTS

A split interstitial is formed when two interstitials makes a pair as shown in Figure 3.3(a). It is formed by either a pair of two interstitial atoms of same host material or by a pair of two foreign interstitials.

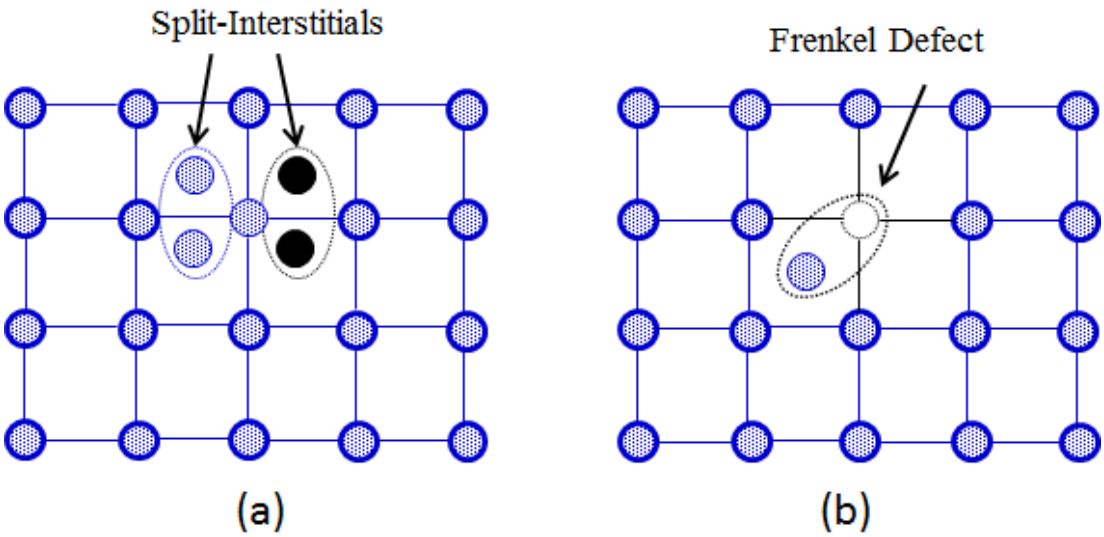

Figure 3.3: Examples of defect complexes (a) split-interstitials and (b) Frenkel defect.

When a vacancy and interstitial atom form a pair, a complex defect formed which is called Frenkel defect as shown in Figure 3.3(b).

2 VACANCY COMPLEXES AND IMPURITY RELATED COMPLEXES

There are different forms of vacancies complexes in a crystalline material as illustrated in Figure 3.4 (a). When two vacancies interact with each other and form a pair the resultant complex is called Di-vacancy. A split vacancy occurs when two vacancies and interstitial atom forms a pair. A pair of a vacancy and a foreign interstitial atom is called vacancy-impurity complex.

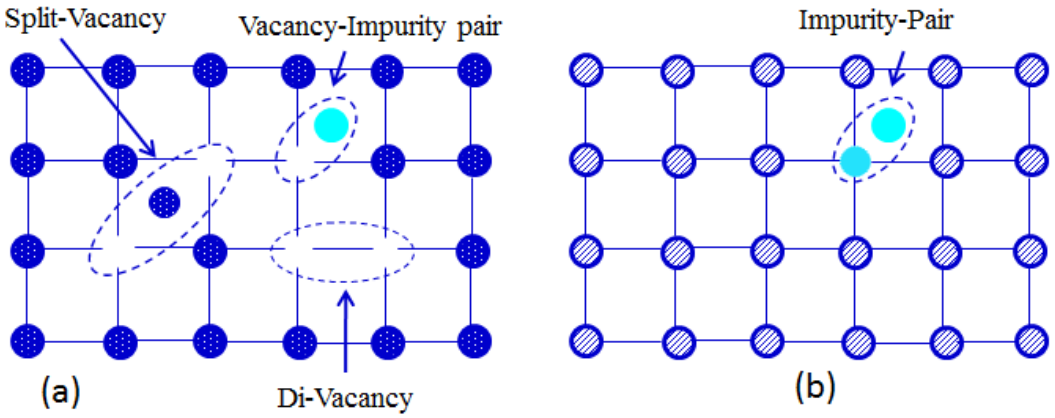

Figure 3.4: Complex defects (a) Di-vacancy, split-vacancy and vacancy-impurity pairs and (b) complexes of impurity-pair.

Figure 3.4(b) shows an impurity-pair which is created when a substitutional impurity atom form a pair with another impurity atom located at an interstitial site.

3.1.3 LINEAR OR 1-D DEFECTS

The linear or 1-D defects are different than point or 0-D defects. These types of defects are formed when a line of atoms are displaced from regular position of the crystal. These defects are called dislocations and are known as most common structural defects in semiconductors. This line defect is further divided into two classes, namely, edge dislocations and screw dislocations.

Edge dislocation shown in Figure 3.5 (a) is formed when an extra half plane of atoms is introduced in regular crystal and disturbs nearby atoms. If one part of the crystal is displaced with respect to another part this defect is referred to as screw dislocation (Figure 3.6 (b)).

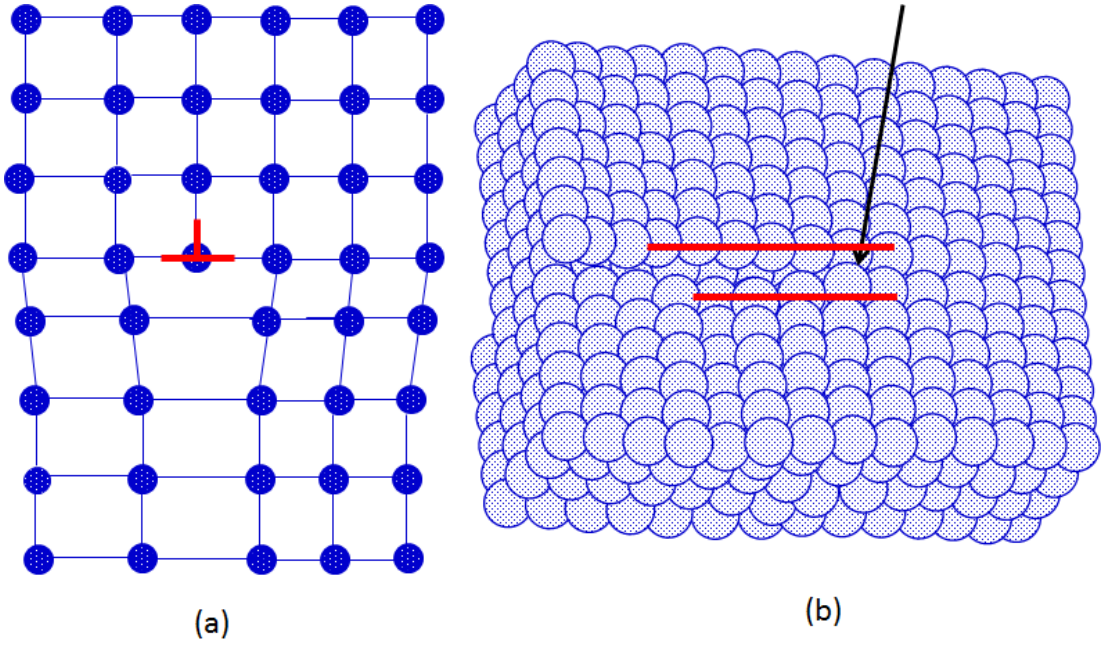

Figure 3.6: Line or 1- D defects: (a) edge dislocation and (b) screw dislocation

3.2 DEFECTS AND THEIR CARRIER KINETICS

3.2.1 SHALLOW LEVELS AND DEEP LEVELS DEFECTS

Current electronic and optoelectronics industries widely use semiconductors as basic elements for many modern devices. But one of the major hurdles that semiconductor industry is facing is the quality of the crystal, because it is impossible to grow perfect crystals which are free of defects. For example, the materials may contain chemical impurities or lattice defects. Such defects are grouped into point defects (e.g. vacancies, interstitials, and substitutions) and extended defects such as edge dislocation and screw dislocation. The presence of such defects cause poor performance of the devices made from such materials. It is therefore very important to study the defects created during growth and find procedures to reduce them in order to achieve devices with very high performance. When defects are created in a semiconductor, they have energies within the bandgap of the material. The defects which are much closer to the

valence band or conduction band are called shallow level impurities. If an impurity donates an electron to the conduction band it is called shallow donor level and if it donates a hole it is called shallow acceptor level as shown in Figure 3.7.

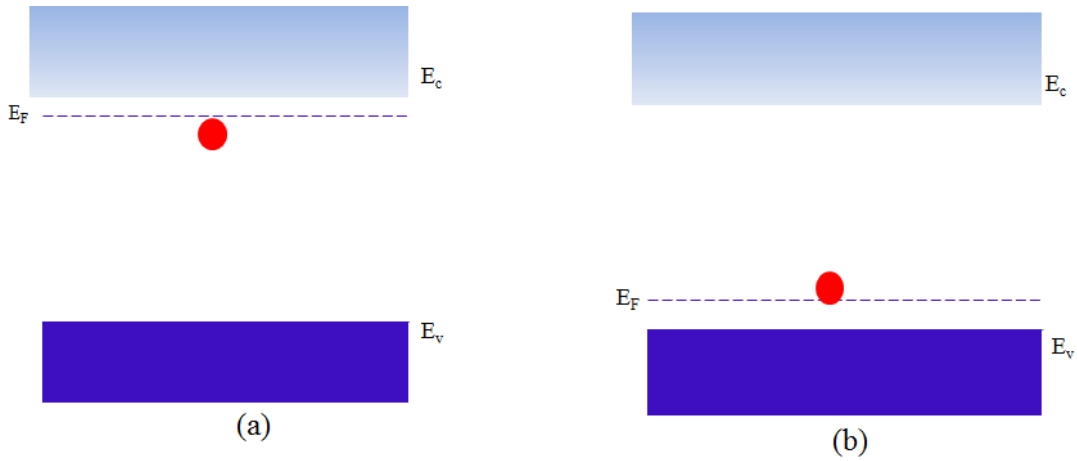

Figure 3.7: Schematic diagram of (a) shallow donor level (b) shallow acceptor level.

The energy of the shallow levels varies between approximately 5 – 10 meV below the conduction or valence bands. Impurities with energies > ~ 100meV are called deep level impurities as shown in Figure 3.8. It is important to understand the conduction mechanism involving these impurities levels. This will be explained in the next section.

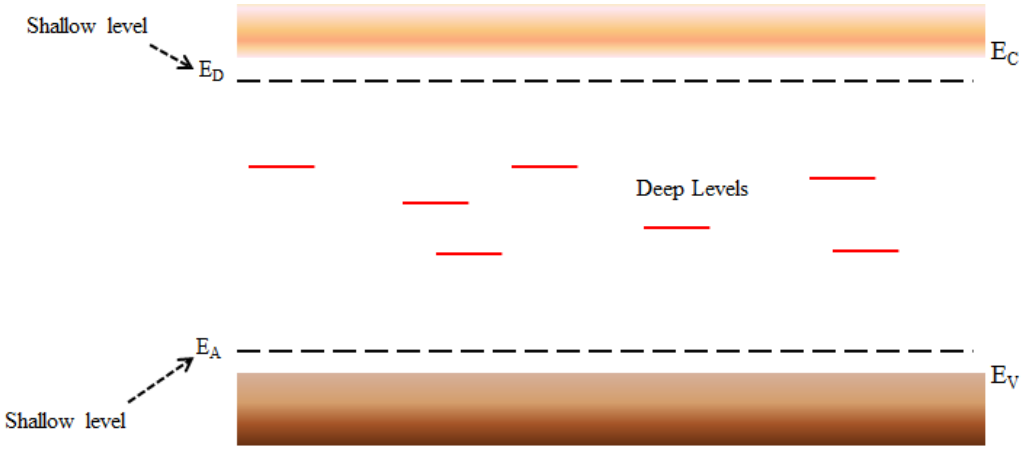

Figure 3.8: Schematic diagram of deep level impurities in semiconductors. E_D and E_A are shallow donor and shallow acceptor levels, respectively.

3.2.2 SHOCKLEY-READ-HALL THEORY

Deep defect states in semiconductors are also known as trap centers (electron traps or hole traps), recombination-generation centers (G-R), and deep levels. The emission and capture rates of charge carriers determine the occupancy of a center at equilibrium. Let us consider the energy of an impurity is E_T. To study the various capture and emission processes, first one should consider the capture of an electron from the conduction band as shown in Figure 3.9 (I). When an electron is captured, one of two processes take place, either this electron is emitted back to the conduction band (Figure 3.9 (II) this is called emission 'e_n') or it will capture a hole from the valence band (Figure 3.9 (III)). After a hole is captured in a deep centre, there will be again two cases, either the centre emits a hole back to the valence band (Figure 3.9 (IV)) or it can capture an electron from the conduction band (Figure 3.9 (I)) [2,3].

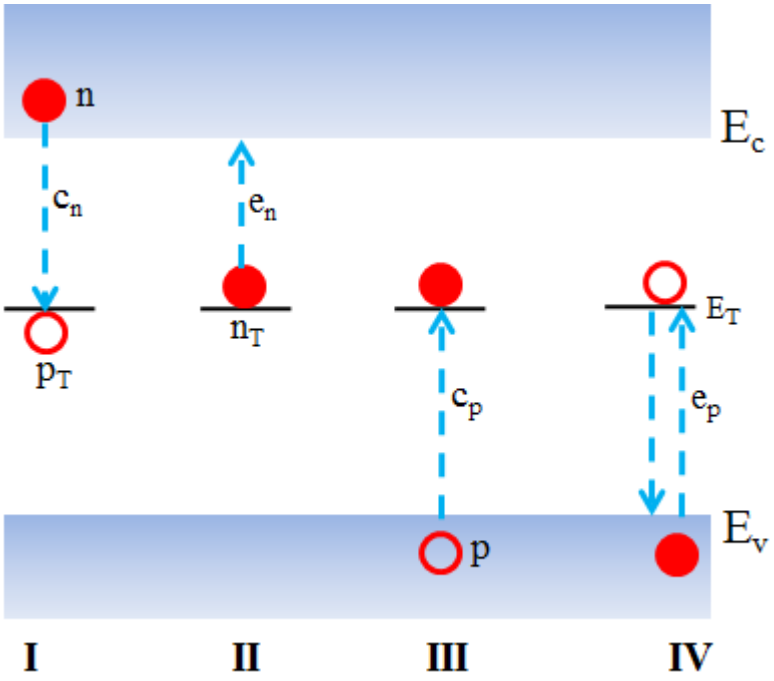

Figure 3.9: Schematic diagram of capture and emission processes: (I) capture of electron, (II) emission of electron, (III) capture of hole, (IV) emission of hole [2].

From the above 3.9, p_T represents centre occupied by hole, n_T represents centre occupied by electron, e_n is emission of an electron from the centre, e_p is emission of a hole. C_n and C_p are the capture rate of electrons and holes, respectively. Generally, the electron emission rate in the upper half of the bandgap is higher than the hole emission rate. Similarly, the hole emission rate in the lower half of the bandgap is higher than the electron emission rate. Usually, one of the two emission rates dominates, and the other can be neglected. There are two possibilities to occupy a G-R center. When a centre is occupied by an electron it is in state *'*n_T*'*, and when a centre is occupied by a hole it is in state p_T as shown in Figure 3.9. For a donor like G-R centre, the state *'*n_T*'* is neutral, and when it emits an electron it will act *as '*p_T*'*. Similarly for acceptor like G-R centre, the state *'*p_T*'*

is neutral and when it captures an electron, it will be in state n_T. The total density of G-R centers *'N_T'* must be equal to the density of electron and hole states. A centre can either be occupied by an electron or a hole. When an electron or hole is generated by a centre or recombine in a centre, the density of electron in conduction band *'n'*, the density of hole *'p'* in valence band and charge states of the centers 'n_T' and 'p_T' are all time dependent.

When a center captures an electron from the conduction band (I) the density of electrons in the conduction band is reduced and the electron density increases in conduction band as emission increases (II). The rate of change of electrons in G-R center is given by

$$\frac{dn}{dt}|_{G-R} = (II) - (I) = e_n n_T - c_n n p_T \qquad 3.1$$

Here, only the G-R mechanism is considered. The radiative or Auger recombinations are not taken into accountd. From equation 3.1, the relation II ($e_n n_T$) does not depend on electrons being in the conduction band. However, to capture an electron I ($c_n n p_T$) (see equation 3.1), there must be electrons in the conduction band. A similar relation for the hole applies;

$$\frac{dp}{dt}|_{G-R} = (IV) - (III) = e_p p_T - c_p p n_T \qquad 3.2$$

where c_n and c_p are the capture rates of electrons and holes, respectively. The capture rate c_n is defined as

$$c_n = \sigma_n v_{th} \qquad 3.3$$

where v_{th} is the electron thermal velocity and σ_n is the capture cross section of G-R center. Whenever an electron or hole is emitted or captured, the occupancy of the G-R state changes. This rate of change is calculated from equation 3.1 and 3.2, and is given by [3]

$$\frac{dn_T}{dt}\Big|_{G-R} = \frac{dp}{dt} - \frac{dn}{dt} = \left(c_n n + e_p\right)(N_T - n_T) - \left(c_p p + e_n\right)n_T \qquad 3.4$$

For the steady state condition

$$\frac{dn_T}{dt} = 0$$

$$\text{therefore} \quad \left(c_n n + e_p\right)(N_T - n_T) - \left(c_p p + e_n\right)n_T = 0 \qquad 3.5$$

$$\left(c_n n + e_p\right)(N_T - n_T) = \left(c_p p + e_n\right)n_T \qquad 3.6$$

In semiconductors, at thermal equilibrium the rate of creation and rate of absorption are the same.This is known as detailed balance principle.

According to the detailed balance principle;

$$e_n n_T = c_n p_T n \qquad 3.7$$

$$c_n = \sigma_n v_{th} \qquad 3.8$$

$$\text{therefore,} \qquad e_n n_T = \sigma_n v_{th} p_T n \qquad 3.9$$

$$e_p p_T = c_p n_T p \qquad 3.10$$

$$where \qquad c_p = \sigma_p v_{th}$$

$$e_p p_T = \sigma_p v_{th} n_T p \qquad 3.11$$

As the total density of states available is equal to the density of states occupied by electrons and holes, then

$$N_T = n_T + p_T \qquad 3.12$$

if *'f'* is the Fermi Dirac distribution function which represents the number of states occupied by electrons, then *'(1-f)'* will be the number of states occupied by holes.

That is;

$$n_T = N_T f \qquad 3.13$$

$$p_T = N_T(1 - f) \qquad 3.14$$

Equation 3.12 becomes;

$$N_T = N_T f + N_T(1-f) \qquad 3.15$$

$$f = \left[\frac{1}{1+\exp\left(\frac{E_T - E_f}{kT}\right)}\right]$$

Here E_T = energy of deep level, E_f= energy of Fermi level, k = Boltzmann constant and T = temperature.

Equation 3.14 can be expressed as;

$$e_n N_T f = \sigma_n v_{th}(1-f) N_T n \qquad 3.16$$

Where n is the electron density and is given by;

$$n = n_i \exp\left(\frac{E_f - E_i}{kT}\right) \qquad 3.17$$

n_i is the density of states of intrinsic material;

$$n_i = N_c exp\left(\frac{E_i - E_c}{kT}\right) \qquad 3.18$$

Therefore

$$n = N_c exp\left(-\frac{E_c - E_f}{kT}\right) \qquad 3.19$$

By putting the value of equation 3.19 in equation 3.16 one can get information about the emission processes as described by the following equations.

$$e_n = \sigma_n < v_n >_{th} N_c exp\left(-\frac{E_c - E_T}{kT}\right) \qquad 3.20$$

$$e_p = \sigma_p < v_p >_{th} N_v exp\left(-\frac{E_T - E_v}{kT}\right) \qquad 3.21$$

where N_c and N_v are the density of states in conduction band and valence band, respectively. The values of N_c, N_v, $< v_n >_{th}$ and $< v_p >_{th}$ are given by;

$$N_c = 2\left(\frac{2\pi m_e^* kT}{h^2}\right)^{3/2}$$

$$N_v = 2\left(\frac{2\pi m_h^* kT}{h^2}\right)^{3/2}$$

$$< v_n >_{th} = \frac{(3kT)^{1/2}}{m_e^*}$$

$$< v_p >_{th} = \frac{(3kT)^{1/2}}{m_h^*}$$

where m_e^* and m_h^* are the effective mass of electrons and holes, respectively.

If these values are substitued in corresponding equations (3.20) and (3.21), and all constant values are represented by A then one gets

$$e_n = AT^2\sigma_n \exp\left(-\frac{E_c - E_T}{kT}\right) \qquad 3.22$$

$$\text{Where } A = 2\frac{\sqrt{3k}}{m_e}(2\pi m_e)^{3/2}$$

$$e_p = AT^2\sigma_p exp\left(-\frac{E_T - E_v}{kT}\right) \qquad 3.23$$

The Arrhenius plot of $\left(\frac{e_{n,p}}{T^2}\right)$ versus $\left(\frac{1000}{T^2}\right)$ yields a straight line and the slope of this line gives the activation energy of the deep level.

3.2.3 INTERFACE STATES

Semiconductor devices are adversely affected by the presence of unwanted defect states, which are introduced near to the band edges or in the middle of the band gap of semiconductor materials. These types of defects directly affect the operation of devices for example, transistors, light-emitting diodes and other electronic and opto-electronic devices based on semiconductor materials. Deep-level traps shorten the non-radiative life time of charge carriers, and promote recombination of minority carriers, which has adverse effects on the

semiconductor device performance. On the other hand there are some other traps known as interface traps which are also very important to understand. These interface traps (states) are created during either fabrication process of devices [4] or during p-n heterojunction growth [5, 6].

The energy of these traps is distributed along the bandgap of the semiconductor. When electrons or holes are trapped in these states they act like charges at interface.

Figure 3.10 represents a schematic diagram of localized interface states in a p-n junction. The conduction process could occur via tunnelling of electrons through the interface states or recombination with the interface states and/or trap capture processes. The probability that an electron or hole occupies a given interface state depends on the energetic location of the interface state relative to the Fermi energy. The interface states also behave like impurities in bulk semiconductors. The interface states are neutral. However, when they emit electrons they behave as donors and become positively charged. On the other hand when states capture electrons they will be negatively charged and behave as acceptors as shown in Figure 3.11 (a, b).

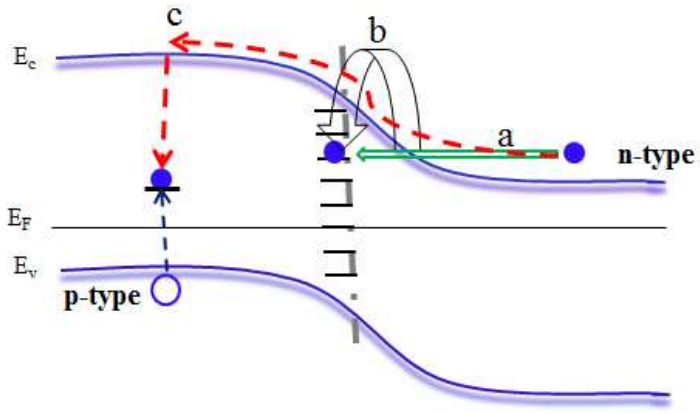

Figure 3.10: Schematic illustration of p-n junction band diagram showing different conduction processes: (a) recombination of tunnelling electrons into

interface states, (b) recombination of electrons via interface states (c) recombination via trap in the band gap [6].

The interface behaves as positively and negatively charge state and the sum of these two states can be expressed as interface states density (D_{it}) distribution having characteristic energy level called charge neutrality level (E_{CNL}). The interface states that are above this charge neutrality level behaves as acceptors and if the Fermi level (E_F) is above E_{CNL}, the interface states are negatively charged. Interface states which are below the E_{CNL} are donor states, and if the E_F is below E_{CNL}, the states are positively charged as shown in Figure 3.11 (a, b).

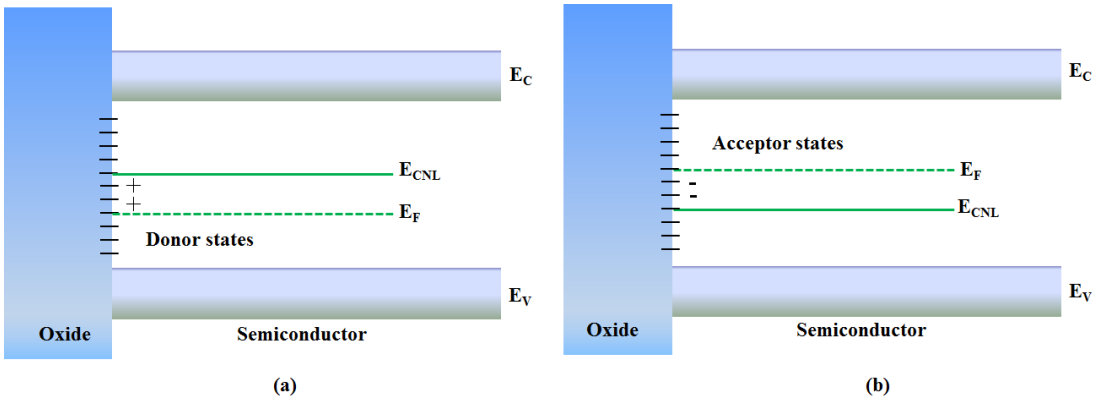

Figure 3.11: Schematic representations of (a) donor type interface state and (b) an acceptor type interface state.

The occupancy of traps at the interface can by calculated by assuming the occupancy as zero "0" when above E_F and one "1" when below E_F. By using this assumption, interface trap charges can be calculated by using the following equation;

$$Q_{it} = -q \int_{E_{CNL}}^{E_F} D_{it}\, dE \qquad E_F \text{ above } E_{CNL} \qquad 3.24$$

$$Q_{it} = -q \int_{E_F}^{E_{CNL}} D_{it}\, dE \qquad E_F \text{ below } E_{CNL} \qquad 3.25$$

where q is the elementary charge.

The density of interface states distribution across the energy gap can be expressed as:

$$D_{it} = \frac{1}{q}\frac{dQ_{it}}{dE} \qquad \text{traps}/\text{cm}^2.\text{eV} \qquad 3.26$$

The change in interface charges arises by changing the Fermi level which is used to calculate D_{it}. The detail of these calculations will be discussed in Chapter 8.

3.3 DEFECTS IN III-V COMPOUND SEMICONDUCTORS

Electronic and optoelectronic devices are seriously affected by the presence of defects, which could have many different origins. These could be intrinsic defects, foreign impurities related defects, and defects due to interface states. Therefore it is important to have knowledge of these defects to better understand the performance of the devices made from semiconductors. In this section a literature review of defects in GaAs, GaSb and GaInAsSb materials will be presented.

3.3.1 DEFECTS IN GaAs

Native defects in GaAs are primarily concerned with vacancies, interstitials, and antisite defects. Such native defects are mostly created during growth. In GaAs the most common intrinsic defect is EL2. The position of this defect in the energy gap as determined by DLTS measurements is ~0.8 eV below the conduction band edge [7]. The origin of this defect is still controversial but most commonly accepted theories predict this defect to be due to Arsenic antisite (As_{Ga}) [8-10]. Arsenic antisite is most likely associated with the family of GaAs defects; an example of this family is Gallium vacancy (V_{Ga}), Arsenic vacancy (V_{As}) and

interstitial arsenic (As_i) [11, 12]. The most complex nature of EL2 was suggested [13] to be As_{Ga} and an intrinsic interstitial (As_i) rather than just an isolated As_{Ga} defect. Similarly, A. Castaldini et al [14] studied the effect of different Te doping in GaAs. They observed a shift of energy of EL2 defect by increasing the doping concentration of Te. An increasing of Te doping resulted in the lowering of EL2 activation energy. This reduction was explained to be due to either strain in the lattice induced by dopant atoms which creates more states near the band edges or rearrangement of the atomic configuration of EL2 with the increase of doping.

Other very common intrinsic defects in GaAs are EL3, EL5 and EL6. The energy of EL3 defect ranges from 0.41 eV to 0.58 eV [15-17]. This defect is considered as complexes of Arsenic-interstitial (As_i) – Arsenic-vacancy (V_{As}) [18]. The defects EL5 and EL6 energies are ~0.43 eV to ~0.35 eV with respect to conduction band. These defects are considered as complexes of As interstitials (As_i) - Ga vacancies (V_{Ga}) and V_{Ga}-V_{As}, respectively [19-22]. Similarly two more intrinsic defects in MBE grown GaAs are named as EL7 and EL10. The energies of these defects are ~0.30eV and 0.18eV, respectively, but their origin are unclear [22, 7].

3.3.2 DEFECTS IN GaSb

GaSb, a III-V semiconductor material, has many applications in optoelectronics devices due to its band gap of ~ 0.72eV. The intrinsic defects in GaSb are Antimonide antisite (Sb_{Ga}), gallium antisite (Ga_{Sb}), Antimonide vacancy (V_{Sb}), gallium vacancy (V_{Ga}) and complexes (Ga_{Sb}-V_{Ga}). E. Kuramochi et al [25] studied MBE grown undoped and Te doped GaSb structures and observed two defects having energies of 0.25eV and 0.63eV, respectively. They attributed the defect

having energy 0.25eV to a complex of gallium antisite (Ga_{Sb}) - gallium vacancy (V_{Ga}) (Ga_{Sb}-V_{Ga}). The defect energy of 0.63 eV was attributed to the interdiffusion of Te atoms in GaSb [25]. The 0.33eV defect observed in Te doped GaSb epilayer was also attributed to the Ga_{Sb}-V_{Ga} complex of [26]. In another study of extremely low doped GaSb by W. Masonand et al [27], a trap with energy of 0.219eV was detected and assigned to a native Ga_{Sb}-V_{Ga} defect. MOCVD grown GaSb epilayers [28] also displayed a defect having energy of ~ 0.3 eV and was attributed to a Ga_{Sb} antisite or (Ga_{Sb}-V_{Ga}) complex. It is considered that this defect can be easily created and its concentration can increase in non-equilibrium way. M. Hakala et al [29] investigated theoretically native defects in GaSb by using ab-initio method. They considered fully relaxed vacancies, interstitials, and antisite defects, and found that defects in GaSb behave more or less in a similar way to those in GaAs. In addition, it was found that during diffusion of Ga atoms, Ga interstitials are formed instead of gallium vacancies (V_{Ga}) as proposed by other models. Similarly, they predicted an increase of concentration of Sb interstitials in the Sb rich diffusion condition. Figure 3.12 represents different defect states in the band gap of GaSb as calculated by M. Hakala et al [29].

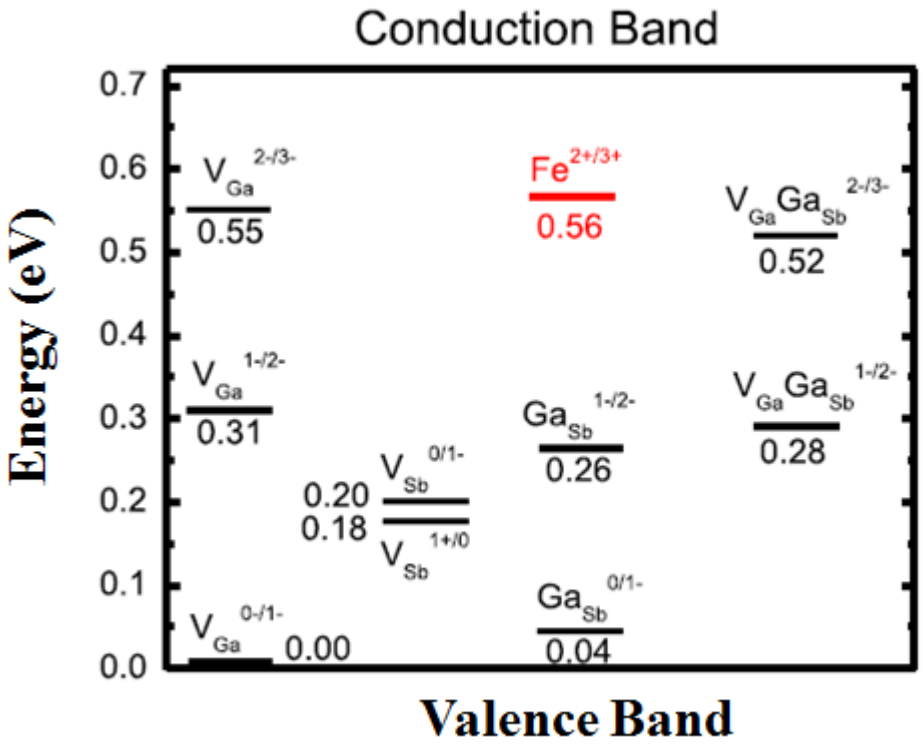

Figure 3.12: Ionization energies of native defects at 300K in GaSb calculated by M. Hakala et al [29, 30] using ab-initio method.

Venter et al [30] performed DLTS and Laplace DLTS on lower Te doped GaSb samples. They found three prominent traps having activation energies of 0.167eV, 0.243eV and 0.295eV. In their investigation they observed electrical field enhanced emission in trap having energy 0.167 eV. This is a positively charged trap with Poole Frenkle emission enhancement behavior was attributed to Antimony Vacancy (V_{Sb}). The origins of the other two traps with activation energies of 0.243 and 0.295 eV were assigned to Antimony antisite (Ga_{Sb}) and complex of vacancy-antisite (V_{Sb}-Ga_{Sb}), respectively. These activation energies were comparable to those calculated by M. Hakala et al [29].

3.3.3 DEFECTS IN GaInAsSb

The operation of infrared detectors (IR) in the 2 - 2.6 μm range made GaInAsSb an interesting candidate for use as gas sensing, chemical process monitoring, photovoltaics, and astronomy applications. The commonly used detectors in this range are HgCdTe and strained InGaAs grown on InP substrates. However, the alternative to these conventionally available detectors are quaternary GaInAsSb alloys which are very promising materials and cover the wavelength range of 1.7-2.6 μm [31].

The quaternary GaInAsSb material grown on GaSb substrate suffers carrier losses due to high density of defects in GaSb. The GaSb substrate with defects density of $<10^3$ defects/cm^2 is very expensive and also not available with large diameter of wafer (maximum available wafer size is 3 inches) [32]. The alternative is to grow GaInAsSb material on conventional substrates such as GaAs. However, the large mismatch between GaAs and GaInAsSb could cause serious degradation of such IR operating devices. This can be overcome by growing GaInAsSb material on top of GaSb. K. C. Nunna et al [33] studied GaInAsSb based detectors grown on GaAs substrates. The approach they used to grow GaInAsSb is named as Interfacial Misfit (IMF) technique. On GaAs substrate, GaSb material is grown by IMF technique with expectedly lower density of threading dislocations. On top of GaSb they grew GaInAsSb, and it was claimed that the peak responsivity and maximum detectivity of these devices are comparable to those grown on GaSb substrates. Furthermore, they concluded that high internal quantum efficiency and low dark currents at room temperature provide evidence of good crystalline quality of GaInAsSb alloys achieved by the IMF-array technique. Dashiell et al [34] who studied InGaAsSb thermo-photovoltaic devices, found that the thermo-

photovoltaic efficiency (TPV) and power density (PD) of InGaAsSb were well below than those they expected. They explained that the open circuit voltage (V_{oc}) of the device is dominated by intrinsic recombination processes of bulk defect states. T. I. Voronina et al [35] investigated the electrical properties of GaSb based material (including InGaAsSb) by using temperature dependent Hall effect, conductivity, mobility and spectral dependence of photoconductivity. It was found that by increasing the composition of In, x, in the $In_xGa_{1-x}As_ySb_{1-y}$ material system reduced the formation of $Ga_{Sb}V_{Ga}$ complexes and lowered the concentration of deep acceptors in the crystal. They detected four impurity states in InGaAsSb, two of which were believed to be of the same origin as in GaSb.

S. Li et al [36] studied structural defects in InGaAsSb grown on GaSb using Scanning Tunnelling Electron Microscopy (STEM). The defects observed in InGaAsSb were mixture of 60^o and 90^o stacking faults and some threading dislocations. Among these strained induced defects, 60^o and 90^o dislocations propagated to the surface of InGaAsSb. The 90^o dislocations are most favourable to accommodate lattice mismatch and reduce threading.

The photoluminescence (PL) spectra of LPE (Liquid Phase Epitaxy) grown $Ga_{0.96}In_{0.04}As_{0.11}Sb_{0.89}$ was studied by K.D. Moiseev et al [37] at different temperatures and laser-excitation intensities. The main radiative transitions were observed in Te doped $Ga_{0.96}In_{0.04}As_{0.11}Sb_{0.89}$. The radiative transitions detected at low temperatures between (4K-150K) were believed to involve the first and second ionization state of native-antisite defects (V_{Ga}-Ga_{Sb}) while the interband transition was dominant at higher temperatures (>150K).

The current transfer mechanism was studied in p-GaSb/p-GaInAsSb/n-GaAlAsSb heterojunctions with p-type GaInAsSb as an active region [38]. The I-

V and C-V analysis was performed on devices in the temperature range of 10–360 K. It was concluded that the current transport through the devices can be accounted for by three different mechanisms namely, diffusion, generation and tunnelling. The diffusion current is the dominant component at high temperatures (230K–360K). At intermediated temperature (160K-230K), the current is influenced by the mid-gap generation centre, originating from GaInAsSb, with activation energy 0.26 eV as determined from I-V measurements. The low temperatures (≤150K) current was dominated by the tunnelling mechanism.

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CHAPTER 4

EXPERIMENTAL TECHNIQUES

This chapter describes the electrical characterization techniques such as conventional DLTS , Laplace DLTS, and conductance and capacitance as function of frequency that are used to investigate the samples presented in this thesis. The details of hardware and software of these methods will also be presented. In conventional DLTS and LDLTS techniques space charge capacitance as function of the space charge region of a p-n junction or Schottky diode are used. The properties of p-n diodes, which were utilised to study deep traps will be discussed.

4.1 P-N JUNCTION

A p-n junction is formed when p-type material make contact with n-type material. The energy band diagram of such p-n junction is shown in Figure 4.1. Two rules are used to construct the energy band diagram of a p-n junction: (1) the vacuum level should be continuous and (2) the Fermi energy should be constant across the junction at thermal equilibrium.

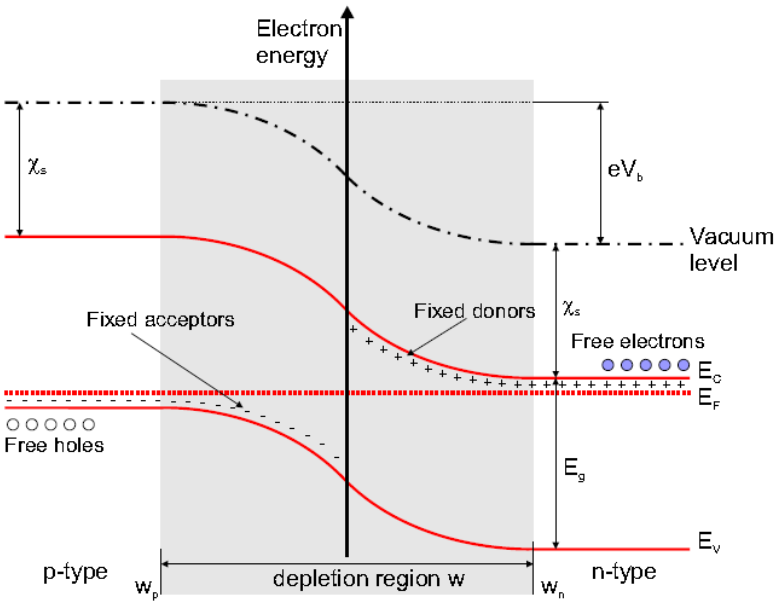


Figure 4.1: Energy band diagram of a p-n junction under reverse bias.

The electron affinities (χ_s) of both n and p type semiconductors are the same on both sides, and therefore the band bending is caused entirely by the difference in Fermi energies with respect to the conduction band of both materials and is given by:

$$(\mathrm{E_c^p} - \mathrm{E_F}) + \chi_\mathrm{s} = (\mathrm{E_c^n} - \mathrm{E_F}) + \chi_\mathrm{s} + \mathrm{eV_b} \qquad 4.1$$

Where E_c^p and E_c^n are conduction bands for p and n side, E_F is the Fermi energy, χ_s is the electron affinity and V_b is the built-in voltage.

From equation 4.1 the built-in voltage is calculated as

$$eV_b = E_g + (E_F - E_c^p) - (E_c^n - E_F) \qquad 4.2$$

where E_g is the energy gap of a semiconductor. The built-in voltage, which represents the total net electrostatic charges semiconductors, is temperature dependent and is given as;

$$V_b = \frac{k_b T}{e}\left(\frac{N_a N_d}{n_i^2}\right) \qquad 4.3$$

where N_a and N_d are the acceptor and donor concentrations in p and n side of the junction, respectively. n_i is intrinsic charge density and is given by

$$n_i = \sqrt{N_c N_v} exp^{\left(-\frac{E_g}{2k_b T}\right)}$$

where N_c and N_v are effective density of states in conduction and valence band, respectively.

A depletion region exists on both n and p side of the junction where the fixed donor and acceptor charges at the interface of the p-n junction lead to the band bending. There are no charges in the depletion region and the following relationship will be hold:

$$N_a w_p = N_d w_n$$

where w_p and w_n are width of depletion region on p and n side of junction, respectively. For similar doping concentrations on both of n and p sides of the semiconductor, the depletion width will be comparable. Such a junction is called linearly graded junction. However, if the doping concentrations on either side of semiconductor are different, the depletion width will be one sided and such junction is called abrupt junction.

4.1.1 WIDTH OF THE DEPLETION REGION

The entire band bending across the depletion region is defined by the sum of the built-in voltage (V_b) and applied external bias V_R. The depletion width of asymmetric junction (or abrupt junction) where doping on n side (N_d) >> doping

on p side (N_a). The electric field and potential is calculated by using Poisson equation

$$\frac{\mathrm{dE}}{\mathrm{dx}} = \frac{\rho}{\varepsilon} = \frac{q}{\varepsilon}(-N_a + N_d) \qquad 4.4$$

Where $$\rho = \begin{cases} -qN_a & for\ -w_p \leq w \leq 0 \\ qN_d & for\ \ 0 \leq w \leq w_n \end{cases}$$

The electric field can by calculated by following equation,

$$E = \begin{cases} \frac{qN_a(w+w_p)}{\varepsilon} & for\ -w_p \leq w \leq 0 \\ \frac{qN_d(w_n-w)}{\varepsilon} & for\ 0 \leq w \leq w_n \end{cases} \qquad 4.4a$$

Whereas, the potential across the junction is calculated by following equation.

$$\mathrm{V} = \frac{1}{\varepsilon_s}\int_0^{w_n} x\rho(x)dx \qquad 4.4b$$

ρ(x) is the charge density of the space charge region of width (W) and is given by $\rho(x) = -qN_d$.

Hence the width of the depletion region on the n side can be calculated from equation 4.4,

$$w_n = (2\varepsilon_s \frac{(V_b+V_R)}{qN_d})^{1/2} \qquad 4.5$$

If the p-n junction is symmetric, the depletion region extends equally into the p- and n-doped semiconductors. The total depletion width is given by:

$$w = w_n + w_p = [2\varepsilon_s \frac{(N_a+N_d)}{qN_dN_d}\ (V_b + V_R)]^{1/2} \qquad 4.6$$

Similarly when a forward bias V_F is applied to the p-n junction the depletion width is expressed as:

$$w = w_n + w_p = [2\varepsilon_s \frac{(N_a+N_d)}{qN_dN_d}\ (V_b - V_F)]^{1/2} \qquad 4.7$$

4.1.2 DEPLETION LAYER CAPACITANCE

The capacitance associated with space charge region of a p-n junction is called depletion capacitance. The differential form of depletion capacitance can be expressed as:

$$C = \frac{dQ}{dV_R} \qquad 4.8$$

The entire stored charge inside the asymmetric depletion region p-n junction is given by:

$$Q = qN_d \mathrm{A}.w_n = A.\sqrt{q\varepsilon_s N_d V}$$

The capacitance of asymmetric p-n junction is given by:

$$C = \frac{dQ}{dV} = A.\sqrt{\frac{q\varepsilon_s A N_d}{V_b + V_R}} \qquad 4.9$$

Similarly, the capacitance of a symmetric p-n junction is given by:

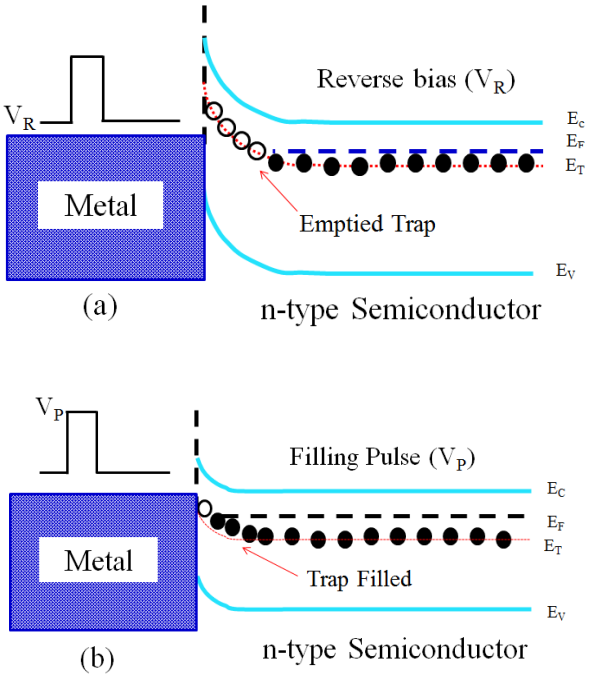
$$C = \frac{dQ}{dV} = \sqrt{\frac{q\varepsilon_s A(N_a + N_d)}{(V_b + V_R).(N_a.N_d)}} \qquad 4.9$$

The capacitance-voltage characteristics of a p-n junction allow the measurement of the background doping concentration and doping concentration profile of the semiconductor. The plot of $1/C^2$ versus (V_b+V_R) results in a straight line and the slope of this line gives the doping concentration whilst the intercept at $1/C^2 = 0$ yields the built-in-voltage across the junction. Information about interface states can also be extracted using the capacitance-voltage characteristics using plots of $1/C^2$ versus V_R and C versus $(V_b+V_R)^{-1/2}$. In both cases one should get a straight line with intercept passing through the origin. If the plot of C versus $(V_b+V_R)^{-1/2}$ does not go through the origin of the axes one can directly extract information about the value of interface capacitance [1].

4.2 DEEP LEVEL TRANSIENT SPECTROSCOPY (DLTS)

Historically, the time-resolved capacitance measurement was initially used to study and characterize deep levels caused by impurities or defects. In 1974 D. V. Lang et al [2] introduced a very powerful technique, namely DLTS, to characterize the electrical defects present in devices. They used the concept of space charge capacitance to determine the activation energies and capture cross-sections of defects by variation of the depletion width and the sample temperature.

In order to understand the basic principle of operation of the DLTS technique, one must have some basic knowledge of the capacitance transients arising from the space charge region of a p-n or Schottky diode as shown in Figure 4.2.



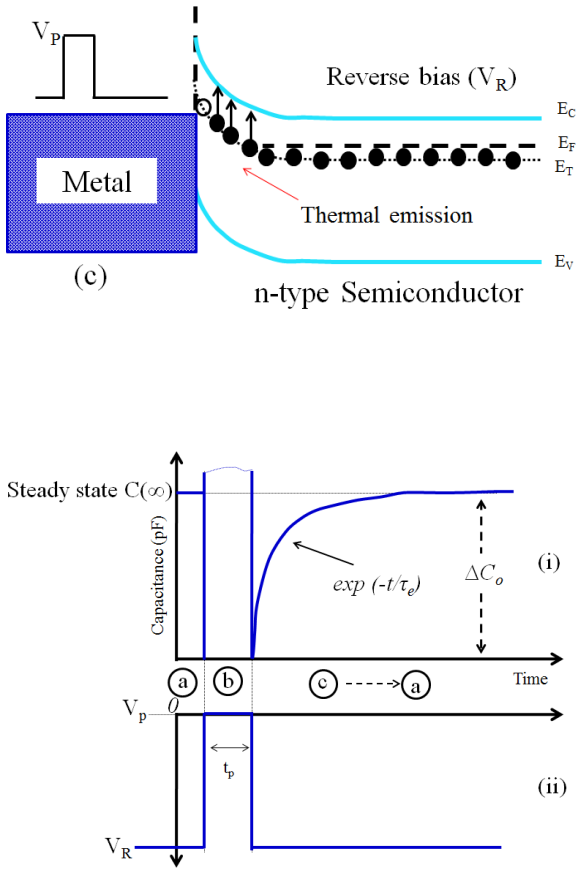


Figure 4.2: Schematic representation (a) emptying of traps with reverse bias (V_R) (b) filling of traps with filling pulse (V_P), (c) thermal emission from the filled traps and (d) DLTS pulses.

Figure 4.2 (a,b,c) represent a simple case of the energy band diagram of a Schottky diode. In an initial step [Figure. 4.2(a)], a reverse bias V_R is chosen in such a way that the Fermi level move up, and therefore the traps above the Fermi level will be empty. In Figure 4.2 (b), a filling voltage pulse (V_P) is applied so that the traps capture electrons. In order to fill the traps completely, a long duration filling pulse (t_p) is applied. After the pulse the reverse bias is restored, i.e. the depletion region moves back to its original width. The trap thermally emits electrons between the voltage pulses as shown in Figure 4.2 (c). The schematic representation of emptying and filling of traps with the DLTS pulses are shown in Figure 4.2.

4.2.1 CAPACITANCE TRANSIENTS

In order to define the initial state of traps in the device under investigation one needs to extend the depletion width by applying a certain reverse bias (V_R) as shown in Figure 4.2a. This will empty the traps and the rate equation of capturing electrons by these traps is given by:

$$\frac{dn_t}{dt} = c_n(N_T - n_T) \qquad 4.10$$

Where c_n is the capture coefficient of electrons, N_T is total number of available trap states and n_t is number of trap states occupied by electrons. The capture coefficient of electrons is given by,

$$c_n = \sigma_n < v_{th} > n$$

Where $\sigma_n$the capture cross-section of electrons, $< v_{th} >$ is the thermal velocity of electrons and $n \cong N_d$is the effective doping concentration.

Now when the filling pulse V_P is applied for a particular filling pulse time t_P, the depletion width will go back to initial position (equilibrium position) and the traps outside of the depletion will fill completely as shown in Figure 4.2b. After the filling pulse V_P, the depletion width is increased again due to the large reverse bias as shown in figure 4.2c. The electrons will re-emit and the corresponding emission rate equation is expressed as:

$$\frac{dn_t}{dt} = e_p N_T - (e_n + e_p)n_T \qquad 4.11$$

where e_n, e_p, n_T and N_T are electron emission, hole emission, number of states occupied and total number of available states, respectively. The emission of free electrons is an instantaneous process on time scale of experiment. However, the emission of electrons from localized traps is usually a slow process and its time

dependence can be determined by capacitance transient measurements. The trap emission process and respective change in capacitance in time scale is shown in Figure 4.2 (i, ii).

Equation 4.11 will have the following form when traps are full at time t = 0

$$n_t(t) = \begin{cases} N_T & for\ t \leq 0 \\ \left(\frac{e_p}{e_p+e_n}\right) N_T \exp(-(e_p + e_n)t\ ) & for\ t > 0 \end{cases} \qquad 4.12$$

Similarly when the trap is empty it will have following form,

$$n_t(t) = \begin{cases} 0 & for\ t \leq 0 \\ \left(\frac{e_p}{e_p+e_n}\right) N_T\{1 - \exp(-(e_p + e_n)t)\} & for\ t > 0 \end{cases} \qquad 4.13$$

From equation 4.12 it is clear that the emission of charges from the traps follow an exponential behaviour with a time constant given by:

$$\tau = \frac{1}{e_p + e_n}$$

Thus the concentration of the deep level trap can be determined from the amplitude of the transient, and the time constant gives the emission rate of electrons. Hence for electron emitting trap, $e_n \gg e_p$, equation 4.11 will have following form:

$$n_t(t) = N_T \exp(-\left(\frac{t}{\tau}\right)) \qquad 4.14$$

Similarly, from equation 4.13, the concentration for initially empty trap will be

$$n_t(t) = N_T(1 - \exp(-\left(\frac{t}{\tau}\right))) \qquad 4.15$$

where

$$\tau = \frac{1}{e_n}$$

The simplest indirect method of measuring the variation of occupancy of traps is measured by monitoring the capacitance changes.

As described in the previous section, the capacitance of a junction is expressed by:$C = \frac{\varepsilon A}{W}$

The width of depletion region including filled traps contribution becomes:

$$w = \sqrt{\frac{2\varepsilon(V_b + V_R)}{qN_d^*}} \qquad 4.16$$

where $N_d^* = N_d - n_t$ and ε is the relative permittivity of semiconductors, V_b is built-in voltage and V_R is the applied reverse bias. For $n_t \ll N_d$, equation 4.16 can be expanded and will have the following expression:

$$\Delta C = C_\infty(1 - \frac{n_t}{2N_d}) \qquad 4.17$$

where ΔC is the amplitude of the capacitance transient and C_∞ is the steady state capacitance.

From equation 4.17 the information about majority carrier traps can be deduced from:

$$\Delta C = C_\infty(1 - \frac{n_t}{2N_d}\exp(-\left(\frac{t}{\tau}\right))) \qquad 4.18$$

Similar information for minority carrier traps can also be deduced. The sign of capacitance transient is opposite to the of majority carrier traps. In this way distinction between majority and minority carrier traps can be made from the sign of the capacitance transients.

4.2.2 CONVENTIONAL DLTS

This technique is based on the change in capacitance between two points in time t_1 and t_2 during the carrier emission process. The difference in capacitance

$[C(t_1) - C(t_2) = \Delta C]$ as function of temperature 'T' produces the conventional DLTS output signal.

The DLTS signal is given by:

$$S(t) = C(t_1) - C(t_2) = \Delta C_0[exp(-e_n t_1) - exp(-e_n t_2)] \qquad 4.19$$

or

$$S(t) = C(t_1) - C(t_2) = \Delta C_0 \left[exp\left(-\frac{t_1}{\tau}\right) - exp\left(-\frac{t_2}{\tau}\right)\right] \qquad 4.20$$

where "τ" is the inverse of emission rate.

ΔC_0 is the change in capacitance at time t = 0 and is given by

$$\Delta C_0 = \frac{C_0 N_T}{2N_d} \qquad 4.21$$

The DLTS signal will be small if $\tau\left(\frac{1}{e_n}\right) \ll (t_1 - t_2)$ and $\tau\left(\frac{1}{e_n}\right) \gg (t_1 - t_2)$. The DLTS signal is maximum when $\tau\left(\frac{1}{e_n}\right) \approx (t_1 - t_2)$.

The maximum emission will be obtained when $\frac{dS(T)}{d\tau} = 0$, for

$$\tau = \tau_{max} = \frac{(t_2 - t_1)}{ln\left(\frac{t_2}{t_1}\right)} \qquad 4.22$$

Equation 4.22 is called the rate window and has typical values from $5s^{-1}$ to $5000s^{-1}$. The value of rate window can be changed by choosing different time t_1 and t_2. Different rate windows produce different DLTS peaks at different temperatures. Thus the activation energy of the trap can be determined by measuring the emission rates as a function of temperature using different rate windows and then plotting them in the Arrhenius plot as shown in Figure 4.3.

Equations 4.21 and 4.22 show that the maximum peak height does not depend upon the absolute value of t_1 and t_2. However, it depends upon the ratio (t_2/t_1).

ΔC_o corresponds to the maximum amplitude of DLTS signal, and therefore by using equation 4.21 one can determine the trap concentration.

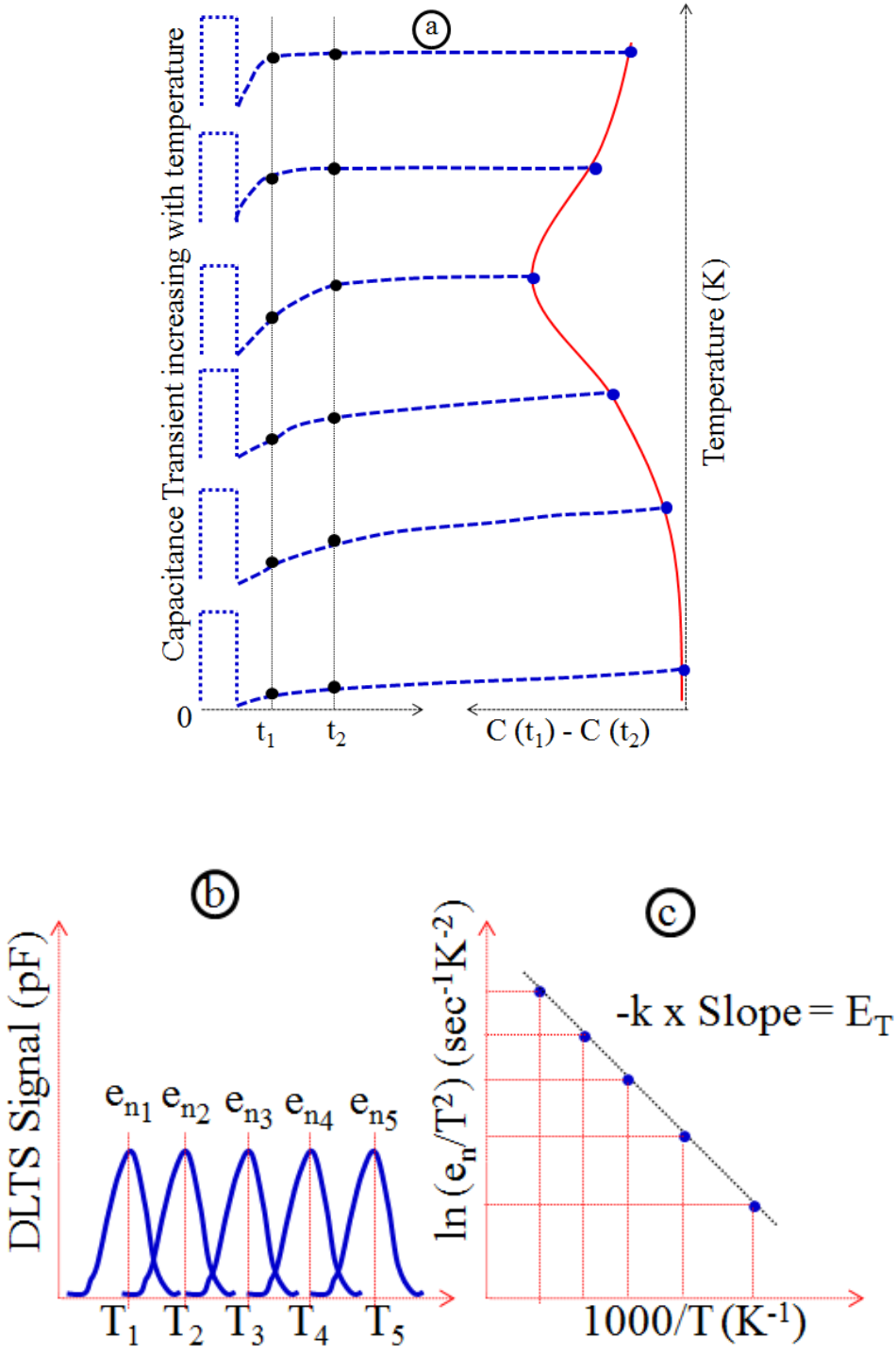


Figure 4.3: (a) Schematic diagram illustrating the formation of DLTS spectra. , (b) DLTS signal at different rate windows and (c) extraction of activation energy from DLTS signals by using Arrhenius plot.

The activation energy and capture cross-section of traps can be calculated by using equation 3.23. The activation energy is extracted from the slope of the Arrhenius plot and the capture cross-section is estimated from the intercept of the Arrhenius plot shown in Figure 4.3.

4.2.2.1 CAPTURE CROSS-SECTION MEASUREMENTS

The value of capture cross-section obtained from Arrhenius plot is an estimated value. However, the actual value of capture cross-section can be determined by using the "filling pulse" technique. The filling pulse time used in DLTS experiments is long enough to fill all the traps. However, by varying the filling pulse time (from short to long filling pulses) one can ascertain the temperature dependence of the trap capture process. It also provides information about the nature of the defect, e.g. a point defect or band like defect (closely spaced defects) [3, 4]. The capture measurements are carried out by changing the filling pulse time and measuring the corresponding DLTS peak amplitude by fixing the reverse bias and temperature. The capture kinetic of an ideal case is given by:

$$\frac{\Delta C_o^{max} - \Delta C_o(t_p)}{\Delta C_o^{max}} = exp(-c_n t_p) \qquad 4.23$$

where ΔC_o^{max} is the maximum DLTS amplitude corresponding to complete trap filling and $\Delta C_o(t_p)$ is the DLTS amplitude at each filling pulse time. Hence from equation 4.23 the value of the capture coefficient c_n can be calculated by plotting $\frac{\Delta C_o^{max} - \Delta C_o(t_p)}{\Delta C_o^{max}}$ versus filling pulse time t_p.. The trap capture cross-section can be calculated using equation 3.11 (see section 3.3.2).

$$c_n = \sigma_n < v_{th} > n$$

This method allows determining the accurate capture cross-section of a trap and not the apparent capture cross section that one can calculate from Arrhenius plot. This method is also effectively used to distinguish between point defects and extended defects by varying filling pulse time [3]. As for point defects, the DLTS amplitude will be completely saturated for a certain duration of the filling pulse. The plot of log (t_p) versus DLTS amplitude will have an exponential behaviour. However, for the case of extended defects, the DLTS amplitude will never saturate and as a result the plot of log (t_p) versus DLTS amplitude is expected to have logarithmic behaviour.

4.2.2.2 CONCENTRATION DEPTH PROFILING MEASUREMENTS

The defects distribution in semiconductors is usually non-uniform. In order to get information about defects distribution the double pulse DLTS (DDLTS) [5] technique is usually employed. The schematic representation of DDLTS is shown in Figure 4.4.

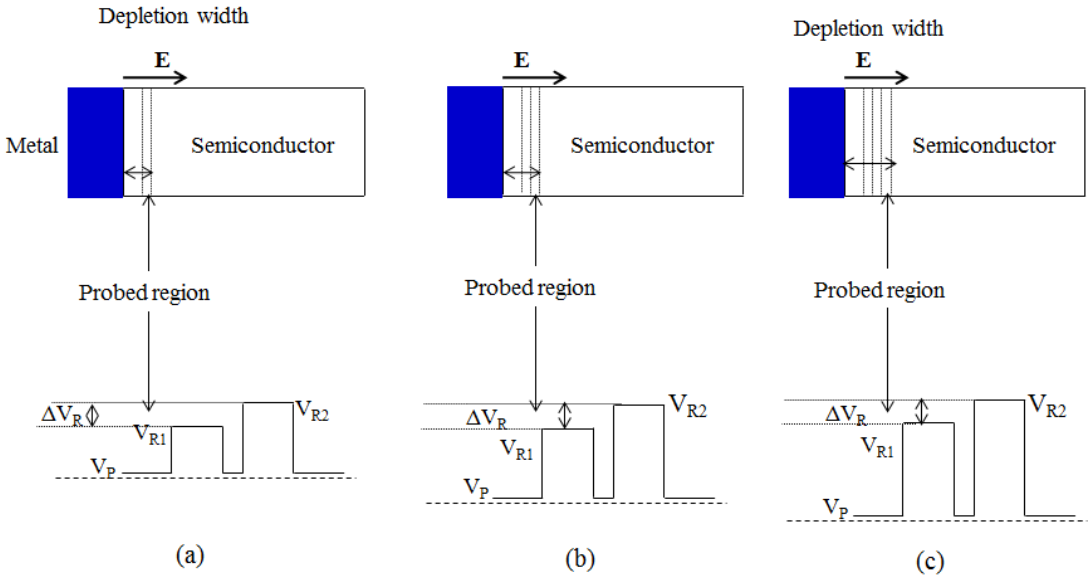


Figure 4.4: Schematic representation of probing different regions in a semiconductor structure by applying the double pulse DLTS technique.

In this method two pulses are used: pulse one with reverse bias V_{R1} and pulse two with reverse bias V_{R2} are applied. The ratio V_{R2}/V_{R1} is kept constant while the amplitudes of V_{R1} and V_{R2} are changed in order to get information about emissions in a small selected area of the device. This technique is very accurate as it minimises the Debye tailing effect. By careful analysis of the data, the doping concentration from each measurement can be extracted, and the defect concentration depth profile can be determined. This method is also used to investigate the field dependence of the emission rate of the defect. The detail about field dependence effect by using DDLTS is given in detail in reference [6].

4.3 LAPLACE DLTS SPECTROSCOPY

One of the problems by using conventional DLTS technique is the accurate measurement of the temperature during the thermal scan process. It is difficult to measure accurately the activation energies as the temperature increases or decreases during the measurements. Another issue by using conventional DLTS is poor time constant resolution for studying fine structures during the emission process. Any variation in time constant will result in a broader DLTS spectrum. Thus, the resolved structure is not achievable unless the time constants are well separated. By using Laplace DLTS spectroscopy technique all these issues are addressed and an improved resolution is obtained. Laplace DLTS is an isothermal technique in which the sample is held at fixed temperature. In the Laplace DLTS the signal from time domain (conventional DLTS Mode) are converted to the frequency domain. LDLTS digitizes the analog transient output using different

schemes, and averages many digitized transients during the emission process in order to increase the signal to noise ratio [7].

The mathematical approach, which has been utilized for the quantitative description of the capacitance transients, is given by

$$f(t) = \int_0^\infty F(s) \exp^{-st} ds \qquad 4.24$$

where f(t) is the recorded transient and F(s) represents the spectral function. The mathematical representation of the capacitance transient given in equation (4.24) is the Laplace transforms of the true spectral function F(s). To deduce the different emission rates embedded in f(t) one needs to apply any suitable algorithms that perform the inverse Laplace transform for the function f(t). To do so three main algorithm routines known as FLOG, CONTIN and FTIKREG have been used in Laplace DLTS technique [8]. The three algorithm are used to increase the confidence level of spectra obtained by Laplace DLTS. Only one routine is used to analyse the data. The result of such procedure is a spectrum of delta-like peaks for the multi-exponential transients as illustrated in Figure 4.5 (b). Laplace DLTS shows the output intensity as a function of emission rates and the area under the peaks is related to the trap concentration. The capacitance transient acquired by Laplace DLTS is shown in Figure 4.5 (a). Due to its high resolution, Laplace DLTS has been used to separate the conventional DLTS peaks obtained from very closely spaced defects, for example when their emission rates are different from each other, or in some cases even if the emission rates are nearly similar but their energies are different. For example, Laplace DLTS has been used previously to separate the two closely spaced hydrogen and gold related defects in silicon [9]. Conventional DLTS scan in Figure 4.6 shows only

one broad peak for both defects. However Laplace DLTS shows two well resolved peaks related to hydrogen and gold (as shown in Figure 4.6) [9].

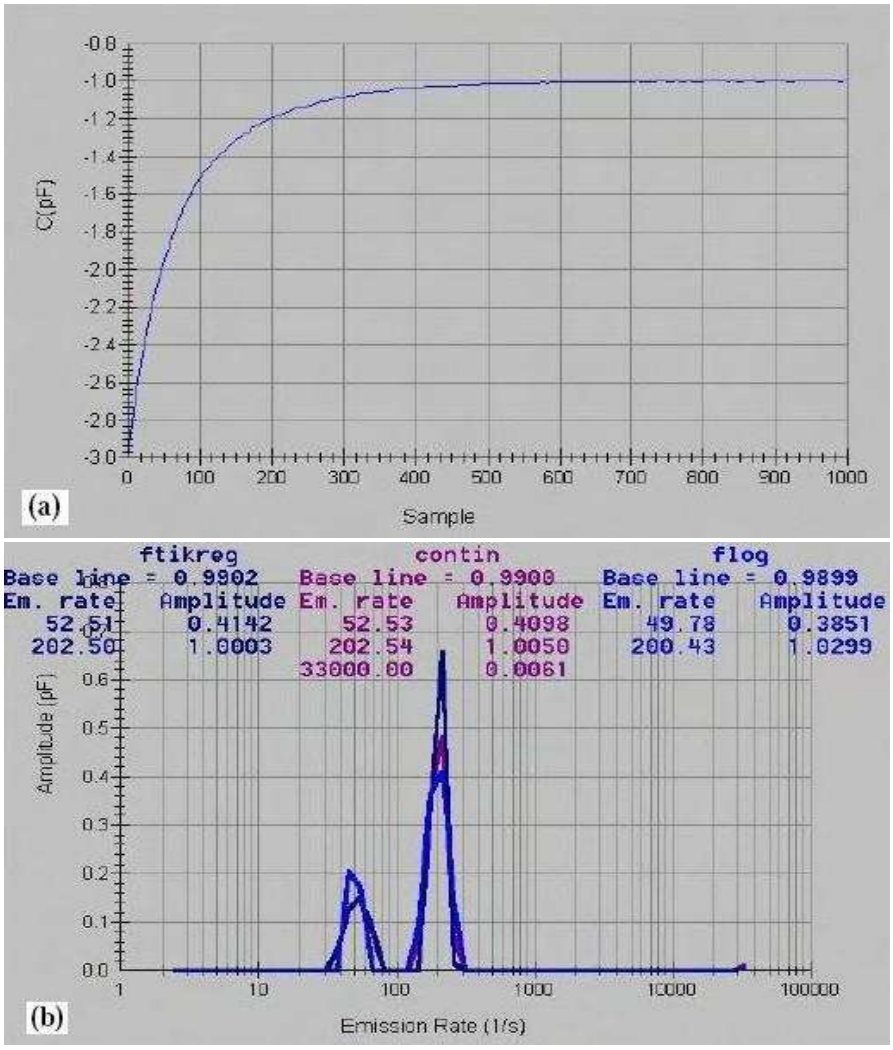


Figure 4.5: (a) Capacitance transient of Laplace DLTS (b) spectrum of delta-like peaks for multi-exponential Laplace DLTS transients.

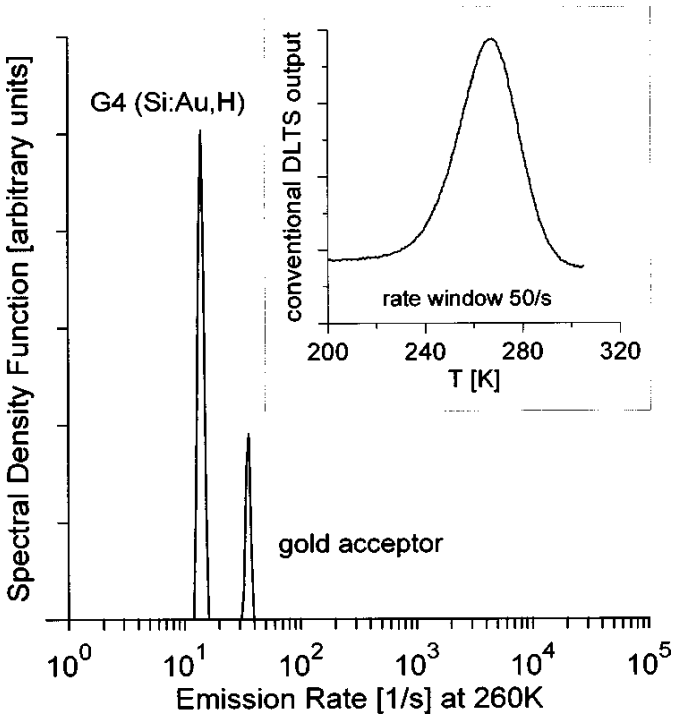


Figure 4.6: DLTS and LDLTS spectra of hydrogenated Si containing gold. The conventional DLTS spectrum have ratewindow $50s^{-1}$ is shown as an inset at the top right. The broad DLTS peak centered at 260 K is observed. The Laplace DLTS technique clearly separates two traps from broader DLTS peak [9].

4.4 CONDUCTANCE AND CAPACITANCE METHODS FOR DENSITY OF INTERFACE STATES (D_{IT})

Interfaces trapped charges, also called interface states, are attributed to dangling bonds or other defects at semiconductor/insulator or between heterojunctions interfaces. In order to extract information about the density of these interface state charges, capacitance and conductance measurement techniques are usually employed.

High and low frequency capacitance measurements are used to determine specific the capacitances of the device [10]. The capacitance at high frequency is given by

$$C_{HF} = \left[\left(\frac{C_D.C_{ox}}{C_{ox}+C_D}\right)\right] \qquad 4.25$$

where C_D is the depletion-layer capacitance and C_{ox} is the oxide capacitance. Similarly the capacitance at low frequency is given by

$$\frac{1}{C_{LF}} = \left[\frac{1}{C_{ox}} + \frac{1}{C_{it}+C_D}\right] \qquad 4.26$$

where C_{it} is the interface trap capacitance. By using Equations (4.25) and (4.26), the interface trap capacitance is calculated as,

$$C_{it} = \left[\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right]^{-1} - \left[\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right]^{-1} \qquad 4.27$$

The interface states density (D_{it}) is then given by

$$D_{it} = \frac{C_{it}}{qA} \qquad 4.28$$

where q is the electronic charge and A is the area of the device.

By substituting equation 4.27 in equation 4.28, D_{it} will have the following form.

$$D_{it} = \frac{1}{qA}\left[\frac{C_{LF}C_{HF}}{(C_{ox}-C_{LF})} - \frac{C_{LF}C_{HF}}{(C_{ox}-C_{HF})}\right] \qquad 4.29$$

Nicollian and Goetzberger [11] proposed one of the most sensitive methods to evaluate the interface trap density D_{it}, known as the conductance method. The conductance method is based on measuring the parallel conductance G_P of a device as a function of bias voltage and frequency. This G_P represents the loss mechanism caused by capture and emission of carriers from the interface traps, and can be used to extract the interface state density.

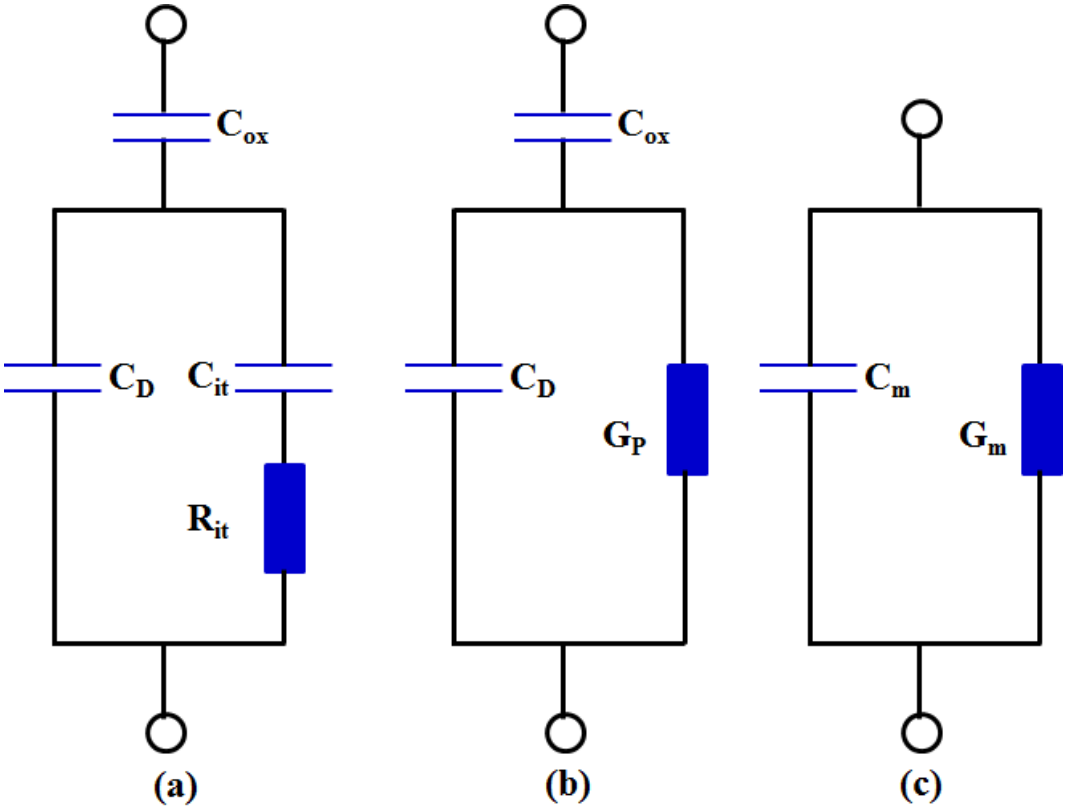


Figure 4.6: Schematic diagram of equivalent circuits for conductance method; (a) device with interface trap with time constant $\tau_{it}=R_{it}C_{it}$; (b) simplified circuit of (a); (c) circuit using measured capacitance (C_m) and conductance (G_m).

Figure 4.6 (a) illustrates the equivalent circuit of the conductance method, where C_D represents the depletion capacitance, C_{it} is the interface state capacitance, C_{ox} is the oxide capacitance and R_{it} is the loss mechanism during the capture and emission of carriers from the interface traps. Figure 4.6 (a) can be replaced by the circuit of Figure 4.6 (b), where C_P and G_P are calculated capacitance and calculated conductance and are given by,

$$C_P = C_D + \frac{C_{it}}{1+(\omega\tau_{it})^2} \qquad 4.30$$

$$\frac{G_P}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \qquad 4.31$$

where $C_{it}=q^2D_{it}$, $\tau_{it}=R_{it}C_{it}$ and $\omega= 2\pi f$ (f is the measurement frequency), τ_{it} is the interface state time constant and is given by

$$\tau_{it} = \left[v_{th}\sigma N_d exp^{(-qVb/KT)}\right]^{-1} \qquad 4.32$$

Comparing the two circuits in Figure 4.6(b) and 4.6(c), G_P/ω can be expressed in terms of C_m, C_{ox} and G_m as [12],

$$\frac{G_P}{\omega} = \frac{\omega C_m G_m (C_m - C_{HF})}{G_m + (C_m - C_{HF})^2(\omega)^2} \qquad 4.33$$

The conductance G_P is measured as a function of frequency and plotted as G_P/ω versus ω [12]. G_P/ω has a maximum and the density of interface states is determined from the maxima of G_P/ω as

$$D_{it} = \frac{2.5}{q}\left(\frac{G_P}{\omega}\right)_{max}.$$

4.5 SYSTEM HARDWARE IMPLEMENTATION

4.5.1 DESCRIPTION OF SYSTEM HARDWARE

The detail of the experimental setup used for conventional DLTS, Laplace DLTS and conductance measurements consist of following equipment: (1) Janis cryostat and temperature controller, (2) capacitance meter, (3) Current-Voltage source meter, (4) data acquisition and BNC connectors box for analog Input (I)/Output (O). All these equipments are controlled through core i-3, 64bit computer. Figure 4.7 shows the block diagram of the Laplace DLTS setup.

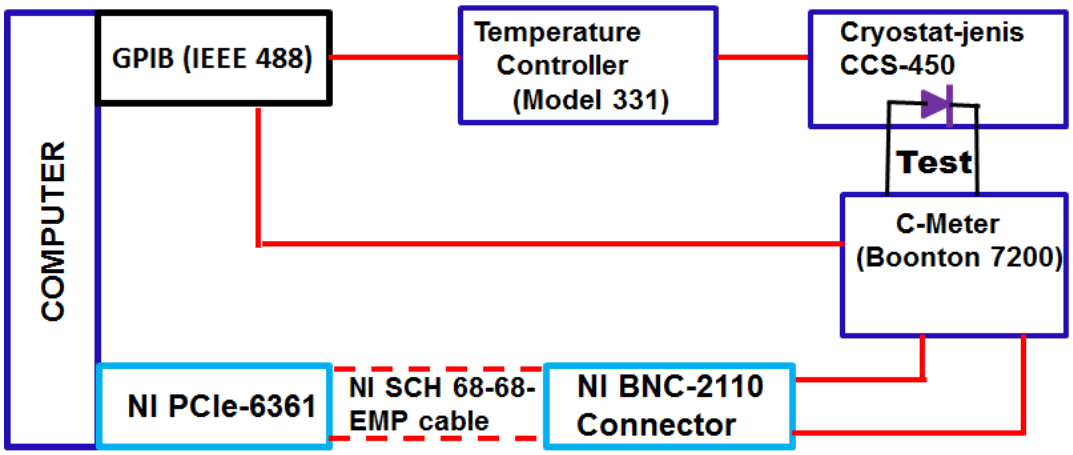


Figure 4.7: Block diagram of Laplace DLTS setup.

4.5.1.1 CRYOSTAT AND TEMPERATURE CONTROLLER

The emission from the traps depends upon the temperature. In order to get accurate information about defects, one needs very stable temperature. The cryostat (model Janis CCS-450) is used for this purpose. It operates for a temperature range of 10K to 450K with stability of ±1K.

The internal structure of the cryostat system as shown in Figure 4.8 consists of (1) a cold finger which is attached with sample holder, (2) a radiation shield, (3) lightweight aluminium vacuum shroud, and (4) electrical ports for sample contacts and thermal sensors. The cryostat is a closed cycle refrigeration system which operates with a compressor which ensures the continuous flow of helium gas (He) through a high efficiency flexible six feet cryogen transfer line.

The temperature of the samples is monitored with Lake Shore 331, which senses the temperature in the cryostat through a sensor located very close to the sample.

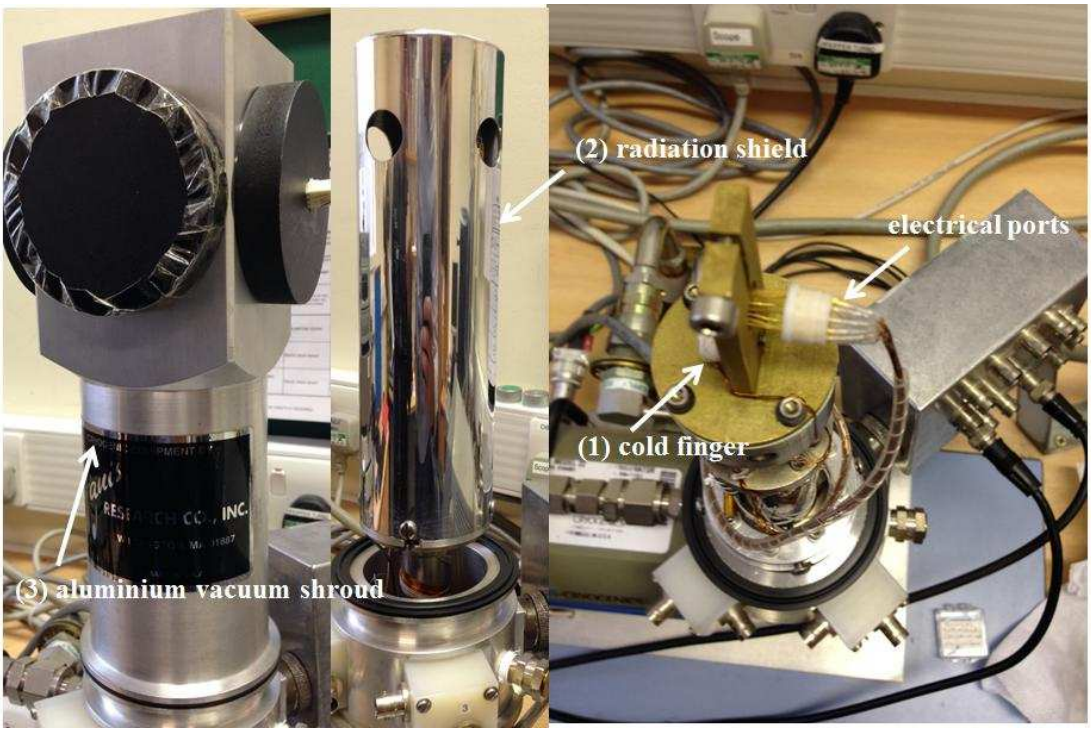


Figure 4.8: Photograph of the cryostat (model Janis CCS-450) used for the DLTS experiments.

4.5.1.2 CAPACITANCE METER

The capacitance meter which measures the transient should have a high response time. The capacitance Boonton 7200 meter is used for this purpose. It has a response time of ~120μs which is suitable for DLTS measurements. It is also used to perform C-V measurements at a range of temperatures. The Boonton 7200 meter sampling frequency for the capacitance transient is 1MHz.

4.5.1.3 CURRENT-VOLTAGE SOURCE METER

The I-V characteristics are performed by using current-voltage source-meter, model Keithley 236. The I-V measurements are performed on each sample to determine their suitability (reverse current in the range of few micro Amps) for DLTS measurements. Keithley 236 current meter offers a source voltage and

source current in the range 100μV-110V and 100fA-100mA, with a good sensitivity of ±10μV and 10fA, respectively.

4.5.1.4 DATA ACQUISITION AND BNC-2110 CONNECTOR

DATA acquisition card is used to apply biasing and pulsing to the diode. The National instrument (NI) PCIe-6361 is used for this purpose. It is interfaced through the SHC68-68-EPM matching cable with BNC-2110 connector box. The BNC-2110 connector box collects information from the diode and sends it to the computer for processing. The input voltages of ± 10.0V can be applied through acquisition card and with pulse width from 0.5μs.

4.5.1.5 COMPUTER INTERFACE

All the experimental equipment is connected to the computer with general-purpose interface bus (GPIB) which provides high speed interface between computer and equipment. The equipment is controlled remotely through software.

4.6 SYSTEM SOFTWARE

Laplace DLTS software is developed by a joint project of University of Manchester (Prof. A. R. Peaker) and Institute of Physics Polish Academy of Sciences, Warsaw, Poland (Prof. L. Dobaczewski) under the project *"Copernicus* Project CIPA CT-94-0172 and The Foundation for Polish Science Serial No: C*3.2.041".* The software works in two modes, namely conventional DLTS and Laplace DLTS mode. The detail about both of the software option will be discussed below.

4.6.1 CONVENTIONAL DLTS MEASUREMENT MODE

In conventional DLTS the temperature is set between start point and end point with increasing steps (2K/minutes). It has basically three different operating modes, namely Multi-rate window, trapview and exponential fitting. All these modes work on the concept of rate window and are discussed below.

In "MULTIRATE WINDOW" mode one can scan the samples with nine different rate windows. Each rate window has different t_1 and t_2, so nine signals are generated with peak maximum at nine different temperatures. The rate windows are 5 s^{-1}, 10 s^{-1}, 20 s^{-1}, 50 s^{-1}, 100 s^{-1}, 200 s^{-1}, 500 s^{-1}, 1000 $s^{-1}$and 2000 s^{-1}.This is the quickest way to get information about defects in the sample.

The "TRAPVIEW" mode works with a pair of 5 different rate windows and there is a choice to select one pair at a time. These 5 pairs of rate windows are (4, 10 s^{-1}), (20, 50 s^{-1}), (80, 200 s^{-1}), (400, 1000 s^{-1}), (2000, 5000 s^{-1}).

The "EXPONENTIAL FITTING" works with only one rate window. However, in this mode there is a choice to select either rate window mode or lock-in mode. The lock-in has better resolution but it suffers from a poor signal to noise ratio. In the EXPONENTIAL FITTING mode one can view the Arrhenius plot to estimate defects activation energies and capture cross-section.

In all three operating modes the reverse bias, forward bias, pulse 1, pulse 2, duration of pulses and temperature interval of the experiment can be set remotely.

4.6.2 LAPLACE TRANSIENT PROCESSING MODE

The Laplace DLTS mode is used to increase S/N ratio. The measurements are performed at fixed temperatures. Three different algorithms are applied to generate Laplace DLTS peaks as discussed in section 4.3.

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CHAPTER 5

EXPERIMENTAL DETAILS

This chapter describes the growth details of the samples used in this study, and discusses briefly the experimental procedures, namely, I-V, C-V, C-F, G-F, conventional DLTS and Laplace DLTS employed to investigate their electrical properties.

5.1 SAMPLES USED IN THIS STUDY

The main focus of this thesis is to investigate the electrical active defects present in Interfacial Misfit (IMF) Molecular Beam Epitaxy grown devices, and their role in the transport mechanism. Two different types of materials are studied, namely, as-grown and thermally annealed IMF GaSb/GaAs, and InGaAsSb grown on IMF GaSb/GaAs. The IMF GaSb/GaAs samples consisted of two different structures, namely, uncompensated (IMF without δ-doping) and compensated (after δ-doping with Te-atoms at IMF). The details of the samples are given below.

5.1.1 INTERFACIAL MISFIT GaSb/GaAs WITH MISFIT AT THE INTERFACE

The samples were grown using the same procedure as reported in references [1, 2]. Briefly, the samples are grown by molecular beam epitaxy (MBE) on (100) GaAs substrates. After oxide removal, the RHEED (Reflection High Energy Electron Diffraction) pattern shows a (2 x 4) reconstruction demonstrating a high quality As rich stabilized GaAs surface. This was followed by desorption of As which resulted in a Ga rich surface as confirmed by the (4 x 2) RHEED

reconstruction. The IMF is then created by exposing the surface to Sb atoms. This results in a (2 x 8) reconstruction which confirms the atomic packing instead of tetragonal distortion. The substrate temperature was then reduced and GaSb growth started resulting in a bulk (1 x 3) reconstructed GaSb growth. The layer structure of the devices investigated is shown in Figure 5.1 (a and b). The energy band diagram is calculated by using SilVACO software. The energy band diagram of uncompensated with using without Te at interface is shown Figure 5.1c and compensated samples with 10^{12} cm^{-2} of Te atoms at the interface is shown in Figure 5.1d.

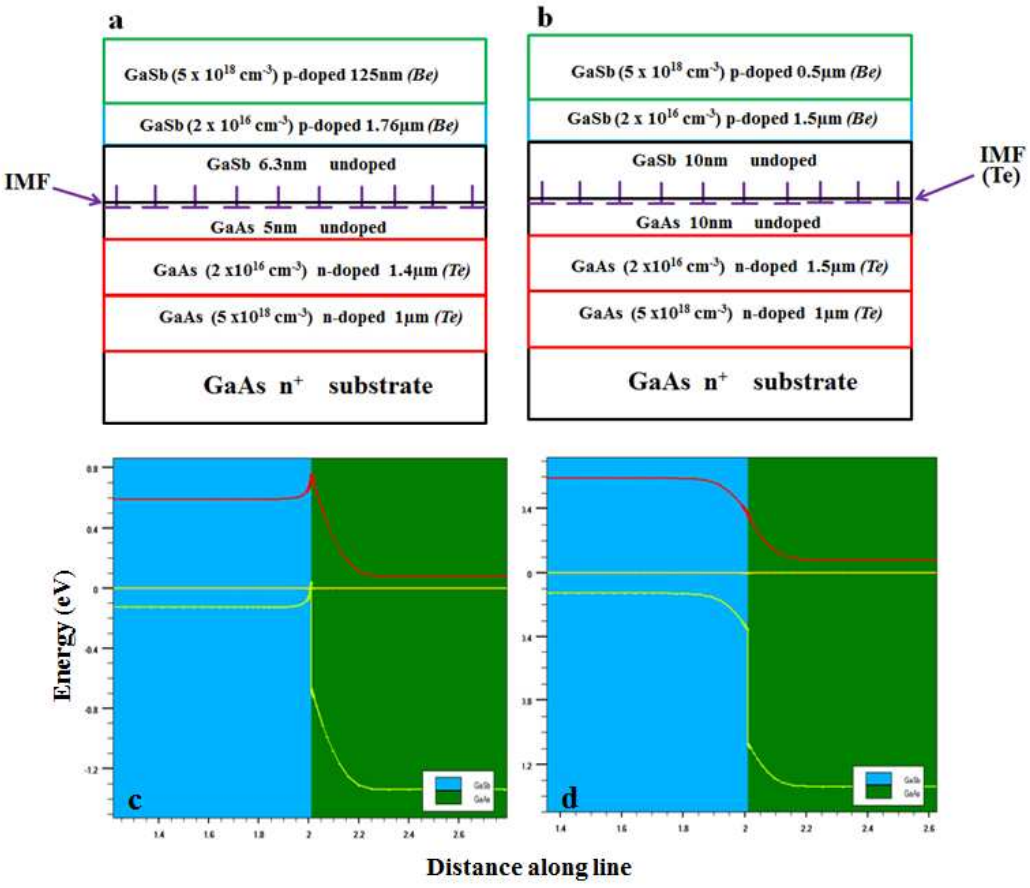

Figure 5.1. Structure of (a) uncompensated (IMF before δ-doping), (b) compensated samples (after δ-doping with Te-atoms at IMF), (c) energy band diagram of uncompensated samples and (d) energy band diagram of Te compensated IMF samples have Te concentration of $10^{12}cm^{-2}$ at the interface.

In these structures Be and Te are used as p and n type dopants, respectively. The doping concentration of the contact layers, i.e. p-GaSb and n-GaAs, for both uncompensated and compensated samples, are 5 x 10^{18} cm^{-3}, whereas for the other layers the doping is 2 x10^{16} cm^{-3}. In uncompensated diodes, the p-n junction is formed by a 1.76 μm thick GaSb and 1.4 μm GaAs layers on either side of the junction, respectively. The compensated GaSb/GaAs devices have an additional sheet of 10^{12} cm^{-2} Te atoms at the interface, and are used to compensate the interface states. In δ-doped IMF diodes, the IMF region is embedded in a 10 nm unintentionally doped GaSb and GaAs regions on the respective sides of the interface. In uncompensated diodes the IMF region is embedded between 6.3 nm GaSb and 5 nm GaAs layers. The difference in intrinsic region of both samples is due to the disruption during growth of uncompensated samples. The segregation of Be and Te dopants into the IMF region can be neglected since the samples were grown at relatively low temperatures (520^{o}C). In addition, the undoped spacer layers on either side of the IMF region will further limit the diffusion of dopants into the IMF. The samples are mounted on TO5 headers with top and bottom ohmic contacts. The samples were processed into circular mesas having 200 μm diameters.

The uncompensated samples were annealed in a rapid thermal annealer (RTA) in a N_2 ambient. The annealing temperatures were 400 ^{o}C, 500 ^{o}C and 600 ^{o}C for 2 minutes.

Similarly, RTA and furnace annealing were performed on Te-compensated samples. The annealing time for RTA samples was about 2 minutes at 400 ^{o}C. The furnace annealed samples were annealed in a N_2-purged glass furnace for

about 4 minutes; it took the sample about 2 minutes to reach 400 ^{o}C from room temperature, and then left at 400 ^{o}C for about 2 minutes.

After post growth RTA and furnace annealing, the ohmic contacts were formed on the top of the p^{+} GaSb layer and the bottom of the n^{+} GaAs substrates. Mesas with 200µm diameter were formed and isolated from each other by using wet chemical etching.

5.1.2 InGaAsSb GROWN ON INTERFACIAL MISFIT GaSb/GaAs

The growth details of the samples are given in the reference 3. In summary, the InGaAsSb samples are grown using solid source MBE with As and Sb valved crackers on n^{+} GaAs substrates. The layer structure, thickness and doping used for these p^{+}-i-n^{+} devices are given in Figure 5.2.

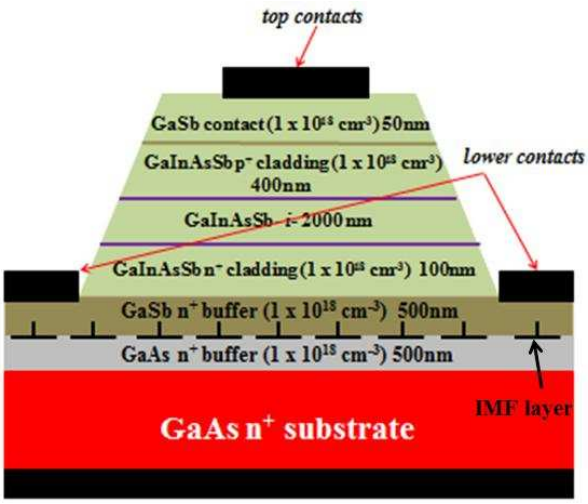

Figure 5.2: Layer structure of InGaAsSb devices grown on Interfacial Misfit GaSb/GaAs.

Starting from the top of the GaAs substrate, Interfacial Misfit GaSb/GaAs is grown using exactly the same procedure as described in section 5.1.1. Following the IMF array, a GaSb buffer layer is grown at a temperature of 500^{o}C. The

temperature was then reduced to 470^{o}C for the growth of the InGaAsSb layers, which consisted of (i) 100nm n^{+} InGaAsSb doped to a level of 1 x 10^{18}cm^{-}3; (ii) a 2000nm thick unintentionally p-doped intrinsic layer of InGaAsSb; 400nm p^{+} InGaAsSb doped layer with a concentration of 1 x 10^{18} cm^{-3}. Finally a top 50nm p^{+} GaSb cap layer is grown.

5.2 MEASUREMENT DETAILS

The details of the measurements carried out in this thesis are given in the following sections.

5.2.1 I-V MEASUREMENTS

The DLTS and Laplace DLTS system used for these studies are based on the measurement of capacitance transients. Therefore, in order to avoid the misinterpretation of the data, the selected devices are those that have a low reverse current in the range of few μA. In order to perform the I-V characteristics a computer controlled Keithley 236 source measure unit is used. The current values are measured with 10 mV increment. Depending on the diode quality steady state reverse biases ranging from -1 to -5V were applied.

5.2.2 C-V MEASUREMENTS

The analysis of the C-V characteristics provides information about many important parameters such as the built-in voltage, background doping concentration, accumulation region, interface states and concentration depth profile. It is worth pointing out here that the concentration of defects depends upon ratio of the DLTS peaks and capacitance (C_{∞}) as explained in Chapter 4.

Therefore, the acquisition of the C-V characteristics of each device is very important, and these are obtained using a computer controlled BOONTON 7200 Capacitance Meter operating at a fixed frequency of 1MHz.

5.2.3 C-F AND G-F MEASUREMENTS

The C-F measurements give very important information about interface states. These interface states do not follow the test signal at high frequency (~ 1MHz). In order to get information about these states C-F is performed at a range of temperatures (20K – 300K) and biasing conditions (reverse and forward bias). Another important parameter that can be determined through C-F measurements is the density of interface states (D_{it}). Similarly, conductance as a function of frequency (G-F) also provides information about interface traps and density of states as function of temperature. The C-F and G-F measurements are performed using an Agilent E4980A LCR meter. The LCR meter, which operates at frequencies between 20Hz and 2MHz, is controlled through Visual Basic program via GPIB/USB interface.

5.2.4 DLTS MEASUREMENTS

The DLTS and Laplace DLTS techniques discussed in Chapter 4, are used in this thesis to investigate the electrical active defects present in the materials. In this section the details of the experimental procedures will be described. The samples were first processed into circular mesas, mounted on 12 pin TO5 headers, and fitted into a holder inside a closed cycle cryodyne refrigerator, model number CCS-450 cryostat capable to cool the samples to a temperature of 10K. DLTS

measurements were then started by ramping the temperature at a rate of 2K/min up to 450K. A train of electrical pulses generated through National instrument Box were applied to the samples. The input (electrical pulses to the samples) and output (transient capacitance) of the samples are taken through Boonton 7200 capacitance meter. The change in capacitance transient is stored in computer in the form of DLTS signal at the desired reverse bias (V_R) and filling pulse (V_P).

5.2.5 LAPLACE DLTS MEASUREMENTS

In order to resolve featureless and broad DLTS peaks, High Resolution Laplace DLTS measurements were carried out. Laplace DLTS is an isothermal DLTS process in which the samples are kept at a constant temperature. The measurements are performed in the range of temperatures where the DLTS peak is detected. The details about this technique are discussed in Chapter 4.

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CHAPTER 6

I-V, C-V AND DLTS OF INTERFACIAL STATES IN "BUFFER-FREE" P-I-N GaSb/GaAs DEVICES

This chapter describes the I-V, C-V, DLTS and Laplace DLTS measurements performed on uncompensated and Te-compensated GaSb/GaAs p-i-n samples. A detailed analysis of their electrical properties is discussed. A brief literature survey is also presented.

6.1 INTRODUCTION

GaSb is a direct band gap material with an energy gap of 0.72eV. Due to its narrow band gap, it has potential applications in long wavelength optoelectronic devices [1, 2], solar cells [3] and quantum dots (QDs) memory devices [4]. The research on GaSb material system has increased considerably [5] due to the fact that high quality epilayers can be grown on low-cost GaAs substrates as compared to the native substrate. However, GaSb is not lattice-matched to GaAs and the use of standard epitaxial growth techniques will result in the generation of defects at the interfaces and in the active regions of the devices. The merits of the Interfacial Misfit (IMF) growth technique, which has shown that defect free interfaces can be achieved, will be reviewed.

By using the Interfacial Misfit (IMF) growth mode, the strain between the substrate and epitaxial layer is in principle relieved by the formation of two-dimensional misfit array parallel to the interface between GaAs and GaSb; these

are referred to as 90^o dislocations [6-8]. The strain relief in 90^o misfit is completely along [110] and [$1\bar{1}0$] direction. The well-known threading dislocations in GaSb/GaAs/ are caused by the 60^o misfit dislocations at the interface. These are formed to relieve the strain after the growth of a GaSb layer beyond the critical thickness. The undesirable threading dislocations can thread through the active region of a sample affecting the electrical and optical properties of the device [7].On the other hand, the 90° dislocations, which are confined to the interface and propagate only laterally, are the efficient mechanism to relieve the strain [9]. These 90° IMF dislocations which create interfacial states are made of Ga-dangling bonds localized at the GaSb/GaAs interface. These interfacial states significantly affect various electrical characteristics of devices [10], such as the turn-on voltage and the reverse-bias leakage current [11, 12]. It is therefore important to study their electronic properties. One of the major issues that affect the performance of the devices is the presence of Ga dangling bonds because they trap carriers. It is therefore essential to compensate these unwanted channels. The delta doping technique of the region near the interface between GaAs and GaSb [12] by a suitable dopant atom has been used as an alternative approach to achieve this compensation. For example, it has been shown that the electronic properties of GaSb/GaAs based devices can be improved by using Te atoms [11, 12]. However, in order to understand the influence of the interfacial states on optoelectronic devices such as lasers, detectors, solar cells, it is vital to study the defects present near the IMF-GaSb/GaAs and their interactions with delta doping processes.

In this Chapter electrically active defects in IMF-GaSb/GaAs heterostructures are investigated for the first time by employing DLTS technique, C-V and I-V techniques.

6.2 RESULTS AND DISCUSSIONS

In order to study the electrical properties of IMF and to understand the role of Te compensation, I-V, C-V and DLTS measurements were performed.

6.2.1 I-V MEASUREMENTS

Figure 6.1 represents the I-V characteristics for both uncompensated and Te-compensated samples at room temperature. The inset of Figure 6.1 shows the linear I-V plot, where it can be seen that the turn-on voltage (V_{on}) of both samples is different. Jallipalli et al [11, 12] explained the low value of V_{on} in their compensated samples as due to the compensation of interfacial states by Te atoms. It is worth pointing out that the value of the turn-on voltage can only be considered as qualitative since there are several parasitic current paths which shunt the hetero-barrier and make the I-V characteristics more complicated. Among the most important sources of currents one may cite thermal generation of carrier in the bulk semiconductor or via deep levels at the hetero-interface, tunnelling across the narrow heterojunction barrier and shunt current along the edge of the sample. All these sources will contribute to different extents to the measured current, thereby making it difficult to ascertain the value of the barrier limited current. However, the main contribution of the current is through the interfaces states resulting from the significant lattice mismatch between GaSb and GaAs in this material system. Therefore, the general trend is that the compensated samples exhibit a lower turn-on voltage which is in agreement with the fact (and also as demonstrated throughout this study) that the compensation

process introduces more interface traps than it is supposed to suppress as claimed in the work reported by Jallipalli et .al [11,12]. These interface states increase dramatically the tunnelling current, and thereby reducing the turn-on voltage. In addition to the interface states, the current through the devices may be influenced by the series resistance effect as discussed by P. Chattopadhyay et al [13]. However, in the devices investigated in his work the series resistance plays a minor role since the tunnelling current remained unchanged as demonstrated by recording the I-V characteristics at different temperatures (data will be discussed in Chapter 8). One therefore can conclude that the major contribution to the measured current in the compensated samples is due to the higher interface states.

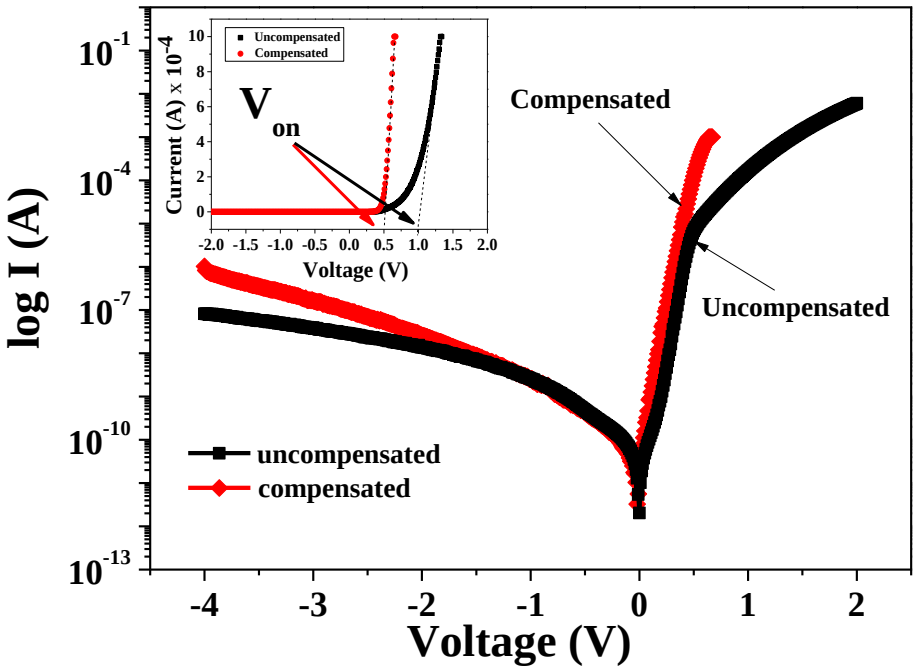

Figure 6.1: Semi-logarithmic plots of dark I-V characteristics of uncompensated and compensated IMF diodes at room temperature with diameter of 200µm. The inset shows linear I-V plot for uncompensated and compensated samples.

6.2.2 C-V MEASUREMENTS

In order to analyse the C-V data and its correlation with interface states and turn-on voltage of the devices, one needs to distinguish between several cases [14, 15] which will be discussed below.

A. IDEAL CASE WITH NO SERIES RESISTANCE AND NO BULK AND INTERFACE TRAPS

In this case the turn-on voltage would be 0V at 0K. At any other temperature above 0K the system has some thermal energy kT (kT at room temperature is 25meV), and the thermionic emission model [16] is used to describe the I-V characteristics of the devices as expressed by:

$$I = I_s \left[exp^{\left(\frac{V}{\eta V_T}\right)} - 1 \right] \qquad (6.1)$$

where η is the ideality factor (supposed to be unity) and V_T = kT/q.

The equivalent circuit of an ideal diode [14] (i.e. with no series resistance and bulk and interface traps) is shown in Figure 6.2.

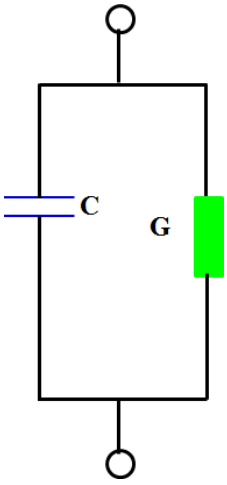

Figure 6.2: The schematic representation of the equivalent circuit of diode with no bulk and interface defects.

Both capacitance (C) and conductance (G) are voltage dependent. In this configuration C is expressed as:

$$C = A(V_B - V_R)^{-1/2} \qquad (6.2)$$

where A contains the electron charge, the dielectric constant and the doping concentration that is assumed to be uniformly distributed in the bulk. C is thus proportional to $(V_B - V_R)^{-1/2}$, where V_B is the built-in voltage and V_R is the reverse bias voltage. It follows that:

The plot of $1/C^2$ versus $(V_B - V_R)$ should be linear and crossing the origin

The plot of C versus $(V_B - V_R)^{-1/2}$ should also be linear and crossing the origin.

In other words, one possibility of checking the quality of the diode (or its deviation from being ideal) is to plot C as a function of $(V_B - V_R)^{-1/2}$ and $1/C^2$ as a function of $(V_B - V_R)$ and check with the above assumptions.

B. REAL CASE WITH SERIES, SEMICONDUCTOR BULK AND CONTACT RESISTANCES, AND NO TRAPS.

For this case the equivalent circuit of a 'real diode (i.e. with series resistance, bulk and contact resistance) is represented in Figure 6.3 [14].

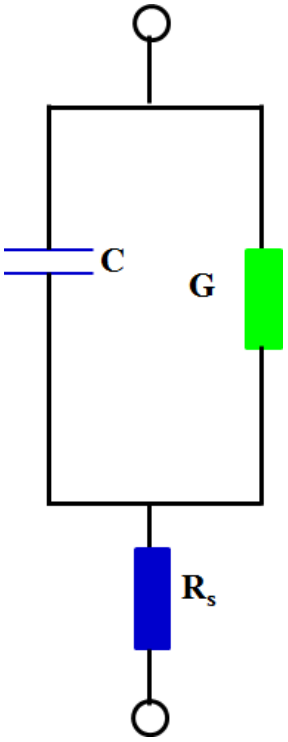

Figure 6.3: The schematic representation of the equivalent circuit of diode with bulk, contact and series resistance but no defect states.

In this case, the total capacitance C' of the diode is given by:

$$C' = \left[\frac{A(V_B - V_R)^{-\frac{1}{2}}}{\left\{1+B[A(V_B - V_R)^{-\frac{1}{2}}]^2\right\}}\right] \qquad (6.3)$$

where B = $2\omega^2R^2$, ω is the frequency of the measuring signal and R_s the series resistance. Rearranging equation 6.3, C' can be expressed as

$$C' = \left[\frac{C}{\{1+2\omega^2R^2C^2\}}\right] \qquad (6.4)$$

where C (given in equation 6.2) is the diode capacitance for the ideal case discussed in above section (6.2.2.1).

$$\frac{1}{C'^2} = \frac{1}{C^2} + B^2C^2 + 2B \qquad (6.5)$$

By using equation (6.5) the plots of $\frac{1}{C'^2}$ versus (V_B - V_R) and C' versus $(V_B - V_A)^{-\frac{1}{2}}$ will not be linear for the following reasons:

The plot of $\frac{1}{C'^2}$ versus (V_B - V_R) will not be linear because of the term B^2C^2 in which C depends on (V_B - V_R). However, for moderate frequency and moderate series resistance the term B^2C^2 can be negligible and thus the plot of $\frac{1}{C'^2}$ versus (V_B - V_R) will be linear but with a positive intercept on the y-axis ($\frac{1}{C'^2}$). Whereas in the ideal case the same plot goes through the origin. This is an important plot which will indicate whether the device has a series resistance or not.

The plot of C′ versus (V_B - V_R)$^{-1/2}$ is also no longer linear and the nonlinearity depends on the frequency and on the value of the series resistance. It tends to approach linearity at very low frequencies ($B = 2\omega^2R^2$) and moderate series resistance. The lower the frequency the smaller the factor B, allowing C versus (V_B - V_R)$^{-1/2}$ to approach linearity.

However, it is worth mentioning that unless the series resistance is abnormally large (several kΩ's) the factor $2\omega^2R_s^2$ is always negligible compared to $1/C^2$. For a diode having an ideal capacitance around 30pF, $\omega^2R_s^2C^2$ is << 1 for R_s << 30kΩ. Therefore, the deviation from linearity of the plot of C versus (V_B - V_R)$^{-1/2}$would be negligible.

C. REAL CASE WITH BULK AND INTERFACE TRAPS

In this case one can neglect the series resistance and consider the interface traps with a density D_{it}. This density is due to a total charge at the interface Q_{it}. The total capacitance is given by:

$$C = \frac{d(Q_{sc}+Q_{it})}{dV} \qquad (6.6)$$

or $$C = C_{sc} + C_{it} \qquad (6.7)$$

where C_{sc} and C_{it} are the capacitances due to space charge region and interface states, respectively. Equation (6.7) indicates that the two capacitances are in parallel. Here C_{sc} represents the capacitance of the ideal diode as given by equation (6.2).

Two subcases have to be distinguished here, D_{it} can indeed be either constant and bias independent or changing with the bias voltage. If Q_{it} is bias independent then $\frac{dQ_{it}}{dV_R} = 0$ and no change on the shape of the C-V would occur. However, if Q_{it} is bias dependent ($\frac{dQ_{it}}{dV_R} \neq 0$), the C-V characteristics will deviate from linearity. In fact to be more precise one should actually express the capacitance as

$$C = \frac{d(Q_{sc}+\beta Q_{it})}{dV} \qquad (6.8)$$

where β is a frequency dependent factor. For ω = 0 and ω=∞ (β = 1 and β = 0), respectively. In other words at very high frequencies the interface states do not respond to the signal and thus their dynamics may be neglected. However, at low frequencies their presence is important. β represents actually the fraction of the interface states that are sensitive to a given frequency. If the interface states are deep then they would not react at high frequencies, while all or most of them would react at low frequencies. Without going too much into the details one can clearly see that [14, 15]:

$$C = C_{sc} + C_{it} = A\,(V_B - V_R)^{-1/2} + C_{it} \qquad (6.9)$$

From equation (6.9), the plot of $1/C^2$ versus $(V_B - V_R)$ or $(V_{on} + V_R)$ is not linear. This will be illustrated in the experimental results section shown below.

The plot of C versus $(V_B - V_R)^{-1/2}$ or $(V_{on} + V_R)$ is perfectly linear crossing the y-axis with an intercept representing C_{it} or C_0. Now it is evident that the intercepts are directly linked to the interface states at the hetero-junction.

By using room temperature C-V measurements it is found that the density of interfacial states in compensated samples is higher than in uncompensated samples. In this work by a careful analysis of the C-V data it is explained that a lower value of V_{on} in the compensated samples is not necessary an evidence of lower interfacial states. The capacitance of an ideal heterojunction is given by [16]:

$$C = A\left(V_{on} + V_R\right)^{-1/2} \qquad (6.10)$$

Where *"V_{on}"* is the diffusion or turn-on voltage, *"V_R"* the applied reverse bias and A is a constant containing the doping concentration on both sides of the heterojunction (one for each material) and the corresponding dielectric constants. This proportionality factor can easily be derived in the case of an ideal heterojunction.

In any type of ideal homojunction or heterojunction system plotting $1/C^2$ as a function of $(V_{on}+V_R)$ or C as a function of $(V_{on}+V_R)^{-1/2}$ is obviously linear. However, there are cases where departure from linearity of either of the types of plotting may provide very instructive information as discussed in section 6.2.2.3. The nonlinearity of $1/C^2$ versus $(V_{on}+V_R)$ of heterojunctions, especially near $(V_{on}+V_R) = 0$, has been discussed at length in the literature [17]. These nonlinearity effects are mainly caused by the interface states which make the equivalent circuit much more complicated than a simple series connection of two equivalent devices (a capacitance in parallel with a conductance), representing each side of the heterojunction. In this work it is shown that the simple parallel

connection of two capacitances model as reported by S. Pandey et al.[15], one representing the total capacitance of the heterojunction (both sides included) and the other representing the interface contribution, fit the experimental data reported in this thesis. In the following analysis I will exploit the trivial but interesting case where the plot of $1/C^2$ as a function of $(V_{on}+V_R)$ is non-linear while the plot of C as a function of $(V_{on}+V_R)^{-1/2}$ is linear allowing the determination of valuable information of the structures investigated in this work.

As explained above, it is important to notice here that relying on equation (6.10), whether C versus $(V_{on}+V_R)^{-1/2}$ or $1/C^2$ versus $(V_{on}+V_R)$ are plotted, one should in principle obtain a linear behaviour for which the intercept is at the origin. This simple analysis has been applied to the data obtained at 300K for both compensated and uncompensated samples. The two plots are shown in Figure 6.4 and Figure 6.5. V_{on} values are extracted from the I-V characteristics at 300K.

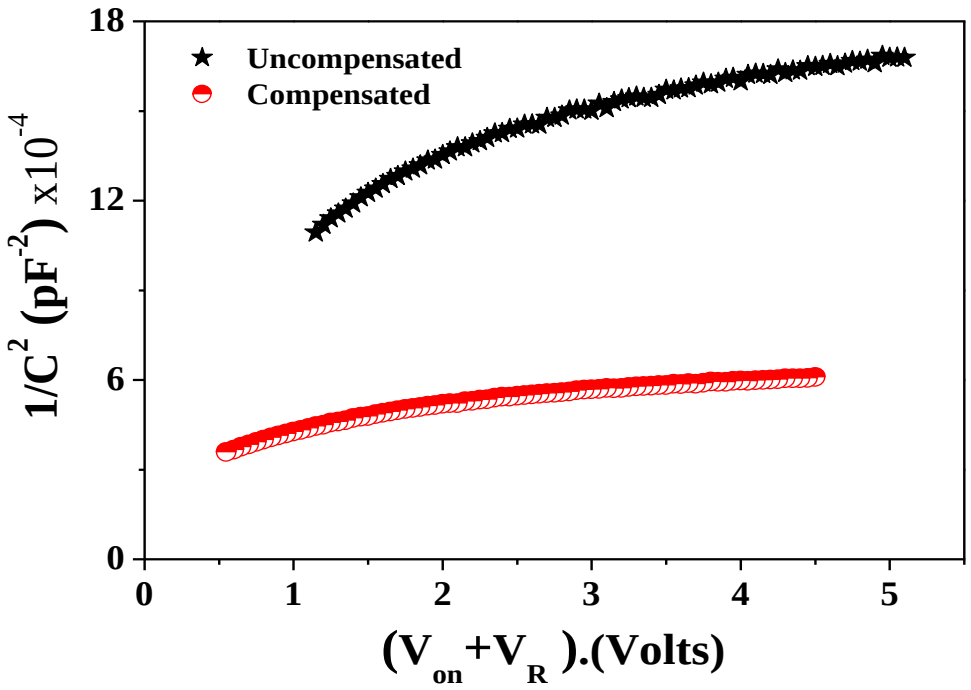

Figure **6**.4: Plot of $1/C^2$ as a function of $(V_{on}+V_R)$. The capacitance was measured at a frequency of 1MHz. Clearly there is no abrupt change of the charge distribution on both sides of the heterojunction.

It is absolutely clear from Figure 6.4 that $1/C^2$ as a function of $(V_{on}+V_R)$ is not linear, whereas plotting C as a function of $(V_{on}+V_R)^{-1/2}$ leads to a perfect straight line as shown in Figure 6.5 but with a non-zero intercept.

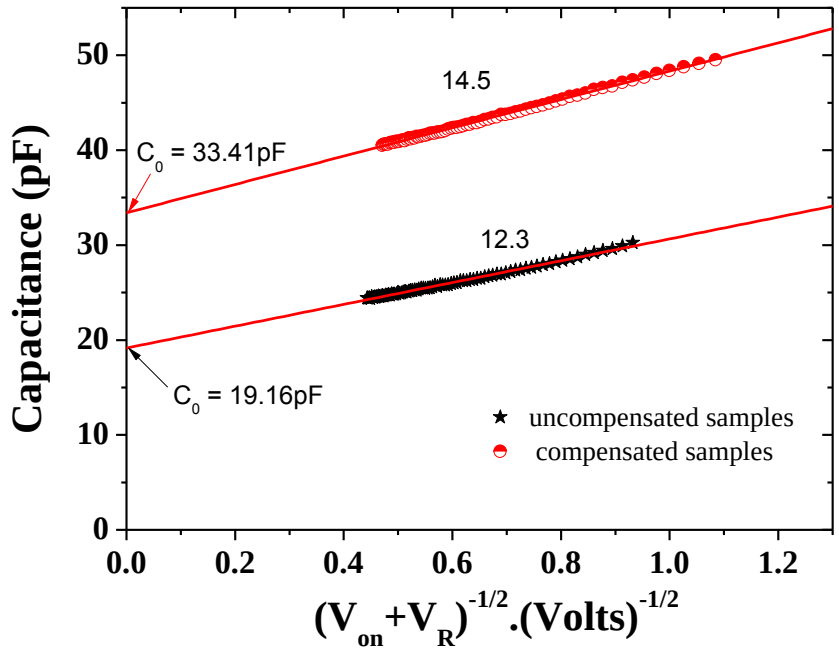

Figure 6.5: Plot of C as a function of $(V_{on}+V_R)^{-1/2}$. The important result here is that the slope (14.5) is slightly increased in the compensated sample compared to uncompensated sample (12.3). The corresponding V_{on} values of each device were extracted from the experimental data shown in Figure 6.1.

The 300K plots shown in Figure 6.4 and Figure 6.5 have similar behaviour for temperatures ranging from 20K to 400K.

To account for the non-zero intercept in Figure 6.5, equation (6.10) must however be modified by adding a constant term C_o. This leads to:

$$C = A\left(V_{on} + V_R\right)^{-1/2} + C_0 \qquad (6.11)$$

The total capacitance of the device is thus equivalent to two separate capacitors in parallel; one due to the depletion region, called also the junction capacitance, and the second due to the interfaces states. It is worth pointing out that the term C_0 is also affected by the value of V_{on} of the compensated and uncompensated samples as demonstrated in Figure 6.5. In order to explain the reason why the intercepts, i.e. values of C_0, are different for both structures one needs to introduce some

extra charges that add up to or subtract from the doping densities in the interface regions between GaSb and GaAs layers. Moreover, as extra charges are expected to affect the band bending, V_{on} must also be affected. Due to the mismatch between the two materials it is natural to assign the observed non-zero intercept to the existence of a sheet layer (δ-layer) at the heterojunction that contains interface states with a total charge Q_{it} and a density D_{it}. These two parameters are linked by the relation:

$$Q_{it} = \pm qD_{it}\left(E_{Fs} - E_0\right) \qquad (6.12)$$

Where the signs ± refers to donors and acceptors, respectively, E_{Fs} is the Fermi level at the interface and E_0 is the so-called neutral level introduced originally by Bardeen [18] to take into account the surface states at the interface between a metal and semiconductor. Avoiding detailed calculations it is easy to show that in the ideal case where there are no interface states, C_0 should be equal to zero and A is given by:

$$A = \left[\frac{q\varepsilon_0 N_a N_d \varepsilon_1 \varepsilon_2}{2\left(N_a\varepsilon_1 + N_d\varepsilon_2\right)}\right]^{1/2} \qquad (6.13)$$

Where N_a and N_d are doping densities in p and n region of the diodes, and ε_1 and ε_2 are dielectric constants of GaSb and GaAs, respectively. If one assumes that the incorporation of Te at the interface does not affect N_a and N_d, or very negligibly, then equation (6.13) can be simplified since in our samples $N_a = N_d = 2x10^{16}$ cm^{-3}. However, according to the C-V results, it can be concluded that while compensating the IMF, Te-delta doping introduces extra charge states breaking down the symmetry of the doping in the compensated samples, i.e. N_a is no longer equal to N_d. It would then be more reasonable to consider that the difference in

slopes in both structures (12.3 in uncompensated and 14.5 in compensated) can be accounted for by the Te modification of N_a and/or N_d.

6.2.3 C-F MEASUREMENTS

Furthermore, in order to confirm the existence of interface states in both samples, capacitances (C) as function of frequency (f) measurements were performed. It is well-known that the higher values of capacitance at low frequencies are attributed to the excess capacitance resulting from the interface states as reported by other workers [19, 20]. Figure 6.6 shows room temperature C-f characteristics for a DC-bias of zero Volt for both samples. It can clearly be seen from Figure 6.6 that the capacitance is significantly higher at low frequencies and drops considerably as the frequency increases. This is seen as an evidence of the presence of interface states in both samples. As long as these interface states are able to follow the variations of the AC test signal at low frequencies, they contribute to the measured capacitance. While at higher frequencies, the interface states are not able to follow the AC test signal (capture-emission rates are much slower) and as a result only the junction capacitance persists. It can also be noted from Figure 6.6, that Te compensated samples have much higher capacitance than uncompensated devices, which further supports our C-V analysis discussed in the previous section.

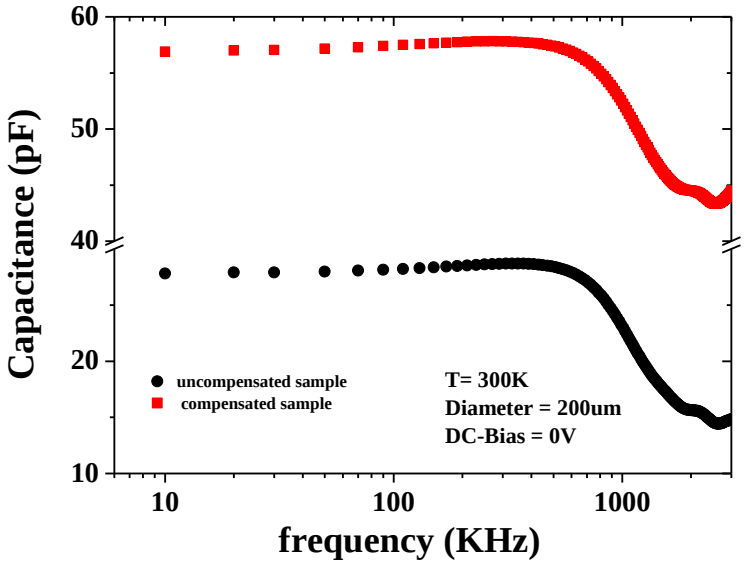

Figure 6.6: Room temperature capacitance versus frequency (f) characteristics of uncompensated and compensated samples.

6.3 DLTS MEASUREMENTS

In order to understand the interaction of IMF and Te, and its influence on the electronic transport mechanism, it is important to study the electrically active defects in both samples. DLTS and Laplace DLTS are powerful techniques to detect traps in the bandgap of semiconductor materials. The details of these techniques are given elsewhere [21, 22].

6.3.1 DLTS MEASUREMENTS ON UNCOMPENSATED GaSb/GaAs

DLTS experiments were performed at different reverse bias conditions. By applying a reverse bias one can control the depletion region where trapping and de-trapping of charge carriers processes occur. This will allow the measurement of the emissions of trapped carriers at a particular region of the device. The DLTS signals from the uncompensated samples, recorded at different reverse biases starting from V_R = - 0.25V (very close to the interface) to V_R = - 4V (away from

the interface) are displayed in Figure 6.7a. The filling pulse was kept constant at V_p = 0V and t_p = 1msec duration for all the measurements. By applying reverse bias of V_R = - 0.25V, the depletion width increase from 0.20 µm to 0.364 µm. Similarly by applying larger reverse bias of V_R = - 4V, the depletion width will extend up to 0.791 µm.

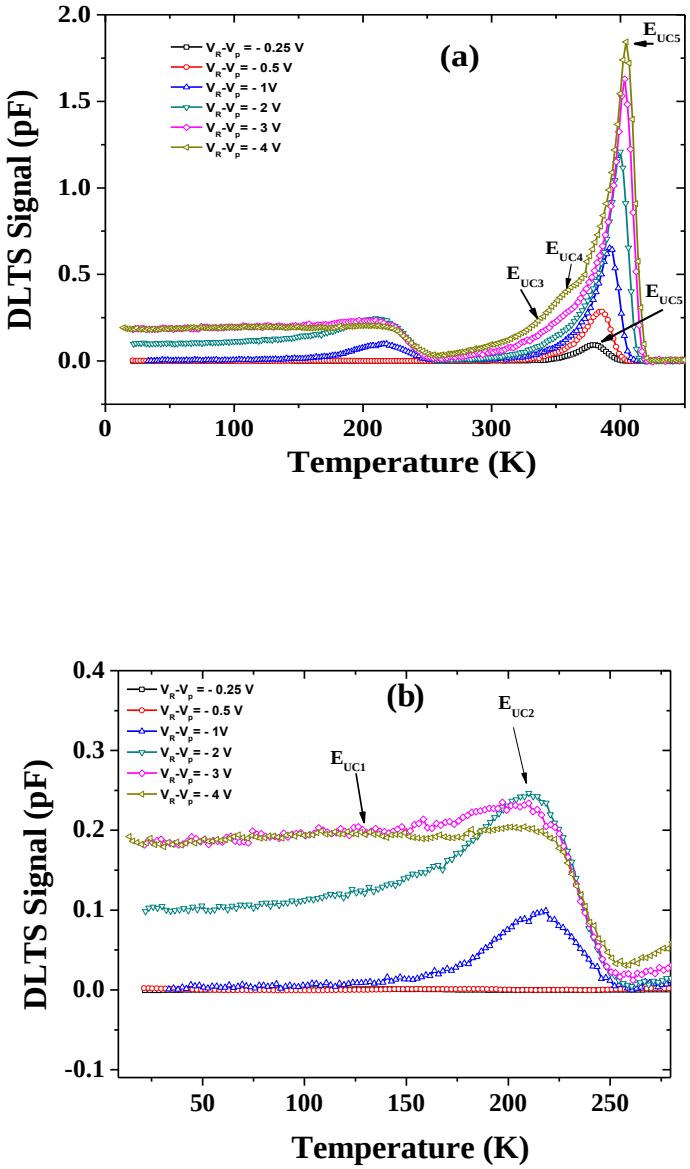

Figure 6.7: Conventional DLTS measurements of (a) uncompensated samples at different reverse biases from V_R = - 0.25V to V_R = -4V. The filling pulse characteristics were: V_p = 0V, t_p = 1msec, and rate window= 200 s^{-1}. For clarity the low temperature peaks are shown in Figure 6.7b.

It can be seen that for a reverse bias V_R = -0.25V (the region probed is near the interface) only one peak at about 383K is detected. The isothermal Laplace DLTS technique in which the emission rate is measured at a constant temperature has been applied to get deeper insight into this well-defined peak. By plotting the temperature versus emission rate one can obtain the energy of the trap. From the Arrhenius plot shown in Figure 6.8a, an activation energy of 0.79eV (defect E_{UC5}) was determined with an apparent capture cross-section of 1.14×10^{-12} cm^2. The Figure 6.8b illustrates the Laplace DLTS peak at temperature of 383K. The full width at half maximum (FWHM) of the single peak detected by conventional DLTS at V_R = -0.25V (see Figure 6.7) is lower than $0.1T_m$ (where T_m is the maximum peak intensity), indicating that a single level is present [23]. This is clearly confirmed by the high resolution Laplace DLTS measurements in the Figure 6.8b.

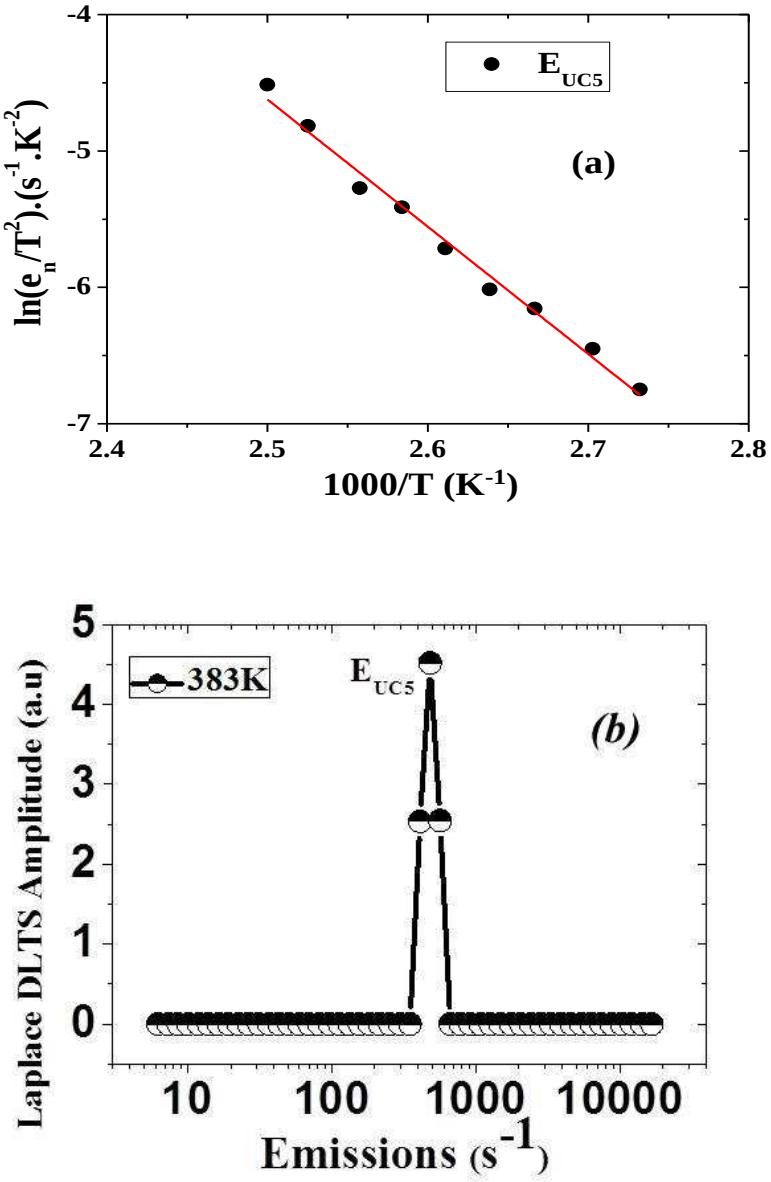

Figure 6.8: (a) Arrhenius plot of uncompensated samples at reverse bias V_R = -0.25V and (b) Laplace DLTS peak at 383K.

Increasing the reverse bias from V_R = -0.25V to V_R = -4V leads to another increasing signal on the low temperature side of the main peak. This observation means that we are not necessarily probing a single state as will be demonstrated below. Above V_R = -1V another peak starts appearing at a temperature of ~217K (for clarity this additional DLTS peak is shown in Figure 6.7b) and broadens on the left hand side (lower temperature) when the bias is increased further up to V_R

= -4V. This broadening is typical for tunnelling processes through the interface between the two materials, namely GaAs and GaSb that have different band gaps. As the band bending increases with applied bias, the thickness of the triangular barrier reduces accordingly allowing the carriers trapped at or close to the interface to escape easily by tunnelling [24].

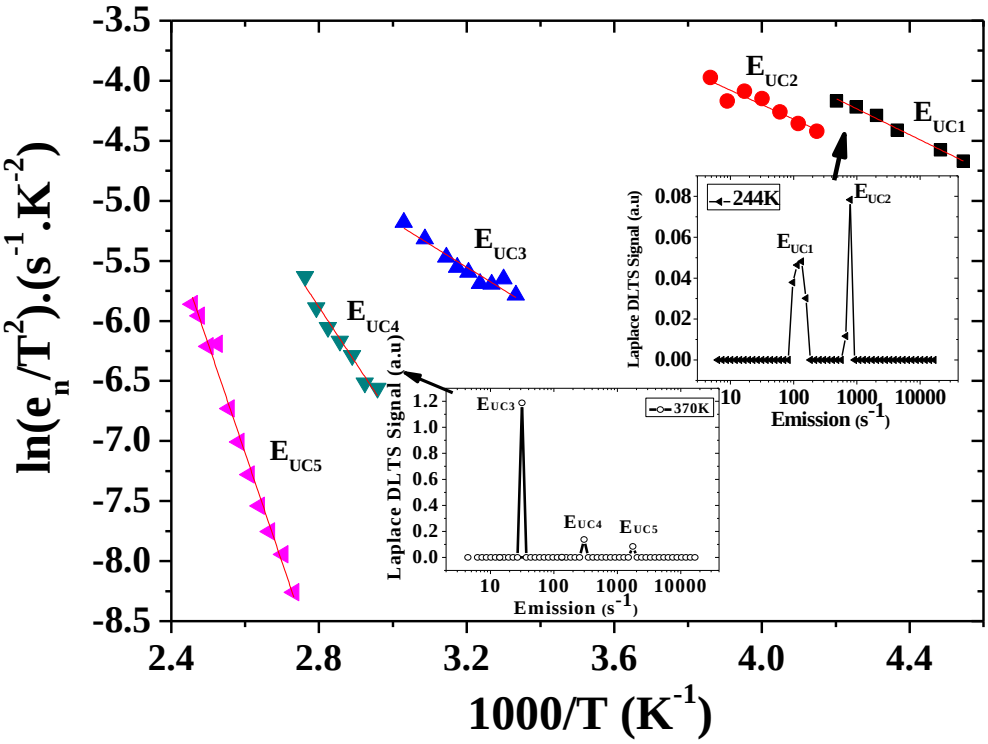

Figure 6.9: Arrhenius plot of uncompensated sample at reverse bias V_R = -4V. The red line represents the linear fit to the data. The inset shows that the main DLTS peak observed for V_R= -0.25V (as shown in Figure 6.7b) splits in three clear peaks as detected by the high resolution Laplace DLTS.

On the other hand, the peak that was very well resolved at the low reverse bias of -0.25V becomes somehow distorted when the bias increases up to -4V suggesting that more than one level exist (Figure 6.7a). To elucidate this further, the Laplace DLTS was done at reverse bias of V_R= -4V and it can be clearly seen from the

inset of Figure 6.9 that there are three peaks (E_{UC3}, E_{UC4}, E_{UC5}), one of which (E_{UC5}) has exactly the same activation energy and capture cross-section as the one detected at the reverse bias of V_R= -0.25V in the uncompensated samples. On the other hand, for the peak that appears at 217K (large "plateau" at low temperatures for higher reverse bias values) in uncompensated samples, the Laplace DLTS reveals two closely spaced peaks (E_{UC1}, E_{UC2}). As shown in Figure 6.9, more defects are detected in the uncompensated samples for a larger reverse bias of V_R= -4.V.

6.3.2 THEORY ABOUT EL2 DEFECT

Native defects are primarily concerned with vacancies, interstitials and antisite defects. If one assumes that in GaAs the majority of gallium vacancies (V_{Ga}) recombine with gallium interstitials (Ga_i) through the Frenkel mechanism, only a small number of remaining V_{Ga} react with arsenic interstitials (As_i) to form As_{Ga} antisites, referred to as EL2 [25, 26].

The capture mechanism of interstitials (Ga_i and As_i) at dislocations has been observed to create arsenic vacancies (V_{As}) and gallium vacancies (V_{Ga}) [26-28]. When As_i are available the following reaction will occur that involve dislocations.

$$\text{Dislocation} + As_i \rightarrow \text{dislocation climb} + V_{Ga}$$

$$V_{Ga} + As_i \rightarrow As_{Ga}$$

Similarly, when gallium vacancies (V_{Ga}) are available the reaction will be

$$\text{Dislocation} + V_{Ga} \rightarrow \text{dislocation climb} + As_i$$

$$V_{Ga} + As_i \rightarrow As_{Ga}$$

The LDLTS results indicate that E_{UC5} for V_R = -0.25 and E_{UC5} for V_R = -4V have the same origin. The associated peak is well identified in the literature [25] with its known energy and capture cross-section. In uncompensated samples it could originate from the GaAs layers and can thus be assigned to the well-known electron trap EL2 in GaAs [25].

The incorporation of Te at the interface between GaSb and GaAs could favour the formation of complexes involving vacancies, antisites and interstitials. According to the literature [29], the self-diffusion in GaSb occurs through the following reaction:

$$Ga_{Ga}V_{Sb} \rightarrow V_{Ga}Ga_{Sb}$$

V_{Sb} being unstable, the pair $Ga_{Ga}V_{Sb}$ converts into $V_{Ga}Ga_{Sb}$ in which Ga forms an antisite leaving a gallium vacancy behind. When Te is incorporated into GaSb it occupies a V_{Sb} site, forming the complex $V_{Ga}Te_{Sb}$ giving to Te the acceptor character.

If Te acts as a donor then the following reaction will result [26]:

$$Te + V_{As} \rightarrow Te_{As}^{+} + e^{-}$$

According to this assumption, in the compensated samples Te atoms could create a channel of free electrons. The low V_{on} in compensated samples observed in this work and in reference [12] can therefore be explained by this model involving the presence of Te atoms. Te could also react with V_{Ga} to form $Te_{As}V_{Ga}$ complex which act as an acceptor. These complexes which have been detected by using forward bias voltage conditions are not reported here but will be discussed in Chapter 8. It is worth noting that this acceptor level has not been detected in uncompensated samples which do not contain Te. One can conclude from this

analysis that the incorporation of Te creates additional states in the compensated samples. This is further confirmed from C-V and C-f analysis.

6.3.3 DLTS MEASUREMENTS ON Te-COMPENSATED GaSb/GaAs

The DLTS spectra obtained on compensated samples are displayed in Figure 6.10. Clearly new peaks appear as shown in Figure 6.10b. These additional peaks, which were absent in the uncompensated samples, start appearing for a reverse bias of $V_R \geq -0.25V$. Figure 6.11a shows the Arrhenius plots of six peaks obtained by Laplace DLTS in the compensated samples for $V_R = -0.25V$ (region probed is close to the interface). These six new defects (E_{C1}, E_{C2}, E_{C3}, E_{C4}, E_{C5} and E_{C6}) as shown in Figure 6.11b are directly or indirectly related to Te doping since these were not observed in uncompensated samples. The most striking feature in Figure 6.10a is the shape of the peaks in compensated samples (temperature 350K-420K) as compared to those obtained in the uncompensated samples. However, while the peak extends on both sides in the uncompensated devices, when the reverse bias is increased in the compensated structure the peaks enlarge mainly on the left hand side whereas an increasing contribution from hole capture-emission shows up on the right hand side as a negative peak.

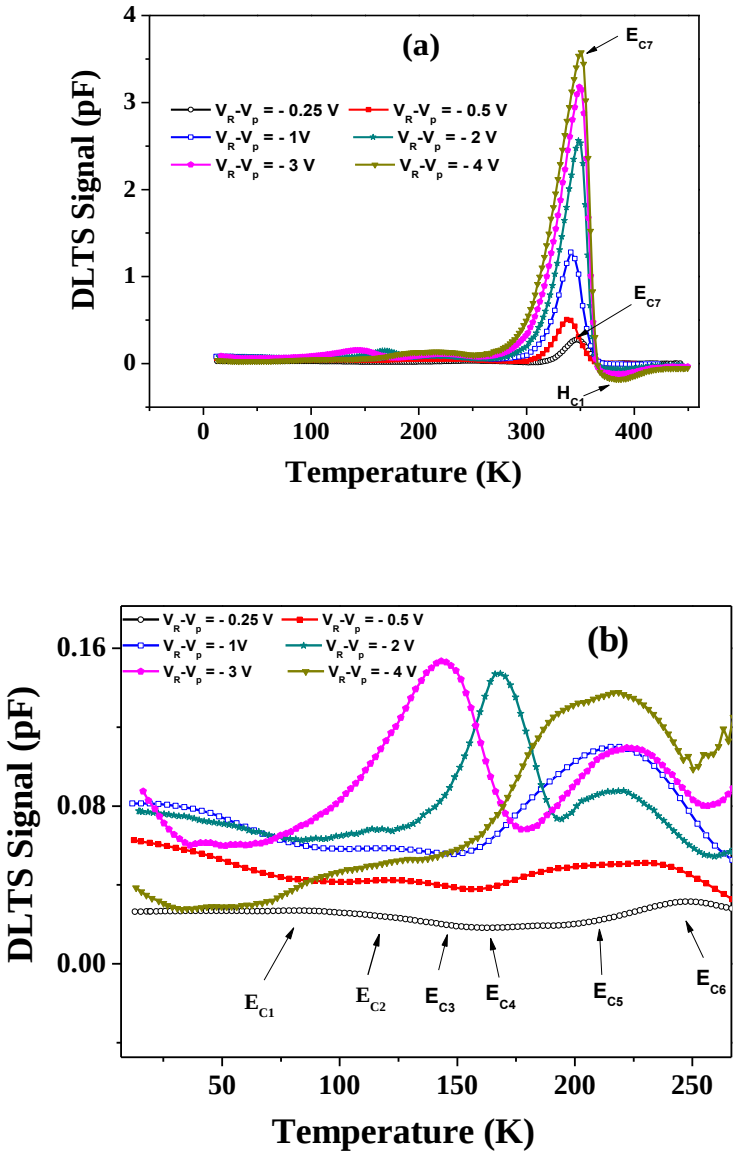

Figure 6.10: (a) DLTS measurements of compensated samples at different reverse biases from V_R = - 0.25V to V_R = -4V. The filling pulse characteristics were: V_p = 0V, t_p = 1msec, and rate window= 200 s^{-1} and (b) For clarity the low temperature peaks are shown.

It can also be noted from Figure 6.10a that at a reverse bias of V_R = -4V, electron and hole peaks are prominent in the temperature range 350 - 420K, particularly under a large reverse bias. However, the hole peak is not detected at small reverse bias of V_R = -0.25V in compensated samples.

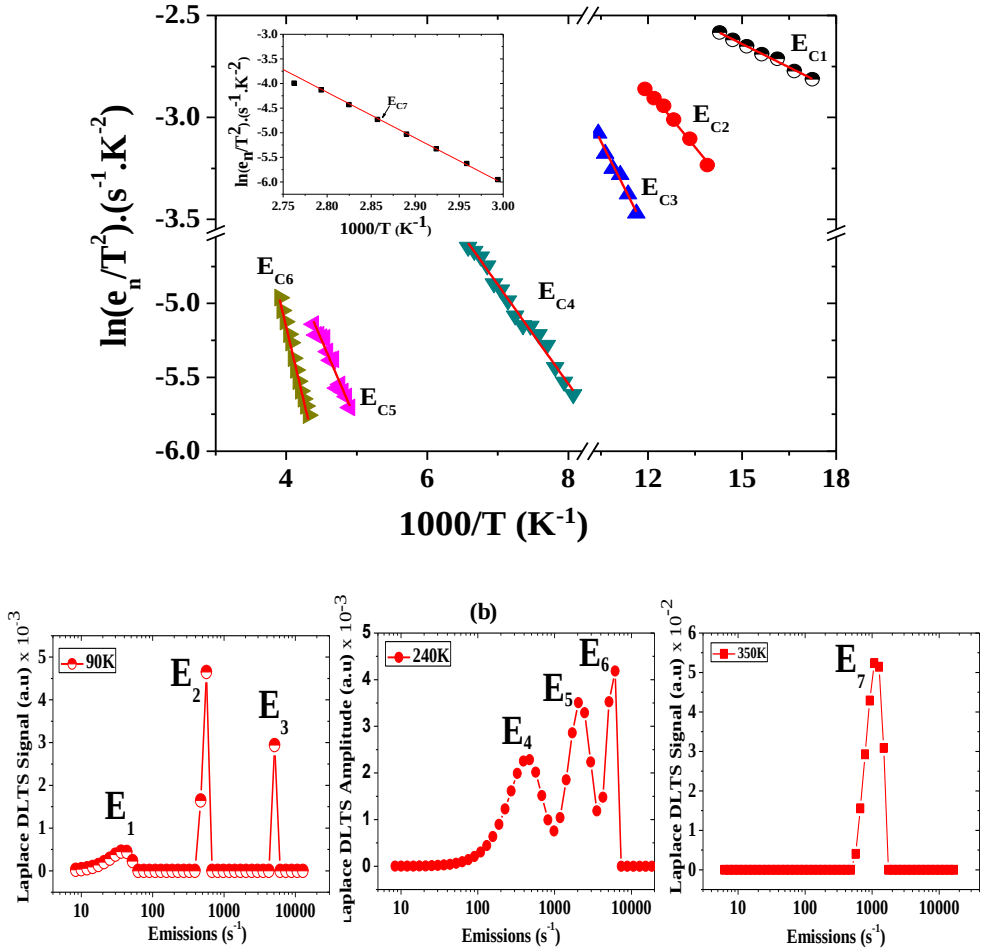

Figure 6.11: (a) Arrhenius plots obtained from Laplace DLTS spectra of compensated samples at reverse bias V_R = -0.25V and (b)Laplace DLTS peaks at different fix temperatures.

The Arrhenius plot for the reverse bias of V_R = -4V is shown in Figure 6.12. It can be seen that the electron peak in the compensated samples at reverse bias of -4V (the activation energy of E_{C7} is shown in Figure 6.12) is the same as the one recorded at the small reverse bias V_R = -0.25V (activation energy of E_{C7} is shown in Figure 6.11a), and has the same origin (EL2) as it was already discussed in the case of the uncompensated samples. On the other hand, the hole peak (H_{C1} shown in Figure 6.10a) with an activation energy (calculated from Arrhenius plot shown in Figure 6.12) of ~ 0.72eV was previously reported in undoped GaSb [30]. It was

attributed to the interdiffusion of Te in undoped GaSb; in our case Te is present at the interface between GaSb and GaAs in compensated samples and might diffuse to the GaSb side.

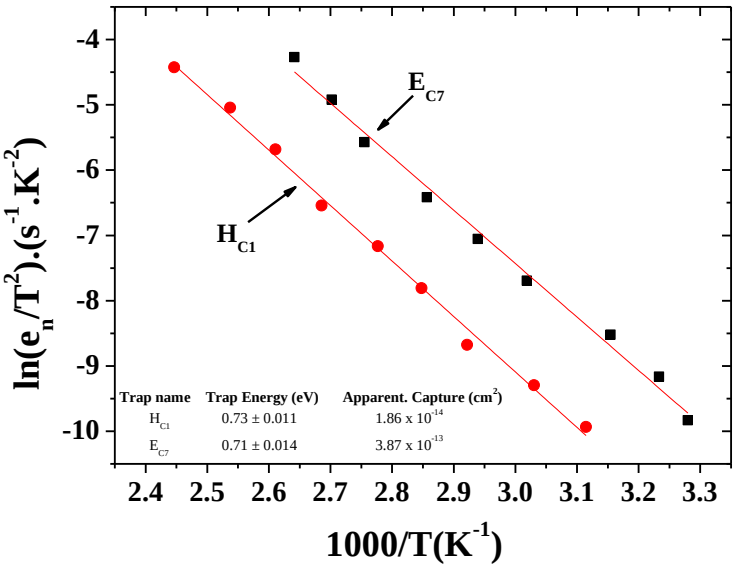

Figure 6.12: Arrhenius plots derived from conventional DLTS for electron and hole traps detected in compensated samples at a reverse bias V_R = -4V.

The activation energies, capture cross-section and defect concentrations are summarised in Table 6.1 for a reverse bias V_R = -0.25V that allows probing the region close to the interface between GaAs and GaSb. As shown from both Figure 6.7a and Figure 6.10a increasing $V_R - V_p$ leads to a very unique behaviour that is not possible to attribute to a single level. In other words one can no longer be assigned to EL2 because the observed signal shifts to higher temperatures and distorts. Laplace DLTS spectra illustrated in Figure 6.9 and Figure 6.11b shows that several deep levels are present in both samples when $V_R - V_p$ is increased. Such a behavior is very likely to be due to interface states. This can easily be explained by the following: increasing the voltage pulse height will increase the energy range from which the carriers emit to the conduction band on one side

(GaAs) and to the valence band on the other side (GaSb). These emission rates are energy-dependent. The situation becomes also complex as one must bear in mind that for interface states the capture cross-section is not only temperature dependent but also energy dependent. This is the reason for the distortion. In other words the traps close to the interface (i.e. interacting with the interface states) have larger capture cross sections than those away from the interface. These various contributions increase the capacitance transient by increasing the components of the various transients and shift the peak position due to the fact that the overall transient is far from the ideal exponential that should be observed for a single trap, no matter how large is the reverse bias. As a consequence, a small voltage pulse $V_R - V_p$ would be preferred for minimizing the shift of the peak and increasing the energy resolution.

In order to correlate the relationship between C-V and DLTS of both compensated and uncompensated samples, one considers the areas below the DLTS signals recorded under the same conditions. This allows the determination of their ratio which matches surprisingly with the ratio of the intercepts in Figure 6.3. Therefore, both the intercepts obtained from the C-V analysis and the deep DLTS peaks are very likely due to the interface states induced by the remaining dislocations generated by the strain energy that is not fully relieved by the 90° IMF dislocations to which one must add the proper role of Te atoms incorporated to compensate those dislocations.

Table 6.1: Summary of trap parameters for both uncompensated and compensated samples at V_R = -0.25V , V_P = 0V and t_p = 1msec.

Sample Name	Trap Name	E_T (eV)	Capture cross-section, σ(cm^2)	Trap Concentration (cm^{-3})
Uncompensated IMF	E_{UC5}	0.79 ± 0.01	1.14×10^{-12}	3.09×10^{14}
Compensated IMF	E_{C1}	0.007 ± 0.001	2.05×10^{-21}	2.49×10^{13}
	E_{C2}	0.016 ± 0.001	4.89×10^{-21}	2.52×10^{13}
	E_{C3}	0.026 ± 0.002	9.89×10^{-21}	2.50×10^{13}
	E_{C4}	0.058 ± 0.004	7.61×10^{-21}	2.28×10^{13}
	E_{C5}	0.096 ± 0.004	7.15×10^{-21}	2.53×10^{13}
	E_{C6}	0.173 ± 0.002	1.58×10^{-19}	2.93×10^{13}
	E_{C7}	0.75 ± 0.01	4.81×10^{-12}	2.51×10^{14}

6.4 CONCLUSION

Uncompensated (without Te at the interface) and compensated (with Te at the interface) MBE grown Interfacial Misfit GaSb/GaAs samples have been investigated. The Current-Voltage characteristics in the reverse bias condition in both samples show that the leakage current is higher in compensated samples than in uncompensated ones for values of voltages greater than -1.5V. Moreover, a lower V_{on} in the compensated samples could be attributed to more defects than in the uncompensated samples. The detailed C-V analysis and C-f measurements also confirm that the incorporation of Te at the interface results in an increase of the interface states. This is also supported by the larger number of traps detected by DLTS in the compensated samples near the interface between GaAs and GaSb. Among these traps, EL2 (E_{uc5} and E_7) is the main midgap defect detected in both

uncompensated and compensated samples. This EL2 trap plays a role near the interface between GaAs and GaSb. Other studies on similar samples have shown that Te plays a role in improving the structural properties of the interface by reducing the dislocation density. However, it is clear from this work that the electrical properties of the compensated samples are not as good as those of the uncompensated devices in terms of the number of electrically active defects.

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CHAPTER 7

EFFECT OF POST GROWTH ANNEALING TREATMENT ON INTERFACIAL MISFIT GaSb/GaAs

This chapter describes the effect of rapid thermal annealing on uncompensated samples, and furnace annealing and rapid thermal annealing on Te compensated samples. The I-V, C-V and DLTS measurements were performed on both uncompensated and Te-compensated samples. The results are analysed by comparing them with those obtained on as-grown samples.

7.1 INTRODUCTION

Antimonide based semiconductors are widely used in electronic and optoelectronic devices due to unique band-structure alignments, small electron effective mass, and high electron mobility [1–3]. Although high quality lattice matched GaSb material is grown on its native substrate, GaAs substrates are most desirable for many applications due to cost and large wafer size. However, the high density of defects due to 7.8% lattice mismatch between GaSb epilayer and GaAs substrate is deleterious to both the electrical and optical properties of the device structures [4, 5] . Researchers have attempted to reduce defects due to lattice mismatch between these two materials [6–8] with the introduction of strained superlattice layers, step, and continuously graded metamorphic buffer layers. These techniques are effective in the reduction of threading dislocations, but they have many drawbacks including the poor thermal conductivity and

generation of non-radiative defects due to the thick buffer layer (>1 µm thickness) which causes a degradation of the devices performance [9].

Recently, many attempts have been made to increase the performance of heterostructure devices [10, 11]. The introduction of Interfacial Misfit array results in the relief of strain at the interface between the lattice-mismatched materials involving two dimensional misfit arrays, referred to as 60^o and 90^o misfit dislocations. Heterostructures without threading dislocations are expected only for a 90^o misfit dislocation. However, if the growth conditions are not optimised either a mixture of 90^o and 60^o or pure 60^o misfit dislocations [10] are created. The 60^o dislocations cause threading dislocations and other native defects near to the interface and away from the interfaces. In the previous Chapter a detailed account of interface states and their role in the transport mechanism was discussed. In this chapter an investigation of the effect of post growth annealing treatment on the defects observed in as-grown devices is presented. The purpose of these annealing studies is to annihilate defects using two annealing processes, namely rapid thermal annealing and heat treatment under inert gas conditions in a tubular furnace. In addition, the annealing process results in better compensation of electrical active defects near to and away from the interfaces. There are two defect mechanisms which can occur upon the annealing procedure, namely, diffusion and disassociation of the traps. The defects could migrate towards the surface or the grain boundaries during the diffusions process. While in the disassociation process traps could split with the increase of thermal energy. The defects can be trapped by other impurities, for example recombination of an interstitial with a vacancy. In the dissociation process the intrinsic defects can break-up into separate defect complexes upon annealing. A brief literature review

on the effects of post growth annealing on the deep levels and its role in the improvements/degradation of devices is given below.

A. Jallipalli et al [12] studied Molecular Beam Epitaxy (MBE) grown GaSb/GaAs structures grown by interfacial misfit (IMF) technique. Electrical measurements on samples with Te compensated IMF and without Te at IMF were carried out. Furthermore, thermal annealing was performed on both samples at 300^{o}C for a short period of time (30sec). According to their findings the annealed samples without Te at IMF showed a reduction of the forward turn-on voltage (V_{on}) and an increase in the reverse current. However, for the Te compensated IMF diodes a small reverse current was observed as compared to the un-annealed samples. They concluded that Te compensation introduced Te interstitials which are the cause of higher leakage current in as-grown samples. When samples are annealed electrons from Te atoms make bonds with Ga atoms at the interface and hence decrease the reverse current in annealed Te IMF samples.

Ville Polojärvi et al [13] performed post-growth annealing on GaSb/GaAs quantum dots (QDs) grown with different V/III ratios (V/III beam-equivalent-pressure ratio used varied between 3 and 7) by using MBE growth technique**.** The decrease in photoluminescence (PL) intensity and redshift is observed by increasing V/III ratios. However, the decrease in FWHM of PL peaks and blue shifts are observed in all samples after the annealing treatment above 800 ^{o}C. They attributed this to the compensation of defects in the QDs, at the interface region as well as in the surrounding GaAs host materials. The temperature dependent PL reveals a reduction in hole thermal activation energy with smaller V/III ratio. These activation energies are further reduced in smaller V/III ratio after annealing.

Sb/As intermixing in MBE grown self-assembled GaSb/GaAs type II quantum dots was studied by rapid thermal annealing [14]. It was observed that in GaSb/GaAs structures (in contrary to InAs/GaAs systems) Sb/As intermixing led to a prominent exponential increase in PL intensity for GaSb QDs with annealing temperature up to 800^{o}C. Three major results were reported in GaSb/GaAs due to the intermixing caused by rapid thermal annealing: (1) pronounced blue shift in energy ;(2) reduction of inhomogeneous broadening; (3) considerably increase in PL peak from GaSb QDs region and from GaAs wetting layers.

S. J. Brown et al [15] investigated the effect of growth temperatures on the interfaces of MBE grown GaSb and GaAs. The surface morphology was studied by using in situ ultra-high vacuum scanning tunneling microscope (STM). A noticeable decrease in the surface roughness was observed by increasing the growth temperature from 400 ^{o}C to 550 ^{o}C. This surface roughness is considered to be directly related to the roughness at the hererostructure interface between GaSb and GaAs.

A.S. Mahajumi et at [16] studied the effect of rapid thermal annealing on MBE grown GaSb/GaAs QDs and Quantum Rings (QRs) by using (PL). They observed enhancement of the PL intensity and blue shift of the PL peak by increasing the annealing temperature from 550 ^{o}C up to 800 ^{o}C. They attributed this enhancement in PL intensity by either the annealing of defects in GaSb/GaAs QDs/QRs or by the intermixing of Sb and As atoms at the interface. This intermixing caused by annealing results in the reduction of strain at the interface between GaSb and GaAs.

The effect of infrared rapid thermal annealing (radiations from halogen lamps are used for annealing) and furnace annealing on electrical properties of n-GaAs made with Si implantation was investigated by H. Kohzu et al [17]. They observed that in n-type GaAs, the carrier concentration profile as determined by capacitance-voltage measurements was different for both types of annealing techniques. In infrared rapid thermal annealing, the carrier concentrations were higher than furnace annealed samples. However, the electron mobilities for rapid thermal annealed samples and furnace annealed samples were very similar. They concluded that in terms of carrier concentration profiles; infrared rapid thermal annealing was superior to furnace annealing due to slightly or negligible implant diffusion. S. Dhar et al [18] performed one step and two steps rapid thermal and furnace annealing on bulk GaAs, and carried out PL and DLTS measurements. According to their findings, one step rapid thermal annealed samples (where the annealing time was very small) show poor mobilities and PL intensities compared to furnace annealed and two step rapid thermal annealed samples. The two steps annealing process involves the same samples annealed at two different times consecutively. In addition, the defect concentrations obtained by DLTS were about two orders of magnitude lower in rapid thermal annealed samples than in furnace annealed samples.

Auret et al [19] reported the well-known EL2 defect in LPE grown GaAs. It is observed that annealing in the temperature range of 400 ^{o}C to 700 ^{o}C did not affect the concentration of EL2. However, they tried two different annealing procedures namely “face to face (where two samples are placed in face to face contact)” and “normal annealing”. They observed that in face to face annealing with temperature of 800 ^{o}C the EL2 concentration was reduced by approximately

two orders of magnitude. However, in normal annealing the decease of the EL2 concentration near to the surface was not as significant as in face to face annealing.

As demonstrated by several studies summarized above, the effect of annealing temperatures and annealing methods have great influence on the properties of materials. It is therefore of paramount importance to understand the annealing effect on the electrical properties of heterostructure devices. The I-V, C-V and DLTS are major tools to investigate electrical performance of as-grown and annealed devices. In the study reported in this chapter, the effects of rapid thermal annealing on uncompensated samples, and different annealing procedures, namely rapid thermal annealing and furnace annealing on Te compensated samples will be discussed. The annealed Te compensated samples, which were provided by our research collaborator from Sheffield University, are furnace and rapid thermal annealed at 400 ^{o}C. Therefore, the measurements are only performed on Te-compensated samples annealed under the above conditions.

7.2 EFFECT OF ANNEALING ON DEFECTS IN UNCOMPENSATED SAMPLES: RESULTS AND DISCUSSIONS

7.2.1 I-V MEASUREMENTS

The uncompensated samples were annealed at different temperatures of 400 ^{o}C, 500 ^{o}C and 600 ^{o}C for 2 minutes using a rapid thermal annealer. Their current voltage characteristics are shown in Figure 7.1a and b. The reverse current is reduced considerably when the samples are annealed. However, the reverse current increases when the annealing temperature increases from 400 ^{o}C to 500 ^{o}C. This increase in the reverse current could be due to an increase in the defects

concentration or to the generation of new defect states. This effect will be further investigated using DLTS experiments as described below.

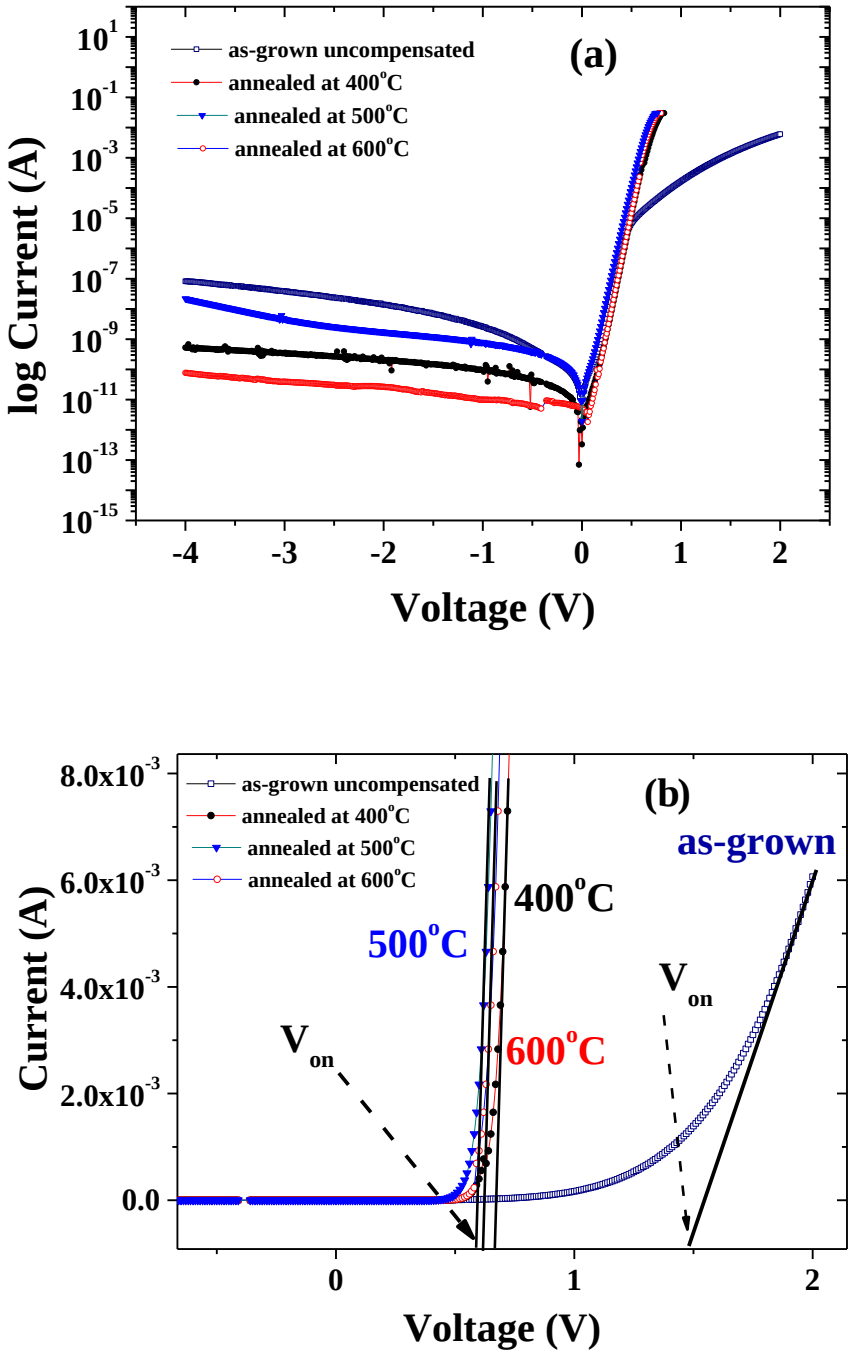


Figure 7.1: (a) Current voltage (I-V) characteristics of as-grown and annealed uncompensated samples. The annealing temperatures are 400 ^{o}C, 500 ^{o}C and 600 ^{o}C and (b) The turn on (V_{on}) values of as-grown, 400 ^{o}C, 500 ^{o}C and 600 ^{o}C annealed samples, respectively.

7.2.2 C-V MEASUREMENTS

The effect of annealing on the interface states can be investigated by using C-V technique as described in Chapter 6. The room temperature C-V characteristics of as-grown and annealed samples are shown in Figure 7.2 as a plot of $1/C^2$ versus $(V_{on} + V_R)$, where V_{on} is the turn on voltage of devices as determined from I-V measurements, and V_R is the applied reverse bias. As can be seen in Fig. 7.2, the as-grown uncompensated samples exhibit a non-linear behaviour, while all the other annealed samples (400 ^oC, 500 ^oC and 600 ^oC) display a linear relationship.

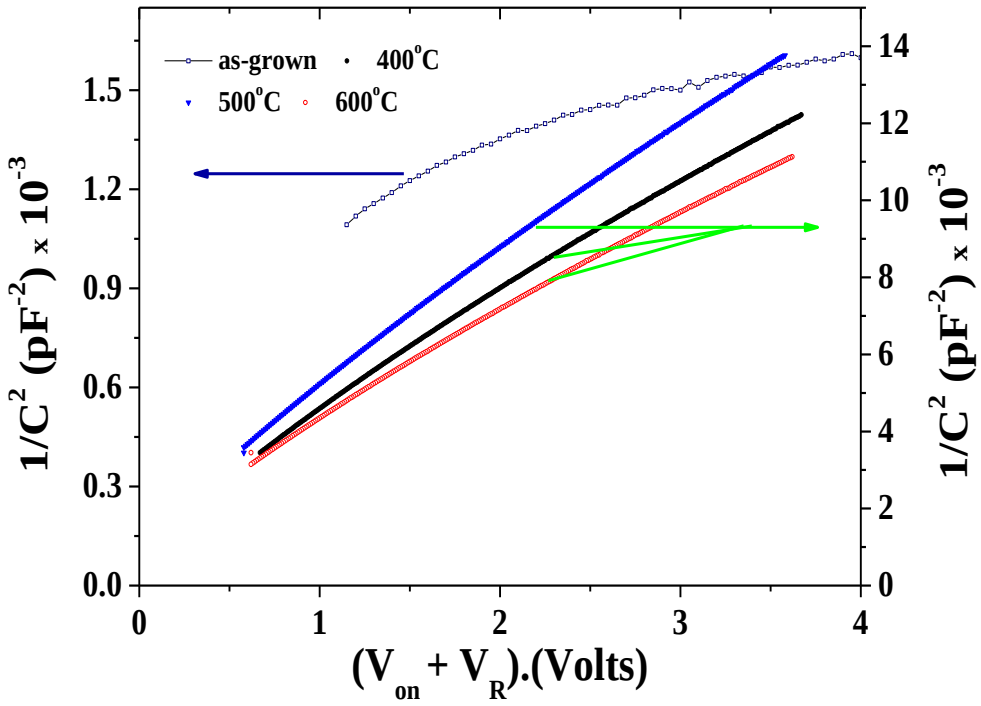


Figure 7.2: $1/C^2$ versus $(V_{on} + V_R)$ plots for as-grown and annealed uncompensated samples.

Figure 7.3 shows plots of capacitance versus $(V_{on} + V_R)^{-1/2}$ from which the interface capacitance can be determined from the intercept. Clearly the annealing process reduces the interface capacitance significantly. If one compares, the C-V results (Figure 7.2 and Figure 7.3) with the I-V characteristics the following conclusions can be drawn: (1) the reverse current is reduced dramatically in annealed uncompensated samples. This could be explained by the reduction of interface states and the compensation of defects as reported by several researchers [13-16] who investigated the effect of annealing on the interfaces of GaAs/GaSb devices. The Intermixing of Sb and As atoms at the interface, due to the effect of thermal annealing, is believed to reduce the interface roughness by decreasing the strain between GaAs/GaSb [13-16]; (2) the C-V analysis, showing a linear behaviour of the plots of capacitance as function of $(V_{on} + V_R)^{-1/2}$ and $1/C^2$ versus $(V_{on} + V_R)$ confirms that the annealed samples have a lower interface capacitance than the as-grown samples.

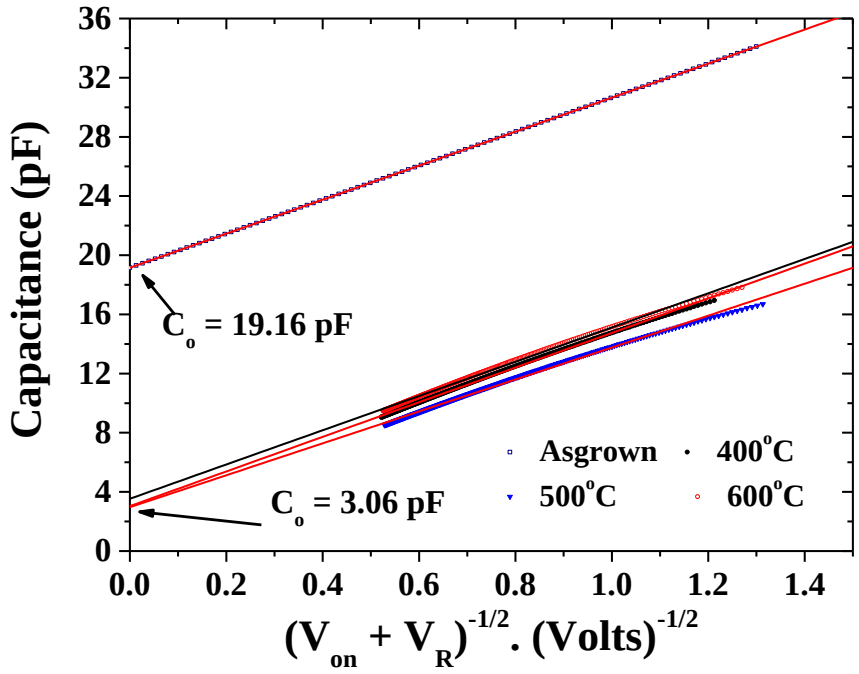


Figure 7.3: Capacitance (C) as function of $(V_{on} + V_R)^{-1/2}$ characteristics of as-grown and annealed uncompensated samples. The as-grown uncompensated samples shave a higher interface capacitance than the annealed samples. The measurements were performed at 300K with a fixed frequency of 1MHz where straight lines are fit to the data points.

7.2.3 C-F MEASUREMENTS

In order to confirm further the role of interface states measurements of capacitance (C) as function of frequency (F) from 500Hz to 2MHz are performed. The C-F characteristics at 0V DC bias are shown in Figure 7.4. It can be seen that the capacitance at low frequencies (~1KHz) is very high for the as-grown samples while the capacitance change is almost negligible from low to high frequencies in all annealed samples (400 ^{o}C, 500 ^{o}C and 600 ^{o}C). These results provide another

evidence of the reduction of interface states after rapid thermal annealing at 400 ^{o}C, 500 ^{o}C and 600 ^{o}C.

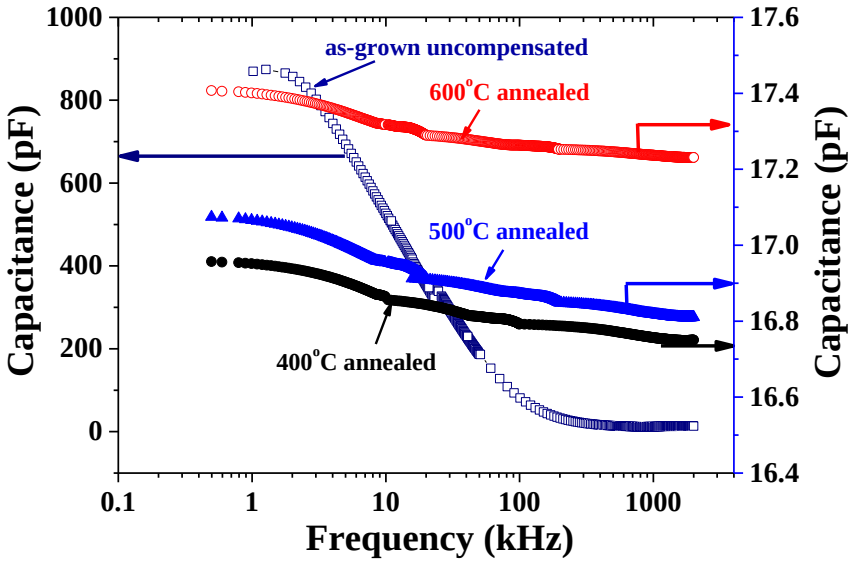


Figure 7.4: Capacitance (C) versus frequency (F) characteristics of as-grown and annealed uncompensated samples. Clearly, the capacitance of the as-grown uncompensated samples is very high at low frequencies and drops significantly at high frequencies.

7.2.4 DLTS MEASUREMENTS

In order to elaborate further on the role of annealing on the electrically active defects in uncompensated samples, DLTS measurements are performed. Figure 7.5 shows the DLTS spectra obtained for the region close to the interface of the p-n devices by using a low reverse bias. The DLTS experiments conditions are V_R = -0.25V, V_P= 0V, and t_p =1msec. The peaks $E_{asgrown}$, E_{A400} and E_{A500} detected in the temperature range (~350 K – 410 K) for as-grown and annealed samples at 400 ^{o}C and 500 ^{o}C are exactly the same for this low bias condition. This peak, identified as EL2 defect, has been discussed in detail in Chapter 6. However, this

DLTS peak is absent in the samples annealed at 600°C. The signal $E1_{A600}$ observed in the 600°C annealed samples in the temperature range (~300 K – 360 K) has activation energy of 0.53 ± 0.01eVas determined from the Arrhenius plot. This trap, which is assigned to the well-known EL3 defect in GaAs, originates from a complex of As interstitial (As_i) and As vacancy (V_{As}) [20]. It was suggested that the EL2 electron trap, which is formed by V_{As} and Arsenic antisite (As_{Ga}), is disassociated into EL3 after ion bombardment of GaAs [21]. The energy that is used to break EL2 by ion bombardment is possibly equivalent to the thermal energy provided in our samples by annealing at 600 °C. All the peaks observed at V_R = -0.25V, V_P= 0V, and t_p =1msec are very symmetric with FWHM <0.1T_m which is the finger print of a single level [22]

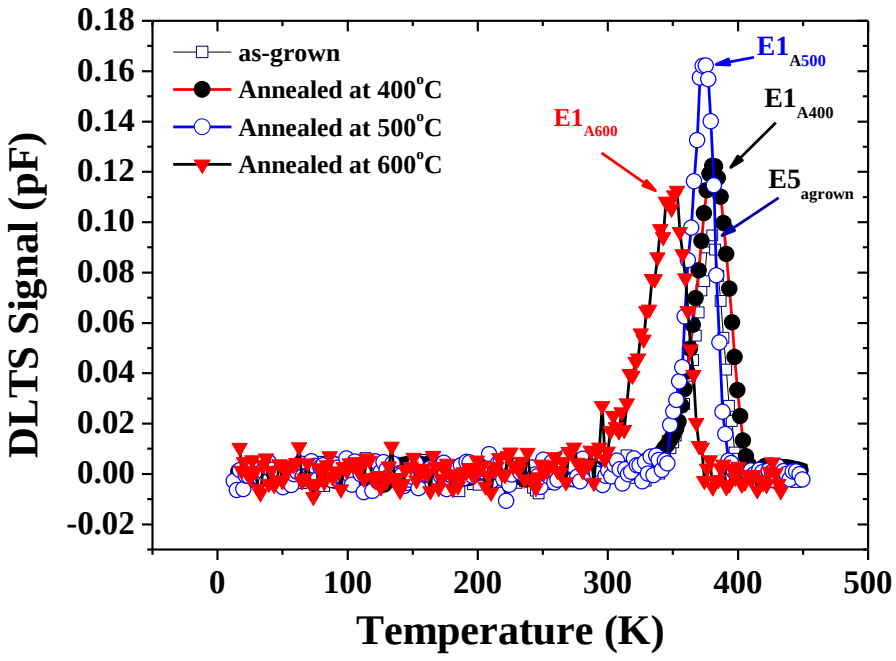


Figure 7.5: DLTS measurements near the interface region of as-grown and annealed uncompensated samples using with a low reverse bias V_R = -0.25V. The filling pulse characteristics were: V_p = 0V, t_p = 1msec, and rate window= 200 s^{-1}.

The activation energies and apparent capture cross sections of as-grown and annealed samples are calculated from Arrhenius plots as shown in Figure 7.6. As discussed previously the activation energies and capture cross-sections are calculated from the slope and intercept, respectively.

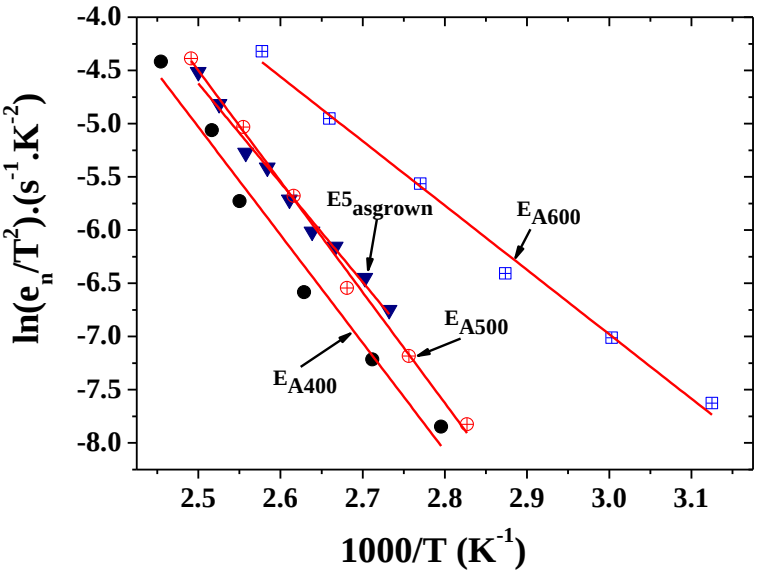


Figure 7.6: Arrhenius plots obtained from conventional DLTS spectra of as-grown and annealed (400^{o}C, 500^{o}C and 600^{o}C) samples for a reverse bias V_R = -0.25V.

Table 7.1summarises the activation energies, capture cross-sections and concentrations of the defects detected in as-grown and annealed uncompensated samples. One can observe from Table 7.1 that the concentration of the defect with energy ~0.8 eV increases as the annealing temperature is raised to 500^{o}C. However, as the annealing temperature is increased to 600 ^{o}C the ~0.8 eV defect is annihilated by dissociation to form EL3 trap with a concentration of 3.66×10^{-14} cm^{-3}. This investigation confirms that the EL2 defect is the dominant trap, which is also contributing to the higher reverse leakage current of the as-grown and annealed samples at 400 ^{o}C and 500 ^{o}C devices. The I-V characteristics illustrated

in Figure 7.1 show that the 600^{o}C annealed samples have the smallest reverse current than all the other samples. This clearly confirms that the reduction of the reverse current in the 600 ^{o}C annealed samples is due to the annihilation of EL2.

Table 7.1: Summary of trap parameters for as-grown and annealed (400^{o}C, 500^{o}C and 600^{o}C) uncompensated samples, for a reverse bias V_R = -0.25V , V_P = 0V and t_p = 1msec.

Sample Name	Trap Name	Activation energy (eV)	Apparent capture cross-section (cm^2)	Trap concentration (cm^{-3})
Uncompensated as-grown	$E5_{asgrown}$	0.79 ± 0.01	1.14×10^{-12}	3.09×10^{14}
Uncompensated 400 ^{o}C annealed	$E1_{A400}$	0.87 ± 0.02	5.66×10^{-12}	4.43×10^{14}
Uncompensated 500 ^{o}C annealed	$E1_{A500}$	0.89 ± 0.01	6.18×10^{-11}	6.17×10^{14}
Uncompensated 600 ^{o}C annealed	$E1_{A600}$	0.53 ± 0.01	1.91×10^{-16}	3.66×10^{14}

In order to probe defects in regions away from the interface and the effect of post-growth annealing, further DLTS experiments with larger reverse biases are carried out. By applying reverse bias of V_R = -4V the depletion width will extend from equilibrium (depletion width of 0.20 µm) to the depletion width of 0.84 µm. Figure 7.7a shows DLTS spectra with reverse bias of V_R = -4V, and filling pulse amplitude and duration of V_P = 0V and t_p = 1msec, respectively.

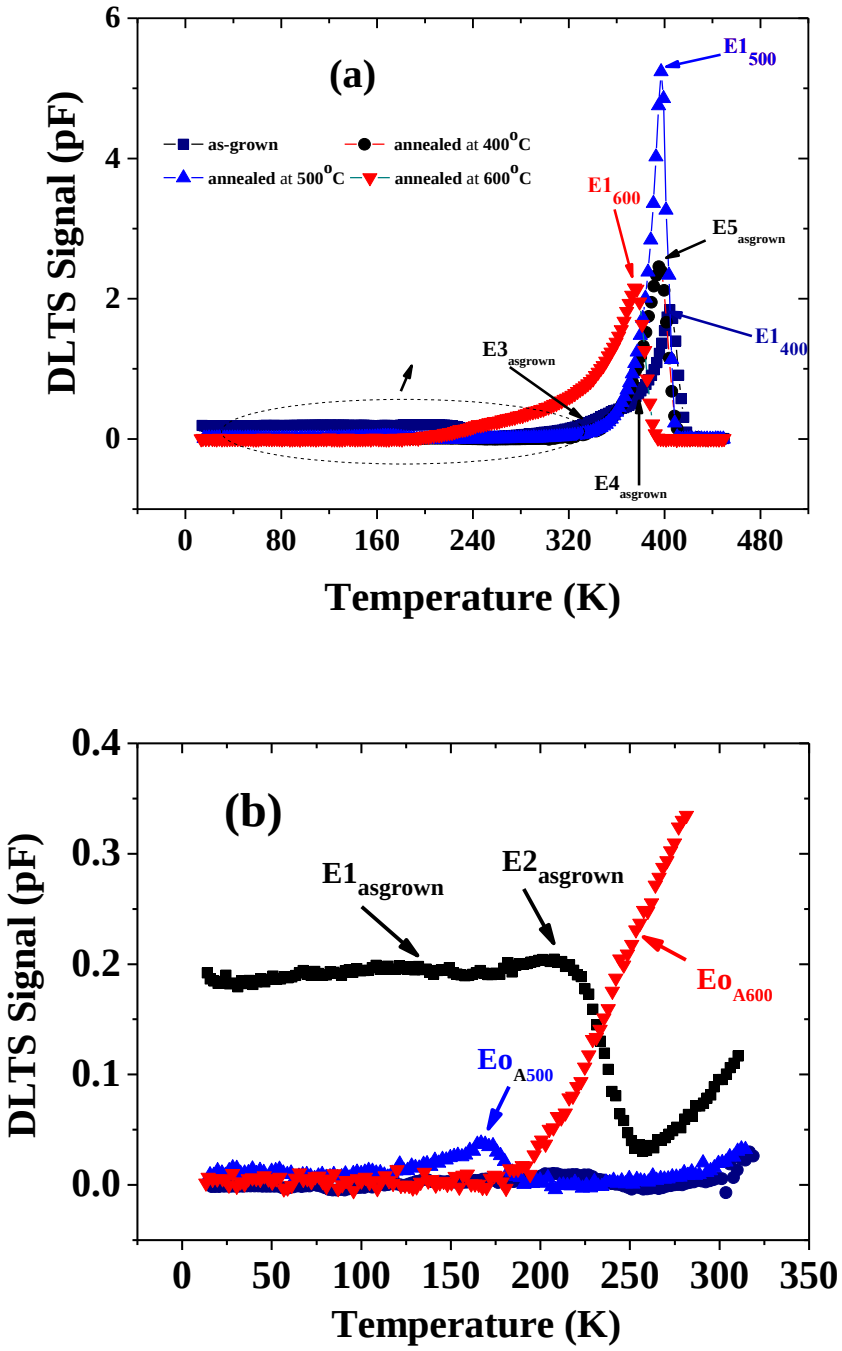


Figure 7.7: (a) DLTS measurements of as-grown and annealed (400°C, 500°C and 600°C) uncompensated samples. A large reverse bias V_R = - 4V is used in order to probe a wider region from the interface (moving depletion from 0.20 µm to 0.84 µm). The filling pulse characteristics were: V_p = 0V, t_p = 1msec, and rate window= 200 s^{-1} and (b) The low temperature peaks are shown for clarity.

It can be seen from Figure 7.7 that in as-grown samples at a larger reverse bias five electron defects are observed. These five defects, namely, $E1_{asgrown}$, $E2_{asgrown}$, $E3_{asgrown}$, $E4_{asgrown}$ and $E5_{asgrown}$ are detected when the depletion width is extended from ~0.20 µm at 0V to 0.84µm at -4V, respectively. However, when the samples are annealed at 400^{o}C only trap $E1_{400}$, also observed at low reverse bias of -0.25V, is detected, and all the other defecst observed in as-grown samples are annihilated. For the higher heat treatment, two traps labelled $E0_{500}$ and $E1_{500,}$ and $E0_{600}$ and $E1_{600}$ are detected in the samples annealed at 500 ^{o}C and 600 ^{o}C, respectively. The traps $E5_{asgrown}$, $E1_{400}$ and $E1_{500}$ common in all samples (except those annealed at 600 ^{o}C) and attributed to EL2 is present both near the interface (for small reverse bias of -0.25V (depletion width extends from 0.20 µm to 0.364 µm)) and away from the interface (for large reverse bias -4V (depletion width extends from 0.20 µm to 0.84 µm). Arrhenius plots of all the defects and their properties detected for a reverse bias V_R = -4V are shown in Figure 7.8 and Table 7.2, respectively.

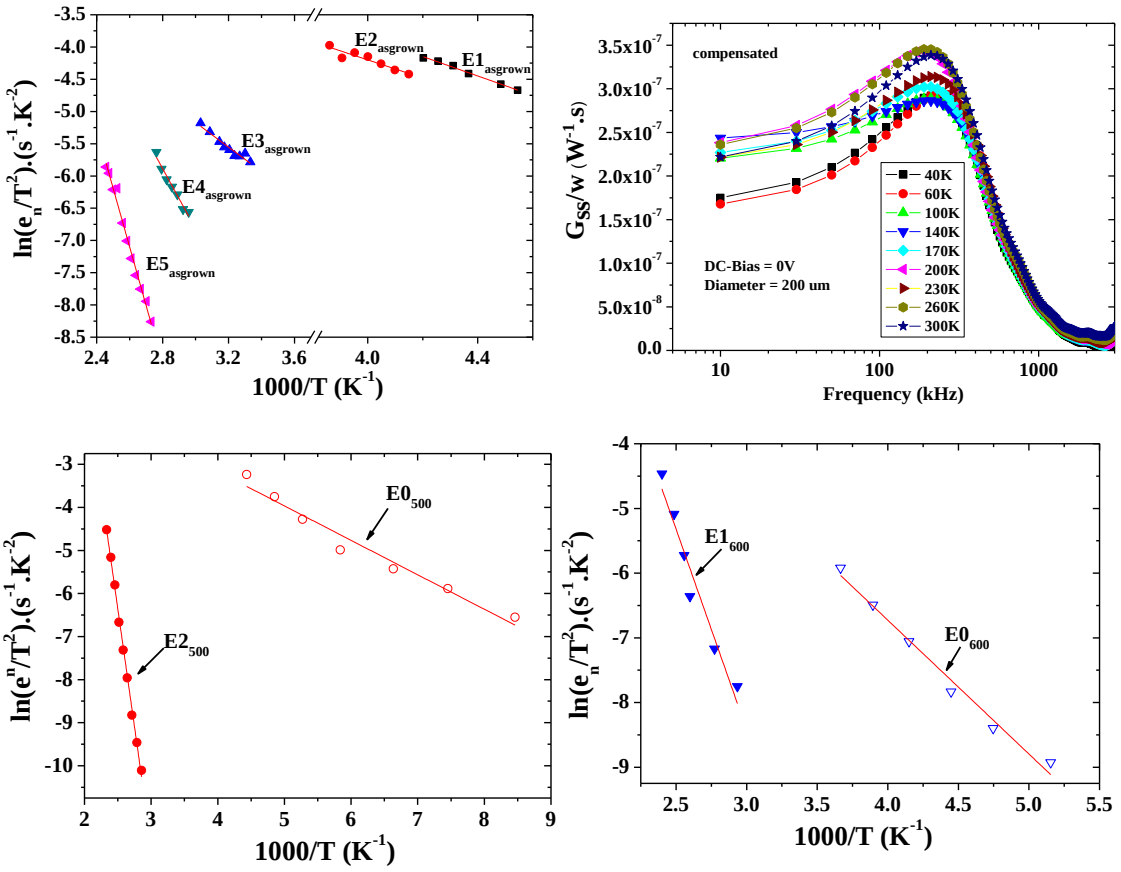


Figure 7.8: Arrhenius plots obtained from conventional DLTS spectra of as-grown and annealed (400°C, 500°C and 600°C) uncompensated samples, A large reverse bias of V_R = -4V is used to probe an extended region from the interface of the p-n devices. Clearly, as-grown samples have a large number of defects, which are reduced using heat treatment process.

Table 7.2: Summary of trap parameters for as-grown, 400°C, 500°C and 600°C annealed samples at reverse bias at V_R = -4V , V_P = 0V and t_p = 1msec.

Sample Name	Trap Name	Activation energy (eV)	Apparent capture cross-section (cm^2)	Trap concentration (cm^{-3})
Uncompensated as-grown	$E1_{Asgrown}$	0.11 ± 0.01	3.76×10^{-20}	5.99×10^{14}
	$E2_{Asgrown}$	0.130 ± 0.001	1.29×10^{-19}	6.20×10^{14}
	$E3_{Asgrown}$	0.17 ± 0.01	2.52×10^{-20}	5.60×10^{14}
	$E4_{Asgrown}$	0.40 ± 0.01	1.90×10^{-17}	1.23×10^{15}
	$E5_{Asgrown}$	0.78 ± 0.01	2.12×10^{-13}	5.63×10^{15}
Uncompensated 400 °C annealed	$E1_{400}$	0.93 ± 0.02	1.10×10^{-11}	1.88×10^{16}
Uncompensated 500 °C annealed	$E0_{500}$	0.07 ± 0.02	9.38×10^{-21}	5.40×10^{14}
	$E1_{500}$	0.92 ± 0.01	1.12×10^{-11}	4.21×10^{16}
Uncompensated 600 °C annealed	$E0_{600}$	0.18 ± 0.01	4.24×10^{-20}	1.54×10^{15}
	$E1_{600}$	0.53 ± 0.03	2.05×10^{-16}	1.52×10^{16}

7.3 EFFECT OF ANNEALING ON DEFECTS IN Te-COMPENSATED SAMPLES

The effect of thermal annealing on Te compensated GaAs/GaSb samples is studied by using two different thermal annealing procedures, namely rapid thermal annealing and furnace annealing. The temperature and duration of annealing used are 400^{o}C and 2 minutes, respectively.

7.3.1 I-V MEASUREMENTS

I-V measurements performed on as-grown and annealed Te compensated samples are shown in Figure 7.9. The reverse current of rapid thermal annealed samples is one and two orders of magnitude lower than as-grown and furnace annealed samples, respectively. However, the 400^{o}C furnace annealed samples exhibit the highest reverse current.

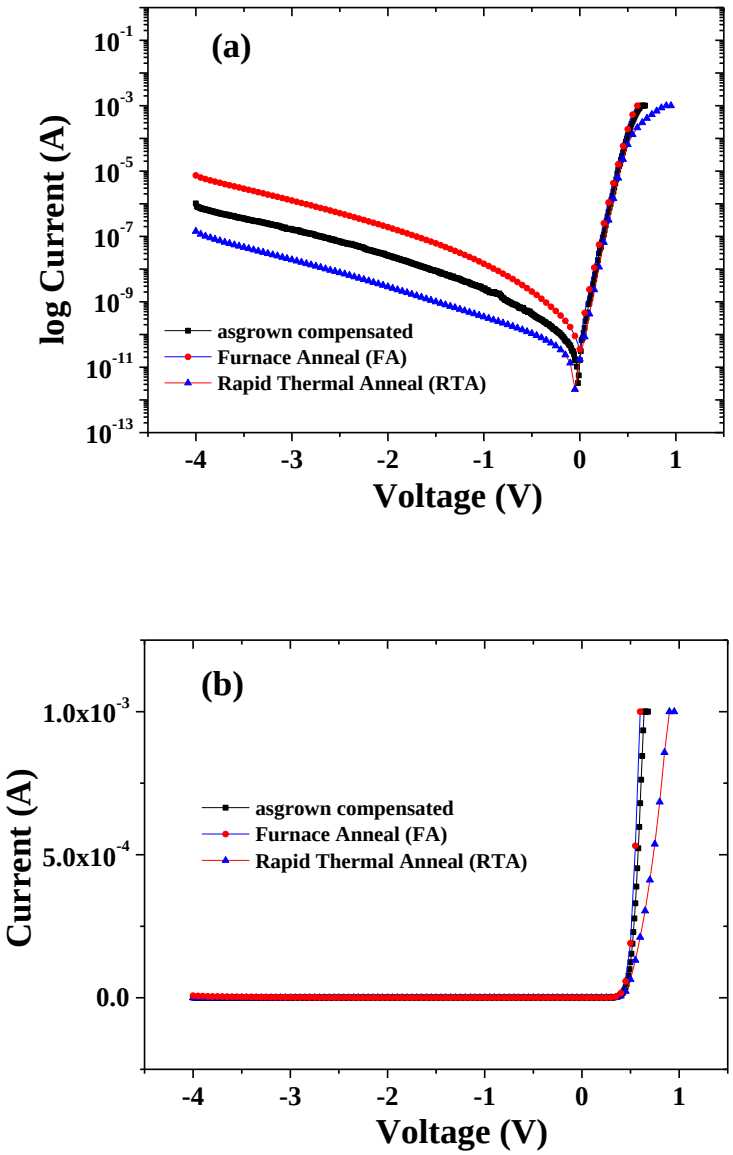


Figure 7.9: (a) I-V characteristics of as-grown and annealed (400 ^{o}C rapid thermal and furnace anneal) Te compensated GaAs/GaSb, samples and (b) shows the turn on (V_{on}) of as-grown and annealed (400 ^{o}C rapid thermal and furnace anneal) devices.

7.3.2 C-V MEASUREMENTS

Figure 7.10 displays plots of $1/C^2$ versus (V_{on} +V_R) of as-grown and rapid thermal and furnace annealed samples which reveal a non-linear behaviour. The interface

state capacitance is extracted from the plot of C versus $(V_{on} + V_R)^{-1/2}$ as shown in Figure 7.11.

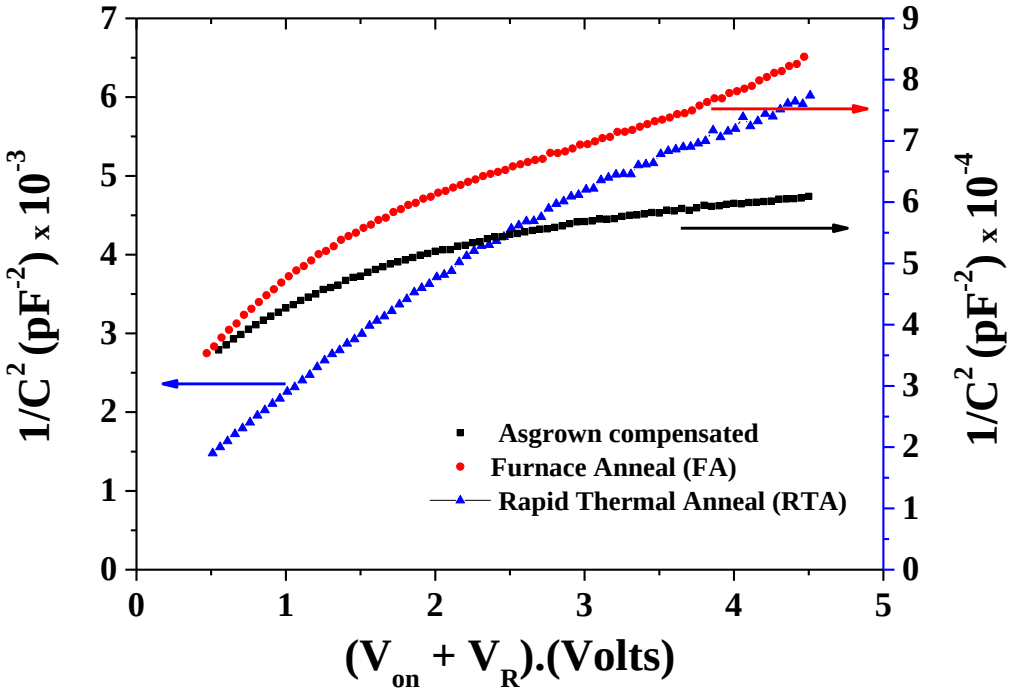


Figure 7.10: Room temperature plots of $1/C^2$ as function of $(V_{on} + V_R)$ for as-grown and annealed (400^{o}C rapid thermal and furnace anneal) Te-compensated samples.

It is worth pointing out that the value of interface states capacitance is lowest in rapid thermal annealed samples. Both I-V and C-V characteristics shown in Figure 7.9a and Figure 7.11, respectively, confirm the effect of annealing on the interface in terms of low reverse leakage current and small interface capacitance of the devices. The rapid thermal annealed samples have the smallest reverse current and interface state capacitance.

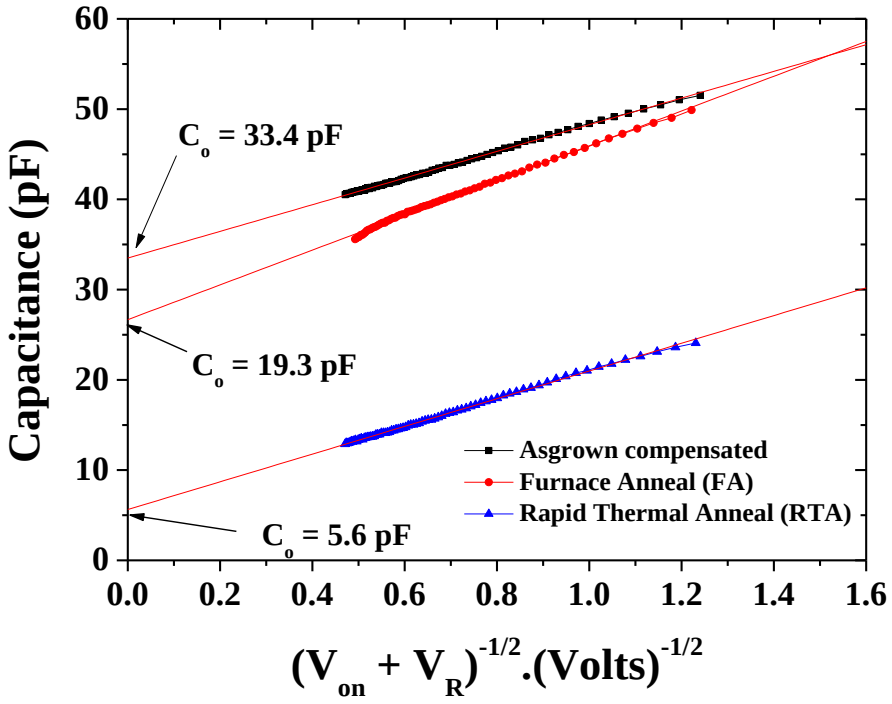


Figure 7.11: plots of Capacitance (C) as function of $(V_{on} + V_R)^{-1/2}$ for as-grown and annealed (400^{o}C rapid thermal and furnace anneal) Te-compensated samples. The rapid thermal annealed samples exhibit the lowest interface state capacitance compared to as-grown and furnace annealed samples.

7.3.3 DLTS MEASUREMENT

The existence of and the effect of annealing (rapid thermal and furnace annealing) on electrically active defects near and away from the interface of Te-compensated GaSb/GaAs samples are investigated by applying small to large reverse biases using DLTS. Figure 7.12a shows the DLTS spectra of as-grown and 400 ^{o}C rapid thermal and furnace annealed samples for a reverse bias of V_R = -0.25V, V_P = 0V and t_p = 1msec. The depletion width extend from 0.20 µm from equilibrium condition (0V) to o.315 µm at a reverse bias of V_R = -0.25V. For clarity Figure 7.12b displays the peaks detected in the temperature range 10-300 K.

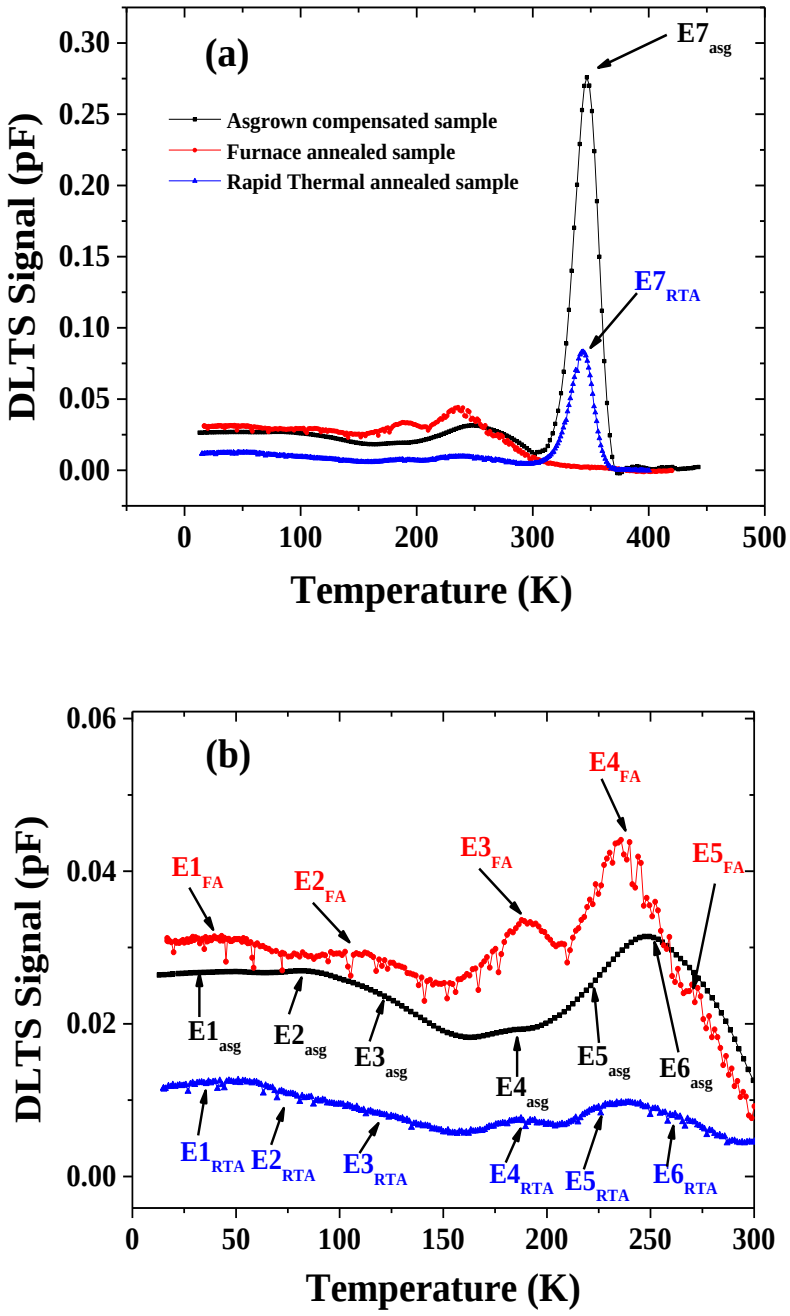


Figure 7.12: DLTS spectra of as-grown and annealed (400^{o}C rapid thermal and furnace anneal) Te compensated samples. The DLTS measurements were taken with a small reverse bias, V_R = -0.25V, in order to probe the region near to the interface (depletion width extend from 0.20 µm to o.315 µm). The filling pulse characteristics were: V_p = 0V, t_p = 1msec, and rate window= 200 s^{-1} and (b) For clarity the peaks detected in the temperature range 10-300 K are shown in Figure b.

Seven electron trap peaks, labelled $E1_{asg}$, $E2_{asg}$, $E3_{asg}$, $E4_{asg}$, $E5_{asg}$, $E6_{asg}$ and $E7_{asg}$ are observed in as-grown samples. A similar number of defects is also detected in rapid thermal annealed samples, labelled here as $E1_{RTA}$, $E2_{RTA}$, $E3_{RTA}$, $E4_{RTA}$, $E5_{RTA}$, $E6_{RTA}$ and $E7_{RTA}$. However, in furnace annealed samples five electron peaks, $E1_{FA}$, $E2_{FA}$, $E3_{FA}$, $E4_{FA}$ and $E5_{FA}$ are detected. The amplitude of the DLTS signal in rapid thermal annealed samples ($E7_{RTA}$) is lower than that of the as-grown samples ($E7_{asg}$). The peaks $E7_{asg}$ and $E7_{RTA}$ are identified as EL2 trap, which is well-known in GaAs. Its concentration is much lower in rapid thermal annealed samples than in the as-grown samples. However, this defect is absent in furnace annealed samples. Figure 7.13a and b shows the Arrhenius plots of as-grown, rapid thermal and furnace annealed samples for a small reverse bias of V_R = -0.25, V_P =0V and tp =1msec. The traps emission rates are extracted from Laplace DLTS. The traps activation, energies capture cross-sections and traps concentrations are summarized in Table 7.3.

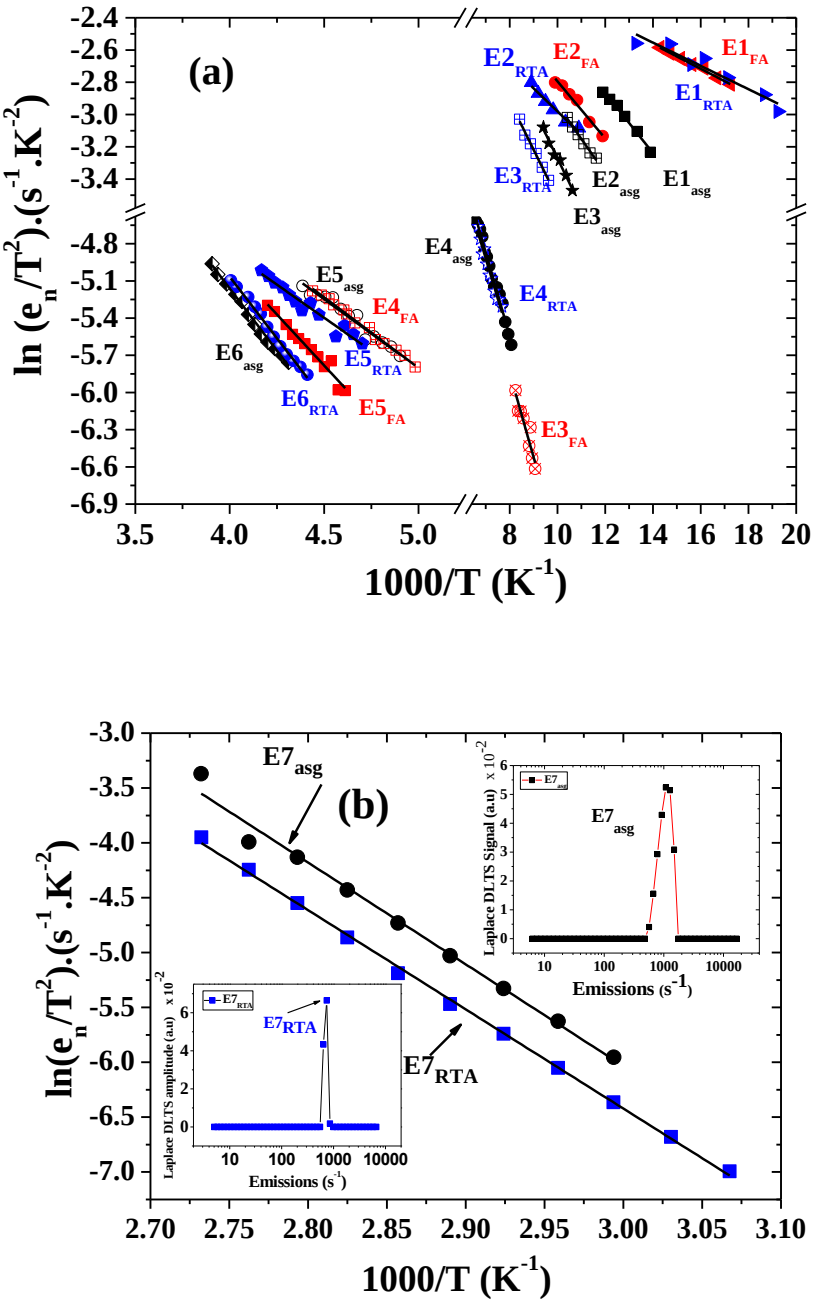


Figure 7.13: Arrhenius plots obtained from Laplace DLTS of as-grown and annealed (400^{o}C rapid thermal and furnace anneal) Te-compensated GaSb/GaAs samples using a small reverse bias of V_R = -0.25V and (b) shows Arrhenius plots of peaks $E7_{asg}$ and $E7_{RTA}$ for as-grown and rapid thermal annealed compensated samples, respectively.

Table 7.3: Trap activation energies, capture cross-sections and trap concentrations of Te-compensated as-grown, furnace annealed and rapid thermal annealed samples at V_R = -0.25V, V_P = 0V, and t_p = 1msec.

Sample ID	Traps	Activation Energy (eV)	Apparent Capture cross-section (cm^{-2})	Trap concentration (cm^{-3})
Compensated as-grown (asg)	$E1_{asg}$	0.007 ± 0.001	2.05×10^{-21}	2.49×10^{13}
	$E2_{asg}$	0.016 ± 0.001	4.89×10^{-21}	2.52×10^{13}
	$E3_{asg}$	0.026 ± 0.002	9.89×10^{-21}	2.50×10^{13}
	$E4_{asg}$	0.058 ± 0.004	7.61×10^{-21}	2.28×10^{13}
	$E5_{asg}$	0.096 ± 0.004	7.15×10^{-21}	2.53×10^{13}
	$E6_{asg}$	0.173 ± 0.002	1.58×10^{-19}	2.93×10^{13}
	$E7_{asg}$	0.75 ± 0.004	4.81×10^{-12}	2.51×10^{14}
Furnace Annealed (FA)	$E1_{FA}$	0.006 ± 0.004	3.17×10^{-21}	1.09×10^{13}
	$E2_{FA}$	0.012 ± 0.002	3.15×10^{-21}	9.87×10^{12}
	$E3_{FA}$	0.052 ± 0.002	2.89×10^{-21}	1.13×10^{13}
	$E4_{FA}$	0.098 ± 0.002	1.34×10^{-20}	1.50×10^{13}
	$E5_{FA}$	0.142 ± 0.004	7.42×10^{-20}	8.56×10^{12}
Rapid Thermal Annealed (RTA)	$E1_{RTA}$	0.007 ± 0.002	3.35×10^{-21}	8.45×10^{11}
	$E2_{RTA}$	0.015 ± 0.002	5.32×10^{-21}	6.38×10^{11}
	$E3_{RTA}$	0.026 ± 0.002	1.19×10^{-19}	5.08×10^{11}
	$E4_{RTA}$	0.055 ± 0.003	9.72×10^{-21}	5.60×10^{11}
	$E5_{RTA}$	0.092 ± 0.004	8.22×10^{-21}	6.54×10^{11}
	$E6_{RTA}$	0.171 ± 0.002	2.57×10^{-19}	5.10×10^{11}
	$E7_{RTA}$	0.78 ± 0.01	1.37×10^{-11}	5.62×10^{12}

DLTS spectra obtained for a larger reverse bias of V_R = -4V, V_P = 0V and t_p =1msec for as-grown, rapid thermal and furnace annealed samples are shown in Figure 7.14. The depletion width extends from 0.20 µm to 0.81 µm from thermal equilibrium (0V) to V_R = -4V. As can be seen from Figure 7.14a the amplitude of all the DLTS peaks increases. This indicates an increase of the concentration of all traps. In particular, the concentration of trap $E7_{asg}$ (EL2 defect) is increased

from 2.51×10^{14} cm^{-3} close to the GaSb/GaAs interface region (V_R = -0.25V (0.315 µm) to 3.36×10^{15} cm^{-3} away from interface region. (V_R = -4V (0.81 µm).

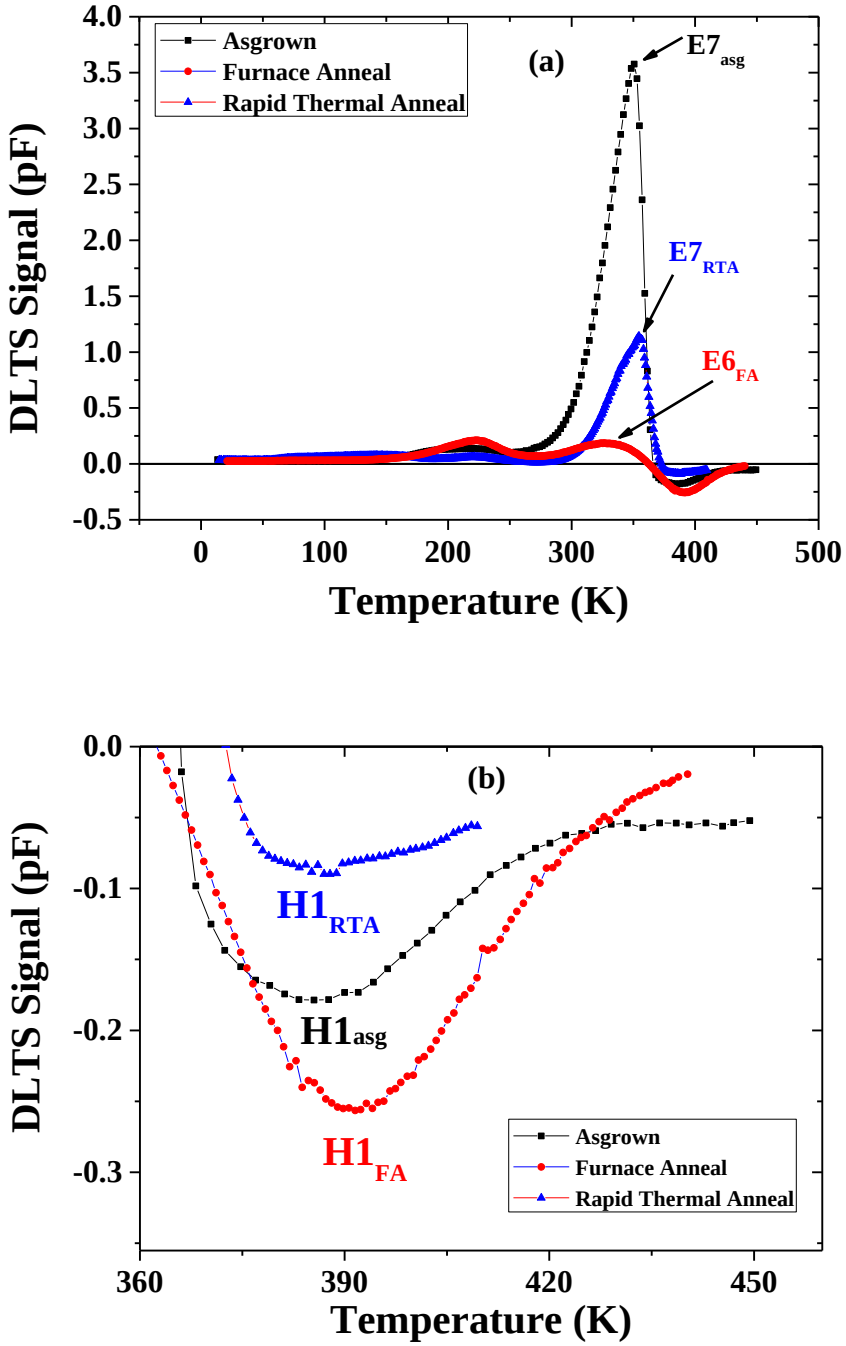


Figure 7.14: DLTS spectra of as-grown and annealed (400^{o}C rapid thermal and furnace anneal) Te-compensated samples. The DLTS spectra shown are taken with a large reverse bias, V_R = - 4V, in order to probe an extended region from the

interface. The filling pulse characteristics were: V_p = 0V, t_p = 1msec, and rate window= 200 $s^{-1}$and (b) Shows hole peaks for as-grown, rapid thermal and furnace annealed samples for the clarity .

However, for rapid thermal annealed devices the concentration of $E7_{RTA}$ (EL2) has increased only by a smaller amount from 5.62×10^{12} cm^{-3} to 7.91×10^{12} cm^{-3}. The concentration increase of EL2 in rapid thermal annealed samples is much lower as compared to as-grown samples. This trap (EL2) which was absent near the GaSb/GaAs interface in furnace annealed samples at smaller reverse bias is detected away from the interface for V_R = -4V with a concentration of 1.96×10^{14} cm^{-3}. It is worth pointing out that new hole trap is detected in as-grown and annealed samples when a larger reverse bias of V_R = -4V is applied as shown in the Figure 7.14b. The activation energy of this hole trap in as-grown , rapid thermal and furnce annealed samples is $H1_{asg}$ = 0.72 eV, $H1_{RTA}$= 0.66 eV and $H1_{FA}$ = 0.68 eV, respectively. The concentration of this defect is similar in all samples. The origin of this hole trap can be related to Te inter-diffusion as observed by E. Kuramochi et al in GaSb samples [23]

Figure 7.15a and b shows the Arrhenius plot of as-grown, and rapid thermal and furnace annealed samples at V_R = -4V. In the following, only the activation energies of the main electron trap (EL2) (Figure 7.15a) and the new hole trap are extracted and discussed (Figure 7.15b). Their properties are summarised in Table 7.4.The other DLTS peaks shown in Figure 7.12b, and summarized in Table 7.3, in Te-compensated samples in the temperature range of ~ 50K-300K are similar to those observed near the interface (V_R= -0.25V).

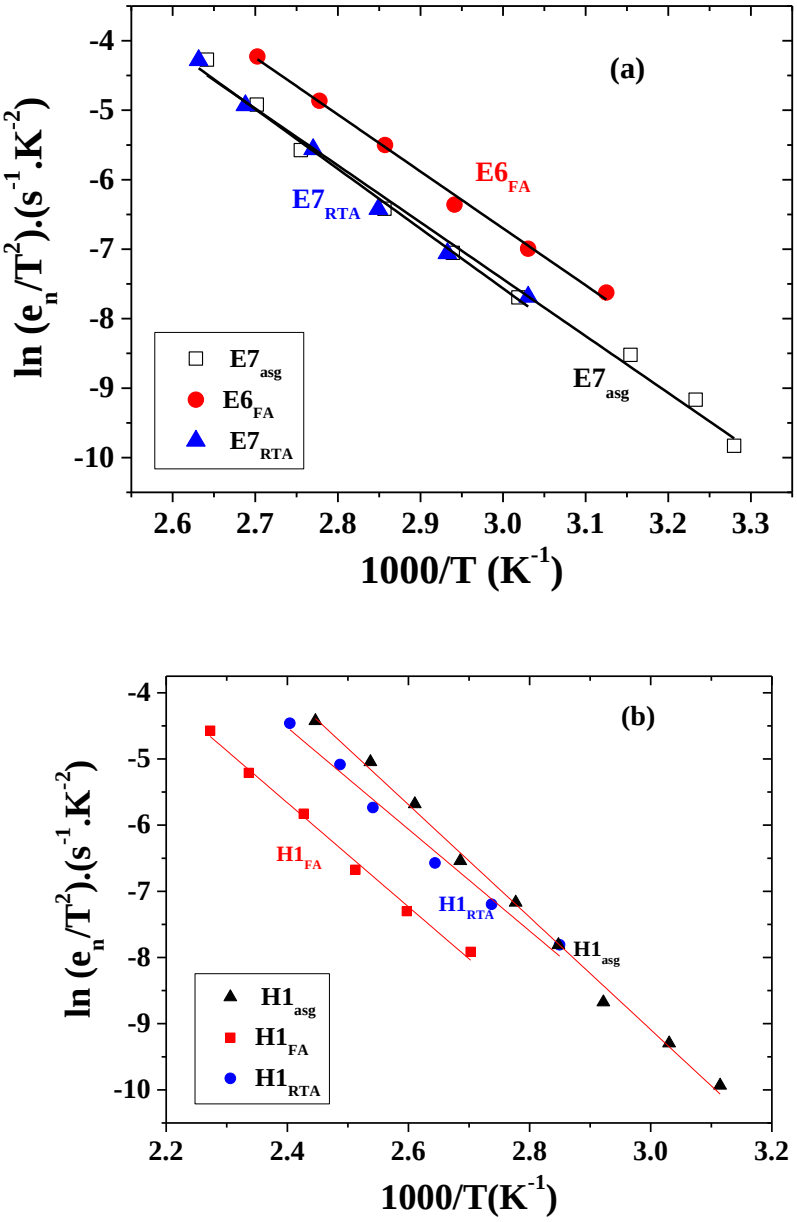


Figure 7.15: (a) Arrhenius plots obtained from Laplace DLTS data for as-grown and annealed (400 ^{o}C rapid thermal and furnace anneal) Te-compensated samples at a larger reverse bias of V_R = -4V which allows probing the region away from the interface of GaAs/GaSb heterojunction devices and (b) A new hole trap is detected in all Te-compensated as-grown and annealed devices.

Table 7.4: Trap activation energies, capture cross-sections and traps concentrations of Te-compensated as-grown, furnace annealed and rapid thermal annealed samples at V_R = -4V, V_P = 0V, and t_p = 1msec.

Sample ID	Traps	Activation Energy (eV)	Apparent Capture cross-section (cm^{-2})	Trap concentration (cm^{-3})
Compensated as-grown (asg)	$H1_{asg}$	0.73 ± 0.01	1.86×10^{-13}	1.58×10^{14}
	$E7_{asg}$	0.71 ± 0.01	7.76×10^{-15}	3.36×10^{15}
Compensated Furnace Anneal (FA)	$H1_{FA}$	0.68 ± 0.01	7.76×10^{-15}	1.21×10^{14}
	$E6_{FA}$	0.71 ± 0.01	8.10×10^{-13}	1.96×10^{14}
Compensated Rapid Thermal Anneal (RTA)	$H1_{RTA}$	0.66 ± 0.01	1.55×10^{-14}	1.65×10^{14}
	$E7_{RTA}$	0.74 ± 0.01	1.18×10^{-12}	7.91×10^{12}

In order to study further the existence of defects at/or close to the interface between GaAs and GaSb, a forward pulse is applied. The DLTS experimental conditions used for this study are V_R = 0V, V_P = 0.5V and tp = 1msec. The filling pulse V_P = 0.5V is equivalent to the turn on voltage observed from the I-V characteristics. The DLTS spectra are shown in Figure 7.16 for as-grown, rapid thermal and furnace annealed samples.

As shown in Figure 7.16, the shape of the signal due to the hole trap is asymmetric in as-grown, rapid thermal and furnace annealed samples. The DLTS hole peak amplitude is however lowest in rapid thermal annealed samples. The furnace annealed samples exhibit the highest DLTS hole peak. In addition, a broader electron peak is also detected in the temperature range of 10 K -200 K as shown in the inset of Figure 7.16. In order to resolve the asymmetric hole peaks, Laplace DLTS measurements are performed. Figure 7.17 (b, c and d) shows Laplace DLTS peaks detected four hole peaks in asgrown, furnace annealed and

rapid thermal annealed samples. Arrhenius plots of the emission rate versus temperature for all samples are plotted and shown in Figure 7.17a.

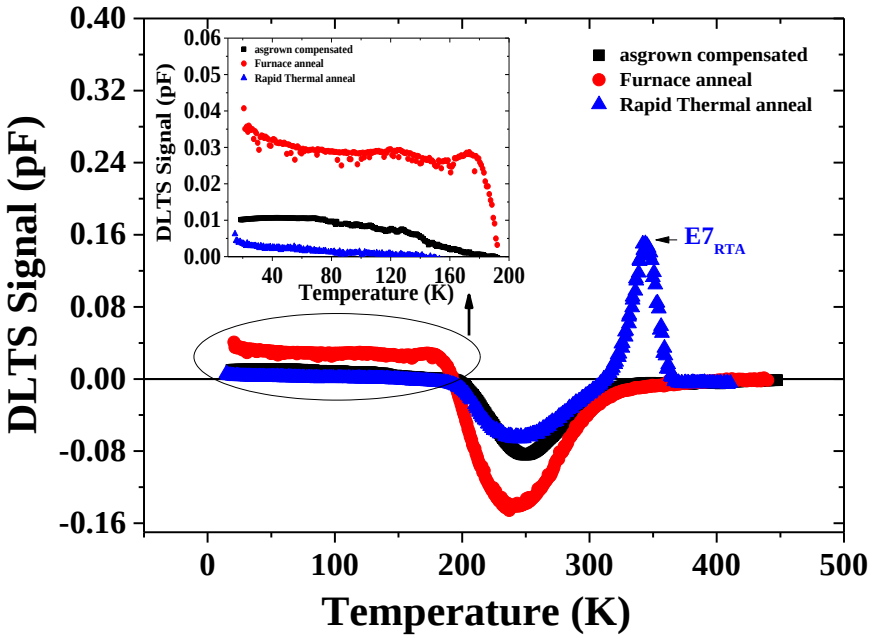
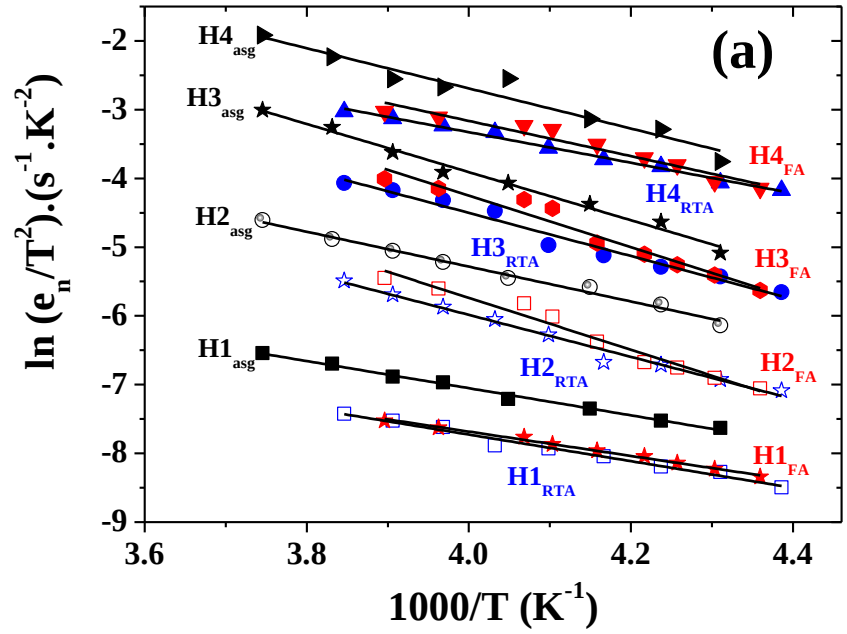
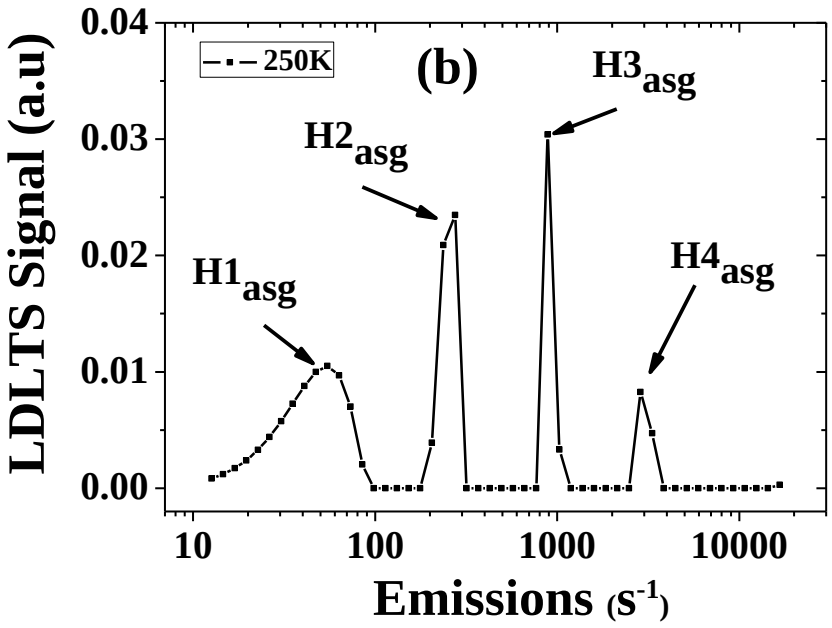


Figure 7.16: DLTS spectra of as-grown and annealed (400^{o}C rapid thermal and furnace anneal) Te-compensated GaSb/GaAs samples. The DLTS spectra shown are taken at a forward voltage with an amplitude equivalent to the turn on voltage of the devices in order to probe the interface between GaSb and GaAs. The reverse bias is V_R = 0V and the filling pulse characteristics were: V_p = 0.5V, t_p = 1msec, and rate window= 200 s^{-1}. For clarity the inset displays the peaks detected in the temperature range 10-200 K.


(a)
H4asg
H3asg
H2asg
H1asg
H4FA
H4RTA
H3RTA
H3FA
H2RTA
H2FA
H1FA
H1RTA
ln (en/T2).(s-1.K-2)
1000/T (K-1)


(b)
250K
H1asg
H2asg
H3asg
H4asg
LDLTS Signal (a.u)
Emissions (s-1)

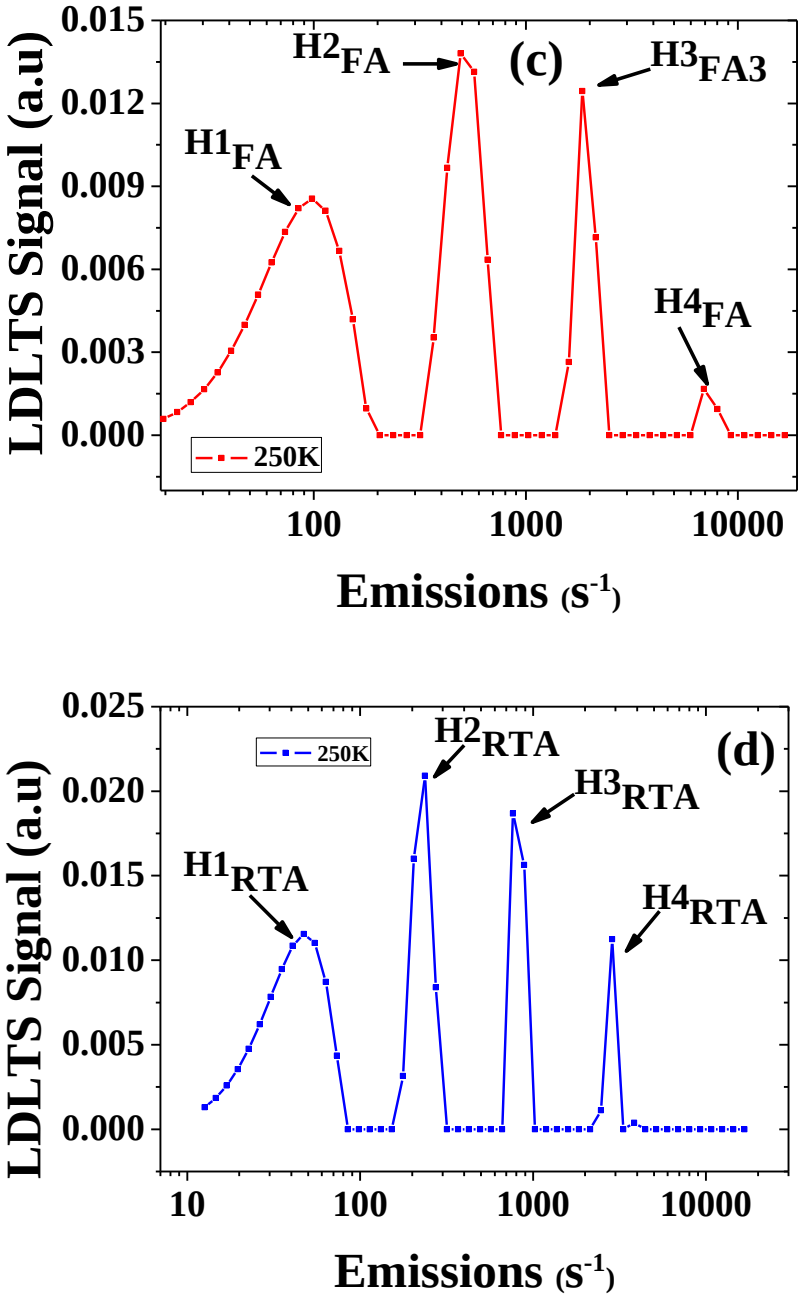


Figure 7.17: (a) Arrhenius plots obtained from Laplace DLTS for as-grown and annealed (400 ^{o}C rapid thermal and furnace anneal) Te-compensated samples for a forward bias voltage of V_p = 0.5V which allows probing the interface region of GaAs/GaSb heterojunction devices, (b) Four hole traps are detected all compensated as-grown sample by Laplace DLTS, (c) Four hole traps are detected all Furnace annealed compensated sample by Laplace DLTS and (d) Four hole traps are detected Rapid thermal annealed compensated sample by Laplace DLTS.

Four very well resolved peaks are detected in as-grown ($H1_{asg}$, $H1_{asg}$, $H1_{asg}$, $H1_{asg}$), rapid ($H1_{RTA}$, $H1_{RTA}$, $H1_{RTA}$, $H1_{RTA}$) and furnace ($H1_{FA}$, $H1_{FA}$, $H1_{FA}$, $H1_{FA}$) annealed samples by using Laplace DLTS as shown in Figure 7.17 b, c and d. It is worth mentioning here that these peaks are only present in as-grown and annealed Te compensated samples. These are absent in uncompensated samples. One can therefore infer that these hole traps are due to the incorporation of Te. The summary of the traps detected at V_R = 0V, V_P = 0.5V and t_p = 1msec are given in Table 7.5.

Table 7.5: Trap activation energies, capture cross-sections and traps concentrations of as-grown, rapid thermal and furnace annealed Te-compensated samples at V_R = 0V, V_P = 0.5V, t_p = 1msec.

Sample ID	Traps	Activation Energy (eV)	Apparent Capture cross-section (cm^{-2})	Trap concentration (cm^{-3})
Compensated as-grown (asg)	$H1_{asg}$	0.163 ± 0.003	2.57×10^{-21}	2.49×10^{13}
	$H2_{asg}$	0.219 ± 0.005	1.89×10^{-19}	2.52×10^{13}
	$H3_{asg}$	0.252 ± 0.013	1.56×10^{-17}	2.50×10^{13}
	$H4_{asg}$	0.302 ± 0.007	3.46×10^{-17}	2.28×10^{13}
Furnace Annealed (FA)	$H1_{FA}$	0.153 ± 0.004	8.10×10^{-22}	1.09×10^{13}
	$H2_{FA}$	0.221 ± 0.009	1.72×10^{-18}	9.87×10^{12}
	$H3_{FA}$	0.302 ± 0.010	6.52×10^{-17}	1.13×10^{13}
	$H4_{FA}$	0.325 ± 0.009	1.67×10^{-17}	1.50×10^{13}
Rapid Thermal Annealed (RTA)	$H1_{RTA}$	0.167 ± 0.004	1.45×10^{-21}	8.45×10^{11}
	$H2_{RTA}$	0.191 ± 0.003	3.76×10^{-19}	6.38×10^{11}
	$H3_{RTA}$	0.263 ± 0.007	7.43×10^{-19}	5.08×10^{11}
	$H4_{RTA}$	0.290 ± 0.008	4.51×10^{-18}	5.60×10^{11}

Some of these defects have energies close to the ones calculated by M. Hakala et al [24], who studied native defects in GaSb with respect to the valence band.

Figure 7.18 shows the defects observed in GaSb by M. Hakala et.al. The trap $H4_{asg}$, $H4_{RTA}$ and $H3_{FA}$ have energies ~ 0.30 eV could be related to the trap observed by Hakala et al with energy 0.31 eV and which was assigned to Gallium vacancies (V_{Ga}). Another common trap $H3_{asg}$, $H3_{RTA}$ and $H2_{FA}$ in as-grown compensated, rapid thermal and furnace annealed samples with energy ~ 0.26 eV also have same energy as Gallium antisite (Gallium on Antimony site (Ga_{Sb}) detected by Hakala with energy 0.26 eV. All the other traps detected in the samples investigated in this work are reported here for the first time. Their origin is not clear and further investigations are needed.

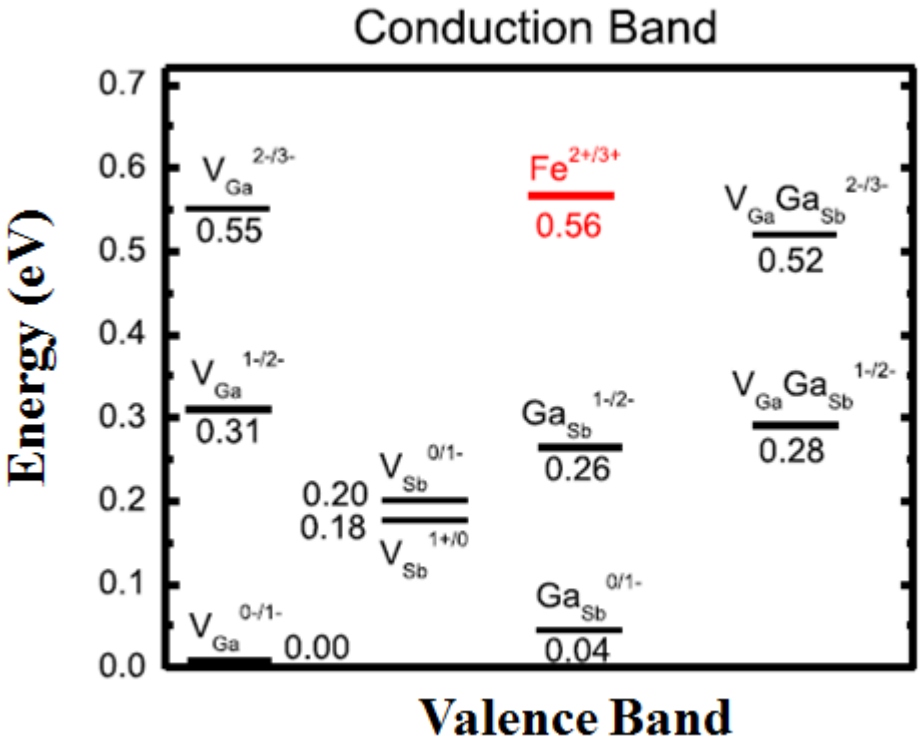


Figure 7.18: Charge native defects detected in GaSb by M. Hakala et al [24]

7.4 CONCLUSION

In summary, the effect of thermal treatment is studied in uncompensated and Te compensated p-n GaSb/GaAs samples. The heat treatment on uncompensated samples is performed by rapid thermal annealing procedure at three different temperatures 400 ^{o}C, 500 ^{o}C and 600 ^{o}C. The lowest reverse current is observed in600 ^{o}C annealed samples. Annealing of uncompensated samples resulted in a significant reduction of the interface state density for all heat treatments. The well-known EL2 defect is detected by DLTS in as-grown, 400 ^{o}C and 500 ^{o}C annealed samples. However, this defect is completely annihilated in samples annealed at 600 ^{o}C. These results provide strong evidence that the EL2 defect contributes to the reverse leakage current of the devices. Furthermore, annealing treatment is also performed on Te compensated samples by using two different annealing procedures, namely rapid thermal and furnace annealing. Both types of annealing are performed at 400 ^{o}C for 2 minutes. I-V and C-V characteristics show that the smallest reverse current and the lowest interface states capacitance are obtained when the Te compensated samples are thermally treated by using the rapid thermal annealing process. The furnace annealing procedure resulted in the highest value of reverse current. Furthermore, DLTS measurements are performed with small to large reverse biases and also with forward filling pulse voltages. The concentration of all traps detected in rapid thermal annealed samples are lowest than as-grown and furnace annealed samples. Forward bias DLTS measurements detected four hole traps in all samples, and the traps concentration is lowest in rapid thermal annealed samples. One can therefore conclude that rapid thermal annealing is far more effective annealing treatment compared to the furnace annealing process in terms of better electrical properties of devices.

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CHAPTER 8

ADMITTANCE SPECTROSCOPY AND DLTS STUDIES OF INTERFACE RELATED TRAPS IN INTERFACIAL MISFIT (IMF) GaSb/GaAs Heterostructures

In this chapter a detailed investigation of the interaction between the interface states and deep traps in Interfacial Misfit (IMF) GaSb/GaAs uncompensated and Te compensated samples is reported using DLTS and admittance spectroscopy measurement techniques. The DLTS experimental conditions are such that only the region close the interface is probed. The admittance technique involves the measurements of capacitance and conductance as function of frequency.

8.1 INTRODUCTION

Antimony-based III-V compounds, such as GaNAsSb grown on GaAs with a band gap of 1eV, have also several other applications, including multi-junction solar cells and surface emitting lasers (VCSELs). AlGaAsSb on InP substrates has been used to fabricate VCSELs operating at 1.55µm [2]. In addition, AlGaAsSb and GaInAsSb grown on GaSb have found applications in thermo photovoltaic [3, 4], IR LEDs, lasers [5] and detectors. One of the major issues to get maximum efficiencies from any heterostructure semiconductor device is the lattice mismatch between the active layers and the substrate. Due to this mismatch many channels are created near to the interfaces and active region of devices. One of the conventional way to reduce this mismatch is to grow new ternary, quaternary or pentary compound materials. However, there are some

growth and defects issues with these materials. The other method is to introduce a thick buffer layer on top of the substrate, which also has some drawbacks in terms of cost and devices performance. One of the best way to avoid such problems in growing heterostructures in lattice mismatched systems is by using a special growth method commonly referred to as Interfacial Misfit (IMF) technique [6, 7]. By using IMF technique all the energy resulting from the lattice mismatch is released laterally along the interfaces, and as a result one can grow any materials with minimum threading dislocations [6].In order to fully understand the role and behaviour of IMF detailed structural, optical and electrical measurements are required. Recently, improvements in the electrical performance have been demonstrated in GaAs/GaSb based heterostructures devices [8]. The samples investigated were named as uncompensated (simple GaAs/GaSb with IMF interfaces) and compensated samples (Te is used at the interface to act as compensation of dangling bond created during IMF).The improvement of electrical performance has been achieved in Te compensated samples. Current Voltage (I-V) measurements on both samples reveal that uncompensated samples have higher turn-on (V_{on}) voltage, while in the Te compensated samples the turn-on voltage is much smaller. This effect was explained in terms of compensation of unwanted channels with Te atoms [9]. In this work defects measurement on devices grown by the same technique showed similar I-V characteristics as reported in reference [9]. In order to fully understand the behaviour of I-V data, DLTS technique was employed. The focus of the studies reported in Chapter 6 was mainly near to the interface using small reverse biases. From DLTS, C-V and C-F measurements it was concluded that the compensated samples have more defects and interface states than uncompensated samples. In this chapter the main

focus is to understand interface states by use of conductance (G) as function of frequency (f), capacitance (C) as function of frequency (f) and density of interface states (N_{ss}) calculated by the well-established methods [10, 11].

8.2 RESULTS AND DISCUSSIONS

8.2.1 I-V CHARACTERISTICS AT DIFFERENT TEMPERATURES

Dark I-V characteristics as a function of temperature (180–420 K at 20 K intervals) were measured on both uncompensated and Te compensated samples, as shown in Figure 8.1 (for clarity purposes only selected representative curves are shown). It was found and discussed in previous studies (the results are discussed in detail in chapter 6) that the low value of turn on (V_{on}) is due to the interface states generated by the incorporation of Te atoms at the interface in compensated samples. The reverse current varies as a function of temperature as shown in Figure 8.1. The reverse current variation as function of temperature for compensated samples is higher than for uncompensated samples. This behaviour can be explained by using the characteristics parameters of the devices, which will be discussed later. By comparing the uncompensated and compensated samples, it is clear that after δ-doping with Te-atoms at IMF the reverse leakage current increases. Additionally, it can be seen from Figure 8.1 that the reverse current in compensated samples is temperature dependent and increases dramatically. However, in the uncompensated samples the reverse current is not sensitive to the temperature. This behaviour in the uncompensated samples is attributed to the lower probability of formation of defects that act as recombination levels. This is confirmed by DLTS results which were discussed in Chapter 6 for a range of voltage biases.

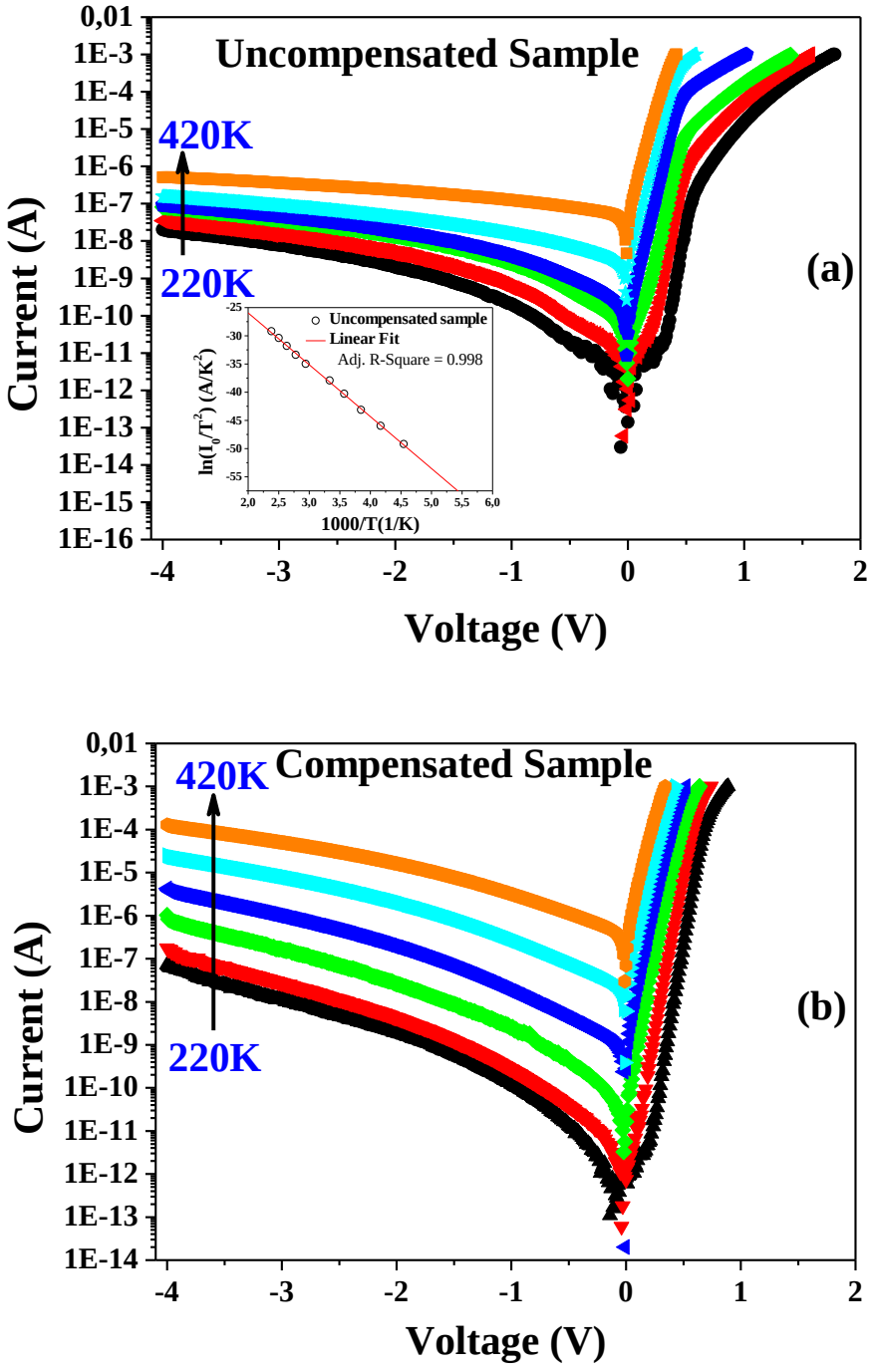

Figure 8.1: Semi-logarithmic plots of dark I–V characteristics (a) Uncompensated and (b) Compensated samples in the temperature range of 220–420 K at 40 K intervals. The inset in (a) shows the thermionic emission current as a plot of ln (I_0/T^2) vs. 1000/T.

On the other hand, the rectification ratio (which is the ratio of forward current (I_F) to the reverse current (I_R)) was evaluated at the applied voltage of 0.5 V. It was observed that at room temperature the value of the rectification ratio is approximately $8x10^3$ and 300 $x10^3$ for the uncompensated and compensated samples, respectively.

The current–voltage (I–V) characteristics of ideal diodes as described by the thermionic emission of conduction electrons including the series resistance is given by [12]

$$I = I_0\left(\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right) \tag{8.1}$$

where the saturation current, I_0, is defined by:

$$I_0 = AA^*T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \tag{8.2}$$

In the equations 8.1 and 8.2, A is the effective diode area (A= $0.314 \times 10^{-3} cm^2$), A^* is the effective Richardson's constant, k is the Boltzmann's constant, T is the temperature, and q is the elementary charge. The value of the effective Richardson constant used was 8.7 $A/cm^2.K^2$. Additionally, ϕ_b **,** n and R_s represent the barrier height, ideality factor, and series resistance, respectively, and were calculated from I-V measurements as shown in Figure 8.2 The plot of ln (I_0/T^2) vs. 1000/T (inset of Figure 8.1(a)) in the temperature range from 220 to 420 K follows a straight line, which suggests that the conduction mechanism may be governed by thermionic emission and the saturation current can be obtained by using Eq. 8.2 [13]. The compensated samples also show similar behavior [not shown in Figure 8.1 (b)].

The apparent room temperature barrier height was found to be 0.83eV and 0.76 eV for the uncompensated and compensated samples, respectively. These values decrease as the temperature decreases as can be clearly seen in Figure 2(a); at 180 K this value is 0.75 eV and 0.54 eV for uncompensated and compensated samples, respectively. The ideality factor with a value between 1.17 and 1.04 (a mean value of 1.05) confirms the stability of the uncompensated samples in the temperature range 180–420 K. However, experimental values of n for the compensated samples (with a mean value of 1.3) exhibit an increase when the temperature decreases, changing from 1.4 at 180 K to 1.15 at 420 K. The values of the ideality factor for compensated samples are higher than those of the uncompensated samples. The larger deviation of n from unity for the compensated samples is probably due to the presence of Te-atoms incorporated by the δ-doping technique at IMF producing interface states.

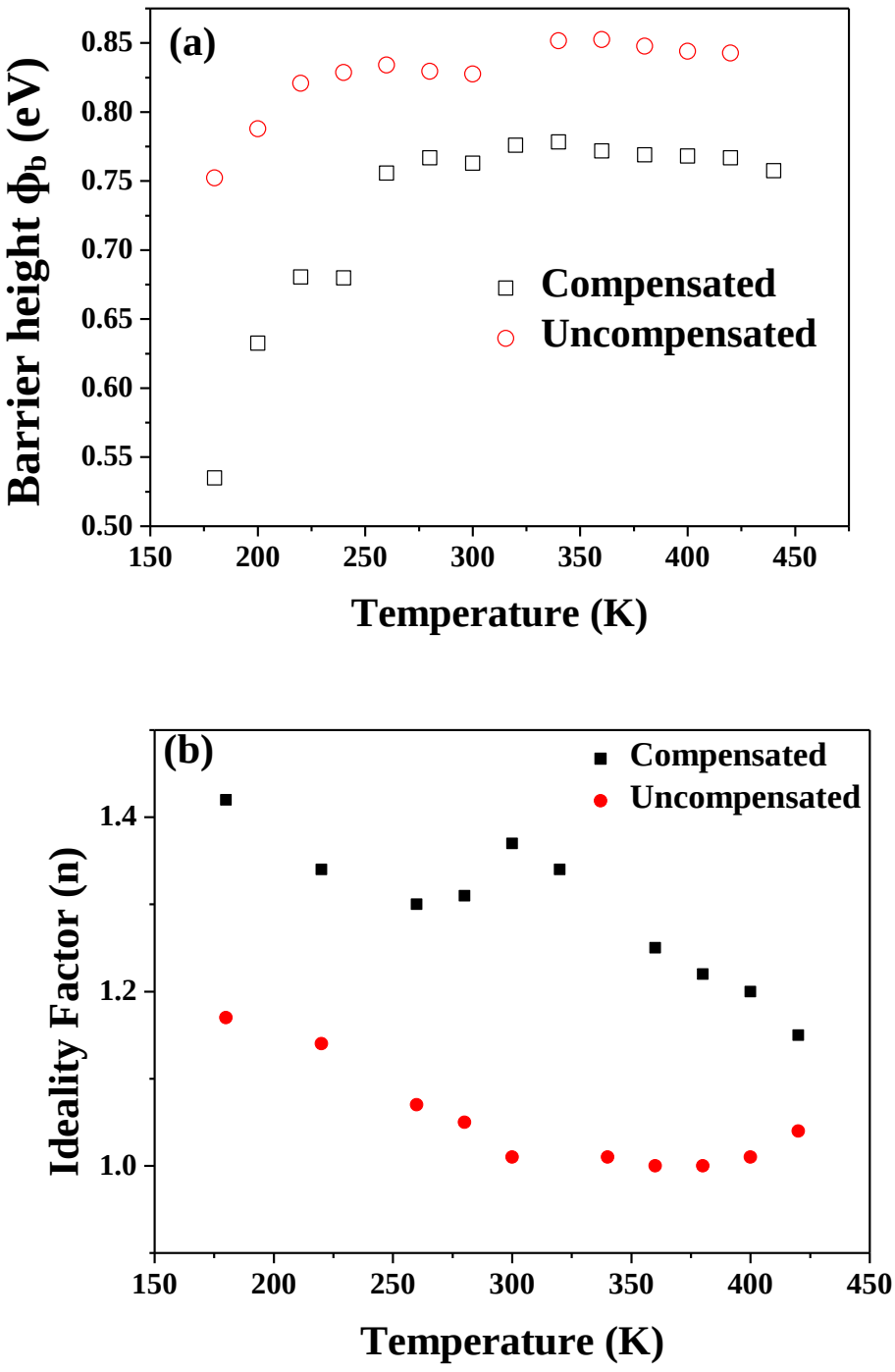

Figure 8.2: Temperature dependence of the experimental barrier height (a) and ideality factor (b) determined from I–V characteristics of uncompensated and compensated samples in the temperature range of 180–420 K at 20 K intervals.

The I-V measurements at different temperatures are used to calculate the main trap contributing to the leakage current [14]. Figure 8.3 presents plots of the reverse current in the dark versus 1000/T measured at a bias voltage of -0.25V. The main trap in the uncompensated samples has an activation energy EA_{UC} = 0.81 ± 0.01 eV. On the other hand for the Te compensated samples two dominant traps were detected with activation energies EA_{C1} = 0.16 ± 0.02 eV and EA_{C2} = 0.82 ± 0.01 eV. It is important to point out that the defects EA_{UC} and EA_{C2} observed in uncompensated and Te compensated samples, respectively, have similar activation energies as the well-known EL2 in GaAs. The additional trap with activation energy of 0.16 ± 0.02 eV detected in Te compensated samples could be related to antimony vacancy (V_{Sb}) [15]. This defect (V_{Sb} vacancy) along with EL2 could explain the larger value of reverse current in compensated samples. The presence of the larger number of defects determined from I-V characteristics could explain the higher reverse current observed in the compensated samples [14].

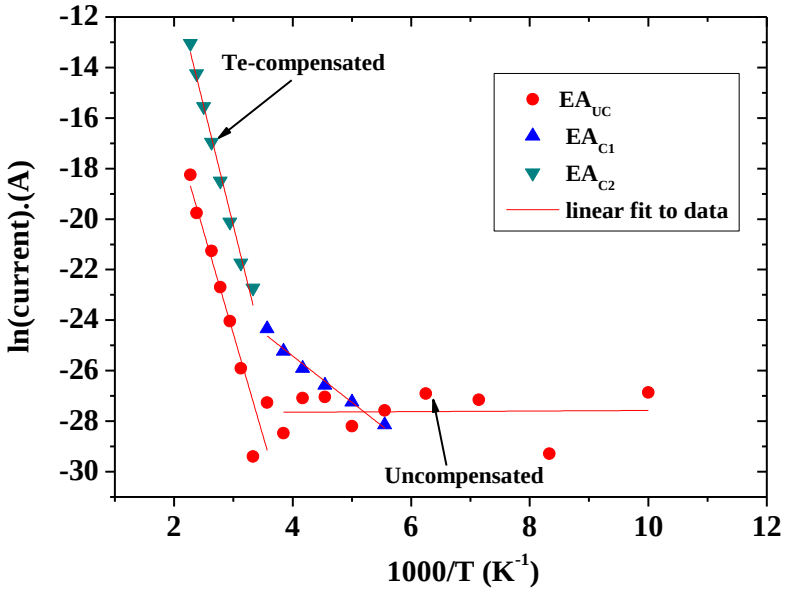

Figure 8.3: plots of the reverse dark current versus inverse of temperature for reverse bias voltage of V_R =-0.25 V

In summary, three main observations were made from the I-V results (i) the compensated samples have higher values of ideality factor ; (ii) The compensated samples have lower values of turn-on voltage; (iii) the compensated samples have lower values of barrier height and larger leakage currents. The inferior properties of the compensated samples can be due to the presence of two main defects states, which could be related to the incorporation of Te atoms to create interface states.

8.2.2 DENSITY OF INTERFACE STATES IN UNCOMPENSATED AND COMPENSATED SAMPLES

C-F measurement is one of the most popular non-destructive methods for getting information about interfaces [16, 17]. At sufficiently high frequencies, normally the capacitance due to interface states does not follow the AC signal. The only capacitance is due to the space-charge capacitance detected at higher frequencies.

At low frequencies, the experimental capacitance obtained from the C–F measurements approximately equals to the sum of space-charge capacitance (Cs) and the interface capacitance (Cit) [18, 19]. The distribution of interface states can be calculated by using capacitance–frequency measurements at forward biases. Figure 8.4 shows the equivalent circuit with oxide capacitance (C_{ox}), interface state capacitance (C_{it}) and depletion layer capacitance (C_s), respectively.

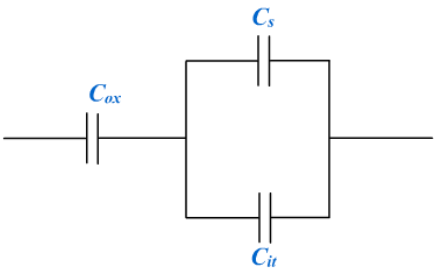

Figure 8.4: schematic diagram of equivalent circuit of parallel combination of interface state capacitance and depletion layer capacitance in series with oxide capacitance.

C_{ox} is the capacitance measured in strong accumulation (i.e. in GaSb/GaAs heterostructures system this value is deduced from the forward C-V peak). This value of C_{ox} (obtained from high frequency (2 MHz)) is in series with the parallel combination of C_{it} and C_s as can be seen in Figure 8.4 showing the equivalent circuit model of a real diode.

In order to measure the density of interface states, the C-F measurements are performed at 300K in the forward DC-bias (from 0V to 0.40V). Figure 8.5 and Figure 8.6 show the C-F measurements obtained on uncompensated and Te compensated samples, respectively. The discontinuities observed in the data points of Figure 8.5 and Figure 8.6 is due to instrumental error.

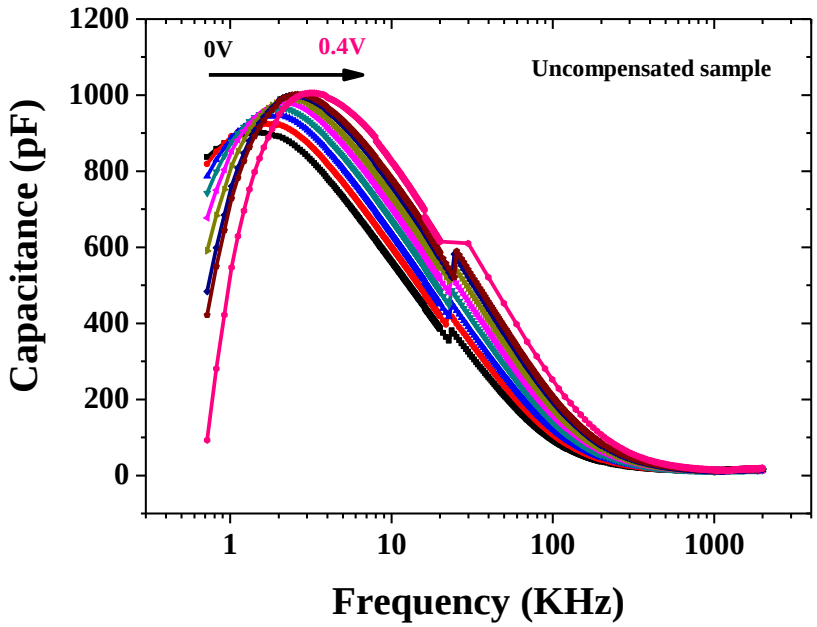

Figure 8.5: Room temperature experimental C–F curves of the IMF-GaSb/GaAs uncompensated samples recorded for voltages ranging from 0V to 0.40V (forward voltage steps of 0.02 V are used for these measurements).

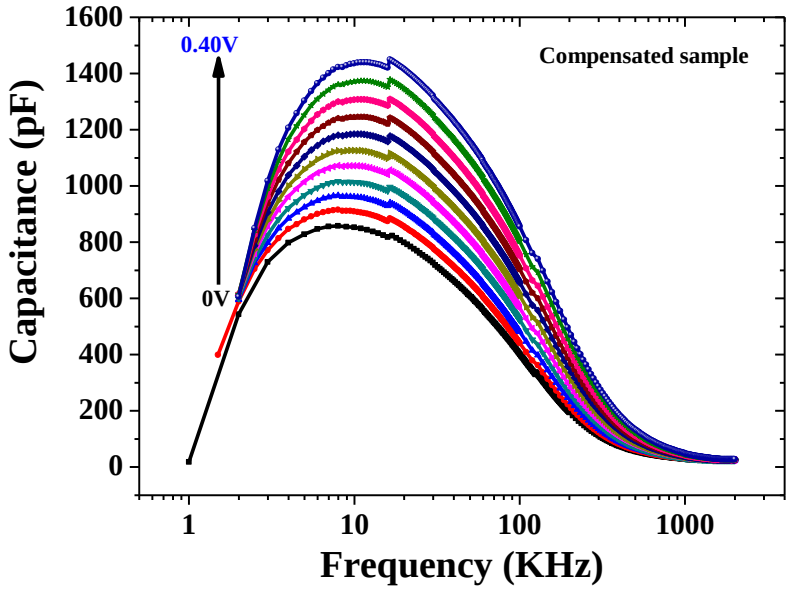

Figure 8.6: Room temperature experimental C–F curves of the IMF-GaSb/GaAs compensated samples recorded for voltages ranging from 0V to 0.40V (forward voltage steps of 0.02 V are used for these measurements).

The capacitances at low frequencies (C_{LF}) and at high frequencies (C_{HF}) for uncompensated and compensated samples are determined from Figure 8.5 and Figure 8.6, respectively. The C-V measurements are performed on both samples at a frequency of 2MHz. The capacitance peak maximum that appears in the forward voltage is used as C_{ox} as shown in Figure 8.7 for both uncompensated and Te compensated samples.

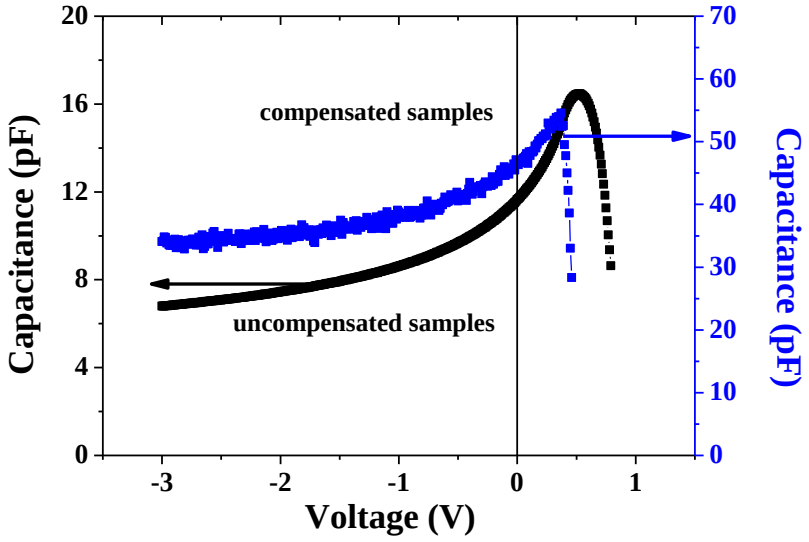

Figure 8.7: The experimental C–V plots of the IMF-GaSb/GaAs uncompensated and compensated samples at T = 300 K and frequency of 2 MHz.

Thus the density of interface state profile is calculated by using Eq. (8.3) as follows:

$$D_{it} = \frac{1}{qA}\left[\left(\frac{C_{LF}.C_{ox}}{C_{ox}-C_{LF}}\right) - \left(\frac{C_{HF}.C_{ox}}{C_{ox}-C_{HF}}\right)\right] \qquad (8.3)$$

where A is the area of the rectifier contact ($A=3.14x10^{-4}$ cm^{-2}) and q is the electronic charge. In Equation (8.3) C_{LF} is the capacitance at a frequency of 10 kHz, and C_{HF} is the capacitance at 2 MHz frequency.

From the measured low frequency capacitance at 10 kHz and high frequency capacitance at 2 MHz curves and using Equation (8.3), the D_{it} values were determined and the plots of D_{it} versus voltage is shown in Figure 8.8.

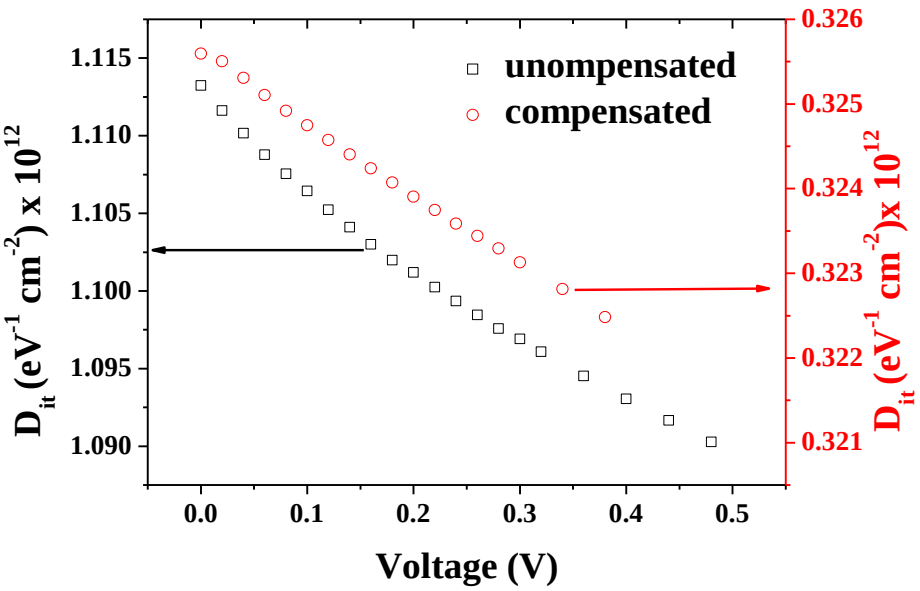

Figure 8.8: The energy distribution profile of D_{it} obtained from high-low frequency capacitance technique for uncompensated and compensated sample at room temperature.

The values of D_{it} for uncompensated and compensated samples are of the order of 10^{11} $eV^{-1}cm^{-2}$ and 10^{12} $eV^{-1}cm^{-2}$, respectively. These values are in good agreement with those reported in the literature, i.e, about 10^{12} eV^{-1} cm^{-2} [20]. As expected and as shown in Figure 8.8, D_{it} for compensated samples is approximately one order of magnitude higher than uncompensated samples. Thus, the higher interface trap density is very probably the cause of the larger leakage current, higher ideality factor and lower value of turn-on voltage in compensated samples. As can be observed in Figure 8.8, the density of interface states decreases as the bias voltage increases from 0 V to 0.5 V. This behaviour confirms that there are various energy levels at the GaSb/GaAs junction [20].

The frequency dependent series resistance, which gives information about interface states, can be calculated from the experimental Capacitance-Conductance-Frequency (C–G–F) measurements by using the following relationship [21]

$$R_s = \frac{G}{G^2+(\omega C)^2} \qquad (8.4)$$

where C and G are the measured capacitance and conductance values, respectively.

Figure 8.9 and Figure 8.10 represent the series resistance (R_s) versus frequency (F) of uncompensated and compensated samples at 300K and at different forward bias voltages, respectively. It is clear from both Figures (8.9, 8.10) that at low frequencies the series resistance is considerably higher than that at high frequencies, where it reaches a steady value. This frequency dependent series resistance is attributed to the distributions of interface states [21, 22]. It is worth pointing out here that R_s values are higher in compensated samples than those of the uncompensated samples, indicating higher interface traps. This supports further the above analysis of D_{it}, which is calculated as one order of magnitude higher in compensated samples.

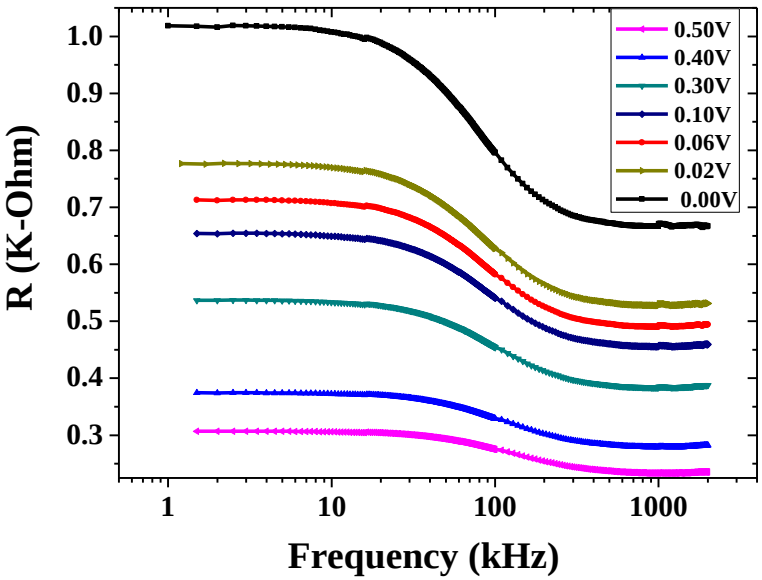

Figure 9: Room temperature series resistance versus frequency plots at various forward bias voltages of the uncompensated IMF samples.

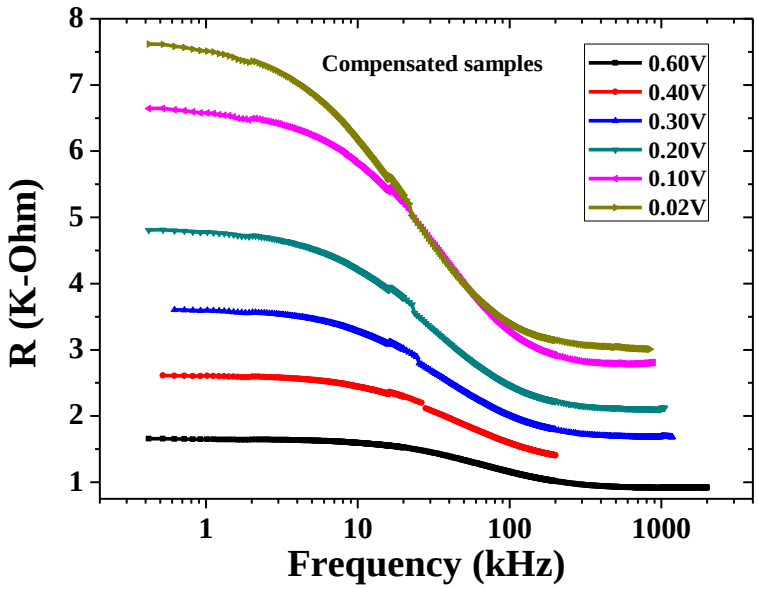

Figure 10: Room temperature series resistance versus frequency plots at various forward bias voltages of the compensated IMF samples.

8.2.3 G-F MEASUREMENTS

The conductance method is considered to be one of the most sensitive methods to extract information about density of states [19, 23]. The thermionic current is affected by the presence of interfacial states which contribute to the capture and emission process of electron/holes between the conduction/valence band and traps. These conductance (G_{ss}) losses due to the capture and emission of carriers can be calculated using Nicollian's method [19]. In this method the conductance (G_{ss}) as function of frequency characteristics are measured for a range of temperatures and biases [10]. The G_{ss}/ω as function ω is plotted at different temperatures using Arrhenius plot. The probability for an electron or hole to occupy a given interface state depends on the energetic location of the interface state relative to the Fermi energy, just like the impurity energy states in the bulk of a semiconductor. The conductance as function of frequencies measurements are performed on uncompensated and Te compensated samples in the temperature range 40K to 300K as shown Figure 8.11 and Figure 8.12, respectively. The value of G_{ss} is calculated from the measured conductance (G_m) and measured capacitance (C_m) of uncompensated and compensated samples by using the following equation [10].

$$G_{ss}/\omega = \frac{\omega\, C_m G_m (C_m - C_{HF})}{G_m^2 + (C_m - C_{HF})^2 \omega^2} \qquad (8.5)$$

where C_m and G_m are measured capacitance and conductance at different frequencies, respectively, and C_{HF} is capacitance at high frequency (2MHz).

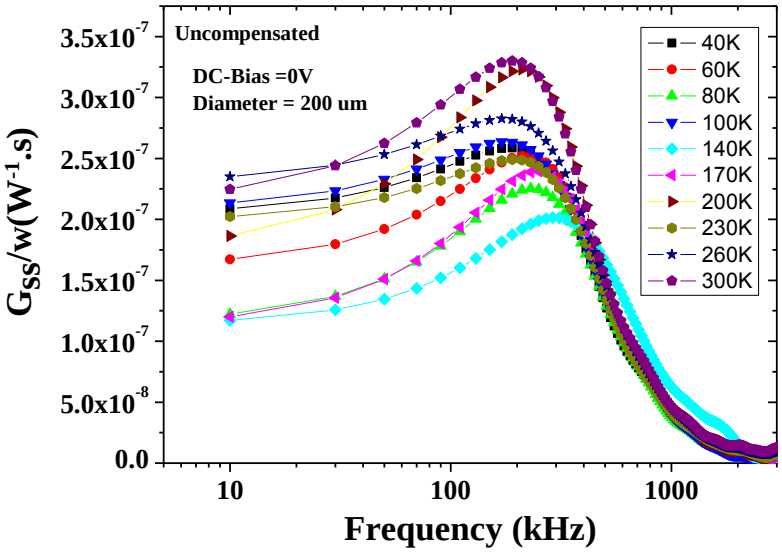

Figure 8.11: The frequency dependent variations of interface conductance at range of temperatures for uncompensated samples.

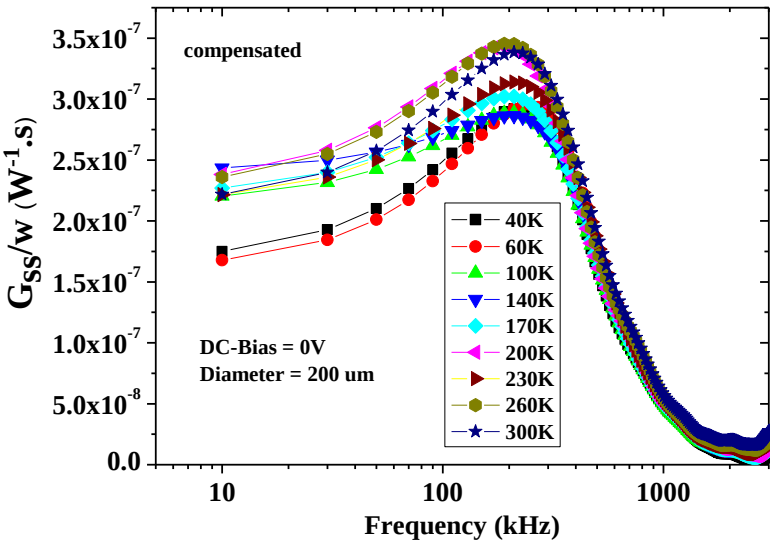

Figure 8.12: The frequency dependent variations of interface conductance at range of temperatures for compensated samples.

By using the peak maxima of Figure 8.11 and Figure 8.12, the activation energy of the corresponding trap is calculated by plotting ω_{max}/T^2 ($\omega_{max}=2*\pi*f_{max}$) versus 1/T. Figure 8.13a and b shows the Arrhenius plot of both uncompensated and compensated samples. Two shallow level traps with energies T_{uc1}=10 meV and T_{uc2}= 46meV are detected in uncompensated samples shown in Figure 8.13a. Similarly, two defects T_{c1}=11 meV and T_{c2}= 33meV are detected in compensated samples as shown in Figure 8.13b. It is worth pointing out that these traps were not detected in uncompensated samples using DLTS, and their origin is still not known. However, these traps might be interface traps since they are detected at low frequencies (~100 KHz to 400 KHz) as shown in Figure 8.11 and Figure 8.12. The emission from interface traps is a slow process which is only activated at low frequencies. The DLTS measurements are performed on both samples with fixed frequency of 1MHz. This could be one of the reasons why these traps are detected by conductance methods and not by standard DLTS technique.

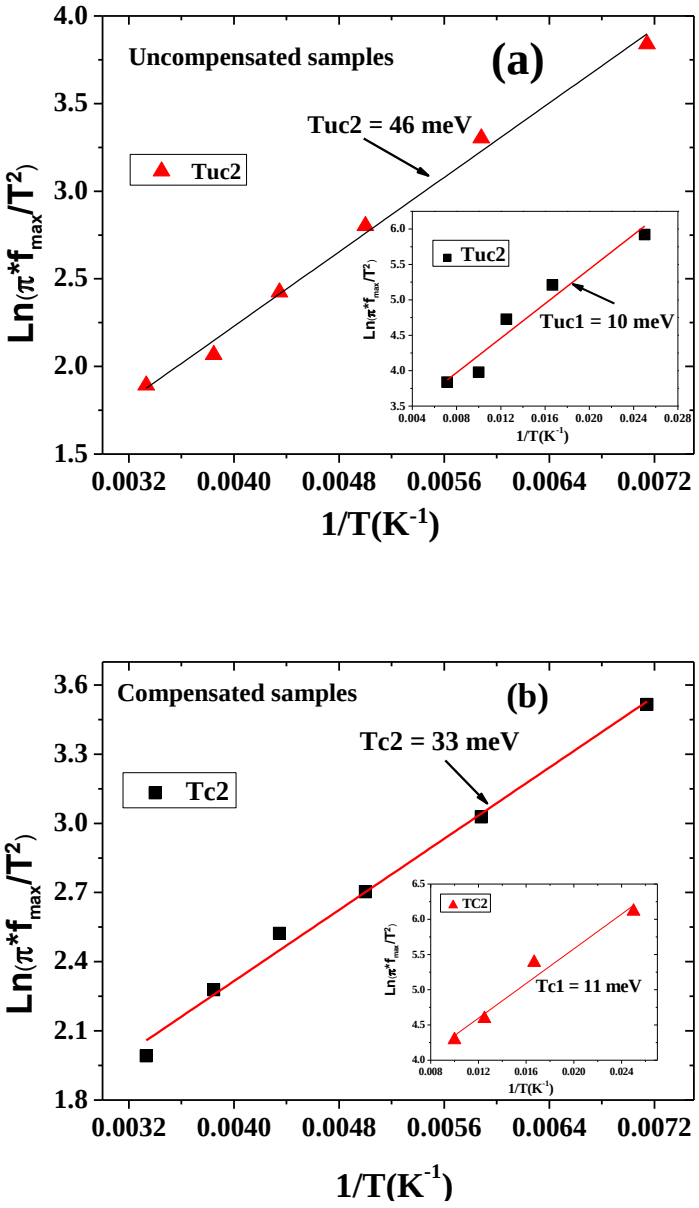

Figure 8.13: Arrhenius plot of activation energies calculated from peak maximum of G_{ss}/ω at a range of temperatures for (a) uncompensated sample and (b) Te-compensated samples.

The value of density of states (D_{it}) can be obtained from the magnitude and frequency position of the peak of G_{ss}/ω (from Figure 8.11 and 8.12) at given temperature. The value of D_{it} is given by

$$D_{it} = (G_{ss}/\omega)_{peak}/0.4029qA \qquad (8.6)$$

where q is the charge and A is the area of the diode. D_{it} is calculated by using Figure 8.11 and 8.12, and is shown in Figure 8.14 for uncompensated and Te-compensated samples. D_{it} for the uncompensated samples decreases at low temperatures and then it starts increasing from ~170K. On the other hand the density of interface states remains constant in this temperature range and then starts increasing in compensated samples. This behaviour could explain the higher R_s values observed in compensated samples as compared to those of the uncompensated samples (shown in Figure 8.9 and 8.10).

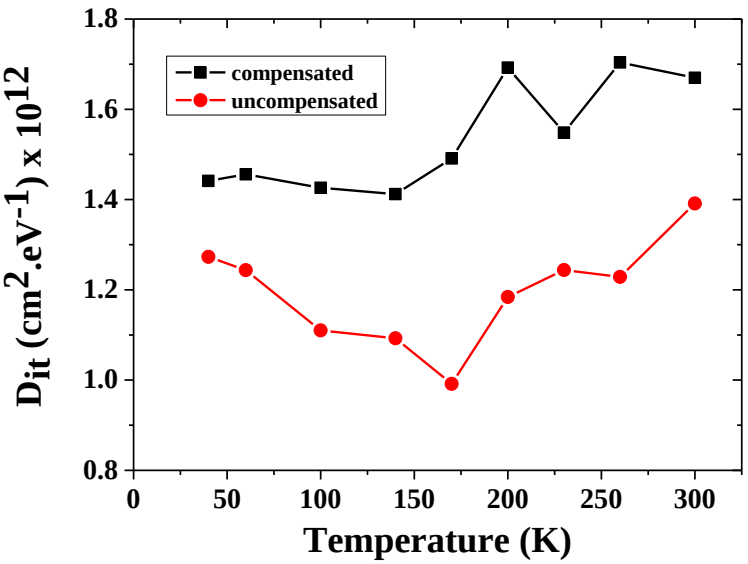

Figure 8.14**:** variations of density of states as function of temperature for both compensated and uncompensated samples.

8.2.4 DLTS MEASUREMENTS IN FORWARD BIAS

Systematic studies have been performed and discussed in Chapter 6 on uncompensated and Te compensated samples by using DLTS at various biasing conditions. It was concluded that Te-atoms in compensated samples introduce more electrical active defects near the interfaces. The well-known EL2 level, considered as an antisite defect, was reported as the common trap in both samples.. In the previous sections a detailed study was performed by analysing I-V, C-G-F, Rs-F, D_{it} and D_{it} as function of temperature characteristics. It was also concluded that Te compensated samples show poor electrical performance. In this section DLTS measurements carried out on both samples will be discussed using forward bias conditions, which will allow moving the depletion region towards the interface from equilibrium position. The DLTS experimental conditions are V_R = 0V, V_P = 0.5V and filling pulse duration (t_p) = 1msec for both samples. Figure 8.15 shows DLTS spectra of uncompensated and compensated samples.

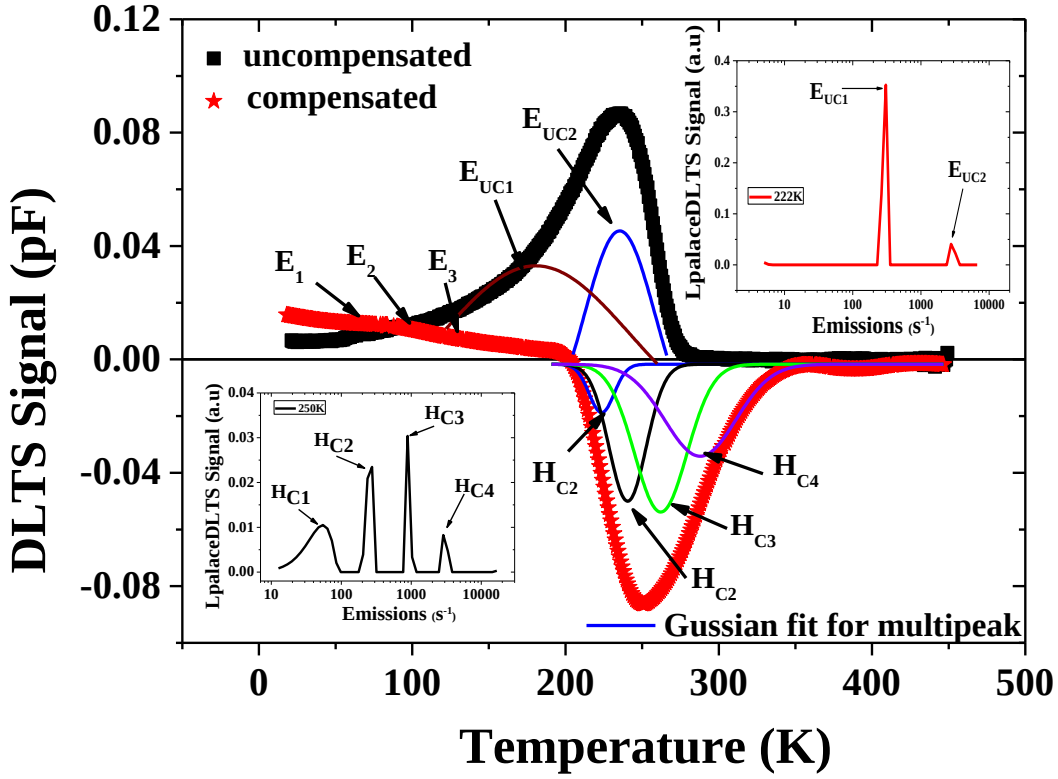

Figure 8.15**:** DLTS spectra of uncompensated and compensated samples taken near the interface region between GaSb/GaAs using forward DLTS biasing conditions, namely V_R = 0, V_P =0.5V, and t_p =1msec. Also shown are Gaussian fits to the broad DLTS peaks. The insets show Laplace DLTS peaks detected in both devices.

It can be seen from Figure 8.15 that in the uncompensated samples only one electron peak is detected. This peak is asymmetric and the Guassian fitting to the conventional DLTS peak shows two peaks (as seen in Figure 8.15). In order to resolve this peak, Laplace DLTS is employed, which clearly separates two very well resolved peaks, namely E_{UC1} and E_{UC2} (shown in the inset of Figure 8.15). On the other hand for the compensated samples show a broad hole peak and a broader electron peak. Laplace DLTS on these Te compensated samples resolve four hole peaks H_{C1}, H_{C2}, H_{C3} and $H_{C4,}$ and three electron peaks (E_1, E_2 and E_3).

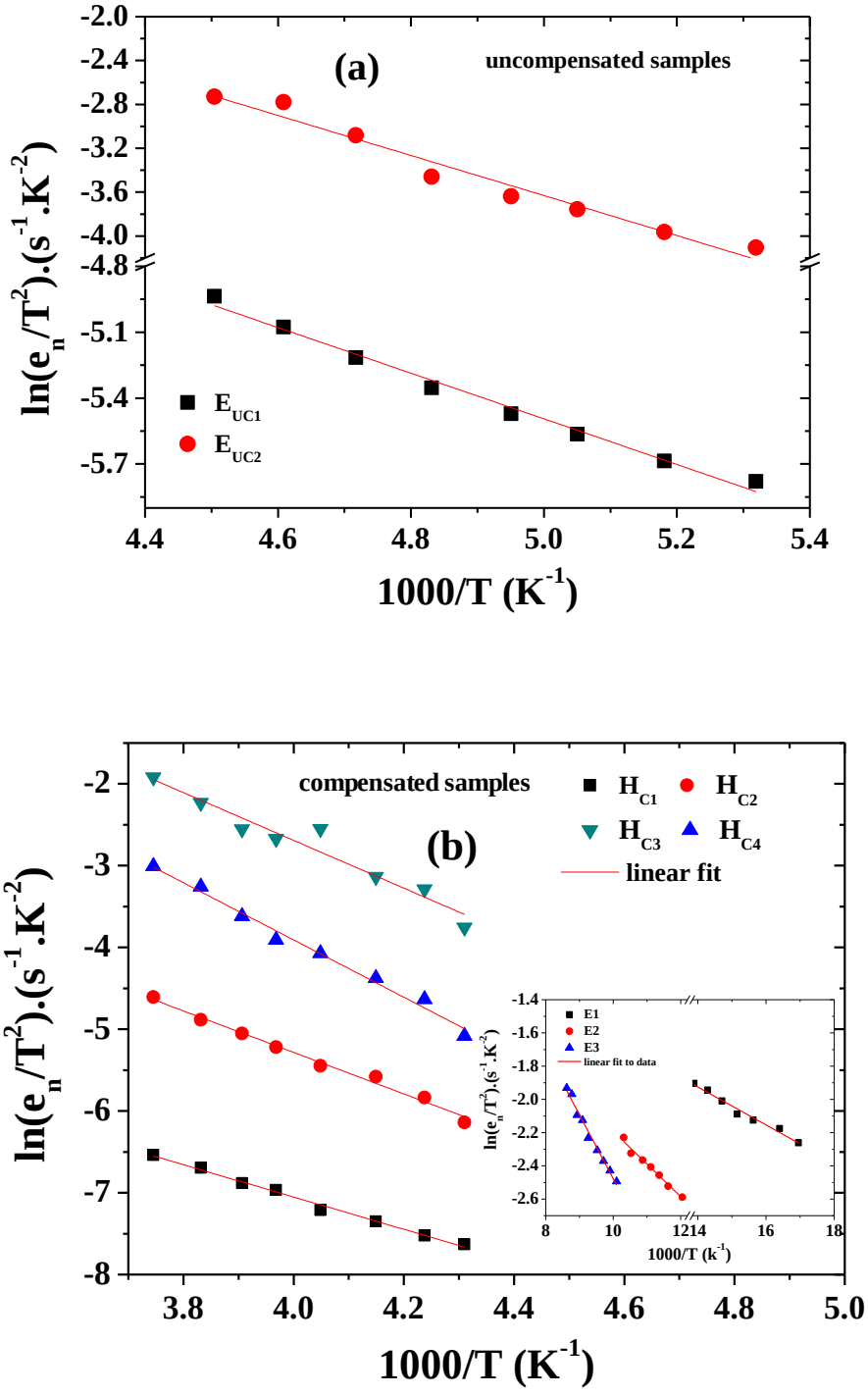

Figure 8.16**:** Arrhenius plots of (a) uncompensated samples and (b) Te-compensated samples at reverse bias of V_R = 0V, V_P = 0.5V and t_p =1msec. Whereas the inset in (b) shows Arrhenius plots for the detected electron traps.

The activation energies, capture cross-section and concentrations calculated from Arrhenius plot are shown in Table 8.1.

Te is considered to diffuse easily into bulk GaSb [24]. In compensated samples Te atoms are present at the interface and they could diffuse into either side of the interface. They could also create complexes and other intrinsic defects such as tellurium donors (Te_{As}), Ga vacancies (V_{Ga}), and Ga vacancy–donor complexes (V_{Ga}–Te_{As}), Ga_{Sb}–V_{Ga}, Te_{Sb}, Ga_{Sb} [25-27]. As discussed in Chapter 6, only electron traps are detected close to the interface with the DLTS experimental condition V_R = -0.25 V, V_P = 0 V and t_p =1 msec. However, when the forward biasing is increased to probe the region closer to the interface using V_R = 0V, V_P = 0.5V and t_p =1msec,, two electron traps, E_{1UC} and $E_{2UC,}$ are observed in uncompensated samples with activation energies 0.090 ± 0.002 eV and 0.157 ± 0.009 eV, respectively. M. Kaniewska et al [28] studied trapping centers at the interface of GaAs/GaAs homostructures grown by MBE-interruption growth technique using capacitance versus voltage (C–V) and DLTS measurements. They observed two electron traps, one of which has an activation energy of 0.16 eV. They suggested that the formation of this defect is related to the arsenic overpressure. They also detected a defect in MBE grown InAs/GaAs samples with a similar activation. M. Kaniewska et al [28] argued that the excess of As is also responsible for the generation of this defect in InAs/GaAs heterostructures instead of strain built at the interface. It also important to point out that an unidentified trap with similar activation energy in Te-Doped GaSb was reported by A. Venter et al [29]. However, the Te compensated samples investigated in this work displayed four new hole traps (H_{C1}, H_{C2}, H_{C3} and H_{C4}) which were not observed in uncompensated samples. The three electron traps E1, E2 and E3 at V_R

= 0V, V_P = 0.5V and t_p = 1msec (region probed is more closer to the interface) are exactly the same as those reported in Chapter 6 in Te compensated samples at V_R = -0.25V, V_P = 0V and t_p = 1msec (region probed is further away from the interface). Since these traps are absent in uncompensated samples it is most probable that they are related to the incorporation of Te atoms. E. Kuramochi et al [26] reported two acceptor level defects in Te-doped GaSb layers using DLTS. They assigned the 0.25 eV level to Ga_{Sb}-V_{Ga} complex. M. Hakala [15], studied self-diffusion in GaSb by using ab initio methods and also assigned the 0.27eV acceptor level to Ga_{Sb}-V_{Ga}. In the samples investigated here the H_{C3} acceptor with energy 0.252 ± 0.02eV could be assigned the Ga_{Sb}-V_{Ga} complex. The acceptor trap H_{C4} present in the compensated samples having an activation energy of 0.302 ± 0.01eV could have the same origin as the one reported in references [30, 31] The other defects detected in this work are believed to be new and their origin is still unknown.

Table 8.1: summary of traps detected by DLTS and conductance methods in uncompensated and Te-compensated samples.

Samples name	Trap	Activation Energy (eV)	Apparent Capture cross-section (cm^2)	Trap concentration (cm^{-3})
Uncompensated samples	E_{u1}	0.090 ± 0.002	1.10×10^{-20}	3.18×10^{-12}
	E_{u2}	0.16 ± 0.01	3.55×10^{-18}	1.36×10^{-13}
Conductance Method	Tuc1	0.046± 0.01		
	Tuc2	0.010± 0.02		
Compensated samples	E_{C1}	0.010 ± 0.002	1.08×10^{-20}	5.51×10^{-13}
	E_{C2}	0.017 ± 0.002	1.18×10^{-20}	1.93×10^{-12}
	E_{C3}	0.033 ± 0.002	5.75×10^{-20}	4.34×10^{-12}
	H_{C1}	0.17 ± 0.01	1.06×10^{-19}	3.33×10^{-13}
	H_{C2}	0.22 ± 0.02	6.81×10^{-19}	8.01×10^{-13}
	H_{C3}	0.25 ± 0.02	6.65×10^{-17}	1.04×10^{-12}
	H_{C4}	0.30 ± 0.01	1.16×10^{-16}	5.11×10^{-12}
Conductance Method	Tc1	0.033± 0.01		
	Tc2	0.011± 0.01		

8.3 CONCLUSION

In summary a detailed analysis of the I-V, C-G-f and DLTS measurements of uncompensated and compensated samples was carried out. From the I-V measurements the ideality factor of the compensated devices is found to be higher than that of the uncompensated samples. I-V-T measurements on the compensated samples allowed the detection of two main traps which are identified as the possible cause of the larger leakage current in these Te-compensated devices. From C-G-f measurements it was found that the density of interface traps in compensated samples is one order of magnitude higher than in uncompensated samples. Furthermore, the DLTS measurements performed in the forward pulse condition confirms that Te compensated samples have both electron and hole traps present at the interface of GaSb/GaAs. This finding further supports the results reported in Chapter 6 that adding Te at the interface IMF grown devices introduce more interface traps and electrical active defects than in uncompensated samples.

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CHAPTER 9

Deep defects in $Ga_{0.82}In_{0.18}As_{0.16}Sb_{0.84}$/GaAs Photodiodes Grown by Interfacial Misfit Array Molecular Beam Epitaxy Technique

In this chapter the electrical (I-V, C-V and DLTS) and structural (Transmission Electron Microscopy) characterization of GaInAsSb grown on Interfacial Misfit (IMF) GaSb/GaAs are performed. The DLTS measurements on GaInAsSb are employed here for the first time where the defects are characterized by filling pulse time technique. In addition, in order to determine the distribution of defects in the depletion region the Double pulse DLTS (DDLTS) method is used.

9.1 INTRODUCTION

Antimony-based compound semiconductors have attracted considerable attention due to their applications in optoelectronic from the mid-to-far-infrared region [1, 2]. Efficient long-wavelength detectors operating in the wavelength region of 2–2.6 µm have great potential in gas sensing, chemical process monitoring, photovoltaics, and astronomy. The InGaAsSb can be grown on lattice matched GaSb with the composition given by $(GaSb)_{1-z}$ $(InAs_{0.91}Sb_{0.09})_z$ [3]. This enables the cut-off wavelength to be tuned from 1.7 µm to 5 µm. The InGaAsSb material lost its interest due to its disadvantage of growing devices on GaSb substrates. The high quality GaSb wafers are very expensive compared to GaAs and also not commercially available in diameter larger than 4 inches. Furthermore, GaSb substrates are not optically transparent due to strong absorption of mid-infrared

wavelength below the bandgap [4, 5]. Moreover, undoped GaSb has an acceptor concentration of 10^{17} cm^{-3} due to its native defects. Hence GaSb wafers are not available in semi-insulating or high resistivity form. In order to overcome such disadvantages of growing InGaAsSb on GaSb substrates, InGaAsSb material is grown on GaAs substrates [6, 7]. The optically transparent, low cost, high quality and larger wafer size makes GaAs substrates a strong candidate for Sb-based devices. One of the disadvantages of growing GaInAsSb devices on GaAs is the lattice mismatch between the two different materials. However, such mismatch is overcome by growing first GaSb on top of GaAs substrates with Interfacial misfit (IMF) technique as discussed in detail in Chapter 3 and Chapter 6, and is given in reference [8]. K. C. Nunna et al [9] studied the p^+-i-n^+ InGaAsSb photodetectors grown on top of IMF GaSb/GaAs. The observed photoresponse of InGaAsSb detectors was 2.2 µm and it was concluded that the observed responsivity and detectivity is comparable to similar detectors grown on the native GaSb substrates. However, the presence of non-radiative recombination centers in the bandgap could seriously affect the performance of such photo-diodes. The motivation of this work is to study for the first time such non-radiative recombination traps by using the powerful DLTS technique in similar photodiodes which were studied by K. C. Nunna et al [9].

9.2 RESULTS AND DISCUSSIONS

9.2.1 I-V AND C-V MEASUREMENTS

The I-V measurements are performed at different temperatures on both InGaAsSb samples grown on uncompensated (Figure 9.1) and compensated IMF (Figure 9.2) GaSb/GaAs templates.

For the uncompensated samples the forward bias I-V characteristics are linear on a semi-logarithmic scale at low forward bias voltages (0-0.3V) as shown in Figure 9.1. However, when the applied forward voltage is increased (> 0.3V) the I-V curves deviates substantially from linearity due to the effect of series resistance.

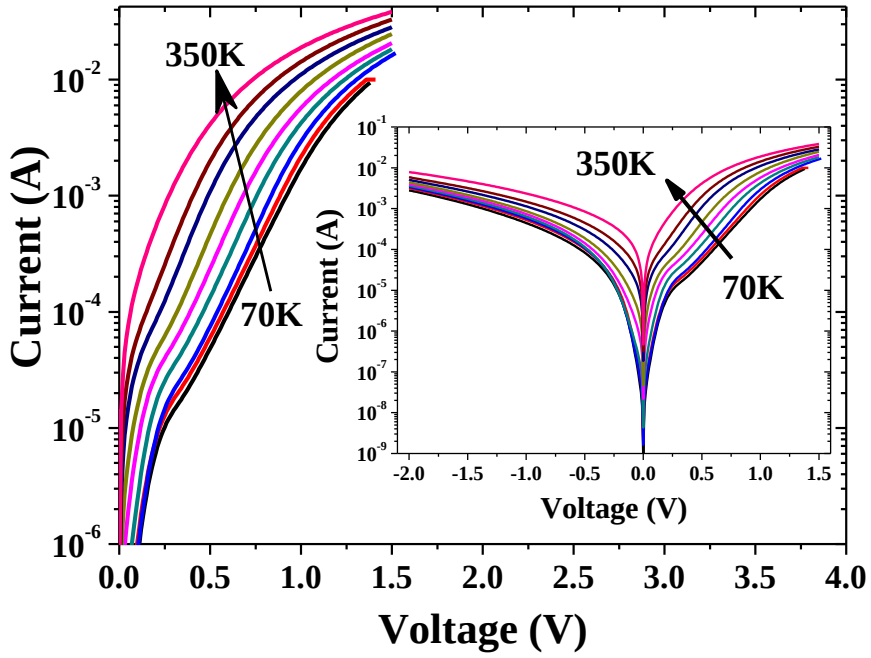


Figure 9.1: Semi-logarithmic forward I-V plot of InGaAsSb on uncompensated GaSb/GaAs in the temperature range of 70–350 K at 30 K intervals. The inset shows semi-logarithmic plots in the forward and reverse I-V characteristics at different temperatures.

Similar I-V measurements at a range of temperatures are also performed on InGaAsSb grown on Te-compensated IMF GaSb/GaAs/ samples as shown in Figure 9.2. However, a negative differential resistance (decrease in the forward current as the voltage is increased) is observed from 20K to 190K.This behaviour is observed in p-n junctions when electrons tunnel from the n-type side to the p-type side of the diode as shown in the inset of Figure 9.2. This effect is also observed in tunnel or Esaki diodes. When the applied forward voltage varies from ~ 0.1 – 0.35 V, a large tunneling current passes through the interface. When the forward voltage is further increased from 0.4 – 0.5 V, the tunneling current vanishes. According to Dashiell et al [10] the current at/and beyond the valley voltage, referred to as the excess current, was shown to be due to tunneling through defect levels in the forbidden energy gap up to a voltage where the thermal current begins to dominate, i.e. diffusion or recombination. The schematic diagram for the generation of peak current (I_P), valley current (I_V) and current through normal diode (I_{diode}) are shown in the inset of Figure 9.2. The two important figures of merit of tunnel diodes are the peak to valley current ratio (PVCR) and the peak current (I_P). Table 9.1 lists the peak and valley current and their PVCR. From this Table and Figure 9.2, the PVCR of the device decreases with temperature in the range 20K to 190K, and the tunnelling current vanishes for temperatures > 190 K. This behaviour is probably due to the thermally activated current which dominates due diffusion or recombination process.

The Te atoms used compensate the dangling bonds formed during IMF, create defects at the interface, and thus contribute to the tunnelling current at temperatures lower than 190 K.

Table 9.1 : lists of peak and valley current and their PVCR of compensated InGaAsSb samples.

Temperature (K)	I_p (A) x10^{-5}	I_v (A) x10^{-5}	PVCR
70	2.94	2.42	1.21
100	3.69	3.16	1.17
130	4.5	4.04	1.11
160	5.70	5.43	1.05
190	7.14	7.09	1.01

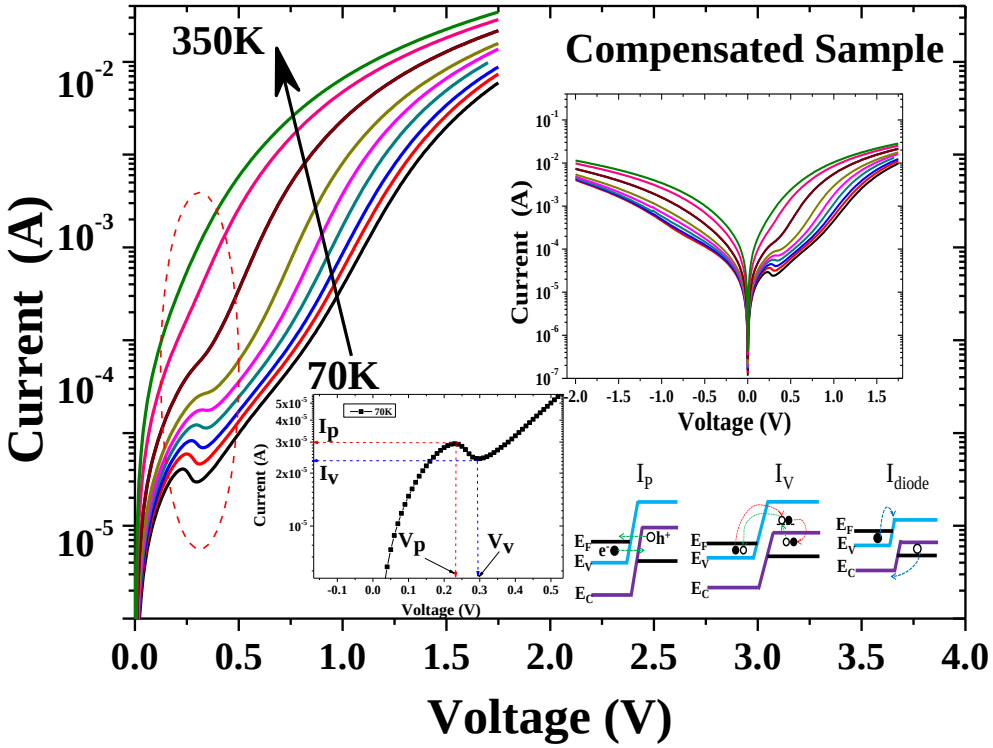


Figure 9.2: Semi-logarithmic I-V plots of InGaAsSb on Te-compensated GaSb/GaAs in the temperature range of 70–350 K at 30 K intervals. The inset shows semi-logarithmic plots in the forward and reverse I-V characteristics at different temperatures and schematic representation of current flow from pn junction.

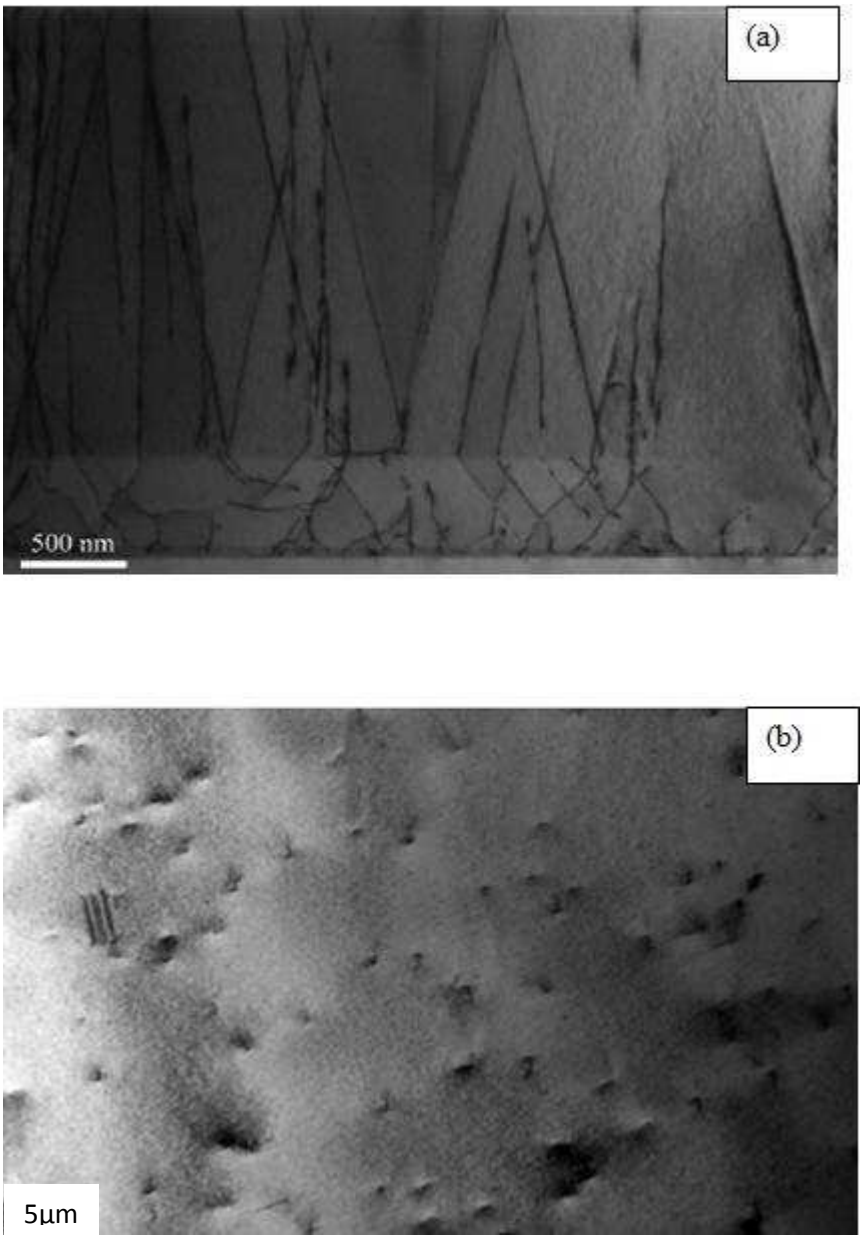


Figure 9.3: (a) Cross-section TEM image of $Ga_{(x)\ 0.82}In_{\ (1-x)\ 0.18}As_{(y)\ 0.16}Sb_{(1-y)0.84}$ showing threading dislocations in the active region of the devices (b) plan view TEM image of $Ga_{(x)\ 0.82}In_{\ (1-x)\ 0.18}As_{(y)\ 0.16}Sb_{(1-y)0.84}$ [courtesy of Dr. S.L. Tan (Sheffield University) who also provided these samples for electrical characterization]

The structural analysis is performed by using Transmission Electron Microscopy (TEM). Figure 9.3a shows TEM cross-section view where it can be seen that the

threading dislocations are originating from GaSb/GaAs/ and propagate into the active region of the GaInAsSb layer. However, only few of the threading dislocations reach the top surface of the samples as shown in Figure 9.3 (b). It can be confirmed that threading dislocations are the cause of such high values of reverse currents in both samples as shown in Figures 9.1 and 9.2.

The C-V measurements are performed on both samples and the doping concentrations are determined from the plot of $1/C^2$ versus V as shown in Figure 9.4.

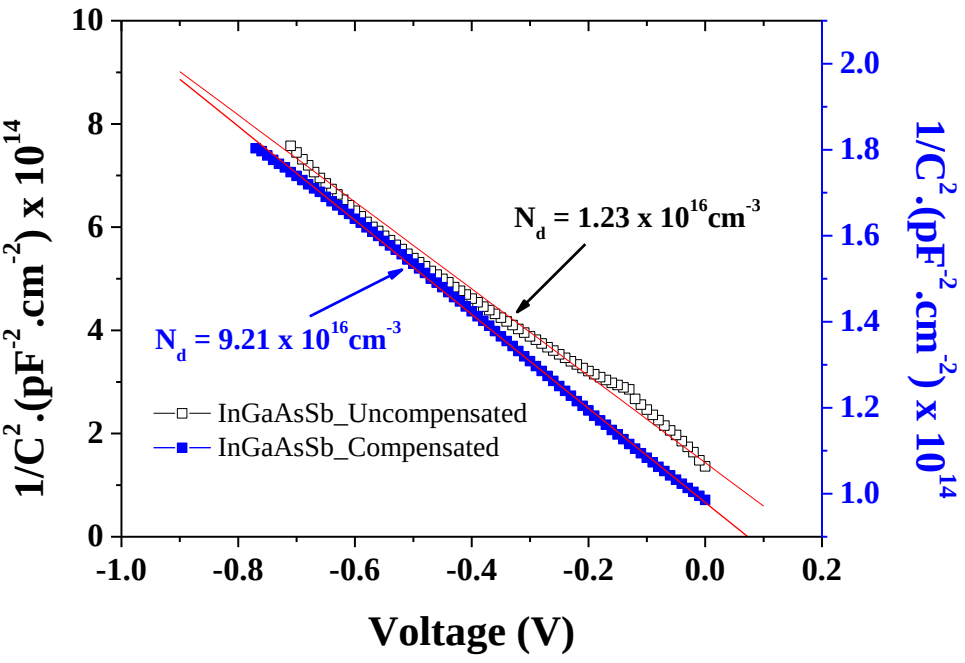


Figure 9.4: Plots of $1/C^2$ versus V of GaInAsSb layers grown on uncompensated IMF GaSb/GaAs and Te compensated IMF GaSb/GaAs structures. Background doping concentrations are extracted in order to determine trap concentration detected by DLTS measurements.

The undoped GaInAsSb regions are found to be p-type with a doping concentration of 1.23 x 10^{16} cm^{-3} and 9.21 x 10^{16} cm^{-3} for uncompensated and Te

compensated samples, respectively. This doping concentration is in agreement with the findings of K. C. Nunna at al [9] who reported doping concentrations on the same batches of samples as 2 x 10^{16} cm^{-3} in uncompensated GaInAsSb samples.

9.2.2 DLTS MEASUREMENTS

DLTS measurements are used to characterize the electrically active defects in p^+-i- n^+ InGbAsSb devices. The experimental conditions used are as follows: V_R= -1V, V_P= 0V and t_p= 1msec. Figure 9.5 shows the DLTS spectra for InGbAsSb grown on uncompensated and Te-compensated IMF GaAs/GaSb samples.

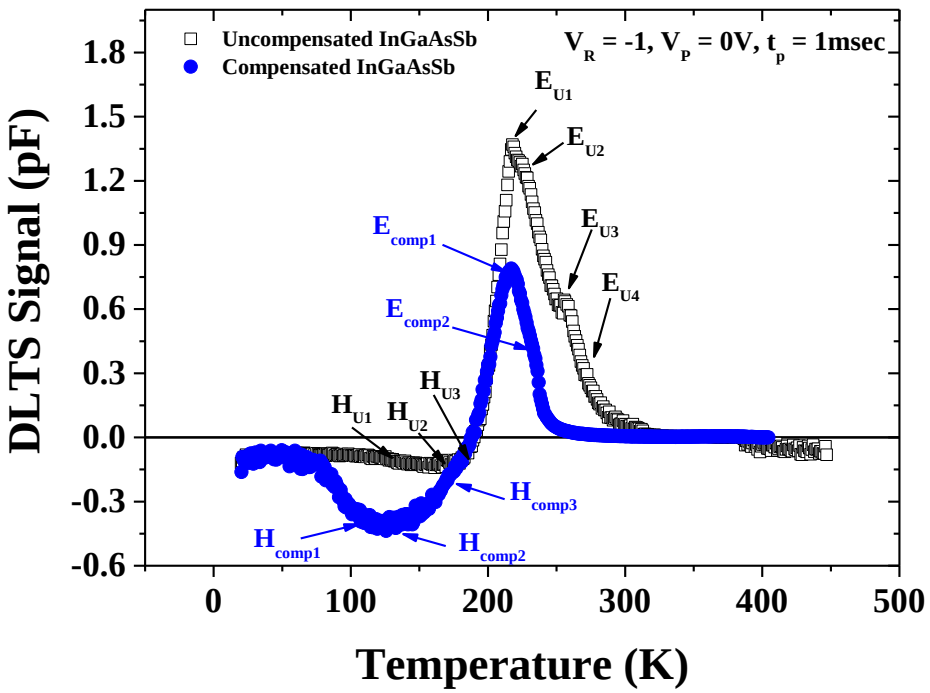
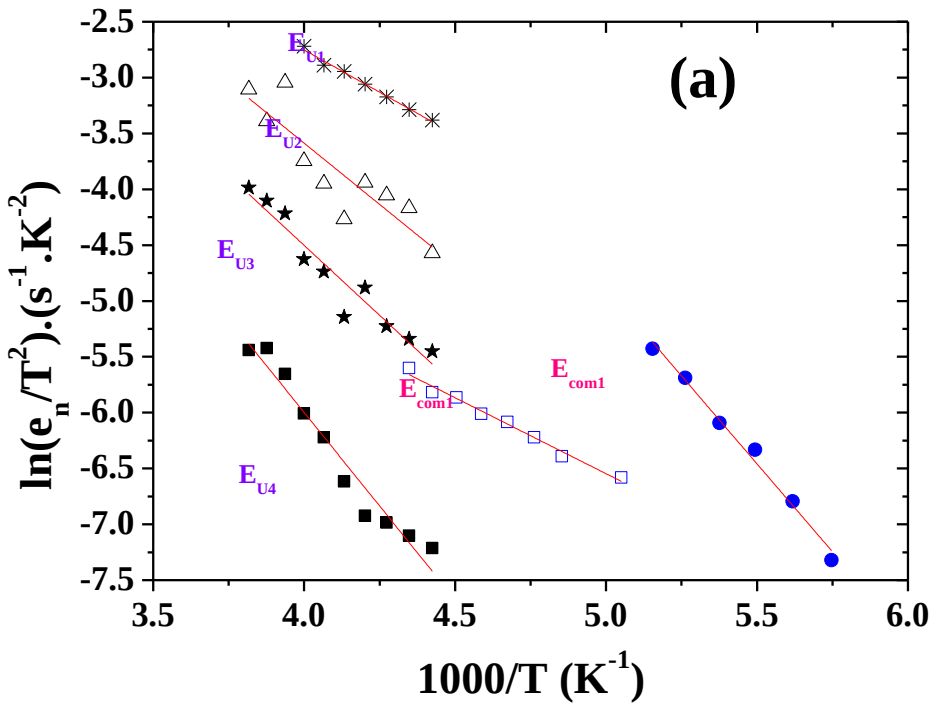
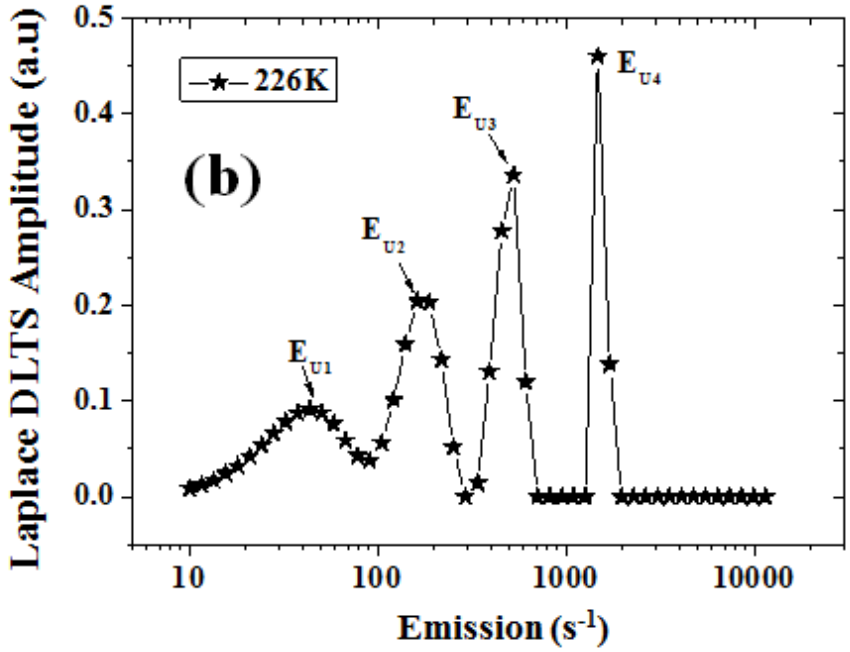


Figure 9.5**:** Conventional DLTS measurements of InGaAsSb grown on Interfacial Misfit (IMF) uncompensated and Te compensated GaAs/GaSb layers. The DLTS experiment conditions are as follows: reverse bias V_R = - 1V, filling pulse V_p = 0V, t_p = 1msec, and rate window= 100 s^{-1}.

It can be seen from Figure 9.5 that broader electron and hole peaks are detected in both samples. In order to resolve these peaks, Laplace DLTS is employed in the temperature range where the DLTS peaks appear. Figure 9.6a shows the Arrhenius plots of uncompensated and Te compensated InGbAsSb samples extracted from Laplace DLTS measurements. Four electron defects, namely, E_{U1}, E_{U2}, E_{U3} and E_{U4} are detected by Laplace DLTS (Laplace peaks are shown in Figure 9.6b) in uncompensated samples in the temperature range ~190K-300K. On the other hand two electron peaks E_{com1} and E_{com2} are detected in compensated samples in the temperature region of ~190K-250K by Laplace DLTS (Laplace peaks are shown in Figure 9.6c).





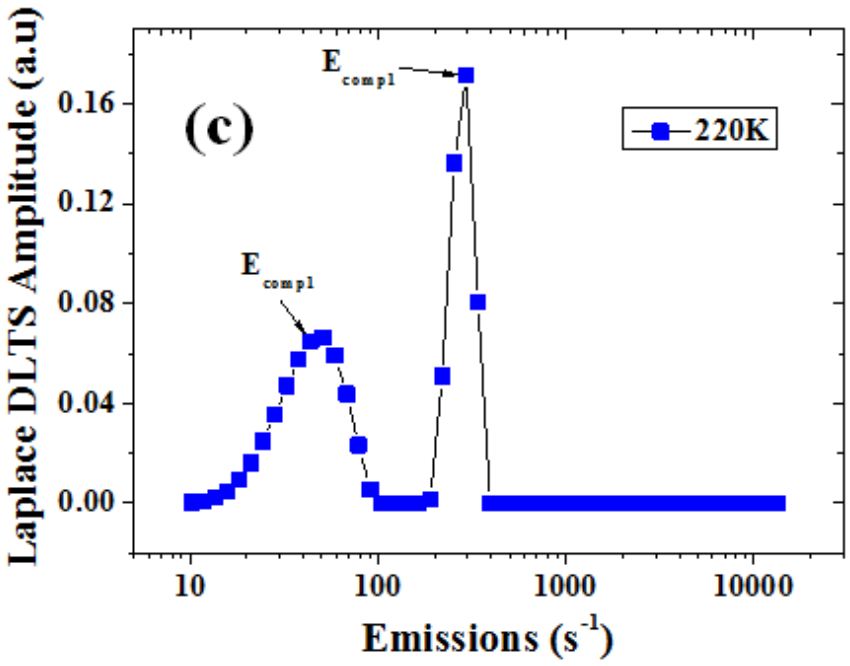


Figure 9.6: (a) Arrhenius plots of electron traps in InGaAsSb layers deposited on uncompensated and compensated IMF GaAs/GaAs for a reverse bias V_R = -1V, (b) show prominent Laplace peaks for uncompensated sample and (c) compensated sample.

The activation energies, capture cross-sections and traps concentrations are calculated and summarized in Table 9.1. Two of the defects E_{U1}, E_{U4} and E_{com1}, E_{com2} in the uncompensated and Te-compensated samples, respectively, have exactly the same activation energies (E_{U1}/E_{com1}= 0.13 ± 0.01 eV and E_{U4}/ E_{com2} = 0.27 ± 0.01 eV). It is well known that in MBE as well as MOCVD undoped GaInAsSb layers have a p-type background character (~$1x10^{16}$ cm^{-3}) which has been attributed to the formation of native defects and not impurities [11]. The i-region of the n^+-i-p^+ structures investigated in this thesis are in fact n^+-p-p^+. Therefore the depletion region will form between the n+ and p regions. For a small reverse bias the depletion will be closer to the p-region. As reported by M. J. Cohen et al [11] the InGaAsSb p-region contains native defects which could be related to the standard defects such as V_{Ga}, Ga_{Sb}, Sb_{Ga}, V_{Ga}-Ga_{Sb} etc. In the following the defects that have already been reported will be discussed first before commenting on the defects that are detected in this study.

I. Riech et al [12] studied n and p type GaInAsSb epilayers grown on n and p type GaSb substrates. They found that Te atoms used for n-type doping affect the morphology at the interface between the epilayer and the n-type substrate. However, the interface between the p-type GaInAsSb layer and the n-type GaSb substrates was unaffected. The interface roughness, as confirmed by Atomic Force Microscopy (AFM), was attributed to diffusion of Te atoms towards the interface. T. I. Voronina et al [13] studied the temperature dependence of the Hall coefficient, the conductivity, the mobility, and photoconductivity of InGaAsSb grown by Liquid-Phase Epitaxy (LPE). They reported acceptor levels in GaInAsSb having energies of 8 meV, 30 meV and 70 meV. They attributed them to similar acceptor levels present as native defects in GaSb. Furthermore, they

also studied the role of Te in GaInAsSb and observed that Te creates two acceptor defects in GaInAsSb, having energies E_{A4}= 0.1eV and E_{A2}= 0.38 eV. They assigned E_{A2} to a structural defect, and E_{A4} to the diffusion of Te from the Te-doped GaSb substrate to form a complex with Gallium vacancy (V_{Ga}Te). The electrical properties on GaInAsSb [14] show that Te in GaInAsSb has two roles. Firstly it creates shallow donor levels, and secondly it interacts with native acceptor defects having energies 35 meV and 70 meV to create (V_{Ga}Te) complex with an activation energy of 0.1 eV.

Electroluminescence (EL) spectra of n-InGaAsSb/p-GaSb heterostructures emitting in the region of 2–2.5 µm were studied by T. I. Voronina et al [15] at T = 77 K and 300 K. The EL spectra exhibit a number of peaks corresponding to recombination mechanisms that involve interband transitions and various levels. The two EL spectra at λ = 2.35 µm and λ = 2.24 µm are related to the interband recombination centers. The peaks due to recombination level E_{A2} = 0.035 eV at λ = 2.35 µm and E_{A3} = 0.07 eV at λ = 2.24 µm are due to first and second charge states of $V_{Ga}Ga_{Sb}$, respectively.

The current transfer mechanism was studied in p-GaSb/p-GaInAsSb/n-GaAlAsSb heterojunctions with p-type GaInAsSb as an active region [16]. The I-V and C-V analysis performed on devices in the temperature range of 10–360 K, indicate that the current transport through the devices can be accounted for by three different mechanisms, namely, diffusion, generation and tunnelling. The diffusion current is the dominant component at high temperatures (230 K–360 K). At intermediate temperatures (160 K-230 K), the current is influenced by the mid-gap generation centre, originating from GaInAsSb, with activation energy 0.26 eV as determined

from I-V measurements. The low temperature (≤150K) current was dominated by the tunnelling mechanism.

The study of electrically active defects in GaInAsSb is performed here for the first time. It certainly would not be possible to comment on the nature of these defects at the present without further studies using different defect characterization techniques. However, advanced experiments are performed by using double pulse DLTS (DDLTS) and filling pulse DLTS techniques to identify the nature of the detected defects (i.e. differentiate between point defects and extended defects). In DDLTS measurements, two pulses are applied having the same reverse bias (V_R) and changing the ratio of V_{P1} and V_{P2}. In this way the whole region of the junction is scanned and the defects concentration depth profiles are determined. Figure 9.7 represents the depth profiling of the detected electron peaks in both samples. In the InGaAsSb samples grown on uncompensated IMF GaSb/GaAs, it can be seen from Figure 9.7 that traps E_{U1}, E_{U2} and E_{U3} have a similar concentration profiles, where the traps concentration first increases then decreases. On the other hand the defect E_{U4} concentration shows a decreasing trend.

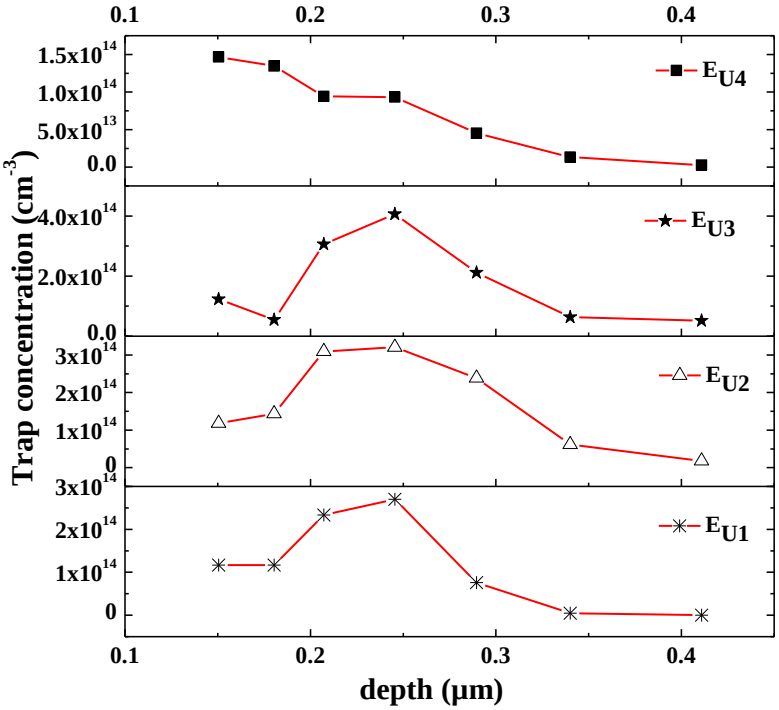


Figure 9.7**:** Traps concentration versus depth of InGaAsSb sample grown on uncompensated GaSb/GaAs IMF. The junction is formed between n^+ InGaAsSb-p InGaAsSb and major contribution of defects (depth profiling) is detected from intrinsic (p) region of InGaAsSb.

The distribution profiles suggest that all these traps could be related to defects near the interface of the n^+-p region of GaInAsSb since their concentrations decrease away from the interface.

In GaInAsSb grown on Te-compensated IMF samples the distributions of both traps E_{comp1} and E_{comp2} have different behaviour as shown in Figure 9.8. The E_{comp1} trap distribution has a peak close to the interface and decreases away from the interface region. On the other hand the E_{comp2} trap distribution strongly increases from ~ 8 x 10^{13} cm^{-3} to ~5x 10^{14} cm^{-3} away from the interface. This could be due to the presence of Te atoms at the IMF of GaSb/GaAs where

diffusion from heavily doped n+ cladding layer to the unintentionally doped GaInAsSb is further enhanced. This effect could also be related to the C-V characteristics where the doping concentration of GaInAsSb samples grown on Te doped IMF is ~ one order of magnitude higher than GaInAsSb samples grown on uncompensated IMF. The incorporation of Te in GaInAsSb shifted the Fermi energy towards the conduction band as the Te (acting as donor) concentration increases [17]. The detected donor defects in the GaInAsSb samples investigated in this thesis could be related to complexes involving Te atoms, due to diffusion from the n^+ contact layer. However, it is difficult to determine the exact nature of these defects as in-depth characterization of the electrical/optical/structural of GaInAsSb is required.

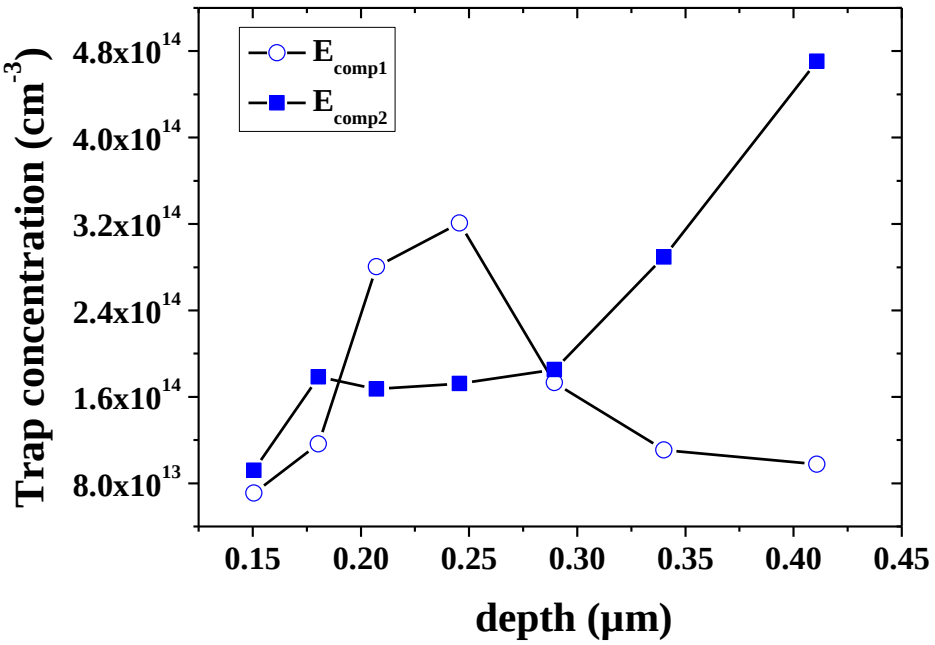
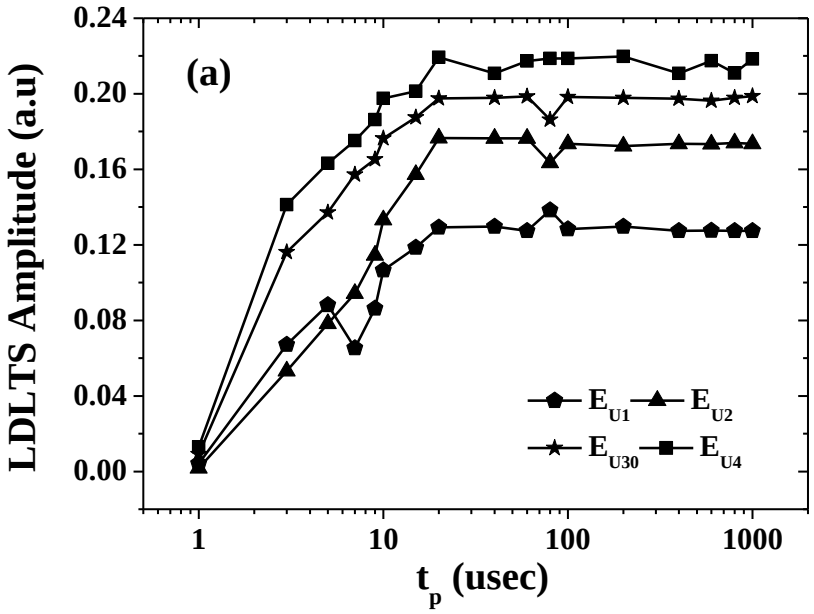
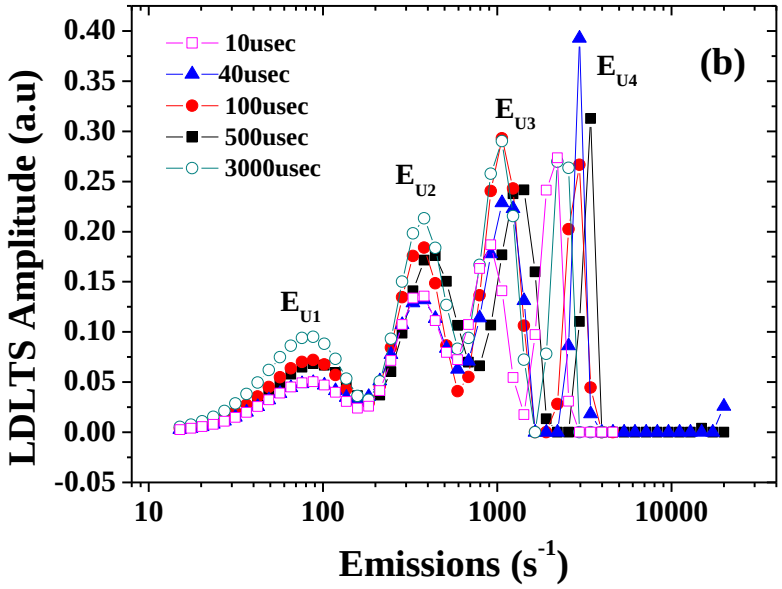


Figure 9.8**:** Traps concentration versus depth of InGaAsSb sample grown on Te-compensated IMF. The junction is formed between n^+ InGaAsSb- p InGaAsSb and major contribution of defects (depth profiling) is detected from intrinsic (p) region of InGaAsSb.

In order to differentiate between point defect and extended defect, measurements using the filling pulse technique [18] are performed by changing the filling pulse time from 1μsec to 5msec. A point defect is formed when an atom replace another atom, or when an atom is missing from the crystal structure. Examples of such point defects include impurities, vacancies, interstitials, or their clusters. In contrast to point defects, spatially extended defects form deep lying closely spaced electronic states in the band gap. Dislocations, grain boundaries, precipitates, and surface and interface states are examples of extended defects [18]. Extended defects, which can interact with point defects, could create adverse effects in microelectronic devices. Such extended or point defects can be studied by using the filling pulse DLTS technique [18]. Point and extended defects can be distinguished by plotting the DLTS signal amplitude as function of filling pulse time (t_p). Point defects show exponential capture kinetics, while extended defects show logarithmic capture kinetics. The filling pulse experiments are performed on GaInAsSb grown on uncompensated and Te-compensated samples as shown in Figure 9.9 (a) and Figure 9.9 (c), respectively. It can be seen from Figures 9.9 (b) and (d) that all electron traps (E_{U1}, E_{U2}, E_{U3} and E_{U4} in uncompensated samples and E_{comp1} and E_{comp2} in compensated samples) show a saturation of amplitude as a function of filling pulse time t_p, which are the characteristic of point defects.


(a)
LDLTS Amplitude (a.u)
0.24
0.20
0.16
0.12
0.08
0.04
0.00
1
10
100
1000
t_p (usec)
E_U1
E_U2
E_U30
E_U4


(b)
LDLTS Amplitude (a.u)
0.40
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0.00
-0.05
10
100
1000
10000
Emissions (s^-1)
10usec
40usec
100usec
500usec
3000usec
E_U1
E_U2
E_U3
E_U4

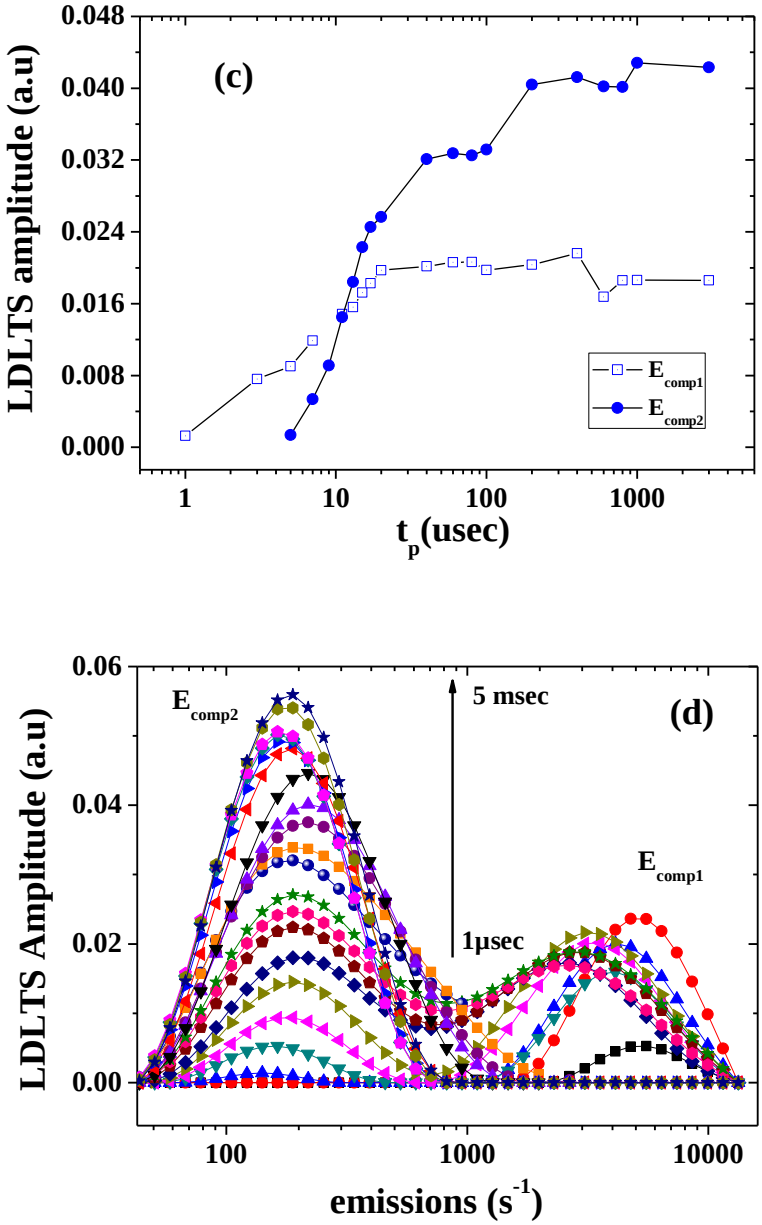


Figure 9.9: (a) log t_p versus Laplace DLTS amplitude uncompensated sample, (b) Laplace DLTS peaks at different filling pulse durations for uncompensated sample (c) log t_p versus Laplace DLTS amplitude compensated samples and (d) Laplace DLTS peaks at different filling pulse durations for compensated sample. Exponential behavior confirming point defects at reverse bias voltage V_R = -1V, V_p = 0V and varying the filling pulse time, t_p from 1µsec to 5msec

The hole peaks observed in both samples in the temperature range ~ 90K to 180K for uncompensated and compensated samples are shown in Figure 9.5. The Laplace DLTS measurements are performed to resolve these broad hole peaks. The activation energies are calculated by using Arrhenius plots as shown in Figure 9.10.

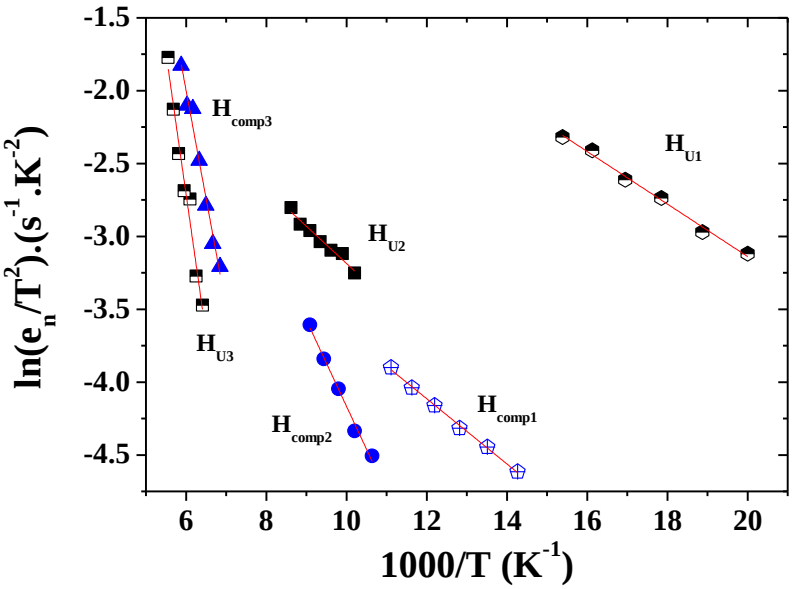
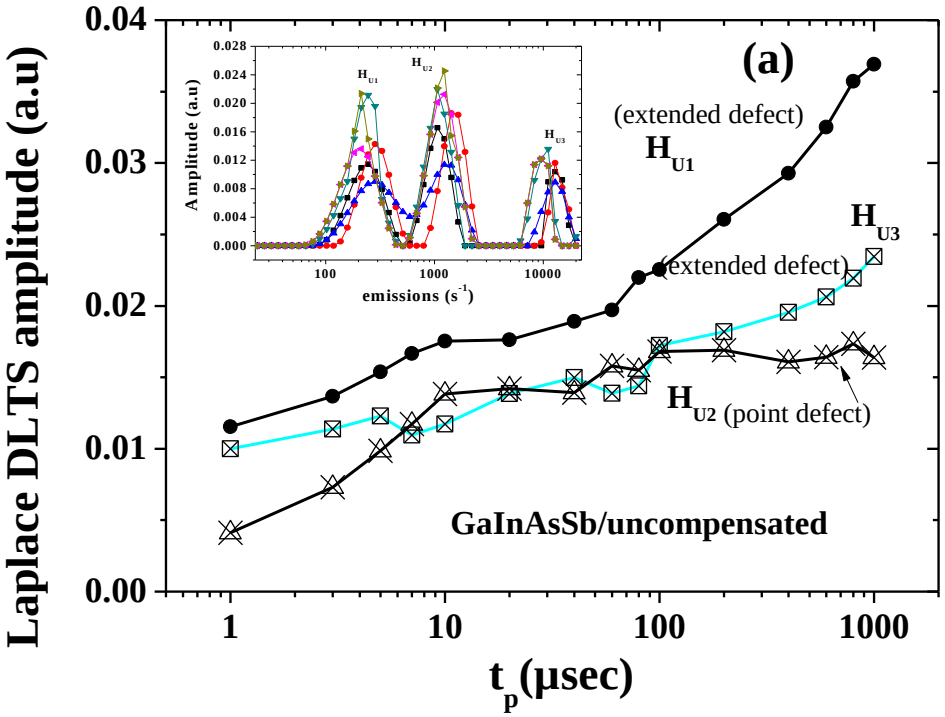


Figure 9.10: Arrhenius plots of hole traps in InGaAsSb samples grown on uncompensated and compensated IMF GaSb/GaAs at reverse bias V_R = -1V.

The calculated values of the activation energies, capture cross-sections and traps concentration of these hole traps in both samples are summarized in Table 9.2. The three hole traps H_{U1}, H_{U2} and H_{U3} having activation energies 0.016 ± 0.003 eV, 0.028 ± 0.002 eV and 0.12 ± 0.01 eV are detected in GaInAsSb grown on uncompensated IMF. Similarly three hole traps with activation energies 0.020 ± 0.001 eV, 0.050 ± 0.004 eV and 0.16 ± 0.01 eV are observed in GaInAsSb grown on Te compensated IMF. Previous studies on GaInAsSb materials suggested that the native defects such as V_{Ga}, Ga_{Sb} and V_{Ga}-Ga_{Sb} are most commonly observed

defects in this material [11, 15, 19]. As reported by many researchers, the most common amongst these native defects in GaInAsSb is V_{Ga}-Ga_{Sb} which has an activation energy of 0.035 meV. Here it is also concluded that H_{U2} (0.028 ± 0.002 eV) and H_{comp2} (0.050 ± 0.004 eV) having energies close to 0.035 meV could therefore be assigned to V_{Ga}-Ga_{Sb} defect [15, 19]. The defect H_{comp2} could also be attributed to the second charge states of V_{Ga}-Ga_{Sb} defect with activation energy of 0.070 meV as reported by T. I. Voronina et al [15]. T. I. Voronina et al [13] reported several acceptor levels in GaInAsSb having energies 8 meV, 30 meV and 70 meV, which they attributed to native defects in GaInAsSb. However they did not discuss the origin of any of these defects. Defect H_{U3} in uncompensated GaInAsSb having activation energy of 0.11 eV could be related to V_{Ga}-Te. A similar energy defect was observed by A. N. Baranov [19] and T. I. Voronina et al [13] and they assigned this defect to the diffusion of Te atoms forming a complex structural defect involving V_{Ga} (V_{Ga}-Te). In order to shed some light on the origin of the hole defects present in the investigated samples in this thesis, the filling pulse DLTS measurements are used. Figure 9.11 shows the filling pulse measurements for uncompensated and compensated samples. It is interesting to note in Figure 9.11 (a) that two of the defects H_{U1} and H_{U3} show logarithmic behavior which is evidence of extended defects. In addition, H_{U3} can be assigned to the structural defect V_{Ga}-Te because of similar activation energies. However, the origin of defect H_{U1} is not clear but could possibly originate from threading dislocations created between GaSb/GaAs. These threading dislocation are also observed by TEM as discussed in Figure 9.3. The other defect H_{U2} shows exponential behavior which is confirmation of a point defect due possibly to a native defect, however, its exact origin is unclear.

Similar measurements on compensated GaInAsSb samples are shown in Figure 9.11 (b). The defects H_{comp1} and H_{comp2} show exponential behavior (point defects) while the defect H_{comp3} shows logarithmic behavior (extended defect). The defect H_{comp3} could also have a dislocation related origin. However, there are two dislocation inducted defects in uncompensated samples while only one is present in compensated samples. This could be related to the compensation of dangling bonds at the interface of GaSb/GaAs, since Te is introduced to compensate the dangling bonds. These dangling bonds are considered as a source of threading dislocations in GaSb/GaAs IMF devices [20].



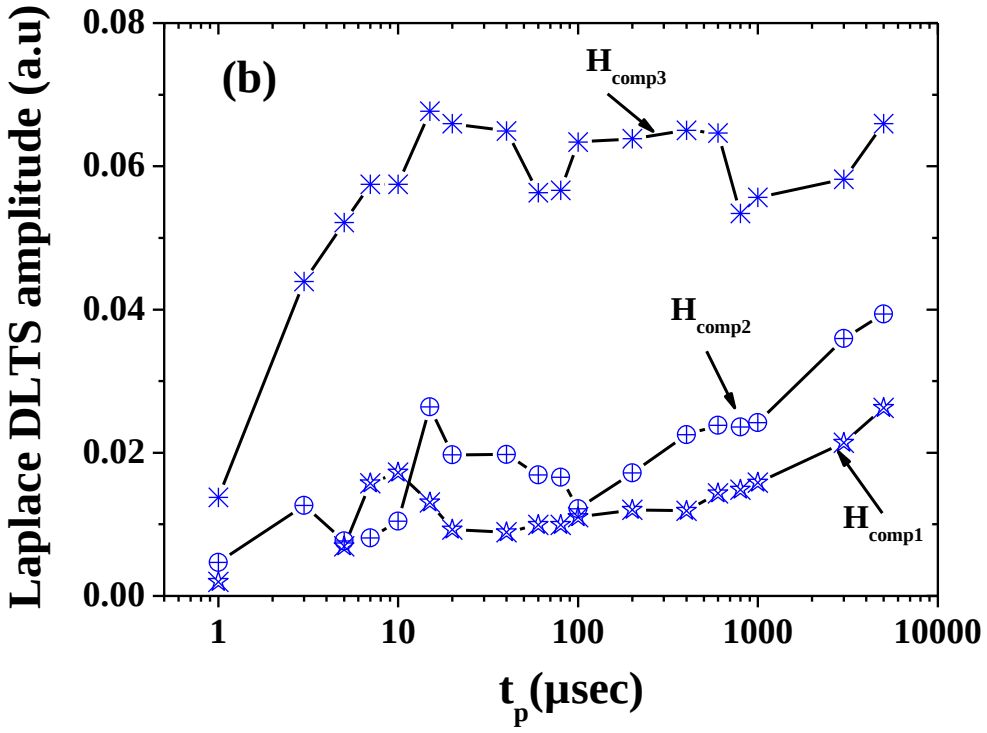


Figure 9.11**:** log "t_p" versus Laplace DLTS amplitude of hole traps in InGaAsSb grown on (a) uncompensated and (b) compensated GaSb/GaAs templates.

Table 9.2: Summary of defects activation energies, capture cross-sections and trap concentrations for GaInAsSb grown on uncompensated and Te compensated IMF GaSb/GaAs

Sample Name	Trap Name	E_T (eV)	Capture cross-section σ(cm^{-2})	Trap Concentration (cm^{-3})
InGaAsSb Uncompensated IMF	E_{u1}	0.130 ± 0.002	6.79×10^{-19}	7.47×10^{14}
	E_{u2}	0.19 ± 0.02	4.40×10^{-18}	8.74×10^{14}
	E_{u3}	0.22 ± 0.01	6.14×10^{-18}	8.03×10^{14}
	E_{u4}	0.29 ± 0.01	4.04×10^{-17}	5.47×10^{14}
	H_{u1}	0.016 ± 0.003	1.79×10^{-21}	7.47×10^{14}
	H_{u2}	0.028 ± 0.002	1.05×10^{-21}	7.07×10^{14}
	H_{u3}	0.12 ± 0.01	7.81×10^{-18}	6.16×10^{14}
InGaAsSb Compensated IMF	E_{comp1}	0.13 ± 0.01	5.63×10^{-20}	1.24×10^{15}
	E_{comp2}	0.27±0.01	1.26×10^{-15}	1.89×10^{15}
	H_{comp1}	0.020 ± 0.001	2.69×10^{-22}	2.50×10^{13}
	H_{comp2}	0.050 ± 0.004	1.68×10^{-21}	2.28×10^{13}
	H_{comp3}	0.16 ± 0.01	3.25×10^{-17}	2.53×10^{13}

9.3 CONCLUSION

In summary DLTS measurements are performed on GaInAsSb epilayers grown on IMF GaSb/GaAs uncompensated and Te compensated samples. The TEM images show threading dislocations starting from GaSb/GaAs interface and propagating towards the GaInAsSb epilayer. Both electron and hole defects are detected and some of these could originate from native defects in GaInAsSb. The filling pulse DLTS measurements confirm two structural defects in uncompensated GaInAsSb and one structural defect in compensated GaInAsSb samples. As reported in the literature it is believed through structural studies that the incorporation of Te atoms at the GaSb/GaAs interface act as compensation of the dangling bonds and therefore reducing structural defects and dislocations. However, the findings reported in this thesis confirm that the incorporation of Te introduces electrically active defects which could have adverse effects in devices.

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CHAPTER 10

CONCLUSION AND FUTURE WORK

The research carried out on GaSb/GaAs IMF samples are summarised in this chapter. The future direction of characterization on these Interfacial Misfit grown samples is also discussed. The defect characterization techniques such as DLTS, I-V, C-V, C-F and G-F are performed to study electrically active defects near to the interfaces and their influences away from the interfaces of GaSb/GaAs heterostructures.

10.1 CONCLUSION

10.1.1 INTERFACIAL MISFIT GaSb/GaAs UNCOMPENSATED AND Te-COMPENSATED SAMPLES

The electrically active defects are studied in uncompensated and Te compensated samples. The I-V measurements show lower value of turn on voltage (V_{on}) and higher reverse currents in Te compensated samples. The C-V analysis confirms the higher value of interface capacitance in Te compensated samples compared to the uncompensated samples. The C-F measurements also confirmed the role of interface states in Te compensated devices compared to the uncompensated devices. Furthermore, DLTS measurements detected a common deep level defect which was assigned to the well-known EL2 defect in GaAs. This is the only deep level which was detected in uncompensated GaSb/GaAs samples near to the interface. On the other hand in Te compensated samples six additional electron

defects are observed. These are thought to be related to the incorporation of Te-atoms which are used to compensate the dangling bonds. Hence, the role of Te as a delta dopant makes such devices electrically worse by creating more defects at interfaces and away from the interfaces.

10.1.2 EFFECT OF ANNEALING ON IMF GaSb/GaAs UNCOMPENSATED AND Te COMPENSATED SAMPLES

In order to improve the quality of the devices a heat treatment is performed. The rapid thermal annealing is carried out on all uncompensated GaSb/GaAs samples at three different temperatures 400 ^{o}C, 500 ^{o}C and 600 ^{o}C for 2 minutes. On the other hand rapid thermal annealing and furnace annealing treatments are performed on Te compensated GaAs/GaSb samples at 400 ^{o}C for 2 minutes. The I-V measurements on annealed uncompensated samples reveal dramatic improvements in terms of reverse currents with the increase of the annealing temperature. It was also noticed that the reverse currents in all annealed uncompensated devices are smaller than those in as-grown uncompensated devices. Furthermore, C-V analysis on all uncompensated annealed devices shows negligible effect of interface states. This observation confirms that rapid thermal annealing treatment has a large effect on the reduction of interface states in the uncompensated samples. The C-F measurements further confirm lower effect of interface states after rapid thermal annealing treatment on uncompensated samples. The DLTS measurements carried out close to the interface of uncompensated GaSb/GaAs samples confirm one common deep defect EL2 in as-grown, and 400 ^{o}C and 500 ^{o}C annealed devices. On the other hand the dissociation from EL2 to EL3 is observed at 600 ^{o}C in uncompensated devices

with a much lower concentration than EL2. The observed values of reverse currents are much smaller in 600 ^{o}C annealed devices compared to as-grown and 400 ^{o}C and 500 ^{o}C annealed devices. This is an evidence of the large contribution of EL2 to the reverse leakage current observed in the devices. The I-V measurements showed that as-grown and rapid thermal annealed Te-compensated samples exhibit lower values of reverse currents than the furnace annealed devices. The non-linearity observed in C-V analysis confirms the presence of interface states in as-grown and annealed devices. The DLTS measurements detected additional hole traps near the interfaces in furnace annealed samples. The concentration of electron defects detected by DLTS in rapid thermal annealed samples is lower than as-grown and furnace annealed samples. This finding also confirms that rapid thermal annealing treatment is more effective in terms of reducing electrically active defects in devices.

10.1.3 INTERFACE STATES IN IMF GaSb/GaAs UNCOMPENSATED AND Te COMPENSATED SAMPLES BY ADMITTACE SPECTROSCOPY MEASUREMENTS

The I-V characteristics obtained at a range of temperatures allowed the determination of the ideality factor and barrier height of the GaSb/GaAs heterostructures. It was observed that the ideality factor is higher in Te compensated samples which confirms that these samples are not ideal diode. It is found that the density of interface states calculated from C-F measurements is one order of magnitude higher in Te compensated samples compared to uncompensated samples. Furthermore, resistance-frequency (R-F) measurements also confirm that interface states in Te compensated samples play a dominant

role. The DLTS measurements at forward bias detected two electron traps in uncompensated samples, while in Te compensated samples both electrons and holes are observed near the interfaces of GaSb/GaAs. These studies also confirm that adverse electrical activity occurs after the incorporation of Te at the interface of GaSb/GaAs.

10.1.4 DLTS MEASUREMENTS ON N-I-P GaInAsSb DEVICES GROWN ON IMF GaSb/GaAs

The I-V, C-V and DLTS measurements are performed for the first time on p^+-i-n^+ GaInAsSb devices grown on IMF uncompensated and Te compensated structures. The I-V measurements carried out at a range of temperatures demonstrate standard diode behavior in GaInAsSb devices grown on uncompensated GaSb/GaAs. On the other hand a negative differential resistance is observed in the forward bias region of GaInAsSb grown on Te compensated GaSb/GaAs devices. The DLTS and Laplace DLTS studies show four electron and two electron traps in uncompensated and Te compensated devices, respectively. The origin of all the observed defects are not clear but one deep level defect common in both samples having energy of 0.26 eV could originate from GaInAsSb. This defect is the main contributor to the reverse current of the devices. In addition, four hole traps are also detected in both samples at the same reverse bias conditions. The filling pulse DLTS measurements confirm two and one structural defects in uncompensated and compensated GaInAsSb, respectively. The role of Te is considered as a compensation mechanism of the dangling bonds that are created at the interfaces, and these studies confirm that one of the positive role of Te incorporation is the reduction of dangling bonds since there is only one extended

defect in compensated samples as compared to two extended defects in uncompensated samples.

10.2 FUTURE WORK SUGGESTIONS

The growth technique of Interfacial Misfit is very promising in terms of material cost and reducing the mismatch in lattice mismatched heterostructures. However, there are many challenges that need to be addressed some of which are given in the following:

1. The electrically active defects studied in this thesis were present in samples where the IMF is embedded in the intrinsic region of p-i-n devices. In order to understand the role of IMF it is important to investigate different samples where the IMF could be on one side. For example, a device including an additional p-layer into the n^+i-p^+ structure, i.e. n^+p-i-p^+, where the IMF is away from the depletion layer (i.e. in the intrinsic region). The detailed study carried out in this thesis confirms the adverse role of interdiffusion of Te atoms used to compensate the dangling bonds. It is worth investigating some other dopants with less diffusivity compared to Te to better understand the compensation mechanism.

2. DLTS technique is very sensitive, can detect small concentrations of defects and distinguish between point like defects and extended defects. However, the exact origin of defect states cannot be determined by this technique. It is therefore important to use structural techniques such as X-ray Diffraction (XRD), and high resolution Transmission Electron Microscopy (HRTEM) to correlate the origin of defects to those observed by DLTS.

3. The effect of annealing is also studied in these devices; it will be worth to expand rapid thermal annealing treatments to Te compensated samples having different positions of IMF to investigate the effect of interdiffusion on IMF.
4. A preliminary study of the effect of gamma irradiation on the observed defects in the samples discussed in this thesis was carried out. However, due to lack of samples this study could not be completed. It would be worth studying the effect of different level of gamma irradiations on such IMF devices. This kind of study would be helpful for the use of such materials for device applications in space where irradiation could affect their performances. This will also help to understand the effects of irradiation and the inherent defects.