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# A VECTOR CONTROLLED MATRIX CONVERTER INDUCTION MOTOR DRIVE 

## By

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## 7nativb

Aven.
wry

Thesis submitted to the University of Nottingham
for the degree of Doctor of Philosophy, July, 1995

To My Wife

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## ABSTRACT

This thesis concerns the design and construction of a closed-loop controlled matrix converter induction motor drive, using transputer parallel processors. The modulation algorithms used for the matrix converter are described. A 2.5 kW experimental matrix converter using IGBT switching devices has been constructed and tested. An analysis of the losses in the converter has been carried out and this gives good agreement with the measured losses.

Two modulation algorithms, the Venturini algorithm and the scalar algorithm have been implemented in real-time on a network of parallel transputer processors. Experimental results are presented to compare the operation of these two algorithms. Open-loop constant V/F control of the matrix converter induction motor drive has been demonstrated. A controller has been designed to achieve closed-loop speed control of the drive system, employing the slip regulation technique. The experimental results under various operating conditions have verified the correct operation of both control systems. The indirect vector control technique has also been implemented. The results demonstrate the steady-state and transient performance as well as the regenerative operation of the drive system. The application of a matrix converter to a high performance induction motor servo drive rated at 2.5 kW with true four quadrant capability and minimum passive components has been demonstrated.

## LIST OF SYMBOLS

$f_{i} \quad$ : input frequency
$\mathrm{f}_{\mathrm{o}} \quad$ : output frequency
$\mathrm{f}_{8} \quad:$ switching frequency
$\mathrm{I}_{\mathrm{A}}, \mathrm{I}_{\mathrm{B}}, \mathrm{I}_{\mathrm{C}}:$ instantaneous three phase input currents of the converter
$\mathrm{I}_{a}, \mathrm{I}_{\mathrm{b}}, \mathrm{I}_{\mathrm{c}}:$ instantaneous three phase output currents of the converter
$\mathbf{L}_{i}(\mathbf{t}) \quad$ : input current vector
$\mathrm{I}_{\mathrm{o}}(\mathrm{t}) \quad$ : output current vector
$\mathrm{I}_{\mathrm{om}} \quad$ : maximum output current
$\mathrm{I}_{\mathrm{d}} \quad:$ device current
$I_{s} \quad:$ snubber current
$i_{s a}, i_{s b}, i_{s c}$ : instantaneous three phase stator currents
$i_{s d} i_{s q} \quad$ : stator currents in a synchronously rotating $d-q$ axis frame of reference
$\mathrm{i}_{\mathrm{dd}}, \mathrm{i}_{\mathrm{rq}} \quad$ : rotor currents in a synchronously rotating d - q axis frame of reference
$\mathrm{i}_{\text {ard }} \quad$ : magnetising current
J : momentum of inertia
$\mathrm{L}_{s}, \mathrm{~L}_{\boldsymbol{r}} \quad:$ stator and rotor self inductance
$\mathrm{M}(\mathrm{t}) \quad$ : modulation matrix
m : element of the modulation matrix, $M(t)$
M : stator/rotor mutual inductance
$\mathrm{P}_{\mathrm{c}} \quad$ : conduction loss
$\mathrm{P}_{\mathrm{s}} \quad$ : switching loss
Poff : switching loss at turn-off
$\mathrm{P}_{\text {on }} \quad:$ switching loss at turn-on
$\mathrm{P}_{\text {toss }} \quad:$ total converter loss
$\mathrm{P}_{\mathrm{j}, 1} \quad:$ power loss in the IGBT
$\mathrm{P}_{\mathrm{j}, \mathrm{d}} \quad:$ power loss in the diode
$\mathrm{P}_{\text {snub }} \quad$ : snubber loss

| $\mathrm{P}(\mathrm{t})$ | : instantaneous power dissipation |
| :---: | :---: |
| p | : number of pole pairs |
| q | : voltage ratio of the matrix converter |
| $\mathrm{q}_{\mathrm{m}}$ | : maximum voltage ratio (0.866) |
| R | : snubber resistance |
| $\mathrm{R}_{\mathrm{jc}}$ | : junction to case thermal resistance |
| $\mathrm{R}_{\text {cs }}$ | : case to sink thermal resistance |
| $\mathrm{R}_{2}, \mathrm{R}_{\text {t }}$ | : stator and rotor resistance |
| $\mathrm{S}_{\mathrm{A} a}, \ldots, \mathrm{~S}_{\mathrm{Cc}}$ | : bidirectional switches in the converter |
| s | : Laplace operator |
| S | : differential operator |
| Ts | : sequence time |
| $t_{\text {Aa }}, \ldots, t_{\text {cl }}$ | : on time of the switches in the converter |
| $\mathrm{T}_{\beta \gamma}$ | : duty cycle for the switch connected between the input phase, $\beta$ and output phase, $\gamma$ |
| $\mathrm{t}_{\text {on }}$ | : rise time of the IGBT |
| $\mathrm{t}_{\text {off }}$ | : fall time of the IGBT |
| T | : junction temperature |
| $\mathrm{T}_{\text {amb }}$ | : ambient temperature |
| $\mathrm{T}_{\text {sink }}$ | : sink temperature |
| T | : transputer 1 |
| T | : transputer 2 |
| Te | : electrically developed torque |
| $\tau_{\text {r }}$ | : rotor time constant |
| $\tau$ | : delay time between the drive signals of the devices |
| $\mathrm{V}_{\mathrm{A}}, \mathrm{V}_{\mathrm{B}}, \mathrm{V}_{\mathrm{C}}$ | : instantaneous three phase input voltages of the converter |
| $V_{a}, V_{b}, V_{c}$ | : instantaneous three phase output voltages of the converter |
| $\mathrm{V}_{\mathrm{L}}$ | : rms value of the input line voltage |
| $\mathrm{V}_{\mathrm{im}}$ | : maximum input voltage |
| $\mathrm{V}_{\text {imin }}$ | : minimum input voltage |


| $\mathrm{V}_{\text {omin }}$ | minimum output voltage |
| :---: | :---: |
| $\mathrm{V}_{0}(\mathrm{t})$ | : output voltage vector |
| $\mathrm{V}_{\mathrm{i}}(\mathrm{t})$ | : input voltage vector |
| $\mathrm{V}_{\mathrm{R}}$ | : resistor voltage |
| $\mathrm{V}_{\mathrm{c}}$ | : capacitor voltage |
| $\mathrm{V}_{\mathrm{c}}(\mathrm{o})$ | : initial voltage of a capacitor |
| $\mathrm{V}_{\mathrm{f}}$ | : forward voltage drop across bidirectional switch |
| $\mathrm{V}_{\text {f }}$ | : forward voltage drop across IGBT |
| $V_{f d}$ | : forward voltage drop across diode |
| $\mathrm{V}_{\mathrm{sd}}, \mathrm{V}_{\mathrm{sq}}$ | : stator voltage in a synchronously rotating d-q axis frame of reference |
| $\omega_{i}$ | : angular frequency of input waveform |
| $\omega_{0}$ | : angular frequency of output waveform |
| $\omega_{\mathrm{m}}$ | : modulation angular frequency |
| $\omega_{\text {sl }}$ | : slip angular frequency |
| $\omega_{\text {e }}$ | : stator angular frequency |
| $\omega_{\text {r }}$ | : rotor angular frequency |
| $\mathrm{X}_{\mathrm{s}}, \mathrm{X}_{\mathrm{r}}$ | : stator and rotor reactance |
| $\phi_{\mathrm{rd}}, \phi_{\mathrm{rq}}$ | : d and q axis flux linking the rotor windings |
| $\phi_{i}$ | : input phase angle |
| $\phi$ 。 | : load phase angle |
| $\theta_{e}, \varepsilon$ | : angular co-ordinates |
| $\theta$ | : relative phase |
| $\Theta$ | : heat sink rating |
| $\sigma$ | : leakage coefficient |
| $\Psi$ | : phase shift ( $0,2 \pi / 3,4 \pi / 3$ ) |
| S | : used as a unit for seconds |

## CHAPTER 1

## INTRODUCTION

### 1.1 Introduction

Rapid technical advancements in power semiconductor and microprocessor technology over the last 15 years have released the induction motor from its previous position as a fixed speed motor. Traditionally, DC motors were used for variable speed applications despite the many advantages of the AC induction motor such as; lower cost, robustness, low maintenance and reliability. The reason for this was the ease with which DC motors can be controlled to provide variable speed operation with good dynamic response and four-quadrant capability. The improvement in power switches and microprocessor technology over the last 15 years has resulted in the development of many AC-AC converters which basically transform the fixed frequency AC supply into a variable frequency, variable voltage source such as required by the induction motor in variable speed applications.

This thesis is concerned with a particular type of AC-AC converter known as the matrix converter. Before considering this in more detail however it is instructive the briefly review AC-AC converter circuits in general. AC-AC converter topologies may be classified into three categories, depending upon the type of internal power transfer link;

- DC link
- AC link
- Direct link

DC Link: The DC link converter is the most common AC variable speed drive system used in the market [1]. It consists of two stages. Firstly, the AC power supply is converted to DC by means of a rectifier circuit. Secondly, the DC voltage
is converted to a variable frequency, variable voltage AC output by an inverter circuit. The configuration of the DC link results in two types of converter: The Voltage Source Inverter (VSI)[2] and the Current Source Inverter (CSI)[3]. The VSI has a large filter capacitor across the inverter input terminals which maintains a constant DC link voltage. The inverter provides an adjustable-frequency voltage source in which the output voltage is essentially independent of load current. On the other hand, the CSI is supplied with a controlled current provided by a large inductance connected in series with the inverter input. In this case the load current is controlled rather than the load voltage. The inverter output voltage is dependent upon the load impedance. One difficulty that is encountered with the VSI circuit fed from a diode rectifier is its inability to regenerate power back to the supply. An increasingly popular way of overcoming this limitation is to use the so-called "back to back" circuit where the diode rectifier is replaced by a PWM inverter operating in the rectifying mode [1].

AC Link: The AC link converter is an alternative to the DC link converter which attempts to minimizing switching losses and reduce low-order harmonics. These converters employ a high-frequency resonant LC circuit in the DC link and therefore, they are also known as resonant converters. The form of the resonant waveform can be either an AC waveform or an AC waveform superimposed on a DC level which eliminates the need for bidirectional switches. Resonant converters make use of a zero-voltage and/or a zero-current condition at turn-on and turn-off in order to reduce switching losses [4-5]. The need for a higher number of switching devices and resonant components in addition to the complex control of bidirectional power flow is the major disadvantage of resonant converters. Therefore, at present resonant link converters cannot compete with DC link converters in the market place.

The resonant circuit in the DC link can either be arranged in parallel (PRC) or series (SRC). In the PRC an LC resonant circuit connected in parallel to the input of the inverter provides an oscillation around the DC link voltage so that the input voltage remains zero for a finite duration in which the state of the switches can be changed, thus resulting in zero-voltage switching. The SRC is formed by connecting
the resonant circuit in series with the input of the inverter. The zero-crossing of the resonant link current allows zero-current switching as well as natural commutation of the inverter switches. Therefore, this topology can use relatively inexpensive and higher rating devices. In order to remove the need of the bidirectional switches for both the PRC and the SRC a DC bias voltage is added to the AC link voltage.

Direct Link: Direct frequency changers (DFC) perform AC-AC conversion without the need for intermediate energy storage. With a properly operated set of switches the input lines are connected directly to the output lines. The DFC can be constructed in the form of a cycloconverter [11] or a matrix converter [12]. Both types suffer from the need for bidirectional switches which leads to a large number of switching devices and therefore, complex control [6].

The cycloconverter is used in high-power motor drives and slip energy recovery schemes [7]. The output frequency is usually limited to one third of the input frequency to operate with high efficiency. More complex cycloconverter designs have been proposed [8] which use forced-commutated or load-commutated techniques to provide a much wider frequency range. However, the need for a load which has the correct characteristics for the load-commutated cycloconverter and the increased complexity and cost of forced-commutated cycloconverters make these circuits unattractive. Other applications of the cycloconverter include voltage stabilization of transmission and distribution lines, correction of the power factor of drives and static conversion equipment and reduction of voltage flicker and voltage regulation of arc furnaces.

This thesis is concerned with the matrix converter which is effectively a forced commutated cycloconverter. The matrix converter consists of a matrix of bidirectional switch elements such that there is a switch for each possible connection between the input and output lines. In the 3-phase to 3 -phase matrix converter there are 9 bidirectional switching elements as shown in Figure 1.1. The matrix can be switched to connect any output line to any input line provided that short circuit of the input and open circuit of the output (assuming an inductive load) are avoided. Control of the output voltage is achieved by switching between the allowed switching
states using a predetermined sequence such that the "average" value of the output voltage spectrum mainly consists of the wanted component plus high frequency components associated with the switching which can be removed with filters or by the inductance of the load [9]. On the supply side, the current is built up from segments of the three output currents and blank intervals during which the output currents are circulated through the converter. The input current spectrum mainly consists of a supply frequency component plus high frequency components which are circulated through input filters to leave a virtually sinusoidal supply current [10]. The converter is capable of operating at lagging, unity, or even leading fundamental input displacement factor regardless of the load displacement factor. The converter offers the advantages of:

- Four quadrant operation
- Sinusoidal input and output waveforms
- Minimum energy storage components
- Controllable displacement factor


Figure 1.1 Switch Layout of the Matrix Converter

A disadvantage of the matrix converter is the fact that the maximum output voltage is limited to $86.6 \%$ of the input voltage. In addition, its physical realisation is not straightforward due primarily to the absence of naturally occurring freewheeling paths. Consequently the timing of the switch actuation signals is particularly critical. Table 1.1 shows a comparison of the AC-AC converters.

Table 1.1 A Comparison of 3-Phase to 3-Phase AC-AC Converters

| Converter Topology | No. of Device <br> Controlled <br> (Diodes) | Number of Quadrants | Basic Passive <br> Components | Input <br> Current <br> Quality | Device <br> Requirement | Control | Development <br> Status |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Inverter | 6 (12) | 2 | 1 C | Poor | Tum-off | Simple | established |
| Back to Back | 12 (12) | 4 (Controlled) | 1 C |  | Tum-off | Simple | Well established |
| RDCL Basic Parallel | 6 (12) | 2 | 2C, 1L | Poor | Turn-off | Complex | Emerging |
| RDCL Basic Series | 6 (12) | 2 | 2L, 1C | Poor | SCR | Complex | Emerging |
| Parallel Resonant AC Link | 12 (24) | 2 | 1L, 1C | Poor | Tum-off | Complex | Emerging |
| Series Resonant AC Link | 12 (24) | 2 | 1L, 1C | Poor | SCR | $\begin{array}{\|l\|} \hline \text { Very } \\ \text { Complex } \end{array}$ | Emerging |
| Cycloconverter | 36 | 4 (Natural) | 0 | Sinusoidal | SCR | Complex | established |
| Matrix | 18 (18) | 4 (Natural) | 0 |  | Tum-off | Complex | Potential |

### 1.2 Review of Matrix Converter Developments

The matrix converter topology was first proposed by Gyugyi and Pelly in 1976 [11]. They extended the principle of the cycloconverter to obtain an unrestricted output frequency by using controllable bidirectional switching devices. The main
disadvantage of the original arrangement is that it generates large unwanted input current and output voltage harmonics which cannot easily be removed by filters. This problem was solved in $[9-10,12]$ by Venturini who proposed a new PWM control algorithm. This algorithm provides sinusoidal input currents and output voltages with unrestricted output frequency and controllable input displacement factor. However, unfortunately the maximum output to input voltage ratio is $50 \%$. The Venturini control algorithm was extended by Maytum and Colman [13] to increase the voltage ratio to 86.6 \%. In [14] Alesina and Venturini published a rigorous mathematical proof of the maximum output amplitude capability along with modified version of Venturini original algorithm. This modified version allows a maximum voltage ratio of $86.6 \%$ and fully controllable input displacement factor, within a limited range of voltage gain with respect to the output phase displacement. Other publications [1518] have subsequently dealt with the modulation and analysis of matrix converters operating with the Venturini algorithm.

In 1985 Ziogas et al [19-21] proposed some new algorithms in which the conversion process is considered in two stages with an intermediate fictitious DC link. Whilst these algorithms can produce a voltage ratio approaching $100 \%$ the output frequency is restricted and the input current contains increased low order harmonics. Consequently, many of the attractive features of the matrix converter are lost.

In [24-27] a new class of algorithms called scalar algorithms were proposed. These are based on the scalar comparison of the instantaneous input voltages and enable the drawing of sinusoidal input currents by applying the principle that the current drawn from each phase is proportional to the input voltage on each phase in every sampling time. The method used in [24-26] provides synchronous and asynchronous operation of the matrix converter with controllable input displacement factor. However, the real-time implementation of the control algorithm requires a large number of comparisons to be made at each sampling instant which is very demanding on processor time. The scalar algorithm proposed in [27] uses a two-phase-switching method instead of using three input line to line voltages. This
simplifies the real-time implementation of the algorithm, but sacrifices the control of the input displacement factor.

More recently an output voltage control method using space vector modulation has been proposed [28-30]. This control algorithm uses a PWM method which is claimed to provide a considerable improvement of the output voltage waveforms. However, this improvement is obtained at the expense of a degradation in the quality of the input current waveforms.

The unrestricted frequency changing properties of the matrix converter mean that it can also be used as an AC to DC converter (rectifier) or as a DC to AC converter (inverter). These properties have been explored in detail in a number of publications by Holmes and Lipo [31-33] although it is difficult to see where this approach would have significant advantages over the conventional circuits.

Other more recent publications have been concerned with increasing the efficiency of the matrix converter by minimizing the switching loss [34-37]. This has been achieved by employing either zero-current at turn-on or zero-voltage at turn-off ( which requires additional components in the bidirectional switch structure) [34-35], or semi-soft current commutation proposed in [36-37].

### 1.3 Project Objectives

The overall objective of this project was to investigate the application of matrix converter technology to induction motor drives. The first objective was to build a reliable power circuit rated at 2.5 kW based on IGBT devices. To evaluate the possibilities the following types of drive of increasing sophistication were to be developed using this power circuit:

1- Open loop drive with volt/hertz control of flux,
2- Closed loop drive with slip regulation and volt/hertz control of flux,
3- Closed loop drive with vector control of the torque and flux producing components of stator current.

For a research and development drive a main requirement is that the system controller is easily modified (both hardware and software) to meet many specifications. To achieve this objective, a transputer parallel processor network controller was used that by its very nature provides such a system.

Most of the previous publications on matrix converters have dealt specifically with modulation algorithms or with aspects of power circuit design. Very few publications have considered complete drive systems or the problems associated with implementing the modulation algorithms in real time where the output voltage demand is continually varying (as it does in a vector control scheme for example). Throughout the project therefore, the principal focus has been the ultimate development of a reliable closed loop vector controlled matrix converter drive that has servo performance and true four quadrant capability rated at 2.5 kW . This final objective has been met and the real possibilities of using the matrix converter as the basis for both low performance and high performance drive systems have been shown.

### 3.4 Structure of the Thesis

In Chapter two, the modulation algorithms, namely Venturini's algorithm and the scalar algorithm which are used in this work are described. The method to control the input displacement factor regardless of the load displacement factor using Venturini's algorithm is presented. The maximum output voltage limitations of the matrix converter are discussed and the modified Venturini's algorithm which is capable of achieving the maximum output voltage is given.

Chapter three considers the physical realization of the matrix converter power circuit. A controllable switching device for the prototype converter is chosen by considering the current state of semiconductor technology. A bidirectional switch is constructed from a suitable combination of unidirectional switches. A gate drive circuit which does not require an additional isolated power supply is designed for driving isolated gate switches. A simple snubber circuit for each bidirectional switch
is arranged to limit the device voltage.
In Chapter four, the semiconductor losses in the matrix converter are investigated. The protection of the prototype converter against severe overvoltages and overcurrents is discussed. The prototype is tested with a passive R-L load and experimental results are presented. Finally, the efficiency of the converter is measured and the total losses are compared with the calculated losses.

Chapter five outlines the real-time implementation of the Venturini algorithm and the scalar algorithm on a transputer network. The design and operation of the interface circuits used for voltage, current and motor speed measurements and PWM generation are considered. The dead-lock protection of the prototype converter is described. The pulse steering circuits and the shutdown protection circuit are discussed.

Chapter six investigates the real-time implementation of open-loop and closedloop control of the matrix converter induction motor drive on a transputer network. In open-loop, a constant Volt/Hertz control strategy is used for the speed control of the induction motor. The slip regulation technique is also implemented to demonstrate the closed-loop operation of the drive system. Practical results are presented to show the transient and steady-state operation of the control strategies on the induction motor.

Chapter seven deals with the ultimate objective of this project which is the implementation of the field-orientation control technique (vector control) to the matrix converter induction motor drive using Transputer parallel processors. The indirect vector control strategy is used since this requires no alteration to the basic induction motor. However, the experimental rig is able to implement the other control strategies for evaluation, without major hardware changes. Experimental results are given to demonstrate transient and steady-state operation of the vector control strategy. The results also show the regenerative operation of the matrix converter.

Chapter eight presents the conclusions and possibilities for further work.

## CHAPTER 2

## MATRIX CONVERTER

## MODULATION ALGORITHMS

### 2.1 Introduction

This chapter describes the matrix converter modulation algorithms that have been used in this work, namely the Venturini algorithm $[9-10,12,14]$ and the scalar algorithm [5-7]. Other modulation strategies have been proposed [15,22,27-29] but are not considered here.

The first section describes the Venturini algorithm including the method for controlling the input displacement factor of the converter. The maximum output voltage limitations of the matrix converter and the method to achieve the maximum possible output voltage of the converter are discussed. A form of the Venturini algorithm that is particularly suitable for real-time implementation is then given in the next section. Finally, the scalar modulation algorithm which has been proposed as an alternative to the Venturini algorithm is discussed.

### 2.2 The Venturini Control Algorithm

The matrix converter connects any output line to any input line by means of nine-bidirectional switches constructed in a matrix form, as shown in Figure 2.1. Note that throughout the thesis, uppercase subscripts (A B C) denote the input phases and lowercase subscripts ( a b c) denote the output phases. Only one of the switches on each output phase can be closed at any particular time. The output voltage waveforms are therefore reconstructed from chops of the three input voltages.

To consider the modulation problem we assume that the switches in the converter are ideal that the input voltage waveforms form an undistorted balanced 3phase set. The input voltages can therefore be written as;

$$
\left[\begin{array}{c}
V_{A}(t)  \tag{2.1}\\
V_{B}(t) \\
V_{C}(t)
\end{array}\right]=V_{i m}\left[\begin{array}{c}
\cos \left(\omega_{i} t\right) \\
\cos \left(\omega_{i} t+2 \pi / 3\right) \\
\cos \left(\omega_{i} t+4 \pi / 3\right)
\end{array}\right]
$$

The Venturini algorithm provides a control of the switches, $\mathrm{S}_{\mathrm{Aa}}, \mathrm{S}_{\mathrm{Ba}}, \ldots, \mathrm{S}_{\mathrm{Cc}}$ so that the low frequency parts of the synthesized output voltages $V_{a}, V_{b}, V_{c}$ and input currents $I_{A}, I_{B}, I_{C}$ are purely sinusoidal with the prescribed output frequency, input frequency, amplitude and input displacement factor. The switches on each output phase are closed sequentially and repetitively and we define $t_{A z}, \ldots, t_{C_{c}}$ as the on time for $S_{A d}, \ldots, S_{C c}$ within a sequence. The sequence time, $T_{s}$ is defined as the sum of the switching times;

$$
\mathrm{T}_{3}=\mathrm{t}_{\mathrm{Aa}}+\mathrm{t}_{\mathrm{Ba}}+\mathrm{t}_{\mathrm{Ca}}=\mathrm{t}_{\mathrm{Ab}}+\mathrm{t}_{\mathrm{Bb}}+\mathrm{t}_{\mathrm{Cb}}=\mathrm{t}_{\mathrm{Ac}}+\mathrm{t}_{\mathrm{Bc}}+\mathrm{t}_{\mathrm{Cc}}=1 / \mathrm{f}_{\mathrm{s}}
$$

where; fs is the switching frequency and is constant (ie each sequence has the same length).

### 2.2.1 Output Voltage Waveforms

During any particular sequence the average value of the output voltages, $\mathrm{V}_{\mathrm{a}}(\mathrm{t})$, $\mathrm{V}_{\mathrm{b}}(\mathrm{t})$ and $\mathrm{V}_{\mathrm{c}}(\mathrm{t})$ in Figure 2.1 are;

$$
\begin{align*}
& V_{a}(t)=V_{i m} \cos \left(\omega_{i} t\right) \frac{t_{A a}}{T_{s}}+V_{i m} \cos \left(\omega_{i} t+\frac{2 \pi}{3}\right) \frac{t_{B a}}{T_{s}}+V_{i m} \cos \left(\omega_{i} t+\frac{4 \pi}{3}\right) \frac{t_{C a}}{T_{s}} \\
& V_{b}(t)=V_{i m} \cos \left(\omega_{i} t\right) \frac{t_{A b}}{T_{s}}+V_{i m} \cos \left(\omega_{i} t+\frac{2 \pi}{3}\right) \frac{t_{B b}}{T_{s}}+V_{i m} \cos \left(\omega_{i} t+\frac{4 \pi}{3}\right) \frac{t_{C b}}{T_{s}}  \tag{2.2}\\
& V_{c}(t)=V_{i m} \cos \left(\omega_{i} t\right) \frac{t_{A c}}{T_{s}}+V_{i m} \cos \left(\omega_{i} t+\frac{2 \pi}{3}\right) \frac{t_{B c}}{T_{s}}+V_{i m} \cos \left(\omega_{i} t+4 \frac{\pi}{3}\right) \frac{t_{C_{c}}}{T_{s}}
\end{align*}
$$



Figure 2.1 The Matrix Converter Switch Layout

The resulting output voltage waveforms are discontinuous functions which consist of chops of the three-input voltages. In general, the output voltage spectrum depends on input voltage, frequency and the switching strategy. However, the low frequency part of the output spectrum depends mainly on the average output value in each sequence providing that $2 \pi f_{s} \gg \omega_{i}, \omega_{0}$.

If the switch times are dynamically modulated in a sinusoidal manner at $\omega_{m}$, whilst maintaining a fixed sequence time $T_{s}$, a variable output phasor rotating at an output frequency $\omega_{\mathrm{o}}=\omega_{\mathrm{i}}+\omega_{\mathrm{m}}$ can be obtained. This can be validated as follows: The switching times for three-output phases are;

$$
\begin{aligned}
& t_{A a}=\frac{T s}{3}\left(1+2 q \cos \left(\omega_{m} t+\theta\right)\right) \\
& t_{B a}=\frac{T_{s}}{3}\left(1+2 q \cos \left(\omega_{m} t+\theta-\frac{2 \pi}{3}\right)\right) \\
& t_{C a}=\frac{T}{3}\left(1+2 q \cos \left(\omega_{m} t+\theta-\frac{4 \pi}{3}\right)\right) \\
& t_{A b}=\frac{T_{s}}{3}\left(1+2 q \cos \left(\omega_{m} t+\theta-\frac{4 \pi}{3}\right)\right) \\
& t_{B b}=\frac{T_{s}}{3}\left(1+2 q \cos \left(\omega_{m} t+\theta\right)\right) . \\
& t_{C b}=\frac{T_{s}}{3}\left(1+2 q \cos \left(\omega_{m} t+\theta-\frac{2 \pi}{3}\right)\right) \\
& t_{A c}=\frac{T_{s}}{3}\left(1+2 q \cos \left(\omega_{m} t+\theta-\frac{2 \pi}{3}\right)\right) \\
& t_{B c}=\frac{T_{s}}{3}\left(1+2 q \cos \left(\omega_{m} t+\theta-\frac{4 \pi}{3}\right)\right) \\
& t_{C c}=\frac{T s}{3}\left(1+2 q \cos \left(\omega_{m} t+\theta\right)\right)
\end{aligned} \quad \text { Output Phase a }
$$

Where $\theta$ is the relative phase and q is the voltage ratio.
A control matrix, $M(t)$ is defined to satisfy the condition below;

$$
\begin{equation*}
V_{o}(t)=M(t) . V_{i}(t) \tag{2.4}
\end{equation*}
$$

where the elements of M are the duty cycles of the 9 switches.
The $\mathrm{M}(\mathrm{t})$ matrix can be derived by substituting Equation 2.3 into Equation 2.2. Hence,

$$
M(t)=\left[\begin{array}{ccc}
\frac{1}{3}(1+2 q \cos (A)) & \frac{1}{3}\left(1+2 q \cos \left(A-\frac{2 \pi}{3}\right)\right) & \frac{1}{3}\left(1+2 q \cos \left(A-\frac{4 \pi}{3}\right)\right)  \tag{2.5}\\
\frac{1}{3}\left(1+2 q \cos \left(A-\frac{4 \pi}{3}\right)\right) & \frac{1}{3}(1+2 q \cos (A)) & \frac{1}{3}\left(1+2 q \cos \left(A-\frac{2 \pi}{3}\right)\right) \\
\frac{1}{3}\left(1+2 q \cos \left(A-\frac{2 \pi}{3}\right)\right) & \frac{1}{3}\left(1+2 q \cos \left(A-\frac{4 \pi}{3}\right)\right) & \frac{1}{3}(1+2 q \cos (A))
\end{array}\right]
$$

where; $\mathrm{A}=\omega_{\mathrm{m}} \mathrm{t}+\theta, \quad \omega_{\mathrm{m}}=\omega_{0}-\omega_{\mathrm{i}}$

If the control matrix in Equation 2.5 is substituted into Equation 2.4 then,

$$
\left[\begin{array}{l}
{\left[\begin{array}{l}
V_{a}(t) \\
V_{b}(t) \\
V_{c}(t)
\end{array}\right]=\left[\begin{array}{cc}
\frac{1}{3}(1+2 q \cos (A)) & \frac{1}{3}\left(1+2 q \cos \left(A-\frac{2 \pi}{3}\right)\right) \\
\frac{1}{3}\left(1+2 q \cos \left(A-\frac{4 \pi}{3}\right)\right) & \frac{1}{3}(1+2 q \cos (A)) \\
\frac{1}{3}\left(1+2 q \cos \left(A-\frac{2 \pi}{3}\right)\right) & \frac{1}{3}\left(1+2 q \cos \left(A-\frac{4 \pi}{3}\right)\right) \\
\frac{1}{3}\left(1+2 q \cos \left(A-\frac{4 \pi}{3}\right)\right) \\
\frac{1}{3}\left(1+2 q \cos \left(A-\frac{2 \pi}{3}\right)\right) \\
\frac{1}{3}(1+2 q \cos (A))
\end{array}\right]\left[\begin{array}{l}
V_{i m} \cos \left(\omega_{i} t\right) \\
V_{i m} \cos \left(\omega_{i} t+\frac{2 \pi}{3}\right) \\
V_{i m} \cos \left(\omega_{i} t+\frac{4 \pi}{3}\right)
\end{array}\right]} \tag{2.6}
\end{array}\right.
$$

If the matrix multiplication in Equation 2.6 is performed it simplifies to;

$$
\left[\begin{array}{l}
V_{a}(t)  \tag{2.7}\\
V_{b}(t) \\
V_{c}(t)
\end{array}\right]=q V_{i m}\left[\begin{array}{c}
\cos \left(\omega_{o} t+\theta\right) \\
\cos \left(\omega_{o} t+\theta-\frac{4 \pi}{3}\right) \\
\cos \left(\omega_{o} t+\theta-\frac{2 \pi}{3}\right)
\end{array}\right]
$$

where; $0 \leq \mathrm{q} \leq 0.5$ and $\omega_{0}=\omega_{\mathrm{i}}+\omega_{\mathrm{m}}$
This shows that the matrix converter operating under the Venturini algorithm provides a set of sine waves at a frequency of $\omega_{0}$, amplitude $q . V_{i}$ and a relative phase at $t=0$ of $\theta$.

It should be noted that if $\omega_{\mathrm{m}}$ is negative and $\left|\omega_{\mathrm{m}}\right|>\omega_{\mathrm{i}}$ then the phase sequence of the output voltages is reversed $\left(\omega_{0}<0\right)$ and this allows, for example, an induction motor to be driven in both directions. Other specific cases worth noting are $\omega_{\mathrm{m}}=0$ which gives the same input and output frequencies ( $\omega_{\mathrm{o}}=\omega_{\mathrm{i}}$ ) and $\omega_{\mathrm{m}}=-\omega_{\mathrm{i}}$ which gives a DC output $\left(\omega_{0}=0\right)$.

### 2.2.2 Input Current Waveforms

If we assume that the converter is connected to a three phase resistiveinductive load with load phase angle, $\phi_{0}$, the output currents can be considered to be a three phase set of sines;

$$
I_{o}(t)=\left[\begin{array}{c}
I_{a}(t)  \tag{2.8}\\
I_{b}(t) \\
I_{c}(t)
\end{array}\right]=I_{o m}\left[\begin{array}{c}
\cos \left(\omega_{o} t+\phi_{o}\right) \\
\cos \left(\omega_{o} t+\phi_{o}+\frac{2 \pi}{3}\right) \\
\cos \left(\omega_{o} t+\phi_{0}+\frac{4 \pi}{3}\right)
\end{array}\right]
$$

assuming $\theta$ is zero for simplicity.
The input line current consists of the sum of three switch currents connected to the same input line. This is illustrated in Figure 2.2. It should be noted that here,the action of the switches is in the reverse manner to the construction of the output voltage waveforms. Therefore, the nature of the input current may be determined by the multiplication of the transpose of the control matrix, $M(t)$ and the output currents.

$$
\begin{equation*}
I_{i}(t)=M^{T}(t) \cdot I_{0}(t) \tag{2.9}
\end{equation*}
$$



Figure 2.2 The Layout of the Switches for the Current Synthesis

If Equation 2.8 and the transpose of the control matrix in Equation 2.5 are substituted into Equation 2.9 then;

$$
\left.\begin{array}{rl}
I_{i}(t)= & {\left[\begin{array}{l}
I_{A}(t) \\
I_{B}(t) \\
I_{C}(t)
\end{array}\right]=}
\end{array} \begin{array}{cc}
\frac{1}{3}(1+2 q \cos (A)) & \frac{1}{3}\left(1+2 q \cos \left(A-\frac{4 \pi}{3}\right)\right)  \tag{2.10}\\
\frac{1}{3}\left(1+2 q \cos \left(A-\frac{2 \pi}{3}\right)\right) & \frac{1}{3}(1+2 q \cos (A)) \\
\frac{1}{3}\left(1+2 q \cos \left(A-\frac{4 \pi}{3}\right)\right) & \frac{1}{3}\left(1+2 q \cos \left(A-\frac{2 \pi}{3}\right)\right)
\end{array}\right]\left[\begin{array}{l}
\frac{1}{3}\left(1+2 q \cos \left(A-\frac{2 \pi}{3}\right)\right) \\
I_{o m} \cos \left(\omega_{0} t+\theta+\phi_{0}\right) \\
I_{o m} \cos \left(\omega_{o} t+\theta+\phi_{0}+\frac{2 \pi}{3}\right) \\
I_{o m} \cos \left(\omega_{0} t+\theta+\phi_{0}+\frac{4 \pi}{3}\right)
\end{array}\right]
$$

where; $A=\omega_{m} t+\theta, \omega_{m}=\omega_{0}-\omega_{i}$
Equation 2.10 can be simplified to yield;

$$
\left[\begin{array}{l}
I_{A}(t)  \tag{2.11}\\
I_{B}(t) \\
I_{C}(t)
\end{array}\right]=q I_{o m}\left[\begin{array}{c}
\cos \left(\omega_{i} t+\phi_{0}\right) \\
\cos \left(\omega_{i} t+\phi_{0}-\frac{4 \pi}{3}\right) \\
\cos \left(\omega_{i} t+\phi_{0}-\frac{2 \pi}{3}\right)
\end{array}\right]
$$

Thus, the average current drawn from the supply is a balanced 3-phase set at the input supply frequency, $\omega_{\mathrm{i}}$ and with displacement factor equal to the load displacement factor $\cos \left(\phi_{0}\right)$.

It is possible however to repeat the analysis of Section 2.2.1 using $\omega_{m}=-\left[\omega_{0}\right.$ $\left.+\omega_{i}\right]$ (called the negative phase sequence mode) rather than $\omega_{m}=\left[\omega_{0}+\omega_{i}\right]$ (called the positive phase sequence mode). This gives the same output (negative phase sequence) voltages given by Equation 2.7 but the phase angle of the input currents is reversed so that;

$$
\left[\begin{array}{l}
I_{A}(t)  \tag{2.12}\\
I_{B}(t) \\
I_{C}(t)
\end{array}\right]=q I_{o m}\left[\begin{array}{c}
\cos \left(\omega_{i} t-\phi_{0}\right) \\
\cos \left(\omega_{i} t-\phi_{0}-\frac{4 \pi}{3}\right) \\
\cos \left(\omega_{i} t-\phi_{0}-\frac{2 \pi}{3}\right)
\end{array}\right]
$$

As a result of this an inductive load characteristic can be changed into a capacitive characteristic at the converter input terminals and vice-versa.

### 2.2.3 Input Displacement Factor Control

In order to achieve a controllable input displacement factor two converters can be connected in parallel supplying the same load. While one of them provides positive phase sequence $\left(\omega_{\mathrm{m}}=\omega_{\mathrm{i}}+\omega_{0}\right)$, the other provides negative phase sequence ( $\omega_{\mathrm{m}}=-\omega_{\mathrm{i}}-\omega_{0}$ ) as explained by Equations 2.11 and 2.12 and the phasor diagrams given in Figure 2.3. However, the same result can be obtained with a single converter, in which the duty cycle of each switch is the average of the duty cycles of the corresponding switches in the two converters. As can be seen from Figure 2.3 it is possible to operate with unity, inductive or capacitive displacement factor at the converter input terminals regardless of the load displacement factor.


Figure 2.3 Variation of Input Current Phase Angle with Various Operating Modes for Lagging Output Current

The modulation algorithm, $\mathrm{M}(\mathrm{t})$ is redefined to achieve this action. Hence,

$$
\begin{align*}
M(t) & =\frac{1}{3} \alpha_{1}\left[\begin{array}{ccc}
(1+2 q \cos (A)) & \left(1+2 q \cos \left(A-\frac{2 \pi}{3}\right)\right) & \left(1+2 q \cos \left(A-\frac{4 \pi}{3}\right)\right) \\
\left(1+2 q \cos \left(A-\frac{4 \pi}{3}\right)\right) & (1+2 q \cos (A)) & \left(1+2 q \cos \left(A-\frac{2 \pi}{3}\right)\right) \\
\left(1+2 q \cos \left(A-\frac{2 \pi}{3}\right)\right) & \left(1+2 q \cos \left(A-\frac{4 \pi}{3}\right)\right) & (1+2 q \cos (A))
\end{array}\right]  \tag{2.13}\\
& +\frac{1}{3} \alpha_{2}\left[\begin{array}{ccc}
(1+2 q \cos (B)) & \left(1+2 q \cos \left(B-\frac{2 \pi}{3}\right)\right) & \left(1+2 q \cos \left(B-\frac{4 \pi}{3}\right)\right) \\
\left(1+2 q \cos \left(B-\frac{2 \pi}{3}\right)\right) & \left(1+2 q \cos \left(B-\frac{4 \pi}{3}\right)\right) & (1+2 q \cos (B)) \\
\left(1+2 q \cos \left(B-\frac{4 \pi}{3}\right)\right) & (1+2 q \cos (B)) & \left(1+2 q \cos \left(B-\frac{2 \pi}{3}\right)\right)
\end{array}\right]
\end{align*}
$$

where;

$$
\begin{aligned}
& A=\omega_{m} t, \quad B=-\left(\omega_{m}+2 \omega_{i}\right) t \quad \text { at } \quad \theta=0 \\
& \alpha_{1}=\frac{1}{2}\left[1+\tan \phi_{i} \cot \phi_{0}\right], \quad \alpha_{2}=1-\alpha_{1}=\frac{1}{2}\left[1-\tan \phi_{i} \cot \phi_{0}\right] \\
& \phi_{i}=\arctan \left[\left(\alpha_{1}-\alpha_{2}\right) \tan \phi_{0}\right], \quad q=\frac{V_{0}}{V_{i}} \quad \text { with } ; \\
& 1>\left(\alpha_{1}-\alpha_{2}\right)>-1, \quad 0 \leq q \leq \frac{1}{2}
\end{aligned}
$$

Assuming for example an inductive load the converter input characteristic can be made resistive, inductive or capacitive as follows;

$$
\begin{array}{ll}
\alpha_{1}=\alpha_{2}, & \text { resistive characteristic (unity input displacement factor) } \\
\alpha_{1}>\alpha_{2}, & \text { inductive characteristic (lagging input displacement factor) } \\
\alpha_{1}<\alpha_{2}, & \text { capacitive characteristic (leading input displacement factor) }
\end{array}
$$

The converter output voltage, $V_{0}(t)$ and input current, $\mathrm{I}_{\mathrm{i}}(\mathrm{t})$ can be calculated using the equations given below if the low frequency part of input and output waveforms are only considered;

$$
\begin{align*}
& V_{o}(t)=M(t) V_{i}(t)  \tag{2.14}\\
& I_{i}(t)=M^{T}(t) I_{o}(t)
\end{align*}
$$

It should be noted that Equations 2.14 are only valid for $\mathrm{q} \leq 0.5$. As shown in Figure 2.4 , for variable output frequency the output voltage is limited to half the input voltage so that the average output voltage does not exceed the minimum level of the input voltage. This voltage limitation is a disadvantage of the matrix converter when compared to the standard DC link PWM inverter.

### 2.2.4 Maximum Output Voltage Improvement

The output voltage waveforms of the matrix converter must be kept within the envelope of the three-phase input voltage waveforms. Hence, the maximum output amplitude is obtained from the instantaneous minimum input voltage range.


Figure 2.4 Sinusoidal Output Voltage Referenced to the Three-Phase Input Voltage

That is;

$$
\begin{equation*}
\min _{0 \leq \omega_{0} t \leq 2 \pi}\left(V_{i m}-V_{i \min }\right)=\max _{0 \leq \omega_{0} t \leq 2 \pi}\left(V_{o m}-V_{o \text { min }}\right) \tag{2.15}
\end{equation*}
$$

If the input and output waveforms are substituted into Equation 2.15, then;

$$
\frac{3}{2} V_{i}=\sqrt{3} V_{0}
$$

Therefore, the maximum possible output voltage becomes;

$$
\begin{equation*}
V_{o m}=\frac{\sqrt{3}}{2} V_{i}=0.866 V_{i} \tag{2.16}
\end{equation*}
$$

The methods for achieving the maximum output voltage are described in the following section.

### 2.2.5 Third Harmonic Addition

If a third harmonic of the input voltage waveform of amplitude (1/4) $V_{i}$ is added to each of the target output waveforms then the maximum output voltage increases to $75 \%$ of the input voltage [13]. Consequently, the target output voltage set becomes;

$$
\begin{align*}
& V_{o}(t)=\left[V_{o} \cos \left(\omega_{o} t+(k-1) \frac{2 \pi}{3}\right)+\frac{1}{4} V_{i} \cos \left(3 \omega_{i} t\right)\right]_{k=1}^{3}  \tag{2.17}\\
& \text { where; } \quad 0 \leq \frac{V_{o}}{V_{i}} \leq 0.75
\end{align*}
$$

The third harmonic addition causes the neutral point of the output voltage waveforms to move with respect to the neutral of the input waveforms. However, this does not affect the operation of the load since there is no neutral connection between the supply and load of the matrix converter and consequently, the third harmonic addition causes no current flow in the load. Figure 2.5 shows the input and output voltage waveforms for this case. In order to further increase the maximum output voltage a third harmonic of the desired output frequency of amplitude ( $1 / 6 \mathrm{~V}_{0}$ ) is added to each of the target output voltage waveforms [13]. This increases the maximum output to the theoretically optimum value of $86.6 \%$ of the input voltage. Figure 2.6 shows the target output voltage waveforms within the envelope of the three-phase input voltages. The target output voltage for this case is given by;

$$
\begin{equation*}
V_{0}(t)=\left[V_{0} \cos \left(\omega_{0} t+(k-1) \frac{2 \pi}{3}\right)+\frac{1}{4} V_{i} \cos \left(3 \omega_{i} t\right)-\frac{1}{6} V_{0} \cos \left(3 \omega_{0} t\right)\right]_{k=1}^{3} \tag{2.18}
\end{equation*}
$$

where; $\quad 0 \leq \frac{V_{0}}{V_{i}} \leq 0.866$


Figure 2.5 The Input and Output Voltage Waveforms for:
$\mathrm{V}_{0}=\mathrm{V}_{\mathrm{i}}\left[0.75 \cos \left(\omega_{0} \mathrm{t}\right)+0.25 \cos \left(3 \omega_{\mathrm{i}} \mathrm{t}\right)\right]$ with $\omega_{0}=4 \omega_{\mathrm{i}}$

### 2.2.6 Modification of the Venturini Algorithm for Maximum Output Voltage

In [14] a modified form of the Venturini original algorithm is proposed which achieves maximum amplitude capability with input displacement factor control. However, the ability to control the input displacement factor decreases with increasing the output amplitude. The control matrix, $M(t)$ is redefined as follows;

$$
M(t)=\left[\begin{array}{lll}
m(0,0,0,0,0,0) & m(2,4,2,4,2,4) & m(4,2,4,2,4,2)  \tag{2.19}\\
m(2,2,0,0,0,0) & m(4,0,2,4,2,4) & m(0,4,4,2,4,2) \\
m(4,4,0,0,0,0) & m(0,2,2,4,2,4) & m(2,0,4,2,4,2)
\end{array}\right]
$$

Each element of the control matrix is defined as;


Figure 2.6 The Input and Output Voltage Waveforms at Maximum Output Voltage Ratio of $q=0.866$ with $\omega_{0}=4 \omega_{1}$

$$
\begin{array}{r}
m\left(x_{1}, x_{2}, x_{3}, x_{4}, x_{5}, x_{6}\right)=\frac{1}{3}\left(1+\frac{\sqrt{3}}{2} p\left[Z_{1}^{1}\left(x_{1}\right)+Z_{1}^{-1}\left(x_{2}\right)-\frac{1}{6} Z_{3}^{1}\left(x_{3}\right)-\frac{1}{6} Z_{3}^{-1}\left(x_{4}\right)+\right.\right.  \tag{2.20}\\
\left.\left.\operatorname{sgn}(p)\left(-\frac{1}{6 \sqrt{3}} Z_{0}^{4}\left(x_{5}\right)+\frac{7}{6 \sqrt{3}} Z_{0}^{2}\left(x_{6}\right)\right)\right]+a_{1} Z_{1}^{1}\left(x_{1}\right)+a_{2} Z_{1}^{-1}\left(x_{2}\right)\right)
\end{array}
$$

where;
$a=2|\xi| \frac{\phi_{0}}{\phi_{i}} \quad$ with; $\quad \xi=\frac{\tan \phi_{i}}{\tan \phi_{0}}$
$p=\frac{\left(2 \frac{V_{o}}{V_{i}}-a\right)}{\sqrt{3}}$
$\begin{array}{lllll}a_{1}=a & \text { and } & a_{2}=0 & \text { if } & \xi<0 \\ a_{2}=a & \text { and } & a_{1}=0 & & \text { if } \\ a_{1}=a_{2}=0 & & & & \\ & & & \text { if } & \xi=0\end{array}$
and;

$$
Z_{\beta}^{\alpha}(\gamma)(t)=\cos \left(\left[\beta \omega_{o}+\alpha \omega_{i}\right] t+\gamma \frac{\pi}{3}\right)
$$

with the additional limitation;

$$
\begin{equation*}
|p|+a<1 \tag{2.23}
\end{equation*}
$$

In fact, the expression in the square brackets in Equation 2.20 corresponds to the desired output with unity input displacement factor and the two remaining terms, $\mathrm{a}_{1} \cdot \mathrm{Z}_{1}^{1}\left(\mathrm{x}_{1}\right)$ and $\mathrm{a}_{2} \cdot \mathrm{Z}_{1}^{-1}\left(\mathrm{x}_{2}\right)$ are added to change the input phase angle, $\phi_{1}$ according to Equations 2.21 and 2.22.

### 2.3 A Simplified Form of the Venturini Algorithm

A simplified form of the Venturini algorithm proposed by Korti [38] provides a control algorithm with unity input displacement factor and is suitable for real-time implementation. Instead of detecting the zero-crossing point of the input voltage waveform and timing everything from this, the simplified form of the Venturini algorithm is defined in terms of the three-phase input voltages at every sequence time. For unity input displacement factor the duty cycle for the switch connected between the input phase, $\beta$ and output phase, $\gamma$ can be defined as;

$$
\begin{equation*}
T_{\beta \gamma}=T_{s}\left[\frac{1}{3}+\frac{2 V_{\sigma \gamma} V_{i \beta}}{3 V_{i m}^{2}}+\frac{2 q^{2}}{9 q_{m}} \sin \left(\omega_{i} t+\psi_{\beta}\right) \sin \left(3 \omega_{i} t\right)\right] \tag{2.24}
\end{equation*}
$$

where; $\Psi_{\beta}: 0,2 \pi / 3,4 \pi / 3$ corresponding to the input phases $\mathrm{A}, \mathrm{B}, \mathrm{C}$, respectively. $\mathrm{q}_{\mathrm{m}}$ : maximum voltage ratio, 0.886 .
q : demand voltage ratio
and $\mathrm{V}_{\mathrm{of}}$ is;

$$
\begin{equation*}
V_{o \gamma}=q V_{i m} \cos \left(\omega_{0} t+\Psi_{\gamma}\right)-\frac{q}{6} V_{i m} \cos \left(3 \omega_{0} t\right)+\frac{1}{4} \frac{q}{q_{m}} V_{i m} \cos \left(3 \omega_{i} t\right) \tag{2.25}
\end{equation*}
$$

where; $\Psi_{\gamma}: 0,2 \pi / 3,4 \pi / 3$ corresponding to the output phases $\mathrm{a}, \mathrm{b}, \mathrm{c}$, respectively.
Equations 2.24 and 2.25 are used for the duty cycle calculation of the switches in the implementation of open-loop and closed-loop control of the matrix converter induction motor drive discussed later in Chapter 6 and Chapter 7. The algorithm requires only the three-phase instantaneous input voltages to be measured and then, the input vector position is calculated using these voltages. The input and output frequencies of the matrix converter are totally asynchronised and therefore, closed-loop control is easily achieved by recalculating the switching duty cycles every sampling time for the demanded output frequency which is an output from a controller or user input. In the slip control technique discussed in Chapter 6 the demanded voltage ratio q and the output frequency $\omega_{o}$, are obtained directly from the controller and the control algorithm is executed using Equations 2.23 and 2.24. However, the vector control technique described in Chapter 7 provides a three-phase instantaneous output voltage demand with the output vector position. Consequently, only Equation 2.23 is used to implement the control algorithm.

### 2.4 The Scalar Control Algorithm

This method which is proposed in [24] uses the instantaneous ratio of specific input phase voltages to generate the duty cycles of the switches. The control algorithm is valid for both synchronous and asynchronous operation with adjustable input displacement factor, independent of the load displacement factor. According to the control algorithm during a sequence the average value of the output voltage for one phase is defined as;

$$
V_{o}(t)=\frac{1}{T_{s}}\left[t_{K} V_{K}+t_{L} V_{L}+t_{M} V_{M}\right]=V_{o m} \cos \left(\omega_{o} t\right)
$$

where; $\quad t_{K}+t_{L}+t_{M}=T_{s}$
The variable subscripts, K-L-M are assigned to any of the input phase subscripts, A-B-C according to rules given below;

Rule 1: M is the subscript for the input phase which has a polarity different than those of the other two input phases.

Rule 2: $K$ and $L$ subscripts are assigned to the phases which share the same polarity, the biggest one (in absolute value) being L .

The duty cycles are then given for one period, $\mathrm{T}_{\mathrm{s}}$ as;

$$
\begin{align*}
& t_{L}=\frac{\left(V_{o}-V_{M}\right)}{1.5 V_{i m}^{2}} V_{L}  \tag{2.26}\\
& t_{K}=\frac{\left(V_{0}-V_{M}\right)}{1.5 V_{i m}^{2}} V_{K}  \tag{2.27}\\
& t_{M}=T_{s}-\left(t_{L}+t_{K}\right)
\end{align*}
$$

with the condition of $0 \leq\left(V_{K} / V_{L}\right) \leq 1$
The target output voltage, $\mathrm{V}_{\mathrm{o}}$ used in the calculation of Equations 2.26-2.28 is the same as that used for the Venturini algorithm given in Equation 2.25. Therefore, this control algorithm can also operate with the maximum voltage ratio of 0.866 . From Equations 2.26 and 2.27 it can be seen that the converter switching patterns depend only on the scalar comparison of input phase voltages and the instantaneous value of the desired output voltage.

This scalar control algorithm has also been implemented in the practical matrix converter to allow a comparison with the Venturini method. This is discussed further in Chapter 6. The main disadvantage of this algorithm is that it requires very accurate knowledge of the three-phase input voltages because of the way in which the subscripts $\mathrm{K}, \mathrm{L}$ and M are assigned to the input voltages. Any noise on the measurements at the zero crossing of the input line or phase voltages causes unwanted switching of the subscripts $\mathrm{K}, \mathrm{L}$ and M between the input phases at this point. Therefore, a major error will occur in the duty cycle of the switching patterns according to Equations 2.25-2.27.

### 2.5 Conclusions

It has been shown that the matrix converter operating under the Venturini control algorithm provides sinusoidal input currents and output voltages considering ideal input voltage and output current waveforms. The maximum output voltage limitation of the matrix converter is $86.6 \%$ of the input voltage. The method to obtain this maximum output voltage has been discussed.

The Venturini algorithm which is capable of achieving the maximum output voltage and fully controllable input displacement factor was reviewed. A simplified form of this algorithm with unity input displacement factor was given and this is the form that has been used in the practical work. This algorithm simplifies the control equations and therefore reduces the digital implementation time.

A scalar control algorithm based on the scalar comparison of the instantaneous input voltages has been discussed. This algorithm also yields sinusoidal input currents by using the principle that the current drawn from each phase is proportional to the input voltage on each phase in every sampling time. This algorithm has also been implemented in the practical matrix converter in order to make a comparison between the two algorithms.

## CHAPTER 3

## MATRIX CONVERTER POWER CIRCUIT DESIGN

### 3.1 Introduction

This chapter considers the design of a matrix converter power circuit rated at an input voltage of 250 V line and an output current of 7.2 A . The problems associated with the physical realization of the power circuit are addressed and suitable solutions are given.

The choice of controllable switching device is examined by considering the current state of semiconductor technology and the power rating of the prototype converter. A bidirectional switch is designed from a suitable combination of unidirectional switches. Voltage and current ratings of the power semiconductor devices are calculated for the prototype converter.

A gate drive circuit which has a low component count and does not require an additional isolated power supply is designed for driving isolated gate devices. A simple snubber circuit is chosen to limit the device voltage to an appropriate level. Experimental results are presented to confirm the correct operation of the gate drive circuit and the snubber circuit.

### 3.2 Bidirectional Switch Configuration

Since there are no semiconductor devices available which can directly implement the bidirectional switching action required by the matrix converter it is necessary to fulfil this function from a suitable combination of unidirectional
switching elements. There are three possible configurations [39], a bridge structure, a parallel structure and a series structure as shown in Figure 3.1. The BJT represents a controllable device in Figure 3.1. However, this might be any controllable device. These are considered in more detail below.

(a)

(b)

(c)

Figure 3.1 Bidirectional Switch Structures (a) Diode Bridge. (b) Parallel, (c) Series

### 3.2.1 Diode Bridge Bidirectional Switch

This configuration is shown in Figure 3.1(a). This is the simplest arrangement and consists of a controllable switch inside a diode bridge. The semiconductor losses with this arrangement are high since there are always three conducting devices in the current path resulting in a high forward voltage drop. In addition, the diodes in the
bridge must be fast recovery types and this make the structure unattractive in terms of cost, especially at high switching frequencies. Another possible disadvantage of this structure is that the switching device has to carry the full waveform of the AC current since the device stays on for the negative part of the current waveform as well as the positive part. This results in a higher rating for the switching device.

### 3.2.2 Parallel Structure Switch

Figure 3.1(b) shows a structure which has two anti-parallel switches with series blocking diodes. It has a lower forward voltage drop than that of the previous arrangement. It is necessary to use series blocking diodes with each device since most controllable switches cannot support large reverse voltages. The control of this bidirectional switch is much more difficult since the current polarity must be monitored and each device must be driven with respect to a different potential. This increases the complexity and cost of the matrix converter.

### 3.2.3 Series Structure Switch

Figure 3.1(c) shows a series structure bidirectional switch. There are two devices in anti-series each with parallel diodes. If MOSFETs are used in this structure the body-drain diode can be utilised provided that its recovery characteristics are adequate.

This arrangement has been chosen for the prototype converter in preference to the other types since only one control signal is required because both switches are driven with respect to the same point. This makes the control circuitry much less complex and only one isolated driver is needed for each switch combination. Another advantage is that the forward voltage drop is lower or equal to that of the other switches.

### 3.3 Choice of Switching Device

In recent years advances in semiconductor technology have made available new switching devices and have enhanced the characteristics of existing power devices [7]. These technological advances have provided important progresses in power electronic control. The switching devices which are appropriate for use in the matrix converter are discussed below.

Bipolar Junction Transistors(BJTs): BJTs are current controlled devices and require a large, continuous base current in the on-state due to their low current gain. They have high current carrying capabilities compared with MOS type devices. The current gain of BJTs can be considerably improved if they are used in a Darlington configuration. However, this results in a larger switching time with a higher switching loss. The switching frequency of BJTs is mainly limited by the storage time of the devices.

Metal Oxide Semiconductor Field-Effect Transistors(MOSFETs): Power MOSFETs are voltage controlled devices designed for use at high switching frequencies. The rapid switching characteristics of MOSFETs give rise to relatively low switching losses except at very high frequencies. The conduction losses are due to the on-state resistance which is a function of the voltage rating of the device for a given die size [40]. MOSFETs achieve best silicon utilization at voltage ratings between 400 V and 600 V [7]. Above this voltage rating the device becomes increasingly unattractive due to the increasing on-state resistance. The limit of the power rating for single devices is approximately 600 V at 50 A currently.

Insulated Gate Bipolar Transistors(IGBTs): The IGBT is a combination of the MOSFET and the BJT. It has the fast switching features of the MOSFET and the high power handling capability of the BJT. The IGBT is voltage controlled device and has a small on-state voltage drop. For instance, an IGBT with 1200 V, 600 A has a saturation voltage of 3 V with current fall time of 200 nS . IGBTs are available at ratings of 250 V to 1700 V and 8 A to 800 A . Figure 3.2 shows the circuit symbol


Figure 3.2 The Circuit Symbol of the IGBT
of the IGBT.
The IGBT is now widely used in high power and medium frequency applications. Fast switching and easy control features make the IGBT suitable for use in switching power converters such as the matrix converter. IGBTs are easier to drive than BJTs and are capable of operation at higher switching frequencies. Ease of driving is particulary important in the matrix converter due to the number of switch elements [41]. MOSFETs have similar drive requirements to IGBTs but at high voltage and current ratings they are more expensive and have a higher forward voltage drop which makes the conduction loss unacceptably high. Although, the power rating of the prototype matrix converter is suitable for MOSFETs, IGBT switches have been used in preference to MOSFETs to demonstrate the possibilities of operating at higher powers using larger IGBT devices.

### 3.4 Device Ratings

In this section voltage and current ratings of the IGBTs and the diodes are calculated for the prototype matrix converter induction motor drive. In order to simplify the analysis an ideal matrix converter has been considered. Switching losses and harmonic distortions at the input and output ports are ignored.

### 3.4.1 Device Voltage Rating

The maximum voltage for any device in the matrix converter is the maximum voltage difference between the two lines of the three input voltages. Therefore, the maximum device voltage $\mathrm{V}_{\mathrm{dm}}$ is;

$$
\begin{equation*}
V_{d m}=\sqrt{2} \cdot V_{L} \tag{3.1}
\end{equation*}
$$

Where $V_{L}$ is the line to line input voltage.
For the prototype matrix converter the rated line to line input voltage is 250 V . Then, the maximum device voltage for both the IGBT and the diode is;

$$
\begin{aligned}
& V_{d m}=\sqrt{2} .250 \\
& V_{d m}=354 \mathrm{~V}
\end{aligned}
$$

### 3.4.2 Device Current Rating

One output phase of the matrix converter shown in Figure 3.3 has been considered to calculate the device current rating. In the matrix converter the instantaneous output current for one output phase is the sum of the instantaneous currents in each device sharing that output phase as shown in Figure 3.3. The mathematical relationship between instantaneous load and individual switch currents in Figure 3.3 is given by;

$$
\begin{equation*}
I_{a}(t)=I_{A a}(t)+I_{B a}(t)+I_{C a}(t) \tag{3.2}
\end{equation*}
$$

The mean value of the output current, $I_{a}$ is the sum of the mean value of the three switch currents as given below;

$$
\begin{equation*}
T_{a}=T_{A a}+T_{B a}+T_{c a} \tag{3.3}
\end{equation*}
$$

If we assume that each bidirectional switch carries same amount of the output current (this assumption is discussed further in Chapter 4) then;

$$
\begin{equation*}
T_{A a}=T_{B a}=T_{C a}=\frac{T_{a}}{3} \tag{3.4}
\end{equation*}
$$



Figure 3.3 Single Output Phase of the Matrix Converter

As shown in Figure 3.3 while $S_{\text {Ast }}$ and $D_{\text {Aat }}$ carry the positive part of the $I_{A a}$ waveform, $S_{A_{R}}$ and $D_{A_{A}}$ carry the negative part. Assuming that the positive and negative current waveforms are the same shape, the mean current for each device is half of the total mean current for the switch combination and therefore;

$$
\begin{align*}
& T_{A a+}=T_{A a-}  \tag{3.5}\\
& T_{A a}=T_{A a^{+}}+T_{A a-}
\end{align*}
$$

Therefore, the mean value of the positive part of the output current waveform is the sum of the three currents in the switches carrying the positive part of the switch current.

$$
\begin{align*}
& T_{a+}=T_{A a+}+T_{B a+}+T_{C a+} \\
& T_{A a+}=\frac{T_{a+}}{3} \tag{3.6}
\end{align*}
$$

Assuming a sinusoidal output current the mean value of the positive part of the output current waveform is;

$$
\begin{equation*}
T_{a+}=\frac{I_{a m}}{\pi} \tag{3.7}
\end{equation*}
$$

where $\mathrm{I}_{\mathrm{am}}$ is the maximum value of the output current.
The device current rating can be found by substituting Equation 3.7 into Equation 3.6;

$$
\begin{align*}
& T_{A a+}=\frac{I_{a m}}{3 \pi}=\frac{I_{a_{a}} \sqrt{2}}{3 \pi}  \tag{3.8}\\
& T_{A a^{*}}=\frac{I_{a_{a}}}{6.66}
\end{align*}
$$

The full load current of the matrix converter is 7.2 A . Hence, the mean current for both the IGBT and the diode using Equation 3.8 is;

$$
I_{d}=1.06 \mathrm{~A}
$$

The devices used in the prototype are IRGBC20U ultrafast IGBTs rated at 13 A, 600 V at $25^{\circ} \mathrm{C}$ and BYT12-800 fast recovery diodes rated at $12 \mathrm{~A}, 800 \mathrm{~V}$ with 50 nS recovering time at $25^{\circ} \mathrm{C}$. These ratings are significantly higher than the calculated stresses for 5 main reasons:

1) The devices must be derated for operating temperatures above $25^{\circ} \mathrm{C}$.
2) Under certain conditions (as discussed further in Chapter 4) the current stress is not distributed evenly amongst the devices.
3) The simple snubber design used in the prototype results in high peak currents in the devices at turn-on which the device must be able to handle.
4) The delay introduced between the drive signals of the devices causes voltage overshoot across the devices which must be controlled by the snubber circuit discussed in Section 3.6.
5) Slip and vector control techniques for the induction motor as discussed in Chapter 6 and 7, respectively result in high transient output currents which exceed the steady state rating (approximately $150 \%$ ).

### 3.5 Gate Drive Circuit

Each bidirectional switch in the converter requires an isolated drive signal. The isolation can be provided using either pulse transformers or opto-isolators. Optoisolators can work with unrestricted duty cycle ratios but a separate isolated power supply is required for each switching element resulting in a very large component count and cost for the drive circuitry. In addition, the opto-coupler can suffer from noise immunity problems and the isolated power supplies require careful design to avoid capacitive coupling problems due to the large dv/dt encountered. The main problem arising with pulse transformers is that the need for volt-second balance makes it difficult to obtain satisfactory operation with a wide range of duty cycles. With isolated gate devices such as IGBTs or MOSFETs however, this difficulty can be overcome if use is made of the inherent charge storage capability of the device input capacitance. A gate drive circuit using this principle has been developed for the prototype converter. The basic circuit diagram is shown in Figure 3.4. This circuit has a low component count, does not require any isolated power supplies and operates successfully with a wide range of duty cycle.

### 3.5.1 Circuit Operation

The gate drive circuit uses two low power MOSFETs ( $\mathrm{Q}_{1}$ andQ $\mathrm{Q}_{2}$ ) such as IRFD110. The principle of the circuit's operation is shown in Figure 3.5. Figure 3.5(a) is the desired gate signal generated by the control logic for the bidirectional


Figure 3.4 Gate Drive Circuit
switch pair comprising the IGBTs $\mathrm{S}_{\mathrm{Aa}+}$ and $\mathrm{S}_{\mathrm{Aa}-}$. When this signal is applied to the primary of the transformer, $\mathrm{T}_{1}$, the voltage is initially supported by the changing core flux until saturation occurs as illustrated in Figure 3.5(b). After saturation occurs the winding voltages remain at zero until the core is brought out of saturation by the negative portion of the signal. Saturation occurs in the opposite sense when the negative pulse exceeds the volt-second capability of the core. The voltage waveform across the transformer primary (and secondary) is therefore a series of short pulses of alternate polarity aligned with the on and off commands from the control logic.

During the positive part of the secondary waveform the combinated gate capacitance of $S_{\text {Ast }}$ and $S_{A 2}$ is charged through $Q_{2}$ and the intrinsic diode of $Q_{1}$. When the secondary voltage falls to zero the intrinsic diode of $Q_{1}$ is reverse biassed and the combinated gate capacitance holds the charge allowing $S_{\text {Aat }}$ and $S_{\text {Aa- }}$ to remain on for a time dictated by the gate leakage current. If this time is not sufficient, it can be extended by adding extra capacitance in parallel with the gate. It should be noted that the maximum on-time for each device is clearly defined in the matrix converter by the modulation strategy and the switching frequency.


Figure 3.5 Principle of Gate Drive Circuit
$S_{\text {Aat }}$ and $S_{A a-}$ are turned off when the transformer secondary voltage goes negative causing the combined gate capacitance to charge negatively through $Q_{1}$ and the intrinsic diode of $Q_{2}$. The intrinsic diode of $Q_{2}$ blocks when the transformer secondary voltage returns to zero and the gate capacitance is left with a negative charge until the next command to turn on is received and this gives good noise immunity.

### 3.5.2 The Gate Drive Circuit Performance

Figure 3.6 shows the performance of the gate drive circuit. Back to back zener diodes connected across the secondary coil are used to limit the peak. voltage to 18 V . In addition, a damping resistor is connected in parallel with the secondary
coil. The practical results show that the gate drive circuit has a 150 nS delay time with 50 nS rise and fall times. The results also show that the negative charge during the off period provides excellent noise immunity and ensures that spurious turn-on is not possible.


Figure 3.6 Practical Waveforms from the Gate Drive Circuit

### 3.6 Snubber Circuit Design

The square safe operating area of the IGBT for switch mode operation minimizes the need for snubber circuits in most applications such as the voltage source inverter. However, it is necessary to use a snubber circuit in the matrix converter due to the absence of freewheeling paths. In the matrix converter the load current is always commutated from one controlled switch to another. This is in direct contrast to a conventional voltage source inverter where commutation is always from a controlled device to a complementary freewheeling diode or vice-versa. In a conventional inverter a time delay can be easily introduced between drive signals for complementary devices in order to avoid simultaneous conduction. During this delay time the inductive load current is taken over by a freewheeling diode. There is no
such freewheeling path in the matrix converter but it is still necessary to introduce a delay between drive signals to avoid a short circuit of the input lines. During this delay time the inductive load current is taken over by a snubber circuit. In the converter a small R-C turn-off snubber connected across to each bidirectional switch is used to limit the device voltage to an appropriate level. Unfortunately, this simple snubber circuit arrangement has the disadvantage of high current stress in the devices at turn-on. The main focus of this project was to develop a complete closed loop control induction motor drive and therefore the problem of optimised snubber design was not pursued further. It is recognised that a more sophisticated snubber design or elimination of the snubber [37] would be required for operation at higher powers and/or higher switching frequencies.

### 3.6.1 Analysis of the Snubber Circuit

One output phase of the matrix converter shown in Figure 3.7 has been considered for the analysis. A delay of 500 nS is introduced between drive signals to avoid a short circuit of the input lines. It has been assumed that the 3-phase input voltage and the output current of the converter stay constant during one period of the switching frequency. In addition, stray inductances in the commutation path are ignored. The worst case operating condition for the snubber circuit occurs when maximum output current flows when any one of the line to line input voltages is a maximum. This situation is depicted in Figure 3.7. The snubber circuit operation is analysed for a complete switching sequence assuming initially that $\mathrm{S}_{\mathrm{Aa}}$ is on followed by commutation to $S_{B a}$ then to $S_{C A}$ and finally back to $S_{A A}$.

The analysis is started assuming that the bidirectional switch, $\mathrm{S}_{\mathrm{Aa}}$ has been on and the switches $\mathrm{S}_{\mathrm{Ba}}$ and $\mathrm{S}_{\mathrm{ct}}$ have been off for some time. This condition can be represented by the equivalent circuit shown in Figure 3.8(a). During this interval the output current is supplied by $S_{A d}$ bidirectional switch and the voltages across the bidirectional switches stay at constant level. Figure 3.8(b) shows the equivalent circuit for the instant in which $S_{A a}$ is just turned-off. During this interval where all
three bidirectional switches are off, the load current is supplied by the three snubbers. If the equivalent circuit shown in Figure 3.8(b) is analysed, it is found that the snubber currents are equal and add to give the output current. Assuming a maximum output current of 10 A peak the snubber currents are given by;

$$
I_{S 1}=I_{s 2}=I_{s 3}=3.33 \mathrm{~A}
$$

Therefore, the voltages across the snubber resistance and capacitance during this interval are given by;

$$
\begin{align*}
& V_{R}=I_{s} R \\
& V_{c}=\frac{I_{s}}{C} t+V_{c}(o) \tag{3.9}
\end{align*}
$$

where, $I_{S}$ is the snubber current
$\mathrm{V}_{\mathrm{C}}$ is the capacitor voltage
$V_{c}(0)$ is the initial capacitor voltage
Since the snubber current is constant during this interval the voltages across the snubber resistances remain constant at 70 V . The change of the snubber capacitance voltage after the 500 nS delay time can be calculated by using Equation 3.9.

$$
\Delta V_{C}=\frac{3.33}{0.022 *(10 E-6)} 0.5 *(10 E-6)=76 \mathrm{~V}
$$

This condition is shown in Figure 3.8(c). Figure 3.8(d) shows the equivalent circuit for the instant at which $\mathrm{S}_{\mathrm{Ba}}$ is turned-on. Again, if this condition is analysed, the snubber currents can be found to be;

$$
\begin{equation*}
I_{S 1}=I_{S 2}=I_{S 3}=13.1 e^{-\frac{1}{R C}} A \tag{3.10}
\end{equation*}
$$

It is important to note from Figure 3.8(d) that, the snubber current, $\mathrm{I}_{\mathrm{S} 2}$ is taken over by the switch, $\mathrm{S}_{\mathrm{Ba}}$. This explains why this snubber arrangement causes an increase in the device current rating mentioned earlier in this chapter. This also increases the switching losses. Figure 3.9(a) shows the instant after $S_{B a}$ has been on for some time. During this interval, the load current is supplied by $\mathrm{S}_{\mathrm{Ba}}$. The analysis can be
continued until the end of the switching period as shown in Figure 3.9. In Figure 3.9 the equivalent circuits are valid at the following times:
(a) After $\mathrm{S}_{\mathrm{Ba}}$ has been on for some time
(b) Instant $\mathrm{S}_{\mathrm{Ba}}$ is just turned-off
(c) 500 nS later after $\mathrm{S}_{\mathrm{Ba}}$ is turned-off
(d) Instant $\mathrm{S}_{\mathrm{Ca}}$ is just turned-on
(e) After $S_{C_{a}}$ has been on for some time
(f) Instant $S_{C_{a}}$ is just turned-off
(g) 500 nS later after $\mathrm{S}_{\mathrm{Ca}}$ is turned-off
(h) Instant $S_{A z}$ is just turned-on
(i) After $S_{A s}$ has been on for some time

As can be seen from Figure 3.9(h), the maximum device current reaches 54 A. The devices used in the prototype converter are able to handle this peak current. From this analysis the worst case the snubber current waveform, $\mathrm{I}_{31}$ and the device voltage, $\mathrm{V}_{\mathrm{A}}$ shown in Figure 3.10 can be obtained. Unfortunately, it proved very difficult to obtain practical results for the snubber waveforms at full power due to interference between the measuring equipment and the control circuitry. For this reason, the previous analysis was repeated for an output current of 4 A and practical results for this condition were taken as shown in Figure 3.11 and 3.12. Very good correlation between the theoretical and measured results were obtained at 4 A suggesting that the analysis can be used with confidence to predict the device stresses at 10 A . The analysis results show that the design snubber parameters for a 500 nS delay are suitable to keep the device voltage and current stresses below the device ratings.


Figure 3.7 Snubber Circuits with the Bidirectional Switches


Figure 3.8 Equivalent Circuits for Snubber Circuit Analysis


Figure 3.9 Equivalent Circuits for Snubber Circuit Analysis


Figure 3.10 Worst Case Waveforms of Snubber Current and Device Voltage for Switch $\mathrm{S}_{\mathrm{As}}$


Figure 3.11 Experimental Snubber Current and Device Voltage at Turn-on


Figure 3.12 Experimental Snubber Current and Device Voltage at Turn-off

### 3.7 Construction of the Power Circuit

The large number of devices in the matrix converter and the complicated nature of the commutation path mean that the layout of the power circuit is critical to achieving correct operation [42]. For an experimental converter it is important to be able to get easy access to all of the devices to make measurements and to replace devices in the event of failure. There is a conflicting requirement between ease of access and compactness of construction. For this reason the prototype converter has been built as three modules, one for each output phase. Each module is constructed in a very compact fashion on its own heatsink and includes all the power devices, gate drives, decoupling capacitors and snubbers. The layout of the power devices on the heatsink is shown in Figure 3.13. Sufficient space is left between modules to allow easy access for measurements to be made and for components to be replaced.

In this way the critical commutation path between devices sharing the same output phase can be kept very short by decoupling the input lines at each module
with $0.47 \mu \mathrm{~F}$ capacitors. Larger $16 \mu \mathrm{~F}$ capacitors for filtering purposes are placed where the input lines for the three modules are connected. Each module is self contained and it is possible to run them individually as three phase to single phase converters for test and development purposes. Since it is assumed that the converter will supply an inductive load, no filtering was considered necessary at the output of the converter. During testing however, it was found that the very high rates of change of voltage at the output caused significant current spikes due to the capacitance of the cable supplying the load even though this was only a few metres long. This problem was cured by placing small inductors in series with the converter output. A photograph of the practical converter is shown in Figure 3.14.


Figure 3.13 Location of the Power Devices (a) Top View (b) Bottom View


Figure 3.14 A Photograph of the Power Circuit

### 3.8 Conclusions

The possible configurations of the bidirectional switch from unidirectional switching elements have been discussed and a suitable bidirectional switch configuration which requires one control signal and has a low forward voltage drop has been chosen. An overview of the advances in the semiconductor technology has been presented. The IGBT has been chosen as the most suitable controllable device for the matrix converter. The minimum device ratings for the unidirectional devices
have been calculated by considering the operation of the bidirectional switches in the matrix converter. A gate drive circuit which does not require an additional isolated power supply has been developed and tested. A simple R-C snubber circuit has been used to limit the device voltage to an appropriate level. The snubber circuit has been analyzed and the experimental results have been presented to confirm its correct operation. The problems associated with the construction of the converter have been addressed and suitable solutions have been given.

## CHAPTER 4

## THE CONVERTER LOSSES PROTECTION AND TESTING

### 4.1 Introduction

This chapter investigates the semiconductor losses in the matrix converter. Regarding these semiconductor losses the required heat sink for each output phase is designed to dissipate the heat away from the junction region.

A voltage clamp circuit at the output of the converter is used to protect the devices against severe overvoltages. A simple over-current protection circuit based on overcurrent sensing is designed. An L-C filter is designed to reduce the harmonics at the input side.

The matrix converter power circuit is tested and the results are presented to confirm its correct operation. The efficiency of the prototype converter is measured and the total converter losses are compared with the calculated losses.

### 4.2 Losses in the Switching Devices

The total semiconductor loss in the matrix converter is the sum of the conduction losses, $\mathrm{P}_{\mathrm{c}}$ and switching losses, $\mathrm{P}_{\mathbf{z}}$. The gate losses and off-state losses due to the leakage current are ignored since they are negligible. The conduction losses are the major component at low switching frequencies, but switching losses will be significant at high operating frequencies. The conduction losses are due to the on-state voltage across the IGBT and the diode when they are conducting. The switching losses are due to the imperfect switching of the devices.

### 4.2.1 Conduction Losses

This section considers the calculation of the conduction losses in the matrix converter. The forward voltage drop across the IGBT and the diode when they are conducting is a function of collector current and the junction temperature, $\mathrm{T}_{\mathrm{j}}$.


Figure 4.1 One Output Phase of the Matrix Converter

One output phase of the matrix converter shown in Figure 4.1 is considered with a sinusoidal output current to calculate the conduction losses. To determine the total forward voltage drop $\left(\mathrm{V}_{\mathrm{f}}\right)$ as a function of current the diode is represented as a fixed voltage $\left(V_{d}\right)$ in series with a slope resistance $\left(R_{d}\right)$ and an expression for the forward characteristic of the IGBT obtained from the manufactures literature [43] is used. Hence, the forward voltage drop across the each bidirectional switch in Figure 4.1 is the sum of the voltage drop across the IGBT and the diode.

$$
\begin{align*}
& V_{f}=V_{f}+V_{f d}  \tag{4.1}\\
& V_{f}=\left(V_{T}+R_{T} I^{\beta}\right)+\left(V_{d}+R_{d}\right)
\end{align*}
$$

Where $V_{T}, R_{T}, V_{d}, R_{d}$ and $\beta$ are constant at a particular temperature and can be found
in the data sheet of the devices [43-44].
The instantaneous power dissipation in each switch is;

$$
\begin{align*}
& P(t)=V_{f}(t) I(t)  \tag{4.2}\\
& P(t)=\left(V_{d}+V_{T}\right) I(t)+R_{d} I^{2}(t)+R_{T} I^{\beta+1}(t)
\end{align*}
$$

Consider the switches $S_{A+t}, S_{\text {Bat }}$ and $S_{C a+}$ in Figure 4.1. The energy dissipated in these switches in any time interval $t_{1} \rightarrow t_{2}$ is given by;

$$
\begin{equation*}
E=\int_{i_{1}}^{t_{2}}\left[\left(V_{d}+V_{T}\right)\left(I_{A a+}+I_{B a+}+I_{C a+}\right)+R_{d}\left(I_{A a+}^{2}+I_{B a+}^{2}+I_{C a+}^{2}\right)+R_{T}\left(I_{A a+}^{\beta+1}+I_{B a+}^{\beta+1}+I_{C a+}^{\beta+1}\right)\right] d t \tag{4.3}
\end{equation*}
$$

These particular switches only conduct during the positive half cycle of the output current and only one switch conducts at a particular time. Therefore;

$$
\left.\begin{array}{ll}
I_{A a+}+I_{B a+}+I_{C a+}=I_{o m} \sin \left(\omega_{o} t\right)  \tag{4.4}\\
I_{A a+}^{2}+I_{B a+}^{2}+I_{C a+}^{2}=I_{o m}^{2} \sin ^{2}\left(\omega_{o} t\right) \\
I_{A a+}^{\beta+1}+I_{B a+}^{\beta+1}+I_{C a+}^{\beta+1}=I_{o m}^{\beta+1} \sin ^{\beta+1}\left(\omega_{o} t\right)
\end{array}\right\} \quad 0<t \leq \frac{\pi}{\omega_{o}}
$$

Where $I_{o m}$ is the peak value of the output current.
Hence, the total energy lost by these three switches in one cycle of the output current is found by substituting Equation 4.4 into Equation 4.3;

$$
\begin{equation*}
E=\int_{0}^{\pi / \omega_{o}}\left[\left(V_{d}+V_{T}\right) I_{o m} \sin \left(\omega_{o} t\right)+R_{d o m}^{2} \sin ^{2}\left(\omega_{o} t\right)+R_{T} I_{o m}^{\beta+1} \sin ^{\beta+1}\left(\omega_{o} t\right)\right] d t \tag{4.5}
\end{equation*}
$$

From Equation 4.5 it can be seen that the total energy loss is independent of the switching pattern and the load displacement factor. The average power loss, $\mathrm{E} /\left(2 \pi / \omega_{0}\right)$ can be obtained by solving Equation 4.5.

$$
\begin{equation*}
P_{c}=\frac{E}{\left(2 \pi / \omega_{o}\right)}=\frac{I_{o m}}{\pi}\left(V_{d}+V_{T}\right)+\frac{I_{o m}^{2}}{4} R_{d}+\frac{I_{o m}^{\beta+1} R_{T}}{\left(2 \pi / \omega_{o}\right)} \int_{0}^{\pi / \omega} \sin ^{\beta+1}\left(\omega_{o} t\right) d t \tag{4.6}
\end{equation*}
$$

The integral in Equation 4.6 can only be solved through numerical routines for particular values of $\beta$. The constants in Equation 4.6 are obtained from the data sheet of the devices as given below;

For IRGBC20U: $\quad V_{T}=1.2 \mathrm{~V}, \quad \mathrm{R}_{\mathrm{T}}=0.16 \Omega, \quad \beta=1.04$ (at $\mathrm{T}_{\mathrm{j}}=150^{\circ} \mathrm{C}$ )
For BYT12PI-800: $\mathrm{V}_{\mathrm{d}}=1.47 \mathrm{~V}, \quad \mathrm{R}_{\mathrm{d}}=0.026 \Omega\left(\right.$ at $\mathrm{T}_{\mathrm{j}}=100^{\circ} \mathrm{C}$ )
In Equation $4.6 \beta+1$ is taken as 2 . This assumption is valid for the device used since $\beta$ is very close to 1 . Therefore, substituting the constants into Equation 4.6;

$$
\begin{equation*}
P_{c}=0.85 I_{o m}+0.0465 I_{o m}^{2} \tag{4.7}
\end{equation*}
$$

The total conduction losses for the entire converter is 6 times the power in Equation 4.7. Hence,

$$
\begin{equation*}
P_{c}=5.1 I_{o m}+0.279 I_{o m}^{2} \tag{4.8}
\end{equation*}
$$

The total conduction losses for the maximum output current, $\mathrm{I}_{\mathrm{om}}=10 \mathrm{~A}$ can be calculated by using Equation 4.8;

$$
\begin{aligned}
& P_{c}=5.1 * 10+0.279 * 10^{2} \\
& P_{c}=78.9 \mathrm{~W}
\end{aligned}
$$

By using a simple simulation model it has been shown that for situations where the input and the output frequencies are asynchronous, the conduction loss is shared almost equally amongst the devices. However, for particular operating frequencies (for instance $f_{i}=f_{0}=50 \mathrm{~Hz}$ ) the power loss in the devices is not shared equally. Under this condition where $q=0.85, f_{i}=f_{o}=50 \mathrm{~Hz}$ and load displacement factor $=1$, three of the switches $S_{\mathrm{As}}, \mathrm{S}_{\mathrm{Bb}}$ and $\mathrm{S}_{\mathrm{Cc}}$ dissipate about $85 \%$ of the total loss. Obviously, this increases the device current rating and as discussed in Chapter 3 is the one of the reasons why the IGBT and the diode current ratings are higher than the calculated stresses.

### 4.2.2 Switching Losses

The product of the switching frequency, $f_{s}$ and the switching energy loss per pulse, $\mathrm{E}_{\text {loss }}$ gives the switching losses per switch in the matrix converter.

$$
\begin{equation*}
P_{z}=f_{z} . E_{\text {loss }} \tag{4.9}
\end{equation*}
$$

The switching losses occur when the devices turn on and off. In this converter the current is always commutated from a conducting device to the R-C snubber circuit or vice-versa. If we assume that the voltage across the snubber capacitor remains constant during the relatively short switching times, the switching locus for the device is resistive and consequently the switching losses are very low.

To calculate the turn-off loss consider the device $\mathrm{S}_{\mathrm{Aa}}$ in Figure 4.1. Just prior to turn-off this device carries the output current $I_{a}$. At the end of turn off, $I_{a}$ is carried by the three snubber circuits on output phase a and the voltage across $S_{A 2}$ is therefore ${ }_{\mathrm{I}}^{\mathrm{a}} \mathrm{R} / 3$ since the snubber capacitor was initially discharged. Assuming the device current changes linearly during turn-off the switching waveforms are as shown in Figure 4.2


Figure 4.2 The Current and Voltage Waveforms of the Device at Turn-off

The energy loss is therefore given by;

$$
\mathrm{S}_{\mathrm{Aa}} \text { turn-off loss }=\frac{I_{a}^{2} R t_{o f f}}{18}
$$

where; R is the snubber resistor ( $21 \Omega$ )
$\mathrm{t}_{\mathrm{off}}$ is the fall time of the device $(200 \mathrm{nS})$
Assuming that the output current is constant during any particular switching sequence the total turn-off energy loss for the output phase a switches will be three times this value. The total energy loss for the entire converter during any particular sequence due to device turn-off can be found by considering the other phases and is therefore given by;

$$
\text { Total turn-off loss }=\frac{R t_{o f f}}{6}\left(I_{a}^{2}+I_{b}^{2}+I_{c}^{2}\right)
$$

However, if we assume that the output currents are sinusoidal and form a balanced 3-phase set then;

$$
\begin{equation*}
I_{a}^{2}+I_{b}^{2}+I_{c}^{2}=3 I_{o}^{2} \tag{4.10}
\end{equation*}
$$

where $I_{0}$ is the rms output current.
Hence the total turn-off energy loss during each sequence is constant and is given by;

$$
\begin{equation*}
\text { Total turn-off loss }=\frac{R t_{o f f} I_{o}^{2}}{2} \tag{4.11}
\end{equation*}
$$

In the prototype converter the switching frequency (sequence repeat rate) is 2 kHz and the power loss (using Equation 4.9) is therefore;

$$
\begin{equation*}
P_{o f f}=\frac{21 * 200 * 10^{-9} *(7.2)^{2} * 2000}{2}=0.22 \mathrm{~W} \tag{4.12}
\end{equation*}
$$

Consequently the turn-off loss is negligible.
To determine the turn-on loss consider the same device $S_{A a}$. Just prior to turnon the output current $I_{a}$ is flowing through the three snubber circuits in parallel and the snubber capacitor associated with $S_{A a}$ is charged to $\left(V_{A C}+\Delta V\right)$ as explained
earlier in Section 3.6.1. The device voltage is therefore $\left(\mathrm{V}_{\mathrm{AC}}+\Delta \mathrm{V}\right)$ plus the drop across the snubber resistor $\left(I_{2} R / 3\right)$. At the end of turn-on the device carries the load current ( $\mathrm{I}_{2}$ ) plus the peak snubber discharge current $3 *\left(\mathrm{~V}_{\mathrm{AC}}+\Delta \mathrm{V}\right) / \mathrm{R}$. Assuming again that the device current changes linearly during switching the waveforms are as shown in Figure 4.3.


Figure 4.3 The Current and Voltage Waveforms of the Device at Turn-on

The energy loss is therefore;

$$
\begin{equation*}
\mathrm{S}_{\mathrm{A} \mathrm{a}} \text { turn-on loss }=\left(I_{a}+\frac{3\left(V_{A C}+\Delta V\right)}{R}\right)\left(\left(V_{A C}+\Delta V\right)+\frac{I_{a} R}{3}\right) \frac{t_{o n}}{6} \tag{4.13}
\end{equation*}
$$

where; $\mathrm{t}_{\mathrm{on}}$ is the rise time of the device ( 100 nS )
The loss for the other two switches on the same output phase $\left(\mathrm{S}_{\mathrm{Ba}}\right.$ and $\left.\mathrm{S}_{\mathrm{Ca}_{a}}\right)$ can be found by replacing $V_{A C}$ with $V_{B A}$ and $V_{C B}$ respectively. Using the following results:

$$
\begin{aligned}
& V_{A C}+V_{B A}+V_{C B}=0 \\
& V_{A C}{ }^{2}+V_{B A}{ }^{2}+V_{C B}^{2}=3 V_{L}^{2} \\
& \Delta V=\frac{I_{a} \tau}{3 C}
\end{aligned}
$$

where; $\tau$ : Delay time between the drive signals of the devices ( 500 nS )

$$
\mathrm{C}: \text { Snubber capacitance }(0.022 \mu \mathrm{~F})
$$

and simplifying the total loss for output phase $a$ is given by:

Phase a turn-on loss $=t_{o n}\left[\frac{3 V_{L}^{2}}{2 R}+I_{a}^{2}\left(\frac{\tau^{2}}{6 R C^{2}}+\frac{R}{6}+\frac{\tau}{3 C}\right)\right]$
To calculate the total turn-on loss for the entire converter we consider the other phases (replacing $I_{a}$ by $I_{b}$ and $I_{c}$ respectively) and again use the result in Equation 4.10 to give the total loss in one switching sequence as;

Total turn-on loss $=t_{o n}\left[\frac{9 V_{L}^{2}}{2 R}+I_{o}^{2}\left(\frac{\tau^{2}}{2 R C^{2}}+\frac{R}{2}+\frac{\tau}{C}\right)\right]$
The turn-on power loss taking into account the switching frequency is therefore;

$$
\begin{align*}
P_{o n} & =\left[\frac{9 *(250)^{2}}{2 * 21}+(7.2)^{2}\left(\frac{\left(500 * 10^{-9}\right)^{2}}{2 * 21 *\left(0.022 * 10^{-6}\right)^{2}}+\frac{21}{2}+\frac{500 * 10^{-9}}{0.022 * 10^{-6}}\right)\right]  \tag{4.14}\\
& * 100 * 10^{-9} * 2000=3.15 \mathrm{~W}
\end{align*}
$$

It should be noted that the majority of the turn-on energy loss comes from the snubber capacitor and this will be allowed for in the snubber loss calculation to determine the total converter losses. The figure calculated above however allows the loss in the devices to be used for heatsink calculations.

### 4.2.3 Heat Sink Design

Each output phase of the prototype converter has been built as a separate module so that it is possible to run them individually as three phase to single phase converters for test and development purposes. Therefore each module has its own heatsink. The heatsink used in the one output phase of the prototype converter is represented in Figure 4.4. Since all the switching devices are located around the centre of the disc, it is necessary to calculate the temperature difference between the centre and the edge of the disc. The thermal resistance of an element length 1 and area A is given by;

$$
\begin{equation*}
\theta=\frac{l}{\lambda \cdot A} \quad{ }^{\circ} C / W \tag{4.15}
\end{equation*}
$$

Where;

$$
\lambda=180 \mathrm{~W} \mathrm{~m}^{-1}{ }^{\circ} \mathrm{C}^{-1}
$$



Figure 4.4 The Representation of the Heatsink

Therefore, splitting the disc into a series of circular elements and integrating the thermal resistance between the centre of the disc and the peripheral is given by;

$$
\begin{aligned}
& \theta_{d i f}=\int_{0}^{9.25 E-2} \frac{d r}{\lambda(2 \pi r d)}=\frac{1}{14.7}[\ln r]_{0}^{9.25 E-2} \\
& \theta_{d i f}=6.610^{-3} \quad{ }^{\circ} \mathrm{C} / W
\end{aligned}
$$

The temperature difference;

$$
\begin{align*}
& T_{d i f}=\theta_{d i f} P  \tag{4.16}\\
& T_{d i f}=\left(6.6 \quad 10^{-3}\right)(27.42)=0.18 \quad{ }^{\circ} \mathrm{C}
\end{align*}
$$

Hence the temperature drop across the disc is negligible even if it is assumed that all the heat loss occurs at the outer edge.

The required heatsink rating for each output phase can be calculated using the thermal equivalent circuit for a bidirectional switch given in Figure 4.5.


Figure 4.5 The thermal equivalent circuit for a bidirectional switch

## In Figure 4.5;

$\mathrm{P}_{\text {loss }}$ : Total semiconductor losses in one bidirectional switch
$P_{j \perp} \quad:$ Power loss in the IGBT
$P_{j, d}:$ Power loss in the diode
$\mathrm{R}_{\mathrm{jc}, \mathrm{d}}$ : Junction to case thermal resistance of the diode $\left(4^{\circ} \mathrm{C} / \mathrm{W}\right)$
$\mathrm{R}_{\mathrm{cs,d}}$ : Case to sink thermal resistance of the diode $\left(0.5^{\circ} \mathrm{C} / \mathrm{W}\right)$
$\mathrm{R}_{\mathrm{j}, \mathrm{I}, \mathrm{I}}$ : Junction to case thermal resistance of the IGBT ( $2.1^{\circ} \mathrm{C} / \mathrm{W}$ )
$\mathrm{R}_{\mathrm{cs,I}}$ : Case to sink thermal resistance of the IGBT $\left(0.5^{\circ} \mathrm{C} / \mathrm{W}\right)$

The thermal resistances of the devices are obtained from the data sheets [4344]. The power loss in the IGBT and the diode can be obtained from Equations 4.6, Equations 4.12 and 4.14 as given in Figure 4.5. The switching losses in the diode is ignored. The total power loss for one bidirectional switch, $\mathrm{P}_{\text {loss }}$ is the sum of the conduction loss and the switching loss. The junction temperature of the diode is taken as $100^{\circ} \mathrm{C}$ although it does not reach to that value. The temperature difference between the sink and the junction of the diode, $\Delta T$ can be calculated using Figure 4.5;

$$
\begin{aligned}
& \Delta T=\left(R_{j c, d}+R_{c s, d}\right) P_{j d} \\
& \Delta T=(4+0.5) 3.55=15.98 \quad{ }^{\circ} \mathrm{C}
\end{aligned}
$$

Hence, the sink temperature is;

$$
\begin{aligned}
& T_{\text {sink }}=T_{j, d}-\Delta T \\
& T_{\text {sink }}=100-15.98=84.02 \quad{ }^{\circ} \mathrm{C}
\end{aligned}
$$

The junction temperature of the IGBT is;

$$
\begin{aligned}
& T_{j, I}=T_{\text {sink }}+\left(R_{j c, J}+R_{c s, J}\right) P_{j, I} \\
& T_{j, I}=84.02+2.6 * 5.58=98.53 \quad{ }^{\circ} \mathrm{C}
\end{aligned}
$$

and the heatsink rating for one bidirectional switch (assuming an ambient of $30^{\circ} \mathrm{C}$ ) is;

$$
\begin{aligned}
& \Theta=\frac{T_{\text {sink }}-T_{\text {amb }}}{P_{\text {loss }}} \\
& \Theta=\frac{84.02-30}{9.16}=5.9 \quad{ }^{\circ} \mathrm{C} / \mathrm{W}
\end{aligned}
$$

Since the heatsink contains three bidirectional switches, the required heatsink rating is one third of the value above;

$$
\Theta_{s}=\frac{5.9}{3}=1.97 \quad{ }^{\circ} \mathrm{C} / W
$$

It is impossible to calculate the heatsink rating accurately for the disc since it depends on many variables. However, the disc size was compared with a heatsink of the required rating and this suggested that the disc was easily large enough. The prototype converter was also operated for sufficient time at full power for the disc temperature to stabilise and it was observed that the heatsink temperature stayed below that calculated above.

### 4.3 Snubber Losses

The snubber circuit discussed in Chapter 3 causes power loss in the matrix converter. This loss occurs when any one of the switching devices turns-on. Additional snubber loss occurs during the delay time in which all devices are off. The snubber loss in the converter can be calculated by following the same analysis method used for calculating the snubber parameters in Chapter 3. These calculations are given in Appendix A. The total snubber loss is given by;

$$
\begin{equation*}
P_{s n u b}=f_{s}\left[3 I_{o}^{2}\left(R \tau+\frac{\tau^{2}}{2 C}\right)+\frac{27 C V_{L}^{2}}{2}\right] \tag{4.17}
\end{equation*}
$$

where; $f_{s}$ is the switching frequency ( 2 kHz )
$\tau$ is the delay time ( 500 nS )
R and C are the snubber parameters ( $21 \Omega$ and $0.022 \mu \mathrm{~F}$, respectively)
$\mathrm{V}_{\mathrm{L}}$ is the rms input line voltage ( 250 V )
$\mathbf{I}_{0}$ is the rms output current
As it can be seen from Equation 4.17 the snubber loss in the matrix converter is independent of input and output frequencies and displacement factors. The snubber loss mainly depends on the input voltage, the snubber capacitance and the switching frequency.

The total snubber loss can be found by substituting the constants into Equation 4.17. Hence,

$$
\begin{equation*}
P_{s n u b}=0.0744 I_{o}^{2}+37.1 \mathrm{~W} \tag{4.18}
\end{equation*}
$$

Therefore, the snubber loss on no load is;

$$
\begin{equation*}
P_{s \text { suub }}=37.1 \mathrm{~W} \tag{4.19}
\end{equation*}
$$

and on full load;

$$
\begin{aligned}
& P_{s n u b}=0.0744 *(7.2)^{2}+37.1 \\
& P_{s n u b}=40.8 \mathrm{~W}
\end{aligned}
$$

The practical snubber loss can be roughly found by measuring the input power of the converter on no load. The input power on no load was measured to be 42 W which is in good agrement.

### 4.4 Matrix Converter Protection

The semiconductor devices in the matrix converter require effective protection against over-current and over-voltage. The absence of freewheeling paths in the converter causes difficulty in protecting the power circuit against fault conditions since the current is always commutated from one controlled device to another. For instance, if the devices are turned-off in response to a fault condition, such as overcurrent, severe over-voltage and destruction of the power circuit results because of the inductive nature of the load current despite the snubber across each switch.

Over-current in the devices can result from shoot-through (two devices on in the same output phase due to malfunction of the control/gating logic) or due to excessive output current caused by inappropriate load conditions.

### 4.4.1 Output Voltage Clamp



Figure 4.6 Output Voltage Clamp Circuit

The interruption of inductive current flow in a matrix converter produces severe overvoltages at the output since there is no freewheeling paths. The clamp circuit shown in Figure 4.6 is used to absorb the excess load energy when all the converter devices are gated off. The clamp becomes active when the converter output voltage is greater than the clamp voltage. The common ends of the capacitors in the clamp circuit are connected to the neutral of the supply in order to limit the device voltage. Therefore, the maximum device voltage in the event of failure is twice the input peak phase voltage. Otherwise, the maximum device voltage would be the sum of the input peak phase and line voltages.

### 4.4.2 Over Current Protection

The block diagram of the over-current protection circuit is shown in Figure 4.7. Over-current protection of the converter is achieved by sensing the three input line currents using Hall effect transducers described in Appendix C. The signals from these transducers are fed to an arrangement of six LM319 comparators and compared with reference voltages which correspond to the positive and negative overcurrents. The output of the comparators are input to a logic circuit which produces a latched overcurrent signal for each input line. This circuitry has six LEDs for each polarity of the three input currents to help with fault tracing. These overcurrent signals are ORed together and then ANDed with all of the gate drive signals. In the event of either positive or negative overcurrent all of the converter devices are gated off. This arrangement has been seen to work very satisfactorily for a wide range of fault conditions. The whole circuit diagram is given in Appendix B.


Figure 4.7 Block Diagram of the Over-current Protection Circuit

### 4.5 Input Filter

The input current of the matrix converter is built up from segments of the three output currents and blank intervals during which the output currents are circulated through the converter. The input current spectrum mainly consists of a supply frequency component plus high frequency components associated with the switching frequency. Distortion of the input current around the switching frequency can be easily removed by using a small L-C filter.


Figure 4.8 The Input Filter

An optimised input filter design was not pursued since the main focus of this project was to develop a complete closed loop control induction motor drive. Instead, the input filter shown in Figure 4.8 has been used which was fabricated from readily available components. The subject of optimised filter design has been considered elsewhere [45-46].

### 4.6 Power Circuit Testing

At the development stage of the power circuit a simple controller based on
the Z180 microprocessor was used to generate a fixed switching pattern according to the Venturini original control algorithm [9]. Due to the limited capability of this controller the switching frequency was restricted to 1 kHz and the output frequency was set at 50 Hz with a voltage ratio between input and output of 0.5 . The problems involved in this condition were observed and solved. Subsequently, the power circuit has been operated using a more sophisticated controller based on Transputer parallel processors. The results shown below have been obtained for various operating conditions with a passive R-L load and 2 kHz switching frequency.

Figure 4.9 shows the output line to line voltage and the output current for an output frequency of 20 Hz and a voltage ratio between output and input of 0.328 . Figures 4.10 and 4.11 show the output line to line voltage and the output current with a voltage ratio of 0.82 for output frequencies of 50 Hz and 70 Hz , respectively. Figures 4.12 and 4.13 show the input current spectrum and the output voltage spectrum for an output frequency of 50 Hz , respectively and they agreed well with the calculated spectrums [38].


Figure 4.9 Output Line to Line Voltage and Output Line Current of the Matrix Converter Operating with an Output Frequency of 20 Hz


Figure 4.10 Output Line to Line Voltage and Output Line Current of the Matrix Converter Operating with an Output Frequency of 50 Hz


Figure 4.11 Output Line to Line Voltage and Output Line Current of the Matrix Converter Operating with an Output Frequency of 70 Hz


Figure 4.12 Input Current Spectrum of the Matrix Converter Operating with an Output Frequency of 50 Hz


Figure 4.13 Output Voltage Spectrum of the Matrix Converter Operating with an Output Frequency of 50 Hz

### 4.7 Converter Efficiency Measurements

The efficiency of the prototype converter was determined by measuring the input and the output powers using a VOLTECH PM 3000 power analyzer. The converter was operated with a passive R-L load up to $60 \%$ of its rated power which was the limit of the loading system used. The test results have been taken at various output frequencies. It has been seen that the output frequency of the converter does not have any measurable influence on the efficiency. This is because the converter losses are independent of the output frequency as was shown in Sections 4.2 and 4.3.

The total converter losses at an input voltage of 250 V line and an output current of 4.25 A were measured as 81 W giving an efficiency of $89 \%$. In order to make a comparison between the experimental and theoretical results the total converter losses can be calculated for the same conditions. These losses are the sum of the snubber loss, conduction loss and switching loss ignoring the losses in the input filter.

The snubber loss in the converter is found by using Equation 4.18;

$$
\begin{aligned}
& P_{s n u b}=(4.25)^{2} 0.0744+37.1 \\
& P_{s n u b} \cong 38 \mathrm{~W}
\end{aligned}
$$

The conduction loss using Equation 4.8;

$$
\begin{aligned}
& P_{c}=5.1(\sqrt{2} 4.25)+0.279(\sqrt{2} 4.25)^{2} \\
& P_{c} \cong 41 \mathrm{~W}
\end{aligned}
$$

Since the switching loss at turn-off is negligible and the turn-on loss has been already counted in the snubber loss, the total power loss becomes;

$$
\begin{aligned}
& P_{\text {loss }}=P_{s n u b}+P_{c} \\
& P_{\text {lass }}=38+41=79 \mathrm{~W}
\end{aligned}
$$

As it can be seen, this calculated power loss agrees well with the measured
power loss of 81 W .

### 4.8 Conclusions

This chapter has investigated the losses, thermal design, protection, power circuit construction and the efficiency of the matrix converter. The required heat sink rating associated with the semiconductor losses in the converter has been calculated. It has been seen that the simple snubber arrangement used in the converter results in a high power loss compared to the total semiconductor loss. An effective protection of the power circuit against over current and voltage has been presented.

The power circuit has been tested at various operating conditions using an RL load. Reliable operation of the converter regardless of the output frequency has been achieved. An efficiency test of the prototype converter has yielded an efficiency of $89 \%$ at $60 \%$ load. It is understood that it is necessary to eliminate or reduce the snubber size for better efficiency. The total power loss of the converter has been calculated and this has been compared with the test result. It has been found that the both results are very similar.

## CHAPTER 5

## TRANSPUTER NETWORK AND CONTROL HARDWARE

### 5.1 Introduction

Previous chapters have described the design and construction of the matrix converter power circuit. In order to develop a high performance induction motor drive based on this power circuit a relatively powerful digital controller is required. In this project a network of transputers has been used to perform the control tasks. In this chapter the implementation of the transputer network and the design and operation of the interface circuits are discussed. The first section describes the recent developments in microprocessor technology and the transputer parallel processor. The next section outlines the design and operation of the interface circuits used for voltage, current and motor speed measurements and gate drive signal generation. The standard transputer serial communication link which is needed for the interface with the transputer network is also described here. In the following two sections, the deadlock protection of the prototype converter and delay and disable of the gate drive signals are described.

### 5.2 Microprocessor Technology

The recent developments in microprocessor technology has enabled designers to implement more complex control algorithms. More complicated processors can also execute instructions in a shorter time, resulting in a decrease of the system sample time, $\mathrm{T}_{5}$ (or inversely increase of the sample frequency) in which
measurements, calculations and actuation are executed, allowing the design of systems with a higher control bandwidth.

The range of processor hardware used in real-time implementation of control applications may be divided into the following categories:

1-Single conventional processor: This establishes the memory and arithmetic unit of the control system. A high interface chip count such as analogue to digital converter together with an external coprocessor are required for fast real-time processing.

2- Microcontroller: This combines a microprocessor with peripheral devices such as; timers, analog to digital converters, digital to analog converters, interrupt logic and pulse width modulation outputs. It has the advantage that these peripheral devices are on board reducing off processor chip count and increasing the speed. The Siemens SAB80C167, 16- bit microcontroller with a 10 bit A/D and sixteen PWM output channels on-board is an example of this type of processor.

3-Application specific integrated circuits (ASICS): This is an extension of the microcontroller which minimizes off processor chip count and on-chip silicon for a specific application. ASICS may be used in real time control problems of low to medium complexity.

4- Digital signal processor: A high-speed version of the single conventional processor utilising high clock rates and reduced instruction set on-chip architecture for fast arithmetic operations, mainly manipulation. It can also include digital to analog and analog to digital converters. DSPs are useful for state variable based control problems, with manipulation based strategies (eg matrix inversion, Fourier transformation).
5. Concurrent or parallel architectures: Either a number of conventional processors or specific parallel processors are used together in order to increase the speed and/or flexibility of control processing. Two or more microprocessors can be used together to implement more complex control algorithms, such as vector control for induction motors. In this case, the processors share the control task [47-49]. However, this parallel processing technique suffers from design and hardware
complexity and chip count due to the parallel bussed architectures. The transputer parallel processor developed specially as a device to be implemented in parallel processing networks does not suffer from these problems and offers an increase in speed and hence an increase in the degree of processing within the control system sample time $\mathrm{T}_{\mathbf{2}}$. The transputers are connected together by serial links to build multiprocessor systems and they do not require additional interface hardware resulting in the increase of the overall performance and flexibility.

The transputer parallel processor has been chosen to implement the control algorithms in this project. The availability of a transputer based parallel processing system and the expertise within the department at using transputers have been major factors in choosing transputers for this task.

### 5.2.1 The Transputer

The transputer is a single-chip microprocessor, specially designed for use in parallel processing systems [50]. It contains a processor, RAM, a memory interface to access external local memory, two on board timers, interrupt logic and four serial bidirectional links for communication with other transputers or transputer look alike peripherals. The structure of a transputer is shown in Figure 5.1.

A transputer can be used in a single processor system or in networks to build high performance concurrent systems. Several types of transputers such as T212 (16bit), T414 (32-bit), T800 (32-bit with on board 64-bit floating point unit) are available. Internal memory varies from 2 KBytes to 4 KBytes . The communication rate over the links is either $20 \mathrm{MBits} / \mathrm{s}$ or $10 \mathrm{MBits} / \mathrm{s}$. More information on transputers and system applications are given in several publications [50-54]. In order to gain maximum benefit from the transputer architecture the transputers and transputer based networks are configured and programmed in occam, a high level programming language developed specially for parallel processing. However, the transputers may be programmed in other high level languages, such as $C$. The description and characteristic of the occam language can be found in [55].


Figure 5.1 Block Diagram of a Transputer

Processes written in the occam language are edited, compiled and configured in a specific environment called The Transputer Development System (TDS) [51-52]. This provides the facility to develop and download concurrent programs for real-time applications.

The occam structure provides a systematic and disciplined planning of parallel algorithms with the resulting low system development time. The hardware is very simple and easily expanded. The high cost of the transputer is a major disadvantage. Transputer networks are established as versatile processors for experimental research for evaluation of real-time control techniques [56]. The computational ability of the transputer network is easily expanded to suit future research requirements in this area.

### 5.2.2 Parallel Processing for Real Time Control

The tasking philosophy for a generalised drive controller using parallel processing is illustrated in Figure 5.2. It can be seen that the processes have been


Figure 5.2 Tasking Schemat for Motor Control
subdivided into two categories as low level and high level. The low level process executes sequential procedures and requires a fast processing time. There are no true parallel constructs within the low level and all statements and procedures within the process are timed to execute within the system sample time, $\mathrm{T}_{\mathrm{s}}$. The low level process cannot be delayed otherwise it will result in loss of control. The high level process does not execute its procedures every sampling time and is therefore not synchronised to low level procedures.

When assigning processes to particular processors in a parallel processing system it is necessary to consider several factors:

1) Number of Processors Available: The minimum number of processors for a certain control task is determined by considering the required system sample time, $\mathrm{T}_{5}$ and complexity of the control task. If the number of processors available is more than the minimum number then, the control task can be efficiently distributed onto the extra processors using a pipelined technique [56], which effectively decreases the sampling time and allows the control system to be expanded for future research requirements. In this project, the system sampling time, $\mathrm{T}_{\mathrm{s}}$ has been chosen as 500
$\mu \mathrm{S}$. This is because, two transputers were available and the minimum implementation time of the control algorithms (namely vector control) using these transputers has been found as $500 \mu \mathrm{~S}$ [56]. This results in a switching frequency of 2 kHz .
2) Communication to Peripherals: Four links are available on the transputer for communicating to peripherals or another transputer. Since one of the links is already used for communicating to another transputer (unless a single transputer is used), only three links remain for peripherals. This is an important point when the processes are assigned to the processors and there are a high number of peripherals to communicate to.
3) Synchronisation: The synchronisation between different parts of the control system (eg measurement, timer board, or another transputer) is provided via communication protocol. Since the communication statements must be sequentially constructed for synchronisation, no work can be done whilst the transputer is waiting to communicate. Therefore, a process which takes longer than $\mathrm{T}_{\mathrm{s}}$ will result in loss of synchronisation, whilst a process which takes less than $T_{s}$ does not need to fully utilise the system sample time. This must be considered carefully to ensure synchronism and also maintain a high system efficiency.
4) Granularity: In order to increase the efficiency of parallel processing network it is necessary to minimize the communication time by a proper control task assignment between the processors. It is desirable to have a high ratio of calculation time to communication time (granularity) to take full advantage of the parallel processing network. Therefore, the processes should be assigned to processors in a way that the communication time is kept at a minimum level.

Figure 5.3 shows the tasking philosophy for the matrix converter induction motor drive. It was found that the measurements, control and calculation routine for the actuation signal generation are inherently sequential and can be implemented on one transputer within the system sample time, $\mathrm{T}_{\mathrm{s}}$. This time provided an adequate sample time for the sampled control design and allowed the use of a single transputer for all the low level control processing. The control system does not require background calculations or diagnostic as illustrated in Figure 5.2 but still needs the
data $\log$ and user interface. Consequently, a second transputer which is effectively a low priority process is used. However, the second transputer can provide extra "intelligence" as system complexity expands. This will be explained in detail with reference to the speed control in the next chapter.


Figure 5.3 Tasking Schemat for Matrix Converter Induction Motor Drive

The overall control system is made up of two T805 floating point transputers, $\mathrm{T}_{1}$ and $\mathrm{T}_{2}$ mounted on a TMB04 transputer mother board [57] within an IBM PC clone. The use of a transputer with a floating point unit makes code development easy since scaling factors are not required (a real number multiplication takes 600 nS ). The PC forms the host system, providing user interface, hard disk data storage facilities and access to a plotter during on line operation. The PC communicates with a serial link of transputer 1 via a parallel-serial interface on the TMB04 board.

Transputer $1\left(T_{1}\right)$, called the 'supervisor', decodes the user's instructions and passes them if necessary to the second transputer. Transputer $2\left(\mathrm{~T}_{2}\right)$ provides all the low level functions, measurement, control and switching signal generation. These functions are executed within the system sample time, $\mathrm{T}_{\mathrm{s}}(500 \mu \mathrm{~S})$ to provide a fast sampled control system. The sample time is set by using the high priority on-board
timer of transputer $T_{2}$. Synchronisation of this sample time is propagated throughout the system via communication with the measurement board, timer board and $T_{1}$ every sample period. Communication with $\mathrm{T}_{1}$ (supervisor) is executed every sample time ( $500 \mu \mathrm{~S}$ ), during which all other low level processes are executed.

Between these communications the supervising transputer, $\mathrm{T}_{1}$ executes two processes running in parallel. The first one 'overseer' which is high priority process is initiated by communication with $\mathrm{T}_{2}$ as described above. Then, it performs the speed measurement and speed control (required by slip and vector control schemes) and receives data from $T_{2}$ for monitoring utilities. An OCCAM ALT [55] construction is used with a timing process to enable the second process 'userio' to interact with 'overseer' if required. This construction ensures that if there is no input communication from userio within a set time, the input is ignored and the rest of the process 'overseer' continues. Userio is not synchronized with the low level processes. This is because the transputer does not know when a user input will occur. Therefore, the second process 'userio' always waits for the user interrupt. If it happens, the process decodes the user's instruction and passes it to the first process 'overseer' which executes the OCCAM ALT construction described above. The userio procedure can be seen as equivalent to interrupt processing used with conventional architectures. The basic flowchart diagram for these processes with occam pseudocode is given in Figure 5.4 (vector control is taken here as an example).

The host machine provides a monitoring utility which includes commands for resetting the TMB04 transputer board, user interaction (sending and receiving various data types), access to the hard disk for permanent data storage, graphics and plot utilities and loading code from the PC.

Figure 5.4 Occam Pseudo-Code for the Vector Controlled Drive

### 5.3 Interface Boards

This section describes the interface circuits used for voltage, current, motor speed measurements and gate drive signal generation. The interface circuits communicate to the transputer board via standard serial communication links.

### 5.3.1 The C011 Link Adapter

The INMOS IMS C011 Link Adapter [58] provides the communication interface for the peripheral devices on the external interface circuits. The device acts as a transputer "look alike" peripheral when connected to a transputer via a link. The C011 can be configured to operate in two modes. In Mode 1, it acts as a bidirectional serial-parallel converter, providing separate input and output ports. In Mode 2, it provides an interface between the serial communication link and a microprocessor bus via a bidirectional byte wide port. All of the link adapters employed in this project have been used in Mode 1.

### 5.3.2 Voltage and Current Measurements

The PSM voltage transposer has been used to measure the input line voltages. The transposer offers complete electrical isolation and has a large measurement range (fixed ratio 50:1). The secondary voltage obtained from the transposer is in the range $\pm 10 \mathrm{~V}$ and is passed through a low pass filter circuit (cut-off frequency 100 Hz ).

The output currents of the prototype converter are measured using two Hall effect transducers, HTP25. The transducer provides complete electrical isolation and has a 25 A measurement range with 100 kHz bandwidth. The secondary current of the transducer is converted to a voltage in the range $\pm 10 \mathrm{~V}$ using a $300 \Omega$ resistor and the signal is then buffered and passed through a low pass filter with cut-off frequency 600 Hz . The specifications for the transposer and transducer are given in Appendix C.

An analogue to digital converter board (A/D) has been built to convert the analogue voltage and current signals into the 12 bit digital format, which can be read directly by the transputer. The resultant scaling factors for voltage and current signals were 0.125 V per bit and 10 mA per bit, respectively. The circuit provides a multichannel A/D card for interfacing to a transputer [56] and is able to convert up to 8 independently addressable analogue signals into the digital forms. The data acquisition time for each sample is $15 \mu \mathrm{~S}$. The whole circuit diagram is given in Appendix D. More information on the circuit operation may be found in [56].

### 5.3.3 Speed Measurement

The motor speed signal is derived from an encoder (BEC 735) mounted directly on the shaft of the induction motor. The encoder described in Appendix C provides six channels (three complementary pair lines) A, B and C with 5 V CMOS differential line driver outputs. A and B are quadrature signals which provide information on the speed and direction of the shaft rotation. Z acts as a zero position reference.

The circuit design employs the HCTL-2016 encoder chip [59] which can take the signals $\mathrm{A}, \mathrm{B}, \mathrm{C}$ and convert them to absolute shaft position measurement. The full circuit is illustrated in Figure 5.5. Complementary line receivers are used to connect the encoder to the interface board to increase noise immunity. The overall system resolution is 10000 pulses per revolution or $0.036^{\circ}$ per bit.

Speed measurement simply requires position measurement at regular intervals. In this case, a position sample time of 5 mS has been chosen providing a speed resolution of 1.2 rpm . Further details of the encoder and circuit operation can be found in Appendix C. The total program time for speed input measurement is $35 \mu \mathrm{~S}$.

### 5.4 Timing Circuitry

The pulse widths of the switching patterns in the matrix converter must be recalculated every sample period to allow the closed-loop control of the induction motor. Hence, at every sampling time the input voltage vector position is updated by measuring the input line voltages and the pulse widths are calculated according to the demanded output frequency and amplitude. The output frequency of the converter is not synchronised to the mains input.

The control transputer provides the real-time calculation of the duty cycles for the switching patterns. The matrix converter requires nine drive signals, three per output phase. These are used to connect the three output phases to the three input phases over a switching cycle as illustrated in Figure 5.6(a) and 5.6(b). It can be seen that the transputer only needs to calculate two switching times per phase per sampling time, $\mathrm{T}_{\mathbf{s}}$. With a fixed sample time, for example, $\mathrm{t}_{\mathrm{Ca}}$ can be easily calculated as $T_{s}-t_{A a}-t_{B a}$. Rather than actually download and time out pulse $t_{C a}$, it can simply be derived from pulses $t_{A a}$ and $t_{\mathrm{Ba}}$ using gate logic as illustrated in Figure 5.7 and 5.8.

Two INTEL 8254 programmable interval timers (PITs) [60] were used to convert the calculated byte values into the pulses required for the gate drive circuits. The timing information from the control transputer is passed to the PITs using two C011 link adapters. While one of the link adapters provides the control and address signals, the other one provides the configuration data and count values.

The six counters are initiated by taking the gate pin high and the count values are then timed out using a $0.2 \mu \mathrm{~S}$ external clock circuit. The counter enable signal is synchronised to the transputer's on board timer, but actual loading of the count values can be done at any time during the previous sample period. When the gate is enabled the output of the counters goes low and when the terminal count is reached the output goes high. Therefore, these output signals, one per phase are inverted to get the correct gate drive signals.

Since all the gates are enabled together all counters start timing out at the same time. Therefore (considering output phase for example) in order to obtain the


Figure 5.5 The Speed Measurement Circuit

(a)

(b)

Figure 5.6 (a) Switch Layout, (b) Switching Pulses for Matrix Converter
correct signal from the counter output, the second counter is loaded with the count value for $S_{A a}\left(t_{A a}\right)$ plus that for $S_{B a}\left(t_{B a}\right)$. Then, the remain correction is done in hardware. The required signal for $S_{B a}$ is obtained by ANDing the output of the first counter with the inverted output of the second counter. This signal is NORed with the inverted output of the first counter to generate the signal for $S_{C a}$ shown in Figure 5.7. This logic gate arrangement also ensures that two or more switching devices in one output phase never conduct at the same time. The timing diagram for output phase, $a$ is given in Figure 5.7.

The operation of this circuit has proved very effective down to $500 \mu \mathrm{~S}$ sampling time and it is mainly restricted by the load time of the counters, which was $100 \mu \mathrm{~S}$.


Figure 5.7 The Timing Diagram


### 5.5 Dead-Lock Protection Circuitry

Loss of synchronisation occurs when one transputer waits for communication which never comes. This phenomenon is called as dead-lock and usually occurs because of noise pick up on the serial cables. For instance, assume that there is a communication problem between the overseer ( $\mathrm{T}_{1}$ ) and the speed input board because of the noise interference on the serial links. In this case, $T_{1}$ locks up and consequently, $\mathrm{T}_{2}$ locks up since it waits for communication to $\mathrm{T}_{1}$. If this happens the timing circuitry losses the count information resulting in a wrong fire sequence of the power switches. The circuit shown in Figure 5.9 provides an effective protection against the dead-lock of the transputer board. This circuit cooperates with the overcurrent protection circuit discussed in Section 4.4.2.


Figure 5.9 Dead-Lock Protection Circuit

Under normal operation, the circuit receives a trigger signal from the transputer board every sampling time, $500 \mu \mathrm{~S}$. This signal is an input to the clear pin of the counter, 74590 . The counter counts up using a $2 \mu \mathrm{~S}$ external clock circuit. If there is no fault condition (dead-lock) in transputer board the counter will be reset
every $500 \mu \mathrm{~S}$ providing the normal operation of the matrix converter. If the trigger signal is not received from the transputer board because of dead-lock the flip-flop (4027) will provide a latched trip signal (after $512 \mu \mathrm{~S}$ ) disabling all of the gate signals by means of the disable circuit discussed in the next section. The circuit is reset by using the reset button on the over-current protection board.

### 5.6 Delay and Disable Circuitry



Figure 5.10 Delay and Disable Circuit

In the prototype converter it is necessary to introduce a delay between drive signals to avoid a short circuit of the input lines. The circuit shown in Figure 5.10 performs this task and also disables the drive signals in case of a fault condition. The input to the delay circuit is from the timing circuitry and the output is connected to the disable circuit. The delay time can be varied between 0 and $1.5 \mu \mathrm{~S}$ by setting the variable resistor on the circuit board. The circuit also shifts the voltage level from +15 V to +5 V .

The disable circuit ensures that if there is a fault signal from the over-current
protection circuit it disables all the gate drive signals of the power switches. The signals from the delay circuit are ANDed with the fault signal which is high at normal operation. If there is a fault condition which might be a result of over-current or dead-lock, the fault signal will go down to zero. This will result in turning all of the gate drive signals off.

The opto-isolation circuit provides the ground isolation between the power supplies of the gate drive circuit and the control circuitry to avoid large earth loops. This circuit also shifts the level of the control signals from $0 / 5 \mathrm{~V}$ to $+/-15 \mathrm{~V}$ to meet the input requirement of the gate drive circuit.

### 5.7 Conclusions

The transputer parallel processor was chosen to implement the matrix converter control due to the availability of the processor and peripherals, ease of implementation and the expertise within the department at using transputers.

An interface board for the measurement of the instantaneous input voltages and output currents has been described. A timing circuit using programmable interval timers has been designed to generate the switching patterns. This board reduces the calculation time by generating the third drive signal of each output phase in hardware. It also ensures that two or more switches sharing the same output phase cannot conduct simultaneously. An effective protection circuit has been developed to protect the prototype converter in the case of transputer dead-lock. A delay circuit has been designed to introduce a controllable delay between the gate drive signals to avoid a short circuit of the input lines.

## CHAPTER 6

## CONSTANT V/F AND SLIP CONTROL OF MATRIX

## CONVERTER INDUCTION MOTOR DRIVES

### 6.1 Introduction

This chapter presents the real-time implementation of open-loop $V / F$ and closed-loop slip control of the matrix converter induction motor drive on a transputer parallel processing network. The occam implementation of the Venturini and scalar algorithms for open-loop control are described and experimental results are given to verify the correct operation of the control algorithms. Secondly, the speed control of the induction motor using constant Volt/Hertz control strategy in open-loop is given with its occam implementation. Test results are presented at the end of the section.

The final section discusses a closed-loop control strategy using the slip regulation technique. The drive system structure and the design of the speed controller are described. The user interface with the supervising transputer and their routines are given as they are common to the vector control algorithm discussed in the next chapter. The occam implementation of the control strategy is presented and experimental results are given which show the transient and steady-state operation of the control strategy.

### 6.2 Real-Time Implementation of Control Algorithms

Many of the published papers on the implementation of modulation algorithms for the matrix converter have employed fixed switching patterns. In this case, for certain output conditions (amplitude, frequency etc.) duty cycles for the switching patterns are pre-calculated and placed into the memory. The fixed switching patterns using the Venturini algorithm can be only created for certain output frequencies where input and output frequencies are synchronised such as; $25 \mathrm{~Hz}, 50, \mathrm{~Hz}, 100 \mathrm{~Hz}$ etc. However, in general the input and output frequencies will be asynchronous, consequently the switching patterns may never repeat and cannot therefore be precalculated. Therefore, it is necessary to calculate the duty cycles every sampling time in order to achieve voltage control in which the output frequency is continuously variable.

In this project, the duty cycles for the switches are updated every sampling time, $500 \mu \mathrm{~S}$, enabling closed-loop control of the induction motor drive. The method for the duty cycle calculations is explained in the following section.

### 6.2.1 Real-Time Implementation of the Venturini Algorithm

The scalar form of the Venturini algorithm for unity input displacement factor given in Equation 6.2 and 6.3 is used. The algorithm requires the position of the input vectors, instantaneous input voltages and desired output voltage. The input position can be obtained using a zero-crossing detector. However, the noise on the input voltage and timing error (since it is read once in one input period) will affect the modulation algorithm. In addition, transputers do not have direct interrupt facilities unlike conventional sequential processors. They require additional hardware and software to handle the interrupt request, which increases the system complexity. For these reasons, the instantaneous input voltages which are also needed for the modulation algorithm are measured and the input angle is then calculated using the equations given below;

$$
\begin{align*}
& V_{i m}=\frac{\sqrt{V_{A}^{2}+V_{B}^{2}+V_{C}^{2}}}{1.5}  \tag{6.1}\\
& \omega_{i} t=\arccos \frac{V_{A}}{V_{i m}}
\end{align*}
$$

Where; $\mathrm{V}_{\mathrm{A}}, \mathrm{V}_{\mathrm{B}}$ and $\mathrm{V}_{\mathrm{C}}$ are the instantaneous input voltages
$\mathrm{V}_{\mathrm{im}}$ is the maximum input voltage
$\omega_{\mathrm{i}} \mathrm{t}$ is the input angle
Since the input voltages are measured every sampling time, $\mathrm{T}_{\mathrm{s}}$ the input angle is updated avoiding phasing errors. The output angle is calculated every sampling time regarding the desired output frequency and the sampling time, $\mathrm{T}_{\mathrm{s}}$ as;

$$
\left(\omega_{0} t\right)_{k}=\left(\omega_{o} t\right)_{k-1}+2 \pi T_{s} f_{0}
$$

where $\left(\omega_{0} t\right)_{k-1}$ is the previous value of $\omega_{0} t$
The switching time for each switch is calculated using;

$$
\begin{equation*}
T_{\beta \gamma}=\left[\frac{1}{3}+\frac{2 V_{\partial \gamma} V_{i \beta}}{V_{i m}^{2}}+\frac{2 q}{9 q_{m}} \sin \left(\omega_{t} t+\Psi_{\beta}\right) \sin \left(3 \omega_{i} t\right)\right] \tag{6.2}
\end{equation*}
$$

Where ; $\boldsymbol{\gamma}$ denotes output
$\beta$ denotes input
$\Psi$ is the phase shift
q is the desired voltage ratio
$\mathrm{q}_{\mathrm{m}}$ is the maximum voltage ratio ( 0.866 )
$\mathrm{V}_{\mathrm{oy}}$ is the desired output voltage given by;

$$
\begin{equation*}
V_{o \gamma}=\left[q V_{i m} \cos \left(\omega_{o} t+\Psi_{\gamma}\right)\right]-\left[\frac{q}{6} V_{i m} \cos \left(3 \omega_{o} t\right)\right]+\left[\frac{q}{4 q_{m}} V_{i m} \cos \left(3 \omega_{i} t\right)\right] \tag{6.3}
\end{equation*}
$$

and voltage ratio are input from the keyboard for testing and another where they are supplied as outputs from a control loop. The input displacement factor is set to 1 which is desired for most applications although the converter can work at different displacement factors (leading or lagging). There are two look-up tables, one for cosines and one for arccosine. This pre-scaling takes up memory, but allows faster calculation of the control functions.

The transputer network illustrated earlier in Figure 5.3 has been used to implement of the Venturini algorithm for testing purposes. The supervisor process receives the desired output frequency and amplitude from the keyboard and ramps the output from the present values to the new demand values. These are input to the second transputer every $500 \mu \mathrm{~S}$.

## Occam Implementation:

The occam implementation of the Venturini algorithm is shown by the pseudo-code given below. Since the control algorithm is implemented on two transputers the occam implementations for both transputers will be given separately. The occam implementation on the supervising transputer is;

PROC soft running
... Declarations -- Declare variables plus libraries SEQ

Initiate values

## WHILE TRUE

SEQ
... Communicate with user -- Get output frequency and amplitude
... Ramping
... Transfer variables -- Send output frequency and amplitude to Transputer 2

The main routine is governed by the WHILE TRUE construct which means that the process will be repeated infinitely. The main fold, "Ramping" is given in detail by the pseudo-code as follows:

IF
demand $=\mathbf{\prime} \mathbf{f} \quad--$ demand on output frequency
... Initialize the timer
... Increase or decrease frequency
demand $=$ ' $q$ ' $\quad-$ demand on amplitude
... Initialize the timer
... Increase or decrease amplitude

## TRUE

... Do nothing
The occam implementation part of the control algorithm on the second transputer is given here;

PROC Venturini
... Declarations -- Declare variables plus libraries SEQ
... Startup
... Set transputer clock -- See text
PRI PAR
WHILE TRUE SEQ

PRI ALT
... Communicate with supervising transputer TRUE\&SKIP

SKIP
... Measure input voltages
... Calculate input angle -- Using Equation 6.1
... Calculate duty cycles for switches -- Using
... Pulse dropping --Ignore pulses less than $3 \mu S$
... Load counters -- See Section 5.3.4
... Wait for clock -- See text
... Enable counters
... Set transputer clock -- See text
SEQ - Skip
... Do nothing
The declaration procedure in this program defines the variables, constants and initial values. The startup procedure loads the cosine and arccosine look-up tables and programs the pulse generation board. The calculation strategy is implemented as a high priority parallel process in order to access the high priority timer and is executed in an infinite loop. The low priority process "skip" does nothing.

The current value of the transputer clock is initialized to the variable "now" and immediately, the demand output frequency and amplitude are received from the supervising transputer. Here, asynchronous communication (using the occam PRI ALT construction) is provided with the supervising transputer. This construction ensures that a new frequency and voltage demand can be input at any time from the keyboard but it will be ignored by the high priority process until the start of the next sample period. This is followed by two instantaneous phase voltage measurements through the A/D board and the input angle is calculated using the procedure given in Section 6.2.1. Subsequently the switch duty cycles for each output phase are calculated using Equations 6.2-6.3. The pulse dropping procedure ensures that narrow pulses ( $<3 \mu \mathrm{~S}$ ) are ignored. The interface board counters are then loaded as described in Section 5.4. The transputer waits until the clock value has reached (now+500). This is achieved by using a "TIME ? AFTER (now + 500)" wait statement which ensures that the pulse initiation is synchronised to the same point in every sampling time. At this point the counters are enabled by outputting the correct control byte to the interface board. The transputer clock is again initialized to the variable "now" and the $500 \mu \mathrm{~S}$ sample period is completed. The total calculation time to execute this high priority process was $265 \mu \mathrm{~S}$ which includes 100 $\mu S$ for loading the counters.

### 6.2.2 Real-Time Implementation of the Scalar Algorithm

The scalar control algorithm for the matrix converter is based on the knowledge of the instantaneous input voltages. Although the control algorithm is easy to implement in real time it requires the instantaneous input voltages to be measured very accurately. As discussed in Chapter 2, there are two rules to determine the duty cycles for the switches:

Rule 1: M is assigned to the input voltage which has a different polarity from the other two voltages.

Rule 2: K and L are assigned to the two input phase voltages which share the same polarity, the smallest one of the two (in absolute value), being K.

Then, the duty cycles for the switches are given as;

$$
\begin{align*}
& T_{L}=T_{s} \frac{\left(V_{0}-V_{M}\right)}{1.5 V_{i m}^{2}} V_{L} \\
& T_{K}=T_{s} \frac{\left(V_{0}-V_{M}\right)}{1.5 V_{i m}^{2}} V_{K}  \tag{6.4}\\
& T_{M}=T_{s}-\left(T_{L}+T_{K}\right)
\end{align*}
$$

Where; $\mathrm{T}_{5}$ : The switching period
$\mathrm{V}_{0}$ : The desired output voltage
$\mathrm{V}_{\mathrm{im}}$ : The maximum input voltage
$\mathrm{V}_{\mathrm{L}}, \mathrm{V}_{\mathrm{K}}, \mathrm{V}_{\mathrm{M}}$ : The instantaneous input voltages
The transputer network used in the implementation of the Venturini algorithm is also used to implement the scalar algorithm. The occam implementation of the scalar algorithm on the second transputer is shown by the pseudo-code given below. The occam implementation of the algorithm on the supervising transputer is the same as for the Venturini algorithm and not repeated here.

PROC Scalar<br>... Declarations -- Declare variables plus libraries SEQ<br>... Startup<br>... Set transputer clock<br>PRI PAR<br>\section*{WHILE TRUE}<br>SEQ<br>PRI ALT<br>... Communicate with supervising transputer TRUE\&SKIP<br>SKIP

... Communicate with supervising transputer
... Measure input voltages
... Assign K,L,M -- See text
... Calculate duty cycles for switches .- Using
Equation 6.4
... Pulse dropping
... Load counters -- See Section 5.3.4
... Wait for clock
... Enable counters
... Set transputer clock
SEQ -- Skip
... Do nothing
The software structure for the implementation of the scalar algorithm is almost same as that of the Venturini algorithm. Here, the only difference is that the " Calculate input angle " fold is replaced by the " Assign K,L,M " fold in which the input voltages are assigned to the variables $\mathrm{K}, \mathrm{L}$ and M according to the rules given for the scalar algorithm. In the following fold the duty cycles are calculated using Equation 6.4. The resultant execution time for the scalar algorithm was $276 \mu \mathrm{~S}$
including time for loading the counters.

### 6.2.3 Experimental Results

Experimental results for both the Venturini and the scalar algorithm have been taken with the converter feeding a passive R-L load ( $0.6 \Omega$ and 70 mH ). Figures 6.1(a) and 6.1(b) show the output currents for both algorithms. In this case, the output frequency is ramped from 10 Hz to 60 Hz . The rms input line voltage was set to 250 V with voltage ratio, $\mathrm{q}=0.3$. The output currents shown in Figures 6.2(a) and 6.2(b) were obtained by ramping the voltage ratio, $q$ from 0.3 to 0.82 at an rms input line voltage of 250 V and a fixed output frequency of 30 Hz .

### 6.3 Open-Loop V/F Induction Motor Control

Open-loop speed control of an induction motor with an adjustable-frequency supply provides a satisfactory adjustable-speed drive when the transient performance characteristics are undemanding and when the motor operates at steady speeds for long periods. The speed of the induction motor can be controlled by varying stator frequency $f_{s}$, which controls the synchronous speed and hence the motor speed if the slip is kept small.

The torque developed by an induction motor is given by Equation 6.5;

$$
\begin{equation*}
T_{m}=K \Phi_{a g}^{2} \frac{\omega_{s l}}{R_{2}} \tag{6.5}
\end{equation*}
$$

where K is a constant and depends on the motor design
$\phi_{\mathrm{ag}}$ is the airgap flux
As can be seen, if the airgap flux is maintained constant under all operating conditions, the induction motor torque is uniquely determined by the slip frequency and is independent of supply frequency. In open-loop control, airgap flux can be maintained constant by keeping the ratio of the airgap voltage to frequency constant.

(a)


Figure 6.1 The Output Currents for ramped frequency from 10 Hz to 60 Hz with a Passive R-L Load
(a) The Venturini Algorithm, (b) Scalar Algorithm


Figure 6.2 The Output Currents for Ramped Amplitude from $q=0.3$ to $q=0.84$ with a Passive R-L Load (a) The Venturini Algorithm, (b) Scalar Algorithm

This is done by keeping the terminal voltage to frequency ratio constant except at low frequencies where it is necessary to boost the voltage to overcome the drop across the stator resistance. This method is commonly referred to a terminal Volt/Hertz (V/F) control and is widely used in simple open-loop systems.

Constant V/F operation cannot be achieved at above synchronous speed since it is impossible to increase the motor terminal voltage more than its rated value. This results in weakening of airgap flux and reduction of maximum torque. In this case, the motor operates in constant power region where maximum torque changes inversely with square of the stator frequency.

### 6.3.1 Occam Implementation of the Control Algorithm

The Venturini algorithm is used in the implementation of the constant $\mathrm{V} / \mathrm{F}$ control. The occam implementation of the control strategy is almost the same as for the Venturini algorithm described in Section 6.2.1. Here, the only difference is the process on the supervising transputer. Therefore the occam implementation part of the control algorithm on the second transputer is not repeated. The occam implementation on the supervising transputer is given by pseudo-code below;

> PROC V/F control
... Declarations -- Declare variables plus libraries SEQ
.. Initiate values
PRI PAR
WHILE TRUE
SEQ
... Communicate with user -- Get output
frequency
... Constant V/F and ramping -- See below
SEQ
... Do nothing

The main fold, "Constant V/F and ramping" is given in detail by the pseudo-code as follows:

```
WHILE (f.demand > f.present)
    SEQ
    clock ? now -- initialize the timer
    f.present := f.present +0.1 -- increase output frequency
    ... Perform constant V/F control
    clock ? AFTER now PLUS (delay) -- wait for delay
    ... Transfer variables -- send frequency \& amplitude to second transputer
```

WHILE f.demand < f.present
SEQ
clock ? now -- initialize the timer
f.present := f.present - 0.1 -- decrease output frequency
... perform constant V/F control
clock ? AFTER now PLUS (delay) -- wait for delay
... Transfer variables -- send frequency \& amplitude to second
transputer

This fold provides constant V/F control and ramping. If there is an output frequency demand from the user, it is compared with the present value of the output frequency. Then, using the occam WHILE construction, the output frequency is increased or decreased until it reaches the demand value. A timing process (which provides a wait until the transputer clock value "delay" is reached) is used to introduce a delay at each step of the frequency change in order to provide a slow increase or decrease. After that the amplitude and frequency are sent to the second transputer which executes the Venturini algorithm and calculates the pulse widths. The communication between the supervising transputer and the second transputer is asynchronised using the occam PRI ALT construction as explained in Section 6.2.1.

### 6.3.2 Experimental Results

2.2 kW induction motor has been used as a load to demonstrate the operation of open-loop V/F control strategy. The specifications of the motor are given in Appendix C. Results have been taken for below rated, rated and above rated speed of the induction motor. Figures 6.3 and 6.4 show the motor line currents for constant V/F operation at $600 \mathrm{rpm}(20 \mathrm{~Hz})$ and $1500 \mathrm{rpm}(50 \mathrm{~Hz})$, respectively. Figure 6.5 shows the motor current at 80 Hz output frequency running with 2400 rpm . In this case the motor operates in the field weakening region. All these results have been taken on no-load.


Figure 6.3 The Motor Line Current Operating at 20 Hz with Open-Loop Constant V/F Control


Figure 6.4 The Motor Line Current Operating at 50 Hz with Open-Loop Constant V/F Control


Figure 6.5 The Motor Line Current Operating at 80 Hz in Field Weakening Region

### 6.4 Closed-Loop Control Using the Slip Regulation Technique

Open-loop speed control has the disadvantage that the induction motor speed slows down slightly when load torque is applied. Moreover, this control technique is not satisfactory where the dynamics of speed control need to be very fast and precise. Therefore, closed-loop control is necessary for precise steady-state operation in the presence of supply voltage fluctuations and load disturbances and also when fast dynamic response is required. A wide variety of closed-loop control techniques are used to meet different applications and performance requirements. An effective torque control loop for a high-performance induction motor drive may include control loops for airgap flux, slip frequency, or stator current (in terms of amplitude and phase). These inner loops require additional sensing or estimating of motor quantities, but result in high-quality drive performance. However, the control structure of the induction motor drive can be simplified when fast response is not a priority. In this case, the inner torque loop or stator current loop can be omitted. These simplified control structures allow a significant reduction in drive cost and are satisfactory for many industrial applications such as; speed control of fans, pumps, compressors and the like.

The control scheme shown in Figure 6.6 has been implemented in the matrix converter drive. This control technique provides constant V/F control using slip regulation. In this method, the motor shaft position is read using an encoder and the speed, n is then calculated as described in Appendix C. The demand speed, $\mathrm{n}^{*}$ is compared with the actual shaft speed, $n$. The resulting speed error, $n^{*}-n$ is passed thorough the speed controller which defines the converter frequency and voltage. A proportional-Integral (PI) controller is used to perform the speed controller. A slip limit is introduced in the control system so that the demanded slip frequency can never exceed the breakdown value in the motoring or generating regions. Thus, stable operation is possible close to the breakdown point, giving a high torque per ampere and good dynamic performance for sudden changes in demanded speed. The compensated speed error is used to generate the slip frequency command, $\omega_{s 1}^{*}$. This
signal is added to the actual motor speed signal, $\omega_{\mathrm{r}}$ to determine the converter frequency command $\omega^{*}$. Another signal is also supplied to a function generator that produces the voltage command, $\mathrm{V}_{\mathbf{8}}^{*}$. The function generator implements a voltage boost at low frequencies in order to keep the airgap flux constant. The induction motor torque is therefore proportional to the slip frequency, as shown by Equation 6.5 and the slip control loop acts as a inner torque loop.


Figure 6.6 Closed-Loop Adjustable-Speed Induction Motor Drive Using Slip Regulation

The direction of motor rotation is determined by the phase sequence of the stator frequency. The modulation algorithm automatically reverses the phase sequence when the demanded frequency is negative as explained in Section 2.2.1. Independent control of the direction and the slip polarity means that four-quadrant operation is possible, giving motor or generator operation for either direction of rotation. A rapid reduction or reversal in demanded speed results in the generation of a negative slip command, causing the machine to operate as an induction generator. As a result of bidirectional operation of the matrix converter, this regenerated energy is easily returned to the AC utility network. This is one of the advantages of the matrix converter over the voltage-source inverter.

### 6.4.1 System Layout

Figure 6.7 shows the whole block diagram for closed-loop control of the matrix converter induction motor drive. Two transputers running in parallel are used to implement the slip regulation control technique. One of the transputers, 'supervisor' provides on-line communication between the user and the control transputer, $\mathrm{T}_{2}$ and executes the speed measurement and speed control. The process on the second transputer, $\mathrm{T}_{2}$ is inherently sequential and it implements the input voltage and output current measurements, calculations for the Venturini algorithm and actuation of the timing board.

### 6.4.2 Speed Controller Design

For good transient and steady-state performance, the speed controller must be properly designed so that the closed-loop transfer function of the drive system has the desired structure. A PI speed controller has been employed for the system to provide a speed control system with no steady-state error and minimal overshoot during transients. Figure 6.8 shows the Laplace block diagram of the controller. The CODAS software package program [61] was used for the design of the controller. The block diagram in Figure 6.8 consists of the PI controller characterised by $\mathrm{K}_{\mathrm{c}}$ and a, a limiter for the slip frequency and the mechanical characteristic of the machine with the torque constant $\mathrm{C}(0.61)$ and the inertia, $\mathrm{J}\left(0.0115 \mathrm{kgm}^{2}\right)$. The resultant PI controller has $K_{c}=0.3$ and $a=50$ giving a natural frequency of 12 Hz and $a$ damping factor of 0.707 with the machine unloaded.



Figure 6.8 Laplace Block Diagram for the Design of the Speed Controller

### 6.4.3 Occam Implementation of the Control Algorithm

The user interface to the slip control algorithm is provided by supervisory routines running on the B004 motherboard and the IBM PC itself. The user routine on the IBM PC is written in Turbo Pascal [62] according to the PC input/output configuration. The reason for using Turbo Pascal instead of occam is that it provides simplicity for the monitoring utility. This software includes commands for resetting the B004, loading code from the PC and bidirectional data transfer. The routine provides:

1) Keyboard and screen drivers for direct motor speed control
2) An ability to capture data over a prescribed period and transfer this data to a disk file.
3) Access to graphics and plot routines to allow visual data analysis whilst the motor is running.

The user routine written in Turbo Pascal allows access to graphics and plot routines without disturbing the operation of the transputer network. When the user program
is terminated the transputer network continues to run but with no user interface. The plotting and graphics routines can then be called up for visual analysis of the transient and steady-state data. The user routine written in Turbo Pascal will not be given in detail here.

The control algorithm on the supervising transputer $\left(\mathrm{T}_{1}\right)$ provides two parallel processes on a single transputer. Two procedures are defined, one high and one low priority process. The high priority process (overseer) provides the speed measurement and speed control and synchronised communication with the second transputer, $\mathrm{T}_{2}$ whereas the low priority process, 'userio' interfaces between the overseer and the user, preventing the long interface and calculation processes from extending the sample time of the control system as described in detail in Section 5.2.2. The occam implementation for this program with pseudo-code is shown in Figure 6.9. The six procedures used are "n.in" and "n.out", which provide 16 bit integer communication between the user (Pascal routine) and the B004 motherboard via the IBM PC input/output port-transputer serial link, "userio.to.overseer" and "overseer.to.userio", which provide 32 bit serial link interface between the two transputers, "speed.in" and "read.speed", which are used to read the 12 bit shaft position through the A/D. The initiate routine is used to set up the initial values for the variables used.

The PRI PAR statement is used to execute the two processes, 'overseer' and 'userio' in parallel. The process 'overseer' is governed by a WHILE TRUE statement which means that the process will be repeated infinitely. The routine starts by assigning the current value of the transputer timer to the variable "now"and communicates with the second transputer, $\mathrm{T}_{2}$ for synchronisation. The process then reads the shaft position through the A/D. In the following step of the process, a counter is used to set the position sample time of 5 mS , providing a speed resolution of 1.2 rpm . If the counter reaches 10 , the speed is calculated, filtered and the PI speed controller is executed. The digital implementation of this controller is given in Appendix F. The output of the speed controller sets the frequency for the constant V/F control with voltage boost below 20 Hz . After that, the counter is set to 1 , enabling another 5 mS sample time. Every $500 \mu \mathrm{~S}$ the frequency and voltage demand
is passed from $T_{1}$ to $T_{2}$ and immediately afterwards the voltages, currents and control variables are sent from $T_{2}$ to $T_{1}$ for monitoring purposes. The interface between the user and the control network is created by the ALT construct which uses the input from the internal channel "userio.to.overseer" and the transputer clock as its operands. If the 'userio' routine is ready to communicate with the network it will output the speed demand or data capture to the 'overseer' on channel "userio.to.overseer". The overseer will either read the demanded speed or send data to the user using channel "overseer.to.userio". The userio has a period of $450 \mu \mathrm{~S}$ in which to initiate this communication from the time that the transputer clock is read. If this communication does not occur the TIME ? AFTER(now+450) input to the ALT construct dictates that this communication is ignored for this cycle and the overseer procedure returns to its initial mode for synchronisation with $\mathrm{T}_{2}$. The principle behind the time-slicing technique employed by the transputer ensures that the userio process will always be executed on demand.

The userio routine acts as a software buffer between the user and the control transputer. The user demand can be on speed or on-line data capture for monitoring purposes. The routine has its own local variables defined within the process and is executed in an infinite loop. The 'userio' process starts by reading the command value "choice" from the user and selects a process depending on the value of this parameter. These values are:
's' the new speed demand is read from the user. This is then passed to the overseer, and the previous set of sampled data are read into this process from 'overseer' and put into a two dimensional array. The array pointer is incremented and this process repeated 1500 times to capture data over the speed transient period. Then, this data array is sent to the user for monitoring utility.
' $r$ ' only a single sample set is captured and this is passed to the user for screen display.
'd' this command provides a capture of data over 1500 consecutive samples from the overseer and then these are passed to the user for steady-state observation on the screen display.

Figure 6.9 Occam Pseudo-Code for the Slip Controlled Drive

On completion of any of these processes the routine returns to the start to wait for the new command value from the user.

The occam implementation part of the control algorithm on the second transputer is given under the $\mathrm{T}_{2}$ label in Figure 6.9. This software basically performs pulse width calculations using the Venturini algorithm. The software structure is almost the same as that described in Section 6.2.1 but here additionally, the output currents and input voltages are sent to the supervising transputer. The rest of the program is the same and is not described again.

### 6.4.4 Experimental Results

Experimental results have been taken for transient operation of the induction motor in closed-loop control using the slip regulation technique. Figure 6.10 shows the transient motor current and speed waveforms for speed reversal in which the motor speed was changed from 1500 rpm to -1500 rpm . The results shown in Figure 6.11 have been taken to demonstrate the regenerative operation of the matrix converter. In this case, the motor speed was reversed from 2400 rpm to -2400 rpm in order to get more regenerative energy (note that the rated motor speed is 1500 $\mathrm{rpm})$. The regeneration starts at 40 mS where the speed is reduced and the input current changes its phase as shown in Figure 6.11. Note that in this figure the input current has been filtered. Figure 6.12 shows the motor current and speed waveforms whilst the motor is accelerating from 200 rpm to 1500 rpm .


Figure 6.10 The Transient Motor Current and Speed Waveforms for Speed Reversal from 1500 rpm to -1500 rpm


Figure 6.11 The Input Phase Voltage and Current Waveforms of the Matrix Converter in Regenerative Mode


Figure 6.12 The Transient Motor Current and Speed Waveforms in Acceleration from 200 rpm to 1500 rpm

### 6.5 Conclusions

The real-time implementation of open-loop and closed-loop control of the matrix converter induction motor drive on a transputer parallel processing network has been described. Both the Venturini and the scalar algorithm have been implemented. Both algorithms show similar results with a passive R-L load. It has been found that the scalar algorithm needs very accurate input voltage measurement since the duty cycles for the scalar algorithm are mainly determined by the instantaneous input voltages. Any noise on the input voltages will result in the distortion of the output currents. In addition, the occam implementation time for the scalar algorithm was found to be slightly longer than that for the Venturini algorithm. For these reasons, the Venturini algorithm has been used to implement closed-loop of the matrix converter.

Open-loop constant V/F control of the matrix converter induction motor drive has been explained and demonstrated. The experimental results given under various
operating conditions have verified the correct operation of the control system. Finally, closed-loop control of the drive using the slip regulation technique has been achieved. The occam implementation of the control strategy and the user interface routines has been given. The operation of the control system under steady-state and transient conditions has been examined and the results presented. The matrix converter has been shown to be capable of operation as a four quadrant drive, with natural regeneration.

## CHAPTER 7

## VECTOR CONTROL OF MATRIX

## CONVERTER INDUCTION MOTOR

## DRIVES

### 7.1 Introduction

This chapter investigates the application of the vector control (field oriented) technique to matrix converter induction motor drives. The first section describes the principle of vector control with its mathematical structure. Section two outlines the implementation of the vector control technique used in the matrix converter drive. The problems associated with the implementation of this technique for a high performance matrix converter induction motor drive are discussed. The next section deals with the design of the speed and current controllers. The implementation of the vector control technique on the transputer network is given with its occam structure.

Finally, in the last section experimental results are given which show the transient and steady-state operation of the drive. It is demonstrated that high performance operation with full four-quadrant capability can be achieved with this type of drive.

### 7.2 Vector Control

Vector control is a technique which allows the induction motor to act like a separately excited DC machine with decoupled control of torque and flux, making it possible to operate the induction motor as a high-performance four-quadrant servo
drive. The principle of vector control was devised by Hasse and Blaschke [63] and was developed by Leonard [64-66].

In separately excited DC machine with a constant field excitation, torque is directly proportional to armature current. The orthogonal relationship between air gap flux and torque is independent of the speed of rotation so that the torque of the DC machine is proportional to the product of the flux and armature current. If the magnetic saturation is ignored, field flux is proportional to field current and is unaffected by armature current because of the orthogonal orientation of the stator and rotor fields. Therefore, direct control of armature current gives direct control of motor torque and fast response, because motor torque can be altered as rapidly as armature current can be altered.


Figure 7.1 Vector Diagram for Induction Motor Currents

The vector control technique provides a similar control strategy for the induction motor. The idea behind vector control is that the stator current of the induction motor is decomposed into orthogonal components as a magnetization component (flux producing) and a torque component. These components are controlled individually. In order to obtain high dynamic performance of the induction motor, the magnetizing current component is maintained at its rated level while the torque should be controlled through the torque component of the stator current.

A generalized d-q axis dynamic model of the induction motor in a rotating frame of reference is used to derive the vector control algorithm. The equations defining the stator and rotor dynamics in a synchronously rotating frame of reference ( rotating at $\omega_{e}$ ) shown in Figure 7.1 are given in the matrix form below [64];

$$
\left[\begin{array}{c}
V_{s d}  \tag{7.1}\\
V_{s q} \\
0 \\
0
\end{array}\right]=\left[\begin{array}{cccc}
R_{s}+\sigma L_{s} S & -\omega_{e} \sigma L_{s} & \frac{M_{2}}{L_{r}} & -\omega_{e} \frac{M}{L_{r}} \\
\omega_{e} \sigma L_{s} & R_{s}+\sigma L_{s} S & \frac{\omega_{e} M}{L_{r}} & \frac{M_{S}}{L_{r}} \\
-M \frac{R_{r}}{L_{r}} & 0 & \frac{R_{r}}{L_{r}}+ & -\omega_{s l} \\
0 & -M \frac{R_{r}}{L_{r}} & \omega_{s l} & \frac{R_{r}}{L_{r}}+S
\end{array}\right]\left[\begin{array}{c}
I_{s d} \\
I_{s q} \\
\Phi_{r d} \\
\Phi_{r q}
\end{array}\right]
$$

where: M is the mutual inductance between the stator and rotor
$\sigma$ is the leakage coefficient
$\omega_{\mathrm{si}}$ is the slip frequency
$S$ denotes $\mathrm{d} / \mathrm{dt}$
$\mathrm{L}_{3}$ is the stator self inductance
$\mathrm{L}_{\tau}$ is the rotor self inductance
$\phi_{\mathrm{rd}}, \phi_{\mathrm{rq}}$ are d-q axis rotor fluxes
The d axis flux linking the rotor windings is;

$$
\begin{equation*}
\Phi_{r d}=M i_{s d}+L i_{r d} \tag{7.2}
\end{equation*}
$$

The $q$ axis flux linking the rotor windings is;

$$
\begin{equation*}
\Phi_{r q}=M i_{s q}+L_{r} i_{r q} \tag{7.3}
\end{equation*}
$$

The torque expression for this system is;
$T_{e}=\frac{2}{3}\left(\frac{p}{2}\right) \frac{M}{L_{r}}\left(i_{s q} \Phi_{r d}-i_{s d} \Phi_{r q}\right)$
where $p$ is the number of pole pairs.

If the $d$ axis (real axis) of the rotating frame of reference is aligned to the rotor flux axis, then the d - q model simplifies significantly. Therefore;

$$
\begin{align*}
& \Phi_{r q}=0  \tag{7.5}\\
& \left|\Phi_{r}\right|=\Phi_{r d}
\end{align*}
$$

Substituting Equation 7.5 into Equation 7.1;

$$
\left[\begin{array}{c}
V_{s d}  \tag{7.6}\\
V_{s q} \\
0 \\
0
\end{array}\right]=\left[\begin{array}{ccc}
R_{s}+\sigma L_{s} S & -\omega_{s} \sigma L_{s} & \frac{M}{L_{r}} S \\
\omega_{s} \sigma L_{s} & R_{s}+\sigma L_{s} S & \frac{\omega_{s} M}{L_{r}} \\
-M \frac{R_{r}}{L_{r}} & 0 & \frac{R_{r}}{L_{r}}+S \\
0 & -M \frac{R_{r}}{L_{r}} & \omega_{s l}
\end{array}\right]\left[\begin{array}{l}
I_{s d} \\
I_{s q} \\
\Phi_{r d}
\end{array}\right]
$$

The torque equation becomes;
$T_{e}=\frac{2}{3}\left(\frac{p}{2}\right) \frac{M}{L_{r}} i_{s q} \Phi_{r d}$
$T_{e}=k i_{s q} \Phi_{r d}$
where $k=\frac{2}{3}\left(\frac{p}{2}\right) \frac{M}{L_{r}}$
In Equation 7.7 it should be noted that the rotor flux, $\Phi_{\mathrm{rd}}$ differs from the air gap flux by the rotor leakage. The rotor flux is used instead of the true air gap flux in the torque expression since it simplifies the dynamic equations used later. The rotor flux is compensated for in the torque expression by the factor ( $\mathrm{M} / \mathrm{L}_{r}$ ) [67].

Rearranging rows 3 and 4 of Equation 7.6 ;
$M \frac{R_{r} i_{t_{d}}}{L_{r}}=\frac{R_{r}}{L_{r}} \Phi_{r d}+\frac{d \Phi_{r d}}{d t}$

$$
\begin{equation*}
\omega_{s l}=M\left(\frac{R_{r}}{L_{r}}\right)\left(\frac{i_{s q}}{\Phi_{r d}}\right) \tag{7.9}
\end{equation*}
$$

Introducing the defined relation $\Phi_{r d}=M . i_{\operatorname{mrd}}$ (where $i_{\operatorname{mrd}}$ is the magnetising current) and also the rotor time constant, $\tau_{\mathrm{r}}=\mathrm{L}_{\mathrm{r}} / \mathrm{R}_{\mathrm{r}}$ then Equations 7.8 and 7.9 become;

$$
\begin{align*}
& i_{s d}=\tau_{r} \frac{d i_{m r d}}{d t}+i_{m r d}  \tag{7.10}\\
& \omega_{s l}=\left(\frac{1}{\tau i_{m r d}}\right) i_{s q} \tag{7.11}
\end{align*}
$$

For an induction motor operating with a constant rotor flux;

$$
\begin{equation*}
\Phi_{r d}=M i_{m r d}=M i_{s d} \tag{7.12}
\end{equation*}
$$

and the torque equation becomes;

$$
\begin{equation*}
T_{e}=\frac{2}{3}\left(\frac{p}{2}\right) \frac{M^{2}}{L_{r}} i_{s d} i_{s q} \tag{7.13}
\end{equation*}
$$

Equations 7.10, 7.11 and 7.13 are the fundamental equations for vector control. Equation 7.10 is exactly the same as the dynamic equation for the field of a DC motor which is;

$$
\frac{V_{f}}{R_{f}}=i_{f}+\left(\frac{L_{f}}{R_{f}}\right) \frac{d i_{f}}{d t}
$$

Here, $i_{s d}$ corresponds to $V_{f} / R_{f}$ which is the steady-state field current. Since in steady-state $i_{s d}=i_{\text {madd }}, i_{z d}$ is directly proportional to the flux level in the induction motor. For this reason, $i_{s d}$ is called the "field component" of the stator current. Under constant torque operation of the induction motor, $i_{s d}=i_{\text {mrd }}$ is kept constant.

In Equation 7.11, $\mathrm{i}_{\mathrm{sq}}$ is analogous to the armature current in the DC machine. It is called the "torque current" which corresponds to the torque component of the
stator current. Here, if $i_{\text {mrd }}$ is kept constant then under vector conditions the slip frequency is directly proportional to the torque current. The torque equation of the induction motor (Equation 7.13) corresponds to the torque equation of a DC motor where $i_{s q}$ controls the induction motor torque.

### 7.3 Implementation of Vector Control

Vector control can be applied to all frequency controlled induction motor drives including matrix converter drives. The instantaneous position of the rotor flux vector, as expressed by the magnitude and angle of the rotor magnetizing current vector, $i_{m r}$ is required to implement vector control for induction motor drives. The technique for finding the rotor flux vector results in two vector control strategies; direct and indirect vector control.

In direct vector control, the flux density in the air gap of the machine is measured directly either by placing Hall-sensors in the air gap or search coils in the stator slots. Both techniques however require a specially modified induction motor, which is not generally practicable. The search coil signals are proportional to flux change which must be integrated to obtain the main flux. The drift of integration causes problem below 0.5 Hz . This limitation precludes the application of this method to drives requiring position control. The requirement of the specially modified induction motor for direct vector control can be avoided by measuring terminal voltages in which the stator windings are used as flux sensing coils. However, this technique requires accurate voltage compensation due to the resistive voltage drop, which dominates at low frequencies. The voltage compensation becomes difficult since the stator resistance changes with temperature, limiting the application of this technique below 3 Hz .

An alternative solution to this technique is the indirect vector control technique which eliminates measurement or computation of the rotor flux. There are two forms of the indirect control; flux angle observer and feedforward or slip-gain control. The flux angle observer technique uses a flux model to calculate the rotor
flux [63]. The feedforward technique aligns the d axis to the rotor flux vector by controlling the slip angular velocity according to Equation 7.11 using the controller reference values of $i_{s q}$ and $i_{\text {mrd }}$ rather than the actual machine value. It thus relies upon the precise control of the $d$ and $q$ axis currents using fast current controllers. For this technique, three input variables are required, the shaft speed and two of the three stator currents. The instantaneous position of the rotor flux is determined by summing the rotor position signal and the commanded slip position obtained by integrating Equation 7.11. In this project the feedforward indirect vector control technique has been used. This technique has the advantage that zero-speed operation is possible because the equations are valid when $\omega_{r}$ is zero and therefore, it is suitable for a servo drive.

All indirect methods are sensitive to variations in machine parameters. The calculation process requires the rotor time constant, $\tau_{\mathbf{r}}$ which involves the temperature-dependent rotor resistance, $\mathrm{R}_{\mathrm{T}}$ and saturation-dependent inductance, $\mathrm{L}_{\mathrm{r}}$. If the value of $\tau_{r}$ used in the calculation is not equal to the actual value, the desired decoupling of flux and torque is not achieved, resulting in the undesirable effects in both the steady-state and dynamic performance of the drive. Parameter adaptation can be used to overcome this problem. Sophisticated adaptive techniques have been developed where parameter changes are continuously sensed and appropriate corrections made online [67]. However, these techniques have not been implemented in this project due to the requirement for an additional transputer.

Figure 7.2 shows the block diagram for a vector-controlled matrix converter induction motor drive. The indirect vector control technique using impressed voltages and control of field and torque current components has been implemented in the matrix converter induction motor drive. The controller imposes a rotor flux vector angle $\theta_{e}$ which is aligned to the d axis. The motor speed, $\omega_{\mathrm{I}}$ is measured by determining the rate of change of the position encoder output and is compared to the demanded speed, $\omega_{\text {ref }}$ The resulting speed error is then processed by a proportionalintegral (PI) controller to produce an $i_{s q}^{*}$ demand, which in the constant torque region is proportional to the torque demand providing that the system is field orientated. The
torque demand current is limited to prevent motor drawing very high currents ( $\mathrm{i}_{\mathrm{sa}}, \mathrm{i}_{\mathrm{sb}}$, $i_{s c}$ ). The flux current demand is maintained constant at just under saturation level when machine runs below synchronous-speed. However, field weakening must be introduced above synchronous-speed operating conditions so that the flux current reference is reduced as the speed is increased above its synchronous base.

The transformation of the instantaneous stator currents into field oriented d and q axis components is carried out in two stages. First, the three instantaneous stator currents, $i_{20}(t), i_{s b}(t)$ and $i_{c c}(t)$ are transformed to the stationary two axis currents, $i_{s \alpha}(t)$ and $i_{s \beta}(t)$. These are then transformed into the rotating $d, q$ axis currents, $i_{s d}$ and $i_{s q}$. The equivalent complex operator $e^{-j \theta e}$ is used in this transformation. $\theta_{\mathrm{e}}$ denotes the instantaneous flux vector angle. The transformations are given in Appendix E. The inverse transformation of $d$ and $q$ axis values to the instantaneous stator reference frame is also given in Appendix E and is represented by the complex operator $\mathrm{e}^{\mathrm{j} \theta}$.

The voltage referenced scheme shown in Figure 7.2 is based on the stator dynamic equations derived from Equation 7.6. The two components of the current, one relating to the establishment of the flux and the other to the torque, are determined by reference to the motor parameters a control loop acting on the stator voltages draws these to their demanded values. The stator dynamic equations derived from Equation 7.6 are;

$$
\begin{align*}
& V_{s d}=R_{s} i_{s d}+\sigma \cdot L_{s} \frac{d i_{s d}}{d t}-\omega_{e} \cdot \sigma \cdot L_{s} i_{s q}+\frac{L_{o} d \Phi_{r d}}{L_{R} d t}  \tag{7.14}\\
& V_{s q}=R_{s} \cdot i_{s q}+\sigma \cdot L_{s} \frac{d i_{s q}}{d t}+\omega_{e} \cdot \sigma L_{s} i_{s d}+\omega_{e} \frac{L_{o}}{L_{R}} \Phi_{r d} \tag{7.15}
\end{align*}
$$

Figure 7.2 Block Diagram for a Vector-Controlled Matrix Converter Induction Motor Drive

The two current controllers which employ proportional integral (PI) control process the $i_{s d}$ and $i_{s q}$ errors to give $V_{s d}^{\prime}$ and $V_{s q}^{\prime}$. The relevant equations for controller design correspond to the first two terms of Equations 7.14 and 7.15.

$$
\begin{align*}
& V_{s d}=\left(R_{s}+s \sigma L_{s}\right) i_{s d}  \tag{7.16}\\
& V_{s q}=\left(R_{z}+s \sigma L_{s}\right) i_{s q} \tag{7.17}
\end{align*}
$$

The details of the control design are discussed later in Section 7.4.
The remaining terms in Equations 7.14 and 7.15 must be added to the output of each current controller for voltage compensation. Here, $\Phi_{\mathrm{rd}}$ is replaced by $\mathrm{L}_{0} . \mathrm{i}_{\mathrm{mrd}}$. Since the field weakening is not applied, it can be assumed that ;

$$
i_{s d}=i^{*}{ }_{s d}=i_{m r d}=i_{m r d}^{*}=\text { constant }
$$

Therefore, the term $\left(L_{d} / L_{R}\right)\left(d \Phi_{r d} / d t\right)$ in Equation 7.14 becomes zero and is not used in the voltage compensation. The resulting voltage reference signals $\mathrm{V}^{*}{ }_{s d}$ and $\mathrm{V}^{*}{ }_{\mathrm{sq}}$ are then converted to the three-phase voltages using the complex operator $\mathrm{e}^{\mathrm{j} \theta e}$. The threephase voltages $\mathrm{V}_{\mathrm{ao}}^{*}, \mathrm{~V}_{\mathrm{bo}}^{*}$ and $\mathrm{V}_{\mathrm{co}}^{*}$ are used as the input signals for the Venturini algorithm to generate the duty cycles for each switch in the matrix converter.

### 7.3.1 Third Harmonic Addition

In order to obtain the intrinsic maximum output voltage of the matrix converter the third harmonic of the input and output voltage waveforms are added to each of the output waveforms. As described in Chapter 2 the maximum output voltage is equal to $86.6 \%$ of the input voltage. This is achieved by using Equation 6.3 which consists of three terms, one for output voltage and the other two for third harmonic of the output voltage and input voltage, respectively. In the implementation of the Venturini algorithm it is straightforward to add the third harmonic of the input voltage waveform since the input angle is known. The vector control scheme illustrated in Figure 7.2 provides the instantaneous reference voltages and the
converter frequency, $\omega_{e}$. The reference voltages correspond to the first term of Equation 6.3. The third harmonic and the maximum value of the output voltage (q. $\mathrm{V}_{\mathrm{im}}$ ) can be calculated using this information.

### 7.4 Controller Design

### 7.4.1 Speed Controller

The block diagram of the controller is shown in Figure 7.3. The control loop consists of the PI controller characterised by $\mathrm{K}_{\mathrm{c}}$ and a , a limiter for the torque current and the mechanical characteristic of the machine with torque constant $\mathrm{C}(0.84)$ and inertia, $\mathrm{J}\left(0.015 \mathrm{kgm}^{2}\right)$. The delay caused by the current controller and the processing time has been ignored. As discussed in Section 3.6, large transient currents cause high peak currents in the switching devices. For this reason, the output of the speed controller is limited to avoid large currents in the motor and therefore in the snubber circuit. This ensures that the matrix converter operates within its rating during transients.


Figure 7.3 Laplace Block Diagram for the Design of Speed Controller

The CODAS software package program [61] was used for the design of the controller. The resultant PI controller for the induction motor has $\mathrm{K}_{\mathrm{c}}=0.5$ and $\mathrm{a}=$ 13.3 giving a bandwidth of 20 Hz and a damping factor of 0.707 on no-load. The torque current was limited to 4 A corresponding to the line output current of 7.2 A .

### 7.4.2 Current Controller

The block diagram shown in Figure 7.4 is common to both controllers since they are governed by the same "effective" armature time constant, $\sigma L_{s} / R_{8}$. The current control loop includes the PI controller, a limiter which represents the maximum phase voltage obtainable from the prototype converter ( 145 V ) and the stator characteristics of the induction motor with the resistance $\mathrm{R}_{\mathrm{s}}(2.75 \Omega$ ) and effective inductance $\sigma L_{s}(0.028 \mathrm{H})$. The delay caused by the control processing time has been ignored.

The PI parameters for d and q axis currents derived from the simulation (CODAS) are $\mathrm{K}_{\mathrm{c}}=7.8$ and $\mathrm{a}=397$. The bandwidth of the controller is 50 Hz . The response time to step changes in reference current is around 5 mS .


Figure 7.4 Laplace Block Diagram for the Design of the Current Controller

### 7.5 Implementation of Vector Control On the Transputer Network

### 7.5.1 Transputer Layout

Figure 7.5 illustrates the transputer network used for the implementation of the vector control strategy. The network is identical to that used for the slip control strategy described in Section 6.4. Two transputers are used in the network. The first one, "supervisor" executes two processes ("overseer" and "userio") running in parallel as discussed in Section 6.4.1. Here, the major difference is that the process, "overseer" reads the shaft position every sampling time, $500 \mu \mathrm{~S}$ and then calculates the flux angle. The speed is still sampled at a rate of 200 Hz . The process "overseer" on the first transputer is synchronised to the second transputer.

The second process, "userio" on the supervisor transputer executes the same program as that used for the slip control strategy apart from the "user menu" which includes more commands.

The second transputer, "control" which executes a sequential process performs measurements, two current controllers, the duty cycle calculations and the timer loading and control. This process has the high priority and is repeated every sampling time, $500 \mu \mathrm{~S}$.

### 7.5.2 Occam Implementation of the Vector Control Technique

The occam implementation on the supervising transputer ( $\mathrm{T}_{1}$ ) in pseudo code is shown in Figure 7.6. Two processes run in parallel under the reserved occam statement 'PRI PAR'. The first process, 'overseer' is a high priority process and is synchronised to the transputer, 'control'. The other process, 'userio' is a low priority process and it is only executed when there is a user interrupt.

The process 'overseer' is governed by a WHILE TRUE statement which provides an infinite loop. Position reading and speed calculation routines are identical
to those of the slip control. The torque current demand, $\mathrm{i}_{\mathrm{sq}}{ }^{\mathrm{q}}$ is derived from a digitally implemented PI controller acting on the speed error value. The digital implementation of the controller is described in Appendix F. In the 'calculate flux angle procedure', the slip frequency, $\omega_{s 1}$ is calculated by using Equation 7.11. This is then integrated and added to the shaft position, $\theta_{\mathrm{r}}$ to obtain the flux angle, $\theta_{\mathrm{e}}$. Flux angle cosine and sine values are read from the look-up table. The next routine provides communication with the transputer, 'control'. The demand flux current, $\mathrm{i}_{\mathrm{sd}}{ }^{*}$, torque current, $\mathrm{i}^{*}{ }_{\mathrm{sq}}, \omega_{e}$, $\cos \theta_{\mathrm{e}}, \sin \theta_{\mathrm{e}}$ and the 'enable/disable' command are sent to the control transputer. Then, the variables (for monitoring purposes) are received from the control transputer. The ALT construct performs the same task as that used for the slip control described in Section 6.4.3. The only difference is the disable command and the command for changing the demand flux current, $\mathrm{i}^{{ }^{*}}{ }_{\mathrm{sd}}$.

The 'userio' process is also similar to that used for slip control but there are two extra commands.
' i ' the new flux current demand is read from the user. This is then passed to 'overseer'.
' $b$ ' this demand disables the closed-loop control. 'Userio' passes the demand to 'overseer' and then the vector control is disabled.

When a speed demand is input from the user, this automatically enables the vector control. Therefore, there is no need to input another command to enable the closedloop control.

The occam implementation part of the control algorithm on the control transputer $\left(\mathrm{T}_{2}\right)$ is also given in Figure 7.6. Declarations and startup procedures are similar to those of the slip control. The current value of the transputer clock is initialized to the variable 'now'. The vector control process is sequentially executed and it is governed by a WHILE TRUE statement. The process starts communicating with the supervising transputer, $T_{1}$ to provide synchronisation. Then, the input phase voltages and output currents are measured through the $A / D$ converter. In the following procedure the input angle is calculated by using Equation 6.1 as described in Section 6.2.1. After that, the process receives the variables and 'code' from $T_{1}$



" $\operatorname{dGASA}$ NO "

Declarations
Initiate variables
Startup
HILE TRUE
SEQ
Clock ? now
TRUE
counter $=$ counter +1
. Calculate flux angle
... Calculate flux angle $\ldots$ Send i ${ }_{2}, i_{1}, \omega_{0}, \omega_{0}, \sin \theta_{0}, \cos \theta_{0}$

IF
demand $=$ '.. Pass variables to process 'userio'
$\square$... Receive demand speed from userio
demand $={ }^{\prime} \mathrm{i}_{\text {def }}$ '
Calculate duty cycles
-- Using Equations 6.2-6.3 ... Pulse dropping
... Load counters
...TIME?AFTER(now+500)
... Enable counters
required for vector control. The output currents are transformed to $d$ and $q$ axis currents as demonstrated in Appendix E . The measured values of input voltage $\mathrm{V}_{\mathrm{A}}$, input current $\mathrm{I}_{\mathrm{A}}$ and output current $\mathrm{I}_{\mathbf{L}}$ and $\mathrm{d}-\mathrm{q}$ axis currents $\mathrm{i}_{\mathrm{sd}}$ and $\mathrm{i}_{\mathrm{sq}}$ are then passed to $T_{1}$. The value of 'code' is used to determine which control is implemented. If 'code' $=\mathbf{0}$ the controller disables the vector control and initialises all the variables including the field and torque components of the current and the flux angle which are set to zero. In this case, the system operates in open-loop and does basically nothing. If the value of 'code' is not zero, then the vector control calculations are executed. The flux and torque current controllers are executed using the method outlined in Appendix $F$. The outputs of the current controllers are the $\mathrm{V}^{\prime}{ }_{\mathrm{sd}}$ and $\mathrm{V}^{\prime}{ }_{\mathrm{sq}}$ voltage demands which are limited to a value representing the maximum output voltage of the matrix converter. The voltage compensation described in Section 7.2 is applied to the demand voltages, $\mathrm{V}^{\prime}{ }_{s d}$ and $\mathrm{V}^{\prime}{ }^{\mathrm{sq}}$ by using the demand values for $\mathrm{i}_{\mathrm{sd}}$, $\mathrm{i}_{5 q}$ and frequency to modify the d and q axis voltage demands. This is achieved by using Equations 7.19 and 7.20 which are based on Equations 7.14 and 7.15, respectively.

$$
\begin{align*}
& V_{s d}^{*}=V_{s d}^{\prime}-\omega_{s} \sigma L_{s} i_{s q}^{0}  \tag{7.19}\\
& V_{s q}^{\cdot}=V_{s q}^{\prime}+\left(\omega_{s} \sigma L_{s}+\frac{L_{0}^{2}}{L_{R}} \omega_{e}\right) i_{s d} \tag{7.20}
\end{align*}
$$

The $\mathrm{V}_{\Delta \alpha}^{*}$ and $\mathrm{V}_{\Delta q}$ reference voltages are then transformed to three-phase demand voltages, $\mathrm{V}_{o c}{ }^{\circ}, \mathrm{V}_{\infty}^{\circ}$ and $\mathrm{V}_{\infty}^{*}$ to generate pulse widths using the Venturini algorithm. The inverse transformation is described in Appendix E. The third harmonic of the output voltage is calculated as outlined in Section 7.3.1. The rest of the process which consists of the pulse width calculation and counter control is similar to that used for the slip control. The total execution time for this process is $430 \mu \mathrm{~S}$ including the time to load the counters.

### 7.6 Experimental Results

A number of experimental tests have been performed to confirm the correct operation of the vector control implementation. Figure 7.7 shows the motor speed and current for a speed reversal from 1000 rpm to -1000 rpm with a torque current limit of 2.7 A (\% 80 of rated torque). The motor in this instance was not loaded and the total load is the inertia of the motor itself and the load from the cooling fan attached to the rotor. Figure 7.8 illustrates the $\mathrm{d}-\mathrm{q}$ axis currents and the speed for the same conditions. During the transient the torque current demand saturates and only comes out of saturation when the motor approaches the demanded speed. Figure 7.9 demonstrates the regenerative operation of the matrix converter. In this case, the input voltage and current are shown for the speed reversal above. The regeneration starts at 53 mS where the input current changes its phase. Figure 7.10 illustrates the transient performance of the machine in acceleration mode from standstill to 1000 rpm on no-load. The results in Figure 7.11 are for the same speed condition as Figure 7.10 but with the machine driving the extra inertia ( $0.132 \mathrm{kgm}^{2}$ ) of a DC load machine and with the torque current limit increased to $2.9 \mathrm{~A}(90 \%)$. The linear acceleration shows that the torque is held at its limiting value throughout the entire transient. Figure 7.12 and 7.13 show the corresponding $\mathrm{d}-\mathrm{q}$ axis currents and speed for the same conditions in Figure 7.10 and Figure 7.11, respectively. As can be seen from Figure 7.13 the torque current, $i_{s q}$ stays at its maximum value until the speed reaches its demand value.

Figure 7.14 shows the input phase voltage and current of the converter at the rated output current when the induction motor operates on load. The phase shift is due to the low-pass filter which is used to filter the input current for monitoring purposes. The input displacement factor is in fact unity. The waveforms in Figure 7.15 show the continuous operation of the converter in the naturally regenerative mode. A DC machine fed from a thyristor drive is used to drive the induction motor into regeneration. Figure 7.16 illustrates the transient performance of the system on load. In this case, the motor speed was increased from 500 rpm to 1000 rpm with $\%$

60 of the rated torque. The steady-state torque current, $i_{s q}$ stays at the value which is required to drive the load. However, $i_{2 q}$ saturates during the transient operation to accelerate the motor until the demand speed is reached. The transient performance of the motor for a speed reversal from 500 rpm to -500 rpm with load is shown in Figure 7.17. The load is maintained at $60 \%$ of the rated torque by the thyristor drive. The speed rapidly decelerates because of the load effect. The torque current, $i_{49}$ stays at the negative limit until the speed reaches the demanded value, -500 rpm . However, after the transient operation $i_{\text {sp }}$ returns close to its previous value since the drive is now regenerating. In fact during this transient the drive operates in all fourquadrants. Finally. Figures 7.18 and 7.19 show the steady-state motor line currents for rated torque at $23 \mathrm{~Hz}(700 \mathrm{pm})$ in the regenerative mode and motoring mode respectively.

The control system has been tested with different torque current limits. The results have shown that the rate of acceleration for the system increases proportionally with the torque current limit. This is good evidence that the vector control strategy is working well. In the results given the d and q axis currents are filtered with a low-pass filter for demonstration purposes (cut-off frequency is 18 Hz ) but, the control strategy uses unfiltered current measurements.


Figure 7.7 The Speod and Lixc Current of the Motor for Speed Reversal from 1000 rpm to -1000 rpm


Figure 7.8 The d-q Acis Currents and Spoci of the Mlotor for Speed Reversal from 1000 rpm to -1000 Tm


Figure 7.9 Regenerative Operation of the Alarix Converter for Speal Reversal from 1000 rpm to 1000 mm


Figure 7.10 The Motor Current and Speed for Acceleration from Standstill to 1000 rpm on No-Load


Figure 7.11 The Motor Current and Spead for Acceleration from Standstill to 1000 rpm with Large Incria Lo3d


Figure 7.12 The d-q Axis Currents and Moror Speed for Acceleration from Standstill to 1000 rpm on No-Lond


Figure 7.13 The d-q Axis Currents and Motor Speed for Acceleration from Standstill to 1000 rpm with Large Incrtia Load


Figure 7.14 The Input Phase Voltage and Current Waveforms of the Matrix Converter in Motoring Mode at Rated Output Current


Figure 7.15 The Input Phase Voltage and Current Waveforms of the Matrix Converter in Regenerating Mode at Rated Ouqput Current


Figure 7.16 The d-q Axis Currents and Motor Speed for Acceleration from 500 rpm to 1000 rpm with Constant Torque Load


Figure 7.17 The d-q Axis Currents and Motor Speed for Speed Reversal from 500 rpm to -500 rpm with Constant Torque Load


Figure 7.18 The Motor Line Current in Regenerative Mode at Rated Current ( 23 Hz )


Figure 7.19 The Motor Line Current in Motoring Mode at Rated Current ( 23 Hz )

### 7.7 Conclusions

A high performance vector-controlled matrix converter induction motor drive has been developed. The indirect vector control technique was chosen because it could be implemented with a drive system which consists of an ordinary induction motor coupled with a speed encoder. The occam implementation of the vector control technique with the user interface has been presented. The steady-state and transient performance of the induction motor drive with load and without load under the vector control technique used has been demonstrated with experimental results. The results show that the $d$ and $q$ axis currents were well decoupled although on-line identification of the rotor time constant, $\tau_{\mathrm{r}}$ has not been employed. The results also demonstrate the regenerative operation of the matrix converter in transient and steady-state. The torque component of the current, $i_{s q}$ was limited to ensure that the converter operates just under its current rating during transients.

## CHAPTER 8

## CONCLUSIONS

### 8.1 Summary of the Work

This thesis has discussed the design and implementation of a high performance vector-controlled matrix converter induction motor drive using transputer parallel processors. The Venturini PWM control algorithm has been analysed and implemented in real time on a transputer parallel processing network. This algorithm is capable of operating with sinusoidal input and output waveforms, whilst giving the intrinsic maximum output to input voltage ratio and enabling control of the input displacement factor. A scalar control algorithm which is based on the scalar comparison of the instantaneous input voltages has also been considered. The scalar algorithm also enables sinusoidal input currents to be drawn with adjustable input displacement factor. Both algorithms provide lagging or leading input displacement factor at the same angle as the load displacement factor, or any value in between these limits including unity, with a limited range of voltage gain.

A 3-phase to 3-phase prototype matrix converter rated at 2.5 kW has been constructed. The possible configurations of the bidirectional switch from unidirectional switching elements have been discussed and a series structure switch which has two devices in anti-series each with parallel diodes was used. This arrangement requires only one control signal and has a low forward voltage drop. The IGBT switching device has been chosen as the most appropriate controllable switch for the matrix converter by examining the current state of semiconductor technology from the point of view of controllability and power handling. A gate drive circuit for isolated gate devices has been developed using pulse transformers. The circuit eliminates the need for the isolated power supply by using the inherent charge
storage capability of the device input capacitance. The drive circuitry has a low component count and operates successfully with a wide range of duty cycle. A small R-C snubber circuit connected across to each bidirectional switch has been designed to limit the device voltage to an appropriate level. Very good correlation between the analysis and measured results were obtained. However, the results have shown that this simple snubber arrangement causes high current stresses in the devices at turn-on and increases the total converter losses.

The power losses in the converter have been analysed and calculated. It has been found that the snubber circuit results in a high power loss compared to the total semiconductor loss. The calculated value of the total power loss in the prototype converter has been verified by measurement. The efficiency of the converter has been measured as $89 \%$ and it is understood that for better efficiency either the snubber need should be eliminated by employing soft switching techniques or a more sophisticated snubber circuit should be designed. An effective protection of the prototype converter against over voltage and current has been provided to ensure the converter reliability. The converter power circuit has been tested at various operating conditions using a passive R-L load and the experimental results have shown the correct operation of the converter.

Transputer parallel processors were used to implement the matrix converter control algorithms. A suitable transputer network which can be easily modified to meet many diverse specifications for further research in this area has been designed along with the interface circuits, PWM generation and control. Two T800 transputers (INTEL) were found enough to implement the closed-loop control task for the matrix converter induction motor drive. Whilst one of the transputers performs the user interface and, speed measurements and control, the second executes the remaining part of the control task including voltage and current measurements and PWM calculations. The transputer network has been tested in open-loop by implementing both the Venturini algorithm and the scalar algorithm in real-time. Both algorithms give similar results with a passive R-L load. However, it has been found that the scalar algorithm is more sensitive to the input voltage measurements because of the
way in which the duty cycles are calculated for the switches. In addition, the realtime implementation of the scalar algorithm takes longer to compute than the Venturini algorithm. For these reasons, the Venturini modulation algorithm has been used in all control applications in this thesis.

The constant $\mathrm{V} / \mathrm{F}$ control strategy has been used to show the performance of the matrix converter driving an induction motor in open-loop. The drive system has been operated at rated, below rated and above rated speeds to verify its correct operation. In order to see the performance of the matrix converter induction motor drive in closed-loop control, a simple control system which provides constant $\mathrm{V} / \mathrm{F}$ control using slip regulation has been implemented. The drive system has been tested in both motoring and regenerative modes for steady-state and transient operation. The results have shown that the speed reversal from 1500 rpm to -1500 rpm takes 500 mS on no-load. The results also demonstrate the natural regenerative operation of the matrix converter.

The flexibility of the transputer network has been demonstrated in this project by developing a vector-controlled matrix converter induction motor drive using the same experimental rig as the slip regulation technique. The experimental rig is able to perform either control techniques with no hardware modifications. The only requirement was to modify some of the software routines on Transputer 2 and minor modifications on Transputer 1.

The indirect vector control technique was chosen for real-time implementation since the drive system used, which consists of an ordinary induction motor coupled with speed encoder, was suitable for this application. The performance of the drive system was demonstrated by the speed and current transients shown in the experimental results. In this control system the speed reversal from 1000 rpm to 1000 rpm takes 150 mS on no-load. The torque current limit was set just under the current rating of the prototype converter. However, various values of torque current limits were used to track the rate of acceleration for the system. It has been seen that the rate of acceleration increases proportionally with the torque current limit, which confirms the correct operation of the vector control strategy. A DC load machine fed
from a thyristor converter was used to demonstrate sustained regeneration and operation in all four quadrants of the torque-speed plane.

### 8.2 Potential Applications and Future Work

The high number of switching devices and the complicated protection requirements (because of the absence of freewheeling paths) in addition to the limited voltage ratio ( $\mathrm{q}=0.866$ ) of matrix converters makes it difficult for them to compete with inverters in the near future, although the matrix converter has many advantages over the inverter such as; four quadrant operation, sinusoidal input and output currents and controllable input displacement factor. However, the matrix converter may be used in the applications where the bulk of the drive becomes important and large capacitors are not desirable. The feature of unrestricted frequency changing of matrix converters can be applied to situations where a constant output frequency is required from an input supply with a variable frequency, for instance, generation of electricity from natural sources (eg wind turbines, wave power) [45] or the converter can be used to supply both AC or DC drives, by simply setting the output frequency to the desired frequency or zero, respectively.

As future work, the matrix converter may be commercialized if a bidirectional switch is made in a single package including the gate drive circuit. In this case, the converter will require only nine switches in order to provide direct AC-AC conversion without the need for a DC link. A more sophisticated snubber design can be considered to minimize the total converter losses and increase the converter current rating using the same devices.

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## APPENDIX A

## SNUBBER LOSS

One output phase of the matrix converter shown in Figure A. 1 is considered for the snubber loss calculations. It is assumed that the input voltages and the output current are constant during each switching sequence and all switching actions in the converter are ideal.


Figure A. 1 One Output Phase of the Matrix Converter

Consider the situation in which $\mathrm{S}_{\mathrm{Aa}}$ has been closed for some time and has just opened. This moment is represented in Figure A.2(a). In this condition all switches remain open for a delay time, $\tau$. During this delay time the energy lost in each resistor is;

$$
\begin{aligned}
E_{R} & =\left(\frac{I_{a}}{3}\right)^{2} R \tau \\
& =\frac{I_{a}^{2}}{9} R \tau
\end{aligned}
$$

and the total energy lost, $\mathrm{E}_{\mathrm{RT}}$ during this condition is the sum of the energy losses in the resistors. Therefore;

$$
\begin{align*}
& E_{R \tau}=E_{R 1}+E_{R 2}+E_{R 3} \\
& E_{R \tau}=\frac{I_{a}^{2} R \tau}{3} \tag{A.1}
\end{align*}
$$

In the delay time the capacitor charges by an amount $\Delta \mathrm{V}$ given by;

$$
\begin{equation*}
\Delta V=\frac{I_{a} \tau}{3 C} \tag{A.2}
\end{equation*}
$$

The condition just before $\mathrm{S}_{\mathrm{Ba}}$ closes is shown in Figure A.2(b).


Figure A. 2 Equivalent Circuits for Snubber Loss Analysis

While $S_{B a}$ is closed shown in Figure A.2(c) it is assumed that $C_{2}$ gets completely discharged. Hence, all energy stored in $\mathrm{C}_{2}$ when $\mathrm{S}_{\mathrm{Ba}}$ is first closed gets dissipated in $R_{2}$. Therefore, energy lost in $R_{2}$ is;

$$
E_{R 2}=\frac{1}{2} C\left(V_{B A}+\Delta V\right)^{2}
$$

While $S_{B a}$ is closed the current waveforms in $R_{1}, R_{2}$ and $R_{3}$ are the same (as shown in Chapter 3) hence, the same energy is dissipated in $R_{1}$ and $R_{3}$. Therefore, the total energy dissipated in the resistors during this condition is three times energy loss in the resistor, $\mathrm{R}_{2}$;

$$
\begin{equation*}
E_{R}=\frac{3}{2} C\left(V_{B A}+\Delta V\right)^{2} \tag{A.3}
\end{equation*}
$$

If the analysis is continued for one switching sequence, it is easy to show that the total energy dissipation, $\mathrm{E}_{\tau}$ in the resistors during the three delay times within one switching sequence is the sum of the energy losses in each delay time. Therefore;

$$
E_{\tau}=3 \frac{I_{a}^{2}}{3} R \tau=I_{a}^{2} R \tau
$$

The total energy dissipated in the resistors when each of the switches, $\mathrm{S}_{\mathrm{Aa}} \mathrm{S}_{\mathrm{Ba}}$ or $\mathrm{S}_{\mathrm{Ca}}$ is closed during one switching sequence is;

$$
\begin{align*}
& E_{o n}=\frac{3}{2} C\left[\left(V_{A C}+\Delta V\right)^{2}+\left(V_{B A}+\Delta V\right)^{2}+\left(V_{C B}+\Delta V\right)^{2}\right]  \tag{A.4}\\
& E_{o n}=\frac{3}{2} C\left[\left(V_{A C}^{2}+V_{B A}^{2}+V_{C B}^{2}+3 \Delta V^{2}+2 \Delta V\left(V_{A C}+V_{B A}+V_{C B}\right)\right]\right.
\end{align*}
$$

but,

$$
\begin{aligned}
& V_{A C}+V_{B A}+V_{C B}=0 \\
& V_{A C}^{2}+V_{B A}^{2}+V_{C B}^{2}=3 V_{L}^{2}
\end{aligned}
$$

where $V_{L}$ is the rms value of the input line voltage. and therefore;

$$
\begin{align*}
& E_{o n}=\frac{3}{2} C\left(3 V_{L}^{2}+3 \Delta V^{2}\right) \\
& E_{o n}=\frac{9 C V_{L}^{2}}{2}+\frac{9 C \Delta V^{2}}{2} \tag{A.5}
\end{align*}
$$

Substituting Equation A. 2 into Equation A.5;

$$
E_{o n}=\frac{9 C V_{L}^{2}}{2}+\frac{I_{a}^{2} \tau^{2}}{2 C}
$$

Hence, the total energy lost in the part of the converter feeding output phase a during the sequence is;

$$
\begin{aligned}
& E=E_{\tau}+E_{o n} \\
& E=I_{a}^{2} R \tau+\frac{9 C V_{L}^{2}}{2}+\frac{I_{a}^{2} \tau^{2}}{2 C} \\
& E=I_{a}^{2}\left(R \tau+\frac{\tau^{2}}{2 C}\right)+\frac{9 C V_{L}^{2}}{2}
\end{aligned}
$$

Where, $I_{a}$ is the output current during the sequence.
The total snubber loss of the entire converter in a particular sequence can be found by considering the other two output phases;

$$
E=\left(R \tau+\frac{\tau^{2}}{2 C}\right)\left(I_{a}^{2}+I_{b}^{2}+I_{c}^{2}\right)+3 \frac{9 C V_{L}^{2}}{2}
$$

but,

$$
I_{a}^{2}+I_{b}^{2}+I_{c}^{2}=3 I_{o}^{2}
$$

where $\mathrm{I}_{0}$ is the rms output current assuming the three output currents are sinusoidal and form a balanced 3-phase set. Hence, the total snubber loss in each sequence is constant and equals;

$$
E=3 I_{o}^{2}\left(R \tau+\frac{\tau^{2}}{2 C}\right)+\frac{27 C V_{L}^{2}}{2}
$$

Therefore, the total power loss in the snubbers is;

$$
P_{s n u b}=f_{s}\left[3 I_{o}^{2}\left(R \tau+\frac{\tau^{2}}{2 C}\right)+\frac{27 C V_{L}^{2}}{2}\right]
$$

Where; $f_{s}$ is the switching frequency.

## APPENDIX B

## OVER-CURRENT PROTECTION CIRCUIT



# APPENDIX C SPECIFICATIONS AND SPEED MEASUREMENT 

## C. 1 LEM Current Transducer

| Type | LEM LA 50-S/SP1 |
| :--- | :--- |
| Nominal Primary Current | 50 A |
| Ratio | $1: 2000$ (used 3:2000) |
| Accuracy | $\pm 0.5 \%$ |
| Linearity | $0.1 \%$ |
| Band Width | 150 kHz |
| Power Supply Range | $\pm 15 \mathrm{~V} \mathrm{( } \mathrm{ \pm 5} \mathrm{\%)}$ |

## C. 2 HTP 25 Current Transducer

| Type | Low profile HTP 25 |
| :--- | :--- |
| Nominal Primary Current | 25 A |
| Ratio | $1: 1000$ |
| Accuracy | $0.5 \%$ |
| Linearity | $0.1 \%$ |
| Band Width | 100 kHz |
| Power Supply Range | $\pm 15 \mathrm{~V}( \pm 5 \%)$ |

C. 3 Voltage Transposer

| Type | PSM |
| :--- | :--- |
| Max. Peak Input Voltage | $\pm 1 \mathrm{kV}$ |

Fixed Ratio 1:50

Programmable Ratio R/5000
Accuracy $1 \%$
Linearity $0.1 \%$
Band Width d.c to 50 kHz
Supply Voltage $\pm 15 \mathrm{~V}$
Input Impedance $\quad 5 \mathrm{M} \Omega$
Output Impedance $\quad 75 \Omega$

## C. 4 Squirrel Cage Induction Motor

This motor was originally designed to operate at 415 V and was rewound for the project. The new ratings of the three phase, $50 \mathrm{~Hz}, 207 \mathrm{~V}$, delta connected, 2.2 $\mathrm{kW}, 1420 \mathrm{rpm}$ squirrel cage induction motor are:

| $\mathrm{R}_{\mathbf{i}}=2.75 \Omega$ | $\mathrm{R}_{\mathrm{T}}^{\cdot}=2.14 \Omega$ |
| :--- | :--- |
| $\mathrm{~L}_{\mathrm{i}}=0.24 \Omega$ | $\mathrm{~L}_{\mathrm{t}}=0.244 \mathrm{H}$ |
| $\sigma=0.0979$ | $\mathrm{R}_{\mathrm{Fe}^{2}}=600.3 \Omega$ |

## C. 5 The Speed Encoder and Circuit Operation

Type BEC 735

Pulses Per Revolution 2500
Supply Voltage Range 5 V to 24 V
Frequency Response $\quad 125 \mathrm{kHz}$
Output Signals $\quad \mathrm{ChA}, \mathrm{ChB}, \mathrm{ChZ}$ (complementary pairs)
Output Format Complementary pair using 88C30 TTL/CMOS line driver

The HCTL-2016 CMOS compatible chip is used to proceed the pulse trains on the encoder lines. These signals are input to the HCTL-2016 via DS88C20 CMOS compatible differential line receivers used to reduce noise interference. The HCTL2016 provides a 16 -bit count value with its direction. More information on this chip may be found in the data sheet [59]. One of the advantages of this chip is that it multiplies the resolution of the signals by a factor of four ( 4 x decoding) so that the encoder signals become 10000 ppr of the shaft.

The control signals $\mathrm{Q}_{0}, \mathrm{Q}_{1}$ and $\mathrm{Q}_{2}$ from the controlling transputer shown in Figure 5.4 provide successive two-byte data reading from the HCTL-2016. The timing diagram for the control signals are shown in Figure C.1.

The OCCAM procedure executed every sample time, $500 \mu \mathrm{~S}$ for inputting the two-byte speed count value and calculating the speed is:

```
SEQ -- input speed
IF
counter := 10
        SEQ
        control.to.speed ! #00; #01
        speed.to.control ? msb
        control.to.speed! #04 ; #05
        speed.to.control ? lsb
        control.to.speed! #06 --reenable latch
        position := (msb << 8)\(lsb)
        SEQ
```

            Calculate speed
            ... Filter speed
            counter := 1
    TRUE
counter := counter +1

Once the position of the motor shaft is read from the encoder the "calculate
speed" fold executes the speed calculation of the motor in revolution per minute (rpm). This is done by using the equation given below;

$$
\text { speed }=\frac{\text { deltaposition }}{p p r * t}=\frac{(\text { position-position.l) }}{p p r * t} \quad(r p s)
$$

Where;
deltaposition : The position change on the shaft in 5 mS

| position | $:$ The updated value of the position |
| :--- | :--- |
| position.l | $:$ The last value of the position |
| $t$ | $:$ Speed sample time $(5 \mathrm{mS})$ |
| ppr | $:$ Pulses per revolution $(10000)$ |



Figure C. 1 Timing Diagram for Speed Input Board

## APPENDIX D

## ANALOG TO DIGITAL BOARD




# APPENDIX E <br> TRANSFORMATION EQUATIONS 

## E. 1 Three to Two (3/2) Phase Transformation

The instantaneous line quantities are transformed to the field orientated reference frame using a three to two phase transformation in the stator frame reference followed by a vector rotation from two-phase to two-axis field coordinates. The stator two-phase quantities are denoted by the subscripts $\alpha$ and $\beta$. Transformation of the current vector is shown as an example. However, the equations are valid for any machine variables.

The stator current vector is written as;

$$
\begin{align*}
& \bar{i}_{s}=i_{s c}+i_{s b} e^{j 2 \pi \sqrt{3}}+i_{\alpha c} e^{j \pi \sqrt{3}}  \tag{E.1}\\
& i_{s}=i_{s c}+j i_{s \beta}
\end{align*}
$$

Where;

$$
\begin{aligned}
& e^{j 2 \times \sqrt{3}}=-\frac{1}{2}+j \frac{\sqrt{3}}{2} \\
& e^{j \pi \sqrt{3}}=-\frac{1}{2}-j \frac{\sqrt{3}}{2}
\end{aligned}
$$

In Equation E.1, real and imaginary terms are separated to obtain $i_{s \alpha}$ and $i_{s \beta}$ currents. Thus;

$$
\begin{align*}
& i_{s c}=\frac{3}{2} i_{s a}  \tag{E.2}\\
& i_{s \beta}=\frac{\sqrt{3}}{2}\left(i_{s b}-i_{\alpha c}\right)
\end{align*}
$$

Transformation to field coordinates then follows as;

$$
\begin{align*}
& \bar{i}_{s} e^{-j \theta_{c}}=\left(i_{s \alpha}+j i_{s \beta}\right)\left(\cos \theta_{c}-j \sin \theta_{e}\right)=i_{s d}+j i_{s q}  \tag{E.3}\\
& i_{s d}=i_{s \alpha} \cos \theta_{c}+i_{s \beta} \sin \theta_{c}  \tag{E.4}\\
& i_{s q}=i_{s \beta} \cos \theta_{c}-i_{s \alpha} \sin \theta_{c}
\end{align*}
$$

## E. 2 Two to Three (2/3) Phase Transformation

Two to three phase transformation is achieved using the flux angle information as follows;

$$
\begin{align*}
& \bar{i}_{s}=\left(I_{s \alpha}+j i_{s \beta}\right)=\left(i_{s d}+j i_{s q}\right) e^{j \theta_{\rho}} \\
& i_{s \alpha}=i_{s d} \cos \theta_{e}-i_{s q} \sin \theta_{e}  \tag{E.5}\\
& i_{s \beta}=i_{s q} \cos \theta_{e}+i_{s d} \sin \theta_{e}
\end{align*}
$$

The two to three phase transformation is then obtained by solving Equation E. 2 together with $i_{s a}+i_{s b}+i_{s c}=0$;

$$
\begin{align*}
& i_{s a}=\frac{2}{3} i_{s \alpha} \\
& i_{s b}=-\frac{1}{3} i_{s \alpha}+\frac{1}{\sqrt{3}} i_{s \beta}  \tag{E.6}\\
& i_{\alpha c}=-\frac{1}{3} i_{s \alpha}-\frac{1}{\sqrt{3}} i_{s \beta}
\end{align*}
$$

## APPENDIX F

## DIGITAL IMPLEMENTATION OF LAPLACE COMPENSATION FUNCTIONS

The discretisation of the Laplace transfer functions employed in this project was achieved using the Bilinear Transformation given in Equation F.1.

$$
\begin{equation*}
s=\frac{2\left(1-Z^{-1}\right)}{T\left(1+Z^{-1}\right)} \tag{F.1}
\end{equation*}
$$

Where; s : The Laplace operator
$Z^{-1}$ : A unit delay operator
T : The sampling time

Discretisation of the original transfer function is accomplished by substituting Equation F. 1 into the Laplace equation and manipulating the resultant equation to give a transfer function for the current sampled signals in terms of previously sampled signals. The following definitions are required for the digitised transforms described:
$y_{k}$ : Current transfer function output
$e_{k}$ : Current transfer function input
$y_{(x-1)}$ : Previous transfer function output
$\mathbf{e}_{(\Omega-1)}$ : Previous transfer function input

## F. 1 First Order Low-Pass Filter

A simple first order low-pass filter is given by the Laplace transfer function;

$$
\begin{equation*}
\frac{y}{e}=\frac{\omega}{s+\omega} \tag{F.2}
\end{equation*}
$$

Where; $\omega$ is the cut-off angular velocity

Substituting Equation F. 1 into Equation F.2;

$$
\begin{equation*}
y\left[1+\left(\frac{\omega-2 / T}{\omega+2 / T} z^{-1}\right]=e\left(\frac{\omega}{\omega+2 / T}\right)\left(1+Z^{-1}\right)\right. \tag{F.3}
\end{equation*}
$$

The resultant digital filter is thus implemented as;

$$
\begin{equation*}
y_{k}=y_{(k-1)}\left(\frac{2 / T-\omega}{2 / T+\omega}\right)+\left(e_{k}+e_{(k-1)}\right)\left(\frac{\omega}{\omega+2 / T}\right) \tag{F.4}
\end{equation*}
$$

## F. 2 Proportional Plus Integral (PI) Compensation

The Laplace transform for a PI controller is given as;

$$
\begin{equation*}
\frac{y}{e}=K \frac{s+\omega}{s} \tag{F.5}
\end{equation*}
$$

Substituting Equation F. 1 into Equation F.5;

$$
\begin{equation*}
y\left(1-Z^{-1}\right)=e\left(\frac{K T}{2}\left((2 / T+\omega)-Z^{-1}(2 / T-\omega)\right)\right) \tag{F.6}
\end{equation*}
$$

The resultant digital PI controller is thus implemented as;

$$
\begin{equation*}
y_{k}=y_{(k-1)}+\left(K+\frac{\omega K T}{2}\right) e_{k}-\left(K-\frac{\omega K T}{2}\right) e_{(k-1)} \tag{F.7}
\end{equation*}
$$

