Matrix Converter for Frequency Changing Power Supply Applications

Saúl López Arévalo, MSc

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Abstract

The purpose of this work is to investigate the design and implementation of a 7.5kVA Matrix Converter-based power supply for aircraft applications (GPU Ground Power Unit). A Matlab/Simulink as well as SABER simulation analysis of the candidate Matrix Converter system is provided. The design and implementation of the Matrix Converter is described, with particular attention to the strict requirements of the given power supply application. This AC-AC system is proposed as an effective replacement for the conventional AC-DC-AC system which employs a two-step power conversion.

The Matrix Converter is an attractive topology of power converter for power supply applications where factors such as the absence of electrolytic capacitors, the potentiality of increasing power density, reducing size and weight and good input power quality are fundamental.

An improved control structure is proposed. This structure employs an ABC reference frame implementation comprising at the Repetitive Control strategy combined with a traditional tracking controller in order to attenuate or eliminate the unwanted harmonic distortion in the output voltage waveform of the Matrix Converter and to compensate for the steady-state error. The system with the proposed control was initially fully analyzed and verified by simulation. The analysis of the input and output waveforms identified the constraints that need to be satisfied to ensure successful operation of the converter. Finally, to demonstrate both the Matrix Converter concept and the control strategy proposed, a 7.5kVA prototype of the proposed system was constructed and tested in Nottingham PEMC laboratory. The experimental results obtained confirmed the expectations from the simulation study and the validity of the power converter and control design.

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Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 The Matrix Converter

This thesis is concerned with the design and implementation of a Matrix Converter for Frequency Changing Power Supply Applications. Typically such units are used to convert between 50/60Hz supplies available in airports to a 400Hz one for aircraft supply when they are parked in their bays. This work will consider the design, simulation, practical construction and testing of a 7.5kVA system prototype. A Matrix Converter is a device used for converting directly AC energy into AC energy; the main feature of this device is to convert the magnitude as well as the frequency of the input into a desired magnitude and frequency of the output with an "all-silicon" solution. Mainly, a Matrix Converter consists of nine bi-directional switches, which are required to be commutated in the right way and sequence in order to minimize losses and produce the desired output with a high quality input and output waveforms.

After the controlled rectifiers were developed in the early 1930's, it was realized that this provided the possibility of generating alternating currents of variable frequency directly from a fixed frequency AC supply, the positive rectifier supplying the positive half cycles of current and the negative rectifier the negative half cycles. This

system was called cycloconverter at its early stage and this proved to be so appropriate that nowadays it is still used in some high power applications because of high power requirements and the Matrix Converter technology is still not available widely. Moreover, most of the industrial applications require frequencies in the range of 50Hz-60Hz, which is easily obtained by the cycloconverter. For a three-phase to three-phase cycloconverter, 36 thyristors are required. This makes that cycloconverter systems are large and complicated and tend to be used in applications where high power is required (1MW and up) [2]. Today, high power, multi-megawatts, thyristor based cycloconverters are very popular for driving induction and wound field synchronous motors. Some general applications of cycloconvertesr are [3]:

- **Cement and ball mill drives**
- **Rolling mill drives**
- **Slip-power recovery Scherbius drives [4] [5]**
- **Variable-speed, constant-frequency (VSCF) power generation for aircraft 400Hz power supplies**

Frequency conversion or modulation techniques can be used to take a fixed frequency or DC source and provide any load with a different or variable frequency supply. Cycloconversion is mostly concerned with converting directly a low-frequency waveform into a desired different frequency waveform. A cycloconverter is an arrangement of two converter connected back to back as shown in Figure 1.1 [6].

Matrix Converters were first mentioned in the early 1980's by Alesina and Venturini [7]. They proposed a general model and a relative mathematical theory for high-frequency synthesis converters. They stated that the maximum input-output transformation ratio possible for the new AC-AC converter is $\sqrt{3}/2$ and also, they suggested a specific modulation and a feed-back-based control implementation of the proposed converter [8]. The AC-AC Matrix Converter is optimal in terms of minimum switch number and minimum filtering requirements. A three-phase AC-AC Matrix

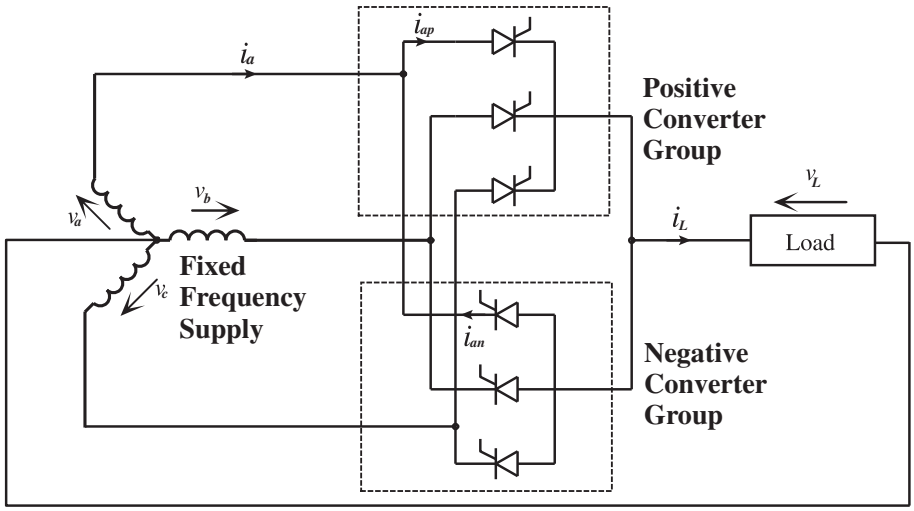


Figure 1.1: Single-phase load fed from a three-pulse cycloconverter.

Converter consists basically of nine bidirectional voltage-blocking current-conducting switches. These switches are arranged in a matrix and by using this arrangement any input phase can be connected to any output phase at any time. Figure 1.2 shows such arrangement [9].

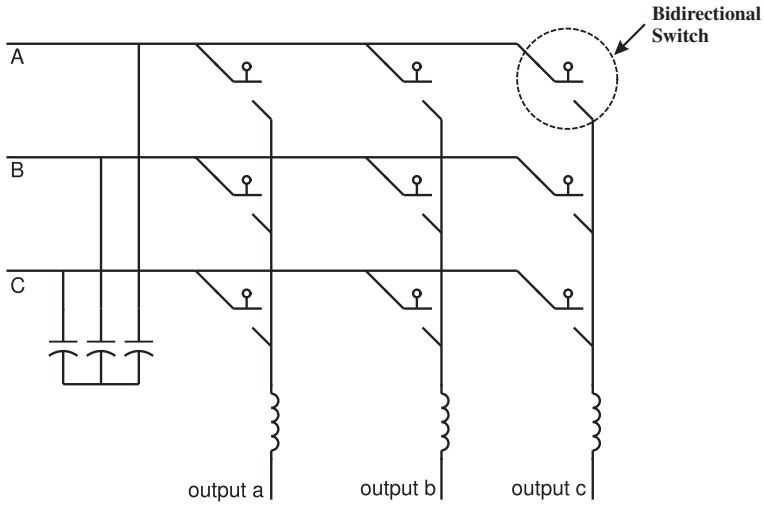


Figure 1.2: Structure of Matrix Converter.

1.2 Control

There has been a gap between modern control theory and practice. However, a practicing engineer who knows a control system well, modifies, extends, and combines modern control theory with classical control theory. Successful results using developed control theory, especially to servo-motor and motion control, have been widely reported in the literature [10] [11] [12]. The theory may be given in s domain (continuous). However, using bilinear transformation or direct design the theory can be replaced by a discrete (digital) control method (which is needed when implementing the control with a DSP). Digital controllers can be considered sometimes as digital filters, they introduce delays. These delays depend on the order of the polynomial implemented as the controller. The control is defined as to manipulate an object (in this case the Matrix Converter) so as to serve a certain purpose (that is to make it work as required) [13].

The term controller in a feedback control system is often associated with the elements of the forward path, between the error signal and the control variable. But it also sometimes includes the summing point, the feedback elements, or both, and some times the term controller or compensator is used synonymously [14]. Figure 1.3 shows a general structure of a plant with a second order controller.

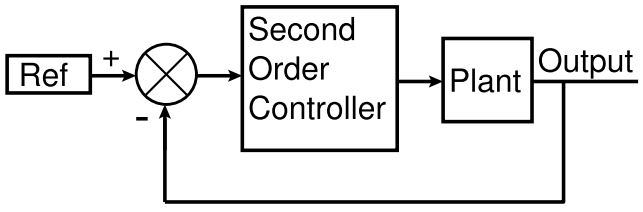


Figure 1.3: Structure of plant with second order controller.

1.3 Modulation

Applications areas of power converters still expand thanks to improvements in semiconductor technology, which offer higher voltage and current ratings as well as better switching characteristics. The main advantages of modern power electronic converters, such as high efficiency, low weight, small dimensions, fast operation, and high power densities, are being achieved though the use of the so-called switch mode operation, in which power semiconductor devices are controlled in ON/OFF fashion (no operation in the active region) [15]. This leads to different types of pulse width modulation (PWM), which is a basic energy processing technique applied in power converter systems. In modern converters, PWM is a high-speed process ranging from a few kiloHertz (motor control) [16] up to several megaHertz (resonant converters for power supply) depending on the rated power [17].

Figure 1.4 shows a Voltage Source Converter (VSC) which is used to provide ac variable voltage - variable frequency to a load from a fixed voltage - fixed frequency supply. This has been the traditional power converter employed for variable speed drive applications [3]. According to Figure 1.4, the input supply is first rectified then it is applied to the load by the inverter stage. The control of the output of this two stage converter is achieved by modulating the duty cycles of the devices in the inverter stage so as to produce near sinusoidal output currents in the inductive load machine, at a desired amplitude and frequency [18].

Figure 1.4 shows a large capacitor placed across the DC link to provide a constant DC voltage source with small variation and energy storage. This capacitor is considered large compared to the size of the rectifier and inverter semiconductor components. This means that a large capacitance is needed but within a reasonable volume, therefore electrolytic capacitors are normally used for the DC link components. Electrolytic capacitors typically occupy $30 - 50\%$ of the total volume of the converter for power levels greater than a few kW and in addition to this they are temperature sensitive.

Due to the diode bridge front end, the inverter circuit shown in Figure 1.4 will draw

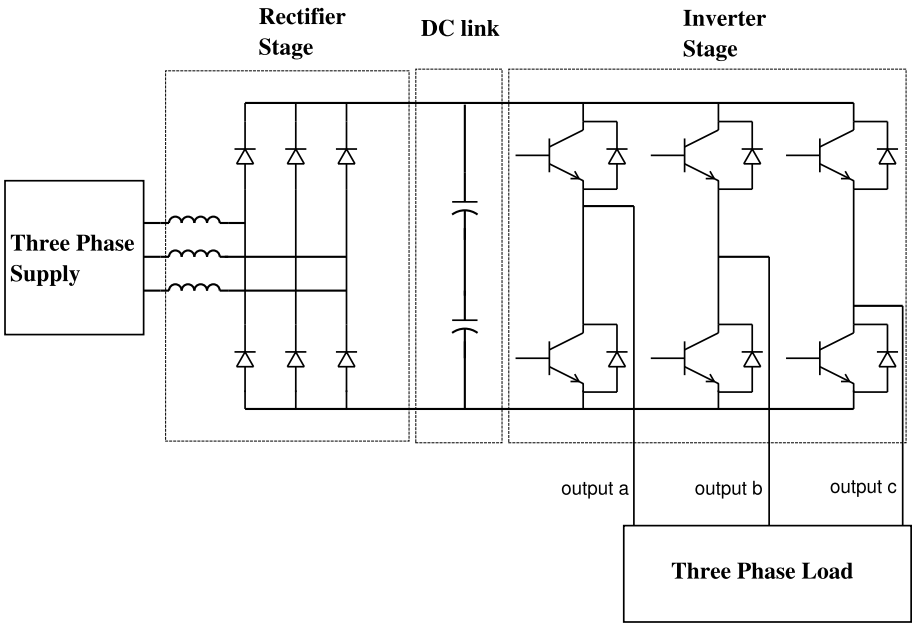


Figure 1.4: Basic diagram of the Voltage Source Converter, power components.

input currents that are rich in 5th and 7th harmonics, which can become a significant problem at increased power levels because the harmonic distortion injected to the mains and the power losses. This problem can be solved by employing an active PWM rectifier front end as shown in Figure 1.5, which can be modulated to draw near sinusoidal input currents. The active, or sinusoidal front end inverter, has the added advantage that the power flow can be bi-directional. However the DC link capacitors are still large (around 30-50% of the total volume) and so are the input inductors [19] [20].

An alternative AC-AC power converter, the Matrix Converter, is discussed and used in this thesis. The Matrix Converter, shown in Figure 1.6, consists of an array of bi-directional switches where any input phase can be connected to any output phase. The duty cycle of the switches can be modulated to produce the desired output amplitude and frequency. The Matrix Converter is also described as a direct AC-AC converter because it requires no intermediate energy storage [21] [22].

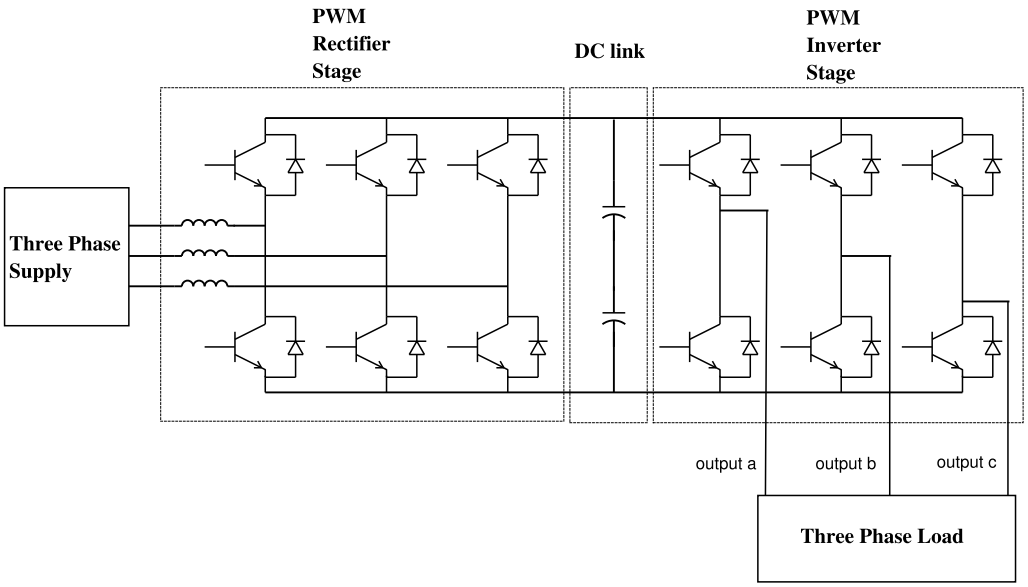


Figure 1.5: Schematic of the back to back converter.

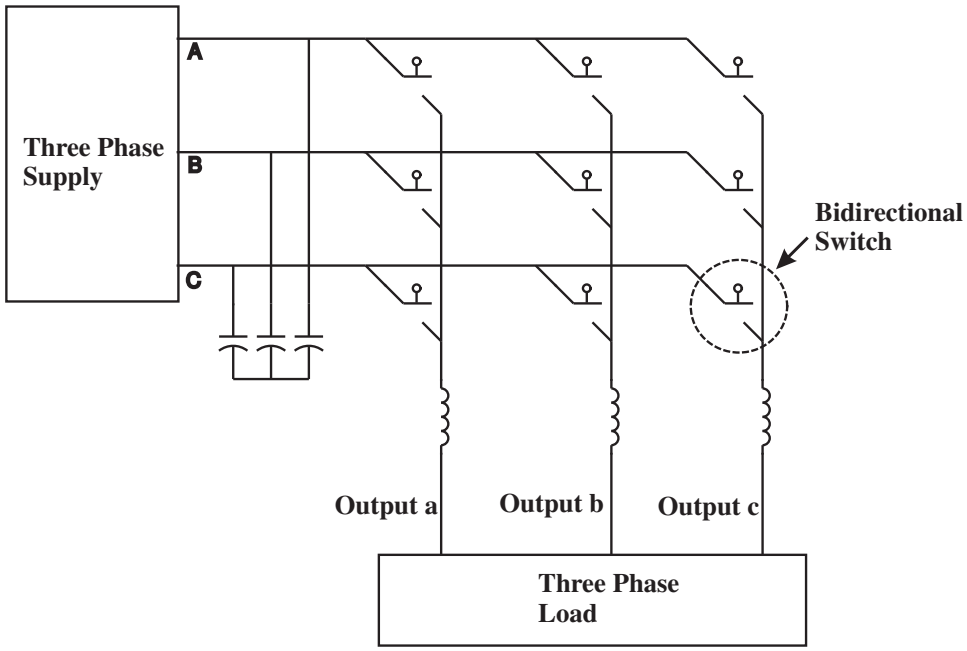


Figure 1.6: Simplified representation of a Matrix Converter system.

Much of the work on Matrix Converters over the past twenty years has been concentrated on modulation algorithms and, more recently, on the practical implementation issues such as the devices commutation, have largely been solved. One of the key benefits of the Matrix Converter technology is the possibility of greater power density due to the absence of a DC link. This is translated into a realistic advantage if the filter size is also optimized, by having a sufficiently high switching frequency of semiconductor devices. This means, though, a compromise between filter size and semiconductor losses must be found.

Factors such as the absence of electrolytic capacitors, the advantage for increasing power density, reducing size, reducing weight and obtaining good input power quality are fundamental to power supply applications [23] [24] [25].

The purpose of this work is to investigate the design and implementation of a 7.5kVA Matrix Converter for frequency changing power supply applications. SABER and Matlab/Simulink simulations of the whole system (which includes the Matrix Converter, input and output filters) are provided. The design and implementation of the Matrix Converter is described, with particular attention to the strict requirements of the given power supply application. Finally, the Matrix Converter system using different types of load is assembled and tested.

1.4 Research Outcomes

The system will have the following technical specifications:

- **Rated input voltage:** 415V (rms, line voltage). Three-phase, three-wire
- **Input frequency:** 50Hz.
- **Input harmonics:** relevant IEEE standards, IEEE 519 [26].
- **Rated output voltage:** 117V (rms, phase voltage). Three-phase, three-wires.

- **Voltage tolerance:** 114V to 120V
- **Output frequency:** 400Hz.
- **Voltage total harmonic distortion:** to be less than 4%.
- **Voltage individual harmonic distortion:** to be less than 2%.
- **Voltage transients:** not to exceed 10% of nominal voltage when switching the load between 0% and 100% and back.
- **Rated output power:** the Matrix Converter system is designed for a total power of 7.5kVA.
- **Load conditions:** unbalanced condition of 40%. Resistive-inductive load.

1.5 Project Objectives

The research work presented in this thesis has generated the following novel achievements:

- A comparative study has been performed to ascertain the suitability of different Matrix Converter systems for power supply applications. A Matrix Converter control system was devised for each of the different load conditions. These include resistive load balanced, resistive load unbalanced, resistive-inductive load balanced, resistive-inductive load unbalanced and load disconnected. An improved control structure for the Matrix Converter system was introduced in simulation to control the output voltage. This structure which includes a Repetitive Control was simulated and the physical effects on the Matrix Converter system such as instability and harmonic distortion were investigated and results presented. Each of the control systems were then compared on the basis of the results of their analysis and their potential merits for power supply application in terms of power quality, harmonic content and power density determined.

- A 7.5kVA Matrix Converter has been designed and built to meet the requirements of power supplies driving different types of load. Issues which have previously prevented successful implementation such as device packaging, converter layout and protection have been addressed and solutions have been presented.
- The use of the overvoltage clamp circuit to improve the reliability of the Matrix Converter circuit by giving it the ability to withstand a circuit failure, such as current direction feedback failure has been investigated. No electrolytic capacitors were employed in the protection circuit or the input filter. In response to important issues such reliability requirements, polypropylene film capacitors were utilized to minimize the power converter volume.

1.6 Thesis Overview

The remainder of this thesis is divided into the following Chapters:

In Chapter 1, the Matrix Converter research concept for power supply applications is introduced and discussed. Particular attention is given to the different load conditions driven by the Matrix Converter system and how these conditions influence the output voltage waveform quality.

In Chapter 2, the Matrix Converter concept is discussed and the mathematical model from which the modulation problem can be derived is introduced. A brief description of the Venturini and Space Vector Modulation methods are given. The practical implementation issues are introduced and the proposed solutions are discussed. A comparison between the conventional topology of power converters for AC-AC conversion and the Matrix Converter is provided in terms of a predicted reliability study.

SABER as well as Simulink simulation analysis of the Matrix Converter system, driving different types of load, is described in Chapter 3. The main differences between the control systems used are highlighted and the reason for the choice of the proposed

control structure for the given application, is discussed.

The design and construction of the 7.5kVA Matrix Converter is described in Chapter 4. The output voltage control of the power converter is also described and the used of the Repetitive Controller is proposed.

In Chapter 5, a full description is given of the different assembly and testing stages of the power converter first, the Matrix Converter system and, finally, the control strategy of the output voltage. The correspondent series of results is presented. The Chapter concludes with the description of the testing of the Matrix Converter based power supply.

In Chapter 6, conclusions are drawn from the work presented and the goals achieved. Also, areas of further research are highlighted.

Chapter 2

Modulation Techniques and Control

2.1 Introduction

AC to AC power conversion can be realized by using a rectifier stage and an inverter stage or by using a Direct or Matrix Converter (MC). A Matrix Converter uses only one conversion stage compared to two stages for the rectifier/inverter solution. Each converter topology has particular advantages and disadvantages, the choice, therefore, depends on the requirements of the application.

The state of the art in Matrix Converter technology is presented in this chapter. The Matrix Converter concept is introduced with the mathematical model circuit operation and associated modulation techniques. Modulation techniques used in Matrix Converters have been considered by researches for many years [27]. These papers have proposed different modulation techniques. The modulation techniques section of this chapter presents the main modulation techniques used in Matrix Converters. The two Venturini modulation methods [28][8] and the scalar modulation scheme [29][30] are reviewed. A detailed analysis of Space Vector Modulation (SVM) algorithms for

Matrix Converters is then presented. The conventional SVM algorithm [1] usually generates both even and odd order harmonic voltages. The basic diagrams and the permitted switching states of the converter are included. Finally, this section presents the indirect modulation method [31][32].

The next two sections present the implementation of the required bi-directional switches and the techniques used for safe current commutation between these switches.

Issues regarding the design of both the output and input filters are included in the filters design section. Frequency response plots are also included in order to show the cut-off and resonant frequencies for both filters.

In order to control the output voltage of the converter a voltage control loop is used. The control section of this chapter focuses on the design of the second order controller required for this voltage control loop in both the s and z domain. The design of output filter described in the previous section is used to design the controller. In order to improve the output voltage waveform quality a Repetitive Controller (RC) is proposed. The design of this controller is included in the Repetitive Controller section. A structure of the proposed Repetitive Controller is given, as well as the values of parameters used in the implementation.

2.2 Matrix Converter Concept

The power converter topologies used in industry can be grouped as follows:

- **Inverters:** used to change DC voltage or current to AC voltage or current. Inverters are widely used in variable-speed drives and AC power supplies.
- **Rectifiers:** used to change AC voltage or current (usually from a grid supply of 50 or 60Hz) to DC voltage or current.

Rectifiers and inverters are often combined to form indirect AC to AC Converters, as shown in Figure 2.1.

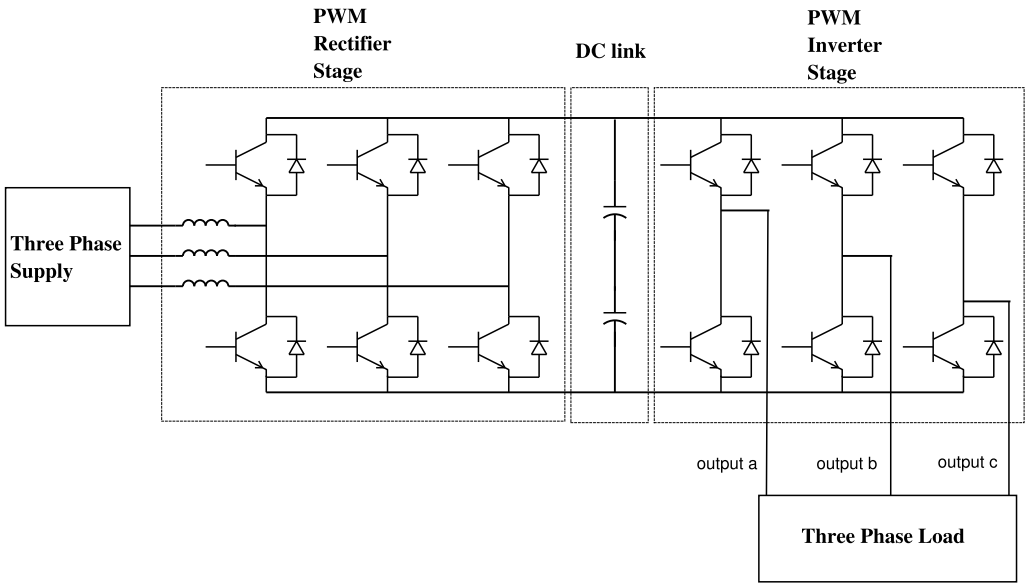


Figure 2.1: Schematic of AC to AC converter.

Figure 2.2 shows a simplified block diagram of a 3-phase to 3-phase Matrix Converter drive system. As it can be seen in the figure, the Matrix Converter circuit consists of an array of nine bi-directional switches, constructed from unidirectional power devices, arranged in such a way as to enable any input line to be connected to any output line at any time. The switch duty cycles are modulated to generate the desired output waveform on the basis of the input supply voltages and the demanded output voltages. The demanded voltages are generally the output of a cascaded speed and current control loop. A Matrix Converter can be viewed as an "all-silicon solution" to the general AC-AC power conversion problem. Compared to the conventional rectifier/inverter topology, Matrix Converters have many advantages. No DC-link energy storage is required for the Matrix Converter topology. This removes the necessity for bulky electrolytic capacitors, which are intolerant to high temperatures and have a relatively short life time [33] [34] [35] [36]. As a result of the elimination of the DC-link a potentially compact converter system can be designed. Bi-directional power flow is straightforward with a Matrix Converter. By controlling the switching devices

appropriately both the output voltage and the input current are sinusoidal with harmonics only around or above the switching frequency of semiconductor devices. The displacement factor (df) is used to quantify the fact that not all of the fundamental current gives rise to power when there is a phase shift between voltage and current. Unity displacement factor can be achieved if an appropriate modulation strategy is used, and can be achieved irrespective of the load. The type of load for this case is resistive-inductive and the capacitive load has not been considered.

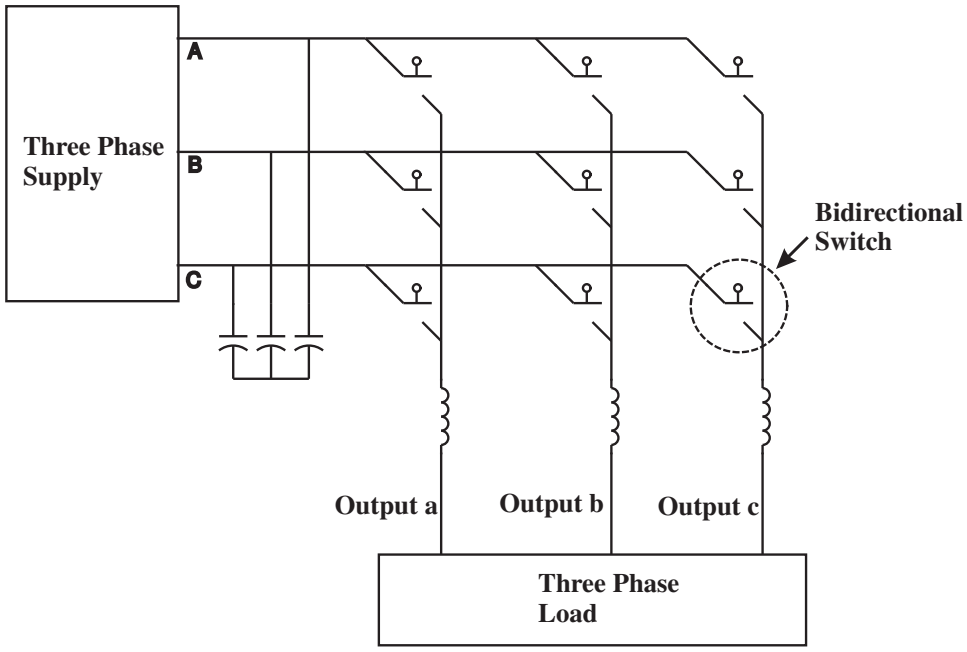


Figure 2.2: Simplified representation of a Matrix Converter system.

To understand the modulation problem and its solution, consider the arrangement shown in Figure 2.2. The fundamental requirement can be stated as follow; a balanced set of three-phase input voltages is expressed as,

$$[\mathbf{V_i}(\mathbf{t})] = \begin{pmatrix} V_{i1}(t) \\ V_{i2}(t) \\ V_{i3}(t) \end{pmatrix} \tag{2.1}$$

Where:

$$[\mathbf{V_i(t)}] = \begin{pmatrix} V_i cos(\omega_i t) \\ V_i cos(\omega_i t - 2\pi/3) \\ V_i cos(\omega_i t + 2\pi/3) \end{pmatrix} \tag{2.2}$$

With these input voltages the switching function $M(t)$ that will produce a set of desired three-phase output voltages can be determined,

$$[\mathbf{V_o(t)}] = \begin{pmatrix} V_{o1}(t) \\ V_{o2}(t) \\ V_{o3}(t) \end{pmatrix} \tag{2.3}$$

Where:

$$[\mathbf{V_o(t)}] = [M(t)]. \begin{pmatrix} V_{i1}(t) \\ V_{i2}(t) \\ V_{i3}(t) \end{pmatrix} \tag{2.4}$$

$$[\mathbf{V_o(t)}] = \begin{pmatrix} V_o cos(\omega_o t + \theta_o) \\ V_o cos(\omega_o t + \theta_o - 2\pi/3) \\ V_o cos(\omega_o t + \theta_o + 2\pi/3) \end{pmatrix} \tag{2.5}$$

where θ_o is an arbitrary output voltage phase angle [9]. The switching function, $M(t)$, must satisfy the previous stated conditions. Several modulation strategies have been proposed [37] [38] [39]. These modulation strategies give different voltage conversion ratios and the number of commutations employed in each modulation strategies is different.

With the price of power semiconductors falling, Matrix Converters could become a more attractive alternative to the back-to-back converter in applications where sinusoidal input currents and true bi-directional power flow are required. The voltage transfer ration (q) is the relationship of the output voltage to the input voltage. The voltage transfer ratio limitation, which will be shown in Section 2.3.2, is a real problem if a standard machine and a standard supply are to be used. The voltage ratio limitation is not the main issue in the design of the Matrix Converter system when the application allows the specification of the output voltage. More important innovative and efficient strategies of implementing circuit protection [40] for the Matrix

Converter will ease the way for the commercialization of this converter in applications such as integrated motor drives, aerospace and marine propulsion applications where power density, space and weight play a fundamental role. This view is reinforced by the possibility that the Matrix Converter could be the ideal converter topology to employ future technologies such as high temperature silicon carbide devices because they can work a environments with a large range of temperatures. Adding to this, the absence of large electrolytic capacitors helps to overcome the problem of electronic equipment operating in difficult environmental conditions [41]. The electrolytic capacitors are limited in the range of temperature in what they can operate.

2.3 Modulation Techniques

In 1964 Schönung and Stemmler [42] proposed the triangular carried-based sinusoidal pulse width modulation (PWM) strategy for three-phase inverter modulation. The space vector modulation (SVM) strategy was proposed by Pfaff, Weschta and Wick [43] in 1982. They based the proposed SVM method on the development of new technology microprocessors. The SVM algorithm was improved by van der Broeck, Skudelny and Stanke [44]. This method become a basic modulation technique for three-phase PWM inverters. Pulse width modulated three-phase inverters can operate under voltage (open loop) or current (closed loop) control. Current-controlled systems have better performance and faster response than the voltage-controlled systems because the control of the current is done in the inner loop of the control system [15]. AC industrial drives normally employ cascade control structure. It consists of multiple loops: the inner most loop is the current loop (which is the fastest), followed by speed loop and position loop. Implementing cascade control structure requires the current to be controlled. Good current controlled schemes should produce low current ripple, good tracking capability with zero steady state error, and fast dynamic response. The faster the response of the loop, the faster the disturbance is taken into consideration. The inner current loop ia a servo motor drive plays a more important role than just limiting the current incase of overload. This loop operates continuously to regulate

the motor-developed torque so as to meet the load demand, and for meeting the speed trajectory specified by the motion controller. Motor drives of high dynamic response currently employ PWM current source [45]. Current-controlled systems connected to AC motors are used to reduce the dependence on stator parameters and also to allow fast action on the flux and torque developed by the controlled motor. Current is regulated to achieve the desired active and reactive power. It is also controlled to minimize or compensate the line power factor and current harmonics. A control structure comprising of an internal current feedback loop is a vital part of most applications of three-phase voltage-source power converters. Due to this fact, the quality of the applied current control strategy has an important role in the performance of the power converter system.

In principle, all modulation schemes aim to create trains of switched voltage or current pulses which have the same fundamental volt-second or amp-second average (i.e, the integral of the waveform over time) as a target reference waveform. The major difficulty with these trains of switched pulses is that they also contain unwanted harmonic components which should, ideally, be minimized since they are injected to the mains and degrade the quality of energy. This degradation of energy cause malfunction of other equipments.

The Matrix Converter control strategies were first mentioned by Alesina [7] and Venturini [28]. The block diagram of the Matrix Converter is represented in Figure 2.2. Various modulation techniques can be applied to the AC-AC matrix Converter to achieve sinusoidal output voltages and input currents. An optimal modulation strategy should minimize the input current and the output voltage harmonic distortion and device power loss [46]. The first modulator proposed for Matrix Converters, known as the Venturini modulation, employed a scalar model [7]. This model gives a maximum voltage transfer ratio of 0.5. An injection of a third harmonic of the input and output voltage was proposed in order to fit the reference output voltage in the input system envelope. This technique is used to achieve a voltage transfer ratio with a maximum value of 0.866.

In this analysis, a three-phase input, three-phase output converter is considered. Because the Matrix Converter is symmetrical, the designation of input and output ports is arbitrary. However, for any sensible mode of operation, one port should be considered to have a voltage stiff characteristic and the other port a current stiff characteristic. In this case stiff means that the voltage or current must be constant with no interruptions or sudden variations. For the following analysis it is assumed that the input port is voltage stiff and the output port is current stiff. In a practical Matrix Converter an input filter is included to circulate the high frequency switching harmonics and provide the voltage stiff characteristic. The output inductance is usually part of the load giving a current stiff characteristic. This study considers that upper case suffixes always denote the input phases and lower case suffixes denote the output phases as shown in Figure 2.2.

The concept of switching functions [47] is used to derive a mathematical model of the Matrix Converter. Ideal switching is assumed in this analysis. The switching function, S_{Kj}, is defined as the representation of the switch connecting input line K to output line j. When the switch is ON, the switching function has a value of 1 and when the switch is OFF, the switching function has a value of 0. The instantaneous current and voltage relationships can then be written as given in Equations 2.6.

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} S_{Aa}(t) & S_{Ba}(t) & S_{Ca}(t) \\ S_{Ab}(t) & S_{Bb}(t) & S_{Cb}(t) \\ S_{Ac}(t) & S_{Bc}(t) & S_{Cc}(t) \end{bmatrix} \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix}$$

$$\begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} = \begin{bmatrix} S_{Aa}(t) & S_{Ab}(t) & S_{Ac}(t) \\ S_{Ba}(t) & S_{Ba}(t) & S_{Bc}(t) \\ S_{Ca}(t) & S_{Cb}(t) & S_{Cc}(t) \end{bmatrix} \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \tag{2.6}$$

One of the most important rules that Matrix Converters must obey is the one expressed by Equation 2.7. This equation states that at any instant one and only one switch on each output phase must be closed. Analyzing the arrangement shown in Figure 2.2, which shows that there are no freewheeling diodes, this restriction means that the short circuit in the capacitive input as well as the open circuit in the inductive

output must be avoided.

$$\sum_{K=A,B,C} S_{Ka}(t) = \sum_{K=A,B,C} S_{Kb}(t) = \sum_{K=A,B,C} S_{Kc}(t) = 1 \tag{2.7}$$

For the following analysis, it is assumed that Equation 2.7 is obeyed and, because ideal switches are used, the commutation between switches is instantaneous.

A typical switching pattern for Matrix Converter is shown in Figure 2.3. If conventional PWM is employed the switching sequence T_{seq} has a fixed period.

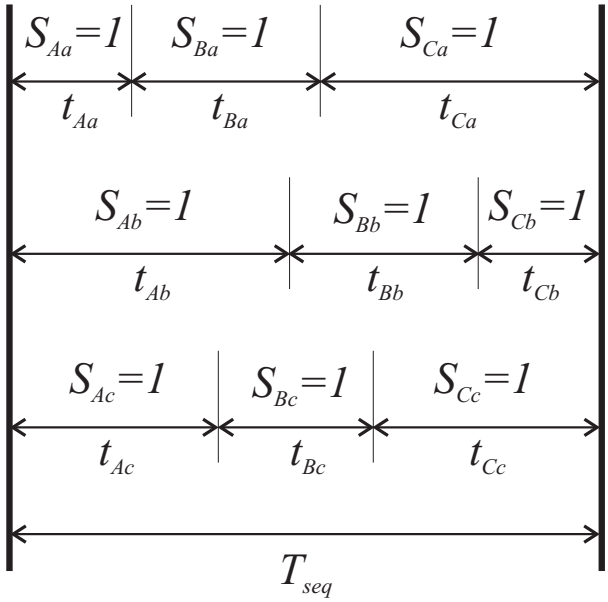


Figure 2.3: General form of switching pattern.

A modulation duty cycle should be defined for each switch in order to determine the average behavior of the Matrix Converter output voltage waveform. The modulation duty cycle is defined by,

$$m_{Aa}(t) = \frac{t_{Aa}}{T_{seq}} \tag{2.8}$$

where t_{Aa} represents the time when switch Aa is ON and T_{seq} represents the time of the complete sequence in the PWM pattern.

The modulation strategies are defined by using these continuous time functions. Equation 2.9 shows the use of these functions for the three-phase Matrix Converter.

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} m_{Aa}(t) & m_{Ba}(t) & m_{Ca}(t) \\ m_{Ab}(t) & m_{Bb}(t) & m_{Cb}(t) \\ m_{Ac}(t) & m_{Bc}(t) & m_{Cc}(t) \end{bmatrix} \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix}$$

$$\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} = \begin{bmatrix} m_{Aa}(t) & m_{Ab}(t) & m_{Ac}(t) \\ m_{Ba}(t) & m_{Ba}(t) & m_{Bc}(t) \\ m_{Ca}(t) & m_{Cb}(t) & m_{Cc}(t) \end{bmatrix} \begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} \tag{2.9}$$

Voltages v_a, v_b & v_c and currents i_a, i_b & i_c in Equation 2.9 are now values averaged over the sequence time. In Equation 2.10, which is a representation in a more compact notation of Equation 2.9, the matrix $M(t)$ is known as the ***modulation matrix***.

$$\begin{aligned} [v_o(t)] &= [M(t)][v_i(t)] \\ [i_i(t)] &= [M(t)]^T[i_o(t)] \end{aligned} \tag{2.10}$$

Using this nomenclature, the constraint equation for Matrix Converters can now be written as,

$$\sum_{K=A,B,C} m_{Ka}(t) \;=\; \sum_{K=A,B,C} m_{Kb}(t) \;=\; \sum_{K=A,B,C} m_{Kc}(t) = 1 \tag{2.11}$$

2.3.1 Basic Solution for the Modulation Problem

As stated in Section 2.2, the modulation problem assumes that a set of sinusoidal output voltages, $v_o(t)$, and input currents, $i_i(t)$, are required. These sets can be represented as,

$$[v_i(t)] = V_{im} \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t + \frac{2\pi}{3}) \\ \cos(\omega_i t + \frac{4\pi}{3}) \end{bmatrix} \tag{2.12}$$

$$[i_o(t)] = I_{om} \begin{bmatrix} \cos(\omega_o t + \phi_o) \\ \cos(\omega_o t + \phi_o + \frac{2\pi}{3}) \\ \cos(\omega_o t + \phi_o + \frac{4\pi}{3}) \end{bmatrix} \tag{2.13}$$

The aim is to find a modulation matrix, $M(t)$, such that Equations 2.14 and 2.15 are satisfied, as well as the constraint Equation 2.11.

$$[v_o(t)] = qV_{im} \begin{bmatrix} \cos(\omega_o t) \\ \cos(\omega_o t + \frac{2\pi}{3}) \\ \cos(\omega_o t + \frac{4\pi}{3}) \end{bmatrix} \tag{2.14}$$

$$[i_i(t)] = q\frac{\cos\phi_o}{\cos\phi_i} I_{om} \begin{bmatrix} \cos(\omega_i t + \phi_i) \\ \cos(\omega_i t + \phi_i + \frac{2\pi}{3}) \\ \cos(\omega_i t + \phi_i + \frac{4\pi}{3}) \end{bmatrix} \tag{2.15}$$

In Equations 2.14 and 2.15 q is the voltage transfer ratio, ω_i and ω_o are the input and output frequencies and ϕ_i and ϕ_o are the input and output phase displacement angles respectively. The problem was treated by Venturini, who found two solutions [28]. The solutions are expressed in Equations 2.16 and 2.17.

$$[M1(t)] = \frac{1}{3} \begin{bmatrix} 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t - \frac{2\pi}{3}) & 1+2q\cos(\omega_m t - \frac{4\pi}{3}) \\ 1+2q\cos(\omega_m t - \frac{4\pi}{3}) & 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t - \frac{2\pi}{3}) \\ 1+2q\cos(\omega_m t - \frac{2\pi}{3}) & 1+2q\cos(\omega_m t - \frac{4\pi}{3}) & 1+2q\cos(\omega_m t) \end{bmatrix} \tag{2.16}$$

with $\omega_m = (\omega_o - \omega_i)$

$$[M2(t)] = \frac{1}{3} \begin{bmatrix} 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t - \frac{2\pi}{3}) & 1+2q\cos(\omega_m t - \frac{4\pi}{3}) \\ 1+2q\cos(\omega_m t - \frac{2\pi}{3}) & 1+2q\cos(\omega_m t - \frac{4\pi}{3}) & 1+2q\cos(\omega_m t) \\ 1+2q\cos(\omega_m t - \frac{4\pi}{3}) & 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t - \frac{2\pi}{3}) \end{bmatrix} \tag{2.17}$$

with $\omega_m = (\omega_o + \omega_i)$.

Considering the solution in Equation 2.16, the phase displacement at the input is the same as in the output because $\phi_i = \phi_o$ whereas the solution in Equation 2.17 yields $\phi_i = -\phi_o$ giving reversed phase displacement at the input. If both solutions are combined, the result provides the means for input displacement factor control,

$$[M(t)] = \alpha_1[M1(t)] + \alpha_2[M2(t)] \qquad \text{where } \alpha_1 + \alpha_2 = 1 \tag{2.18}$$

Regardless of the load displacement factor, if α_1 is set to be equal to α_2 ($\alpha_1 = \alpha_2$), the input displacement factor at the converter terminals is unity. Other possibilities exist, through the choice of α_1 and α_2, to have any combination of leading or lagging displacement factor at the input with a lagging or leading power factor load at the output.

If $\alpha_1 = \alpha_2$ is used, the modulation functions can be expressed in a compact equation:

$$m_{Kj} = \frac{t_{Kj}}{T_{seq}} = \frac{1}{3}\left(1 + \frac{2v_K V_j}{V_{im}^2}\right) \quad \text{for } K = A, B, C \text{ and } j = a, b, c \tag{2.19}$$

Where V_{im} is the average input voltage.

Considering Equation 2.19, which represents the basic method, the average output voltages (taken over the switching sequence) are equal to the target output voltages $[v_o(t)]$ during each switching sequence. This is only possible if the target output voltages must fit within the input voltage envelope for all operating conditions. Using this solution the maximum value of input to output voltage ratio, q, that the converter can achieve is 50%, as shown in Figure 2.4. The modulation algorithm represented by Equation 2.19 is suitable for real time implementation but in practice it is not used due to the 50% voltage transfer ratio limitation.

2.3.2 Venturini's Optimum Method

The method described in previous section can be improved. This improvement can be achieved by modifying the target output voltage matrix $V_o(t)$ to include third harmonics of the input and output frequencies. This new strategy is known as Venturini's optimum method and employs the common-mode addition technique defined in [48]. The target output voltages in Equation 2.14 are modified in order to include the third harmonics. The maximum theoretical output to input voltage ratio, q, can be increased up to 86%, as shown in Equation 2.20. The complete use of the input voltage envelope is employed by the target output voltages as shown in Figure 2.5. The voltage transfer ratio may be defined as the output fundamental to

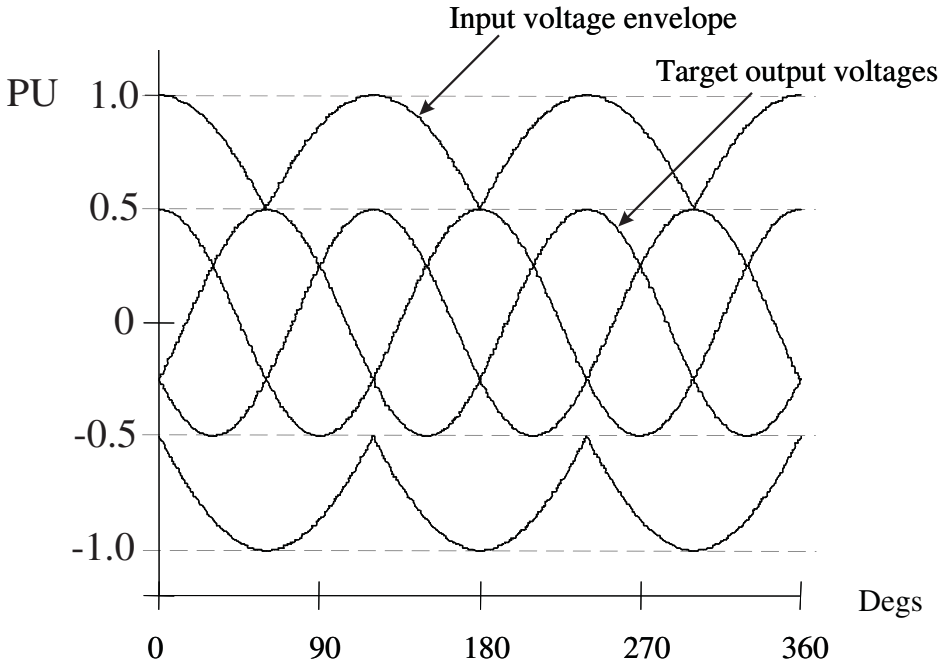


Figure 2.4: Theoretical waveforms illustrating the 50% voltage ratio limit.

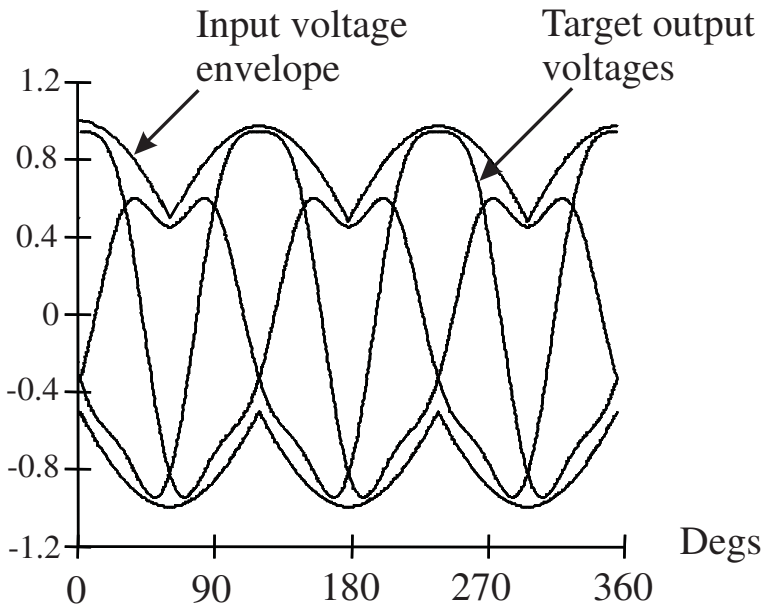


Figure 2.5: Theoretical waveforms illustrating the third harmonic addition to obtain the 86% optimum voltage ratio limit. This is a rms value to rms value ratio.

the input fundamental ratio and its maximum value is 0.866.

$$[v_o(t)] = qV_{im} \begin{bmatrix} \cos(\omega_o t) - \frac{1}{6}\cos(3\omega_o t) + \frac{1}{2\sqrt{3}}\cos(3\omega_i t) \\ \cos(\omega_o t + \frac{2\pi}{3}) - \frac{1}{6}\cos(3\omega_o t) + \frac{1}{2\sqrt{3}}\cos(3\omega_i t) \\ \cos(\omega_o t + \frac{4\pi}{3}) - \frac{1}{6}\cos(3\omega_o t) + \frac{1}{2\sqrt{3}}\cos(3\omega_i t) \end{bmatrix} \tag{2.20}$$

Note that triple harmonics in the input frequency as well as in the output frequency are added. According to [8], when unity displacement factor is required the Equation 2.19 becomes,

$$m_{Kj} = \frac{1}{3}[1 + \frac{2v_k V_j}{V_{im}^2} + \frac{4q}{3\sqrt{3}}\sin(\omega_i t + \beta_K)\sin(3\omega_i t)] \tag{2.21}$$

for K=A,B,C and j=a,b,c

$\beta_K = 0, \frac{2\pi}{3}, \frac{4\pi}{3}$

for K=A,B,C respectively.

This implementation is readily handled by modern microprocessors up to switching frequencies of tens of kHz. Input displacement factor control can be introduced into the formulation in Equation 2.20 by inserting a phase shift between the actual input voltages and the input voltages, v_K. If the input displacement factor is different from unity, the output voltage limit will be reduced from $0.86V_{im}$(86% of the input voltage value) to a small value, which depends on the displacement factor achieved in the input. Therefore, the value of the output voltage must be lower than 86% of the input voltage.

2.3.3 Scalar Method

In 1987 G. Roy proposed a scalar control algorithm for [29]. The modulation duty cycle for this method is given by

$$\begin{aligned} m_{Lj} &= \frac{(v_j - v_M)v_L}{1.5V_i m^2} \\ m_{Kj} &= \frac{(v_j - v_M)v_K}{1.5V_i m^2} \\ m_{Mj} &= 1 - (m_{Lj} + m_{Kj}) \quad \text{for } j = a, b, c \quad \text{respectively} \end{aligned} \tag{2.22}$$

Here, the subscript M is assigned to the input voltage which has a different polarity to the other two inputs and the subscript L is assigned to to the smallest of the other two input voltage magnitudes. The third input voltage is assigned subscript K. As in the previous method, the common-mode addition is used in order to modify the target output voltages, v_j. This modification (by adding the third harmonics) is employed to achieve 86% voltage ratio capability. Although some differences can be observed, this method yields virtually identical switch timings to Venturini's optimum method. Using a similar expression to Equation 2.21, the modulation duty cycles for the scalar method can be represented by Equation 2.23.

$$m_{Kj} = \frac{t_{Kj}}{T_{seq}} = \frac{1}{3}[1 + \frac{2v_k V_j}{V_{im}^2} + \frac{2}{3}\sin(\omega_i t + \beta_K)\sin(3\omega_i t)] \tag{2.23}$$

for K=A,B,C and j=a,b,c

$\beta_K = 0, \frac{2\pi}{3}, \frac{4\pi}{3}$

for K=A,B,C respectively.

Equations 2.21 and 2.23 are equal when the output voltage is maximum ($q = \frac{\sqrt{3}}{2}$). The only difference between the methods is that the right most term is used in conjunction with q in the Venturini method and is fixed at its maximum value in the scalar method. The effect on output voltage is negligible except at low switching frequencies, where the Venturini method is superior.

2.3.4 Space Vector Modulation (SVM) Method

The concept of a "Space Phasor" is very important in the analysis of the space vector modulation method (SVM). This method is well known in conventional PWM inverters. The "Space Phasor" was originally a method used for representing and analyzing three-phase machines. This method of analysis is particularly popular with researchers in the area of vector control. It allows the visualization of the spatial and time relationships between the resultant current and flux vectors in various reference frames.

2.3.4.1 Space Vectors

Matrix Converter operation can be explained in more general terms using a space vector approach. For operation of the Matrix Converter one and only one switch in each output phase must be conducting. This leads to twenty seven possible switching combinations for the Matrix Converter. By applying Equations 2.25 and 2.26 to determine the output voltage and input current vectors respectively, the magnitude and phase of these vectors for all possible combinations are given in Table 2.1. The shorthand notation for the converter states gives the input phases connected to output phases 1,2 and 3 in the first, second and third subscript respectively. α_o is the angle of the output voltage vector and β_i is the angle of the input current vector.

$$\overrightarrow{\mathbf{v}}_o(t) = (qV_{im}\sqrt{3})\cos(\omega_o t) \tag{2.24}$$

$$\overrightarrow{\mathbf{v}}_o(t) = \frac{2}{3}(v_{1o} + av_{2o} + a^2 v_{3o}) \tag{2.25}$$

$$\overrightarrow{\mathbf{i}}_o(t) = \frac{2}{3}(i_{1i} + ai_{2i} + a^2 i_{3i}) \tag{2.26}$$

Where

v_{1o}, v_{2o}, v_{3o} are output phase voltages

i_{1i}, i_{2i}, i_{3i} are input line currents

$a \equiv e^{j\frac{2\pi}{3}}$

The vector $\overrightarrow{\mathbf{v}}_o(t)$ has a constant length of $(qV_{im}\sqrt{3})$ and it is rotating at frequency ω_o. The basis of the space vector modulation technique is that the possible output voltages for the converter can be expressed in the same form as Equation 2.25. At each sampling instant, the position of $\overrightarrow{\mathbf{v}}_o(t)$ is compared with the possible vectors and the desired output voltage is synthesized by time averaging (within the switching interval) between adjacent vectors to give the correct mean voltage. For a conventional DC link inverter this process is very simple because there are only eight possible switching states ($2^3 = 8$; two possible states per output leg and three phases). The situation with a Matrix Converter is more complex as there are twenty seven possible switching states and the input voltages are time varying.

2.3.4.2 Matrix Converter Switching States

As mentioned previously, in a three-phase to three-phase Matrix Converter there are twenty seven possible switching states. These switching states and the resulting output voltages are tabulated in Table 2.1. Analyzing this table, the output voltage states may be categorized in three groups:

Group I . 18 combinations where the output voltage and the input current vectors have fixed directions with magnitudes that vary with the input voltage phase angle and the output current phase angle respectively. These combinations result when any two output phases are connected to the same input phase.

Group II 3 combinations giving null output voltage and input current vectors. All three output phases are connected to the same input phase in these combinations.

Group III 6 combinations in which each output phase is connected to a different input phase. Both magnitude and phase of the resultant vectors are variable in these cases.

Switching Configuration	Converter State	v_o	α_o	i_i	β_i
$+1$	S_{122}	$\frac{2}{3}v_{12i}$	0	$\frac{2}{\sqrt{3}}i_{1o}$	$-\frac{\pi}{6}$
-1	S_{211}	$-\frac{2}{3}v_{12i}$	0	$-\frac{2}{\sqrt{3}}i_{1o}$	$-\frac{\pi}{6}$
$+2$	S_{233}	$\frac{2}{3}v_{23i}$	0	$\frac{2}{\sqrt{3}}i_{1o}$	$\frac{\pi}{2}$
-2	S_{322}	$-\frac{2}{3}v_{23i}$	0	$-\frac{2}{\sqrt{3}}i_{1o}$	$\frac{\pi}{2}$
$+3$	S_{311}	$\frac{2}{3}v_{31i}$	0	$\frac{2}{\sqrt{3}}i_{1o}$	$\frac{7\pi}{6}$
-3	S_{133}	$-\frac{2}{3}v_{31i}$	0	$-\frac{2}{\sqrt{3}}i_{1o}$	$\frac{7\pi}{6}$
$+4$	S_{212}	$\frac{2}{3}v_{12i}$	$\frac{2\pi}{3}$	$\frac{2}{\sqrt{3}}i_{2o}$	$-\frac{\pi}{6}$
-4	S_{121}	$-\frac{2}{3}v_{12i}$	$\frac{2\pi}{3}$	$-\frac{2}{\sqrt{3}}i_{2o}$	$-\frac{\pi}{6}$
$+5$	S_{323}	$\frac{2}{3}v_{23i}$	$\frac{2\pi}{3}$	$\frac{2}{\sqrt{3}}i_{2o}$	$\frac{\pi}{2}$
-5	S_{232}	$-\frac{2}{3}v_{23i}$	$\frac{2\pi}{3}$	$-\frac{2}{\sqrt{3}}i_{2o}$	$\frac{\pi}{2}$
$+6$	S_{131}	$\frac{2}{3}v_{31i}$	$\frac{2\pi}{3}$	$\frac{2}{\sqrt{3}}i_{2o}$	$\frac{7\pi}{6}$
-6	S_{313}	$-\frac{2}{3}v_{31i}$	$\frac{2\pi}{3}$	$-\frac{2}{\sqrt{3}}i_{2o}$	$\frac{7\pi}{6}$
$+7$	S_{221}	$\frac{2}{3}v_{12i}$	$\frac{4\pi}{3}$	$\frac{2}{\sqrt{3}}i_{3o}$	$-\frac{\pi}{6}$
-7	S_{112}	$-\frac{2}{3}v_{12i}$	$\frac{4\pi}{3}$	$-\frac{2}{\sqrt{3}}i_{3o}$	$-\frac{\pi}{6}$
$+8$	S_{332}	$\frac{2}{3}v_{23i}$	$\frac{4\pi}{3}$	$\frac{2}{\sqrt{3}}i_{3o}$	$\frac{\pi}{2}$
-8	S_{223}	$-\frac{2}{3}v_{23i}$	$\frac{4\pi}{3}$	$-\frac{2}{\sqrt{3}}i_{3o}$	$\frac{\pi}{2}$
$+9$	S_{113}	$\frac{2}{3}v_{31i}$	$\frac{4\pi}{3}$	$\frac{2}{\sqrt{3}}i_{3o}$	$\frac{7\pi}{6}$
-9	S_{331}	$-\frac{2}{3}v_{31i}$	$\frac{4\pi}{3}$	$-\frac{2}{\sqrt{3}}i_{3o}$	$\frac{7\pi}{6}$
0_1	S_{111}	0	$-$	0	0
0_2	S_{222}	0	$-$	0	0
0_3	S_{333}	0	$-$	0	0
$FR1$	S_{123}	*variable*	*variable*	*variable*	*variable*
$FR2$	S_{231}	*variable*	*variable*	*variable*	*variable*
$FR3$	S_{312}	*variable*	*variable*	*variable*	*variable*
$BR1$	S_{132}	*variable*	*variable*	*variable*	*variable*
$BR2$	S_{213}	*variable*	*variable*	*variable*	*variable*
$BR3$	S_{321}	*variable*	*variable*	*variable*	*variable*

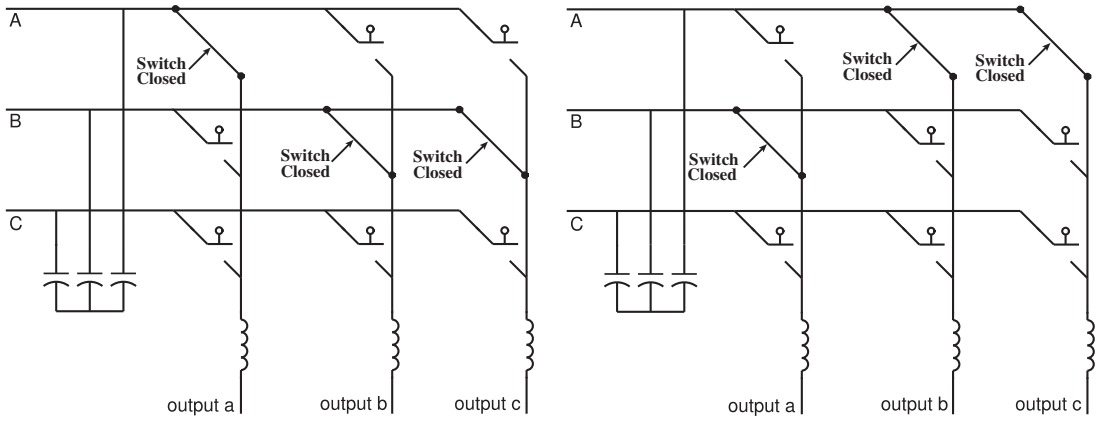
Table 2.1: Switching States for a three-phase to three-phase Matrix Converter [1].

Group I vectors are split into three sub-groups as shown in Table 2.1. The six states in each sub-group produce a space phasor in a defined direction. For the three sub-groups the directions are displaced by 120°. The amplitude and polarity of the space phasor along the defined direction depends on which of the line to line voltages is used. The rotating vectors of Group III are not used.

The first column in table 2.1 represents the 27 possible switching configurations of the converter. States of the converter for the two first switching configurations are shown in Figure 2.6. Switching configuration +1 indicates that the state of the converter is S_{122}. The position of suffixes 122 indicates the a, b and c output phases respectively. The first position is for the output phase a. The second position is for the output phase b. The third position is for the output phase c. The values 1, 2 and 3 indicate the input phase A, B and C respectively. For example, S_{122} means that in output phase a the switch in the input phase A is closed, in the output phase b the switch in the input B is closed and in the output phase c the switch in the input B is closed. This can be seen in Figure 2.6(a). The switching configuration -1 (converter state S_{211}) is shown in Figure 2.6(b). In this case, switch in output phase a and input phase B is closed, switch in output phase b and input phase A is closed and switch in output phase c and input phase A is also closed.

2.3.4.3 Selection of Switching States

The space vector modulation strategy presented in [1], makes use of the eighteen fixed-directions and three null vector combinations to achieve the desired output voltage vector and input current direction. Figure 2.7 shows the output line-to-neutral voltage vector and input line current vector directions generated by the 18 fixed-direction configurations, a complete description of which is included in [1]. K_V denotes the sector containing the output voltage vector and K_I denotes the sector containing the input current vector. From this figure it can be noted that for any combination of output voltage and input current sectors, four configurations can be identified that produce output voltage vectors and input current vectors lying adjacent to the desired



(a) Converter State S_{122} (b) Converter State S_{211}

Figure 2.6: States of the converter for switching configuration +1 and -1.

vectors. The switching configurations used for any output voltage sector (KV) and input current sector (K_I) are given in Table 2.2 and Table 2.3.

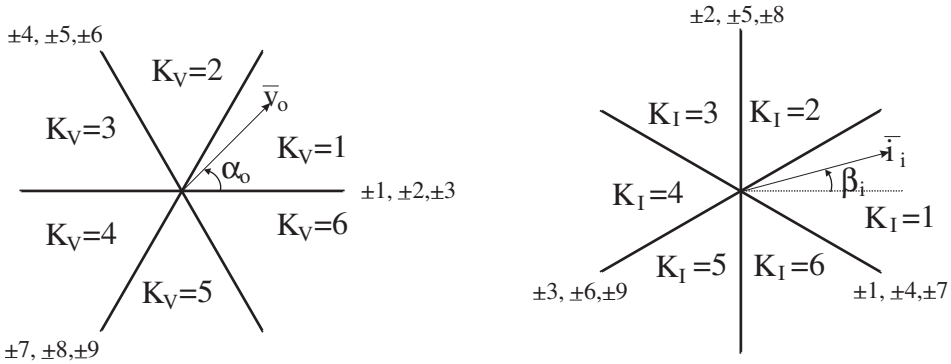


Figure 2.7: Synthesis of output voltage and input current space phasor.

It can be shown [1] that the required modulation duty cycles for the switching configurations I, II, III a,d IV are given by Equations 2.27 - 2.30:

$$\delta^I = \frac{2}{\sqrt{3}} \cdot q \cdot \frac{\cos\left(\widetilde{\alpha}_o - \frac{\pi}{3}\right) cos(\widetilde{\beta}_i - \frac{\pi}{3})}{\cos\phi_i} \tag{2.27}$$

K_I		K_V											
	Sector	1				2				3			
	1	+9	-7	-3	+1	-6	+4	+9	-7	+3	-1	-6	+4
	2	-8	+9	+2	-3	+5	-6	-8	+9	-2	+3	+5	-6
	3	+7	-8	-1	+2	-4	+5	+7	-8	+1	-2	-4	+5
	4	-9	+7	+3	-1	+6	-4	-9	+7	-3	+1	+6	-4
	5	+8	-9	-2	+3	-5	+6	+8	-9	+2	-3	-5	+6
	6	-7	+8	+1	-2	+4	-5	-7	+8	-1	+2	+4	-5
		I	II	III	IV	I	II	III	IV	I	II	III	IV

Table 2.2: Selection of switching configurations for each combination of K_V and K_I [1].

K_I		K_V											
	Sector	4				5				6			
	1	-9	+7	+3	-1	+6	-4	-9	+7	-3	+1	+6	-4
	2	+8	-9	-2	+3	-5	+6	+8	-9	+2	-3	-5	+6
	3	-7	+8	+1	-2	+4	-5	-7	+8	-1	+2	+4	-5
	4	+9	-7	-3	+1	-6	+4	+9	-7	+3	-1	-6	+4
	5	-8	+9	+2	-3	+5	-6	-8	+9	-2	+3	+5	-6
	6	+7	-8	-1	+2	-4	+5	+7	-8	+1	-2	-4	+5
		I	II	III	IV	I	II	III	IV	I	II	II	IV

Table 2.3: Selection of switching configurations for each combination of K_V and K_I (continuation) [1].

$$\delta^{II} = \frac{2}{\sqrt{3}} \cdot q \cdot \frac{\cos(\widetilde{\alpha}_o - \frac{\pi}{3}) cos(\widetilde{\beta}_i + \frac{\pi}{3})}{\cos\phi_i} \tag{2.28}$$

$$\delta^{III} = \frac{2}{\sqrt{3}} \cdot q \cdot \frac{\cos(\widetilde{\alpha}_o + \frac{\pi}{3}) cos(\widetilde{\beta}_i - \frac{\pi}{3})}{\cos\phi_i} \tag{2.29}$$

$$\delta^{IV} = \frac{2}{\sqrt{3}} \cdot q \cdot \frac{\cos(\widetilde{\alpha}_o + \frac{\pi}{3}) cos(\widetilde{\beta}_i + \frac{\pi}{3})}{\cos\phi_i} \tag{2.30}$$

Where $\widetilde{\alpha}_o$ and $\widetilde{\beta}_i$ are the angles of the output voltage and input current vectors measured from the bisecting line of the corresponding sectors. ϕ_i is the input phase displacement angle.

For unity input power factor operation and $q \leq \frac{\sqrt{3}}{2}$, Equation 2.31 applies:

$$\delta^I + \delta^{II} + \delta^{III} + \delta^{IV} \leq 1 \tag{2.31}$$

Then δ_0 is the total modulation duty cycle for the zero configuration(s) required to complete the modulation period:

$$\delta_0 = 1 - (\delta^I + \delta^{II} + \delta^{III} + \delta^{IV}) \tag{2.32}$$

If a double-side modulation pattern is used δ_0 is distributed in the modulation period by two equal parts. This is independent of the type of zero modulation configuration used. If a three-zero symmetrical configuration is used, δ_0 is distributed in the modulation period by six equal parts [49] [23] [50] [51].

2.4 Topologies of Bi-directional Switches

Bi-directional switches capable of blocking voltage and conducting current in both directions are required by the Matrix Converter. Unfortunately these devices are not widely available. Hence, discrete devices are used to construct suitable bi-directional switch cells and fulfil those requirements. The choice of bi-directional switches also dictates which current commutation methods can be used. This section describe some possible bi-directional switch configurations and the advantages and disadvantages of

each arrangement. In the discussion below it has been assumed that the switching device would be an IGBT, but other devices such as MOSFETs, MCTs and IGCTs can be used in the same way [52].

2.4.1 Diode Bridge Topology

The diode bridge arrangement is the most simple bi-directional switch structure. This arrangement consists of an IGBT at the center of a single phase diode bridge arrangement, as illustrated in Figure 2.8. The main advantage of this arrangement is that only one active device is need, reducing the cost of the power circuit and the complexity of the control/gate drive circuits. Conduction losses are relatively high since there are three devices in each conduction path. The main disadvantage is that the direction of the current through the switch cannot be controlled. Many of the advanced commutation techniques described later rely on independent control of the current in each direction.

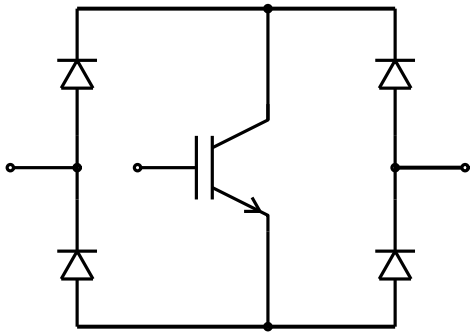


Figure 2.8: Diode bridge bi-directional switch

2.4.2 IGBT with Anti-parallel Diode Topologies

There are different configurations for bi-directional switches which use IGBTs with anti-parallel diodes. Such configurations are mentioned below.

- **Common Emitter Bi-directional Switch**. This switch arrangement consists of two diodes and two IGBTs connected in anti-parallel as shown in Figure 2.9. The diodes are included to provide the reverse blocking capability. The reverse blocking capability is a weak of the early IGBT technology [53] [54]. There are several advantages in using this arrangement when compared to the diode bridge switch. The first advantage is that it is possible to independency control the direction of the current. Conduction losses are also reduced as only two devices carry the current at any one time. As with the diode bridge switch each bi-directional switch cell requires an isolated power supply.

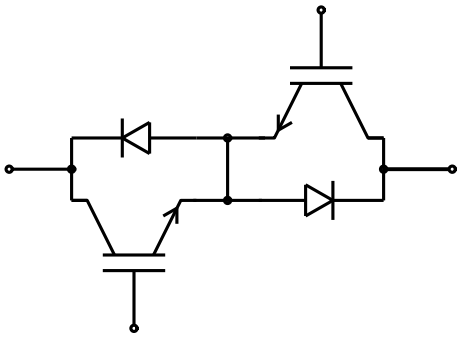


Figure 2.9: Common emitter bi-directional switch

- **Common Collector Bi-directional Switch**. This arrangement is similar to the arrangement presented in the previous configuration. The difference is that the IGBTs are arranged in a common collector configuration as shown in Figure 2.10. The conduction losses are the same as the common emitter configuration. One possible advantage of the common collector configuration is that only six isolated power supplies are required to supply the gate drive signals. This is possible if the inductances between the devices sharing the same isolated power supply is low. This is the case for Matrix Converter modules where all bi-directional switches are integrated in one package [55]. However, as the power levels increase, the stray inductance of the individual bi-directional switches becomes more important. Therefore at higher power converters it is desirable to package the IGBTs into individual bi-directional switches or complete output

legs. Hence the common emitter configuration is usually preferred for higher power levels [56].

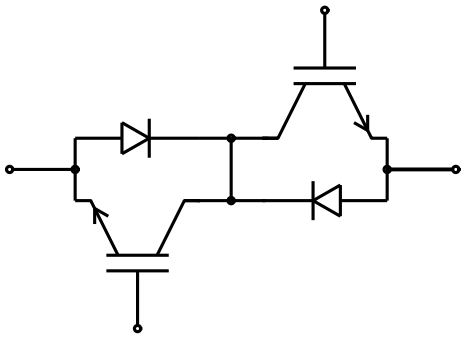
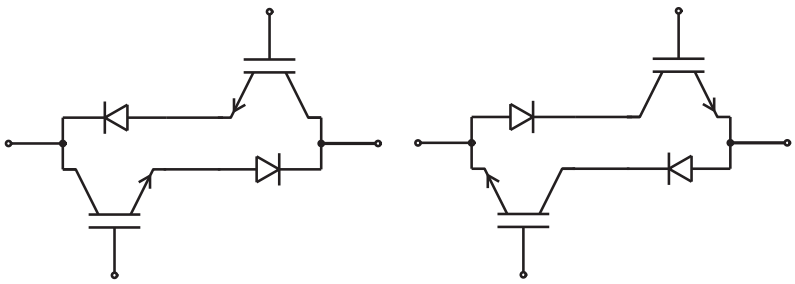


Figure 2.10: Common collector bi-directional switch

- **Series IGBT Diode Configurations**. Both the common emitter and the common collector configurations can be used without the central connection as shown in Figure 2.11. In the case of common emitter configuration, this will remove the advantage of being able to drive the two IGBTs from the same isolated power supply.



(a) Common emitter (b) Common collector

Figure 2.11: Back to back devices without central connection

- **Anti-parallel Reverse Blocking IGBTs**. If the switching devices used for the bi-directional switch have a reverse voltage blocking capability then it is

possible to build the bi-directional switches by simply placing two devices in anti-parallel as shown in Figure 2.12 [57] [58] [59]. This arrangement leads to a very compact converter with the potential for substantial improvements in efficiency. However, to date reverse blocking IGBTs have shown poor reverse recovery characteristics which decreases the efficiency by increasing the switching losses and has prevented widespread use of this configuration.

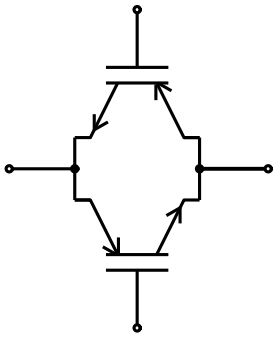
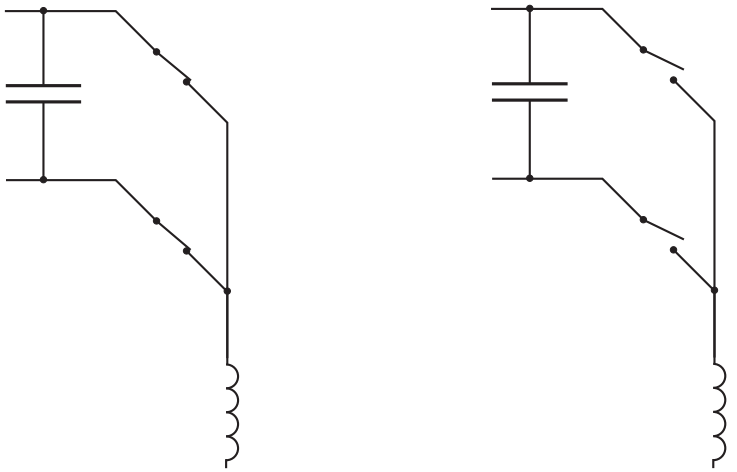


Figure 2.12: Reverse blocking IGBT bi-directional switch

2.5 Matrix Converter Commutation Methods

Reliable current commutation between switches in Matrix Converters is more difficult to achieve than a conventional voltage source inverters (VSI) since there are no natural freewheeling paths. The commutation has to be actively controlled at all times and must respect to two basic rules. This can be visualized by considering just two switches on one output phase of a Matrix Converter. It is important that no two bi-directional switches are switched on at any one time, as shown in Figure 2.13(a). This would result in line-to-line short circuits and the destruction of the Matrix Converter due to overcurrent. Also, the bi-directional switches for each output phase should not all be turned off at any point in time as shown in Figure 2.13(b). This would result in the absence of a path for the inductive load current causing large over-voltages. These two considerations cause a conflict as semiconductor devices cannot be switched

instantaneously due to propagation delays and finite switching times.



(a) Short circuit of capacitive input (b) Open circuit of inductive load

Figure 2.13: These conditions must be avoided for safe operation.

2.5.1 Simple Commutation Methods

2.5.1.1 Deadtime Commutation Method

The deadtime method is commonly used in inverter systems. The load current free-wheels through the anti-parallel diodes during the deadtime period. In the case of a Matrix Converter using deadtime commutation will cause an open circuit of the load (Figure 2.13(b)). This will result in large voltage spikes across the switches which would destroy the Matrix Converter unless snubbers or clamping devices are used to provide a path for the load current during the deadtime period [60, 61]. This method is undesirable since the energy in the snubber circuit is lost during every commutation. In addition to this disadvantage the bi-directional nature of the Matrix Converter circuit further complicates the snubber design.

2.5.1.2 Overlap Commutation Method

This method also breaks the rules of Matrix Converter current commutation and needs extra circuitry to avoid destruction of the Matrix Converter. In overlap current commutation, the incoming switch is turned on before the outgoing switch is turned off. This will cause a line-to-line short circuit (Figure 2.13(a)) during the overlap period unless extra line inductance is added to slow the rise of the current [62]. This is not a desirable method since the inductors are in the main conduction path therefore the conduction losses would be increased. in addition to this disadvantage there will be significant distortion of the output voltage waveform during the overlap period. The switching time for each commutation is increased and will vary with commutation voltage which may cause control problems.

One possible advantage of these simple commutation methods is that the diode bridge bi-directional switch arrangement as described in Section 2.4.1 may be used. However, this advantage is outweighed by the problems discussed above. For these reasons the advanced commutation methods described in next section are now preferred in all Matrix Converters.

2.5.2 Advanced Commutation Methods

The four-step commutation strategy is one of the methods that meet the rules of the Matrix Converter. This strategy can be implemented in a Matrix Converter, to do this the direction of the current in each bi-directional switch must be controlled.

2.5.2.1 The Current Direction Based Commutation Method

Figure 2.14 shows a schematic of a two phase to single phase Matrix Converter. In steady state both of the devices in the active bi-directional switch are gated to allow both directions of current flow. The following explanation assumes that the load

current is in the direction shown and the upper bi-directional switch (S_A) is closed. When a commutation to S_B is required, the current direction is used to determine which device in the active switch is not conducting. This device is then turned off, in this case $Q2$ is turned off. The device that will conduct the current in the incoming switch is then gated, $Q3$ in this example. The load current transfers to the incoming device either at this point or when the outgoing device ($Q1$) is turned off, depending on the polarity of the input voltages. The remaining device in the incoming switch ($Q4$) is turned on to allow current reversals. This process is shown as a timing diagram in Figure 2.15. The delay added between each switching event is determined by the device characteristics. An open circuit in the load current will result if a mistake is made as to the current direction either due to circuit failure or due to the uncertainty at low currents. This can be a problem if no protection strategy is employed.

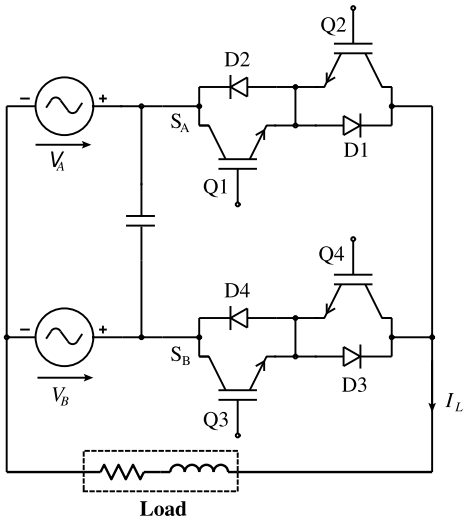


Figure 2.14: Two-phase to single-phase converter.

A variation on the four-step current commutation concept is to only gate the conducting device, which creates a two-step current commutation strategy as shown in Figure 2.16. This is done to reduce commutation times and hence reduce the minimum pulse width. This is desirable because the minimum pulse width often dictates the maximum voltage transfer ratio of the converter [46].

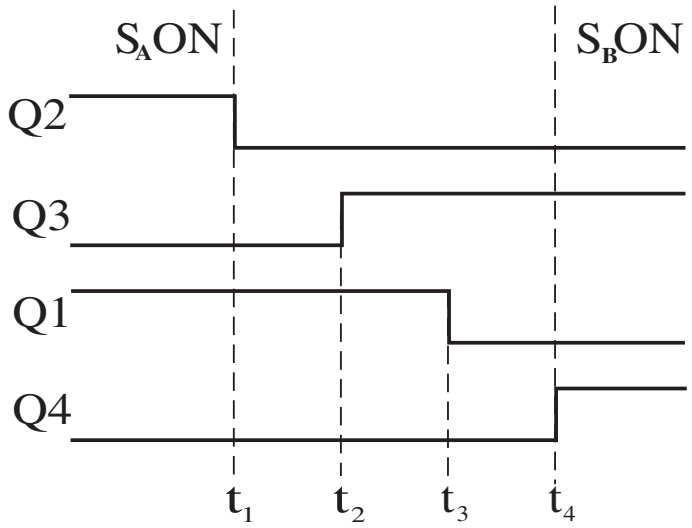


Figure 2.15: Timing diagram for four-step current commutation between two switches.

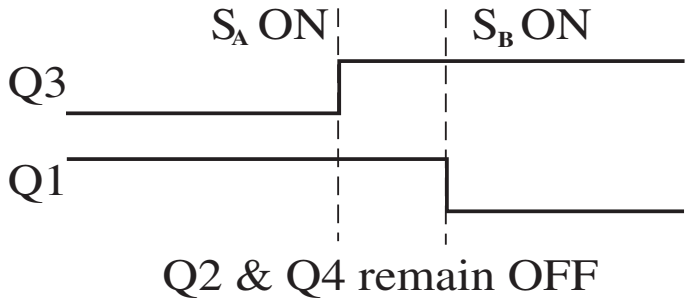


Figure 2.16: Timing diagram for two-step current commutation between two switches.

All the current commutation techniques included in this category need to know the output phase current direction. This current direction can be difficult to determine, especially in high power drives when the levels of current are low. To solve this problem, a new technique has been developed [63]. This technique uses the voltage across the bi-directional switch to determine the current direction. It is based on an intelligent gate drive circuit, which is used to control the firing of the IGBTs and detect the current direction, which flows within the bi-directional switch cell. A FPGA driver is employed to obtain the current direction information and then this information is transmitted to all the other gate drivers located in the same output phase. This action assures that all gate drivers are being considered to operate a safe commutation. As all the two-step commutation technique, considering this method, the performance obtained is very poor and the output waveform presents distortion when the current in the load is low. This problem is easily overcome by using the four-step method because the commutation is completed by the the final step of turning on the non-conducting device.

2.5.2.2 The Voltage Magnitude Based Commutation Method

This advanced commutation strategy uses the input voltage magnitude to determine the switch sequence for each commutation [64]. Referring to Figure 2.14 consider a commutation from S_A to S_B if $V_A > V_B$, $Q3$ can be turned on because $D3$ is reverse biased. If the current is in the direction shown it will commutate to $Q3$ when $Q1$ is turned off, otherwise the commutation will take place when $Q4$ is turned on. The reverse biased device ($Q4$) can then be turned off completing the commutation. Contrary to the previous commutation technique, when a mistake in sensing the input voltage direction occurred the wrong calculated commutation sequence would provoke a line-to-line short circuit of the supply. In this case, it very difficult to protect the supply as well the Matrix Converter system.

The method discussed in [65], which is the two-step variant of the voltage magnitude based commutation, is different in that only the devices needed to prevent shoot-

through are turned off. The implementation of this method requires a very accurate measurement of the input voltage. When implementing this method, some problems are presented at the zero crossing points of the line-to-line voltage; these problems are found when any inaccuracy in the measurement of the input voltage is presented and it will cause the commutation sequence be wrong. The same authors presented an improved method [66], which provides a path for the current during the zero crossing point of the line to line voltage. This is a partial solution because commutation between certain phases is inhibited. The critical and uncritical areas of commutation are shown in Figure 2.17.

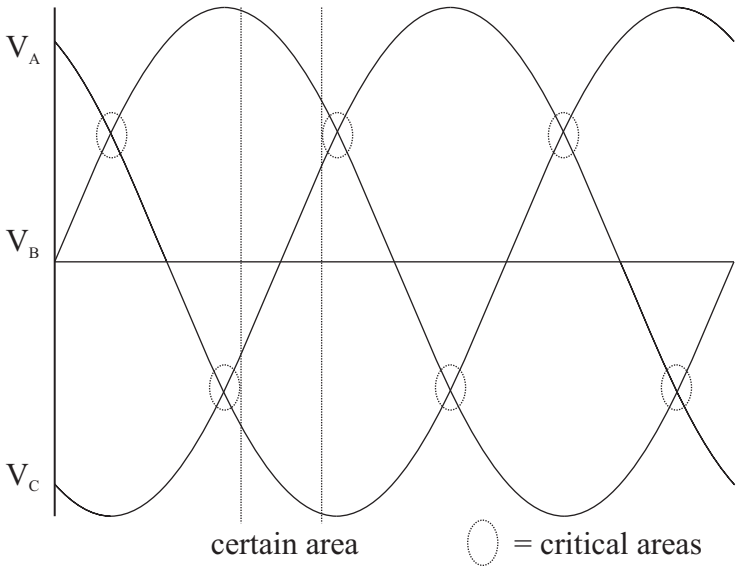


Figure 2.17: Critical areas of commutation sequence selection.

A technique to avoid critical situations of commutation, such as when two voltages of the input phases become equal, is discussed in [67]. This technique is based on the concept of replacing the critical commutation sequence with two uncritical sequences which will commutate to the remaining third input phase and then to the desired destination phase. Figure 2.18 explains the proposed sequence replacement.

The method proposed is effective and implemented easily, but disadvantages appear in the commutation logic when extra sequences are inserted.

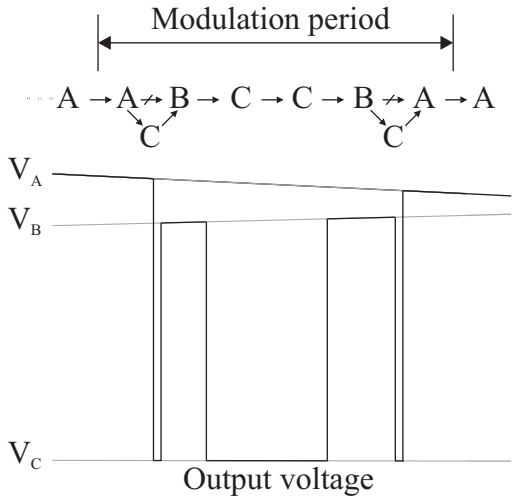


Figure 2.18: Critical areas between phase A and B - Two additional sequences to phase C are inserted in the modulation period.

These extra sequences increase the converter switching losses.

2.5.2.3 The Voltage Magnitude and Current Direction Method

Both the current direction detection and the input voltage magnitude measurement techniques are put together to propose a new method [68]. The main idea is to turn on all the devices that will conduct in the same direction as the load current. Commutation between the three-phases can be achieved by turning off one or two of the devices simultaneously depending on the required switching state and the relative magnitude of the input voltages. This is a one-step commutation method as there is no need for staggered switch sequencing.

This method takes the advantages and disadvantages of both of the current direction detection and the input voltage magnitude measurement techniques. Basically, the disadvantages shown are:

- The input current distortion generated by the commutation to the wrong input

phase due to the inaccurate measurements of the input voltage at zero crossing point of the line to line currents, and

- Reverse current, which cannot be conducted due to the lack of a path, which is absent because the device conducting in one direction is turned on. Distortion is presented in the output waveforms at the zero crossing point of current in the load [69].

2.6 Input Filter

Power electronics circuits switch on and off large amounts of current at high voltages and thus can generate unwanted electrical signals that affect other electronic systems. In practice, the magnitudes of the higher-order harmonics can also be significantly affected by the current spikes caused by the finite slopes of the switching transitions [70]. In consequence, it is always required that a filter be added at the power input of a power converter. By attenuating the switching harmonics that are presented in the converter input current waveform, the input filter allows compliance with regulation that limit conducted electromagnetic interference. The input filter can also protect the converter and its load from transients that appear in the input voltage, thereby improving the system reliability.

As mentioned previously, to reduce the input current ripple with minimum dissipated energy on the reactive elements, it is necessary to add an input filter to the power converter. An LC low-pass filter is added to the input of converter. The use of more complex topologies has been recommend in the literature in order to achieve higher attenuation at the switching frequency, but they are not practical. The LC filter attenuates the currents harmonics produced by the switching frequency in the power converter, and thereby smooths the current waveform drawn from the power source.

The design of the input filter has to accomplish the following [15]:

- Produce an input filter with a cut-off frequency lower that the switching frequency,

$$L_{in} \cdot C_{in} = \frac{1}{\omega_0^2} \tag{2.33}$$

  Where L_{in}, C_{in} are the values of the inductor and the capacitor of the input filter and $\omega_0 = 2\pi f_0$ is the resonance frequency pulsation of the input filter.

- Maximize the displacement angle ψ_{min-in} for a given output power.

- Minimize the input filter volume or weight for a given reactive power, by taking into account the energy densities which are different for film capacitors than for iron chokes.

- Minimize the voltage drop on the filter inductance at the rated current in order to provide the highest voltage transfer ratio.

Usually, the cut-off frequency of the LC input filter ω_0 is chosen to provide a given attenuation at the switching frequency. In addition, the value of the capacitor or inductance is chosen based on one of the previous criteria.

To improve the reliability of the system, input filters are sometimes required to operate normally when transients or periodic disturbances are applied to the power input. Such conducted susceptibility specifications force to damp the input filter resonances, so that input disturbances do not produce excessive current or voltages within the filter or power converter. It has been established both by analysis and practical tests that in Matrix Converter application it is advisable to incorporate damping in the filter, in the form of resistors in parallel with the inductors, since there is a high probability that at some operating point the matrix converter input currents will contain a component close to the resonant frequency of the filter [71], [72].

Figure 2.19 shows the LC input filter with the damping resistor added. The internal resistance of the inductor is represented by r. Using this schematic diagram, the transfer function of the input filter can be calculated [14], [10]. This transfer function is used to determine the resonance and cut-off frequency of the input filter. Bode plots are employed to find graphically the resonance and cut-off frequencies.

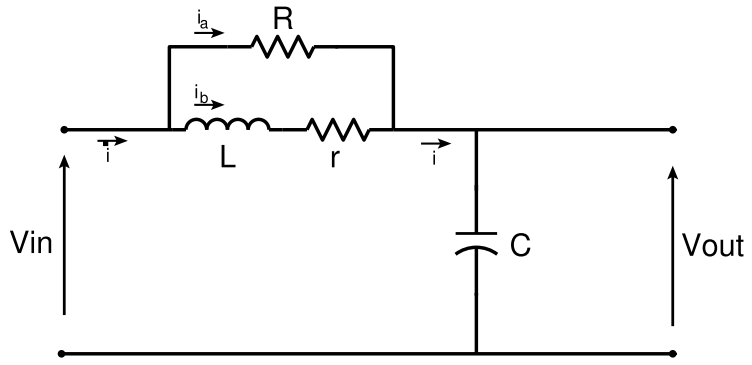


Figure 2.19: Diagram to calculate transfer function of input filter.

The transfer function is defined as the relation between the output to the input, i.e.

$$TF = \frac{V_{out}}{V_{in}} \tag{2.34}$$

Substituting the input and output voltage expression for each of the circuit components,

$$V_{out} = V_C = \frac{1}{C}\int idt = \frac{1}{C}\int (i_a + i_b)dt \tag{2.35}$$

$$V_{in} = L\frac{di_b}{dt} + ri_b + \frac{1}{C}\int idt = L\frac{di_b}{dt} + ri_b + \frac{1}{C}\int (i_a + i_b)dt \tag{2.36}$$

The relationship between i_a and i_b can be found as,

$$V_R = V_L + V_r; \quad Ri_a = L\frac{di_b}{dt} + ri_b \tag{2.37}$$

$$\Rightarrow \quad i_a = \frac{L}{R}\frac{di_b}{dt} + \frac{r}{R}i_b \tag{2.38}$$

Substituting Equation 2.38 into Equations 2.35 and Equation 2.36 and applying Laplace transform,

$$V_{out} = \frac{Ls + r + R}{RCs} \tag{2.39}$$

$$V_{in} = \frac{RLCs^2 + (rRC + L)s + (r + R)}{RCs} \tag{2.40}$$

Finally, the expression of the input filter transfer function is found as,

$$TF = \frac{\frac{Ls+r+R}{RLC}}{s^2 + (\frac{r}{L} + \frac{1}{RC})s + (\frac{r}{LRC} + \frac{1}{LC})} \tag{2.41}$$

Equation 2.41 expresses the general form of the input filter transfer function and is used to obtain the resonance and cut-off frequencies.

2.7 Output Filter

The power converter requires a LC filter at the output side to reduce the harmonics generated by the pulsating modulation of voltage waveform. A power converter with higher switching frequency will result in smaller LC filter size. However, switching frequency is generally limited in high power applications. For the design of the LC low-pass filter, the cut-off frequency is considered to be able to eliminate the most low order harmonics of the output voltage waveform [20]. The output impedance of the power converter must be keep close to zero to operate as an ideal voltage source. Ideal voltage source have no additional voltage distortion even though under the load variation or a nonlinear load. To satisfy this requirement the capacitance value should be maximized and the inductance value should be minimized at the selected cut-off frequency of the low-pass filter. When the value of the capacitor is increased the power rating of the matrix Converter is increased as well. This is due to the increment of the filter reactive power. The capacitor value is limited to some value and the value of the inductor is increased as much as the decrement of the capacitor value. It is difficult to obtain zero output impedance when the LC filter is used [73]. The gain and bandwidth of the voltage regulating loop can theoretically control the output impedance of the power converter [74]. The structure of the controller, the power converter switching frequency and the sampling frequency of the digital signal processor limit the response of the control system. Therefore, when the feedback controller of the power converter is designed the component values of the LC filter are modified.

The optimal output LC filter design has been carried out in many studies. Most of these studies are based on the cost function. This cost function is defined by the reac-

tive power rating of the filter components under the steady state condition [75], [76]. To minimize the reactive power in the inductor and the capacitor each value of L and C have to be determined. But, if the value of LC filter is selected to minimize the cost function, then it is common that the filter components are chosen from a set of small capacitance and large inductance values. As a consequence, the output impedance of the power converter is too high. The output voltage waveform of the power converter can be sinusoidal under the linear load or steady state condition if the values mentioned previously are used.

The distortion of the output voltage waveform can be mitigated with an additional voltage feedback controller. The performance of the controller is limited by the power converter switching frequency and the sampling frequency of the digital signal processor. The trial and error method is used to modified the filter design values to reduce the distortion of the output voltage waveform.

Figure 2.20 shows the schematic of the output filter. In this figure r represents the internal resistance of the inductor. The transfer function of the output filter can be calculated from this figure [14], [10]. The resonance and cut-off frequencies are determined according to the values of the capacitor and the inductor. Bode plots are employed to find such frequencies.

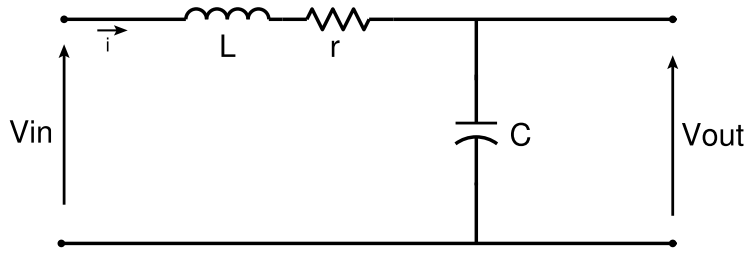


Figure 2.20: Diagram to calculate transfer function of output filter.

The transfer function is defined by Equation 2.42.

$$TF = \frac{V_{out}}{V_{in}} \tag{2.42}$$

The input voltage considered to calculated the transfer function is defined by Equation 2.43 and the output voltage by Equation 2.44.

$$V_{out} = V_C = \frac{1}{C}\int idt \tag{2.43}$$

$$V_{in} = L\frac{di}{dt} + ri + \frac{1}{C}\int idt \tag{2.44}$$

Applying Laplace transform to Equation 2.43 and Equation 2.44, the output and input voltage can be expressed as,

$$V_{out} = \frac{1}{Cs} \tag{2.45}$$

$$V_{in} = Ls + r + \frac{1}{Cs} \tag{2.46}$$

The general expression of the output filter transfer function is given by Equation 2.47

$$TF = \frac{\frac{1}{LC}}{s^2 + \frac{r}{L}s + \frac{1}{LC}} \tag{2.47}$$

2.8 Control

An AC-AC power electronic converter is essentially a device for creating a variable frequency output from an AC input supply. The frequency of the output voltage or current is readily established by simply switching. However, the variable frequency ability is nearly always accompanied by a corresponding need to adjust the amplitude of the fundamental component of the output waveform as the frequency changes, i.e. voltage control [77].

The use of reference frame theory can simplify the analysis of electric machines and also provide a powerful tool for the digital implementation of sophisticated control schemes for AC drives and power supplies. A number of reference frames have been

proposed over the years, of which the stationary and synchronous reference frames are the most commonly used.

The application of digital control techniques to switch mode power supplies has always been considered very interesting, mainly because of the several advantages a digital controller shows when compared to an analog one. Surely, the most relevant one is the possibility it offers for implementing sophisticated control law, taking care of nonlinearities, parameter variations or construction tolerances by means of self-analysis and autotunning strategies are very difficult or impossible to implement analogically. Another very important advantage is the flexibility inherent in any digital controller, which allows the designer to modify the control strategy, or even to totally reprogram it, without the need for significant hardware modifications. Also very important are the higher tolerance to signal noise and the complete absence of ageing effects of thermal drifts.

2.8.1 Transformations

The $\alpha\beta$ transformation represents a very useful tool for the analysis and modeling of three-phase electrical systems. In general, a three-phase linear electrical system can be properly described in mathematical terms only by writing a set of tridimensional dynamic equations, providing a self-consistent mathematical model for each phase. In some cases though, the existence of physical constraints makes the three models not independent from each other. In these circumstances the order of the mathematical model can be reduced without any loss of information [11]. The diagram shown in Figure 2.21 is considered for the following discussion.

Supposing that it is physically meaningful to reduce the order of the mathematical model from three to two dimensions, the $\alpha\beta$ transformation represents the most commonly used relation to preform the reduction of order. A tridimensional vector

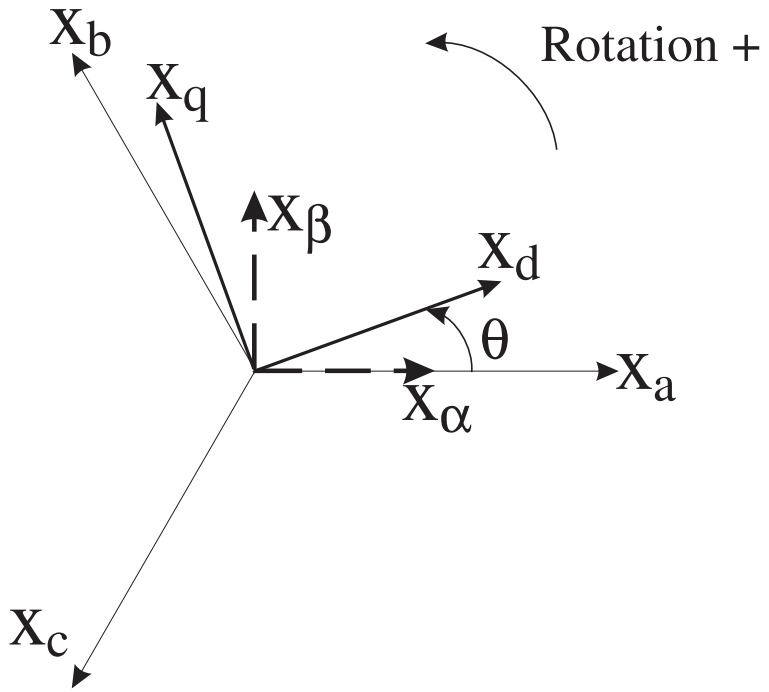


Figure 2.21: $d-q$ rotating reference frame and its relationship with the *abc* stationary reference frame.

represented by Equation 2.48 is considered.

$$\overrightarrow{\mathbf{x}}_{abc}(t) = \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{2.48}$$

This vector can represents any triplet of the systems's electrical variables (voltages or currents). The linear transformation $\mathbf{T}_{\alpha\beta o}$ represented by Equation 2.49 is considered. This transformation is known as the Clarke transformation [78]. It transforms a three-phase system into a two-phase orthogonal system.

$$\mathbf{T}_{\alpha\beta o} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & \frac{1}{3} \\ 0 & \frac{2}{\sqrt{3}} & -\frac{2}{\sqrt{3}} \\ \frac{2}{3} & \frac{2}{3} & \frac{2}{3} \end{bmatrix} \tag{2.49}$$

This transformation is known as the Clarke transformation and transforms a three-

phase system into a two-phase orthogonal system.

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_o \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & \frac{1}{3} \\ 0 & \frac{2}{\sqrt{3}} & -\frac{2}{\sqrt{3}} \\ \frac{2}{3} & \frac{2}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{2.50}$$

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_o \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \sqrt{3} & -\sqrt{3} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{2.51}$$

With x_α and x_β in an orthogonal reference frame and x_0 the homopolar component of the system.

In many applications, the homopolar component is absent or is less important. In this way, in absence of homopolar component the space vector $u = u_\alpha + ju_\beta$ represents the original three-phase input signal. When x_α is superposed with x_a and $x_a + x_b + x_c$ is zero, x_a, x_b and x_c can be transformed to x_α and x_β with the mathematical transformation represented by Equation 2.52,

$$\begin{aligned} x_\alpha &= i_a \\ x_\beta &= \tfrac{1}{\sqrt{3}} \cdot x_a + \tfrac{2}{\sqrt{3}} \cdot x_b \\ x_a + x_b + x_c &= 0 \end{aligned} \tag{2.52}$$

The two-phases α, β frame representation calculated with the Clarke transformation is then convert to a vector rotation block where it is rotated over an angle θ to follow the $d-q$ frame. The rotation over an angle θ is done according to Equation 2.53. This transformation is known as the Park transformation.

$$\begin{aligned} x_d &= x_\alpha \cdot \cos\theta + x_\beta \cdot \sin\theta \\ x_q &= -x_\alpha \cdot \sin\theta + x_\beta \cdot \cos\theta \end{aligned} \tag{2.53}$$

The vector in the $d-q$ frame is transformed from $d-q$ frame to the two-phase frame representation calculated with a rotation over an angle θ according to the Equation 2.54. This transformation is called the Inverse Park transformation.

$$\begin{aligned} x_\alpha &= x_d \cdot \cos\theta - x_q \cdot \sin\theta \\ x_\beta &= x_d \cdot \sin\theta + x_q \cdot \cos\theta \end{aligned} \tag{2.54}$$

The modification from a two-phase orthogonal α, β frame to a three-phase system is done by the Equation 2.55.

$$\begin{aligned} x_a &= i_\alpha \\ x_b &= -\tfrac{1}{2} \cdot x_\alpha + \tfrac{\sqrt{3}}{2} \cdot x_\beta \\ x_c &= -\tfrac{1}{2} \cdot x_\alpha - \tfrac{\sqrt{3}}{2} \cdot x_\beta \end{aligned} \tag{2.55}$$

The transformation of the *abc* frame reference to the equivalent $d-q$ reference frame can be performed directly by Equation 2.56.

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta - \frac{4\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{4\pi}{3}) \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{2.56}$$

Where x represents either current, voltage, or flux linkage, and θ is the angular displacement between the a-axis and d-axis of the three-phase and two-phase reference frame. The three-phase variables, x_a, x_b and x_c, are in the stationary reference frame which does not rotate in space whereas the two-phase variables, x_d and x_q, are in the synchronous reference frame whose direct (d) and quadrature (q) axes rotate in space at the synchronous speed ω_e [79].

The two-phase variables in the synchronous $d-q$ frame can be transformed directly to the *abc* stationary frame by using Equation 2.57.

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) \\ \cos(\theta - \frac{4\pi}{3}) & -\sin(\theta - \frac{4\pi}{3}) \end{bmatrix} \begin{bmatrix} x_d \\ x_q \end{bmatrix} \tag{2.57}$$

2.8.2 Tracking Controller

A control system is an arrangement of physical component connected or related in such manner as to command, direct or regulate itself or another system. In the

most abstract sense it is possible to consider every physical object a control system. In engineering and science the meaning of control system is restricted to apply to those systems whose major function is to dynamically or actively command, direct or regulate. The input is the stimulus, excitation or command applied to a control system typically from an external energy source, usually in order to produce a specified response from the control system while the output is the actual response obtained from a control system. It may or may not be equal to the specified response implied by the input.

The closed loop control system is often called feedback control system. Figure 3.19 shows a diagram of a close loop control system.

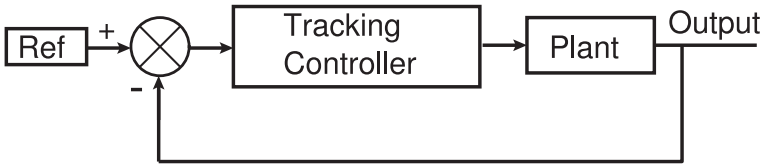


Figure 2.22: Diagram of a control system.

Considering Figure 3.19, the plant is represented by LC filter which is has a transfer function of second order. A second order controller is proposed as the tracking controller. This kind of controller is chosen because it has the same order as the plant. For the design of the tracking controller the root-locus method is employed. The poles and zeros of a transfer function can be displayed graphically in the s-plane or z-plane by means of a pole-zero map [14]. This method displays the location of the poles of the closed-loop transfer function in Equation 2.58 as a function of the gain factor K of the open-loop function GH.

$$\frac{G}{1+GH} \tag{2.58}$$

In Equation 2.58 G represents the transfer function of plant and H represents the transfer function of the feedback. In this study, the transfer function of the feedback has a unity value.

The root-locus method requires that only the location of the poles and zeros of GH be known, and does not require factorization of the characteristic polynomial. Root-locus techniques permit accurate computation of the time-domain response in addition to yielding readily available frequency response information.

The root-locus method can be quite effective in the design of either continuous or discrete-time feedback control systems, because it graphically illustrate the variation of the system closed-loop poles as a function of the open-loop gain factor K. In its simplest form, design is accomplished by choosing a value of K which results in satisfactory closed-loop behavior. This is called gain factor compensation. Specifications on allowable steady state errors usually take the form of a minimum value of K, expressed in terms of errors constants. If it is not possible to meet all system specifications using gain factor compensation alone, other forms of compensation can be added to the system to alter the root-locus as needed, for example, lag, lead, lag-lead networks, or PID controllers.

In order to accomplish system design in the s-plane or the z-plane using root-locus techniques, it is necessary to interpret the system specifications in terms of desired pole-zero configurations. Digital computer programs as Matlab/Simulink for constructing root-loci can be very helpful in system design as well as analysis.

If the pole-zero configuration of the plant is such that the system specifications cannot be met by an adjustment of the open-loop gain factor, a more more complicated cascade compensator can be added to the system to cancel some or all of the poles and zeros of the plant. The cascade compensator is represented by the tracking controller in Figure 3.19. Due to the realizability considerations, the compensator must have no more zeros than poles. Consequently, when poles of the plant are canceled by zeros of the compensator, the compensator also adds new poles to the forward-loop transfer function. The philosophy of this compensation techniques is then to replace undesirable with desirable poles.

The difficulty encountered in applying this scheme is that it is not always apparent

what open-loop pole-zero configuration is desirable from the standpoint of meeting specifications on closed-loop system performance.

As stated before the poles cancelation is used in the root-locus method. In this case, the denominator of transfer function of the plant is canceled by the numerator of the transfer function of the tracking controller. Equation 2.59 can be considered as a general transfer function of the second order system.

$$T.F. = \frac{\omega_n^2}{s^2 + 2\xi\omega s + \omega_n^2} \tag{2.59}$$

System expressed by Equation 2.59 represents the plant. The plant is basically an LC filter.

Equation 2.59 can be expressed as.

$$\frac{\omega_n^2}{s^2 + 2\xi\omega s + \omega_n^2} = \frac{K_1}{(s + p_1^p)(s + p_2^p)} \tag{2.60}$$

where $K_1 = \omega_n^2$

The tracking controller must a second order polynomial, the form of which is represented by Equation 2.61

$$\frac{(s + z_1^c)(s + z_2^c)}{(s + p_1^c)(s + p_2^c)} \tag{2.61}$$

In order to use the pole cancelation method, the following condition must be satisfied,

$$(s + p_1^p)(s + p_2^p) = (s + z_1^c)(s + z_2^c) \tag{2.62}$$

This yields to,

$$\frac{K_1}{(s + p_1^p)(s + p_2^p)} \cdot \frac{(s + z_1^c)(s + z_2^c)}{(s + p_1^c)(s + p_2^c)} \tag{2.63}$$

Equation 2.64 represents the new transfer function of the closed-loop system when the second order tracking controller is added.

$$\frac{K_1}{(s + p_1^c)(s + p_2^c)} \tag{2.64}$$

Finally, it can be stated that the tracking controller must be chosen as a second order controller, which representation is expressed by Equation 2.65.

$$\frac{(s+p_1^p)(s+p_2^p)}{(s+p_1^c)(s+p_2^c)} \tag{2.65}$$

2.8.3 Repetitive Controller

In recent years, the development of new technologies in the field of power electronics and micro-electronics has been increasing rapidly [13]. This has led to the application of more intelligent control. Digital signal processors were developed for application in the field of communications, but nowadays they can be found in different systems such as uninterruptible power supplies and motor drives, due to their ability to execute very fast and complex calculations.

Repetitive control is a very effective control strategy if the external signals (external disturbance and references) are periodical. Let

$$U(N) = [u(0), u(1), ..., u(n)]^T \tag{2.66}$$

$$U(N+1) = [u(N), u(N+1), ..., u(N+n)]^T \tag{2.67}$$

where $U(N)$ is the previous period of the output signal to be controlled and $U(N+1)$ is the current period of the output signal. $u(0)$ is the sample at instant zero when the previous period starts and $u(N)$ is the sample at instant N when the current period of signal starts. T denotes the transpose. Let the error E be

$$E(N) = [e(0), e(1), ..., e(n)]^T \tag{2.68}$$

$$E(N+1) = [e(N), e(N+1), ..., e(N+n)]^T \tag{2.69}$$

$$e(i) = r(i) - y(i); \qquad i = 0, 1, \ldots, n, N, N+1, \ldots, N+n \tag{2.70}$$

Where $e(i)$ is the error, $r(i)$ is the reference and $y(i)$ is the output. These are instantaneous values. Then, the repetitive control algorithm is

$$U(N+1) = U(N) + K[E(N) - E(N+1)] \tag{2.71}$$

There are different algorithms used for cancelation of periodic or repetitive disturbances. These algorithms are described in next sections.

2.8.3.1 Internal mode-based Repetitive Controller

According to the internal model principle [80], regulation under the presence of disturbances generated by a free dynamical system is achieved by placing a model of the disturbance generator in the feedback loop. In the discrete time domain, the z-transformation of a periodic signal with a period of N, $w(k)$, can be expressed as

$$W(z) = \frac{W_o(z)}{1 - z^{-N}} = \frac{W_o(z)^N}{z^N - 1} \tag{2.72}$$

Where W_o is defined from the first N values of $w(k)$, i.e.

$$W_o(z) = w(0) + w(1)z^{-1} + \cdots + w(N-1)z^{-(N-1)} \tag{2.73}$$

Equation 2.73 can be graphically represented as shown in Figure 2.23. The figure implies that the generator for repetitive signals is a N-step delay chain with positive feedback around it.

A servo-plant is described by

$$A(q^{-1})e(k) = q^{-d}B(q^{-1})u_r(k) + w(k) \tag{2.74}$$

where q^{-d} is the system delay operator. The q^{-d} operator is different from z^{-d}. q^{-d} is used in the representation of the system before applying the z-transformation to indicate that the system has already introduce a delay by itself while z^{-d} represents the delay introduced in the loop due to the sampling period when the z-transformation have been already applied.

$$A(q^{-1}) = 1 + a_1q^{-1} + \cdots + a_nq^{-n} \tag{2.75}$$

$$B(q^{-1}) = B_0 + b_1q^{-1} + \cdots + b_mq^{-m} \qquad b_0 \neq 0 \tag{2.76}$$

where d represents known delay steps, $e(k)$ is the tracking error, $u_r(k)$ the control input and $w(k)$ is the periodic disturbance.

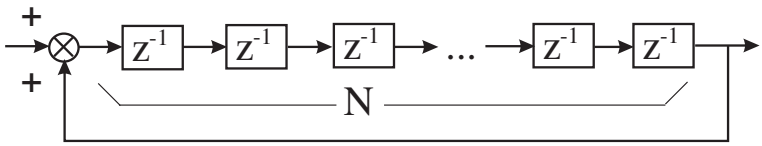


Figure 2.23: Generation of repetitive signal.

The repetitive controller, $G_r(z^{-1})$, is placed in the feedback loop. The most general form of the internal model-based repetitive controller is

$$G_r(z^{-1}) = \frac{R(z^{-1})}{S(z^{-1})(1 - z^{-N})} \tag{2.77}$$

Unfortunately, the controller given by Equation 2.77 is not robust to unmodeled dynamics. To increase robustness, the generator in Figure 2.23 must be modified by placing a low-pass filter in the feedback path. It is noted that if periodic disturbance is dominated by one frequency component, $\omega_n = \frac{\pi n}{N}$, the repetitive controller may include the sinusoidal generator as internal model, i.e,

$$G_r(z^{-1}) = \frac{R(z^{-1})}{S(z^{-1})[1 - 2\cos(\omega_n)z^{-1} + z^{-2}]} \tag{2.78}$$

2.8.3.2 External model-based Repetitive Controller

For the design of the external model-based repetitive controller, the model of the servo-plant represented by Equation 2.79 is applicable

$$A(q^{-1})e(k) = q^{-d}B(q^{-1})[u_r(k) + w'(k)] \tag{2.79}$$

The system described by Equation 2.79 is equivalently expressed by Equation 2.74 except for the first $m+d$ time-steps, provided that $B(z^{-1})$ and $(1-z^{-N})$ are coprime. Coprime numbers or polynomials means that they have no common factor other than 1.

Note that the disturbance, $w'(k)$, can be regarded as the output of the generator. If the initial conditions of the generator is set such that all modes can appear in the response, any periodic signal of a period N can be constructed by properly assigning

values for the parameters, $b'_{di}s$. This implies that the disturbance can be expressed as

$$w'(k) = \theta_d^T \phi_d(k) \tag{2.80}$$

where

$$\theta_d^T = [b_{dN}, \ldots, b_{d2}, b_{d1}] \tag{2.81}$$

$$\phi_d(k) = [x_{d1}, x_{d2}, \ldots, b_{dN}] \tag{2.82}$$

and T denotes the transpose.

Equation 2.79 can be expressed as

$$A(q^{-1})e(k) - B(q^{-1})u(k-d) = B(q^{-1})w'(k-d) \tag{2.83}$$

Equation 2.80 and 2.83 yield

$$v(k) = \theta_d^T \phi_{db}(k-d) \tag{2.84}$$

Where $v(k)$ represents the left-hand side of Equation 2.83, which is known at time k, i.e., $v(k) = A(q^{-1})e(k) - B(q^{-1})u(k-d)$, and

$$\phi_{db}(k) = B(q^{-1})\phi_d(k) \tag{2.85}$$

Notice that $\phi_d(k)$ is directly available and $\phi_{db}(k)$ can be computed from $\phi_d(k)$ because $B(q^{-1})$ is known. The estimation of the parameter vector, θ_d, at time k is denoted by $\widehat{\theta}_d(k)$. The a priori predictor output is defined by

$$\widehat{v}^0(k) = \widehat{\theta}_d(k-1)\phi_{db}(k-d) \tag{2.86}$$

Disturbance rejection or regulation is achieved by letting

$$u(k) = \widehat{\theta}_d^T(k)\phi_d(k) \tag{2.87}$$

The disturbance rejection controller includes a model of the disturbance generator. The point to be noted here is that the disturbance $w'(k)$ is unknown because b'_{bi}s are

unknown, while $\phi_d(k)$ is known. Therefore, the state vector of the disturbance model is set equal to that of the disturbance generator and the $\widehat{b}'_{bi}(k)$'s of the disturbance model are adjusted. The state of the disturbance model is outside the regulation loop for $e(k)$, i.e. the disturbance model is an external model.

The approach outlined above can be extended to the case of unknown plant parameters.

From a practical point of view, the internal model-based repetitive control is the simplest in terms of coding and computational requirements. Furthermore, this is a linear control approach and is transparent to users. However, it should be noted that low-pass filtering inside the internal model is essential for robust stability. One advantage of this control is that a long repetitive period does not change the coding complexity and execution speed. Internal model-based control is the most practical, but the others algorithms can also be used in a near future, when new digital signal processor technology is developed. External model-based control is similar to new learning schemes. Parameter identification approach for Fourier-based control does not require structural information of the controlled plant, this characteristic makes it unique. One condition for all repetitive approaches is that the number of periods k should be known and fixed [13].

2.9 Summary

In this chapter, a brief description of Matrix Converter technology is given. This description includes topologies of bi-directional switches, commutation techniques for each topology and modulation techniques for Matrix Converters. Another advantage of the Matrix Converter technology is that the Matrix Converter does not employ the large electrolytic capacitor used in the rectifier/voltage source inverter topology. For some applications the physical size of the converter is of significant importance, so the lack of large capacitor makes the Matrix Converter to be very interesting topic.

The literature reviewed highlights that despite the advantages, the commercial exploitation of Matrix Converters has been limited to date by the high number of semiconductor devices used and by the limit of the voltage conversion ratio. Though much research effort has been carried out to overcome these problems [81] [33]. In applications where the size (and consequently the weight) of the converter is of vital importance and the output voltage does not need to be higher than 86% of the input voltage, such as aerospace industry applications, the Matrix Converter topology has been widely accepted.

Theory about input and output filter used in the Matrix Converter system was given. General deduction of both the input and output filter transfer function was presented. Brief review of the control theory has been given. The transformations used in the control strategy were presented. These transformations are employed to transform from the *abc* reference frame to the α-β reference frame and then to the *d*-*q* reference frame. The direct transformations from *abc* reference frame to α-β reference were given. All of the transformations have their respective viceversa transformations. These transformations will be used in Chapter 3. To control the output voltage of the converter a second order controller will be designed, this controller acts as a tracking controller. A review of Repetitive Controllers (RC) was given. By using the bilinear transformation both the tracking controller and the Repetitive Controller can be expressed in discrete time (z) domain. These methods will be used in the design given in Chapter 3.

Chapter 3

Matrix Converter Power Supply Simulation

3.1 Introduction

Many comparative studies have been carried out to find the most appropriate system configuration for a Ground Power Unit (GPU) [82] [83]. Issues such as reliability, fault tolerance, size and weight have been considered without paying much attention to the topology of the power converter. The choice of the novel structure control for this study is the result of a detailed examination and comparison of different drive systems which have been configured on the basis of the application, the desired control strategy and the type of converter to be implemented [84] [85].

This chapter refers to the simulation of the proposed GPU system and its control strategy under different operative conditions. The purpose of this simulation is to verify the effectiveness of the Matrix Converter used in this specific application and of the control structure proposed in the previous chapter. Moreover, the simulation helps to gain insights into the effect of different parameters on the converter performance.

This chapter begins with the technical specifications of the Matrix Converter system. The design of an equivalent resistive-inductive load is then shown. Then the chapter presents a review of both software Matlab/Simulnk and Saber and the comparison of results between both packages is discussed. The open loop Matrix Converter operation is then simulated with no input filter neither output filter.

Next the Matrix Converter system with a simple voltage control loop is simulated. The tracking controller is designed and included in the system. Simulations with different load conditions are performed. Then a discussion about the opportunity of employing a control based on the d-q reference frame or the ABC reference frame is carried out. The effectiveness of the Matrix Converter control is verified by observing the converter response to a change neither in the load or in the voltage reference. Based on the data obtained, the harmonic spectra of the output voltage and input current are also presented in order to evaluated the converter performance. An improved control structure is then presented. It employs the Repetitive Control strategy combined with the designed tracking controller in order to attenuate or eliminate the unwanted harmonic distortion in the output voltage waveform of the Matrix Converter and to compensate for the steady-state error introduced by the use of a classical tracking controller with limited bandwidth in a 400Hz application. Simulation using this novel control structure is carried out to verify the output voltage control and the quality of the waveform obtained. The maximum ripple in the output voltage is then investigated and compared with the analysis carried out in Chapter 5.

By doing so, successful operation of the converter control is presented in this chapter. This helps to ensure that the laboratory prototype described in Chapter 4, will work successfully.

Early in this study, the major advantages of using a Matrix Converter for an aerospace application, in particular the absence of bulky and unreliable electrolytic capacitors, in this topology of converter has been mentioned. The use of a Matrix Converter means that, unless heavily filtered, power fluctuations in the load are directly fed to the input supply with consequent distortion of the line currents. A series of simulations

of different load conditions have been run to understand the impact of the choice of the control strategy.

The different load conditions will be analyzed as follow:

- **Matrix Converter connected to a Balanced Load**
- **Matrix Converter connected to an Unbalanced Load**
- **Matrix Converter with Load Disconnected**

3.2 Technical Specifications

In order to verify the effectiveness of this power supply and the output voltage control strategy proposed, the Matrix Converter system is simulated considering practical values for the electronic component and load conditions. The system has main technical specifications as follow:

- **Rated input voltage:** Three-phase 415V (rms, line voltage), 50Hz mains supply.
- **Rated output power:** The Matrix Converter system is designed for a total power of 7.5kVA. In practical testing a total output power of 5kVA was chosen due to limitations of the available test facility.
- **Rated output voltage:** Three-phase 117V (rms, phase voltage).
- **Output frequency:** This system is for aircraft application, so the output frequency is set to 400Hz.

The total output power is 7.5kVA. The power per phase is calculated as,

$$S = \frac{7500}{3} = 2500 \tag{3.1}$$

An equivalent load impedance can be obtained as,

$$S = VI = V\frac{V}{Z} = \frac{V^2}{Z} \tag{3.2}$$

$$Z = \frac{V^2}{S} = \frac{117^2}{2500} = 5.48\Omega \tag{3.3}$$

Considering a value of 0.6 for the power factor (pf),

$$|Z|^2 = R^2 + X_L^2 \quad \Rightarrow \quad |Z| = \sqrt{R^2 + X_L^2} \tag{3.4}$$

$$pf = \cos\theta = 0.6 \quad \Rightarrow \quad \theta = \arccos 0.6 = 53.1301^\circ \tag{3.5}$$

$$R = |Z|\cos\theta = 3.29 \tag{3.6}$$

$$X_L = |Z|\sin\theta = 4.38 \tag{3.7}$$

$$X_L = \omega L = 2\pi f L = 2\pi(400)L = 800\pi L \tag{3.8}$$

$$L = \frac{X_L}{800\pi} = \frac{4.38048}{800\pi} = 1.74mF \tag{3.9}$$

The final values for the equivalent phase resistive-inductive load, considering a $pf = 0.6$, are,

$R = 3.29\Omega$
$L = 1.74mH$

3.3 Comparison between Matlab/Simulink and Saber

Two models of the system are considered and simulated by using both Matlab/Simulink and Saber. They differ for the modulation algorithms used: the Venturini's Optimal Method in the first and the Space Vector Modulation (SVM) in the

second model. As it was described in Chapter 2 the Basic Venturini method achieves a voltage conversion ratio of 50% and is implemented by using the Equation 3.10.

$$m_{Kj} = \frac{t_{Kj}}{T_{seq}} = \frac{1}{3}[1 + \frac{2v_k v_j}{V_{im}^2}] \tag{3.10}$$

for K=A,B,C and j=a,b,c

The Optimum Amplitude Method is employed to achieve a better voltage conversion ratio. As mentioned previously a voltage conversion ration of only 50% can be achieved by using the Basic Venturini method. A better voltage conversion ratio up to 86% can be achieved with the Venturini's Optimum Amplitude method thanks to a third harmonic injection into the modulating signal of the Basic Venturini method. The equation employed for calculating the switching times in the Venturini's Optimal Amplitude method is given by Equation 3.11,

$$m_{Kj} = \frac{t_{Kj}}{T_{seq}} = \frac{1}{3}[1 + \frac{2v_k v_j}{V_{im}^2} + \frac{4q}{3\sqrt{3}} \sin(\omega_i t + \beta_K) \sin(3\omega_i t)] \tag{3.11}$$

for K=A,B,C and j=a,b,c

$$\beta_K = 0, \frac{2\pi}{3}, \frac{4\pi}{3} \tag{3.12}$$

for K=A,B,C respectively.

The Matrix Converter power supply is also simulated by using the Space Vector Modulation (SVM) algorithm. The algorithm of the SVM to be implemented was taken from [1] and detailed analysis was done in Chapter 2 for the whole understanding of this modulation strategy.

Saber is a powerful simulation software. It is more accurate than Matlab/Simulink because the parameters and algorithms for solving equations can be adjusted. In order to get a very accurate precision the component models can be modified to include environmental operating conditions. The models are written in MAST language, which can be easily edited. Saber allows to simulate using model of included components and the possibility of defining user-implemented parts by using of the versatile MAST

language, but it locks in the simulation of control systems. The disadvantage of Saber is that it takes a long time to execute a simulation. The long time required in the simulation is due to the solving algorithms employed and to the fact that it stores all the variables of interest of the system during the simulation. The waveforms obtained by using Saber in this study are similar to those obtained by using Matlab/Simulink. The waveforms resulted from the simulation by using Matlab/Simulink are shown in the following sections. Saber is used only for the calculation of the harmonic spectra of the experimental results.

3.3.1 Simulation in Saber

As mentioned early Saber is a powerful tool used in electrical and electronic systems simulations. This numerical engine allows the simulation of mixed-technology systems and also it permits the analysis of every change of the system under different operating conditions. Each block in the system consists of different components. These component can be electrical, electronic, mechanical or hydraulic and they are found in libraries of standard components or user-defined templates. The user-defined templates are models of components defined by the user using programs written in the MAST modeling language. A standard template or user-defined template has an associated symbol. This symbol can be drawn by using the drawing palette included as a tool in the Saber environment. A network list (netlist) is used to interconnect all the components in the system. This network list converts the simulated model into an ASCII file which contains the connection points and values for the model parameters. The simulated system can contain elements of different type such as linear, non linear, continuous, time discrete, digital or analogue, mechanical, electrical and hydraulic. The software generates a set of equations. The size of the set of equations depends on the model complexity and are solved by Saber which chooses the appropriated algorithm to both verify the functionality of the model and to tune the design parameters. The model can be simulated in the time or frequency domain. Many subtle effects and environmental conditions in the components not included in other simulation software can be included in Saber. This characteristic makes the

effectiveness of Saber a notable advantage.

Before any control system could be simulated, the Matrix Converter needed to be modeled. The following parts needed to be implemented.

- Output filter
- Input filter
- Matrix of bidirectional switches
- PWM generator
- Modulation strategies

The electronics have been modeled using electrical components (i.e. switches, diodes, capacitors, resistors, inductors, power supplies and comparators) from the SABER standard library, selecting for each of them the desired parameter values. The bi-directional switches have been modeled by using MAST language. In early work, electronic devices from the standard library have been employed to simulate the bi-directional switches, but it was concluded that the simulation runs faster when the devices are simulated by using MAST language.

The next stage was to create the necessary switching signals which would generate a safe commutation of the bi-directional switches. Using MAST, events can be scheduled at particular points in time so that logic signals can be generated to mimic the digital logic functionality of a Field Programmable Gate Array (FPGA)(which would be used for logic implementation in a real controller) with the correct time resolution of a real system. The two techniques were tested with the SABER simulator by simulating the logic signals coming from a modulator using two ideal clock units with different duty cycles. The results were compared and were both found to work well according to the literature. Since the protection of a Matrix Converter is more robust when using a current direction based commutation technique [86], this method was used in all of the Matrix Converter system simulations.

Using the MAST language the modulator has been successfully designed. The three different modulation techniques have all been implemented and compared using simple models of test circuits such as a three input phase to single output phase Matrix Converter. The modulation techniques implemented are as follows:

- Venturini basic algorithm (Section 2.3.1)
- Optimum Amplitude Venturini Algorithm (Section 2.3.2)
- Space Vector Modulation methods (Section 2.3.4)

The events were scheduled using MAST language to generate the same type of PWM resolution that would be used in a physical prototype. A simulation of the Matrix Converter driving different types of loads was run using different modulation techniques. These results show that there is obviously a different harmonic content in the output waveform for each modulation technique. The source codes using MAST language for the simulation of the Matrix Converter system are listed in Appendix C. The source code shown uses the Space Vector Modulation (SVM) modulation technique for the simulation of the Matrix Converter system.

The schematic diagram of the Saber simulation model in Saber is shown in Figure 3.1. Resistor R4 has a big value (10MΩ) and it is used to isolate the system from ground. In Saber simulations, the model must be grounded in order to allow the algorithm to solve the equations. The arrangement of a big resistor connected to a ground point is to create a floating point with no connection. A more detail schematic diagrams can be seen in Appendix B. It should be noted that in this initial simulation the load is considered as a pure resistive load. Both the commutation and sampling frequency are set up to 12.8kHz. When the commutation and sampling frequency was changed to check the reliability of the model, the output voltage was different from the voltage expected. This was due to the waveform samples taken and the conditions imposed in the modulation template code. The MAST code was then modified and logic conditions were included to solve the problem presented.

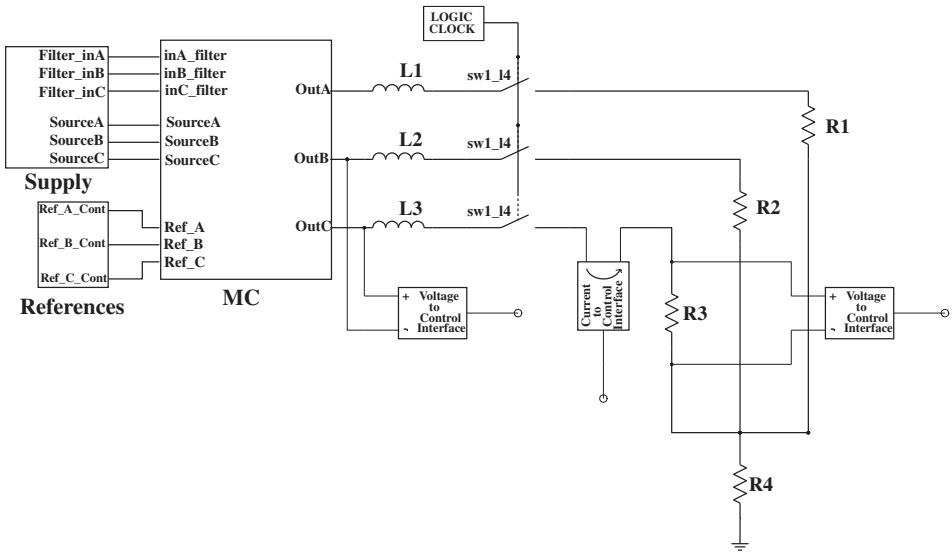


Figure 3.1: Schematic of Matrix Converter used in Saber simulation.

Figure 3.2 shows the output voltage of phase c simulated via Saber. As it can be in Figure 3.1, no output voltage controller was employed.

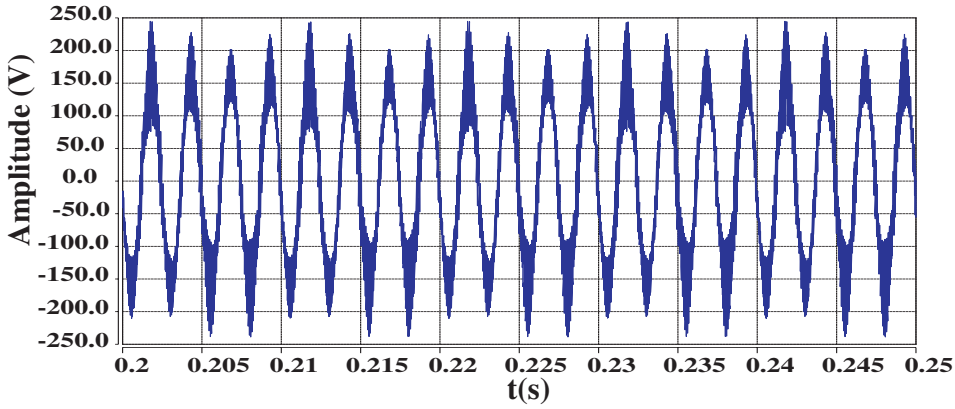
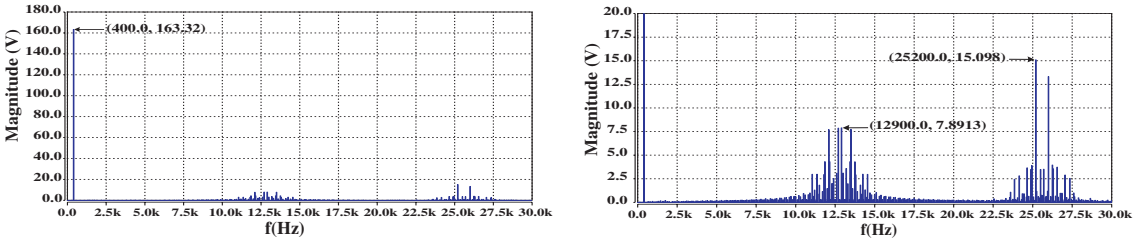


Figure 3.2: Waveform of load voltage in phase c when simulated in Saber.

The harmonic spectra of the output voltage in phase c is shown in Figure 3.3. This harmonic spectra is calculated using the calculator tool included in Saber. This is a powerful tool that also allows to calculate different performance factors in a waveform (mean value, maximum value, minimum value, RMS value, etc).



(a) Harmonic spectra of load voltage without filters

(b) Details of the harmonic spectra

Figure 3.3: Harmonic spectra of load voltage in phase c using Saber.

3.3.2 Simulation using Matlab/Simulink

In order to get faster simulations, but still good results and to be able to implement the control system in a more straightforward way, the software Matlab/Simulink was used. All simulations obtained in Matlab/Simulink were compared to those obtained in Saber which has been used in the end only for the purpose of comparison. The schematic diagram used for the model simulation of model in Matlab/Simulink is shown in Figure 3.4.

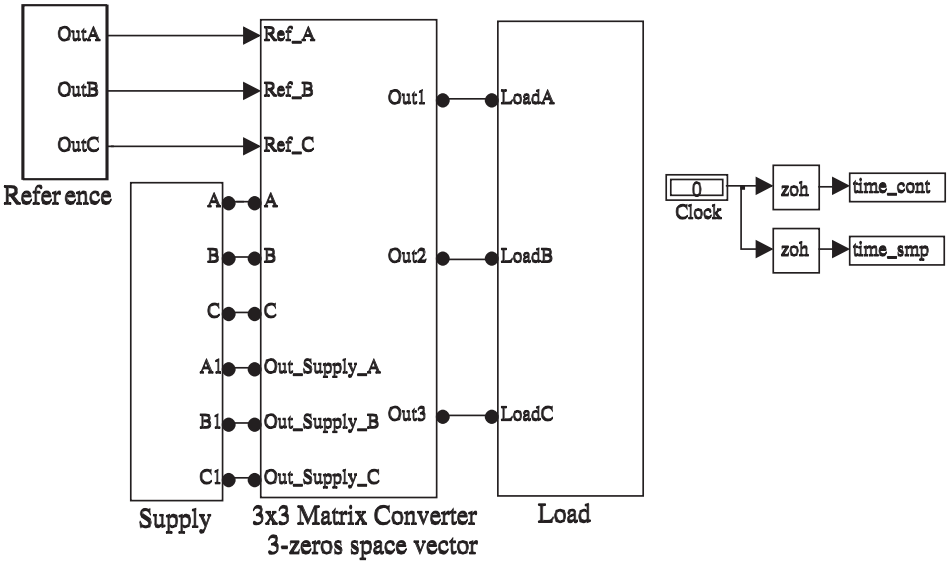


Figure 3.4: Schematic of Matrix Converter used in Matlab/Simulink simulation.

Figure 3.5 shows the output voltage waveform obtained in phase c when Matlab/Simulink is employed. In this simulation the output voltage controller is not used, neither is the input or output filter.

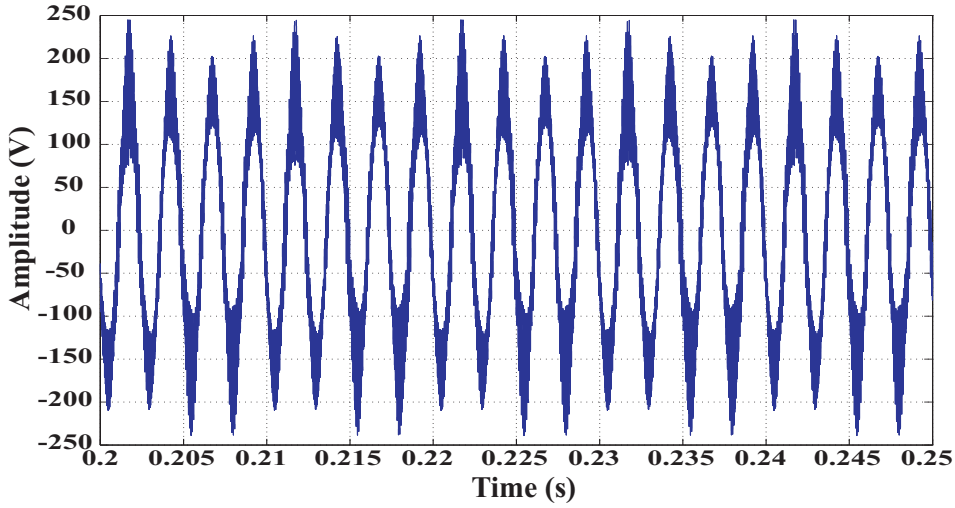


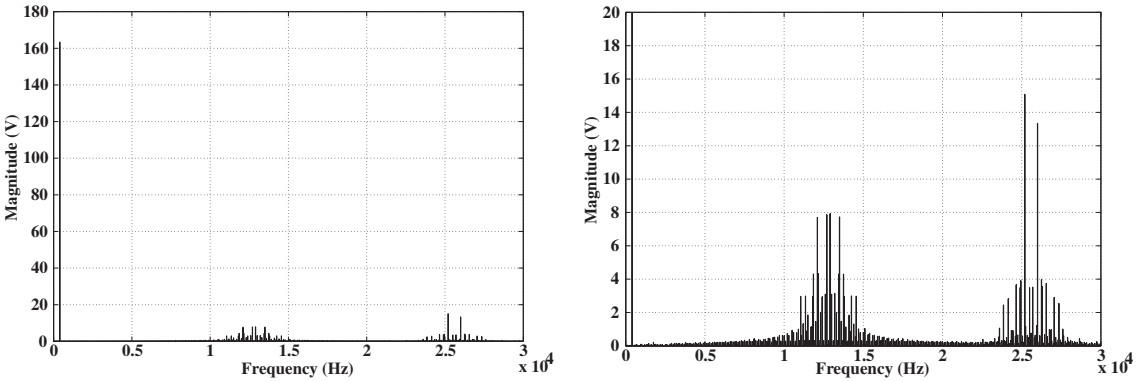
Figure 3.5: Load voltage in phase c when simulated in Matlab/Simulink.

Figure 3.6 shows the harmonic spectra of the output voltage in phase c. This harmonic spectra is obtained by using a program developed in Matlab. The data is saved in a Matlab file and then the program developed in Matlab code is used to calculate the Fast Fourier Transform (FFT).

3.4 Simulation without Controller

3.4.1 Matrix Converter with neither Input or Output Filter

One of the first simulations to be run was the Matrix Converter system without input and output filter. As it was mentioned previously, the load operation conditions of the system included a load perfectly balanced, then an unbalanced load and finally a no load connected. Figure 3.7(a) shows the waveform obtained when the Matrix Converter system is connected to a perfectly balanced load, while Figure 3.7(b) shows

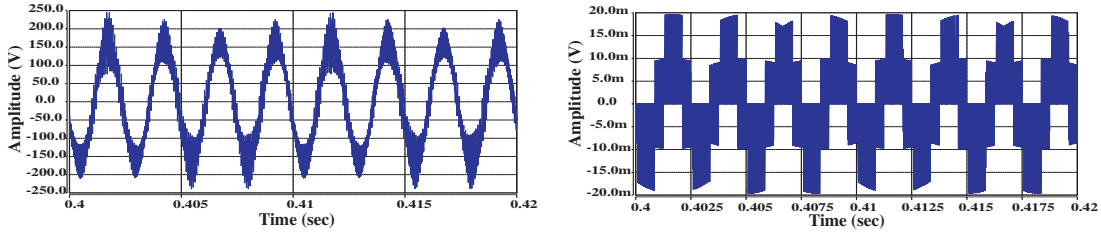


(a) Harmonic spectra of load voltage without filters

(b) Details of the harmonic spectra

Figure 3.6: Harmonic spectra of load voltage in phase c using Matlab/Simulink.

the waveform obtained in phase c when the load is disconnected. It should be noticed that no input filter or output filters are connected to the Matrix Converter.

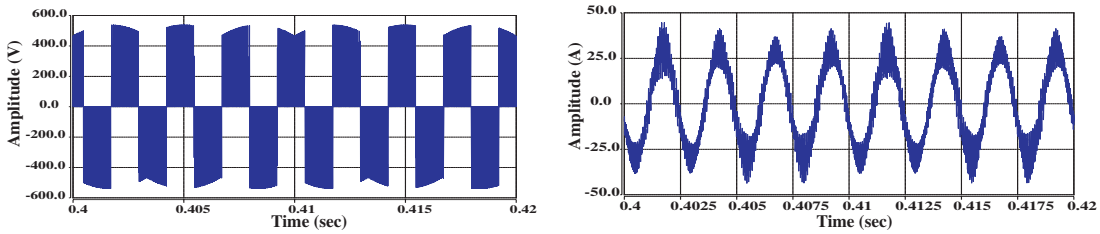


(a) MC is connected to a balanced load.

(b) Load is not connected to MC.

Figure 3.7: Output voltage in phase c without filters.

The waveform of the the Matrix Converter output voltage between phase a and b is shown in Figure 3.8(a) while the load current in phase c can be seen in Figure 3.8(b).



(a) Line-to-line voltage.

(b) Load current in phase c.

Figure 3.8: Line-to-line voltage and load current of the Matrix Converter.

3.4.2 Matrix Converter with Output Filter

Figure 3.9 shows the diagram of the output filter to be designed for using in the system. The filter must be suitable to produce a sinusoidal output voltage waveform at 400Hz.

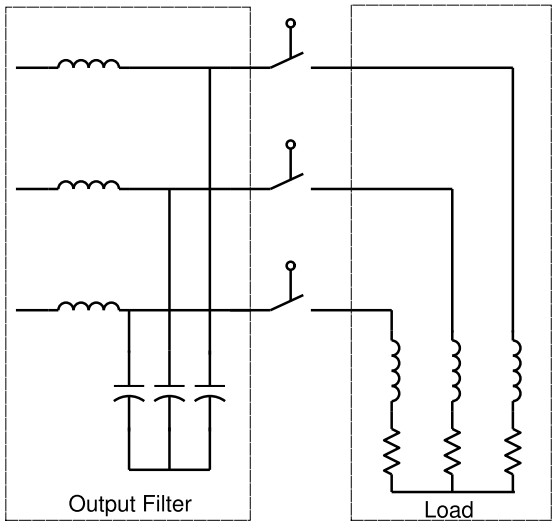


Figure 3.9: Structure of output filter.

The output filter is designed by using its transfer function expressed by Equation 2.47. In this equation variables L, C and r refer to inductance, capacitance and internal resistance of inductor respectively. The value of the capacitor is calculated by math-

ematical method and by using Bode plots. Because low order harmonics must be attenuated in order to meet the requirements imposed in the output voltage, the cut-off frequency is chosen to be above 1500Hz. The ripple in the output voltage waveform must not exceed 3V (2.6%) of the nominal output voltage and the voltage total harmonic distortion must not exceed 4%. Another requirement to be considered when designing the output filter is that the resonance frequency must be chosen in a way that it is put lower than the switching frequency used by the bi-directional switches. The switching frequency of the bi-directional switches is 10kHz, so the resonant frequency is chosen around 10000 rad/sec, which represents $\frac{10000 rad/sec}{2 \cdot \pi} =$ 1591.55kHz.

The resonance frequency is calculated by using the Equation 3.13.

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{3.13}$$

Calculating the value of the capacitor as a function of the value of the inductor Equation 3.13 yields,

$$\sqrt{LC} = \frac{1}{\omega_0} \tag{3.14}$$

$$C = \frac{1}{{\omega_0}^2 L} \tag{3.15}$$

According to [20] the value of the inductor must be small as possible in order reduce the output impedance of the power converter. The output impedance must be low because the power converter is operating as a voltage source. Considering a fixed value of the inductor equal to 128μH with an internal resistance of 50mΩ Equation 3.15 can be written as,

$$C = \frac{1}{{\omega_0}^2 \cdot 128\mu} = \frac{7812.5}{\omega_0^2} \tag{3.16}$$

The value of the resonance frequency should be around 10000rad/sec. A range between $\omega_{o1} = 9000 rad/sec$ and $\omega_{o2} = 11000 rad/sec$ is proposed to calculate the value

of the capacitor. Assuming this range, Equation 3.16 can be expressed in two parts,

$$C_1 = \frac{7812.5}{9000^2} = \frac{7812.5}{\omega_{01}^2} = 96.45\mu F \tag{3.17}$$

$$C_2 = \frac{7812.5}{11000^2} = \frac{7812.5}{\omega_{02}^2} = 64.57\mu F \tag{3.18}$$

Therefore the value of capacitor C must be between the range,

$$C_2 < C < C_1 \tag{3.19}$$

$$64.57\mu F < C < 96.45\mu F \tag{3.20}$$

The value of the capacitor is chosen the be the smallest possible to reduce the size of the power converter and also it have to be a commercial values. Analyzing this requirement different values were proposed and finally a value of 68μF was chosen for the capacitor. Therefore the final suitable values for the output filter are as follow:

- $R_L = 50m\Omega$
- L = 128μH
- C = 68μF

Using these values the final output filter transfer function expressed in the s-domain is given by Equation 3.21

$$\frac{1.149 \cdot 10^8}{s^2 + 390.6s + 1.149 \cdot 10^8} \tag{3.21}$$

The Bode plot of Equation 3.21 can be found by using Matlab/Simulink. Analyzing this plot, it can be seen that the cut-off frequency is obtained at 2.65kHz and the resonant frequency is found at 1.71kHz. The gain at the resonant frequency is 28.8dB. Figure 3.10 shows the frequency response of the output filter transfer function.

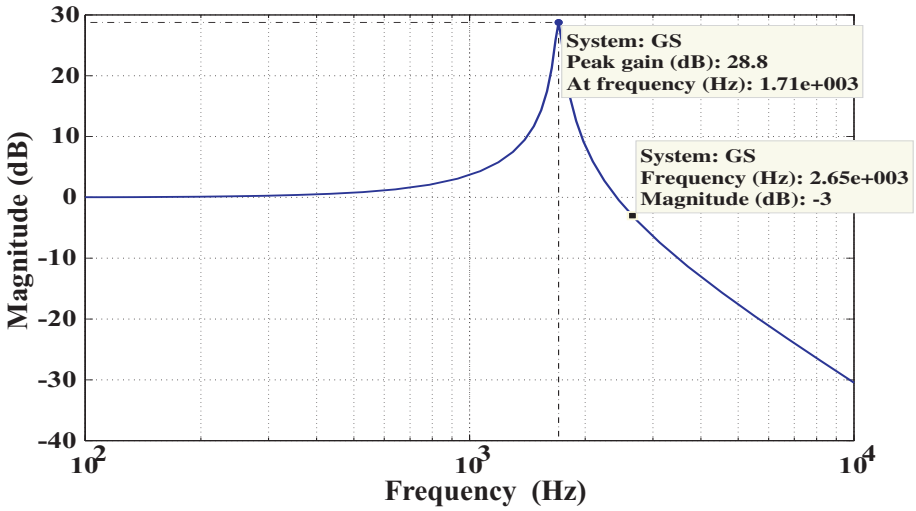
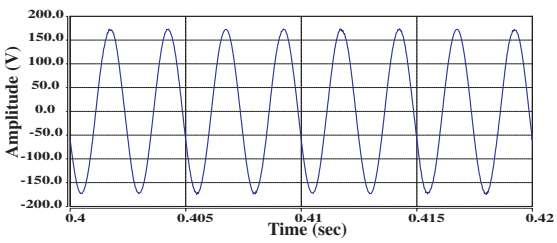


Figure 3.10: Bode plot of the output filter transfer function in s domain.

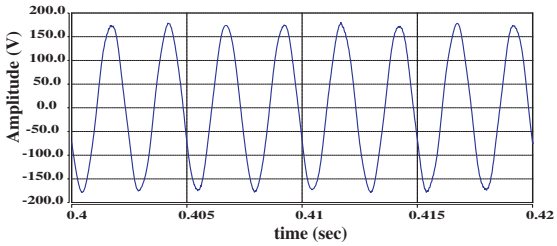
Once the output filter is designed in the s-domain, it is transformed to discrete time domain (z-domain) by using the zero-order-hold function in Matlab. The sampling frequency used in the discrete time model is the same as the one that will be used in the practical implementation. The sampling frequency has a value of 12.8kHz. The output filter transfer function in discrete time domain (z-domain) is expressed by Equation 3.22. This transfer function will be used in the plant evaluation for the design of the output voltage controller.

$$\frac{0.3273z + 0.3239}{z^2 - 1.319z + 0.9699} \tag{3.22}$$

The output voltage waveforms obtained when the Matrix Converter system is simulated with the output filter added are shown in Figure 3.11. In Figure 3.11(a), the MC is connected to a perfectly balanced load. The worst case is when the Matrix Converter is not connected to a load. Figure 3.11(b) shows the waveform of the output voltage when the load is disconnected. Its harmonic spectra is shown in Figure 3.12.

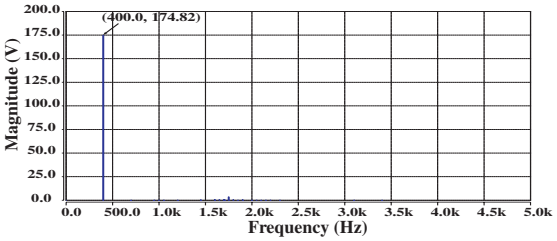


(a) MC is connected to a balanced load.

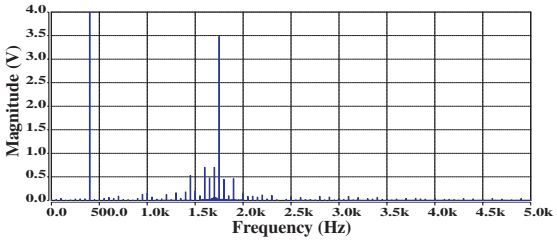


(b) The load is disconnected.

Figure 3.11: Output voltage in phase c using the output LC low-pass filter.



(a) Harmonic spectra with load disconnected



(b) Details of the Harmonic spectra with load disconnected

Figure 3.12: Harmonic spectra of output voltage in phase c.

3.4.3 Matrix Converter with Input and Output Filter

The operation of power converters produce harmonic distortion. This distortion is injected to the grid and cause problems to other electronic equipments. This situation was explained in section 2.6. The power converter must meet the requirements given in IEEE 519 [26]. This standard refers to the harmonic content that is allowable to inject into the electrical network. In order to reduce or attenuate the current harmonics in the supply an LC low-pass input filter has to be included. The LC filter causes disruptions during the power-up procedure of the power converter. The transients of current at the startup can cause over voltage situations just after the LC filter which can destroy the power devices of the converter [87]. A damping resistor is added as a solution to this problem. This damping resistor has the purpose of attenuating the current through the inductor. The value of the damping resistor is chosen in such way that its power losses are as low as possible. The diagram of the input filter to be included in the power supply side is shown in Figure 3.13.

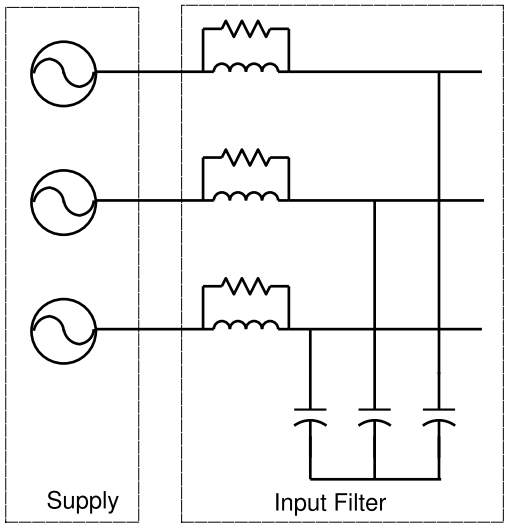


Figure 3.13: Structure of input filter.

The input filter is designed by using the transfer function expressed by Equation 3.23. In this equation variables L, C, R and r refer to the values of the inductor, capacitor, damping resistor and internal resistance of inductor respectively. The input frequency is the mains frequency, which has a value of 50Hz. The input filter must attenuate

low order harmonic multiples of 50Hz. Values of components in the input filter must be as small as possible.

$$F(s) = \frac{\frac{Ls+r+R}{RLC}}{s^2 + (\frac{r}{L} + \frac{1}{RC})s + (\frac{r}{LRC} + \frac{1}{LC})} \tag{3.23}$$

A value of 700μH is proposed as initial value for the inductor. The internal resistance of the inductor is 50mΩ. Using Equation 2.41 and substituting these values,

$$F(s) = \frac{\frac{700\mu \cdot s+0.05+R}{R \cdot 700\mu \cdot C}}{s^2 + (\frac{0.05}{700\mu} + \frac{1}{RC})s + (\frac{0.05}{700\mu \cdot RC} + \frac{1}{700\mu \cdot C})} \tag{3.24}$$

$$F(s) = \frac{\frac{s+71.43+1428.57 \cdot R}{RC}}{s^2 + (71.43 + \frac{1}{RC})s + (\frac{71.43}{RC} + \frac{1428.57}{C})} \tag{3.25}$$

$$F(s) = \frac{s + 71.43 + 1428.57 \cdot R}{RC \cdot s^2 + (71.43 \cdot RC + 1)s + (1428.57 \cdot R + 71.43)} \tag{3.26}$$

The transfer function expressed by Equation 3.26 can be plotted for different values of capacitor and damping resistor. Matlab/Simulink was used to generate the Bode plots. An important consideration to be taken in account is that the cut-off frequency of the input filter must be quite lower that the switching frequency. In the design, it should also be considered the power losses due to the value of the damping resistor. The maximum permitted value of the damping resistor losses is stated around 1W. If the value of the damping is high the power losses reduce but the total harmonic distortion (THD) increases. If the value of the damping resistor is low, the power losses increase but the THD decreases, so the value chosen should be the most suitable in order to have a balance between power losses and THD. Also, there is a problem when the value of the damping resistor is low. If its value is low the power losses and total harmonic distortion are in the range of acceptable values, but the tracking controller does not work properly. Some simulations have been done using different values of the damping resistor in order to know the behavior of the system.

Software Saber was employed to calculate the power losses and THD of the input filter. Matlab/Simulink was used to obtain the frequency response of the input filter. The most suitable values of capacitor and damping resistor that meet the requirements for the input filter are 26μF and 56Ω respectively.

The final values of the output filter that meet the requirements are:

- L=700μH (Inductor)
- r=50mΩ (Internal resistance of inductor)
- C=26μF (Capacitor)
- R=56Ω (Damping resistor)

The final transfer function of the input filter in s-domain using these values is given by Equation 3.27.

$$\frac{686.8s + 5.499 \cdot 10^7}{s^2 + 758.2s + 5.499 \cdot 10^7} \tag{3.27}$$

Taking this equation the frequency response of the input filter can be obtained. Figure 3.14 shows both the cut-off frequency and the resonance frequency, It can be seen that the cut-off frequency occurs at 1.83kHz while the resonance frequency happens at 1.18kHz. The gain (attenuation) at the resonant frequency is 19.8dB.

After designing the input filter in s-domain, it was transformed to discrete time domain (z-domain) by using the zero-order-hold function in Matlab. The sampling frequency used in the discrete time model is 12.8kHz which is the same as the one used in the practical implementation. The input filter transfer function in discrete time domain is expressed by Equation 3.28,

$$\frac{0.2093z + 0.1076}{z^2 - 1.626z + 0.9425} \tag{3.28}$$

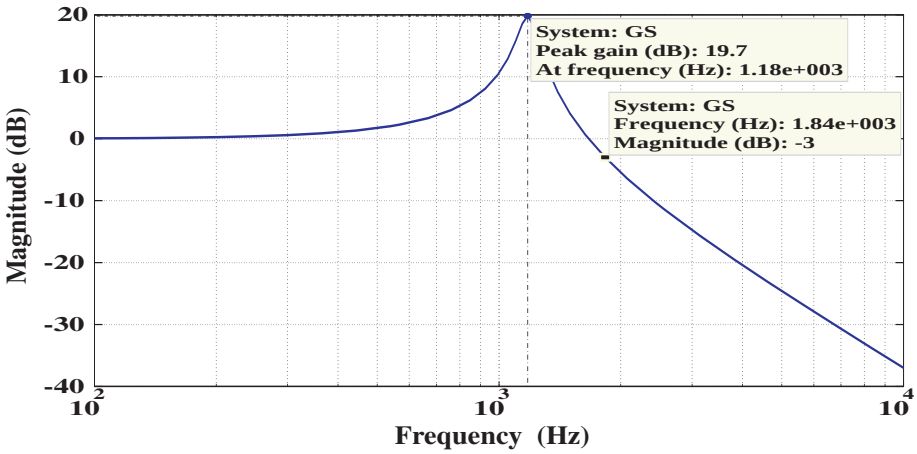


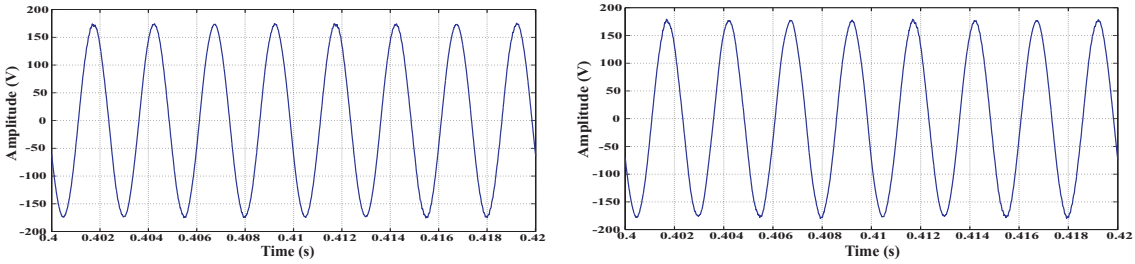
Figure 3.14: Bode plot of the input filter transfer function in s domain.

The transfer function represented by Equation 3.28 has influence in the performance of the output voltage controller. The input filter provokes a disturbance in the input voltage. This disturbances affect the quality of the input voltage waveforms used as supply references for the modulator where the modulation algorithm is implemented and therefore the pulse trains needed to commute the bi-directional switches in the Matrix Converter.

After including the output filter in the Matrix Converter system, the input filter is added. The output voltage waveforms obtained when the Matrix Converter system is simulated including the output and input filter are shown in Figures 3.15(a) and 3.15(b).

The waveforms of the input current without and with input filter are shown in Figure 3.16.

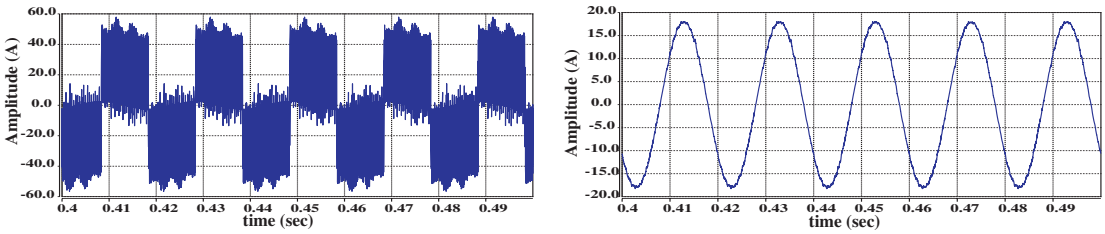
Figure 3.17 shows the harmonic spectra of the input current using the input filter when the input filter is used the total harmonic distortion is 0.1289%.



(a) MC connected to a balanced load.

(b) The load is disconnected.

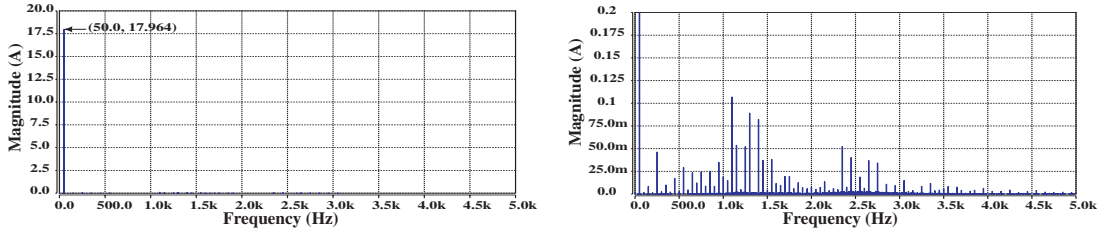
Figure 3.15: Waveform of the output voltage in phase c using both the input and output filter.



(a) Without input filter

(b) With input filter

Figure 3.16: Waveform of the input current in phase C.



(a) Harmonic Spectra of the input current

(b) Details of the input current harmonic spectra

Figure 3.17: Harmonic spectra of the input current in phase C.

3.5 Simulation with Tracking Controller

In an ideal scenario the plant of our system is represented by the output filter, a delay and a gain (the last two being a representation of the Matrix Converter and the modulation system). Equation 3.22 represents the transfer function in z-domain of the output filter that will used in the design of the tracking controller.

The root locus in the z-plane of the plant function is generated by using Matlab/Simulink. This root locus is shown in Figure 3.18.

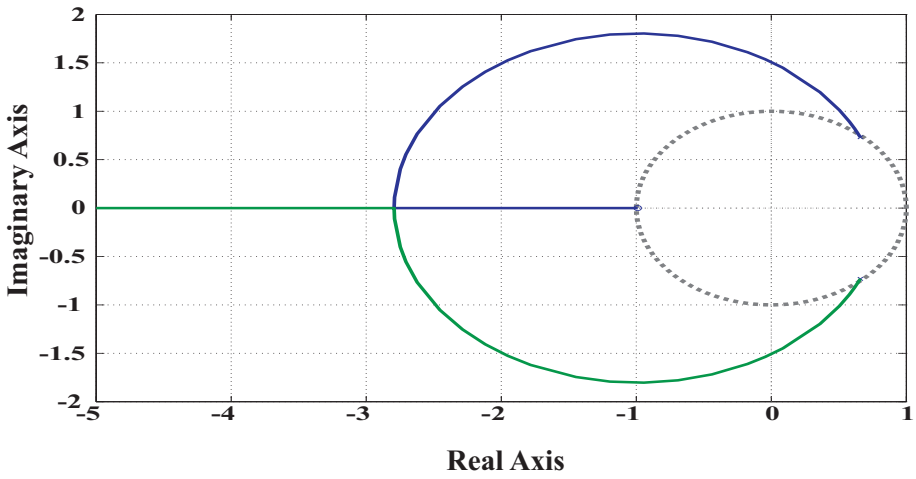


Figure 3.18: Root locus of the input filter transfer function.

The poles cancelation method presented in 2.8.2 is used in the design of the controller. By using this method, the new transfer function can be expressed as,

$$\frac{0.3273z + 0.3239}{z^2 - 1.319z + 0.9699} \cdot k \cdot \frac{z^2 - 1.319z + 0.9699}{az^2 + bz + c} = \frac{0.3273z + 0.3239}{az^2 + bz + c} \tag{3.29}$$

The tracking controller is represented by the expression,

$$k \cdot \frac{z^2 - 1.319z + 0.9699}{az^2 + bz + c} \tag{3.30}$$

Solving the characteristic equation of 3.30 gives the coefficients of the controller

denominator. The solution of this equation is a pair of poles. The poles are chosen to be inside the unity circle and they must be on the real axis.

$$az^2 + bz + c = (z + p_1) \cdot (z + p_2) \tag{3.31}$$

After using the "sisotool" option in Matlab, the poles are chosen as:

$$p_1 = -0.4999 \qquad \& \qquad p_2 = 0.9999 \tag{3.32}$$

Where p_1 and p_2 are interpreters. Using these values the tracking controller can be written as

$$k \cdot \frac{z^2 - 1.319z + 0.9699}{(z + 0.4999)(z - 0.9999)} = k \cdot \frac{z^2 - 1.319z + 0.9699}{z^2 - 0.5001z - 0.4999} \tag{3.33}$$

Once again, the "sisotool" option is used to find the gain of the controller. The most suitable value of the gain to assure the stability of the system is $k = 0.05$. The final equation of the tracking controller is,

$$0.05 \cdot \frac{z^2 - 1.319z + 0.9699}{z^2 - 0.5001z - 0.4999} \tag{3.34}$$

Figure 3.19 shows the structure of the system. The controller block is represented by Equation 3.34. The plant block is represented by the output filter transfer function (Equation 3.22). Figure 3.20 shows the root locus of the whole system shown in Figure 3.19.

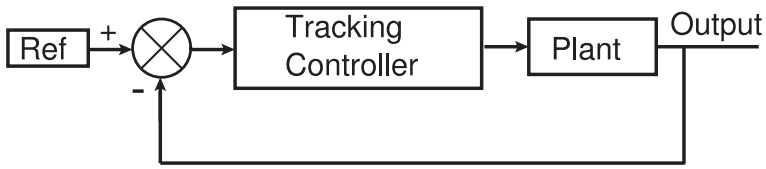


Figure 3.19: Structure of the system using a second order controller as a tracking controller.

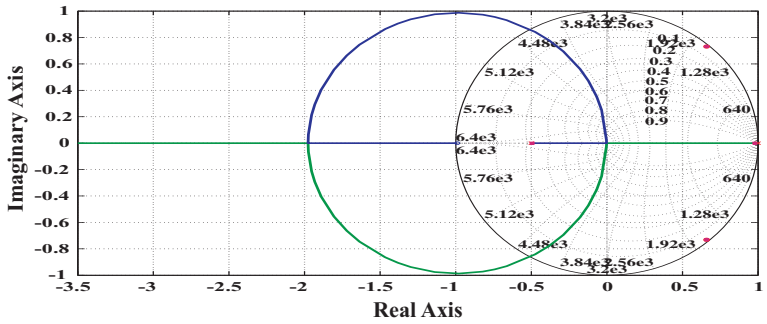


Figure 3.20: Root locus of the whole system shown in Figure 3.19.

3.5.1 Voltage Control in d-q Reference Frame

The output voltages are measured across the capacitors in the output filter and are then feedback separately to the system control. In the d-q reference frame the three-phase output voltages are transformed into two dc signals on the d and q axis. Using the designed tracking controller on each of the two axes, the presence of the interpreter will ensure a small steady state error on the voltage loop. The control signal in d-q frame are converted back to the ABC reference frame an applied to the modulator. These signal are the reference signal required by the modulator in order to produce the pulses needed to commutate the bi-directional switches. Figure 3.21 shows the control strategy in d-q reference frame.

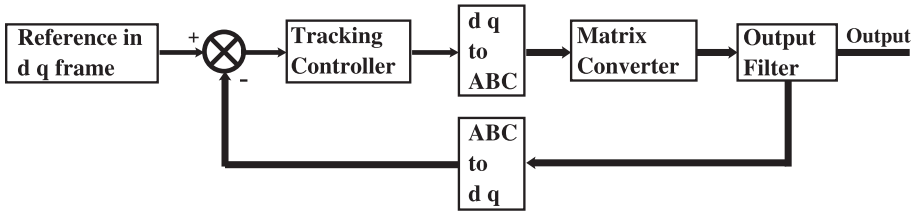


Figure 3.21: Control strategy in d-q reference frame.

Figure 3.22 shows the final structure and configuration of the tracking controller.

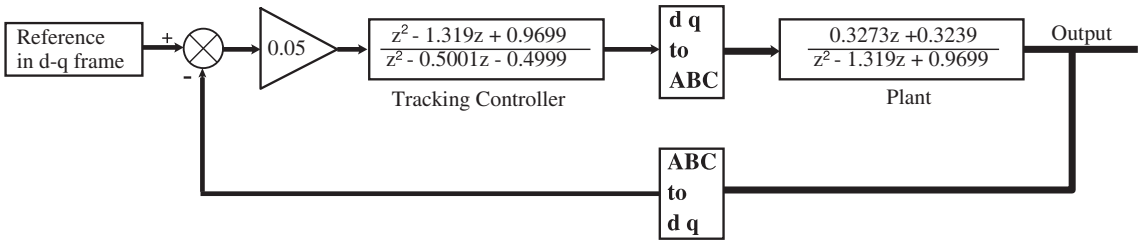


Figure 3.22: Structure and final values of tracking controller when using control strategy in d-q reference frame.

Figure 3.23 shows the waveform of the output filter obtained in all phases when the controller is used in the d-q reference frame and the Matrix Converter is connected to a perfectly balanced load. Figure 3.24 shows the waveform obtained when the load is disconnected.

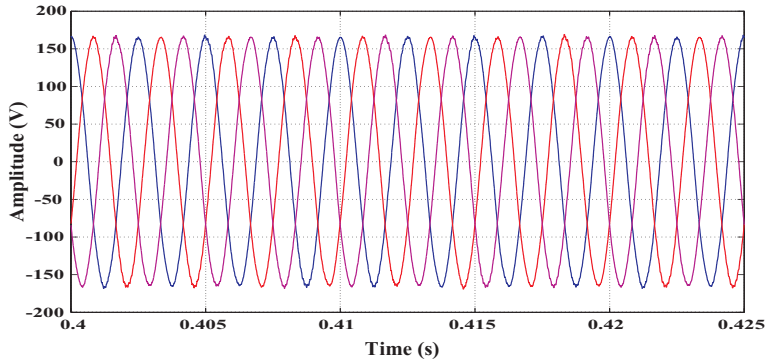


Figure 3.23: Output voltage all phases using tracking controller when matrix Converter is connected to a perfectly balanced load.

The designed tracking controller works very well when the load is perfectly balanced. With this kind of control there is obviously a problem when the load is unbalanced since the transformations ABC to d-q and viceversa d-q to ABC are defined only in the case of a balanced system. As a result of this inconvenience with the transformation, the signals generated by the tracking controller are not sinusoidal and consequentially the ABC reference signals to the Matrix Converter are distorted.

Figure 3.25 shows all three-phase waveforms of the output voltage when the Matrix Converter is connected to an unbalanced load. For this study the unbalanced load

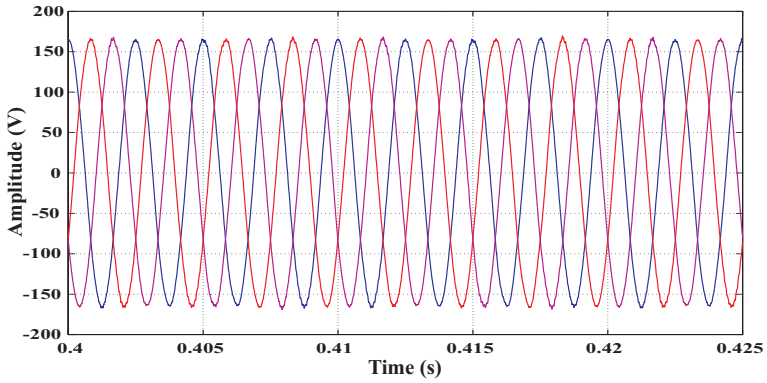


Figure 3.24: Output voltage in all phases using tracking controller when the Matrix Converter is not connected to a load.

has been produced in a way that the load in phase a is connected to 140% of the nominal load, load in phase b is connected to 100% of the nominal load and load in phase c is connected to 60% of the nominal load. The level of distortion presented in the output waveforms obtained is not acceptable due to requirements imposed in the design of the power converter. These requirements dictate that the level of the output voltage in each phase must be 117Vrms with a variation less than 3V. The level of the output voltage must be maintained when the load is unbalanced or even if the load is disconnected.

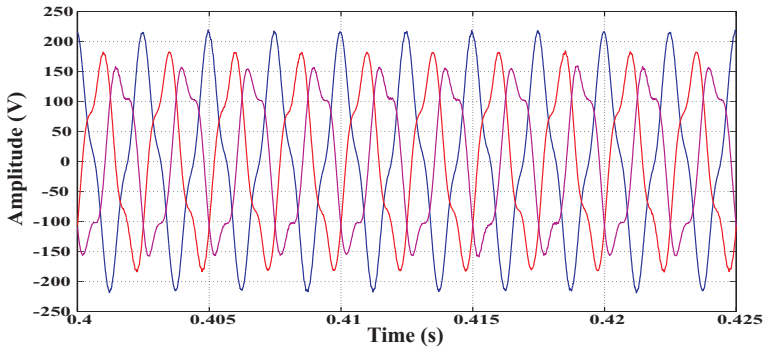


Figure 3.25: Output voltage in all phases using tracking controller and connected to an unbalanced load.

3.5.2 Voltage Control in ABC Reference Frame

The problem presented in previous section when the Matrix Converter is connected to an unbalanced load can be solved using a control system working directly in the ABC reference frame. The reference signals which are a set of a three-phase rms voltages at 400Hz in the ABC frame are compared to the voltages measured across the output filter capacitors. The error signal obtained is then applied to the tracking controller on each phase. Each tracking controller generates a control signal which is applied directly to the modulator. Then the modulator produces the pulses required to commutate the bi-directional switches. The general scheme of the system used is shown in Figure 3.26.

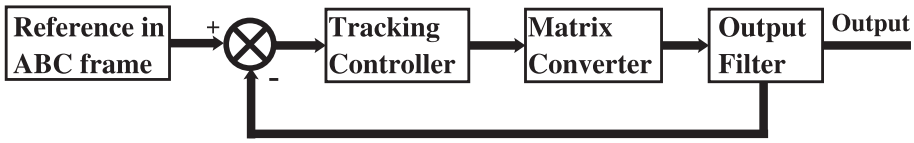


Figure 3.26: Control strategy in ABC reference frame.

Figure 3.27 shows the final structure and configuration of the control system when the ABC reference frame is used. The controller is a second order polynomial and it has the coefficients represented by Equation 3.34. The procedure used to design the tracking controller of for the ABC reference is the same as the one used in the design of the tracking controller in the d-q reference frame. In this case because the The gain is now set as 0.6. Since the reference of our control is a 400Hz three-phase signal, the interpreter present in the controller will not be able to achieve a small steady state error, being the all closed-loop system of a limited bandwidth. Therefore a gain has been introduced in order to compensate for the amplitude mismatch in the output. The value of this gain has been found to be 6 by trial and error. When the control system was design, the block representing the Matrix Converter was considered as a unity gain. In the practical implementation, the Matrix Converter consists of electronic components which have voltage drops and dissipate energy and therefore the Matrix Converter has a transfer function different from a unity gain. This modifies the closed loop considered in the design of the tracking controller. In the design of

the controller, only the output filter has been considered as the plant. The Matrix Converter block is not considered as part of the closed loop. In practice, it have been found that the Matrix Converter can be replaced by a gain with a value between 5 and 6. Also, the block representing the Matrix Converter introduces a delay. This delay can be compensated by the controller.

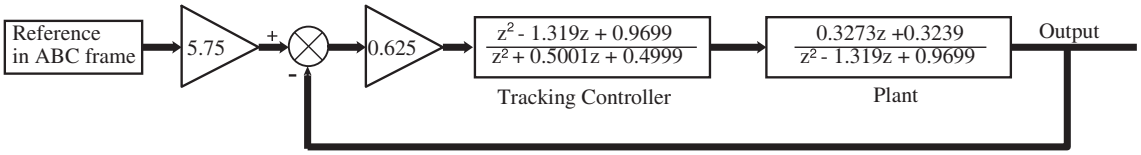


Figure 3.27: Structure and final values of tracking controller when using control strategy in ABC reference frame.

Figures 3.28 and 3.29 shown the waveforms of the output voltage obtained when the tracking controller in the ABC reference frame is used and the Matrix Converter system is connected to a perfectly balanced load and to an unbalanced load respectively. The waveforms of the output voltages obtained when the load is disconnected are shown in Figure 3.30.

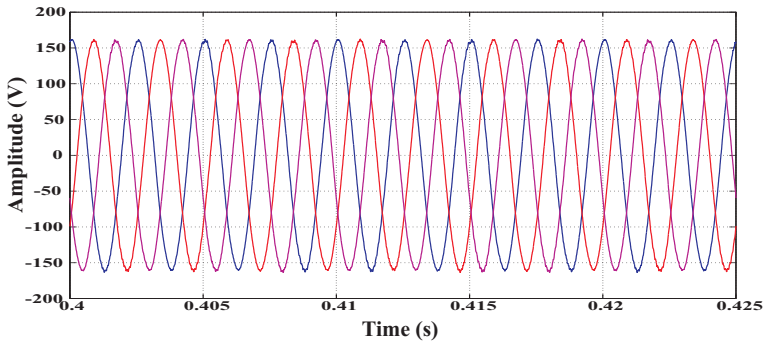


Figure 3.28: Output voltage in phase c using tracking controller and connected to a balanced load.

It still results a phase shift in the system response as it can be seen in Figure 3.31. The introduction of a Repetitive Control structure will be able to compensate for the amplitude and phase steady-state errors and for the distortion introduced by the unbalanced load.

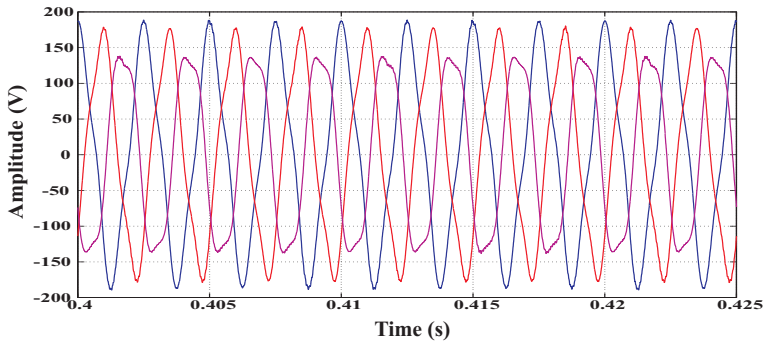


Figure 3.29: Output voltage in phase c using tracking controller and connected to an unbalanced load.

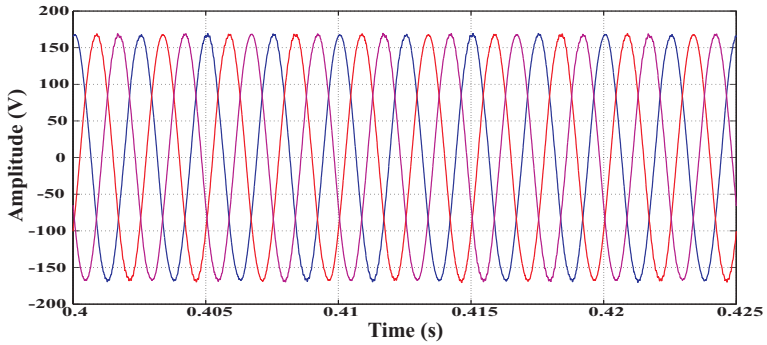


Figure 3.30: Output voltage in phase c using tracking controller and load disconnected.

3.6 Voltage Control with Tracking Controller plus Repetitive Controller

Many research works in literature have presented different configurations for the structure of a Repetitive Controller according to the application to which they need to be applied. Mainly, Repetitive Controllers are employed in robot applications and in those applications which requires tracking a repetitive reference pattern. A comparison of these topologies for this Matrix Converter application was carried out and two of the topologies reviewed were specifically chosen to be suitable. The first configuration considered is mentioned in [88] while the second configuration analyzed is proposed in [89]. Both configurations have different ways for calculating the values of their parameters. The details for calculating such parameters will be given later.

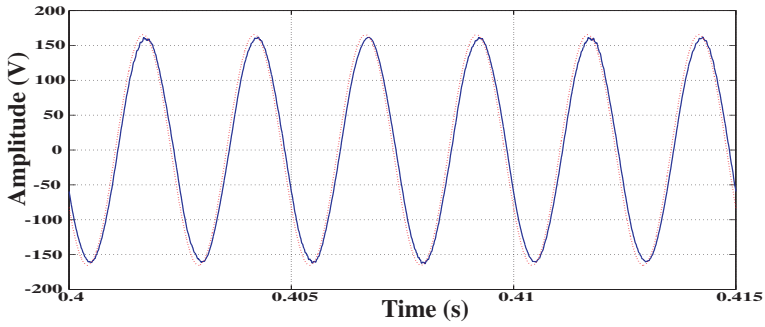


Figure 3.31: Output voltage in phase c compared to the reference signal when tracking controller is used.

For simulation purposes, some values are proposed.

Matlab/Simulink were used for the design of the Repetitive Controller. First, the number of sample k in a period of the output signal is calculated. Since the frequency of the output is 400Hz and the sampling frequency is 12.8kHz, the value of k is 32. This will be explained later, but it should be noted that the Repetitive Control is more effective when the value of k is high.

The Repetitive Control reduces the distortion caused in the output of a system by periodic errors or disturbances. This controller works by adding some signals to the reference in order to compensate the disturbances in the output. Between the two selected configurations one has proved to be the most effective and it is going to be employed in the following of this work. The configuration of the Repetitive Controller is shown in Figure 3.32. This configuration will be implemented using the digital signal processor.

In the design of a Repetitive Controller several parameters need to be taken in account. One of the most important parameter is k (the number of samples taken in each reference period); this parameter is used for calculating the values of the delays required in the pre-delay filter and also in the post-delay filter. The design of the compensator depends on the frequency response of the transfer function of the system, which will be compensated.

Some plots are obtained in order to compare the output voltage of the system with

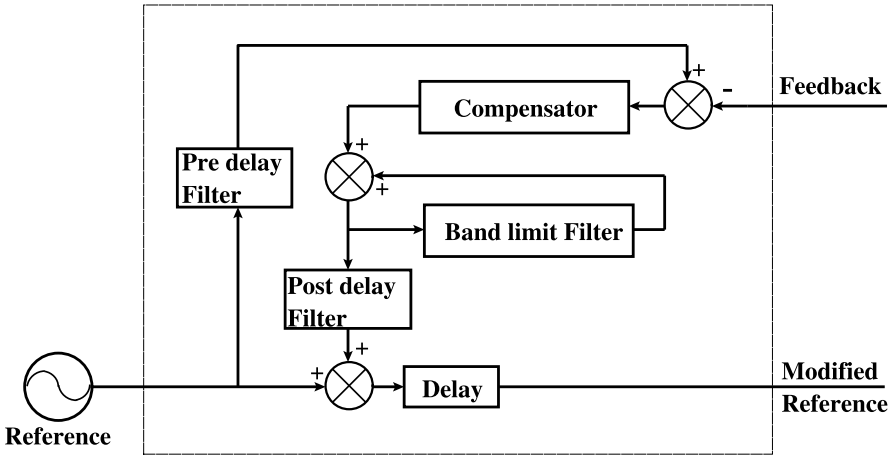


Figure 3.32: Structure of Repetitive Controller.

the Repetitive Controller and the output voltage without it. Plots for different values of N and M were also obtained in order to compare the performance of the Repetitive Controller.

The repetitive Controller consists of four fundamental components: compensator, band-limit filter, pre-delay filter and post-delay filter.

As already mentioned the variable k is defined as the number of samples in one period of the output waveform. The output signal has a frequency of 400Hz and the sampling frequency is 12.8kHz.

k is calculated as,

$$k = \frac{sampling frequency}{output frequency} = \frac{12800}{400} = 32 \tag{3.35}$$

The compensator is designed as a second order low-pass filter. The cut-off frequency of the compensator is set at 1800Hz. This cut-off frequency must be enough to allow the filter to pass the frequencies below 1800Hz. Frequencies higher that 1800Hz are considered as noise and not as harmonic distortion of the output waveform to be compensated. The frequencies affecting the output waveform are in the range 50Hz to 1800Hz. In fact, the most significant distortion frequency produced by the Matrix

Converter modulation is around 1200Hz. This frequency must be considered as the frequency of the distortion signal or error and it must be used as the signal to be compensated by the Repetitive Controller.

The compensator has the following expression,

$$\frac{0.1072z^2 + 0.2145z + 0.1072}{z^2 - 0.8845z + 0.3135} \tag{3.36}$$

The band-limit filter is a polynomial expressed as,

$$Q(z^{-1})z^{-k} \tag{3.37}$$

The most simple form of $Q(z^{-1})$ is a constant. The constant must be less that unity to assure convergence otherwise the Repetitive Controller becomes unstable and the signal tends to increase its previous value in each period of the repetitive loop up to infinity.

The proposed value of the band-limit filter is,

$$Q(z^{-1}) = 0.95 \tag{3.38}$$

Which is found empirically to give the best results.

The pre-delay filter is used to delay the original reference signal in order to put it in phase with the feedback signal. This action is needed to obtain the actual error between the output waveform and the reference signal.

The pre-delay filter is designed as,

$$\alpha \cdot z^{-N} \tag{3.39}$$

N is the number of delay steps needed to be applied to the reference signal in order to delay and compared it to the feedback signal. The value of α is a constant and

chosen to a value of 1; after simulation analysis in Matlab/Simulink and using trial and error the value of N is chosen as 1.

$$\alpha \cdot z^{-N} = 1 \cdot z^{-1} \tag{3.40}$$

The post-delay filter is used to delay the new signal generated by the repetitive loop. This generated signal is added to the original reference signal. The original signal is modified in order to compensate the distortion or errors in the output signal.

The post-delay filter has the following expression,

$$\beta \cdot z^{-M} \tag{3.41}$$

The value of β is chosen as 0.055 and M is chosen as 5. These values are found by trial and error using Matlab/Simulink. The signal generated by the repetitive loop must be in phase with the original referenced signal in order to be added, therefore the new signal generated must be delayed and the value of M=5 meets this strict requirement.

$$\beta \cdot z^{-M} = 0.055 \cdot z^{-5} \tag{3.42}$$

The final configuration of the Repetitive Controller is shown in Figure 3.33. The overall structure of the control proposed in the ABC reference frame can be seen in Figure 3.34 where the Repetitive Control scheme is repeated identically on each phase.

Figure 3.35 shows the output waveform of the voltage obtained in phases a, b and c when the configuration of Repetitive Controller shown in Figure 3.34 is employed and the Matrix Converter system is connected to a perfectly balanced load. Also, a good performance of the Repetitive Control is achieved when an unbalanced load is connected to the Matrix Converter system.

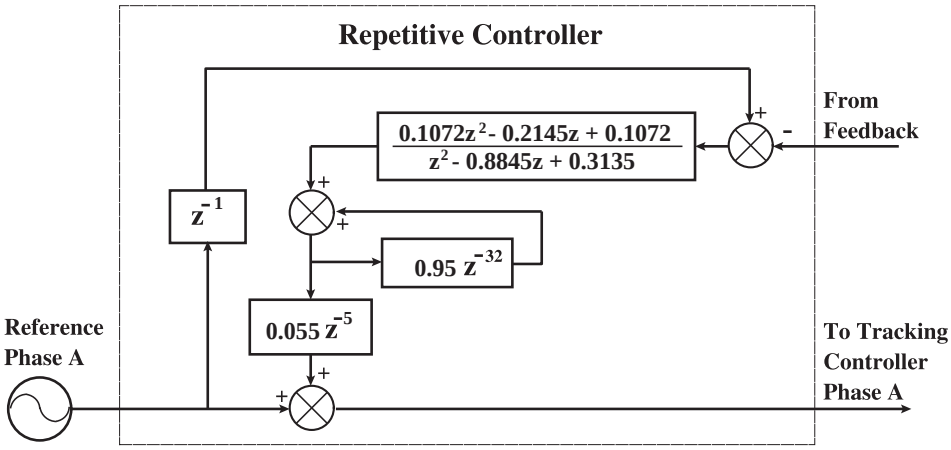


Figure 3.33: Diagram of the Repetitive Controller proposed.

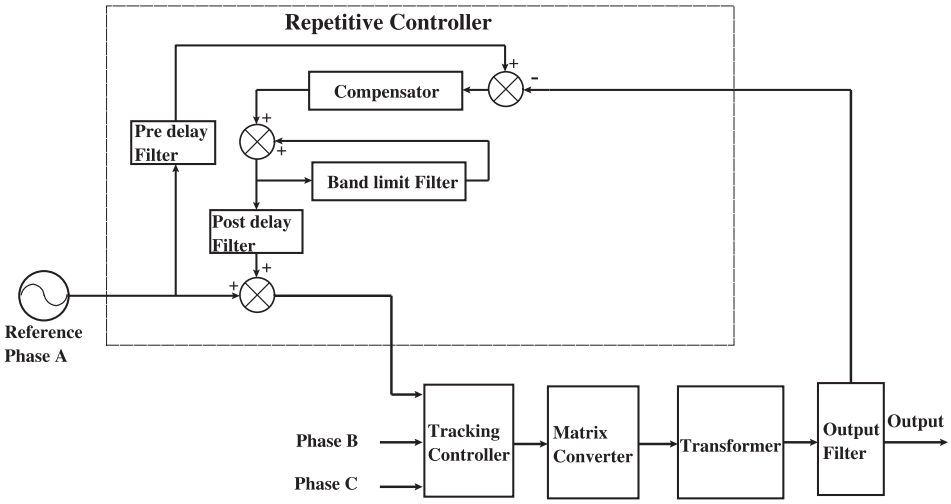


Figure 3.34: Overall diagram of the control structure proposed in ABC reference frame.

The tracking controller plus Repetitive Controller structure follows and compensates the errors produced in the output voltage waveform. The unbalanced load conditions do not affect the performance of the control strategy because each phase has its own controller structure. The controller in each phase works independently of others phases and consequently the unbalanced load conditions are not considered in any reference frame transformation. These results can be seen in Figure 3.36. Using the $d-q$ reference frame the third harmonic appears with a high value when an unbalanced load is connected. This harmonic represents 18.7% of the fundamental component. Also, the amplitude of the output voltage is increased up to 153.31Vrms.

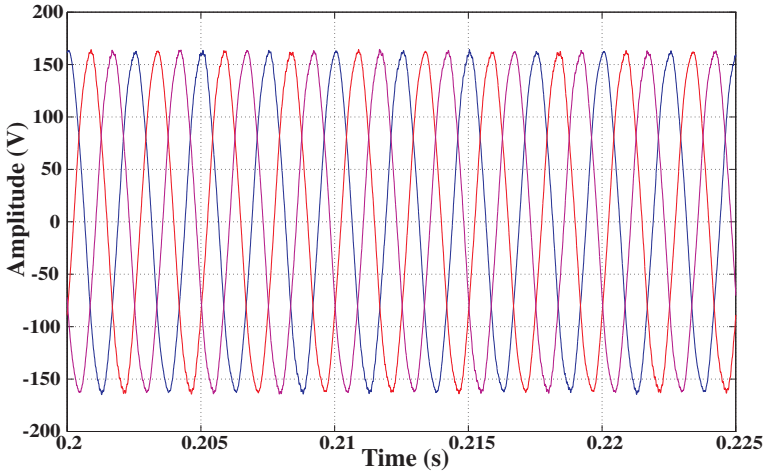


Figure 3.35: Output voltage in all phases using tracking controller plus repetitive controller. A perfectly balanced load is connected.

According to requirements imposed, the amplitude must be 165Vrms ±3V. Using the tracking controller plus the Repetitive Controller in the ABC reference frame, the output voltage in each phase is controlled and its amplitude is 115.97Vrms, which meets the requirements imposed in the design. The third harmonic is only 4% of the fundamental component.

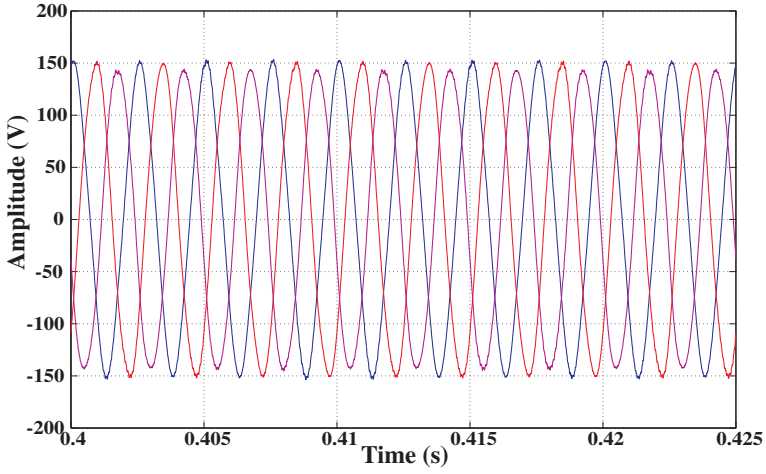


Figure 3.36: Output voltage in all phases using tracking controller plus repetitive controller. An unbalanced load is connected.

Finally, the Matrix Converter system is simulated with load disconnected. One again the performance of the control structure proposed is excellent. As it can be seen in Figure 3.37 all three-phase output voltage waveforms are sinusoidal as expected.

The output voltage waveforms obtained have also less harmonic distortion than those obtained without the Repetitive Controller. The advantage of using the Repetitive Controller is clearly seen. The amplitude of the output voltage in phase a is 116.91Vrms with a THD of 2.27%. The third harmonic does not appears, the fifth harmonic component has a value of 0.54% of the fundamental component.

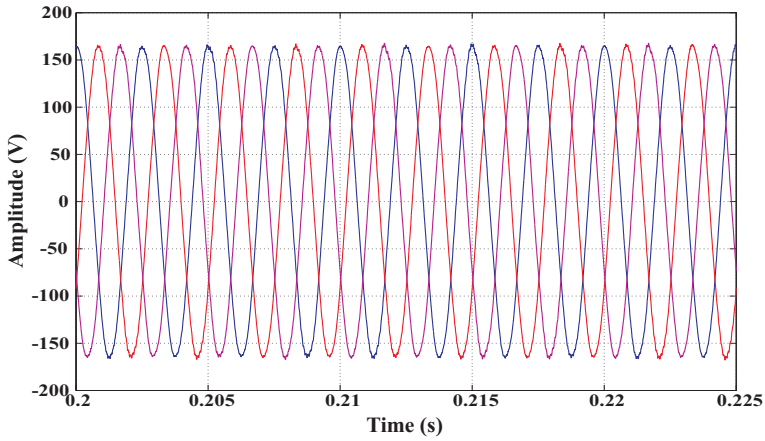


Figure 3.37: Output voltage in all phases using tracking controller plus repetitive controller. Load is disconnected.

3.7 Summary

The analysis of two different control strategies has been carried out to investigate the most appropriate topology of the control system for the application described in this study, the Matrix Converter for frequency changing power supply applications. Different load conditions has been studied in simulation. These loads are driven by the Matrix Converter system and for each of the load conditions the two control strategies have been tested. The aim was to highlight their advantages and disadvantages with the prospect of real implementation in order to optimize the design of the control system. The choice of the control strategy implemented is mainly dependent on the operative conditions.

The technical specifications and operative conditions were presented. A brief comparative review of both package software Matlab/Simulink and Saber was mentioned.

The comparison of results between Matlab/Simulink and Saber was discussed. The design of the input and output filter was carried output by using Matlab/Simulink software package. A system plant transfer function is derived and used to design the tracking controller. Bode plots are used to find the most suitable values for the tracking controller parameters. A control strategy in d-q reference frame is presented. This control topology has the disadvantage of not working properly when an unbalanced load is connected to the Matrix Converter system. This problem is solved by using a control strategy in ABC reference frame with a structure consisting of a tracking controller and a Repetitive Controller. The tracking controller is used to follow or track the reference signal and the Repetitive Controller is employed to eliminate or attenuate the distortion in the output voltage signal produced by the Matrix Converter modulation and steady state errors generated in the output voltage waveform for the controller limited bandwidth. The design of the Repetitive Controller was reviewed and values for its components were proposed.

The different load conditions simulated and presented in this chapter can be summarized as:

- **Simulation of Matrix Converter power supply connected to a Balanced Load**. Total power is 7.5kW, power is distributed equally between all phases.
- **Simulation of Matrix Converter power supply connected to an Unbalanced Load**. Output phase a connected to 140% of nominal load, output phase b connected to 100% of nominal load and output phase c connected to 60% of nominal load.
- **Simulation of Matrix Converter power supply with Load Disconnected**. This is the worst case in term of controlling the output voltage. In this an abnormal condition of instant disconnection of full load, the Matrix Converter system is required to keep the same level of the output voltage, with a very small voltage overshoot.

Chapter 4

Matrix Converter Implementation

4.1 Introduction

Chapter 3 presented simulation results from the Matrix Converter system using Saber and Matlab/Simulink software packages. These simulations have helped to analyze and investigate the design of the power converter. It is necessary to validate, experimentally, the power converter controls proposed and analyzed in previous chapters. Therefore, this chapter is dedicated to the practical implementation of the concepts presented in this thesis. To demonstrate the viability of the work, the design and construction a 7.5kVA laboratory prototype will be presented.

In this chapter the structure of the prototype converter is presented. The design parameters of this prototype are those from the design presented in Chapter 3. This is followed by the detail design of various circuits used in the prototype. These circuits include the power plane, the gate drives, the control platform, the data acquisition system and the measurement board. Test results will be presented in Chapter 5.

4.2 Overview of prototype converter

A simplified representation of the Matrix Converter system is shown in Figure 4.1. The Matrix Converter drives a resistive-inductive load which is connected to the Matrix Converter after the output filter. The load applied to the Matrix Converter system will decrease linearly from 7.5kVA to a minimum load of zero. The maximum voltage and frequency required for the system is 117Vrms and 400Hz respectively.

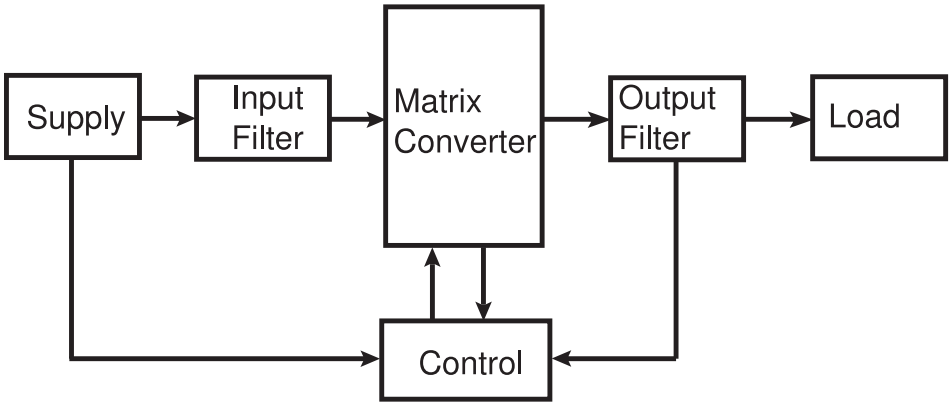


Figure 4.1: Schematic of the rig.

In the abnormal condition of instant disconnection of full load, the Matrix Converter system is required to keep the same level of 117Vrms at 400Hz, with a very small voltage overshoot. This is the worst case in terms of controlling the output voltage since the controller must be able to maintain the voltage across the output filter capacitor. In the zero output power case the power drawn by the power converter from the supply is minimal because no current is flowing through the load.

The power electronic components used in the implementation of the Matrix Converter need to be optimized in terms of the volume because one of the aims in the design of the power converter is to reduce its size. The following sections will describe the design and construction of the Matrix Converter.

The specification for this project was to develop a Matrix Converter system capable

of delivering 10kVA. Due to the availability of silicon components on the market, the power circuit of the converter was built as a 7.5kVA Matrix Converter system. The power converter had to address not only the electrical specifications but also requirements linked to the nature of the application. Because of the compact size required by the application, the space used has been optimized and special care has been taken in the choice of passive components. Indeed, no electrolytic capacitors have been used for either the input filter or the protection circuit. The performance of the power converter, as will be shown later in Chapter 5, confirms the validity of the design and compactness of the power converter. The main elements of the power converter circuit are described in the following sections and include the power modules and low inductance power plane which allow the input power connections to be connected to the inputs of the power modules, the IGBT gate drive boards and the active over-voltage clamp circuit.

A block diagram of the Matrix Converter implementation is shown in Figure 4.2. This structure can be divided in four sub-structures, which are the power circuit, the control platform, the measurement circuit and the gate driver. In this diagram, blocks shadowed indicate the boards that were designed previously in the PEMC group of the University of Nottingham. These boards have been used in previous prototypes in the laboratory and they worked well. They were not redesigned to use them in this implementation, they were only populated.

The control platform used in this laboratory prototype consists of a digital signal processor (DSP) and an field programmable gate array (FPGA) board, which interactively interface to each other. The DSP is used to performance all calculations necessary for the power converter modulation and control. The FPGA board is used to handle all logic tasks such as four-step commutation, analogue-to-digital conversion (A/D) and so on.

The input data required by the control platform is supplied from the measurement board. This data includes the input voltages, output current and output voltages. Besides that, the control platform also needs to know the direction of the input

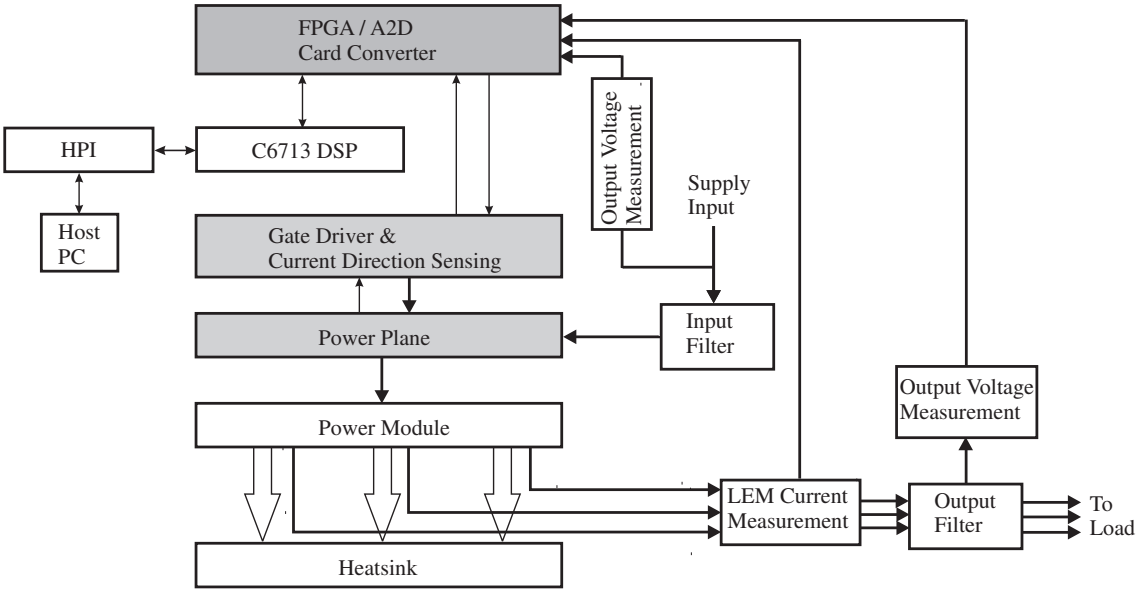


Figure 4.2: Diagram of the Matrix Converter implementation.

currents in order to control the current commutation for switching devices. To fulfil these requirements, the measurement board consists transducers which are needed for the voltage and current measurement.

The output signals, which result from the calculation performed by the control platform, are switching control signals. These signals are eventually sent to the gate driver board so that they can be used to gate the switching devices on the power plane.

4.3 Matrix Converter Power Circuit

The power circuit consist of the input filter, the power plane, the bi-directional switches and the output filter. The power plane is used to link all switching devices in order to establish a switching matrix with the nine bi-directional switches as required. The three-phase input filter and the output filter are connected to the

input and output sides of the power plane respectively.

4.3.1 Power Module

The central part of the power circuit of a Matrix Converter are the bi-directional switches. Therefore, a bi-directional switch needs to be built up with devices that are commercially available. Based on common IGBTs and fast diodes there are different possible switch layouts as explained in Section 2.4. These layouts of bi-directional switches can be made in a simple package, which is known as the power module. The power module used for the implementation of this Matrix Converter is manufactured by Eupec [55]. The model of the module is FM35R12KE3. This power module has a nominal collector emitter voltage of 1200V and a DC collector current of 35A at 80° of temperature. Figure 4.3 shows the schematic of the power module [55].

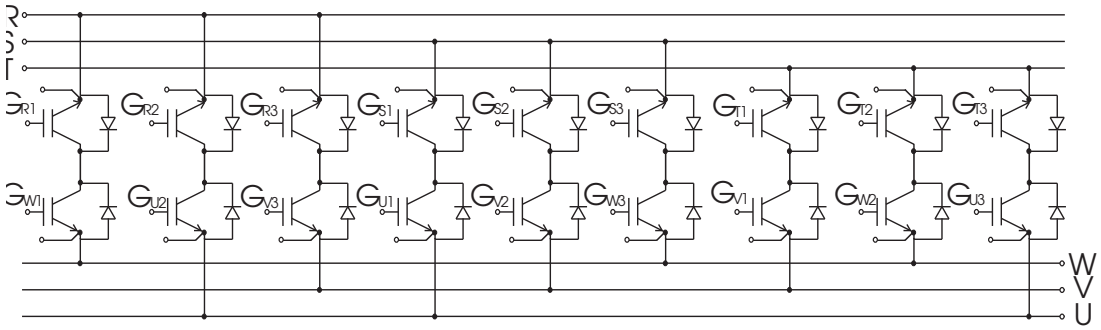


Figure 4.3: Diagram of the power module.

As it can be seen in Figure 4.3, the power module has the common collector configuration. A power stage of a Matrix Converter using the common collector configuration for the bi-directional switches can be built up with only six independent levels of common emitter potential. A power stage based on common emitter configuration of bi-directional switches uses nine independent potentials for the common emitters. This is critical not only in terms of isolation distance between such independent potentials, but also because for the gate drive unit of IGBTs an isolated voltage source is required for each emitter potential. In case of common collector configuration this

adds up to six, a common emitter based power stage would need nine of these. A photograph of the power module is shown in Figure 4.4

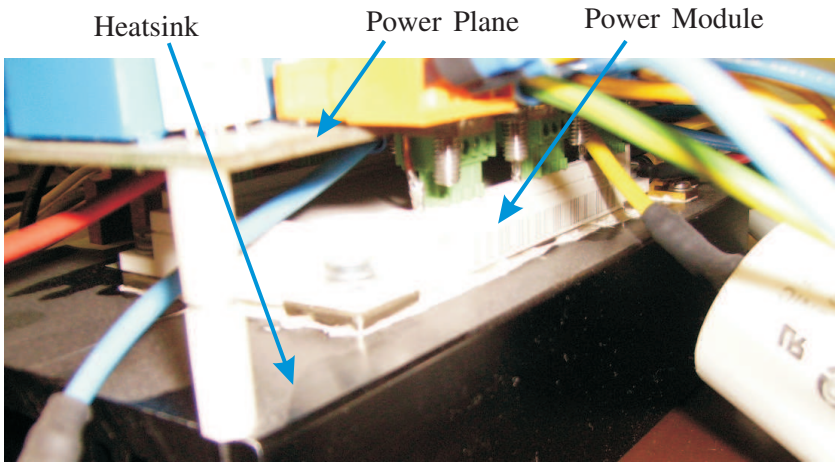


Figure 4.4: Photograph of the power module.

4.3.2 Power Plane

It was decided to use standard double-sided printed-circuit board (PCB) for the implementation of the power plane. The input and output terminals of the power converter were built directly on the PCB so that connections can be made using brass nuts and bolts. The power module was soldered directly to the PCB and then mounted onto the heatsink, which has natural convention cooling. The heatsink has a thermal resistance of 0.42°C/W and is made of aluminium with a surface finished of black anodised. Its external dimensions are 125mm, 200mm and 50mm for width, depth and length respectively. The total power dissipation of the power module is 200W under normal conditions of operation at 25°C.

The Matrix Converter consists of one power module containing nine bi-directional switches connected to form a three-phase input three-phase output Matrix Converter. The power module is rated at 35A and 1200V which means that the Matrix Converter implemented could easily drive systems up to 7.5kVA from a 415V three phase input

supply.

4.3.3 Gate Drive Circuit

The gate drives have been designed to optimize their functionality and to fit in the space available on and around the power module. These circuits have been implemented on a single printed circuit board (PCB), described from now on as the gate drive board.

The voltage and current signals provided by the Digital Signal Processor (DSP) are not capable of turning the high power switching devices on and off unless adequately interfaced according to the device's requirements. A gate drive circuit is therefore required.

The gate drive serve two purposes. Firstly, it provides the isolation between the control (low power) and the power circuit (high power). Secondly, the gate drive provides the power to drive the switching devices, such as the IGBT in the power module, from the control signal (normally low power). The gate drive circuit fulfills this requirement by providing +15V between gate and emitter of the IGBTs to switch the device ON when the digital signal is HIGH and -15V between gate and emitter of the IGBTs to switch the device OFF when the digital signal is LOW. This is achieved through the use of HCPL3120 (2.0 Amp Output Current IGBTs Gate Drive Optocoupler) which has a drive capability for IGBTs and also provides electrical isolation for the control signal.

Power supply isolation between the ground of the 5V control electronics supply and the local signal references is provided by dc to dc converters which generate isolated $\pm$5V and $\pm$15 V from the 5V supply. For the gate driver circuit a Texas Instrument DCP020515DU was chosen especially for its flexibility. It is a 2W DC-DC converter with a maximum 1kV isolation potential with the possibility of being directly connected in parallel with another if higher power is required.

Also placed near the power module there are three separate current direction detectors, each for a single phase. These circuits are used to detect the current direction information, which is fed back to the FPGA to carry out a safe commutation of the IGBTs. The voltage across the two anti-parallel diodes caused by positive or negative load current provides the information on the direction of the output current. The 30CTQ045S Schottky diodes with nominal average forward current of 30A and a low voltage drop of 0.56V were used to convert current into voltage signal with low additional power loss. The diode voltage is then convert into a logic signal by using a comparator circuit (LM311M). The comparator output drives the opto-coupler (HCPL-0601), whose logic output provides the information on the output current direction to the control platform (FPGA board).

The communication to and from the FPGA is done via a planar cable interfaced with the appropriate connectors to provide both voltage isolation and good noise immunity. The signals from the voltage across the anti-parallel diodes is transmitting to the comparator in the gate driver board by a coaxial cable. As mentioned previously, the gate drive board has been optimized in size to be able to use the space above the power module between the signal connections and the input and output power connections. The aim is a more compact arrangement of the whole power circuit together with the FPGA board, as will be shown later in the description of the assembly of the prototype matrix converter.

Photographs of the top and bottom views of the gate driver boards are shown in Figures 4.5 and 4.6.

4.3.4 Output Filter

The output filter is used to filter the output voltage of the Matrix Converter and produce a sinusoidal waveform. This is done by attenuating or eliminating the harmonic content and the ripple that appear in the output waveform. The voltage across the output filter capacitors is used as the feedback signal employed by the controller to

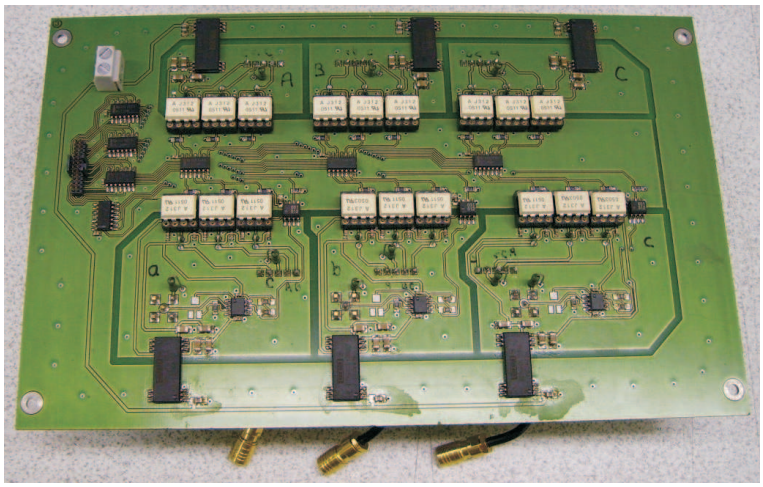


Figure 4.5: Photograph of the gate driver, top view.

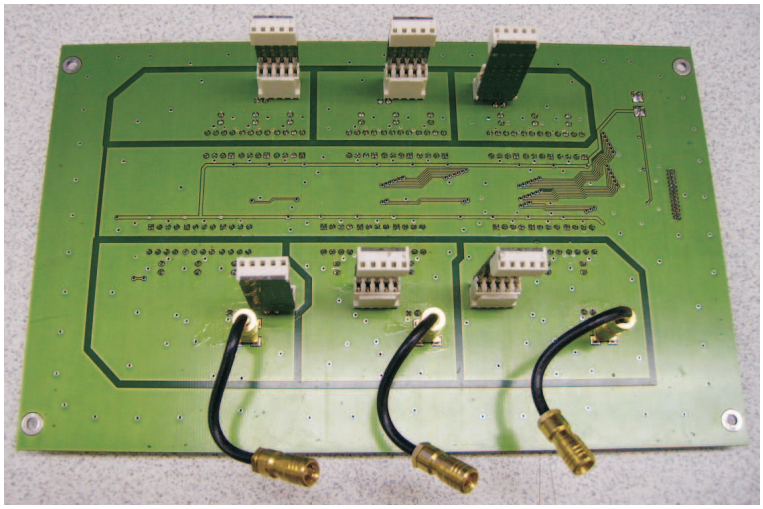


Figure 4.6: Photograph of the gate driver, bottom view.

control the output voltage.

Figure 4.7 shows the schematic diagram of the output filter. Values of components of output filter were calculated in section 3.4.2.

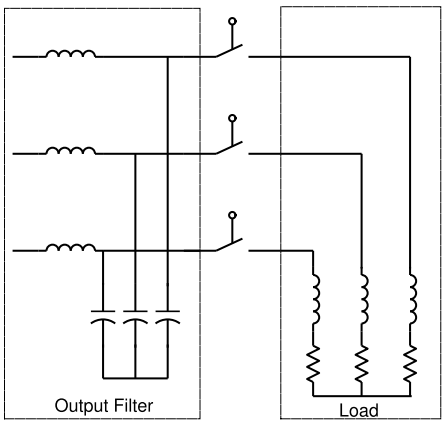


Figure 4.7: Schematic diagram of the output filter.

Capacitors of the output filter have the following specifications:

- Capacitance: 68μF
- Tolerance: 5%
- Nominal voltage: 175Vrms AC
- Dissipation factor: <0.001 at 1kHz and 20±3°
- RMS current rating: typically 50A - 100A at 400Hz
- Temperature range: -55° to +100°
- Material: Metallized polypropylene

Figure 4.8 shows the capacitors used in the implementation of the output filter.

The inductor of the output filter have the following specification:

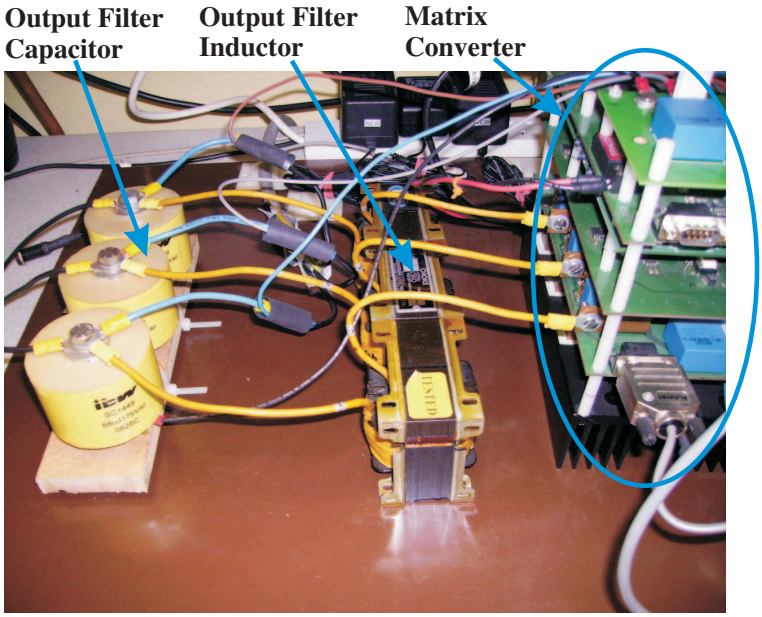


Figure 4.8: Photograph of the output filter.

- Inductance: 128μH
- Nominal voltage: 117Vrms
- Nominal current: 25Arms
- Frequency: 400Hz

4.3.5 Input Filter

The input filter is used to attenuate the harmonics injected to the three phase power supply (mains). These harmonics are generated by the modulator of Matrix Converter. The switching frequency used by the modulator to generate the modulation pulses produces harmonics. These harmonics provoke distortion of the waveform of the input currents.

Figure 4.9 shows the schematic diagram of the input filter. Values of component of

input filter were calculated in Section 3.4.3.

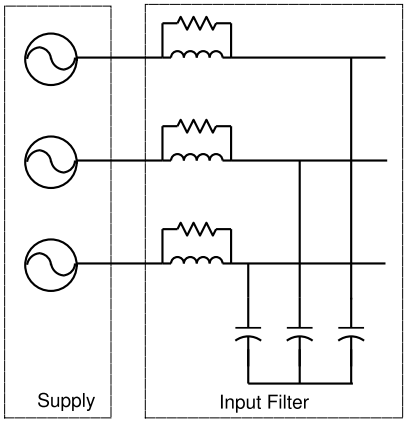


Figure 4.9: Schematic diagram of the input filter.

Capacitors for the input filter have the following specification:

- Capacitance: 26μH
- Tolerance: 3%
- Nominal voltage: 300Vrms AC at 60Hz
- Dissipation factor (maximum): <0.1 at 120Hz and 25°
- RMS current rating: 28.2A at 25° and 50Hz
- Temperature range: -55° to +85°
- Material: Polypropylene

The inductor of the input filter have the following specifications:

- Inductance: 700μH
- Nominal voltage: 220Vrms

- Nominal current: 8Arms
- Frequency: 50Hz

A parallel damped single section filter configuration [71] [90], was chosen for this application, as shown in Figure 4.9. A resistor is placed in parallel with the inductor to provide appropriate damping. A very small value of R would result in a high degree of damping but a higher dissipation of energy, a 56Ω resistor was chosen for this power converter.

The input filter was designed by choosing C first, its size, type and ratings being based on the application. As mentioned earlier metallized polypropylene capacitors have been used and a total of 8.666μF capacitance per line to line (2μF line to line plus 20μF line to neutral, equivalent to 26μF) was chosen.

Figure 4.10 shows a photographs of the input filter implemented.

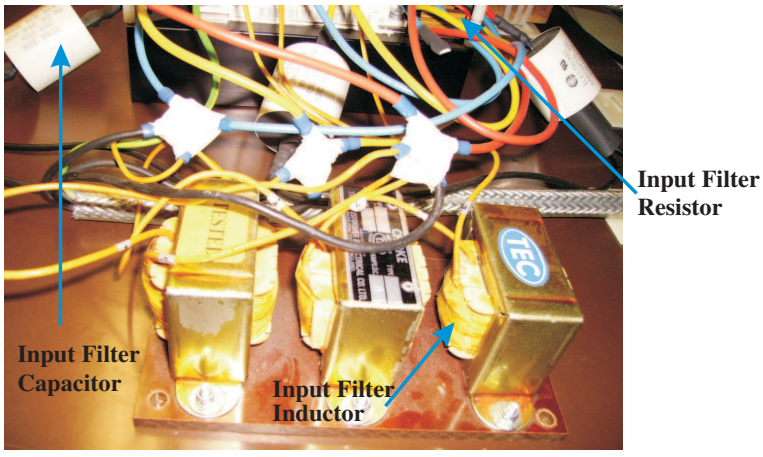


Figure 4.10: Photograph of the input filter.

4.3.6 Measurement Boards

The input data required by the control platform is supplied from the measurement boards. This data includes the line to line input voltages, the three output currents and the output voltages. The measurement boards consists of transducers which are needed for voltage and current measurements and signal conditioning circuits.

The current transducers used in the output of the Matrix Converter are the LAH 25-NP manufactured by LEM [91]. These transducers are used to measure all three instantaneous output currents. The LAH 25-NP has a maximum current handling capability of 25A, a conversion ratio of 1:1000 and a bandwidth of 200kHz. This transducer uses the Hall effect. The transducer has a galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit). The current transducer is supplied by ±15V, supplied from FPGA board. The output of all the LEM transducers is a current signal for a better noise immunity when transferring this information to the control platform. The output of the LAH 25-NP is loaded with a measuring resistor. This measuring resistor should be of high precision and should match the signal to an input range of the analogue input hardware located in the FPGA board. Moreover the value of the resistor must be taken into account regarding the range of measured current. The output current resulting from the secondary current flowing through the measuring resistance is then sent to the analogue to digital converters in the FPGA board.

The maximum value of current allowed in the output of the converter is set up in the DSP program. With a limit on the current in each output phase, the Matrix Converter is protected against overcurrent. In the event of an overcurrent condition, the DSP automatically shuts down the system.

The voltage transducers are used to measure the input voltages and the voltage of the clamp circuit. A PCB has been designed to measure the output voltages across the capacitors in the output filter. The voltage transducers used are LV25-P model manufactured by LEM. The transducer is supplied by a ±15V power supply. For

the voltage measurement, a current proportional to the measured voltage must be passed through an external resistor which in chosen according to the application and installed in series with the primary circuit of the transducer. The output voltage measurement is similar to that of the input voltage. For the input voltage only two voltage transducers are used. These line to line voltages are measured and then converted into three-phase voltages using the appropriated transformations. For the output voltage measurement, three voltage transducers are used. This is because the system will work under unbalanced load conditions and the three voltage needed to be taken separately. The control strategy is implemented in the ABC reference frame. The voltage transducers boards are shown in Figure 4.11.

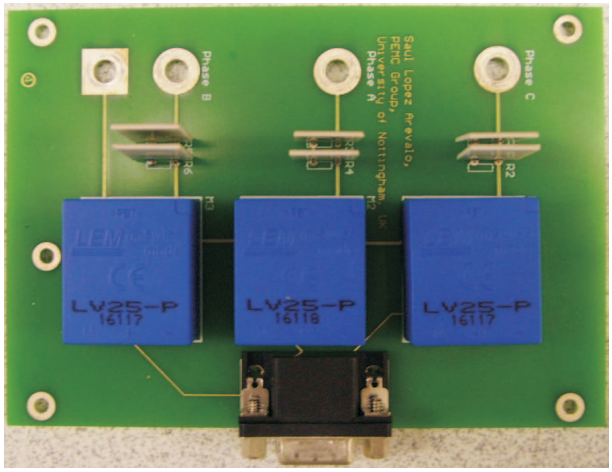


Figure 4.11: Photograph of the voltage transducers.

4.4 Matrix Converter Control Implementation

The modulation and control of the Matrix Converter is implemented using a Digital Signal Processor(DSP)/Field Programmable Gate Array(FPGA) based controller interfaced. This interface consists of a series of circuits which allow information such as gate drive signals and feedback measurement signals to be transferred to and from the controller boards. A block diagram of the overall control structure implemented

is shown in Figure 4.12.

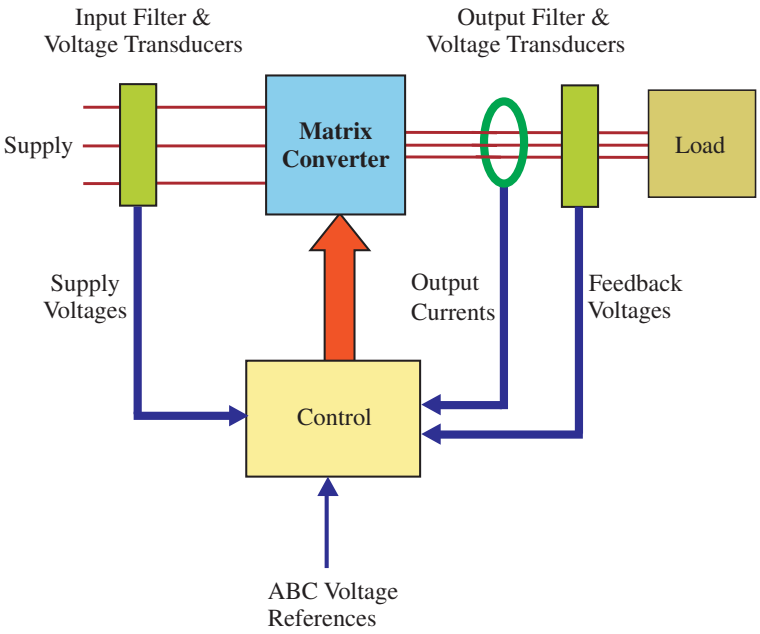


Figure 4.12: Diagram to show the overall control structure.

The voltage control loop of the Matrix Converter system is implemented in the DSP which requires information on the input phase voltages and output phase voltage feedbacks as well as the output current of the Matrix Converter. The signals are provided by the voltage and current transducers and are fed to a series of A/D channels on the FPGA board. The digitized information is then transferred to the DSP via the FPGA using an external memory interface. The DSP processes the information and demands the correspondent output voltages to achieve the desired control which is then executed by the FPGA through the appropriate sequence of gate drive signals. The gate drive signals are transferred from the FPGA to the gate drive board via a planar cable. The following sections will explain in more details the implementation of the control structure at a lower level.

4.4.1 Digital Signal Processor

The Digital Signal Processor (DSP) employed in this application was the TMS320C6713 manufactured by Texas Instruments. This DSP is available as a starter kit, known as the DSK C6713. This starter kit was used for the control platform to reduce development time. The general structure of the DSK C7613 is shown in Figure 4.13.

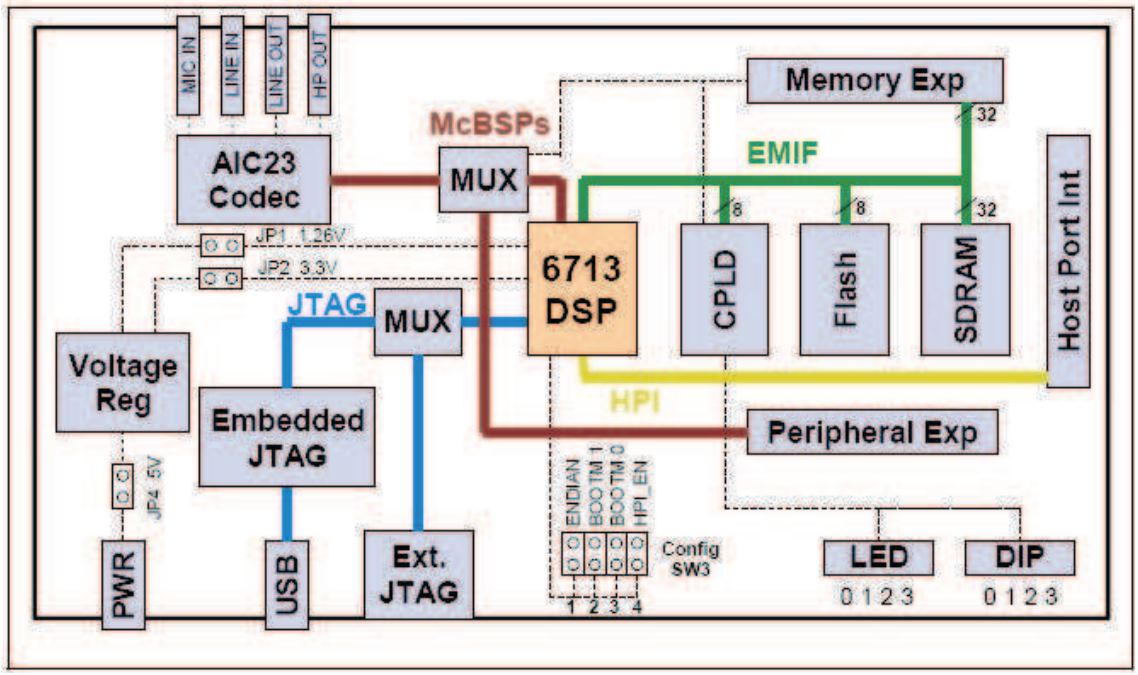


Figure 4.13: Structure of the DSK C6713.

A fast and effective control of the power converter has been achieved using the DSP Starter Kit (DSK) which, with its Host Port Interface (HPI) daughtercard, allows the user to fulfil the specific application and connects the controller to a host computer for development and control purposes. The DSK C6713 is a versatile kit with a high speed floating point processor which runs at 225MHz and can perform up to 1800 millions instructions per second. One of the major advantages of employing the DSK C6713 is linked to its peripherals and the ability to add external peripherals. Above all the External Memory Interface (EMIF) which not only supports 64MB of on board SDRAM memory, Flash ROM, I/O port but also expands the memory

interface through an expansion memory interface connector for a daughter board.

The DSP has four dedicated address spaces which allow both the on-board devices and the expansion memory interface to be selected individually without conflict. The expansion memory interface connector is mapped into the DSP's chip enable two (CE2) and chip enable three (CE3) address space. Only one of the two memory space enables (CE2) has been used in this application because only one daughter board was implemented, the FPGA card. All of the accesses to the EMIF are clocked at 100MHz while the CPU is clocked at 225MHz.

The HPI daughtercard mounted in the DSK incorporates a connection to the Host Port Interface (HPI) of the C6713. The HPI daughtercard is a high speed data card which allows a host to access the internal memory of the C6713 without interrupting the central processing unit (CPU) of the DSP. This allows a bi-directional data transfer between the host PC and the DSP to control the converter and download sampled variables. The HPI daughtercard also provides access to an embedded JTAG emulator for source code debugging.

A bottom view of the HPI of the HPI daughtercard is shown in Figure 4.14.

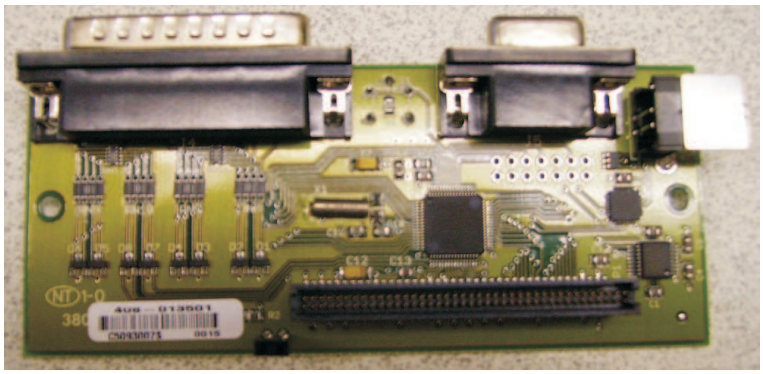


Figure 4.14: Host port Interface (HPI) daughtercard.

Figure 4.15 shows a view of the DSP used in the implementation of the Matrix Converter system.

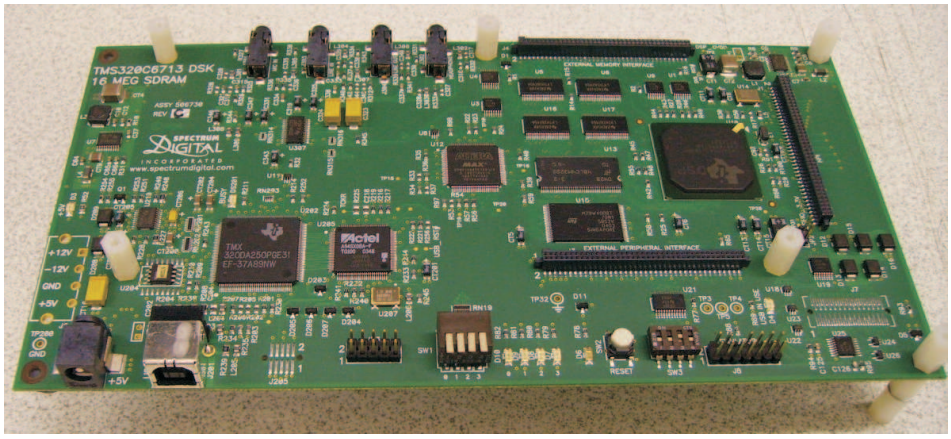


Figure 4.15: Photograph of the Digital Signal Processor (DSP).

4.4.2 Field Programmable Gate Array

The FPGA card represents not only a possibility to expand the functionality of the DSP using the memory mapped interface of the FPGA itself, but also provides the DSK with more interface circuitry and allows the analogue to digital (A/D) conversion of all the measured analogue signals. The FPGA card was developed by the PEMC group at the University of Nottingham [92]. This board has proved to be a very flexible and versatile card in many applications. The board contains a total of nine, 12-bit A/D channels which are employed for this application as follows:

- ×**3** Output currents
- ×**2** Input voltages
- ×**3** Output voltages

It also provides for four D/A conversion channels, hardware comparators for overcurrent protection and digital I/O capabilities for trip information output, trip source inputs, event triggering.

The main function of the FPGA is to provide the space vector PWM generator unit and the three state machines (one for each output leg of the Matrix Converter) to correctly commutate the current between the bi-directional switches depending on the direction of the load current and the demanded switch state. A schematic diagram of the FPGA is shown in Figure 4.16. The FPGA also provides a watchdog timer, trip monitor, trip information interface and temperature sensor interface.

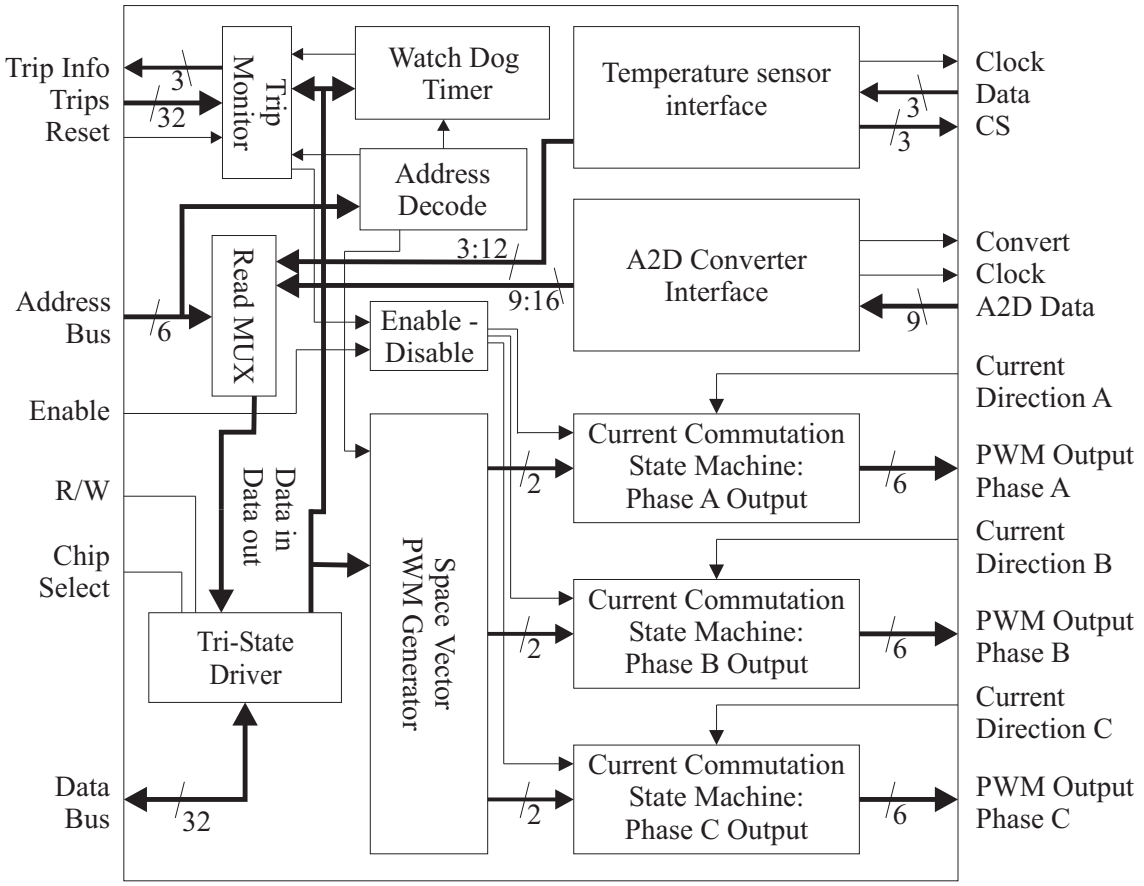


Figure 4.16: FPGA block diagram.

As mentioned previously, the FPGA also provides an interface for the nine serial A/D converter channels. Once the A/D information has been gathered by the interface, it is transferred into registers within the FPGA which are memory mapped to the DSP's memory interface. The trip monitor disables the output of the state machines if any of the hardware or software trips occur. A maximum of sixteen hardware trips and

sixteen software based trips can be used although not all are used for this application. Table 4.1 shows the trip sources used.

Hardware	**Software**
Over-current	Instantaneous over-current
PWM FIFO empty	Averaged over-current
Watchdog	Loss of supply
Resolver fail	Load over-temperature
Clamp over-voltage	Converter over-temperature
Clamp chopper fail	
28V supply fail	

Table 4.1: Hardware and software trip usage.

The output of the watchdog timer feeds directly into the trip monitor. The watchdog timer is serviced at the beginning of each control interrupt. If it is not serviced, for example if the DSP has crashed or is not functioning correctly, a trip will be generated and the converter disabled. The output voltage transducer board is located at the top of the power converter and is connected to the FPGA board through a data cable. The A/D converters within the FPGA received the signals, converter them and send them to the DSP. The data from each of the three output voltages is continually placed in memory mapped registers within the FPGA.

The source code executed by the DSP controls the Matrix Converter and its output. In the main program of the source code, after having set all the bits to prepare the external memory interface, FPGA configuration registers and PWM generator period, the main routine of the DSP enables the PWM interrupt and then waits for the interrupt to occur, after the PWM generator timer is started. The PWM generator functions as the interrupt generator for the DSP. Each time the PWM generator reaches the end of the current period, an interrupt is generated. For this application a PWM sequence time of 78.125μs was desired because the implementation of the Repetitive Controller requires to have an integer number of samples within the output period. Hence the sampling frequency for the system was set up as 12.8kHz. Using this sampling frequency, a value of 32 is obtained for the number of samples in an output period (12800Hz/400Hz).

During the interrupt routine the information from the A/D channels are extracted from the FPGA registers and manipulated so that the scaled output voltages and input line to line voltages are calculated. This information, together with the desired input current angle and the output voltage angle and magnitude is used to calculate the duty cycles implemented in the Space Vector Modulation (SVM) algorithm. Finally, using the DATA BUS in the FPGA, the space vectors calculated by the DSP are loaded into the appropriate FPGA register to allow it to perform the built in Space Vector PWM generator. The final sequence of digital signals which will drive the IGBTs is the output of the state machine for each output phase. The state machines require the output of the PWM generator and information about the current direction to perform a 4-step current direction based commutation routine. The calculated vectors will be output during the next PWM period. Figure 4.17 shows a diagram that represents the DSP functions during the interrupt routine.

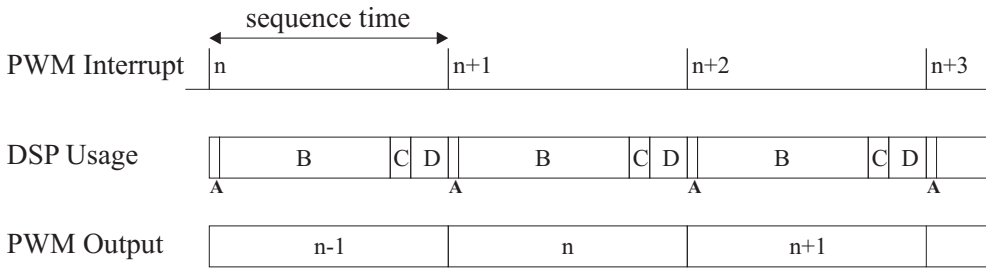


Figure 4.17: Diagram to show PWM interrupt DSP usage.

At point **A** the A/D channels are sampled and the data is moved from the FPGA to the DSP. The time period labeled **B** is used to calculate the output PWM vectors and vector times according to the space vector control algorithm. The vectors and vector times are then transferred into the PWM generator within the FPGA at point **C**. The time remaining (**D**) before the next interrupt occurs is free to be used for the communication with the host PC. The combination of the characteristics of the high speed DSP and the versatility of the FPGA allows all of the necessary controller functionality to be implemented and the control calculations can be performed at the necessary speed.

Figure 4.18 shows the top view of the FPGA board use in the implementation of the Matrix Converter system.

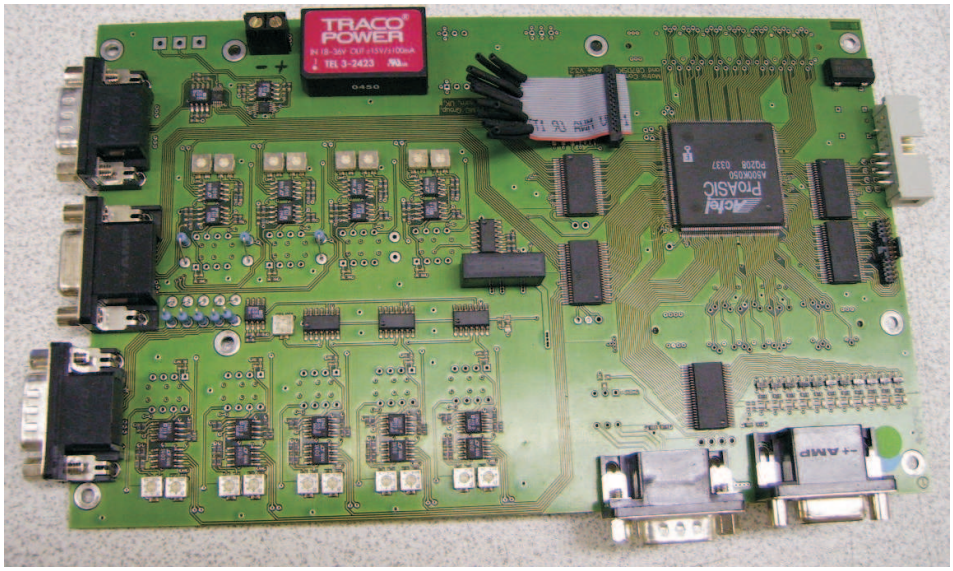


Figure 4.18: Photograph of the FPGA board, top view.

4.4.3 Host Port Interface

The Host Port Interface (HPI) daughtercard can only work with the DSK C6713. Figure 4.19 shows the HPI daughtercard mounted on the DSP.

The HPI daughtercard provides a variety of interfaces to the Host Port Interface on the DSK C6713. In its host services mode, the daughter card allows serial, parallel and USB access to the HPI port in the DSK. With this access in place, a Matlab application can be used, and also stand-alone applications can be developed to permit a PC host to download software to the DSP and then control its operation. With this advantage, an interface outside of Code Composer Studio can be implemented.

The HPI daughtercard resources can also be used by the DSP application, through a simple set of function calls that control the daughtercard in its the service mode.

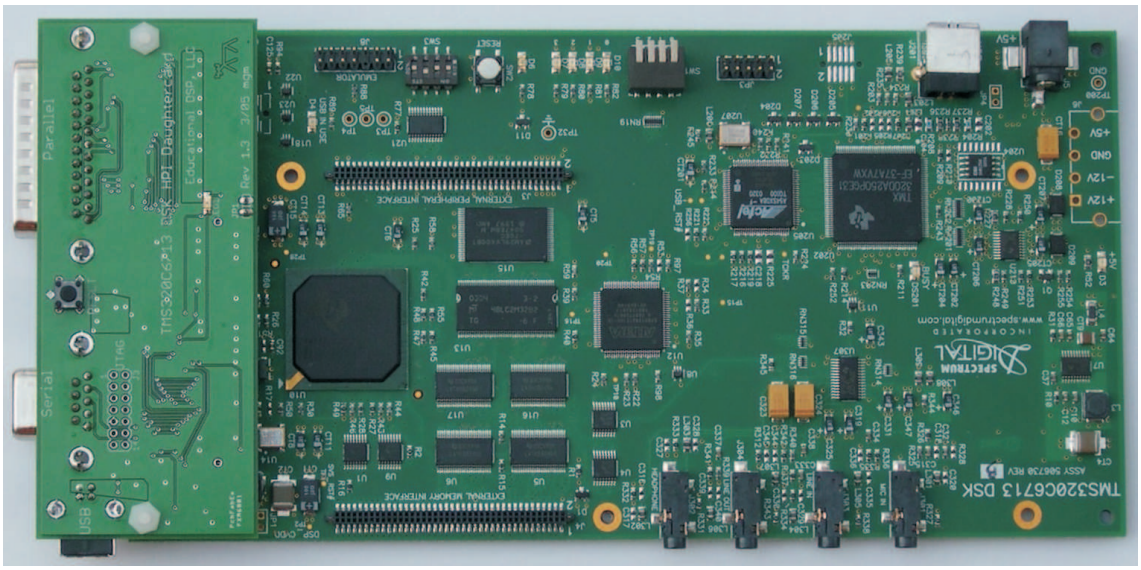


Figure 4.19: Photograph of the HPI mounted on the DSP, top view.

This feature gives a DSP application control over up to 16-bits of digital I/O with individually selectable directions, up to eight 12-bit analog inputs, and easy access to communication over the serial and USB links.

A host program in Matlab have been developed in order to monitor and control the variables used in the DSP. This host program generates a graphical interface and has been modified to adapt it to the application. These modifications include the addition of new fields to introduce the amplitude and the frequency required in the output voltage. Figure 4.20 shows the graphical interface developed in Matlab. This interface is user-friendly. The code source developed in Code Composer Studio (CCS) should be loaded into the DSP by this interface in order to set and monitor variables. The host program needs the sampling frequency at which the DSP is operating. The source code of main program implemented in the DSP can be seen in Appendix D.1. Once the prototype is turned on and the graphical interface of the host program is executing the variables displayed in the interface screen can be monitored. The level of voltage and frequency can be changed at anytime by introducing new values in the fields of output voltage and output frequency. The graphical interface displayed in

the computer when the host program is executed is shown in Figure 4.20.

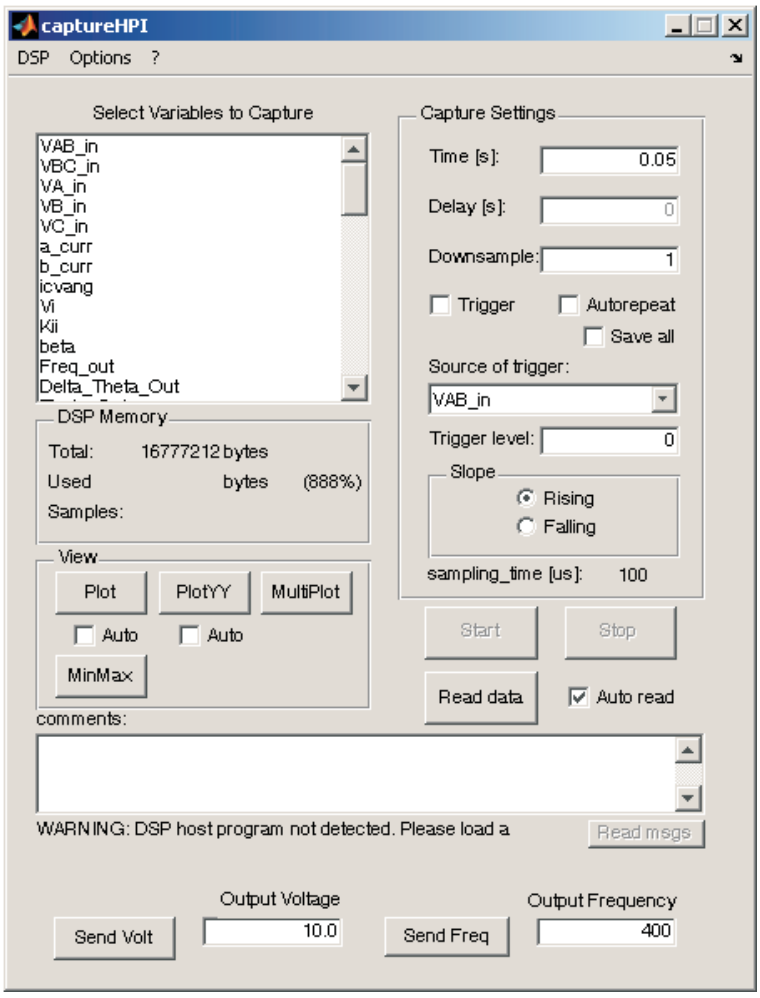


Figure 4.20: Screen from the HPI Interface in Matlab.

4.4.4 Second Order Controller

The first step in the design of a digital controller is always the implementation of a suitable data acquisition path. While signal acquisition organization is somehow implicit in analog control design, because both the plant and the controller operate in continuous time domain, digital control requires particular care in signal conditioning and analog to digital conversion implementation. The reason for this is ultimately

that, while the control signals are taken from a plant that operate in the continuous time domain, the operation of the controller takes place in the discrete time domain. Therefore, signals have to be converted from the continuous to the discrete time domain and, or course, the other way around. It is very important to be aware of the fact that not every implementation of this conversion process leads to a satisfactory controller performance. The control of the conversion noise and the avoidance of aliasing phenomena play a critical role.

The implementation of the tracking controller was done in both the d-q reference frame and the ABC reference frame. The implementation of the Repetitive Controller is only done in the ABC reference frame because all tests will be carried on using unbalanced load conditions. If d-q reference frame is used the control of the output voltage when the Matrix Converter system is operating in the unbalanced load condition cannot be achieved because the d-q to ABC transformation does not work properly. This transformation is used for the controller to provide the three-phase reference to the Matrix Converter modulator.

4.4.4.1 Implementation of Tracking Controller in the d-q Reference Frame

The design of the tracking controller has been presented in Section 3.5.

The controller to be implemented in the d-q reference frame is given by Equation 4.1

$$C(z) = 0.05 \cdot \frac{z^2 - 1.319z + 0.9699}{z^2 - 0.5001z - 0.4999} \tag{4.1}$$

Expressing as a transfer function,

$$C(z) = \frac{Y(z)}{U(z)} = 0.05 \cdot \frac{z^2 - 1.319z + 0.9699}{z^2 - 0.5001z - 0.4999} \tag{4.2}$$

Multiplying by z^{-2},

$$\frac{Y(z)}{U(z)} = 0.05 \cdot \frac{1 - 1.319z^{-1} + 0.9699z^{-2}}{1 - 0.5001z^{-1} - 0.4999z^{-2}} \tag{4.3}$$

Rearranging,

$$Y(z)[1 - 0.5001z^{-1} - 0.4999z^{-2}] = 0.05 \cdot [1 - 1.319z^{-1} + 0.9699z^{-2}]U(z) \quad (4.4)$$

$$Y(z) - 0.5001z^{-1}Y(z) - 0.4999z^{-2}Y(z) = 0.05 \cdot [U(z) - 1.319z^{-1}U(z) + 0.9699z^{-2}U(z)] \quad (4.5)$$

This yields to,

$$Y(z) = 0.5001z^{-1}Y(z) + 0.4999z^{-2}Y(z) + 0.05 \cdot [U(z) - 1.319z^{-1}U(z) + 0.9699z^{-2}U(z)] \quad (4.6)$$

Rearranging again,

$$Y(z) = 0.4999z^{-2}Y(z) + 0.5001z^{-1}Y(z) + 0.05 \cdot [0.9699z^{-2}U(z) - 1.319z^{-1}U(z) + U(z)] \quad (4.7)$$

$$Y(k) = 0.4999Y(k-2) + 0.5001Y(k-1) + 0.05 \cdot [0.9699U(k-2) - 1.319U(k-1) + U(k)] \quad (4.8)$$

Where, $U(k)$ represents the error and it is defined as,

$$U(k) = reference\ signal - feedback\ signal \quad (4.9)$$

Equation 4.8 in the one that is implemented in the DSP for each of the d-q components of the controller. Because this controller is a second order function, it has a two-step delay. Controllers represented by high order function are more complicated to implement due to the addition of extra lines in the DSP program to generated the step delays.

4.4.4.2 Implementation of Tracking Controller in the ABC Reference Frame

The implementation of the tracking controller in the ABC reference frame is quite similar to that implementation shown in the Section 4.4.4.1. The exception in this implementation is that the reference for each phase is defined as,

$$reference\ signal^* = 6 \cdot reference\ signal \quad (4.10)$$

And the controller in ABC reference frame is define by Equation 4.11,

$$0.6 \cdot \frac{z^2 - 1.319z + 0.9699}{z^2 + 0.5001z + 0.4999} \tag{4.11}$$

Considering a similar procedure as the one used for the implementation of the tracking controller in the d-q reference frame, the expression to be implemented for the ABC reference frame in the DSP is given by Equation 4.13

$$Y(z) = -0.4999z^{-2}Y(z) - 0.5001z^{-1}Y(z) + 0.6 \cdot [0.9699z^{-2}U(z) - 1.319z^{-1}U(z) + U(z)] \tag{4.12}$$

$$Y(k) = -0.4999Y(k-2) - 0.5001Y(k-1) + 0.6 \cdot [0.9699U(k-2) - 1.319U(k-1) + U(k)] \tag{4.13}$$

In the ABC reference frame the error $U(k)$ is given by Equation 4.14

$$U(k) = reference\ signal^* - feedback\ signal \tag{4.14}$$

The expression given by Equation 4.13 have to be implemented in the DSP. Because the ABC reference frame is used, the Equation 4.13 must be implemented three times, one for each phase. The source code used in the DSP for the implementation of the tracking controller can be seen in Appendix D.2.

4.4.4.3 Implementation of Repetitive Controller in the ABC Reference Frame

The implementation of the Repetitive Controller is not as easy as the tracking controller. The main problem is the implementation of the output period delay. The structure of the Repetitive Controller is shown in Figure 3.32. As it can be seen in this figure, the first task of the implementation of the Repetitive Controller is to determine the difference between the feedback signal and the actual reference. The

implementation of this task is basically very simple. One step delay is applied to the reference signal. This delay applied is called the pre-delay. The feedback signal is taken as it is produced by the voltage transducer. The second task is to implement the compensator. The compensator was design as second order low pass filter. The implementation of the a second order filter generates two step delays in the calculation of values. The implementation of this filter is very similar to that of the tracking controller. The third task is to apply the output period delay. This delay is generated by using a loop. This loop has a gain of 0.95 and a delay function of 32 steps. The loop requires 32 delays because the output period is 0.0025 sec and the sampling frequency has a value of 12.8kHz which give a sampling period of 78.125μsec. The value of number of sample in one output period, k, is calculated as,

$$k = \frac{output \quad period}{sampling \quad period} = \frac{2500\mu sec}{78.125\mu sec} = 32 samples \tag{4.15}$$

The actual cycle and the previous cycle must be in phase in order to find appropriately the differences appeared in the actual signal. Basically this is the core of the Repetitive Control: delay one cycle of the signal and compare it to the actual signal.

The fourth task is to applied a post-delay to the signal generated by the delay loop. This post-delay has five step delays and a gain of 0.055. The post-delay operation is applied in order to have both the signal generated and the reference signal in phase.

The fifth task is to find the difference between the signal generated and the actual reference signal. This new signal generated by the comparator is then amplified by a gain. This signal is called the reference modified and is applied to the tracking controller. The source code used in the DSP for the implementation of the Repetitive Controller can be seen in Appendix D.3

4.5 Summary

This chapter has presented the implementation of a 7.5kW laboratory prototype in order to verify the control strategies proposed for the power converter under investigation. The design, construction and assembly of the Matrix Converter prototype used for frequency changing power supply applications has been described in details. The power converter has been tested in the laboratory to evaluate the control performance. The final implementation of the Matrix Converter system does not employ the full potential in terms of the rated power which the Matrix Converter is capable of delivering. The Matrix Converter, rated at 7.5kVA, is only be required to delivery 117Vrms at 400Hz. The output current depends on the load conditions. The results presented in Chapter 5 have been obtained from this experimental rig. A photograph of the completed Matrix Converter system can be seen in Figure 4.21.

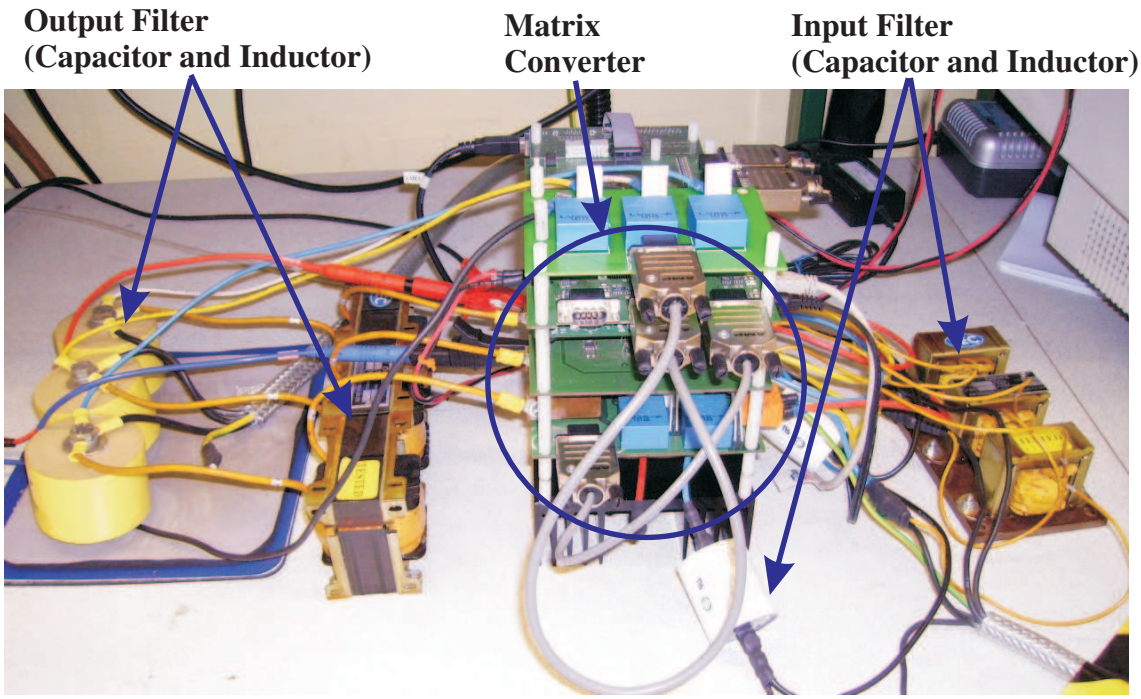


Figure 4.21: Photograph of the final Matrix Converter prototype.

Chapter 5

Experimental Results

5.1 Introduction

This chapter presents results obtained from the experimental prototype whose design and construction has been described in Chapter 4. These practical results validate the control structure proposed in this thesis. Both the Tracking Controller and the Tracking Controller plus the Repetitive Controller have been evaluated and implemented. This chapter starts with the performance of the Matrix Converter system operating in open loop. These results verified the Space Vector modulation (SVM) technique. Then, the control performance employing only the Tracking Controller is presented. Finally, the Tracking Controller plus the Repetitive controller is tested. All tests are performed using the different load conditions described in Chapter 3.

According to the SVM technique theory the maximum voltage that can be obtained in the output of the Matrix Converter is 86% of the input voltage. In the DSP program a condition for the maximum voltage drawn by the system is stated. This condition is used as a protection for the system. The voltage conversion ratio allowable is set to 75% because the maximum nominal output voltage required is 117V rms. With this output voltage required the maximum modulation index obtained is 53%.

The values of the required output voltage and frequency are set in the DSP by using the Matlab interface. This interface is linked directly to the DSP program and read and write values from and to the variables used. The values of each of the variables used in the DSP program are monitored in a window displayed in the Matlab environment. This interface is used to load the program into the DSP without the necessity of the Code Composer Studio (CCS) software. CCS software was used mainly to develop and implement the modulation technique and the controller.

5.2 Control of the Output Voltage with No Controller using ABC Reference Frame

Once the designed and construction of the Matrix Converter prototype was completed it was necessary to run a series of test to verify the power converter performance. Initially a two input phase commutation test was followed by a fixed duty cycle PWM generation test where the commutation of all the tree output phases to each of the input phases was tested using a fixed number of output vectors for fixed times. For this test the output of the Matrix Converter system which includes the input and output filter was connected to a perfectly balanced resistive-inductive load. The output vectors were arranged in such way that each output phase would commutate sequentially between input A, B and C using different duty cycle for each output phase. No controller was used in this test and the reference signals used in the digital signal processor were given in the d-q reference frame and then transformed to the ABC reference frame by using the appropriate transformations.

To carry out the test in open loop a three-phase star-connected resistive-inductive load was used. This balanced load consists of:

Resistive load:

- Phase a = 5.3Ω

- Phase b = 5.3Ω
- Phase c = 5.3Ω

Inductive load:

- Phase a = 3.75mH
- Phase b = 3.75mH
- Phase c = 3.75mH

These values of resistors and inductors were used as the load because they were the only ones available in the facilities at the time of testing the prototype.

The encouraging results of the initial test showed that the Matrix Converter system practical implementation and control including the communication and transfer of information between the Host PC, the DSP/FPGA board and the gate drive board were working as expected.

Figure 5.1 shows the output voltage in phase c obtained. This output waveform is compared to the reference signal. As can be seen, there a notable difference between the amplitude of the output voltage and the reference. The output signal is completely out of phase. This is because the output voltage controller is not used. The output voltage is not controlled and the reference signal is used only by the modulator in order to generated the output voltage required for the modulation strategy. The reference signal is purely controlling the converter output voltage but the phase is not controlled. The waveform obtained is distorted, the amplitude does not keep constant in the same level.

The waveform of the line to line voltage obtained in the output of the Matrix Converter before the output filter is shown in Figure 5.2. This result obtained was as expected and confirms that the Matrix Converter excluding the output filter is working appropriately.

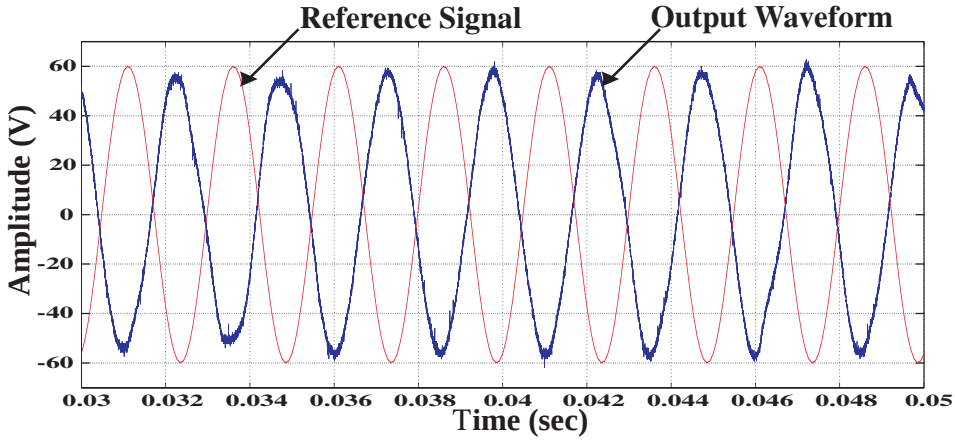


Figure 5.1: Output voltage in phase c with a balanced RL load and no controller.

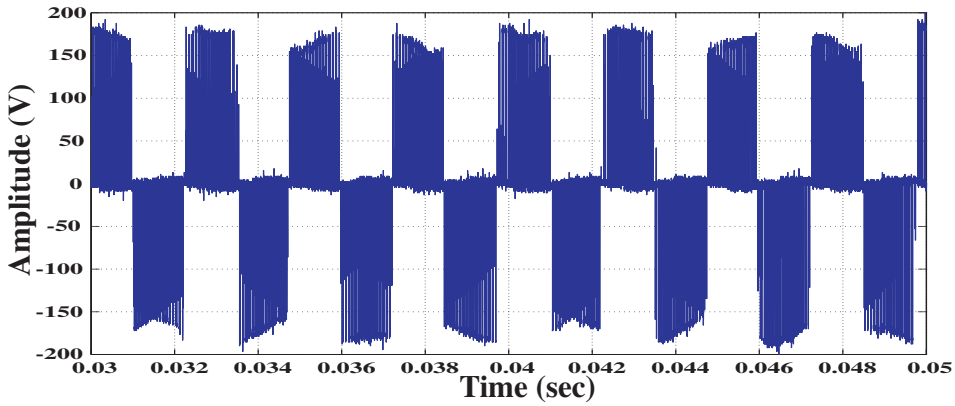


Figure 5.2: Output line to line voltage with a balanced RL load and no controller.

The input current in phase c is shown in Figure 5.3. This waveform is obtained when input filter is included. As expected, the waveform is sinusoidal but contains harmonic distortion. This harmonic distortion is attenuated when the output voltage waveform is improved by using the voltage controller.

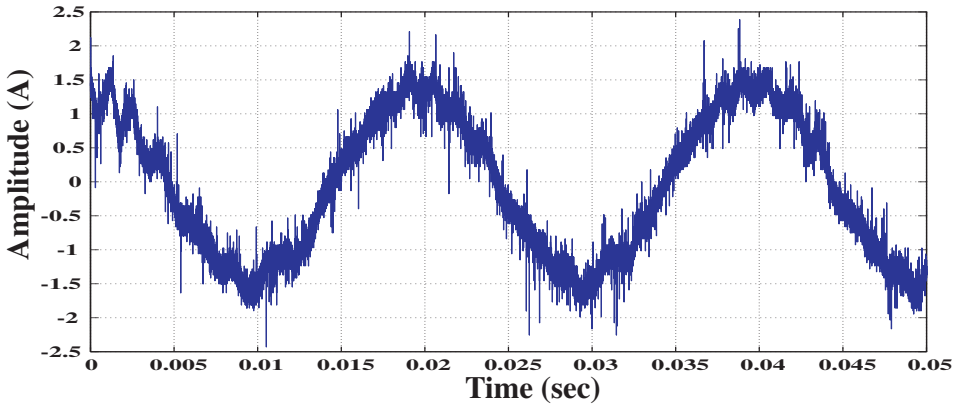


Figure 5.3: Input current in phase c with a balanced RL load and no controller.

Figure 5.4 shows the phase shift between the voltage and current in the load phase c. This phase shift is introduced because the load connected to the system is inductive-resistive.

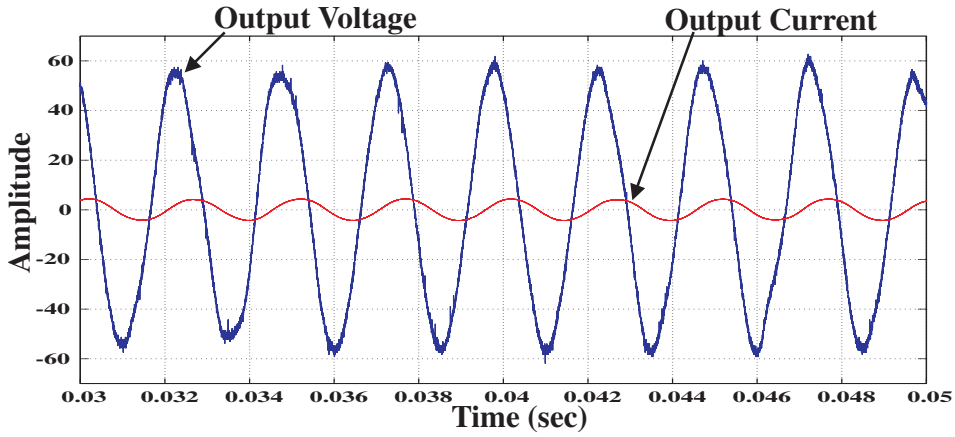


Figure 5.4: Load voltage and current in phase c with a balanced RL load and no controller.

After the performance of the Matrix Converter system was verified the next step was

to replace the source code in the DSP by the source code containing the tracking controller.

5.3 Control of the Output Voltage using Tracking Controller

The tracking controller has been described in Chapter 3. Before implementation, this tracking controller was tested in simulation using different values of the gain. According to simulations the most suitable gain was 0.6, therefore the tracking controller was implemented in the DSP using this value of gain. All the results present in this section use the ABC reference frame which allows the Matrix Converter to operate under any load condition.

5.3.1 Matrix Converter connected to a Resistive Balanced Load

For this test, the inductive load is removed and only the resistive balanced load is connected. As in previous test the resistive load has the following values:

- Phase a = 5.3Ω
- Phase b = 5.3Ω
- Phase c = 5.3Ω

The next sections present the input and output waveforms obtained when a purely resistive load is connected to the system output. The diagram of the basic circuit used in the test is shown in Figure 5.5.

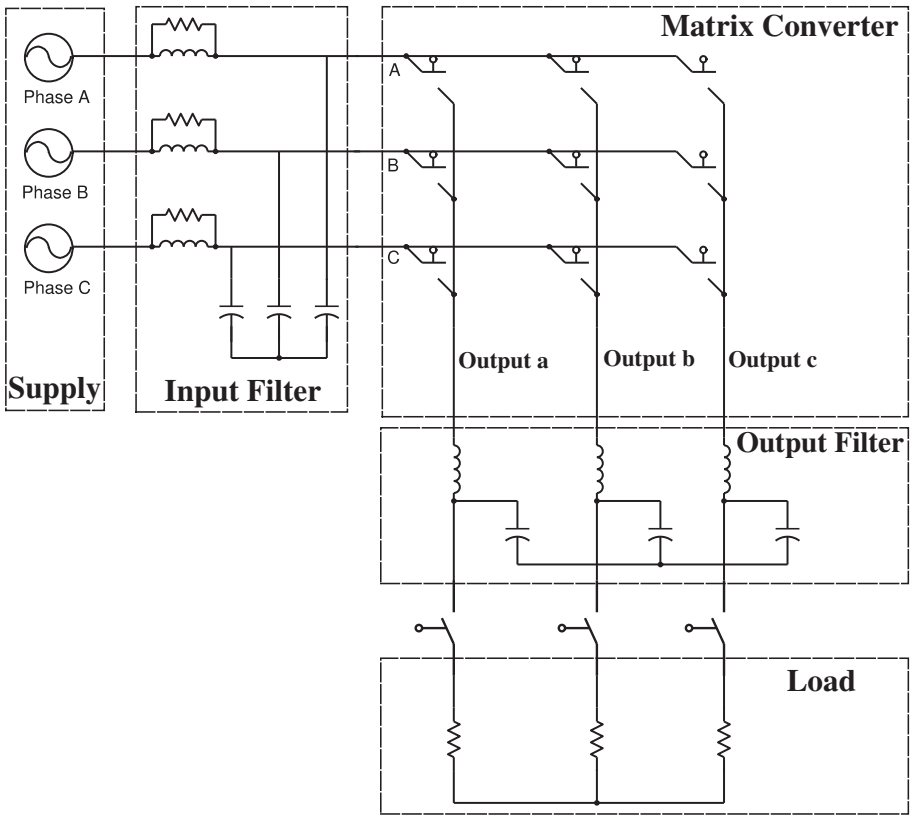


Figure 5.5: Diagram of basic circuit used in the test.

The output voltage waveform obtained when only the tracking controller is used can be seen in Figure 5.6. This figure shows the output voltage compared to the reference signal and it can be seen that there is a phase shift. The output voltage phase is not controlled and the control signal generated by the controller is used only to control the level of output voltage required. Because the ABC reference frame is employed in the design of the control system, the level of voltage in each phase is controlled independently. The voltage controller in each phase generates a sinusoidal signal with the required amplitude. This signal is applied to the Matrix Converter modulator in order to produce a modulation pattern for each of the bi-directional switches. There is an improvement of the amplitude of the output voltage when compare to the use of no controller.

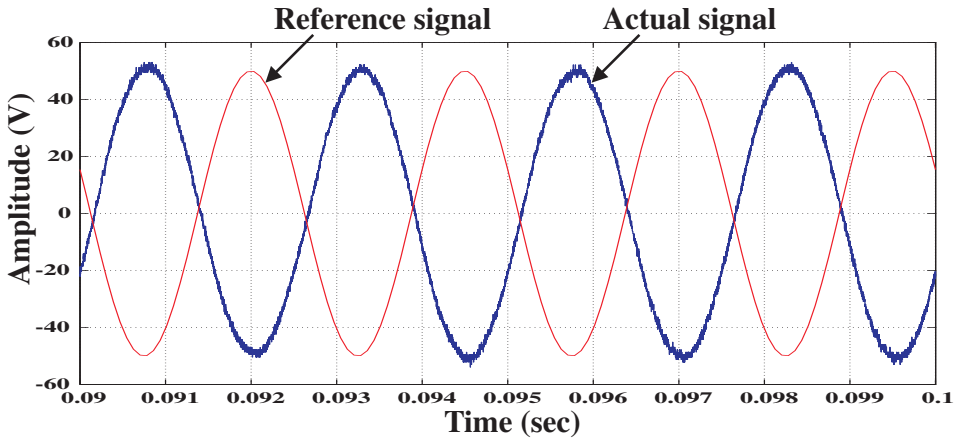


Figure 5.6: Reference signal and output voltage in phase a with a pure resistive, balanced load and tracking controller.

The input current waveform is presented in Figure 5.7 and its corresponding harmonic analysis is shown in Figure 5.8. The use of the input filter reduces the harmonic distortion in the input current waveform. As can be seen in these figures, the harmonic components appear in the low frequency range because the input filter was designed with a cut-off frequency of 1.18kHz. The input current waveform is not very distorted because the load connected to the Matrix Converter system is purely resistive and balanced.

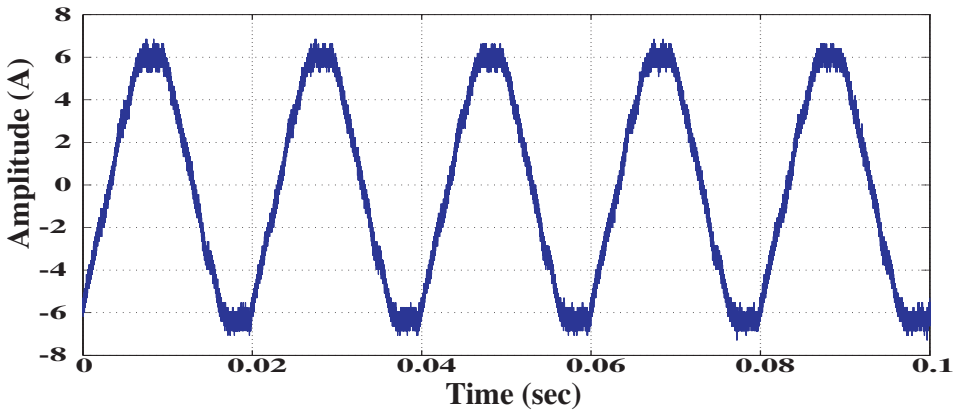
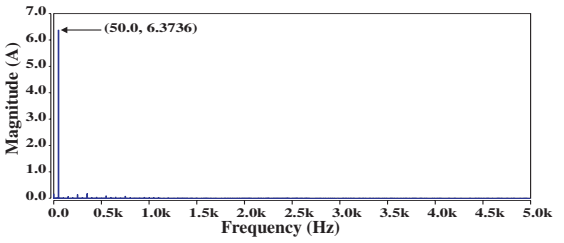
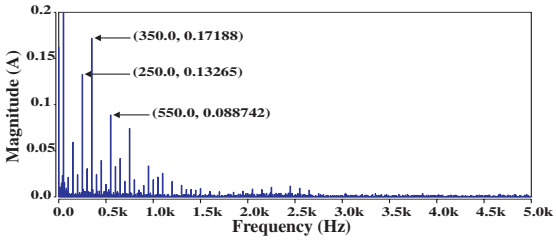


Figure 5.7: Input current in phase a with a pure resistive, balanced load and tracking controller.



(a) Harmonic spectra with resistive load connected



(b) Details of the harmonic spectra with resistive load connected

Figure 5.8: Harmonic spectra of input current in phase A when tracking controller is used.

The Matrix Converter (MC) current is shown in Figure 5.9. This current is used to determine the current direction employed for the commutation of the bi-directional switches. The Matrix Converter current waveform has an improvement when the tracking controller is used and the current direction can be easily determined.

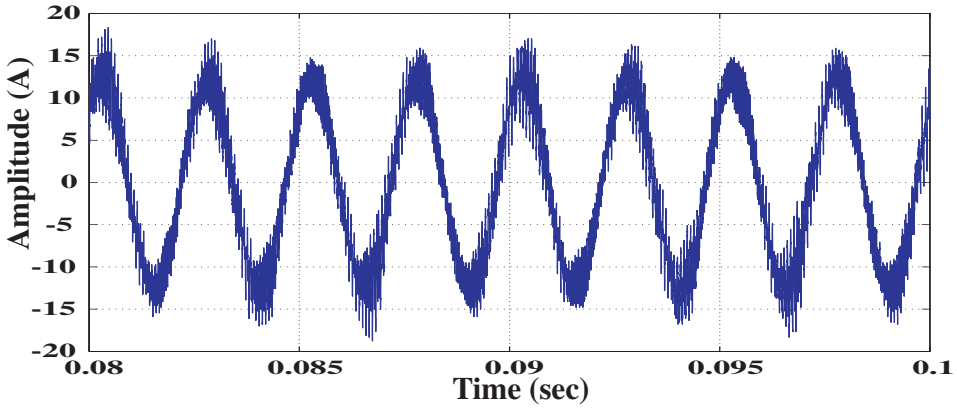


Figure 5.9: MC Current in phase a with a pure resistive, balanced load and tracking controller.

Finally, with a purely resistive balanced load connected to the Matrix Converter system the waveform of the current in the load is obtained, this waveform is shown in Figure 5.10.

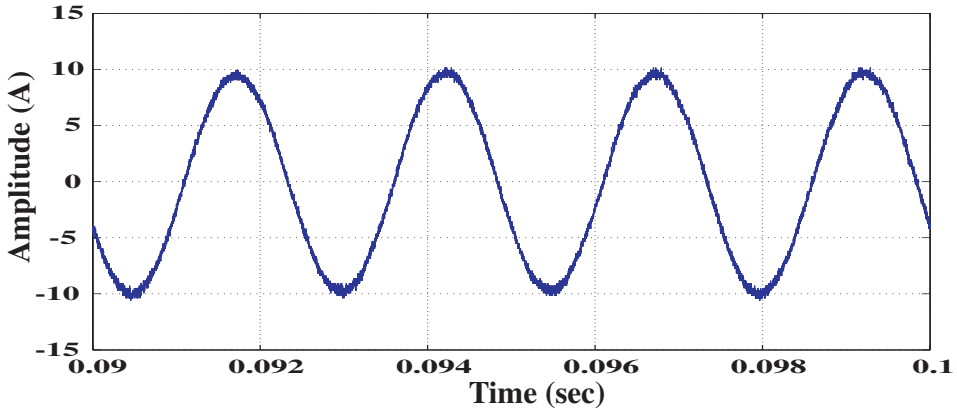


Figure 5.10: Current in the load phase a with a pure resistive, balanced load and tracking controller.

5.3.2 Matrix Converter connected to a Resistive, Unbalanced Load

For this test the purely resistive, balanced load was replaced by a resistive, unbalanced load. This unbalance load has the following values:

- Phase a = 16.1Ω
- Phase b = 11.1Ω
- Phase c = 6.1Ω

The voltage achieved at the output as well as the input and output current waveforms obtained are presented below.

The use of a tracking controller in the ABC reference frame allows the Matrix Converter based power supply to operate under unbalanced load conditions. The unbalanced condition of the load used in this test has been produced in a way that the load in phase a is connected to 144% of the nominal load, load in phase b is connected to 100% of the nominal load and load in phase c is connected to 56% of the nominal load. The excellent performance of the voltage controller in the ABC reference frame is verified by the practical results obtained. These results are shown in Figure 5.11. As can be seen, the output voltage in each of the three phases has the same level even with the unbalanced condition in the load.

The problem with the unbalanced load condition is that the input current waveform is distorted, as can be seen in Figure 5.12. The harmonic distortion injected to the electrical network is increased because the current flowing through the load remains unbalanced, as can be seen in Figure 5.13. The input filter has been designed as a low pass filter to eliminate the harmonics of frequency higher that 1.83kHz but the low frequency harmonics remain. The resonance frequency is set to 1.18kHz because it must be far away from the output frequency which has a value of 400Hz. It is

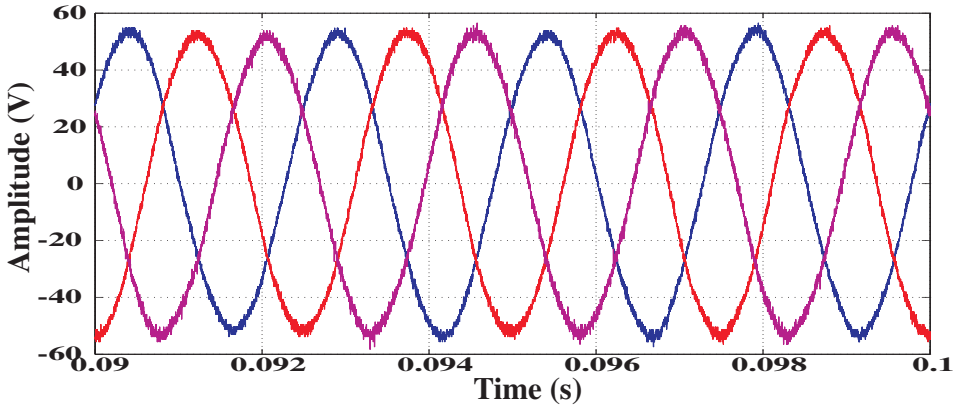


Figure 5.11: Output voltages with a pure resistive, unbalanced load and tracking controller.

dangerous if the resonance frequency is set close to the output frequency because the equipment could be destroyed. Therefore, input currents can have high values of harmonic components with frequencies in the range from 0Hz to 1.18kHz.

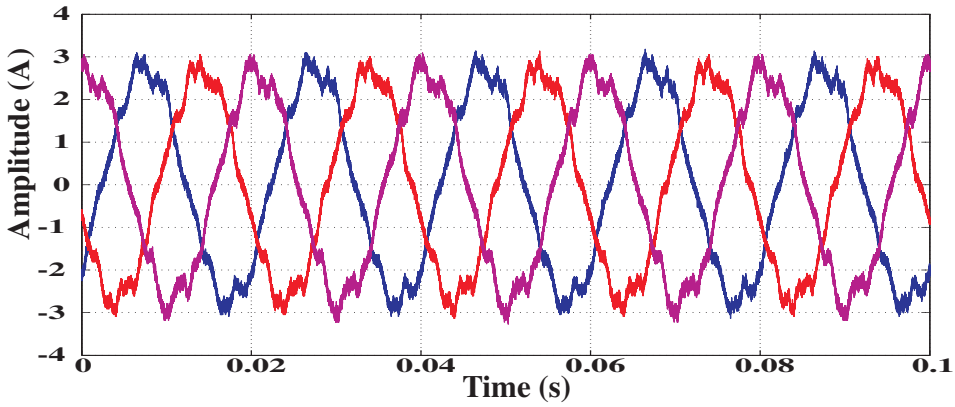


Figure 5.12: Input currents with a pure resistive, unbalanced load and tracking controller.

The Matrix Converter output current in phase a is shown in Figure 5.14. Note that this more distorted that the one obtained when the Matrix Converter system is connected to a purely resistive balanced load. These Matrix Converter output currents are balanced because the tracking controller maintains the voltage across the output filter capacitor in the same level for all three phases.

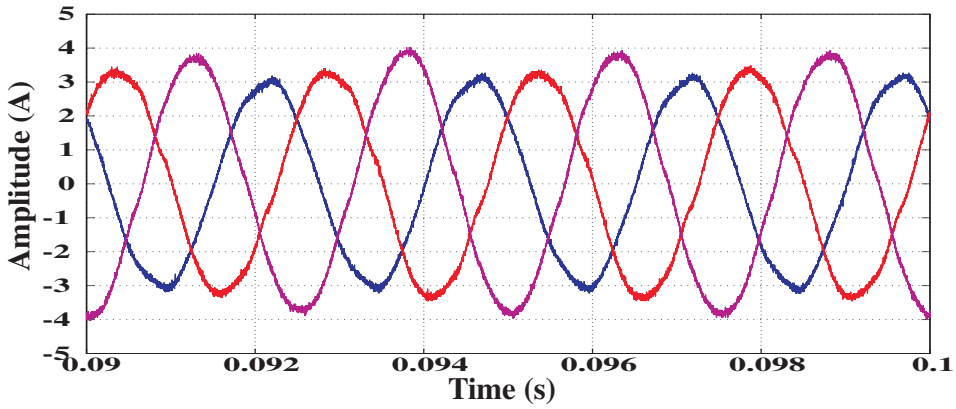


Figure 5.13: Currents in the load with a pure resistive, unbalanced load and tracking controller.

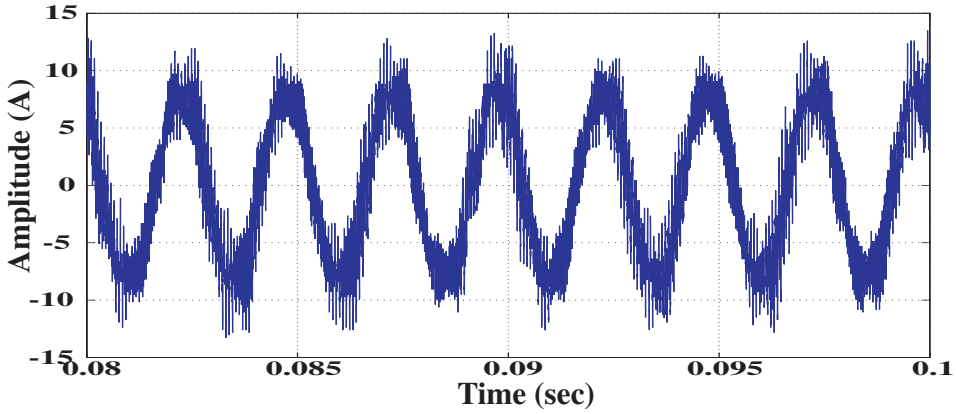


Figure 5.14: Matrix Converter output current in phase a with a pure resistive, unbalanced load and tracking controller.

5.3.3 Matrix Converter connected to a Resistive-Inductive Balanced Load

The Matrix Converter system has also been tested using a resistive-inductive balanced load. Obviously, the practical results obtained are different to those obtained when a purely resistive load is connected. The use of an inductive-resistive load adds more distortion to the output voltage waveform due to the nature of the inductive load.

Resistive part of the load has the values mentioned is Section 5.3.1. The inductive part added to the load has the following values:

- Phase a = 3.75mH
- Phase b = 3.75mH
- Phase c = 3.75mH

The amplitude of the output voltage is not completely maintained when the tracking controller is used and the load connected to the system is balanced. The distortion introduced in the output voltage waveform is caused due to the inductive part of the load. This can be seen in Figure 5.15. This problem is solved by using the Repetitive Controller which is implemented later on this thesis.

Figure 5.16 shows the input current which are distorted due to the addition of an inductive load even considering a balanced load condition. For measuring input currents, two Lecroy current probes and one Rogowski coil were used. Input current in phase a and phase b were taken using the Lecroy current probes and input current in phase c was taken using the Rogowski coil. The distortion observed in input current in phase c is due to the use of the Rogowski coil, which has a bandwidth different from bandwidth of the Lecroy current probes. Typical bandwidths of the Rogowski coil used are from 0.1Hz to 16MHz. Input currents in phases a and b are bandwidth limited by the measurement, they depend on the measurement instrument resolution.

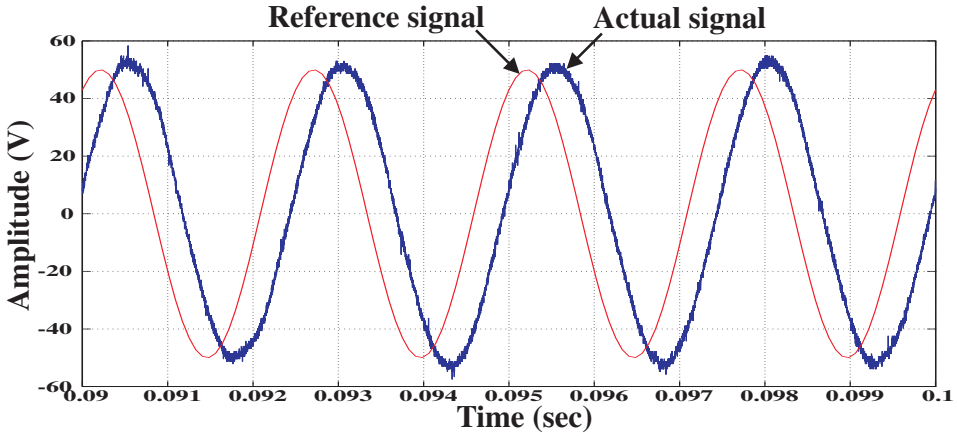


Figure 5.15: Output voltage in phase a with a balanced RL load and tracking controller.

The Matrix Converter current in phase a can be seen in Figure 5.17. Finally for this test, Figure 5.18 shows the current in the resistive-inductive load phase a. The current are the same for each phase because of the balanced condition of the load.

5.3.4 Matrix Converter connected to a Resistive-Inductive Unbalanced Load

For the resistive-inductive unbalanced condition test, the restive part of the load has the values given in Section 5.3.2 and the inductive part has those values given in Section 5.3.3. Should be noted that only the resistive part is unbalanced while the inductive part remains balanced. This is because a three-phase choke is used for the inductive load and it is not possible to change the value of the inductance in each phase.

The output voltage waveform has the same amplitude in each phase, but also they have the same distortion, as can be seen in Figure 5.19. This distortion is due to the fact that an resistive-inductive load is connected.

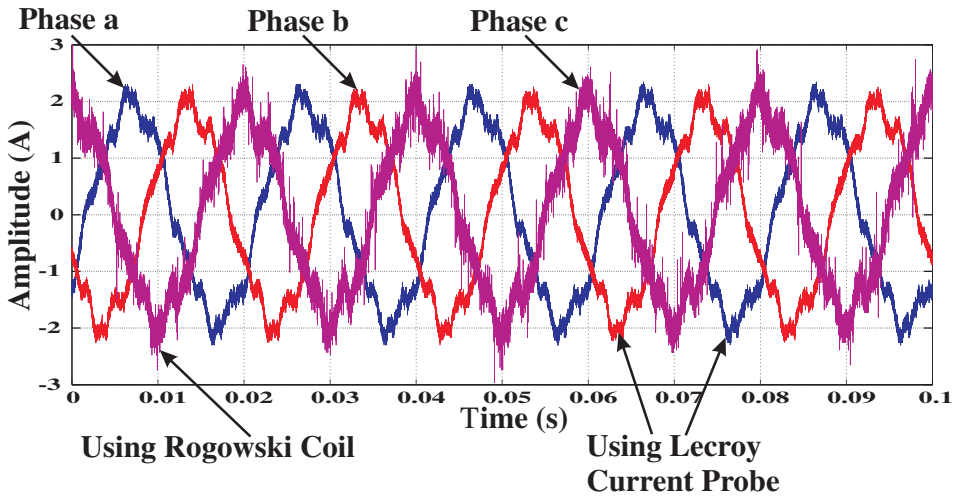


Figure 5.16: Input currents with a balanced RL load and tracking controller. Note: the load current waveform in phase c looks more distorted than the other waveforms but this is due the use of a current probe with a different bandwidth range of operation.

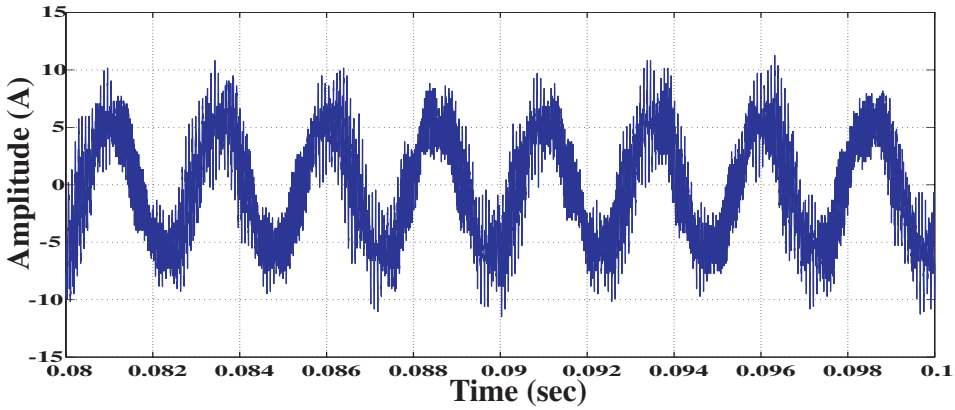


Figure 5.17: Matrix Converter current in phase a with a balanced RL load and tracking controller.

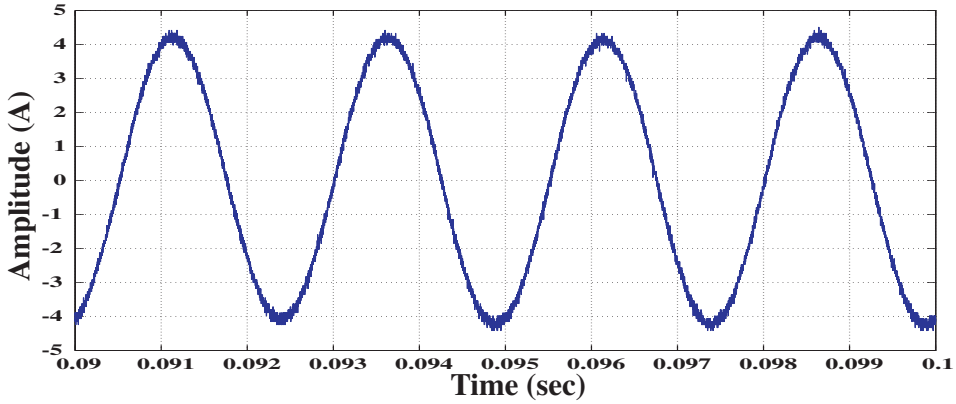


Figure 5.18: Current in load phase a with a balanced RL load and tracking controller.

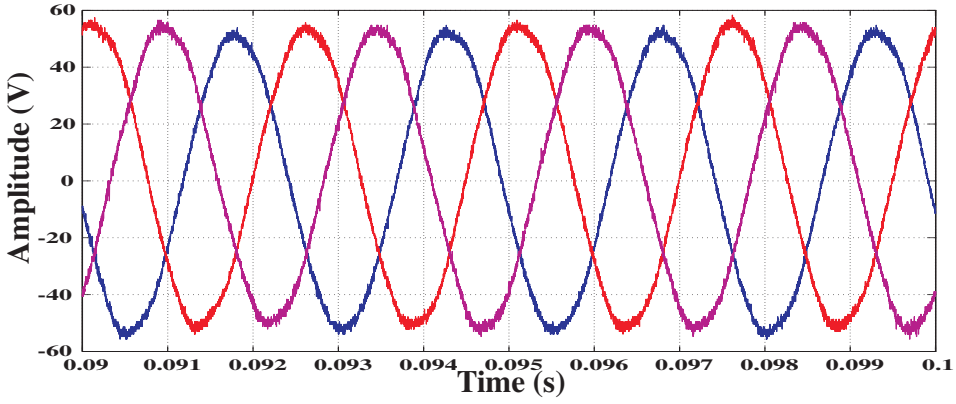


Figure 5.19: Output voltages with an unbalanced RL load and tracking controller.

When only the tracking controller is implemented in the DSP and the Matrix Converter system is connected to a RL unbalanced load the output voltage does not match the reference signal as can be seen in Figure 5.20. There are differences in the amplitude as well as in the phase.

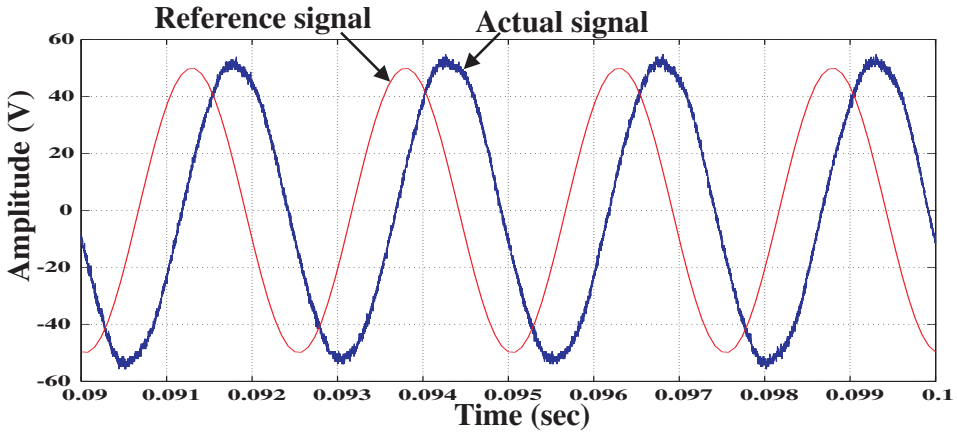


Figure 5.20: Output voltage in phase a with an unbalanced RL load and tracking controller.

As can be seen, the harmonic distortion is quite similar to that obtained when the load is unbalanced but purely resistive, as shown in Figure 5.21. The nature of the inductive load acts as the unbalanced condition in a purely resistive load.

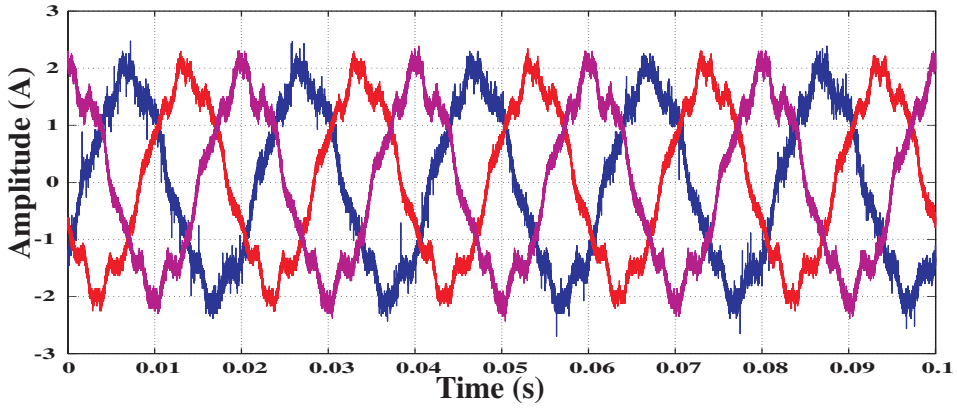


Figure 5.21: Input currents with an unbalanced RL load and tracking controller.

The waveform of output current in the Matrix Converter before the output filter can

be seen in Figure 5.22. The harmonic distortion content in this waveform is similar to that obtained when a purely resistive balanced load is connected.

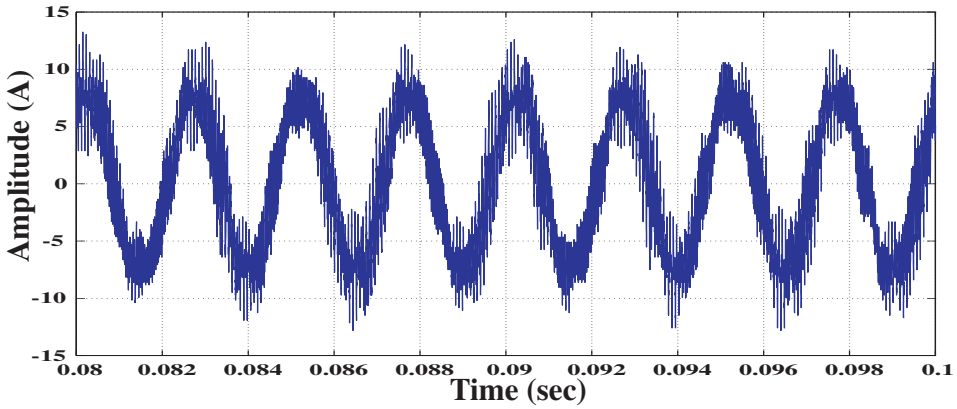


Figure 5.22: Output current of the Matrix Converter in phase a with an unbalanced RL load and tracking controller.

All three currents present in a RL unbalanced load are shown in Figure 5.23. Even if the tracking controller maintains the amplitude of all the three output voltages in the same value, the load current waveforms remain unbalanced. The tracking controller only controls the output voltages and not the output currents.

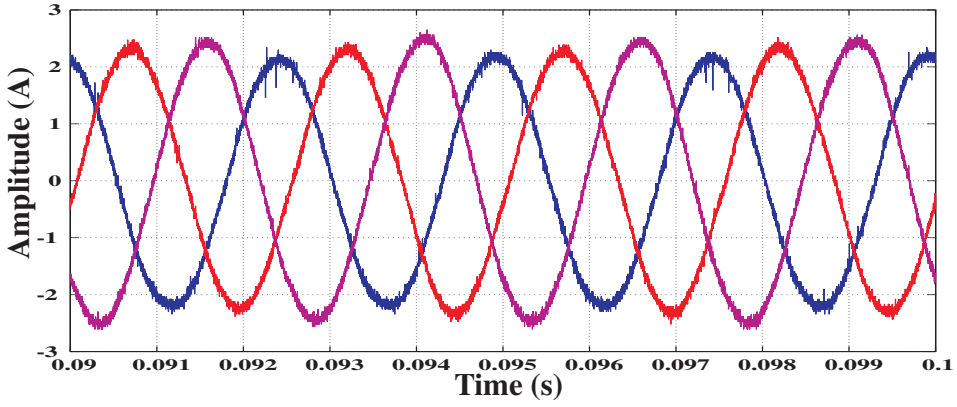


Figure 5.23: Currents in load with an unbalanced RL load and tracking controller.

5.3.5 Matrix Converter with Load Disconnected

The disconnected load condition is the worst case of operation of the Matrix Converter based power supply. In these tests the load was completely disconnected. A three-phase contactor was used to make the disconnection. Neither resistive or inductive load is connected to the system. The tracking controller must then be able to maintain the voltage across the output filter capacitor in each phase.

At full input voltage and delivering full power at the load, the modulation index has a value of

$$\frac{Output \quad voltage}{Input \quad voltage} = \frac{117Vrms}{240Vrms} = 0.4875 \tag{5.1}$$

The modulation index achieved in this test has the value shown in Figure 5.24. The variation is due to the distortion in the input voltage and in less importance the sampling frequency.

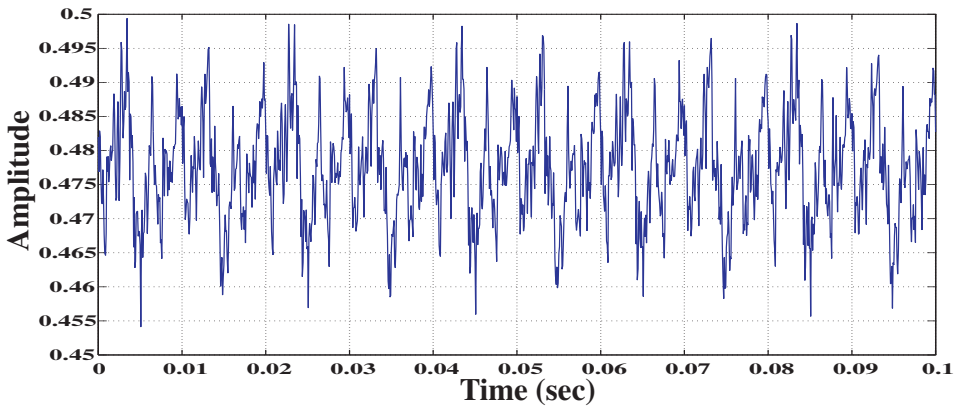


Figure 5.24: Modulation index with load disconnected.

The waveform of the three output voltages obtained when the load is disconnected is shown in Figure 5.25. As expected the tracking controller produce sinusoidal waveforms with the same amplitude in each of the phases.

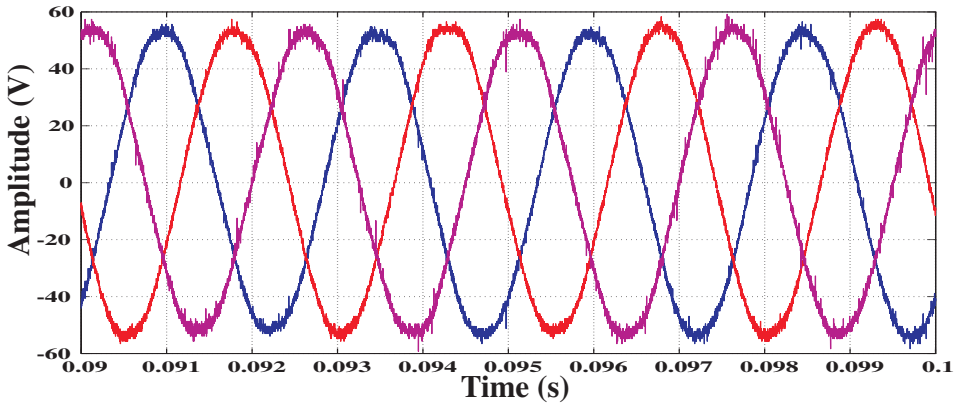


Figure 5.25: Output voltages with load disconnected and using tracking controller.

As can be noted in Figure 5.26 the amplitude of the output voltage does not match the amplitude of the reference signal. The tracking controller is not completely able to track the reference signal. The amplitude of the three output voltages has slightly increment when the load is disconnected. This situation was the main reason to search for better solution and as a result the Repetitive Controller structure was proposed.

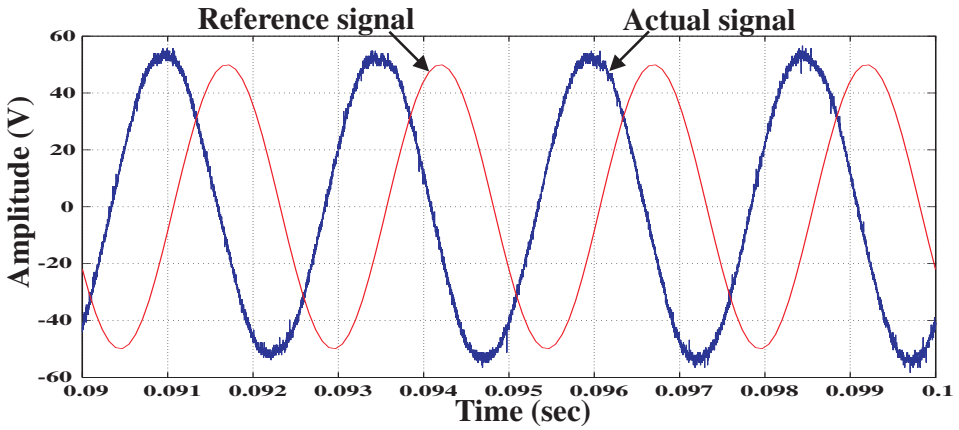


Figure 5.26: Output voltage in phase a with load disconnected and using tracking controller.

The waveform of the input current obtained in phase a is shown in Figure 5.27. Compared to that obtained in the previous test, the harmonic distortion is very similar. There is not much improvement because the tracking controller only controls

the voltage across the output filter capacitor and not the current flowing through the output filter inductor.

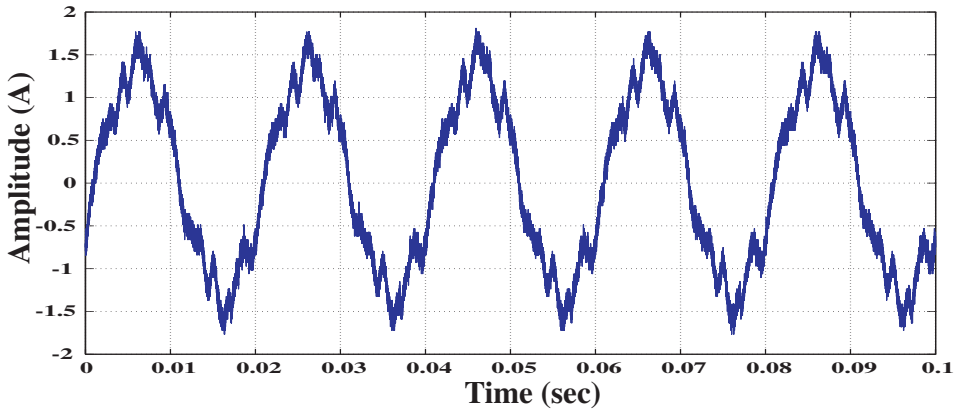


Figure 5.27: Input Current in phase a with load disconnected and using tracking controller.

Figure 5.28 shows the Matrix Converter current waveform. As can be seen there is not much improvement because the tracking controller only controls the voltage across the output filter capacitor and not the current flowing through the output filter inductor.

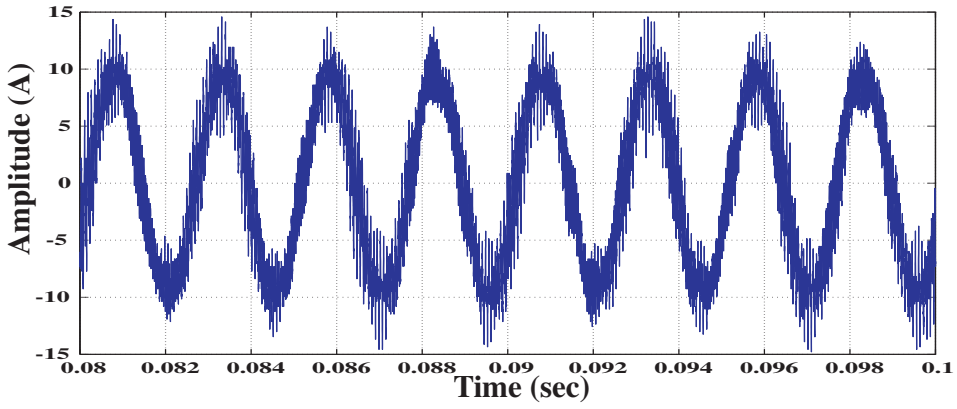


Figure 5.28: Current before output filter with load disconnected and using tracking controller.

Because no load is connected, the current flowing through it is zero.

5.4 Control of the Output Voltage using Tracking Controller plus Repetitive Controller

The control structure proposed to solve the problem present when the load is disconnected is implemented and discuss in this section. When only the Tracking Controller is implemented, the amplitude of the output voltage obtained increased slightly. Results obtained in Section 5.3.5 shown this mismatch between the the output signal and the reference signal. The same tests done when only the tracking controller was implemented are done in this section but adding the Repetitive Controller structure.

5.4.1 Matrix Converter connected to a Resistive Balanced Load

In this test, the resistive load is balanced and has the following values:

- Phase a = 5.3Ω
- Phase b = 5.3Ω
- Phase c = 5.3Ω

The Matrix Converter system is connected to a three-phase balanced load. The output voltage obtained in phase a is shown in Figure 5.29. The reference signal is also included in this figure for comparison purposes. As can be seen when the load is purely resistive and balanced, the output voltage obtained tracks the reference signal.

Figure 5.30 shows input currents of the power converter. These input currents are obtained when the power converter is connected to a pure resistive load which is balanced. The harmonic distortion present is due the addition of the Repetitive Control structure. The Repetitive Control structure contains a low-pass second order filter

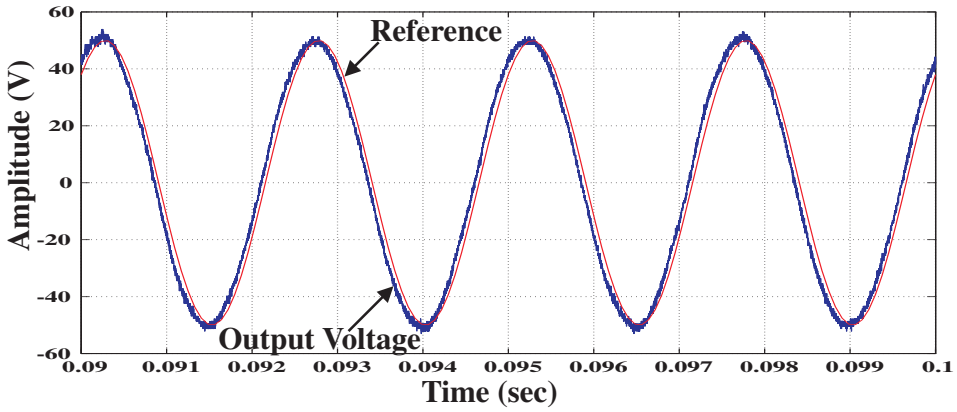


Figure 5.29: Output voltage in phase a with a pure resistive, balanced load and Repetitive Controller.

and a delay loop. This control topology modifies the transfer function of the plant and consequently the behavior of the Matrix Converter. The currents harmonics produced by the switching frequency used in the power converter modulator contribute to this harmonic distortion.

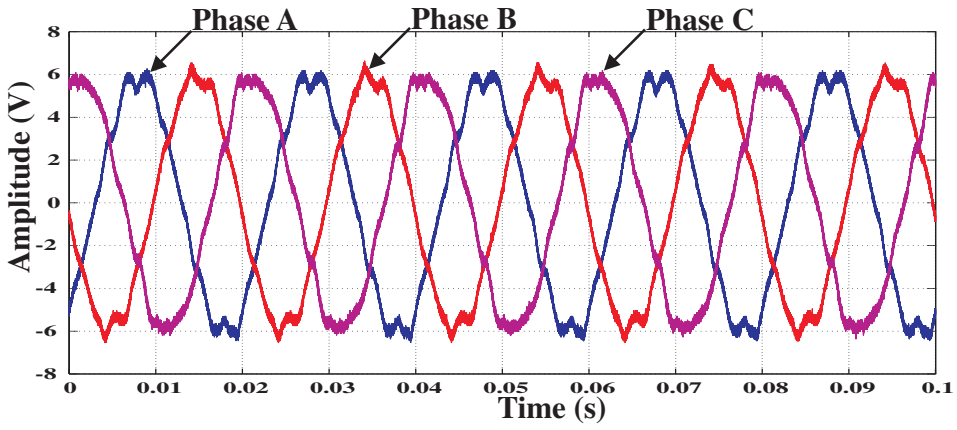


Figure 5.30: Input currents with a pure resistive, balanced load and Repetitive Controller.

Figure 5.31 shows output current of the Matrix Converter in phase a before the output filter. There is an improvement of this waveform when the Repetitive Controller is used and also because power converter is connected to a pure resistive load which is

balanced.

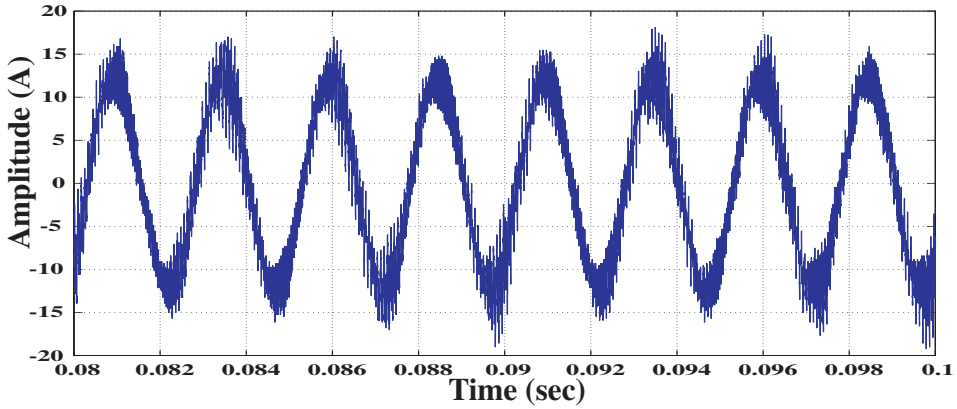


Figure 5.31: Output current in phase a with a pure resistive, balanced load and Repetitive Controller.

The waveforms of currents in the load are shown in Figure 5.32. These waveforms are almost sinusoidal and the contains very small harmonic distortion as can be seen in the figure.

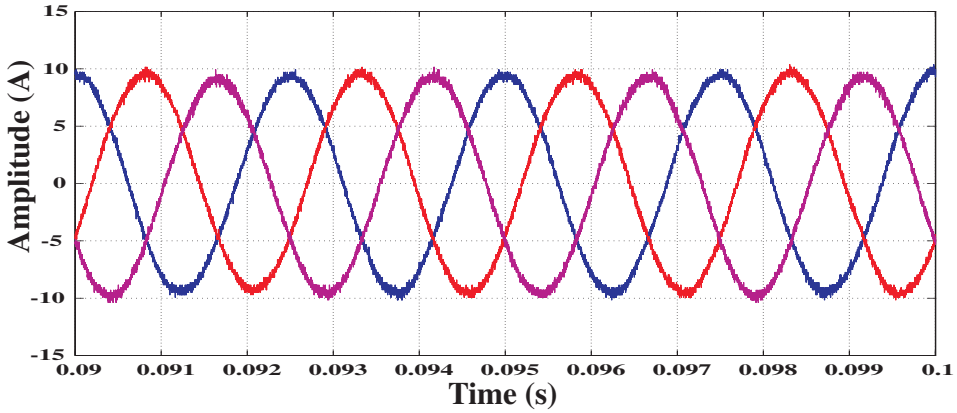


Figure 5.32: Load currents with a pure resistive, balanced load and Repetitive Controller.

5.4.2 Matrix Converter connected to a Resistive Unbalanced Load

The resistive load is unbalanced and has the following values:

- Phase a = 16.1Ω
- Phase b = 11.1Ω
- Phase c = 6.1Ω

Note that this unbalanced condition has been produced in such way that the load in phase a is 144% of the nominal load which is set in phase b while the load in phase c has a value 56% of the nominal load.

The three output voltages waveforms are shown in Figure 5.33. As can be seen the amplitude of the three output voltage is maintained even with an unbalanced condition of ±44% of the nominal load.

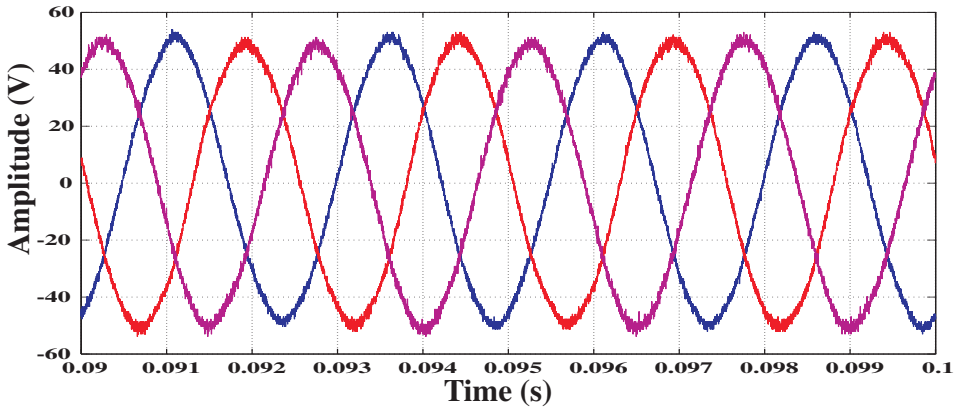


Figure 5.33: Output voltages with a pure resistive, unbalanced load and Repetitive Controller.

Figure 5.34 shows the input currents waveforms obtained when the Matrix Converter system is connected to an purely resistive unbalanced load. The addition of the

Repetitive Controller topology plus the unbalanced condition of the load makes no difference to the harmonic distortion of the input current because of the currents in the load are unbalanced and the voltage controller does not have control over that.

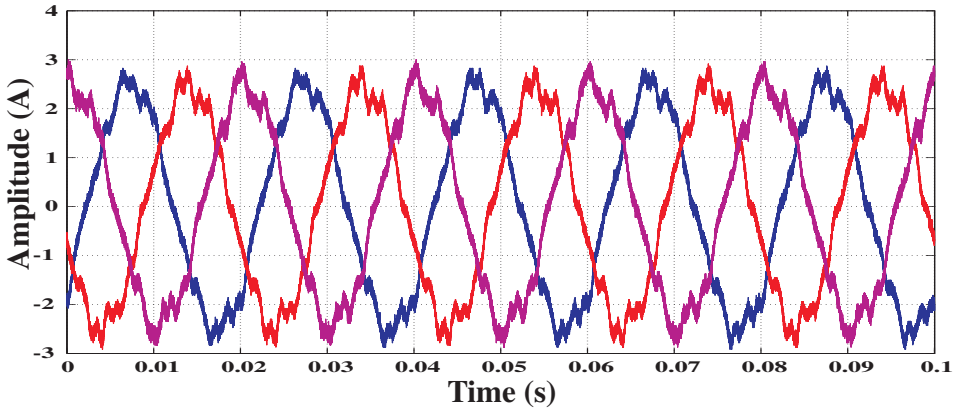


Figure 5.34: Input currents whit a pure resistive, unbalanced load and Repetitive Controller.

The current in the output of the Matrix Converter in phase a and the currents in the load are shown in Figure 5.35 and 5.36 respectively.

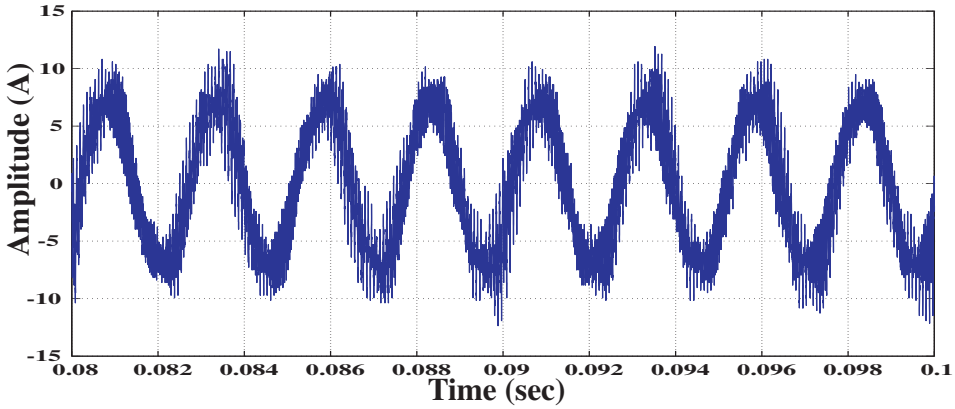


Figure 5.35: Matrix Converter current in phase a with a pure resistive, unbalanced load and Repetitive Controller.

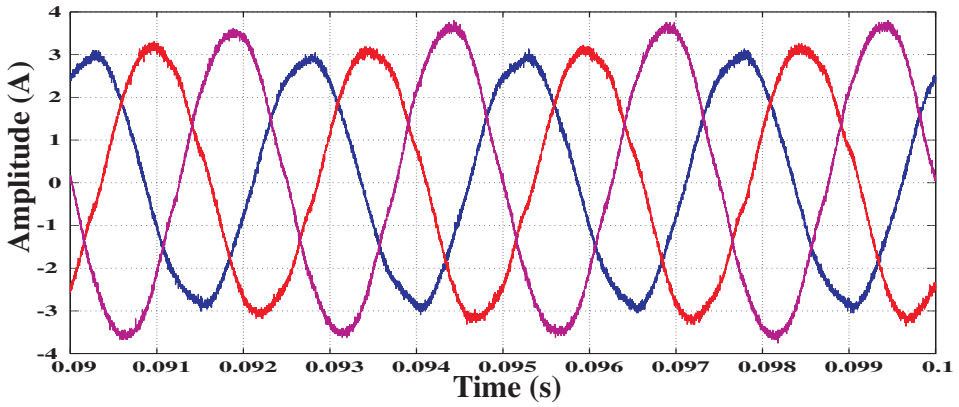


Figure 5.36: Load currents with a pure resistive, unbalanced load and Repetitive Controller.

5.4.3 Matrix Converter connected to a Resistive-Inductive Balanced Load

The value of the resistive-inductive balanced load used in this test has the same values as in section 5.3.3, i.e.,

- Resistive load in phase a = 5.3Ω
- Resistive load in phase b = 5.3Ω
- Resistive load in phase c = 5.3Ω

- Inductive load in phase a = 3.75mH
- Inductive load in phase b = 3.75mH
- Inductive load in phase c = 3.75mH

The reference signal and the output voltage signal are shown in Figure 5.37. This figure indicates that the amplitude of the output voltage is the same as the amplitude of the reference signal. However a phase shift appears between these two signals and

this is due to the fact that the Repetitive Controller introduces delays in the system and the transfer function of the plant was calculated considering only the output filter and not considering the load connected. The voltage controller compensate only the phase shift added by the output filter and it does not compensate the phase shift added by the RL load.

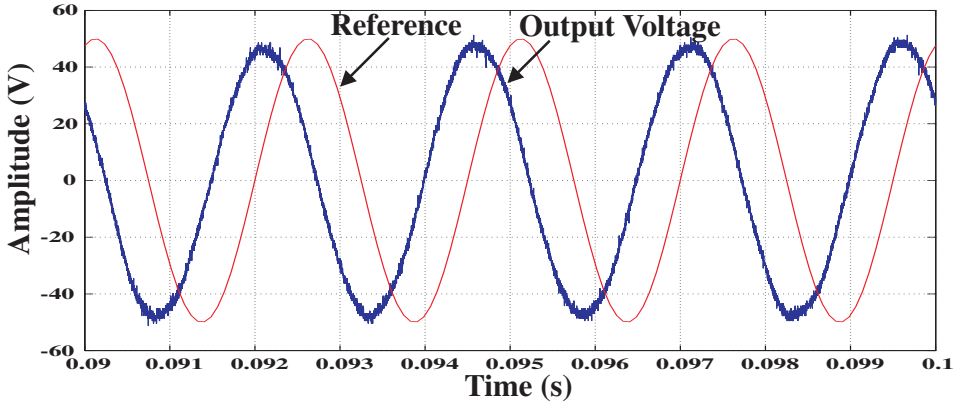


Figure 5.37: Output voltage in phase a with a balanced RL load and Repetitive Controller.

The input current waveform in phase A is shown in Figure 5.38. There is a improvement in the harmonic distortion because the load connected to the Matrix Converter system is perfectly balanced and even using a resistive-inductive load.

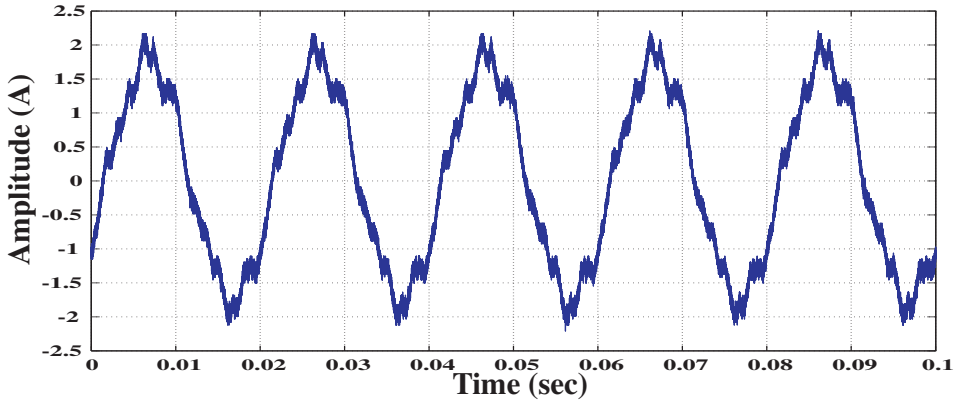


Figure 5.38: Input current in phase A with a balanced RL load and Repetitive Controller.

Figures 5.39 and 5.40 show the Matrix Converter and the load current in phase a respectively. The Matrix Converter current shows the addition of high frequency harmonic distortion while the waveform of the current in the load is completely sinusoidal. The high frequency harmonic distortion in the MC current is because the Repetitive Controller tries to compensate the errors in the output voltage by modifying the switching pattern in the modulator.

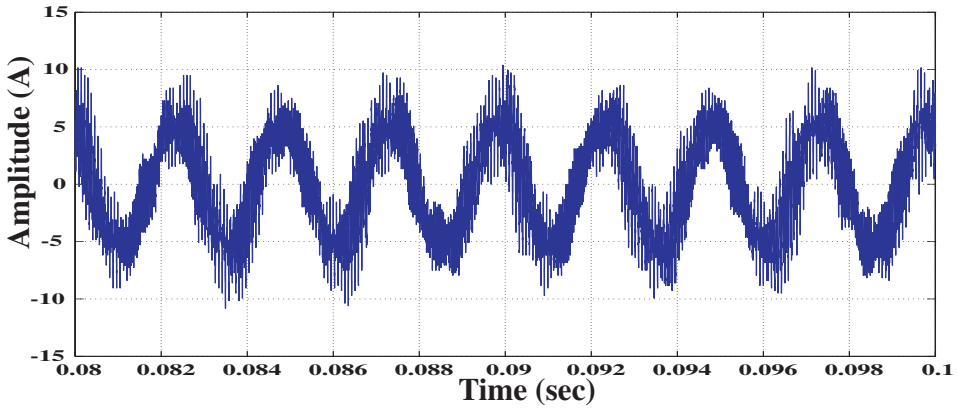


Figure 5.39: Matrix Converter output current in phase a with a balanced RL load and Repetitive Controller.

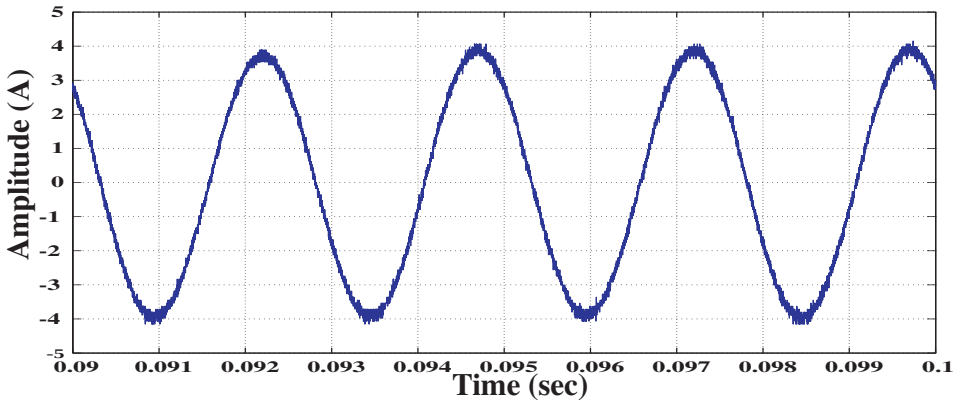


Figure 5.40: Load current in phase a with a balanced RL load and Repetitive Controller.

5.4.4 Matrix Converter connected to a Resistive-Inductive Unbalanced Load

For this test, the resistive-inductive load is balanced and has the same values used in section 5.3.4.

Resistive part of the load:

- Phase a = 16.1Ω
- Phase b = 11.1Ω
- Phase c = 6.1Ω

Inductive part of the load:

- Phase a = 3.75mH
- Phase b = 3.75mH
- Phase c = 3.75mH

All three output voltages waveforms can be seen in Figure 5.41. Once again the performance of the controller in the ABC reference frame is verified with the results obtained. The amplitude in each of the phases is maintained in the level determined by the reference signal. Even with the unbalanced condition of the load and the resistive-inductive nature of the load, the waveforms obtained are sinusoidal.

The harmonic spectra of the output voltage is shown in Figure 5.42. As can be seen the harmonic distortion is minimal compared to the fundamental component which value is 49.199. A zoomed-in plot is shown in Figure 5.42(b) and indicates that the biggest harmonic component occurs at 2kHz and has a value of 0.39258 which compared to the fundamental component is only 0.80%. Also, a second biggest harmonic appears

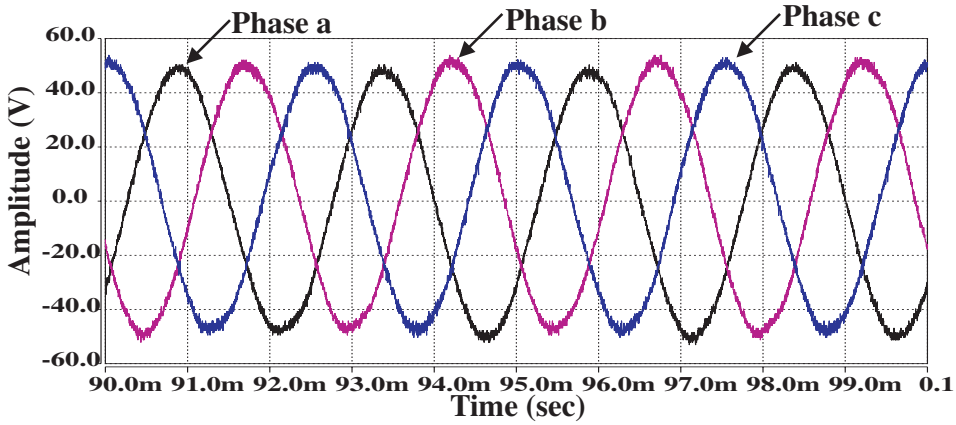
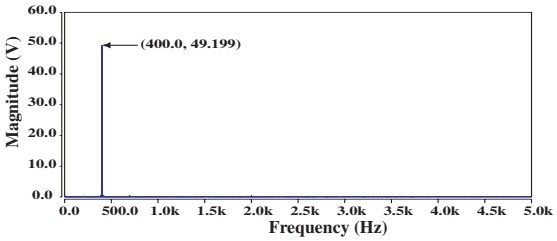
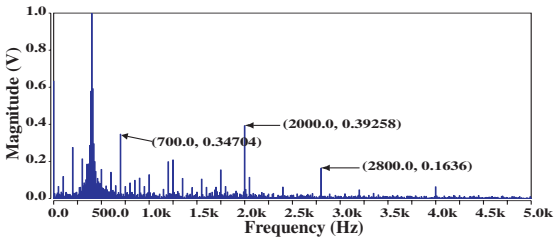


Figure 5.41: Output voltages with an unbalanced RL load and Repetitive Controller.

at 700Hz. This harmonic component has a considerable value compared to the fifth harmonic (at 2kHz). The Total Harmonic Distortion (THD) is 2.15% which basically meets the requirements imposed in the design of the Matrix Converter based power supply.



(a) Harmonic spectra with load unbalanced, phase a



(b) Details of the harmonic spectra with load unbalanced, phase a

Figure 5.42: Harmonic spectra of output voltage in phase a. THD = 2.1526%

The input current waveform obtained is distorted as can be seen in Figure 5.43. The unbalanced condition of the load causes this distortion which is even increased by the use of the Repetitive Controller as was explained in section 5.4.1. Its harmonic spectra is shown in Figure 5.44. The details in Figure 5.44(b) show that 5th, 7th and 13th harmonics are the biggest component adding the distortion. The calculation of

the Total Harmonic Distortion gives a value of 6.15%. This value is slight higher than the value imposed in the requirements for the design of the system.

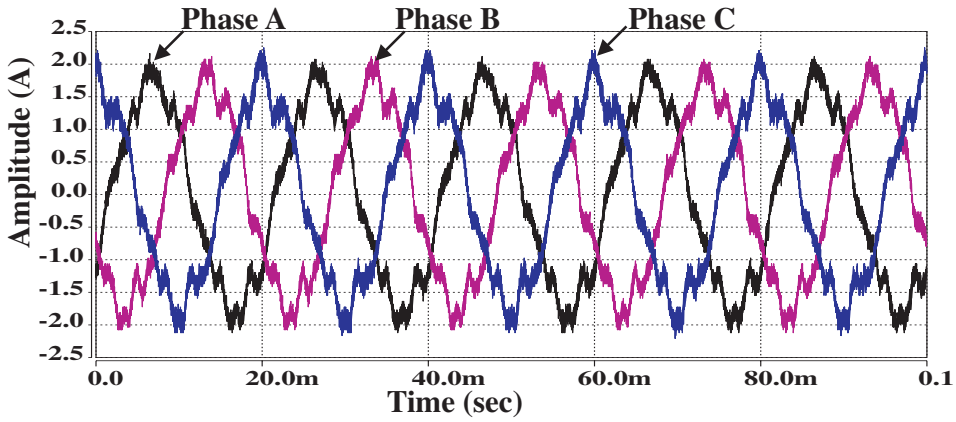
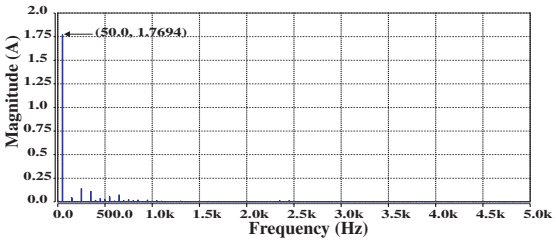
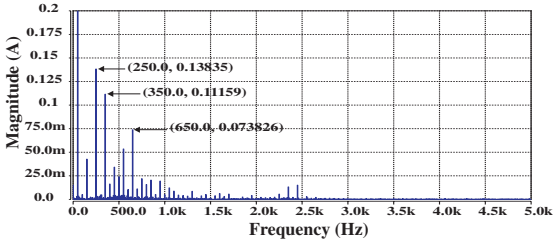


Figure 5.43: Input currents with an unbalanced RL load and Repetitive Controller.



(a) Harmonic spectra with load unbalanced, phase A



(b) Details of the harmonic spectra with load unbalanced, phase A

Figure 5.44: Harmonic spectra of input current in phase A. THD = 6.15%

The waveform of the Matrix Converter current is included in Figure 5.45. Its harmonic spectra shown in Figure 5.46(a) indicates that the high frequency harmonics occur at multiples of the switching frequency which has a value of 12.8kHz. The Total Harmonic Distortion (THD) is 0.61% and low harmonic components appear at 2kHz and 2.8kHz.

The resistive-inductive nature and unbalanced condition of the load produce the load currents shown in Figure 5.47. The controller was designed to control the output

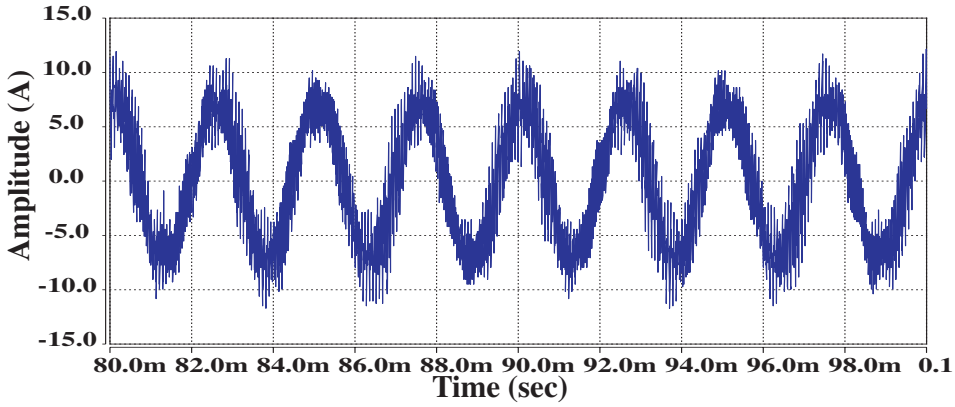
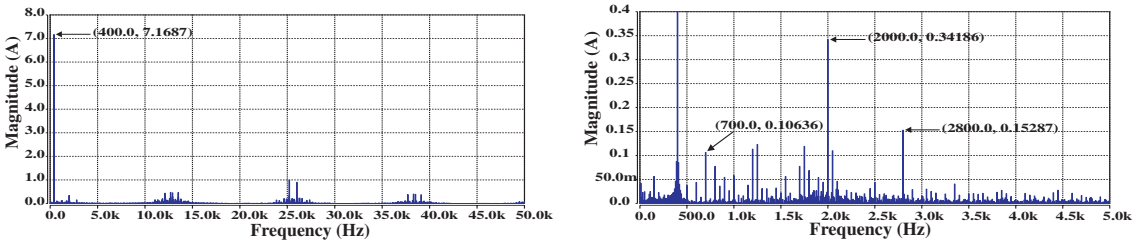


Figure 5.45: Matrix Converter output current in phase a with an unbalanced RL load and Repetitive Controller.



(a) Harmonic spectra with load unbalanced

(b) Details of the harmonic spectra with load unbalanced

Figure 5.46: Harmonic spectra of Matrix Converter output current in phase a. THD = 0.61%

voltage therefore the currents in the load remain unbalanced due its unbalanced condition.

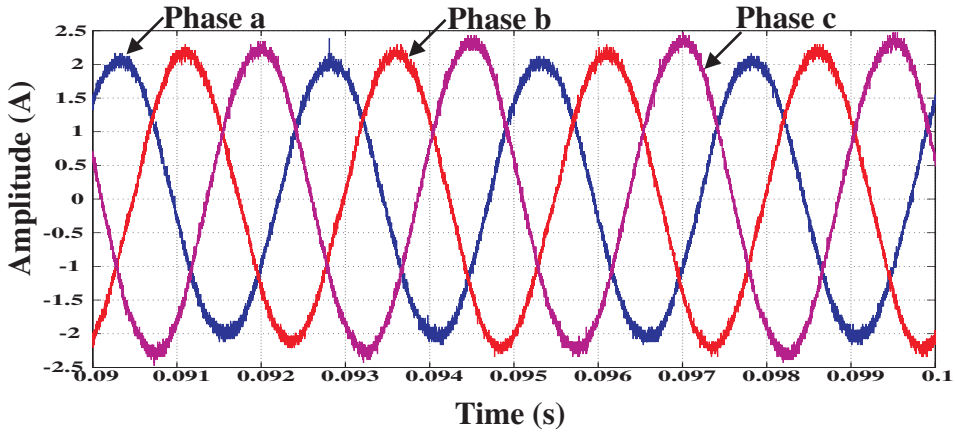
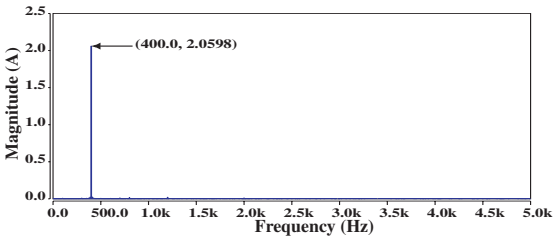
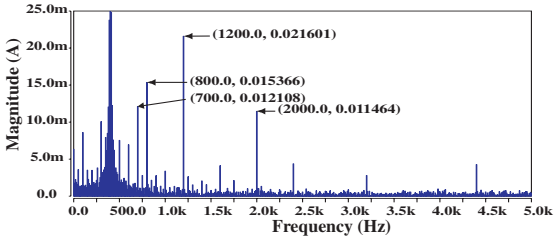


Figure 5.47: Load currents with an unbalanced RL load and Repetitive Controller.

The harmonic spectra of the load current in phase a is shown in Figure 5.48. As can be seen the waveform is sinusoidal and its harmonic distortion is very small. Details of the harmonic spectra can be seen in Figure 5.48(b). Note that for analysis purposes the plot has been zoomed-in and the axis y is expressed in mA, therefore the harmonic components shown in this figure are very small compared to the fundamental.



(a) Harmonic spectra with load unbalanced



(b) Details of the harmonic spectra with load unbalanced

Figure 5.48: Harmonic spectra of the load current in phase a. THD = 1.68%

5.4.5 Matrix Converter with Load Disconnected

The no load condition is the worst case in terms of controlling the output voltage because there is no power flowing to the load. A three-phase contactor is used to connect and disconnect the load. The Saber software package has been used to calculate the harmonic spectra and the Total Harmonic Distortion (THD).

5.4.5.1 Output Voltage of the Matrix Converter

The good performance of the control structure proposed is confirmed with the output voltage waveform obtained. The reference signal and the waveform obtained in phase a are shown in Figure 5.49. The reference signal cannot be seen clearly because it is exactly in phase with the output voltage signal. Both the amplitude and the phase are matched with the use of the Repetitive Controller. The harmonic spectra of the output voltage is shown in Figure 5.50. As can be seen the harmonic distortion is minimal compared to the fundamental component. A zoomed-in plot is shown in Figure 5.50(b) and indicates that the biggest harmonic component occurs at 2kHz and has a value of 0.4484 which compared to the fundamental component is only 0.90%. The Total Harmonic Distortion (THD) is 1.93% which meets the requirements imposed in the design of the Matrix Converter based power supply.

5.4.5.2 Input and Output Currents of the Matrix Converter

Figure 5.51 shows the waveform of the input current obtained when the load is disconnected. As can be seen its amplitude decreases because no power is applied to the load. The harmonic spectra of the input current is shown in Figure 5.52. The requirement for the THD of the input current is not completely satisfied because its value increases up to 5.56%. The biggest harmonic components are the 5th, the 9th, the 11th and the 13th as can be seen in Figure 5.52(b).

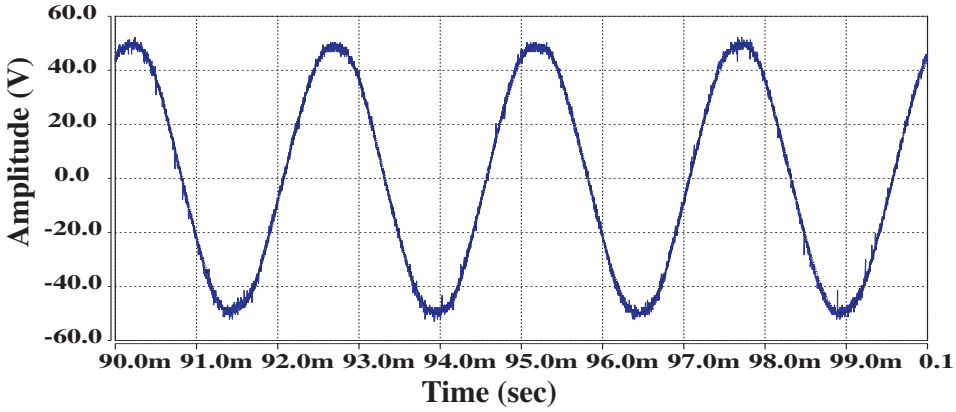
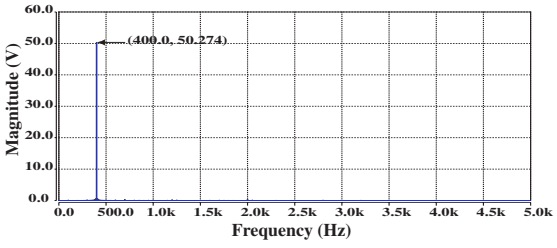
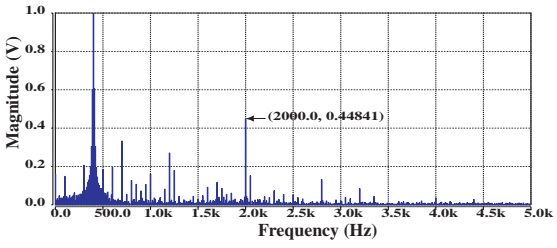


Figure 5.49: Output voltage in phase a with load disconnected and using Repetitive Controller.



(a) Harmonic spectra with load disconnected



(b) Details of the harmonic spectra with load disconnected

Figure 5.50: Harmonic spectra of output voltage in phase a. THD = 1.93%

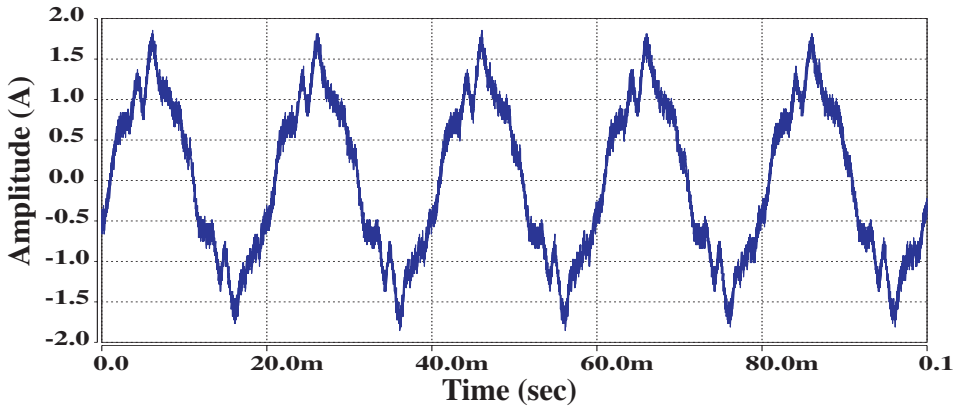
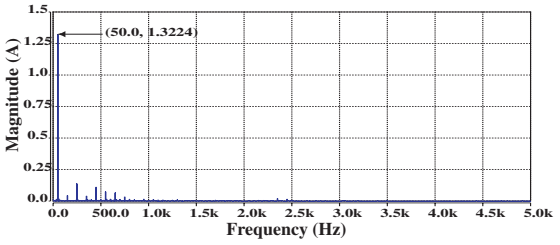
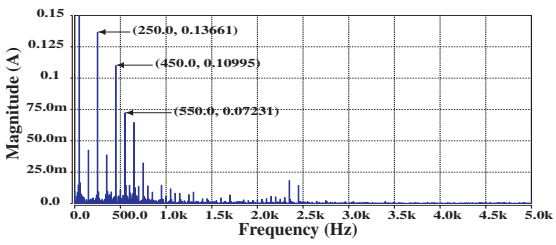


Figure 5.51: Input current in phase a with load disconnected and using Repetitive Controller.



(a) Harmonic spectra with load disconnected



(b) Details of the harmonic spectra with load disconnected

Figure 5.52: Harmonic spectra of input current in phase A. THD = 5.56%

The waveform of the Matrix Converter output current is shown in Figure 5.53 and its corresponding harmonic spectra can be seen in Figure 5.54. Figure 5.54(b) shows that the high frequency harmonics appear around multiples of the switching frequency. The details of the harmonic spectra shown in Figure 5.54(b) indicates that the biggest low harmonic component appears at 2kHz as well. In this case the Total Harmonic Distortion of the output current is calculated using Saber as 0.83%.

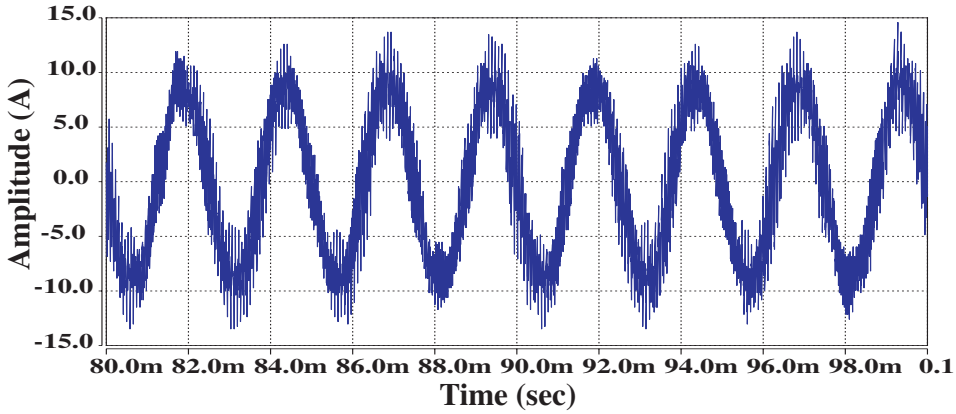
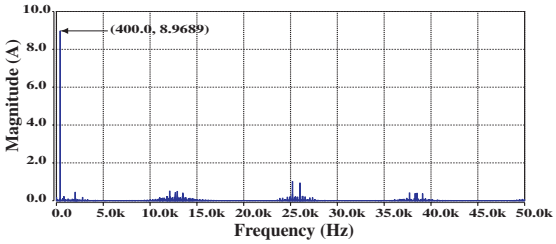
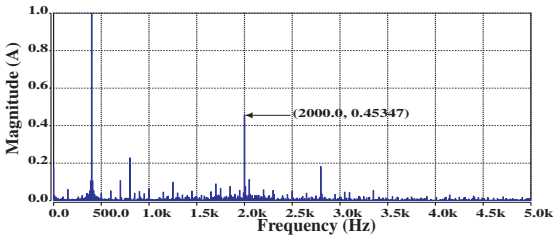


Figure 5.53: Matrix Converter output current in phase a with load disconnected and using Repetitive Controller.



(a) Harmonic spectra with load disconnected, phase a



(b) Details of the harmonic spectra with load disconnected, phase a

Figure 5.54: Harmonic spectra of MC output current in phase a. THD = 0.83%

No waveform of the current in the load is shown here because in this load condition no current is flowing through the load.

5.5 Summary

In this chapter details of the final tests of the Matrix Converter based power supply have been discussed. As soon as the implementation of the Matrix Converter was completed, its functionality and the communication between the Host PC, the DSP/FPGA board and finally the gate drive board were tested. This has been done by progressively testing the Matrix Converter performance when connecting it to, first a resistive-inductive balanced load without using a voltage controller, then using it to drive the same load but using a tracking controller in the d-q reference frame.

The next task performed consisted of testing the Matrix Converter system under unbalanced conditions, achieving gradually and successfully, the implementation of the tracking controller in the ABC reference frame. Then, the practical implementation of the output voltage Repetitive Controller was done in order to verify the control structure as presented in previous chapters. The performance of the Matrix Converter system using the Repetitive Control strategy and operating under unbalanced conditions and with the load disconnected was clearly illustrated and was as predicted in simulations.

The improvement in the quality of the input and output waveforms obtained by using the Repetitive Control was investigated in this chapter. By doing this, it can be confirmed the excellent property of the Repetitive Control strategy over the traditional control such as PI or PID control.

The performance of the Matrix Converter system employing the Repetitive Controller strategy was compared to the performance of the Matrix Converter System using only the second order tracking controller. From the experimental results obtained, it is concluded that the implementation of the control strategy proposed can be feasible in practice and has an acceptable control performance under different load conditions of operation of the Matrix Converter based power supply. A comparison of practical results obtained can be seen in Table 5.1.

	Tracking Controller	**Tracking Controller plus Repetitive Controller**
RL unbalanced load (THD in %)		
Input current	5.73	6.15
Matrix Converter current	0.86	0.61
Output voltage	2.31	2.15
Load current	2.10	1.68
Load disconnected (THD in %)		
Input current	6.34	5.56
Matrix Converter current	0.92	0.83
Output voltage	2.52	1.93
Load current	–	–

Table 5.1: THD of practical results in phase a with the tracking controller and the tracking controller plus the Repetitive Controller.

There were some problems in the practical implementation of the Matrix Converter system. The value of the gain representing the Matrix Converter block was found by trial and error. This task required a lot of time to find the suitable value. The load conditions were done with the components available in the facilities at the time of testing the prototype. This implies that the converter was not tested at full power. Finally, the prototype was tested to demonstrate that the performance of the control structure proposed is acceptable and results are very similar to those obtained in simulations.

Chapter 6

Conclusions

The work presented in this thesis has made an exciting contribution to the research applications of Matrix Converters. One interesting aspect of the development of Matrix Converter driven power supplies is the power electronics employed to drive loads which operate under different conditions. The novelty introduced by the work of this thesis is to offer an alternative topology of power converter, the Matrix Converter, to drive loads in different condition of operation, instead of the conventional Voltage Source Inverter (VSI) currently used in most power supply systems. In the conventional VSI, the multi-pulse (12 or 18) rectification stage, the DC link and associated input filters add volume and complexity, for example, electrolytic capacitors are temperature sensitive and therefore unreliable in the target application where the typical ambient temperature range varies between -55°C to +70°C. To create the equivalent capacitance sized for the DC link using film capacitors would require a considerable amount of space compared to electrolytic capacitors. This space is usually around 30% more of that used for the electrolytic capacitors.

As it has been shown that Matrix Converters are able to offer direct conversion, thus avoiding a DC conversion stage. The absence of a DC link in a Matrix Converter allows for an increase in the power density of the converter. It is possible to achieve bi-directional power flow with a Matrix Converter and by controlling the switching

devices appropriately, both output voltage and input current can be sinusoidal. This is only true if there are no power fluctuations in the load which would be fed to the input supply with a consequent distortion of the line currents. Switches with the capability of current flow both directions (to and from the load) must be used in order to permit the bi-directional power flow. This is an important issue which has been taken into consideration when looking at the characteristics of any application.

In order to optimize the design of the Matrix Converter system, which is going to operate as a power supply for aircraft applications, a detailed analysis using both Saber and Matlab/Simulink software packages were used to select the best topology of Matrix Converter system that could satisfy the specifications. When Saber was used, the Matrix Converter modulation and control were implemented by using the MAST language, which discretised the modulation strategies applied. As a result, the source code obtained from the simulation resembles the final program implemented on a DSP, thus facilitating the implementation of the digital control platform for the converter.

To experimentally verify the proposed control strategy for the Matrix Converter based power supply, a laboratory prototype was designed and constructed. The rig consists of a 3-phase to 3-phase direct AC-AC converter (Matrix Converter) which is used as the power conditioning core of the power supply, working in conjunction with input and output LC filters. The control of the experimental rig is performed by a cooperation between a Digital Signal Processor (DSP, TMS320C6713) and a Field Programmable Gate Array (FPGA) board. Data acquisition and pulse generation are coordinated by the FPGA board. The program implemented in the DSP is written in C using Code Composer Studio. Practical results show good performance of the proposed control strategy when implemented in the Matrix Converter based power supply operating at different loading conditions, besides the capability of bi-directional power flow of the converter.

6.1 Control of output voltage under unbalanced conditions

A control strategy has been investigated in order to drive a load under unbalanced conditions. In previous work, the d-q reference frame strategy has been successfully implemented. This strategy has a good performance when the load is balanced. The proposed tracking controller can be used to control the output voltage under unbalanced conditions using the ABC reference frame. The reference signal is given in the d-q reference frame and then they are transformed to the ABC reference frame by using the appropriate transformations. The three output voltages are measured separately (one voltage transducer per phase) and then compared to the ABC reference signals. Simulation and experimental results have proven that the proposed tracking controller can successfully cope with unbalanced conditions in the load as high as 40%. However, this unbalanced condition in the load causes degradation of the input current quality and consequently distortion of the input voltage. The Matrix Converter system has been tested using a resistive load as well as a resistive-inductive load. The tracking controller proposed is able to maintain the voltage across the output filter capacitor under any load condition, even if the abnormal condition of instant disconnection of full load, which is the worst case in terms of controlling the output voltage waveform.

6.2 Repetitive control strategy

The design and implementation of the Matrix Converter based power supply was not only an opportunity to achieving a practical realization which could respond to the strict requirements of the particular application. Indeed, it has also been an opportunity to design an improved control strategy for implementing the control of output voltage in Matrix Converter system, which even if inspired by it, is not dependant on the specific application. The use of a traditional linear digital control implementation

in the ABC stationary frame results in relevant steady-state amplitude and phase errors in the output voltage due to the control bandwidth limitation given the chosen sampling frequency of 12.8kHz and the target 400Hz output voltage. The use of a Repetitive Controller in conjunction with the ABC reference frame control has been considered as an alternative solution to solve this problem given the periodical nature of the control. The proposed structure employs the tracking controller previously designed in the ABC reference frame. A Repetitive Controller works by modifying the reference in order to compensate periodic errors or disturbances in the output. In the design of the Repetitive Controller several parameters are taken in account. One of the most important parameters is k (the number of samples taken in each reference period); this parameter is used in the design of the band-limit filter polynomial and in the calculation of the values of the delays required in the pre-delay filter and in the post-delay filter. The tracking controller has the role of stabilizing the closed loop system and determines the system transient performance. In this case it needs to be designed to meet a compromise in terms of stability and bandwidth. With the presence of the input filter, the Matrix Converter supply voltage becomes very distorted due to the distorted input currents before filtering. The presence of a Repetitive Controller also contributes to reduce this risk by compensating the distortion caused by these periodic disturbances.

6.3 Further work

Although the output voltage control based on Repetitive Controller has been successfully implemented on an experimental rig and its performance has been proven, the following are some of the interesting topics in which further research can be undertaken in order to archive a better design of the Matrix Converter system:

Input Filter Design . This needs more analysis of the power supply system at different input supply frequencies with different amount of supply distortion in order to characterize the values of L, C and R which generate the attenuation of

specific harmonics, whilst still trying to optimize the filter size. Different filter topologies could also be investigated with the aim of improving power quality whilst also improving the size and weights.

The effect of the filter design on the capacitive input power factor observed in simulation and experimentally needs to be addressed. It has mentioned that one of the advantage of using a Matrix Converter over other topologies of converters is (depending on the modulation method used) the possibility of controlling the input displacement factor, irrespective of the type of load. This means that it may be possible to compensate for the poor power factor due to the input filter using the Matrix Converter modulation. However, this would not be possible under no load conditions.

Stability of Control System . The design of the Repetitive Controller plays a very important role in the stability of the system. The higher the sampling frequency used the better the level of compensation of errors. The problem is that the DSP should be fast enough to execute all the instruction and apply the delays in one switching period of the output. Higher switching frequencies can make the control system design easier since the higher control bandwidth can be obtained, however this is at the expense of higher switching losses.

Investigation of factor 6 included in the tracking controller . The design of the tracking controller was done by considering the Matrix Converter as a block with a unity gain in the closed loop. When the designed tracking controller is implemented in the prototype this consideration does not work. Because of the electronic components used in the practical implementation, the block representing the Matrix Converter has a gain grater than unity and also it introduced some delays due to the time spent by the DSP in the execution of the control strategy. In practice, when the tracking controller is implemented in the DSP, a gain must be introduced in the control loop. By research experience and previous works developed, it has been suggested that the value of the gain representing the Matrix Converter is in the range of 5 to 6. More research should be carried out to find the way of calculating the value of this gain.

6.4 Publications resulting from the work

The work carried out over the course of this project has resulted in a paper being published in a conference. The published paper is listed at the end of this thesis in Appendix A.

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Appendix A

Paper Published

Lopez Arevalo S, Zanchetta P, Wheeler P W, "Control of a Matrix Converter-based AC Power Supply for Aircrafts under Unbalanced Conditions", *33rd Annual Conference of the IEEE Industrial Electronics Society (IECON'07), Taipei, Taiwan, R.O.C.*, November 2007.

Appendix B

Schematic Diagrams used in Saber

B.1 General Schematic Diagram of the System used in Saber Simulations

The general diagram used in Saber to simulate the Matrix Converter power supply can be seen in Figure B.1. This diagram includes all the components of system. Resistor r6 and r7 have a value of 10MΩ and they are used to isolate the system from ground. In Saber simulations, the model must be grounded in order to allow the algorithm to solve the equations. The arrangement of a big resistor connected to a ground point is acting as floating point with no connection.

B.2 Schematic Diagram of the Matrix Converter used in Saber Simulations

The schematic diagram of the Matrix Converter without the input and output filter can be seen in Figure B.2. This schematic diagram shows basically the modulator

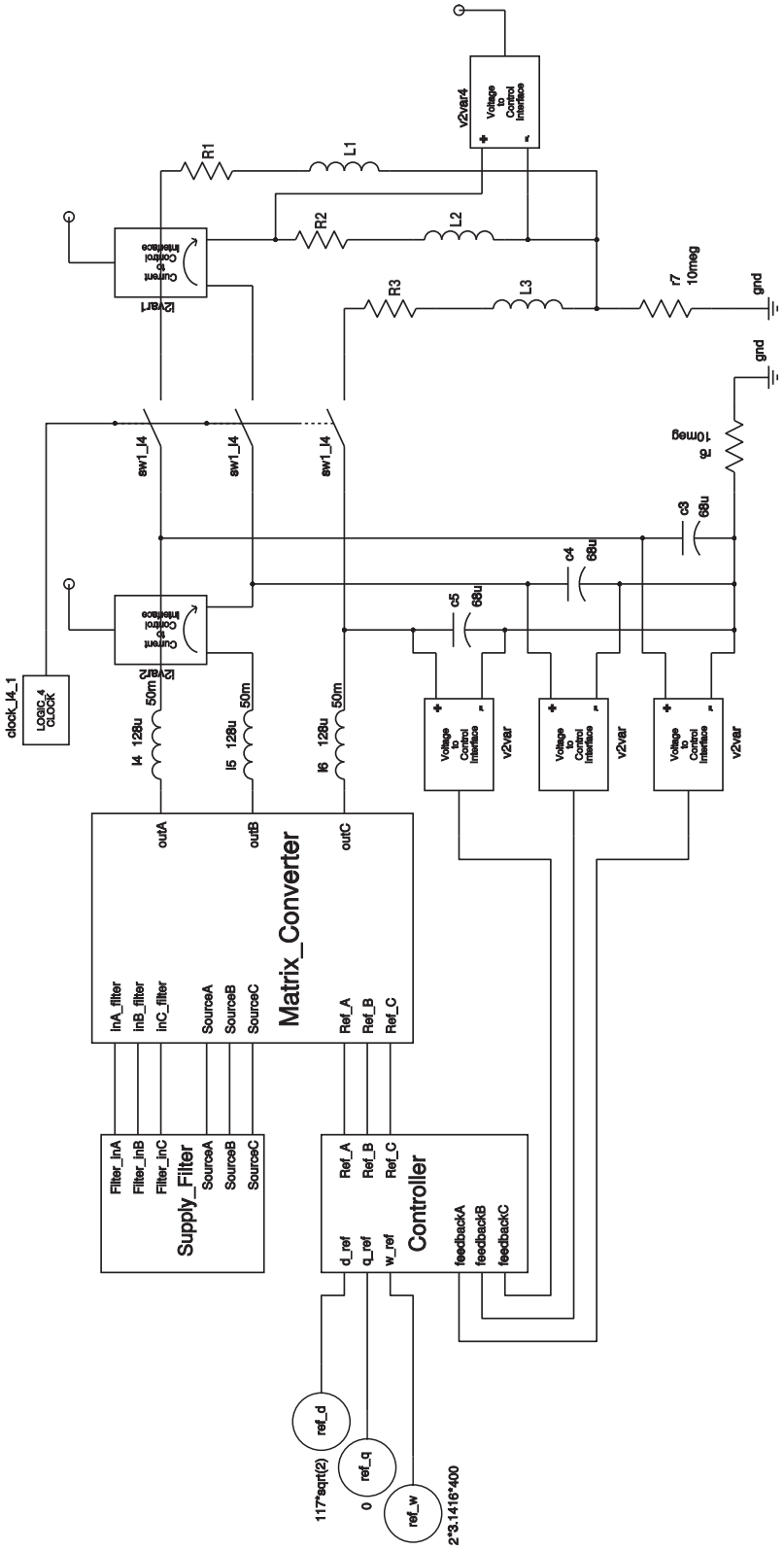

Figure B.1: Overall diagram of the whole Matrix Converter system used Saber.

and the Matrix Converter, which is the core of the power supply system.

B.3 Schematic Diagram of the Controller used in Saber Simulations

Figure B.3 shows the diagram of the controller used in the power supply system. This diagram employed in Saber simulations was used in the d-q reference frame control.

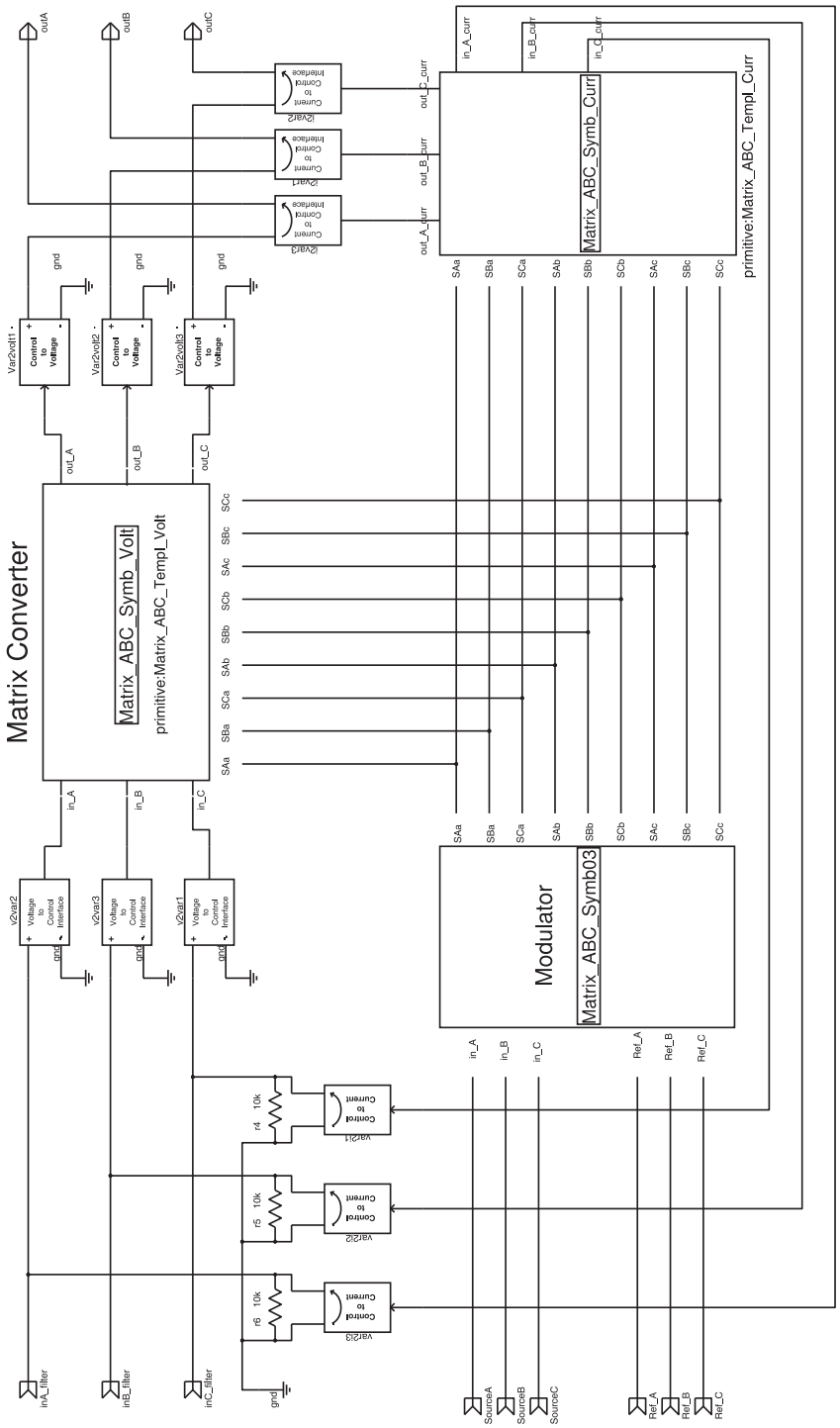

Figure B.2: Schematic diagram of the MC and modulator used in the power supply system.

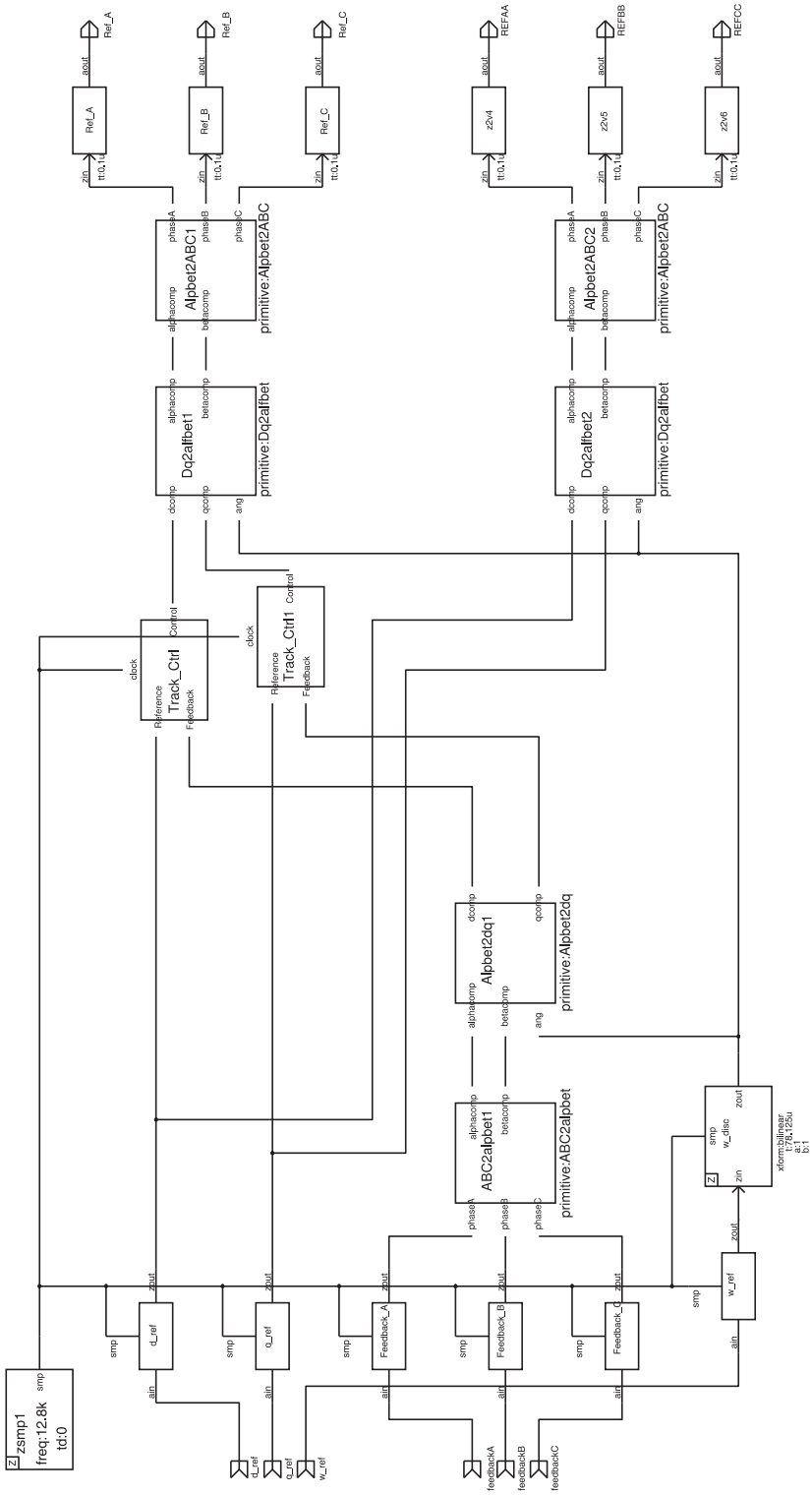

Figure B.3: Schematic diagram of the controller used in the power supply system.

Appendix C

Source Code using MAST Language

This appendix contains the codes written in MAST language for simulations in Saber. This appendix shows the source code for the modulator, the source code for determination of angles and sectors of both the input current vector and the output voltage vector and the code source for the bi-directional switches. Theses MAST codes are used in the simulations of the Matrix Converter system under different load conditions described in Chapter 3.

C.1 MAST Code used in the Modulator

```
#Template Space Vector Modulation#
template SVM_B  Kvv Kii alfa beta phi q SAa SAb SAc SBa SBb SBc SCa
SCb SCc = fc
ref nu phi, q
state logic_4 SAa, SAb, SAc, SBa, SBb, SBc, SCa, SCb, SCc
state nu Kvv, Kii, alfa, beta
number fc
{
```

```
var nu DI, DII, DIII, DIV, TI, TII, TIII, TIV, Tzero, Z1, Z2, Z3,
varia
state logic_4 awake_B, awake_BB
number Tc = (1/fc),
       pi = 3.1415926535
when(dc_init){
    schedule_event(time,SAa,l4_0)
    schedule_event(time,SBa,l4_0)
    schedule_event(time,SCa,l4_0)
    schedule_event(time,SAb,l4_0)
    schedule_event(time,SBb,l4_0)
    schedule_event(time,SCb,l4_0)
    schedule_event(time,SAc,l4_0)
    schedule_event(time,SBc,l4_0)
    schedule_event(time,SCc,l4_0)
    }
when(time_init){
    schedule_event(time,awake_B,l4_1)
    }
when(event_on(awake_B)){
#############setting of switches#########################
schedule_event(time,SAa,l4_0) schedule_event(time,SBa,l4_0)
schedule_event(time,SCa,l4_0) schedule_event(time,SAb,l4_0)
schedule_event(time,SBb,l4_0) schedule_event(time,SCb,l4_0)
schedule_event(time,SAc,l4_0) schedule_event(time,SBc,l4_0)
schedule_event(time,SCc,l4_0)
     if(((Kvv==1) & (Kii==1)) | ((Kvv==4) & (Kii==4))){
    schedule_event(time,SCa,l4_1)
    schedule_event(time+Z3,SCa,l4_0)
    schedule_event(time+Z3,SAa,l4_1)
    schedule_event(time+Z3+TIII+TI+Z1+TII+TIV,SAa,l4_0)
    schedule_event(time+Z3+TIII+TI+Z1+TII+TIV,SBa,l4_1)
    schedule_event(time+Z3+TIII+TI+Z1+TII+TIV+2*Z2,SBa,l4_0)
    schedule_event(time+Z3+TIII+TI+Z1+TII+TIV+2*Z2,SAa,l4_1)
    schedule_event(time+Z3+TIII+TI+Z1+TII+TIV+2*Z2+TIV+TII+Z1+TI+TIII,SAa,l4_0)
    schedule_event(time+Z3+TIII+TI+Z1+TII+TIV+2*Z2+TIV+TII+Z1+TI+TIII,SCa,l4_1)
    schedule_event(time,SCb,l4_1)
    schedule_event(time+Z3+TIII,SCb,l4_0)
```

```
    schedule_event(time+Z3+TIII,SAb,l4_1)
    schedule_event(time+Z3+TIII+TI+Z1+TII,SAb,l4_0)
    schedule_event(time+Z3+TIII+TI+Z1+TII,SBb,l4_1)
    schedule_event(time+Z3+TIII+TI+Z1+TII+TIV+2*Z2+TIV,SBb,l4_0)
    schedule_event(time+Z3+TIII+TI+Z1+TII+TIV+2*Z2+TIV,SAb,l4_1)
    schedule_event(time+Z3+TIII+TI+Z1+TII+TIV+2*Z2+TIV+TII+Z1+TI,SAb,l4_0)
    schedule_event(time+Z3+TIII+TI+Z1+TII+TIV+2*Z2+TIV+TII+Z1+TI,SCb,l4_1)
    schedule_event(time,SCc,l4_1)
    schedule_event(time+Z3+TIII+TI,SCc,l4_0)
    schedule_event(time+Z3+TIII+TI,SAc,l4_1)
    schedule_event(time+Z3+TIII+TI+Z1,SAc,l4_0)
    schedule_event(time+Z3+TIII+TI+Z1,SBc,l4_1)
    schedule_event(time+Z3+TIII+TI+Z1+TII+TIV+2*Z2+TIV+TII,SBc,l4_0)
    schedule_event(time+Z3+TIII+TI+Z1+TII+TIV+2*Z2+TIV+TII,SAc,l4_1)
    schedule_event(time+Z3+TIII+TI+Z1+TII+TIV+2*Z2+TIV+TII+Z1,SAc,l4_0)
    schedule_event(time+Z3+TIII+TI+Z1+TII+TIV+2*Z2+TIV+TII+Z1,SCc,l4_1)
    }
else if(((Kvv==1) & (Kii==2)) | ((Kvv==4) & (Kii==5))){
    schedule_event(time,SBa,l4_1)
    schedule_event(time+Z2+TI+TIII,SBa,l4_0)
    schedule_event(time+Z2+TI+TIII,SCa,l4_1)
    schedule_event(time+Z2+TI+TIII+Z3,SCa,l4_0)
    schedule_event(time+Z2+TI+TIII+Z3,SAa,l4_1)
    schedule_event(time+Z2+TI+TIII+Z3+TIV+TII+2*Z1+TII+TIV,SAa,l4_0)
    schedule_event(time+Z2+TI+TIII+Z3+TIV+TII+2*Z1+TII+TIV,SCa,l4_1)
    schedule_event(time+Z2+TI+TIII+Z3+TIV+TII+2*Z1+TII+TIV+Z3,SCa,l4_0)
    schedule_event(time+Z2+TI+TIII+Z3+TIV+TII+2*Z1+TII+TIV+Z3,SBa,l4_1)
    schedule_event(time,SBb,l4_1)
    schedule_event(time+Z2+TI,SBb,l4_0)
    schedule_event(time+Z2+TI,SCb,l4_1)
    schedule_event(time+Z2+TI+TIII+Z3+TIV,SCb,l4_0)
    schedule_event(time+Z2+TI+TIII+Z3+TIV,SAb,l4_1)
    schedule_event(time+Z2+TI+TIII+Z3+TIV+TII+2*Z1+TII,SAb,l4_0)
    schedule_event(time+Z2+TI+TIII+Z3+TIV+TII+2*Z1+TII,SCb,l4_1)
    schedule_event(time+Z2+TI+TIII+Z3+TIV+TII+2*Z1+TII+TIV+Z3+TIII,SCb,l4_0)
    schedule_event(time+Z2+TI+TIII+Z3+TIV+TII+2*Z1+TII+TIV+Z3+TIII,SBb,l4_1)
    schedule_event(time,SBc,l4_1)
    schedule_event(time+Z2,SBc,l4_0)
```

```
    schedule_event(time+Z2,SCc,l4_1)
    schedule_event(time+Z2+TI+TIII+Z3+TIV+TII,SCc,l4_0)
    schedule_event(time+Z2+TI+TIII+Z3+TIV+TII,SAc,l4_1)
    schedule_event(time+Z2+TI+TIII+Z3+TIV+TII+2*Z1,SAc,l4_0)
    schedule_event(time+Z2+TI+TIII+Z3+TIV+TII+2*Z1,SCc,l4_1)
    schedule_event(time+Z2+TI+TIII+Z3+TIV+TII+2*Z1+TII+TIV+Z3+TIII+TI,SCc,l4_0)
    schedule_event(time+Z2+TI+TIII+Z3+TIV+TII+2*Z1+TII+TIV+Z3+TIII+TI,SBc,l4_1)
    }
else if((Kvv==1 & Kii==3) | (Kvv==4 & Kii==6)){
    schedule_event(time,SAa,l4_1)
    schedule_event(time+Z1,SAa,l4_0)
    schedule_event(time+Z1,SBa,l4_1)
    schedule_event(time+Z1+TIII+TI+Z2+TII+TIV,SBa,l4_0)
    schedule_event(time+Z1+TIII+TI+Z2+TII+TIV,SCa,l4_1)
    schedule_event(time+Z1+TIII+TI+Z2+TII+TIV+2*Z3,SCa,l4_0)
    schedule_event(time+Z1+TIII+TI+Z2+TII+TIV+2*Z3,SBa,l4_1)
    schedule_event(time+Z1+TIII+TI+Z2+TII+TIV+2*Z3+TIV+TII+Z2+TI+TIII,SBa,l4_0)
    schedule_event(time+Z1+TIII+TI+Z2+TII+TIV+2*Z3+TIV+TII+Z2+TI+TIII,SAa,l4_1)
    schedule_event(time,SAb,l4_1)
    schedule_event(time+Z1+TIII,SAb,l4_0)
    schedule_event(time+Z1+TIII,SBb,l4_1)
    schedule_event(time+Z1+TIII+TI+Z2+TII,SBb,l4_0)
    schedule_event(time+Z1+TIII+TI+Z2+TII,SCb,l4_1)
    schedule_event(time+Z1+TIII+TI+Z2+TII+TIV+2*Z3+TIV,SCb,l4_0)
    schedule_event(time+Z1+TIII+TI+Z2+TII+TIV+2*Z3+TIV,SBb,l4_1)
    schedule_event(time+Z1+TIII+TI+Z2+TII+TIV+2*Z3+TIV+TII+Z2+TI,SBb,l4_0)
    schedule_event(time+Z1+TIII+TI+Z2+TII+TIV+2*Z3+TIV+TII+Z2+TI,SAb,l4_1)
    schedule_event(time,SAc,l4_1)
    schedule_event(time+Z1+TIII+TI,SAc,l4_0)
    schedule_event(time+Z1+TIII+TI,SBc,l4_1)
    schedule_event(time+Z1+TIII+TI+Z2,SBc,l4_0)
    schedule_event(time+Z1+TIII+TI+Z2,SCc,l4_1)
    schedule_event(time+Z1+TIII+TI+Z2+TII+TIV+2*Z3+TIV+TII,SCc,l4_0)
    schedule_event(time+Z1+TIII+TI+Z2+TII+TIV+2*Z3+TIV+TII,SBc,l4_1)
    schedule_event(time+Z1+TIII+TI+Z2+TII+TIV+2*Z3+TIV+TII+Z2,SBc,l4_0)
    schedule_event(time+Z1+TIII+TI+Z2+TII+TIV+2*Z3+TIV+TII+Z2,SAc,l4_1)
    }
else if((Kvv==1 & Kii==4) | (Kvv==4 & Kii==1)){
```

```
    schedule_event(time,SCa,l4_1)
    schedule_event(time+Z3+TI+TIII,SCa,l4_0)
    schedule_event(time+Z3+TI+TIII,SAa,l4_1)
    schedule_event(time+Z3+TI+TIII+Z1,SAa,l4_0)
    schedule_event(time+Z3+TI+TIII+Z1,SBa,l4_1)
    schedule_event(time+Z3+TI+TIII+Z1+TIV+TII+2*Z2+TII+TIV,SBa,l4_0)
    schedule_event(time+Z3+TI+TIII+Z1+TIV+TII+2*Z2+TII+TIV,SAa,l4_1)
    schedule_event(time+Z3+TI+TIII+Z1+TIV+TII+2*Z2+TII+TIV+Z1,SAa,l4_0)
    schedule_event(time+Z3+TI+TIII+Z1+TIV+TII+2*Z2+TII+TIV+Z1,SCa,l4_1)
    schedule_event(time,SCb,l4_1)
    schedule_event(time+Z3+TI,SCb,l4_0)
    schedule_event(time+Z3+TI,SAb,l4_1)
    schedule_event(time+Z3+TI+TIII+Z1+TIV,SAb,l4_0)
    schedule_event(time+Z3+TI+TIII+Z1+TIV,SBb,l4_1)
    schedule_event(time+Z3+TI+TIII+Z1+TIV+TII+2*Z2+TII,SBb,l4_0)
    schedule_event(time+Z3+TI+TIII+Z1+TIV+TII+2*Z2+TII,SAb,l4_1)
    schedule_event(time+Z3+TI+TIII+Z1+TIV+TII+2*Z2+TII+TIV+Z1+TIII,SAb,l4_0)
    schedule_event(time+Z3+TI+TIII+Z1+TIV+TII+2*Z2+TII+TIV+Z1+TIII,SCb,l4_1)
    schedule_event(time,SCc,l4_1)
    schedule_event(time+Z3,SCc,l4_0)
    schedule_event(time+Z3,SAc,l4_1)
    schedule_event(time+Z3+TI+TIII+Z1+TIV+TII,SAc,l4_0)
    schedule_event(time+Z3+TI+TIII+Z1+TIV+TII,SBc,l4_1)
    schedule_event(time+Z3+TI+TIII+Z1+TIV+TII+2*Z2,SBc,l4_0)
    schedule_event(time+Z3+TI+TIII+Z1+TIV+TII+2*Z2,SAc,l4_1)
    schedule_event(time+Z3+TI+TIII+Z1+TIV+TII+2*Z2+TII+TIV+Z1+TIII+TI,SAc,l4_0)
    schedule_event(time+Z3+TI+TIII+Z1+TIV+TII+2*Z2+TII+TIV+Z1+TIII+TI,SCc,l4_1)
    }
else if((Kvv==1 & Kii==5) | (Kvv==4 & Kii==2)){
    schedule_event(time,SBa,l4_1)
    schedule_event(time+Z2,SBa,l4_0)
    schedule_event(time+Z2,SCa,l4_1)
    schedule_event(time+Z2+TIII+TI+Z3+TII+TIV,SCa,l4_0)
    schedule_event(time+Z2+TIII+TI+Z3+TII+TIV,SAa,l4_1)
    schedule_event(time+Z2+TIII+TI+Z3+TII+TIV+2*Z1,SAa,l4_0)
    schedule_event(time+Z2+TIII+TI+Z3+TII+TIV+2*Z1,SCa,l4_1)
    schedule_event(time+Z2+TIII+TI+Z3+TII+TIV+2*Z1+TIV+TII+Z3+TI+TIII,SCa,l4_0)
    schedule_event(time+Z2+TIII+TI+Z3+TII+TIV+2*Z1+TIV+TII+Z3+TI+TIII,SBa,l4_1)
```

```
    schedule_event(time,SBb,l4_1)
    schedule_event(time+Z2+TIII,SBb,l4_0)
    schedule_event(time+Z2+TIII,SCb,l4_1)
    schedule_event(time+Z2+TIII+TI+Z3+TII,SCb,l4_0)
    schedule_event(time+Z2+TIII+TI+Z3+TII,SAb,l4_1)
    schedule_event(time+Z2+TIII+TI+Z3+TII+TIV+2*Z1+TIV,SAb,l4_0)
    schedule_event(time+Z2+TIII+TI+Z3+TII+TIV+2*Z1+TIV,SCb,l4_1)
    schedule_event(time+Z2+TIII+TI+Z3+TII+TIV+2*Z1+TIV+TII+Z3+TI,SCb,l4_0)
    schedule_event(time+Z2+TIII+TI+Z3+TII+TIV+2*Z1+TIV+TII+Z3+TI,SBb,l4_1)
    schedule_event(time,SBc,l4_1)
    schedule_event(time+Z2+TIII+TI,SBc,l4_0)
    schedule_event(time+Z2+TIII+TI,SCc,l4_1)
    schedule_event(time+Z2+TIII+TI+Z3,SCc,l4_0)
    schedule_event(time+Z2+TIII+TI+Z3,SAc,l4_1)
    schedule_event(time+Z2+TIII+TI+Z3+TII+TIV+2*Z1+TIV+TII,SAc,l4_0)
    schedule_event(time+Z2+TIII+TI+Z3+TII+TIV+2*Z1+TIV+TII,SCc,l4_1)
    schedule_event(time+Z2+TIII+TI+Z3+TII+TIV+2*Z1+TIV+TII+Z3,SCc,l4_0)
    schedule_event(time+Z2+TIII+TI+Z3+TII+TIV+2*Z1+TIV+TII+Z3,SBc,l4_1)
    }
else if((Kvv==1 & Kii==6) | (Kvv==4 & Kii==3)){
    schedule_event(time,SAa,l4_1)
    schedule_event(time+Z1+TI+TIII,SAa,l4_0)
    schedule_event(time+Z1+TI+TIII,SBa,l4_1)
    schedule_event(time+Z1+TI+TIII+Z2,SBa,l4_0)
    schedule_event(time+Z1+TI+TIII+Z2,SCa,l4_1)
    schedule_event(time+Z1+TI+TIII+Z2+TIV+TII+2*Z3+TII+TIV,SCa,l4_0)
    schedule_event(time+Z1+TI+TIII+Z2+TIV+TII+2*Z3+TII+TIV,SBa,l4_1)
    schedule_event(time+Z1+TI+TIII+Z2+TIV+TII+2*Z3+TII+TIV+Z2,SBa,l4_0)
    schedule_event(time+Z1+TI+TIII+Z2+TIV+TII+2*Z3+TII+TIV+Z2,SAa,l4_1)
    schedule_event(time,SAb,l4_1)
    schedule_event(time+Z1+TI,SAb,l4_0)
    schedule_event(time+Z1+TI,SBb,l4_1)
    schedule_event(time+Z1+TI+TIII+Z2+TIV,SBb,l4_0)
    schedule_event(time+Z1+TI+TIII+Z2+TIV,SCb,l4_1)
    schedule_event(time+Z1+TI+TIII+Z2+TIV+TII+2*Z3+TII,SCb,l4_0)
    schedule_event(time+Z1+TI+TIII+Z2+TIV+TII+2*Z3+TII,SBb,l4_1)
    schedule_event(time+Z1+TI+TIII+Z2+TIV+TII+2*Z3+TII+TIV+Z2+TIII,SBb,l4_0)
    schedule_event(time+Z1+TI+TIII+Z2+TIV+TII+2*Z3+TII+TIV+Z2+TIII,SAb,l4_1)
```

```
    schedule_event(time,SAc,l4_1)
    schedule_event(time+Z1,SAc,l4_0)
    schedule_event(time+Z1,SBc,l4_1)
    schedule_event(time+Z1+TI+TIII+Z2+TIV+TII,SBc,l4_0)
    schedule_event(time+Z1+TI+TIII+Z2+TIV+TII,SCc,l4_1)
    schedule_event(time+Z1+TI+TIII+Z2+TIV+TII+2*Z3,SCc,l4_0)
    schedule_event(time+Z1+TI+TIII+Z2+TIV+TII+2*Z3,SBc,l4_1)
    schedule_event(time+Z1+TI+TIII+Z2+TIV+TII+2*Z3+TII+TIV+Z2+TIII+TI,SBc,l4_0)
    schedule_event(time+Z1+TI+TIII+Z2+TIV+TII+2*Z3+TII+TIV+Z2+TIII+TI,SAc,l4_1)
    }
.
.       : all else if statements for Kvv = 2-6 and Kii = 1-6
        : remainder omitted for clarity
.
# else{
# schedule_event(time,SAa,l4_0)
# schedule_event(time,SBa,l4_0)
# schedule_event(time,SCa,l4_0)
# schedule_event(time,SAb,l4_0)
# schedule_event(time,SBb,l4_0)
# schedule_event(time,SCb,l4_0)
# schedule_event(time,SAc,l4_0)
# schedule_event(time,SBc,l4_0)
# schedule_event(time,SCc,l4_0)
# }
schedule_event(time+Tc,awake_B,l4_1)
} ###closes when(event_on(awake_B))
    equations{
    DI:    DI = (1.154700538)*q*cos(alfa - (pi/3))*cos(beta - (pi/3))/cos(phi)
    DII:  DII = (1.154700538)*q*cos(alfa - (pi/3))*cos(beta + (pi/3))/cos(phi)
    DIII:DIII = (1.154700538)*q*cos(alfa + (pi/3))*cos(beta - (pi/3))/cos(phi)
    DIV:  DIV = (1.154700538)*q*cos(alfa + (pi/3))*cos(beta + (pi/3))/cos(phi)
    TI:    TI = DI*0.5*Tc
    TII:  TII = DII*0.5*Tc
    TIII:TIII = DIII*0.5*Tc
    TIV:  TIV = DIV*0.5*Tc
    Tzero: Tzero = (0.5*Tc) - (TI+TII+TIII+TIV)
    Z1: Z1 = Tzero/3
```

```
    Z2: Z2 = Tzero/3
    Z3: Z3 = Tzero/3
    varia:varia=Z3+TIII+TI+Z1+TII
    }#closes equations
}###end main
```

C.2 MAST Code used in for the Input Current Vector

```
#Template Input Current Vector Angle#
template icvang in_A in_B in_C Kii beta Vim
ref nu in_A, in_B, in_C
var nu Vim
state nu Kii, beta
{
val nu ang
var nu smpaa, smpbb, smpcc, a_curr, b_curr
state nu awake_A
number pi = 3.1415926535
when(dc_init){
    schedule_event(time,Kii,0)
    schedule_event(time,beta,0)
    }
when(time_init){
    schedule_event(time,awake_A,1)
    }
when(awake_A){ #################current angle#################
     if((0*pi/6)<=ang & ang<(1*pi/6)){
    schedule_event(time,Kii,1)
    schedule_event(time,beta,ang)
        }
else if((1*pi/6)<=ang & ang<(3*pi/6)){
    schedule_event(time,Kii,2)
    schedule_event(time,beta,ang-(1*pi/3))
        }
```

```
else if((3*pi/6)<=ang & ang<(5*pi/6)){
    schedule_event(time,Kii,3)
    schedule_event(time,beta,ang-(2*pi/3))
        }
else if((5*pi/6)<=ang & ang<(7*pi/6)){
    schedule_event(time,Kii,4)
    schedule_event(time,beta,ang-(3*pi/3))
        }
else if((7*pi/6)<=ang & ang<(9*pi/6)){
    schedule_event(time,Kii,5)
    schedule_event(time,beta,ang-(4*pi/3))
        }
else if((9*pi/6)<=ang & ang<(11*pi/6)){
    schedule_event(time,Kii,6)
    schedule_event(time,beta,ang-(5*pi/3))
        }
else if((11*pi/6)<=ang & ang<(12*pi/6)){
    schedule_event(time,Kii,1)
    schedule_event(time,beta,ang-(6*pi/3))
        }
    else {
    schedule_event(time,Kii,0)
    schedule_event(time,beta,0)
        }
schedule_event(time,awake_A,1) } ### closes when(awake_A)
values{ ################input current vector####################
     if((a_curr>0.0001) & ((-0.0001<b_curr) & (b_curr<0.0001))){
    ang = 0
    }
else if((a_curr>0.0001) & (b_curr>0.0001)){
    ang = atan(b_curr/(a_curr+0.0001))
    }
else if(((-0.000001<a_curr) & (a_curr<0.0001)) & (b_curr>0.0001)){
    ang = pi/2
    }
else if((-0.0001>a_curr) & (b_curr>0.0001)){
    ang = pi+atan(b_curr/(a_curr+0.0001))
    }
```

```
else if((-0.0001>a_curr) & ((-0.0001<b_curr) & (b_curr<0.0001))){
    ang = pi
    }
else if((-0.0001>a_curr) & (-0.0001>b_curr)){
    ang = pi+atan(b_curr/(a_curr+0.0001))
    }
else if(((-0.0001<a_curr) & (a_curr<0.0001)) & (-0.0001>b_curr)){
    ang = (3*pi)/2
    }
else if((a_curr>0.0001) & (-0.0001>b_curr)){
    ang = (2*pi)+atan((b_curr)/(a_curr+0.0001))
    }
    else{
    ang=pi
    }
}###end values

equations{
    smpaa:smpaa = in_A
    smpbb:smpbb = in_B
    smpcc:smpcc = in_C
    a_curr:a_curr = (2/3)*(smpaa - 0.5*smpbb - 0.5*smpcc)
    b_curr:b_curr = (2/3)*(sqrt(3)/2)*(smpbb -  smpcc)
    Vim:Vim = sqrt(a_curr**2 + b_curr**2)
    }#closes equations
}###end main
```

C.3 MAST Code used in for the Output Voltage Vector

```
#Template Output Voltage Vector Angle#
template ovvang Ref_A Ref_B Ref_C Kvv alfa Vom
ref nu Ref_A, Ref_B, Ref_C
var nu Vom
state nu Kvv, alfa
```

```
{
val nu ang
var nu Vo11, Vo22, Vo33, a_volt, b_volt
state nu awake_A
number pi = 3.1415926535
when(dc_init){
    schedule_event(time,Kvv,0)
    schedule_event(time,alfa,0)
    }
when(time_init){
    schedule_event(time,awake_A,1)
    }
when(awake_A){ ################voltage angle#################
     if((0*pi/6)<=ang & ang<(1*pi/3)){
    schedule_event(time,Kvv,1)
    schedule_event(time,alfa,ang-(pi/6))
        }
else if((1*pi/3)<=ang & ang<(2*pi/3)){
    schedule_event(time,Kvv,2)
    schedule_event(time,alfa,ang-(3*pi/6))
        }
else if((2*pi/3)<=ang & ang<(3*pi/3)){
    schedule_event(time,Kvv,3)
    schedule_event(time,alfa,ang-(5*pi/6))
        }
else if((3*pi/3)<=ang & ang<(4*pi/3)){
    schedule_event(time,Kvv,4)
    schedule_event(time,alfa,ang-(7*pi/6))
        }
else if((4*pi/3)<=ang & ang<(5*pi/3)){
    schedule_event(time,Kvv,5)
    schedule_event(time,alfa,ang-(9*pi/6))
        }
else if((5*pi/3)<=ang & ang<(6*pi/3)){
    schedule_event(time,Kvv,6)
    schedule_event(time,alfa,ang-(11*pi/6))
        }
    else    {
```

```
    schedule_event(time,Kvv,0)
    schedule_event(time,alfa,0)
        }
schedule_event(time,awake_A,1) } ### closes when(awake_A)
values{ ###############output voltage vector###################
     if((a_volt>0.0001) & ((-0.0001<b_volt) & (b_volt<0.0001))){
    ang = 0
    }
else if((a_volt>0.0001) & (b_volt>0.0001)){
    ang = atan(b_volt/(a_volt+0.0001))
    }
else if(((-0.000001<a_volt) & (a_volt<0.0001)) & (b_volt>0.0001)){
    ang = pi/2
    }
else if((-0.0001>a_volt) & (b_volt>0.0001)){
    ang = pi+atan(b_volt/(a_volt+0.0001))
    }
else if((-0.0001>a_volt) & ((-0.0001<b_volt) & (b_volt<0.0001))){
    ang = pi
    }
else if((-0.0001>a_volt) & (-0.0001>b_volt)){
    ang = pi+atan(b_volt/(a_volt+0.0001))
    }
else if(((-0.0001<a_volt) & (a_volt<0.0001)) & (-0.0001>b_volt)){
    ang = (3*pi)/2
    }
else if((a_volt>0.0001) & (-0.0001>b_volt)){
    ang = (2*pi)+atan((b_volt)/(a_volt+0.0001))
    }
    else{
    ang=pi
    }
}###end values
equations{
    Vo11:Vo11=Ref_A
    Vo22:Vo22=Ref_B
    Vo33:Vo33=Ref_C
    a_volt:a_volt = (2/3)*(Vo11 - 0.5*Vo22 - 0.5*Vo33)
```

```
    b_volt:b_volt = (2/3)*(sqrt(3)/2)*(Vo22 -  Vo33)
    Vom:Vom = sqrt(a_volt**2 + b_volt**2)
    }#closes equations
}###end main
```

C.4 MAST Code used to model Bi-directional Switches

```
#Template Matrix_ABC_Templ_Volt#
template Matrix_ABC_Templ_Volt in_A in_B in_C out_A out_B out_C SAa
SBa SCa SAb SBb SCb SAc SBc SCc
var nu out_A, out_B, out_C
ref nu SAa, SBa, SCa, SAb, SBb, SCb, SAc, SBc, SCc
ref nu in_A, in_B, in_C
{
    equations{
    out_A: out_A = SAa*in_A + SBa*in_B + SCa*in_C
    out_B: out_B = SAb*in_A + SBb*in_B + SCb*in_C
    out_C: out_C = SAc*in_A + SBc*in_B + SCc*in_C
    }
}
```

Appendix D

Programs Implemented in the DSP

This Appendix contains the codes for program implemented in the DSP for this project. Theses programs are used in the implementation both the tracking controller and the Repetitive controller described in Chapter 4.

D.1 Main Program Implemented in the DSP

```
/*********************************************************************/
/***main.c for SVM and using host program with Matlab Interface***/
/*********************************************************************/
#include <stdio.h>
#include <math.h>
#include <c6x.h>
#include "c6x11dsk.h"
#include "timer_lib.h"
#include "FPGA.h"
#include "controller.h"
#include "constants.h"
#include "dsk6713.h"
#include "fastrts67x.h"
#define LENGTH_BUFFER           8000    //Lenght of an array in the
internal memory float buffer_int_memory[LENGTH_BUFFER];
```

```
/*TO ENABLE THE OUTPUT OF MCSP TO CPLD*/ unsigned char *mscb_mux=
(unsigned char*)0x90080006;
//Array gives vector codes PVE for vectors 0 to 21
unsigned int VCT[22] =
    {   0x004000,   //VCT [0], dummy for vectors to start from VCT[1]
        0x280000,   //VCT [1], +1
        0x020000,   //VCT [2], -1
        0x160000,   //VCT [3], +2
        0x290000,   //VCT [4], -2
        0x010000,   //VCT [5], +3
        0x140000,   //VCT [6], -3
        0x220000,   //VCT [7], +4
        0x080000,   //VCT [8], -4
        0x190000,   //VCT [9], +5
        0x260000,   //VCT[10], -5
        0x040000,   //VCT[11], +6
        0x110000,   //VCT[12], -6
        0x0A0000,   //VCT[13], +7
        0x200000,   //VCT[14], -7
        0x250000,   //VCT[15], +8
        0x1A0000,   //VCT[16], -8
        0x100000,   //VCT[17], +9
        0x050000,   //VCT[18], -9
        0x000000,   //VCT[19], O1
        0x2A0000,   //VCT[20], O2
        0x150000    //VCT[21], O3
    };
//***Variables used in timer0_init()***//
//***Variables used in timer1_init()***//
//***Variables used in init_FPGA()***//
//***Variables used in init_controller()***//
int SamplingOn = 1, DriveOn = 1; float Tseq_2, TWOTseq_Pulses_2;
unsigned int Tseq_Pulses, Tseq_Pulses_2; float Volt_phase_a_error,
Volt_phase_a_error_last1, Volt_phase_a_error_last2; float
Volt_phase_b_error, Volt_phase_b_error_last1,
Volt_phase_b_error_last2; float Volt_phase_c_error,
Volt_phase_c_error_last1, Volt_phase_c_error_last2; float
Volt_phase_a_ctrl, Volt_phase_a_ctrl_last1, Volt_phase_a_ctrl_last2;
```

```
float Volt_phase_b_ctrl, Volt_phase_b_ctrl_last1,
Volt_phase_b_ctrl_last2; float Volt_phase_c_ctrl,
Volt_phase_c_ctrl_last1, Volt_phase_c_ctrl_last2;
//***Variables used in init_default_sampling()***//
//***Variables used in reset_controller()***//
//***Variables used in init_ADCs()***//
int adc1, adc2, adc3, adc4, adc5, adc6, adc7, adc8, adc9;
float IgainA, IgainB, IgainC, VgainAB, VgainBC, Vgaina, Vgainb,
Vgainc;
float offset1, offset2, offset3, offset4, offset5, offset6, offset7,
offset8, offset9;
//***Variables used in init_McBSP0(void)***//
//***Variables used in pwm_isr()***//
unsigned int dpr0, dpr1, dpr2, dpr3, dpr4, dpr5, dpr6, dpr7, dpr8,
dpr9;
float Delta_Theta_In, Theta_In = 0.0;
float cos_Theta_In, cos_Theta_In_menos_2PI_3,
cos_Theta_In_menos_4PI_3;
float VAB_in_real, VBC_in_real;
float VAB_in, VBC_in;
float VA_in, VB_in, VC_in;
float Freq_in=50.0;
float Delta_Theta_Out, Theta_Out = 0.0;
float cos_Theta_Out, sin_Theta_Out;
float ia_out, ib_out, ic_out;
float Volt_d_ref=10.0;
float Volt_q_ref=0.0;
float Freq_out=400.0;
float Volt_alpha_ref, Volt_beta_ref;
float Volt_phase_a_ref, Volt_phase_b_ref, Volt_phase_c_ref;
float Volt_FB_a, Volt_FB_b, Volt_FB_c;
float Volt_phase_a_ctrl, Volt_phase_b_ctrl, Volt_phase_c_ctrl;
float a_curr, b_curr, atansp_in, icvang, beta, ang_volt;
int Ki;
float a_volt, b_volt, alfa, ang_curr;
int Kv; float Vi, Vo, q; //phi
float cos_alfa_menos_PI_3, cos_alfa_mas_PI_3, cos_beta_menos_PI_3,
cos_beta_mas_PI_3;
```

```
float eq_I, eq_II, eq_III, eq_IV;
unsigned int D0, D0_3, TWOD0_3, DI, DII,DIII, DIV;
float D_0, D_0_3, TWOD_0_3, D_I, D_II, D_III, D_IV;
float Kvv, Kii;
unsigned int int_delay;
////////////////////////////////////////////////
/*                  Functions                  */
////////////////////////////////////////////////
void timer0_init(); void timer1_init(); void init_FPGA(); void
init_controller(); void reset_controller(); void init_ADCs(); void
init_McBSP0(); void init_default_sampling(); void pwm_isr(); void
timer0_isr();
#include "host.h"
////////////////////////////////////////////////
/*  ================ main ================    */
////////////////////////////////////////////////
void main(void) {
    *mscb_mux = 3;
    timer0_init();
    *(unsigned int*)TIMER0_CTRL |= 0x00C0;
    //Reset & start Timer0
    timer1_init();
    *(unsigned int*)TIMER1_CTRL |= 0x00C0;
    //Reset & start Timer1
    *(unsigned volatile int *)PLL_CSR = 0x8;
    //Start reset PLL
    *(unsigned int*)TIMER1_COUNT = 0;
    //Set Timer1_Count to Zero
    *(unsigned int*)TIMER1_CTRL |= 0x00C0;
    //Start time
    while ((*(unsigned int *)TIMER1_COUNT)<3000);
    //Wait time
    *(unsigned volatile int *)PLL_M = 0x4;
    //PLL X4
    *(unsigned volatile int *)PLL_DIV0 = 0x00008000;
    //ENABLE THE DIV0 FOR 1
    *(unsigned volatile int *)PLL_CSR = 0x0;
    //End reset PLL
```

```
*(unsigned int*)TIMER1_COUNT = 0;
//Set Timer1_Count to Zero
*(unsigned int*)TIMER1_CTRL |= 0x00C0;
//Start timer
while ((*(unsigned int *)TIMER1_COUNT)<3000);
//Wait time
*(unsigned volatile int *)PLL_CSR |= 0x1;
//Start reset PLL
DSK6713_init();
//Initialize the board support library, must be first BSL call
host_init(78.125e-6);
//Sampling period for host program (in seconds)
for(i=0;i<LENGTH_BUFFER;i++)
    buffer_int_memory[i] = 0;
*(unsigned volatile int *)TIMER0_CTRL &= 0xFF3F;
//Hold the timer
CSR = 0x100;
//Control Status Register, Global disable maskable interrupts
puts("Global disable maskable interrupts !");
IER = 2;
//Interrupt Enable Register, Disable all interrupts except NMI
puts("Disable all interrupts except NMI !");
*(unsigned volatile int *)EMIF_GCR = 0x3360;
//EMIF global control
*(unsigned volatile int *)EMIF_CE0 = 0x30;
//EMIF CE0 control
*(unsigned volatile int *)EMIF_CE1 = 0xFFFFFF03;
//EMIF CE1 control, 8bit async
*(unsigned volatile int *)EMIF_CE2 = 0x30D3C321;
//FPGA memory space
*(unsigned volatile int *)EMIF_SDCTRL = 0x57116000;
//EMIF SDRAM control ZZ
*(unsigned volatile int *)EMIF_SDRP = 0x61A;
//EMIF SDRM refresh period
init_FPGA();
*(unsigned volatile int *)EXTPOL &= 0xFFFFFFFE;
//EXT INT4 triggered on rising edge
ICR = 0xFFFF;
```

```
    //Interrupt Clear Register
    IER |= 0x0010;
    //Interrupt Enable Register, Enable interrupt EXT_INT4 (pwm_isr)
    puts("EXT_INT4 enabled");
    IER |= 0x0002;
    //Interrupt Enable Register, NMIE = 1: enable NMIs
    CSR |= 0x1;
    //Control Status Register, GIE = 1: enable global interrupt
    puts("Global Interrupts Enabled !\n");
    init_ADCs();
    init_controller();
    *(unsigned int *)DPR1 = 0x150000; // PVT=0 => should last whole period
    *(unsigned int *)DPR1 = 0x150000; // PVT=0 => should last whole period
    init_McBSP0();
    //Enable PWM, 0x00004000 = 0000 0000 0000 0000 0100 0000 0000 0000
    *(unsigned int *)DPR0 |= 0x00004000;
    *(unsigned int *)TIMER1_COUNT = 0;      //Set Timer1_Count to Zero
    *(unsigned int *)TIMER1_CTRL |= 0x00C0; //Reset & Start timer
    while ((*(unsigned int *)TIMER1_COUNT)<15000);
    //Hold Timer1,           0x0000FF7F = 0000 0000 0000 0000 1111 1111 0111 1111
    *(unsigned int *)TIMER1_CTRL &= 0xFF7F;
    //Enable ESTOP circuit,  0x80000000 = 1000 0000 0000 0000 0000 0000 0000 0000
    *(unsigned int *)DPR9 |= 0x80000000;
  HPImsg(1);
  while (1)
    {
    if (message_sent)
        {
        HPImsg(7);
        decode_host_msg();
        message_sent = 0;
        }
    }
}   //End of main()
void timer0_init(void) {
    *(unsigned volatile int *)TIMER0_CTRL &= 0xFF3F;
    //Hold the timer
    *(unsigned volatile int *)TIMER0_CTRL |= 0x0200;
```

```
    //Use internal (CPU) clock (CLK) - 56.25MHz
    *(unsigned volatile int *)TIMER0_CTRL &= 0xFEFF;
    //Pulse mode
    *(unsigned volatile int *)TIMER0_PRD   = 0xFFFFFFFF;
    //Set period to maximum
    //(about 76.3549741333333428777051 sec)
    //Set period to 78.125 us, 4394 = 0x0000112A
    *(unsigned volatile int *)TIMER0_CTRL |= 0x0001;
    //FUNC=1 => timer signal STOUT is present on external pin
}
void timer1_init(void) {
    *(unsigned volatile int *)TIMER1_CTRL &= 0xFF3F;
    //Hold the timer
    *(unsigned volatile int *)TIMER1_CTRL |= 0x0200;
    //Use internal (CPU) clock (CLK) - 56.25MHz
    *(unsigned volatile int *)TIMER1_CTRL &= 0xFEFF;
    //Pulse mode
    *(unsigned volatile int *)TIMER1_PRD   = 0xFFFFFFFF;
    //Set period to maximum
    //(about 76.3549741333333428777051 sec)
    //Set period to 78.125 us, 4394 = 0x0000112A
}
void init_FPGA(void) {
    /*Reset all FPGA registers to zero*/
    *(unsigned int *)DPR0 = 0;
    *(unsigned int *)DPR1 = 0;
    *(unsigned int *)DPR2 = 0;
    *(unsigned int *)DPR3 = 0;
    *(unsigned int *)DPR4 = 0;
    *(unsigned int *)DPR5 = 0;
    *(unsigned int *)DPR6 = 0;
    *(unsigned int *)DPR7 = 0;
    *(unsigned int *)DPR8 = 0;
    *(unsigned int *)DPR9 = 0;
    *(unsigned int *)DPR0 |= 0x00000100;    //Emulate power on reset
    /*Set PWM period: 0xFCF3 = 0xFFFF- (781-1) => 10MHz/781 = 12.8kHz*/
    *(unsigned int *)DPR0 |= 0xFCF30000;
    //0xFCF30000 --> 12.8kHz; 0xFC180000--> 10.0kHz
```

```
    /*PWM Reset*/
    *(unsigned int *)DPR0 |= 0x00008000;
    *(unsigned int *)DPR0 |= 0x0000C000;
    *(unsigned int *)DPR0 &= 0xFFFFBFFF;
    *(unsigned int *)DPR0 &= 0xFFFF3FFF;
    //Set PWM level to 6,    0x00000C00 = 0000 0000 0000 0000 0000 1100 0000 0000
    *(unsigned int *)DPR0 |= 0x00000C00;
    /*Set Watchdog Period: 0xFB6D = 0xFFFF - (1171.0-1) => 10MHz/1171.5 = 8536.064874Hz,
    approx. 1.5*PWM period*/
    *(unsigned int *)DPR9 = 0xFB6D;//0xFB6D --> (1.5)*78.125us; 0xFA24 --> (1.5)*100us
    /*set state machine timers*/
    *(unsigned int *)DPR2 = 0x00300C03; //bin = 0000 0000 0011 0000 0000 1100 0000 0011
}
void init_controller(void)
{
SamplingOn = 0; DriveOn = 0;
Tseq_2 = (0.5)*(78.125e-6); // = 39.0625e-6;  = (1/(2*FSW));
Tseq_Pulses = 2*Tseq_2*FPGA_CLOCK + 0.5;
//FPGA clock pulses in one modulation period Tseq_Pulses_2 =
(0.5*Tseq_Pulses)+0.5;
TWOTseq_Pulses_2 = (float)(2*Tseq_Pulses_2);
Volt_phase_a_error_last2=0; Volt_phase_a_error_last1=0;
Volt_phase_a_ctrl_last2=0; Volt_phase_a_ctrl_last1=0;
Volt_phase_b_error_last2=0; Volt_phase_b_error_last1=0;
Volt_phase_b_ctrl_last2=0; Volt_phase_b_ctrl_last1=0;
Volt_phase_c_error_last2=0; Volt_phase_c_error_last1=0;
Volt_phase_c_ctrl_last2=0; Volt_phase_c_ctrl_last1=0;
}
void init_default_sampling(void)
{
}
void reset_controller(void)
{
Volt_phase_a_error_last2 = 0; Volt_phase_a_error_last1 = 0;
Volt_phase_a_ctrl_last2 = 0; Volt_phase_a_ctrl_last1 = 0;
Volt_phase_b_error_last2 = 0; Volt_phase_b_error_last1 = 0;
Volt_phase_b_ctrl_last2 = 0; Volt_phase_b_ctrl_last1 = 0;
Volt_phase_c_error_last2 = 0; Volt_phase_c_error_last1 = 0;
```

```
Volt_phase_c_ctrl_last2 = 0; Volt_phase_c_ctrl_last1 = 0;
}
void init_ADCs(void)
{
int x; int sum1, sum2, sum3, sum4, sum5, sum6, sum7, sum8, sum9;
IgainA=IGAINA; IgainB=IGAINB; IgainC=IGAINC; VgainAB=VGAINAB;
VgainBC=VGAINBC; Vgaina=VGAINA; Vgainb=VGAINB; Vgainc=VGAINC;
sum1=0; sum2=0; sum3=0; sum4=0; sum5=0; sum6=0; sum7=0; sum8=0;
sum9=0;
for(x=0;x<1;x++)
    {
    *(unsigned int *)DPR3 |= 0x1;
    while ((*(unsigned int *)DPR1)&0x0080);
    //Wait for completion of ADC conversion
    /*Read adc1 to adc5*/
    adc1 = (*(unsigned int *)DPR3)&0x0FFF;
    if(adc1&0x0800)
        adc1 |= 0xFFFFF000;
    adc2 = *(unsigned int *)DPR4;
    adc3 = (adc2&0x0FFF0000)>>16;
    if(adc3&0x0800)
        adc3 |= 0xFFFFF000;
    adc2 &= 0x0FFF;
    if(adc2&0x0800)
        adc2 |= 0xFFFFF000;
    adc4 = *(unsigned int *)DPR5;
    adc5 = (adc4&0x0FFF0000)>>16;
    if(adc5&0x0800)
        adc5 |= 0xFFFFF000;
    adc4 &= 0x0FFF;
    if(adc4&0x0800)
        adc4 |= 0xFFFFF000;
    adc6 = *(unsigned int *)DPR6;
    adc7 = (adc6&0x0FFF0000)>>16;
    if(adc7&0x0800)
        adc7 |= 0xFFFFF000;
    adc6 &= 0x0FFF;
    if(adc6&0x0800)
```

```
        adc6 |= 0xFFFFF000;
    adc8 = *(unsigned int *)DPR7;
    adc9 = (adc8&0x0FFF0000)>>16;
    if(adc9&0x0800)
        adc9 |= 0xFFFFF000;
    adc8 &= 0x0FFF;
    if(adc8&0x0800)
        adc8 |= 0xFFFFF000;
    sum1+=adc1;
    sum2+=adc2;
    sum3+=adc3;
    sum4+=adc4;
    sum5+=adc5;
    sum6+=adc6;
    sum7+=adc7;
    sum8+=adc8;
    sum9+=adc9;
    *(unsigned int *)TIMER0_COUNT = 0;
    *(unsigned int *)TIMER0_CTRL |= 0x00C0;
    //Start timer0
    while ((*(unsigned int *)TIMER0_COUNT)<4000);
    //Wait for CPU clock cycles
    *(unsigned int *)TIMER0_CTRL &= 0xFF7F;
    //Hold timer
    }
offset1 = (float)sum1/1.0;
offset2 = (float)sum2/1.0;
offset3 = (float)sum3/1.0;
offset4 = (float)sum4/1.0;
offset5 = (float)sum5/1.0;
offset6 = (float)sum6/1.0;
offset7 = (float)sum7/1.0;
offset8 = (float)sum8/1.0;
offset9 = (float)sum9/1.0;
}
/* Initializing multi channel buffered serial port McBSP0 */
void init_McBSP0(void)
{
```

```
    *(unsigned volatile int *)McBSP0_SPCR &= 0xFF3EFFFE;
    //Reset following: FSRT, GRST, XRST  & RRST
    *(unsigned volatile int *)McBSP0_SRGR = 0x2000000C;
    //0x50630C07 for FPGA CLKS (10MHz)
    *(unsigned volatile int *)McBSP0_SPCR &= 0xFFFFF7FF;
    *(unsigned volatile int *)McBSP0_SPCR |= 0x00001000;
    //Initialise remaining fields of SPCR
    *(unsigned volatile int *)McBSP0_PCR &= 0xFFFFFFFD;
    *(unsigned volatile int *)McBSP0_PCR |= 0x00001B09;
    //FSX ACTIVE LOW, data transmitted at rising edge
    *(unsigned volatile int *)McBSP0_XCR = 0x00050040;
    //SINGLE PHASE frame, 16 bits, 1-bit delay
    *(unsigned int *)TIMER0_COUNT = 0;
    *(unsigned int *)TIMER0_CTRL |= 0x00C0;
    //Start timer
    while ((*(unsigned int *)TIMER0_COUNT)<2);
    //Wait for 8 CPU clock cycles
    *(unsigned int *)TIMER0_CTRL &= 0xFF7F;
    //Hold timer
    *(unsigned volatile int *)McBSP0_SPCR |= 0x00400000;
    //Set GRST=1, Sample-rate
    //generator is taken out of reset
    *(unsigned int *)TIMER0_COUNT = 0;
    *(unsigned int *)TIMER0_CTRL |= 0x00C0;
    //Start timer
    while ((*(unsigned int *)TIMER0_COUNT)<6);
    //Wait for 24 CPU clock cycles
    *(unsigned int *)TIMER0_CTRL &= 0xFF7F;
    //Hold timer
    *(unsigned volatile int *)McBSP0_SPCR |= 0x00010000;
    //Set XRST=1, serial port
    //transmitter is enabled
}
/* pwm0_isr() - interrupt service routine generating PWM */
interrupt void pwm_isr(void)
{
DataSetting(); //Start data transmission settings
*(unsigned int *)DPR3 |= 0x1;               //Start A2D conversion
```

```
*(unsigned int*)TIMER0_COUNT = 0;           //Start timing
*(unsigned int*)TIMER0_CTRL |= 0x00C0;
/*Output storage scope trigger*/
*(unsigned int *)DPR9 |= 0x10000000;
/*Service & enable Watchdog*/
*(unsigned int *)DPR9 |= 0x00030000;
/*Extract information from FPGA registers*/
dpr0 = *(unsigned int *)DPR0;
dpr1 = *(unsigned int *)DPR1;
dpr2 = *(unsigned int *)DPR2;
dpr3 = *(unsigned int *)DPR3;
dpr4 = *(unsigned int *)DPR4;
dpr5 = *(unsigned int *)DPR5;
dpr6 = *(unsigned int *)DPR6;
dpr7 = *(unsigned int *)DPR7;
dpr8 = *(unsigned int *)DPR8;
dpr9 = *(unsigned int *)DPR9;
if((dpr3&0x00080000)||(dpr8))
    DriveOn=0;
else if(!DriveOn)
    {
    reset_controller();
    DriveOn=1;
    /*Enable State Machine*/
    *(unsigned int *)DPR3 |= 0x00070000;// 0x00070000 --> enable all 3 outputs,
                                        // 0x00010000 --> enable output phase a,
                                        // 0x00020000 --> enable output phase b,
                                        // 0x00040000 --> enable output phase c,
    }
if(dpr8)
    *(unsigned int *)DPR8 |= 0x00008000;
if((!(dpr3&0x00100000))&&(dpr3&0x00080000))
    *(unsigned int *)DPR8 &= 0xFFFF0000;
/*Read all output currents, line-line input voltages and phase
output voltages*/
adc1 = dpr3&0x0FFF; if(adc1&0x0800)
    adc1 |= 0xFFFFF000;
//adc2 = *(unsigned int *)DPR4;
```

```
adc3 = (dpr4&0x0FFF0000)>>16; if(adc3&0x0800)
    adc3 |= 0xFFFFF000;
adc2 = dpr4&0x0FFF; if(adc2&0x0800)
    adc2 |= 0xFFFFF000;
//adc4 = *(unsigned int *)DPR5;
adc5 = (dpr5&0x0FFF0000)>>16; if(adc5&0x0800)
    adc5 |= 0xFFFFF000;
adc4 = dpr5&0x0FFF; if(adc4&0x0800)
    adc4 |= 0xFFFFF000;
//adc6 = *(unsigned int *)DPR6;
adc7 = (dpr6&0x0FFF0000)>>16; if(adc7&0x0800)
    adc7 |= 0xFFFFF000;
adc6 = dpr6&0x0FFF; if(adc6&0x0800)
    adc6 |= 0xFFFFF000;
//adc8 = *(unsigned int *)DPR7;
adc9 = (dpr7&0x0FFF0000)>>16; if(adc9&0x0800)
    adc9 |= 0xFFFFF000;
adc8 = dpr7&0x0FFF; if(adc8&0x0800)
    adc8 |= 0xFFFFF000;
/*SCALE LINE TO LINE INPUT VOLTAGE ADC RESULTS*/
VAB_in=(float)(adc1-offset1)*VgainAB;
VBC_in=(float)(adc2-offset2)*VgainBC;
/***INPUT VOLTAGE VECTOR***/
/*pf = 1.0 --> Input Current == Input Voltage Extract input voltage
information from line-line input samples*/
VA_in=(2*VAB_in+VBC_in)/3;
VB_in=VA_in-VAB_in;
VC_in=-VA_in-VB_in;
a_curr = (TWO_3)*(VA_in-0.5*VB_in-0.5*VC_in);
b_curr = (I_SQRT3)*(VB_in-VC_in);
Vi = sqrtsp(a_curr*a_curr+b_curr*b_curr);
atansp_in=atansp(b_curr/a_curr);
if((a_curr>0) && (b_curr==0))
    icvang = 0.0;
else if((a_curr>0) && (b_curr>0))
    icvang = atansp_in;
else if((a_curr==0) && (b_curr>0))
    icvang = 0.5*PI;
```

```
else if((a_curr<0) && (b_curr>0))
    icvang = PI + atansp_in;
else if((a_curr<0) && (b_curr==0))
    icvang = PI;
else if((a_curr<0) && (b_curr<0))
    icvang = PI + atansp_in;
else if((a_curr==0) && (b_curr<0))
    icvang = 1.5*PI;
else if((a_curr>0) && (b_curr<0))
    icvang = 2*PI + atansp_in;
else
    icvang = atansp_in;
Ki=(icvang+PI_2)/PI_3;
Ki=((Ki==7)?1:Ki);
ang_curr=((float)Ki-1)*PI_3;
beta=icvang-ang_curr;
beta=((beta>PI)?(beta-TWOPI):beta);
/*SCALE CURRENT ADC RESULTS*/
ia_out = (float)(adc3-offset3)*IgainA;
ib_out = (float)(adc4-offset4)*IgainB;
ic_out = (float)(adc5-offset5)*IgainC;
if ((ia_out>IMAX)||(-ia_out>IMAX)||(ib_out>IMAX)||
(-ib_out>IMAX)||(ic_out>IMAX)||(-ic_out>IMAX))
    {
    *(unsigned int *)DPR8 |= 0x0001;
    DriveOn=0;
    *(unsigned int *)DPR3 &= 0xFFF8FFFF; //disable state machine
    }
/**********REFERENCES SIGNALS FOR EACH PHASE**************/
/********************** SET UP*****************************/
Delta_Theta_Out = (TWOPI*Freq_out)/(FSW);
Theta_Out+=Delta_Theta_Out;
Theta_Out=((Theta_Out>=TWOPI)?(Theta_Out-TWOPI):Theta_Out);
cos_Theta_Out=cossp(Theta_Out); sin_Theta_Out=sinsp(Theta_Out);
//Conversion of references from d-q to alpha-beta
Volt_alpha_ref=Volt_d_ref*cos_Theta_Out-Volt_q_ref*sin_Theta_Out;
Volt_beta_ref= Volt_d_ref*sin_Theta_Out+Volt_q_ref*cos_Theta_Out;
//Conversion of references from alpha-beta to ABC
```

```
Volt_phase_a_ref=Volt_alpha_ref;
Volt_phase_b_ref=1.5*(-ONE_3*Volt_alpha_ref+I_SQRT3*Volt_beta_ref);
Volt_phase_c_ref=1.5*(-ONE_3*Volt_alpha_ref-I_SQRT3*Volt_beta_ref);
//Scale phase output voltage (feedback signals) adc results
Volt_FB_a=(float)((adc9-offset9)*Vgaina);
Volt_FB_b=(float)((adc8-offset8)*Vgainb-0.175);
Volt_FB_c=(float)((adc7-offset7)*Vgainc);
/*No Controller, phase a*/
Volt_phase_a_ctrl=Volt_phase_a_ref;
if(-62<Volt_phase_a_ctrl && Volt_phase_a_ctrl<62)
    Volt_phase_a_ctrl=Volt_phase_a_ctrl;
else
    Volt_phase_a_ctrl=60;
/*No Controller, phase b*/
Volt_phase_b_ctrl=Volt_phase_b_ref;
if(-62<Volt_phase_b_ctrl && Volt_phase_b_ctrl<62)
    Volt_phase_b_ctrl=Volt_phase_b_ctrl;
else
    Volt_phase_b_ctrl=60;
/*No Controller, phase c*/
Volt_phase_c_ctrl=Volt_phase_c_ref;
if(-62<Volt_phase_c_ctrl && Volt_phase_c_ctrl<62)
    Volt_phase_c_ctrl=Volt_phase_c_ctrl;
else
    Volt_phase_c_ctrl=60;
/**********************END OF*********************************/
/************REFERENCES SIGNALS FOR EACH PHASE****************/
/***TARGET VOLTAGE VECTOR***/ a_volt =
(TWO_3)*(Volt_phase_a_ctrl-0.5*Volt_phase_b_ctrl-0.5*Volt_phase_c_ctrl);
b_volt = (I_SQRT3)*(Volt_phase_b_ctrl-Volt_phase_c_ctrl);
Vo=sqrtsp(a_volt*a_volt + b_volt*b_volt); /***TARGET VOLTAGE ANGLE
AND SECTORS***/ Kv=(Theta_Out+PI_3)/PI_3;
ang_volt=((float)Kv-0.5)*PI_3; alfa=Theta_Out-ang_volt;
Kii=(float)Ki; Kvv=(float)Kv; q=Vo/Vi;    //Modulation index
if(q>0.75)
    q=0.75;
cos_alfa_menos_PI_3=cossp(alfa - PI_3);
cos_alfa_mas_PI_3=cossp(alfa + PI_3);
```

```
cos_beta_menos_PI_3=cossp(beta - PI_3);
cos_beta_mas_PI_3=cossp(beta + PI_3);
//phi= (0.000001/180)*PI;
//cos_phi=cossp(phi);
      eq_I = 1.154700538*q*cos_alfa_menos_PI_3*cos_beta_menos_PI_3; // cos_phi
     eq_II = 1.154700538*q*cos_alfa_menos_PI_3*cos_beta_mas_PI_3;   // cos_phi
    eq_III = 1.154700538*q*cos_alfa_mas_PI_3*cos_beta_menos_PI_3;   // cos_phi
     eq_IV = 1.154700538*q*cos_alfa_mas_PI_3*cos_beta_mas_PI_3;     // cos_phi
      DI = Tseq_Pulses_2*eq_I + 0.5;
     DII = Tseq_Pulses_2*eq_II + 0.5;
    DIII = Tseq_Pulses_2*eq_III + 0.5;
     DIV = Tseq_Pulses_2*eq_IV + 0.5;
D0 = (Tseq_Pulses_2) - (DI+DII+DIII+DIV);
D0_3 = ONE_3*D0 + 0.5;
TWOD0_3 = 2*D0_3;
D_I = (float)DI;
D_II = (float)DII;
D_III = (float)DIII;
D_IV =(float)DIV;
D_0 = (float)D0;
D_0_3 = (float)D0_3;
TWOD_0_3 = (float)TWOD0_3;
/***PLACE VECTOR INFORMATION INTO PGFA FIFO***/
pVS=&VS[Ki-1] [Kv-1];
if (!DriveOn)
    *(unsigned int *)DPR1 = (VCT[21]); // PVT=0 => should last whole period
else
    {
    if((Ki+Kv)&1) //if (Ki+Kv) is odd
        {
        //Only load vectors with non-zero times
                    *(unsigned int *)DPR1 = (VCT[(*pVS)[0]])|D0_3;
        if(DI>1)    *(unsigned int *)DPR1 = (VCT[(*pVS)[1]])|DI;
        if(DIII>1)  *(unsigned int *)DPR1 = (VCT[(*pVS)[2]])|DIII;
                    *(unsigned int *)DPR1 = (VCT[(*pVS)[3]])|D0_3;
        if(DIV>1)   *(unsigned int *)DPR1 = (VCT[(*pVS)[4]])|DIV;
        if(DII>1)   *(unsigned int *)DPR1 = (VCT[(*pVS)[5]])|DII;
                    *(unsigned int *)DPR1 = (VCT[(*pVS)[6]])|TWOD0_3;
```

```
        if(DII>1)   *(unsigned int *)DPR1 = (VCT[(*pVS)[7]])|DII;
        if(DIV>1)   *(unsigned int *)DPR1 = (VCT[(*pVS)[8]])|DIV;
                    *(unsigned int *)DPR1 = (VCT[(*pVS)[9]])|D0_3;
        if(DIII>1)  *(unsigned int *)DPR1 = (VCT[(*pVS)[10]])|DIII;
        if(DI>1)    *(unsigned int *)DPR1 = (VCT[(*pVS)[11]])|DI;
                    *(unsigned int *)DPR1 = (VCT[(*pVS)[12]]);
                    // PVT =0 for last vector
        }
    else //if (Ki+Kv) is even
        {
                    *(unsigned int *)DPR1 = (VCT[(*pVS)[0]])|D0_3;
        if(DIII>1)  *(unsigned int *)DPR1 = (VCT[(*pVS)[1]])|DIII;
        if(DI>1)    *(unsigned int *)DPR1 = (VCT[(*pVS)[2]])|DI;
                    *(unsigned int *)DPR1 = (VCT[(*pVS)[3]])|D0_3;
        if(DII>1)   *(unsigned int *)DPR1 = (VCT[(*pVS)[4]])|DII;
        if(DIV>1)   *(unsigned int *)DPR1 = (VCT[(*pVS)[5]])|DIV;
                    *(unsigned int *)DPR1 = (VCT[(*pVS)[6]])|TWOD0_3;
        if(DIV>1)   *(unsigned int *)DPR1 = (VCT[(*pVS)[7]])|DIV;
        if(DII>1)   *(unsigned int *)DPR1 = (VCT[(*pVS)[8]])|DII;
                    *(unsigned int *)DPR1 = (VCT[(*pVS)[9]])|D0_3;
        if(DI>1)    *(unsigned int *)DPR1 = (VCT[(*pVS)[10]])|DI;
        if(DIII>1)  *(unsigned int *)DPR1 = (VCT[(*pVS)[11]])|DIII;
                    *(unsigned int *)DPR1 = (VCT[(*pVS)[12]]);
                    // PVT =0 for last vector
        }
   }
*(unsigned int *)TIMER0_CTRL &= 0xFF7F; //Hold timer
int_delay = *(unsigned int *)TIMER0_COUNT;
DataCapture(); //Store data in external memory, used in host program
}
interrupt void timer0_isr(void) { puts("\n INT14 is working"); }
```

D.2 Code of the Tracking Controller Implementation

```
/*******************START OF CONTROLLER*********************/
Delta_Theta_Out = (TWOPI*Freq_out)/(FSW);
Theta_Out+=Delta_Theta_Out;
Theta_Out=((Theta_Out>=TWOPI)?(Theta_Out-TWOPI):Theta_Out);
cos_Theta_Out=cossp(Theta_Out); sin_Theta_Out=sinsp(Theta_Out);
//Conversion of references from d-q to alpha-beta
Volt_alpha_ref=Volt_d_ref*cos_Theta_Out-Volt_q_ref*sin_Theta_Out;
Volt_beta_ref= Volt_d_ref*sin_Theta_Out+Volt_q_ref*cos_Theta_Out;
//Conversion of references from alpha-beta to ABC
Volt_phase_a_ref=Volt_alpha_ref;
Volt_phase_b_ref=1.5*(-ONE_3*Volt_alpha_ref+I_SQRT3*Volt_beta_ref);
Volt_phase_c_ref=1.5*(-ONE_3*Volt_alpha_ref-I_SQRT3*Volt_beta_ref);
//Scale phase output voltage (feedback signals) adc results
Volt_FB_a=(float)((adc9-offset9)*Vgaina);
Volt_FB_b=(float)((adc8-offset8)*Vgainb-0.175);
Volt_FB_c=(float)((adc7-offset7)*Vgainc); /***************Tracking
Controller for phase a******************/
Volt_phase_a_error_last2=Volt_phase_a_error_last1;
Volt_phase_a_error_last1=Volt_phase_a_error;
Volt_phase_a_error=6*Volt_phase_a_ref-Volt_FB_a;
Volt_phase_a_ctrl_last2=Volt_phase_a_ctrl_last1;
Volt_phase_a_ctrl_last1=Volt_phase_a_ctrl;
Volt_phase_a_ctrl=-0.4999*Volt_phase_a_ctrl_last2-
0.5001*Volt_phase_a_ctrl_last1+0.6*(0.9699*Volt_phase_a_error_last2-
1.319*Volt_phase_a_error_last1+Volt_phase_a_error);
if(-168<Volt_phase_a_ctrl && Volt_phase_a_ctrl<168)
    Volt_phase_a_ctrl=Volt_phase_a_ctrl;
else
    Volt_phase_a_ctrl=166;
/**********Tracking Controller for phase b*********************/
Volt_phase_b_error_last2=Volt_phase_b_error_last1;
Volt_phase_b_error_last1=Volt_phase_b_error;
Volt_phase_b_error=6*Volt_phase_b_ref-Volt_FB_b;
Volt_phase_b_ctrl_last2=Volt_phase_b_ctrl_last1;
```

```
Volt_phase_b_ctrl_last1=Volt_phase_b_ctrl;
Volt_phase_b_ctrl=-0.4999*Volt_phase_b_ctrl_last2-
0.5001*Volt_phase_b_ctrl_last1+0.6*(0.9699*Volt_phase_b_error_last2-
1.319*Volt_phase_b_error_last1+Volt_phase_b_error);
if(-168<Volt_phase_b_ctrl && Volt_phase_b_ctrl<168)
    Volt_phase_b_ctrl=Volt_phase_b_ctrl;
else
    Volt_phase_b_ctrl=166;
/*************Tracking Controller for phase c******************/
Volt_phase_c_error_last2=Volt_phase_c_error_last1;
Volt_phase_c_error_last1=Volt_phase_c_error;
Volt_phase_c_error=6*Volt_phase_c_ref-Volt_FB_c;
Volt_phase_c_ctrl_last2=Volt_phase_c_ctrl_last1;
Volt_phase_c_ctrl_last1=Volt_phase_c_ctrl;
Volt_phase_c_ctrl=-0.4999*Volt_phase_c_ctrl_last2-
0.5001*Volt_phase_c_ctrl_last1+0.6*(0.9699*Volt_phase_c_error_last2-
1.319*Volt_phase_c_error_last1+Volt_phase_c_error);
if(-168<Volt_phase_c_ctrl && Volt_phase_c_ctrl<168)
    Volt_phase_c_ctrl=Volt_phase_c_ctrl;
else
    Volt_phase_c_ctrl=166;
/*********************END OF CONTROLLER***********************/
```

D.3 Code of the Repetitive Controller Implementation

```
void RC_phase_a(void)
{
pre_delay_a=Volt_phase_a_ref;
RC_a_1_02=RC_a_1_01; RC_a_1_01=RC_a_1; RC_a_1=pre_delay_a-Volt_FB_a;
RC_a_2_02=RC_a_2_01; RC_a_2_01=RC_a_2;
RC_a_2=-0.3185*RC_a_2_02+0.8845*RC_a_2_01+0.1072*RC_a_1_02+
0.2145*RC_a_1_01+0.1072*RC_a_1; //Compensator
RC_a_3_32=RC_a_3_31; RC_a_3_31=RC_a_3_30; RC_a_3_30=RC_a_3_29;
RC_a_3_29=RC_a_3_28; RC_a_3_28=RC_a_3_27; RC_a_3_27=RC_a_3_26;
RC_a_3_26=RC_a_3_25; RC_a_3_25=RC_a_3_24; RC_a_3_24=RC_a_3_23;
```

```
RC_a_3_23=RC_a_3_22; RC_a_3_22=RC_a_3_21; RC_a_3_21=RC_a_3_20;
RC_a_3_20=RC_a_3_19; RC_a_3_19=RC_a_3_18; RC_a_3_18=RC_a_3_17;
RC_a_3_17=RC_a_3_16; RC_a_3_16=RC_a_3_15; RC_a_3_15=RC_a_3_14;
RC_a_3_14=RC_a_3_13; RC_a_3_13=RC_a_3_12; RC_a_3_12=RC_a_3_11;
RC_a_3_11=RC_a_3_10; RC_a_3_10=RC_a_3_09; RC_a_3_09=RC_a_3_08;
RC_a_3_08=RC_a_3_07; RC_a_3_07=RC_a_3_06; RC_a_3_06=RC_a_3_05;
RC_a_3_05=RC_a_3_04; RC_a_3_04=RC_a_3_03; RC_a_3_03=RC_a_3_02;
RC_a_3_02=RC_a_3_01; RC_a_3_01=RC_a_3;
RC_a_4=0.95*RC_a_3_32; RC_a_3=RC_a_2+RC_a_4;
RC_a_4_06=RC_a_4_05; RC_a_4_05=RC_a_4_04; RC_a_4_04=RC_a_4_03;
RC_a_4_03=RC_a_4_02; RC_a_4_02=RC_a_4_01; RC_a_4_01=RC_a_4;
post_delay_a=0.055*RC_a_4_05;
Volt_phase_a_ref_mod=0.525*(Volt_phase_a_ref+post_delay_a);
}
void RC_phase_b(void)
{
pre_delay_b=Volt_phase_b_ref;
RC_b_1_02=RC_b_1_01; RC_b_1_01=RC_b_1; RC_b_1=pre_delay_b-Volt_FB_b;
RC_b_2_02=RC_b_2_01; RC_b_2_01=RC_b_2;
RC_b_2=-0.3185*RC_b_2_02+0.8845*RC_b_2_01+0.1072*RC_b_1_02+
0.2145*RC_b_1_01+0.1072*RC_b_1; //Compensator
RC_b_3_32=RC_b_3_31; RC_b_3_31=RC_b_3_30; RC_b_3_30=RC_b_3_29;
RC_b_3_29=RC_b_3_28; RC_b_3_28=RC_b_3_27; RC_b_3_27=RC_b_3_26;
RC_b_3_26=RC_b_3_25; RC_b_3_25=RC_b_3_24; RC_b_3_24=RC_b_3_23;
RC_b_3_23=RC_b_3_22; RC_b_3_22=RC_b_3_21; RC_b_3_21=RC_b_3_20;
RC_b_3_20=RC_b_3_19; RC_b_3_19=RC_b_3_18; RC_b_3_18=RC_b_3_17;
RC_b_3_17=RC_b_3_16; RC_b_3_16=RC_b_3_15; RC_b_3_15=RC_b_3_14;
RC_b_3_14=RC_b_3_13; RC_b_3_13=RC_b_3_12; RC_b_3_12=RC_b_3_11;
RC_b_3_11=RC_b_3_10; RC_b_3_10=RC_b_3_09; RC_b_3_09=RC_b_3_08;
RC_b_3_08=RC_b_3_07; RC_b_3_07=RC_b_3_06; RC_b_3_06=RC_b_3_05;
RC_b_3_05=RC_b_3_04; RC_b_3_04=RC_b_3_03; RC_b_3_03=RC_b_3_02;
RC_b_3_02=RC_b_3_01; RC_b_3_01=RC_b_3;
RC_b_4=0.95*RC_b_3_32; RC_b_3=RC_b_2+RC_b_4;
RC_b_4_06=RC_b_4_05; RC_b_4_05=RC_b_4_04; RC_b_4_04=RC_b_4_03;
RC_b_4_03=RC_b_4_02; RC_b_4_02=RC_b_4_01; RC_b_4_01=RC_b_4;
post_delay_b=0.055*RC_b_4_05;
Volt_phase_b_ref_mod=0.525*(Volt_phase_b_ref+post_delay_b);
}
```

```
void RC_phase_c(void)
{
pre_delay_c=Volt_phase_c_ref;
RC_c_1_02=RC_c_1_01; RC_c_1_01=RC_c_1; RC_c_1=pre_delay_c-Volt_FB_c;
RC_c_2_02=RC_c_2_01; RC_c_2_01=RC_c_2;
RC_c_2=-0.3185*RC_c_2_02+0.8845*RC_c_2_01+0.1072*RC_c_1_02+
0.2145*RC_c_1_01+0.1072*RC_c_1; //Compensator
RC_c_3_32=RC_c_3_31; RC_c_3_31=RC_c_3_30; RC_c_3_30=RC_c_3_29;
RC_c_3_29=RC_c_3_28; RC_c_3_28=RC_c_3_27; RC_c_3_27=RC_c_3_26;
RC_c_3_26=RC_c_3_25; RC_c_3_25=RC_c_3_24; RC_c_3_24=RC_c_3_23;
RC_c_3_23=RC_c_3_22; RC_c_3_22=RC_c_3_21; RC_c_3_21=RC_c_3_20;
RC_c_3_20=RC_c_3_19; RC_c_3_19=RC_c_3_18; RC_c_3_18=RC_c_3_17;
RC_c_3_17=RC_c_3_16; RC_c_3_16=RC_c_3_15; RC_c_3_15=RC_c_3_14;
RC_c_3_14=RC_c_3_13; RC_c_3_13=RC_c_3_12; RC_c_3_12=RC_c_3_11;
RC_c_3_11=RC_c_3_10; RC_c_3_10=RC_c_3_09; RC_c_3_09=RC_c_3_08;
RC_c_3_08=RC_c_3_07; RC_c_3_07=RC_c_3_06; RC_c_3_06=RC_c_3_05;
RC_c_3_05=RC_c_3_04; RC_c_3_04=RC_c_3_03; RC_c_3_03=RC_c_3_02;
RC_c_3_02=RC_c_3_01; RC_c_3_01=RC_c_3;
RC_c_4=0.95*RC_c_3_32; RC_c_3=RC_c_2+RC_c_4;
RC_c_4_06=RC_c_4_05; RC_c_4_05=RC_c_4_04; RC_c_4_04=RC_c_4_03;
RC_c_4_03=RC_c_4_02; RC_c_4_02=RC_c_4_01; RC_c_4_01=RC_c_4;
post_delay_c=0.055*RC_c_4_05;
Volt_phase_c_ref_mod=0.525*(Volt_phase_c_ref+post_delay_c);
}
```