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Experimental verification of trinary DC source cascaded H-bridge multilevel inverter using unipolar pulse width modulation

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ABSTRACT

Multilevel inverters (MLIs) are an imperative solution for high power and high voltage applications. The MLIs can be classified into two categories such as symmetric and asymmetric. The asymmetric type MLIs has large number of output voltage steps with less number of input DC voltage sources and switching devices. In this paper, a single phase asymmetric (trinary sequence DC source) Cascaded H-Bridge MLI has been developed using unipolar PWM control schemes. The topology can produce 27-level output voltage with the help of 12 switches and 3 DC sources. It has been examined with a diverse combination of multicarrier unipolar PWM control. The PWM control includes Phase Disposition (PDPWM), Alternative Opposition Disposition (APODPWM), Carrier overlapping (COPWM), and Variable Frequency (VFPWM). The harmonic content of output voltage for each technique has been observed with different modulation indices. The demonstration of proposed topology for generating 27-level output voltage has been tested through simulation in MATLAB-SIMULINK and verified with laboratory-based experimental setup. From the results, it is evident that the APODPWM offers quality output voltage with relatively low harmonic distortion. Also, it has been observed that COPWM performance is superior since it delivers relatively higher fundamental RMS output voltage.

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KEYWORDS
Asymmetric multilevel inverter; single phase trinary DC source; unipolar PWM; cascaded multilevel inverter

1. Introduction

Multilevel inverters (MLI) are utilized for creating a near sinusoidal output voltage waveform from different levels of input DC source voltage. The Diode Clamped MLI (DCMLI), Flying Capacitor MLI (FCMLI) and Cascaded H-Bridge MLI (CHBMLI) are the most commonly used MLI topologies. The topologies mostly standardize the staircase output voltage waveform which has reduced the total harmonic distortion (THD). But, the component count is the major concern. Therefore, the new topologies are preferred with lesser power semiconductor switching devices as compared to the conventional MLI topologies. A complete survey of the reduced switch MLI topologies with different categories are as described in [1]. The half bridge MLI in both symmetric and asymmetric condition is discussed in [2]. It requires bidirectional switches to generate the required output voltage level. Field Programming Gate Array (FPGA) based single phase CHBMLI for adjustable speed drive applications is discussed in [3]. Increased number of power semiconductor switches is required to create an output voltage with stable number of steps. In [4–6], the topology is developed based on reduction of power semiconductor switches to achieve quality output voltage with low %THD. An 11 level flying capacitor MLI switching pattern has been explained for induction motor drive application in [7]. Commercial two-level inverter requires large passive filters to reduce the harmonic content in high power voltage applications [8–11]. A 9 level grid connected inverter topology photovoltaic structure operated without including single phase transformer is discussed in [12–14]. CHBMLI using single phase non regenerative power units has been implemented to improve the quality of output voltage/power in [15]. The large frequency-link cascaded multilevel inverter is operated with the average voltage for direct grid integration of RES (Renewable Energy Sources) in [16]. The new topology of MLI with self-balancing concept has been discussed in [17]. Single DC source with floating MLI or FCMLI is developed [18–21] for reducing the DC source count. The developed configuration utilizes bidirectional switches and floating capacitors which makes the circuit complex and increases the switch count [20]. Extra control circuits are needed for balancing the capacitor voltage [21]. On the other hand, a single-phase transformer/three-phase transformer based CHBMLI is developed in [22]. In this case, primary of each transformer is connected to cascaded H-bridge (CHB) output side and secondary is connected in series to achieve the desired voltage level [22]. The disadvantage of this configuration is while

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deciding the turns ratio of the transformer, its size increases due to rise in output voltage level. Hybrid topologies are also recently developed for improving the quality of output voltage waveform in [23–25], which require higher number of different voltage magnitude DC sources. In literature, many reduced switch topologies have been introduced for various advantages. Among those MLI topologies, CHBMLI has the benefit of modularity and flexibility to create any number of output voltage levels.

This article deals with the trinary DC source CHBMLI to decrease the number of power semiconductor switches. The ratio of DC sources is 1:3:9. So, the sequence is called trinary sequence. The trinary sequence CHBMLI can produce all additive and subtractive combination of input DC levels in the output voltage waveform. The proposed topology generates 27-level output voltage with the help of three DC sources and 12-switches. Also, the paper mainly focuses on the testing of unipolar pulse width modulation (UPWM) control with four different carrier arrangements such as Phase Disposition (PD), Alternative Phase Opposition and Disposition (APOD), Carrier Overlapping and Variable Frequency. The main advantage of unipolar PWM requires only half carrier count as compared with conventional PWM carrier count. The proposed topology is tested with these four types of carrier arrangement in MATLAB-SIMULINK. Also, the simulation result of PDPWM is verified with laboratory-based experimental setup.

2. Proposed trinary DC source inverter topology

The proposed topology is a series connection of H-bridge inverter. Each H-bridge has a set of DC sources with dissimilar values. It utilizes three DC sources for generating 27-level output voltage with the help of only 12-switches and eliminates the requirement of large number of transformers for grid integration. The output voltage level of the proposed topology has appropriate steps equal to the sinusoidal voltage waveform. Figure 1(a) demonstrates proposed asymmetrical CHBMLI with trinary sequence input DC source. The three different DC sources like V_{DC}, $3V_{DC}$ and $9V_{DC}$ produces 27-level output voltage. The output voltage levels of the proposed topology in the range of $-13V_{DC}$ to $13V_{DC}$ with a step of $V_{DC.}$ For utilization of two DC sources 9-level output voltage is generated whereas three level output voltage is generated with the help of one DC source. Here, the final output voltage level becomes the algebraic sum of each terminal output voltage of H-Bridge inverter and it is shown in the following equation.

$$V_{out} = V_{Dc} + 3V_{DC} + 9V_{DC} \quad (1)$$

Here, V_{DC}, $3V_{DC}$, $9V_{DC}$ are the DC source value of three H-Bridge unit. Figure 1(b) represents few modes of operation of the positive polarity output voltage level generation. In the proposed MLI topology, if m number of H-bridge unit has dissimilar input DC source with geometric progression of 3, the expected output voltage levels are given below in the generalized expression

$$V_m = 3^m, m = 1, 2, 3 \ldots \quad (2)$$

In trinary sequence, the amplitude of input DC sources are in the ratio of 1:3:9:27 . . . :3m and the maximum output AC voltage reaches to $((3^m - 1)/2)$ V_{DC} and the output voltage levels will be (3^m). Table 1 represents the generation of output voltage level with appropriate DC source. From the table, it is clearly understood that the polarity of DC sources of each H-bridge in the appropriate voltage level. Here, 1 represents the "On state" of the DC source in the H-bridge and 0 represents the "off state" and −1 represents "on state with reverse polarity". For example, generating the maximum voltage level by adding all DC sources is cascaded with positive polarity.

3. Multicarrier pulse width modulation schemes

Different types of pulse width modulation (PWM) controls have been discussed in the literature in [1]. Carrier Based Pulse Width Modulation (CBPWM) and Space Vector based Pulse Width Modulation (SVPWM) are the most popular schemes. But, CBPWM is often used for higher voltage levels. Whereas the SVPWM is difficult for generating pulses for more than five levels due to the redundancy of switching states [26–29]. Therefore, CBPWM control is chosen as the control technique for the proposed topology in this article. Different types of CBPWM are used to generate switching pulses in the proposed topology. In CBPWM method, multiple carriers ("m" level inverter output require "(m–1)/2" carriers) are formed together which are continuously compared with sinusoidal reference and creates the PWM signals [30]. The multiple carriers can be arranged in many ways based on control freedom technique [30]. This paper focuses on four different carriers by using unipolar reference with multiple carriers. The unipolar scheme requires half of the carriers as compared to conventional (bipolar) PWM scheme which is the major advantage. The four different types of carrier arrangements are examined in this work such as PDPWM, APODPWM, COPWM and VFPWM. The reference waveform is considered as unipolar sinusoidal signal and 13 carrier waveforms considered as triangular signal. The reference unipolar sinusoidal waveform is continuously compared with each triangular carrier signals. If the reference sinusoidal wave is more than a triangular carrier signal, then the active switching devices equivalent to the triangular

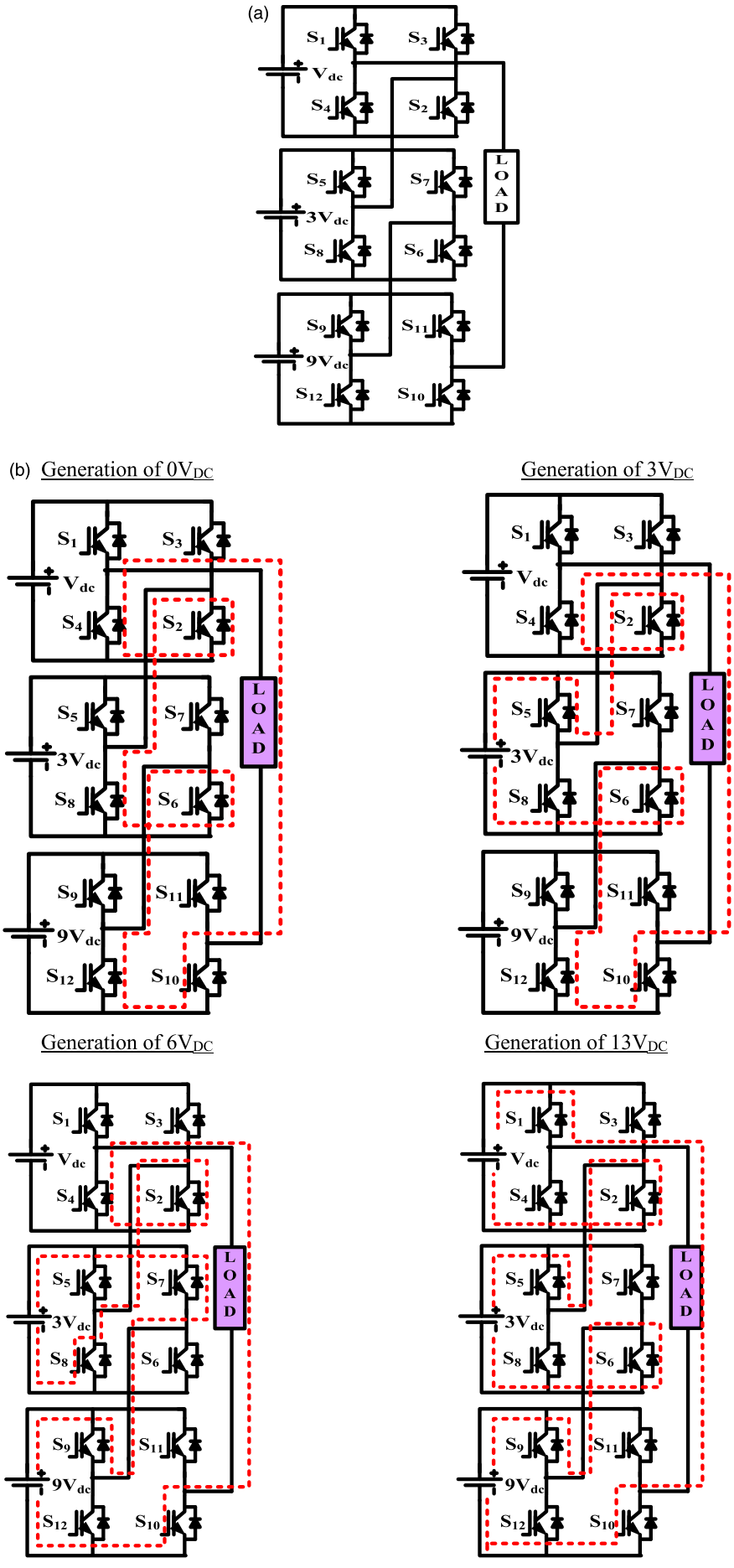


Figure 1. (a) Proposed trinary DC source multilevel inverter. (b) Sample modes of operation of proposed trinary MLI for positive polarity generation.

Table 1. Switching sequence of trinary MLI.

First full bridge (HB1)	Second full bridge (HB2)	Third full bridge (HB3)	Output voltages (V_{out})
1	1	1	$+13\,V_{DC}$
0	1	1	$+12\,V_{DC}$
−1	1	1	$+11\,V_{DC}$
1	0	1	$+10\,V_{DC}$
0	0	1	$+9\,V_{DC}$
−1	0	1	$+8\,V_{DC}$
1	−1	1	$+7\,V_{DC}$
0	−1	1	$+6\,V_{DC}$
−1	−1	1	$+5\,V_{DC}$
1	1	0	$+4\,V_{DC}$
0	1	0	$+3\,V_{DC}$
−1	1	0	$+2\,V_{DC}$
1	0	0	$+1\,V_{DC}$
0	0	0	$0\,V_{DC}$
−1	0	0	$-1\,V_{DC}$
1	−1	0	$-2\,V_{DC}$
0	−1	0	$-3\,V_{DC}$
−1	−1	0	$-4\,V_{DC}$
1	1	−1	$-5\,V_{DC}$
0	1	−1	$-6\,V_{DC}$
−1	1	−1	$-7\,V_{DC}$
1	0	−1	$-8\,V_{DC}$
0	0	−1	$-9\,V_{DC}$
−1	0	−1	$-10\,V_{DC}$
1	−1	−1	$-11\,V_{DC}$
0	−1	−1	$-12\,V_{DC}$
−1	−1	−1	$-13\,V_{DC}$

carriers are turned ON. Otherwise, the switching device is turned OFF. In this paper, the carrier frequency ratio is considered as 60 and a modulation index varies from 0.9 to 1.

3.1. Phase disposition PWM (PDPWM)

The phase disposition PWM type utilizes 13-carrier signals with sinusoidal reference waveform for generating 27-level output voltage. In PDPWM, all 13 carriers are in phase with same amplitude and same switching frequency. Figure 2(a) shows the multicarrier arrangement of PDPWM type with the amplitude modulation index ($m_a = 1$) and modulation frequency ($m_f = 60$).

3.2. Alternative phase opposition disposition PWM (APODPWM)

In Alternative Phase Opposition Disposition (APOD) type, 13-carrier signals are utilized for generating 27-level output voltage. The adjacent carriers are displaced from the neighbouring carrier by 180° alternately phase shifted. Figure 2(b) shows the multicarrier arrangement of APODPWM type with the amplitude modulation index ($m_a = 1$) and modulation frequency ($m_f = 60$).

3.3. Carrier overlapping PWM (COPWM)

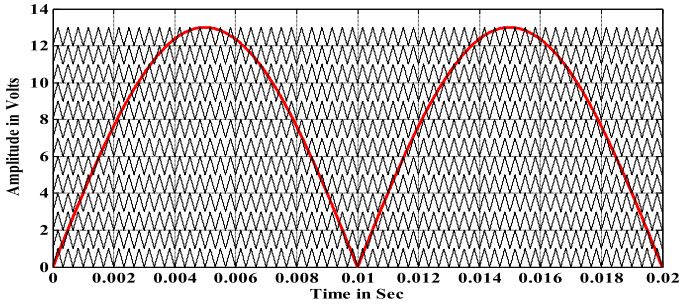
The Carrier Overlapping (CO) PWM type, "((m–1)/2)" carrier waves are disposed such that the carrier wave bands they occupy overlap with another carrier wave. The overlapping is compensated vertically on the amplitude of next carrier wave signal. Figure 2(c) shows the multicarrier arrangement of COPWM type with the amplitude modulation index ($m_a = 1$) and modulation frequency ($m_f = 60$).

3.4. Variable frequency PWM (VFPWM)

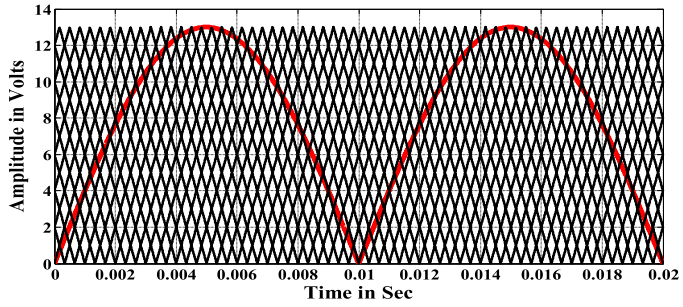
This type of PWM strategy provides odd number of carrier wave having one set of frequency (3000 Hz) and even number of carrier wave having another set of frequency (6000 Hz). But the amplitude of all carriers should be same and the each carrier is in phase only. Figure 2(d) shows the multicarrier arrangement of VF PWM type with the amplitude modulation index ($m_a = 1$) and modulation frequencies ($m_f = 60$ and 120).

4. Simulation results

The 27-level single phase trinary sequence DC source CHBMLI is demonstrated in MATLAB/SIMULINK which is shown in Figure 2(e). The switching signals for proposed CHBMLI are generated using multicarrier sinusoidal unipolar PWM methods. Figures 3–6 shows the output voltage and current waveform for different types of carrier arrangement along with its voltage FFT plot at the modulation index of 1. The %THD depends on the range of switching frequencies. The frequency modulation index m_f is defined as the ratio between the frequencies of the carrier f_{cr} and modulating wave f_m. When m_f is a small number (i.e. less than 21), it's output spectrum contains low-frequency harmonics (sub-harmonics) causing high currents in transformers and inductors. Note that in the case of m_f being a



(a)



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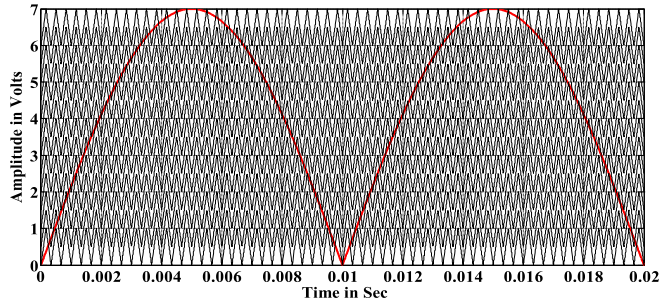
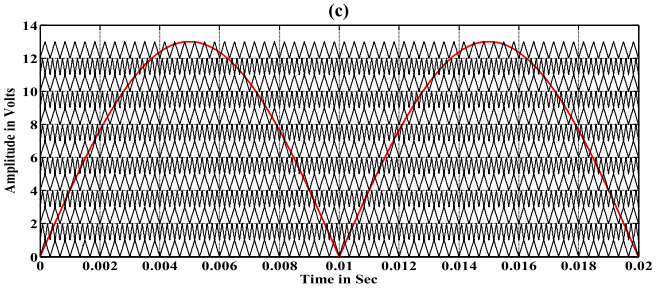
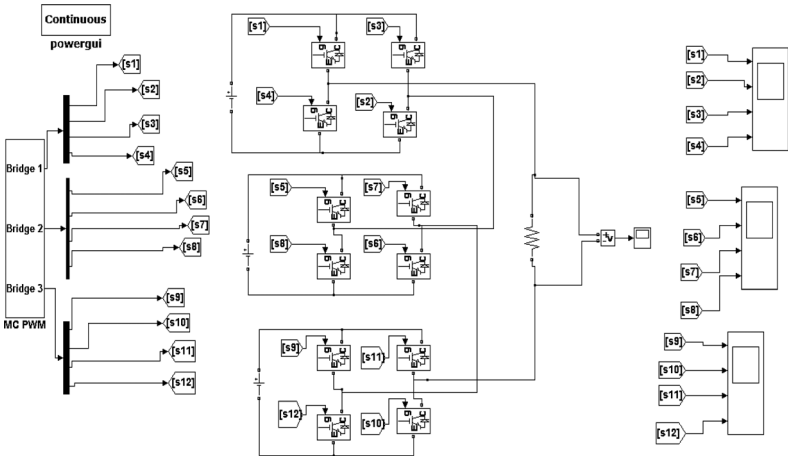


(c)



(d)



(e)

Figure 2. Carrier arrangement: (a) PD PWM type; (b) APOD PWM type; (c) COP PWM type; (d) Carrier arrangement of VF PWM type (e) simulation circuit.

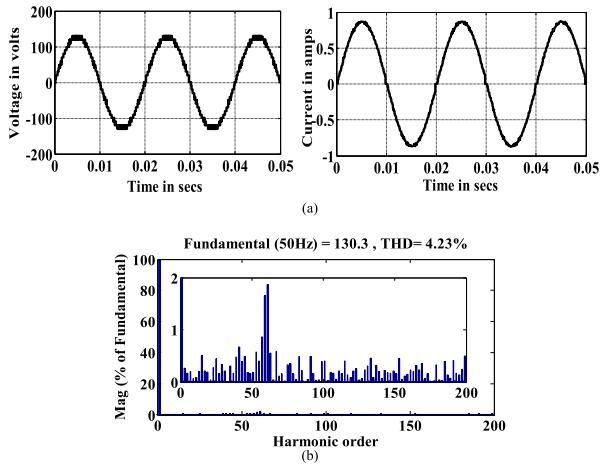


Figure 3. Output voltage and current with FFT Plot for PDPWM scheme.

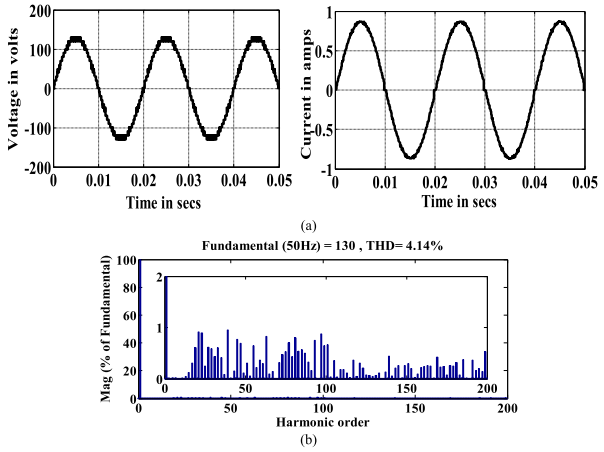


Figure 4. Output voltage and current with FFT plot for APOD-PWM Scheme.

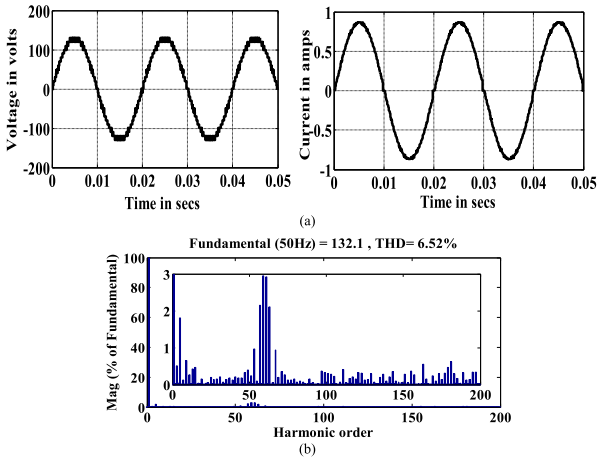


Figure 5. Output voltage and current with FFT plot for CO PWM Scheme.

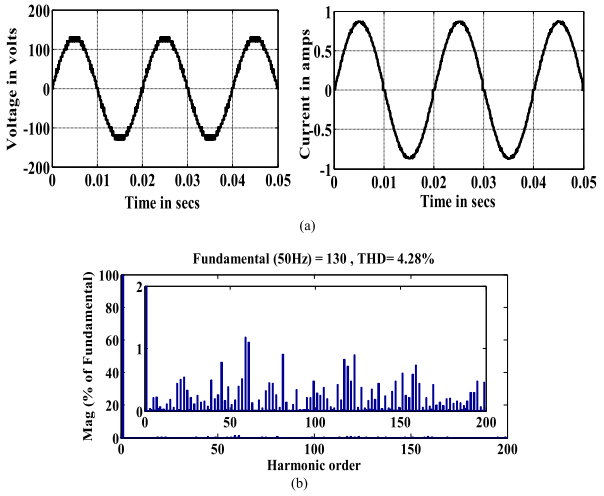


Figure 6. Output voltage and current with FFT Plot for VF PWM scheme.

large number, the amplitudes of the sub-harmonics are highly reduced and do not pose critical problems with the currents by inductors and transformers. Therefore, the selected topology generates low order harmonics with the obtained high frequency, but the order harmonic values have considerable limits, i.e. within the IEEE 519 standard. Hence, low order harmonics do not affect the system. The FFT subplots are with low individual harmonic order and thus do not affect the system performance [31,32]. The simulation results are examined for different range of modulation index values of 0.85–1 and the values are tabulated. Table 2 shows the values of simulation parameters. The %THD (a quantity of similarity in shape concerning a waveform and its essential component) is evaluated for different types of carrier arrangement using the FFT block and their values are tabulated in Table 3. APODPWM provides lesser %THD as compared with other type of carrier arrangement. Table 4 shows the fundamental V_{RMS} value of output voltage for different types of carrier arrangement. COPWM method provides better V_{RMS} as compared to other methods. Table 5 presents the Crest Factor (CF) value which is used to identify peak

Table 2. Simulation parameters.

Parameter	Value
First full bridge (HB_1) DC source: (V_{DC})	10 V
Second full bridge (HB_2) DC source: ($3V_{DC}$)	30 V
Third full bridge (HB_3) DC source: ($9V_{DC}$)	90 V
Load resistance (RL)	150 ohms & 25 mH
Carrier frequency (fc)	3000 Hz & 6000 Hz
Modulation frequency m_{f1}	60
Modulation frequency m_{f2}	120
MATLAB-SIMULINK	2009b, Power system block set, continuous powergui
Switch	IGBT with Diode

current evaluation of the semiconductor device. The value of CF is almost same for all PWM methods at different modulation indices. Table 6 shows the Distortion Factor (DF) of the output voltage. PDPWM method provides lesser distortion factor as compared with other PWM methods. Table 7 shows the Form Factor (FF) associated with power quality problem. The formulas

Table 3. %Total harmonics distortion for various modulation indexes.

Ma	PD	APOD	COP	VF
1	4.23	4.14	6.52	4.28
0.95	5.00	4.57	7.13	4.74
0.9	4.99	4.23	7.92	4.92
0.85	5.32	4.93	8.20	5.12

Table 4. Fundamental V_{RMS} output voltage for various modulation indexes.

Ma	PD	APOD	COP	VF
1	92.15	91.93	93.38	92
0.95	87.2	87.34	89.32	87.24
0.9	82.73	82.7	84.61	82.76
0.85	78.35	78.14	79.59	78.22

Table 5. Crest factor for various modulation indexes.

Ma	PD	APOD	COP	VF
1	1.41486	1.41472	1.41411	1.41413
0.95	1.41499	1.41438	1.41255	1.41401
0.9	1.41423	1.41424	1.41475	1.41437
0.85	1.41416	1.41412	1.41475	1.41461

Table 6. %Distortion factor for various modulation indexes.

Ma	PD	APOD	COP	VF
1	1.05	2.07	3.05	1.08
0.95	1.04	2.05	3.05	1.08
0.9	1.05	2.09	3.09	1.09
0.85	1.02	2.06	3.10	1.20

Table 7. Form factor for various modulation indexes.

Ma	PD	APOD	COP	VF
1	39631.53	1.7710	1.46E+09	2.22E+09
0.95	1.95E+06	3.7710	5266.08	40125.78
0.9	35339.6	680.077	17266.08	19051.57
0.85	33903.07	1.83E+09	11963.02	11757.1

for calculating the CF, FF and DF are follows

$$\mathrm{CF} = \frac{V_{\mathrm{peak}}}{V_{\mathrm{rms}}} \tag{3}$$

$$\mathrm{FF} = \frac{V_{\mathrm{rms}}}{V_{\mathrm{dc}}} \tag{4}$$

$$\mathrm{DF} = \frac{1}{V_{01}}\left(\sum_{n=2,3..}^{\infty}\left(\frac{V_{\mathrm{on}}}{n^2}\right)^2\right)^{1/2} \tag{5}$$

5. Experimental setup and results

The laboratory-based experimental testing of the 27 level single phase trinary sequence DC source CHBMLI is shown in Figure 7. The Experimental setup contains proposed inverter, Personal Computer, FPGA controller and Driver circuit (TLP250). The proposed topology contains 3-full bridge inverters connected in a cascaded manner. Every full bridge inverter requires one input DC source. The input DC voltage may be

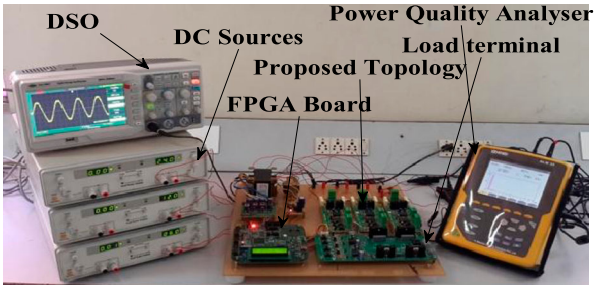


Figure 7. Prototype model of proposed 27 level single phase trinary DC source CMLI.

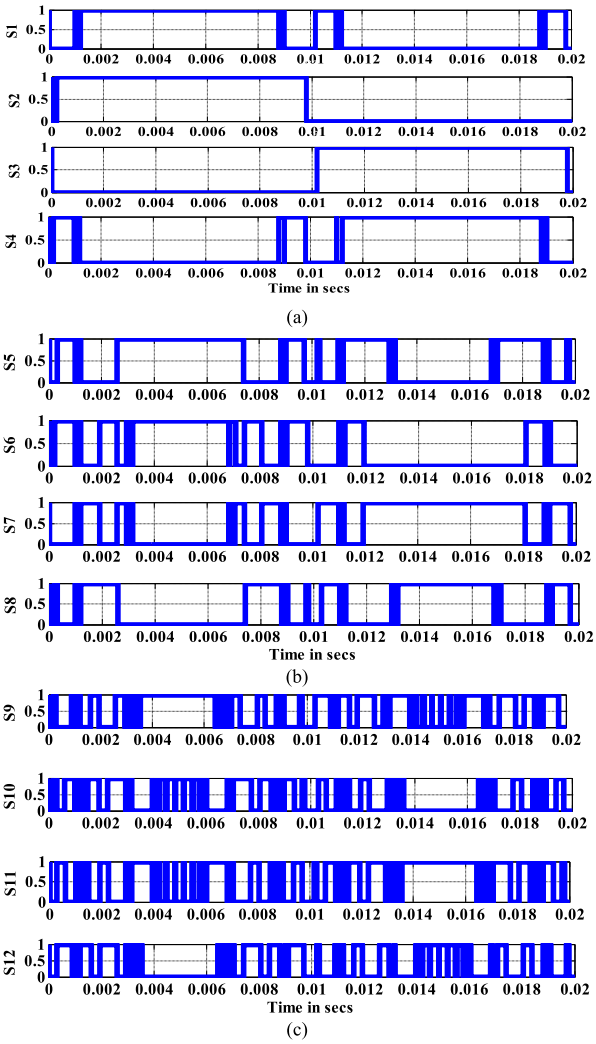


Figure 8. Switching signals for the proposed topology. (a) Switching signal for first bridge, (b) switching signal for second bridge, and (c) switching signal for third bridge.

attained from the full bridge rectifier linked to the AC supply. Each semiconductor switch accompanies a snubber circuit to offer over voltage and over current protection. The output voltage of the full bridge inverter is used to feed the RL load. The essential PWM pulses for triggering the semiconductor switches are generated from the Field Programming Gate Array (FPGA) controller. The generated PWM pulses are applied to the gate terminal of the IGBT (FGA25N120). The FPGA

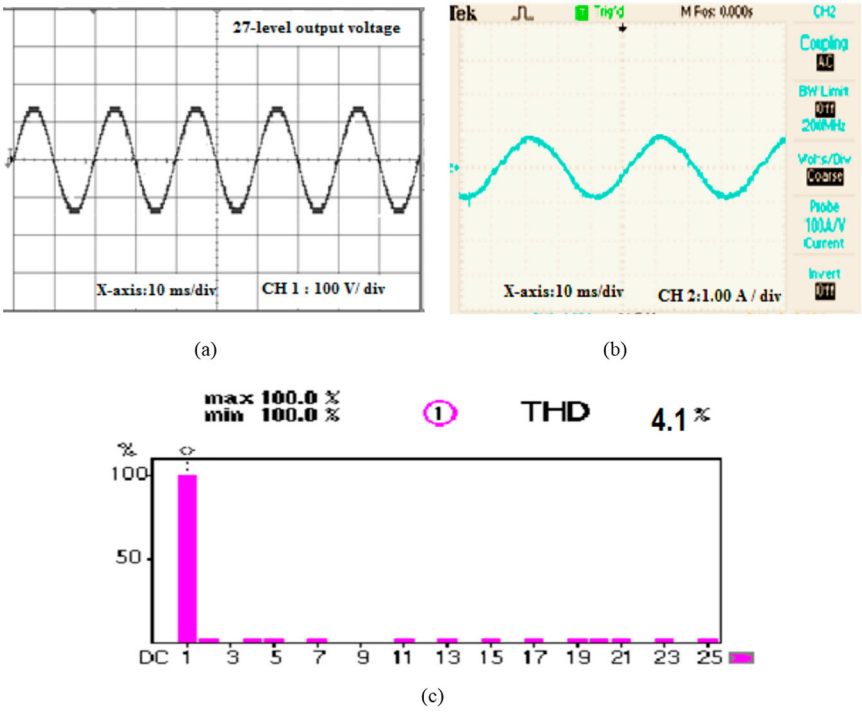


Figure 9. Experimental results: (a) output voltage, (b) output current, and (c) voltage FFT Plot for PD PWM type.

controller arrangement using a HDL contains a phase locked Loop (PLL), DAC, ADC and serial input/output port etc. Personal computer (PC) is used to develop programmes for the Field Programming Gate Array (FPGA) in XILLINX software package. JTAG is an important IEEE standard great speed protocol which is used to provide interfaces to the FPGA processor and the PC (Personal computer). The written programme coding is fed to the FPGA processor through JTAG Protocol (emulator). Frequency (f) & M_a (Modulation index) keys are used to provide input to the Field Programming Gate Array (FPGA) processor. Frequency key is used to change the inverter output frequency. M_a (Modulation index) key is used to change the modulation indices. The switching signals are produced using FPGA, passes through the OPTO isolator which provides isolation to the switching signals from higher voltage segment. These switching signals are connected to driver circuit. The driver circuit offers the essential voltage to be applied in between gate to source terminal of the IGBTs. The power semiconductor switches are fired using the driver circuit. Figure 8 provides the PDPWM switching pulses of the proposed inverter switches for generating the 27-level output voltage. The experimental results are carried out for the modulation index of one. Figure 9 shows the experimental output voltages and current with its voltage and the corresponding harmonic spectrum plot for PD type carrier arrangement. The maximum output voltage and output current of the proposed topology are 130 V and 0.87 A, respectively.

6. Conclusion

This paper deals with a single phase trinary sequence DC source CHBMLI for generating 27-level output voltage level. The ratio of DC sources in trinary sequence is 1:3:9. The unipolar PWM with different carrier arrangement has been implemented with the trinary sequence DC source multilevel inverter. The different performance parameters such as THD, Fundamental V_{RMS} voltage, Crest Factor, Form Factor and Distortion Factor are calculated and compared with different carrier arrangement for different modulation indices. The 27-level output voltage ensures to meet the fundamental AC output voltage waveform so that it produces the lowest %THD. The operating principle of the proposed MLI for generating 27-level output voltage has been verified by simulation and also in the laboratory-based experimental test setup using FPGA. From the results, it is concluded that the APOD carrier arrangement generates less %THD as compared to other carrier arrangements. Also, it is evident that the CO carrier arrangement provides higher fundamental RMS voltage and the PD carrier arrangement provides less %DF. Crest Factor should be same for all carrier arrangements. This proposed topology could be useful for effective speed control operation in AC motor drives and also in photovoltaic applications.

Disclosure statement

No potential conflict of interest was reported by the authors.

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