DESIGN AND TESTING OF HIGH FREQUENCY CONVERTERS FOR PHOTOVOLTAIC SYSTEM INTEGRATION

by

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Bachelor of Science, University of Pittsburgh, 2012

Submitted to the Graduate Faculty of

The Swanson School of Engineering in partial fulfillment

of the requirements for the degree of

Master of Science

University of Pittsburgh

2014

UNIVERSITY OF PITTSBURGH

SWANSON SCHOOL OF ENGINEERING

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This thesis presents simulation, modelling, and testing for the complete photovoltaic (PV) system, including the PV panels themselves, the converters necessary for grid connection, and the testbed environments required for their testing. Investigating such systems is crucial, as PV systems are becoming increasingly prevalent. Converters are evolving and so too are the semiconductor devices of which they are comprised. Advanced topologies such as the modular multilevel converter (MMC) are allowing for radical changes in converter design and control, raising performance and efficiency ever higher. Buoying that growth is the development of wide bandgap (WBG) semiconductors, which are enabling faster, smaller, and more efficient converters.

In light of these advancements, significant room for modeling and analysis of the various phenomena that occur in PV systems is critical. In order to address this need, this thesis will present analysis, simulation, and testing of a number of key elements within the PV system, such that the whole may be better understood. It will begin with the DC-DC converter itself, modeling transient events in synchronous buck converters, as well as demonstrating the implementation of maximum power point tracking (MPPT) in boost converters. Next, the inverter portion of the system will be examined, focusing on development of a single phase, low voltage version of the MMC topology that has been previously demonstrated in high voltage direct current (HVDC) systems. Finally, a

design for a test bank and workbench will be discussed, shedding light on the laboratory apparatus necessary for proper evaluation and testing of new power electronic devices and systems. In short, the complete PV system is presented, its individual components are modeled and analyzed, and the conditions and materials necessary for testing are established, such that the understanding of PV integration in modern power systems can be better understood.

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AKNOWLEDGEMENTS

There are an enormous number of co-workers, friends, and family without whom this thesis would never have been completed. Their support, input, assistance, and constructive criticism were absolutely essential to this process, helping me to polish this work into the document that appears here.

I would first like to thank my colleagues at the University of Pittsburgh's Electric Power Initiative. These are my co-workers, but more truthfully my friends, who have helped to buoy me throughout this process with both their stimulating intellectual contributions, as well as their friendship and support. In no particular order, these fine engineers are: Patrick Lewis, Alvaro Cardoza, Rusty Scioscia, Hashim Al-Hassan, Dr. Emmanuel Taylor, and Dr. Matthew Korytowski. I also want to particularly thank Dr. Brandon Grainger and Dr. Raghav Khanna, who mentored me throughout this work, and have served as inspirations and guides as to what a graduate student should be. Dr. Khanna worked with me extensively, and his support cannot be understated.

I would also like to thank my committee and advisors, Dr. Gregory Reed, Dr. William Stanchina, and Dr. Zhi-Hong Mao. Their advice, guidance, and technical support has been incredible, and the breadth of the knowledge that they are passing along to the generation of students following in their footsteps is immense. In particular I want to thank my advisor, Dr. Reed for believing in me despite a rather rocky start to my graduate career. I hope I have validated his belief in me.

A special thanks as well is owed to Jim Lyle and Bill Mcgahey, who have provided an incredible amount of technical support to me throughout this process.

Another is owed to Dan Carnovale and Bri Groden, who gave me the absolute best work environment for any budding electrical engineer, and who have been incredibly supportive of this process.

I would also like to thank my parents, Aaron and Aenne Barchowsky, and my brother, Andrew Barchowsky, for being such incredibly positive influences in my life and for helping me to reach towards this goal. Their love and support has been amazing, and I could never have made it here without them.

Finally, I would like to thank my wonderful, beautiful wife Katelyn Barchowsky, for everything that she has done, is continuing to do, and will do for me in the future. She is the love of my life and all of these achievements are equally, if not more so, a reflection of her than me.

1.0 INTRODUCTION

As power systems modernize, photovoltaic systems are becoming essential components in achieving a sustainable energy portfolio nationally and worldwide. They reduce economic dependence on fossil fuels, improve availability of resources, and reduce harmful environmental effects caused by increased carbon emissions. In commercial, residential, and industrial systems, PV panels are seeing increased use and penetration. As the PV systems improve, and new technologies such as concentrated solar, thin film solar, and solar thermal systems are developed, the growth potential for such renewable energy integration only increases. A strong case is being made for increased use of PV generation, in both AC and DC micro and macro grid-integrated systems. As the penetration of PV in the generation mix grows, improved power electronics systems must be developed, in order to integrate the PV resources without detrimental effects to the grid. Advanced power electronics can be used to avoid transient problems, track systems at their maximum power point, and reduce harmonics injected into the grid.

Integrating PV systems into local AC or DC microgrids or the larger electrical grid is not a trivial matter, however. Rather, power electronics converters are required for integration, regulating the power output of the panel and converting the DC power produced by the PV panels to the AC or DC required by the grid. DC-DC converters, as well as inverters, are crucial components of PV system integration, and power electronics themselves are constantly improving.

New system topologies and control architectures are being developed, providing improved capabilities, raising efficiency, and reducing size requirements [1], [2], [3].

One major trend contributing to the rapid improvement of power electronic systems is improvements in the power semiconductors used as the switched transistors to enable power conversion. Specifically, the emergent field of wide bandgap semiconductors is providing power engineers with devices capable of handling higher switching frequencies, creating lower losses, and reducing space requirements for converter systems. Two examples, Silicon Carbide (SiC) and Gallium Nitride (GaN) are showing massive growth, as evidenced in [4] and [5]. These devices are enabling dramatic increases in power density and converter performance, as well as allowing for more rapid controller convergence [6]. Rapid controller convergence allows for the creation of control systems that better track the maximum power point of PV systems in DC-DC and other converters. The rapid development of these technologies, as well as the increasing importance of power electronics in renewable energy integration, suggest that there a number of relevant avenues for research into how best to integrate PV into grid systems.

This thesis will investigate several key issues for PV systems, including transient concerns, maximum power point tracking, modular inverter topologies, and testbed environments for evaluating designed systems. The thesis will be divided into five chapters, all examining individual elements of the complete PV system presented in Figure 1. Each component will be considered, and the specific concerns related to each element will be explored. In doing so, a broad range of topics regarding the PV system as a whole will be addressed. The thesis is organized as follows:

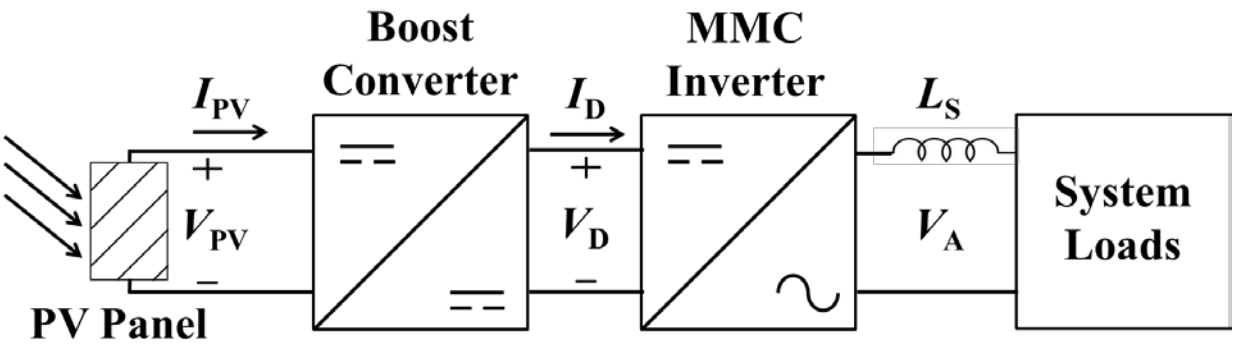


Figure 1. Complete PV system. From left to right: PV panel model, boost converter, MMC inverter, and dynamic system loads

Chapter 2 investigates the occurrence of undesired transients during the turn-on of WBG semiconductors in switched DC-DC converters. Specifically, the synchronous buck converter is analyzed, with a focus on the occurrence of false turn-on. Mathematical models were developed using both frequency domain and state space analysis in order to model the characteristic voltages on both transistors during the turn-on period of the series transistor device. Experimental sensitivity analysis will then be presented, demonstrating the impact of intrinsic capacitances on converter transients.

Chapter 3 presents the use of DC-DC converter for maximum power point tracking (MPPT) for PV panels. A boost converter is examined in order to show its capability for MPPT using a ripple correlation control (RCC) algorithm. A model for the PV panel is implemented in PSCAD providing characteristic I-V curves for a known PV panel based on the manufacturer's datasheet. This model is then used to power a boost converter, running a frequency domain version of the RCC system presented in [7]. This system is shown to accurately track and rapidly converge to the MPP of the system.

Chapter 4 develops an inverter system for PV integration based on the modular multilevel converter (MMC) topology common to modern HVDC systems [8]. The MMC takes advantage

of switching small voltage steps stored on submodule capacitances in order to build an approximately sinusoidal voltage waveform for system integration. In doing so, smaller, more efficient semiconductor devices can be employed and the filtering requirements of the converter system are reduced. This section will first explore the MMC topology. It will then present a PSCAD model of a low voltage, single phase, MMC converter. Analysis will be provided on the process of voltage balancing between submodule capacitances. Finally, system output will be examined and will be shown to be desirable for both grid tied and islanded system integration.

Chapter 5 examines the development of a new laboratory workbench for load simulation in electric power systems labs. The testbed will be shown to be an excellent source of both linear and non-linear loads, and to provide the capability to emulate residential, commercial, and industrial systems. This system allows for testing of the PV integration systems previously described.

Chapter 6 will conclude the thesis, and will examine key points from the presented material. It will also identify future work to be undertaken.

2.0 TRANSIENT BEHAVIOR OF WIDE-BANDGAP SEMICONDUCTORS IN DC-DC CONVERTERS

As power electronics develop, the emphasis on size reduction coupled with improved efficiency cannot be understated. The goals, as expressed in [5], are twofold. First, many applications have space or weight restrictions that benefit from size minimization, such as shipboard or avionic systems or in-home PV converters. Second, many new topologies and implementations can be realized using modern power electronic devices. The rapid development of WBG semiconductors and of higher voltage capabilities in both SiC [4] and GaN [3] have enabled a new generation of DC-DC converters to meet both of the previously stated goals. Both SiC and GaN, the structures of which are shown in Figure 2, have been shown to maintain superior performance in high switching frequency applications, thereby enabling the use of smaller filter components within the converter topology and leading to a reduction in power conversion volume. Additionally, both of these WBG semiconductor types can sustain relatively high operating temperatures, making them particularly attractive for renewable energy applications [9].

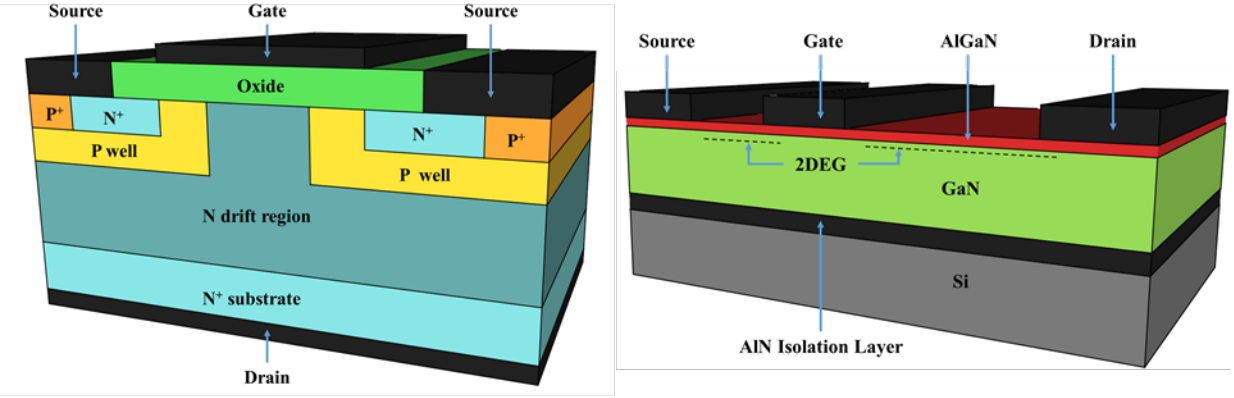


Figure 2. Transistor structures. Left: SiC MOSFET, Right: GaN HEMT

In the case of the PV system shown in Figure 1, the application of WBG semiconductors can drastically reduce the size requirements of the DC-DC converter required for system integration. However, the same characteristics of these devices that allow for faster state transition can result in undesired transients in either the device itself or the converter as a whole. At the device circuits level, the fast switching capability of SiC and GaN have led to detrimental transient behavior such as overshoot, ringing, and false turn-on [10], [11], [12]. In order for WBG semiconductors to deliver their full potential of enhancing DC-DC power electronics devices, the aforementioned unfavorable characteristics of GaN and SiC must be understood, modeled, and mitigated.

This chapter therefore develops analytical modeling techniques for characterizing the circuits-level transient phenomena affecting SiC MOSFETs. First, a high *dv/dt* test circuit is proposed for evaluating the effect of the parasitic devices capacitances on overshoot, ringing, and false turn-on. Initially, the test circuit is analyzed using semiconductor equivalent circuit modelling techniques in the frequency domain. The analytical results are then supplemented with experimental results which validate the model's predictions. Second, the SiC MOSFET is implemented both analytically and experimentally in a synchronous buck converter system. The synchronous buck converter is often used in place of a traditional buck converter in PV systems when losses are a large concern, as it replaces the diode with a second MOSFET, improving the efficiency of the converter [13]. After performing the frequency domain analysis, a state space model was developed, in order to allow for inclusion of the initial conditions of system elements at the time of switching, improving the accuracy of the analytical model.

To derive these models, equivalent circuit models of the high *dv/dt* test circuit and synchronous buck converter were developed. These equivalent circuits were derived to model the dynamic behavior of the device during various sub-stages of the switching period. In [14] and [15],

comprehensive analytical models for a transistor which included the parasitic inductances of the device were presented. In the topology of the synchronous buck converter presented here, the equivalent circuit includes the detailed analytical device models are included. In doing so, the interaction between the multiple devices within the converter are taken into account, allowing for more accurate modeling of the transient phenomena created during switching. In converters such as the synchronous buck converter this is particularly important, as the efficiency of these converters is significantly influenced by the devices' switching losses [2].

In this chapter, the equivalent circuit models presented in [14] and [15] are given practical implementation in a circuit, so as to assess the influence of the parasitic device capacitances on overshoot, ringing, and false turn-on. It will be shown that the source of these detrimental characteristics is due to the low capacitance to inductance ratio in SiC MOSFETs. This will be first observed in a high *dv/dt* test circuit, and will then be expanded to a full model of a synchronous buck converter at the moment of turn on in the first device. The analytical model for the synchronous buck converter is then improved by deriving a state-space model for the same equivalent circuit, allowing for the inclusion of initial charge on device capacitances. This work provides a foundation for semiconductor device optimization. That is, the results presented here can be extended to other switching events and can be used to optimize the size of certain device capacitances, so that switching losses can remain low while the previously described transient concerns can be mitigated. Additionally, although this work is based on the characterization of a SiC MOSFET, many of the transient, many of the transient circuit-level effects discussed apply to GaN HEMTs and GaN MOSFETs.

2.1 PROBLEM CONTEXT: TRANSIENTS IN WBG SEMICONDUCTORS

2.1.1 Voltage Overshoot

The first transient characteristic to be described here is voltage overshoot. This event occurs when a terminal voltage on the device exceeds its maximum rated specification, causing failure of the device. To demonstrate this, consider the EPC2007 [16], a 100 V GaN device from *Efficient Power Conversion* ®. For full channel conductivity, the EPC2007 requires a gate-source voltage of 5 V. At this voltage, the on-resistance of the device is minimized. However, it is also specified on the datasheet of the device that the maximum operating gate-source voltage is 6 V. Thus, only one volt of safety margin is allowed between the desired steady-state operating voltage and the maximum allowable voltage. Due to the fast switching capability of GaN, overshoot is often observed and is usually mitigated with added gate resistance.

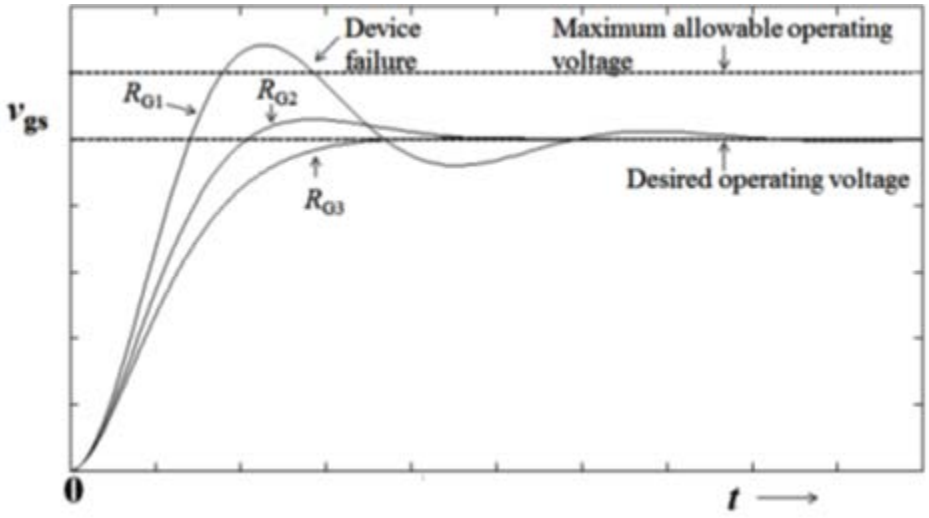


Figure 3. Turn-on characteristic. $R_{G1} < R_{G2} < R_{G3}$

Although the added gate resistance keeps the device in its safe operating regime, it can slow the switching speed of the device and thus increase switching losses. To illustrate this, consider the commonly observed turn-on-characteristic of a device, *v*gs vs *t* as shown in Figure 3 the gate resistance, r_g is varied and $r_{g1} < r_{g2} < r_{g3}$. When r_{g1} is used, the turn-on characteristic is rapid, however the overshoot exceeds the maximum operating voltage of the device, thus causing failure. Conversely, when r_{g3} is used, the device is kept in its safe operating regime, but with reduced switching speed (efficiency). These observations can be illustrated quantitatively if one considers a gate-charging model as shown in Figure 4.

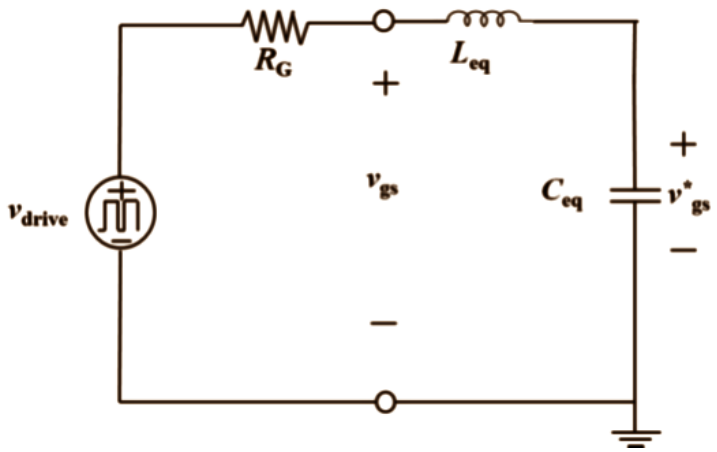


Figure 4: Gate charging circuit

This is an equivalent circuit of the device while charging to conduction. When v_{drive} is a step function (whose laplace transform, $v_{drive}(s)$ equals 1/s), v_{gs} can be derived using frequency domain analysis and expressed as shown in (1):

$$v_{gs}(s) = \frac{1}{s}\left[\frac{\frac{1}{C_{eq}L_{eq}} + s^2}{s^2 + \frac{R_G}{L_{eq}}s + \frac{1}{C_{eq}L_{eq}}}\right] \quad (1)$$

Here s is the Laplace variable, and the system is represented as:

$$v_{\mathrm{gs}}(s) = \mathcal{L}\left(v_{\mathrm{gs}}(t)\right), \quad C_{eq} = C_{\mathrm{GS}} + C_{\mathrm{GD}}, \quad \text{and} \quad L_{\mathrm{eq}} = L_{\mathrm{g}} + \frac{L_{\mathrm{s}} L_{\mathrm{d}}}{L_{\mathrm{s}} + L_{\mathrm{d}}} \tag{2}$$

The definition of all variables are presented in Table 1.

Table 1: Variable Definitions

Component Name	**Full Definition**
C_{GD}	Gate-drain capacitance
C_{GS}	Gate-source capacitance
C_{DS}	Drain-source capacitance
L_{G}	Parasitic gate inductance
L_{D}	Parasitic drain inductance
L_{S}	Parasitic source capacitance
R_{ON}	Transistor on-state resistance

The denominator of (1) can then be compared with the canonical form of second-order systems:

$$s^2 = 2\zeta\omega_{\mathrm{n}} s + \omega_{\mathrm{n}}^2 \tag{3}$$

where ζ is the damping ratio and ω_{n} is the natural frequency of the system. From inspection of (1) and (3), it can be seen that:

$$\zeta = \frac{R_{\mathrm{G}}}{2}\sqrt{\frac{C_{\mathrm{eq}}}{L_{\mathrm{eq}}}} \tag{4}$$

and

$$\omega_{\mathrm{n}} = \frac{1}{\sqrt{C_{\mathrm{eq}} L_{\mathrm{eq}}}} \tag{5}$$

As reported in [12] and [17], WBG transistors traditionally have lower intrinsic capacitance thus making the damping ratio in (4) relatively small. Consequently, the voltage overshoot seen in WBG based conversion circuits can be significant and damaging. The example given here also applies to the drain-source terminal voltage where maximum values are specified.

2.1.2 Ringing

The second transient characteristic examined here is ringing. This characteristic is described by repeated oscillations of a device's voltage for an extended period of time. One example of the detrimental effect of ringing is during device turn-off, as seen in Figure 5.

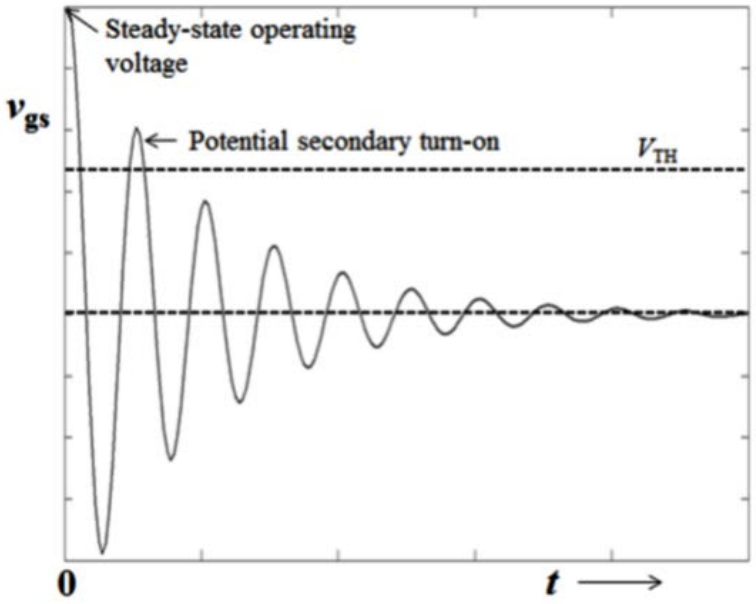


Figure 5. Turn-off characteristic of a device

Due to the relatively low parasitic capacitances in WBG semiconductors, the ringing frequency, seen in (5) is particularly high. As such, there is a possibility of a secondary turn-on by the device

during the transient ringing of the turn-off sequence if the ringing voltage exceeds the threshold voltage, V_{TH} [17]. Both GaN and SiC have relatively low threshold voltages, and therefore the risk of the secondary turn-on during the turn-off cycle is even greater. To damp out the ringing frequency, a higher R_G is required, which again can increase switching losses.

2.1.3 False Turn-on

To illustrate the mechanism of false turn-on, we chose a first order circuit model for a transistor in its off state as shown in Figure 6 [18]. Since the transistor is in its off-state, there is no channel between its drain and source terminals, and the input gate signal is effectively at ground potential. If during power conversion operation, a high *dv/dt* is induced on the drain terminal of the transistor in Figure 6, a current will flow through the gate-drain capacitance, C_{GD}.

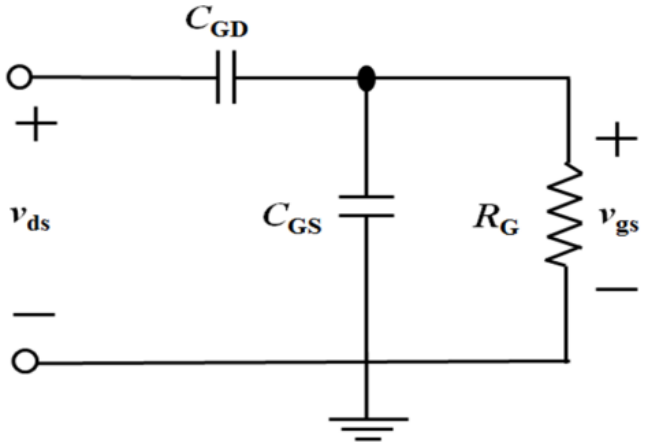


Figure 6. First order circuit model for transistor in off-state **[19]**

In turn, a current flows out of the gate of the transistor and across the external gate resistor, R_G. If the resulting voltage across R_G exceeds the threshold voltage of the device, the transistor is forced

into conduction spuriously leading to significant switching losses [19]. In analyzing the circuit in Figure 6, the transfer function from v_{ds} to v_{gs} can be expressed as follows:

$$\frac{v_{gs}(s)}{v_{ds}(s)} = \frac{sR_G C_{GD}}{1 + sR_G(C_{GD} + C_{GS})} \tag{6}$$

The Laplace variable, "*s*" in a transfer function also corresponds to an operation of differentiation in the time domain. Therefore (6) offers insights about the *dv/dt* in the power conversion circuit. In WBG based power converters, the *dv/dt* is significantly high, due to the very fast switching capability of GaN and SiC. This can make the susceptibility to false turn-on higher in WBG based circuits. Furthermore, from (6) it can be seen that higher values of R_G will induce a larger v_{gs} during false turn-on. It has been explained in previous sections that a larger R_G may be necessary in WBG based circuits to damp out transient overshoot and oscillation, and thus tuning the value of R_G to obtain optimal circuit behavior is particularly essential yet time-consuming in WBG based power converters. Finally, the lower threshold voltage of WBG devices also makes them more vulnerable to high *dv/dt* induced false turn-on effects, but on the other hand, WBG based devices have a low gate charge ratio, Q_{GD} to Q_{GS} which may prevent false turn-on behavior [20]. These opposing effects point to the increased need for accurate device/circuit models such that circuit performance can be optimized through design simulation.

Having discussed three common transient phenomena particularly affecting the performance of WBG semiconductors, the goal of this paper is to model these characteristics, with experimental validation. The results obtained from the analytical equivalent models can be used to optimize the design of next generation WBG semiconductors so that switching losses remain low while undesirable transient behavior is eliminated.

2.2 HIGH *DV/DT* TEST CIRCUIT

2.2.1 System Modeling and Validation

Shown in Figure 7(a) is the proposed high *dv/dt* test circuit utilized here to analytically and experimentally study transient behavior in an example SiC MOSFET [21], from Powerex®. The gate terminal of the MOSFET is grounded via an external gate resistor, R_G. A square wave from a function generator is used to drive the drain terminal of the transistor, via an external test resistance, R_D. Shown in Figure 7(b) is the complete circuit model for Figure 7(a), which includes all the parasitic components of the MOSFET, as well as the parasitic inductance of the two resistors, denoted as L_{RD} and L_{RG}. A rearrangement of the elements in Figure 7(b) is shown in Figure 7(c), where the MOSFET is in its off-state, with no channel formed.

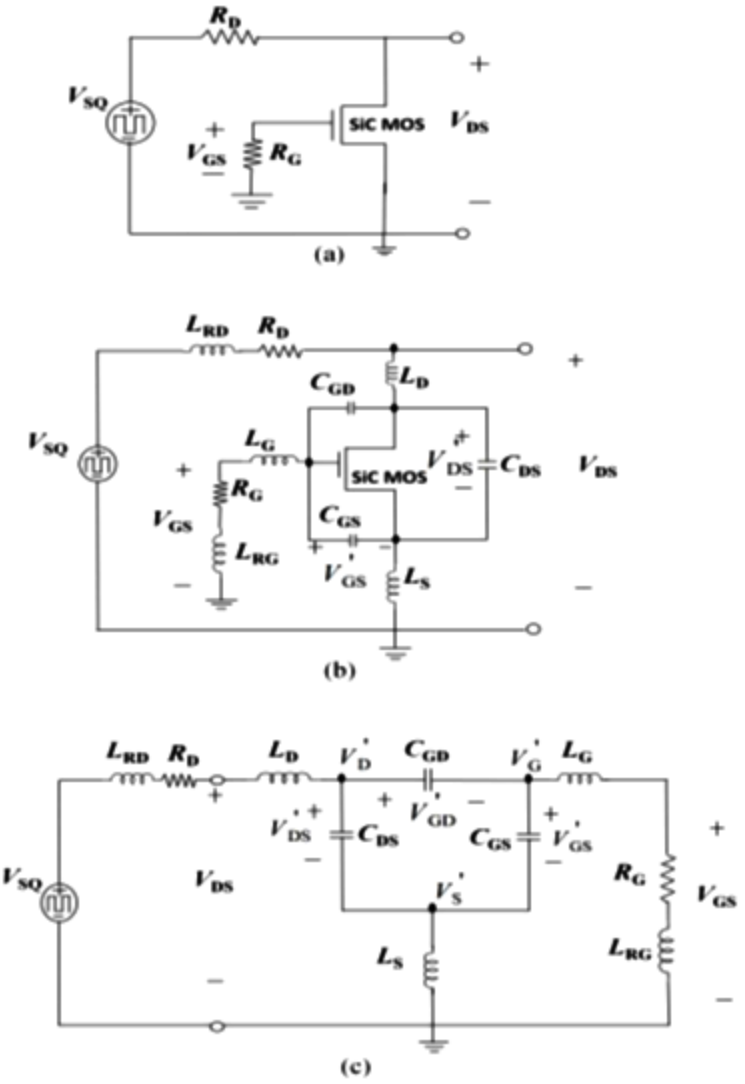


Figure 7. (a) High *dv/dt* test circuit. (b) Test circuit including parasitic components. (c) Equivalent test circuit with SiC MOSFET in off state.

It is desired to analytically model the behavior of the gate-source and drain-source voltages, where the generated square wave input is modeled as a unit step function. From analyzing the node currents in Figure 7(c), the following expressions can be obtained. Table 2 provides the parameters of the components in the derived equations.

$$\frac{V_{\mathrm{SQ}} - V_{\mathrm{DS}}}{sL_{\mathrm{RD}} + R_{\mathrm{D}}} = \frac{V_{\mathrm{DS}} - V'_{\mathrm{D}}}{sL_{\mathrm{D}}} \tag{7}$$

$$\frac{V_{\mathrm{DS}} - V'_{\mathrm{D}}}{sL_{\mathrm{D}}} = (V'_{\mathrm{DS}})sC_{\mathrm{DS}} + (V'_{\mathrm{GD}})sC_{\mathrm{GD}} \tag{8}$$

$$(V'_{\mathrm{GD}})sC_{\mathrm{GD}} = (V'_{\mathrm{DS}})sC_{\mathrm{DS}} + \frac{V'_{\mathrm{G}}}{sL_{\mathrm{G}} + R_{\mathrm{G}}} \tag{9}$$

$$\frac{V'_{\mathrm{S}}}{sL_{\mathrm{S}}} = (V'_{\mathrm{DS}})sC_{\mathrm{DS}} + (V'_{\mathrm{GS}})sC_{\mathrm{GS}} \tag{10}$$

$$\frac{V'_{\mathrm{G}} - V_{\mathrm{GS}}}{sL_{\mathrm{G}}} = \frac{V_{\mathrm{GS}}}{R_{\mathrm{G}} + sL_{\mathrm{RG}}} \tag{11}$$

Table 2. Parameters for high *dv/dt* test circuit

Parameter	Value
C_{DS}	2.75 nF
C_{GD}	0.25 nF
C_{GS}	11 nF
L_{D}	15 nH
L_{G}	15 nH
L_{S}	1 nH
L_{RD}	50 nH
L_{RG}	50 nH
R_{D}	5 Ω
R_{G}	5 Ω
V_{SQ}	50 V

In solving (7)-(11) simultaneously, the step responses for the gate-source and drain-source voltages were obtained. These modeled results are shown in Figure 8 and Figure 9 with their experimental counterparts plotted simultaneously with the analytical data. Both analytical figures show relatively good agreement with their experimental counterparts. As seen in Figure 8, the gate-source voltage rises rapidly to approximately 3 V during the false turn-on, and then oscillates

around 0 V for approximately 500 ns before settling. The minimum threshold voltage of the SiC MOSFET is 1.5 V, and therefore false turn-on occurs.

As can be seen in Figure 9, the drain-source voltage rises and oscillates for approximately 500 ns before settling at 50 V. It should be noted that the minor discrepancies between the analytical and experimental waveforms can be attributed to the linear modeling of the parasitic device capacitances. In reality, the capacitances vary non-linearly with both the drain-source and gate-source voltages. Creating an analytical switched model that can account for these dynamics is the subject of our future work.

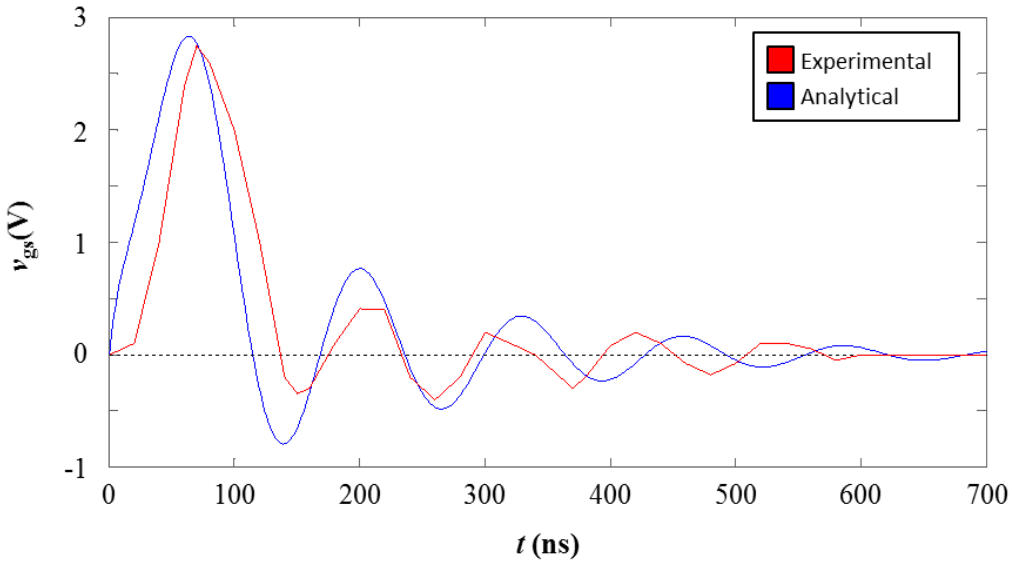


Figure 8. Analytical and experimental step response for v_{gs}

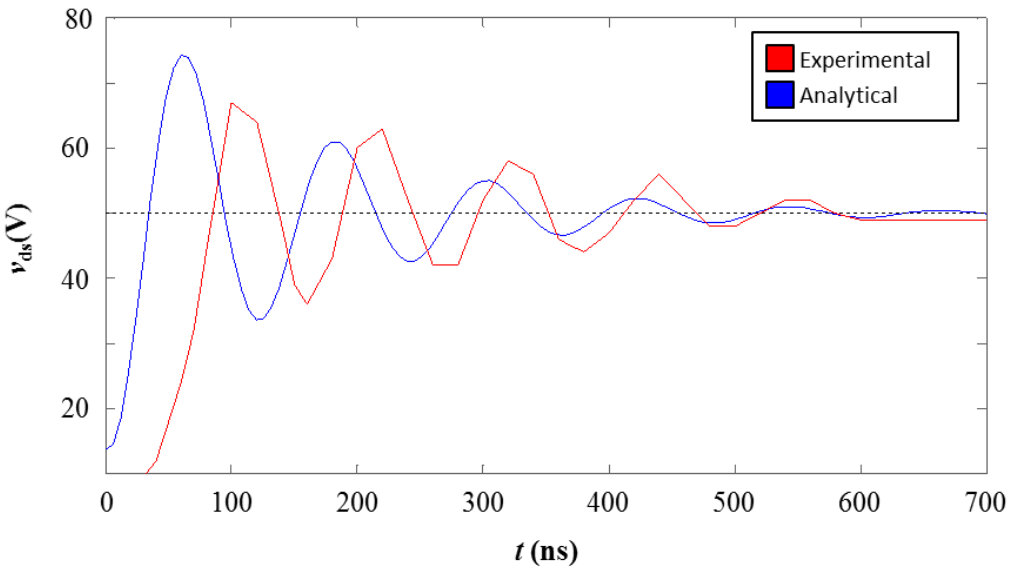
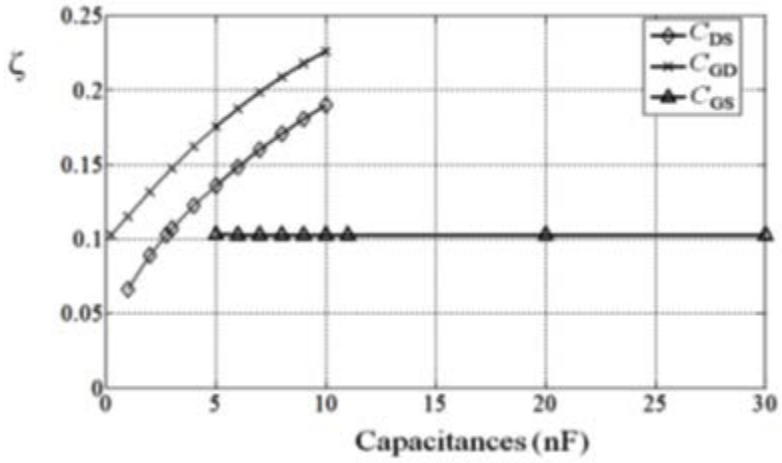
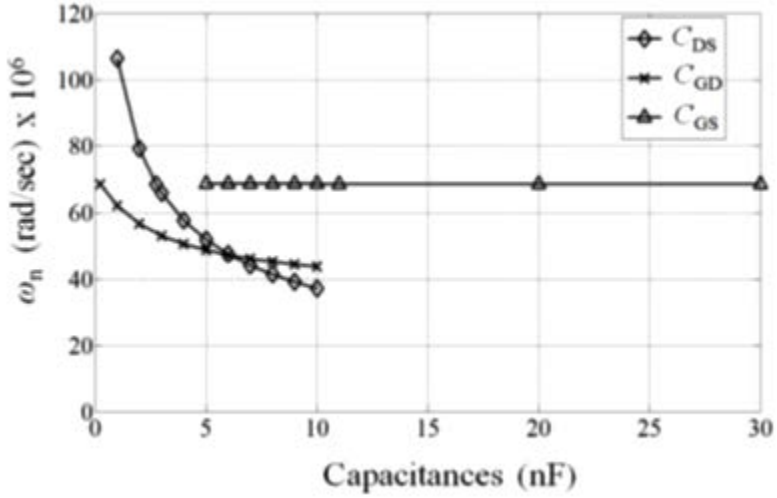


Figure 9. Analytical and experimental step response for v_{ds}

In the proposed analytical model, the frequency domain expression for the drain source voltage consists of a damping ratio, ζ and natural frequency, ω_n. Figure 10(a) and Figure 10(b) show how each of the capacitances of the SiC MOSFET affect ζ and ω_n. This analysis was accomplished by individually varying each capacitance in the model and consequently evaluating the system's new ζ and ω_n. The trends shown in Figure 10 provide a better picture about how each capacitance affects the overshoot, ringing, rise time, and settling time of approximately 1 V, whereas previously in Figure 8 it was shown to be 3 V under nominal conditions. This shows the advantage of C_{GS} in suppressing the magnitude of the induced gate-source voltage during false turn-on. It should be noted that higher values of C_{GS} would lead to increased switching losses during intended turn-on of the device, thereby pointing to the need of parameter optimization in WBG based power conversion circuits which contain high *dv/dt* effects.



(a)



(b)

Figure 10. Damping ratio and natural frequency vs device capacitances.
(a) Damping ratio. (b) Natural frequency.

2.2.2 Effect of C_{GS} on Gate-Source Voltage

To further demonstrate the model's validity, it was desired to assess the effect of the gate-source capacitance on the magnitude of the induced gate-source voltage. From analysis of the transfer

function seen in (6), it can be inferred that large values of C_{GS} can suppress the magnitude of the induced gate-source voltage during false turn-on. Shown in Figure 11 is the analytical model's predicted gate-source voltage when the value of C_{GS} is increased to 30 nF. The experimental counterpart is also shown in Figure 11. To experimentally obtain 30 nF of gate-source capacitance, a 19 nF capacitor was placed across the gate and source terminals of the SiC MOSFET. This external capacitance was effectively in parallel with the device's intrinsic C_{GS} of 11 nF. Therefore the total C_{GS} is 30 nF. As seen in Figure 11, reasonable agreement is obtained in the trend and behavior of the induced gate-source voltage during false turn-on. The peak voltage is now approximately 1 V, whereas previously in Figure 8 it was shown to be 3 V under nominal conditions. This shows the advantage of C_{GS} in suppressing the magnitude of the induced gate-source voltage during false turn-on. It should be noted that higher values of C_{GS} would lead to increased switching losses during intended turn-on of the device, thereby pointing to the need of parameter optimization in WBG-based power conversion circuits which contain high *dv/dt* effects.

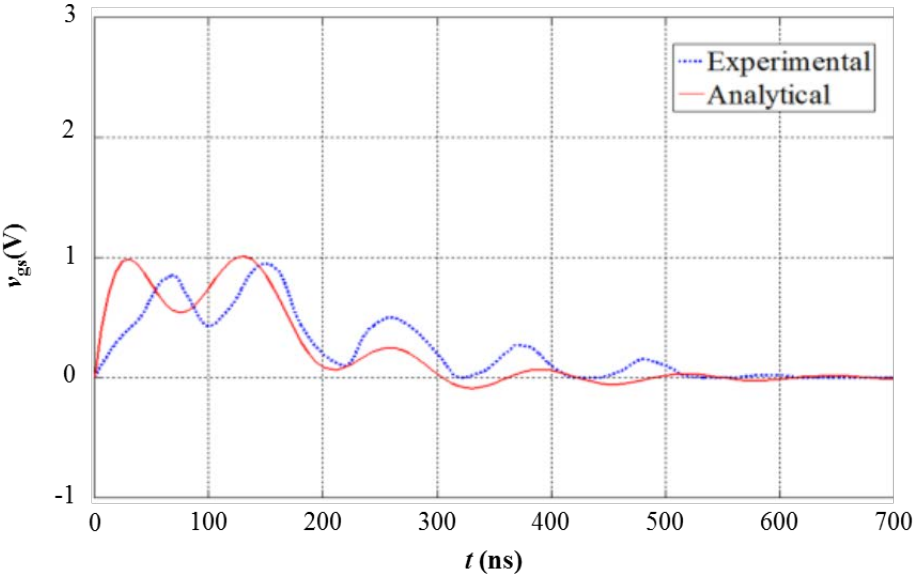


Figure 11. Analytical and experimental induced gate-source voltage with C_{GS} = 30 nF

The data reported in this section are intended to aid in the design of future generation WBG semiconductor devices. The equivalent circuit models shown here can be used to optimize the area and layout of forthcoming WBG devices, so that certain capacitances can be retained to reduce detrimental transient behavior while keeping switching losses minimal. In the next section, a practical example for such a problem is presented, using the synchronous buck converter, a classic low voltage power conversion circuit.

2.3 FALSE TURN-ON IN SYNCHRONOUS BUCK CONVERTERS

2.3.1 Problem Context

The synchronous buck converter shown in Figure 12 is becoming the preferred circuit topology for low voltage power electronic applications requiring attenuation of the input signal [22]. The synchronous buck converter contains a high side FET, Q_1, and a low side FET, Q_2.

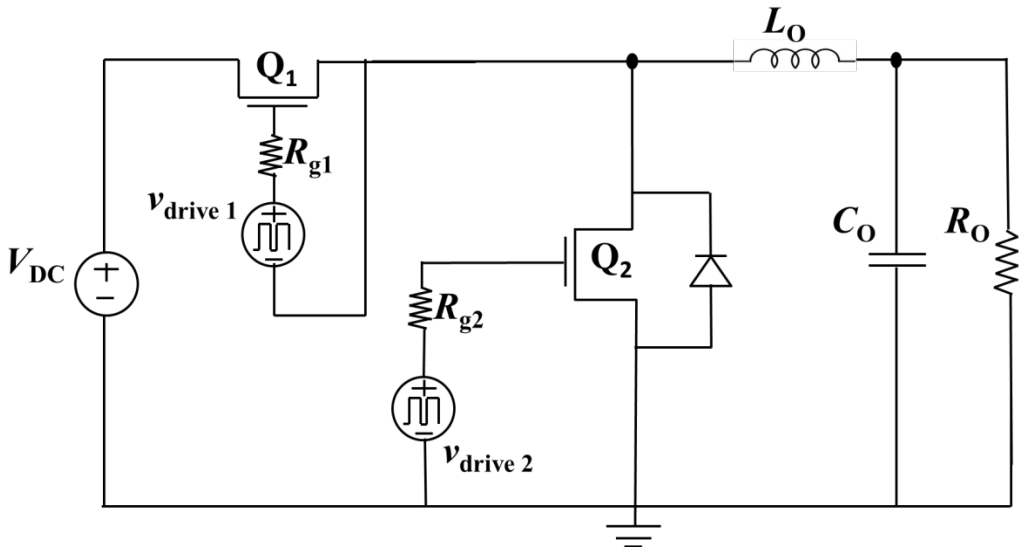


Figure 12. Synchronous buck converter

Relative to the conventional buck converter which uses a diode instead of Q_2, the synchronous buck converter has the advantage of significantly reducing the conduction losses observed in the conventional buck converter.

However, if Q_2 suffers from high *dv/dt* induced false turn-on during its off-state, the switching losses of the synchronous buck converter can become undesirably high. To illustrate the mechanism of false turn-on, a first order circuit model for Q_2 in its off-state is shown in Figure 6

[18]. Since Q_2 is in its off-state, there is no channel between its drain and source terminals, and the input gate signal is effectively at ground potential. During the rapid turn-on of Q_1, a high *dv/dt* is induced on the drain terminal of Q_2 leading to a current through the gate-drain capacitance, C_{gd2}. In turn, a current flows out of the gate of Q_2 and across the external gate resistor, R_{g2}. If the resulting voltage across R_{g2} exceeds the threshold voltage V_{TH2}, of Q_2, the device is forced into conduction spuriously leading to significant switching losses. When analyzing Figure 6, it can be inferred that larger values of C_{gs2} will reduce the induced gate-source voltage, v_{gs2}, during false turn-on. However, the value of C_{gs2} should not be designed to be too large, otherwise the switching losses during intended turn-on will become undesirably high. This optimization problem necessitates a better understanding of the false turn-on of Q_2 in synchronous buck converters as well as other high *dv/dt* circuits for improving the efficiency of future generation power electronics [23], [24].

The issue of false turn-on has been discussed in previous reports from the literature. In [25], it was shown that the existence of the common source inductance between Q_1 and Q_2 can reduce the possibility of false turn-on. In [19], the potential benefits of false turn-on were discussed, where it was demonstrated that false turn-on can reduce the oscillations in various signals of the synchronous buck converter. Therefore, optimizing the amount of false turn-on of Q_2 in synchronous buck converters is crucial in order to ensure more efficient converter operation. As a necessity for optimization, an analytical model which can accurately reproduce the experimental waveforms of the converter is needed. The goal of this paper then is to present a comprehensive analytical converter model which includes all the parasitic components of both Q_1 and Q_2 and reproduces the experimental waveforms of the converter during false turn-on. Once the waveforms can be reproduced and the model is proven to be valid, optimization of each circuit parameter can occur so that the potential benefits of false turn-on can be fully utilized and its

parasitic effects can be mitigated. Analytically reproducing experimental waveforms in order to gain more insight into false turn-on behavior is the subject of this section, while optimization of the analytical model will be the subject of our future work.

2.3.2 Experimental Waveforms

In order to understand the phenomenon of false turn-on in Q_2, the synchronous buck converter in Fig. 1 was experimentally constructed and tested. An analytical model would then be developed around the measured data from the circuit. The nominal parameter values and testing conditions used in the circuit are seen in Table 3.

Table 3. Nominal circuit parameters used to construct synchronous buck converter.

Parameter	Value
R_{g1}	100 Ω
R_{g2}	5 Ω
L_O	2.5 mH
C_O	10 mF
R_O	10 Ω
V_{DC}	50 V
v_{drive1}	20 V
v_{drive2}	20 V
f_{sw}	10 kHz

A Silicon (Si) based MOSFET from Vishay [26] (P/N IRF740A) served as Q_1, while a Silicon Carbide (SiC) MOSFET from Powerex [27] (P/N QJD1210007) was used as Q_2. For the explicit purpose of preventing false turn-on, using a Si FET as Q_1 and a wide bandgap semiconductor like SiC as Q_2 simulates a an ideal scenario. If a Si FET is used as Q_1, it would, take longer to charge the FET to conduction, since Si based FETs generally have relatively larger parasitic capacitances.

Thus a slower *dv/dt* would appear at the drain terminal of Q_2 and as a result, false turn-on of Q_2 would be less likely to occur. Further, the magnitude of the induced v_{gs2} on wide bandgap semiconductors like SiC is likely to be less than it would in a traditional FET during false turn-on, since C_{gd} in a SiC FET is relatively smaller. Thus, in this case study, any observed false turn-on in Q_2 implies that even more false turn-on would occur if a faster wide bandgap semiconductor would be used for Q_1 (with similar voltage and current ratings) and/or if a Si based FET would be used for Q_2 (with similar voltage and current ratings). This is an essential study particularly as the adoption of wide bandgap semiconductors becomes more widespread for enhancing the performance of next generation power electronic systems.

During the interval where Q_1 is at the point of turn-on, voltage measurements were then taken for v_{gs1}, v_{ds2}, and v_{gs2}, which can be seen in Figure 13. In order to account for extraneous experimental parasitics both from instrumentation and circuit wiring, the insight and observations presented in [28] were taken into consideration. As observed in Figure 13, v_{gs1} initially increases towards its steady-state value with no oscillation. However, as the channel completely forms in Q_1, the impedance of Q_2 becomes apparent to Q_1. This can be observed as the drop and subsequent transient recovery of v_{gs1} and corresponding dramatic rise of v_{ds2}. Both of these phenomena can be seen clearly within the first 250 nanoseconds in the plots for v_{gs1} and v_{ds2}. Furthermore, the quick rise in v_{ds2} corresponds to a rapid transient response in v_{gs2}, one that is sufficiently large enough to produce false turn-on in Q_2.

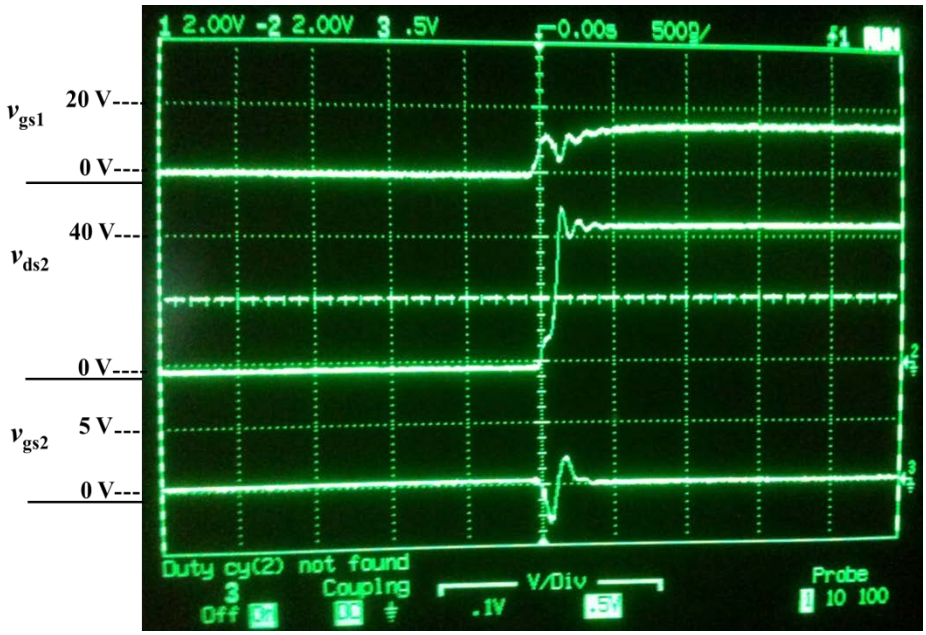


Figure 13. Experimental waveforms for false turn-on. 10:1 testing probes were used for measurement, while the scope measurement is set to 1:1.

As seen in Figure 13, the waveform for v_{gs2}, its induced magnitude is approximately 2.5 V, which is higher than the SiC MOSFET's minimum threshold voltage of 1.5 V, and therefore false turn-on occurs.

From inspection of the converter in Figure 12, the waveform for v_{ds1} can be surmised as the difference between a constant DC voltage source and the given waveform for v_{ds2} seen in Figure 13. Therefore, any oscillations in v_{ds2} can be inferred to occur in v_{ds1} but opposite in direction. Thus, the ability of the parasitic components of Q_2 to affect the behavior of v_{gs1} and v_{ds1} shows that the switching losses of Q_1 will depend not only on its own parasitic components, but also on the parasitic components of Q_2. Consequently, a full circuit model for Q_1 during turn-on should include a model for Q_2 as well. The goal then becomes to model this phenomenon analytically in order to predict false turn-on and optimize system parasitics. The following section will therefore analytically detail the stages of false turn-on in the synchronous buck converter where the results

will match the experimental waveforms given here, thereby providing a path towards system optimization.

2.3.3 Frequency Domain Model of Synchronous Buck Converter: Stages of False Turn-on

A. Substage I: Charging of Q_1 to Conduction

Just prior to false turn-on occurring, the converter is in its "dead-time" where both devices are non-conductive so that the "shoot through" (simultaneous conduction) problem is avoided. During the dead-time, Q_1 is in its off state while the body diode of Q_2 conducts current in the upward direction. The equivalent circuit for this situation is shown in Figure 14, where v_{drive1} is effectively zero volts.

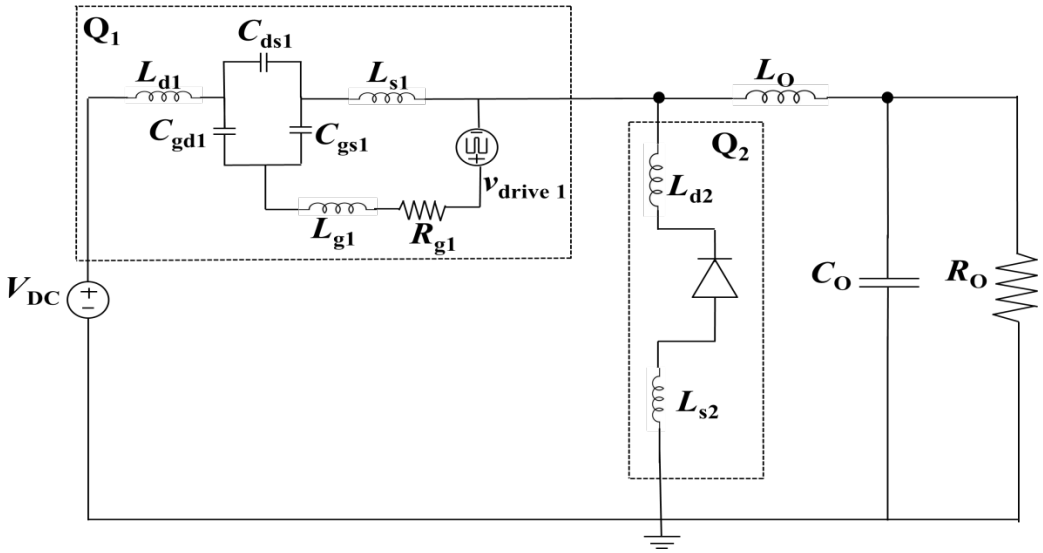


Figure 14. Synchronous buck converter during dead time interval

Then v_{drive1} begins to charge the gate of Q_1 so that v^*_{gs1} increases towards V_{TH1}. Before v^*_{gs1} reaches V_{TH1}, the MOSFET is open-circuited, and therefore v_{ds1} remains constant implying that C_{ds1} can be removed from the initial analysis. As the body diode of Q_2 has a very small voltage across it, the source-terminal of Q_1 is effectively at ground potential during this phase. The equivalent circuit for this sub-stage is shown in Figure 4, and experience turn-on as described in section 2.1.1, with the waveform described by (1).

B. Substage II: Formation of Q_1 Channel

As v_{drive1} charges the gate of Q_1, the circuit in Figure 4 is valid until v^*_{gs1} reaches V_{TH1} at which point a channel is gradually formed across the drain and source terminals of Q_1. As the channel forms, v_{ds1} decreases. When the channel is completely formed, v_{ds1} reaches its minimum steady-state value (approximately zero, depending on the value of R_{ON1}) and remains constant. The equivalent circuit for the entire synchronous buck converter at this particular moment is shown in Figure 15. Since the entire circuit now feels the effect of V_{DC}, the body diode of Q_2 stops conducting and therefore Q_2 assumes its off-state model. A simplified version of Figure 15 is shown in Fig. 6(b) where the node voltages are clearly indicated. From analysis of Fig. 6(b) the following equations can be used in order to analytically create the experimental waveform of v_{gs1} seen in Figure 13.

$$\frac{v_{ds2} + v_{drive1} - v^*_{g1}}{R_{g1} + sL_{g1}} + sC_{gd1}\left(v^*_{d1} - v^*_{g1}\right) = sC_{gs1}(v^*_{g1} - v^*_{s1}) \tag{12}$$

$$\frac{v_{ds2} + v_{drive1} - v_{g1}}{R_{g1}} = \frac{v_{g1} - v^*_{g1}}{sL_{g1}} \tag{13}$$

$$\frac{V_{DC} - v^*_{d1}}{sL_{d1}} = \frac{v^*_{d1} - v^*_{s1}}{R_{ON1}} + sC_{gd1}\left(v^*_{d1} - v^*_{g1}\right) \tag{14}$$

$$\frac{v_{\mathrm{d1}}^{*}-v_{\mathrm{s1}}^{*}}{R_{\mathrm{ON1}}+sC_{\mathrm{gs1}}\left(v_{\mathrm{d1}}^{*}-v_{\mathrm{s1}}^{*}\right)}=\frac{v_{\mathrm{s1}}^{*}-v_{\mathrm{ds2}}}{sL_{\mathrm{s1}}} \tag{15}$$

$$\frac{v_{\mathrm{s1}}^{*}-v_{\mathrm{ds2}}}{sL_{\mathrm{s1}}}=\frac{v_{\mathrm{ds2}}+v_{\mathrm{gs1}}-v_{\mathrm{g1}}^{*}}{sL_{\mathrm{g1}}}+\frac{v_{\mathrm{ds2}}}{Z_{\mathrm{eq}}} \tag{16}$$

$$v_{\mathrm{gs1}}=v_{\mathrm{g1}}-v_{\mathrm{ds2}} \tag{17}$$

where Z_{eq} represents the equivalent impedance of the off-state model for Q_2 in parallel with the output of the converter, seen in Fig. 6(c).

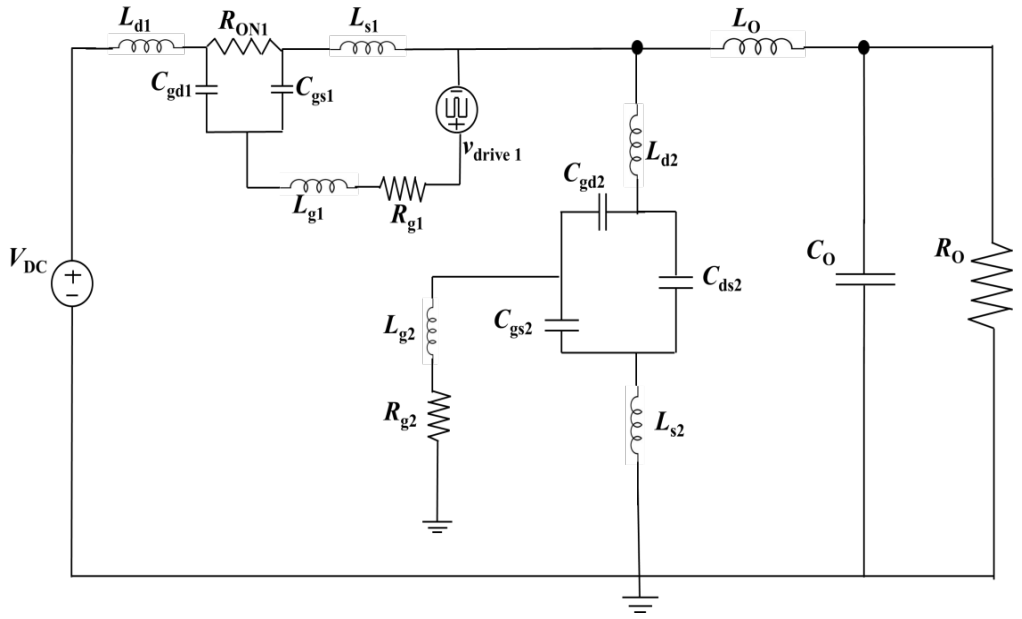


Figure 15. Equivalent circuit for the converter immediately after formation of Q_1 channel

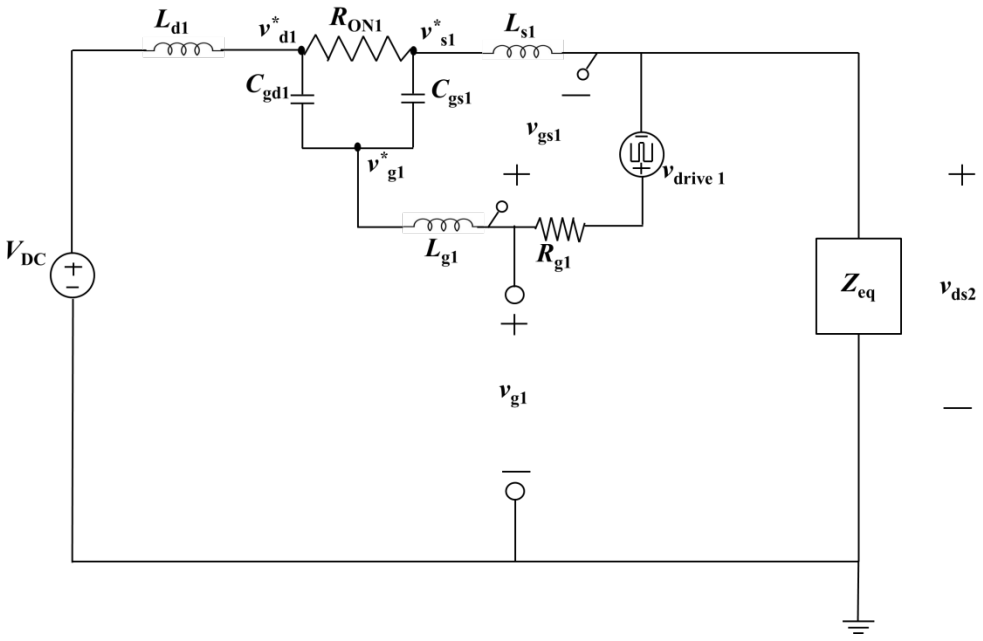


Figure 16. Simplified version of Figure 15 with node voltages indicated for Q_1

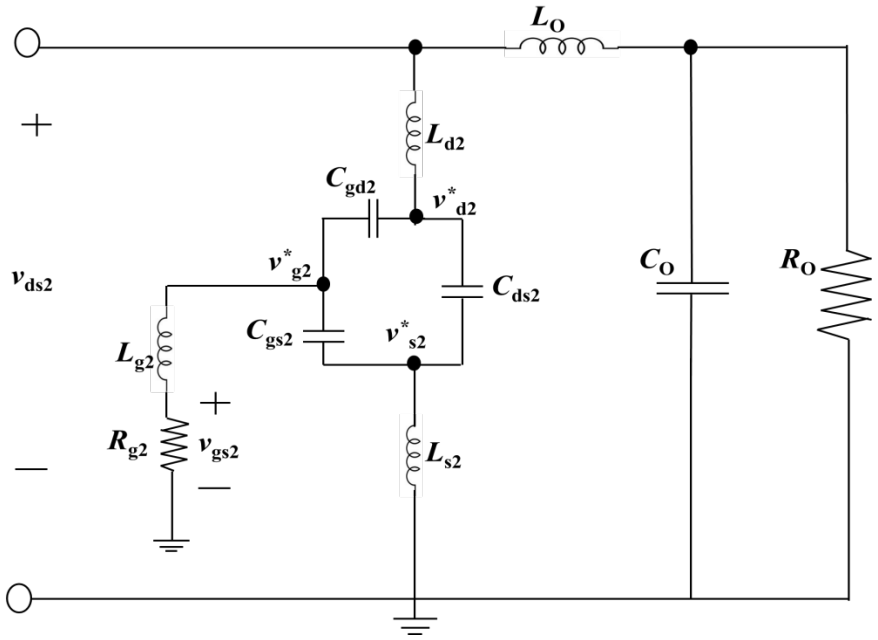


Figure 17. Equivalent circuit for Zeq of Figure 16 with node voltages indicated for Q_2

Shown in Table 4 are the circuit and transistor parameter values corresponding to the physical circuit, which were used to perform the calculations presented in this section. The capacitance values for each transistor were taken from the datasheets. Constant values for the parasitic capacitances were used, thus making the analytical model a linear approximation of the nonlinear parasitic elements. It is known that each parasitic capacitance varies nonlinearly with the drain-source voltage, but has shown that using linear circuit approximations for transistors can still produce valid results.

Table 4. Analytical model parameter values

Parameter	Value
R_{ON1}	0.5 Ω
R_{g1}	100 Ω
R_{g2}	5 Ω
R_O	10 Ω
C_O	10 mF
C_{gd1}	0.0077 nF
C_{gs1}	1.022 nF
C_{gd2}	0.25 nF
C_{gs2}	10.75 nF
C_{ds2}	2.75 nF
L_O	2.5 mH
$L_{d1}, L_{g1}, L_{s1}, L_{s2},$	1 nH
$L_{d2}, L_{g2},$	15 nH
V_{DC}	50 V
v_{drive1}	20 V
v_{drive2}	20 V

The parasitic inductance values were estimated using $v=L\,di/dt$. While it is known that the parasitic inductors can also play a role in the false turn-on of Q_2 in synchronous buck converters due to increased di/dt, this section only examines the effects of dv/dt as induced by the parasitic capacitances. The value for R_{ON1} was taken from the datasheet of Q_1. Equations (12) through (17) were solved simultaneously in order to evaluate the turn-on characteristics of Q_1. The result of the solved system is the step response for v_{gs1}, seen in Fig. 7, is obtained. Here, the step response for v_{gs1} is obtained by treating both V_{DC} and v_{drive1} as step-input voltages and thus invoking the superposition theorem. It should be noted that in practice V_{DC} is always on, and is therefore not a step function. However, modeling V_{DC} as a step function simulates the formation of the channel and the resulting near-instantaneous effect that V_{DC} has on the rest of the circuit.

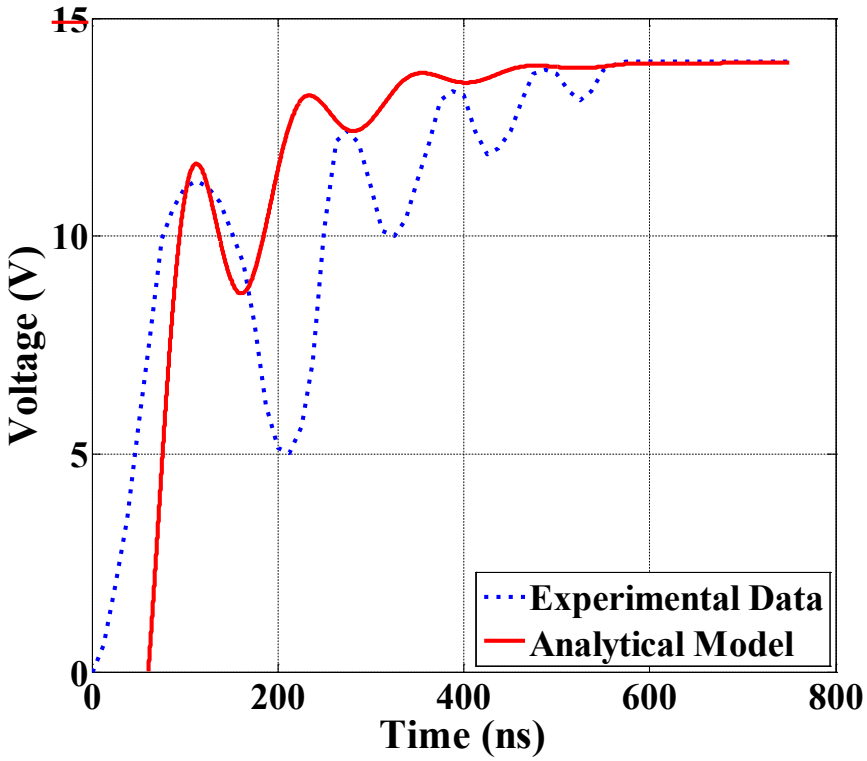


Figure 18. Analytical step response for vgs1 compared with experimental vgs1

When comparing the analytical step response for v_{gs1} with the experimental result, reasonable agreement is obtained. Both waveforms show significant oscillation, with no overshoot above the steady-state value of 14V. The trend and phase of the oscillations in both waveforms are similar as well. However, the magnitude of the oscillations is greater for the experimental result. This could be due to additional parasitics induced by the testing and measuring equipment, or from lack of inclusion of initial stored energy on the device capacitances.

Using the proposed model, the oscillations in v_{gs1} can now be explained. Prior to v^*_{gs1} reaching V_{TH1}, the gate of Q_1 is charged by v_{drive1} and the circuit in Figure 4 is valid. During this interval, v_{gs1} increases with no oscillation. When v^*_{gs1} reaches V_{TH1}, a channel is formed across Q_1 and v_{ds1} decreases to its steady-state value. When the channel is completely formed, the circuit in Figure 15 applies: current flows through Q_1 and charges the parasitic capacitances of Q_2, forcing v_{ds2} to increase. As v_{ds2} increases and the parasitic capacitances of Q_2 continue to charge, the current through Q_2 decreases, thus decreasing the current through Q_1. As a result, v_{ds1} decreases since now the product of i_1 and R_{ON1} will be lower. Due to capacitive coupling, the transient decrease in v_{ds1} leads to a transient decrease in v_{gs1}, which is the first oscillatory dip at 125 nanoseconds seen in both the analytical and experimental result in Figure 18. As v_{drive1} continues to charge the gate of Q_1, v_{gs1} resumes its exponential increase towards its steady state value before settling at approximately 500 nanoseconds.

In order to derive the proper response for v_{gs1}, the parasitic components of Q_2 needed to be included in the full circuit model. Thus, the switching losses of Q_1 depend not only on its own parasitic components, but also on the parasitic components of Q_2. In subsequent sections, it will be shown that inducing false turn-on in Q_2 will affect both the turn-on behavior and the switching losses of Q_1, thus necessitating design optimization.

C. Substage III: Rise in v_{ds2}

After the channel across the drain and source terminals of Q_1 forms, v_{ds2} increases approximately to the value of the input voltage, V_{DC}. Therefore the relations seen in (12)-(17) remain relatively unchanged, with the exception that v_{drive1} is no longer considered an input as it is assumed to have reached its steady-state value. Thus, to derive the proper response for v_{ds2}, only V_{DC} is considered as a step input voltage. As a result, (12) and (13) take on the form seen in (18) and (19), respectively, while the relationships (14)-(17) remain the same.

$$\frac{v_{\mathrm{ds2}} - v_{\mathrm{g1}}^*}{R_{\mathrm{g1}} + sL_{\mathrm{g1}}} + sC_{\mathrm{gd1}}\left(v_{\mathrm{d1}}^* - v_{\mathrm{g1}}^*\right) = sC_{\mathrm{gs1}}(v_{\mathrm{g1}}^* - v_{\mathrm{s1}}^*) \tag{18}$$

$$\frac{v_{\mathrm{ds2}} - v_{\mathrm{g1}}}{R_{\mathrm{g1}}} = \frac{v_{\mathrm{g1}} - v_{\mathrm{g1}}^*}{sL_{\mathrm{g1}}} \tag{19}$$

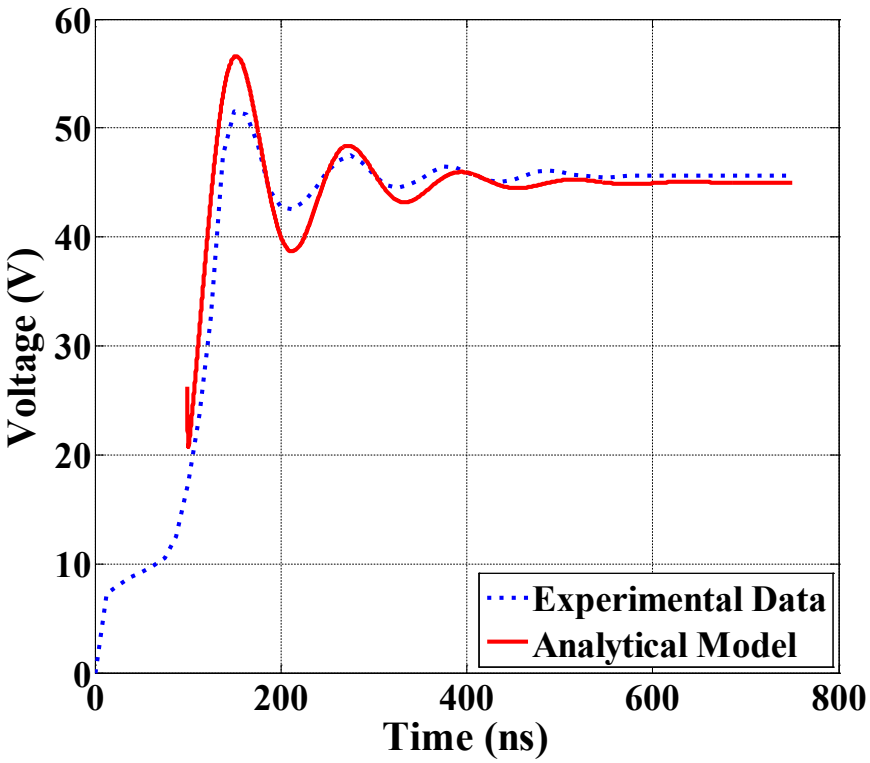


Figure 19. Step response for v_{ds2} compared with experimental v_{ds2}.

Upon solving (14)-(19) simultaneously, the step response for v_{ds2} as a result of the turn of Q_1 and the can be obtained as shown in Figure 19. When comparing the analytical v_{ds2} with the experimental v_{ds2}, adequate agreement is again obtained. As seen in both figures, immediately after the channel of Q_1 is formed, v_{ds2} rises, overshoots, and undershoots its steady state value three times, with each overshoot and undershoot becoming smaller in magnitude. Eventually v_{ds2} reaches its steady-state value at approximately 500 nanoseconds. As previously mentioned, the waveform for v_{ds1} can be assumed as the difference between V_{DC} and v_{ds2}. Therefore, the oscillations seen for v_{ds2} in Figure 19 also occur in v_{ds1} but opposite in direction. In the previous section it was demonstrated that the parasitic components of Q_2 will affect the behavior of v_{gs1} during turn-on. Here, it is shown that the parasitic components of Q_2 will affect the behavior of v_{ds1} during turn-on as well. Thus, the parasitic components of Q_2 have an influence on the switching losses of Q_1 during turn-on and should not be excluded when analyzing the turn-on behavior of Q_1.

D. Substage IV: Spike in v_{gs2}

When v_{ds2} increases rapidly, the *dv/dt* seen at the drain terminal of Q_2 is high, thus inducing a current through C_{gd2} as well as through C_{ds2}. Consequently, C_{gd2} current will cause a voltage to develop across R_{g2} despite the fact that the driving signal of Q_2 is effectively at ground potential. If the voltage across R_{g2} exceeds V_{TH2}, the device is forced into conduction, creating the condition of false turn-on. To model these transitions, the circuit in Figure 17 is utilized where v_{ds2} is a known quantity found in the derivation of Substage III. This leads to the derivation of (20) through (24).

$$\frac{v_{\mathrm{ds2}} + v_{\mathrm{d2}}^*}{sL_{\mathrm{d2}}} + sC_{\mathrm{ds2}}(v_{\mathrm{d1}}^* - v_{\mathrm{s2}}^*) = sC_{\mathrm{gd2}}(v_{\mathrm{d2}}^* - v_{\mathrm{g2}}^*) \tag{20}$$

$$C_{\mathrm{gd2}}\left(v_{\mathrm{d2}}^{*}-v_{\mathrm{g2}}^{*}\right)=\frac{v_{\mathrm{g2}}^{*}}{R_{\mathrm{g2}}+sL_{\mathrm{g2}}}+sC_{\mathrm{gs2}}(v_{\mathrm{g2}}^{*}-v_{\mathrm{s2}}^{*}) \tag{21}$$

$$sC_{\mathrm{ds2}}(v_{\mathrm{d2}}^{*}-v_{\mathrm{s2}}^{*})+sC_{\mathrm{gs2}}(v_{\mathrm{g2}}^{*}-v_{\mathrm{s2}}^{*})=\frac{v_{\mathrm{s2}}^{*}}{sL_{\mathrm{s2}}} \tag{22}$$

$$\frac{v_{\mathrm{g2}}^{*}-v_{\mathrm{gs2}}}{sL_{\mathrm{g2}}}=\frac{v_{\mathrm{gs2}}}{R_{\mathrm{g2}}} \tag{23}$$

$$\frac{v_{\mathrm{ds2}}}{V_{\mathrm{DC}}}\frac{v_{\mathrm{gs2}}}{v_{\mathrm{ds2}}}=\frac{v_{\mathrm{gs2}}}{V_{\mathrm{DC}}} \tag{24}$$

In solving (20)-(24) simultaneously, the step response for v_{gs2} can be obtained as seen in Figure 20, where again V_{DC} is the input and is considered to be a unit step function. When comparing the analytical result with the experimental result**,** reasonable agreement is again obtained.

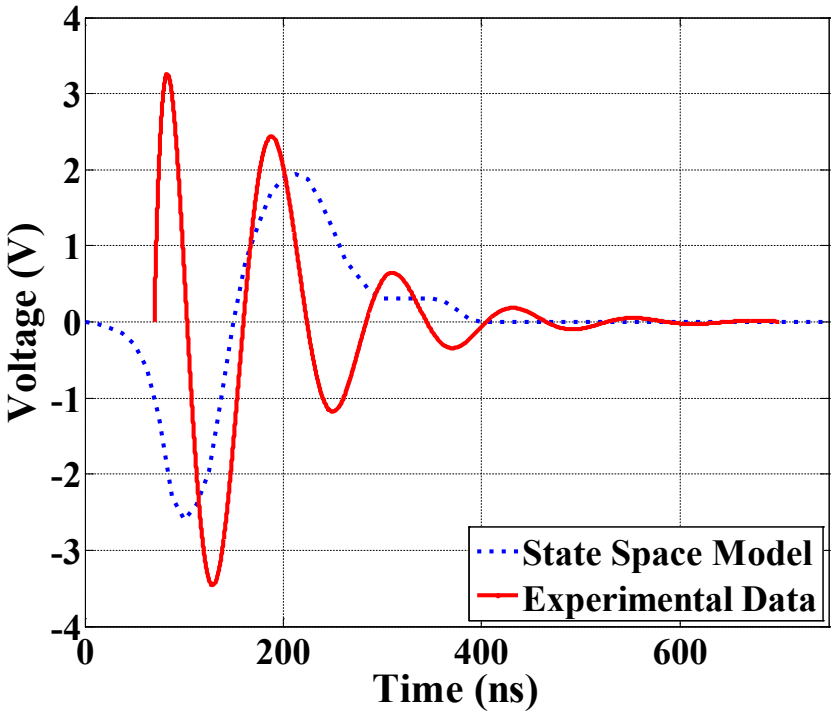


Figure 20. Step response for v_{gs2} compared with experimental v_{gs2}

Both waveforms oscillate above and below zero for 300 nanoseconds before settling at zero after 500 nanoseconds. One discrepancy between the analytical model result and the experimental result is in the initial condition. In the analytical result, the voltage initially climbs, while in the experimental result, the voltage initially drops below zero. This difference can most likely be attributed to the modeling of V_{DC} as a unit step function. In reality, V_{DC} is always on and just prior to Q_1 turning on, Q_2 is entirely decoupled from the circuit. Therefore in practice, the voltages and currents across the parasitic components in Q_2 have reached their steady-state values. However in the model, treating V_{DC} as a unit step function makes the system even more dynamic thus leading to the observed discrepancy. Additionally, it is evident that the analytical v_{gs2} exhibits more oscillations than the experimental result.

Thus, it is clear from the model presented here that the switching losses of Q_1 depend not only on its own parasitic components, but also on the parasitic components of Q_2. Therefore, any model of Q_1 during turn-on should also contain a circuit model for Q_2 during the proper intervals. Furthermore, the induced v_{gs2} during false turn-on is highly dependent on the rapid turn-on of Q_1. That is, the faster that Q_1 turns on, the higher the *dv/dt* will be at the drain terminal of Q_2 thus leading to a higher current through C_{gd2}. Subsequently, the magnitude of the induced v_{gs2} will be larger. In order to optimize the various components of Q_1 and Q_2 to ensure more efficient converter operation, an analytical model such as the one presented above can be used. In the next section, experimental data is presented to further illustrate the effects of the complex interactions between the two devices.

2.3.4 State Space Model of Synchronous Buck Converter: Stages of False Turn-on

In the previous section, analytical models for v_{gs1}, v_{gs2}, and v_{ds2} were presented, based on derivations made using frequency domain analysis of the equivalent circuit of synchronous buck converter. While reasonable agreement was obtained between the derived analytical model and the experimental results obtained from the experimental testbed, some discrepancy was apparent between the two. In particular, the analytical waveform of v_{gs2}, which demonstrates the induction of false turn-on, quite notably experiences an initial rise, as opposed to the experimental which experiences an initial fall. One explanation for such discrepancy is that in the frequency domain model, initial conditions were not considered. Quite notably, the capacitors voltages at the moment of the event are non-zero, but are not included in the frequency domain model.

In order to develop a more accurate model, a state space model of the same synchronous buck converter system that was described in the previous section was derived. The state-space model facilitates the definition of the circuit's initial conditions, which are constantly varying throughout the dynamic switching process. To obtain analytical waveforms for v_{gs1}, v_{ds2}, and $v_{gs2,}$ state variables were assigned for inductor currents and capacitor voltages. As seen in Figure 21, symbols across inductors indicate current state variables, while symbols across capacitors denote voltage state variables. The definition of all state-variables is summarized in Table II. Parasitic capacitance values were extracted from the datasheets of the MOSFETs, while package inductances were estimated using $V=Ldi/dt$.

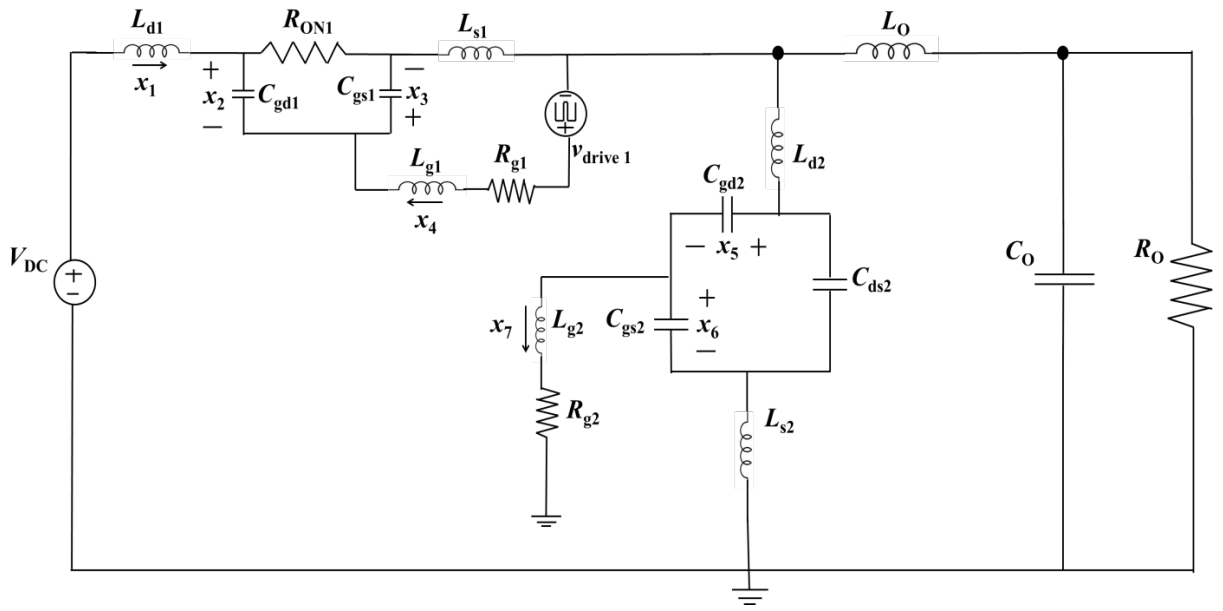


Figure 21. Definition of state variables in equivalent circuit of synchronous buck converter

Table 5. State variable assignments from Figure 21

Parameter	Element	State Variable
i_L	L_{d1}	x_1
v_L	C_{gd1}	x_2
v_C	C_{gs1}	x_3
i_L	L_{g1}	x_4
v_C	C_{gd2}	x_5
v_C	C_{gs2}	x_6
i_L	L_{g2}	x_7

From analysis of Figure 21 and the state variable assignments, the equations seen in (5)-(11) was derived in order to generate a model from which the desired voltage waveforms could be extracted.

$$\left(L_{d1}+L_{s1}+L_{d2}\right)\dot{x}_1 - R_{ON1}C_{gd1}\dot{x}_2 + L_{s1}\dot{x}_4 + L_{g2}\dot{x}_7 = -R_{ON1}x_1 - x_5 - R_{g2}x_7 + V_{DC} \tag{25}$$

$$R_{ON1}C_{gd1}\dot{x}_2 = R_{ON1}x_1 - x_2 - x_3 \tag{26}$$

$$L_{s1}\dot{x}_1 + \left(L_{g1} + L_{s1}\right)\dot{x}_4 = -x_3 - R_{g1}x_4 + V_{drive1} \tag{27}$$

$$-L_{s2}\dot{x}_1 + \left(L_{g2} + L_{s2}\right)\dot{x}_7 = x_6 - R_{g2}x_7 \tag{28}$$

$$C_{gd1}\dot{x}_2 - C_{gs1}\dot{x}_3 = -x_4 \tag{29}$$

$$\left(C_{gd2} + C_{ds2}\right)\dot{x}_5 + C_{ds2}\dot{x}_6 = x_1 \tag{30}$$

$$C_{gd2}\dot{x}_5 - C_{gs2}\dot{x}_6 = x_7\,. \tag{31}$$

The expressions seen in (25)-(31) can be transformed into matrix form and solved with linear algebra as seen in (32),

$$E\left[\dot{x}\right] = F\left[x\right] + G\left[u\right]. \tag{32}$$

Using (25)-(31), the formulation of matrices [E], [F] and [G] from (32), are given in (33)-(36),

$$E = \begin{bmatrix} L_{d1} + L_{s1} + L_{d2} & -R_{ON1}C_{gd1} & 0 & L_{s1} & 0 & 0 & L_{g2} \\ 0 & R_{ON1}C_{gd1} & 0 & 0 & 0 & 0 & 0 \\ L_{s1} & 0 & 0 & L_{g1} + L_{s1} & 0 & 0 & 0 \\ -L_{s2} & 0 & 0 & 0 & 0 & 0 & L_{g2} + L_{s2} \\ 0 & C_{gd1} & -C_{gs1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{gd2} + C_{ds2} & C_{ds2} & 0 \\ 0 & 0 & 0 & 0 & C_{gd2} & -C_{gs2} & 0 \end{bmatrix} \tag{33}$$

$$F = \begin{bmatrix} -R_{ON1} & 0 & 0 & 0 & -1 & 0 & -R_{g2} \\ R_{ON1} & -1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & -R_{g1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & -R_{g2} \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{34}$$

$$G_{DC} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{35}$$

$$G_{drive1} = \begin{bmatrix} 0 \\ 0 \\ 1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}. \tag{36}$$

In (35) and (36), the variables $[G_{DC}]$ and $[G_{drive1}]$ represent matrices for the two enabled sources at the instance of false turn-on. The system of equations can then be solved using (37) and (38),

$$[\dot{x}] = E^{-1}F[x] + E^{-1}G[u] \tag{37}$$

$$[\dot{x}] = A[x] + B[u]. \tag{38}$$

By solving the state-space equations (17) and (18), the step response for v_{gs1}, $v_{ds2,}$ and v_{gs2}, seen in Figure 22, Figure 23, and Figure 24, respectively, are obtained.

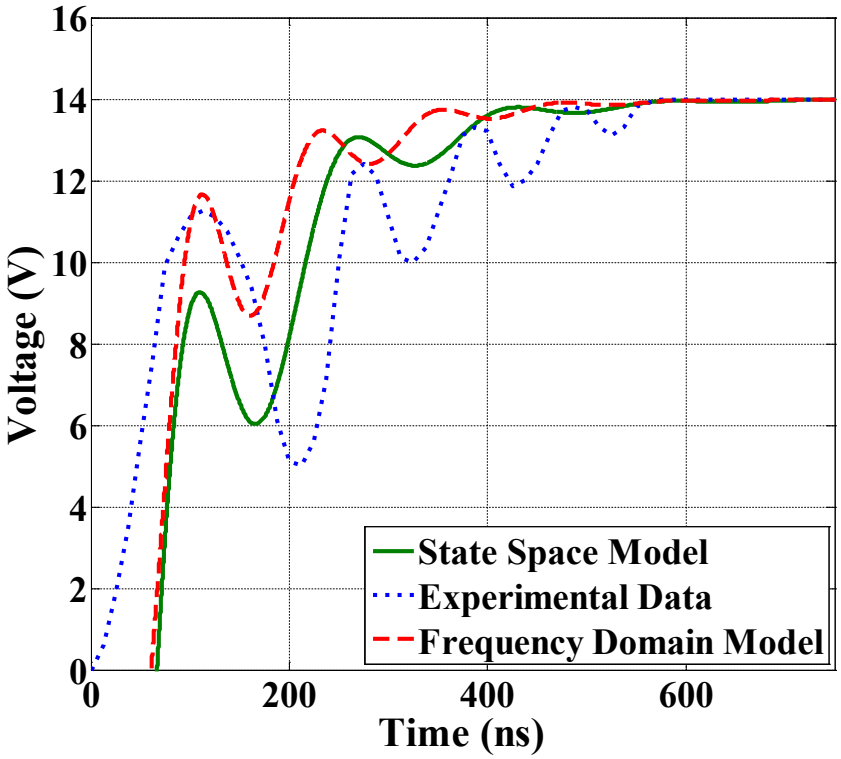


Figure 22. Turn-on response for v_{gs1}

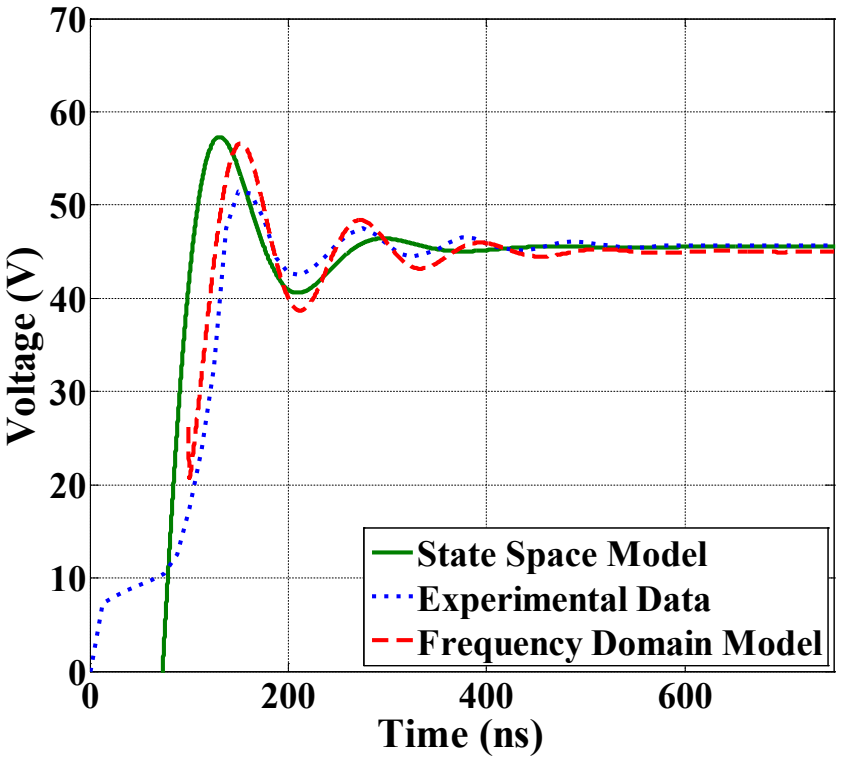


Figure 23. Turn-on response for v_{ds2}

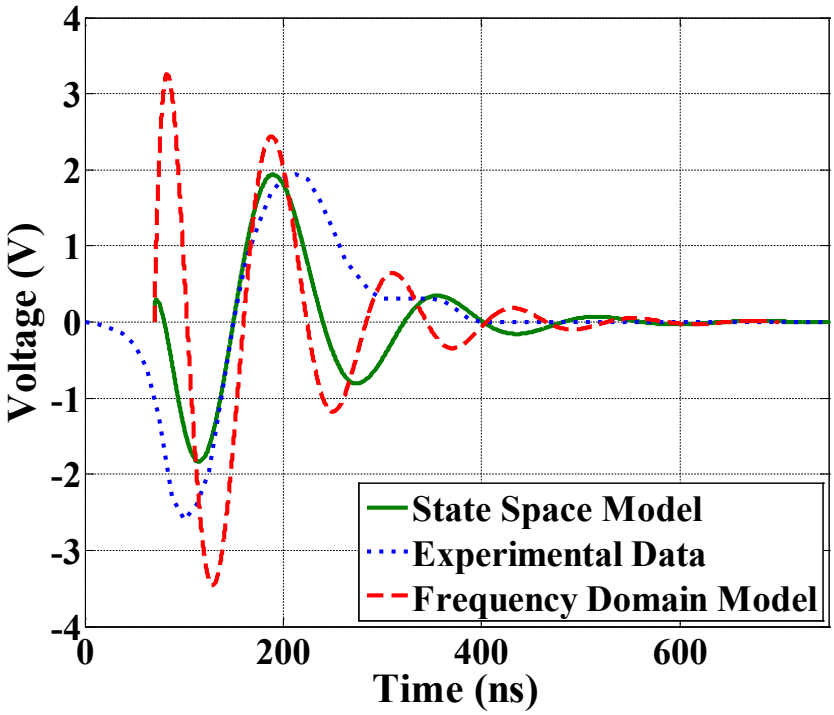


Figure 24. Turn-on response for v_{gs2}

From Figure 22, Figure 23, and Figure 24, it can be seen that the systems modeled in the state space match closely to both the experimental results and the frequency domain model that was previously derived. This shows that not only is the state space model valid, but further confirms that the equivalent circuit model presented in Figure 15 is a close approximation of the synchronous buck converter circuit at the moment of channel formation in Q_1. Additionally, it can be clearly seen that for v_{gs1}, v_{gs2}, and v_{ds2}, the state space model, including the initial voltage charges on the capacitors, improves the accuracy of the analytical simulation.

For v_{gs1}, the state space model shows minimal improvement over the frequency domain model. As seen in Figure 22, the step response is more damped, with lower overshoot. Additionally, the ringing frequency that occurs during turn on more closely matches that of the

experimental results. Note that both models reach the same steady state value of 14 V at approximately 550 ns, which matches well to the experimental system.

The response of v_{ds2} shows significant improvement over the frequency domain model. As seen in Figure 23, the model properly starts at 0 V, unlike in the frequency domain response. The magnitude of the two responses are similar, although the state space model reaches a steady state which exactly matches that of the experimental results, 45 V, unlike the frequency domain model, which is off by 1.25 V. Additionally, the settling time more closely matches that of the experimental results, at the same 550 ns mark as seen in v_{gs1}. However, neither the state space nor the frequency domain models accurately predict the non-linear portion of the experimental v_{ds2} waveform. This is due to the fact that the equivalent circuit representing the two devices in the synchronous buck converter is a snapshot of the system after the moment of channel formation in Q_1. The initial rise in v_{ds2} can be attributed to the non-linear formation of the channel, which is not taken into account by either analytical model. The state space model, however, closely fits the remainder of the waveform, and improves on the results from the state space model.

In the case of the turn-on response for v_{gs2}, which is the model predicting false turn on, the state space model shows the greatest amount of improvement over the frequency domain model. This is particularly important, as it can be accurately used to predict false turn-on in the synchronous buck converter, and can therefore be used to properly tune system capacitance values in order to optimize the amount of false turn-on that occurs. In analyzing the waveforms presented in Figure 24, significant improvement can be seen, as the state space model very closely approximates the experimental results, including the demonstration of occurrence of false turn-on. Most importantly, the state space model avoids the large initial positive peak seen in the frequency domain model, avoiding the inaccurate prediction of two instances of false turn-on in one

switching cycle. This is crucial for prediction of converter performance, as the extra occurrence of false turn-on seen in the frequency domain model will inaccurately predict system efficiencies and incorrect operations. The state space model additionally has a frequency of oscillation that much more closely matches the experimental results, including the prediction of a non-linear peak experienced close to 350 ns. The experimental system in this case is not linear during the discharge of gate voltage, which is not perfectly modeled. However, the state space model provides a much closer approximation the non-linear behavior than the frequency domain model did.

As a whole, it can be see that the state space derivation of the system dynamics experienced by the equivalent circuit model represents a much more accurate model of the system than the previous frequency domain derivation. It has been shown that the analytical model can be used to closely predict the response of the experimental system during turn-on of Q_1, including the prediction of the phenomenon of false turn-on experienced by Q_2. This can be used to predict system losses, efficiency, and operation. This can, as previously described, be used to tune the parasitic capacitances of the devices used in the circuit, in order to optimize system losses. Specifically, the trade-off between low switching losses from WBG semiconductors at high switching frequencies can be balanced against the losses created from the false turn-on resulting from their low intrinsic capacitance values. The next section will demonstrate experimental results detailing such system tuning, with analytical results to be presented as future work.

2.3.5 State Space Model of Synchronous Buck Converter: Stages of False Turn-on

A. Synchronous Buck Converter Sensitivity Analysis

To further investigate the interactions between Q_1 and Q_2 in the synchronous buck converter and to validate the conclusions from the previous section, the effects that false turn-on has on the oscillations in the various signals of the converter were experimentally measured. This required externally varying the circuit parameters that have the most influence on the false turn-on of Q_2. To determine which circuit parameters to tune and in which direction they should be tuned in order to induce less (or more) false turn-on, one can analyze the frequency response function for the first order circuit model of Q_2 seen in Figure 13:

$$\frac{v_{gs2}(j\omega)}{v_{ds2}(j\omega)} = \frac{j\omega R_{g2} C_{gd2}}{1 + j\omega R_{g2}(C_{gd2} + C_{gs2})}. \tag{39}$$

To reduce the possibility of false turn-on, the magnitude of the left hand side of (39) should be small so that v_{gs2} does not exceed the threshold voltage, or conversely large if false-turn on is desired. In analyzing (17), it can be inferred that low values of R_{g2} and C_{gd2} can decrease the possibility of false turn-on. It can also be seen that high values of C_{gs2} will decrease the possibility of false turn-on at sufficiently high rise-time frequencies.

Table 6. Nominal converter values for R_{g2}, C_{gd2}, and C_{gs2}

Parameter	Value
R_{g2}	5 Ω
C_{gd2}	0.25 nF
C_{gs2}	10.75 nF

Shown in Table 6 are the nominal values of R_{g2}, C_{gd2}, and C_{gs2} that led to the results shown in Figure 13. The values for the capacitances are taken from the Powerex datasheet of the SiC MOSFET [27].

Figure 25 illustrates the experimental waveforms obtained for v_{gs1}, v_{ds2}, and v_{gs2} after the value of R_{g2} was increased to 45 Ω. As seen in Figure 25, the magnitude of the induced v_{gs2} is now 5 V, twice the amount seen in the nominal condition of Figure 13. However, the oscillations in all three signals are significantly less after R_{g2} was increased. It is particularly intriguing to note that R_{g2} can have an effect on the oscillations in v_{gs1}, since R_{g2} is far away from v_{gs1} in the circuit. In addition, the change in oscillatory behavior observed in v_{ds2} will also occur in v_{ds1}. Thus the ability of R_{g2} to noticeably affect the behavior of v_{gs1} and v_{ds1} implies that R_{g2} will have an influence on the switching losses in Q_1. Although a larger R_{g2} lowered the oscillations in the converter, the effect of increasing R_{g2} (and inducing more false turn-on) can also be detrimental to converter operation in many ways. First, as seen in Figure 25, by increasing R_{g2} to 45 Ω, the induced v_{gs2} reaches an undesirably high value which would lead to significant switching losses in Q_2. Furthermore, if the induced current through Q_2 is significantly large, the switching losses in Q_1 can be severely impacted since Q_1 and Q_2 share the same current during false turn-on. Ideally, an optimal R_{g2} can be found which would reduce oscillations in all three signals while not allowing the switching losses in both Q_1 and Q_2 to become undesirably high. In our future work, the analytical model presented in Section III will be utilized to perform this optimization. It is further instructive to note that in this model/experiment, Q_2 is a 1200V device and therefore at the applied voltage of 50V the reduction in signal oscillation induced by false turn-on will have minimal beneficial effects. However, the observations presented here demonstrate that by inducing a certain

amount of false turn-on to a transistor rated at a significantly smaller voltage, the resulting reduction in signal oscillation could be more advantageous.

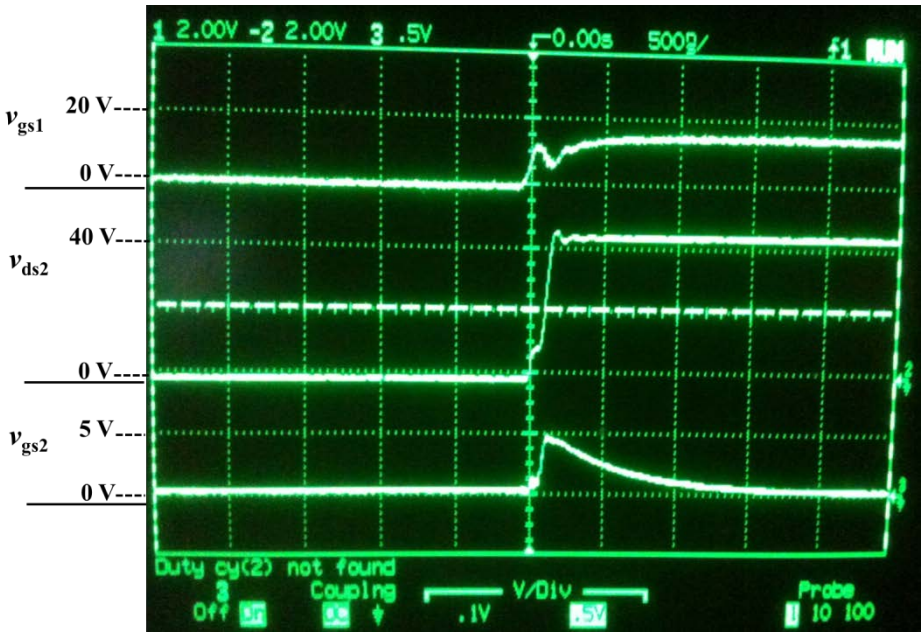


Figure 25. Experimental waveforms after R_{g2} is raised to 45 Ω. 10:1 testing probes were used for measurement, while the scope measurement is set to 1:1.

Shown in Figure 26 are the experimental results obtained for the three signals after C_{gd2} is increased to a total of 1.25 nF. This was done simply by connecting a 1 nF capacitor across the internal C_{gd2} of Q_2. In this analysis, the value of R_{g2} was reduced to its nominal value of 5 Ω. As seen in Figure 26**,** the magnitude of the induced v_{gs2} is 3.75 V, or 50% higher than in the nominal condition. Also, the oscillations in all three signals have been reduced compared to the nominal condition. As a result, C_{gd2} can have an effect on the switching losses in Q_1 as well. Again, the effect of increasing C_{gd2} and inducing more false turn-on may also lead to more switching losses in Q_1, particularly if the shared current between Q_1 and Q_2 is large enough.

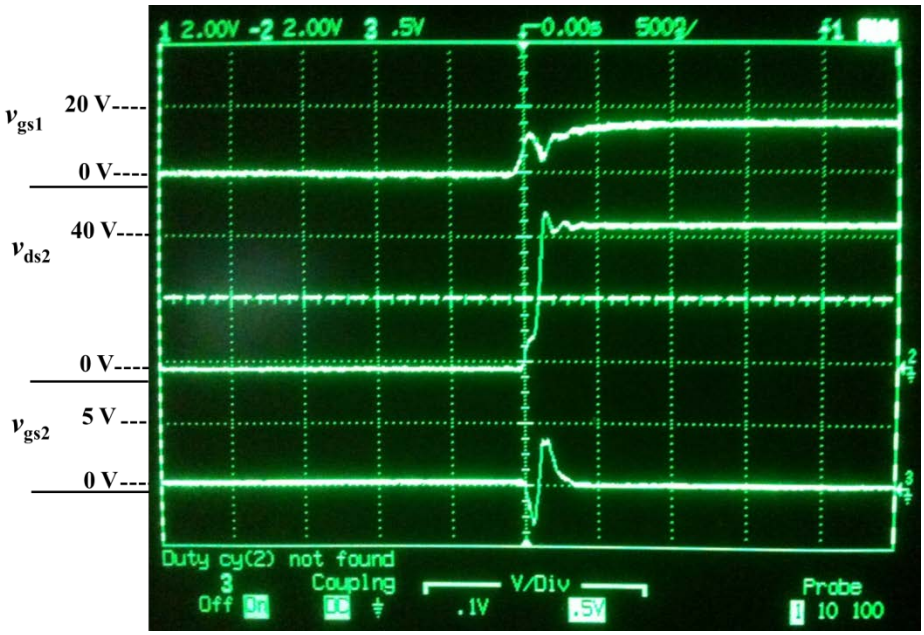


Figure 26. Experimental waveforms after C_{gd2} is raised to 1.25 nF. 10:1 testing probes were used for measurement, while the scope measurement is set to 1:1.

Figure 27 depicts the experimental results obtained after a 10 nF capacitor was connected across C_{gs2} to obtain a total gate-source capacitance of 20.75 nF. The other circuit parameters were reduced to their nominal values. As seen in Figure 27**,** the magnitude of the induced v_{gs2} is now 1.25 V, half the voltage seen in the nominal condition. However, the oscillations in only v_{gs2} are slightly greater than in the nominal condition. The oscillations in v_{gs1} and v_{ds2} remain relatively unchanged. In the synchronous buck converter, C_{gs2} is an essential parameter to optimize. This is because larger values of C_{gs2} will increase switching losses during intended turn-on, but will reduce the magnitude of the induced gate-source voltage during false turn-on as shown here. As such the state space analytical model presented in the previous section can be utilized to perform this crucial optimization.

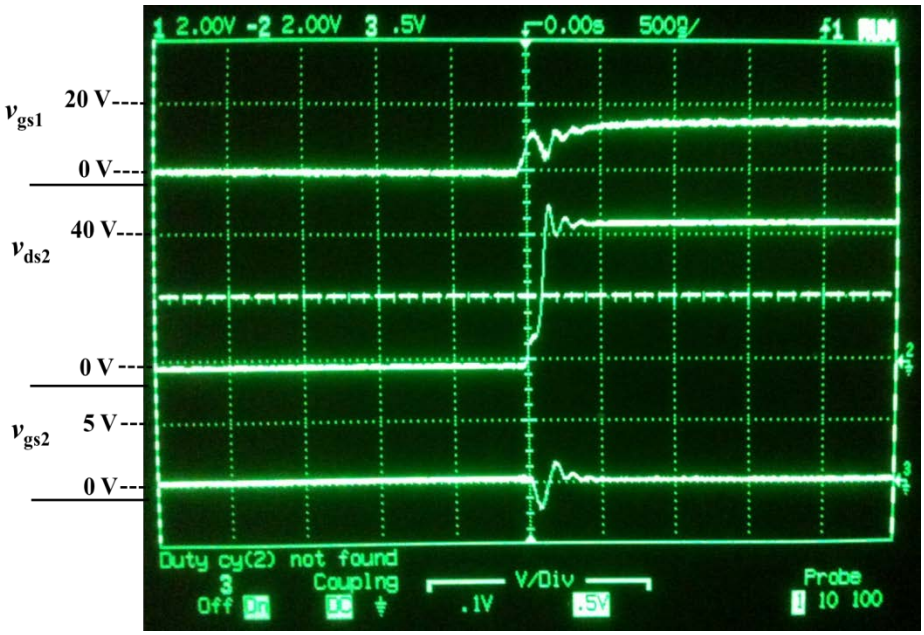


Figure 27. Experimental waveforms after C_{gs2} is raised to 20.75 nF. 10:1 testing probes were used for measurement, while the scope measurement is set to 1:1.

The data in this section is in agreement with the results presented in Section 2.2 and [11]. Values of C_{gd2} will increase the damping ratio of v_{ds2} while also reducing the natural frequency of v_{ds2}. As a result, larger values of C_{gd2} will decrease the oscillations in v_{ds2}, as shown in this paper. Furthermore in Section 2.2, larger values of C_{gd2} were shown to reduce the magnitude of the induced v_{gs2}, as shown here. Finally, the data in Section 2.2, showed that larger values of C_{gs2} will have minimal effect on the oscillations of v_{ds2} while also reducing the magnitude of the induced v_{gs2} which is again consistent with the data demonstrated in this report.

Thus, the experimental data here confirms that the internal and external circuit parameters of Q_2 will affect the behavior of Q_1 during turn-on. Therefore, any model of Q_1 should contain the components of Q_2 during the proper intervals. As shown here, raising both R_{g2} and C_{gd2} will decrease the oscillations in the various signals of the converter but increase the magnitude of the induced v_{gs2}. Conversely, raising C_{gs2} will decrease the magnitude of the induced v_{gs2} but with

minimal effect on the voltage-oscillations of the converter. These observations point to the necessity of design optimization for next generation synchronous buck converters. Design optimization is made possible through the analytical model presented in Section 2.3.

It should be noted that in many power conversion circuits, two transistors are intentionally conducting simultaneously and it is therefore intuitive that the parasitic elements of one transistor may affect the behavior and oscillations in the signals of the other transistor. However, in the synchronous buck converter, Q_1 and Q_2 never intentionally conduct at the same time. It is thus logical to assume that when Q_2 turns on spuriously, the simultaneous cross conduction between Q_1 and Q_2 will lead to different signal oscillations and circuit behaviors than if Q_2 had not turned on falsely. The work presented here demonstrates this phenomenon both analytically and experimentally.

2.4 CONCLUSION

The occurrence of false turn-on in the synchronous buck converter was investigated, and the interaction between the two MOSFET devices was explored. This phenomenon was first demonstrated in a high *dv/dt* test circuit, with a frequency domain model showing close matching to the experimental demonstration of false turn-on. Next the full synchronous buck converter was investigated. It was shown that the interaction between the devices is non-trivial and cannot be predicted directly from the device characteristics. Rather, an analytical model was developed based first on frequency domain analysis, the on state space analysis of the circuit during the moments after application of voltage to the gate of Q_1. It was shown that an equivalent circuit can be created for the converter at the time of the formation of the channel in Q_1, allowing for analysis of the

system without relying on complex physics models for the semiconductor devices. This model was shown to closely approximate the experimental response of the circuit during the turn-on of Q_1, taking into account the impact of the parasitic components of Q_2. As a result, it was concluded both analytically and experimentally that Q_2 should not be excluded from circuit models of Q_1 during turn-on. Furthermore, the voltages v_{gs1}, v_{ds2}, and v_{gs2} from the analytical model matched the experimental waveforms and clearly demonstrated the ability of the model to predict false turn-on in Q_2. This matching was shown to be improved from the frequency domain model by instead using the state space model, allowing for the inclusion of the initial charge on the intrinsic capacitances. The state space model provided better accuracy in matching the experimental results. Those experimental results were then expanded to show the effect of variance in device intrinsic capacitance values on the turn-on transients of the synchronous buck converter. The ability to accurately model the false turn-on phenomenon will enable system designers to determine the optimal sizes of parasitic components of Q_2. This will allow for development of converters with parasitic components which have been optimized for their specific semiconductor devices, striking a balance between minimizing losses from false turn-on and retaining enough capacitance to lower the oscillations in the various signals of the converter. This model is intended to offer a better understanding of those interactions while also providing a path towards better design procedures for new generations of devices.

3.0 RIPPLE CORRELATION CONTROL FOR MAXIMUM POWER POINT TRACKING IN A PV CONNECTED BOOST CONVERTER

As penetration of photovoltaic systems to the grid increases, especially at the distributed generation level, their performance, in terms of both power output and efficiency, becomes increasingly important. To improve the power output from photovoltaic systems, maximum power point tracking (MPPT) algorithms are employed, typically implemented using a DC-DC boost converter as the tracking device [29], or a buck converter as described in Chapter 2.0 . The previous chapter explored transient interactions in the synchronous buck converter system, focusing on the use of WBG semiconductors and their effect on system performance. This chapter will instead focus on the development of MPPT in a boost converter, and will examine how the power generated by PV panels can most efficiently be forced to perform near its theoretical limit. To do so, this chapter will first present a MPPT algorithm based on Ripple Correlation Control (RCC). This will be presented first through a mathematical description of the RCC control process, then through analysis of a PSCAD simulation model of the boost converter system with RCC implemented via frequency control. First, however, it is important to understand other MPPT methods, such that a baseline can be developed to which RCC can be properly compared.

The objective of MPPT is to force a system of PV panels to operate at its maximum power point (MPP). This is done by manipulating the apparent impedance seen by the PV system such that the operating point of the system is forced to the maximum point of the non-linear IV curve of the PV panels, which can be seen in Figure 28. Of note is the fact that as the solar insolation (S), or the ambient temperature (T) change, the entire curve will be shifted up or down.

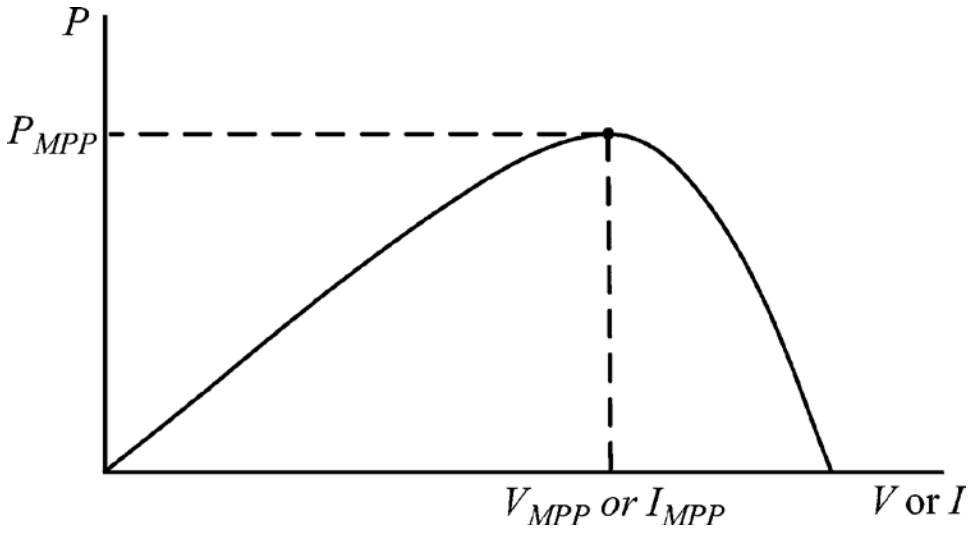


Figure 28. Power versus voltage or current for PV panels

This means that even if the system is operating at the MPP at one environmental point, a change in either condition will move the system away from the MPP. It is this situation that MPPT algorithms are designed to remedy. The natural though would be to examine *S* and *T* and to use the difference between the current values and their references to control the duty cycle of the converter. However, monitoring *S* and *T* require complex circuitry and sensor systems, and are vulnerable to degradation in solar panels over time. It is therefore preferable to force the system to reach the MPP through direct observation of the current and voltage experienced in the system, as almost all of the MPPT algorithms presented in the literature have been.

A vast variety of MPPT algorithms have been developed, the most common of which are perturb and observe [30] and incremental conductance [31] both of which are employed throughout the industry. The perturb and observe strategy relies on an external electronic system to create small steps in the array voltage on a fixed duty cycle. The change in power output resulting from the array is then measured, positive change implying convergence towards the MPP, negative change implying divergence. While this control strategy is simple to implement, it has distinct

disadvantages, namely that the constant perturbations result in steady state error, as well as an inability to rapidly converge to the MPP due to fixed step sizes. The incremental conductance method relies instead on measuring the instantaneous change in power relative to voltage and determining the relative position to the MPP, as described in [32].

$$\begin{cases} dP/dV = 0, & \text{at the MPP} \\ dP/dV > 0, & \text{left of the MPP} \\ dP/dV < 0, & \text{right of the MPP} \end{cases} \tag{40}$$

However, in practice $\Delta P/\Delta V$ must be employed in order to avoid constant fluctuation about the MPP due to converter ripple. Because of this there is an inherent tradeoff to be made between the use of a step size large enough to allow for rapid convergence to the MPP, yet small enough to avoid steady state error and fluctuation. Additionally, incremental conductance typically shows longer response times due to complex hardware and software requirements [31]. More complex algorithms, such as Fuzzy logic and neural network-based algorithms have also been developed. These generally demonstrate rapid convergence and good performance under varying solar insolation and ambient temperature, but tend to be much more complicated to implement in hardware [32].

As opposed to many of the algorithms demonstrated previously, RCC directly calculates the duty cycle required to force the system to the MPP via monitoring of the inherent switching ripple induced by the boost converter. These ripples on v_{PV} and i_{PV} are naturally present in the boost converter connected PV system, and RCC takes advantage of this in order to replace the intentionally added Δv_{PV} and Δi_{PV} perturbations in algorithms such as perturb and observe. In doing so, two advantages are clear: First that the steady state operation of the system does not have the added ripple experienced by other MPPT implementations, and second that the system will rapidly converge, without the "hill-climbing" experienced during transient changes in *S* and *T*.

This is achieved through the observation that the product of the time-based derivatives of v_{PV} and i_{PV} will be greater than zero to the left of the MPP, less than zero to the right of the MPP, and exactly zero at the MPP as referenced in Figure 28. This results in the set of equation seen in (41), (42), and (43) [33]:

$$\frac{dp_{\mathrm{PV}}}{dt} \cdot \frac{dv_{\mathrm{PV}}}{dt} > 0, \quad V_{\mathrm{PV}} < V_{\mathrm{MPP}} \tag{41}$$

$$\frac{dp_{\mathrm{PV}}}{dt} \cdot \frac{dv_{\mathrm{PV}}}{dt} < 0, \quad V_{\mathrm{PV}} > V_{\mathrm{MPP}} \tag{42}$$

$$\frac{dp_{\mathrm{PV}}}{dt} \cdot \frac{dv_{\mathrm{PV}}}{dt} = 0, \quad V_{\mathrm{PV}} = V_{\mathrm{MPP}} \tag{43}$$

From this set of equations, the control law derived in [34] is extracted, as shown in (44), where *k* is a constant of negative gain, used to properly tune the system:

$$\frac{dd(t)}{dt} = k \frac{dp_{\mathrm{PV}}}{dt} \cdot \frac{dv_{\mathrm{PV}}}{dt} \tag{44}$$

Or alternatively:

$$d(t) = k \int \frac{dp_{\mathrm{PV}}}{dt} \cdot \frac{dv_{\mathrm{PV}}}{dt} dt \tag{45}$$

However, p_{PV} cannot be directly measured. Instead the v_{PV} and i_{PV} must be measured instead, resulting in a more complex time-based implementation of the system:

$$d(t) = k \int \frac{d(v_{\mathrm{PV}} i_{\mathrm{PV}})}{dt} \cdot \frac{dv_{\mathrm{PV}}}{dt} dt = k \int \left(i_{\mathrm{PV}} \frac{dv_{\mathrm{PV}}}{dt} + v_{\mathrm{PV}} \frac{di_{\mathrm{PV}}}{dt} \right) \cdot \frac{dv_{\mathrm{PV}}}{dt} dt \tag{46}$$

The goal of this control system is therefore to drive $dd(t)/dt$ to 0, and $d(t)$ to $d_{\mathrm{MPP}}(t)$. Previous works, such as [33] and [34], have shown that RCC can mathematically yield the optimal value of the duty cycle in order to force the system to operate at the MPP. In these citations, analog control

systems have been implemented, using operational amplifiers to perform the calculations necessary to evaluate (45) in real time. Analog control systems, however, are not necessarily the optimal way to implement such systems, as at high frequency, the desired v_{PV} and i_{PV} waveforms can experience phase shift due to both the inherent capacitance of the PV panel, as well as any input capacitor that may be included in the converter system [7].

In this chapter, a PV system is implemented, relying on a boost converter being controlled by a frequency domain implementation of the RCC control law described in (44). First, a model of a PV panel is described and implemented in PSCAD, based on previous work described in [35] and [36]. Next, a DC-DC boost converter will be designed and described. The combination of these two models will be used to represent the system shown in Figure 29.

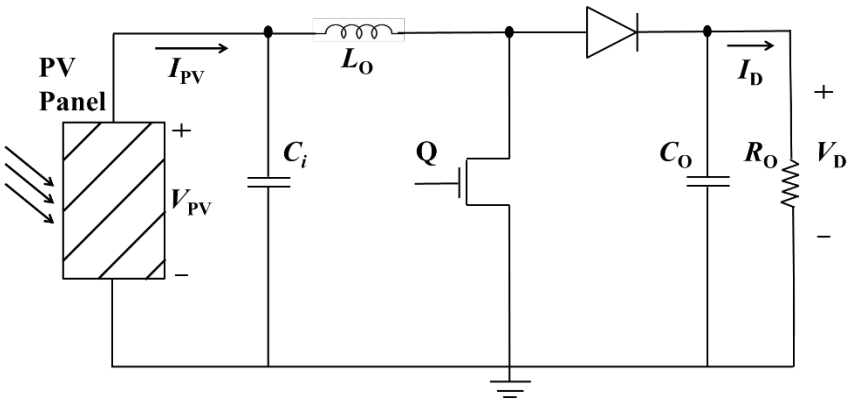


Figure 29. PV connected DC-DC boost converter system for MPPT

Finally, a frequency domain RCC system will be implemented to control the duty cycle of the designed converter, and the system's ability to accurately track the MPP will be demonstrated.

3.1 PHTOVOLTAIC PANEL AND SYSTEM MODELING

The objective of this portion of the system was to model the PV panel themselves, as the dynamics experienced by the panel have a large impact on the performance of the RCC algorithm and the effectiveness of the MPPT system as a whole. In order to implement this system in the PSCAD environment, a piecewise linear model was used in order to create a simple implementation. The current produced by a PV panel can be described via non-linear effects as described by [35]:

$$i_{\mathrm{PV}} = i_{\mathrm{SC}} - i_{\mathrm{o1}}\left(e^{\frac{q(v_{\mathrm{PV}}+i_{\mathrm{PV}}R_{\mathrm{S}})}{kT}} - 1\right) - \frac{v_{\mathrm{PV}} + i_{\mathrm{PV}}R_{\mathrm{S}}}{R_{\mathrm{S}}} \tag{47}$$

where i_{SC} is the generated current at the current solar and thermal conditions of the panel, q is the charge of an electron, k is the Boltzman constant, T is the temperature of the cell, and R_{S} is the series resistance of the panel. The non-linearity of (47) is a result of the fact that the current and voltage produced based on systemic changes is recursive, based on the existing v_{PV} and i_{PV} of the system. Recursive systems are computationally bulky for implementation in PSCAD and can create lengthy simulation times. Because of this, a piecewise-linear model based on [35] and [36] was implemented. This piecewise linear model is described in [35] and can be seen in Figure 30.

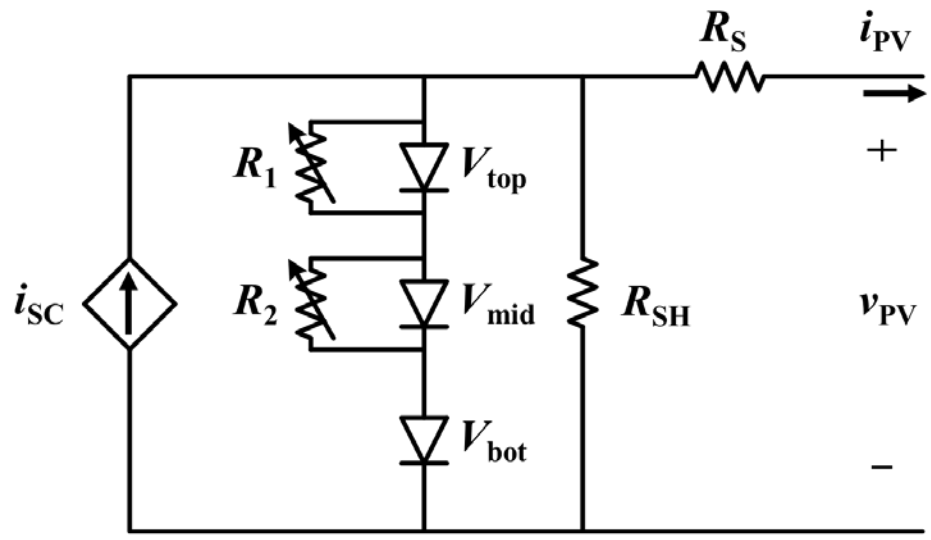


Figure 30. Piecewise linear PV module model based on diode turn-on **[35]**

The model operates by turning on the various diodes in the parallel branch based on the voltage experienced by the circuit, creating a piecewise linear model based on the resistances of R_1 and R_2 and the turn-on voltages of the diodes. As the voltage thresholds of the various diodes are turned on, the model will move to a new slope, creating an approximation of the non-linear PV current-voltage curve.

Table 7. CanadianSolar CS6P-240P panel characteristics [37]

Parameter	Value
P_{max}	240 W
V_{mpp}	29.9 V
I_{mpp}	8.03 A
V_{oc}	37 V
I_{sc}	8.59 A

The sizing of the resistances and voltages used in the system are described in [35], and for this model were based on the panel parameters for a CanadianSolar CS6P-240P panel for which the

characteristic parameters are given in Table 7, and the characteristic I-V curves are shown in Figure 31 [37].

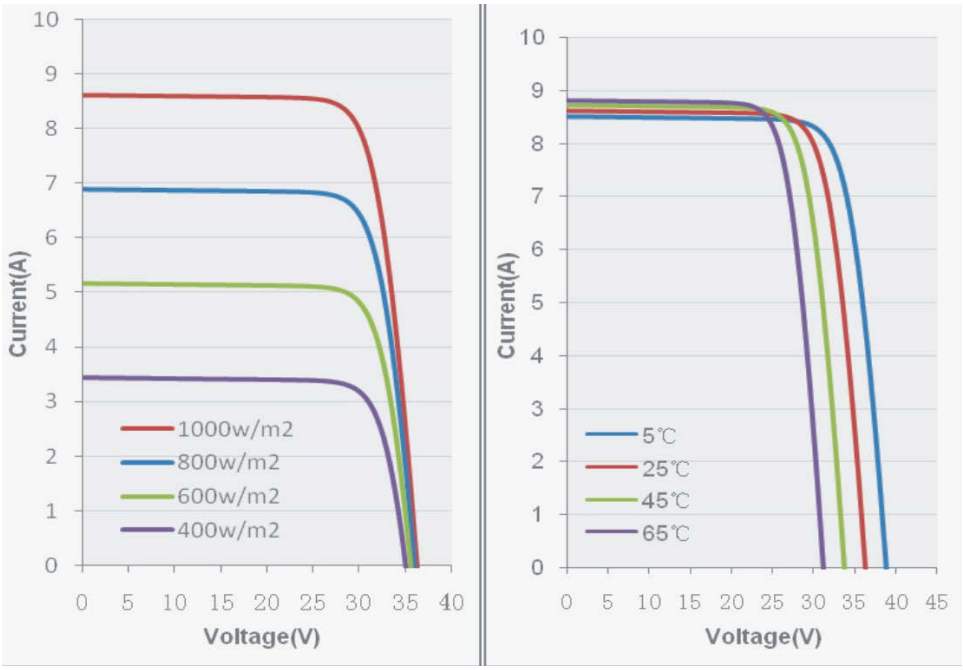


Figure 31. CanadianSolar CS6P-240P panel I-V curves [37]

The piecewise linear model results in an I-V curve that closely matches the current and voltage of the actual panel, and that allows for rapid simulation of the DC-DC boost converter and demonstration of the RCC MPPT algorithm. It was implemented and tested in PSCAD, the simulation circuit for which can be seen in Figure 32 [36].

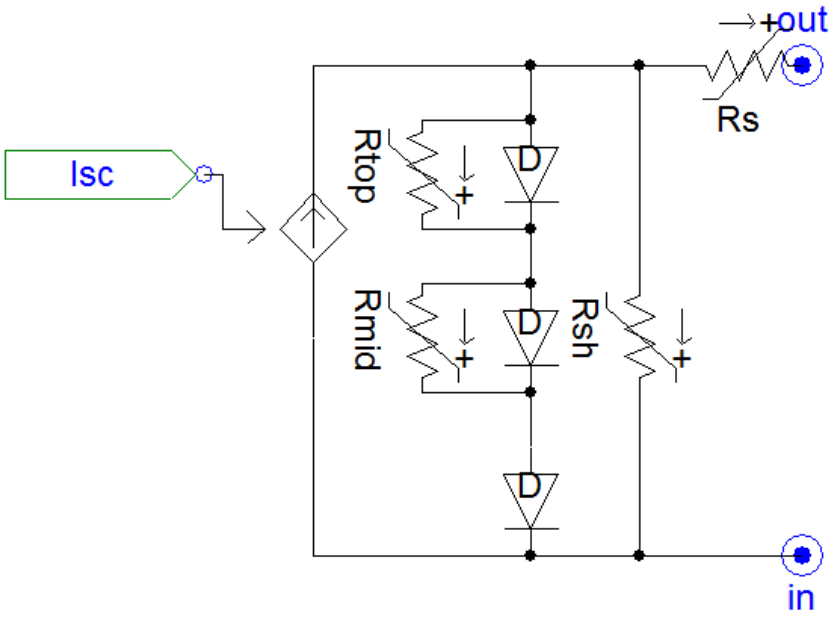


Figure 32. PSCAD implementation of CanadianSolar CS6P-240P [36]

Through evaluating the equations presented in [35], the size of the resistors and voltage used in this circuit were determined as given in Table 8.

Table 8. Calculated parameters for piecewise linear model for CanadianSolar CS6P-240P

Parameter	Value
R_{SH}	616.67 Ω
R_S	0.7245 Ω
R_{TOP}	0.4080 Ω
R_{MID}	21.101 Ω
V_{BOT}	24.701 V
V_{MID}	10.807 V
V_{TOP}	1.4923 V

By implementing the piecewise linear model as described above, the V-I curve shown in Figure 33 was produced. It can be seen that this model shows excellent agreement with the curve shown in Figure 31 from the manufacturer's datasheet.

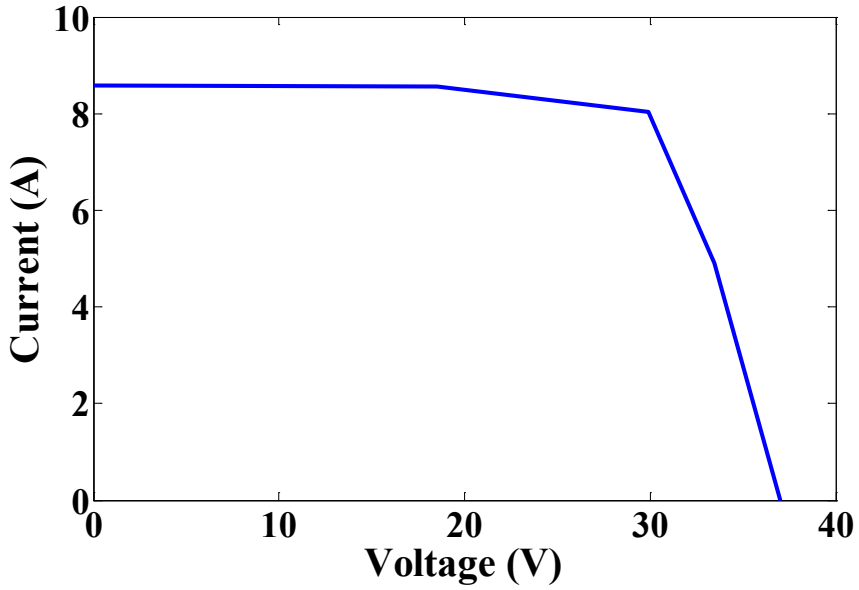


Figure 33. V-I curve for CanadianSolar CS6P-240P generated by the piecewise linear model

In implementing the piecewise linear model of the CanadianSolar CS6P-240P, it can be seen that the model closely approximates the known performance characteristics in a simple circuit-based system. In order to model the physical system being considered, 9 panels were connected in series. This yields a string of panels producing a V_{MPP} of 269.1 V and an I_{MPP} of 8.03 A, for a maximum power of 2161 W at standard temperatures and conditions (STC: S = 1000 W/m^2 and T = 25° C). In further sections, this panel system model will be used to evaluate the DC-DC boost converter and its RCC MPPT driving algorithm.

3.2 BOOST CONVERTER MODEL WITH RCC MPPT ALGORITHM

3.2.1 Simulation Model Development

In order to properly integrate the PV model described in Section 3.1, a boost converter was designed, designed to handle up to 2.5 kW of power transfer over a sustained period of time. The function of the boost converter is such a situation is to add an additional control variable, namely the duty cycle, in order to change the amount of impedance seen by the panel. This allows, the panel voltage to be manipulated in such a way that the panel can be forced to perform at the MPP. Namely, the output resistor R_o has a fixed impedance. However, the amount of current drawn through that impedance is directly dependent on the output voltage, which depends on the duty cycle. Therefore, by manipulating the duty cycle, the apparent size of R_o, as seen by the PV panel, can be varied in order to force the panel to operate at the desired point. In doing so, the boost converter allows the PV system as a whole to adjust to changes, whether fast or slow, in either *S* or *T*, as experience by the PV panels.

In order to simulate the system presented in Figure 29 a simulation of model of the boost converter was required. The EMPT simulation environment used was PSCAD.

Table 9. Characteristic parameter values for the boost converter

Parameter	Value
C_i	2 mF
L_o	200 µH
C_o	200 µF
R_o	100 Ω

The design was based on operating point at the MPP at STC, resulting in the characteristic system components described in Table 8. The resulting complete boost system can be seen in Figure 34.

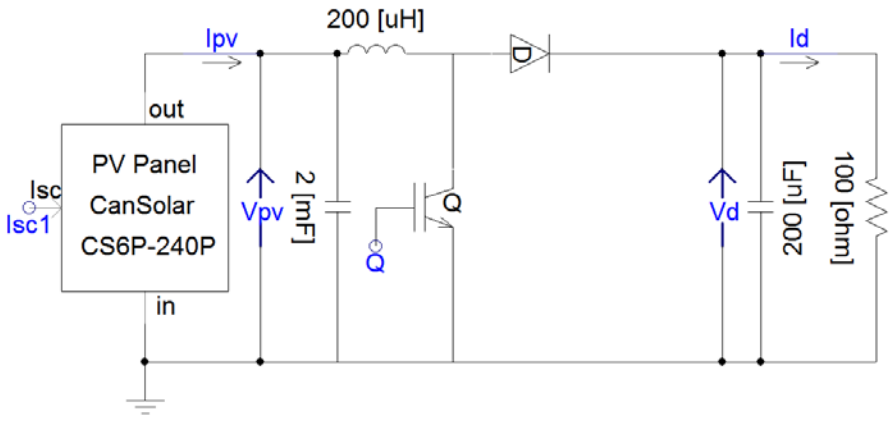


Figure 34. Simulated PV panel and boost converter system

With the converter system modeled, it was then necessary to control the duty cycle of the MOSFET Q, such that the MPP is reached via the desired control strategy. To do so, the RCC MPPT algorithm described in Section 3.0 was implemented in the frequency domain. As seen in (46), the control laws governing RCC become complicated when time-based solutions are relied upon. Because of this, it was determined that implementation in the frequency domain would allow for a much simpler control structure. If converted directly to the frequency domain, (46) becomes:

$$d(s) = k \cdot \frac{1}{s}\left((i_{\mathrm{PV}} s v_{\mathrm{PV}} + v_{\mathrm{PV}} s i_{\mathrm{PV}}) s v_{\mathrm{PV}}\right) = k \cdot \frac{1}{s}(2 s^2 v_{\mathrm{PV}}^2 i_{\mathrm{PV}}) \tag{47}$$

However, (47) involved a double derivative in its implementation, which is not desirable from a control standpoint, particularly because of the added complexity of physical implementation. Particularly, derivatives can lead to instability in system dynamics, and while that is not the case with the boost converter topology, the added instability is still undesired. Because of this, the equation in (47) can be left instead in its form from (46). That is, allowing the multiplication in the system to occur before differentiation, resulting in:

$$d(s) = k \cdot \frac{1}{s}(s(v_{\mathrm{PV}} i_{\mathrm{PV}}) \cdot s v_{\mathrm{PV}}) \tag{48}$$

The control structure presented in (48) was implemented in the EMPT environment in order to integrate it into the boost converter model in order to control the duty cycle. The PSCAD implementation of the control system can be seen in Figure 35.

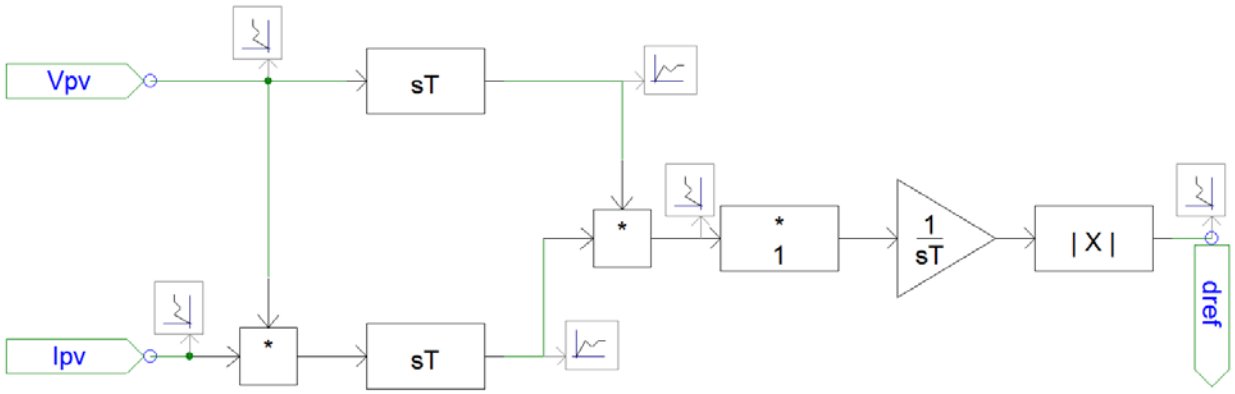


Figure 35. RCC implementation in PSCAD

The duty cycle, d_{ref} ,generated by the control structure shown in Figure 35 was then passed to a pulse generator operating at 50 kHz, with the pulse width adjusted by d_{ref}. This allowed the system to rapidly converge to the MPP, reaching the steady state with minimal overshoot. By implementation of the MPPT through RCC, a system has been designed that allows for extremely efficient power conversion from the PV panels described in Section 3.1 to the balance of the system. Will RCC implemented, the system will next be tested, and its ability to adjust to changes in the environmental conditions.

3.2.2 Simulation Results for RCC under Changes in Solar Insolation

In order to validate the system in terms of both its function under nominal conditions, as well as its ability to properly perform MPPT, the system was tested under three specific test conditions. First, the system was operated under STC, which, as previously described, sets S to 1000 W/m^2 and T to 25° C. The second test examined system dynamics under small changes of 100 W/m^2, introduced intentionally into the system at 1s intervals. The third test examined system dynamics under large changes of 500 W/m^2 at 1s intervals. The three tests together show robust system performance under all three test conditions, demonstrating that the RCC MPPT algorithm coupled with a properly designed boost converter is capable of handling dynamic system changes. Note that in these simulations S was used as the dependent variable, rather than T. This is because in general, large changes in T are not experience in short time periods in PV installations. However, the RCC MPPT would be able to equally handle such perturbations in T, especially considering the smaller increments generally experience in changes in T. The expected MPP conditions, based on the datasheet values is shown in Table 10.

Table 10. Predicted V_{MPP}, I_{MPP}, P_{MPP}

S (W/m2)	V_{MPP} (V)	I_{MPP} (A)	P_{MPP} (kW)
1000	269.1	8.03	2.161
900	279	7.2	2.009
800	283.5	6.3	1.786
700	289.2	5.5	1.591
600	293	4.61	1.351

A. Test Condition I: Simulation for RCC MPPT Boost Converter at STC

The first test performed on the system was used to demonstrate its capability to perform as desired at STC, generating the ideal MPP from the PV panels and the system as a whole. To do so, the *S* input to the system was fixed at 1000 W/m^2, as shown in Figure 36. The system *T* was held constant at 25° C. The simulation was run for a duration of 6 seconds, with a simulation time step of 1 µS. Note that the RCC control was initiated at 1s into the simulation, after it has reached a stable initialized steady state.

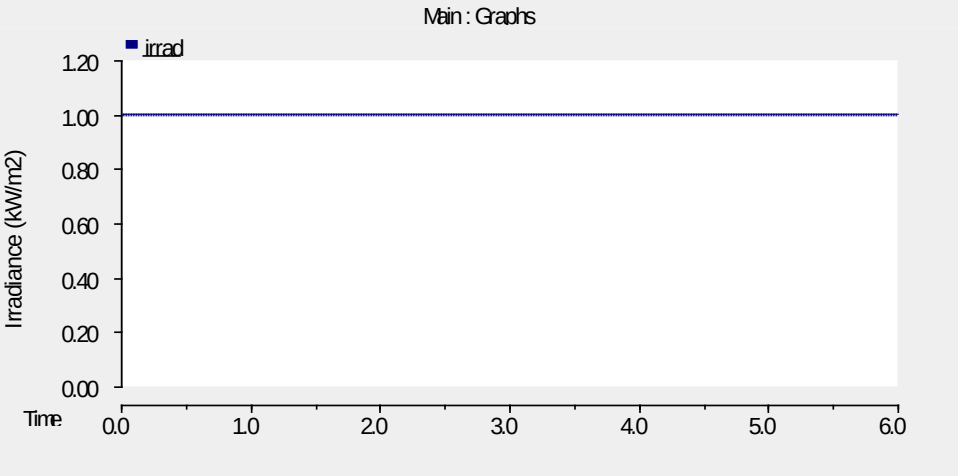


Figure 36. Test Condition I: *S* input to PV panel model

With the input set as shown in Figure 36, output waveforms were generated for the input variables I_{PV}, V_{PV}, and P_{PV}, as well as the output variables I_D, V_D, and P_D. These values were then compared to those predicted in Table 10, in order to determine the accuracy with which the simulated model matches the theoretical values at the MPP for each *S*. The results for Test Condition 1 are presented for input (shown in blue) and output (shown in green) current, voltage and power in Figure 37, Figure 38, and Figure 39, respectively.

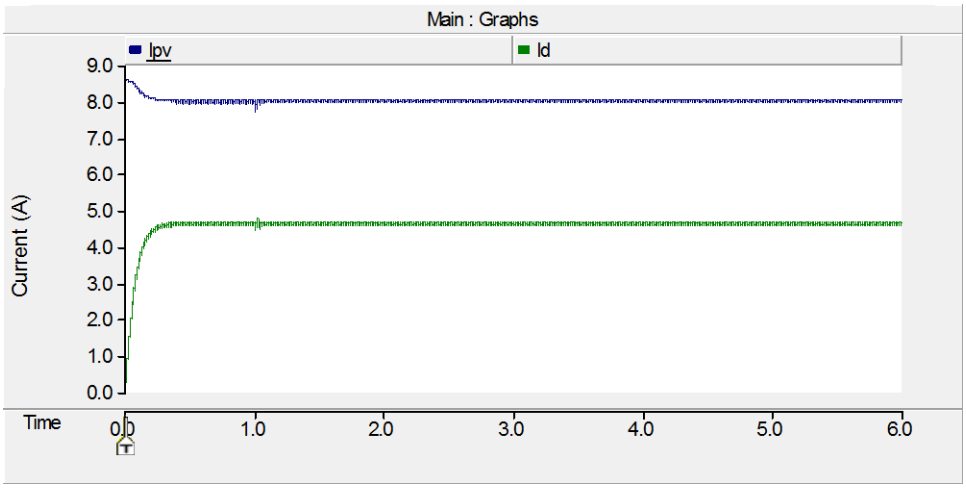


Figure 37. Test Conditions I: input and output current waveforms

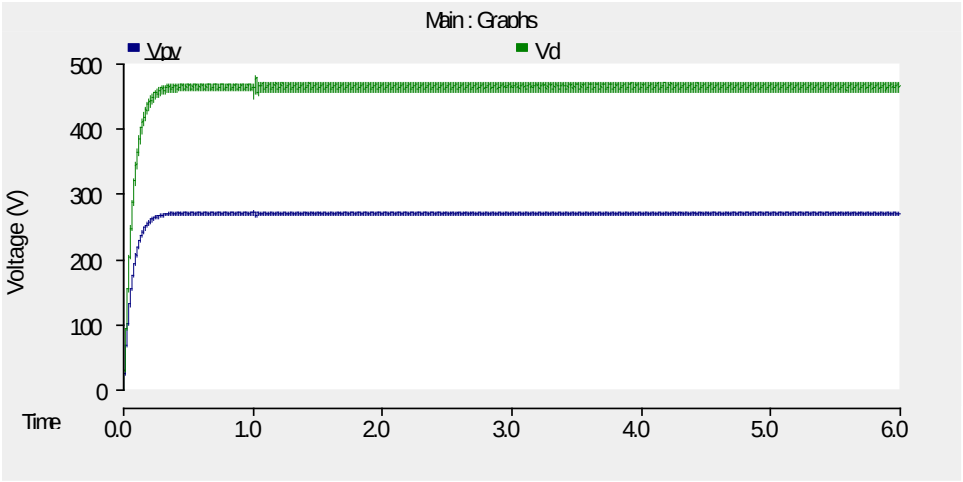


Figure 38. Test Condition I: input and output voltage waveforms

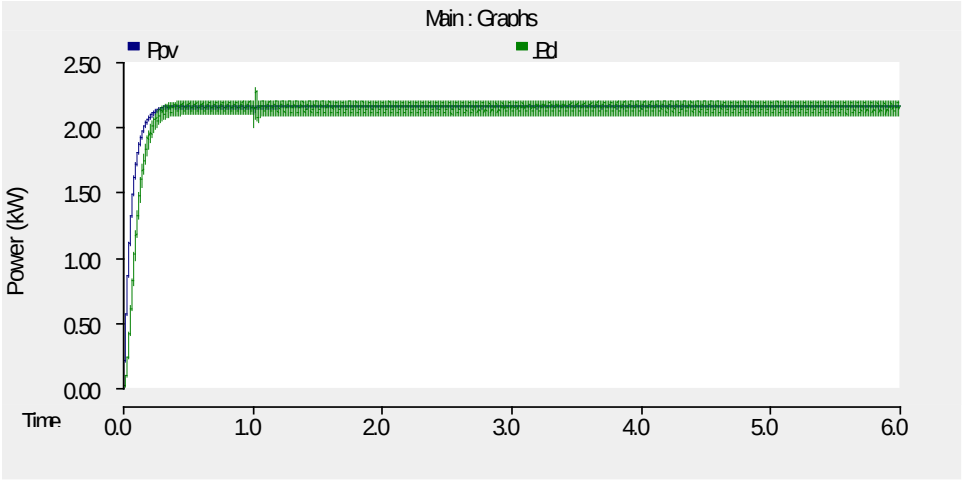


Figure 39. Test Condition I: input and output power waveforms

From the figures presented on the previous page, it can be seen that the system rapidly converges to the MPP at STC, and performs with minimal ripple under steady state conditions. The simulated system reaches within a very small margin of error of the expected MPP presented in Table 10, as the V_{MPP}, I_{MPP}, and P_{MPP} reach 268.7 V, 8.02 A, and 2.155 kW. These values are essentially identical to those presented by the datasheet, and demonstrate that both the PV model presented in Section 3.1, as well as the boost converter and RCC models presented in Section 3.2.1.

B. Test Condition II: Simulation for RCC MPPT Boost Converter with Small S Changes

The second test performed on the system was used to demonstrate its capability to adjust to small changes in *S*, converging quickly as well as matching the ideal MPP from the PV for each irradiance step. To do so, the *S* input to the system was fixed at 1000 W/m^2, and then, following system initialization, was decreased by 100 W/m^2 at 1s intervals, as shown in Figure 40. The system *T* was held constant at 25° C. The simulation was run for a duration of 6 seconds, with a simulation time step of 1 µS. Note that the RCC control was initiated at 1s into the simulation, after it has reached a stable initialized steady state.

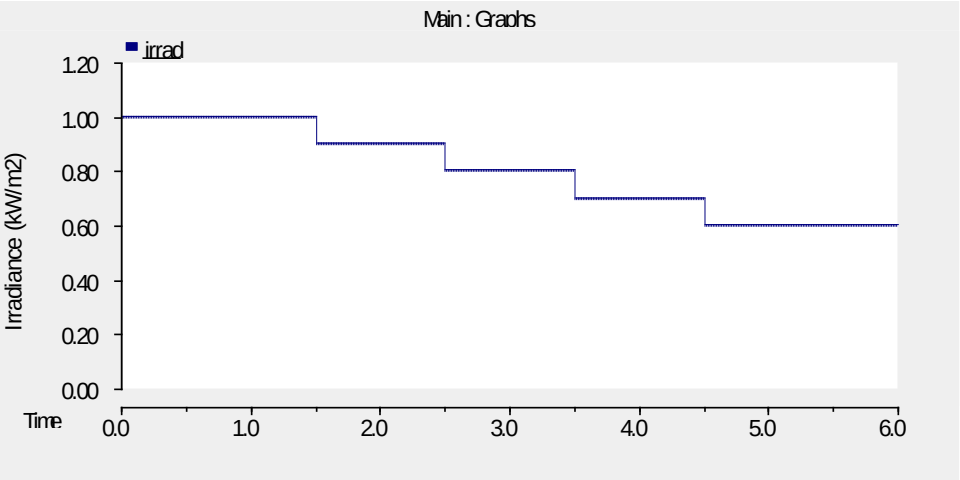


Figure 40. Test Condition II: *S* input to PV panel model

With the input set as shown in Figure 36, output waveforms were generated for the input variables I_{PV}, V_{PV}, and P_{PV}, as well as the output variables I_D, V_D, and P_D. These values were then compared to those predicted in Table 10, in order to determine the accuracy with which the simulated model matches the theoretical values at the MPP for each S. The results for Test Condition II are presented for input (shown in blue) and output (shown in green) current, voltage and power in Figure 41, Figure 42, and Figure 43, respectively.

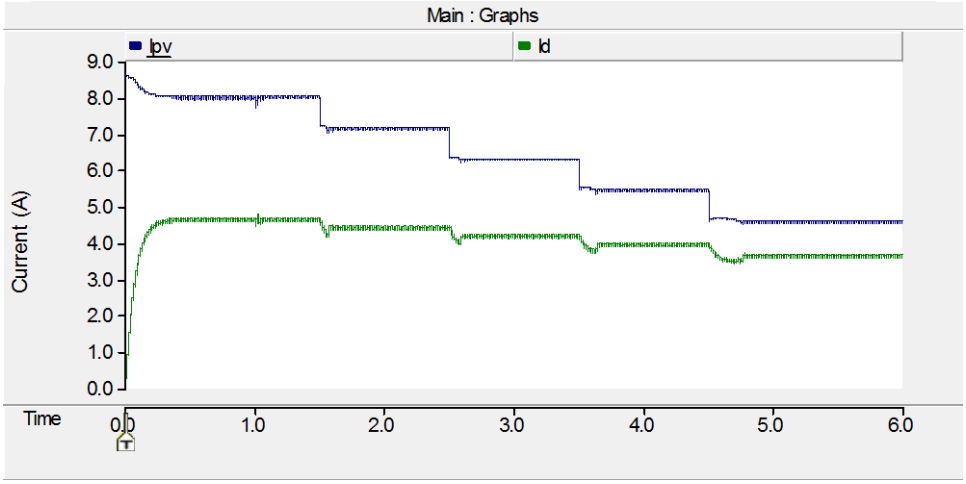


Figure 41. Test Conditions II: input and output current waveforms

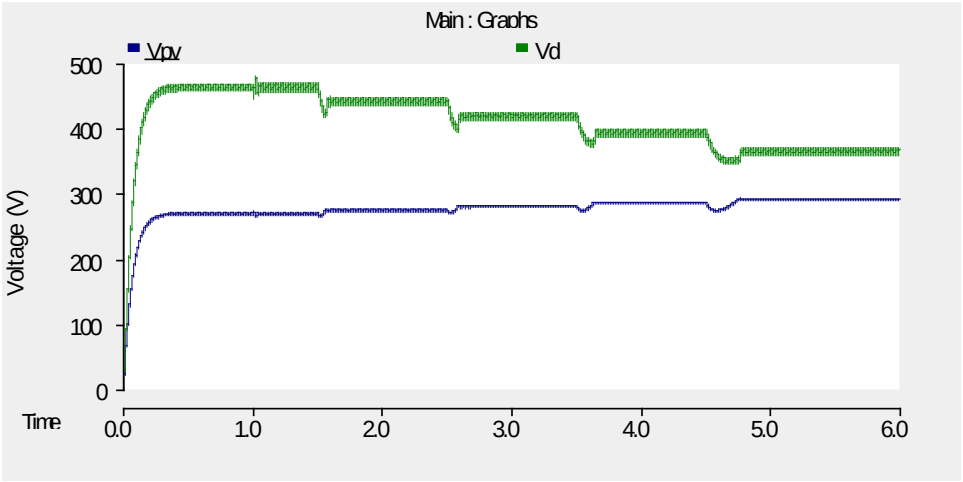


Figure 42. Test Condition II: input and output voltage waveforms

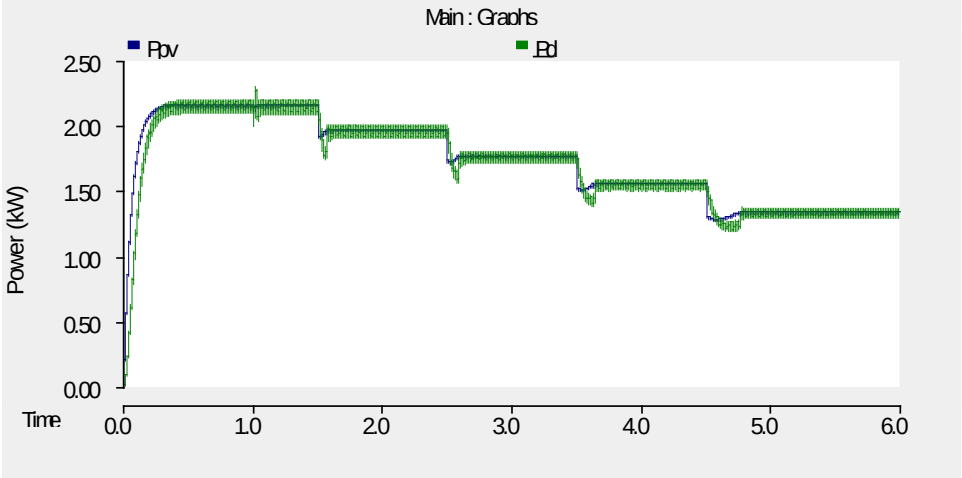


Figure 43. Test Condition II: input and output power waveforms

From Figure 41, Figure 42, and Figure 43, it can be seen that the system rapidly converges to the MPP at each value of *S*, and performs with minimal ripple under steady state conditions. The simulated system reaches within a very small margin of error of the expected MPP presented in Table 10, as shown in Table 11.

Table 11. Simulated values at varying *S* and their percent error relative to Table 10

***S* (W/m2)**	**V_{MPP} (V)**	**Error**	**I_{MPP} (A)**	**Error**	**P_{MPP} *(kW)***	**Error**
1000	268.7	99.9%	8.02	99.9%	2.155	99.7%
900	274	98.2%	7.14	99.2%	1.962	97.7%
800	280.6	99.0%	6.28	99.7%	1.762	98.7%
700	285.9	98.9%	5.44	98.9%	1.555	97.8%
600	289.1	98.7%	4.58	99.3%	1.324	98.0%

These values are essentially identical to those presented by the datasheet, and demonstrate that both the PV model presented in Section 3.1, as well as the boost converter and RCC models presented in Section 3.2.1. Also of note are the settling times, as the convergence to MPP with small steps in *S* can be seen to range from less than 50 ms in the step change from 1000 W/m^2 to

900 W/m^2, to approximately 200 ms in the step change from 700 W/m^2 to 600 W/m^2. This demonstrates the rapid convergence that is expected from the RCC MPPT algorithm.

C. Test Condition III: Simulation for RCC MPPT Boost Converter with Large S Changes

The second test performed on the system was used to demonstrate its capability to adjust to small changes in *S*, converging quickly as well as matching the ideal MPP from the PV for each irradiance step. To do so, the *S* input to the system was fixed at 1000 W/m^2, and then, following system initialization, was decreased by 400 W/m^2 at 1s intervals, as shown in Figure 44. The system *T* was held constant at 25° C. The simulation was run for a duration of 6 seconds, with a simulation time step of 1 µS. Note that the RCC control was initiated at 1s into the simulation, after it has reached a stable initialized steady state.

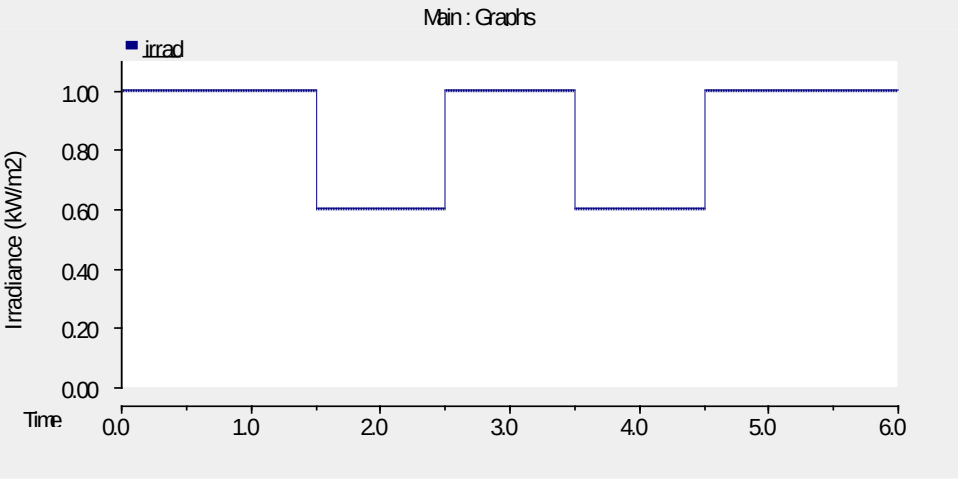


Figure 44. Test Condition III: *S* input to PV panel model

With the input set as shown in Figure 36, output waveforms were generated for the input variables I_{PV}, V_{PV}, and P_{PV}, as well as the output variables I_D, V_D, and P_D. These values were then compared to those predicted in Table 10, in order to determine the accuracy with which the simulated model

matches the theoretical values at the MPP for each *S*. The results for Test Condition III are presented for input (shown in blue) and output (shown in green) current, voltage and power in Figure 45, Figure 46, and Figure 47, respectively.

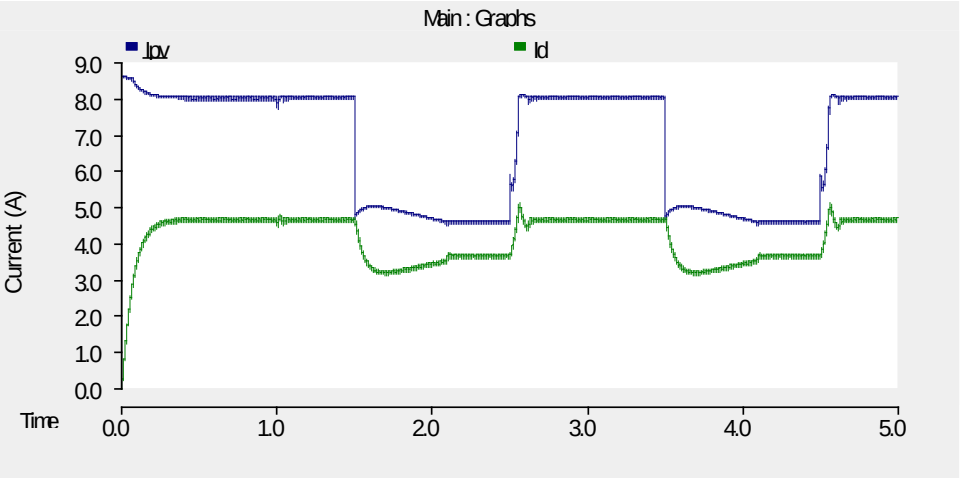


Figure 45. Test Conditions III: input and output current waveforms

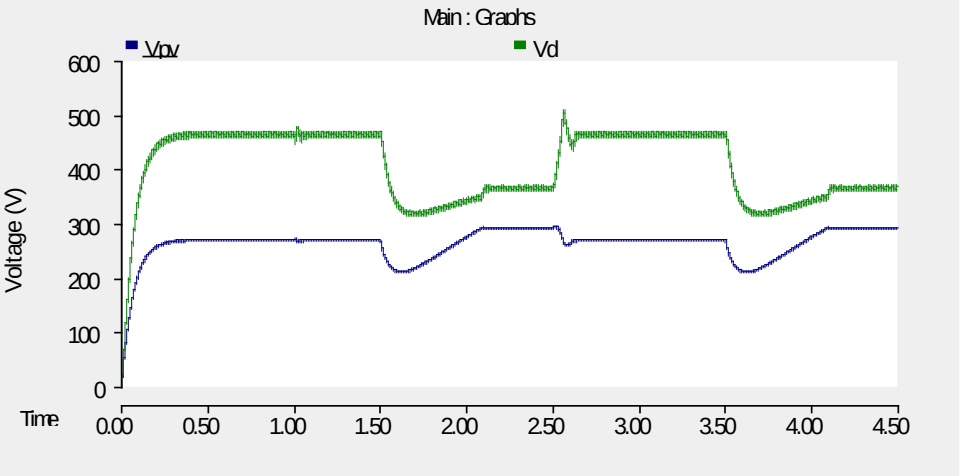


Figure 46. Test Condition III: input and output voltage waveforms

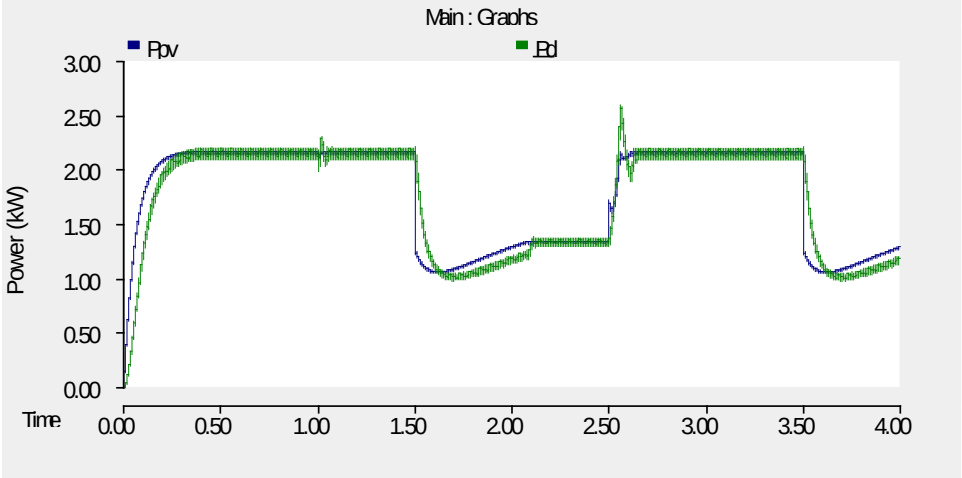


Figure 47. Test Condition III: input and output power waveforms

From Figure 45, Figure 46, and Figure 47, it can be seen that the system rapidly converges to the MPP at each value of *S*, and performs with minimal ripple under steady state conditions. Here, the steady state results were the same as presented in Table 11. However, here the settling time is significantly larger during the negative transition from1000 W/m^2 to 600 W/m^2. Here it can be seen that the system takes approximately 600 ms to stabilize that the MPP. However, while this is significantly longer than under Test Condition II, it can still be seen to be faster than most other MPPT methods, as seen in [32]. Also of note is that the positive transition is much more rapid, occurring in approximately 100 ms. However, there is significant overshoot initially, again pointing to larger transient concerns under extremely rapid change. Pure step changes, however, are generally uncommon in *S*, as even with rapid cloud cover, PV panels are rarely shaded instantaneously. This section of the simulation again confirms the performance of the RCC MPPT algorithm, and its implementation in the boost converter system.

3.3 CONCLUSION

This chapter presented an alternative to the synchronous buck converter which had been previously demonstrated in Chapter 2. Here instead, the PV panels were integrated to the balance of the system using a boost converter, for which the duty cycle was set via a MPPT algorithm. The algorithm used in this chapter was RCC as presented in [33] and [7] and implemented in the frequency domain as described in (48) and implemented as shown Figure 35. This control structure was applied to the boost converter system shown in Figure 34, for which the PV panel was modeled by the equivalent circuit described in [35] and implemented as shown in Figure 32 [36]. The performance of this system was then demonstrated, first at STC, then with small step changes in *S* and finally with large step changes in *S*. In these simulations, the capability of the RCC MPPT algorithm was shown to rapidly converge to the MPP of the system, and to be accurate to within 98% of the expected values given by the manufacture's datasheet [37] as shown in Table 10 and Table 11. The results from the varying simulations then showed that even with large step changes in *S*, which are unlikely in natures, the system could rapidly adjust to new conditions, finding the MPP just over 600 ms. These results demonstrate the capability of the RCC MPPT system in the boost converter topology, and indicate the importance of MPPT in general for the integration of PV generation sources into the system as a whole. MPPT allows for panels to operate at vastly varying environmental conditions, while maintaining high efficiency and extracting as much power as possible from the installed capacity of the system.

4.0 THE LOW VOLTAGE, SINGLE PHASE, MODULAR MULTILEVEL CONVERTER (MMC)

In order to integrate the PV panel array and DC-DC converters described in previous chapters to an AC grid, an inverter is required, as shown in Figure 1. In most moderns system integrations, manufacturers are moving towards topologies based on voltage-source converters (VSCs), as they provide a number of advantages over current source inverters when coupled with a PV system [38]. Specifically, multilevel converter topologies, such as the neutral point clamped converter [1] provide the capability to "build" voltage waveforms from fixed step sizes, rather than relying on large filtering components to smooth out square waves generated from pulse width modulation (PWM). One specific example of the growth of the multilevel topology in power electronics can be seen in the area of High Voltage Direction Current (HVDC), where many leading manufacturers and researchers are now turning toward a system topology known as the Modular Multilevel Converter (MMC). The MMC provides a means by which large voltages can be broken into small switching events, allowing voltage waveforms to be built from small step sizes, improving output performance, minimizing filtering requirements, and reducing stress on individual semiconductor devices. Extensive documentation exists for the MMC topology in the HVDC setting, as it provides a number of advantages for long distances transmission systems, especially when underground or underwater transmission is a necessity, or when space is at a premium [39]. In this chapter, a MMC system will be explored, focused on scaling systems designed for HVDC power transmission to a power and voltage levels suitable for use in PV systems, either for integration to the grid, or for islanded operation for local loads.

A number of topologies exist for MMC systems, which range from systems comprised of half H-bridge, full H-bridge, hybrid H-bridge, and more [40]. Additionally, literature has been developed showing interest in low voltage, high power-density applications for modular converter topologies, as shown in [41]. Here, a similar approach will be taken, focusing on a low voltage system for PV integration based on the half H-bridge topology presented in [42]. This topology consists of series connected switched submodules based on the half H-bridge inverter. Each submodule consists of two semiconductor devices and one switch capacitor, shown in Figure 48. The cell operates as shown in Figure 49. The two semiconductor devices in the system are switched inversely, with S_1 introducing the submodule capacitor into the system, and S_2 removing it.

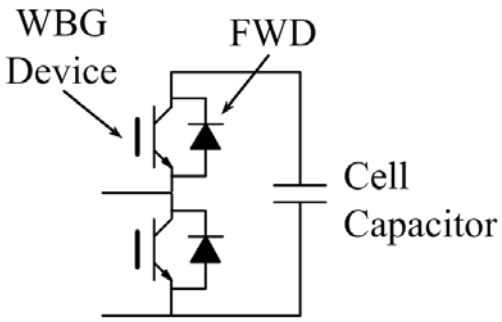


Figure 48. Half-bridge submodule topology for MMC inverter

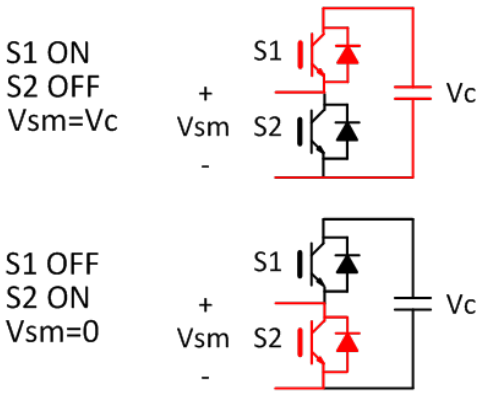


Figure 49. Submodule operation of MMC showing primary switching states

The objective is to add or remove the voltage and charge stored on the capacitance to the system, yielding either 0 V output, or output equal to the voltage on the capacitor, based on the switching state. These submodules are then combined in series to form converter, as shown in Figure 50.

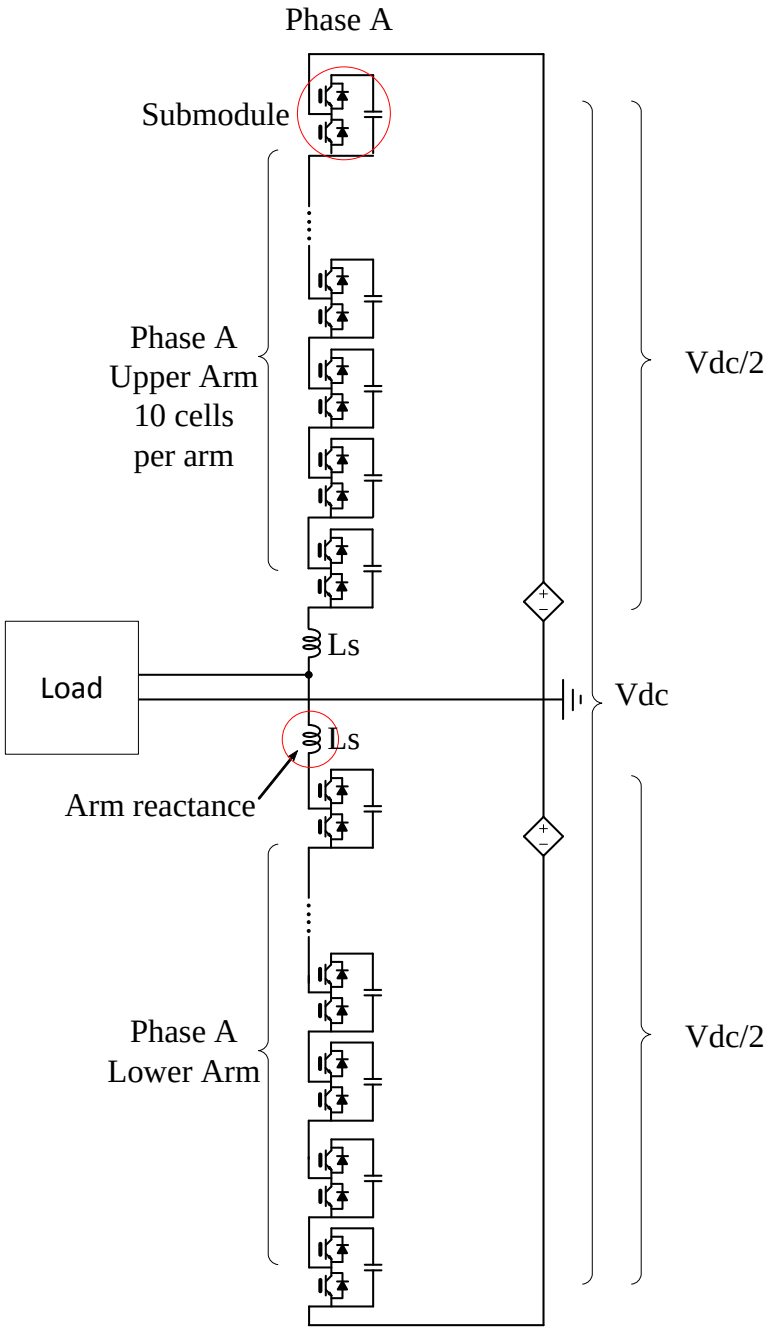


Figure 50. Single phase MMC inverter topology

The series combination of submodules of the MMC, as presented in Figure 50, allows for the creation of a voltage waveform that closely approximates a sinusoidal waveform, with little to no filtering requirements. The voltage of the converter is described by [42]:

$$V_{\mathrm{DC}} = V_{\mathrm{Upper}} + V_{\mathrm{Lower}} \tag{49}$$

$$V_{\mathrm{DC}} = \sum_{i=1}^{N} \left(S_{\mathrm{Upper},i} V_{\mathrm{capacitor},i}\right) + \sum_{i=1}^{N} \left(S_{\mathrm{Lower},i} V_{\mathrm{capacitor},i}\right) + L_{\mathrm{s}} \left(\frac{d}{dt} i_{\mathrm{Upper}} + \frac{d}{dt} i_{\mathrm{Lower}}\right) \tag{50}$$

Where, N is the number of submodules per arm, S is the binary on/off state of submodule i, L_{S} is the inductance of the arm reactor, and *upper* and *lower* designate the upper or lower arm of the converter phase. Note that at any time there can be no more than N submodules in their on state. This can be expressed as:

$$\sum_{i=1}^{N} \left(S_{\mathrm{Upper},i} + S_{\mathrm{Lower},i}\right) = N \tag{51}$$

The AC voltage magnitude can be described by:

$$V_{\mathrm{AC}} = m_{\mathrm{A}} \frac{V_{\mathrm{DC}}}{2} \tag{52}$$

Where m_{A} is the modulation index, between 0 and 1, provided by the control system of the converter. The number of levels in the AC waveform generated by the MMC topology is $N + 1$, as up to *N/2* states exist in both the positive or negative sides of the AC waveform, in addition to the 0 voltage state of the converter. For HVDC MMC systems, N can be in the hundreds, allowing for very fine voltage waveform generation with minimal harmonics produced by the converter, as well as drastically reduced voltages experienced by the semiconductor devices.

In HVDC MMC applications the semiconductor device is typically an IGBT, as seen in [40]. The reliance on IGBTs is a result of the extremely high voltage on those systems, often 10 kV or more on a single device. In the application presented here, however, both system and device voltages are significantly lower, at most on the order of 100 V, enabling the use of WBG semiconductors for switching applications. As discussed previously in Chapter 2.0 these devices can provide significant advantages over their Si counterparts, further improving this already efficient topology. The MMC topology is perfectly suited to construction from many small WBG semiconductors, taking advantage of the superior performance and size of the WBG devices to drastically reduce converter size and improve efficiency.

4.1 MMC SYSTEM DESIGN AND EVALUATION

4.1.1 System Parameters and Model Construction

In the case of the low voltage MMC developed for this chapter, a system was designed with $N = 10$ in order to convert the nominal 460 V_{DC} output from the boost converter described in Chapter 3.0 into the balance of the system to a 120 V_{AC} single phase output suitable for integration into AC system loads. Since the 460 V_{DC} value describes the ideal lighting conditions, and m_A must be kept below 1.0 in order to avoid converter saturation, the MMC system was designed for $V_{DC} = 400$ V. For each of the submodules in the system, two values needed to be calculated. First, the amount of voltage required per submodule was found via:

$$V_{\text{submodule}} = \frac{V_{DC}}{N} = \frac{400V}{10} = \frac{40\text{ V}}{\text{submodule}} \tag{53}$$

Next the capacitor for each submodule was sized. This was done using the reference system presented in [42] and an energy balance equation to resize the previously modeled system for the low voltage converter, described by:

$$C_{\text{new}} = C_{\text{ref}} \cdot \frac{N_{\text{new}}}{N_{\text{ref}}} \cdot \frac{S_{\text{new}}}{S_{\text{ref}}} \cdot \left(\frac{V_{\text{DC}ref}}{V_{\text{DC}new}}\right)^2 = 2500\mu\text{F} \cdot \frac{10}{6} \cdot \frac{2.5\text{ kVA}}{50\text{ MVA}} \cdot \left(\frac{60\text{ kV}}{400\text{ V}}\right)^2 = 7.3\text{ mF} \quad (54)$$

From (52), (53), and (54) the nominal system parameters can be found, as shown in

Table 12. Simulated MMC system parameters

Parameter	Value
P_{NOM}	2.5 kVA
V_{DC}	400 V
V_{AC}	120 V
m_{A}	0.85
V_{SUB}	40 V
C_{SUB}	7.3 mF
L_{ARM}	0 H
f_{SUB}	2.5 kHz

Using these parameters, the system was modeled in the PSCAD EMTP environment, as shown in Figure 51. Of particular note is the large capacitance required by each submodule. This is due to the lower voltage and energy totals of the converter, while still using a low switching speed. In the HVDC implementation of the MMC topology, the switching frequency has to be limited due to very large Si IGBT modules, with multiple modules switching in series. In the low voltage implementation, an opportunity exists for future work in which the switching frequency could be raised significantly, and the benefits of WBG semiconductors could be taken advantage of for improved switching performance.

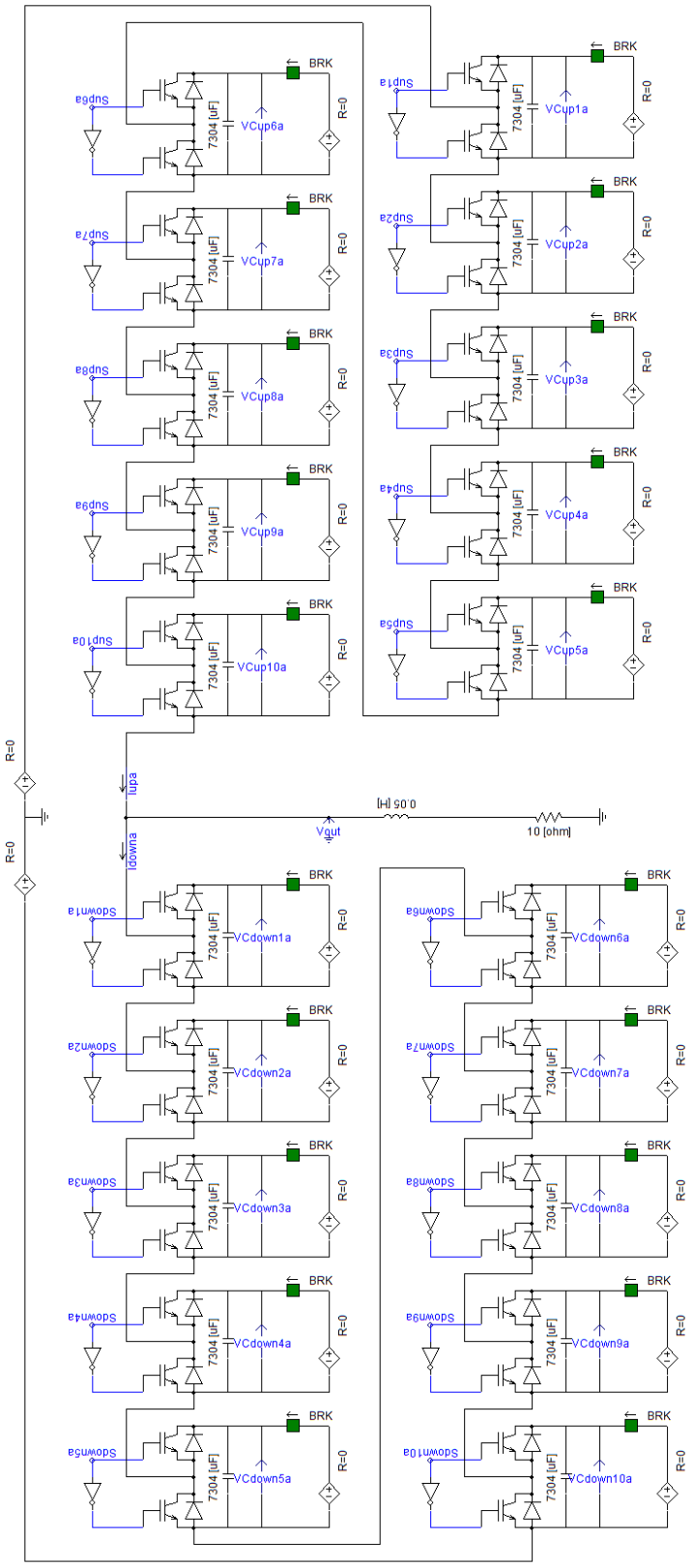


Figure 51. PSCAD implementation of single phase, 10 cell MMC

4.1.2 Capacitor Balancing Algorithm

A problem that arises if left unaddressed is a voltage imbalance between the various capacitors in a given arm. This is due to the different rates at which the capacitors are switched, resulting in more charge being stored in the capacitors that are switched the least frequently. To remedy this problem an algorithm was implemented based on that demonstrated in [42], which relies on selection of cells based on capacitor voltage and the direction of current flow. The strategy can be separated into three distinct portions: determination of the number of conducting cell capacitors per arm, sorting of cells based on capacitor voltage, and selection of the conducting cells based on current direction. An overview of the process can be seen in Figure 52.

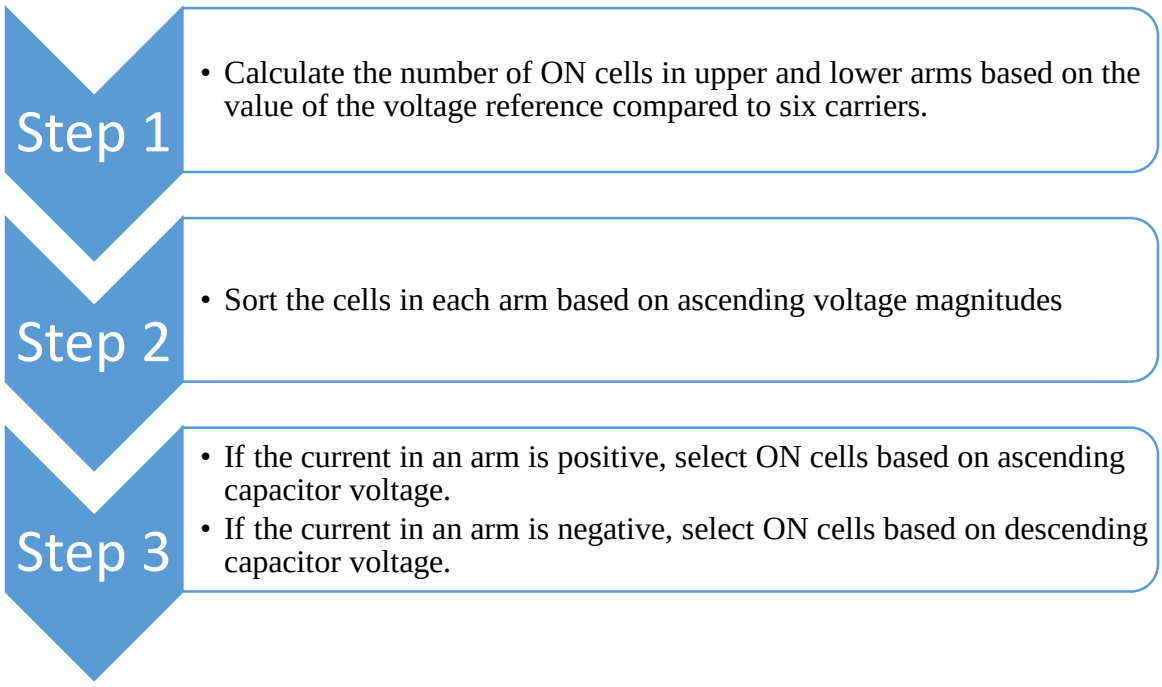


Figure 52: Overview of Capacitor Balancing Process

In a given phase of the converter, there must be exactly ten cell capacitors conducting at any given moment in time. As discussed previously, this can be represented by (51). In order to determine the total number of upper and lower cells that must be on, a comparative algorithm was used. This algorithm compared a third harmonic injected sinusoidal waveform to a series of ten triangular carrier waveforms which evenly divided the magnitude of the reference, as shown in Figure 53. The third harmonic component extends the peak of the waveform, allowing for higher RMS voltage output without pushing m_A over 1.0.

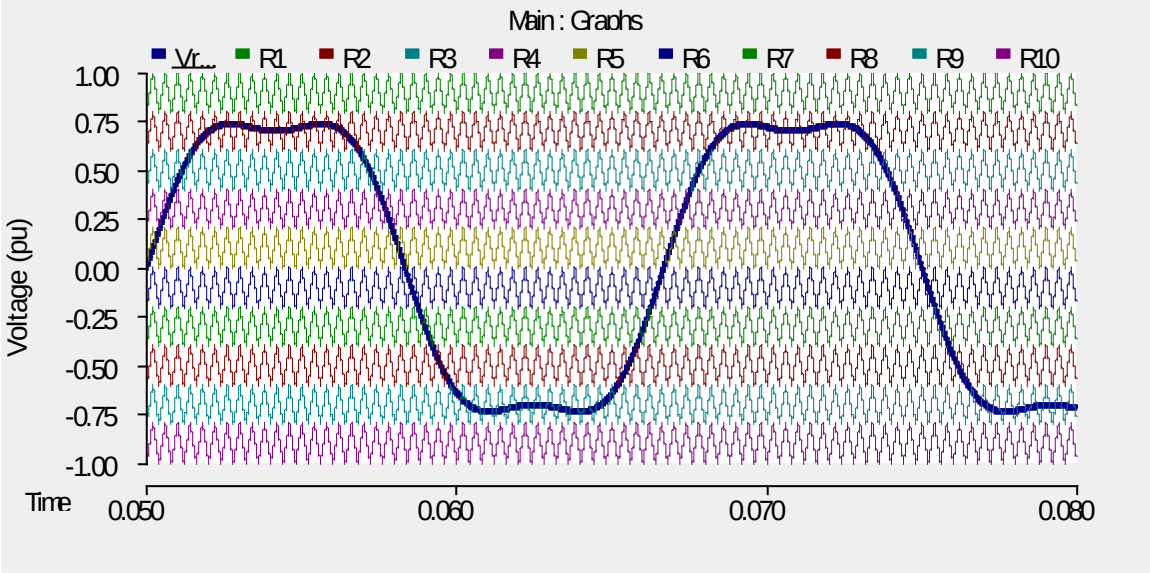


Figure 53: Reference and carrier waveforms for switching algorithm

Each carrier signal was tied to a comparator. The output of each comparator was set equal to 1 when the reference voltage was greater than its corresponding carrier signal, and was set equal to 0 otherwise. The outputs of all of the comparators for a given phase were summed, from which the total number of necessary ON cells was extracted for the upper arm, yielding Nup. The same

was done for the inverse of the comparator outputs, yielding the total number of necessary ON cells for the lower branch, Ndown. This system is shown in Figure 54

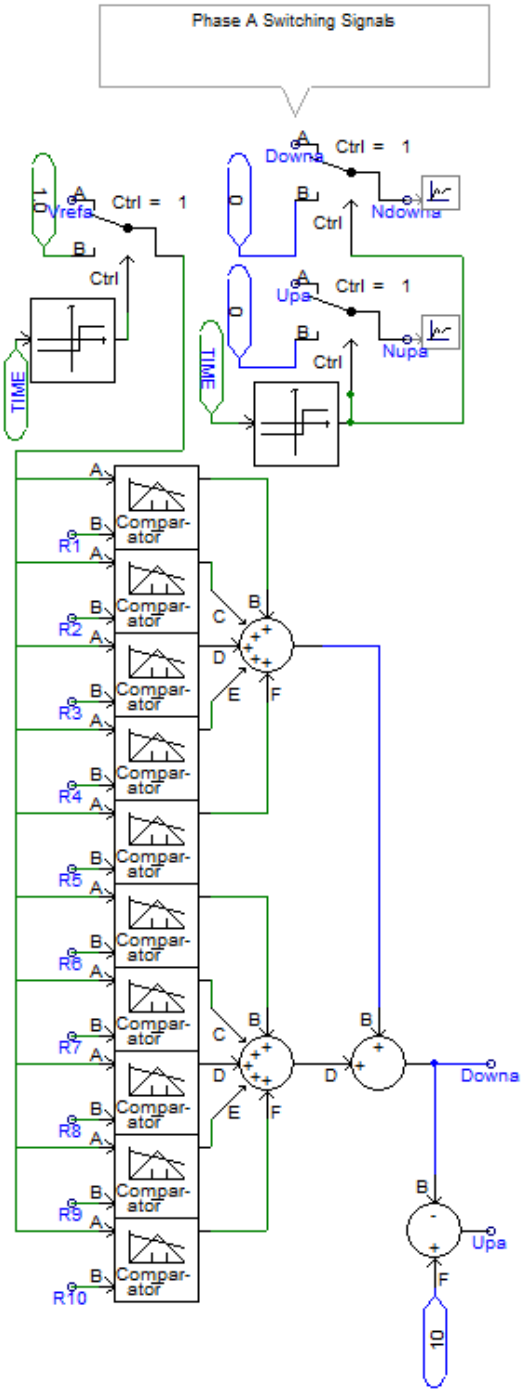


Figure 54: Calculation of the number of ON cells in the upper and lower arms

The next step was to sort the cells in the upper and lower arms of a given phase in order of ascending capacitor voltage. The sorting algorithm chosen was a standard bubble sort, which was chosen for its simplicity in terms of implementation in the PSCAD environment. The bubble sort functions by comparing each capacitor voltage to the next one and pushing the higher voltage towards the top of the array. This process is repeated until the voltages are in ascending order. However, rather than outputting the array of capacitor voltages, the function block that was implemented instead outputs the indices of the corresponding switches. Thus, if cell 5 in the upper arm had the highest capacitor voltage, the last element of the output array would be 5. This sorted array was sent as output to the selection block.

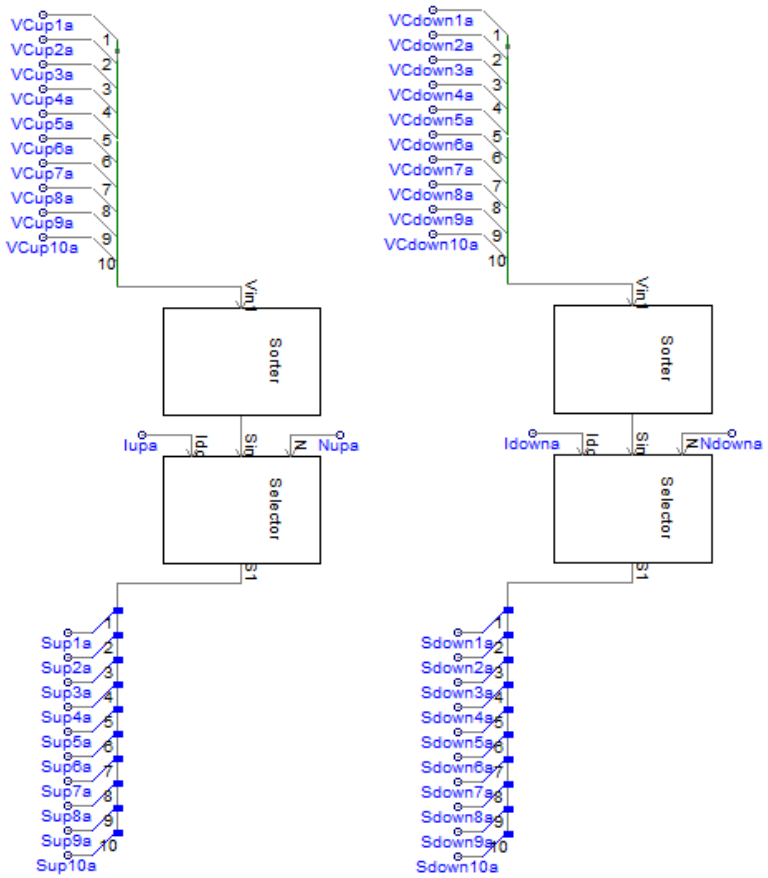


Figure 55: Sorting and Selection Modules for the Upper and Lower Arms of Phase A

The final step of the voltage balancing system was the selection algorithm. This module had 3 inputs: the number of cells ON in the given arm, the measured current flowing in the arm, and the sorted array of cell indices from the capacitor voltage sorting algorithm. If the current flowing in the arm was positive, the module selected the number of cells specified in ascending order. If the current flowing in the arm was negative, the module selected the number of cells specified in descending order. The module then output the necessary signals to switch the IGBTs. An image of the sorting and selection modules can be seen in Figure 55. The Fortran code for both the sorter and selection blocks can be seen in Appendix I. The systems described in this section function together to hold the voltage on the capacitors constant to a constant steady state value with minimal fluctuation around that point.

4.1.3 Simulation Results

The system developed in the previous two sections was simulated in the PSCAD environment, demonstrating the functionality of both the capacitor balancing algorithm and the converter as a whole. First, a demonstration of the capacitor balancing algorithm was performed. Without the algorithm described in Section 4.1.2, the voltage on the capacitors that are switched more or less will gain or lose charge as the system runs. This phenomena decreases the voltage output of the converter, eventually causing the control system to overcompensate, driving m_{A} above one and the converter into saturation. The voltage drift that occurs on the capacitor can be seen in

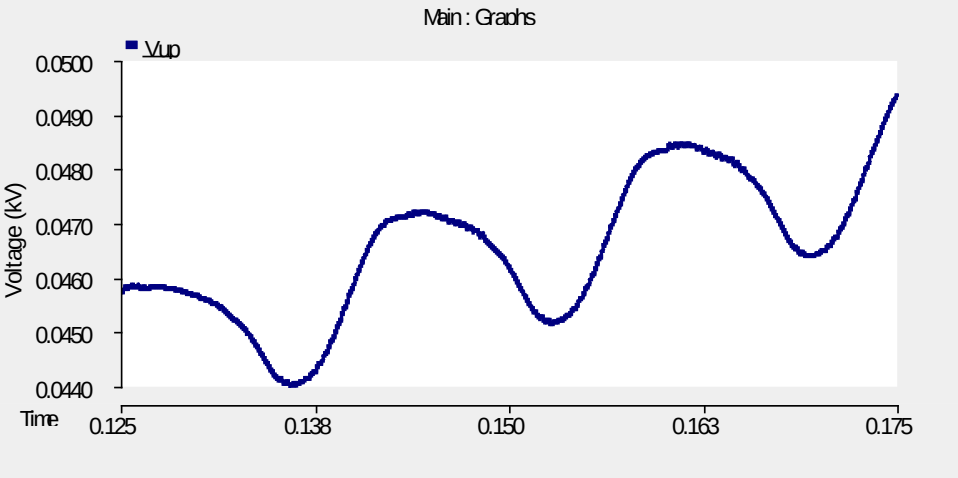


Figure 56. Voltage drift on upper arm capacitor without balancing control

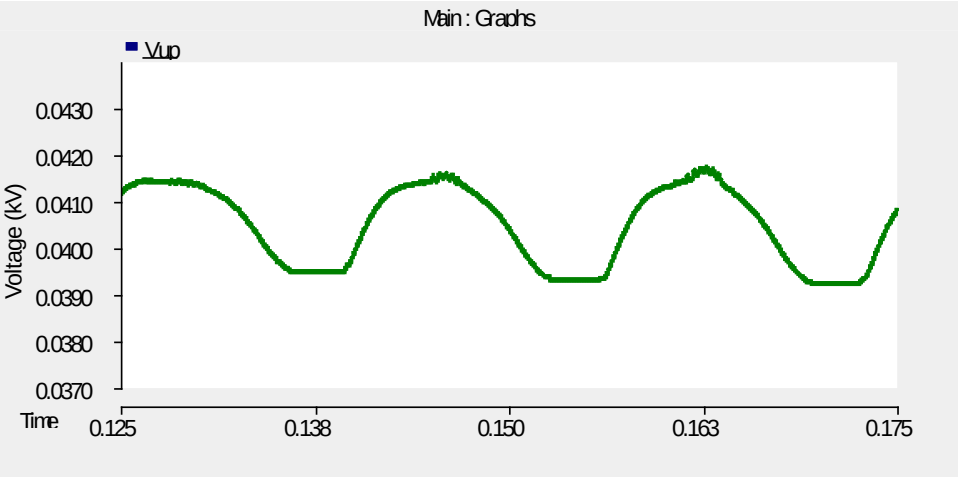


Figure 57. Balanced voltage in upper arm capacitor under balancing control

When the voltages are properly balanced as shown in Figure 57, the system produces a voltage waveform that closely approximates the desired sinusoid. For systems which are islanded, the THD introduced by this waveform is usually acceptable for most applications. That is, most local loads will not be disturbed by the harmonics generated by the system. In grid tied applications through a transformer, the transformer itself is often enough filtering to remove any negative impacts

introduced from the system output. The voltage output waveform can be seen in Figure 58, demonstrating the performance of the MMC topology, even when scaled to low voltages.

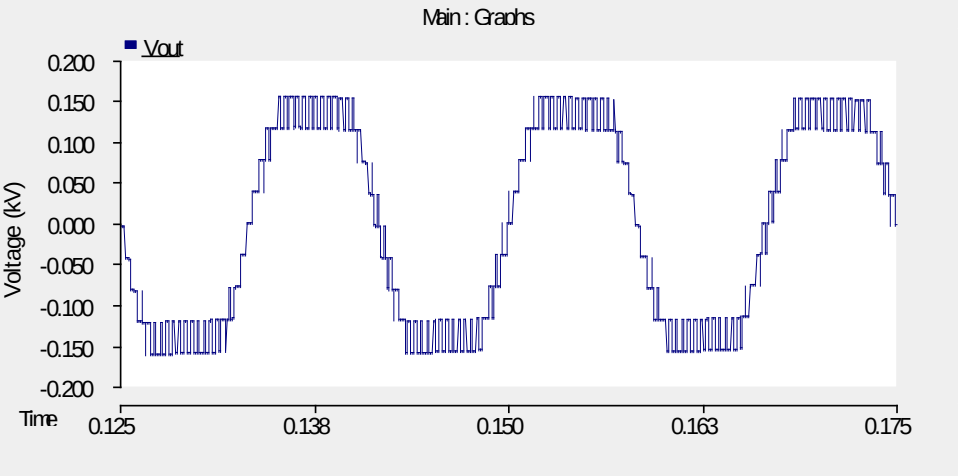


Figure 58. Voltage output from single phase, 10 cell, MMC inverter

4.2 CONCLUSION

In this section, a low voltage, single phase MMC system was designed for the purpose of integrating the DC-DC converter controlling the PV panels to the system. The design was achieved by scaling a common design from HVDC transmission applications to the low voltage level. Designed to take advantage of a 10 cell MMC system, the converter covered in this section takes advantage of small voltage and energy switching events to minimize converter size, while still providing an approximately sinusoidal voltage output to the system. First, the MMC system as implemented in the single phase structure was described, and equations were presented in order to characterize system performance. Next, the system was implemented in the PSCAD EMPT environment in order to demonstrate converter performance. In order to properly regulate the

converter, a capacitor voltage balancing algorithm was also developed in PSCAD, forcing the ripple on the capacitors to stay within an acceptable range and preventing voltage drift. Finally, the system output was shown, demonstrating of the low voltage MMC for system integration.

5.0 DESIGN AND REALIZATION OF AN INNOVATIVE WORKBENCH FOR ELECTRIC POWER SYSTEMS LABORATORIES

The following sections of Chapter 5.0 appears as published under the same title in IEEE Transactions on Power Systems. The laboratory setup presented here allows for testing and integration of the previously discussed power electronics systems, creating an environment with diverse sources and loads to accurately emulate modern grid conditions. In terms of FIG., it represents the system load or the balance of the system. Either grid tied or islanded conditions between the laboratory workbench and the rest of the laboratory, allowing for PV integration and testing in either condition. Additionally, it creates a learning environment in which future students can be trained in power systems using state of the art equipment and techniques.

5.1 INTRODUCTION

One of the essential components of engineering student development is hands on training. While the classroom experience is essential for understanding the fundamentals of power systems, there is no replacement for applied learning on the actual equipment that is used in the field. To facilitate such hands-on learning, the University of Pittsburgh and Eaton are developing the Electric Power Systems Lab at the Swanson School of Engineering [43]. The laboratory will be equally focused on research and education. The layout of the laboratory is designed to integrate a wide array of power systems equipment in a seamless manner, with the central elements being six innovative lab workbenches. A three dimensional rendering of the laboratory can be seen in Figure 59.

Existing educational facilities and laboratories are based upon one of the following three approaches: black box [44], [45], blue box [44], [45], and conceive, design, implement and operate (CDIO) approach [45].

The black box approach utilizes pre-built modules into an experiment, as compared to the blue box approach where the user has understanding of the internal subsystems prior to use and can make adjustments, accordingly. Finally the CDIO approach emphasizes total system design.

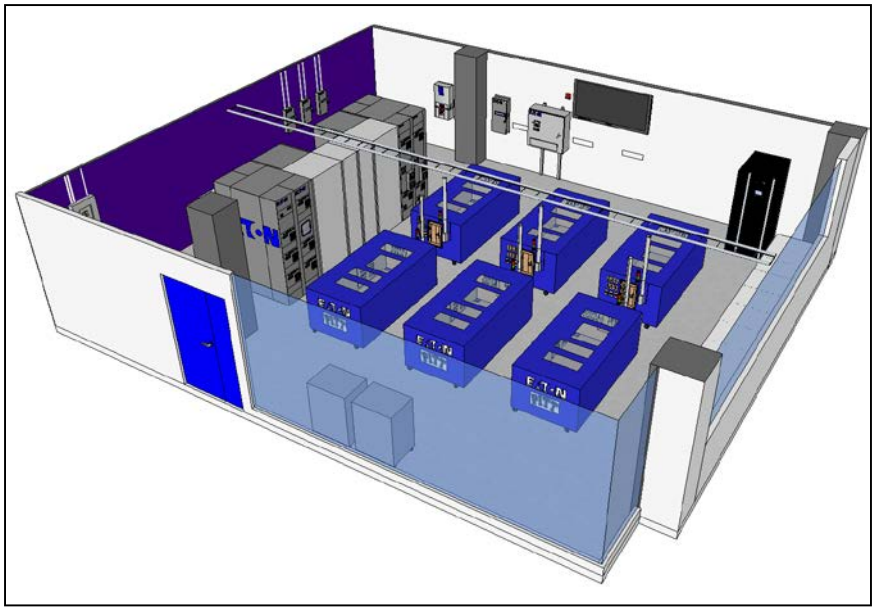


Figure 59. Three-dimensional rendering of the Electric Power Systems Lab.

The bench design described in this paper is a hybrid of the blue box and CDIO approach depending on use. The Faraday machines laboratory established by Gross and Summers, [46], could arguably be the first to have developed a bench equipped with a variety of machines, transformers and measuring devices in one compact unit and established a case for industry involvement in education. Today, organizations like the Grainger Foundation help to support university laboratory designs. One notable lab bench design funded by the Grainger Foundation is published

in [47]. For the University of Pittsburgh, Eaton is providing equipment and design support for the new laboratory which is designed to be completely synergistic with their Power Systems Experience Center (PSEC), [48], in Warrendale, PA. Other options for those institutes without manufacturer support include vendors like Hampden [49] and Lab-Volt [50] who specialize in power systems laboratory equipment and bench design.

The focus of the article is based on the lab workbench design. The lab workbench is integrated into the overall laboratory, however, the bench itself is capable of functioning as a stand-alone entity. The lab workbench, as shown Figure 60, is compatible with other pieces of power system equipment and can be easily reconfigurable, not application specific, for serving both educational and research needs.

Figure 60. Finalized workbench within the overall power systems laboratory.

The objective of the lab workbench is to seamlessly combine the configurable load banks and programmable logic controller (PLC) controls into the workstations. This design not only provides a wide array of functionality in terms of variable loads and controls, but also minimizes space usage within the laboratory. The design includes resistive, inductive, capacitive, and harmonic loads, with auxiliary connections for other loads and the capability to feed an external motor control center (MCC). Integrated with all of the components are advanced metering devices, allowing students to clearly view all of the electrical phenomena within the bench, and to communicate those readings to the entirety of the lab. With this design in mind, a schematic was laid out, and construction of a prototype commenced. After completion of the prototype, significant tests were performed to demonstrate and confirm the various capabilities of the lab workbench. This paper lays out the creation of a prototype, from design, to construction, through testing and verification, culminating in its commercial realization. Additionally, this work describes the research applications of the lab workbench and provides the framework for the planned experiments for courses which will utilize the laboratory.

5.2 CONCEPTUAL DESIGN PROCESS

The design process began with the layout and specification of the lab workbench itself. The goal was to integrate the load banks necessary for laboratory function with a wide variety of other components in a unit that would also provide a seamless workstation environment. In order to do so, the lab workbench needed to be easily accessible to allow new students to quickly become familiarized with the equipment while ensuring their safety. In addition to those concerns, the goals of the laboratory as a whole had to be taken into account. The lab workbenches were to be

connected to the lab 208V load bus via a 60A feeder, and would be easily reconfigurable to simulate a wide range of power systems applications. One example is a smart grid network, where each bench would act as a load within the network, communicating with one another via individual controllers. Others include an industrial facility, with many motors turning on or off at once, or a substation with a capacitor switching event.

In order to satisfy all of these design goals, the vision for the lab workbench evolved from a simple load bank to a configurable workstation. Here the load bank would be merged with accurate metering, advanced communications, and both manual and PLC controls. In addition to the internal components, the lab workbench would have the capability to drive a motor-generator set through the laboratory's MCCs and to switch power supply to photovoltaic or fossil fuel generators. The end result is a tool for education that is easy to use and can perform a wide variety of experiments, as well as a tool for research that is extremely versatile, providing a huge array of features that are adaptable to situational needs. The variety of load provided by the bench will be fed by and equally diverse mix of sources in the lab, including wind and solar, creating an extremely reconfigurable laboratory environment.

5.2.1 Load Requirements and Specifications

Of primary concern was the layout and sizing of the internal load components. The load banks within the bench needed to have the capability of drawing real and reactive power, drawing harmonic current, and providing capability for power factor correction. These base loads were comprised of banks of resistors, reactors and capacitors. Additionally, a bank of compact fluorescent lights (CFLs) was used to draw harmonic current. The specifications for these components are shown in Table 13. A novel layout was developed for these load banks. The

components were designed to be mounted on a pull-out panel, which could be easily removed from the bench for maintenance or modification. The loads were tied to a common 208V, 3-phase input from the main Integrated Facility Switchboard (IFS).

The other main component of the loads in the lab workbench was a connection through a 30A line to the MCC. This connection allowed the bench to start motors up to 15-hp across the line or via soft start, and could be used to run a 5-hp motor-generator set using a variable frequency drive (VFD).

Table 13. Load bank component specifications

Component	Rating	Component Value	Connection Type
Resistor	2 kW	21.6Ω	3-phase Y
Resistor	1 kW	43.3 Ω	3-phase Y
Resistor x 3	0.5 kW	28.8 Ω	1-phase
Reactor	2 kvar	57 mH	3-phase Δ
Reactor	1 kvar	115 mH	3-phase Δ
Reactor x 3	0.5 kvar	76 mH	1-phase
Capacitor	2 kvar	3x38 μF	3-phase Δ
Capacitor	1 kvar	3x19 μF	3-phase Δ
Capacitor x 3	0.5 kvar	92.0 μF	1-phase
CFL x 9	68W	N/A	A, B, C

In addition to the loads internal to the lab workbench and the permanently fixed connection to the MCC, a requirement of the design was that the lab workbench must be modular to allow for the inclusion of other external projects. To accomplish this, 15 external female receptacles were selected such that a variety of loads could be supplied by the bench. Specifically, 2 duplex 1-phase

receptacles were mounted per phase at 20A rated current. Three, 3-phase receptacles were additionally added, one rated for 30A and the others for 20A.

5.2.2 Load Requirements and Specifications

Essential to the design of the lab workbench was to provide clear and accurate metering for the user. With the configurable nature of the lab workbench itself, a need arose for the ability to measure both the standard internal components as well as any auxiliary loads. To satisfy both these needs, two separate metering devices and strategies were employed. To monitor the internal loads, a 2000 Series Power Xpert Meter was permanently mounted to the control panel [51]. It was connected via fixed current transformers (CTs) around the main incoming power to the lab workbench, along with fuse-protected voltage leads to the same point. This meter provides data on current and voltage, real and reactive power, power factor, harmonic distortion, and more, at a 6 MHz sampling rate. All of this data will be available both to the users at the bench, as well as via webpages through an Ethernet connection to the laboratory's network.

However, simply monitoring the main power flowing into each bench may not be sufficient when additional loads are connected. Therefore, an additional metering strategy was developed, which employs portable power quality meters. To enable their use, a system of current loops was developed wherein each of the four load banks had four current loops on the main control panel. Thus, the current of phases A, B, C and neutral for each of the loads within the bench could be monitored independently using portable clamp-on CTs. Additional loops could be added to any of the auxiliary loads connected to the lab workbench in order to acquire any external data. Banana jacks were added for safe and simple voltage connections to the bench. The data can be uploaded

to any network-connected computer within the laboratory in order to supplement any other data collected.

5.2.3 Manual and Digital Control

Advanced control was implemented for the lab workbench, allowing users to either manually or digitally control any element. This was achieved via a control panel on the front of the lab workbench with hand-off-auto switches for each of the elements – 5 resistors, 5 reactors, 5 capacitors, and 9 CFLs. For educational experimental use, the manual controls will primarily be used, allowing students to gain a much greater understanding of the state of the system and the interactions occurring at any given point in time. However, manual control of components would not be sufficient for research purposes, as more responsive controls are needed.

To satisfy this need, digital control was provided to the lab workbench via a XV100 series HMI-PLC [52]. This particular device provides a powerful touch-screen controller capable of running advanced control algorithms in addition to a wide array of communication abilities. The capabilities of the controller are more than sufficient for the switching of any of the devices internal to the lab workbench, while having enough capacity to drive any other projects connected to the bench.

Communications between the lab workbench and the PLC are achieved via SmartWire-DT, a wired communication bus. SmartWire-DT allows up to 100 devices, such as sensors, relays, switches, contactors, breakers, motor controls and more, to be connected along the same wire with all of the data fed back to the central PLC. This will allow for easy expansion and reconfiguration of the control structure for the lab workbench. SmartWire-DT also allows for any external projects to be tied directly into the same communications bus.

In addition to using SmartWire-DT for internal control, the PLC will have the capability of communicating fluidly with any of the other PLCs and the network within the laboratory. This communication can be achieved through a variety of options provided by the PLC. These include Ethernet, CANopen, Modbus and USB, in addition to the SmartWire-DT itself. This inter-bench communication will provide the laboratory with the capability to perform Smart Grid and Microgrid experiments and demonstrations. It will also allow for experiments on remote monitoring and control with the introduction of time delay between the benches.

5.2.4 Safety

An essential concern was the need to ensure the safety of the students and researchers who would be using the equipment. In doing so, many factors were considered. First, the system needed to be protected in terms of the electrical disturbances internal to the lab workbench itself. Protection from faults within the lab workbench was achieved through the layout of circuit breakers for each load and each external connection. The incoming 208V, 3-phase power was protected with a 60A breaker, sufficient for more than the maximum amount of current that could be drawn by the bench. Each of the load banks was then protected with a 20A breaker for potential faults occurring on the loads. The external loads were protected with breakers matching their outlet ratings as described above. The MCC was protected with a 30A breaker. These breakers were mounted within the lab workbench where the incoming power would be delivered. This would allow the student or researcher the ability to turn on those loads required by their research, as well as allowing 3-phase power to be cut completely from the lab workbench.

In addition to fault protection, other key safety features were implemented. An emergency stop circuit was added, which consisted of a 120V, 1-phase circuit which could be broken by pressing

an E-Stop button on the bench. When pressed, an undervoltage release would open the main circuit breaker for the lab, causing not only the lab workbench, but the entire laboratory to safely shut down. Thus, in the event of an emergency situation, no laboratory elements would still be live. In addition to the emergency stop, the lab workbench was illuminated with stack lighting, such that when the control power was activated a green light would turn on and when the main power was activated a red light would turn on. In doing so, a clear and easily visible means of identifying which benches were live was established.

5.3 PROTOTYPE AND REALIZATION

This section explores the physical construction of the lab workbench as well as its custom design features. Based upon the design described in section II, a prototype lab workbench was built. The construction of this prototype demonstrated the feasibility of the desired design and provided the template for the final production models. That template was then realized in a manufacturing facility, resulting in six professional-grade lab workbenches as shown in Figure 60.

5.3.1 External Construction

The external construction of the prototype provided laboratory workspace, while including the electrical components inherent to its design. The lab workbench is a mobile 4ft. x 8ft. x 40inch box. The prototype was constructed using angle iron brackets and plywood by the University of Pittsburgh, while the final product comprised of steel and was built by RAM Industrial. This

workbench is mounted on six wheels to allow for easy mobility for reconfiguring the laboratory. The working surface of the workbench is a clear top made of $1/2$ inch scratch-resistant acrylic.

The control panel is mounted on the front face of the workbench. Placed on this control panel are the hand-off-auto switches, current loops, voltage connections, and power quality meter, all of which are described in Section 5.2. A detailed view of this panel is shown in Figure 61. Recessed into this panel is the touchscreen HMI-PLC. Affixed to the right side of the workbench are the mast, emergency stop trigger, breaker panel, and auxiliary outlets. The mast is a vertically mounted wire conduit for the purpose of safely connecting the lab workbench to overhanging cable tray from the IFS. The mast additionally includes the stack light, indicating the power status of the workbench. The mast feeds directly into the breaker panel, from which all of the loads are fed.

5.3.2 Interior Construction

The resulting workbench has the unique capability of reconfiguring and adjusting to meet undergraduate and graduate needs. Another benefit of this workbench is its compact nature achieved by combining power equipment and workspace into a central unit. This helps to maximize use of limited lab space.

Inside the workbench, the electrical elements include resistive, capacitive, inductive, and CFL loads. These loads were mounted in a unique way with the intent of simplifying access and maintenance. Rather than permanently fixing the loads to the interior, they were collectively placed on a panel which could be easily slid from the workbench, as demonstrated in Fig. 4. Also interior to the workbench are two fans for ventilation and cooling of the elements that will generate heat, primarily the resistor and CFL loads. The fans circulate the air-flow to maintain stable operating temperatures. A top view of the interior is shown in Fig. 5.

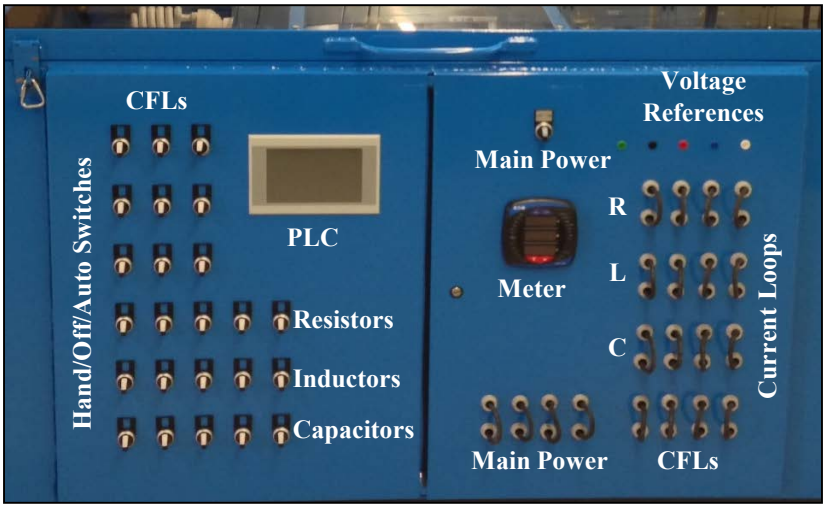


Figure 61. Detailed view of the front control panel.

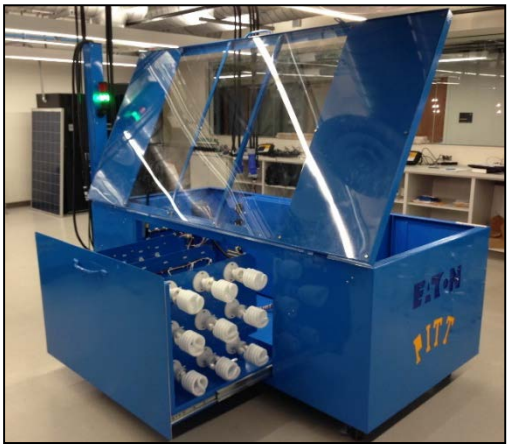


Figure 62. Exploded perspective of the manufactured workbench.

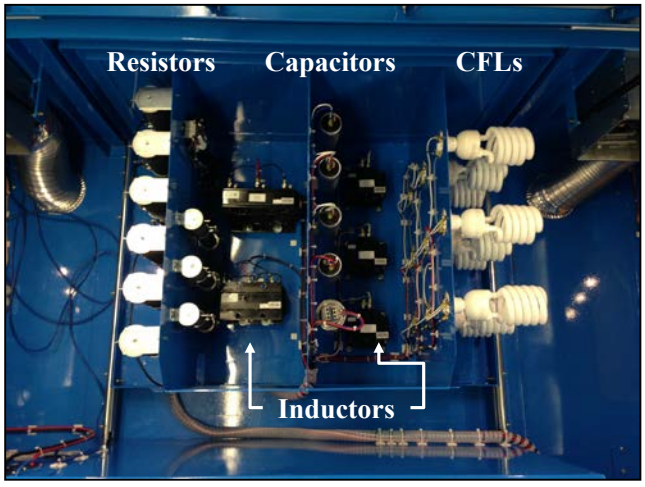


Figure 63. Internal top-down view of workbench

5.4 LABORATORY CAPABILITIES AND PLANNED ACTIVITIES

Starting in 2007, an electric power engineering concentration was developed at the undergraduate level. Prospective students must take two required core courses and have the option of selecting two electives. The two required courses include Power System Engineering & Analysis I and Linear Control Systems. In Power System Engineering & Analysis I, students learn the fundamentals of three-phase power, power transformers, transmission line modeling and design, symmetrical components, and elementary power flow analysis. In linear control systems, system stability is strongly emphasized with methods for predicting instability and core design fundamentals for PID controllers. The electives at the undergraduate level include Electric Machines with an associated machines lab component; Power Generation, Operation, & Control; Electrical Distribution Engineering and Smart Grids; Construction and Cost of Electrical Supply; Power Electronics; Thermodynamics; and Introduction to Nuclear Engineering.

In order to expand upon the existing undergraduate curriculum, new laboratory courses are being developed to take advantage of both the new power systems laboratory (completed by the spring of 2014) and the lab workbenches emphasized throughout this work. Traditionally, Power Systems Analysis & Design is offered every fall term, thus, a natural transition would be to offer a hardware-based course in the spring term emphasizing realization of theoretical concepts and practices. Laboratory experiments are currently being developed to fulfill this role, utilizing the benefits of the lab workbench design. Table 14 provides a list of these planned experiments, as well as the laboratory equipment to be used in each. The topics planned to be covered span the applications of power electronics, smart grid, energy storage, renewable energy, and power quality. Again, a strong benefit of this lab workbench design is its versatility and applicability to a variety

of experiments. Courses will be available at the University of Pittsburgh, Swanson School of Engineering at both the undergraduate and graduate levels in the coming years.

Table 14. List of experiments for the electric power systems laboratory and the equipment to be used

(A)	Laboratory Workbench
(B)	Motor Control Centers
(C)	5-hp Motors
(D)	15-hp Motors
(E)	Photovoltaic Inverter
(F)	Uninterruptable Power Supply
(G)	Natural Gas Generator
(H)	High Impedance Source
(I)	Sag Generator

No.	Experiment	Equipment Used
1)	Safety Training and Metering/Monitoring Orientation	A, B, C, D, E, F, G, H, I
2)	Variable Frequency Drives	A, B, C, G, H, I
3)	Motors/Soft Starting	A, B, D, G, H, I
4)	UPS/Conversion	A, B, C, D, F, I
5)	Solar Energy Integration and Inverters/Balance-of-System	A, B, C, D, E, H
6)	Wind Energy Integration and Inverters/Balance-of-System	A, B, C, D, H
7)	Power Factor Correction	A, B, C, D
8)	Programmable Logic Controller (PLCs) and Industrial Controls	A, B, C, D, E, F
9)	Distribution Relaying and Protection/SKM	A, E, G, I
10)	Transformer and Cable Losses	A, H
11)	Battery and Energy Storage Systems	A, E, F
12)	Lightning	A
13)	Home Automation and Smart Outlets/Breakers	A
14)	Power Quality – Sags, Swells, Harmonics	A, B, C, D, H, I
15)	Advanced Metering	A, B, C, D, E, F, G, H, I

5.5 DEMONSTATION OF PLANNED LABORATORY EXPERIMENTS

In this section we will explore the capabilities of the lab workbench with the purpose of showing how this design is fitting for the planned experiments listed in Table 14. Experiments were

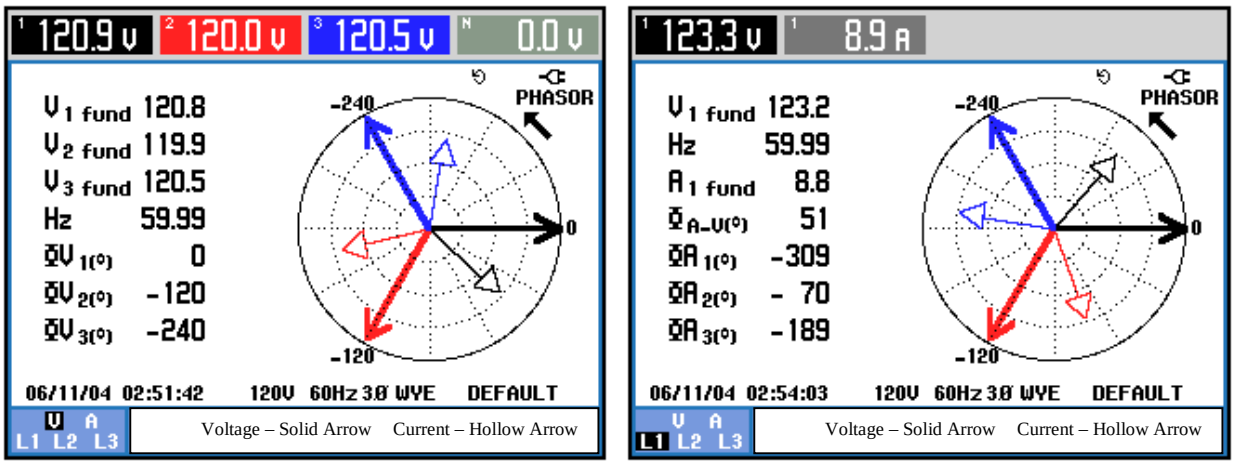
performed with the workbench to demonstrate power factor adjustment, create transient events, generate harmonic content and drive a motor. An example of an experimental setup within the electric power systems laboratory is shown in Figure 64. These demonstrations have been performed with the workbench, producing expected textbook results as shown in Figure 65 through Figure 67.

Figure 64. Experimental setup for testing and validation of motor loads.

The first experiment to be discussed is power factor adjustment, experiment 7 from Table 14. With the utilization of the reactive and capacitive load banks integrated into the workbench, power factor adjustment can be demonstrated. Figure 65 presents phasor diagrams showing the capability to phase shift the current from being in phase with the voltage reference using reactive elements. At reference, phase A has an angle of 0°, phase B an angle of 240°, and phase C an angle

of 120°. As seen in Figure 65(a) , the phase of the current has been shifted approximately 40° from the reference, lagging, because reactance was introduced into the system. When capacitance is added into the system instead of reactance, the phase is shifted such that the current leads the voltage. A positive phase shift of approximately 50° caused by the capacitance is shown in Figure 64(b). By switching reactors and capacitors within the bench, different levels of phase shift can be achieved. This demonstration will allow undergraduate students to achieve a stronger understanding of how power factor is altered through system changes in inductive or capacitive load adjustments. Fundamental power factor correction concepts are thoroughly covered in undergraduate curriculum using [53].

For the second experiment, a DC trapped charge transient was created to simulate a breaker restrike on a capacitor bank. This classic example is covered in graduate level electric power system transients courses offered at the university, and is a component of experiment 9 from Table 14. Using the PLC, the capacitive load bank was brought to full charge, disconnected, and then reconnected 5 cycles later. This procedure results in a switching transient. The voltage waveform of this transient is shown in Figure 66. In theory, a trapped charged transient event creates a two per unit voltage transient due to the mismatch in energy between the capacitor bank and line side. Two per unit voltage is expected if and only if the capacitor switched on a voltage peak and no damping exists in the circuit [54]. As seen in Figure 66, the reclosing of the capacitor bank within the lab workbench created a transient with a smaller than ideal magnitude due to conditions explained previously.



(a) **(b)**

Figure 65. Phasor diagram of the three phase power on the lab workbench with (a) reactive and (b) capacitive load

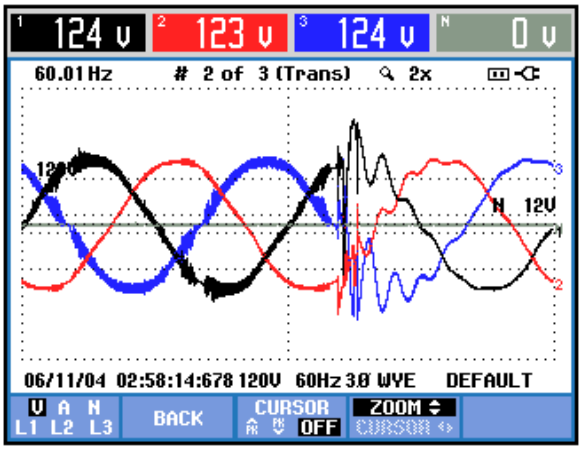


Figure 66. Trapped charge voltage transient on the capacitor bank

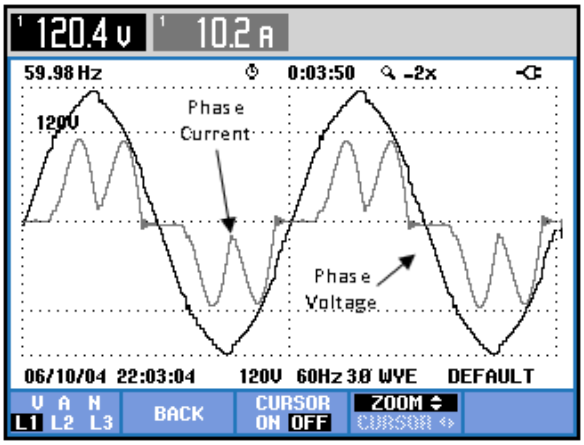


Figure 67. Current and voltage waveforms associated with phase A of the VFD

5.6 LABORATORY WORKBENCH STUDENT ASSESSMENT

During the summer of 2014, the laboratory facility was used for the first time to aid undergraduate education in a course entitled, Distribution Circuits and Smart Grids. This course has been offered every summer since 2009, co-taught with Eaton engineers, and has traditionally only had a lecture component associated with the course. This year, with typically lower enrollment in summer courses, 18 undergraduate students with limited background in power engineering were exposed to three newly developed laboratory exercises in addition to the traditional curriculum of the summer course. The designed labs were focused upon safety training and metering/monitoring orientation (No.1), power factor correction (No.2), motor starting and variable frequency drives (No.3), and power quality analysis (No.1 through 3).

Power Factor Correction Lab: To expose students to three-phase systems, a pre-lab was first designed where students would calculate various electrical characteristics and attempt to draw phasor diagrams for three-phase circuits that were purely resistive, purely inductive, purely capacitive, and mixed based upon the theory that was covered in the classroom. The pre-lab consisted of five main problems with multiple parts to each question. The following week, students performed a series of experiments that reflected the problems solved as part of the pre-lab.

Working in groups of three, students used the designed workbench to quickly alter system loads and used the portable power quality meters to take various measurements (rms voltages, rms currents, real and reactive power, power factor, and harmonic currents) and to observe the meter generated phasor diagrams. Students were then required to type and submit full lab reports, detailing the procedure they followed, the results they obtained, and the resulting conclusions drawn from each of the labs.

Table 15. Questionnaire and survey results for power factor correction lab no. 2
Very Poor – 1; Poor – 2; Fair – 3; Good – 4; Excellent – 5

	Lab Design	Student Average Rating
1.	The course materials (lecture material, pre-lab, and lab instructions) were appropriate for my knowledge level.	4.44 / 5.0
2.	The homework exercises, labs and activities helped me understand the course material.	4.56 / 5.0
3.	My participation in this lab was encouraged and enhanced my understanding of the course material.	4.22 / 5.0
4.	Evaluate the technical quality of the lab.	4.72 / 5.0
5.	Evaluate the organization of the lab procedures. Did the lab logically make sense from beginning to end?	4.44 / 5.0
6.	How was the lab pace? Did you feel you had adequate time to perform the required tasks?	4.56 / 5.0
7.	Overall, I would rate this first lab as:	4.61 / 5.0
	Learning Effectiveness	**Student Average Rating**
8.	The bench design provided an adequate visual of power system components.	4.61 / 5.0
9.	The bench design is easy to use including meters for quickly measuring desired electrical quantities.	4.50 / 5.0
10.	Using various knobs to adjust loads, the bench metering equipment enhanced my understanding of leading / lagging concepts.	4.67 / 5.0
11.	As an introduction, did this lab increase your knowledge of three-phase power?	4.61 / 5.0
12.	I would recommend this lab to peers who haven't taken ECE1710.	4.56 / 5.0

Following their first laboratory experiment, students were required to fill out a 16 question survey. The first 12 questions of the survey and average results based on a 5 point scale are included in Table 15. For the remaining 4 questions, students were asked to comment on the effectiveness of the bench design in aiding their understanding of power system fundamentals. This quote samples the student experience:

"I really liked how simple it was to understand what was going on in the bench, as well as how simple it was to work the bench (e.g. no manual or elongated head-scratching was needed). This really allowed for more time to understand what was actually going on within the bench (i.e. more time to think about the effects on power/voltage/current as the load was varied), rather than trying to figure out how to work the bench. It really helps aid education in visualizing the concepts in real-time."

Motor Starting/Variable Frequency Drives (VFD): First, students were exposed to machine nameplate ratings and the principles of across the line starting and soft starting of induction motors. High emphasis was placed on understanding soft starter topologies and their

impacts on motor inrush currents compared to currents developed with across the line starting of motors. To reinforce conceptual learning, live demonstrations were given by the instructor of motor startups for both scenarios while differentiating the difference thru sound. Demonstrations included measuring the motor inrush currents using the Power Xpert meter installed in the MCC and projecting measured visuals for the whole class.

Second, the laboratory is equipped with 6 variable frequency drive units interfaced to the laboratory benches via each MCC. Students learned the purpose of variable frequency operation by tabulating electrical quantities (V_{LL}, I_L, P) and motor speed as the output frequency of the VFD varied in 0.25 Hz increments from 60 to 61.5 Hz to quantify the relationship between motor speed, motor loading, input current, and slip percentage.

5.7 CONCLUSION

The construction of a new power systems laboratory has been undertaken. This aligns with the established goals of training the next generation of power systems engineers and enabling cutting edge research within the field. In addressing the goals for the laboratory it was determined that an innovative lab workbench would be necessary in order to create an extremely versatile work area while conserving space. To this end a novel lab workbench was brought from concept to design to prototype to professional grade construction, and was vigorously tested to ensure its laboratory capability.

The design process focused on the integration of a load bank with advanced metering and control into a workstation that flowed seamlessly with its surrounding environment, while emphasizing the safety of students and researchers. The design was then realized as a fully

functional prototype of the system. In addition, aesthetic elements which highlight its functionality were created to excite prospective students.

The planned experiments for the laboratory were laid out, the functionality of the lab workbench in terms of each of those was demonstrated through extensive testing, and a few lab exercises were conducted in the university setting with student assessments provided. The end result is a lab workbench which will enable a wide variety of research and education to take place in a rapidly reconfigurable setting.

6.0 CONCLUSION

This thesis has examined the design, operation, testing and evaluation of PV panels and the requisite converters for PV grid connection. Considerations regarding system transients, maximum power point tracking, modular multilevel conversion, and testbed development have been presented, painting a complete picture of the PV system as required for proper operation in either islanded or grid-connected modes. The application of wide bandgap semiconductor devices was discussed, with emphasis on the reduction of power electronic converter sizes and improved performance at high frequencies. The overall unifying theme is a new generation of power electronics devices and converters, enabling the integration of PV generation to power systems at an unprecedented rate. This integration help to shift global power generation away from fossil fuels and towards renewables, preserving the precious resources of the planet.

Various topics were investigated throughout the thesis, covering the complete array of PV system elements and requirements. First, the transient phenomena during the turn-on of WBG semiconductors was examined in the case of the synchronous buck converter. The equivalent circuit was analyzed, with a focus on the occurrence of false turn-on. Mathematical models were developed using both frequency domain and state space analysis in order to accurately model the system transients at the time of turn-on. Next, a boost converter with MPPT implemented using RCC was examined. A model for the PV panel was created, accurately representing a PV panel in the simulated circuit. The system was shown to accurately track and rapidly converge to the MPP of the system. In Chapter 4, an inverter system was developed for PV integration based the half H-bridge MMC architecture. This inverter was shown to produce near sinusoidal output with minimal filtering requirements. Finally, the development of a new laboratory workbench for load

emulation was presented as a testbed environment with which the power electronics systems could be evaluated. The capabilities of the laboratory workbench for both undergraduate education and graduate research activities were presented, and the importance of testbed development was demonstrated.

In demonstrating the complete PV system, this Thesis has provided insight into some of the considerations that must be taken into account in order for PV generation to become a higher percentage of the generation mix. This is crucially important for the future of power generation, as environmental and economic concerns will eventually force reductions in the use of fossil fuels. As the grid matures, and more and more countries around the world begin to develop towards modern power consumption, the global demand for power will overwhelm the limited reserves of fossil fuels. Prices will increase and availability will decrease, especially if the status quo is maintained in the generation mix. PV, wind, and other renewable energy sources are the power generators of the future, and significant improvements will be required in order to achieve a sustainable globe. This Thesis takes a small stab at examining some challenges associated with the integration of PV generation, and some of the solutions to those challenges. In solving them, and so many of the other challenges that exist, a path can be paved towards using PV for renewable, sustainable power generation for the future.

7.0 FUTURE WORK

Future work will include deeper investigation of small energy switching converters – relying on small, efficient, WBG semiconductor devices to create high power converters using man small switching events. Targets for such research activities include high power DC-DC and DC-AC conversion. Emphasis will be placed on achieving extremely high power density in converter systems, allowing for the creation of small converter handling huge amounts of power. Beyond that, the thermal characteristics of WBG semiconductors promise to provide avenues for minimal heat sink requirements, providing high power converters in extremely small packages that run at relatively cool temperatures. These systems will be modeled, evaluated, designed, and constructed, creating a new generation of power electronics converter systems.

APPENDIX

FORTRAN CODE FOR CAPACITOR BALANCING ALGORITHM

A.1 FORTRAN CODE FOR SORTING BLOCK

```
 #LOCAL REAL V 30
#LOCAL REAL S 30
#LOCAL INTEGER N
#LOCAL INTEGER I
#LOCAL INTEGER J
#LOCAL REAL TEMP
#LOCAL INTEGER TEMPS
#LOCAL INTEGER IMIN
!
S(1) = 1
S(2) = 2
S(3) = 3
S(4) = 4
S(5) = 5
S(6) = 6
S(7) = 7
S(8) = 8
S(9) = 9
S(10) = 10
!
V(1) = $Vin1(1)
V(2) = $Vin1(2)
V(3) = $Vin1(3)
V(4) = $Vin1(4)
V(5) = $Vin1(5)
V(6) = $Vin1(6)
V(7) = $Vin1(7)
V(8) = $Vin1(8)
V(9) = $Vin1(9)
V(10) = $Vin1(10)
!
N = 10
```

```
DO J = 1, N
      IMIN = J
      Do I = J, N
         IF (V(I)<V(IMIN)) THEN
             IMIN = I
         END IF
      END DO
      IF (IMIN/=J) THEN
         TEMP = V(J)
         V(J) = V(IMIN)
         V(IMIN) = TEMP
         TEMPS = S(J)
         S(J) = S(IMIN)
         S(IMIN) = TEMPS
     END IF
END DO
!
$Ssort(1)=S(1)
$Ssort(2)=S(2)
$Ssort(3)=S(3)
$Ssort(4)=S(4)
$Ssort(5)=S(5)
$Ssort(6)=S(6)
$Ssort(7)=S(7)
$Ssort(8)=S(8)
$Ssort(9)=S(9)
$Ssort(10)=S(10)
```

A.2 FORTRAN CODE FOR SELECTION BLOCK

```
#LOCAL INTEGER Sout 30
#LOCAL INTEGER LEN
#LOCAL INTEGER J
#LOCAL INTEGER P
!
Sout(1) = 0
Sout(2) = 0
Sout(3) = 0
Sout(4) = 0
Sout(5) = 0
Sout(6) = 0
Sout(7) = 0
Sout(8) = 0
Sout(9) = 0
Sout(10) = 0

LEN = 10
!
IF ($Idc > 0) THEN
!
```

```
    DO J = 1, $N
    !
        P = $Sin(J)
        Sout(P) = 1
    END DO
ELSE
!
    DO J = (LEN-$N+1), LEN
        P = $Sin(J)
        Sout(P) = 1
    END DO
END IF
$S1(1)=Sout(1)
$S1(2)=Sout(2)
$S1(3)=Sout(3)
$S1(4)=Sout(4)
$S1(5)=Sout(5)
$S1(6)=Sout(6)
$S1(7)=Sout(7)
$S1(8)=Sout(8)
$S1(9)=Sout(9)
$S1(10)=Sout(10)
```

BIBLIOGRAPHY

[1] T. Bruckner and P. K. Steimer, "The Active NPC Converter for Medium-Voltage Applications," in Industry Applications Conference, 2005.

[2] B. Hughes, J. Lazar, S. Hulsey, D. Zehnder and K. Boutros, "GaN HFET Switching Characteristics at 350V/2A Synchronous Buck Converter Performance at 1MHz," in Applied Power Electronics Conference, Orlando, Fl, 2012.

[3] Y.-F. Wu, R. Coffie, N. Fichtenbaum, Y. Dora, C. S. Suh, L. Shen, P. Parikh and U. K. Mishra, "Total GaN Solution to Electricity Power Conversion," IEEE 69th Device Research Conference, pp. 217-218, 2011.

[4] D. Grider and e. all, "Advanced SiC Power Technology for High Megawatt Power Conditioning," CREE, 2012.

[5] A. Mantooth, M. D. Glover and P. Shepherd, "Wide Bandgap Technologies and Their Implications on Miniaturizing Power Electronics Systems," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 3, pp. 373-385, 2014.

[6] R. Khanna, Q. Zhang, W. E. Stanchina, G. F. Reed and Z.-H. Mao, "Maximum Power Point Tracking Using Model Reference Adaptive Control," IEEE Transactions on Power Electronics, vol. 29, no. 3, pp. 1490-1499, 2014.

[7] P. K. A. Bazzi, "Ripple Correlation Control: An Extremum Seeking Control Perspective for Real-Time Optimization," IEEE Transactions on Power Electronics, vol. 29, no. 2, pp. 988-995, 2014.

[8] M. Saeedifard and R. Iravani, "Dynamic Performance of a Modular Multilevel Back-to-Back HVDC System," IEEE Transactions on Power Delivery, vol. 25, no. 4, pp. 2903-2912, 2010.

[9] M. Gurfunkle, H. D. Xiong, K. P. Cheung, J. S. Suehle, J. B. Bernstein, Y. Shapira, A. J. Lelis, S. Haberstat and N. Goldsman, "Characterization of Transient Gate Oxide Trapping in SiC MOSFETs Using Fast I-V Techniques," IEEE Transactions on Electron Devices, vol. 55, no. 8, pp. 2004-20012, 2008.

[10] Z. Liu, X. Huang, F. C. Lee and Q. Li, "Package Parasitic Inductance Extraction and Simulation Model Development for the High-Voltage Cascode GaN HEMT," IEEE Transactions on Power Electronics, vol. 60, no. 2, pp. 1977-1985, 2014.

[11] R. Khanna, A. A. Amrhein, W. E. Stanchina, G. F. Reed and Z.-H. Mao, "An Analytical Model for Evaluating the Influence of Device Parasitics on Cdv/dt Induced False Turn-On in SiC MOSFETs," in Applied Power Electronics COnference, Long Beach, CA, 2013.

[12] A. Lemmon, M. Mazolla, J. Gafford and C. Parker, "Stability Considerations for Silicon Carbide Field-Effect Transistors," IEEE Transactions on Power Electronics, vol. 28, no. 10, pp. 4453-4459, 2013.

[13] G. Suman, P. Kumar, S. Kumar, C. Babu and K. R. Subhashini, "Modeling, Analysis and Design of Synchronous Buck COnverter using State Space Averaging Technique for PV Energy System," in International Symposium on Electronic System Design, 2012.

[14] M. Rodriguez, A. Rodriguez, P. F. Miaja, D. G. Lamar and J. S. Zuniga, "An Insight into the Switching of Power MOSFETs: an Improved Analytical Losses Model," IEEE Transactions on Power Electronics, vol. 25, no. 6, pp. 1626-1640, 2010.

[15] Y. Ren, M. Xu, J. Zhou and F. C. Lee, "Analytical Loss Model of Power MOSFET," IEEE Transactions on Power Electronics, vol. 21, no. 2, pp. 310-319, 2006.

[16] Efficient Power Conversion, "EPC 2007".

[17] A. Lemmon, M. Mazzola, J. Gafford and C. Parker, "Instability in Half-Bridge Circuits with Wide Bandgap Transistors," IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2380-2392, 2014.

[18] T. Wu, "Cdv/dt Induced Turn-on in Synchronous Buck Regulators," 2007.

[19] Q. Zhao and G. Stojcic, "Characterization of Cdv/dt Induced Turn-on in Synchronous Buck DC-DC Converters," IEEE Transactions on Power Electronics, vol. 22, no. 4, pp. 1508-1513, 2007.

[20] R. Burra, S. Mazumeder and R. Huang, "DV/DT Related Spurious Gate Turn-on of Bidirectional Switches in High Frequency Cycloconverter," IEEE Transactions on Power Electronics, vol. 20, no. 3, pp. 1237-1243, 2005.

[21] Powerex, Powerex SiC MOSFET Datasheet.

[22] D. K. a. A. P. H. N. Nagaraja, "Design Principles of a Symmetrically Coupled Inductor Structure for Multiphase Synchronous Buck Converters," IEEE Transactions on Industrial Electronics, vol. 58, no. 3, pp. 988-997, 2011.

[23] X. L. a. W. S. S. Xu, "Modeling of Power Metal-Oxide Semiconductor Field-Effect Transistor for the Analysis of Switching Characteristics in Half-Bridge Converters," IET Circuits, Devices & Systems, vol. 4, no. 4, pp. 327-336, 2010.

[24] T. D. a. R. E. T. Tolle, "Switching Loss Contributions of Synchronous Rectifiers in VRM Applications," in Proceedings of the 34th Anual IEEE Power Electronics Specialist Conference, Acapulcu, Mexico, 2003.

[25] B. Y. a. J. Zhang, "Effect and utilization of common source inductance in synchronous rectification," in Proceedings of the 25th Annual IEEE Applied Power Electronics Conference and Exposition, Austin, Texas, USA, 2005.

[26] Vishay, "Vishay Si MOSFET Datasheet".

[27] Powerex, "Powerex SiC MOSFET Datasheet," [Online]. Available: www.pwrx.com/pwrx/docs/qjd1210007.pdf.

[28] H. M. a. A. A. K. Ammous, "Analysis of power switching losses accounting probe modeling," IEEE Transactions on Instrumentation and Measurement, vol. 59, no. 12, pp. 3218-3226, 2010.

[29] M. L. T. K. a. A. D. A. R. A. Mastromauro, "A Single Phase Voltage-Controlled Grid-Connected Photovoltaic System with Power Quality Conditioner Functionality," IEEE Transactions on Industry Electronics, vol. 56, no. 11, pp. 4436-4444, 2009.

[30] B. Z. D. J. A. M. A. Elgendy, "Assessment of Perturb and Observe MPPT Algorithm Implimentation Techniques for PV Pumping Applications," IEEE Transactions on Sustainable Energy, vol. 3, no. 1, pp. 21-33, 2012.

[31] R. T. H. Kumar, "Simulation of Variable Incremental Conductance Method with Direct Control Method Using Boost Converter," in Student Conference on Engineering and Systems, 2012.

[32] P. C. T. Ersam, "Comparison of Photovoltaic Array Maximum Power Point Tracking Techniques," IEEE Transactions on Energy Conversion, vol. 22, no. 2, pp. 439-449, 2007.

[33] J. W. K. P. T. K. P. L. C. a. P. M. T. Esram, "Dynamic Maximum Power Point Tracking of Photovoltaic Arrays Using Ripple Correlation Control," IEEE Transactions on Power Electronics, vol. 21, no. 5, pp. 1284-1291, 2006.

[34] P. T. Krein, "Ripple correlation control, with some applications," in Proceedings of the IEEE International Symposium on Circuits and Systems, 1999.

[35] R. C. Campbell, "A Circuit-based Photovoltaic Array Model for Power System Studies," in North American Power Symposium, 2014.

[36] M. Korytowski, Comparative Analysis of Medium Voltage DC and AC Network Infrastructure Models, Pittsburgh, PA: University of Pittsburgh MS Thesis, 2011.

[37] CanadianSolar, "CS6P Panel Datasheet," [Online]. Available: www.canadiansolar.com.

[38] A. Yazdani, A. R. Di Fazio, H. Ghoddami and M. Russo, "Modeling Guidelines and a Benchmark for Power System Simulation Studies of Three-Phase Single-Stage Photovoltaic Systems," IEEE Transactions on Power Delivery, vol. 26, no. 2, pp. 1247-1264, 2011.

[39] G. F. Reed, B. M. Grainger, H. Bassi, Z.-H. Mao and A. K. Jones, "Analysis of High Capacity Power Electronics Topologies for Intergration of Green Energy Management," in IEEE PES T&D 2010, 2010.

[40] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 37-53, 2015.

[41] M. Kasper, D. Bortis, J. W. Kolar and G. Deboy, "Hyper-Efficient (98%) and Super-Compact (3.3kW/dm3) Isolated AC/DC Telecom Power Supply Module based on Multi-Cell Converter Approach," in IEEE ECCE, 2014.

[42] M. Saeedifard and R. Irvani, "Dynamic Performance of a Modular Multilevel Back-to-Back HVDC System," IEEE Transactions on Power Delivery, vol. 25, no. 4, pp. 2903-2912, 2012.

[43] G. F. Reed, "The University of Pittsburgh Swanson School of Engineering Power & Energy Initiative: Building Engineering Education and Research Partnerships through Academic-Industry Collaboration," IEEE Power and Energy Magazine, vol. 6, no. 2, 2008.

[44] R. Balog, Z. Sorchini, J. Kimball, P. Chapman and P. Krein, "Modern Laboratory Based Education for Power Electronics and Electric Machines," IEEE Transactions on Power Systems, vol. 20, no. 2, pp. 538-547, 2005.

[45] C. Sanghun and M. Saeedifard, "An Educational Laboratory for Digital Control and Rapid Prototyping of Power Electronic Circuits," IEEE Transactions on Education, vol. 55, no. 2, pp. 263-270, 2012.

[46] E. T. Gross and C. M. Summers, "Approach to Experimental Electric Power Engineering Education," IEEE Transactions on Power Apparatus and Systems, Vols. PAS-91, no. 5, pp. 1773-1780, 1972.

[47] A. Emadi, "Grainger power electronics and motor drives laboratories at Illinois Institute of Technology," in IEEE PES General Meeting, 2005.

[48] Eaton, "Power Systems Experince Center," [Online]. Available: www.eaton.com/experience.

[49] Hampden Engineering Corporation, "Electrical Engineering Labs and Layouts," [Online]. Available: http://www.hampden.com.

[50] Lab-Volt Systems, Inc., "Engineering Education & Research Equipment for the 21st Century," [Online]. Available: http://www.labvolt.com.

[51] Eaton, "Power Xpert Meter 2000 Series: Technical Data TD0201017E," 2011. [Online].

[52] Eaton, "The Integrated HMI-PLC: Industry Application IA05003001E," 2012. [Online].

[53] J. D. Glover, M. S. Sarma and T. J. Overbye, Power System Analyis and Design, 4th Edition, Thomas Learning, 2008.

[54] A. Greenwood, Electrical Transients in Power Systems, 2nd edition, Wiley, 1991.