EFFECTS OF THE PHASE LOCKED LOOP ON THE STABILITY OF A VOLTAGE SOURCE CONVERTER IN A WEAK GRID ENVIRONMENT

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B.S., University of Pittsburgh, 2009

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Submitted to the Graduate Faculty of

the Swanson School of Engineering in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

University of Pittsburgh

2014

UNIVERSITY OF PITTSBURGH

SWANSON SCHOOL OF ENGINEERING

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Distributed generation is characterized as a form of generation that is not directly connected to the bulk transmission grid. It is usually connected via power electronic devices if it is a renewable resource, in this case in the form of a voltage source converter (VSC) operating as an inverter (converting DC-to-AC). The grid impedance connected to the VSC has an influence on its stability and control performance. By looking at the output impedance of the VSC, the stability can be determined in relation to the impedance of the grid connection. A number of parameters influence the output impedance of a VSC, one of those being the control scheme used and the phase-locked loop (PLL) contained within it.

The control parameters of the PLL can be adjusted to manipulate the location of the calculated poles and zeros of the open loop output impedance of the VSC. These parameters are the gains of the loop filter, K_p and K_i. Under certain short circuit ratio (SCR) values, having large PLL gain parameters can cause the VSC to become unstable. While a large SCR will be unaffected by the PLL gains, a smaller SCR is more susceptible to PLL gains that are too large. By accounting for the effects of the PLL in the output impedance, it can be found what PLL gains are considered too large for certain SCR values.

A large enough grid impedance can destabilize the VSC and, therefore, cause the renewable generation to be disconnected and unused. Ideally, the output impedance of the VSC will be large. This work analyzes the effect of the PLL on the output impedance of the VSC and ultimately the stability and control performance based on different grid impedances.

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ACKNOWLEDGEMENTS

I would like to thank my parents, Edward and Dedrea, my two sisters, Sara and Lindsey, and my girlfriend, Karen, for their unending support of me through the process of completing this work. Without them, finishing this work would have been much more difficult. They have my utmost gratitude and thanks.

I would also like to thank all of my friends in the research lab and outside as well. In no particular order: Alvaro, Brandon, Pat, Ansel, Hashim, Steve, Chris, Devin, and Steve. They were always there to help me talk through any problems I was running into or to have technical discussions in regards to the work I was doing. They helped to make an environment that was a pleasure to work in and a space to help with the creation of new ideas and research.

Lastly, I would like to thank my advisor, Dr. Reed, and committee members for taking the time to read my work and provide useful feedback. I have very grateful to Dr. Reed for this leadership and guidance throughout the entirety of my enrollment in graduate school. His kind words and motivation helped to keep me focus and to do my very best with all the work I accomplished.

1.0 MOTIVATION

There are two main issues that are investigated in this work, those being an implementation of a distributed generation system network for integration of renewable resources and a stability analysis of the system itself. Specifically, the DG system is connected to a weak AC grid-tie. The renewable resources are represented as wind and solar energy. The weak connection motivates the need for a formal stability analysis. A weak connection can result in stability issues with regards to certain equipment being utilized to connect the renewable energy sources to the rest of the grid.

The analysis of a renewable generation resource connected to a weak grid is relevant in multiple situations. On the large-scale end, an example being a concentrated generation source of hundreds of megawatts, is likely located in a remote location away from the loads to which it is to supply power. This is true for wind and solar resources as is shown in Figure 1-1 and Figure 1-2. On the other end of the spectrum, dealing with single digit to tens of megawatts in the form of distributed generation, these resources may be added to an existing system that cannot handle the added power due to low ratings on existing installed equipment. The result would be to upgrade the necessary equipment to match the required load and generation, but such an upgrade can be expensive. A specific example of this would be an industrial facility that wishes to add a few megawatts of wind and solar generation to their location. The facility may be a fair distance from a strong grid connection and the additional generation may cause stability issues.

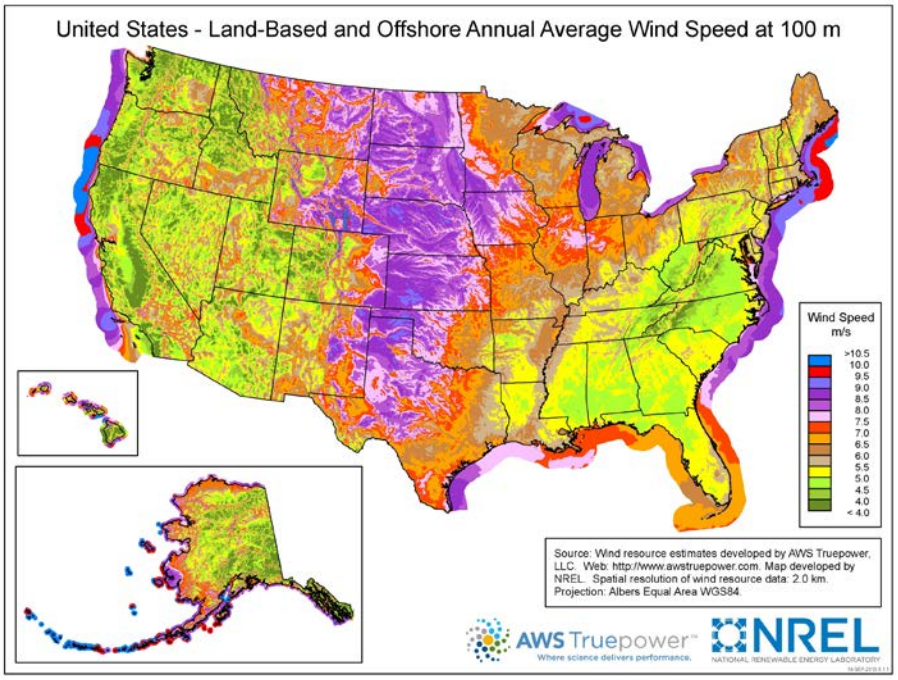

Figure 1-1. Wind resources in the United States [1].

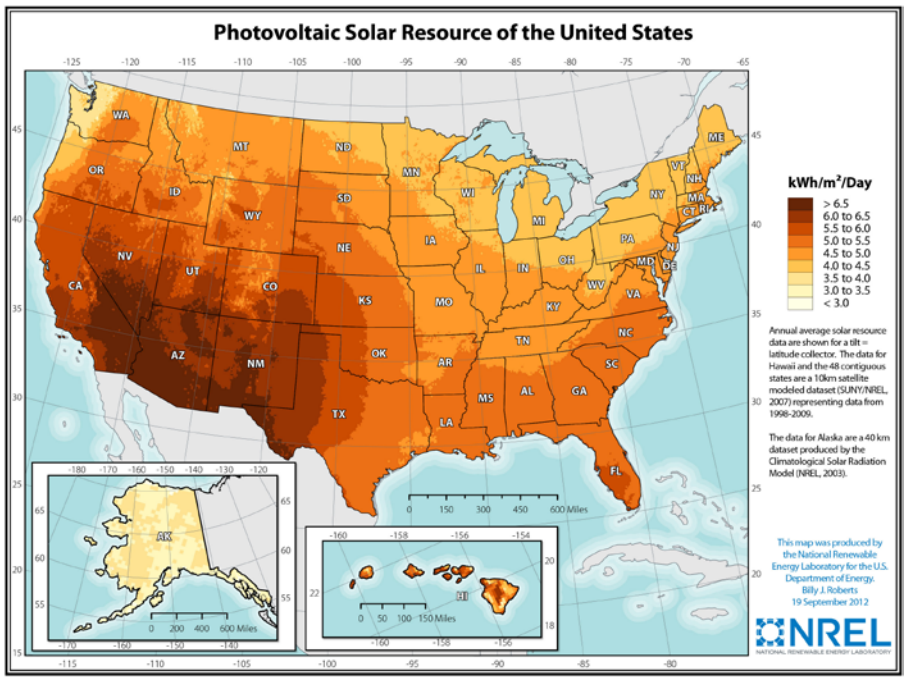

Figure 1-2. Solar resources in the United States [2].

The weak connection to the grid means that a traditional high voltage direct current (HVDC) configuration, like line-commutated converter (LCC), cannot be used since it requires a strong grid and steady voltage for the switching elements to commutate [3]. A comparison of LCC versus VSC can be seen in Table 1-1 [4][5]. While there are a number of differences between the two technologies, the focus of this work is on the requirement of LCC to operate in a strong AC system, whereas the VSC is able to operate in weaker systems.

Table 1-1. Comparison of LCC and VSC.

LCC	**VSC**
High power capability	Lower power capability
Good overload capability	Weak overload capability
Requires stronger AC systems	Operates into weaker AC systems
"Black start" capability requires additional equipment	"Black start" capability
Generates harmonic distortion requiring filtering	Insignificant level of harmonic generation requiring no filtering
Coarser reactive power control	Finer reactive power control
Large site area due to necessary filters	Compact site area 50-60% of LCC site area
Requires converter transformers	Use of conventional transformers
Lower station losses	Higher station losses
Lower cost	Higher cost by 10-15%
Higher reliability	Lower reliability due to high component count
More mature technology	Less mature technology
Power is reversed by changing polarity of the converters	Power is reversed by changing direction of current flow
Requires use of MI cables	Ideal for use with XLPE cables

The focus of this work is on DG connected to a weak grid network. However, by using the output impedance of a system, as will be discussed later, stability analyses can be performed regardless of the grid strength and with limited knowledge of the converters themselves. The dynamics are contained within the small-signal model and are carried through to the output

impedance. The complexity of the output impedance can vary to include only the converter itself and the output filter components or integrate the effects of the control systems that are used to regulate the output values like real and reactive power. This output impedance can then be compared to a Thévenin impedance of the grid system to determine whether it will operate in a stable fashion or require adjustments in order to properly function in different areas.

This will prove to be useful as utilities begin to integrate more and more renewable resources in smaller form factors. The analysis would also be useful for microgrids since stability is of the utmost important because, by its very nature, a microgrid has the ability to operate independently of the larger grid interconnection and must maintain a very high reliability.

In its current state, the grid has fairly large megawatt (MW) generation as its primary contribution for supply. As DG becomes more widespread, smaller, more local generation sources will help to supplement the larger remote power plants. This is a double-edged sword in terms of reliability and stability. With generation closer to the loads being served, there are less losses associated with transmission. Since there are many more smaller generating plants, losing one of many in an area will not have a drastic effect like having a 100 MW power plant go offline. However, with many DG sites, more advanced and sophisticated forms of protection are necessary so that the DG is able to connect and reconnect to the system without causing any issues that would result in negatively affecting the system to which it is connected. For example, if the grid impedance were to change value and the DG power electronics were unable to transition to this new steady-state, issues could arise that would ultimately force the DG to disconnect from the system to prevent any cascading effects from harming the loads or other DG in the area. By designing the output impedance of the DG to operate in a wide range of scenarios, it can continue to supply power without interruptions.

2.0 BACKGROUND AND THEORY

Before performing the analysis on the system and determining the effects of the PLL for various grid impedance conditions, some techniques and nomenclature will be defined. Each section will eventually lead to the PLL analysis of Chapter 4.0

2.1 WEAK GRID

A weak grid connection implies that the local bus voltages can be significantly influenced by load fluctuations and affect power quality and stability. There is not a strict definition of what a weak grid is, but the condition is based on short circuit ratio (SCR), the ratio of S/P_d where S is the three-phase short circuit level in mega-volt amperes (MVA) and P_d is DC terminal power in megawatts (MW), and has characteristically high impedance. Inertia of the system also factors into a system being weak but will not be investigated in this work [6]. These factors are all related and help define what a weak grid is from a mathematical standpoint. Some effects that arise from a weak grid condition are excessive transformer tapping, overloaded lines [7], frequency deviation, and voltage fluctuations in the form of voltage flicker, voltage drop, and harmonic distortion [8]. In order to combat the weak connection, some form of voltage support is necessary. Very fast and continuous control is required for operation in a weak system and support can be added by the addition of synchronous condensers [6].

The SCR is an approximation of an equivalent system that is represented by its Thévenin equivalent impedance and source. It is therefore not a substitute for a full system analysis, but

depending on what is being studied, a detailed system representation may not be required. It should also be noted that SCRs vary depending on the loads being connected and what points in an interconnected system are being analyzed. Any studies will likely consider a range of SCRs to cover many potential situations that may arise. This is especially relevant since the reactive power being supplied by a VSC has an impact on the SCR and will likely vary in real-world installations [9].

Before delving into the issue of stability of the PLL in a weak grid scenario, a brief discussion about some other potential solutions will be presented. These are presented with some simulation results in [10]. The three solutions are static var compensator (SVC), synchronous compensator (SC), a combination of the SVC and SC, and fixed capacitor banks. These options provide dynamic voltage control at the connection point of the VSC. In the case with renewable generation, this connection point is very important for several reasons. In some cases, if the voltage exceeds a certain threshold then it could be disconnected from the system and the power being generated will be lost. Other generation sources would then have to come online in order to compensate for this loss. This is obviously not a desired outcome; therefore, maintaining the voltage at the connection point is of the utmost importance in order to optimize the use of the renewable generation sources. This same issue applies to the frequency at the connection point as well. If it is not maintained within certain limits, the renewable generation may be disconnected to recover and regain stability and is once again lost to provide power for loads. Results from [10] show that a combination of both SVC and SC have the best performance. The SVC is able to operate very quickly and effectively to control overvoltages but actually further decreases the SCR. The SC is slightly the opposite because it has a slower response to controlling voltage but increases the SCR when connected. It makes senses that combining the two would be the best option after

determining how they perform with the appropriate studies. This form of solution, using both SVC and SC, is most appropriate for connections that require a very reliable connection and have loads that must stay operating at all times. It would not be necessary for attaching to sites that have renewable generation and associated weak grid connections. Because, while the loss of the generation is unfortunate, it would be very expensive to have this compensation at every connection point. The results in [10] may also change depending on the voltage level since this research is focused on the medium voltage levels while their system was at 230 kV with larger loads than are being investigated in this research.

2.1.1 Short Circuit Ratio in the Context of Voltage Source Converters

In addition to those issues mentioned previously concerning a weak grid, there are a few additional problems that can directly affect the performance of a VSC. These include: long fault recover times, voltage instability, high temporary overvoltages, risk of commutation failure, and low frequency resonances [10]. The voltage issues can have a correlation to the amount of reactive power that can be supplied by the VSC. If the voltage fluctuations are too great for the VSC to compensate, the system could become unstable. Is it also possible that equipment is damaged from these large voltage swings. A direct impact on the VSC is the risk of commutation failure since this will change the output of the VSC. A VSC is suitable for operation in a weak grid connection due to its ability for self-commutation, but a specific range of appropriate SCR values would be very beneficial. Some research has been done and a value of 1.3 to 1.6 was found but further analysis would be beneficial to affirm these values [11].

2.1.2 Calculating the Short Circuit Ratio of a System

As mentioned in the previous section, the SCR of a system is the ratio of the system short circuit level in megavolt-ampere (MVA) to the DC power of the converter in MW. Another way of defining SCR is the AC system admittance expressed in per unit of DC power. These definitions are expressed in Equations (2-1) and (2-2). The system admittance is with respect to short circuit MVA and the rated AC voltage is used as the base. The rated line RMS voltage is V_s and the Thévenin impedance of the system is Z_s, the local load Z_l, filter impedance Z_f, and compensator impedance Z_c. The definitions and equations disregard the effects on the SCR from filtering elements and other compensation. When these are considered, this is called the effective short circuit ratio (ESCR) and are expressed in Equations (2-3) and (2-4) [9][10].

$$SCR = \frac{S_{ac}}{P_d} = \frac{(V_s^2/|Z_s|)}{P_d}, \tag{2-1}$$

$$SCR = \left(\frac{1}{Z_s} + \frac{1}{Z_l}\right) Z_{base}, \tag{2-2}$$

$$ESCR = \frac{S - Q_c}{P_d}, \tag{2-3}$$

$$ESCR = \left(\frac{1}{Z_s} + \frac{1}{Z_l} + \frac{1}{Z_f} + \frac{1}{Z_c}\right) Z_{base}. \tag{2-4}$$

The maximum power that the VSC is able to transmit has a theoretical limit that is a result of the SCR. This can be seen by looking at the equation,

$$P = \frac{|V_s||V_l|}{\omega L_s} \sin(\theta_c) \approx SCR \sin(\theta_c), \tag{2-5}$$

where $|V_l|$ is the magnitude of the voltage across the load or point of common coupling (PCC), θ_c is the load angle of the converter, and L_s is the inductance of the connected grid system. If it is

assumed that the magnitudes of both V_s and V_l are 1.0 pu, which is accurate during steady-state operation, they can be divided out by the voltage base leaving only the per unit denominator term. It then is equal to the SCR as is evident from Equation (2-2) if Z_{base} is ignored. Therefore, based on Equation (2-5) the load angle cannot be greater than 90º during steady-state conditions [12].

2.2 AVERAGE AND SMALL SIGNAL MODEL OF A VSI

When designing the control scheme that will be used for a converter, the analysis and design is made easier by using an average model of the circuit that is to be controlled. To account for the smaller perturbations that impact the parameters of the circuit during operation, a small-signal model is derived from the average model and further used for analysis with the control scheme. In particular, this work used the small-signal model of a voltage source inverter (VSI). The derivations of these models will not be discussed as there are references that discuss the procedure in detail (See for example [13]–[15]).

The equivalent circuits that are most pertinent are shown in Figure 2-1 and Figure 2-2. The small-signal model is derived from the average model and is the circuit that was used to calculate the needed transfer functions.

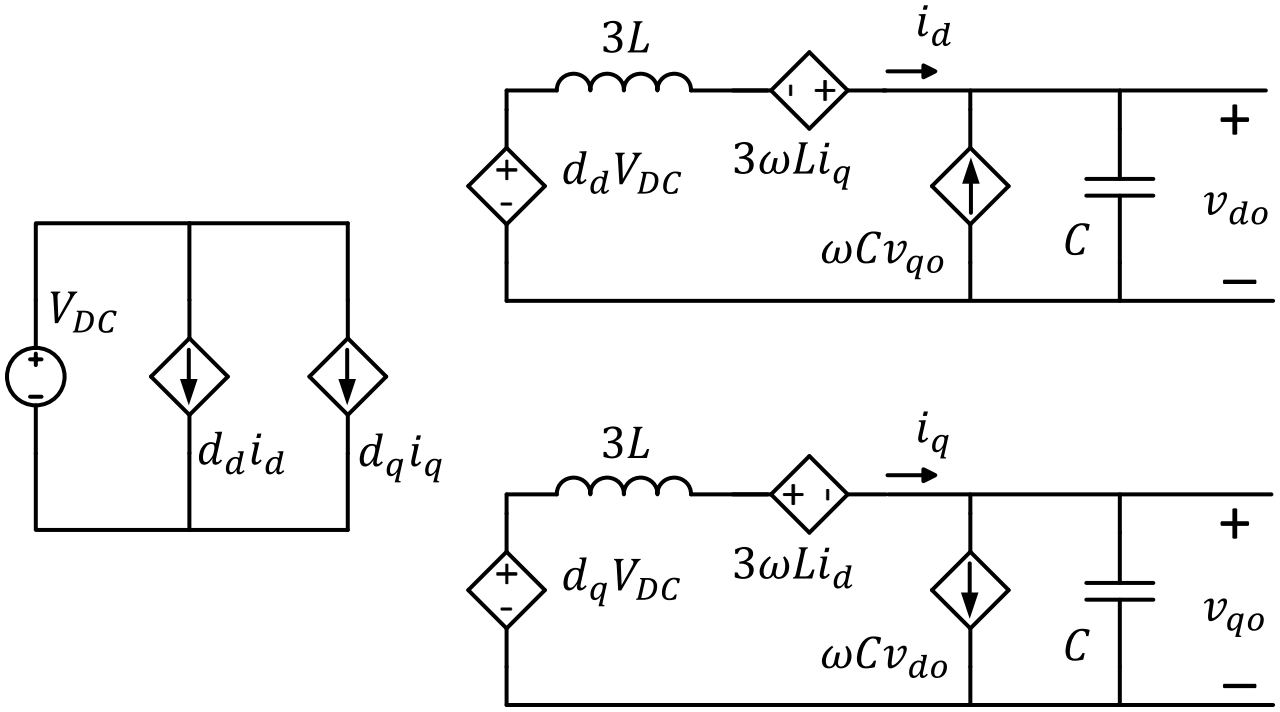

Figure 2-1. Average model of a VSI.

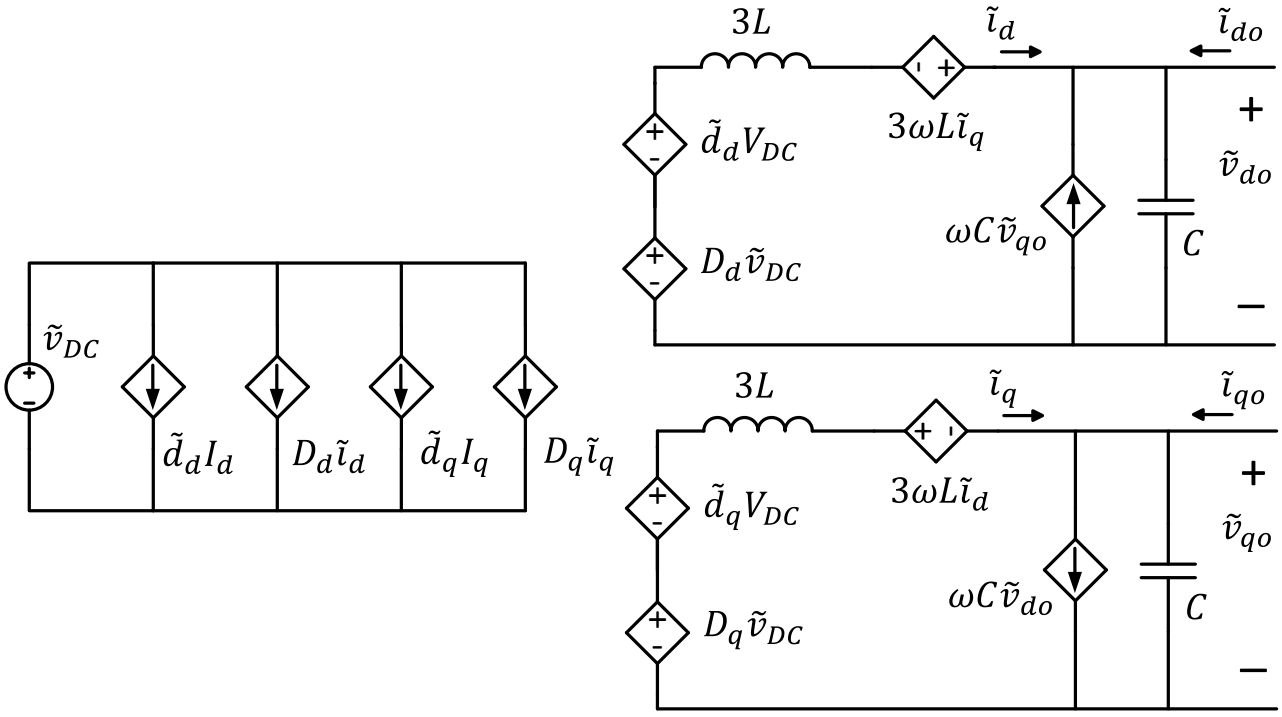

Figure 2-2. Small-signal model of a VSI.

The equations used to create the equivalent circuits are from performing KCL, KVL, and using Ohm's Law to arrive at,

$$\tilde{\imath}_{dc} = \tilde{d}_d I_d + D_d \tilde{\imath}_d + \tilde{d}_q I_q + D_q \tilde{\imath}_q, \tag{2-6}$$

$$3sL\tilde{\imath}_d = 3\omega \tilde{\imath}_q + \tilde{d}_d V_{dc} + D_d \tilde{v}_{dc} - \tilde{v}_d, \tag{2-7}$$

$$3sL\tilde{\imath}_q = -3\omega \tilde{\imath}_d + \tilde{d}_q V_{dc} + D_q \tilde{v}_{dc} - \tilde{v}_q, \tag{2-8}$$

$$\tilde{v}_d = \left(\tilde{\imath}_q + \omega C \tilde{v}_q\right)\left(\frac{1}{Cs+1}\right), \tag{2-9}$$

$$\tilde{v}_q = \left(\tilde{\imath}_d - \omega C \tilde{v}_d\right)\left(\frac{1}{Cs+1}\right). \tag{2-10}$$

Gathering current and voltage terms from Equations (2-6)-(2-10) and converting 's' to the time-domain derivative yields,

$$\frac{d}{dt}\begin{bmatrix}\tilde{\imath}_d \\ \tilde{\imath}_q\end{bmatrix} = \frac{1}{3L}\begin{bmatrix}\tilde{d}_d \\ \tilde{d}_q\end{bmatrix} V_{dc} + \frac{1}{3L}\begin{bmatrix}\tilde{d}_d \\ \tilde{d}_q\end{bmatrix} \tilde{v}_{dc} - \begin{bmatrix}0 & -\omega \\ \omega & 0\end{bmatrix}\begin{bmatrix}\tilde{\imath}_d \\ \tilde{\imath}_q\end{bmatrix} - \frac{1}{3L}\begin{bmatrix}\tilde{v}_d \\ \tilde{v}_q\end{bmatrix}, \tag{2-11}$$

$$\frac{d}{dt}\begin{bmatrix}\tilde{v}_d \\ \tilde{v}_q\end{bmatrix} = \frac{1}{C}\begin{bmatrix}\tilde{\imath}_d \\ \tilde{\imath}_q\end{bmatrix} - \begin{bmatrix}0 & -\omega \\ \omega & 0\end{bmatrix}\begin{bmatrix}\tilde{v}_d \\ \tilde{v}_q\end{bmatrix} \pm \frac{1}{RC}\begin{bmatrix}\tilde{v}_d \\ \tilde{v}_q\end{bmatrix}, \tag{2-12}$$

$$\tilde{\imath}_{dc} = \begin{bmatrix}D_d & D_q\end{bmatrix}\begin{bmatrix}\tilde{\imath}_d \\ \tilde{\imath}_q\end{bmatrix} + \begin{bmatrix}\tilde{d}_d & \tilde{d}_q\end{bmatrix}\begin{bmatrix}I_d \\ I_q\end{bmatrix}. \tag{2-13}$$

In order to use these equations to calculate the desired transfer functions that are needed for the analysis, they are finally placed into a state-space form using the $\mathbf{A}\vec{x}+\mathbf{B}\vec{u}$ format. The result is

$$\frac{d}{dt}\begin{bmatrix}\tilde{\imath}_d \\ \tilde{\imath}_q \\ \tilde{v}_d \\ \tilde{v}_q\end{bmatrix} = \begin{bmatrix}0 & -\omega & -\frac{1}{3L} & 0 \\ -\omega & 0 & 0 & -\frac{1}{3L} \\ \frac{1}{C} & 0 & -\frac{1}{C} & \omega \\ 0 & \frac{1}{C} & -\omega & -\frac{1}{C}\end{bmatrix}\begin{bmatrix}\tilde{\imath}_d \\ \tilde{\imath}_q \\ \tilde{v}_d \\ \tilde{v}_q\end{bmatrix} + \begin{bmatrix}\frac{V_{dc}}{3L} & 0 \\ 0 & \frac{V_{dc}}{3L} \\ 0 & 0 \\ 0 & 0\end{bmatrix}\begin{bmatrix}\tilde{d}_d \\ \tilde{d}_q\end{bmatrix} + \begin{bmatrix}\frac{D_d}{3L} \\ \frac{D_q}{3L} \\ 0 \\ 0\end{bmatrix}\tilde{v}_{dc}, \tag{2-14}$$

where $\tilde{v}_{dc}$and its matrix multiplier are extra terms to complete the set of equations. With the proper format established, it will be much easier to obtain the transfer functions depending on the inputs and outputs that are desired. Again, following the state-space format, the **C** matrix that is the multiplier for the output can be changed to find the desired transfer functions.

All of the desired transfer functions are calculated in Chapter 4.0 the PLL Stability Analysis. However, to establish the formatting and method used to find the transfer functions discussed, an example will be given for context. In this example, the transfer function of the control to the inductor current. The state-space form is known and the transfer functions can be found with the equation,

$$\frac{\boldsymbol{Y}(s)}{\boldsymbol{U}(s)} = \boldsymbol{C}(s\boldsymbol{I} - \boldsymbol{A})^{-1}\boldsymbol{B} + \boldsymbol{D}. \tag{2-15}$$

For the control to inductor current transfer function, the values for each matrix are the following,

$$\boldsymbol{A} = \begin{bmatrix} 0 & -\omega & -\frac{1}{3L} & 0 \\ -\omega & 0 & 0 & -\frac{1}{3L} \\ \frac{1}{C} & 0 & -\frac{1}{RC} & \omega \\ 0 & \frac{1}{C} & -\omega & -\frac{1}{RC} \end{bmatrix},$$

$$\boldsymbol{B} = \begin{bmatrix} \frac{V_{dc}}{3L} & 0 \\ 0 & \frac{V_{dc}}{3L} \\ 0 & 0 \\ 0 & 0 \end{bmatrix},$$

$$\boldsymbol{C} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix},$$

$$\boldsymbol{D} = 0,$$

$$s\boldsymbol{I} = \begin{bmatrix} s & 0 & 0 & 0 \\ 0 & s & 0 & 0 \\ 0 & 0 & s & 0 \\ 0 & 0 & 0 & s \end{bmatrix}.$$

It can then be seen that the output will result in a 2x1 matrix with the output being the inductor current with respect to the *d*-domain ($\tilde{\imath}_d$) and the inputs are the duty cycles in both the *d* and *q* domain ($\tilde{d}_d$ and $\tilde{d}_q$). The resulting equations are,

$$\frac{\tilde{\imath}_d}{\tilde{d}_d} \quad \frac{V_g(Cs + 3Ls + 3C^2Ls^3 + 6CLs^2 + 3C^2Lsw^2 + 1)}{6Ls + 9L^2s^2 + 9L^2w^2 + 18CL^2s^3 + 9C^2L^2s^4 + 9C^2L^2w^4 + 6CLs^2 - 6CLw^2 + 18C^2L^2s^2w^2 + 18CL^2sw^2 + 1}, \quad \text{(2-16)}$$

$$\frac{\tilde{\imath}_d}{\tilde{d}_q} \quad \frac{V_g(3Lw - Cw + 3C^2Lw^3 + 3C^2Ls^2w + 6CLsw)}{6Ls + 9L^2s^2 + 9L^2w^2 + 18CL^2s^3 + 9C^2L^2s^4 + 9C^2L^2w^4 + 6CLs^2 - 6CLw^2 + 18C^2L^2s^2w^2 + 18CL^2sw^2 + 1}. \quad \text{(2-17)}$$

2.3 PHASE-LOCKED LOOP

The phase-locked loop (PLL) is employed in many electronic applications besides the power grid. The PLL is widely used in other fields like communications to phase-lock into an existing signal and match it via its internal oscillator. The signal generated by the PLL is then passed on to the control system to be used for determining signals for the switches of its associated converter. Early PLL techniques used zero-crossing detection for finding the phase of the corresponding signal. However, in weak grid environments, such as the one investigated in this research, more advanced techniques are necessary to avoid the possibility of multiple zero-crossings being detected in the presence of harmonics and noise. A controller that is observed from a stationary frame and rotating with respect to the fundamental grid frequency looks like it has DC variables. These variables can be controlled with DC controllers that are advanced and proven. These also work in such a way to eliminate many problematic harmonics that may have caused issues for the PLL itself.

The basic PLL structure is comprised of three portions. These include a phase detector (PD), loop filter (LF), and voltage controlled oscillator (VCO). A diagram and their associated components are shown in Figure 2-3. The phase detector compares the signal created by the VCO and the desired signal to determine their phase difference and outputs a value proportional to this difference. The output is then fed to a low-pass filter, which is usually represented by a proportional-integrator (PI) controller. Lastly, the value from the LF is used as an input to the VCO to create the desired signal (in this case, a 60Hz sine wave) to match that of the input signal to the PLL.

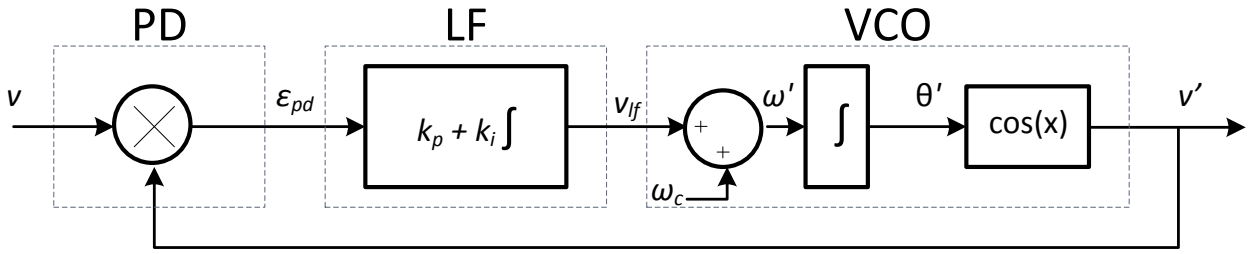

Figure 2-3. Basic PLL Building Blocks.

The PD block is a simple multiplier and the signal coming from the VCO and the input have a unique phase and frequency term. The input signal is expressed as

$$v = sin(\theta) = sin(\omega t + \phi), \tag{2-18}$$

and the signal from the VCO is expressed as

$$v' = \cos(\theta') = cos(\omega' t + \phi'), \tag{2-19}$$

with the phase error at the output of the PD written as

$$\varepsilon_{pd} = V k_{pd} sin(\omega t + \phi) cos(\omega' t + \phi'),$$
$$= \frac{V k_{pd}}{2}\big[\sin\big((\omega - \omega')t + (\phi - \phi')\big) + \sin\big((\omega + \omega')t + (\phi - \phi')\big)\big]. \tag{2-20}$$
low-frequency term high frequency term

It is assumed that the LF will filter out the high frequency components of the result from the VCO and input signal being multiplied together. Therefore, the PD error can be expressed as

$$\bar{\varepsilon}_{pd} = \frac{Vk_{pd}}{2} sin\big((\omega - \omega')t + (\phi - \phi')\big), \tag{2-21}$$

When the frequency of the VCO is well tuned to the frequency of the input signal, and the phase error between the two is very small, the expression for the DC term can be simplified when the PLL is locked-in as

$$\bar{\varepsilon}_{pd} = \frac{Vk_{pd}}{2}(\theta - \theta'). \tag{2-22}$$

Equation (2-22) can be used to implement a small signal linearized model of the PD. Moving to the VCO, its averaged frequency is expressed as,

$$\bar{\omega}' = (\omega_c + \Delta\, \bar{\omega}') = \big(\omega_c + k_{vco}\bar{v}_{lf}\big), \tag{2-23}$$

where ω_c is the center frequency of the VCO. By comparing the right and left sides of Equation (2-23), it can be determined that small variations of VCO frequency can be represented by,

$$\bar{\omega}' = k_{vco}\bar{v}_{lf}. \tag{2-24}$$

By using this result, the phase-angle detected by the PLL itself can be expressed in the time domain as,

$$\theta' = \int \bar{\omega}' dt = \int k_{vco}\bar{v}_{lf} dt. \tag{2-25}$$

2.3.1 Linearized Small Signal Model of a PLL

All equations and derivations have thus far been expressed in the time domain. However, it will be more useful from a design perspective to express them in the frequency domain so that the

transfer function of the PLL can be derived. The derivation will utilize the small signal model for the PLL and is pictured in Figure 2-4.

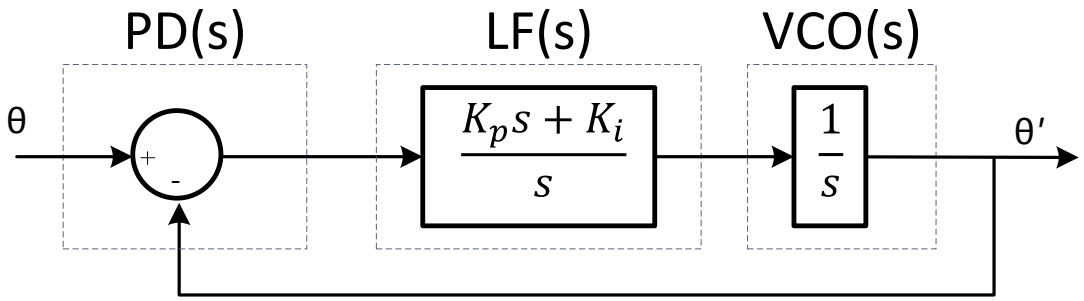

Figure 2-4. Small signal model of a basic PLL [16].

The transfer function expressed in the frequency domain will allow for use of techniques and intuition that are unavailable or more difficult to utilize when the equations and expressions are written only in the time domain. With k_{pd} and k_{vco} equal to one, each component of the PLL is given in its frequency domain format as

Phase detector: $$E_{pd}(s) = \frac{V}{2}(\Theta(s) - \Theta'(s)) \quad (2\text{-}26)$$

Loop filter (LF): $$V_{lf}(s) = \left(K_p + \frac{K_i}{s}\right) E_{pd}(s) \quad (2\text{-}27)$$

Voltage Controlled Oscillator: $$\Theta'(s) = \frac{1}{s} V_{lf}(s) \quad (2\text{-}28)$$

From the frequency domain equations derived above, the closed-loop transfer functions for the phase ($H_\theta(s)$) and error ($E_\theta(s)$) are determined to be

$$H_\theta(s) = \frac{\Theta'(s)}{\Theta(s)} = \frac{LF(s)}{s + LF(s)} = \frac{K_p s + K_i}{s^2 + K_p s + K_i}, \quad (2\text{-}29)$$

$$E_\theta(s) = \frac{E_{pd}(s)}{\Theta(s)} = 1 - H_\theta(s) = \frac{s^2}{s^2 + K_p s + K_i}. \quad (2\text{-}30)$$

These transfer functions can then be written in a normalized format so they can be related to other formats studied in the realm of control systems:

$$H_\theta(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \tag{2-31}$$

$$E_\theta(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \tag{2-32}$$

where $\omega_n = \text{natural frequency}$ and $\zeta = \text{damping coefficient.}$

The closed-loop phase transfer function shows a low-pass filter characteristic for the input phase angle, which is very useful for eliminating unwanted noise and/or high order harmonics from the signal. It can also be seen from the transfer functions that this is a second-order function. A second-order system has been studied extensively in control focused textbooks and that information can be directly applied here. For example, the settling time of this system can be readily estimated as the following,

$$t_s = 4.6\tau \quad \text{with} \quad \tau = \frac{1}{\zeta\omega_n} \tag{2-33}$$

Taking these equations and the normalized transfer functions from above, the tuning parameters for the PLL can be estimated as the following,

$$K_p = 2\zeta\omega_n = \frac{9.2}{t_s}, \qquad K_i = \frac{K_p\omega_n}{2\zeta} = \frac{2.3K_p}{t_s\zeta^2}. \tag{2-34}$$

Bandwidth is a term often used in signal processing and with the operating boundaries and response of a transfer function. In reference to PLLs, their bandwidth does not refer to one description in particular. When used in literature, it may refer to any of the following: (1) natural frequency ω_n, (2) loop gain K, (3) noise bandwidth B_L, and (4) 3-dB bandwidth ω_{3db} [17].

It is noted in [17] that the classification of bandwidth as the natural frequency of the PLL is not an accurate measure. This is because the damping factor ζ has an influence on the response of the PLL transfer function. This effect of ζ on the response of the PLL can be seen in Figure 2-5. The various values of ζ cause the lowpass curves to fall off at different frequency values. This has been illustrated to point out that if using the term bandwidth in reference to the natural frequency, one should use caution because it is not entirely accurate [17].

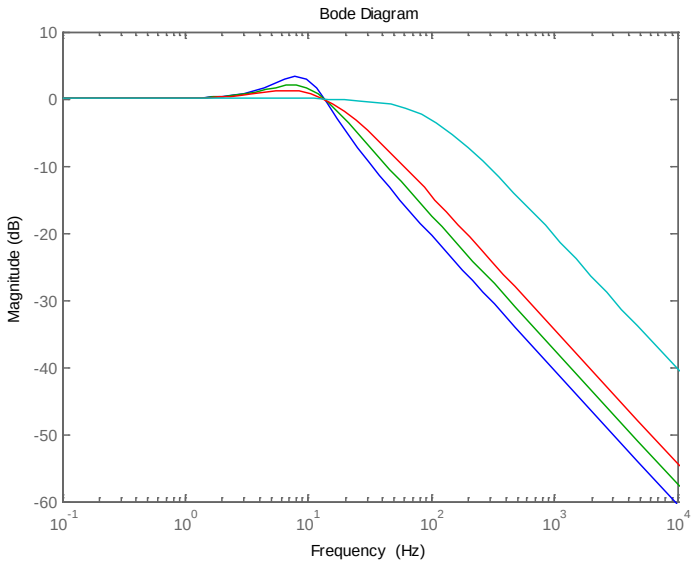

Figure 2-5. Effect of damping factor on the response of the PLL [17].

An important factor of the PLL is the 3-dB bandwidth. It can be increased and decreased depending on the response that is desired. The 3-dB bandwidth is represented mathematically by the following equation:

$$\omega_{-3db} = \omega_\theta \left(1 + 2\zeta^2 + \sqrt{(1+2\zeta)^2 + 1}\right)^{1/2}. \tag{2-35}$$

When designing a PLL, there are four key parameters to consider as outlined in [18]. These four parameters are the hold range, pull-in range, pull-out range, and lock range.

- Hold range $\Delta\omega_H$
- Pull-in range $\Delta\omega_P$
- Pull-out range $\Delta\omega_{PO}$
- Lock range $\Delta\omega_L$

The hold range is stated to be more useful from an academic standpoint. This frequency range of the PLL is representative of the range wherein the PLL can maintain phase lock statically. If the frequency of the input signal exceeds the hold range, the PLL will no longer be able to acquire a phase-lock. The expression of the hold range is

$$\Delta\omega_H = K_{pd}K_{vco}LF(0), \tag{2-36}$$

where the value of LF(0) is the DC gain of the loop filter and varies depending on the type of filter used. A passive lag filter results in LF(0) = 1, for an active lag filter LF(0) = K_a, and lastly for an active PI filter LF(0) = ∞. For this particular application, it is highly likely that a PI controller will be implemented. If that is the case, the hold range will be infinite and the only frequency limit on the PLL will be the frequency range of the VCO.

The pull-in range represents the frequency extents where the PLL will be locked into the phase angle of the input signal. This range is dependent on the type of filter used. As mentioned for the hold range, by using a PI filter, the range is practically infinite. The pull-in time, not to be confused with the pull-in range, is the time needed by the PLL to become locked and is usually much larger than the lock-in time. It can be calculated

$$T_P = \frac{\pi^2}{16}\frac{\Delta\omega_n^2}{\zeta\omega_n^3}. \tag{2-37}$$

The pull-out range is the dynamic limit for stable operation of a PLL. This range is much smaller in comparison to the hold range. If the PLL goes outside the pull-out range and loses tracking, it is possible for it to lock-in again since it is still within the hold range. This range is approximated by the expression

$$\Delta\omega_{PO} = 1.8\omega_n(\zeta + 1). \tag{2-38}$$

The final key parameter is the lock range, which indicates that the PLL will lock very quickly when it falls within this range. Using a PI filter for the LF, the lock range can calculated with the equation

$$\Delta\omega_L = 2\zeta\omega_n = 2\zeta\sqrt{k_p k_i}. \tag{2-39}$$

And consequently the settling time or lock-in time is calculated as

$$T_L \approx \frac{2\pi}{\omega_n}. \tag{2-40}$$

Each range has a corresponding operational stability that varies from dynamically unstable to the actual operating range of the PLL. The simple inequality can be found relating the four key parameters and looks like

$$\Delta\omega_L < \Delta\omega_{PO} < \Delta\omega_P < \Delta\omega_H.$$

2.3.2 PLLs using Quadrature Signals

It is of interest to take a step back to determine why it is beneficial (or quite necessary, in reality) to utilize quadrature signals for the PLL rather than simply applying the basic structure to the electric power system. An example problem, and the issues that arise from it, are presented in [16] and will be reviewed here.

The diagram depicted in Figure 2-3 has several drawbacks when applied to the electric grid where the frequency used is quite low at 60 Hz (or ω = 377 rads/sec). This poses some issues when calculating the parameters discussed earlier due to the assumptions made to determine those expressions. Most notably, an oscillatory frequency appears when the PLL attempts to lock-in with the input signal. This is found to be double that of the grid frequency, which would be 120 Hz in the case of a system using 60 Hz AC. A depiction of this occurring can be seen in Figure 2-6.

The parameters were chosen when designing this PLL to maintain a settle time of 100 ms and a damping factor of 0.707. With these parameters, the pull-in time can be calculated from the equations presented earlier to be 312.7 ms. However, as shown in Figure 2-6 the pull-in time is much greater at 1.75 s. There is a reason for this discrepancy between the derived equations and the results found for this example. It was initially assumed during the expression derivations that the input signal to be phase-locked would be much higher than the bandwidth of the PLL. Under this assumption, the higher frequency terms would be filtered and have no effect on the output result. In the case of an electric power system, the frequency is very close to the cut-off frequency of the PLL. These high frequency terms in the phase-angle error are twice that of the input frequency. In this example, the bandwidth is calculated as 21.3 Hz.

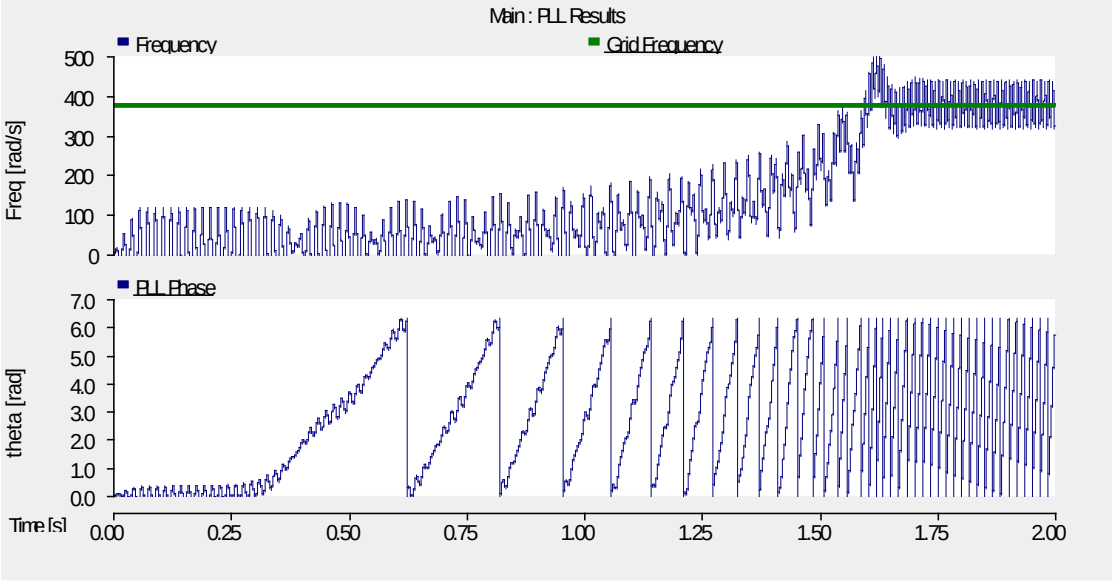

Figure 2-6. Depiction of 120 Hz oscillation.

To overcome this issue of having a 120 Hz oscillation present on the output of the PLL, the phase detector is changed from a simple multiplication block to a quadrature signal generator. The new diagram of the PLL is pictured in Figure 2-7. The new calculation for the phase error ε_{pd}, becomes the following,

$$\begin{aligned} \varepsilon_{pd} &= V\sin(\omega t+\phi)\cos(\omega' t+\phi') - V\cos(\omega t+\phi)\sin(\omega' t+\phi') \\ &= V\sin\big((\omega-\omega')t+(\phi-\phi')\big) = V\sin(\theta-\theta'). \end{aligned} \tag{2-41}$$

According to Equation (2-41), the steady-state error from the new quadrature PD will not contain any steady-state oscillation when the PLL is well synchronized, i.e. with $\omega = \omega'$. Therefore, it can be concluded that by replacing the previous PD with the version using a quadrature signal generator, the equations derived earlier can be applied when designing a PLL for the electric power grid. This is also useful because techniques from other fields that use PLLs can be applied here as well.

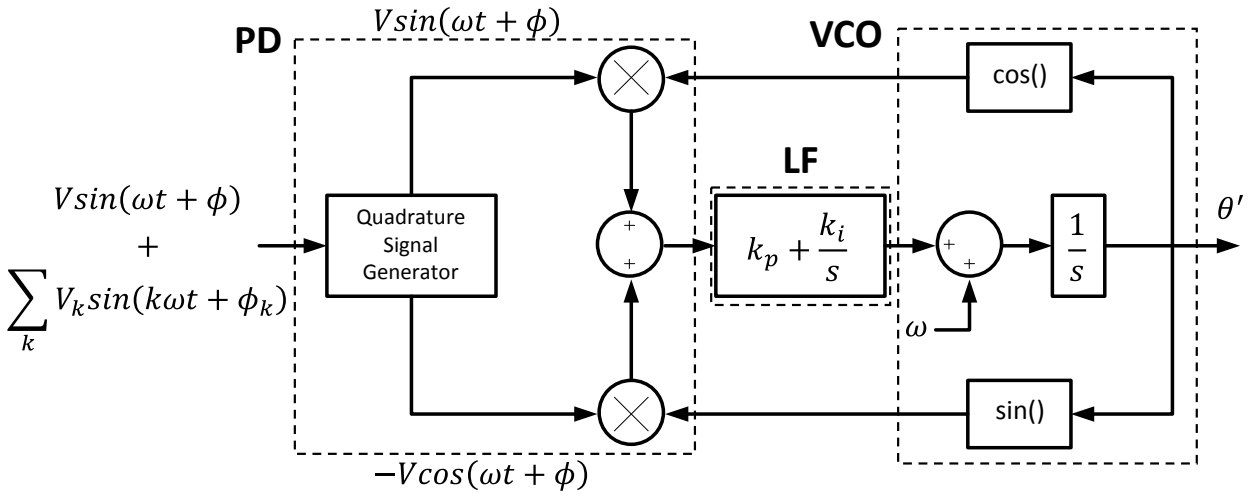

Figure 2-7. PD using quadrature signals in the PLL structure [16].

Once again, referring to Equation (2-41), it will be pointed out that this trigonometric expression is a part of the Park's transformation. The Park's transformation is used extensively in control systems for the electric power network and therefore well studied [19]. Applying to the PLL will modify the model further, as shown in Figure 2-8. Also, with the introduction of the Park's transformation, the VCO is no longer necessary and replaced with a frequency/phase-angle generator (FPG). The $\alpha\beta$ to dq transformation block is represented by the transformation matrix,

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos(\theta') & \sin(\theta') \\ -\sin(\theta') & \cos(\theta') \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}. \tag{2-42}$$

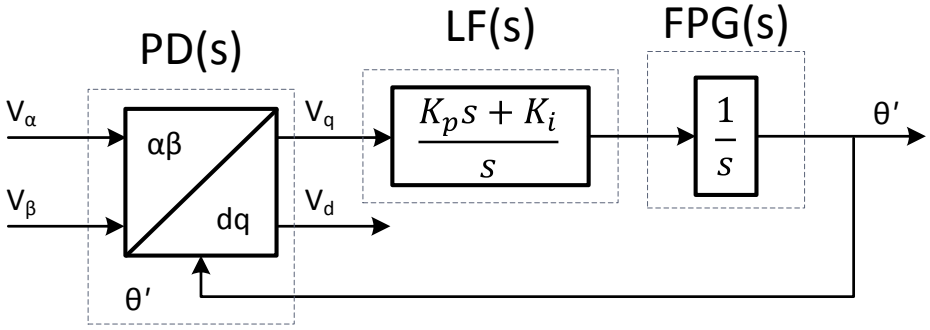

Figure 2-8. PD block adapted using Park's transformation [16].

If the input signal to the PLL is a sine wave expressed as $Vsin(\theta)$, the output of the quadrature signal generator (QSG) is expressed as,

$$\boldsymbol{v}_{\alpha\beta} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = V \begin{bmatrix} \sin(\theta) \\ -\cos(\theta) \end{bmatrix}. \tag{2-43}$$

Finally, by substituting (2-43) into (2-42), the expression for the output of the PD is found and free of oscillations if the PLL is well tuned to the frequency of the input signal,

$$\boldsymbol{v}_{dq} = \begin{bmatrix} v_d \\ v_q \end{bmatrix} = V \begin{bmatrix} \sin(\theta - \theta') \\ -\cos(\theta - \theta') \end{bmatrix}. \tag{2-44}$$

By using the QSG, it allows for regulation of the active and reactive power delivered into a single-phase network by a power converter.

2.4 FORMULATING THE CRITERIA TO EVALUATE STABILITY

The stability of an AC system has been outlined extensively in texts and literature so there is no need to create anything new [20]–[23]. The key fields of stability can fall under one of a few categories. These categories are but not limited to small-signal stability, transient stability, subsynchronous oscillations, and mid-term and long-term stability [20].

Small-signal stability is the ability of the power system to maintain synchronism when subjected to small disturbances. The small-signal stability category has even more meaning when the characteristics and modeling of certain power system components is known. By knowing the components, the equations to represent them can be more easily obtained and understood. Instabilities may result from two forms, steady increase in generator rotor angle due to lack of synchronizing torque, and rotor oscillations of increasing amplitude due to lack of sufficient

damping torque. In the present day power system, one of the main causes for small-signal instability lies with the insufficient damping of system oscillations [20]. With respect to the AC system being studied in this research, small-signal stability will be investigated but not with respect to any rotating machines. The two sources of generation that will be implemented include photovoltaics and wind turbines. The issue of insufficient damping of oscillations will therefore be a non-issue. The photovoltaics have no oscillatory effects in reference to those represented in small-signal stability. While the wind turbines have machines that serve as the creation point of electricity, they will not be modeled in such detail to include the effects that the machine may have. Both generators will be modeled as ideal sources since they are not the focus of this work. The power electronic converters and the control used to transmit power from the renewable generation sources will be the main focus. By perturbing the system about a chosen steady-state operating point, the effects of the control, specifically the PLL, can be observed and understood.

In a typical power system, the large rotating machines that are generating power are of the most interest when investigating transient stability since they govern the reference voltages and angles throughout the rest of the system. If any of these large machines become unstable due to a transient disturbance, such as a transmission line fault, loss of generation, or large load loss, factors like power flows or bus voltages may deviate too far from their ideal values and cause issues to power equipment or loads. However, with the system being studied for this research, transient disturbances such as those mentioned will be regulated by the power electronic converters in the system. Therefore the control schemes of the converters will be the main factor that determines the transient stability of the system [20].

The last topics are of sub-synchronous resonance and mid-to-long term stability. The former topic will not be investigated in this research since these resonances would be from much larger

generating sources than will be used. It would be more applicable to a coal plant with hundreds of generated megawatts versus solar and wind farms that are rated more in the tens of megawatts. The wind turbines may have contribution to sub-synchronous resonance but this will not be investigated. Mid-to-long term stability has mention of power systems being placed into islanded states [20]. One of the benefits of distributed generation is its ability to operate in an islanding mode. The power flows exchanged between generation and load would be the focus of research. These flows would be regulated by the power converters and communication between the converters would be vital for power flows to transfer smoothly.

A look at the stability issues for AC networks has been outlined in this section and compared to the case of a distributed generation branch. Some of the types stability discussed were not investigated because distributed generation did not possess the permissions to regulate voltage levels initially according to the IEEE1547 Standard but an addition has been made recently that addresses this [24].

2.4.1 Output Impedance

An effective method for analyzing the stability of a system that has an inverter connecting renewable generation to the grid is by looking at its output impedance in relation to the grid and line impedances [25]. For this work in particular, the impedance of the grid plays a very important factor. The grid input impedance can be compared to the output impedance of the VSC by using a ratio to determine the stability of the system. The power electronics circuit is nonlinear and therefore the small-signal analysis that was outlined in Chapter 2.2 will be of use. A simple representation is shown in Figure 2-9.

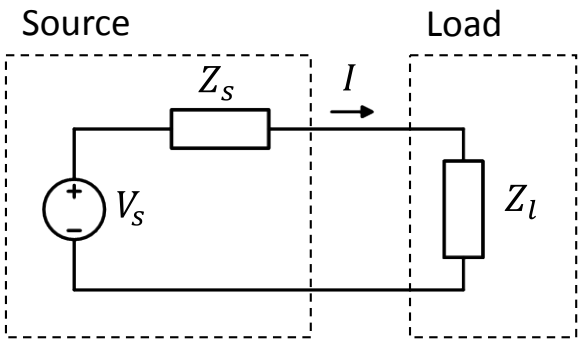

Figure 2-9. Small-signal representation of a VSC and its corresponding load.

The current can be found dividing the source voltage by the series combination of the load and source impedance,

$$I(s) = \frac{V_s(s)}{Z_s(s) + Z_l(s)}, \tag{2-45}$$

While focusing on the stability of the system, it is assumed that the voltage source is stable and the load current is stable as well. This means that $V_s(s)$ and $Z_l(s)$ do not factor into the stability of $I(s)$. If the equation is rearranged to factor out these terms, the parameters that affect the stability of the system can be more easily seen.

$$I(s) = \frac{V_s(s)}{Z_l(s)} x \frac{1}{1 + \frac{Z_s(s)}{Z_l(s)}}. \tag{2-46}$$

It can be that if the ratio of the source voltage to the load impedance is assumed stable that the factor that matters in the analysis lies on,

$$H(s) = \frac{1}{1 + \frac{Z_s(s)}{Z_l(s)}}. \tag{2-47}$$

By applying control theory to this function, the stability can be determined by using the Nyquist stability criterion.

The approached discussed thus far is applicable to voltage sources that are assumed to be stable while unloaded and operating on their own. Since renewable sources are usually connected to the greater electric grid, a model incorporating both the VSC and the grid is needed. To account for this, the new model shown in Figure 2-10 is used.

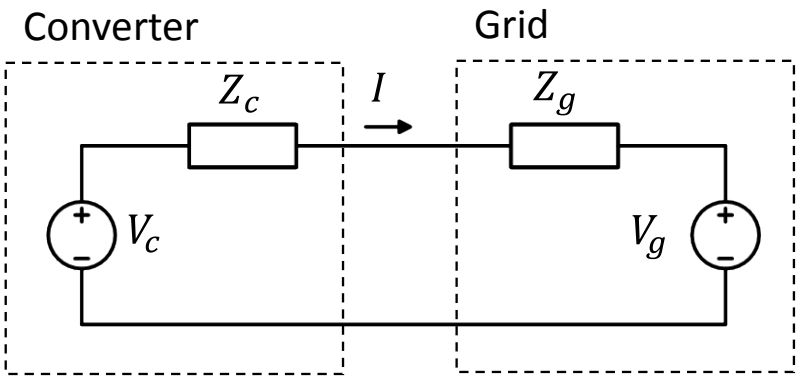

Figure 2-10. Small-signal model with inverter modeled as a voltage source and impedance connected to a grid equivalent model.

By use of superposition, the equation for the current with the connected grid is,

$$I(s) = \frac{V_c(s)}{Z_c(s) + Z_g(s)} - \frac{V_g(s)}{Z_c(s) + Z_g(s)}. \tag{2-48}$$

Based on the stability assumptions of the VSC being stable by itself and the grid being stable by itself, Equation (2-33) can be rearranged by factoring out the VSC impedance to that shown in Equation (2-34).

$$I(s) = \left(\frac{V_c(s)}{Z_c(s)} - \frac{V_g(s)}{Z_c(s)}\right) x \left(\frac{1}{1 + \frac{Z_g(s)}{Z_c(s)}}\right). \tag{2-49}$$

It can be seen that to be stable, the ratio of the grid impedance to the converter impedance must satisfy the Nyquist criterion. The VSC will be stable across a large spread of grid impedances

if it is very large [25]. As will be shown in Chapter 4.0 the PLL will affect the output impedance and can destabilize the system under certain grid impedance values.

2.4.2 Impedance Shaping

An important tool that is available when using the impedance for determining the stability of the system is that adjusting certain aspects of the control system can shape the impedance of the VSC. These include the PLL, current control, and voltage control of the VSC. This grants a few degrees of freedom when presented with a large grid impedance that would cause issues for the VSC, to adjust its parameters in order to reduce or eliminate the instability problems. Each of the three control parts have varying effects on the output impedance and the focus of this work is on the PLL effects. It is stated in [26] that it is typically not practical to keep the ratio of the grid impedance to the VSC output impedance within the unit circle. Furthermore, system stability usually is governed by the phase difference of the two impedances at the frequency where their magnitudes are equal. Therefore, it is desirable to keep a proper phase response within a certain frequency range.

3.0 SYSTEM OVERVIEW

The power system investigated in this work is intended to represent a load that is being supplied by local distributed generation and is connected to a larger grid network via a weak connection. A three-phase system diagram is shown in Figure 3-1. The distributed generation is represented by an ideal DC source. The dynamics from the sources are not of interest in this work and therefore it was chosen to have them as ideal and supplying a constant DC voltage.

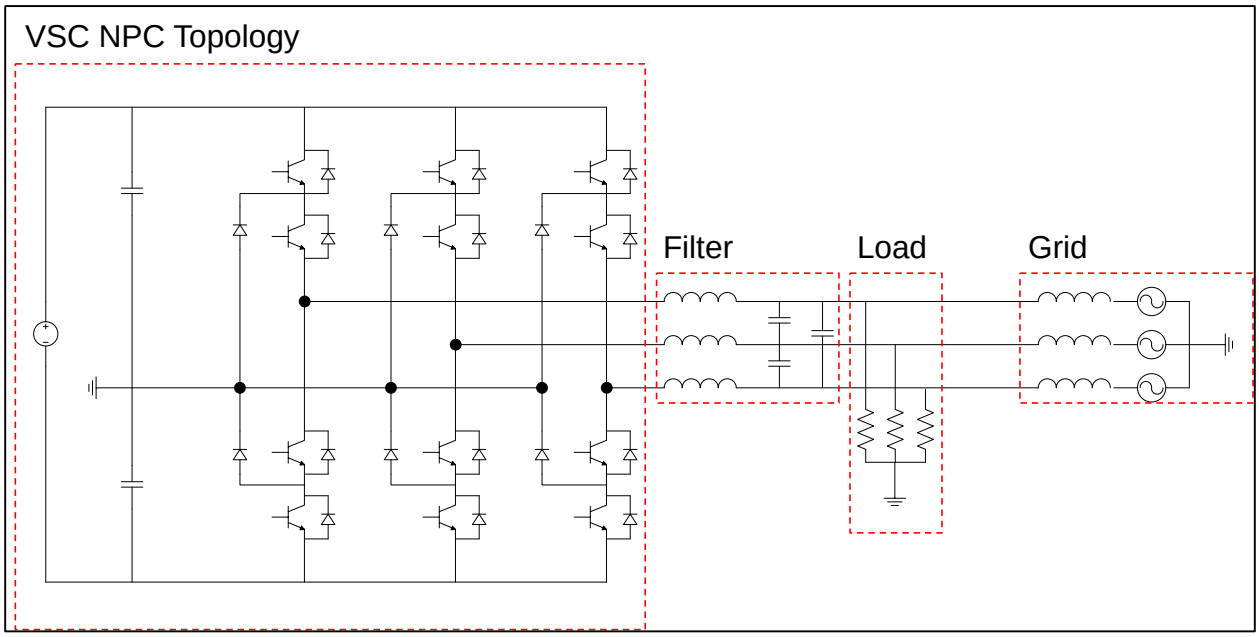

Figure 3-1. System with distributed generation and weak connection.

Coming from the opposite end of Figure 3-1, an infinite bus (ideal three-phase AC source) is representative of the remaining power grid that the load and distributed generation are connected. There is next a series RL impedance that is very important in establishing the weak connection that is vital to the research being performed. The bases used for calculation were V_{base}

= 13.8 kV and S_{base} = 5 MVA. The calculation shown is for a SCR of 1.3 but any value of SCR can be found using the same equation. This value for the impedance of the weak system was determined to be 29.29 Ω.

$$SCR = \left(\frac{1}{Z_s} + \frac{1}{Z_l}\right) Z_{base},$$

$$SCR = 1.3 = \left(\frac{1}{29.29\ \Omega}\right)\left(\frac{(13.8\ kV)^2}{5\ MVA}\right), \tag{3-1}$$

$$Z_s = 29.29\ \Omega.$$

The VSCs are of a neutral point clamped (NPC) circuit topology design. For additional power capacity, a 3-level configuration was chosen. A circuit diagram is shown in Figure 3-2. The output of the converters is connected to the same point, as they are connected in parallel, by very similar impedance values. Part of the impedance is comprised of a *LC*-filter for smoothing of the VSC outputs while the remainder is from transmission cable. Table 3-1 contains the values and ratings used for the various components and equipment for the entire system.

Table 3-1. Parameters for various components of the system.

Parameter	**Value**
VSC DC Source	20 kV
System Voltage	13.8 kV
Z_{source}	31.74 Ω
System Frequency	60 Hz
Filter	L = 10 mH, C = 50 µF
R_{load}	19.044 Ω (0.5 pu)
Switching Frequency	2700 Hz

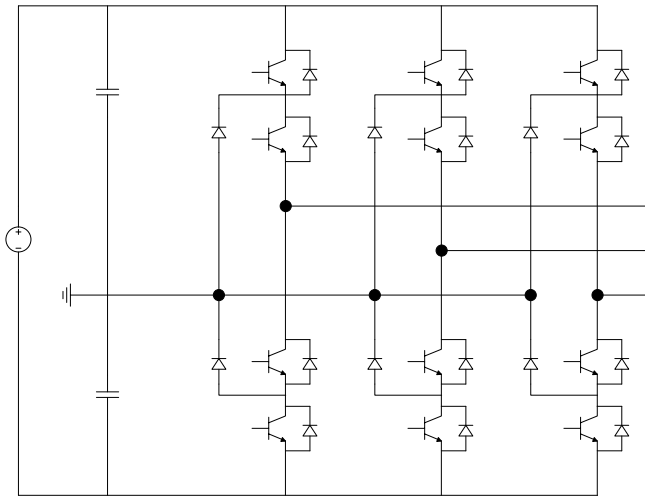

Figure 3-2. NPC circuit topology with 3-levels.

The 3-level NPC is controlled by a closed-loop current controls scheme. More specifically, it is also called PQ closed-loop voltage oriented control based on the synchronous *dq* frame [27]. A diagram of the signal flow is shown in Figure 3-3. The control is derived from performing KVL at the output of the NPC in the *dq* frame and arriving at the equations

$$V_{td} - V_{pd} = L\frac{di_d}{dt} - L\omega i_q + Ri_d, \tag{3-1}$$

$$V_{tq} - V_{pq} = L\frac{di_q}{dt} + L\omega i_d + Ri_q. \tag{3-2}$$

The equations are traditionally written with the inductor and derivative on the left hand side of the equation with all other terms on the right hand side, which leads to

$$L\frac{di_d}{dt} = L\omega i_q - Ri_d + V_{td}, \tag{3-3}$$

$$L\frac{di_q}{dt} = -L\omega i_d - Ri_q + V_{tq}. \tag{3-4}$$

Equations (3-3) and (3-4) are then manipulated further, ultimately leading to the creation of the structure shown in Figure 3-3. The voltage references at the output of the control diagram are used to create the firing pulses for the switches of the NPC.

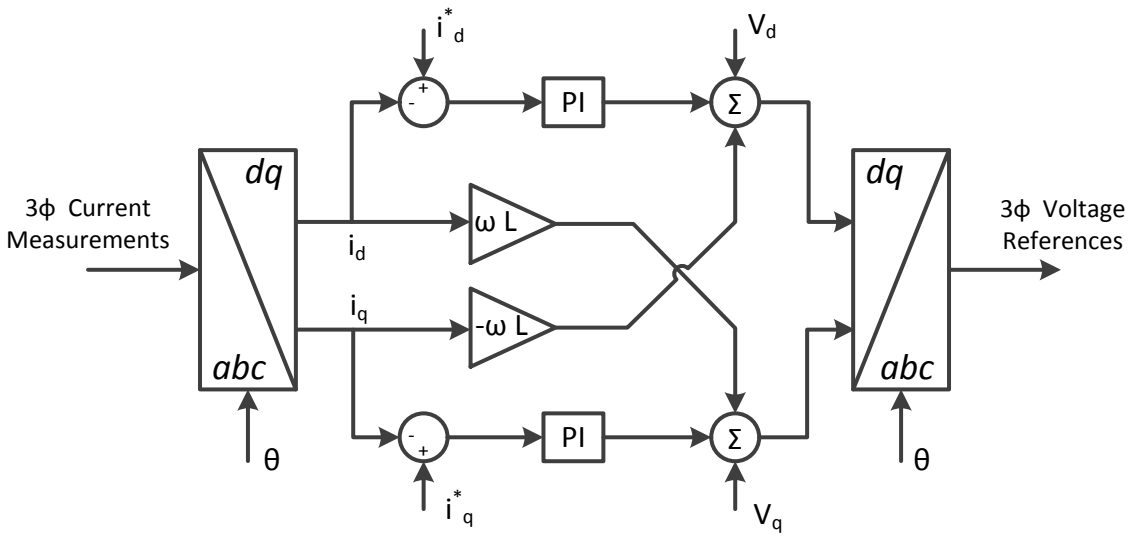

Figure 3-3. Closed-loop current control.

The theta value used for the *dq* transformations in the current control comes from a custom PLL that is a slight deviation from the traditional approach and appears in Figure 3-4.

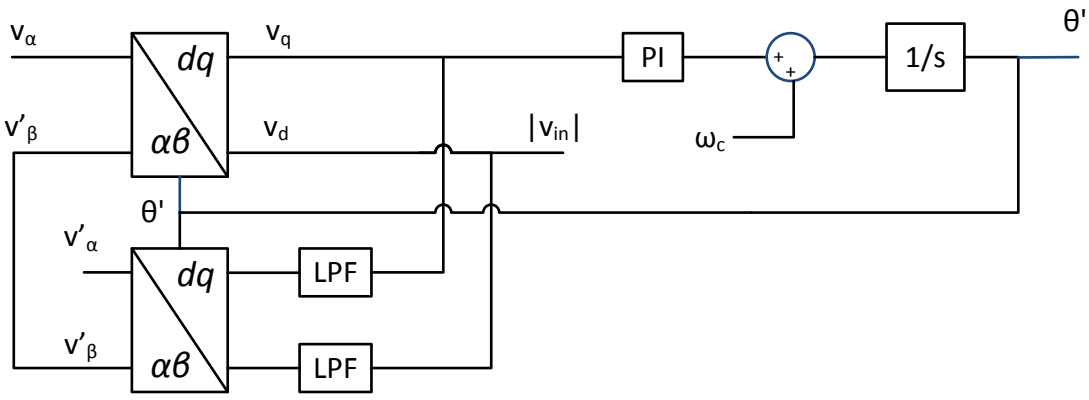

Figure 3-4. PLL Structure.

The PLL is based on the inverse Park transform going from the $\alpha\beta$ to the dq frame. The equation is of the form

$$v_{\alpha\beta} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \cos(\theta') & -\sin(\theta') \\ \sin(\theta') & \cos(\theta') \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix}. \quad (3\text{-}5)$$

A custom method was implemented rather than using the built-in PSCAD module so that dynamics within the PLL itself could be observed. The PLL scheme itself was chosen due to its use of in-quadrature signals in the form of the $\alpha\beta$ to the dq transformations making it applicable to three-phase systems and also because it eliminates a 90° phase shift that is found in other methods. It was also straightforward to implement in PSCAD.

4.0 PLL STABILITY ANALYSIS

They key issue being investigated in this dissertation is the effect that the PLL has on the stability of the remaining system. In this case, the system is composed of a Thévenin equivalent circuit that represents a weak source, which is the grid itself with its impedance. The weak source is more susceptible to faults and stability issues. This can have an effect on the PLL used in the VSC leading to a cascading problem that ultimately causes the system to go unstable and result in outages.

4.1 BRIEF OVERVIEW OF SIGNAL FLOW

Before outlining the mathematical analysis carried out, a high level overview of the flow of how the measurements and control parameters in the system interact with each other will be explained. Perturbations in the system grid voltage measurements feed into the control parameters and this is ultimately where the gains of the PLL control can have an effect on the output of the VSC. An outline can be created following the labels sequentially in Figure 4-1. A voltage perturbation from the grid system voltage (Location 1) is measured and converted into the *dq* domain. These voltages are then used as the inputs for the PLL (Location 2) to generate the angle necessary for conversion between the system *dq* domain to the converter *dq* domain. At the output of the PLL (Location 3), a reference angle is generated and used by the transformation blocks that feed into the controller. These transformation blocks are located at (Location 4a and 4b). The block at (Location 4a) feeds

signals into the controller block whereas the block at (Location 4b) transforms the output signals of the controller back into the system *dq* domain.

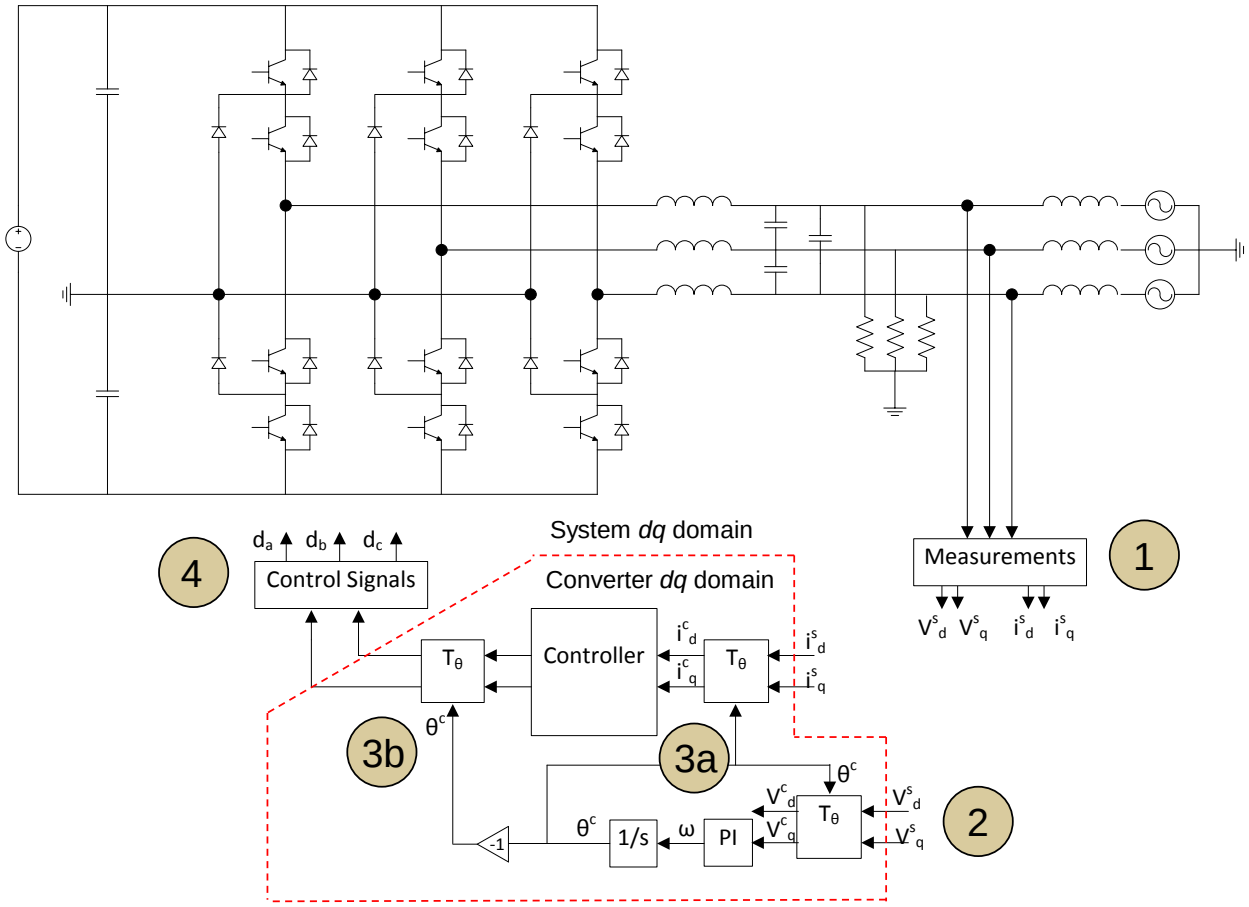

Figure 4-1. Signal flow of control parameters.

4.2 DERIVATION AND ANALYSIS OF OUTPUT IMEPDANCE

An initial hurdle with performing an analysis that includes the effects of the PLL is the inherent non-linear properties that are present. These properties can be linearized by use of the average model of the VSC. The different effects can then be found by decomposing the system

into single-input-single-output (SISO) transfer functions, which can then be organized in a diagram that reflects the system mathematically [28][29]. This is shown in Figure 4-2.

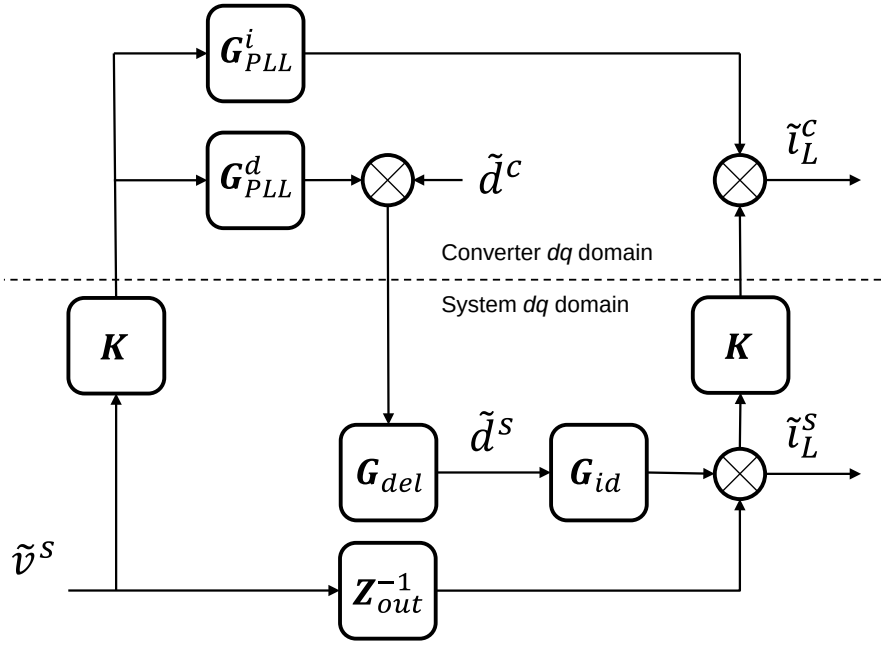

Figure 4-2. Diagram including the effect of the PLL on the output impedance.

The transfer functions are determined going one step further by making use of the small signal model [13][30]. Some of the transfer functions shown in Figure 4-2 can be attained by the VSC small signal model and include duty ratio to inductor current ($\boldsymbol{G_{id}}$), and the open loop output impedance ($\boldsymbol{Z_{out}}$). The measurement filters ($\boldsymbol{K}$) and delay from pulse-width modulation (PWM) control ($\boldsymbol{G_{del}}$) are standard equations that require no derivation and will be discussed later in this section. Additional transfer functions are needed to represent the effects of the PLL ($\mathbf{G}^{\mathrm{i}}_{\mathrm{PLL}}$ and $\mathbf{G}^{\mathrm{d}}_{\mathrm{PLL}}$) and will be derived in this section. [28]

These transfer functions can be found by analyzing the small signal model that was outlined in Chapter 2.2. The equivalent circuit for the VSC is replicated again in Figure 4-3 for easier access when showing the transfer function derivations.

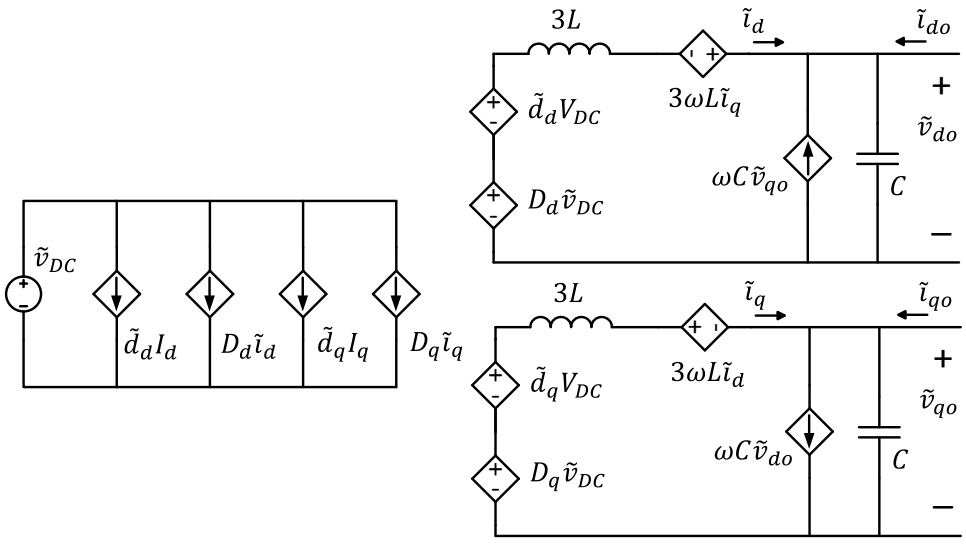

Figure 4-3. VSC small-signal equivalent circuit model.

The most essential transfer function to acquire first is the output impedance as this will be the foundation of the analysis and it will become more complex as the effects of the various control loops are added to it. It is found by setting the both the duty ratios, d_d and d_q, to zero as well as the DC source, v_{dc}. This eliminates the left-hand circuit in Figure 4-3 since the source is zero therefore no current is flowing. The resulting right-hand circuit is simplified to that shown in Figure 4-4.

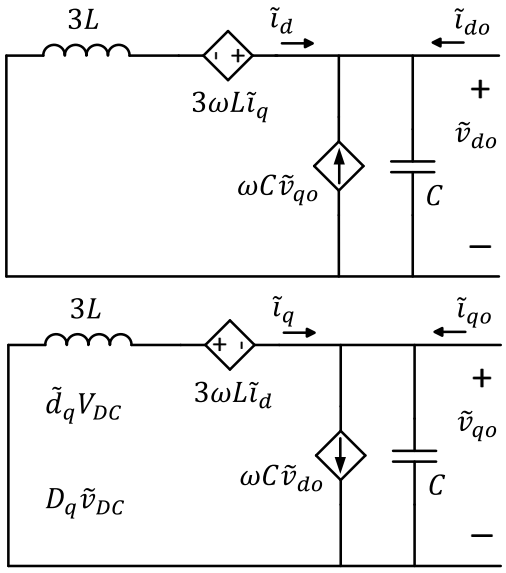

Figure 4-4. Resulting small-signal equivalent circuit for Z_{out}.

From this equivalent circuit, the output impedance can be found by KCL and KVL to get the equations,

$$\tilde{\imath}_d + \omega C\tilde{v}_{oq} + \tilde{\imath}_{od} - sC\tilde{v}_{od} = 0, \tag{4-1}$$

$$\tilde{\imath}_q - \omega C\tilde{v}_{od} + \tilde{\imath}_{oq} - sC\tilde{v}_{oq} = 0, \tag{4-2}$$

$$3\tilde{\imath}_d Ls - 3\omega L\tilde{\imath}_q + \tilde{v}_{od} = 0, \tag{4-3}$$

$$3L\tilde{\imath}_q s + 3\omega L\tilde{\imath}_d + \tilde{v}_{oq} = 0. \tag{4-4}$$

Solving these equations for $\tilde{\imath}_{od}$ to $\tilde{v}_{od}$, $\tilde{\imath}_{oq}$ to $\tilde{v}_{od}$, $\tilde{\imath}_{od}$ to $\tilde{v}_{oq}$, and $\tilde{\imath}_{oq}$ to $\tilde{v}_{oq}$ will net the final transfer function matrix for $\boldsymbol{Z}_{out}$. The four transfer functions are the following,

$$\frac{\tilde{v}_{od}}{\tilde{\imath}_{od}} = \frac{G_z(9\omega^2L^2 - G_z - 3s^2LCG_z)}{(3sL + sCG_z)(9\omega^2L^2 - G_z - 3s^2LCG_z) - 3sL(3\omega L - \omega CG_z)^2}, \tag{4-5}$$

$$\frac{\tilde{v}_{od}}{\tilde{\imath}_{oq}} = -\frac{3sLG_z(-3\omega L + \omega CG_z)}{(3sL + sCG_z)(9\omega^2L^2 - G_z - 3s^2LCG_z) - 3sL(3\omega L - \omega CG_z)^2}, \tag{4-6}$$

$$\frac{\tilde{v}_{oq}}{\tilde{\imath}_{od}} = -\frac{\tilde{v}_{od}}{\tilde{\imath}_{oq}}, \tag{4-7}$$

$$\frac{\tilde{v}_{oq}}{\tilde{\imath}_{oq}} = \frac{\tilde{v}_{od}}{\tilde{\imath}_{od}}, \tag{4-8}$$

where $G_z = 9L^2(s^2 + \omega^2)$.

A bode plot and pole-zero plot of the four transfer functions that make up $\boldsymbol{Z}_{out}$ are shown below. The following notation is used for the four parts of the matrix,

$$Z_{dd} = \frac{\tilde{v}_{od}}{\tilde{\imath}_{od}}, \tag{4-9}$$

$$Z_{dq} = \frac{\tilde{v}_{od}}{\tilde{\imath}_{oq}}, \tag{4-10}$$

$$Z_{qd} = \frac{\tilde{v}_{oq}}{\tilde{\imath}_{od}}, \tag{4-11}$$

$$Z_{qq} = \frac{\tilde{v}_{oq}}{\tilde{\imath}_{oq}}. \tag{4-12}$$

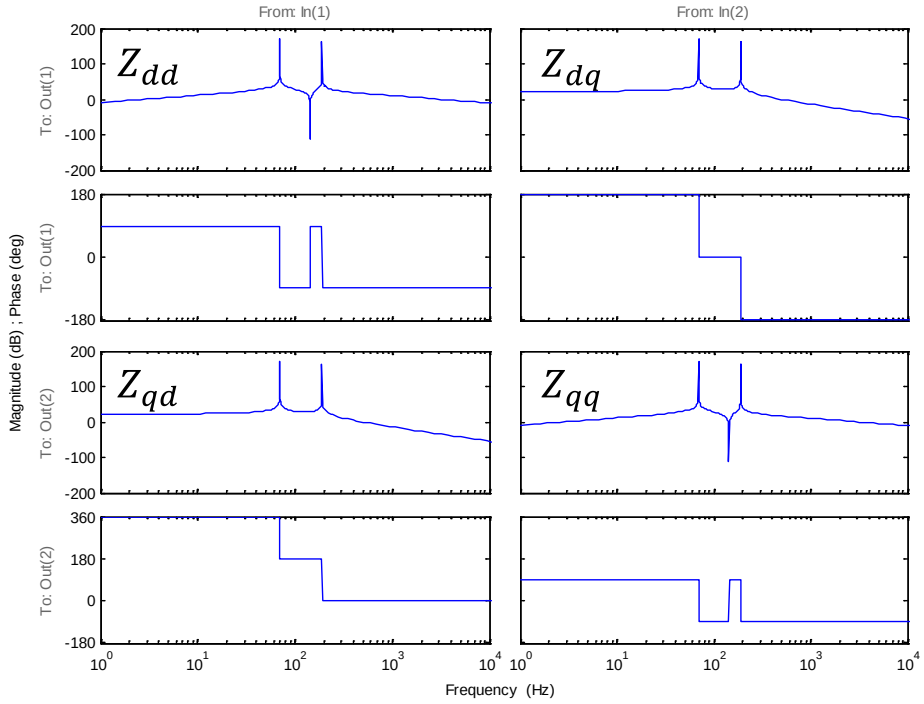

Figure 4-5. Bode plots of the Zout transfer function matrix.

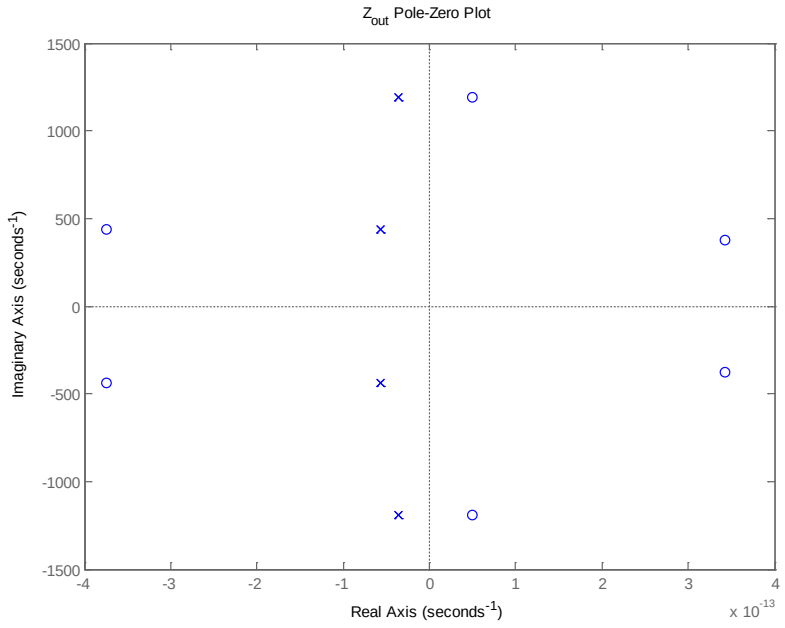

Figure 4-6. Pole-Zero mapping for $\boldsymbol{Z_{out}}$.

The pole-zero placement in Figure 4-6 shows that there are no poles in the right-hand plane (RHP) therefore the output impedance not considering the effects of the control systems is stable.

4.3 DERIVATION AND ANALYSIS OF OUTPUT IMEPDANCE INCLUDING THE EFFECTS OF THE PLL

The transfer function matrix $\boldsymbol{G}_{id}$ needs to be derived as well. This again is the transfer functions from duty cycle to inductor current. A breakdown of how to find $\tilde{\imath}_d/\tilde{d}_d$ and $\tilde{\imath}_d/\tilde{d}_q$ was discussed in Chapter 2.2. The transfer functions $\tilde{\imath}_q/\tilde{d}_d$ and $\tilde{\imath}_q/\tilde{d}_q$ can be found in a similar matter. The only change is the **C** matrix has a value of '1' in the second row rather than the first. The results can be found using Equation (2-27). Alternatively, it is noted that the following equalities hold true as well having already performed the calculations,

$$\frac{\tilde{\imath}_q}{\tilde{d}_d} = -\frac{\tilde{\imath}_d}{\tilde{d}_q}, \tag{4-13}$$

$$\frac{\tilde{\imath}_q}{\tilde{d}_q} = \frac{\tilde{\imath}_d}{\tilde{d}_d}. \tag{4-14}$$

The equations for $\boldsymbol{K}$ and $\boldsymbol{G}_{del}$ are straightforward and do not require any sort of derivation. The transfer function matrix $\boldsymbol{K}$ is a low-pass filter for the measured *dq* voltage and current signals from the system. The filter cleans up the signal of any high frequency components to avoid any obscurities when going through the control system. It has the form

$$\boldsymbol{K} = \begin{bmatrix} \dfrac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} & 0 \\ 0 & \dfrac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \end{bmatrix} \tag{4-15}$$

where ω_n is the natural frequency and ζ is the damping coefficient.

To represent the time delay, $\boldsymbol{G}_{del}$, due to the control and (PWM), a first order Padé approximation is used. The transfer function is

$$\boldsymbol{G_{del}} = \begin{bmatrix} \dfrac{1 - \frac{\tau}{2}s}{1 + \frac{\tau}{2}s} & 0 \\ 0 & \dfrac{1 - \frac{\tau}{2}s}{1 + \frac{\tau}{2}s} \end{bmatrix} \tag{4-16}$$

where τ is the time delay.

The final transfer function matrices needed to analyze the effect of the PLL are the small-signal equations of the PLL itself. Following the steps taken in [28], the process to find the influence of the PLL is as follows:

Begin making the assumption that the duty ratio, voltage, and current vectors are equal in the system domain and the converter domain in steady-state. If this is the case, the angle between them could also be assumed to be zero. To show this mathematically, first a transformation matrix to change between the system domain and converter domain is introduced that includes the effect of a small signal perturbation and is

$$\boldsymbol{T_\theta} = \begin{bmatrix} \cos(\theta + \tilde{\theta}) & \sin(\theta + \tilde{\theta}) \\ -\sin(\theta + \tilde{\theta}) & \cos(\theta + \tilde{\theta}) \end{bmatrix}. \tag{4-17}$$

If the phase angle between the two domains is zero during steady-state, the voltage vectors would have the relationship of

$$\vec{V}^c = \begin{bmatrix} \cos(\tilde{\theta}) & \sin(\tilde{\theta}) \\ -\sin(\tilde{\theta}) & \cos(\tilde{\theta}) \end{bmatrix} \vec{V}^s. \tag{4-18}$$

The small signal perturbation from the PLL is close to zero so by using small-angle approximation on Equation (4-18), it can be simplified to

$$\vec{V}^c \approx \begin{bmatrix} 1 & \tilde{\theta} \\ -\tilde{\theta} & 1 \end{bmatrix} \vec{V}^s. \tag{4-19}$$

Expanding the vectors to show the steady-state and small signal perturbations, multiplying the right-hand side matrix to the system voltage vector, and canceling the steady-state terms for the converter and system voltages yields

$$\begin{bmatrix} V_d^c + \widetilde{v_d^c} \\ V_q^c + \widetilde{v_q^c} \end{bmatrix} \approx \begin{bmatrix} 1 & \tilde{\theta} \\ -\tilde{\theta} & 1 \end{bmatrix} \begin{bmatrix} V_d^s + \widetilde{v_d^s} \\ V_q^s + \widetilde{v_q^s} \end{bmatrix}, \tag{4-20}$$

$$\begin{bmatrix} \widetilde{v_d^c} \\ \widetilde{v_q^c} \end{bmatrix} \approx \begin{bmatrix} V_q^s \tilde{\theta} + \widetilde{v_d^s} \\ -V_d^s \tilde{\theta} + \widetilde{v_q^s} \end{bmatrix} \begin{bmatrix} V_d^s + \widetilde{v_d^s} \\ V_q^s + \widetilde{v_q^s} \end{bmatrix}. \tag{4-21}$$

Substituting Equation (2-15) in for the small signal perturbation of the angle $\tilde{\theta}$, the relationship between the system domain q channel voltage and the PLL is found to be

$$\tilde{\theta} = \frac{LF}{s + V_d^s LF} \widetilde{v_q^s}. \tag{4-22}$$

For use in the equations for the relationships between the PLL to current and duty ratio, it will be set that

$$G_{PLL} = \frac{LF}{s + V_d^s LF}. \tag{4-23}$$

Since the input of the PLL is the system voltage and the resulting angle $\tilde{\theta}$ is used to transform the duty ratio and currents between the system domain and converter domain, a similar analysis can be done with them that will include Equation (4-23). For the duty ratio, the resulting equation is

$$\begin{bmatrix} \widetilde{d_d^c} \\ \widetilde{d_q^c} \end{bmatrix} \approx \begin{bmatrix} 0 & D_q^s G_{PLL} \\ 0 & -D_d^s G_{PLL} \end{bmatrix} \begin{bmatrix} \widetilde{v_d^s} \\ \widetilde{v_q^s} \end{bmatrix} + \begin{bmatrix} \widetilde{d_d^s} \\ \widetilde{d_q^s} \end{bmatrix}. \tag{4-24}$$

From Equation (4-24), the transfer function matrix is found to be

$$\boldsymbol{G_{PLL}^d} = \begin{bmatrix} 0 & D_q^s G_{PLL} \\ 0 & -D_d^s G_{PLL} \end{bmatrix}. \tag{4-25}$$

In a similar fashion, the effect of the PLL on the transformation of the currents between domains is

$$\begin{bmatrix} \widetilde{\imath_d^c} \\ \widetilde{\imath_q^c} \end{bmatrix} \approx \begin{bmatrix} 0 & I_q^s G_{PLL} \\ 0 & -I_d^s G_{PLL} \end{bmatrix} \begin{bmatrix} \widetilde{v_d^s} \\ \widetilde{v_q^s} \end{bmatrix} + \begin{bmatrix} \widetilde{\imath_d^s} \\ \widetilde{\imath_q^s} \end{bmatrix}. \tag{4-26}$$

The transfer function matrix for the effect of the PLL on the current transformation is

$$\boldsymbol{G_{PLL}^i} = \begin{bmatrix} 0 & I_q^s G_{PLL} \\ 0 & -I_d^s G_{PLL} \end{bmatrix}. \tag{4-27}$$

With all of the transfer function matrices shown in Figure 4-2 derived, the effect of the PLL on the output impedance $\boldsymbol{Z}_{out}$ can be found. By inspection, it can be seen that

$$\boldsymbol{Z}_{out\_PLL}^{-1} = \boldsymbol{Z}_{out}^{-1} + \boldsymbol{G}_{id}\boldsymbol{G}_{del}\boldsymbol{G}_{PLL}^{d}\boldsymbol{K}. \tag{4-28}$$

The diagram in Figure 4-2 is based originally on the derivation using the admittance ([28]) so it is important to invert the equation found to ultimately get the equation for the impedance as in Equation (4-29).

$$\boldsymbol{Z}_{out\_PLL} = \left(\boldsymbol{Z}_{out}^{-1} + \boldsymbol{G}_{id}\boldsymbol{G}_{del}\boldsymbol{G}_{PLL}^{d}\boldsymbol{K}\right)^{-1}. \tag{4-29}$$

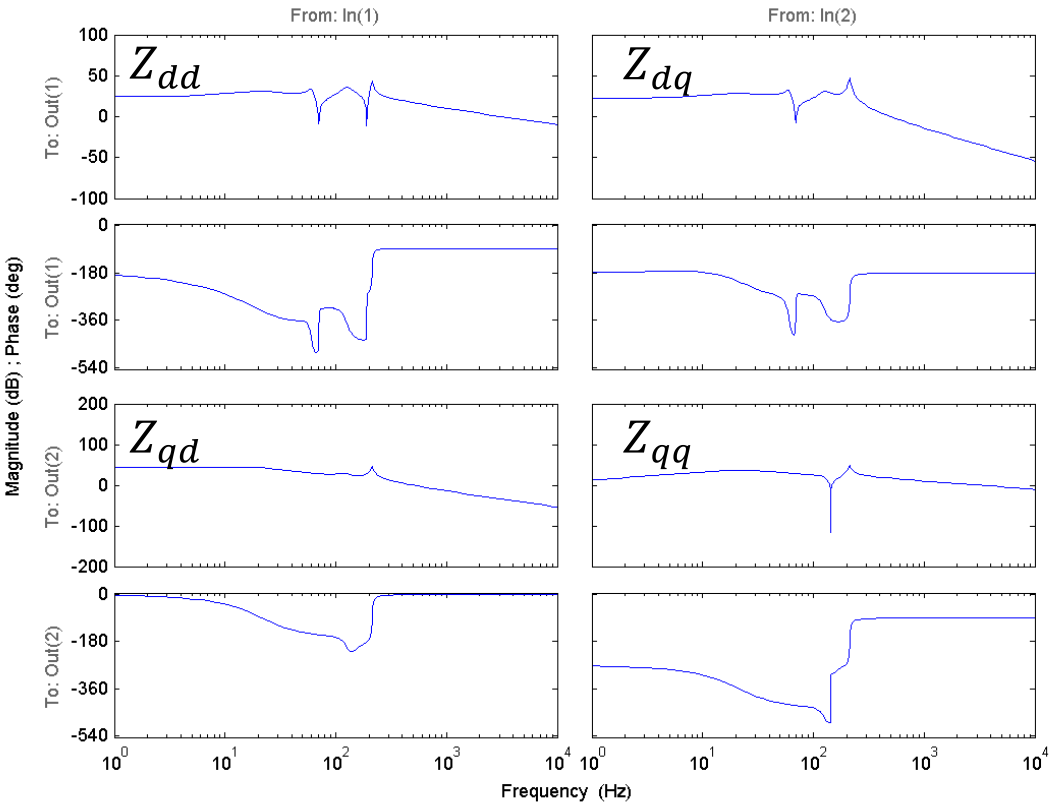

Figure 4-7. Bode plots of $\boldsymbol{Z}_{out}$ with PLL dynamics considered.

Of note in Figure 4-7 is the phase of $\boldsymbol{Z}_{dd}$, which is at -180° in the low frequencies after the effects of the PLL are added. Comparing to Figure 4-5, the phase was acting as an inductor at -90° and is now acting as a negative resistance. This has been documented in other literature [29][31].

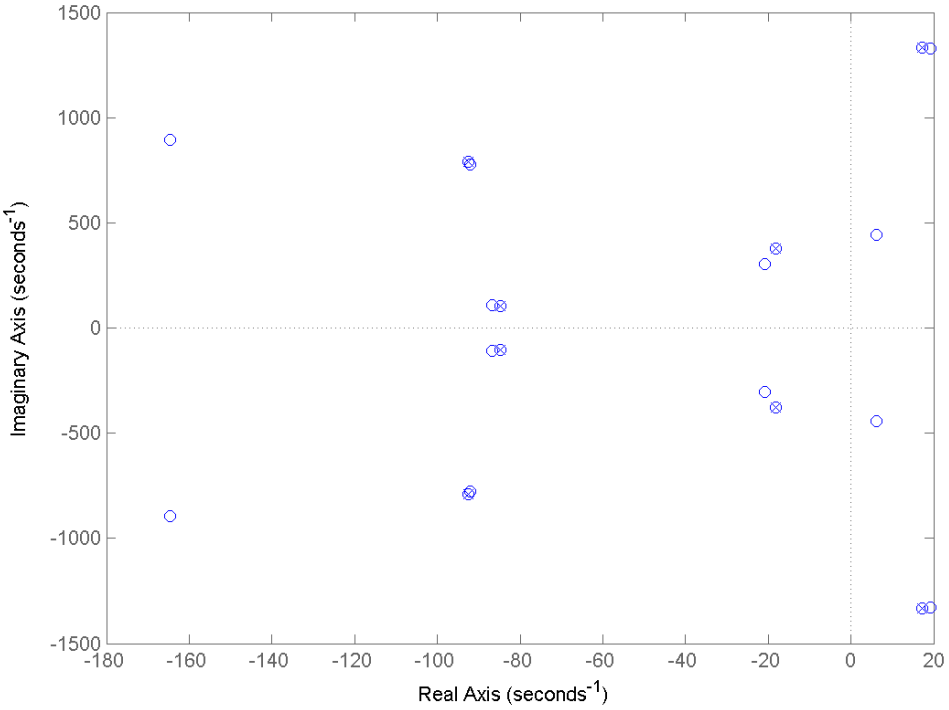

Figure 4-8. Pole-Zero mapping of $\boldsymbol{Z}_{out}$ with PLL dynamics considered.

4.3.1 Stability of the System Considering a Large SCR

Using the theory outlined in Chapter 2.4.1 and the derived output impedance that includes the effects of the PLL, a stability analysis of the complete system is now able to be carried out. The elegance of the stability criteria, a simple ratio of the grid impedance over the output impedance of the VSC, allows for a range of values to be explored while quickly being able to see if stability is maintained. Of particular interest is the effect of the value of the SCR. The SCR determines the value of the impedance of the grid. The grid impedance will be modeled as an inductance. The question of what values are suitable for the system is one of the goals of this work. This type of relationship between the PLL and SCR has been carried out in [11] by analyzing the eigenvalues of the system. A different analysis is performed in this dissertation by using the impedances of

the VSC and grid. The most useful plots are the pole-zero plots as well as the Nyquist stability. A value of 10 was used for the SCR as this corresponds to a stiff grid and will serve as a case where the PLL gains have no effect regardless of how large they are. The PLL gain K_i is equal to five times K_p.

Table 4-1. Stability Analysis Parameters for SCR = 10.

Parameter	**Value**
SCR	10
Grid inductance	10.1 mH
PLL Gain: K_p	10
PLL Gain: K_i	60

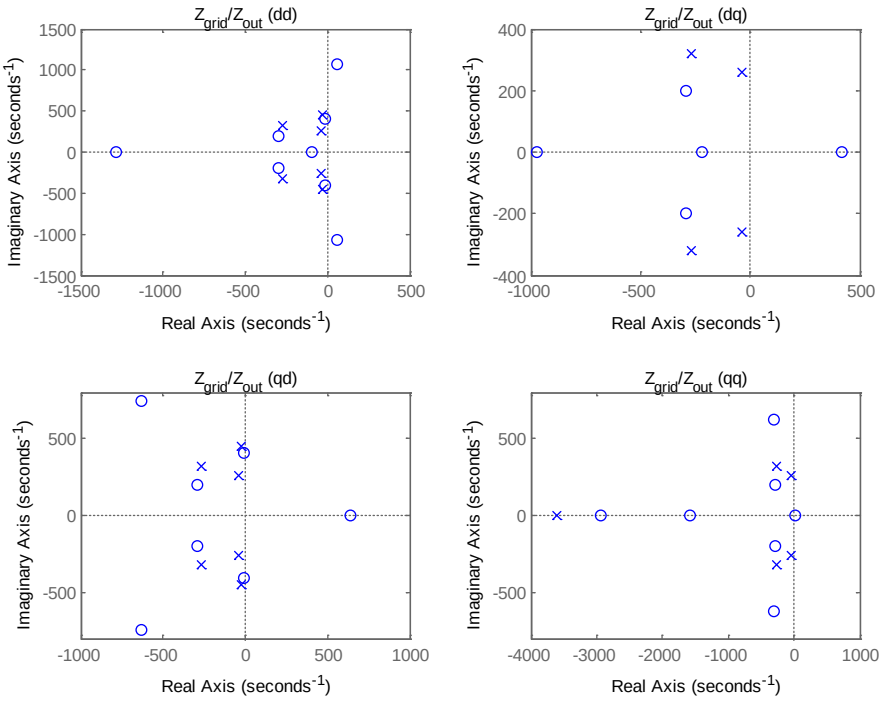

Figure 4-9. Pole-Zero mapping for SCR = 10.

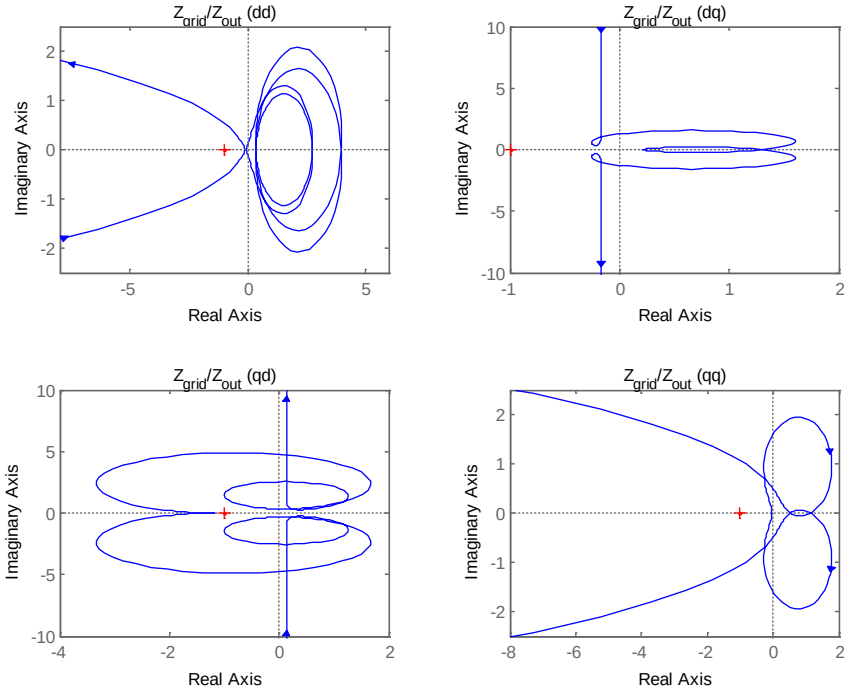

Figure 4-10. Nyquist plots for SCR = 10.

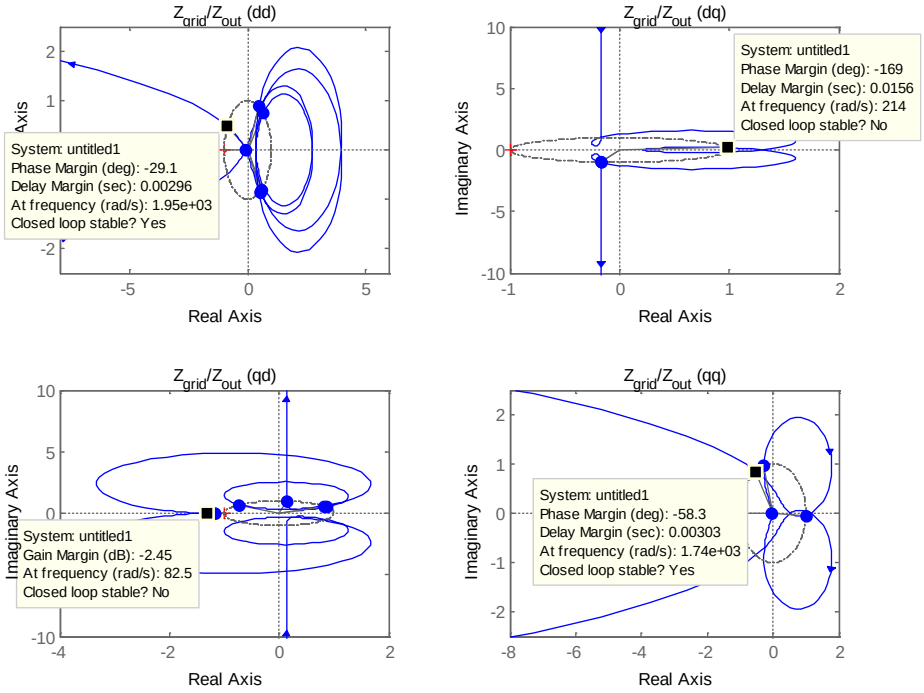

Figure 4-11. Nyquist plots for SCR = 10 with stability results.

The Nyquist plots are important for analyzing stability and so each plot will be shown individually in Appendix A, so a higher resolution figure is available.

The results for an SCR value of 10 are the most telling in Figure 4-11 since it shows whether the transfer function is closed loop stable. It can be seen that the stable cases are the *dd* and *qq* channels whereas the coupled channels of *dq* and *qd* are not stable. It will be shown soon that the SCR and PLL values do not seem to affect the coupled channels of *dq* and *qd*. It is not currently known why this is and will be designated to future work. The channels always appeared unstable regardless of the SCR and PLL values used. The instability is likely being caused by other components and/or parameters of the system. The focus will be on the *dd* and *qq* channels for the remainder of the analysis.

To demonstrate that the PLL gains have no effect on the SCR when it is suitably large, they were increased by a magnitude of two and the results are shown below with the new values shown in Table 4-2.

Table 4-2. Stability Analysis Parameters for SCR = 10 with increased PLL gains.

Parameter	**Value**
SCR	10
Grid inductance	10.1 mH
PLL Gain: K_p	1000
PLL Gain: K_i	6000

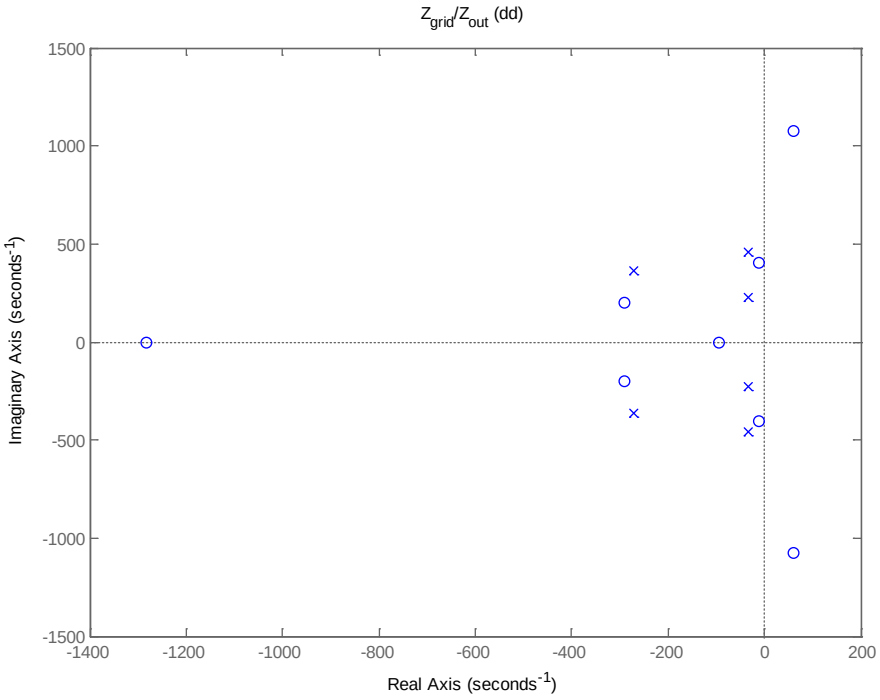

Figure 4-12. Pole-zero mapping for *dd* channel (SCR = 10, K_p = 1000, K_i = 6000).

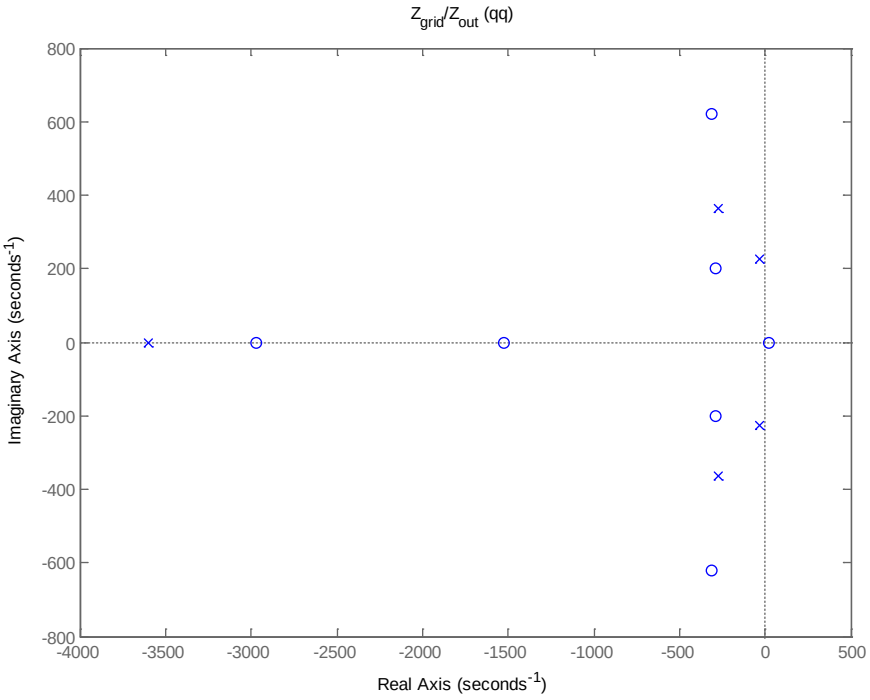

Figure 4-13. Pole-zero mapping for *qq* channel (SCR = 10, K_p = 1000, K_i = 6000).

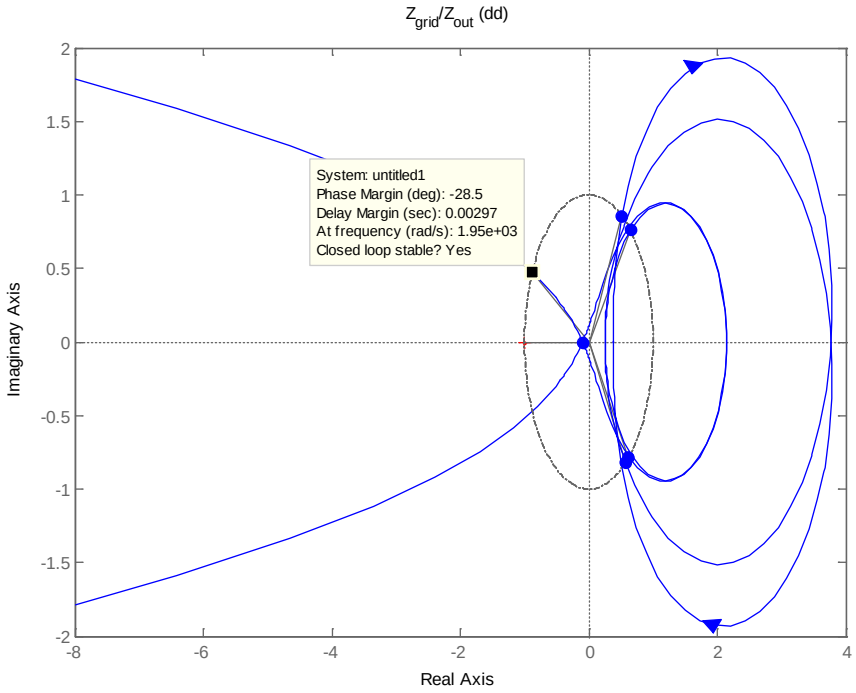

Figure 4-14. Nyquist plot for *dd* channel (SCR = 10, K_p = 1000, K_i = 6000).

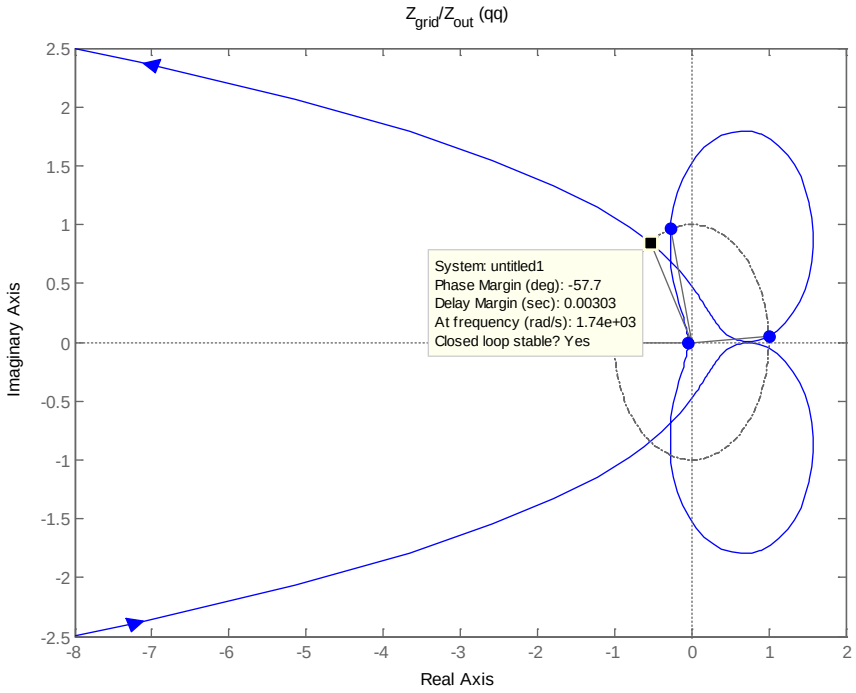

Figure 4-15. Nyquist plot for *qq* channel (SCR = 10, K_p = 1000, K_i = 6000).

As expected, increasing the PLL gains to very large values did not have an effect on stability at the SCR of 10.

4.3.2 Stability of the System Considering a Small SCR

The next set of simulations and values will demonstrate a similar effect but will show that with a very low SCR, the PLL gains are unable to move the system from an unstable state.

Table 4-3. Stability Analysis Parameters for determining minimum SCR.

Parameter	**Value**
SCR	0.971
Grid inductance	104 mH
PLL Gain: K_p	1
PLL Gain: K_i	6

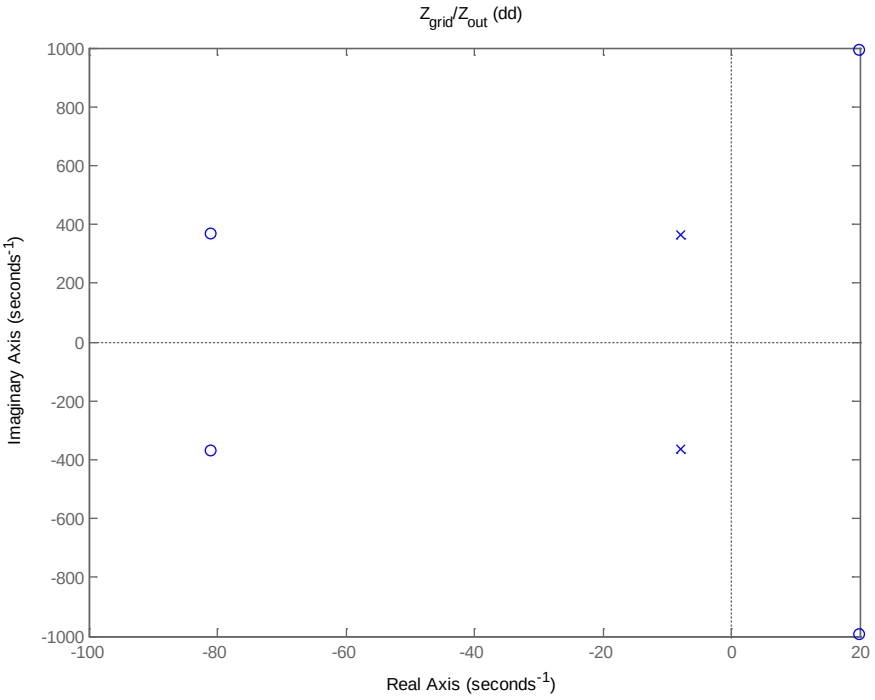

Figure 4-16. Pole-zero mapping for *dd* channel (SCR = 0.971, K_p = 1, K_i = 6).

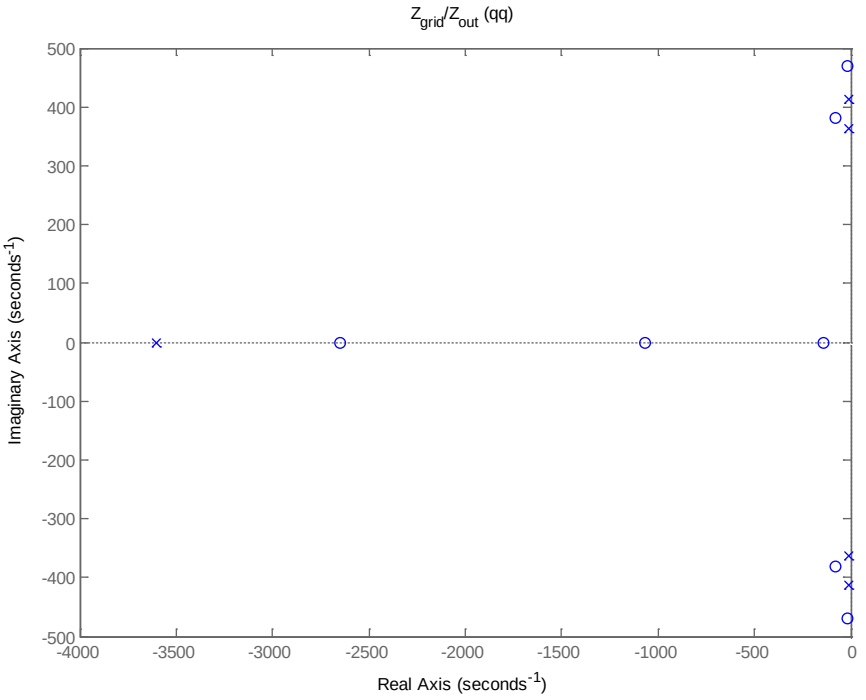

Figure 4-17. Pole-zero mapping for *qq* channel (SCR = 0.971, K_p = 1, K_i = 6).

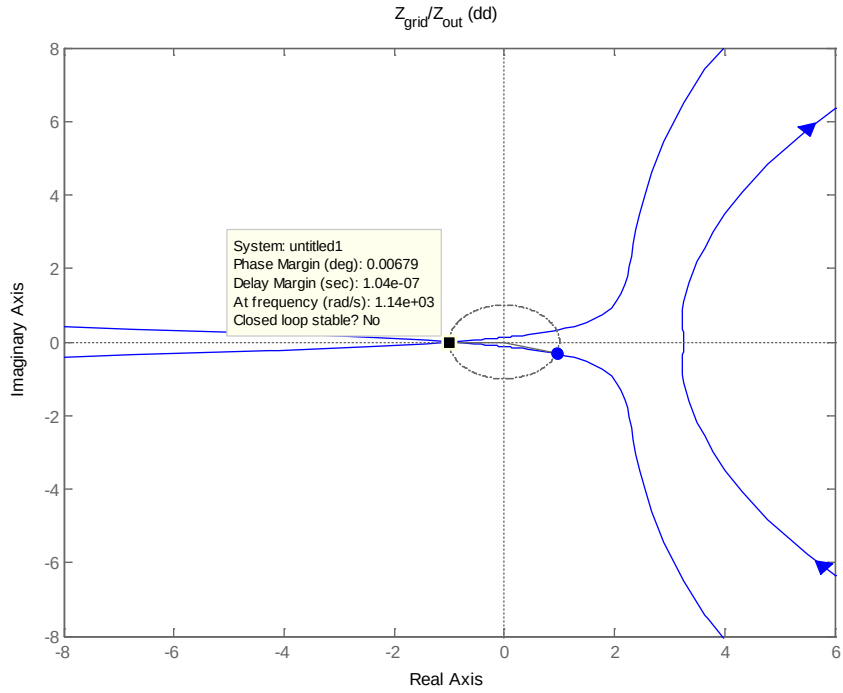

Figure 4-18. Nyquist plot for *dd* channel (SCR = 0.971, K_p = 1, K_i = 6).

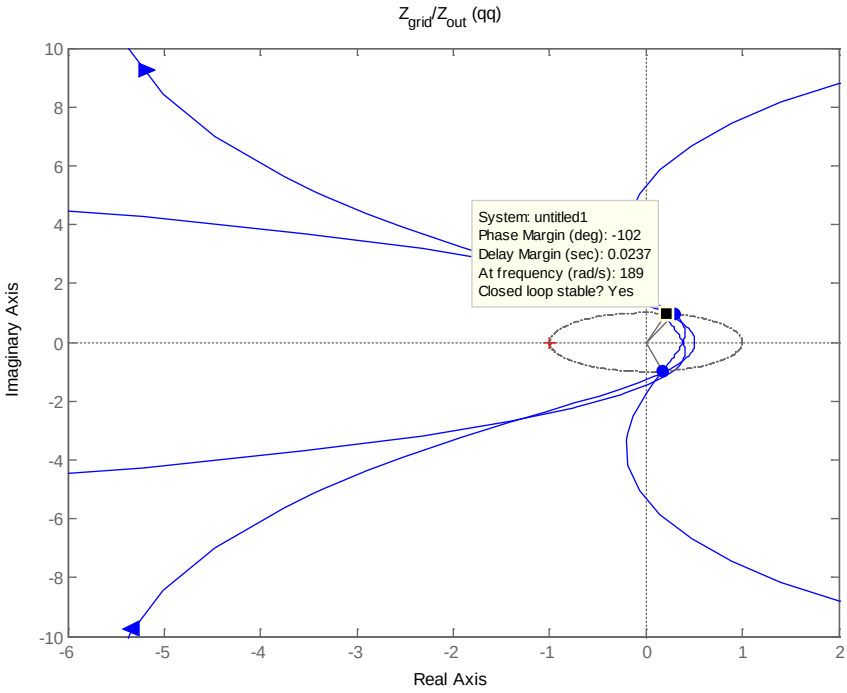

Figure 4-19. Nyquist plot for *qq* channel (SCR = 0.971, K_p = 1, K_i = 6).

The lowest, most reasonable PLL gain of K_p = 1, was maintained while determining the lowest SCR that would cause the system to be unstable. This was determined to be 0.971. It is possible that smaller PLL gains would result in the system being stable but this would result in very slow dynamics for the VSC control and is not realistic and therefore not tested. It is also of interest to note that while the *dd* channel becomes unstable for this value of SCR, the *qq* channel remains stable. The SCR was dramatically lowered (as low as 0.0001) to see if the *qq* channel would eventually become unstable but it continued to remain stable for all cases of SCR values. This is likely due to the fact that the *qq* channel has no poles or zeros in the right-hand plane.

With an upper and lower limit established for the SCR and PLL gains, a middle ground is of interest to find. While stability is maintained for the *dd* channel at low SCR values, the PLL gains are very small and this prevents the system from acting quickly to fluctuations. This dynamic response may be desired and so a compromise between the PLL gains and SCR will be investigated.

4.3.3 Stability Range Considering a Various SCR and PLL Gains

After running sets of simulations ranging from SCR values of 0.8 to 1.8, Figure 4-20 was created to reflect what PLL K_p gain values result in the *dd* channel being stable. There are three crossover points of interest. The first has already been identified at SCR = 0.972. This is the lowest possible SCR value to maintain stability with a PLL K_p gain value of 1. All values of SCR lower than 0.972 are unstable for the *dd* channel. The next is at SCR = 1.506. At this point, the largest value of K_p that is possible while still maintaining stability is K_p = 14. Lastly, the gain K_p has no realistic upper limit after SCR = 1.736. A K_p value of 50 is shown but this is simply to

keep the scale legible. Gain values for K_p greater than 100 were tested and stability was still maintained at these higher SCR values.

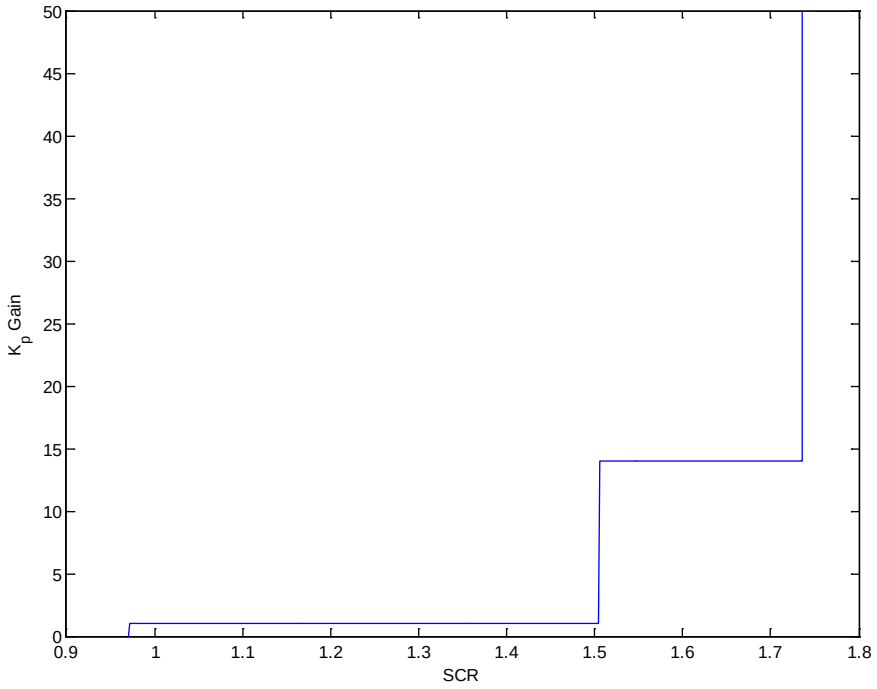

Figure 4-20. Stability range of SCRs with varying PLL K_p gain thresholds.

4.3.4 Stability Analysis using PSCAD Simulations

In order to check the validity of the mathematical model calculations performed and discussed in the previous sections, a second method of using the software package PSCAD was used. The system and its control were discussed in Chapter 3.0 A similar analysis was performed by varying the SCR and PLL gains. The parameters used are identical to those of the mathematical derivations, which again are in Table 3-1 for reference. The simulation is run out to a steady-state

operating point at which point the SCR and/or PLL gains are modified to observe their effect on the operation and stability of the system.

The first case is for a high SCR with large PLL gains. It was shown theoretically that the PLL gains could be very large without the system becoming unstable. This was simulated in PSCAD. The frequency of the PLL is shown in Figure 4-21 with a gain of K_p = 100. The frequency deviates slightly from 60 Hz around ±0.03 Hz, which is within operating conditions. The voltage measured across the load in Figure 4-22 shows a very smooth curve.

The PLL gain was increased to a much larger value of K_p = 1000 in Figure 4-23. While the system maintains stability and reaches a steady-state, the frequency deviation is larger at ±0.13 Hz. A steady-state frequency with this type of fluctuation is not desirable but whether this is within operating regulations depends on the electric system area and what it has deemed acceptable. So while the system is able to maintain stability under very large PLL gains, it is likely not necessary to need such a rapid response from the PLL. Most of the time the system is operating near 60 Hz and only slight deviations need to be accounted for by the PLL.

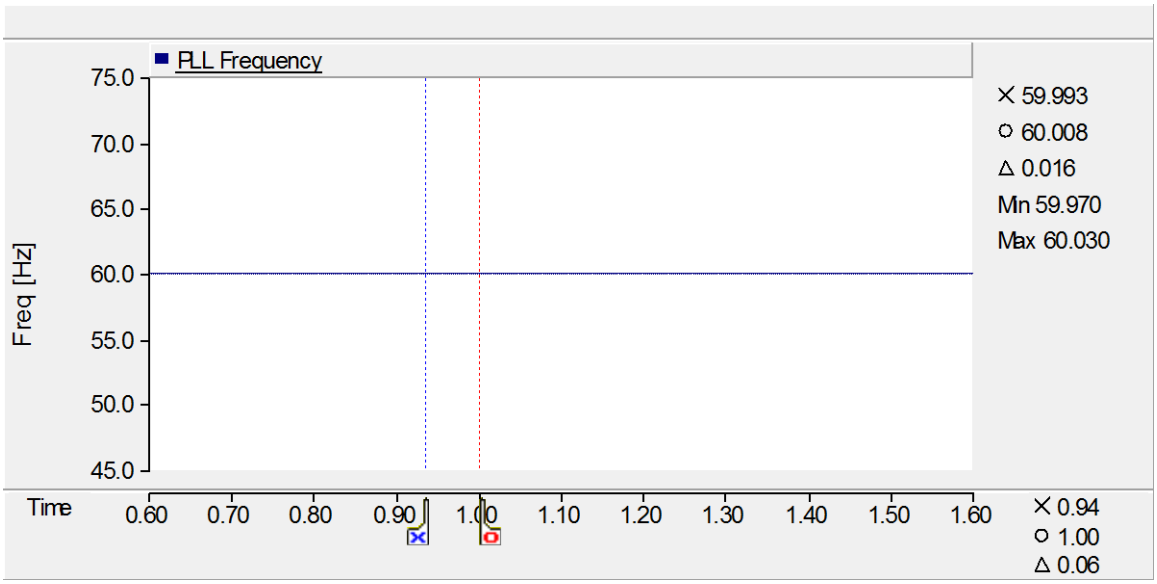

Figure 4-21. Output Frequency of the PLL with moderately large gains (K_p = 100).

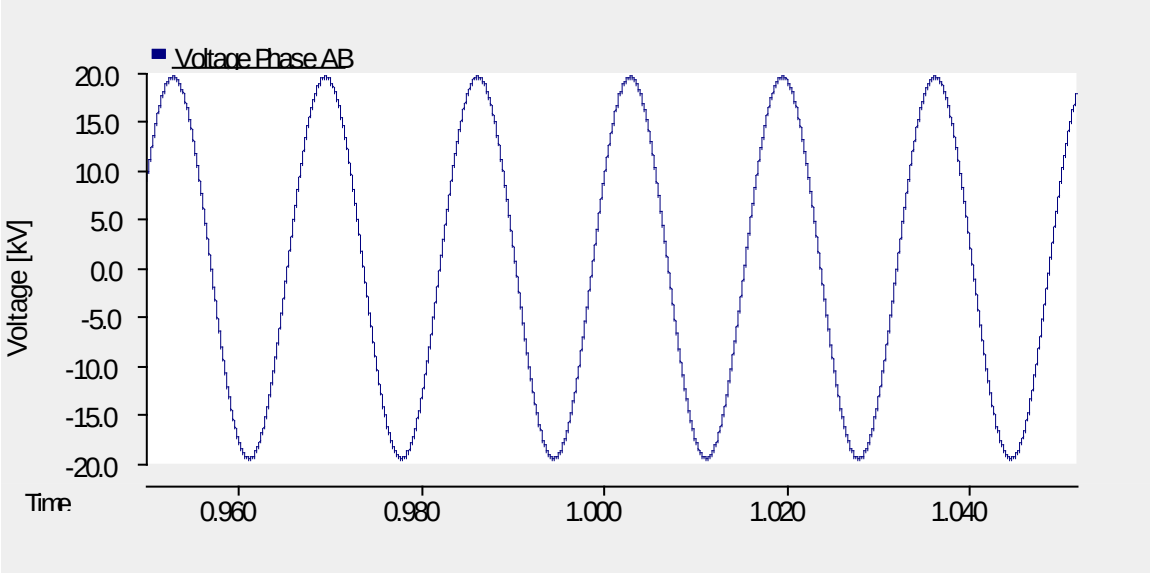

Figure 4-22. Voltage across the load (K_p = 100).

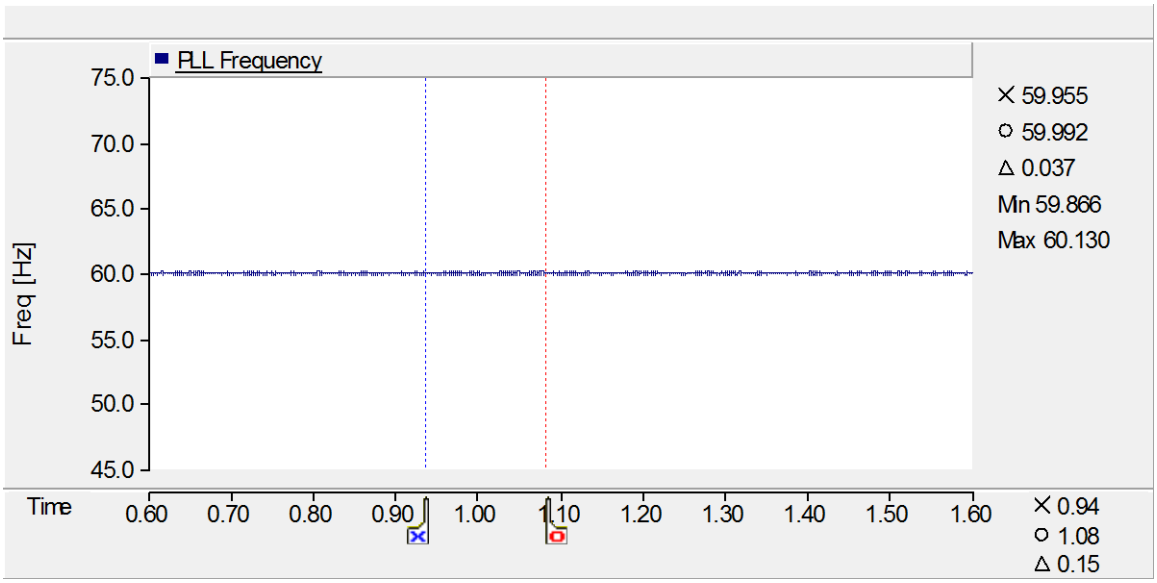

Figure 4-23. Output Frequency of the PLL with very large gains (K_p = 1000).

The next case investigated was using a low SCR value to show that even with very low gains on the PLL the system would become unstable and not operate as expected. This was accomplished by running the simulation to a steady-state using a suitably large SCR value and

then changing it to the new low value. The change is similar to what may occur on the electric grid when an interconnection changed from being strong to being weak from changes happening within the system. The resulting frequency from the PLL is shown in Figure 4-24. As expected, the frequency becomes unstable and continues to drift from 60 Hz in an upward direction. The voltage measured across the grid in Figure 4-25 has harmonic content appearing in its waveform as well.

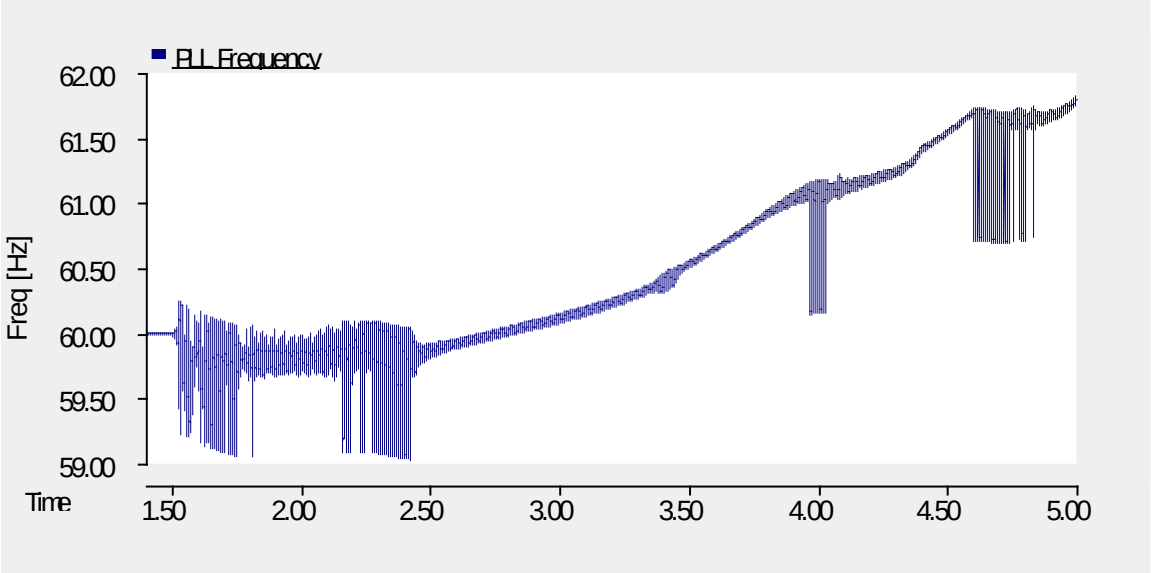

Figure 4-24. Frequency of the PLL with a small, unstable SCR.

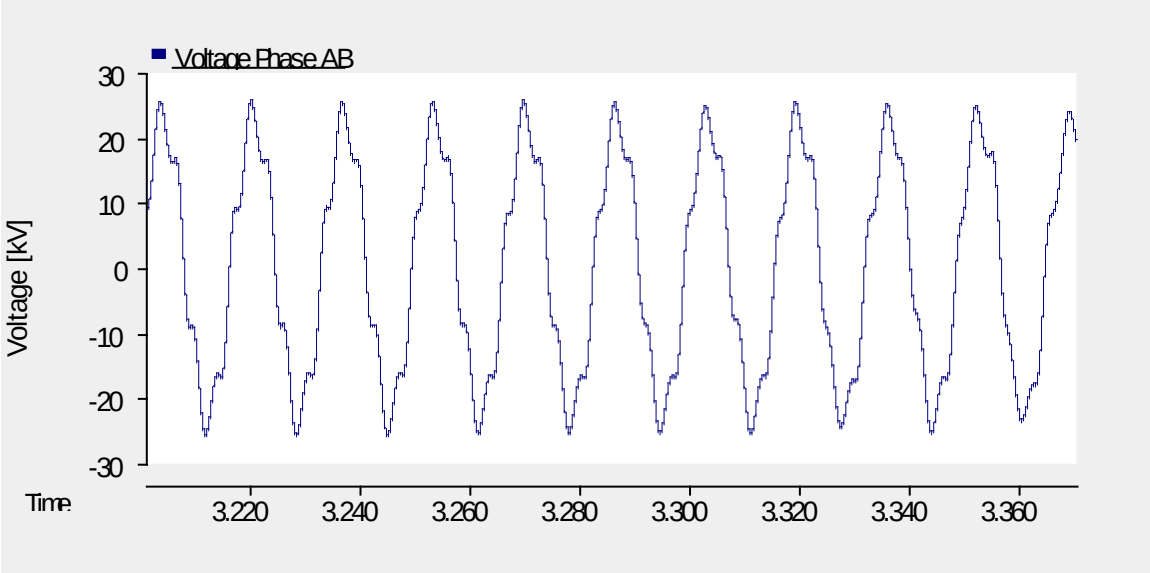

Figure 4-25. Voltage across the load for unstable SCR.

5.0 CONCLUSIONS

A system was modeled after a DG interconnection to a grid system that was represented as a Thévenin circuit. The output impedance was derived for the VSC that served as the DC-to-AC conversion of the DG source to supply a local load. The perturbations from the PLL were added to the output impedance to observe their effect when a weak grid connection was introduced. In order to determine the stability of the system, the Nyquist criterion was used for the ratio of the input impedance of the system grid over the output impedance of the VSC. Various SCR values and PLL gains were investigated to determine the critical point of stability. Any SCR above 1.73 was found to be unaffected by PLL gains and retained stability. On the other hand, a SCR value below 0.97 causes the system to be unstable regardless of PLL gains. The stability of the system at SCR values between these upper and lower thresholds is influenced by the PLL gains. Depending on the SCR value between 0.97 and 1.73, there is a limit on how large the PLL gains can be before the system becomes unstable.

One interesting observation was the *dq* and *qd* channels of the stability test were always unstable regardless of SCR values or PLL gains. The opposite was true for the *qq* channel whereas it was always stable across all tested values of SCR and PLL gain values. While further investigation is necessary to pinpoint why and for what values this occurs, one hypothesis is that the *dq* and *qd* channels are always unstable because the V_q and D_q values were both set to 0 for the simulations. The rationale for doing this is that the simulations were performed at steady-state and ideally there would be no reactive power at the PCC of the VSC. If it is assumed that there is no voltage or current in the *q* channel, then the transfer functions associated with the output impedance of *dq* and *qd* would be zero in the steady-state. However, under this logic the *qq* channel should

be unstable for all cases as well, but it is the complete opposite. Again, more research is required to provide a definitive answer as to why these stability results are occurring.

As for the *dd* channel of the stability tests, a thorough spectrum of values was tested and the results documented. It is most interesting to note the relatively small range between where the system is stable, regardless of PLL gains and where it becomes unstable. This region is possibly the most significant takeaway from this research. The pitfall of this calculated region however is the values and range are very parameter specific. That is to say, if the inductor or capacitor of the VSC output filter were altered, the stability region would be completely different. The stability region of SCR and K_p values would need to be recalculated. On a similar note, with the scripts and code already created to evaluate and create the stability region for the different SCR and PLL gain values, all that would be needed to find this new operating range is to change the necessary parameters and run the script. The result would be a plot showing the region of SCRs that will be stable and at what PLL gain is the threshold for that stability to hold true.

6.0 FUTURE WORK

A natural progression of this work is to apply it or integrate it to a larger, more complex system. A good example would be a DG branch with multiple sources of generation each with their own inverter connected to the main electric grid. In this research, the electric grid was modeled as Thévenin equivalent with an ideal source and impedance. The weak nature of the system is brought about by the large impedance connecting the electric grid to the DG branch. This could be modeled as a long distance transmission line or equivalent component. Further tests for instability could then be carried out with this new, more detailed system. The technique of analyzing the impedances of different inverters is applicable to more than one connected at the same point. The calculation does not require detailed knowledge of the converter other than the output filter parameters. This is assuming that the inverter being used fits the small-signal model well. If this is not the case, a different small-signal model can be substituted in its place. The new transfer functions will then need to be derived. The stability criterion however remains the same.

Applying faults further away from the DG branch would allow one to investigate whether particular faults would propagate into the system, most notably into the DG branch. The DG branch, specifically the inverter control and PLLs, should theoretically be able to handle these disturbances and react accordingly to maintain stability within established grid codes. The controls of the inverter will also have the capability to provide support to the system so it is also possible that the fault is alleviated before affecting more of the system. One form of support would be in the form of reactive power compensation for voltage issues. The power flow, be it real or reactive, will be limited however by the output of the DG located behind the inverter. If ample power is

available, it is plausible that the inverter control would be able to provide support to the fault rather than being influenced by it from a stability standpoint.

As with any theoretical and mathematical derivations, the best way to confirm their accuracy is to create the system using hardware. In a lab environment the voltage and power ratings would be much lower but the method and technique could still be validated. This is especially true since the simulation parameters are easily changed since the script has already been created. The PSCAD model is easily changed to suit a different voltage and power level as well.

APPENDIX A

NYQUIST STABILITY PLOTS OF RESULTS

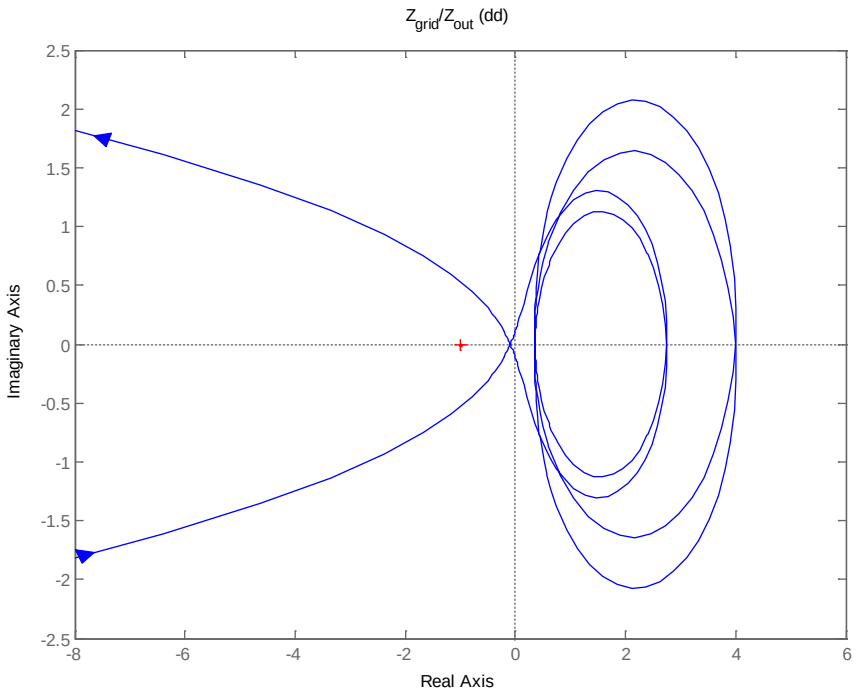

Figure 6-1. Nyquist plot for SCR = 10 (*dd* channel from Figure 4-11).

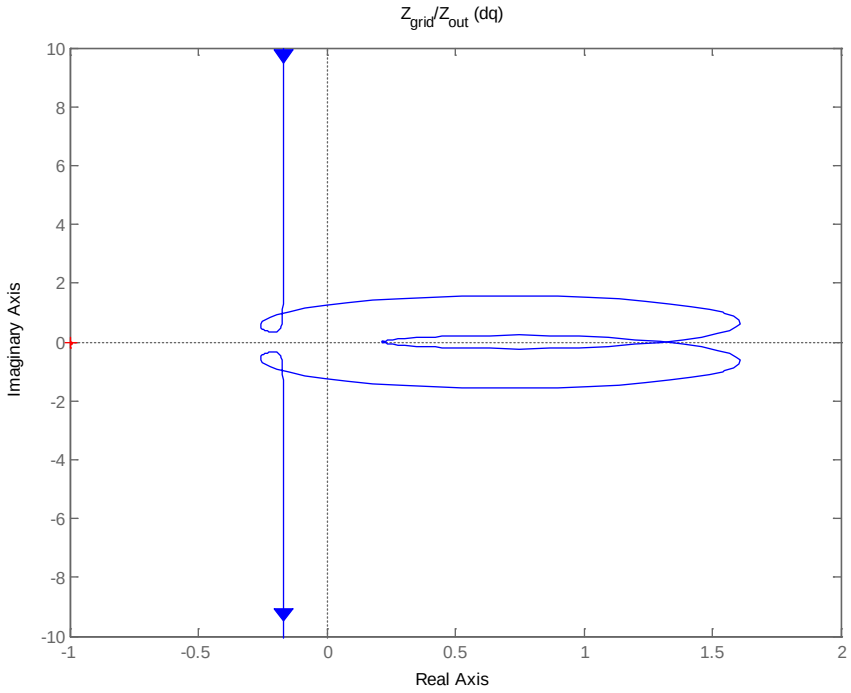

Figure 6-2. Nyquist plot for SCR = 10 (*dq* channel from Figure 4-11).

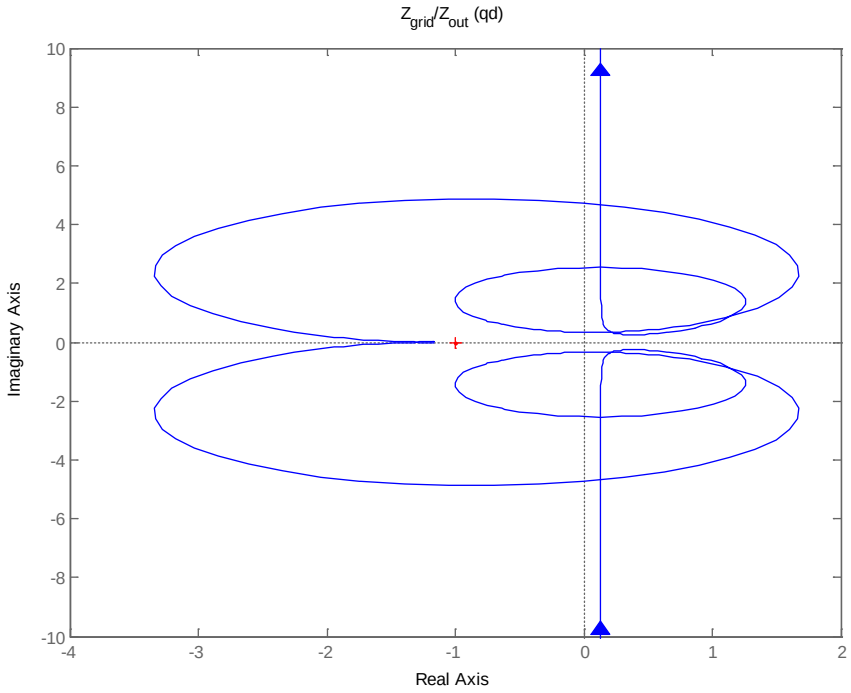

Figure 6-3. Nyquist plot for SCR = 10 (*qd* channel from Figure 4-11).

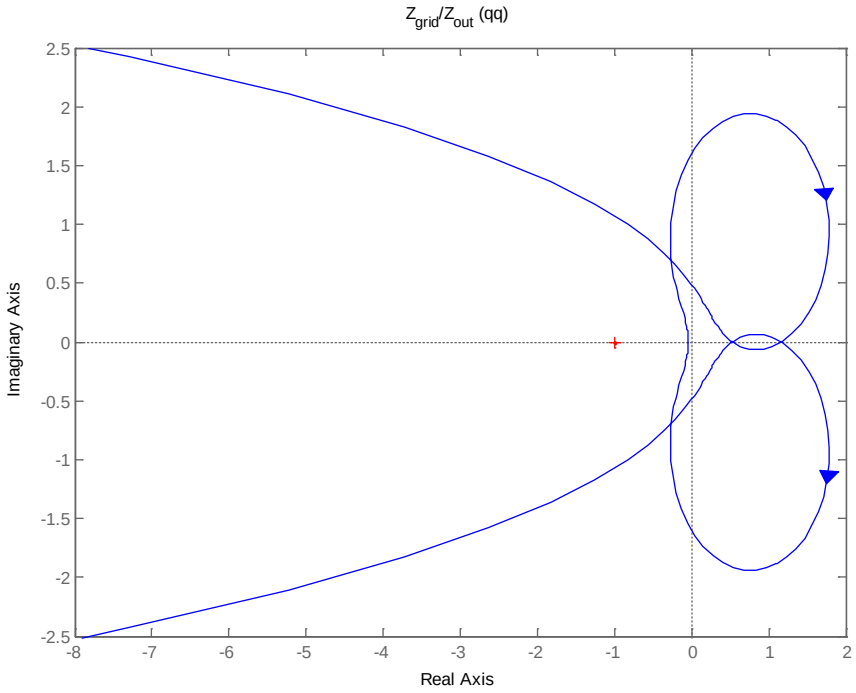

Figure 6-4. Nyquist plot for SCR = 10 (*qq* channel from Figure 4-11).

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