COMPACT MODELING OF INTRINSIC CAPACITANCES IN DOUBLE-GATE TUNNEL-FETS

Atieh Farokhnejad

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Compact Modeling of Intrinsic Capacitances in Double-Gate Tunnel-FETs

Atieh Farokhnejad

DOCTORAL THESIS
2020

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COMPACT MODELING OF INTRINSIC CAPACITANCES IN DOUBLE-GATE TUNNEL-FETS
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DOCTORAL THESIS

Supervised by Prof. Dr. Benjamín Iñíguez
Associate Prof. Dr. François Lime
and Prof. Dr.-Ing. Alexander Kloes

Department of Electronic,
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Tarragona (Spain), June 4, 2020
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to you my beautiful Mama,
to you my lovely Dad,
no matter how hard or easy, how far or close, you never gave up on me...

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List of Symbols

Symbol	Description	Unit
A	Complex constant of the 1D wavefunction	$[1/\sqrt{\mathrm{cm}}]$
B	Complex constant of the 1D wavefunction	$[1/\sqrt{\mathrm{cm}}]$
C	Complex constant of the 1D wavefunction	$[1/\sqrt{\mathrm{cm}}]$
C_{gd}	Gate–drain capacitance	[F]
C_{gg}	Gate–gate capacitance	[F]
C_{gs}	Gate–source capacitance	[F]
C_{dg}	Drain–gate capacitance	[F]
C_{dd}	Drain self capacitance	[F]
C_{sg}	Source–gate capacitance	[F]
C_{ss}	Source self capacitance	[F]
C_{BS}	Bulk source capacitance	[F]
C_{BD}	Bulk drain capacitance	[F]
C_{BG}	Bulk gate capacitance	[F]
C'_{dep}	Depletion capacitance per unit area	$[\mathrm{F/cm^2}]$
C'_{eff}	Effective gate capacitance per unit area	$[\mathrm{F/cm^2}]$
C'_{ox}	Oxide capacitance per unit area	$[\mathrm{F/cm^2}]$
D	Complex constant of the 1D wavefunction	$[1/\sqrt{\mathrm{cm}}]$
D	Diameter of the NW TFET	[nm]
E	Energy level	[eV]
$\vec{E}$	Electric field vector	[V/cm]
E_{c}	Conduction band energy	[eV]
E_{f}	Fermi energy level	[eV]
$E_{\mathrm{f\text{-}init}}$	Initial Fermi energy level	[eV]
E_{g}	Band gap energy	[eV]
E_{v}	Valance band energy	[eV]
F	Complex constant of the 1D wavefunction	$[1/\sqrt{\mathrm{cm}}]$
f	Fermi-Dirac distribution	[−]
g_{d}	Schottky barrier small signal conductance at the drain side	[S]

g_s	Schottky barrier small signal conductance at the source side	[S]
g_ds	Output conductance	[S]
g_m	Transconductance	[S]
$\hbar$	Reduced Planck's constant	[Js]
I_avg	Average current	[A]
I_ds	Drain current	[A]
I_on	On current	[A]
I_out	Output current	[A]
i_d	Drain current	[A]
i_g	Gate current	[A]
i_s	Source current	[A]
k	Wave vector	[cm^{-1}]
$k_{1,\,2,\,3}$	Wave vector in associated region	[cm^{-1}]
k_B	Boltzmann constant	[J/K]
l_ch	Channel length of TFET	[nm]
l_sd	Length of source/drain region	[nm]
L_b	Potential barrier thickness	[nm]
L_G	Gate length of NW device	[nm]
L_GD	Gate–drain underlap in NW device	[nm]
L_GS	Gate–source overlap in NW device	[nm]
L_ch	Channel length of NW device	[nm]
$\vec{n}$	Normal vector	[−]
n_i	Intrinsic carrier concentration	[cm^{-3}]
N_c	Effective density of states in conduction band	[cm^{-3}]
N_ch	Channel doping concentration	[cm^{-3}]
N_d	Drain doping concentration	[cm^{-3}]
N_s	Source doping concentration	[cm^{-3}]
N_t	Interface trap density	[cm^{-2}]
N_inv	Inversion charge density	[$\mathrm{C/cm}^{-3}$]
m^*	Effective charge carrier mass	[kg]
m_0	Free electron mass	[kg]
m_n	Effective electron mass	[kg]
m_p	Effective hole mass	[kg]
P_avg	Average power consumption	[W]
q	Electron charge	[As]
Q_ambi	Total mobile charge in the ambipolar–state	[C]
Q_on	Total mobile charge in the on–state	[C]
Q'_ch	Channel charge per unit area	[$\mathrm{C/cm}^2$]
Q'_i	Mobile charge per unit area	[$\mathrm{C/cm}^2$]

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$Q'_{i,0}$	Minimum value of the channel charge per unit area	[C/cm^2]
$Q'_{b,d}$	Charge at the tunneling barrier on the drain side	[C/cm^2]
$Q'_{b,s}$	Charge at the tunneling barrier on the source side	[C/cm^2]
$Q'_{j,d}$	Charge at the drain junction	[C/cm^2]
$Q'_{j,s}$	Charge at the source junction	[C/cm^2]
Q'_m	1D mobile charge per unit area	[C/cm^2]
R_{ch}	Channel resistance	[Ω]
R_d	Parasitic drain resistance	[Ω]
R_s	Parasitic source resistance	[Ω]
S	Subthreshold swing	[mV/dec]
S_{ideal}	Ideal subthreshold swing	[mV/dec]
T	Temperature	[K]
T_{HP}	Oscillation period of the ring–oscillator in HP mode	[s]
T_{LP}	Oscillation period of the ring–oscillator in LP mode	[s]
T_{lt}	Oscillation period of the ring–oscillator for lt TFET	[s]
T_{pt}	Oscillation period of the ring–oscillator for pt TFET	[s]
T_{tun}	Tunneling probability	[–]
T_{OX}	Oxide thickness in NW TFET	[nm]
t_{ch}	Channel thickness	[nm]
t_{hk}	Thickness of the high–κ oxide	[nm]
$U(x)$	Energy barrier shape as a function of x	[J]
U_0	Height of the constant barrier	[J]
V_d	Drain voltage	[V]
V_g	Gate voltage	[V]
V_s	Source voltage	[V]
V_{ds}	Drain–to–source voltage	[V]
V_{gs}	Gate–to–source voltage	[V]
V_{DD}	Supply voltage of the inverter	[V]
V_{th}	Thermal voltage	[V]
V_{TH}	Subthreshold voltage	[V]
V_{out}	Output voltage	[V]
V_{in}	Input voltage	[V]
V_{fb}	Flat–band voltage	[V]
V_0	Gate bias in the subthreshold regime	[V]
W	Lambert's W function	[–]
w_{ch}	Channel width of TFET	[nm]
x	Cartesian coordinate	[cm]
$X_{b,d}$	Position of the tunneling barrier on the drain side	[nm]
$X_{b,s}$	Position of the tunneling barrier on the source side	[nm]

y	Cartesian coordinate	[cm]
z	Cartesian coordinate	[cm]
α	Slope degradation factor	[−]
Δ	Laplace operator	[−]
ΔV	Channel voltage drop	[V]
ε	Permittivity	[As/Vcm]
$\varepsilon_{1,\ 2,\ 3}$	Energy bands of an atom	[eV]
$\Theta(x)$	Amplitude of the wavefunction	$[1/\sqrt{\text{cm}}]$
κ	Dielectric constant	[−]
κ_{hk}	Dielectric constant of high–κ material	[−]
λ	Wavelength	[cm]
μ_{n}	Electron mobility	[cm^2/Vs]
μ_{p}	Hole mobility	[cm^2/Vs]
$\mu_{\text{tun,n}}$	Tunneling mobility for electrons	[cm^2/Vs]
$\mu_{\text{tun,p}}$	Tunneling mobility for holes	[cm^2/Vs]
ρ	Charge density	[C/cm^3]
τ	Intrinsic inverter delay	[s]
Φ	Electrostatic potential	[V]
Φ_{1D}	Average value of the potential profile from gate to gate	[V]
Φ_{s}	Surface potential	[V]
Φ_{g}	Gate potential	[V]
ϕ	Phase function of the wavefunction	[−]
Ψ	Wavefunction	$[1/\sqrt{\text{cm}}]$
$\Psi_{\text{I, II, III}}$	Wavefunction in associated region	$[1/\sqrt{\text{cm}}]$
Ψ_{in}	Incoming wavefunction	$[1/\sqrt{\text{cm}}]$
Ψ_{r}	Reflected wavefunction	$[1/\sqrt{\text{cm}}]$
Ψ_{t}	Transmitted wavefunction	$[1/\sqrt{\text{cm}}]$
∇	Nabla operator	[−]
∂	Partial differential operator	[−]

List of Acronyms

Symbol	Description
1D	One–dimensional
2D	Two–dimensional
3D	Three–dimensional
ABC	Atanasoff–Berry computer
AC	Alternating current
$Al_xGa_{1-x}As$	Aluminum gallium arsenide
As	Arsenic
B	Boron
BNG	Band gap narrowing
B2B	Band–to–band
CMOS	Complementary metal–oxide–semiconductor
Ch	Channel
D	Drain
DC	Direct current
DG	Double-gate
DIBL	Drain–induced barrier–height lowering
EDVAC	Electronic discrete variable automatic computer
ENIAC	Electronic numerical integrator and computer
EOT	Equivalent oxide thickness
F–N	Fowler–Nordheim
G	Gate
Ge	Germanium
GaAs	Gallium arsenide
HfO_2	Hafnium oxide
HP	High performance
IC	Integrated circuit
ITRS	International technology roadmap for semiconductors
LP	Low power

lt	Line tunneling
MOSFET	Metal–oxide–semiconductor field–effect transistor
NW	Nanowire
P	Phosphorus
pt	Point tunneling
S	Source
SB	Single–band
SCE	Short channel effect
SG	Single gate
Si	Silicon
SiO_2	Silicon dioxide
SOI	Silicon–on–insulator
TAT	Trap–assisted–tunneling
TCAD	Technology computer-aided design
TFET	Tunnel–field–effect transistor
WKB	Wentzel–Kramers–Brillouin

CHAPTER 1

Introduction

1.1 Why TFET?

Our insatiable desire for advancement and heightening is indubitably the mover and shaker of science and is perfectly mirrored in the industry. The gigantic computers have been shrunk a thousandfold and turned to be appreciably more efficient. The fulfillment of this ever–increasing wish for better, thinner, faster and cheaper technology has only become possible because of the miniaturization of *metal–oxide–semiconductor field–effect transistors* (MOSFETs). This astonishing trend has brought the gadgets to a level of complexity and capability that probably few could merely imagine, a century ago. Miniaturization not only yields a reduction in device dimensions, but also improves power efficiency.

At the beginning, according to the scaling rules, the aim was to shrink the vertical and horizontal dimensions of the MOSFET by a specific scaling factor and increasing the doping concentration by the similar factor in a manner such that the electric field inside the device remains unchanged in relation to the original structure [1–3]. In this way the down scaling of MOSFETs has endured for over 30 years, from the micrometer to the nanometer regime [4]. However, this trend began to reach its physical limits when the 65 nm node was reached in 2000 [4]. The electrostatic control of the gate over the channel was negatively impacted by down scaling due to the high electric field. Hence, from this point on, shrinking the structure of the MOSFET was not any further possible just by scaling its dimensions [4]. The leakage current, the subthreshold swing degradation and other short–channel effects (SCEs) are the important challenges for the further down scaling of the MOSFETs.

In the subthreshold or weak inversion region of the MOSFET, where the gate voltage (V_{gs}) is lower than the subthreshold voltage (V_{TH}) and the inversion channel is not fully formed, the charge carriers may anyway flow from the source to the drain. Considering the band diagram of a MOSFET illustrated in Fig. 1.1, the higher the gate voltage, the lower the potential barrier would be. As a result, more electrons can move from source to the drain. This current flow is known as the subthreshold leakage current in MOSFET [5]. By reducing the size of the

MOSFET, the gate oxide which is made of Silicon dioxide (SiO_2) in addition, gets thinner and leads to higher leakage current through the gate terminal [6].

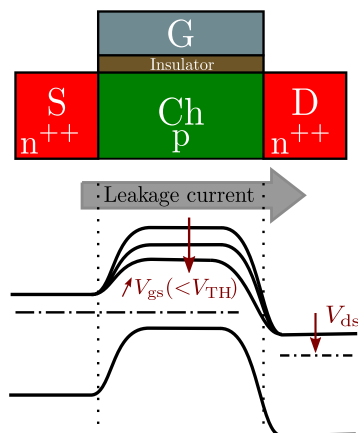

Figure 1.1: Schematic of an n–channel MOSFET and its band diagram. Increasing the gate voltage in subthreshold regime ($V_{gs} < V_{TH}$) results in the potential barrier lowering and consequently increasing the leakage current from source to the drain [5].

The subthreshold slope of a MOSFET refers to the required change in the gate–source voltage in order to increase the drain current (I_{ds}) by a factor of 10. The reciprocal value of this ratio is called subthreshold swing (S) and is given as:

$$S = \frac{dV_{gs}}{d\log_{10} I_{ds}}. \tag{1.1}$$

Although according to this definition the subthreshold slope is the inverse of S, in the literature this value is often quoted as subthreshold slope [7, 8].

Due to the thermionic–emission based current transport mechanism of MOSFETs, their minimum subthreshold swing at the room temperature is theoretically limited to 60 mV/dec [5, 9]. At a constant S the reduction of the supply voltage leads to a higher leakage current and a worse ratio of I_{on}/I_{off}.

By reducing the dimensions of the MOSFET, the widths of the depletion layers on the source and drain side become comparable to the channel length of the device. In this case, the potential of the channel is influenced by a strong lateral and also transverse electric field [1]. The effects resulting from this two–dimensional distribution of the channel potential and the strong electric field are described as short–channel effects. The drain–induced barrier–height lowering (DIBL), threshold voltage roll–off, off–state leakage and subthreshold swing degradation are some examples among these SCEs [10].

The innovative methods and technologies have made it possible to tackle these challenges and go even further with scaling. For instance, by using high–κ insulators instead of SiO_2 and taking advantage of strained silicon technology the leakage current has been reduced [6].

These alternative materials allow the same dielectric capacitance to be achieved with a higher dielectric thickness compared to SiO_2. So, the tunneling barrier would be thicker and can block the gate leakage [11]. Furthermore, multiple–gate structures by increasing the electrostatic control of the gate over the channel make it possible to a better grip on SCEs [12, 13].

Considering the fact that further scaling of the MOSFET leads to other undesirable problems such as quantum mechanical effects, together with the 60 mV/dec limit of the MOSFET and furthermore the strong interest to reduce the subthreshold swing and suppress the power consumption of the circuits, the option to investigate new structures remains. Hence, alternative devices with abrupt switching behavior, which is also not affected by supply voltage, need to be sought [7, 9, 14].

Among these devices *Tunnel field–effect transistors* (TFETs) have been studied as viable successor of conventional MOSFETs. They can overcome the 60 mV/dec S which is due to their alternative current transport mechanism, the so called *band–to–band* (B2B) tunneling. It helps TFETs to operate at a low supply voltage and therefore have a lower power consumption. TFETs show a lower leakage current and in comparison to MOSFETs they have a greater level of stability against short–channel effects [7, 14, 15]. Moreover, they are compatible with the *complementary metal–oxide–semiconductor* (CMOS) fabrication process.

In 2004 for the first time Wang has presented TFETs as the potential successor of MOSFET for low power circuits [16]. In the same year Appenzeller presented a three–terminal tunneling device using a carbon nanotube as the channel with a subthreshold swing of 40 mV/dec [17]. This has led to more attention being paid to TFETs, and then several research groups began to investigate these transistors.

The drawback of TFETs is their low on–current. It is challenging to reach a high on–current without also increasing the off–current and yet keeping the subthreshold swing smaller than 60 mV/dec [18]. Above all, the compatibility to the CMOS technology should also be considered. A combination of different technologies is therefore required to meet this challenge.

Some possibilities to tackle this challenge and enhance the current are using III-V semiconductors, implementing straining techniques, switching to 2D materials and taking advantage of line tunneling [18–20]. As an example, in 2011 Dewey presented a III-V TFET that by taking advantage of hetero–junction achieved a steep subthreshold swing ($S < 60$ mV/dec) and high on–current [21]. In 2013 Knoll reported that the strained Si nanowire (NW) complementary TFET, at room temperature and drain voltage of 0.5 V, shows a minimum subthreshold swing of 30 mV/dec and an on–current >10 μA/μm [22]. In 2017 Memisevic demonstrated an InAs/InGaAsSb/GaSb vertical TFET NW which at the drain voltage of 0.3 V exhibits a minimum subthreshold swing of 43 mV/dec and on–current of 10 μA/μm [23].

1.2 Necessity of Device Simulation and Compact Model

Considering the complexity and high fabrication expenses of new structures such as TFETs, the first step for its design and production is the process and device simulation. It helps

to improve the processing technologies, describe the behavior of the device and reduce the time and resources on test wafers. For this purpose there are powerful tools existing such as Technology Computer–Aided Design (TCAD) softwares provided by companies such as Synopsys [24], Silvaco [25], Global TCAD solutions [26], Crosslight [27] and Cogenda Software [28].

Such a program provides finite–element simulation. Once all the physical parameters of the structure such as dimensions, materials and doping profile are defined, the structure is meshed. That is to say, the structure is divided into many small geometric elements and represented in form of a finite–element structure. Afterwards, depending on the activated models, TCAD solves the physical partial differential equations for every single grid point in the structure. The TCAD simulations usually require a great deal of time and are very computationally demanding. Therefore, in order to enable the circuit simulation including millions of TFETs, compact models of circuit elements are required. Compact models have to be simple and fast, but also accurate in order to provide circuit designers with suitable results. In fact, this is essentially the point that makes the compact modeling field particularly challenging [29].

Principally for circuit analyses three types of models including DC, AC and transient are needed. A DC model predicts the device current in the case that the voltages are fixed and do not vary with time and ignores the energy-storing behavior of the semiconductor device. In an AC model, it is considered that the input voltage changes very slowly with time. It is a small–signal model which calculates the current variations by means of linear relations and includes the effect of energy–storage elements in the structure of the device [1]. A transient model is a large–signal dynamic model which calculates the current for the case that the input voltage varies with time [1]. In order to provide the mean to do the transient analysis, compact models for the capacitances and their charging behavior in TFETs are required. In fact the switching speed of an *integrated circuit* (IC) is depending on the capacitances. Hence, the focus of this thesis lays on compact modeling of intrinsic capacitances in this type of transistors.

Considering the importance of TFETs as a potential successor of MOSFETs technology, a lot of investigations have been carried out on the physics–based compact modeling of TFETs. Mostly these works are focused on the potential characteristic and current in TFETs [30–35]. Nevertheless, also some models to estimate the terminal capacitances are represented. For instance, Yang et al. in [36] have presented a compact model for TFET capacitances using BSIM3 equations [37]. Lu et al. in [38] and Zhang et al. in [39, 40] have developed an analytical charge model for Si double-gate (DG) TFETs based on a surface potential model. Lu et al. in [41] have calculated the terminal charges in TFET using a parameterized empirical expression. Based on this, the capacities are derived by numerical differentiation. The fact that some of these models use numerical iterative methods and that they are very complicated makes them somewhat inadequate and less effective for the use in SPICE and circuit simulations. The charge–based model introduced in this work is very simple and flexible and contains no iterative process, which makes it SPICE friendly and suitable for circuit simulations. In addition, unlike most of the reported models, this compact model is validated not only by TCAD simulations

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of a single device, but also by measurement data of fabricated TFETs with various structures.

1.3 Outline of the Thesis

Chapter 2 is a brief history of transistors and highlights some of the important inventions that have brought technology way beyond expectations and fantasies. This chapter shows how the need for better and faster computers in combination a perfectionist competitive spirit leads to such a great progress and achievements.

Chapter 3 is about the theoretical physics and mathematics backgrounds which are essential to understand this work. The characteristics of semiconductor materials in terms of atomic construction and band structure, doping, quantum mechanical effect of tunneling and the methods to calculate the tunneling probability are introduced in this chapter.

Based on the theories, in chapter 4 the working principle of TFETs is explained. By giving consideration to the device geometry and band diagram, different states and operation regions of transistors are described. Then the current–voltage and the capacitance–voltage relations of TFETs are introduced and explained. This part also shows the capacitances in the TFET, on which the compact model focuses. Furthermore, the capacitances of TFET and MOSFET are briefly compared in the end of the section.

Chapter 5 starts with the existing charge model which is used to develop the intrinsic capacitance model. The steps which are taken to adjust the charge equation to the TFET structure are explained. Afterwards, it is shown how the capacitances in the TFET are calculated by the model. Moreover, it is presented how the effect of parasitic elements as well as the Schottky barrier effect at the terminals are mathematically implemented in the model.

The validity of the capacitance model is investigated in chapter 6. The capacitance model is firstly compared to the results of the TCAD simulations. In the next step it is verified using the measurement data of a fabricated p–type planar TFET. The deviation from measurements have shed light on the importance and effect of parasitic elements on the capacitances in TFET. Hence, in this part a theory about the impact of the Schottky barrier contacts of capacitances is introduced. This theory is then examined on TCAD simulation results of an n–type TFET to see if they produce the same pattern as in the measurements. Further verification of the model is carried out by means of measurement data of a fabricated n–type NW.

After model verification, the intrinsic capacitance model is combined with an existing compact DC model [35] and implemented in Verilog–A language. In order to examine the robustness of the compact model, TFET–based inverters and ring–oscillators are simulated in in chapter 7. These simulations are executed for different device parameters and also for the case that the on–current of the TFET by taking advantage of line–tunneling is improved.

Chapter 8 presents a summary of the entire thesis, highlights the results which are obtained in the course of this dissertation and the points which are still not implemented in the model and need to be in future studies.

CHAPTER 2

History of Microelectronics

To know where we are standing in microelectronics technology and also where the need for such an advanced improvement in this area comes from, it is helpful to glance over the path it has taken so far. All the way from giant mechanical computers to invention of tiny bipolar transistors to nanoscale devices. Hence, in this section some of the most important achievements which have changed the direction of industry and technology are briefly addressed.

2.1 Mechanical Computers

The concept of automatic computing machine was firstly introduced in 1822 by Charles Babbage, a mathematics Professor in Cambridge University. As Babbage and his astronomer friend, John Herschel, were reviewing various publications of mathematical tables like natural logarithm, integrals and astronomical tables, they have actually found many errors and variations. Hence, he came about the idea to make a machine which is capable of automatic production of mathematical tables infallibly. Babbage's first proposed mechanical computer, which today is called *Difference Engine No. 1*, was designed using finite differences methods to solve up to seventh order polynomial equations. As it can be seen in Fig. 2.1, the Difference Engine was built entirely from mechanical components such as gears, ratchets and rods instead of electronic components. To avoid possible human errors, it was planed to be connected to a printer to make hard copies of equations results [42].

The mechanical computer was massive and its reliability depended drastically on the accuracy of the fragments used in it, which in reality meant that its use was very expensive. Anyhow, Babbage always kept going ambitiously and came about so many other ideas for instance reducing the size of mechanical computer, making them programmable and using them for beyond mathematics purposes. Despite investing lots of money and work, unfortunately these notions never got completed and did not come to fruition in Babbage's lifetime. All in all it can be said that the attempts to automatic computation in 19th century did not have much success and this procedure came closer to the goal in 20th century [43].

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Figure 2.1: Small part of Difference Engine No.1 [44].

2.2 Electronic Computers

The invention of the vacuum triode ushered the way to employ binary logic functions and the possibility to replace mechanical computers with electronic computers [45].

In 1937 Professor John Vincent Atanasoff and his graduate student Clifford Berry, by using vacuum tubes built the first automatic electronic digital computer. Anyhow, neither of them had ever applied for a patent. The *Atanasoff–Berry computer* (ABC) could not be reprogrammed and was designed just to solve linear equations. But in any case, it was pioneer in using binary system to represent digits or data and electronic switches, instead of mechanical elements, to do the calculations. In the same era there were some other experiments with computers using vacuum tube circuits existing such as Konrad Zuse's Z3, Manchester machine, Colossus and ENIAC. Colossus was developed in 1941 for military purposes by British engineer Tommy Flowers and it was a fully functional electronic computing machine. Nevertheless, because of the secrecy nature of Colossus and to avoid exposing the secrets of its technology, it was destroyed after the war and left ENIAC to be the pioneer to step from mechanical to

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fully electronic computers [42, 45]. In 1943 J. Presper Eckert and John Mauchly began the construction of ENIAC at the University of Pennsylvania for the United State Army's research, and by 1946 it was completed.

Years later, there were discussions about that who was really the inventor of digital computers and whether ABC was really the first electronic computer. Finally, in 1973 the US federal court declared John Atanasoff as the inventor of first electronic computer and for the ease of developers the patent rights of it were dedicated to public domain [45].

Despite the vote of district court, ENIAC is still widely known as the first electronic digital computer. Similar to the mechanical computers, ENIAC was giant (see Fig. 2.2) and contained almost 18,000 vacuum tubes, occupied over 150 m^2 of space and it weighed about 30 t. It was programmable, but since programes were hard coded into the machine, an implementation of them was only possible by manipulating the switches, function tables and wiring of the machine. Afterwards, the program could be executed step by step for debugging. Nevertheless, it was complicated and very time consuming to perform a complex program on the ENIAC. Besides all difficulties in programming, maintenance of those giant computers was another big problem. Vacuum tubes consume great deal of power and could get very warm. Consequently, they required a lot of space and the rooms that were occupied with vacuum tubes needed to be cooled down continuously, which meant even more energy consumption. Furthermore, considering the short lifetime of vacuum tubes, they had to be replaced quite often. Overcoming these problems has been made possible only by the invention of transistors [42, 45].

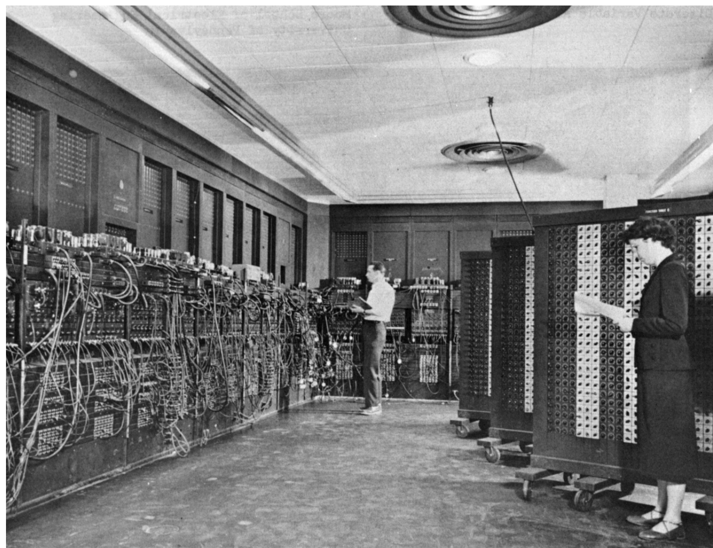

Figure 2.2: ENIAC was massive and its maintenance was complicated, time consuming and energy demanding [46].

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2.3 Invention of Transistors

The biggest challenge in twenties was to find a replacement for vacuum triode and the question was how to go further with electronic industry. Mervin Kelly, the Bell Labs' Director of Research, could see from very beginning of his career the importance and potential of a triode based on semiconductor material to make a big change. To start, he chose the young talented physicist William Shockley from MIT as the leader of this project. Additionally, Kelly gave him the freedom to work with any group working on different projects in Bell Labs to widen his horizon and overcome the obstacles. There he began his work by participating in ongoing projects and studying all work on semiconductors [45].

Soon after, in 1939 Shockley came about the idea to combine Schottky's Metal–Semiconductor Junction rectifier with Brattain's cuprous oxide semiconductor which has led to Shockley's *field–effect* theory. According to his theory, the electrical field close to a semiconductor sample affects the resistance of it and hence, cause the current flows through the semiconductor. Based on field–effect theory and by the help of Brattain, Shockley started some experiments to build a solid–state triode. However, Shockley and Brattain's first attempts did not succeed [45].

Over the course of time, Bell Labs team gained deeper knowledge on semiconductor materials. Also new concepts such as dopant, n–type and p–type semiconductors were addressed by researchers. Thereafter, Walter Brattain and John Bardeen, the solid–state physicists, started to work together on Shockley's field–effect triode. Although Shockley was the leader of this project, he was not much involved with experiments they where dealing with. Finally in 1948 the first functional point contact transistor was represented (see Fig. 2.3) [45].

Shortly after that, Brattain and Bardeen were listed as transistor inventors. Shockley, who was not really happy about this news, has pulled himself together and created his *junction transistor* or *bipolar transistor*. Bipolar transistors were manufactured for several years but it was not the end of the transistor story, rather just the beginning of breathtaking changes and progresses to a new era. In 1958 as Atalla's team were studying the features of a silicon–silicon dioxide interface in Bell Labs, they observed something very similar to the field–effect theory of Shockley. They realized if a metal electrode is deposited on top the oxide, by applying voltage to this electrode, at the silicon–oxide interface a conductive channel is build. Based on this observation, in 1960 Atalla developed the MOSFET [45].

In comparison to bipolar transistors, MOSFETs were easier to be reduced in size and voltage. Furthermore, the power consumption of MOSFETs was lower. Probably at that time the significance of the miniaturization of the transistor and its affects on chip industry was still not fully clear. However, shortly after it turned to be a crucial factor in semiconductor technology. Considering all advantages of MOSFET, they easily and rapidly found their place on large-scale chips and replaced those produced using bipolar transistors [45].

Figure 2.3: First point contact transistor represented by Brattain and Bardeen [44].

2.4 Moore's Law

In 1958 Jack Kilby as well as Robert Noyce came up with the idea to fabricate all required components for a circuit on one single piece of semiconductor material. Combining this idea with the use of metalized connection patterns printed on a board, known as *printed circuit board technology*, led to the invention of IC [45]. The combination of integrated circuit and MOSFET brought the chip industry into a completely new era. By mid–1960s the biggest challenge was to increase the features and capabilities of chips in an economically reasonable way. That is to say, squeezing more and more transistors on a chip without expanding the size and costs of the chip. Miniaturization is not only about reducing the size of transistors, but also lowering power consumption and increasing switching speed to finally achieve an even faster and more powerful computers.

In 1965 Gordon Moore, the outstanding chemist and Fairchild Semiconductor's director, published an article titled "*Cramming more components onto integrated circuits*" [47]. In this article the progress of microelectronics industry between 1962 to 1965 is reviewed. Moore discovered that the number of transistors on a chip is doubled every twelve months and predicted that this trend would remain constant for at least ten years (see Fig. 2.4). This prediction turned to an autogenous road map for semiconductor industry and made its name as *Moore's Law*. Later on he decided that the complexity is doubling every two years, however, his forecast proved to be surprisingly precise.

A simple comparison between modern computers or smart phones and their predecessors, who are not even a decade older, is enough to see how the semiconductor industry has influenced the entire world. Undoubtedly, this is the most relentless technology of all time. It is over 50

years since the observation of Gordon Moore and Moore's Law is still valid and transistors are now scaled into nanometer regime. This question has always been existing, that how further miniaturization can go. It is obvious that in each step, not only the complexity of chips increases, but also the manufacturing progress becomes more difficult and faces greater challenges. Nonetheless, all obstacles and limitations have never been able to stop the number of transistors growing on a chip. Whenever the progress has closely reached its limit, innovation and creativity of researchers has turned it to an opportunity.

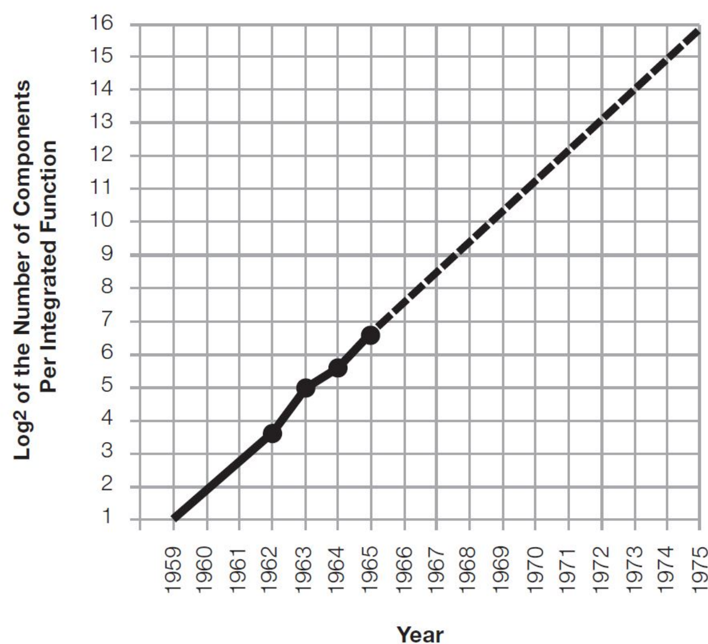

Figure 2.4: Number of transistors on integrated circuit versus year according to Gordon Moore's observation in 1965. He predicted that this number doubles every year [47].

By 2019, the size of transistors has been shrunk to 7 nm and the transistor count has grown to tens of billions on a chip [48]. In such a tiny dimension charge carriers show a special behavior known as quantum tunneling, which is explained in detail in the Sec. 3.2. Since it is impossible to avoid this phenomenon in the nanometer regime, only using new materials, novel device structures and production techniques can actually be of help. TFETs are among recently designed transistors. They work based on quantum tunneling and show the feasibility to overcome challenges on the way of miniaturization. Further details about TFETs are discussed in chapter 4.

CHAPTER 3

Theoretical Backgrounds

The first step to start with modeling the behavior of the TFET is understanding the physical and mathematical principle which a TFET is based on. Sec. 3.1 focuses on the structure of semiconductor materials as single atom and also as a crystalline structure. In Sec. 3.2 the physical basis of tunneling is explained followed by the tunneling probability in Sec. 3.4. In this section, depending on the shape of the barrier, different methods to calculate the tunneling probability are considered.

3.1 Semiconductor Materials

Concerning the conductivity, solid state materials are divided into three categories: insulators, semiconductors and metals. In an insulator all electrons are tightly bound and therefore it can not conduct an electric current. In a metal, the valance electrons of atoms can move freely within the crystalline structure, which means higher concentration of free charge carriers and thus higher conductivity. Semiconductors, as it comes from their name, are between these two groups. Their conductivity in their natural state is poor but it can be varied by many factors such as heat, illumination, electric field and doping. This property makes semiconductors particularly suitable for the usage in the manufacture of electrical appliances. In the following sections the Fermi distribution, band structure of semiconductors and the effect of dopant on their conductance are analyzed.

3.1.1 Fermi Distribution

The probability that an electron occupies an available energy state E is given by the *Fermi–Dirac distribution function* as following:

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_\mathrm{f}}{k_\mathrm{B} T}\right)} \tag{3.1}$$

where k_B is the *Boltzmann constant* and T is the temperature of the material. The E_f presents the *Fermi level*, which refers to the energy level in which the probability to find an electron is exactly 50 % ($f(E_f) = 1/2$).

Considering Fig. 3.1, at T = 0K the Fermi distribution shows an abrupt transition from unity to zero. That means all energy levels above E_f are empty, so $f(E) = 0$ and all energy levels below E_f are full, so $f(E) = 1$.

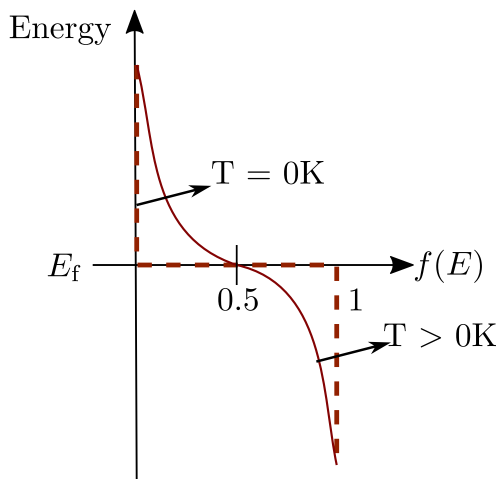

Figure 3.1: Fermi distribution at T = 0 and T > 0K [8].

By increasing the temperature the Fermi distribution changes and becomes smoother. As it is illustrated in Fig. 3.1, in this case it cannot be said that all energy levels above E_f are empty, it is rather likely that an energy state is occupied by an electron. The higher the temperature, the higher the probability to find an electron above the Fermi level.

Fermi level of an intrinsic semiconductor in equilibrium condition lays almost in the middle of its band gap and is referred to as intrinsic Fermi level (E_i) [1, 8, 49].

In the case that the considered E is higher than $3k_BT$, the exponential function in the denominator of the Eq. (3.1) gets much bigger than one. Therefore, the carrier concentration can be approximated by *Maxwell–Boltzmann statistics* [1, 50] as following:

$$f(E) = \exp\left(-\frac{E - E_f}{k_B T}\right). \tag{3.2}$$

3.1.2 Band structure

According to the *Pauli principle*, each energy state with a certain quantum number can only be occupied with two electrons with opposite spins [8, 50]. In other words, an atom orbital has maximum two electrons. When two or more atoms approach to form a bond, the energy levels split as it is shown in Fig. 3.2. Now considering a complex system with a large number of

atoms in its structure, these discrete energy states of the single atoms are widened, superposed and merge into *energy bands*. There are bands in which the charge carriers can move freely and, by contrast, there are bands in which they are involved in covalent bonds, thus charges are immobile. The energies below the highest immobile energy state are called the *valence band*, while the energies above the lowest mobile energy state are called the *conduction band*. Due to quantum physics, there are energy ranges in which no standing waves of electrons fits. These forbidden energy states between conduction band and valence band are called the *band gap* [1].

Generally, the band structure of a material explains how atoms and electrons in that substance interact. Figure 3.3 shows the difference in the band structure of the three aforementioned groups of solids. It can be seen that insulators have a big band gap ($E_g > 5$ eV). Their valence band is completely filled and their conduction band is empty. In contrast to insulators, metals have no band gap and as it is illustrated, the valence band and conduction band overlap which means they have plenty of free electrons in their structures. In semiconductors the energy gap between the valence band and conduction band is adequately small. Therefore, the electrons in the valence band by absorbing enough thermal energy can be excited to the conduction band, leave behind a hole in the valence band and move freely in the lattice.

The materials which are widely used in semiconductor technology are from column III, IV and V of the periodic table. A semiconductor can be composed of only one element, such as Silicon (Si) and Germanium (Ge), which is called *elemental semiconductor* or it can be a combination of two or more elements from group III and V such as Gallium Arsenide (GaAs) or Aluminum Gallium Arsenide ($Al_xGa_{1-x}As$) [8, 51]. Depending on different properties such as the band gap of these materials they can be used for particular purposes.

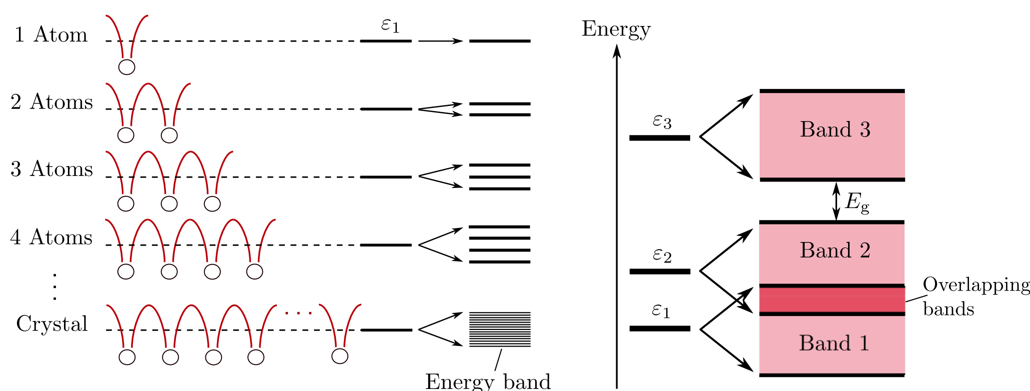

Figure 3.2: Expansion of discrete energy levels of a single atom in the vicinity of other atoms and finally into energy bands in a crystal [8].

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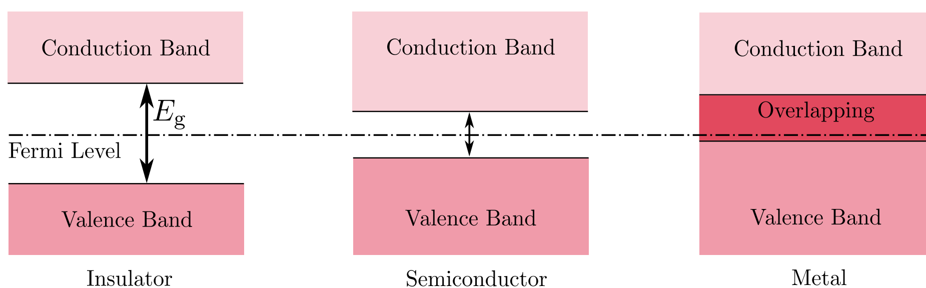

Figure 3.3: Band structure schematic of an insulator, semiconductor and a metal [8].

3.1.3 Doped Semiconductors

To enhance the conductivity of semiconductors, specifically some impurity atoms are added into their crystal lattice. This process is known as *doping* and the material is called *doped* or *extrinsic semiconductor*. By combining doped semiconductors of different types, several electrical components are fabricated such as p–n junction which is the building block of diodes and transistors. The materials that are mostly used in technology as dopants are Boron (B), Phosphorus (P) and Arsenic (As) [1, 52].

Boron is an element in the periodic table group III with three valence electrons and silicon, the most used semiconductor in history of microelectronics, has four valance electrons. Thus, by adding a Boron atom into the silicon crystal it accepts an electron from lattice, makes a negative ion and releases an excess hole in the lattice. Dopants from main group III are called *acceptors* and the semiconductor doped with them is a p–type material. In this case the Fermi level is closer to the valence band of the semiconductor as it is shown in Fig. 3.4(a) [1, 8].

When a semiconductor is doped with impurities from group V, which have five valence electrons, it is called n–type. These dopants add an extra electron to the semiconductor crystal, and therefore they are called *donors*. In an n–type material the Fermi level lays closer to the conduction band (see Fig. 3.4(b)) [1, 8].

If a semiconductor is doped with a concentration higher than 10^{19}cm^{-3}, it is considered as heavily doped and is called *degenerate*. In this case, the carrier concentration is calculated with the Eq. (3.1). If the Fermi level lays within the band gap with a distance of a few $k_\text{B}T$ from either conduction or valence band, it is called *nondegenerated* [1]. In such a semiconductor the carrier concentration is approximated by Eq. (3.2) [1].

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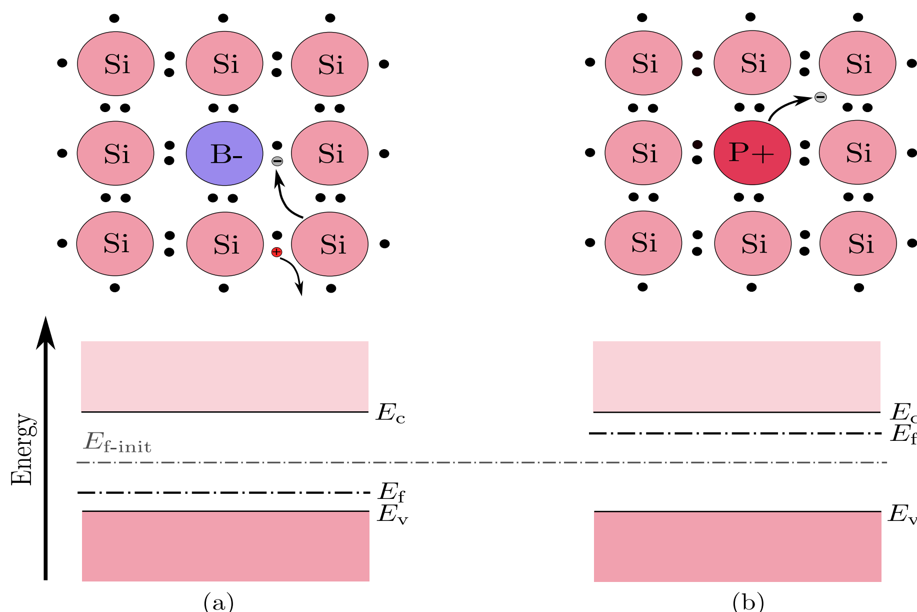

Figure 3.4: Schematic representation of a silicon crystal doped with impurity atoms and the effect of doping on its band structure. (a) By doping silicon with Boron atoms, a free hole is added to the lattice. (b) Doping silicon with Phosphorus releases a free electron to the structure. The $E_{\text{f-init}}$ refers to the initial position of the Fermi level before doping.

3.2 Quantum Tunneling

Quantum mechanics refers to a branch of physics which describes incidences at the microscopic scale. It can explain the nature of the universe, yet it contradicts classic mechanics and the idea of how it all works. Unlike classical physics, where everything follows clear rules and is consequently predictable, quantum physics is based on probabilities. As the Heisenberg's uncertainty principle describes, quantum objects do not have a designated position before they are observed. Rather, the particles are defined with a so called wavefunction Ψ, which indicates the probability where a particle is most likely to be found.

According to the classical mechanics, there are only two possibilities for a charge carrier that encounters an energy barrier; either the energy of the carrier is higher than the barrier and thus it can overcome the barrier or it is not the case and the particle gets reflected. But in quantum physics another scenario is also considered, in which the charge carrier despite its low energy manages to get into and through the barrier. This phenomenon, which is inevitable in atomic and subatomic scale, is known as *tunneling*. Quantum tunneling is the fundament of many physical processes such as radioactivity and also operation of certain semiconductor devices including TFETs.

Figure 3.5 illustrates the incoming wavefunction Ψ_{in} of a free electron. The electron flow

encounters a constant barrier of height U_0 and thickness L_b, part of it is reflected Ψ_r, another part enters the barrier, its amplitude decays and then appears on the other side of the barrier as transmitted wavefunction Ψ_t. The mathematical formulation that can describe the wavefunction behavior, is the *Schrödinger* equation. Solving this equation gives the probability to find the quantum object at a specific position. Depending on the shape of the barrier, different types of tunneling are existing and consequently, particular methods are used to solve the Schrödinger equation. In the following the categories of carrier transport mechanism, Schrödinger equation and different approaches to solve it are explained in detail.

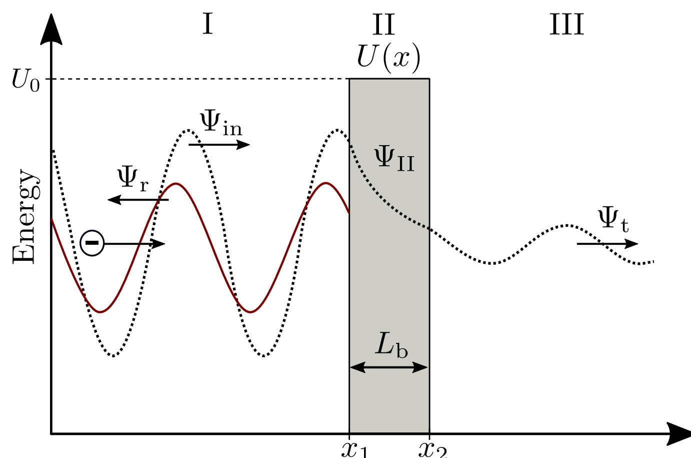

Figure 3.5: Wavefunction describes the behavior of an electron. The incoming wave encounters the rectangular shape barrier. There is the probability that part of it is reflected and part of it can tunnel through the barrier.

3.3 Tunneling Events

Considering the band structure there are two types of tunneling existing: *single–band* (SB) and B2B tunneling. Figure 3.6(a) illustrates the SB tunneling process in a Semiconductor–Insulator–Semiconductor structure. It can be seen that this process is divided to three further sub–categories called: *Fowler–Nordheim tunneling* (F–N), *direct tunneling* and *trap–assisted–tunneling* (TAT). The F–N tunneling refers to the case that the charge carriers tunnel through the triangular barrier which is shaped due to the applied electric field. This mechanism occurs regardless of the thickness of the barrier, as long as the field effect is large enough. In direct tunneling carries penetrate through the whole barrier. Therefore, it is expected just for thinner barriers (< 5 nm) [49].

The TAT takes place due to the existence of *traps* in the band gap of materials. Traps are actually defects in the structure of the material and are caused by the fabrication process. In this case, the charge carriers do not tunnel through the entire thickness of barrier. Rather,

firstly they penetrate from one energy band to a trap inside the barrier and then either hop to the next trap or tunnel to the other side of the barrier.

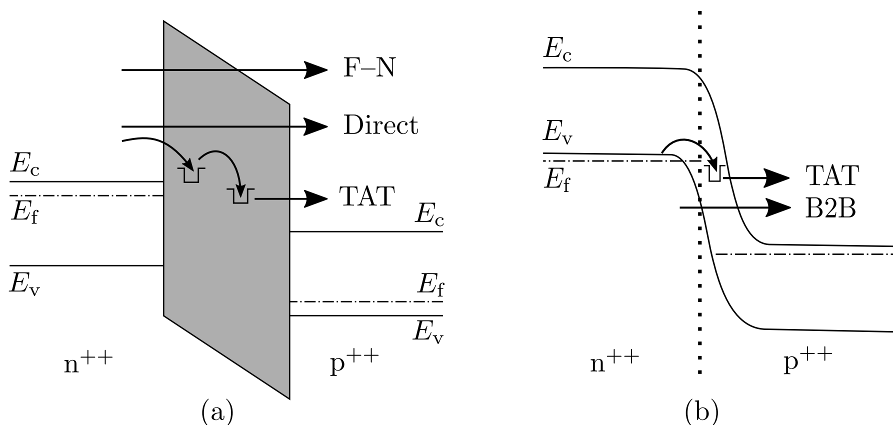

Figure 3.6: (a) Different types of SB tunneling in a semiconductor–insulator–semiconductor structure. (b) The band structure at pn–junction and the band–to–band tunneling processes [35].

The B2B tunneling points out the direct tunneling from valance band to the conduction band or the other way round as it is shown in Fig. 3.6(b) at a pn–junction. This process describes the main current transport mechanism in TFETs. B2B tunneling can be controlled with factors such as bias voltage, doping concentration, device structure and material. Thus, it is responsible for the switching of the device and constitutes the current flow in it. Furthermore, considering that these devices are highly doped and doping semiconductors leads to material defects and thus to a high density of traps, in addition to the direct tunneling also TAT plays an important role. The TAT cannot be controlled and is mostly contributed to the off current of the device. In chapter 4 the working principle of TFETs is explained in detail.

3.4 Tunneling Probability

As it is mentioned above, the tunneling probability can be determined by solving the 1D time–independent Schrödinger equation. This differential equation is defined as [49]:

$$-\frac{\hbar^2}{2m^*} \cdot \frac{\mathrm{d}^2 \Psi(x)}{\mathrm{d}x^2} + U(x) \cdot \Psi(x) = E \cdot \Psi(x), \tag{3.3}$$

where $\hbar$ presents the reduced Planck's constant, m^* is the effective charge carrier mass, $U(x)$ shows the energy barrier, E is the carrier energy and $\Psi(x)$ is the inspected wavefunction of the carrier. Depending on the shape of the barrier, Ψ can be precisely calculated or estimated. Hence, in the following sections the solution of the Schrödinger equation for a rectangular and a triangular energy barrier are considered separately.

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3.4.1 Rectangular Barrier

Considering a constant energy barrier as following:

$$U(x) = \begin{cases} 0, & x < x_1 \\ U_0, & x_1 \leq x \leq x_2 \\ 0, & x > x_2 \end{cases}, \tag{3.4}$$

which characterizes a rectangular barrier similar to Fig. 3.5, it is possible to solve the Schrödinger equation analytically. The wavefunctions in these three regions are investigated independently. That is to say, the Schrödinger equation is solved for each region separately.

As it is shown in Fig. 3.5, the wavefunction in region I (Ψ_I) is actually the superposition of incoming and reflected waves:

$$\Psi_\mathrm{I}(x) = \Psi_\mathrm{in}(x) + \Psi_\mathrm{r}(x) = A \cdot \exp(+\mathrm{j}k_1 \cdot x) + B \cdot \exp(-\mathrm{j}k_1 \cdot x). \tag{3.5}$$

In this equation, which is in fact the solution of the Schrödinger equation for a free particle, A and B are complex constants and k_1 represents the wave vector which is defined as:

$$k_1 = \sqrt{\frac{2m^* \cdot E}{\hbar^2}}. \tag{3.6}$$

Assuming that the energy of the particle in region II is lower than the barrier height ($E < U_0$), the $\Psi_\mathbf{II}$ determines the wavefunction within the energy barrier:

$$\Psi_\mathrm{II}(x) = C \cdot \exp(k_2 \cdot x) + D \cdot \exp(-k_2 \cdot x). \tag{3.7}$$

Here C and D are the complex constants and k_2 is given by:

$$k_2 = \sqrt{\frac{2m^* \cdot (U_0 - E)}{\hbar^2}}. \tag{3.8}$$

On the right side of the barrier similar to region I, the particle can move freely. The only difference to the region I is that here there is no more energy barrier existing and therefore no reflection needs to be considered. Hence, the solution to the Schrödinger equation in region III is determined as:

$$\Psi_\mathrm{III}(x) = \Psi_\mathrm{t}(x) = F \cdot \exp(+\mathrm{j}k_1 \cdot x). \tag{3.9}$$

In this expression F shows the complex constant and k_1, which represents the wave vector outside the barrier, is given by Eq. 3.6.

Having the wavefunction in these three regions and considering the continuity and differentiability of the wavefunction, now the boundary conditions at $x = x_1$ and $x = x_2$ are

implemented to calculate the constants. Regarding the continuity of the wavefunction at $x = x_1$ the following is obtained:

$$\begin{aligned} \Psi_{\mathrm{I}}(x_1) &= \Psi_{\mathrm{II}}(x_1) \\ A \cdot \exp(+\mathrm{j}k_1 \cdot x_1) + B \cdot \exp(-\mathrm{j}k_1 \cdot x_1) &= C \cdot \exp(k_2 \cdot x_1) + D \cdot \exp(-k_2 \cdot x_1) \end{aligned} \tag{3.10}$$

and the differentiability results in:

$$\begin{aligned} \frac{\mathrm{d}\,\Psi_{\mathrm{I}}(x_1)}{\mathrm{d}x} &= \frac{\mathrm{d}\,\Psi_{\mathrm{II}}(x_1)}{\mathrm{d}x} \\ \mathrm{j}k_1 \cdot \big(A \cdot \exp(+\mathrm{j}k_1 \cdot x_1) - B \cdot \exp(-\mathrm{j}k_1 \cdot x_1)\big) &= k_2 \cdot \big(C \cdot \exp(+k_2 \cdot x_1) - D \cdot \exp(-k_2 \cdot x_1)\big). \end{aligned} \tag{3.11}$$

Applying the first boundary condition for $x = x_2$ leads to:

$$\begin{aligned} \Psi_{\mathrm{II}}(x_2) &= \Psi_{\mathrm{III}}(x_2) \\ C \cdot \exp(k_2 \cdot x_2) + D \cdot \exp(-k_2 \cdot x_2) &= F \cdot \exp(+\mathrm{j}k_1 \cdot x_2) \end{aligned} \tag{3.12}$$

and the second one gives:

$$\begin{aligned} \frac{\mathrm{d}\,\Psi_{\mathrm{II}}(x_2)}{\mathrm{d}x} &= \frac{\mathrm{d}\,\Psi_{\mathrm{III}}(x_2)}{\mathrm{d}x} \\ k_2 \cdot \big(C \cdot \exp(+k_2 \cdot x_2) - D \cdot \exp(-k_2 \cdot x_2)\big) &= \mathrm{j}k_1 \cdot F \cdot \exp(+\mathrm{j}k_1 \cdot x_2). \end{aligned} \tag{3.13}$$

The tunneling probability is actually the ratio of transmitted to the incoming wavefunction and is defined by the squared amplitude of $\Psi_{\mathrm{t}}(x)$ and $\Psi_{\mathrm{in}}(x)$ as following:

$$T_{\mathrm{tun}} = \frac{|\Psi_{\mathrm{t}}(x)|^2}{|\Psi_{\mathrm{in}}(x)|^2} = \frac{|F \cdot \exp(+\mathrm{j}k_1 \cdot x)|^2}{|A \cdot \exp(+\mathrm{j}k_1 \cdot x)|^2} = \frac{|F|^2}{|A|^2}. \tag{3.14}$$

If the energy of a particle is lower than the barrier ($E < U_0$), then by replacing the Eq. (3.10) – (3.13) into the Eq. (3.14) the solution to T_{tun} reads as [7, 8, 49]:

$$\begin{aligned} T_{\mathrm{tun}} &= \frac{1}{1 + \left(\frac{k_1^2 + k_2^2}{2k_1 k_2}\right)^2 \cdot \sinh^2(k_2 \cdot (x_2 - x_1))} \\ &= \frac{1}{1 + \frac{U_0^2}{4E \cdot (U_0 - E)} \cdot \sinh^2\left(\frac{L_{\mathrm{b}}}{\hbar} \cdot \sqrt{2m^* \cdot (U_0 - E)}\right)}. \end{aligned} \tag{3.15}$$

The particles with higher energy ($E > U_0$) do not tunnel through the barrier indeed. The

transmission mechanism here is called *thermionic emission* and T_{tun} is:

$$T_{\text{tun}} = \frac{1}{1 + \left(\frac{k_1^2 + k_2^2}{-2k_1k_2}\right)^2 \cdot \sin^2(-k_2 \cdot (x_2 - x_1))} = \frac{1}{1 + \frac{U_0^2}{4E \cdot (U_0 - E)} \cdot \sin^2\left(\frac{L_{\text{b}}}{\hbar} \cdot \sqrt{2m^* \cdot (U_0 - E)}\right)}. \tag{3.16}$$

3.4.2 Triangular Barrier

When it comes to energy barrier in sense of the band structure of the device, the shape of the barrier is more complex than a rectangle. In consideration of the fact that the barrier associated with TFET is similar to a triangle, here a triangular shape energy barrier (see Fig. 3.7) is presented and it is shown how T_{tun} is attained for it.

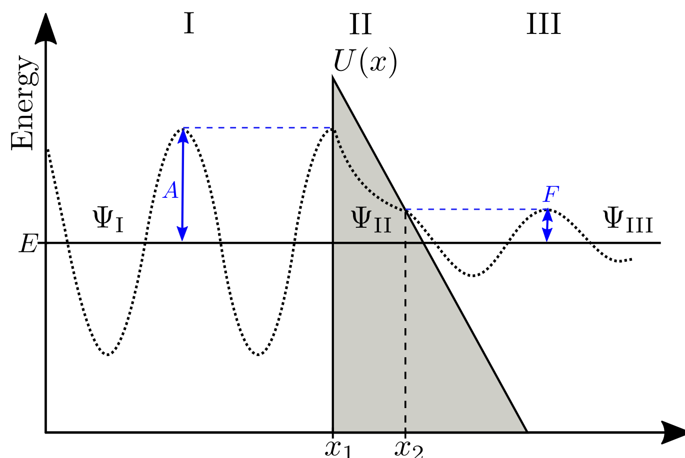

Figure 3.7: The wavefunction of a particle tunneling through a triangular barrier.

For U varying with the position, solving the Schödinger equation and consequently the calculation of the T_{tun} is complicated and time consuming. Therefore, in this case some methods to estimate the T_{tun} are developed. Among them *Wentzel–Kramers–Brillouin–Approximation* known as *WKB* method is the most used one. This semi–classical approximation is commonly used for quantum mechanics problems where the wavefunction is assumed to be an exponential function similar to the case in region II. Hence, the wavefunction reads as [7]:

$$\Psi(x) = \Theta(x) \cdot \exp(\pm \mathrm{j} k_3(x)) \tag{3.17}$$

with an amplitude of $\Theta(x)$ and a phase of $k_3(x)$ which for the case that $E < U(x)$ is defined as:

$$k_3(x) = \sqrt{\frac{2m^* \cdot (U(x) - E)}{\hbar}}. \tag{3.18}$$

If $U(x)$ changes very slowly in comparison to the constant de Brogli wavelength ($\lambda = {}^{2\pi}/_{k_3}$), then in a region including many full wavelengths the potential can be considered as constant [53]. In other words, for $\Theta(x)$ and $k_3(x)$ both varying slowly, the wavefunction remains practically exponential.

Now in order to see how the WKB method is derived, first the wavefunction is rewritten as [35]:

$$\Psi(x) = \Theta(x) \cdot \exp(\mathrm{j}\phi(x)). \tag{3.19}$$

Furthermore, the second derivative of the wavefunction gives:

$$\frac{\mathrm{d}^2\Psi(x)}{\mathrm{d}x^2} = \left(k_3(x)\right)^2 \cdot \Psi(x). \tag{3.20}$$

Replacing Eq. (3.19) in Eq. (3.20) leads to:

$$\frac{\mathrm{d}^2\Theta(x)}{\mathrm{d}x^2} + 2\mathrm{j} \cdot \frac{\mathrm{d}\Theta(x)}{\mathrm{d}x} \cdot \frac{\mathrm{d}\phi(x)}{\mathrm{d}x} + \mathrm{j}\Theta(x) \cdot \frac{\mathrm{d}^2\phi(x)}{\mathrm{d}x^2} - \Theta(x) \cdot \left(\frac{\mathrm{d}\phi(x)}{\mathrm{d}x}\right)^2 = \left(k_3(x)\right)^2 \cdot \Theta(x), \tag{3.21}$$

which brings about two separate equations, one for the real part:

$$\frac{\mathrm{d}^2\Theta(x)}{\mathrm{d}x^2} - \Theta(x) \cdot \left(\frac{\mathrm{d}\phi(x)}{\mathrm{d}x}\right)^2 = \left(k_3(x)\right)^2 \cdot \Theta(x) \;\Rightarrow\; \frac{\mathrm{d}^2\Theta(x)}{\mathrm{d}x^2} = \Theta(x) \cdot \left[\left(\frac{\mathrm{d}\phi(x)}{\mathrm{d}x}\right)^2 + \left(k_3(x)\right)^2\right] \tag{3.22}$$

and the other one for the imaginary part:

$$2\mathrm{j} \cdot \frac{\mathrm{d}\Theta(x)}{\mathrm{d}x} \cdot \frac{\mathrm{d}\phi(x)}{\mathrm{d}x} + \mathrm{j}\Theta(x) \cdot \frac{\mathrm{d}^2\phi(x)}{\mathrm{d}x^2} = 0 \;\Rightarrow\; \frac{\mathrm{d}}{\mathrm{d}x}\left(\Theta^2(x) \cdot \frac{\mathrm{d}\phi(x)}{\mathrm{d}x}\right) = 0. \tag{3.23}$$

Regarding Eq. (3.23) it can be concluded that the term $\Theta^2(x) \cdot {}^{\mathrm{d}\phi(x)}/_{\mathrm{d}x}$ is equal to a constant value which links the phase and amplitude of the wavefunction:

$$\Theta(x) = \frac{C}{\sqrt{\left|\frac{\mathrm{d}\phi(x)}{\mathrm{d}x}\right|}}. \tag{3.24}$$

Considering that the amplitude varies slowly with x, the second derivative of Θ is approximately equal to zero. Hence, Eq. (3.22) leads to:

$$\left(\frac{\mathrm{d}\phi(x)}{\mathrm{d}x}\right)^2 = -\big(k_3(x)\big)^2 \;\Rightarrow\; \phi(x) = \pm \mathrm{j}\int |k_3(x)|\mathrm{d}x. \tag{3.25}$$

By implementing the solutions for the amplitude and phase the wavefunction is approximated as:

$$\Psi(x) \cong \frac{C}{\sqrt{|k_3(x)|}} \cdot \exp\left(\pm \int |k_3(x)|\mathrm{d}x\right). \tag{3.26}$$

Based on the aforementioned assumptions and results, now the T_{tun} can be also estimated. Starting with the wave function within the triangular barrier:

$$\Psi_{\mathrm{II}}(x) \cong \frac{C}{\sqrt{|k_3(x)|}} \cdot \exp\left(+\int_x |k_3(x)|\,\mathrm{d}x\right) + \frac{D}{\sqrt{|k_3(x)|}} \cdot \exp\left(-\int_x |k_3(x)|\,\mathrm{d}x\right), \tag{3.27}$$

where C refers to the amplitude of the incoming wave and D represents the amplitude of the reflected part inside the barrier.

Recalling that the tunneling probability is equal to the ratio of the squared amplitude of the transmitted to the incoming wavefunction and considering Fig. 3.7, in this case the T_{tun} is defined as:

$$\begin{aligned} T_{\mathrm{tun}} = \frac{|F|^2}{|A|^2} &\cong \exp\left(-2\cdot\int_{x_1}^{x2} |k_3(x)|\,\mathrm{d}x\right) \\ &= \exp\left(-2\cdot\int_{x_1}^{x2} \left|\sqrt{\frac{2m^*\cdot(U(x)-E)}{\hbar^2}}\right|\,\mathrm{d}x\right). \end{aligned} \tag{3.28}$$

It must be kept in mind that this solution is only valid if $U(x)$ varies very slowly. For an energy barrier that varies linearly following equation is valid:

$$\begin{aligned} T_{\mathrm{tun}} &= \exp\left(-2\cdot\int_{x_1}^{x_2} \left|\sqrt{\frac{2m^*}{\hbar^2}\cdot\left(\left[-\frac{U(x_1)-E}{x_2-x_1}\cdot x + E\right] - E\right)}\right|\,\mathrm{d}x\right) \\ &= \exp\left(-\frac{4}{3}\cdot\sqrt{\frac{2m^*}{\hbar^2}\cdot\frac{U(x_1)-E}{x_1-x_2}}\cdot\left(x_2^{3/2}-x_1^{3/2}\right)\right). \end{aligned} \tag{3.29}$$

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3.5 Poisson's and Laplace's Equations

The Poisson's equation is a partial differential equation which is widely used for describing the electrical function of field–effect transistors [8, 54]. It is arisen from the Gaussian law of the Maxwell's equation:

$$\nabla \cdot \vec{E}(r) = \frac{\rho(r)}{\varepsilon}, \tag{3.30}$$

in which the divergence of the electric field $\vec{E}(r)$ is related to the charge density ρ and ε is the constant permittivity of the homogeneous material [35, 54]. For the electric field and potential Φ in 3D Cartesian coordinates applies:

$$E(x,y,z) = -\left(\frac{\partial \Phi}{\partial x} + \frac{\partial \Phi}{\partial y} + \frac{\partial \Phi}{\partial z}\right). \tag{3.31}$$

Considering the Laplace's operator (Δ) which is:

$$\Delta = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}, \tag{3.32}$$

combining the Eq. (3.30) and Eq. (3.31) results in the Poisson's equation:

$$\Delta \Phi(x,y,z) = -\frac{\rho(x,y,z)}{\varepsilon}. \tag{3.33}$$

The Laplace's equation refers to the special case of the Poisson's equation in which no space charge is existing:

$$\Delta \Phi(x,y,z) = 0. \tag{3.34}$$

The solutions of the Laplace's equation are known as *harmonic functions* and in fact there are infinite number of them, yet they must fulfill some conditions. A harmonic function needs to have continuous second–order derivative and hold the superposition principle [54, 55]. Furthermore, the solution to the Laplace's equation must satisfy one of the specific boundary conditions on the enclosing boundary, in a way that maximum and minimum amounts are achieved only on the surface and not within the defined region. In general the boundary conditions can be characterized in three groups [35, 55–57]:

1. Dirichlet condition also known as the boundary value problem of the first kind: the value of the harmonic function $\Phi(x,y,z)$, when it gets close to the edge of the enclosed boundary, on the entire area is predetermined.

2. Neumann condition also known as the boundary value problem of the second kind: the value of the normal derivative of the harmonic function $\vec{n} \cdot \nabla\Phi(x,y,z)$, when it reaches the

edge of the enclosed boundary, on the entire area is predetermined. Here the $\vec{n}$ describes the normal vector.

3. Mixed condition: a part of the boundary condition is defined by the Dirichlet condition and another part of it with the Neumann condition.

3.6 Lambert's W function

In the complex plane, the equation $f(x) = xe^x$ cannot be solved elementary to x. But by means of some numerical methods such as Newton or bisection method it is possible to approximate the roots of it. The Lambert's W function refers to a series of functions known as *branches* of this relation and is given as:

$$x = f^-1(xe^x) = W(xe^x). \tag{3.35}$$

This functions is named after *Johann Heinrich Lambert*, the swiss scientist, and is also known as omega function or product logarithm. In 1758 he published a series solution of the trinomial equation $x = q + x^m$ for x. Later in 1783, *Euler* transformed this equation to a more symmetrical form ($x^a - x^b = (a-b)cx^{(a+b)}$) and he also gave a series solution to this equation which reads [58]:

$$\begin{aligned} x^n =& 1 + nc + \frac{1}{2}n(n+a+b)c^2 \\ &+ \frac{1}{6}n(n+a+2b)(n+2a+b)c^3 \\ &+ \frac{1}{24}n(n+a+3b)(n+2a+2b)(n+3a+b)c^4 \\ &+ \ldots \end{aligned} \tag{3.36}$$

As the next step Euler considered the case in which $a = b$, and took the limits of his equation $(b \to a)$. This special case led to the following:

$$\ln x = cx^a. \tag{3.37}$$

Then by putting $a = 1$ and through the change in variable $z = x^a$, he obtained a convergent series solution and finally from this series he derived the standard form of the Lambert's W function (Eq. (3.35)).

Generally it can be said that the Lambert's W function is used to find the solution of transcendental equations. This function has many applications in different fields such as physics, mathematics, quantum statistics and biochemistry. Hence, it is implemented in many programming languages including MATLAB.

There are countably infinite number of branches of the W function. Figure 3.8 illustrates the two real branches of Lambert's W function plotted by MATLAB [59]. It can be seen that for $-e^{-1} < x < 0$, the equation $f(x) = xe^x$ has exactly two real solutions denoted by $W_0(x)$

and $W_{-1}(x)$. For $x \geq 0$, the equation $f(x) = xe^x$ has exactly one real solution which is $W_0(x)$. For $x = -e^{-1}$ this equation has exactly one real solution $W_0(-e^{-1}) = W_{-1}(-e^{-1}) = -1$. The $W_0(x)$ is called the *principle branch* and its series expansion is defined as following [60]:

$$W_0(x) = \sum_{n=1}^{\infty} \frac{(-1)^{n-1}(n)^{n-2}}{(n-1)!} x^n$$
$$= x - x^2 + \frac{3x^3}{2} - \frac{8x^4}{3} + \frac{125x^5}{24} - \frac{54x^6}{5} + \ldots \quad (3.38)$$

in which $(n-1)!$ shows the factorial. It must be mentioned that in this thesis the principal branch of the Lambert's W function in MATLAB is used to do the necessary calculations.

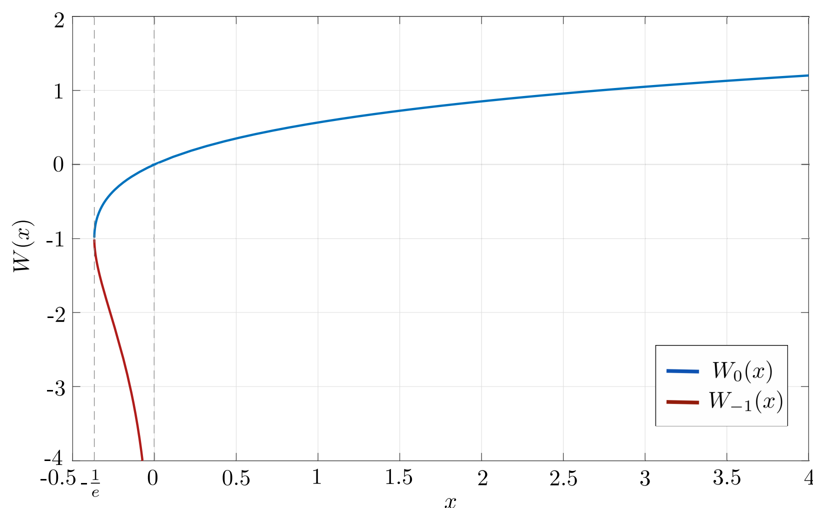


Figure 3.8: The real branches of the Lambert's W function.

CHAPTER 4

TFET Essentials

This chapter focuses on the structure of TFETs. It starts with Sec. 4.1 in which the geometry of the device that is considered in this work and the modeling is done for. In Sec. 4.2 considering the tunneling path in the device, two types of structures are introduced and discussed. Afterwards, with the help of the fundamentals explained in chapter 3 the working principle of TFETs is described in Sec. 4.3. This is followed by the clarification of the transfer characteristics in Sec. 4.4 and the output characteristics of TFETs in Sec. 4.5. The final section of this chapter is dedicated to characterizing the TFET capacitances.

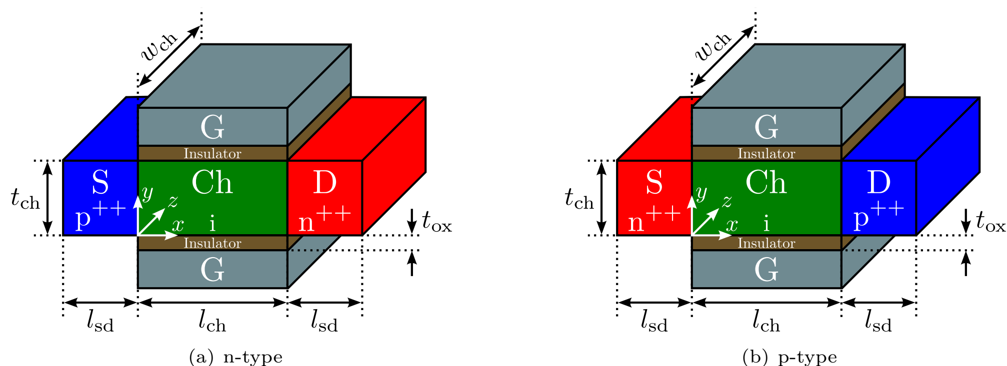
4.1 Device Geometry

TFETs are devices with three terminals called *source*, *gate* and *drain*. The drain current in TFETs arises from B2B tunneling. The tunneling probability depends on the band bending and tunneling distance which is controlled by the gate–to–source (V_{gs}) as well as the drain–to source (V_{ds}) bias [14].

These transistors are designed and also manufactured in various and very individual shapes such as single–gate (SG) planar, NWs and line–tunneling TFETs. In addition to the architecture of a TFET, the material that the device is made of plays an important role in enhancing its functionality. The goal is to increase the control of the gate over the channel region, reduce the unwanted and parasitic effect, such as leakage current and TAT, and all in all improving the performance of TFET.

The structure which is used for the compact modeling in this work is the DG TFET which is depicted in Fig. 4.1. The symmetry of the DG TFET enables the simplicity of the model and allows for implementation of it for other structures.

Depending on the doping type of the source and drain, TFETs are divided in two categories: n–type which refers to the p–i–n structure (see Fig. 4.1(a)) and p–type TFET, the n–i–p structure, is illustrated in Fig. 4.1(b).



(a) n-type (b) p-type

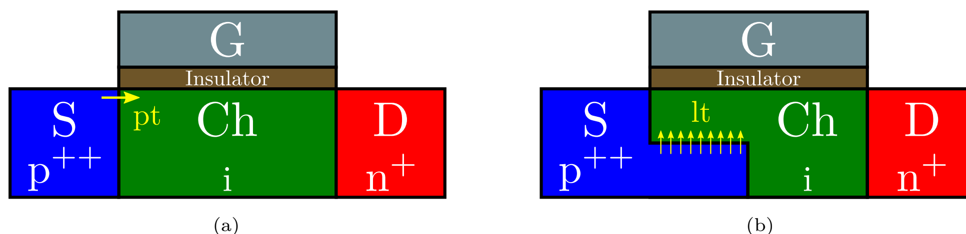
Figure 4.1: 3D sketch of (a) an n-type and (b) a p-type DG TFET geometry. The structural parameters are defined as follows: l_{ch} – channel length, t_{ch} – channel thickness, w_{ch} – channel width, t_{ox} – gate insulator (oxide) thickness, l_{sd} – length of source (S)/drain (D) region. Source and drain are highly doped and the channel is intrinsic.

Here it is considered that the source, drain and channel regions are made of Si, unless another applied material is mentioned. For the gate insulator a high–κ material (HfO_2) is used.

4.2 Point and Line Tunneling TFET

Considering the structure of a TFET, the alignment of the electric field which is caused by the gate bias, affects the tunneling direction. In this regard two types of tunneling paths in TFETs are specified: *point tunneling* and *line tunneling* [61].

Figure 4.2(a) illustrates a structure in which tunneling mainly occurs in the corner under the gate oxide at the source–channel junction. In fact, the tunneling paths start from source tunnel junction, bend around the aforementioned corner point and come to an end at the oxide–channel interface [61]. That is the reason why this type of tunneling is known point tunneling.



(a) (b)

Figure 4.2: Schematic of (a) n–type point tunneling TFET and (b) n–type line tunneling TFET. Point tunneling occurs at the source–channel interface under the gate oxide. Line tunneling takes place along the channel elongated with the gate's electric field [62].

Line tunneling refers to enlargement of the tunneling region. In the structure depicted in Fig. 4.2(b), tunneling happens not only around a little point at the corner, but also along the channel. Considering the gate overlap over the source, the tunneling paths are formed as straight lines in the direction of gate electric field, starting from source junction towards the oxide–channel interface.

In an ideal case, where the parasitic tunneling at edges and the effect of the drain voltage on the source can be neglected, line–tunneling TFETs show a very abrupt turn–on and also a higher on–current (I_{on}) in comparison with the point–tunneling TFETs [61, 63]. Hence, this structures are attracting attention to be able to overcome the low I_{on} problem of point–tunneling devices.

4.3 Working Principle

To explain the working principle of TFET, an n–type device is considered in this section. Regarding the geometry of a DG n–type TFET, the band diagram at the position beneath the gate oxide is depicted in Fig. 4.3. By taking into account the effect of applied voltage at TFET terminals on its band structure, three operation states are defined: *off*–, *on*– and *ambipolar–state*.

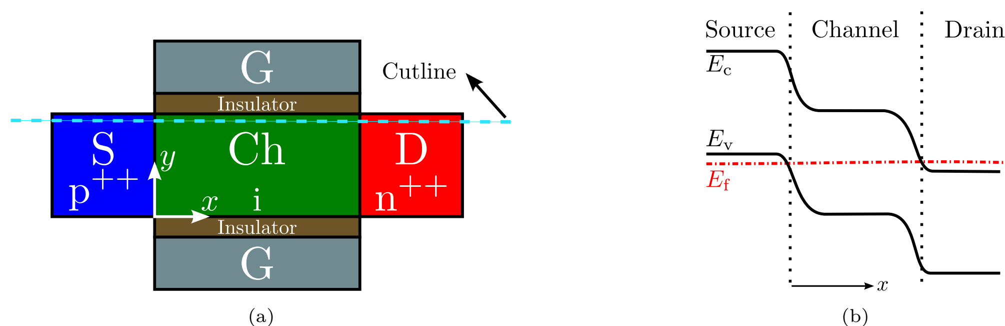
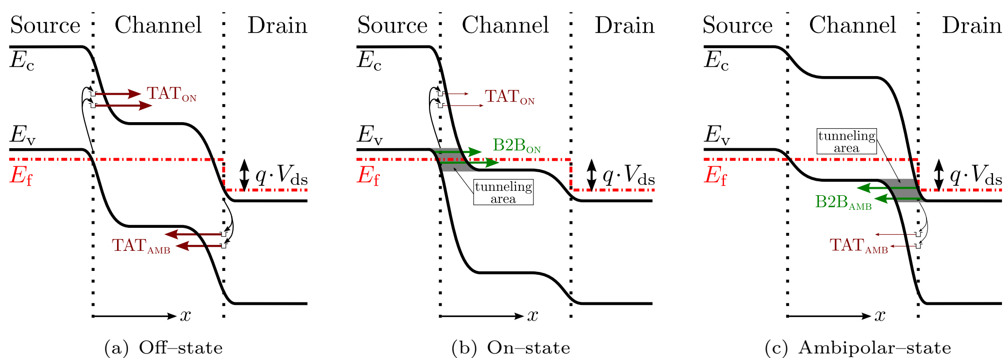


Figure 4.3: (a) 2D geometry of an n–type TFET. A cutline is made just under the gate oxide along the x–axis. (b) Band diagram of the unbiased device at the x–cutline.

4.3.1 Off–State

In this case the drain is connected to V_{ds} but no gate bias is applied ($V_{\mathrm{ds}} > 0$, $V_{\mathrm{s}} = 0$ and $V_{\mathrm{gs}} = 0$). As it can be seen in Fig. 4.4(a) there is no overlap between the valance band of the source and conduction band of the channel or the conduction band of the drain and the valence band of the channel. Therefore, it is expected that the charge carriers can not tunnel into the channel. Anyhow, because of the existence of the traps there is still the probability for carriers to tunnel through the source-channel or drain-channel barrier. The current caused by the TAT in off–state is known as the *leakage current* or *off–current* (see Fig. 4.5) [8].



(a) Off–state (b) On–state (c) Ambipolar–state

Figure 4.4: Band diagram of an n–type TFET for its different operation states. (a) In off–state there is only TAT occurring at both channel junctions, (b) in on–state additionally to the TAT there is also B2B tunneling at the source–to–channel junction and (c) in ambipolar–state tunneling occurs at the drain–to–channel junction [35].

4.3.2 On–State

To turn the TFET on, the charge carries need to flow through the channel. In order to do so, first it is necessary that the electrons tunnel through the potential barrier from source into the channel. Since the source is p–type, the occupied energy states are close to its valance band. Which means, the charge carriers are supposed to tunnel from valance band of the source to the conduction band of the channel [7]. By increasing the gate bias ($V_{ds} > 0$ and $V_{gs} > 0$) the band structure of the channel region decreases. At a certain point this increment in the voltage leads to an overlap between the valance band in the source region and the conduction band in the channel (see Fig. 4.4(b)). Hence, carriers can tunnel from source region into the channel, a conduction path is built under the gate oxide and the on–current flows through it. It must be considered that immediately after two bands overlap, the current starts to flow. Therefore, switching from off– to on–state takes place with an abrupt subthreshold swing [8].

By further increase in V_{gs}, the tunneling length becomes shorter and therefore the current increases. Moreover, the inversion charge layer, which is built under the gate oxide due to the gate bias, grows as well. When the magnitude of inversion layer reaches the point that gets comparable with the electron density of the drain, it causes *pinning* of the channel potential. The channel pinning refers to the incident in which the channel due to the inversion layer is connected to the drain. As the result the channel is shortened and its potential is almost equal to the drain potential. That is to say, after the channel potential is pinned to the drain potential, further increment in V_{gs} has less influence on the channel potential and consequently in increasing the current [7]. This effect can be seen in Fig. 4.5 in the on–state.

4.3.3 Ambipolar–State

When the gate is negatively biased ($V_{\mathrm{ds}} > 0$ and $V_{\mathrm{gs}} < 0$), the bands of the channel shift upwards. As this negative bias grows, the conduction band of the drain overlaps the valance band of the channel. Figure 4.4(c) depicts the band structure of an n–type TFET in ambipolar–state. In this case holes from conduction band of the drain can tunnel into the channel. This current, which is actually not desired in TFETs, is called *ambipolar–current* (see Fig: 4.5).

In addition to the holes B2B tunneling in this state, TAT takes place at the drain–to–channel junction as well. Nonetheless, the current caused by the TAT has a very small contribution to the total tunneling current.

As it is already mentioned, ambipolarity is an unwanted effect and increases the switching leakage in TFET inverters. Various approaches have been deployed to suppress the ambipolarity such as reducing the doping concentration of the drain, employing heterostructure with large band gap at drain side to enlarge the tunneling distance and from drain to channel, using heterogeneous gate dielectric and extending the gate over the drain region [64]. So far it seems to be impossible to get rid of this effect completely. However, ambipolarity can be taken as advantage to develop more compact circuits. For instance in [65] it is shown that by employing ambipolarity in designing logic gates, the number of logic levels, delay and power consumption can be reduced. Moreover in [66] it is considered how replacing unipolar transistors by ambipolar transistors affects and simplifies the analog as well as digital circuit design.

4.4 Transfer Characteristics

The transfer characteristics of TFETs is a curve which illustrates the output I_{ds} as a function of V_{gs}. In Fig. 4.5 the transfer characteristics of an n–type TFET, simulated in TCAD Sentaurus for varying drain biases, are shown. In this example different operating regions of the device can be seen.

The constant off–current is due to the traps which are defined at the tunneling junctions of the device. As it is explained in the previous section, by increasing V_{gs} the tunneling length decreases and therefore, the TAT current rises until the device is switched on and the B2B tunneling takes over. As it is depicted in Fig. 4.5 transferring from off to the on–state occurs abrupt and fast. In this case, the simulated device has a subthreshold swing of almost 30 mV/dec which is beyond the limit of 60 mV/dec for conventional MOSFETs.

By decreasing V_{gs} to negative voltages the output current again increases and the TFET switches to ambipolar–state. It is comparable with the on–state of a p–type device. In this setting, holes tunnel from drain junction into the channel and rise the I_{ds} [61].

Figure 4.5 shows that V_{ds} has a greater influence on the ambipolar–current than on the on–current. The reason is that in the on–state the source junction is the bottleneck for the current and changing the drain bias does not affect the band bending on the source side. Hence,

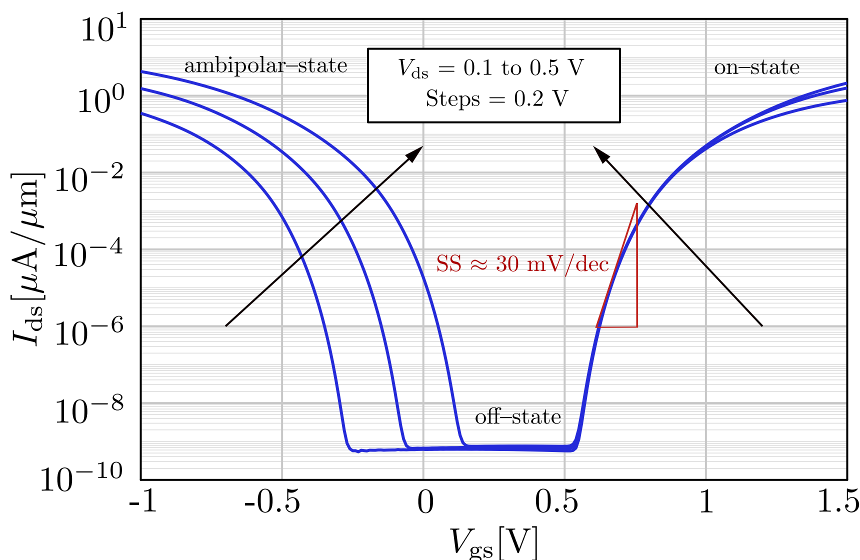


Figure 4.5: Transfer characteristics curves of an n-type TFET are simulated in TCAD for various V_{ds}. The device parameters are defined as following $l_{\mathrm{ch}} = 22$ nm, $t_{\mathrm{ch}} = 10$ nm, $t_{\mathrm{ox}} = 2$ nm and HfO_2 is used as insulator material [67].

by varying V_{ds} no obvious changes can be seen in I_{ds}. On the other hand, in ambipolar–state the drain junction controls the carrier injection in the channel. Considering Fig. 4.4, by increasing V_{ds} the overlap between the conduction band of the drain and the valance band of the channel becomes bigger. Consequently, the tunneling length become shorter and hence, as it is depicted in Fig. 4.5, the ambipolar–state is reached earlier or in other words, it occurs at higher V_{gs}.

4.5 Output Characteristics

The output characteristics refers to a current Vs. voltage curve which depicts the behavior of I_{ds} as a function of V_{ds}. Figure 4.6 shows the output characteristic curves of an n–type TFET simulated in TCAD Sentaurus. It can be seen that for a fixed V_{gs}, increasing V_{ds} leads to higher I_{ds}. In order to clarify the reason of this pattern, the case is considered in which the conduction band of the channel falls below the valence band of the source due to the high V_{gs}.

In this situation the transistor is in on–state and the carriers at source junction are injected into the channel and from this point the current is under the control of drain. Hence, the higher V_{ds} the higher I_{ds}. TFET in this part of the output characteristics is in *linear region*. This increment continues until V_{ds} reaches a specific amount known as *saturation voltage* ($V_{\mathrm{ds,sat}}$). From this point, since the carrier injection has already reached its maximum and the source can not provide the channel with more charges, increasing V_{ds} can not enhance the current any further. In this condition the TFET is known to be in its *saturation region*.

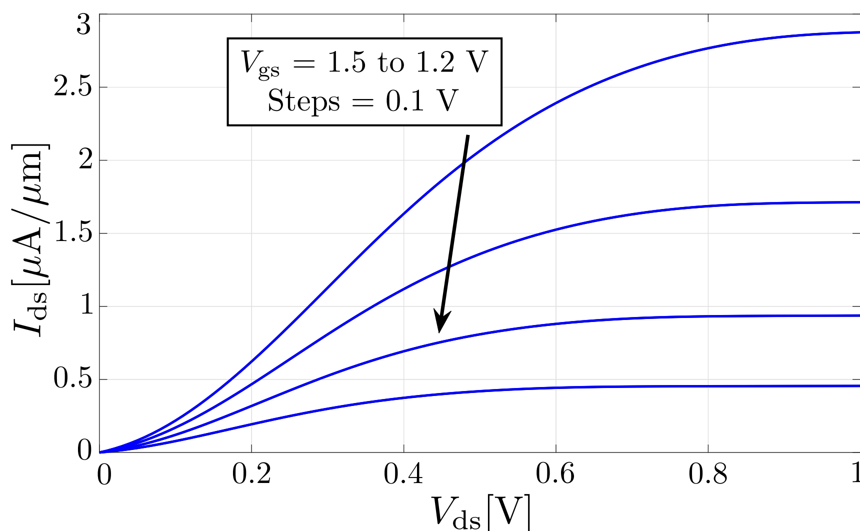


Figure 4.6: Output characteristic curves of an n–type TFET simulated in TCAD for varying V_{gs}. The device parameters are defined as following l_{ch} = 22 nm, t_{ch} = 10 nm, t_{ox} = 2 nm HfO_2 [67].

4.6 Capacitances in TFET

The transient behavior of a TFET is due to its capacitive components which are caused by the stored charges in the device [1]. Figure 4.8 shows the *extrinsic* and *intrinsic* capacitances of a DG TFET which resemble to those in a MOSFET.

Extrinsic Capacitances

Extrinsic capacitances also known as *parasitic capacitances* are of two types. Those which are formed as the result of device fabrication and the junction capacitances which are contributed to the overlaps in construction of the transistor:

- In the manufacturing process of TFETs after doping the source and drain region the semiconductor must undergo a high temperature treatment called *annealing*. This leads to a lateral diffusion of the dopant atoms at the boundary between doped and intrinsic material. Consequently, this border would not be sharp and clear. As the result, the gate overlaps the source and also the drain region. The capacitances C_{GS0} and C_{GD0} which are depicted in Fig. 4.8 are caused by this overlap and are called *gate overlap capacitances* [1].

- The other sort of extrinsic capacitances are those which are formed between bulk and terminals such as C_{BS}, C_{BD} and C_{BG} shown in Fig. 4.8. It must be considered that since TFETs are grown on a wafer with a buried oxide layer, the influence of bulk is negligible.

Intrinsic Capacitances

The intrinsic part of the transistor includes channel, oxide, gate, source and drain junction. The capacitances in this portion of device appear by variations of the voltage at TFET terminals and are risen from the channel charges [1].

In DC analysis it is considered that the mobile charges flow from source to the drain. But in the dynamic analysis, in addition to this flow, the charge current generated by stored charges at the terminals must also be taken into account. Figure 4.7 illustrates the dynamic currents at source (i_s), drain (i_d) and gate (i_g) which are associated with the the stored charges at each corresponding terminal [1].

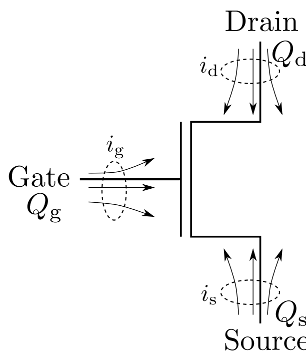


Figure 4.7: Dynamic current associated with the stored charges at the terminals of a TFET [1].

Since the charges at terminals of TFET are a function of applied voltages, the dynamic current flowing through each terminal is formulated as following [1]:

$$i_\mathrm{j} = \frac{dQ_\mathrm{j}}{dt} = \frac{\partial Q_\mathrm{j}}{\partial V_\mathrm{g}}\frac{\partial V_\mathrm{g}}{\partial t} + \frac{\partial Q_\mathrm{j}}{\partial V_\mathrm{s}}\frac{\partial V_\mathrm{s}}{\partial t} + \frac{\partial Q_\mathrm{j}}{\partial V_\mathrm{d}}\frac{\partial V_\mathrm{d}}{\partial t}, \tag{4.1}$$

where Q refers to the charge at the terminal and $\mathrm{j} = \mathrm{g, s, d}$. According to this equation, it can be concluded that at every terminal two capacitances corresponding to other terminals known as *trans–capacitances* and one so called *self capacitance* are existing. That means in total TFET has nine intrinsic capacitances which show how the charge at the terminal i changes with respect to the applied voltage at terminal j and by keeping other voltages constant. Generally this capacitances are defined as [1]:

$$C_{ij} = \begin{cases} -\dfrac{\partial Q_i}{\partial V_j}, & i \neq j \quad i,j = g,s,d \\ +\dfrac{\partial Q_i}{\partial V_j}, & i = j \end{cases} \tag{4.2}$$

All these capacitances can be written together in a matrix as follows:

$$C_{ij} \equiv \begin{bmatrix} C_{gg} & -C_{gd} & -C_{gs} \\ -C_{dg} & C_{dd} & -C_{ds} \\ -C_{sg} & -C_{sd} & C_{ss} \end{bmatrix}. \tag{4.3}$$

The positive and negative signs in these expressions refer to the fact that when the voltage at one terminal increases, the charge at that node also increases, and when the voltage at other terminals increases, the amount of charge decreases. Taking into account the charge conservation law in the device, the sum of each row and column of this matrix must be equal to zero [1]. Thus, each self capacitance can be written in terms of two other capacitances as following:

$$C_{gg} = C_{gs} + C_{gd} = C_{sg} + C_{dg} \tag{4.4}$$

$$C_{ss} = C_{sd} + C_{sg} = C_{ds} + C_{gs} \tag{4.5}$$

$$C_{dd} = C_{ds} + C_{dg} = C_{sd} + C_{gd}. \tag{4.6}$$

In Fig. 4.8 the intrinsic part is surrounded by a yellow dashed line. Considering the TCAD simulation results, the gate–drain (C_{gd}) and the drain–gate capacitances (C_{dg}) as well as the gate–source (C_{gs}) and the source–gate capacitances (C_{sg}) in TFET are similar. Hence, in this work these capacitances are taken to be equivalent:

$$C_{sg} = C_{gs}, \tag{4.7}$$

$$C_{dg} = C_{gd}. \tag{4.8}$$

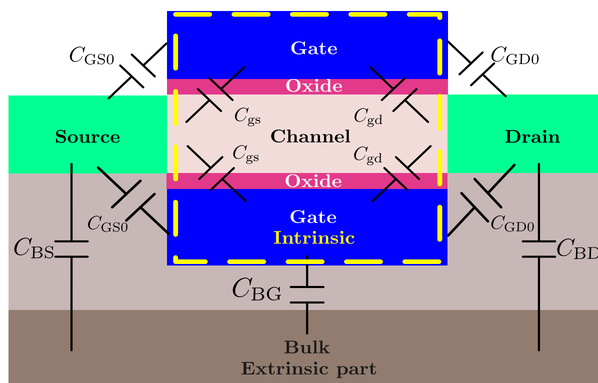
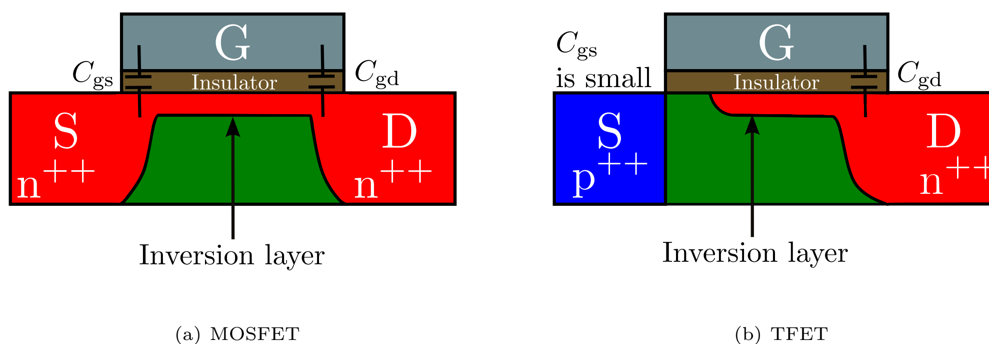


Figure 4.8: Extrinsic and intrinsic capacitances in the structure of a DG TFET.

It must be mentioned that despite the analogy between TFET and MOSFET structure, there is a significant difference in inversion charge distribution in these two types of transistors. For a MOSFET operating in its linear region both source and drain are connected to the inversion channel. Therefore, the charges in channel are equally assigned to the source and drain which means C_{gs} and C_{gd} are equal (see Fig. 4.9). Considering a TFET at $V_{\mathrm{ds}} > 0$, for low gate voltage the inversion layer is built up near the drain junction and first by increasing the V_{gs} this layer is extended towards the source junction. Thus, in a TFET C_{gs} and C_{gd} are not equal [14, 36].



(a) MOSFET (b) TFET

Figure 4.9: Inversion charge distribution in (a) a MOSFET and (b) in a TFET to the source and channel for $V_{\mathrm{ds}} > 0$ and $V_{\mathrm{gs}} > 0$ are illustrated [36].

CHAPTER 5

Model Development

The switching speed of a transistor and generally the dynamic behavior of TFET–based circuits is precisely associated with the capacitances in transistor's construction. Since intrinsic capacitances are much bigger in comparison to the extrinsic ones, they have a greater affect on transient behavior of the TFET. Hence, the focus of this thesis lays on compact modeling of intrinsic capacitances in the TFET structure (see Fig. 4.8).

The compact model is a charge–based model and capacitances are calculated by means of a compact expression for total mobile charge in the channel. In this regard, in Sec. 5.1 the compact expression to calculate the total charge is derived. Considering this expression in Sec. 5.2 intrinsic capacitances are determined. Finally the effect of parasitic elements as well as extrinsic capacitances are added to the model in Sec. 5.3.

5.1 Charge Calculation

In [68] the 1D surface potential in TFET is defined as following:

$$\Phi_{1\mathrm{D}} = \frac{k_{\mathrm{B}}T}{q} \cdot \ln\left(\frac{N_{\mathrm{ch}} \cdot N_{\mathrm{inv}}}{n_{\mathrm{i}}^2}\right), \tag{5.1}$$

where N_{ch} is the channel doping concentration, N_{inv} shows the inversion charge density and n_{i} is the intrinsic electron concentration in silicon. The expression $\frac{k_{\mathrm{B}}T}{q}$ is also well–known as the thermal voltage and is shown with V_{th}. Assuming that $\Phi_{1\mathrm{D}}$ represents an average value for the potential profile from gate to gate, by rearranging the Eq. 5.1, the 1D mobile charge per gate area is expressed as [57, 69]:

$$Q'_{\mathrm{m}} = \int_0^{t_{\mathrm{ch}}} q\,\frac{n_{\mathrm{i}}^2}{N_{\mathrm{inv}}} \cdot \exp\left(\frac{\Phi_{1\mathrm{D}}}{V_{\mathrm{th}}}\right) dy = q\,t_{\mathrm{ch}}\,\frac{n_{\mathrm{i}}^2}{N_{\mathrm{inv}}} \cdot \exp\left(\frac{\Phi_{1\mathrm{D}}}{V_{\mathrm{th}}}\right). \tag{5.2}$$

Hence, the 1D Poisson's equation in terms of integral inversion charge along the gate to gate line reads as following expression [57, 69, 70]:

$$C'_{\mathrm{eff}} \cdot (V_{\mathrm{gs}} - V_{\mathrm{fb}} - \Phi_{1\mathrm{D}}) = \frac{Q'_{\mathrm{m}}}{2} = q\,\frac{t_{\mathrm{ch}}}{2}\,\frac{n_{\mathrm{i}}^2}{N_{\mathrm{inv}}} \cdot \exp\left(\frac{\Phi_{1\mathrm{D}}}{V_{\mathrm{th}}}\right). \tag{5.3}$$

V_{fb} presents the flat–band voltage which refers to the voltage that needs to be applied at the gate in order to have flat energy bands at the surface of the semiconductor [1]. C'_{eff} is the effective oxide capacitance per gate area. It is assumed that the charge centroid is located within the channel in a small distance from the Si–SiO_2 interface. Hence, C'_{eff} as it is shown in Fig. 5.1 includes the oxide (C'_{ox}) and depletion capacitances (C'_{dep}) per gate area in series [67]:

$$C'_{\mathrm{eff}} = \frac{1}{\frac{1}{C'_{\mathrm{ox}}} + \frac{1}{C'_{\mathrm{dep}}}} \tag{5.4}$$

The derivative of Eq. (5.3) regarding the surface potential leads to:

$$\frac{\partial V_{\mathrm{gs}}}{\partial \Phi_{1\mathrm{D}}} = 1 + \frac{q}{C'_{\mathrm{eff}} V_{\mathrm{th}}}\,\frac{t_{\mathrm{ch}}}{2}\,\frac{n_{\mathrm{i}}^2}{N_{\mathrm{inv}}} \cdot \exp\left(\frac{\Phi_{1\mathrm{D}}}{V_{\mathrm{th}}}\right) = 1 + \frac{Q'_{\mathrm{m}}}{2C'_{\mathrm{eff}} V_{\mathrm{th}}}. \tag{5.5}$$

Now considering Eq. (5.2) and Eq. (5.5), $\frac{\partial Q'_{\mathrm{m}}}{\partial V_{\mathrm{gs}}}$ can be written as:

$$\frac{\partial Q'_{\mathrm{m}}}{\partial V_{\mathrm{gs}}} = \frac{\partial Q'_{\mathrm{m}}}{\partial \Phi_{1\mathrm{D}}} \cdot \frac{\partial \Phi_{1\mathrm{D}}}{\partial V_{\mathrm{gs}}} = \frac{Q'_{\mathrm{m}}}{V_{\mathrm{th}}} \cdot \frac{1}{\frac{Q'_{\mathrm{m}}}{2C'_{\mathrm{eff}} V_{\mathrm{th}}} + 1}. \tag{5.6}$$

In order to include the short–channel effect on subthreshold swing in charge calculation an empirical method is introduced in [71]. This approach is derived from the 3D potential solution at the barrier of short–channel silicon–on–insulator (SOI) multi–gate FETs described in [72]. In this method, first the subthreshold swing by means of the surface potential at two

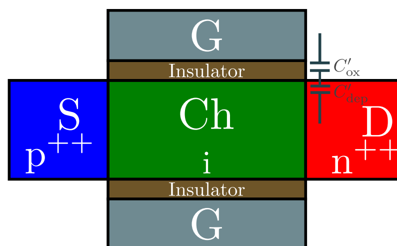


Figure 5.1: The effective oxide capacitance of TFET consists of two capacitances C'_{ox} and C'_{dep} which are placed in series.

gate potentials ($\Phi_\mathrm{s}(\Phi_\mathrm{g})$) with a difference of $dV = 0.1\mathrm{V}$ is estimated as following:

$$S = V_\mathrm{th}\ln(10)\cdot\frac{dV}{\Phi_\mathrm{s}(dV)-\Phi_\mathrm{s}(0))}. \tag{5.7}$$

Afterward, the slope degradation factor (α), which refers to the ratio between the degraded swing and the ideal subthreshold swing (S_ideal), is defined as following:

$$\alpha = \frac{S}{S_\mathrm{ideal}} = \frac{S}{60\,\mathrm{mV/dec}}. \tag{5.8}$$

It needs to be mentioned that α is used as a fitting parameter in intrinsic capacitance model.

Finally, by including this factor the Eq. (5.6) is modified and results in the following:

$$\frac{\partial Q'_\mathrm{m}}{\partial V_\mathrm{gs}} = \frac{\partial Q'_\mathrm{m}}{\partial \Phi_\mathrm{1D}}\cdot\frac{\partial \Phi_\mathrm{1D}}{\partial V_\mathrm{gs}} = \frac{Q'_\mathrm{m}}{V_\mathrm{th}}\cdot\frac{1}{\frac{Q'_\mathrm{m}}{2C'_\mathrm{eff}V_\mathrm{th}}+\alpha}. \tag{5.9}$$

In order to obtain the ∂V_gs in terms of Q_m, Eq. (5.9) is rearranged to:

$$\partial V_\mathrm{gs} = \left(\frac{\alpha V_\mathrm{th}}{Q'_\mathrm{m}}+\frac{1}{2C'_\mathrm{eff}}\right). \tag{5.10}$$

Aiming to include the effect of the channel width of the device in the charge model, an approximation is made to replace Q'_m by $Q'_\mathrm{i} = Q'_\mathrm{m,2D}/w_\mathrm{ch}$ which is the integral inversion charge normalized regarding the channel width [69]. Thus, the total mobile charge in the channel per gate width can be achieved by integration as follows:

$$\int_{V_0}^{V_\mathrm{gs}} dV_\mathrm{gs} = \int_{Q'_\mathrm{i,0}}^{Q'_\mathrm{i}}\left(\frac{\alpha V_\mathrm{th}}{Q'_\mathrm{i}}+\frac{1}{2C'_\mathrm{eff}}\right)dQ'_\mathrm{i} \tag{5.11}$$

$$V_\mathrm{gs}-V_0 = \alpha V_\mathrm{th}\ln\left(\frac{Q'_\mathrm{i}}{Q'_\mathrm{i,0}}\right)+\frac{Q'_\mathrm{i}-Q'_\mathrm{i,0}}{2C'_\mathrm{eff}}. \tag{5.12}$$

To solve this equation for Q'_i, firstly by means of the natural logarithm properties it can be rewritten as:

$$\ln\left(\exp\left(\frac{2C'_\mathrm{eff}(V_\mathrm{gs}-V_0)+Q'_\mathrm{i,0}}{2C'_\mathrm{eff}V_\mathrm{th}\alpha}\right)\right)+\ln(Q'_\mathrm{i,0}) = \ln(Q'_\mathrm{i})+\frac{Q'_\mathrm{i}}{2C'_\mathrm{eff}\alpha V_\mathrm{th}}. \tag{5.13}$$

Now, in order to bring this equation into the form which makes it possible to use the Lambert

function ($xe^x = y$), from both sides of the equation $\ln(2C'_{\text{eff}}V_{\text{th}}\alpha)$ is subtracted and leads to:

$$\ln\left(\exp\left(\frac{2C'_{\text{eff}}(V_{\text{gs}}-V_0)+Q'_{\text{i},0}}{2C'_{\text{eff}}V_{\text{th}}\alpha}\right)\right)+\ln\left(\frac{Q'_{\text{i},0}}{2C'_{\text{eff}}V_{\text{th}}\alpha}\right) = \ln\left(\frac{Q'_{\text{i}}}{2C'_{\text{eff}}V_{\text{th}}\alpha}\right)+\ln\left(\exp\left(\frac{Q'_{\text{i}}}{2C'_{\text{eff}}\alpha V_{\text{th}}}\right)\right) \tag{5.14}$$

which results in:

$$\frac{Q'_{\text{i}}}{2C'_{\text{eff}}V_{\text{th}}\alpha}\exp\left(\frac{Q'_{\text{i}}}{2C'_{\text{eff}}\alpha V_{\text{th}}}\right)=\frac{Q'_{\text{i},0}}{2C'_{\text{eff}}V_{\text{th}}\alpha}\exp\left(\frac{2C'_{\text{eff}}(V_{\text{gs}}-V_0)+Q'_{\text{i},0}}{2C'_{\text{eff}}V_{\text{th}}\alpha}\right). \tag{5.15}$$

So, by applying the principle branch of the Lambert's W function [58] to the Eq. (5.15) the expression for the mobile charge per gate area is obtained:

$$Q'_{\text{i}} = 2C'_{\text{eff}}V_{\text{th}}\alpha \times W\left(\frac{Q'_{\text{i},0}}{2C'_{\text{eff}}V_{\text{th}}\alpha}exp\left(\frac{2C'_{\text{eff}}(V_{\text{gs}}-V_0)+Q'_{\text{i},0}}{2C'_{\text{eff}}V_{\text{th}}\alpha}\right)\right). \tag{5.16}$$

According to the explanations given in [69], $Q'_{\text{i},0}$ is actually referring to the integral inversion charge per gate area for an arbitrary gate bias of V_0 in the subthreshold regime. Considering the Eq. (5.11), $Q'_{\text{i},0}$ shows the lower limit of the integral and is supposed to assure the minimum value of the charge in the channel of the transistor. Hence, in the compact model it is calculated as follows:

$$Q'_{\text{i},0} = qN_{\text{ch}}t_{\text{ch}}. \tag{5.17}$$

In the TFET intrinsic capacitance model V_0 is a fitting parameter that controls when capacitances start to increase. This parameter is defined separately as $V_{0,\text{gs}}$ and $V_{0,\text{gd}}$ in the calculation of C_{gs} and C_{gd}, respectively [67].

5.2 Intrinsic Capacitance Model

To obtain the capacitances in TFET, the calculations are done separately for the on–state and the ambipolar–state. It is considered that the tunneling barrier in the on–state is located close to the source junction and in the ambipolar–state it is at the drain side. In each case, the mobile charge density at two points of the channel, including the position of the tunneling barrier and the edge of the channel, is computed using the voltage drop between them. By having the charge density at these two points, the total mobile charge of the channel and then the capacitances are calculated. In the following all these calculations are explained in detail.

First, in order to capture the effect of drain and source bias on channel charge, the parameter

V is implemented in Eq. (5.16) as follows:

$$Q'_{\rm i} = 2C'_{\rm eff}V_{\rm th}\alpha \times W\left(\frac{Q'_{\rm i,0}}{2C'_{\rm eff}V_{\rm th}\alpha}exp\left(\frac{2C'_{\rm eff}(V_{\rm gs}-V-V_0)+Q'_{\rm i,0}}{2C'_{\rm eff}V_{\rm th}\alpha}\right)\right). \tag{5.18}$$

Then, to calculate the total channel charge in the on–state, the mobile charge is calculated at the drain junction ($Q'_{\rm j,d}$) and also close to the tunneling barrier on the source side ($Q'_{\rm b,s}$). $Q'_{\rm j,d}$ and $Q'_{\rm b,s}$ are obtained by solving the Eq. (5.18) for $V = V_{\rm ds}$ and $V = V_{\rm ds} - \Delta V$, respectively. As it is illustrated in Fig. 5.2(a), the tunneling barrier in the on–state is located within the channel in a distance of $X_{\rm b,s}$ from source–channel junction. The total mobile charge in the on–state is given as:

$$Q_{\rm on} = \frac{Q'_{\rm j,d}+Q'_{\rm b,s}}{2}w_{\rm ch}(l_{\rm ch}-X_{\rm b,s}). \tag{5.19}$$

In the ambipolar–state, the charge per gate area is once calculated at the source junction ($Q_{\rm j,s}$) by solving the Eq. (5.18) for $V = V_{\rm s}$ and then at the tunneling barrier on the drain side ($Q_{\rm b,d}$) for $V = V_{\rm s} - \Delta V$. Then the total mobile charge in ambipolar–state is obtained by:

$$Q_{\rm ambi} = \frac{Q'_{\rm j,s}+Q'_{\rm b,d}}{2}w_{\rm ch}(l_{\rm ch}-X_{\rm b,d}). \tag{5.20}$$

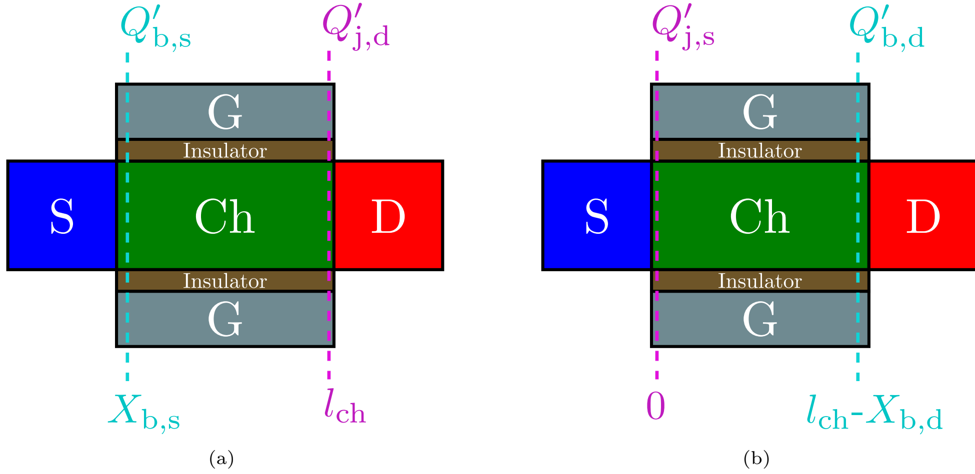


Figure 5.2: The location of the junction and tunneling barrier in the (a) on–state and the (b) ambipolar–state.

In all these aforementioned calculations ΔV refers to the voltage drop in the channel. Analysis of long channel TFETs brought us to the conclusion that the effect of voltage drop in the channel needs to be taken into account. Therefore, firstly by means of an empirical method

the channel charge is calculated by:

$$Q'_{\mathrm{ch}} = Q'_{\mathrm{j,s}} + Q'_{\mathrm{j,d}} + Q'_{\mathrm{i,o}}, \tag{5.21}$$

in which and $Q'_{\mathrm{i,o}}$ ensures a lower limit for the conductivity in the off–state of the device. Next, the resistivity of the channel between the tunneling barrier and the junction is given as:

$$R_{\mathrm{ch}} = \frac{l_{\mathrm{ch}} - X_{\mathrm{b,s}}}{\mu_{\mathrm{n}} Q'_{\mathrm{ch}} w_{\mathrm{ch}}} \tag{5.22}$$

where μ_{n} is the electron mobility. Then, by means of R_{ch} and I_{ds} which are calculated using the TFET DC compact model introduced in [35], the voltage drop is achieved as follows:

$$\Delta V = R_{\mathrm{ch}} I_{\mathrm{ds}}. \tag{5.23}$$

As it is mentioned in 4.6, in this thesis the focus lays on calculation of the $C_{\mathrm{gs}}, C_{\mathrm{gd}}$ and C_{gg}. So, considering the changes in total mobile charge regarding the change in source or drain voltage, the intrinsic capacitances of TFET in on–state are given as:

$$\begin{cases} C_{\mathrm{gs}} = \frac{dQ_{\mathrm{on}}}{dV_{\mathrm{s}}}|_{V_{\mathrm{d}},V_{\mathrm{gs}}} \\ C_{\mathrm{gd}} = \frac{dQ_{\mathrm{on}}}{dV_{\mathrm{d}}}|_{V_{\mathrm{s}},V_{\mathrm{gs}}} \end{cases} \tag{5.24}$$

and in ambipolar–state

$$\begin{cases} C_{\mathrm{gs}} = \frac{dQ_{\mathrm{ambi}}}{dV_{\mathrm{s}}}|_{V_{\mathrm{d}},V_{\mathrm{gs}}} \\ C_{\mathrm{gd}} = \frac{dQ_{\mathrm{ambi}}}{dV_{\mathrm{d}}}|_{V_{\mathrm{s}},V_{\mathrm{gs}}} \end{cases} \tag{5.25}$$

and C_{gg} results from the summation of C_{gs} and C_{gd}. Taking into account the symmetrical geometry of the DG TFET and the fact that in this transistors capacitances associated with each gate are in parallel, the capacitances which are calculated hereby indeed characterize the sum of two capacitances. Therefore, in order to adjust the model for the single–gate case, the calculated capacitances from the model need to be halved.

5.3 Effect of Parasitic Elements on Capacitances

Comparing the intrinsic capacitance models in Sec. 5.2 to measurement data shows that beside the effect of the voltage drop in the channel there are other parasitic effects existing which need to be considered. Hence, the influence of the parasitic resistances are included in the model. It is assumed that there are series resistances at source and drain terminal of the TFET which

affect the C_{gs} and C_{gd} as follows [73]:

$$C'_{\mathrm{gs}} = C_{\mathrm{gs}} - (g_{\mathrm{ds}} + g_{\mathrm{m}}) \cdot (C_{\mathrm{gs}} R_{\mathrm{s}} - C_{\mathrm{gd}} R_{\mathrm{d}}) \tag{5.26}$$

and

$$C'_{\mathrm{gd}} = C_{\mathrm{gd}} + g_{\mathrm{ds}} \cdot (C_{\mathrm{gs}} R_{\mathrm{s}} - C_{\mathrm{gd}} R_{\mathrm{d}}). \tag{5.27}$$

Where C'_{gs} and C'_{gd} refer to the capacitances including the effect of parasitic resistances. R_{s} and R_{d} are the associated series resistances with the source and drain respectively. g_{ds} represents the output conductance and g_{m} is the transconductance which are given as:

$$g_{\mathrm{ds}} = \frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{ds}}} \tag{5.28}$$

and

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{gs}}}. \tag{5.29}$$

g_{ds} shows the ratio of the change in drain current to the V_{ds} changes for constant V_{gs} and g_{m} represents the variation in drain current with varying V_{gs} and a constant V_{ds} [74]. These parameters are calculated with the help of the TFET compact DC model developed in [35].

Furthermore, analyzing the measured capacitances of a fabricated planar device presented in [75] shed light on the fact that the small signal conductance of the Schottky contacts can also influence the behavior of the intrinsic capacitances.

When in the structure of a TFET, a metal with mid–gap work function with respect to the semiconductor material is used as the contact material, an ohmic contact is expected due to the high doping concentration of the semiconductor at source and drain (see Fig. 5.3). Nevertheless, usually in a TFET structure to suppress the ambipolar current the doping concentration of the drain is reduced. As the result, the small signal conductance of this Schottky contact at the drain side becomes smaller and comparable with the g_{ds} and g_{m}. This means that the small signal conductance of the Schottky contact, which is in the same order of magnitude as the output and transfer conductance, can also influence the capacitances. In this regard an empirical method is implemented here to show the effect of Schottky contacts on intrinsic TFET capacitances.

In the on–state it is assumed that $C_{\mathrm{gd}} >> C_{\mathrm{gs}}$ and drain has the main impact on the channel charge. Hence, it is expected that only the small signal conductance associated with the drain Schottky contact (g_{d}), which is depicted in Fig. 5.3, affect the capacitances as follows:

$$C'_{\mathrm{gs}} = C_{\mathrm{gs}} + C_{\mathrm{gd}} \cdot \frac{g_{\mathrm{m}}}{g_{\mathrm{d}}} \tag{5.30}$$

$$C'_{\mathrm{gd}} = C_{\mathrm{gd}} - C_{\mathrm{gd}} \cdot \frac{g_{\mathrm{ds}}}{g_{\mathrm{d}}}. \tag{5.31}$$

In ambipolar–state it is assumed that $C_{\mathrm{gs}} >> C_{\mathrm{gd}}$ and the source controls the channel charge. Therefore, it is considered that the small signal conductance of the source (g_{s}) affect the capacitances. So, the intrinsic capacitances in ambipolar–state are defined as:

$$C'_{\mathrm{gs}} = C_{\mathrm{gs}} - C_{\mathrm{gs}} \frac{g_{\mathrm{ds}}}{g_{\mathrm{s}}} \tag{5.32}$$

$$C'_{\mathrm{gd}} = C_{\mathrm{gd}} + C_{\mathrm{gs}} \frac{g_{\mathrm{m}}}{g_{\mathrm{s}}}. \tag{5.33}$$

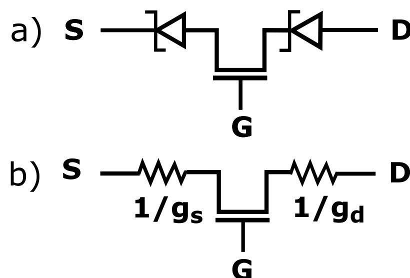


Figure 5.3: Illustration of Schottky barriers at the source and drain of an n–type TFET. (a) To take into account the effect of the Schottky barrier, a Schottky diode is considered at each terminal. (b) The small signal conductance of the diodes are depicted [76].

Both g_{s} and g_{d} are fitting parameters. In order to find a realistic range to estimate their values, first some simulations for Schottky diodes are performed in TCAD. Afterwards, by comparing the diode current with the I_{ds} of the device under investigation, it is considered which Schottky diode with which amount of doping concentration can better characterize the Schottky contact at the barrier of the TFET. Then, the conductance of the chosen diode is calculated and used as the reference to estimate the value of g_{s} and g_{d}. In the following chapter it is shown with more details how the values for these fitting parameters are picked.

CHAPTER 6

Model Verification

In order to inspect the validity of the compact capacitance model, firstly in Sec. 6.1 the results of the compact model are compared to the simulation outputs which are executed in TCAD Sentaurus [24]. Afterwards, in Sec. 6.2 the model is validated by measurement data of fabricated transistors. In Sec. 6.2.1 the model is tailored to a single–gate (SG) p–type device and its results are compared to the measured data of a fabricated planar TFET. In this part the deviation of the model from the measurements is discussed and a theory to explain and compensate this difference is offered. According to this theory, the parasitic effect of Schottky barrier contacts can strongly affect the TFET capacitances. In order to investigate this theory, it is applied on the TCAD simulation results of an n–type device to check if they show the similar pattern as in measurements. In Sec. 6.2.2 the compact model is employed to characterize the intrinsic capacitances of a Nanowire (NW) and the obtained capacitances are compared to the measured capacitances of this device.

6.1 Model Verification by Comparison with TCAD Simulations

For the model verification a 2D DG n–type TFET is simulated in TCAD Sentaurus (see Fig. 4.3(a)). In these simulations a non–local tunneling model for the B2B tunneling current is implemented. To take into account the effect of the TAT current on simulations the *Hurks* model is used. Moreover, to estimate the band gap narrowing (BGN) in highly p–doped regions the *Slotboom* model and in highly n–doped regions the *Del Alamo* model are employed [77, 78]. Considering the BNG in both source and drain affects the on–current and ambipolar–current, respectively.

The B2B tunneling current in the on–state at the source side is calculated with the electron mobility $\mu_n = 1417$ cm^2/Vs, electron tunneling mobility $\mu_{\mathrm{tun,n}} = 3.44$ cm^2/Vs, the effective density of states in valance band $N_{\mathrm{v}} = 2.65 \cdot 10^{19}$ cm^{-3} and the effective electron mass $m_{\mathrm{n}} = 0.25 \cdot m_0$. To obtain the B2B tunneling current in the ambipolar–state at the drain side, the hole mobility is set to $\mu_p = 470$ cm^2/Vs, tunneling mobility for holes $\mu_{\mathrm{tun,p}} = 3.2$ cm^2/Vs,

the effective density of states in conduction band $N_c = 2.8 \cdot 10^{19}$ cm^{-3} and the effective hole mass $m_p = 0.25 \cdot m_0$.

Table 6.1: The parameters used for the TCAD simulations of the short–channel DG n–type TFET.

Parameter	Value	Parameter	Value
l_{ch}	22-90 nm	w_{ch}	1 μm
t_{ch}	10 nm	N_s, N_d	10^{20} cm^{-3}
t_{ox}	2 nm	Ox. Mat	HfO_2
l_{sd}	10 nm	Dev. Mat	Silicon

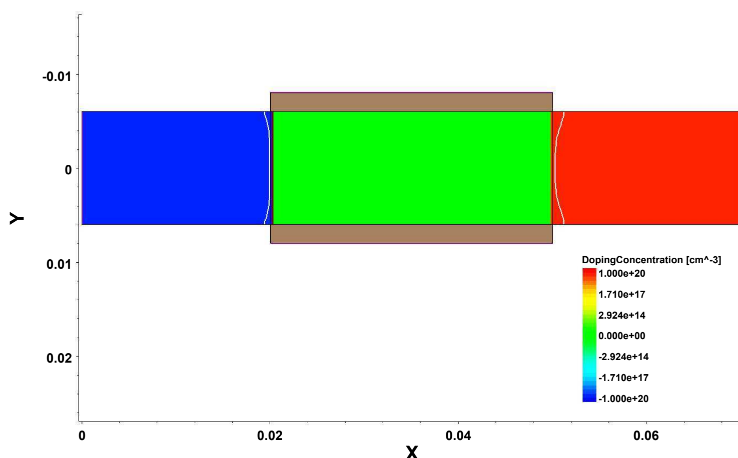


Figure 6.1: The n–type DG TFET structure used for 2D TCAD simulations. Source is doped with a Boron concentration of $N_s = 10^{20}$ cm^{-3} and drain with Phosphorus concentration of $N_d = 10^{20}$ cm^{-3}.

To examine the scalability of the compact model, the drain bias and channel length of the device are varied. The 2D structure used for the TCAD simulation is presented in Fig. 6.1 and the variables and parameters are listed in Table 6.1.

Figure 6.2 depicts the C_{gg} as the function of the gate voltage for varying V_{ds}. The blue solid lines show the results of the model and the dashed black lines are the data resulted from TCAD simulations. Considering the simulated device is an n–type TFET, it is apparent that for $V_{gs} > 0$ and $V_{ds} > 0$ the transistor is in its on–state and for $V_{gs} < 0$ the device is in ambipolar–state. It can be seen that by increasing the drain voltage in on–state, the C_{gg} decreases or namely shifts. The reason for this is that increasing the V_{ds} shifts the Fermi potential in the channel and decreases the charge distribution to the drain, thus the device's intrinsic capacitance is reduced.

In Fig. 6.3 the capacitances C_{gs} and C_{gd} are illustrated against V_{gs} at the constant drain bias ($V_{ds} = 0.5$ V) for varying l_{ch}. When the TFET has a longer l_{ch}, there are more charges

existing in its channel. For this reason, the longer l_{ch}, the greater the intrinsic capacitances are. In this figure the results obtained from model are compared to those from TCAD simulations. It can be seen that the model is in a good agreement with the TCAD simulations.

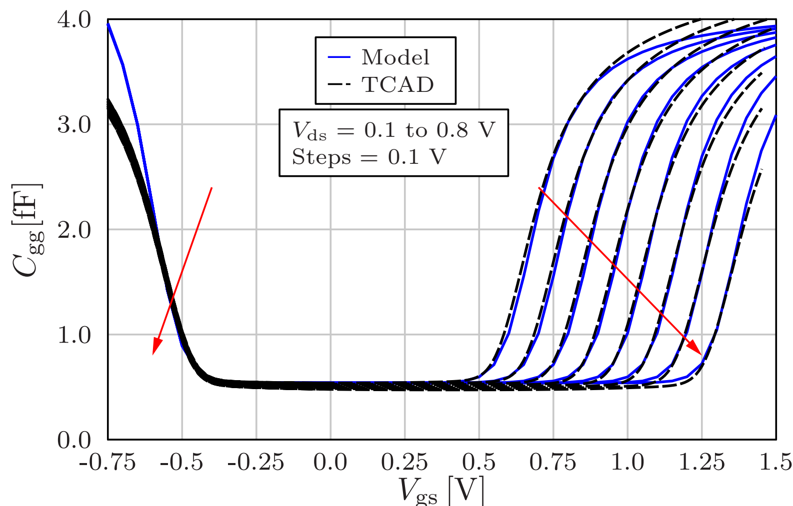


Figure 6.2: C_{gg} of an n–type DG TFET with l_{ch} = 22 nm are compared with the TCAD results for various drain voltages. The fitting parameters of the model are set as $\alpha = 1.62$, $X_{b,s/d} = 3$ nm, $V_{0,gs} = -0.19$ V, $V_{0,gd} = -0.22$ V.

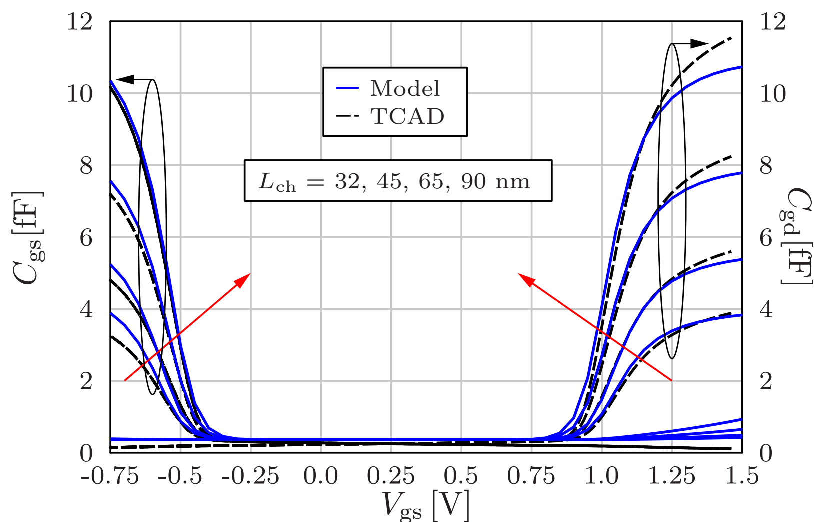


Figure 6.3: C_{gs} and C_{gd} of an n–type DG TFET are obtained by the compact model and compared with TCAD simulations for various channel lengths at V_{ds} = 0.5 V. The fitting parameters are defined as $\alpha = 1.53...1.61$, $X_{b,s/d} = 3$ nm, $V_{0,gs} = -0.19$ V, $V_{0,gd} = -0.22$ V.

6.2 Model Verification by Comparison with Measurements

After verifying the intrinsic capacitance model by results of TCAD simulations, to examine the scalability and flexibility of the model, it is applied to calculate the intrinsic capacitances of other structures including a long–channel p–type SG planar TFET and a NW TFET. In each case the results are compared with the measured data, so that the accuracy of the compact model is also investigated.

6.2.1 Planar TFET

The geometry of the planar TFET, which is produced in the Forschungszentrum Juelich, is depicted in Fig. 6.4. This device is fabricated on a SOI substrates and the $l_{\mathrm{ch}} = 11\,\mu\mathrm{m}$, which means it is a long–channel device. Its gate oxide consists of a thin interface layer of SiO_2 together with 5 nm HfO_2 and on top of it a layer of TiN is deposited as the gate contact.

The tunneling junctions which are formed in Si by ion implantation followed by high temperature annealing, lead to an extensive junction and consequently a low tunneling efficiency. Studies have shown that with the help of low energy ion implantation and low temperature annealing process, an abrupt doping profile and therefore a sharp tunneling junction can be formed [79]. Hence, in the structure of the fabricated planar TFET, first, a layer of $NiSi_2$ is deposited on the surface of the Si to form the source and the drain contacts. Afterward, the Phosphor ions are implanted into the source region of this structure with an energy of 3 keV, a dose of $2 \times 10^{15}\,\mathrm{cm}^{-2}$ and an angle of 45°. In the drain region the Boron ions are implanted with 1.5 keV, a dose of $1 \times 10^{15}\,\mathrm{cm}^{-2}$ and an angle of 135° [75, 76].

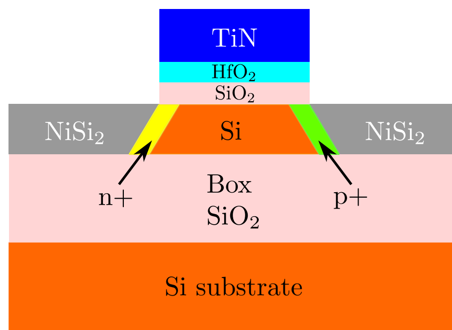


Figure 6.4: Geometry of the fabricated p–type SG planar TFET. The dimensions of the device are as following: $l_{\mathrm{ch}} = 11\,\mu\mathrm{m}$, $t_{\mathrm{ch}} = 10\,\mathrm{nm}$, $t_{\mathrm{ox}} = 5\,\mathrm{nm}$ and $w_{\mathrm{ch}} = 10\,\mu\mathrm{m}$ [75].

In Fig. 6.5 the measured capacitances of the planar structure for different V_{ds} and as a function of V_{gs} are depicted. Since the TFET is p–type for $V_{\mathrm{gs}} < 0$ it is in the on–state and for $V_{\mathrm{gs}} > 0$ it in the ambipolar–state. The increase in V_{ds} shifts the capacitance curves, which meets the expectations. As it is mentioned in Sec. 6.1, this effect occurs due to the charge distribution to the drain. Considering the simulated capacitances of an n-type device, it was

expected that C_{gd} would also be the dominant capacitance for the p-type case in the on-state. But the measured capacitances show an unexpected pattern. It can be seen that in the on–state not only the C_{gd} increases, but also the C_{gs} starts to grow. This effect can be seen in the ambipolar state as well, but on a lower magnitude. This means that in this case, in addition to C_{gs}, C_{gd} is also increased, however this increment is not as big as the one for on-state. Furthermore, in Fig. 6.5 it can be seen that as the negative gate bias grows, C_{gs} gets higher and after that V_{gs} reaches a specific amount, it starts to decrease.

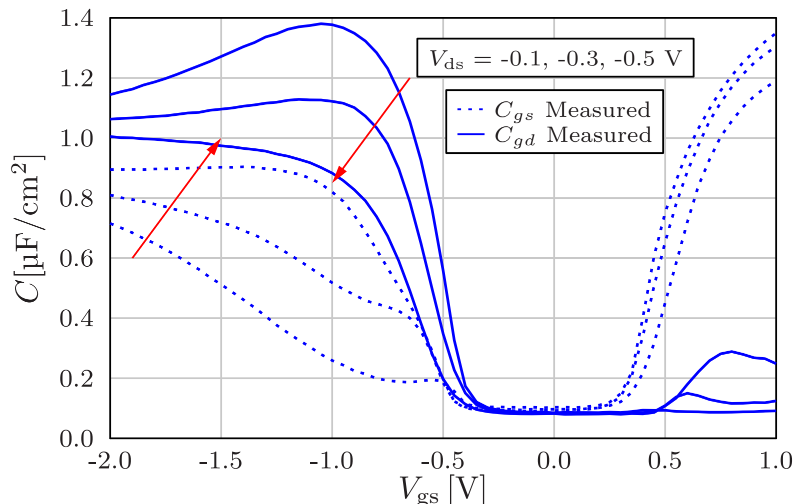


Figure 6.5: The intrinsic capacitances C_{gs} and C_{gd} of the fabricated p–type planar TFET are measured by varying V_{gs} at different V_{ds} [76].

In order to justify this unexpected pattern appearing in measurements, some investigations are carried out to check whether the inclusion of parasitic effects, which do not add complexity to the model and yet make physical sense, compensates this effect in the model.

The very first guess was that due to the long channel of the device the voltage in the channel drops drastically and leads to a change in the charge distribution to the source and drain. To be more specific, regarding the assumption that in TFET the tunneling barrier is the bottleneck for the current, the charge carriers in the on–state from the point that they are injected into the channel are supposedly attributed to the drain. In the case of the long–channel, it is suspected that this charge propagation cannot be employed. It seems that channel charges in on–state, are not only distributed to the drain, rather to both source and drain.

For the purpose of examining this hypothesis, in the compact model the channel voltage drop was multiplied by a constant. As a result of the multiplication of ΔV, C_{gs} was increased in the on-state and with this increase C_{gd} started to decrease. In addition, in the ambipolar–state, C_{gd} began to increase while C_{gs} began to decrease. However, the pattern of the aforementioned changes in the behavior of the capacitances was still different from measurements data.

Studying the small signal analysis of standard MOSFETs has shown that the parasitic resistances at the source and drain contacts affect the intrinsic capacitances. In [73] to address this effect on the MOSFET capacitance in a compact dynamic model, a simple method is introduced. Hence, the next presumption was that by transferring this method to the TFET model, it would probably get closer to the measured data. The effect of parasitic resistances is implemented into the model as it is explained in Sec. 5.3. This method has helped to improve the model, however there are still some deviations from measurements. So, it has brought us to investigating the effect of Schottky barrier contact on intrinsic capacitances.

In spite of that $NiSi_2$ has a mid–gap work function with reference to silicon, at the interface of these two materials an Ohmic contact is expected. That is to say, considering the fact that the source and drain regions in the TFET are highly doped, it is assumed that the charge carriers simply tunnel through the Schottky barrier, because the tunneling length is very low due to the high band bending. But as it is addressed in Sec 5.3, the reduced drain doping concentration leads to a lower small signal conductance at the drain side and affects the intrinsic capacitances. In order to include the impact of the Schottky barrier contact into the model, an empirical approach is developed. To see how this method is implemented in the compact model, it is asked to refer to the Sec. 5.3.

It should be noted that for the purpose of assessing all these hypotheses, they are also implemented and simulated in TCAD Sentaurus [24], ATLAS [25] and Minimos–NT [26]. However, these simulations can not genuinely reproduce the behavior of the measured capacitances. The TCAD simulations considering two Schottky barriers at source and drain show a deficient convergence. Nevertheless, they show results that indicated a tendency, but are not in complete agreement with the expectations [76].

To overcome the convergence problem and estimating the g_d and g_s, which regarding the Eq. (5.30) to Eq. (5.33) are required, firstly some Schottky diodes with different semiconductor doping concentrations are simulated in TCAD. In these simulation Boron is used as the doping material. The current and the small signal conductance of these diodes at a low bias are illustrated in Fig. 6.6. In Fig. 6.7 the compact DC model [35] is fitted to the measured I_ds of the planar TFET. A comparison of these two plots shows that for Schottky diodes with a drain doping concentration lower than $1 \times 10^{19}\,\mathrm{cm}^{-3}$, the current is in the same range as I_ds in the fabricated TFET. Considering the case in which the drain doping is equal to $1 \times 10^{19}\,\mathrm{cm}^{-3}$, the small signal conductance of the Schottky barrier contact at a voltage of $0\,\mathrm{V}$ is almost $5 \times 10^{-5}\,\mathrm{S}/\mu\mathrm{m}$. To put it in another way, these simulations show the range of the small signal resistance of the Schottky barrier and help to make a more realistic estimate of the value of g_d and g_s.

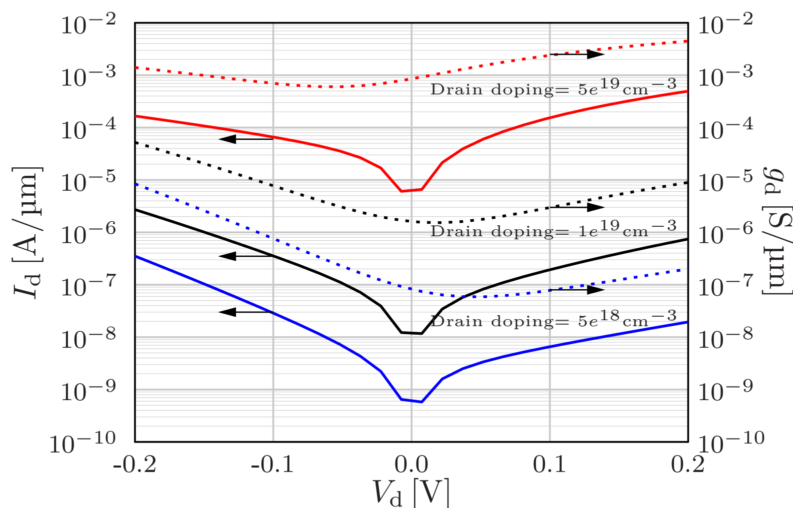


Figure 6.6: Schottky diodes are simulated in TCAD to estimate the small signal conductance of the Schottky barrier contacts at the source and drain of the TFET. In each case the semiconductor part of the diode is doped with different concentrations of Boron. Solid lines depict the diode current and the dotted lines show the small signal conductance of the diodes [76].

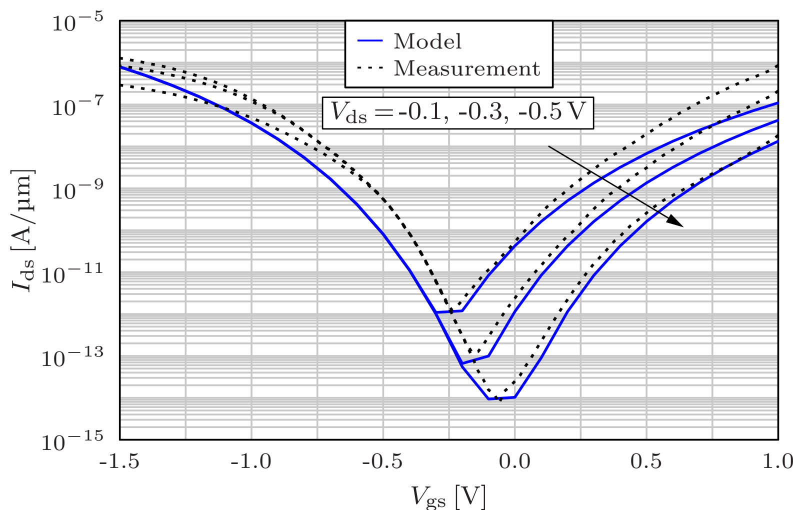
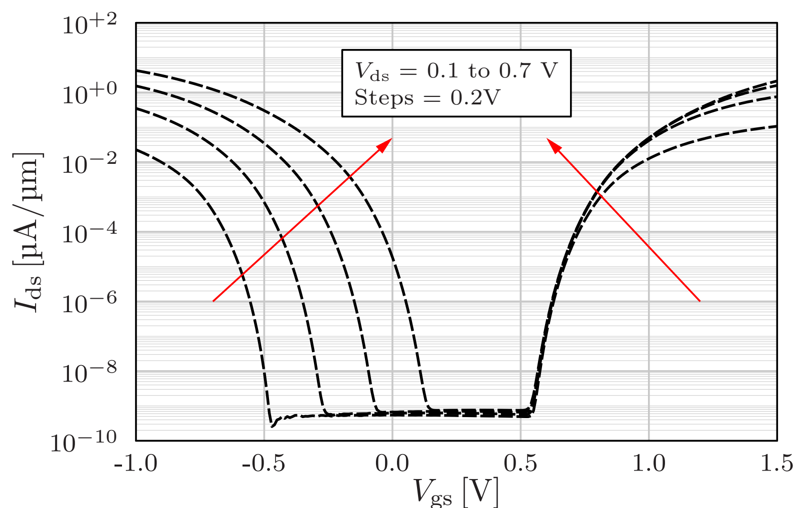
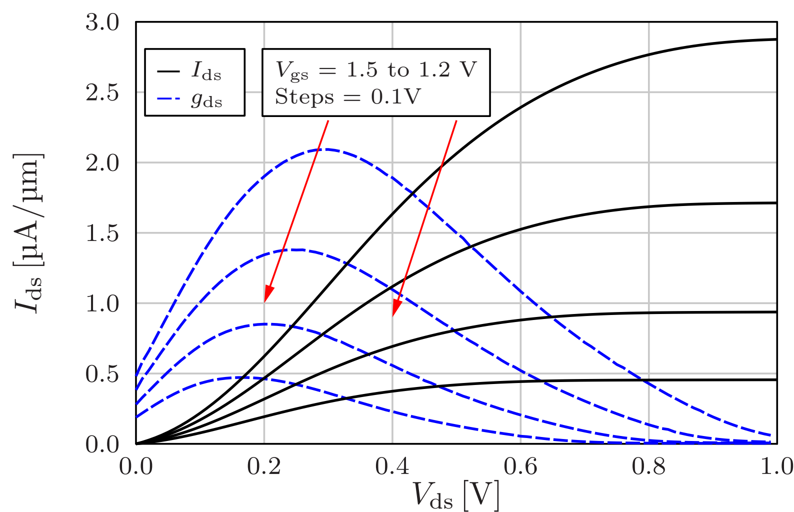


Figure 6.7: The compact DC model [35] is fitted to the measured drain current in the p–type single–gate planar TFET.

To monitor the effect of this theory on the simulated intrinsic capacitance, it is decided to simulate a TFET in TCAD to extract both DC and AC results and then with the help of the compact model apply the Schottky barrier effect on those results. To do so, firstly the transfer and output characteristics of an n–type short–channel device are simulated in TCAD (see Fig. 6.8). The structure of the simulated TFET is equal to the one shown in Fig. 6.1 with $l_{\mathrm{ch}} = 22\,\mathrm{nm}$ and the other parameters are considered to be the same as what is listed in Tab. 6.1. From these simulations g_{ds} and g_{m} as well as intrinsic capacitances are obtained. In Fig. 6.8(b) in addition to the I_{ds} also g_{ds} as a function of V_{ds} for various V_{gs} is depicted. It can be seen that g_{ds} by increasing V_{ds}, firstly tends to increase but then it sinks. In Fig. 6.9(a), g_{ds} is shown on the left axis as a function of V_{gs} for different V_{ds}. For the positive gate bias, or in other words, in the on–state, g_{ds} shows a higher value at lower drain biases. On the other hand in the ambipolar–state, at higher V_{ds}, g_{ds} has a greater value. Additionally, on the right axis the ratio between g_{ds} and g_{d} in the on–state and g_{ds} and g_{s} in the ambipolar–state are presented. Based on the results of the simulations which are performed for the Schottky diodes, the small signal conductances are chosen as $g_{\mathrm{d}} = 8.33 \times 10^{-5}\,\mathrm{S}/\mu\mathrm{m}$ and $g_{\mathrm{s}} = 1 \times 10^{-4}\,\mathrm{S}/\mu\mathrm{m}$. As it is already mentioned, these values are just estimated and used as fitting parameters.

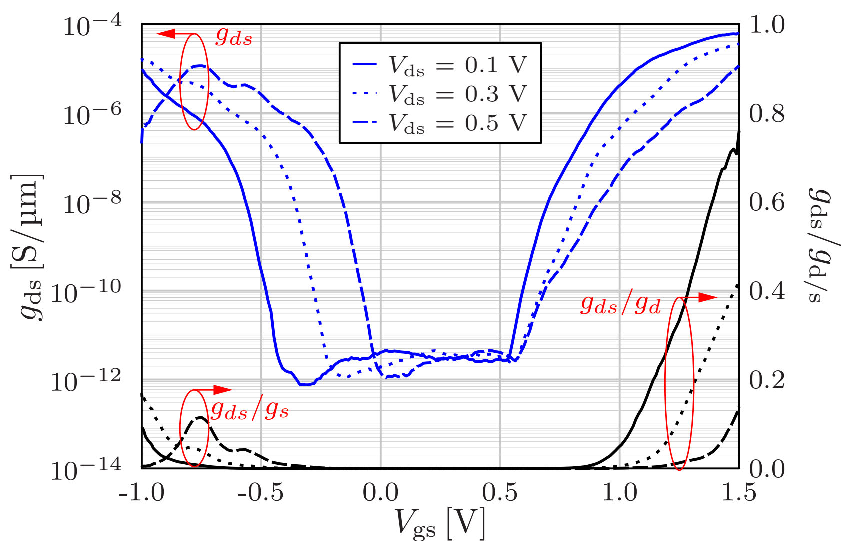


(a)

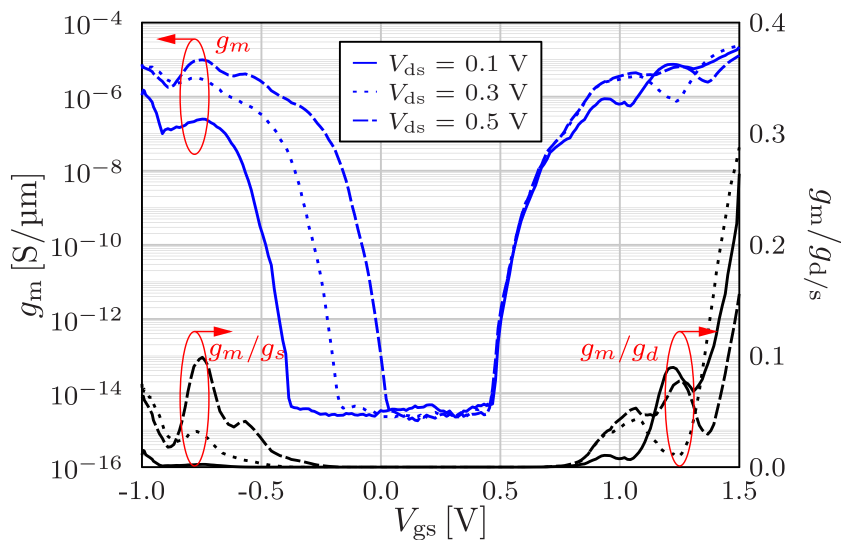


(b)

Figure 6.8: (a) Transfer characteristic of the n–type TFET simulated in TCAD for varying V_{ds}. (b) Output characteristic curves of the n–type TFET simulated in TCAD for various V_{gs} together with their corresponding g_{ds} curves [76]. The geometry of the simulated device is shown in Fig. 6.1. The dimensions of the TFET are set as following: $l_{ch} = 22\,\text{nm}$, $t_{ch} = 10\,\text{nm}$, $t_{ox} = 2\,\text{nm}$ HfO_2.



(a)



(b)

Figure 6.9: (a) The output conductance of a short–channel DG n–type TFET extracted from TCAD simulations. On the right axis g_{ds} is shown, which is normalized in the on–state with respect to g_{d} and in the ambipolar–state with respect to g_{s}. (b) Transconductance of the n–type TFET is extracted from AC analyzes in TCAD. On the right axis the normalized value of g_{m} regarding g_{d} in the on–state and to g_{d} in the ambipolar–state are shown [76].

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Considering all these analyses and according the Eq. (5.31) it is expected that the Schottky barrier in on–state for the lower drain biases has a stronger affect on C_{gd}. Moreover, by taking into account Eq. (5.32) it can be concluded that in the ambipolar–state the small signal resistances of Schottky barrier affect the most C_{gs} when the drain bias is lower.

In Fig. 6.9(b) on the left axis g_{m} against V_{gs} for varying V_{ds} is presented. On the right axis the normalized value $g_{\mathrm{m}}/g_{\mathrm{d}}$ in the on–state and $g_{\mathrm{m}}/g_{\mathrm{s}}$ in the ambipolar–state are shown. In the on–state by varying V_{ds} not a significant change is observed in g_{m}. But in the ambipolar–state it can be seen that for the higher V_{ds}, g_{m} is bigger. Considering the normalized values of g_{m} regarding g_{d} and g_{s} shown on the right axis, it can be said that in the on–state the effect is stronger. However, comparing Fig. 6.9(a) with 6.9(b) it appears that the normalized g_{ds} has a stronger effect on capacitances than the normalized g_{m}.

After analyzing the behavior of g_{ds} and g_{m} in the presence of the small signal conductances of the Schottky barrier contacts, the intrinsic capacitances are finally calculated as explained in section 5.3 of the previous chapter. In Fig. 6.10 the TFET capacitances C'_{gs} and C'_{gd} are presented in comparison to the case where the effect of the Schottky barrier contacts is neglected. The blue solid lines show C'_{gs} and C'_{gd} and the black dotted curves depict C_{gs} and C_{gd}. By incorporating the effect of the Schottky barrier into the TCAD simulation results in the on–state, at a certain gate bias highlighted with a red circle, C'_{gd} starts to fall and C'_{gs} starts to rise. Considering this bias and comparing it to Fig. 6.9, it can be seen that where the $g_{\mathrm{ds}}/g_{\mathrm{d}}$ and $g_{\mathrm{m}}/g_{\mathrm{d}}$ curves begin to rise is actually where the effect of the Schottky barrier contact on capacitances is apparent. The similar pattern can also be observed in the ambipolar–state where C'_{gd} increases and C'_{gs} decreases. It also needs to be pointed out that in the on–state for lower V_{ds} the C'_{gd} is stronger affected than for higher drain bias, which was anticipated by the analyses of the g_{ds}.

Apart from all the aforementioned discussions, there is another point to consider, which is the hump in the measured C_{gd} curves in the ambipolar–state and also in C_{gs} in the on–state. Considering the measurement data of the p–type planner TFET (see Fig. 6.5), at $V_{\mathrm{ds}} = -0.1\,\mathrm{V}$ and for $V_{\mathrm{gs}} = -0.5\,\mathrm{V}$, a sudden growth or a knob can be seen. In [75] it is suggested that this hump is due to the transition from TAT to B2B tunneling. That means, it is assumed that in the planar TFET the TAT occurs first and leads to an increase in C_{gs}. Thereafter, by increasing the gate bias voltage in negative direction, the B2B tunneling also starts and at this point the hump appears in the curve. The higher the drain bias, the less the hump can be seen. The reason for this can be that with the higher drain bias, or more precisely the more negative V_{ds} in this case, this transition occurs faster and therefore it cannot manifests itself. It can be concluded that the behavior of capacitances in TFET is obviously very responsive to the current and all elements such as traps and structure of the transistor which bring about a change in the charge carriers of the channel.

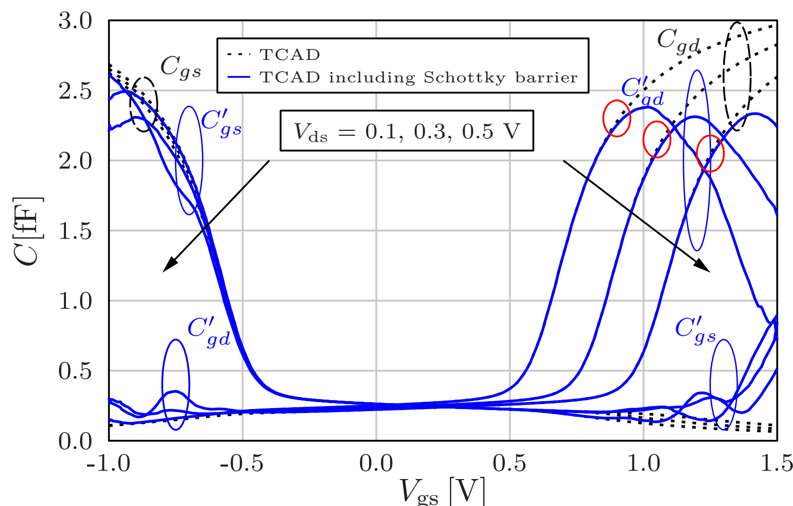

Figure 6.10: The black dotted curves represent the intrinsic capacitances of the n–type DG TFET simulated in TCAD. The blue curves illustrate the capacitances which are recalculated by including the effect of the Schottky barrier contacts effect. The red circles indicate the gate voltage at which the impact of the Schottky barrier shows itself on each curve [76].

6.2.2 NW TFET

The NW TFET are reported to have a higher I_{on}, subthreshold swing below 60 mV/dec and better performance in comparison to the planar structure [80–82]. It is therefore important to check whether the compact model is also suitable for this device and can represent such a TFET.

The geometry of the vertical gate–all–around n–type Si NW TFET, that is investigated here, is illustrated in Fig. 6.11(a) and its geometrical parameters are listed in Tab. 6.2. This device is fabricated by Interuniversity Microelectronics Center (imec) Belgium. The Si substrate on which the NW is grown is heavily doped with arsenic, the channel consists of lightly n–doped Si and the source region of highly Boron–doped Si. Considering the cross section of this TFET depicted in Fig. 6.11(b), it can be seen that the gate overlaps the source area. According to the results reported in [83], increasing the gate–source overlap enhances the on–current of the NW TFET which is due to the control of the gate over the tunneling at the source side.

Another point of attention in this structure is the thick layer of oxide around the channel and the drain region. The purpose of implementation of this layer of oxide is to reduce the gate leakage and also suppressing the ambipolarity. This layer isolates the gate from substrate, hence, it results in a lower gate leakage as well as the gate–substrate capacitance [83]. Furthermore, due to the gate underlap region at the drain side, the tunneling on this side and consequently the ambipolar–current is suppressed. Further information about the steps and details of the fabrication process are given in [83].

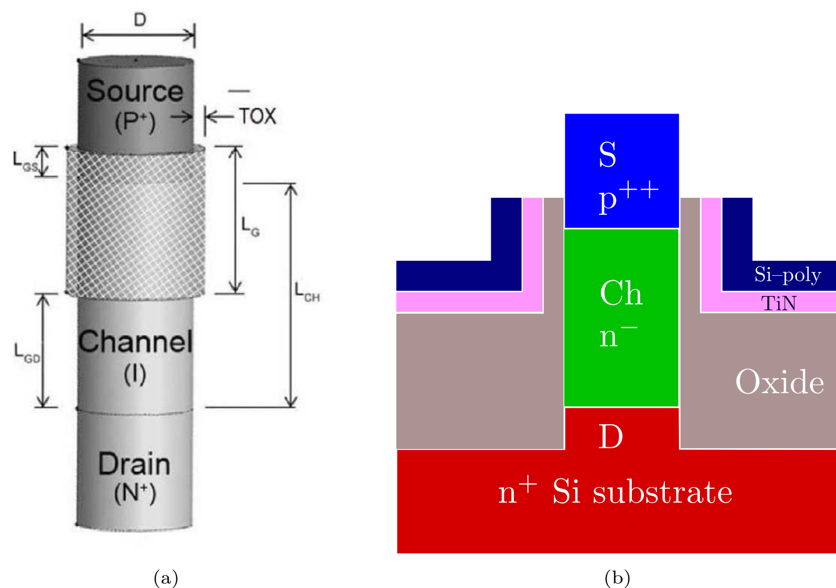

Figure 6.11: (a) The schematic of the fabricated n–type Si NW TFET and (b) its cross section [83, 84].

Table 6.2: The structural parameters of the n–type Si NW TFET.

Parameter	Value	Parameter	Value
L_{CH}	220 nm	L_{G}	150 nm
L_{GS}	30 nm	L_{GD}	100 nm
D	200 nm	N_{CH}	10^{15} cm^{-3}
N_{s}	10^{20} cm^{-3}	N_{d}	10^{19} cm^{-3}
T_{OX}	4 nm	OX. Mat	1 nm SiO_2 + 3 nm HfO_2

The measurement data associated with the NW TFET depicted in Fig. 6.11 are provided by LSI/PSI/USP, University of Sao Paulo, Brazil and are partially presented in [84, 85]. The transfer characteristic curves are obtained doing the measurements for a device with 400 parallel NW TFETs at room temperature [84]. The capacitance measurements are carried out for a device with 4050 NW TFETs connected in parallel at a frequency of 10 kHz, at room temperature, $V_{\mathrm{ds}} = 0\,\mathrm{V}$ and grounded source terminal [85].

Taking into account the fact that the model is originally designed for a DG TFET, and considering the cylindrical shape of the NW and its gate–source overlap, the compact model must first be tailored to this structure in terms of the geometrical parameters of the device and fitting factors. The fitting parameters need to be chosen appropriately so that the model shows a good agreement with the measured data, whereby these parameters should be reasonable and physically justifiable. In this regard, the equivalent geometric parameters are implemented in

the compact model to achieve a perfect match with the measurements.

In the compact model the equivalent oxide thickness (EOT) is assigned to t_{ox}. This value shows, if instead of the material with larger dielectric constant (κ) such as HfO_2, SiO_2 is used, how thick this layer is supposed to be to achieve a similar performance. The EOT is given as [11, 86]:

$$EOT = t_{\text{hk}} \cdot \frac{\kappa_{\text{SiO}_2}}{\kappa_{hk}}, \tag{6.1}$$

where t_{hk} is the thickness of the oxide with high permittivity, κ_{SiO_2} is the dielectric constant of SiO_2 and κ_{hk} characterizes the dielectric constant of the high-κ oxide. Considering Tab. 6.2, the gate oxide in the NW TFET structure consists of 1 nm SiO_2 and 3 nm HfO_2. Hence, the EOT is calculated as follows:

$$EOT = t_{\text{HfO}_2} \cdot \frac{\kappa_{\text{SiO}_2}}{\kappa_{\text{HfO}_2}} + t_{\text{SiO}_2}, \tag{6.2}$$

where $\kappa_{\text{HfO}_2} = 25$ and $\kappa_{\text{SiO}_2} = 3.9$. So, the calculated EOT for this structure device is equal to 1.4 nm.

According to the definition of the channel length in the TFET compact model, it is assumed that l_{ch} of the NW TFET is equal to 220 nm (L_{CH} in Fig. 6.11(a)). However, the studies performed on the DG MOSFET compact model show that the equivalent l_{ch} should be larger than the corresponding value in the structure to allow simulations of the gate–all–around MOSFET with the existing DG model [87]. Based on it, here l_{ch} is chosen to be equal to 250 nm. Regarding the other structural parameters in the compact model, both t_{ch} and w_{ch} are considered to be equal to $D = 200$ nm. In order to compensate the effect of the gate–source overlap, a parallel capacitance to C_{eff} is considered in the model which serves for an increment in the maximum value of the intrinsic capacitances. Since the measurements are performed for devices with multiple NW TFETs, the data is in each case divided by the number of NWs and then the compact model is fitted to the data corresponding to a single NW TFET.

After setting all device parameters in the compact model and choosing appropriate fitting parameter, the measured I_{ds} as a function of V_{gs} at three different V_{ds} is compared to the compact model and the results are illustrated in Fig. 6.12. Also the measured C_{gs}, C_{gd} and C_{gg} are compared to those obtained by the compact model. The results are shown in Fig. 6.13. It must be mentioned that here the effect of the Schottky barrier is neglected in the model. However, as it can be seen in both Fig. 6.12 and Fig. 6.13, the model is in a very good agreement with the measurements.

In this step, it has become apparent that the model can properly and effectively describe the behavior of the intrinsic capacitances in a TFET considered as a single component with respect to the simulations and measured data. So, the compact model is then implemented in Verilog–A language to allow circuit simulations. In the next chapter, the steps which are taken to design some simple circuits and to investigate the efficiency of the compact model in terms of circuit simulation, are presented and discussed in detail.

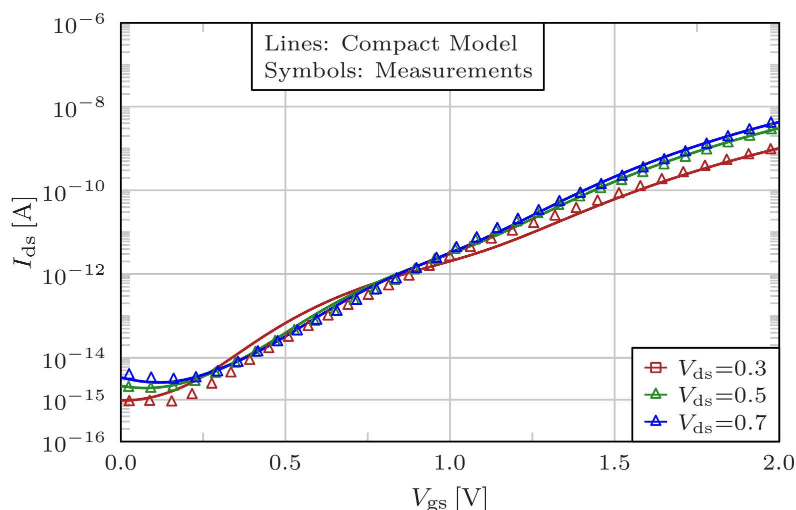

Figure 6.12: The measured I_{ds} of the n–type NW TFET for varying V_{gs} is compared to the results of the compact model at different V_{ds}.

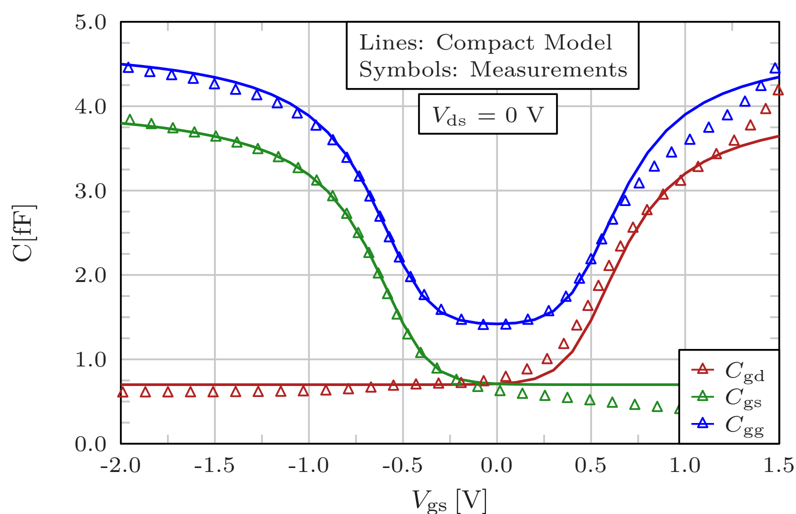

Figure 6.13: The measured capacitances of the n–type NW TFET for varying V_{gs} at V_{ds} = 0 V are compared to the corresponding capacitances obtained by the compact model.

CHAPTER 7

Circuit Simulation

In the following, the model is used to perform circuit simulations. In this regard, the model is firstly implemented in Verilog–A language. Then it is used to design p–type and n–type TFET and by means of them some simple digital circuits, such as inverter and ring–oscillator, are designed. Thereafter, the outputs of these circuits are compared and presented by considering different device parameters.

This chapter is divided into two main parts. In Sec. 7.1 circuit simulations are performed for those circuits which are designed by means of DG TFET and the effect of device parameters on results are studied. The Sec. 7.2 presents the results of simulations in which the circuits are based on SG line tunneling TFETs.

7.1 DG TFET–Based Circuits

It is important to check if the model is robust enough for circuit simulations and also inspect how it responses by varying the device parameters. In this context, after the DC and the intrinsic capacitance models are brought together and linked, some parameters are chosen to be changed and their impact on the static and transient performance of the TFET–based circuits is considered.

The structure which is focused on in this part is a DG TFET with $l_{\mathrm{ch}} = 22\,\mathrm{nm}$ (see Fig. 4.1) and for the sake of the simplicity, the effect of the Schottky barrier contact is neglected in the model. The device parameters which are selected to be examined are the trap density (N_{t}) at the tunneling junction, N_{d} and l_{ch}. Also here the compact model is in the first place compared with the TCAD simulation results of one transistor.

To begin with, the transfer characteristics of the n–type TFET in four cases are compared with corresponding simulations in TCAD Sentaurus in Fig. 7.1. Reducing N_{d} leads to a suppression in ambipolarity and decreasing N_{t} results in lower current in off–state of the device. Considering the first case, which is shown in red, both N_{d} and N_{t} are reduced, it means that the effect of ambipolarity and traps are suppressed. The green curves show the setup in which

only traps are reduced, the blue ones refer to the case that just ambipolarity is suppressed and for the purple curves both effects are remained at their maximum. It can be seen that for all these cases the compact model shows a good agreement with the results obtained from TCAD simulations. The same steps are also taken to validate the compact model in the case of the p–type TFET.

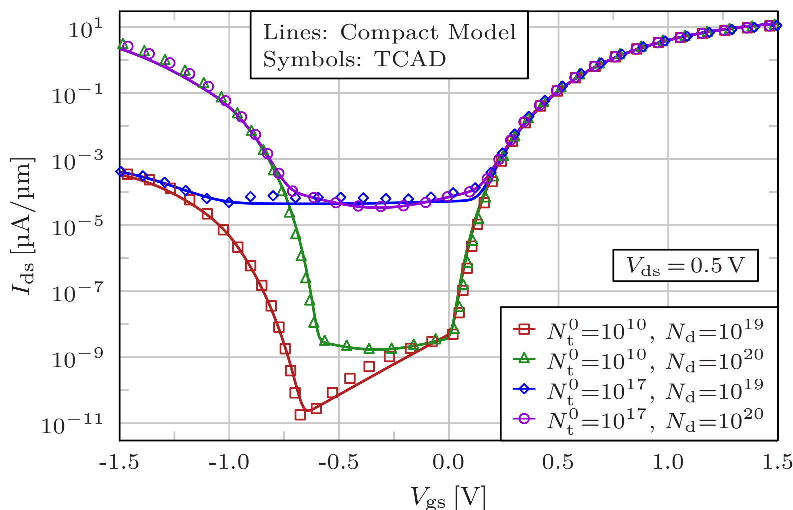

Figure 7.1: Current transfer characteristic of an n–type DG TFET in four different combinations of N_d and N_t. In each case the result of the compact model is compared with TCAD simulation output. The dimensions of the device are defined as following: $l_{ch} = 22$ nm, $t_{ch} = 10$ nm, $t_{ox} = 2$ nm of HfO_2, $w_{ch} = 1\,\mu$m, the source is Boron doped with $N_s = 10^{20}\,cm^{-3}$ and in the drain region Phosphorus with the given doping concentrations is implemented [88].

After verification of the DC model for varying N_t and N_d and for the both n– and p–type transistors, the intrinsic capacitances model is examined in comparison to the TCAD simulations as well. In Fig. 7.2 capacitances of a p–type device are illustrated. For $V_{gs} < 0$ the transistor is in its on–state, hence the mobile charges in the channel cause an increase in C_{gd}. For $V_{gs} > 0$ the p–type TFET is in ambipolar–state and therefore C_{gs} takes over. Considering the green and purple curves in Fig. 7.2 it can be seen that in these setups $N_d = 10^{20}\,cm^{-3}$ but N_t is different. However, the change in N_t has a minimal impact on the C_{gs} and almost no effect on C_{gd}. By comparing these two curves with the red and blue ones, in which $N_d = 10^{19}\,cm^{-3}$ and N_t is equal to $10^{10}\,cm^{-2}$ and $10^{17}\,cm^{-2}$ respectively, it can be said that increasing N_d results into a higher C_{gs}. Generally speaking, in all these four cases the C_{gd} is not significantly affected and C_{gs} is only influenced by the change in the value of N_d. The intrinsic capacitance model, depicted with solid black lines in Fig. 7.2, fulfills the expectations and fits the TCAD simulations.

After calibrating the compact model by means of TCAD simulation for both n–type and p–type devices, it is implemented in the Cadence electronic design automation software [89].

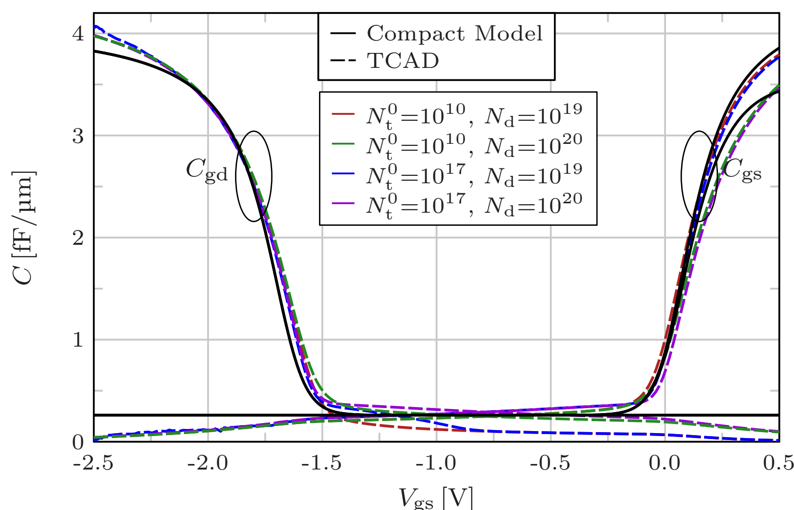

Figure 7.2: The intrinsic capacitances of a p–type DG TFET in four different combinations of N_d and N_t. In each case the result of the compact model is compared with TCAD simulation. The dimensions of the device are defined as following: $l_{ch} = 22\,nm$, $t_{ch} = 10\,nm$, $t_{ox} = 2\,nm$ of HfO_2, $w_{ch} = 1\,\mu m$, the source is Phosphorus doped with $N_s = 10^{20}\,cm^{-3}$ and in the drain region Boron is used as the dopant [88].

Although the aim was focusing on the aforementioned device parameters, in early stages of experimenting with the model it has got apparent that shifting the V_{fb} significantly affects the performance of the TFET–based circuits. In the case that there is no charge existing in the oxide or at the oxide–semiconductor interface, V_{fb} is depending on the work function of the gate metal and the semiconductor. Which means, it is not a fitting parameter and rather supposed to be calculated from band diagram. However, as it is mentioned here the aim is to examine the behavior of the TFET–based circuits considering different device parameters. Hence, after some experiments two main setups are chosen to be used for the simulations, namely the *low–power mode* (LP) and *high–performance mode* (HP). In Fig. 7.3 the tranfer curves of both n– and p–type TFETs in each of these two modes are illustrated. It can be seen that shifting V_{fb} by 50 mV results in a lower I_{ds} for small V_{gs}, which is in fact the reason this mode is called LP. On the other hand, shifting V_{fb} by -200 mV leads to a higher I_{ds}, which means the performance of the transistor for lower V_{gs} is improved and therefore this setup is called HP. Considering Fig. 7.3 it can also be extracted that the maximum slope of the transfer curve in LP mode is around 26 mV/dec, while in the HP mode this value is almost equal to 70 mV/dec. This very moderate slope in HP mode is due to the shift in the V_{fb} and it can be argued that it is far worse than what is expected in the TFET. But it needs to be noted that the main goal of these simulations is to investigate the performance of the circuits for the case in which I_{ds} is higher. Hence, such a trade–off to improve the current, yet by using a simple Si DG TFET structure, would have been inevitable at this point [88]. In the light of these two

setups, an inverter circuit is designed using n– and p–type TFETs in Cadence Virtuoso [89], which is afterwards used to compose a 3–stage ring–oscillator (see Fig. 7.4).

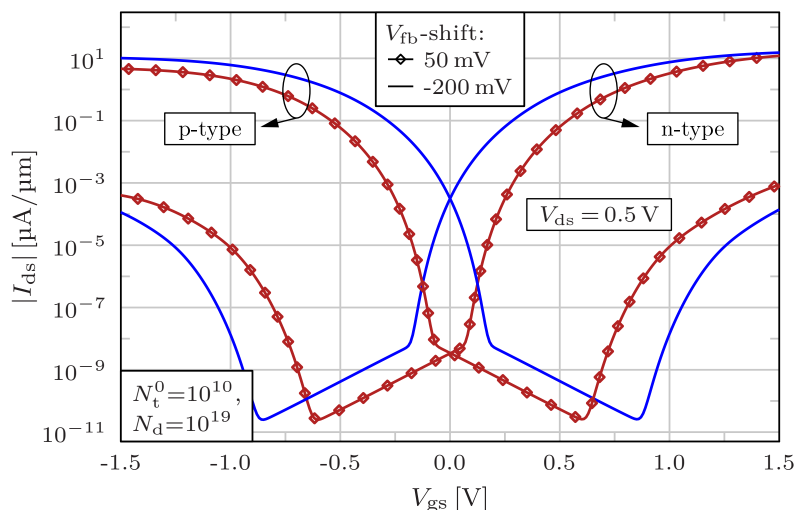

Figure 7.3: Transfer characteristic of the n– and p–type DG TFETs are shown for the LP mode with V_{fb}–shift = 50 mV and HP mode with V_{fb}–shift = -200 mV [88].

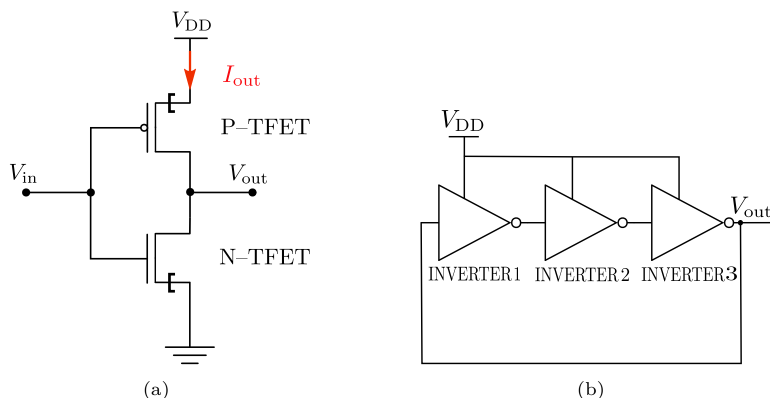

Figure 7.4: (a) Schematic of the TFET–based inverter circuit simulated in Cadence. (b) 3–stage ring–oscillator using the TFET–based inverters. V_{DD} refers to the input voltage, V_{in} is the input voltage of the inverter, V_{out} represents the output voltage and I_{out} refers to the output current [88].

To begin with, it must be specified that the supply voltage of inverters (V_{DD}) (see fig. 7.4), in all following simulations is set to 0.5 V except it is mentioned. In Fig. 7.5(a) the voltage transfer curves (VTC) of TFET–based inverter are shown in HP mode and for three cases regarding the suppression of N_{t} and N_{d}. Furthermore, on the left axis, the output current (I_{out}) which is indicated in Fig. 7.4(a), is illustrated for all these setups. For the input voltage $V_{\mathrm{in}} = 0\,\mathrm{V}$ the p–type TFET is in its on–state. So, it is expected that V_{DD} with a low resistance is connected to the output of the inverter and hence $V_{\mathrm{out}} = 0.5\,\mathrm{V}$. In other words, when the upper transistor, the p–type TFET, is in on–state it can be treated as a low resistance which leads to $V_{\mathrm{out}} = V_{\mathrm{DD}}$. When V_{in} rises, eventually the gate bias of the transistors increases and as a result the n–type TFET begins to switch on and in contrast the p–type device goes off. It can be seen in Fig. 7.5(a) that in the short moment that both transistors are on I_{out} reaches its maximum which is due to the created path between V_{DD} and the ground [88]. Further increment in V_{in} leads to a decrement in the output voltage and finally $V_{\mathrm{out}} = 0\,\mathrm{V}$, which shows the p–type TFET is in the off–state. Considering the changes in N_{t} and N_{d}, it can be seen that all the curves look very similar, which means the traps and ambipolarity do not have a significant influence on the switching behavior of the HP–TFET Inverter.

In Fig. 7.5(b) VTC of the TFET in HP mode is compared with the one in LP mode. Here by contrast, a notable difference between these two setups can be observed. The VTC curve in LP mode has a steeper slope than in HP mode, which means the LP-TFET has a higher gain. Taking the VTC curves into account, the DC gain of the LP–TFET is approximately equal to 14, and in HP mode this value is close to 3.5. In addition, as expected, it can be seen that the HP–TFET has a higher value of I_{out} [88].

Despite the fact that the suppression of the traps and the ambipolarity of the TFET influences its electrical properties, no significant impact on the results of the inverter simulations can be seen. But by considering Fig. 7.5 and looking back at Fig. 7.1, one can see that in the defined range of V_{in} for VTC in both HP and LP mode, neither the effect of TAT on the subthreshold swing nor the effect of ambipolarity suppression is attained. That means, for the applied gate voltage, degradation of the subthreshold swing due to the changes in N_{t} is not manifesting itself and it is also not reached in the ambipolar–state. The current which is dominating in transient simulation is the charging current. So, for example, the effect of N_{t} only becomes visible when the circuit is in a steady state, in which the off–current is influenced by traps [88]. Hence, hereafter the focus is moved to the V_{fb}–shift.

To perform transient simulations for the TFET–based inverter, a rectangular pulse is given as the input of the inverter. In Fig. 7.6 the response of the inverter to the indicated pulse in HP mode is shown in blue and for the LP mode in red. When the input transits from 0 to its high value, the inverter switches off. Before the current tends towards 0, it shows an even higher positive peak during the rise–time of the input pulse and then sinks to reach its low value. While the input drops to its minimum, the output first reaches its negative peak and then rises to its high value. In other words, at the rising edges of the input signal the output shows an overshoot and at the falling edges an undershoot, which is due to the capacitances in

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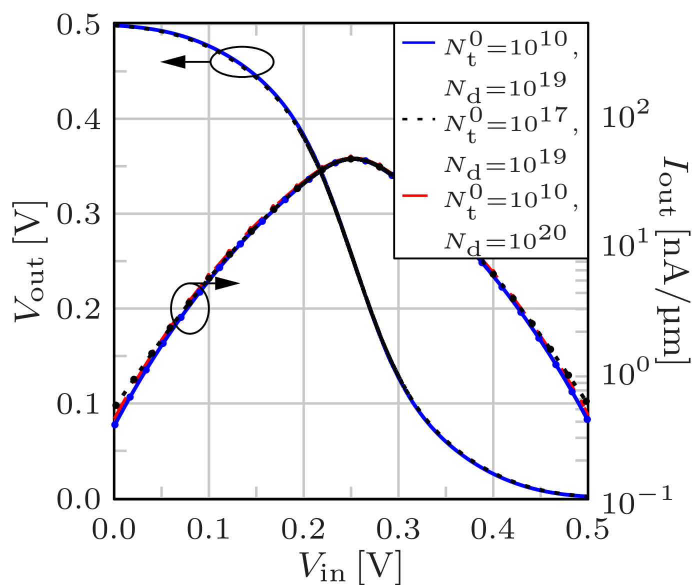
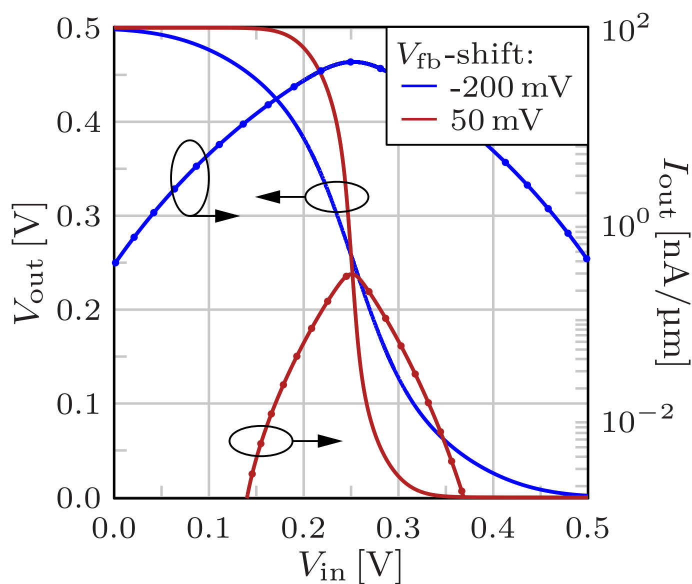
the TFET compact model. Starting from $V_{\mathrm{in}} = 0\,\mathrm{V}$, the p–type TFET is on and the holes are accumulated in the channel. In the moment that it is switching to its high level, the charge carriers in the channel of both transistors proceed as the Miller capacitance. Hence, by further increment in the value of V_{in}, just before that the n–TFET is in on–state, the output signal overshoots and goes beyond V_{DD} [88, 90]. When the n–type TFET is turned on and starts to conduct the current flow, the holes in the channel can move through the n–i–p junction of the p–type TFET which is forward–biased. In this state the negative charge carriers tunnel through the barrier on the source side of the n–type device and accumulate in the channel. As the result, this charging effect reduces the rate at which the output voltage slows down [88].

Considering the HP and LP setups in Fig. 7.6, it can be seen that the overshoot and undershoots have a smaller peak in HP mode, which is due to the fact that in this case the transistors are earlier turned on. In other words, since in HP mode TFETs are supplied by a higher current, the charge carriers get faster accumulated in the channel of the device which is supposed to get on.

At $V_{\mathrm{in}} = 0.5\,\mathrm{V}$, the capacitances in p–type TFET are discharged and the channel of the n–type device is accumulated with electrons. When the input pulse starts to drop, at this moment the n–TFET is forward–biased. Hence, its channel charge carriers get released to the ground and an undershoot in V_{out} appears. Furthermore, in this case holes tunnel through the barrier on the source junction of the p–TFET into its channel and limit the I_{out} as well as the rising time of the V_{out} [88].



(a)



(b)

Figure 7.5: In (a) VTC and current curves of the TFET–based inverter in HP mode for three different cases are presented. In (b) VTC and I_{out} of the HP–TFET inverter with V_{fb}–shift = -200 mV for $N_t = 10^{10}\,cm^{-2}$ and $N_d = 10^{19}\,cm^{-3}$ are compared with those of the LP inverter in which V_{fb}–shift = 50 mV [88].

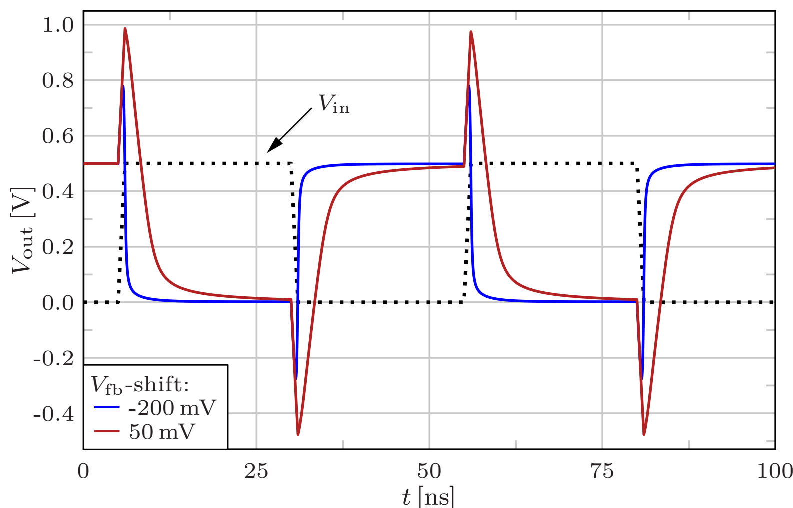


Figure 7.6: The effect of the V_{fb}–shift on the output waveform of the TFET–base inverter is investigated. To perform the transient simulations a trapezoids with very steep edges is considered as the input of the inverter. At the rising edge V_{out} shows a overshoot and at the falling edge it shows an undershoot which is due to the intrinsic capacitances [88].

After analyzing the behavior of the TFET–based inverter, a 3–stage ring–oscillator is simulated. In Fig. 7.7 the output voltage of this oscillator as a function of time is presented. As it is explained in previous paragraphs, it can be said that in HP mode due to a higher on–current charging and discharging of intrinsic capacitances occurs faster than in LP mode. Thus, it is expected that the 3–stage ring–oscillator in HP shows a smaller delay comparing to the LP case and it is exactly what is illustrated in Fig. 7.7 [88].

In order to investigate the effect of the l_{ch}, the ring–oscillator simulations are repeated for different channel lengths of TFETs. With the help of these simulations, first the oscillation periodic represented by T in Fig. 7.7 is calculated and then from this the intrinsic delay of a single inverter (τ) is derived as follows:

$$\tau = \frac{T}{2n}, \tag{7.1}$$

where n refers to the number of stages in the ring–oscillator circuit which in this case is equal to three.

In Fig. 7.8 the calculated τ from ring–oscillator simulations for $l_{ch} = 22, 45, 65, 90, 180$ and 250 nm in HP and LP cases are depicted with symbols. Generally speaking, it can be seen that in HP mode the ring–oscillator shows a smaller delay than in the LP mode and in both setups by increasing l_{ch} also the delay increases. More precisely, for $l_{ch} = 22$ nm the inverter delay in HP mode is equal to 6.7 ns and this value raises to 68 ns for $l_{ch} = 250$ nm. In LP mode these corresponding delay values are 115 ns and 1.2 μs, respectively. Moreover, according to the

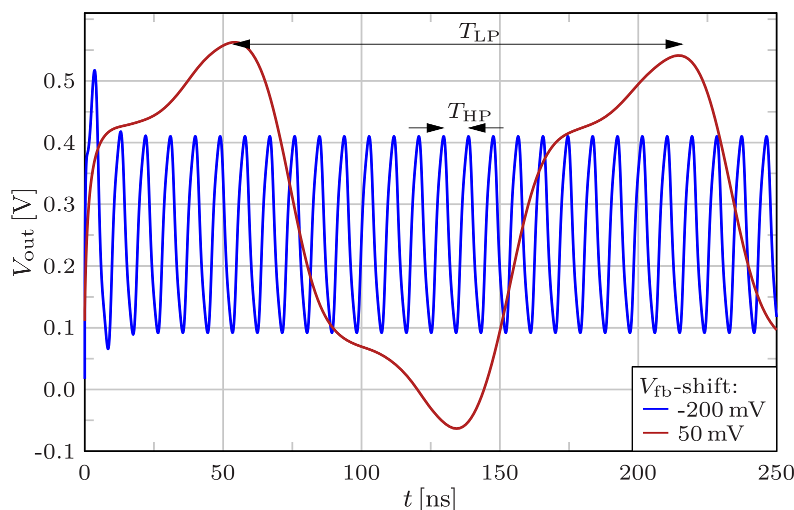


Figure 7.7: V_{out} of the 3–stage ring–oscillator. T_{LP} and T_{HP} refer to the period of the oscillation in LP and HP case, respectively. In LP mode, which is shown in red, the delay is bigger than in the HP mode illustrated in blue. In both setups $V_{DD} = 0.5\,V$ [88].

simulations the average output current of each inverter is remained almost independent from l_{ch}, approximately 55 nA/μm for the HP case and 5 nA/μm for the LP mode. Additionally to the calculated inverter delay from ring–oscillator simulations, it is also estimated based on the following well–known analytical expression:

$$\tau = \frac{C.V}{I} \tag{7.2}$$

In this Eq. it is considered that $C = C'_{ox} w_{ch} l_{ch} + 2C_{ext}$ and C_{ext} refers to the extrinsic capacitance effect on the intrinsic part of the TFETs. The current I is set as a fitting parameter in this case, which is equal to 0.17 μA/μm for the HP mode and 10 nA/μm for the LP mode. In consideration of Fig. 7.3 these values are chosen in a way that they are smaller than the on–current at $|V_{gs}| = 0.5\,V$, which is however not reached in the range that inverters sweep [88].

In the light of Fig. 7.8 one can conclude that the intrinsic delay of a TFET–based inverter is proportional to the l_{ch} of its transistors. It is derived by taking into account the Eq. (7.2) and considering that the capacitances in TFET are a function of l_{ch} but not of the current. In other words, in a TFET the tunneling barriers are the bottleneck for the current, hence varying l_{ch} does not significantly affect the current [35]. For comparison, the corresponding curve of a CMOS inverter in the 32–nm node with $V_{DD} = 0.8\,V$ is also shown here. That is to say, based on the *International Technology Roadmap for Semiconductors* (ITRS) reports [91] the values of on–current and intrinsic inverter delay for the supply voltage of 0.8 V and $l_{ch} = 32$ nm are obtained as: $I_{on} = 1.7\,\mu$A/μm and $\tau = 2.1$ ps. Then, on the basis of these informations and

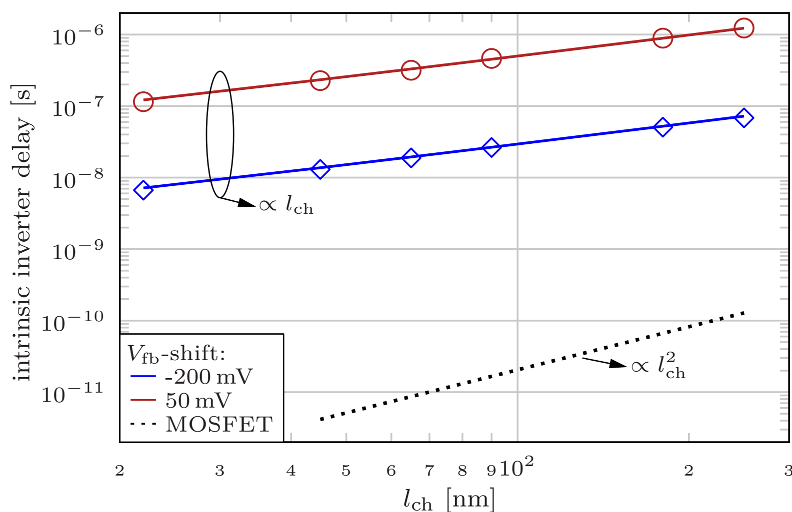


Figure 7.8: Intrinsic inverter delay extracted from simulations of TFET–based ring–oscillator circuit for $l_{ch} = 22, 45, 65, 90, 180$ and 250 nm are shown with symbols. The solid lines represent the theoretical relation between τ and l_{ch}. The dotted line shows the corresponding correlation for the CMOS–inverter [88].

with the help of the Eq. (7.2), first the capacitance and then the CMOS inverter delay for different channel lengths are approximated and depicted in dotted line in Fig. 7.8. Since in a CMOS the current is inversely proportional to l_{ch} and in addition capacitance is directly corresponding to l_{ch}, in this case $\tau \propto l_{ch}^2$ [88].

All in all, these results demonstrate that in order to improve the dynamic performance of TFETs, their on–current must be increased, and the question arises as to how such an improvement can be achieved [76]. Studies have shown that innovative architectures of TFETs, such as those using line tunneling and hetero–structures, increase the potential to achieve a higher I_{on} [92]. Hence, in the following the effect of line–tunneling is implemented in the compact model and inspected.

7.2 SG Line Tunneling TFET–Based Circuits

As it is already explained in Sec. 4.2, line tunneling allows for a larger tunneling region which means the source can provide the channel with more charge carriers and it leads to a higher on–current. Furthermore, since the tunneling region on the drain side stays unchanged as in the point tunneling structure, this concept can additionally reduce the ambipolarity. The aim here is to estimate the potential impact of the improved on–current on the static and dynamic performance of the TFET and circuits based on such a TFET. Hence, in the light of the scalability and flexibility of the compact model, first it is adjusted to a SG TFET, then optimized for the line tunneling case and in the end the model is used to simulate some digital

circuits.

To investigate the accuracy of the model for SG TFET, the structure shown in Fig. 7.9 is simulated in TCAD Sentaurus and the resulting electrical properties are compared with those obtained by means of the compact model. Then to tailor the model to an ideal line tunneling TFET some assumptions are applied. It is considered that the on–current in a line tunneling device is factor β greater than in a point tunneling TFET and in addition, to reduce the ambipolarity N_d is set to 10^{19}. In order to implement this effect in the model, in the point tunneling case $\beta = 1$ and for the line tunneling TFET the factor $\beta = 1000$. In Fig. 7.10 the transfer characteristic of both n–type and p–type TFETs in point tunneling case as well as the line tunneling case are presented. It can be seen that by increasing β the curves are simply shifted and the device shows a higher on–current.

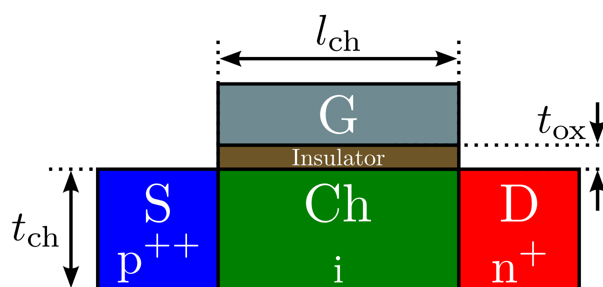


Figure 7.9: 2D sketch of the n–type SG point tunneling TFET. The model verification for the SG device is performed in comparison with the results of the TCAD simulations executed for this structure. The structural parameters are as follows: l_ch = 22nm, t_ch = 10nm, t_ox = 2nm of HfO_2, N_s = 10^{20}cm^{-3}, N_d = 10^{19}cm^{-3} and the channel is intrinsic [62].

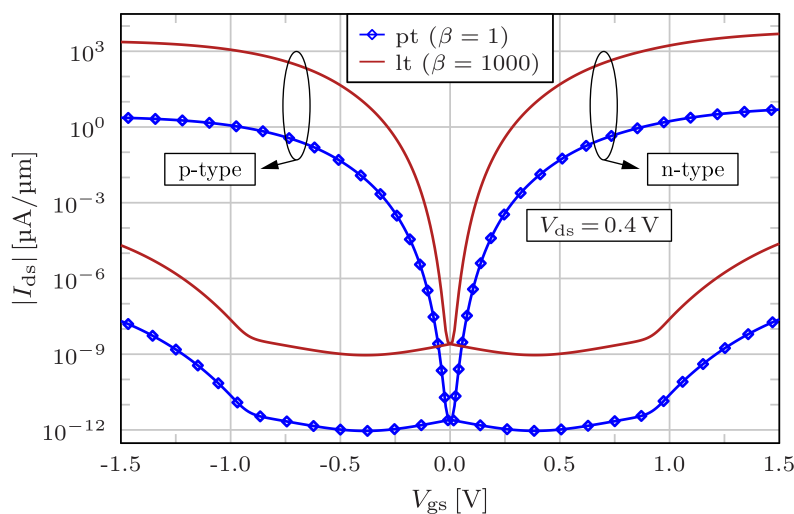


Figure 7.10: Transfer characteristic of the n– and p–type SG line tunneling TFETs in comparison with the point tunneling transistors [62].

By keeping all these assumptions, the model is used to simulate a TFET–based inverter and then with the help of this inverter an 11–stage ring–oscillator is simulated. These simulations are done for both $\beta = 1$ and $\beta = 1000$. Figure 7.11 presents the VTC of the inverter on the left axis and the I_{out} on the right axis. For $V_{\text{in}} = 0\,\text{V}$ and $V_{\text{DD}} = 0.4\,\text{V}$ (see Fig. 7.4(a)), the p–type TFET is in on–state and n–type transistor is in its off-state. Thus, it can be said that the supply voltage with a low resistance is connected to the V_{out} and therefore it is equal to 0.4 V. By increasing the input voltage the n–type TFET in the inverter also starts to conduct the current and switch to the on–state. As the result of the created path between V_{DD} and ground, the output current in this moment reaches its maximum. Finally, by further increment in V_{in} the n–type transistors is situated in on–state and the p–type TFET is turned off. So, this time one can say that the supply voltage with a high resistance is connected to the output and hence $V_{\text{out}} = 0\,\text{V}$. Moreover, it can be seen that for the both point and line tunneling TFET, VTC shows similar slope. However, the inverter which is based on line tunneling TFET obviously I_{out} is β times higher.

From the explanations in Sec. 7.1 and by considering the clarifications in the previous paragraph, one could easily anticipate that the point tunneling ring–oscillator has a longer oscillation period in comparison to the line tunneling one. This effect is due to the lower on–current of the point tunneling device and is shown in Fig. 7.12 that T in this case is almost equal to 15 ns while in line tunneling case $T \approx 15\,\text{ps}$.

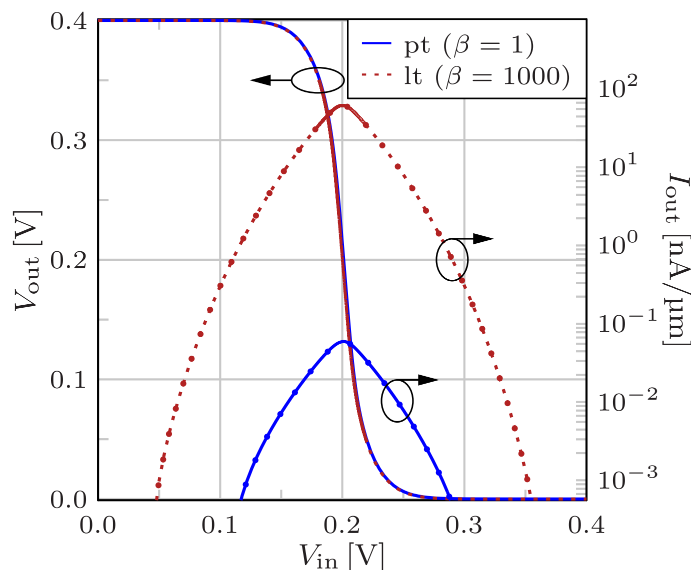


Figure 7.11: Voltage transfer curves of point tunneling and line tunneling inverters simulated in Cadence. The supply voltage is $V_{\text{DD}} = 0.4\,\text{V}$, the solid lines refer to the point tunneling case and the dotted lines represent the line tunneling case [62].

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Consequently, as it is illustrated in Fig. 7.13, the intrinsic delay of each inverter based on the point tunneling TFETs is three orders of magnitude larger than in one designed with the line tunneling transistors. Here τ is also calculated for different channel lengths. That is to say, the simulations of an 11–stage ring–oscillator for $l_{\mathrm{ch}} = 22, 45, 65, 90, 180$ and 250 nm are done. Then, by extracting T from these simulations and setting $n = 11$ in Eq. (7.1), τ is calculated. These values are depicted in Fig. 7.13 with the symbols. Furthermore, similar to 7.8, the relation between τ and l_{ch}, which is approximated by means of Eq. (7.2), is illustrated with solid lines. It can be seen that the obtained values are in a good agreement with the theoretical estimations. According to the Eq. (7.2) and in consideration of the fact that the current in TFET is not a function of l_{ch}, the intrinsic inverter delay is proportional to l_{ch} and both the data from simulations and the theoretical calculations support this concept. In addition, to have a reference for a comparison, the corresponding correlation for a CMOS inverter is also given (see the dotted lines in Fig. 7.13). Here it can be seen that τ is proportional to l_{ch}^2 which is due to the dependency of both current and capacitance of CMOS to the length of its channel [62].

The ring–oscillator simulations for TFET with $l_{\mathrm{ch}} = 22$ nm are repeated by varying V_{dd}. From these simulations the average current in each case is extracted. Then, by having the voltage, current and number of inverters in the circuit the average power consumption of each inverter is calculated:

$$P_{\mathrm{avg}} = \frac{I_{\mathrm{avg}} \cdot V_{\mathrm{DD}}}{n}. \tag{7.3}$$

In Fig. 7.14 the intrinsic inverter delay on the left axis and P_{avg} of each inverter in the ring–oscillator circuit on the right axis as a function of the V_{DD} are illustrated. The line tunneling inverter in comparison to the point tunneling inverter has a shorter τ and bigger average power consumption. Furthermore, it can be seen that an increase of V_{DD} leads to a higher power consumption, but the intrinsic delay is not drastically affected. It indicates that an increment in TFET on–current caused by higher V_{DD} is likely to be compensated by a larger amount of charge carriers stored in the intrinsic capacitances and hence, not a significant change can be seen in τ [62].

Considering Fig. 7.13 and Fig. 7.14 it can be concluded that with the help of innovative structures of TFETs such as line tunneling, it is possible to improve the dynamic performance of these transistors into a level which can compete with CMOS technology yet with lower supply voltage.

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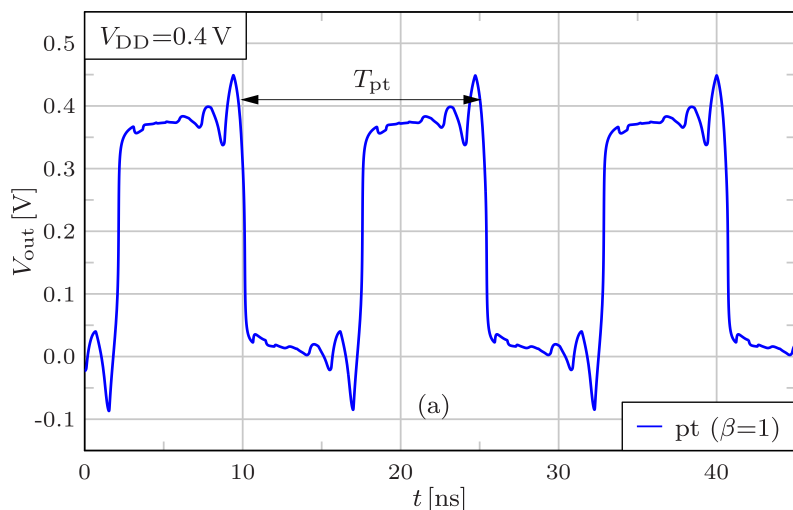
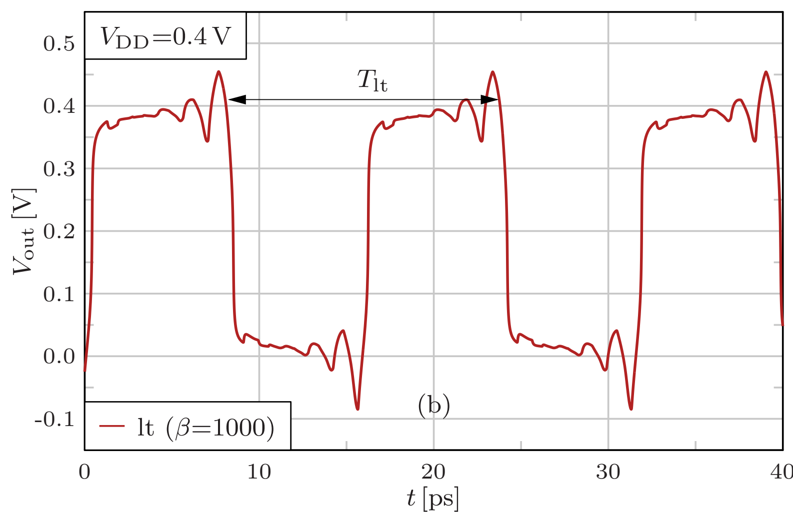


(a)



(b)

Figure 7.12: Output voltage of the 11–stage ring–oscillator in (a) point tunneling and (b) line tunneling case. T_{pt} presents the oscillation's period in [ns] for the point tunneling and T_{lt} refers to the oscillation period in [ps] for the line tunneling mode [62].

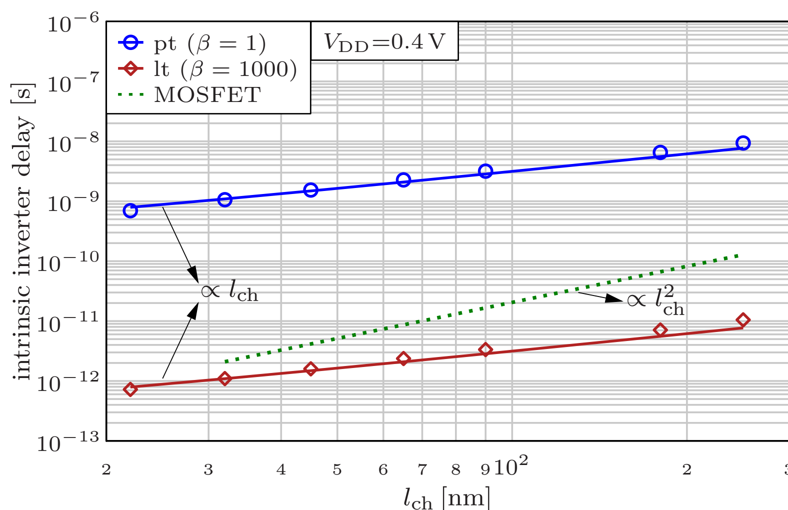


Figure 7.13: Intrinsic inverter delays, which are extracted from oscillation period of the 11–stage ring–oscillator, for both point and line tunneling cases are shown with symbols. The solid lines represent the theoretical relation between of the intrinsic inverter delay and the l_{ch}. The dotted line refers to the corresponding correlation for a CMOS inverter in the 32 nm process node with $V_{DD} = 0.8$ V [62].

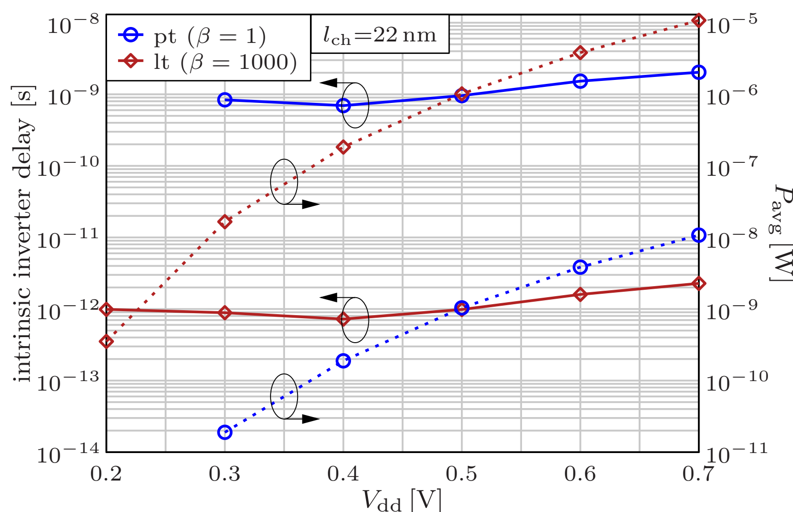


Figure 7.14: Intrinsic inverter delay and the average power consumption in an 11–stage ring–oscillator are shown on the left and right axis, respectively, as a function of V_{DD} [62].

CHAPTER 8

Conclusion

This dissertation presents a charge–based compact model for the intrinsic capacitances in TFETs. The model is based on a closed–form expression for the mobile charge in the channel introduced in [57, 69]. In the following, a brief summary is given of the steps taken in the course of this project from development of the model to the circuit simulations and results. A conclusion is then drawn under consideration of the results that have finally been achieved.

First, the compact model for an n–type Si DG TFET was derived. Similar to the other suggested capacitance models by Zhang et al. in [39] and Lu et al. in [38], in the preliminary assumptions it has been considered that the inversion channel charges are equally distributed. To calculate the total mobile charge of the channel, it was therefore adequate to calculate the charge density at one point of the channel and then integrate it over the entire area. Although this assumption is not valid in a real structure, the resulted capacitances based on it were in a quite good agreement with the TCAD simulations. However, for further investigations the capacitance model was compared to the measured capacitances of a fabricated TFET. In the light of the measurement data, it has become clear that the assumption of a uniform charge distribution in the channel may work if the model is compared with the simulated data, but it is not sufficient to show all the details and gain a deep insight into the capacitive behavior of a real TFET. Hence, it has been concluded that some effects including the channel resistance and parasitic elements are needed to be integrated into the model.

The first series of measurements correspond to a p–type Si SG planar TFET which is fabricated in Juelich Forschungszentrum. In order to include the effect of the channel resistance, the compact DC model provided in [35] is used. That is to say, considering the structural parameters of the device which are under investigation and with the help of the DC model, first I_{ds} is calculated. Then, the bias dependent channel resistivity by means of an empirical method is calculated. Having I_{ds} and R_{ch} allows for calculating the voltage drop between the junction and the tunneling barrier in the channel. Therefore, by applying the V_{ds} into the charge density closed–form expression, the mobile charge density at the drain junction is obtained and by implementing $V_{\mathrm{ds}} - \Delta V$ in the aforementioned formula, the mobile charge

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per gate area at the tunneling barrier in the channel close to the source junction is calculated. Then by taking the average of the two obtained values and multiplying the result with the area of the channel, the total mobile charge of the channel in the on–state is achieved. The compact intrinsic capacitance model considers not only the on–state, but also the ambipolar–state of the transistor. Hence, in the ambipolar–state to calculate the charge density at the junction and tunneling barrier located close to the drain junction, respectively V_s and $V_s - \Delta V$ are used in the charge density expression.

Adding the effect of the channel resistance into the intrinsic capacitance model by combining it with the compact DC model has brought the results of the model closer to the measurement data. Moreover, due to the fact that the DC model takes into account the effect of traps and the doping concentration in the source and drain regions, the capacitance model can also capture the influence of these parameters on the intrinsic capacitances of TFET. Nevertheless, the capacitive behavior of the fabricated TFET could still not be fully reproduced by model. Hence, it has been decided to incorporate the parasitic effect of series resistances into the capacitance model.

To do so, it is considered that a resistance is connected in series at each terminal on the source and drain side. The effect of these resistances on the intrinsic capacitances is implemented with the same method which is introduced in [73]. This approach has been originally developed to enhance the compact model of MOSFETs, though is appropriate for other structures as well. But, after all, the model needed some more details to show the similar behavior of the measured capacitances.

Eventually, these measurement data have led to investigations into the influence of the Schottky barrier at the the source and drain terminals on the intrinsic capacitances of the TFET and to the inclusion of this effect in the compact model. For this purpose an empirical method is used. This method has evolved on the basis of the analysis of experimental data and shows that in the on–state at higher $|V_{gs}|$ the capacitive behavior of the transistor is assigned not only to C_{gd} but also partially to C_{gs}. In the ambipolar–state illustrates that for higher $|V_{gs}|$, the intrinsic capacitance of the TFET is not identical to the C_{gs} however, a sum of both capacitances C_{gs} and C_{gd}.

The results of the TCAD simulations of the planar structure including Schottky barriers at the terminals could not fulfill the expectation and reproduce a similar capacitive behavior as in measurements. Different approaches have been considered to evaluate the correct values and ratios, with which at a certain gate bias one capacitance decreases and the other increases. In the end, with the help of TCAD Sentaurus, some Schottky diodes with different drain doping concentrations are simulated. By comparing their current with the measured I_{ds} in a p–type TFET, the diode with a current closer to I_{ds} is chosen and its conductance is extracted. This value is used to estimate the small signal conductance of the Schottky barrier in the TFET and check the effect on the intrinsic capacitances. Finally, the model could show a similar pattern as in the measured data.

As the last step of verifying the model, it is compared to the measurement data of an

n–type Si NW TFET. This structure is fabricated by imec, Belgium [83] and the measurements are provided by University of Sao Paulo, Brazil. Considering the cylindrical shape of the NW TFET, an equivalent DG l_{ch} is used in the model. Furthermore, to cover the effect of the gate–source overlap in this structure, a constant parallel capacitance to the C_{eff} is implemented in the compact model. Then, with the help of the other already existing fitting parameters, the model is fitted to measurements. Comparing the results to the measured transfer characteristic and capacitances of the NW shows that the model is in a good agreement with the experimental data.

After completion of the model, it is transferred to the Verilog–A language to enable circuit simulations. Using this compact TFET model, an inverter circuit is designed in Cadence Virtuoso. This circuit is then used to design a ring–oscillator. In order to examine the effect of the device parameters on the behavior of circuits, the simulations are performed using different parameters and properties for both p– and n–type TFETs. In each case, to ensure that both the DC and AC simulations of these transistors as a single element are reliable, firstly the results of the compact model simulations of the TFETs are verified against TCAD simulations. The circuit simulations based on verified transistors are then performed. The parameters which are considered in these simulations are: $N_{\mathrm{t}}, N_{\mathrm{d}}, l_{\mathrm{ch}}$ and V_{fb}. Although all the mentioned parameters affect the behavior of the device, only by varying V_{fb} a significant influence in outputs of the circuits has been observed which is due to the operation range of the circuits. Based on these observations, two main setups for the circuit simulations are taken into account: HP and LP mode. In HP mode, V_{fb} is shifted by $-200\,mV$. As a result, the transfer characteristic of the TFET is shifted and it appears as having a higher on–current and thus greater performance. LP refers to the case in which V_{fb}–shift$=\ 50\,mV$. In contrast to the HP mode, in this case the shift in V_{fb} yields to a lower I_{ds} for low V_{gs}.

Comparing the inverter output in HP and LP mode shows that the inverter in LP case has a higher DC gain and lower switching current in comparison to the HP mode. Hence, the transient simulations of the inverter for a pulse input demonstrate higher overshoot and undershoot in LP mode than in HP. Moreover, the 3–stage ring–oscillator in LP case has a lower oscillation frequency in comparison to the HP setup.

Next, by varying l_{ch} of the TFETs, the ring–oscillator simulations are performed in both HP and LP mode. With the aid of these simulations, first the oscillation period is calculated in each case and then by means of T, intrinsic inverter delay is obtained. For comparison purpose, also the intrinsic inverter delay of a CMOS inverter as a function of its channel length is considered.

Bearing in mind the fact that with further innovation of the structures, the TFET on-current can be enhanced, the I_{ds} [92], further circuit simulations are carried out to observe the behavior of TFET–based circuits in case they have a higher current. In this regard, output of the circuits based on the point tunneling TFET are compared to those based on line tunneling TFET. To do so, the compact model is firstly verified against TCAD simulations of a SG n–type TFET as well as p–type TFET. Therefore, the model is fitted for an ideal line tunneling case in which

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the on–current of the TFET is 1000 times higher than in the point tunneling case. Afterwards, simulations of an inverter and a 11–stage ring–oscillator are performed to compare the point and line tunneling setups.

By means of these simulations the oscillation period of the ring–oscillator and from that the intrinsic inverter delay as a function of l_{ch} is obtained. The resulted τ for the point tunneling and line tunneling case are compared to each other and also to the corresponding data of a CMOS inverter. Finally, the average power consumption of the ring–oscillator by varying V_{DD} was achieved.

After all mentioned above and considering the results of the circuit simulation, the following can be concluded:

- The intrinsic capacitance model is flexible and scalable and can be employed for various structures. In the course of the model verification it is shown, despite that the model is designed based on a short–channel Si DG n–type structure, its simplicity and flexibility allows for calculating of various structures and also different types such as the p–type SG planar TFET and the n–type NW TFET.

- The model is applicable for a wide range of V_{gs} and considers not only the on–state of the device but also the off– and ambipolar–state.

- It is accurate. The compact model is validated using both TCAD simulation and measurement data. The results of the model show a good match to those obtained by TCAD simulation and also to the measurements.

- It considers the parasitic effects. The parasitic elements can drastically affect the capacitive behavior of the TFETs. Hence, it is important to include them in the model.

- The model can also include the non–ideal effects such as TAT on the capacitances.

- From all these points, it can be concluded that the compact model can provide a reliable insight about the intrinsic capacitances in TFET.

- Furthermore, the compact model presented here is not time consuming or computationally demanding which allows for circuit simulations including multiple TFETs.

- The compact TFET model is SPICE friendly.

- Although the variation of N_t and N_d has a strong influence on the electrical characteristics of the TFET considered as a single element, no such apparent difference is evident in the circuit simulation results.

- Varying V_{fb} has a major impact on the performance of the TFET–based circuits. In fact, by changing V_{fb} the transfer characteristics of the TFET is shifted. Depending on the direction of this shift, the TFET shows higher or lower current for smaller V_{gs} which

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is similar to the situation that the on–current of the transistor is enhanced or reduced. Thus, the variation of the parameter V_{fb} leads to a drastic change of the output on the circuit level.

- In TFET inverter τ is proportional to l_{ch} whereas for standard MOSFET it is proportional to l_{ch}^2, which is due to the fact that in TFET the current is not a function of l_{ch}.

- To improve the dynamic performance of the TFET–based circuits, the on–current of the TFET needs to be increased.

- By increasing V_{DD} the power consumption in the TFET and consequently the TFET–based inverter goes higher, but the intrinsic inverter delay is not affected.

- There are still challenges that must be tackled before the TFETs can really meet all expectations and conquer the ICs. Researchers are constantly trying out new manufacturing methods, materials and structures to push the limits. With each step, new aspects of the TFET become apparent. In this case, fitting parameters can help to adapt the model and make it work without applying any complicated changes in the model.

- Once the obstacles which limit the on–current of TFET are overcome with the help of novel structures and materials, TFET will be able to stand up to the competition with CMOS technology, however with considerably lower supply voltage requirements.

- There are still factors such as temperature and frequency which have an effect on the capacitive behavior of the TFET and consequently on the output of the circuit which are not considered in this model. Probably in future works they can be included in the compact model as well.

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