QCA based error detection circuit for nano communication network

ABSTRACT

This paper outlines low power nano-scale circuit design for even parity generator as well as even parity checker circuit using quantum-dot cellular automata (QCA). The proposed even parity generator and even parity checker is achieved by using a new layout of XOR gate. This new XOR gate is much denser and faster than existing ones in the state of the art. The proposed parity generator has out shined the existing design by reducing the cell count as 10proposed parity checker has also out shined the existing design with an improvement in cell count as 17.94circuits are denser and faster than existing one. Nanocommunication architecture with the proposed circuits is also demonstrated. The bit-error coverage by the proposed method is described. Besides, the defects in the circuits are explored to facilitate guide to proper implementation. The tests vectors are proposed to identify the defects in the designs and the defect coverage by those test vector are also described. The estimation of dissipated energy by the layouts established the very low energy dissipation nature of the designs. Different parameters like logic gate, density and latency are utilized to evaluate the designs that demonstrate the faster processing speed at nano-scale.

Keyword: Communication; Majority gate; Parity checker; Parity generator; Power dissipation; QCA