ANALYSIS, DESIGN AND CONTROL OF GRID CONNECTED THREE PHASE PULSE WIDTH MODULATED AC-DC CONVERTER

AZZIDDIN MOHAMAD RAZALI

ANALYSIS, DESIGN AND CONTROL OF GRID CONNECTED THREE PHASE PULSE WIDTH MODULATED AC-DC CONVERTER

by

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A thesis submitted
to the School of Graduate Studies
in partial fulfillment of the requirements for the degree of

Doctor Philosophy

Faculty of Engineering and Applied Science
Memorial University of Newfoundland

October 2013

St. John's Newfoundland Canada

ABSTRACT

The increasing penetration of line-commutated power diode and thyristor rectifiers into the grid power system is becoming a problem in transmission and distribution lines due the harmonic and reactive currents they inject to the grid system. Therefore, three-phase pulse width modulation (PWM) ac-dc converters are becoming more and more attractive for replacing the line-commutated rectifiers in the utility-interface applications. With a proper control technique, the PWM ac-dc converter is able to reduce the harmonics in the line currents. This leads to the achievement of almost sinusoidal input currents and provides controllable dc-link output voltage, unity power factor operation and regeneration capability. These features are not necessarily achieved under non-ideal operating conditions such as unbalanced, distorted and disturbed grid supply.

This thesis investigates a virtual flux control for reducing the number of sensors in the direct power control (DPC) and the voltage oriented control (VOC) of a three phase PWM ac-dc converter. The use of input ac voltage sensors to measure the grid voltage for synchronization and estimation of input instantaneous active and reactive powers is avoided by applying a virtual flux concept in the new proposed control schemes. The virtual flux control technique is used to extract the grid voltage information from the converter switching states, dc output voltage and line currents.

A virtual flux direct power control (VFDPC) utilizing an improved virtual flux estimator and a newly designed switching look-up table, is proposed in this thesis.

The switching look-up table is developed based on the instantaneous power derivative method which relies on the sign and magnitude of the change in instantaneous active and reactive powers. In this way, the switching table is able to choose the best converter voltage vector in order to ensure smooth control of active and reactive powers.

Furthermore, a new virtual flux oriented control (VFOC) technique is proposed so that the ac-dc converter operates with a fixed switching frequency. The VFOC control structure is developed by using a newly derived mathematical model of the three phase ac-dc converter incorporating the estimated virtual flux components. Subsequently, the proposed VFOC is able to include the decoupling network and feed-forward control components to enhance the converter performance during the grid and load disturbances.

It has been confirmed through simulation and experiment that the proposed VFDPC and VFOC are able to produce three phase sinusoidal input currents with low total harmonic distortion, near unity power factor and adjustable dc-link output voltage under balanced and non-ideal conditions of the input voltage supply.

ACKNOWLEDGMENT

I would like to express my sincere gratitude and appreciation to my supervisor Professor M. Azizur Rahman for his continuous guidance, advice and encouragement towards the completion of the PhD program.

Special thanks to Dr. Glyn George and Dr. Mohamed Hossam Ahmed, the members of my supervising committee for their useful suggestions.

I am very grateful to University Technical Melaka Malaysia for providing me an opportunity and scholarship to further my Doctoral study at Memorial University of Newfoundland Canada.

My gratitude goes to the technical staff of MUN Engineering Department, Greg O'Leary, George Rioux, Frank Pippy and Tom Pike for having valuable discussion and assistance during the development of experimental set-up and hardware prototype.

Special thanks to all MUN Faculty members and School of Graduate Studies for giving full support and assistantship regarding the university policy and management aspects.

Thanks to my graduate fellows working in MUN Power Devices and System Research Lab for having nice experiences discussing and socializing together.

I also would like to express my deepest gratitude and sincere appreciation to my wife Aslinda Hassan and children, my parents Mr. Mohamad Razali Suprat and Mrs. Haliza Abdullah, as well as other family members, relatives and friends for their understanding and everything they have done for me. They have supported and

encouraged me besides showing their great patience during all my period of studies at MUN. Their existence in my life reminds me that there are things more important than this work.

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LIST OF SYMBOLS

C	-	dc-link capacitor
d,q	-	direct and quadrature axis of rotating synchronous reference frame
f	-	grid voltage frequency
f_s	-	sampling frequency
T_s	-	sample period
$E_{g,i}$	-	grid voltage of phase *i (i=a,b,c)*
E_{LL}	-	grid line to line voltage
E_{phase}	-	grid phase to neutral voltage
$\bar{E}_{g,an}$	-	grid phase a voltage vector
E_m	-	amplitude of the phase voltage
$V_{i,rect}$	-	pole voltage of phase *i (i=a,b,c)* at rectifier side
$\bar{V}_{conv,an}$	-	converter pole voltage vector at leg *a*
$\bar{V}_L$	-	voltage vector of the line filter inductor
$\bar{V}_R$	-	voltage vector of the internal resistor in line filter inductor
S_i	-	gate signal at converter upper switch of leg *i (i=a,b,c)*
$V_{i,inv}$	-	pole voltage of phase *i (i=a,b,c)* at inverter side
S_i'	-	gate signal at converter lower switch of leg *i (i=a,b,c)*
R_i	-	internal resistance in phase *i (i=a,b,c)* inductor
L_i	-	line inductance of phase *i (i=a,b,c)*
$I_{g,i}$	-	grid line current of phase *i (i=a,b,c)*
I_m	-	amplitude of the line current
V_0	-	output voltage
$V_{0,ref}$	-	output voltage reference
V_{dc}	-	dc-link output voltage
$V_{dc,ref}$	-	dc-link output voltage reference
$I_{g,i,ref}$	-	current reference template of phase *i (i=a,b,c)*
$\hat{I}$	-	amplitude of the current reference template
I_{dc}	-	dc-link output current
e	-	error signal
$I_{g,\alpha\beta}$	-	stationary components of the grid current
$I_{g,dq}$, I_{dq}	-	direct and quadrature components of the grid current
$I_{g,dq,ref}$ $I_{dq,ref}$	-	direct and quadrature components of the grid current reference
$E_{g,\alpha\beta}$	-	stationary components of the grid voltage
$E_{g,dq}$	-	direct and quadrature components of the grid voltage
$V_{conv,\alpha\beta}$	-	stationary components of the converter pole voltage
$V_{conv,dq}$	-	direct and quadrature components of the converter pole voltage

ω_e or ω	-	grid operating frequency in radian per second
θ	-	angle of the grid voltage vector or the grid virtual flux vector
$\bar{E}_{g,\alpha\beta}$	-	grid voltage vector in stationary reference frame
$\bar{E}_{g,dq}$	-	grid voltage vector in rotating synchronous reference frame
P	-	estimated active power
P_{ref}	-	command/reference active power
Q	-	estimated reactive power
Q_{ref}	-	command/reference reactive power
Δ_P	-	active power error signal
Δ_Q	-	reactive power error signal
d_P	-	output signal of the active power hysteresis controller
d_Q	-	output signal of the reactive power hysteresis controller
h	-	hysteresis tolerance band
θ_n	-	sector number
δ	-	angle different between the converter pole voltage vector and grid voltage vector
$\bar{\Psi}_{g,\alpha\beta}$	-	grid virtual flux vector in a stationary $\alpha\beta$-reference frame
$\Psi_{g,\alpha\beta}$	-	grid virtual flux components in a stationary $\alpha\beta$-reference frame
$\bar{\Psi}_{g,dq}$	-	grid virtual flux vector in a synchronous rotating dq-reference frame
$\Psi_{g,dq}$	-	grid virtual flux component in a synchronous rotating dq-reference frame
$\bar{\Psi}_{conv,\alpha\beta}$	-	converter pole virtual flux vector in a stationary $\alpha\beta$-reference frame
$\Psi_{conv,\alpha\beta}$	-	converter pole virtual flux components in a stationary $\alpha\beta$-reference frame
$\bar{\Psi}_{conv,dq}$	-	converter virtual flux vector in a synchronous rotating dq-reference frame
$\Psi_{conv,dq}$	-	converter virtual flux component in a synchronous rotating dq-reference frame

LIST OF ABBREVIATIONS

ADC	-	Analog to digital converter
DAC	-	Digital to analog converter
DPC	-	Direct Power Control
DSP	-	Digital signal processor
DTC	-	Direct Torque Control
EMI	-	Electromagnetic Interference
FOC	-	Field Oriented Control
HB	-	Hysteresis band
IGBT	-	Insulated gate bipolar transistor
MRCC	-	Multi-resonant current controller
MUN	-	Memorial University of Newfoundland
PAM	-	Phase and Amplitude Control
pf	-	Power factor
PFC	-	Power factor correction
PI	-	Proportional-Integral
PLL	-	Phase locked loop
PWM	-	Pulse Width Modulation
RMS	-	Root mean square
SPWM	-	Sinusoidal pulse width modulation
SRF	-	Synchronous reference frame
SVM	-	Space vector modulation
THD	-	Total harmonic distortion
UPS	-	Uninterruptible power supply
VFDPC	-	Virtual Flux Direct Power Control
VFOC	-	Virtual Flux Oriented Control
VOC	-	Voltage Oriented Control
VSC	-	Voltage source converter
VSI	-	Voltage source inverter
VSR	-	Voltage source rectifier

Chapter 1

Introduction and State of the Art Review

1.1 Introduction of the Three Phase Front-end AC-DC Converter

Research in the area of power electronics and its applications has been carried out for more than five decades following the introduction of the transistor and thyristor devices in the 1950s. However, the research is still being intensively and progressively carried out by numerous investigators in many universities and industries. For a long time, the emphasis of the research in electrical machine drives system has been put on the machine inverter and its control, while the ac to dc rectification has been realized by a diode bridge rectifier or a line-commutated phase controlled thyristor bridge rectifier. Although both rectifier topologies offer a high reliability and simple structure, they also have major inherent drawbacks. A general electrical machine drives configuration, utilizing three phase diode rectifier and 2-level inverter is shown in Figure 1-1. The diode bridge rectifier generates uncontrolled dc-link output voltage, low power factor and the power flow is unidirectional. Furthermore, the input current of the diode rectifier is highly distorted and has significant harmonic contents [1-2]. An experimental waveform of the phase *a* three phase diode rectifier current as revealed by Figure 1-2, gives confirmation that the three phase diode bridge rectifier generates significant current

total harmonic distortion which might be injected back to the grid system, thus decreasing the quality of grid supply.

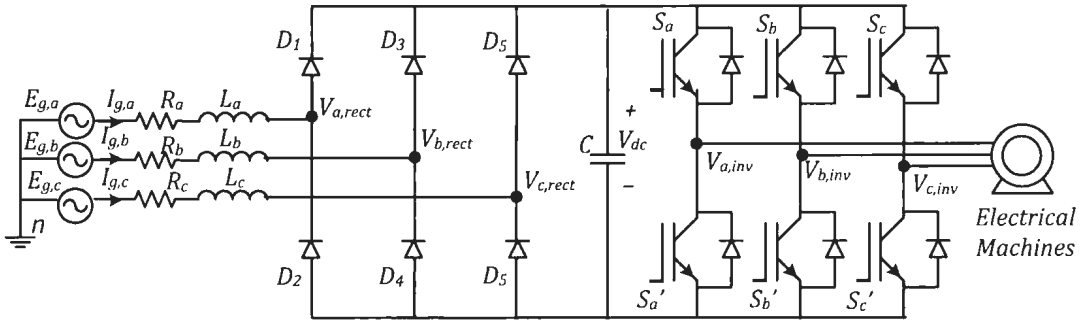


Figure 1-1: Front-end three phase diode bridge rectifier in electrical machine drives system

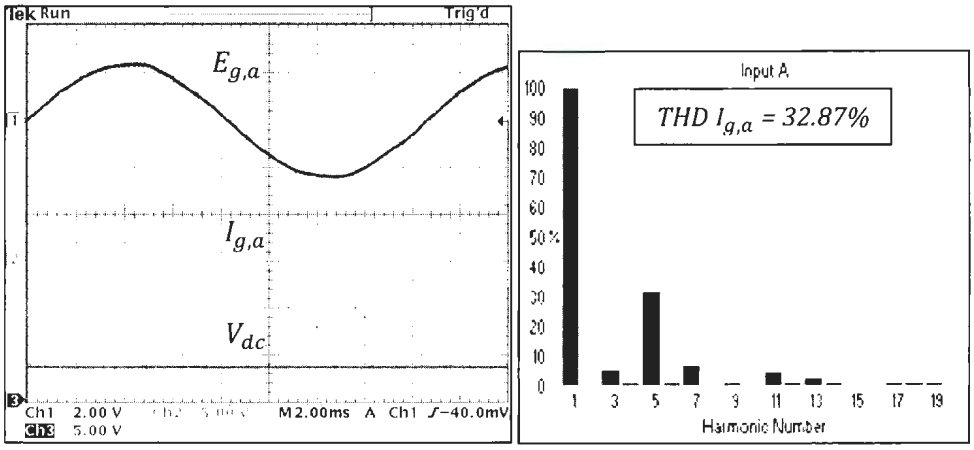


Figure 1-2: Waveforms at the three phase diode rectifier side. Left:- From top to bottom; phase *a* grid voltage (60V/div), phase *a* input current (0.5A/div), dc-link output voltage. Right:- Harmonic spectrum of the phase *a* grid current

Even though regulation of the dc-link output voltage of the thyristor bridge rectifier can be achieved by controlling appropriately the thyristor switching firing angle, the total harmonic distortion (THD) of the line current is still relatively high

[3]. Reversing power flow from the dc side to the ac side is possible by reversing the polarity of the dc voltage. However, polarity reversal is not allowed since the electrolytic capacitor is typically used in the dc-link of a voltage source converter. Bidirectional power flow without dc voltage polarity reversal is possible by connecting two thyristor bridges in anti-parallel. Consequently, the number of the power switches is doubled which will increase the size and cost of the whole system.

High level of harmonic distortion in the line currents and low power factor has negative impacts on the whole power electronic system. The high harmonic currents produced by nonlinear operation of the power switches can interact adversely with a wide range of power system equipment, particularly the capacitors, transformers, generators and transmission lines, which will result in increasing the volt-ampere rating of that equipment, causing additional losses such as overheating and overloading. Excessive line currents above rated value might trip off the protective relays which will interrupt the power grid system. These harmonic currents may also generate electromagnetic interference (EMI) which will affect customers of the power system, particularly those who use sensitive electronic equipment.

International technical organizations and government agencies have introduced standards and regulations such as IEEE-519 in North America and IEC-61000 in the European Union, to maintain the voltage and current quality of utility grids at accepted levels [4]. In order to meet these standards and to improve the power quality, the usage of harmonic compensation techniques which can be realized either by using passive filters [5-6], active filters or hybrid filters [7-8], are normally

employed along with the conventional diode and thyristor rectifiers especially in large power rating and already existing installation facilities. However, these additional devices require extra cost are bulky and have significant losses, which reduce efficiency of the whole power conversion system.

Another way to improve the power quality is by applying the so-called power-factor correction (PFC) methods [9-10]. The PFC is able to mitigate the current harmonics, improve the power factor and generate a stable dc-link output voltage. There are many different topologies with different configurations of ac-dc converter which can be used to implement PFC control schemes such as boost, buck, buck-boost and multilevel ac-dc converters [4, 11]. Each converter topology has different working principles, capabilities and control strategies. In general, the high performance PFC converter feeding the electrical machine inverter drives system should offer following features and abilities:

i) Nearly sinusoidal input current with low total harmonic distortion.

ii) Bidirectional power flow capability to fulfill power regeneration capability.

iii) Controllable dc-link output voltage so that the dc output voltage is well regulated at a desired reference level.

iv) Adjustable power factor to achieve unity power factor operation.

v) Reduction of transformer power rating and cable size due to unity power factor operation. As a result, the total cost of the drives system will be reduced.

vi) Less sensitivity to line voltage variation and load change.

vii) Reduction of dc-link capacitor.

The three phase voltage source ac-dc converter as shown in Figure 1-3 offers additional advantages above other PFC converter topologies. The topology consists of six insulated gate bipolar transistors (IGBTs). Each IGBT is connected to an anti-parallel fast recovery power diode. With proper control strategy and switching technique, this topology is able to fulfill most of the PFC requirements in variable speed drives applications. Besides those advantages offered by this type of converter, the ac-dc converter has poor immunity to shoot-through faults. The shoot-through faults can be eliminated by implementing dead-time control to the switching technique. The dead-time control will ensure that the two IGBTs on the same leg are not turning on at the same time.

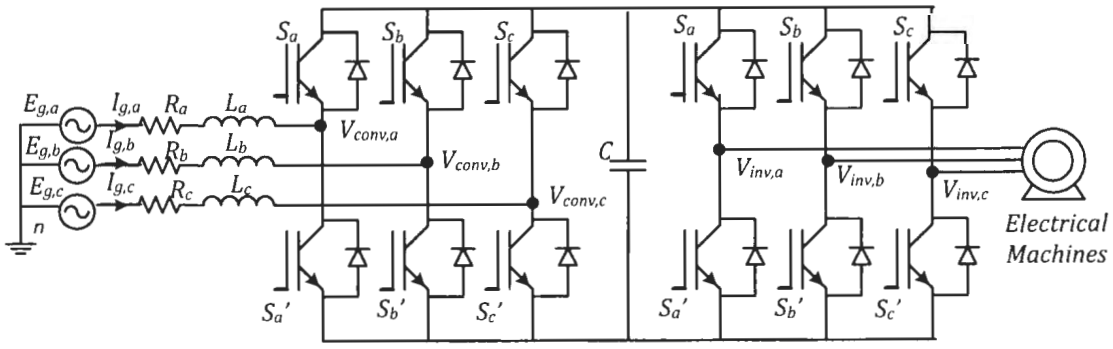


Figure 1-3: Front-end three phase ac-dc converter in electrical machine drives system

The term of an ac-dc converter used in this thesis is also known as pulse width modulated (PWM) voltage source rectifier (VSR). Subsequently, PWM VSR is a voltage source converter (VSC) that converts the ac voltage and current into the dc voltage and current via series of line inductances and transistor switching devices.

In some literatures, the voltage source ac-dc converter is also mentioned as active rectifier or front-end boost type rectifier.

1.2 Review of the Control Techniques for the Three-Phase AC-DC Converter

The performance of the complete converter system is highly dependent on the quality of the applied control technique being used. Various control strategies have been proposed in recent works on the three phase ac-dc converter [9, 12-13]. Each of the control strategies has to fulfill basic requirements of the front-end ac-dc converter such as low harmonic distortion of the input current, unity power factor operation, good dynamic response and regulation of the dc-link output voltage. Although the objectives of the control schemes are same, their principles and approaches in controlling the converter are different.

1.2.1 Phase and Amplitude Control (PAM) Technique

Controllers for the PWM rectifier based on phase and amplitude (PAM) control strategy have been reported by several researchers [9, 14-16]. The PAM control method works by controlling and adjusting the angle and the magnitude of the current template waveforms. Regulation of the dc-link output voltage and adjustment of the power factor are obtained by changing the amplitude of this current template and its phase shift with respect to the main voltage supply. A block

diagram of the voltage source current controlled PWM rectifier utilizing the PAM control method is shown in Figure 1-4.

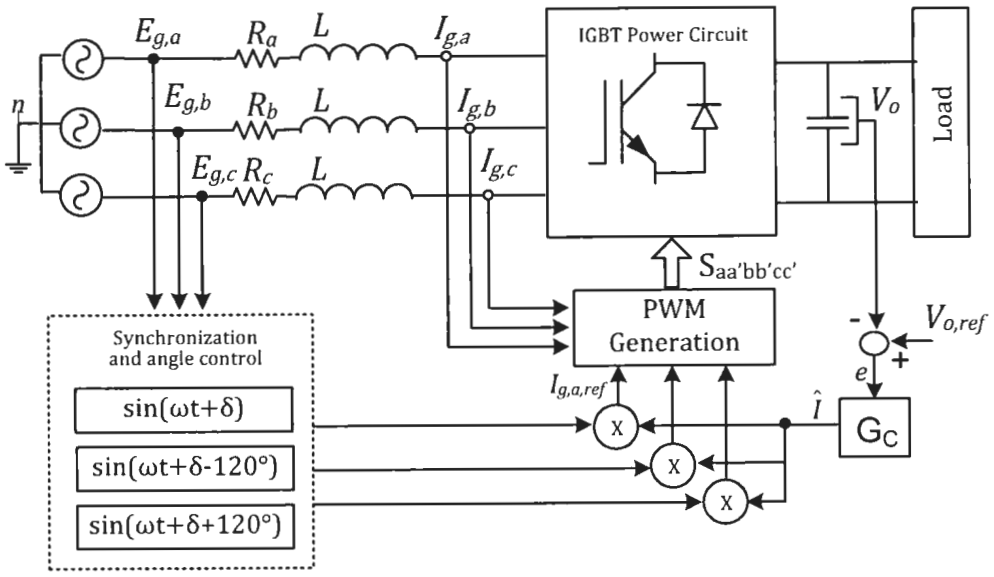


Figure 1-4: Voltage source current controller PWM rectifier utilizing Phase and Amplitude (PAM) control technique

A feedback voltage control loop is required to regulate the dc-link voltage. The dc voltage V_o is compared with a reference $V_{o,ref}$ to obtain the error signal "e". Subsequently, this error signal will be used to generate a current template waveform. The template has a shape of a sinusoidal waveform with the same frequency as the main supply and is used to produce the PWM pattern for the converter switching device. The amplitude of the current reference template $\hat{I}$, is computed using the following equation:

$$\hat{I} = G_C e = G_C(V_{o,ref} - V_o) \tag{1.1}$$

where G_C is shown in Figure 1-4, and represents a controller such as PI, P, Fuzzy Logic, or other control technique. The sinusoidal waveform of the current template is obtained by multiplying $\hat{I}$ with a sine function, with the same frequency of the mains, and with the desired phase shift angle [9]. The converter control is achieved by measuring the three phase currents and forcing them to follow the sinusoidal current reference template, $I_{g,i,ref}$ $(i = a, b, c)$ whose amplitude is given by equation (1.1). Standard modulation techniques such as sinusoidal pulse width modulation (SPWM), space vector modulation (SVM), and hysteresis band (HB) can be used by the converter control system to generate the switching pulses. One major problem arises with the rectifier control system, because the dc-link voltage feedback control loop utilizes a PI controller that can produce instability [15]. Therefore, it is essential to analyze this instability problem during the initial design of the rectifier system so that the PI controller can be tuned appropriately.

1.2.2 Voltage Oriented Control (VOC) Technique

PWM rectifiers can be also controlled by the control strategies analogous to the control methods of induction or synchronous machines [17],[18]. In general, the control schemes associated with the PWM rectifier can be classified into two types:

i) Voltage oriented control (VOC) [19-21]

ii) Direct power control (DPC) [22-24]

VOC is similar to the field-oriented control of the induction motor, where the VOC method is able to produce high dynamic and static performances through the usage of internal current control loops and an outer voltage control loop. VOC is based on the rotating synchronous reference frame orientation with respect to the grid line voltage vector. By transforming the three phase quantities to appropriate dc components, the proportional and integral (PI) controllers are able to lead the estimated *dq* current components to the desired reference values with zero steady state error [20, 25]. The *d*-axis reference current $I_{g,d,ref}$ is controlled to perform the dc-link voltage regulation while the reference current in *q*-axis $I_{g,q,ref}$ is controlled to obtain a unity power factor. Figure 1-5 illustrates the VOC principle involving the use of the rotating synchronous reference frame. In a particular operating condition such as unity power factor operation, the synchronous transformation is oriented so that the *d*-axis is aligned with the grid voltage vector $\bar{E}_{g,dq}$ as shown in Figure 2-6. Two PI regulators in the internal current loops compensate any existing current errors by generating an appropriate converter control voltage vector, which is transformed back to the phase quantities and used as the input signals by the pulse width modulator to generate the switching signals to the power switch devices. Although the VOC approach is able to make the input currents track the reference currents, the PI current regulators do not work well as rapid tracking controllers for the couple system [21]. Equations (1.2) and (1.3) show that the voltage equations of three phase PWM rectifier in the *dq*-frame are dependent due to the cross-coupling terms which are given by $\omega L I_{g,q}$ and $\omega L I_{g,d}$:

$$E_{g,d} = RI_{g,d} + L\frac{dI_{g,d}}{dt} - \omega LI_{g,q} + V_{conv,d} \tag{1.2}$$

$$E_{g,q} = RI_{g,q} + L\frac{dI_{g,q}}{dt} + \omega LI_{g,d} + V_{conv,q} \tag{1.3}$$

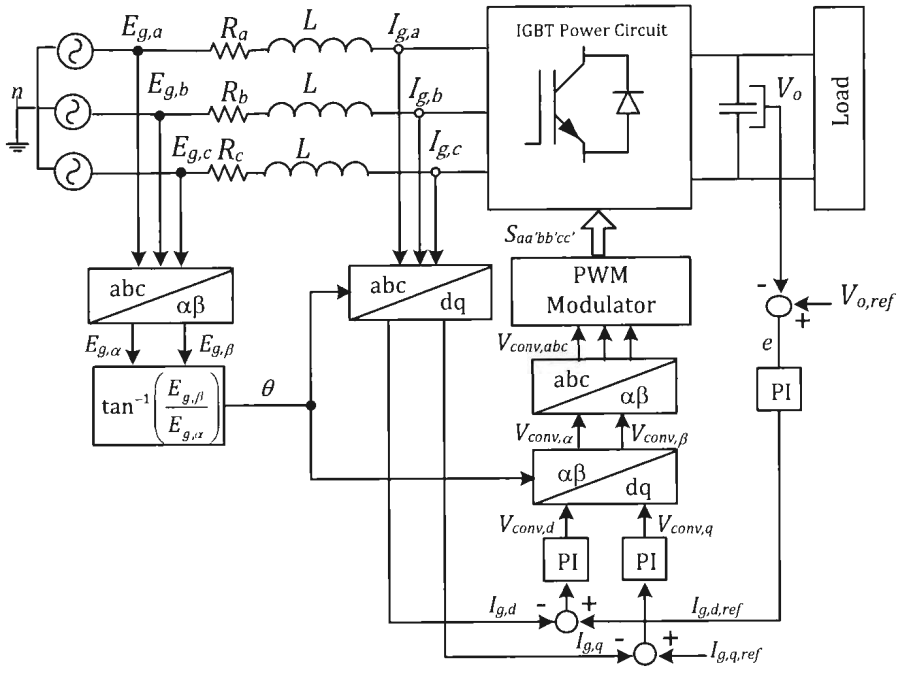


Figure 1-5: Structure of Voltage Oriented Control (VOC) in a rotating synchronous reference frame

In order to apply independent controllers for the two coordinate components, the influences of the q-axis on the d-axis component and the d-axis on the q-axis component have to be removed. A decoupling network using the block containing ωL information can be used to minimize the coupling effects [21, 26-27]. In addition, the measured grid voltages denoted by $E_{g,d}$ and $E_{g,q}$ can be effectively utilized as feed-forward control signals for reducing the effect of grid voltage disturbance to the

PWM rectifier operation. The parameters of the two PI regulators can be calculated based on the designed methods presented in [17, 28]. Poles and zeros of the compensator should be located with the intention to achieve sufficient stability margins so that the system produces good steady-state and dynamic performances. The dc output voltage regulation is typically implemented with a PI regulator in the feedback control loop. The PI regulator provides the value of $I_{d,ref}$, while $I_{q,ref}$ is fixed to zero in order to obtain unity power factor. A better dynamical performance in the dc-link voltage can be achieved by feed-forward compensation by calculating the power in the dc-link [29-30].

1.2.3 Direct Power Control (DPC) Technique

The direct power control (DPC) strategy for the PWM rectifier is the most interesting emerging control technique which is derived from the basic idea of Direct Torque Control (DTC) of induction machines [20], [22]. Similar to the DTC scheme, there are neither internal current control loops nor a pulse width modulator to control the PWM rectifier. Instead, DPC regulates the line currents and dc-link output voltage by controlling the input instantaneous active and reactive power. The three phase supply voltage and current are measured to estimate the instantaneous active and reactive powers. Subsequently, the command active power P_{ref} and reactive power Q_{ref} are compared with the estimated active P and reactive Q power values via two hysteresis controllers. The two hysteresis controllers operate based on P and Q error quantities. The digitized output signals of the

hysteresis controllers and a grid voltage vector angle position are used to select the appropriate switching function for the PWM rectifier according to the switching look-up table. A block diagram of the DPC control structure is shown in Figure 1-6.

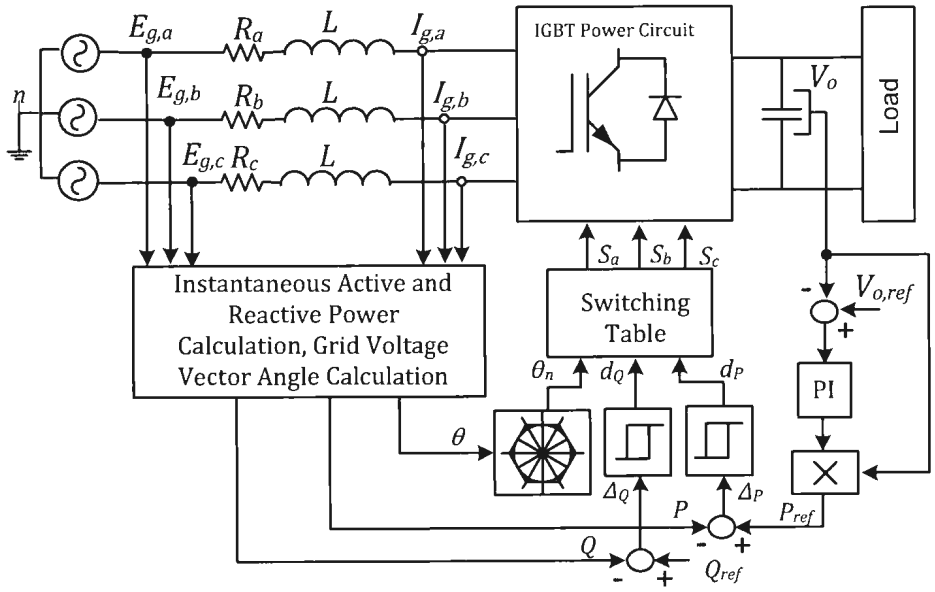


Figure 1-6: Block diagram of Direct Power Control (DPC)

The accurate and fast estimation of the active and reactive power is highly required in DPC to achieve satisfactory performances. This is because inaccurate power estimation results in an incorrect selection of voltage vectors. Based on the measured grid voltages and currents, the power estimation can be performed either based on three phase quantities such as [31]:

$$P = E_{g,a} I_{g,a} + E_{g,b} I_{g,b} + E_{g,c} I_{g,c} \tag{1.4}$$

$$Q = \frac{1}{\sqrt{3}}\left[\left(E_{g,a} - E_{g,b}\right)I_{g,c} + \left(E_{g,b} - E_{g,c}\right)I_{g,a} + \left(E_{g,c} - E_{g,a}\right)I_{g,b}\right] \quad (1.5)$$

or using stationary $\alpha\beta$-coordinates:

$$P = E_{g,\alpha}I_{g,\alpha} + E_{g,\beta}I_{g,\beta} \quad (1.6)$$

$$Q = E_{g,\beta}I_{g,\alpha} - E_{g,\alpha}I_{g,\beta} \quad (1.7)$$

The DPC method excludes the necessity of synchronous reference frame transformation thus reducing the computational effort of the digital microprocessor. Besides less computational burden, a simple implementation and extremely fast dynamic response are frequently mentioned in the literature as the main advantages of DPC. However, the DPC requires high sampling frequency to obtain satisfactory performances. In addition, the required number of sensors will increase since grid voltages and currents have to be measured to calculate input active and reactive powers given in equations (1.6) and (1.7). A large number of sensors will increase the cost and reduce the reliability of the system.

Noguchi et al. [22] propose the use of a grid voltage vector estimation method in order to estimate the power and at the same time reduce the total number of implemented sensors by eliminating the grid voltage sensors. The grid three phase voltage is estimated by adding the voltage across the line filter inductors to the rectifier pole voltage and then calculating the active and reactive powers from equations (1.4) and (1.5), respectively. Thus, the instantaneous values of active and reactive powers are estimated by the new equations given by:

$$P = L\left(\frac{dI_{g,a}}{dt}I_{g,a} + \frac{dI_{g,b}}{dt}I_{g,b} + \frac{dI_{g,c}}{dt}I_{g,c}\right) + V_{dc}\left(S_a I_{g,a} + S_b I_{g,b} + S_c I_{g,c}\right) \tag{1.8}$$

$$Q = \frac{1}{\sqrt{3}}\left\{3L\left(\frac{dI_{g,a}}{dt}I_{g,c} - \frac{dI_{g,c}}{dt}I_{g,a}\right) - V_{dc}\left[S_a\left(I_{g,b} - I_{g,c}\right) + S_b\left(I_{g,c} - I_{g,a}\right) + S_c\left(I_{g,a} - I_{g,b}\right)\right]\right\} \tag{1.9}$$

The first part of both equations represents the power in the line filter inductors and the last part corresponds to the power of the PWM rectifier.

The digital implementation of equations (1.8) and (1.9) has some drawbacks. If the calculation was made at the moment of switching devices changing their switching states, large errors in the calculation of both active and reactive power will occur due to the current ripples. Therefore, the calculation of the differential current expression of equations (1.8) and (1.9) should be avoided at the moment of the switching transition. Moreover, it is essential to reduce the line current ripples by employing relatively large filter inductance and performing the calculation of the current differential with very high sampling frequency which is above the average switching frequency of the PWM rectifier in order to reduce the level of distortion in the converter system.

A power estimation method based on the concept of the virtual flux is introduced in [23]. The power estimation is much simpler since no differential operations are involved. Subsequently a lower sampling frequency can be used by the controller. The key element of the virtual flux based control is the estimation of the grid and converter virtual flux. Because of an inherent relationship between the

stator flux estimation in machine drives application particularly in DTC and the converter virtual flux estimation in DPC, the ideal integrator that is used to calculate the converter virtual flux might generate problems, such as the integration drift and initial condition problems [32-34]. Therefore, a low-pass filter normally replaces the pure integrator. However, a simple low-pass filter reduces the controller system performance because it produces errors in phase and magnitude of the estimated virtual flux components.

The converter average switching frequency is directly related to the upper and lower bands of the hysteresis controllers. The rate of change of active and reactive power flowing via the ac-dc converter system depends on the operating conditions such as grid voltage and frequency, line filter inductance, switching look-up table design and magnitude of dc-link voltage. Consequently, the DPC method utilizing hysteresis controllers produces variable switching frequency which results in unpredictable and wide spread harmonic of the line current. Thus, the maximum capabilities of the rectifier are not fully utilized. These weaknesses can be eliminated by replacing the hysteresis comparators and the switching table by PI controllers and a space vector modulation (SVM) approach, as proposed in [35]. The approach which is named as SVM-DPC produces fixed switching frequency and good steady state performance, however its performance might degrade during transient operation and grid voltage disturbance since no decoupling network and feed-forward components are introduced in the SVM-DPC scheme.

1.2.4 Variation of Control Techniques

Many other control techniques have been presented in the literature due to the availability and continuous development of powerful and fast microprocessors. The control techniques include the use of predictive control scheme [36-37] and fuzzy logic-based control [38-39]. Increases in the complexity of the converter control implementation diminish the uncomplicated control structure in the previous mentioned control schemes particularly the DPC which operates without an inner current controller and pulse width modulator.

The ac-dc converter is sometimes required to operate under unbalanced grid supply. Unbalanced three phase input supplies are quite common in power systems, particularly in a weak ac system. This is a phenomenon appearing in a three phase system, in which the root mean square (RMS) of the phase voltages or the phase angle between consecutive phases is not equal in magnitude. Unevenly distributed single phase load, particularly the fluorescent lighting load in a large scale building can cause unbalanced operating conditions. Short-circuit faults in different points of the power system, and nonsymmetrical transformer windings in a distribution network can also create an unbalanced supply voltage. Although faults in the utility line tend to last for a relatively short duration of time, they might bring in serious unbalanced operating conditions and degrade the converter control system performance [40].

An investigation of ac-dc converter under unbalanced input voltage conditions is presented in reference [41]. The mathematical analysis shows that the input

voltage imbalance generates low frequency harmonic components in the input and output currents of the ac-dc converter. The unbalanced ac input current generates even harmonic components in the order of 2, 4, 8, and so on in the dc output current as well as the dc output voltage. Consequently, the dc-link voltage oscillation provokes low order harmonics in the current injected back into the grid. The interaction between the harmonic components of the dc output voltage and the converter pole voltage creates odd harmonic components in the input ac current [42]. Consequently, these harmonic components will increase the total harmonic distortion (THD) of the ac input current significantly.

The second order harmonic is of more concern since it has a significant impact in determining the size and rating of the output capacitor. This is because the second order harmonic has relatively large amplitude that will increase the dc-link ripple voltage and current which, in turn, increase the size and rating of the dc-link capacitor required to maintain the dc ripples within acceptable limits.

A general model of the ac-dc converter for compensating the effects of unbalanced network is given in reference [43]. The second order harmonic of the dc-link output voltage is minimized by controlling the negative-sequence current along with the positive-sequence current in the positive synchronous reference frame (SRF). A negative-sequence current appears as a 120 Hz ac component (for a 60Hz grid system) in the positive SRF. This implies that both the reference currents and the measured currents consist of 120Hz ac components in the positive SRF. The control bandwidth therefore, needs to be large enough to accommodate the 120 Hz

current command. Due to the physical limitation in hardware implementation such as digital sampling time, time delay and converter switching frequency, a high gain of the current controller may cause instability, and thus the current bandwidth cannot be simply extended. In addition, if the current control loops bandwidth is larger than 120 Hz, a significant amount of phase delay at 120Hz results in unsatisfactory tracking capability.

In references [44] and [45], a method to reduce the level of current harmonics that are injected into the grid or supplied to the load for active filter and uninterruptible power supply (UPS) applications is proposed. The method employs the transformation of the selected harmonic components into their own individual synchronous reference frame. As a result, these components will appear as dc quantities in their own reference frame, and consequently, the PI controller is sufficient to produce a zero-state error. Subsequently, the selected harmonic components can be controlled individually by the proposed control method.

In case of reducing the harmonics from heavily distorted current, a multi-resonant current control (MRCC) method is applicable [46],[47]. An MRCC method consists of several resonant controllers with each of them tuned to a particular harmonic frequency, which results in a zero steady-state error for each frequency. However, these controllers require computationally complex operations.

In conclusion, the non-ideal conditions such as unbalanced, distorted and disturbed three phase grid voltage supply have negative impacts to the performance and size of ac-dc converter system. The increasing magnitude of low order harmonic

components in the input and output sides of the converter necessitates the use of a larger input filter inductor and output filter capacitor to reduce the odd and even order harmonics at the ac input and dc output sides, respectively. As a result, the controls of an ac-dc converter need additional investigation to mitigate those negative impacts during voltage unbalance and disturbance conditions. In the mean time, the implementation of the particular control scheme is able to reduce the total cost of ac-dc converter system without sacrificing the converter performances.

1.3 Thesis Objectives and Organization of the Thesis

The objective of this thesis is to propose and improve the new control techniques for grid connected front-end three phase ac-dc converters with a reduced number of sensors, while preserving the features and abilities of high performance front-end ac-dc converters. Two control methods are extensively studied, analyzed and modified to achieve this objective. The direct power control (DPC) and the voltage oriented control (VOC) are adapted from direct torque control (DTC) and field oriented control (FOC) of the induction machine. The use of input ac voltage sensors to determine the grid voltage vector angle for synchronization and estimate the input instantaneous power is avoided by applying a virtual flux concept in the control schemes.

This thesis consists of six chapters and is organized as follows:

Chapter1 is the introduction of the thesis. Main problems of line-commutated rectifiers are highlighted. A technology overview of the front-end ac-dc converter is given, including a literature review of the control methods on bidirectional PWM ac-dc converters under balanced and unbalanced operating conditions. Finally, the thesis objectives and contributions are also presented in this chapter.

Chapter 2 discusses in detail the topology and working principles of the bidirectional PWM ac-dc converter used in this work. Derivations of the ac-dc converter mathematical models in three types of reference frames, namely *abc*, stationary and rotating synchronous reference frames are discussed in detail.

Chapter 3 presents the development and implementation of the proposed Virtual Flux Direct Power Control (VFDPC) method for the PWM ac-dc converter. An improved virtual flux estimation technique and a systematic approach in developing a new switching look-up table for the VFDPC are explained and discussed in detail. Simulation and hardware implementation results under balanced and non-ideal grid conditions are also presented in this chapter. The theoretical arguments and simulation results are verified and confirmed with the experimental results.

Chapter 4 proposed another new control technique which is able to produce a fixed switching frequency with good control performance both in steady state and transient conditions. The control technique namely, Virtual Flux Oriented Control (VFOC) is developed by adapting the knowledge behind the VFDPC and Voltage Oriented Control (VOC) techniques. Simulation and experimental results, under

balanced and non-ideal grid conditions are presented in this chapter. Moreover, the steady state and dynamic performances of the proposed VFOC are also verified and evaluated.

Chapter 5 describes the development of experimental set-up including a hardware prototype of the PWM ac-dc converter used in the study. The main components of the experimental set-up, which centered around the TMS320F240 Digital Signal Processor (DSP), are presented and described.

Chapter 6 summarizes the work presented in this thesis and addresses the major contributions of this research work. Possible directions of further research on this work are also suggested.

Chapter 2

Three Phase Bidirectional Pulse Width Modulation AC-DC Converter – Topology, Operation and Mathematical Models

2.1 Introduction of the Three Phase Pulse Width Modulation AC-DC Converter

Three phase pulse width modulation (PWM) voltage source ac-dc converters or voltage source rectifiers (VSRs) are increasingly attractive in utility-interfaced applications such as high performance electrical machine adjustable speed drives, active filter and uninterruptible power supply due to the following advantages. The ac-dc converter provides low harmonic content in line currents which leads to the achievement of almost sinusoidal input currents, controllable power factor, adjustable dc-link voltage, regeneration capability, and excellent steady state and dynamic performance. The converter must be controlled properly in order to achieve proper power flow regulation in the power conversion system. A deep understanding of the converter system operation and characteristics is required for developing the converter mathematical model and designing the control system. This chapter introduces and presents a topology, basic operation and mathematical model of the PWM ac-dc converter in different reference frames.

2.2 Topology and Operation of the Three Phase Pulse Width Modulation AC-DC Converter

The topology of the three phase voltage source bidirectional ac-dc converter is shown in Figure 2-1.

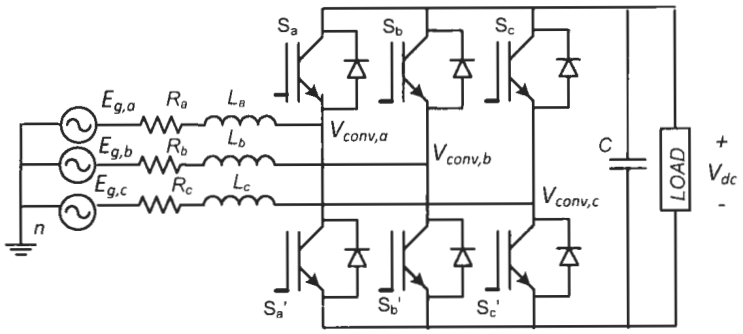
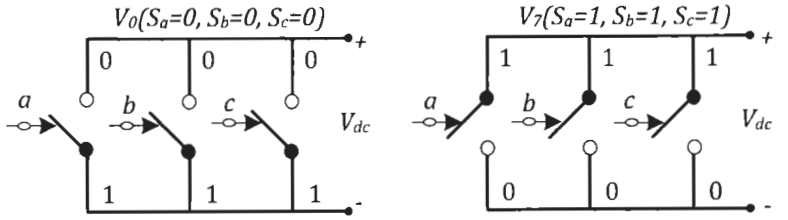


Figure 2-1: Topology of the three-phase bidirectional ac-dc voltage source ac-dc converter

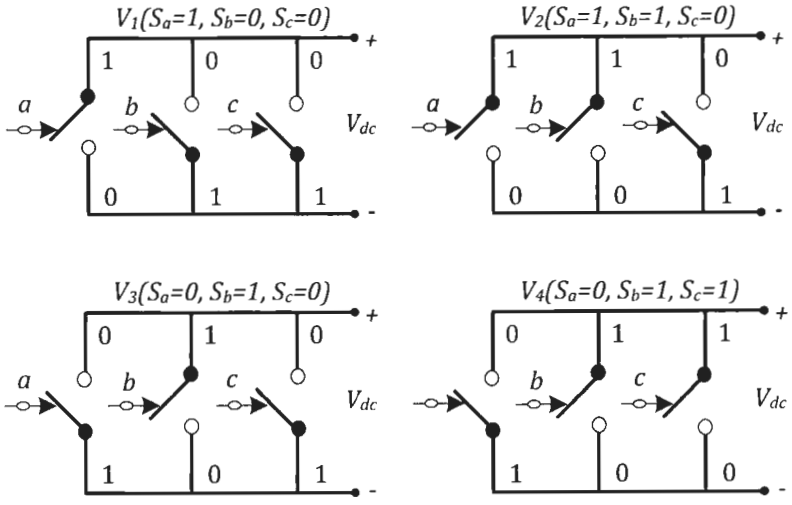
The converter is connected to the three phase power supply via an inductor L and internal resistance R for each phase. The three phase voltage supply is denoted by $E_{g,a}$, $E_{g,b}$ and $E_{g,c}$. Three identical line inductors indicated by L_a, L_b, and L_c act as line filters for smoothing the line currents with minimum ripples. Each inductor has an internal resistance which is denoted by R_a, R_b, and R_c. A part of reducing the total harmonic distortion (THD) of the line currents, the inductors also provide the boost feature of the converter. Six insulated gate bipolar transistors (IGBTs) with anti-parallel fast recovery diodes, are used as the converter bidirectional switches. The IGBT switches have features of high power rating, simple gate drive requirement and suitablity for high frequency applications. The IGBT is "on" when the gate signal is "1" and "off" when the gate signal is "0". Both transistors in the same leg cannot be

turned "on" at the same time to avoid shoot-through fault current flowing in that particular leg. Three legs, with each leg consisting of two identical IGBTs, can produce 64 possible converter switching states. However, only 8 switching states are used to operate the converter. This is due to the fact that both transistors in the same leg cannot be turned "on" at the same time. Six switching states produce active vectors and another two switching states produce zero vectors. Figure 2-2 shows the eight permitted switching states configuration for the converter.

a) Zero vectors:



b) Active vectors



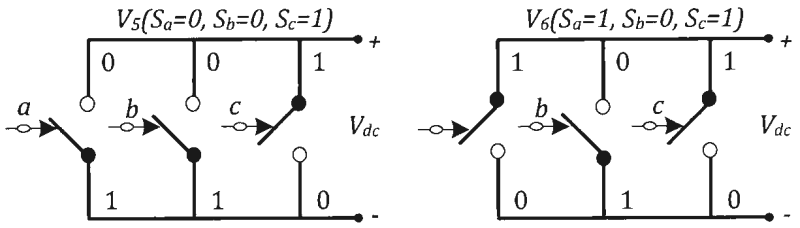


Figure 2-2: Switching states of three phase PWM ac-dc converter

The output of the three phase PWM ac-dc converter is connected to the capacitor bank C and load. This capacitor bank is used to minimize the ripple of the dc output voltage as well as output current. A minimum dc-link voltage is required for proper operation of the rectifier. The dc-link voltage must be able to keep the anti-parallel diodes across IGBTs blocked. Therefore, the dc-link output voltage has to be always higher than the peak of dc voltage generated by the conventional three phase diode rectifier. Generally, the average value of dc output voltage of the three phase diode rectifier can be calculated by equation (2.1) [48]. It should be noted that this equation does not take into account any voltage drops across the line inductors and the diodes.

$$V_{dc} \approx 1.35 E_{LL(rms)} \tag{2.1}$$

Subsequently, the minimum dc-link voltage $V_{dc\,min}$ should be selected so that it fulfills the requirement of equation (2.2).

$$V_{dc\,min} > 1.35 E_{LL(rms)} = 1.35 \times \sqrt{3} E_{Phase(rms)} \tag{2.2}$$

The basic operation of the PWM rectifier in steady-state can be understood by analyzing a single-phase representation of the rectifier circuit as shown in Figure

2-3. L and R represent the line inductor and its internal resistance respectively at phase a. $\bar{E}_{g,an}$ is the grid phase voltage vector and $\bar{V}_{conv,an}$ is the converter pole voltage vector. The magnitude of $\bar{V}_{conv,an}$ is controllable and depends on the modulation index of the switching strategy, the dc-link voltage level and the switching states of the converter.

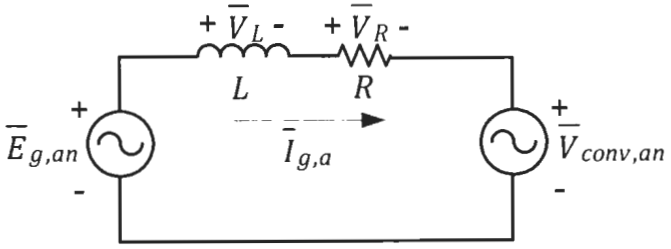


Figure 2-3: Per-phase equivalent circuit for the three phase PWM rectifier

The voltage vector equation in steady-state with the supply voltage as a reference can be written as:

$$\bar{E}_{g,an} = \bar{V}_{conv,an} + \bar{V}_L + \bar{V}_R \tag{2.3}$$

$$\bar{E}_{g,an} = \bar{V}_{conv,an} + j\bar{I}_{g,a}\omega L + \bar{I}_{g,a}R \tag{2.4}$$

where

$$\bar{E}_{g,an} = E_{g,an}\angle 0^{\circ};\ \bar{V}_{conv,an} = V_{conv,an}\angle -\delta;\ \bar{I}_{g,a} = I_{g,a}\angle \emptyset \tag{2.5}$$

Therefore the total power transfer equation between the ac side and the dc load side in steady-state can be written as:

$$\begin{aligned} P_{ac} &= 3 \times Re\{\bar{E}_{g,an}\bar{I}^{*}_{g,a}\} \\ &= 3 \times Re\left\{E_{g,an}\angle 0^{\circ}\left(\frac{E_{g,an}\angle 0^{\circ} - V_{conv,an}\angle -\delta}{Z\angle\gamma}\right)^{*}\right\} \end{aligned} \tag{2.6}$$

where

$$Z\angle\gamma = R + j\omega L \tag{2.7}$$

Subsequently, equation (2.6) can be extended to

$$P_{ac} = 3\left(\frac{\left|E_{g,an}^2\right|}{|Z|}cos(\gamma) - \frac{|E_{g,an}||V_{conv,an}|}{|Z|}cos(\delta + \gamma)\right) \tag{2.8}$$

By considering the line resistance to be much smaller than the inductive impedance ($R \ll \omega L$), the R can be neglected. Therefore, if an angle of the inductive impedance γ is approximately 90°, the power transfer equation of (2.8) can be simplified and written as:

$$P_{ac} = \frac{3|E_{g,an}||V_{conv,an}|sin(\delta)}{\omega L} = V_{dc}I_{dc} \tag{2.9}$$

Equations (2.8) and (2.9) show that by maintaining a certain magnitude of the converter pole voltage $V_{conv,an}$ and its phase shift angle δ relative to the ac supply voltage vector angle, the power flow can be maintained in order to produce the desired output dc voltage and the line current at the preferred power factor. In this way, the phase and amplitude of the line current can be controlled indirectly by controlling the phase angle and amplitude of the converter voltage $V_{conv,an}$. The average value and direction of the dc output current I_{dc} is subject to control which is proportional to the active power conducted through the converter. The reactive power can be controlled independently by shifting the fundamental component of grid line current $I_{g,a}$ with respect to the grid phase voltage $E_{g,a}$.

Figure 2-4 presents the converter general phasor diagram for both rectification and regeneration modes when unity power factor is required. The rectification mode is obtained when the converter operates as a rectifier, meanwhile the converter works as an inverter during the regeneration mode. The figure shows that the converter voltage vector $\bar{V}_{conv,an}$ is slightly higher during regeneration which is normally up to 3% higher than during the rectification mode [49].

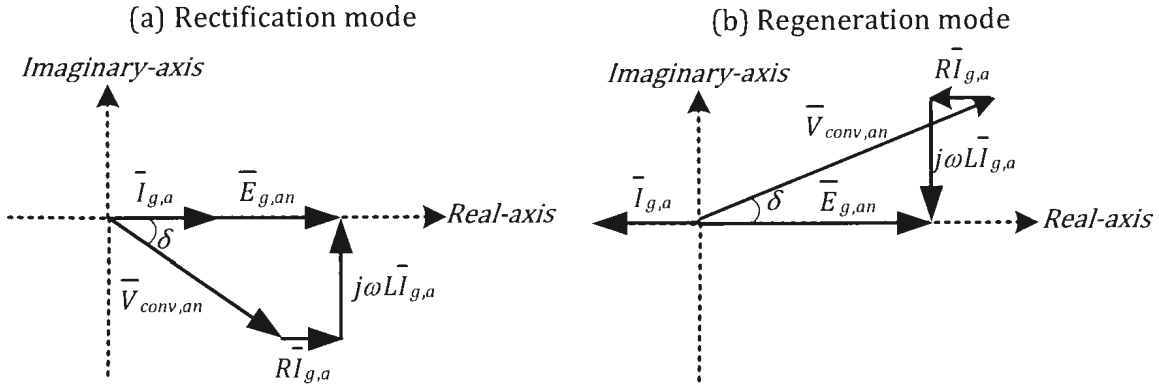


Figure 2-4: General phasor diagram for the voltage source converter during different operating conditions:
a) Rectification at unity power factor b) Regeneration at unity power factor

2.3 Mathematical Model of PWM AC-DC Converter under Balanced Operating Conditions

Mathematical models of the three phase PWM rectifier can be used to perform and simplify the analysis on the rectifier control system. The mathematical models of the ac-dc voltage source converter in stationary and synchronous reference frames are presented in [19]. In general, the models of the PWM rectifier can be divided into three reference coordinates or reference frames which are; natural or *abc*-reference frame, stationary $\alpha\beta$-reference frame and synchronously rotating *dq*-reference frame. All models are developed by assuming that the rectifier is operating under a balanced three phase three-wire system, and the power switches are ideal. The three phase voltage source and line currents for a balanced three phase, three-wire system can be written as:

$$E_{g,an} = E_m cos(\omega t) \tag{2.10}$$

$$E_{bn} = E_m cos\left(\omega t - \frac{2\pi}{3}\right) \tag{2.11}$$

$$E_{g,cn} = E_m cos\left(\omega t + \frac{2\pi}{3}\right) \tag{2.12}$$

$$I_{g,a} = I_m cos(\omega t) \tag{2.13}$$

$$I_{g,b} = I_m cos\left(\omega t - \frac{2\pi}{3}\right) \tag{2.14}$$

$$I_{g,c} = I_m cos\left(\omega t + \frac{2\pi}{3}\right) \tag{2.15}$$

where E_m, I_m and ω represent amplitude of the phase voltage, line current and voltage angular frequency, respectively with assumption that the total of the line currents is zero:

$$I_{g,a} + I_{g,b} + I_{g,c} = 0 \tag{1.16}$$

Equations in (2.10)-(2.15) can be transformed to the $\alpha\beta$-reference frame and the dq-reference frame by using the transformation matrix equations given in (2.17) and (2.18) respectively.

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{2.17}$$

$$\begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos(\theta) & cos\left(\theta - \frac{2\pi}{3}\right) & cos\left(\theta + \frac{2\pi}{3}\right) \\ -sin(\theta) & -sin\left(\theta - \frac{2\pi}{3}\right) & -sin\left(\theta + \frac{2\pi}{3}\right) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{2.18}$$

The stationary $\alpha\beta$ components can be transformed into the stationary abc-reference frame components by using:

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -1/2 & \sqrt{3}/2 & 1 \\ -1/2 & -\sqrt{3}/2 & 1 \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} \tag{2.19}$$

Subsequently, the rotating dq components can be also transformed into the stationary abc-reference frame components by the transformation matrix equation shown in equation (2.20):

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} cos(\theta) & -sin(\theta) & 1 \\ cos\left(\theta - \frac{2\pi}{3}\right) & -sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ cos\left(\theta + \frac{2\pi}{3}\right) & -sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} \tag{2.20}$$

The relationship between all three reference frames can be clearly understood by referring to the vector diagram as shown in Figure 2-5, where x represents either voltage, current, or flux linkage (in machine applications), and θ is the angular displacement between the a-axis and d-axis of the three phase and two phase reference frame, respectively. The three phase variables, x_a, x_b and x_c are in the fixed or stationary reference frame which does not rotate in space whereas the two phase variables, x_d and x_q are in the synchronous reference frame whose direct (d) and quadrature (q) axes rotate in space at the synchronous speed ω_e. The speed ω_e is the angular electrical speed of the grid supply voltage or the speed of the rotating magnetic field of the motor, given by

$$\omega_e = 2\pi f_e \tag{2.21}$$

where f_e in the frequency of the grid voltage supply. The angle θ can be calculated from

$$\theta(t) = \int_0^t \omega_e(t)dt + \theta_0 \tag{2.22}$$

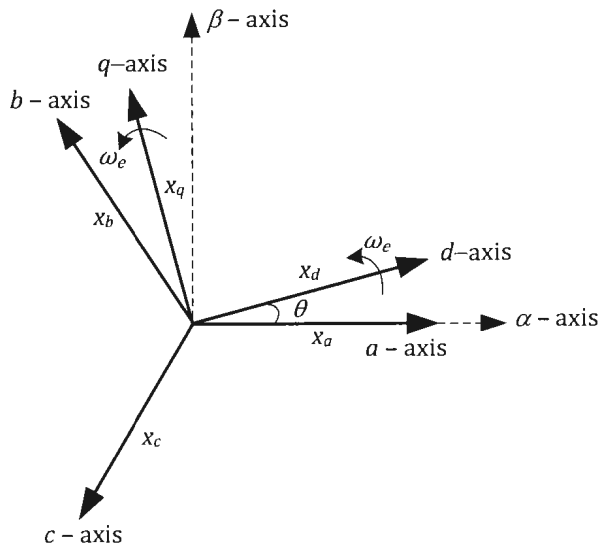


Figure 2-5: Vector diagram showing the relationship between different reference frames

When the rotating speed ω_e of the dq-axis reference frame is set to zero, the direct d-axis and quadrature q-axis will coincide with the α-axis and β-axis of the stationary $\alpha\beta$-reference frame, respectively. Consequently, the dq-axis becomes stationary in space. A transformation of the three phase variables to the two phase variables in the stationary $\alpha\beta$-reference frame can be obtained by setting θ in equation (2.18) to zero.

Figure 2-6 illustrates a general vector diagram of the grid supply voltage and the line current for the three phase VSR. The line current vector $\bar{I}_{g,dq}$ is in the dq-axis synchronous reference frame. Assuming that $\bar{I}_{g,dq}$ rotates at the same speed as that of the dq-axis frame, the line current angle $\emptyset$, which is the angle between $\bar{I}_{g,dq}$ and the d-axis, is constant. The resultant dq-axis current components, denoted by $I_{g,d}$

and $I_{g,q}$, are of dc signals. Therefore, the transformation of *abc*-reference frame to *dq*-reference frame can be utilized to simplify the simulation, controller design, and digital implementation of an ac-dc converter system, where a three phase ac signal is represented by a two phase dc signal.

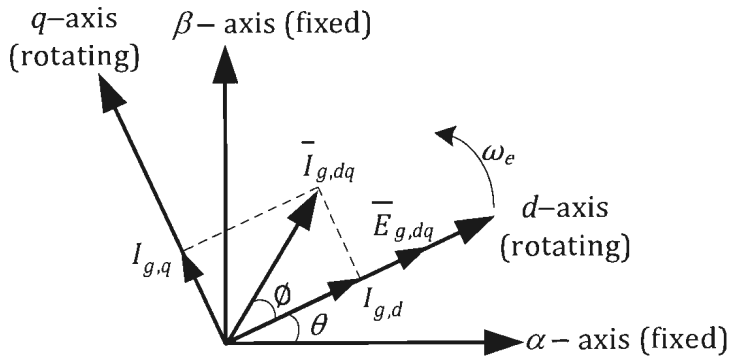


Figure 2-6: Vector diagram of three phase voltage source rectifier

A PWM rectifier is normally employed to produce unity power factor operation. The unity power factor (UPF) condition is achieved when the grid line current vector $\bar{I}_{g,dq}$, is in phase with the grid voltage vector $\bar{E}_{g,dq}$. Therefore, if the rectifier controller is developed using a grid supply voltage oriented synchronous rotating *dq*-reference frame, the reference value of the quadrature line current $I_{g,q}$ depicted in Figure 2-6 is set to zero to achieve UPF operation.

By using matrix transformation as shown in equation (2.17), the input supply voltage in the $\alpha\beta$-stationary reference frame can be written as:

$$E_{g,\alpha} = E_m cos(\omega t) \tag{2.23}$$

$$E_{g,\beta} = E_m sin(\omega t) \tag{2.24}$$

The input voltage in the dq–synchronous reference frame can be expressed by:

$$E_{g,d} = \sqrt{E_{g,\alpha}^2 + E_{g,\beta}^2} = E_m \tag{2.25}$$

$$E_{g,q} = 0 \tag{2.26}$$

2.3.1 Model of PWM Voltage Source Rectifier in Three Phase *abc*-Coordinates

The voltage equation for a balanced three phase and three-wire system can be written as

$$\bar{E}_{g,abc} = \bar{V}_{R,abc} + \bar{V}_{L,abc} + \bar{V}_{conv,abc} \tag{2.27}$$

where $\bar{E}_{g,abc}$ is the grid supply three phase voltage vector, $\bar{V}_{R,abc}$ is the total voltage drop vector across line resistor and internal resistance of line inductor, $\bar{V}_{L,abc}$ is the line inductor voltage drop vector and $\bar{V}_{conv,abc}$ is the converter pole voltage vector. The line to neutral voltage equation of (2.27) can be represented in a matrix form as shown in (2.28):

$$\begin{bmatrix} E_{g,an} \\ E_{g,bn} \\ E_{g,cn} \end{bmatrix} = R \begin{bmatrix} I_{g,a} \\ I_{g,b} \\ I_{g,c} \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} I_{g,a} \\ I_{g,b} \\ I_{g,c} \end{bmatrix} + \begin{bmatrix} V_{conv,an} \\ V_{conv,bn} \\ V_{conv,cn} \end{bmatrix} \tag{2.28}$$

The phase voltages at the poles of the converter are equal to:

$$V_{conv,an} = sw_a \cdot V_{dc} \tag{2.29}$$

$$V_{conv,bn} = sw_b \cdot V_{dc} \tag{2.30}$$

$$V_{conv,cn} = sw_c \cdot V_{dc} \tag{2.31}$$

where:

$$sw_a = \frac{2S_a - (S_b + S_c)}{3} \tag{2.32}$$

$$sw_b = \frac{2S_b - (S_a + S_c)}{3} \tag{2.33}$$

$$sw_c = \frac{2S_c - (S_a + S_b)}{3} \tag{2.34}$$

$S_{a,b,c}$ are the switching states of the converter and, V_{dc} is the dc-link output voltage. The value of switching coefficients sw_a, sw_b and sw_c are assumed to be 0, $(\pm 1/3)$ or $(\pm 2/3)$, depend on the converter switching states.

The equation (2.27) can be also used to represent the line to line voltage of the ac-dc converter system. Sometimes, it is essential to know the converter pole line to line voltages for the analysis purpose. The line to line voltage at the converter poles can be calculated by using:

$$V_{ab} = (S_a - S_b) \cdot V_{dc} \tag{2.35}$$

$$V_{bc} = (S_b - S_c) \cdot V_{dc} \tag{2.36}$$

$$V_{ca} = (S_c - S_a) \cdot V_{dc} \tag{2.37}$$

Additionally, the current equation of the ac-dc converter can be written as:

$$C\frac{dV_{dc}}{dt} = S_a I_{g,a} + S_b I_{g,b} + S_c I_{g,c} - I_{dc} \tag{2.38}$$

The combination of equations (2.28)-(2.34), and (2.38) can be used to develop a block diagram of the VSR in three phase *abc*-coordinates as shown in Figure 2-7.

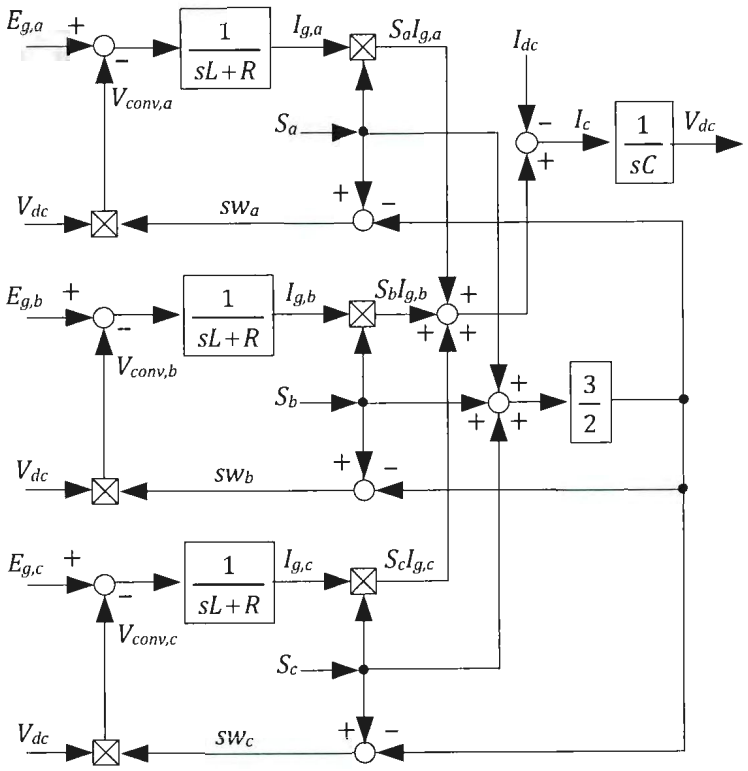


Figure 2-7: Block diagram of the VSR in three-phase *abc*-coordinates

2.3.2 Model of Three Phase PWM Voltage Source Rectifier in Stationary $\alpha\beta$-Reference Frame

In order to simplify the analysis of the converter, it is useful to present the VSR model in a two-axis coordinate system. The voltage and current equations in the stationary $\alpha\beta$-reference frame are obtained by applying a transformation matrix of (2.17) in equations (2.28) and (2.38). After transformation, both equations can be written as:

$$\begin{bmatrix} E_{g,\alpha} \\ E_{g,\beta} \end{bmatrix} = R \begin{bmatrix} I_{g,\alpha} \\ I_{g,\beta} \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} I_{g,\alpha} \\ I_{g,\beta} \end{bmatrix} + \begin{bmatrix} V_{conv,\alpha} \\ V_{conv,\beta} \end{bmatrix} \tag{2.39}$$

and

$$C \frac{dV_{dc}}{dt} = \frac{3}{2}\left(S_\alpha I_{g,\alpha} + S_\beta I_{g,\beta}\right) - I_{dc} \tag{2.40}$$

where:

$$V_{conv,\alpha} = S_\alpha V_{dc} \tag{2.41}$$

$$V_{conv,\beta} = S_\beta V_{dc} \tag{2.42}$$

$$S_\alpha = S_a - \frac{1}{3}(S_a + S_b + S_c)\,;\; S_\beta = \frac{1}{\sqrt{3}}(S_b - S_c) \tag{2.43}$$

Equations (2.39)-(2.43) can be used to develop the ac-dc converter model in the stationary $\alpha\beta$-coordinates as shown in Figure 2-8.

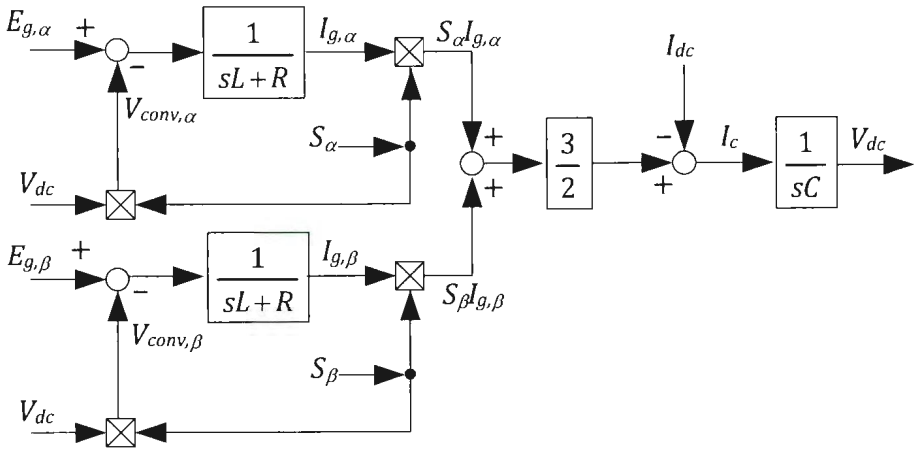


Figure 2-8: Block diagram of the VSR in stationary $\alpha\beta$-reference frame

2.3.3 Model of Three Phase PWM VSR in Synchronously Rotating *dq*-Reference Frame

The model of VSR in *abc*-coordinates can be transformed into the synchronously rotating *dq*-reference frame by using the *abc* to *dq* transformation matrix as shown in (2.18). However, it is possible to obtain the *dq* model of VSR directly from the $\alpha\beta$ model by using the $\alpha\beta$to *dq* transformation matrix given in (2.44).

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{2.44}$$

The model in *dq* coordinates can be changed back to the $\alpha\beta$-coordinates by using the *dq* to $\alpha\beta$transformation matrix shown in (2.45).

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} x_d \\ x_q \end{bmatrix} \tag{2.45}$$

The voltage and current equations for the three phase PWM VSR in the synchronous rotating *dq*-reference frame are given in (2.46)-(2.48):

$$E_{g,d} = Ri_{g,d} + L\frac{di_{g,d}}{dt} - \omega Li_{g,q} + V_{conv,d} \tag{2.46}$$

$$E_{g,q} = Ri_{g,q} + L\frac{di_{g,q}}{dt} + \omega Li_{g,d} + V_{conv,q} \tag{2.47}$$

$$C\frac{dV_{dc}}{dt} = \left(S_d i_{g,d} + S_q i_{g,q}\right) - i_{dc} \tag{2.48}$$

where:

$$V_{conv,d} = S_d V_{dc} \tag{2.49}$$

$$V_{conv,q} = S_q V_{dc} \tag{2.50}$$

$$S_d = S_\alpha cos\omega t + S_\beta sin\omega t\ ;\ S_q = S_\beta cos\omega t - S_\alpha sin\omega t \tag{2.51}$$

Further, based on equations of (2.46)-(2.51), a block diagram of the VSR in *dq*-coordinates can be constructed as shown in Figure 2-9.

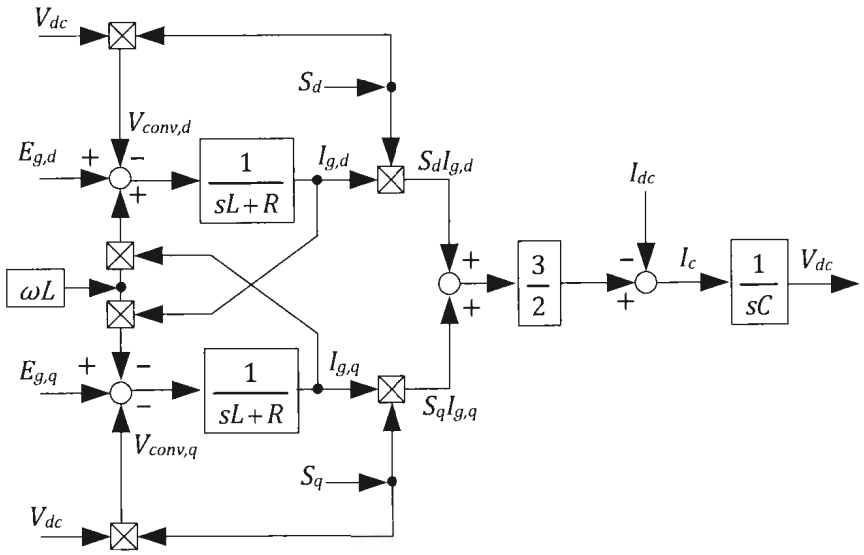


Figure 2-9: Block diagram of the VSR in synchronously rotating *dq*-reference frame

Chapter 3

Development of the Proposed Virtual Flux Direct Power Control for the Three Phase AC-DC Converter

3.1 Introduction to the Direct Power Control Method for the Front-end Three Phase Voltage Source Rectifier

Direct Power Control (DPC) has become an interesting control strategy of grid connected converters due to the advantages of fast dynamic performance and simple control implementation when compared with the other control strategies. The basic idea of DPC is a direct control of instantaneous active and reactive power without any internal current control loop and pulse width modulator. The switching states are selected via a switching look-up table. The switching states are chosen based on the instantaneous error between the estimated and desired active and reactive power. The basic control structure of DPC is shown in Figure 3-1.

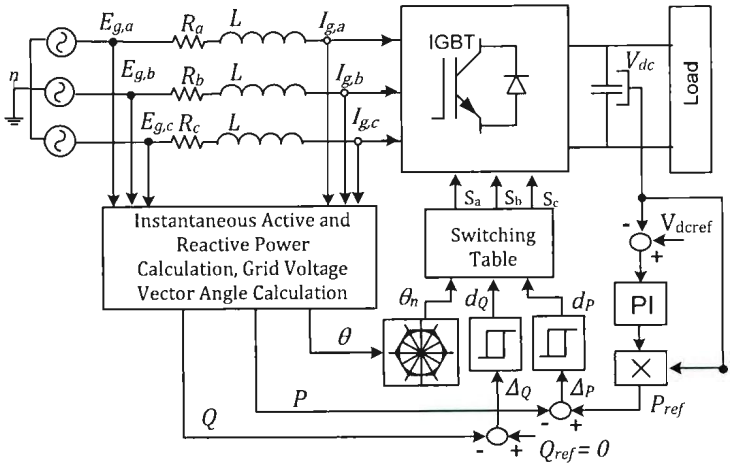


Figure 3-1: Block diagram of the Direct Power Control

In general, the conventional DPC requires three types of sensors such as three current sensors to measure three phase input currents, three voltage sensors to measure three phase input voltages and a dc voltage sensor to measure the dc-link output voltage. The employment all of these sensors will cause the converter system to be bulky and expensive. In addition, the sensing signal is usually subject to high frequency noise and interference. Any incidental misreading of a signal caused by a failed sensor may decrease the system reliability and performance. Therefore, it is desirable to reduce the number of sensors to the minimum possible.

In reference [22], the authors eliminate the employment of ac input voltage sensors by estimating the three phase supply voltage through the computation of the time derivative of measured currents. The authors combined the input voltage source estimation method with the DPC strategy to operate the three phase ac-dc converter. The accurate and fast estimation of the active and reactive power is required in the DPC scheme to achieve satisfactory performance. The computation of the time derivative of the measured current may become noisy, especially if the calculation was made at the instant of power semiconductor devices changing their switching states. As a result, large errors in the calculation of both instantaneous active and reactive power may occur.

A virtual flux control concept is introduced in [23] to estimate both the three phase grid voltage and the input instantaneous active and reactive powers. The estimation procedures are much more reliable, since no differential operations are

involved. Subsequently, a lower sampling frequency can be used during real-time implementation. The authors combine the grid virtual flux control concept with the DPC scheme to operate the ac-dc converter. The key to a successful operation of the DPC utilizing a virtual flux control is dependent on the effectiveness of the virtual flux estimation procedure and the selection of the converter switching states. However, no further explanation is given by the authors regarding the development of any switching look-up table.

This chapter discusses a development of an improved virtual flux direct power control (VFDPC) for a three phase grid connected ac-dc converter. A systematic approach to the development of a new switching look-up table for the virtual flux control is explained in detail. The new switching look-up table is obtained by differentiating the active and reactive power equations. Thus, the switching table is able to choose the best converter voltage vector in order to ensure smooth control of the instantaneous active and reactive powers. Simulation results which are verified by the experimental results are presented to evaluate the new switching look-up table. Furthermore, this chapter introduces a method to compensate the magnitude and phase errors of the virtual flux estimation procedure, which is done by a low-pass filter. Those errors are undesirable since they can generate an incorrect selection of the voltage vectors from the switching look-up table. The performance of the proposed VFDPC utilizing the new switching table is also evaluated for an unbalanced grid supply voltage. A phase locked loop (PLL) is introduced in the VFDPC scheme to mitigate negative impacts on the converter performance during

the unbalanced voltage conditions. The control structure of the proposed virtual flux direct power control (VFDPC) is shown in Figure 3-2.

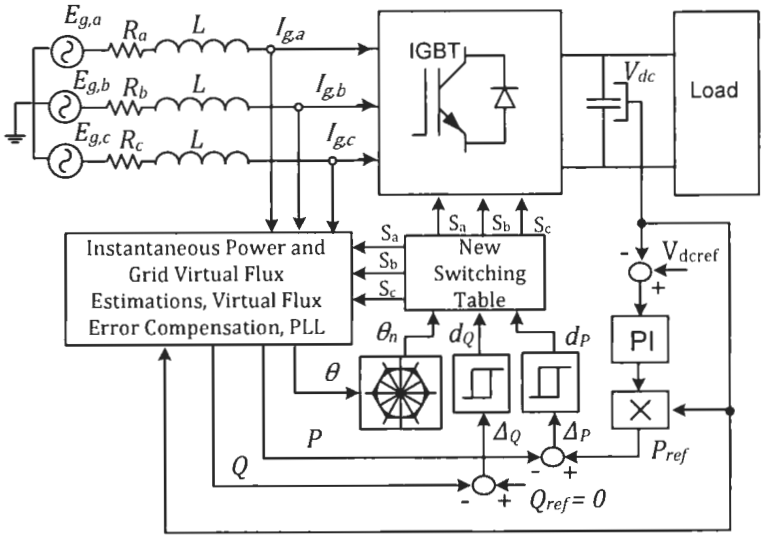


Figure 3-2: Block diagram of the proposed Virtual Flux Direct Power Control

The VFDPC proposed in this thesis is based on the estimation of the three phase grid virtual flux. The estimation of grid virtual flux is made by assuming that both the utility grid and the converter line filters as illustrated in Figure 3-3 behave as a virtual ac machine [23, 50]. Therefore, the internal resistance and the inductance of the line filter inductors are equivalent to the stator winding resistance and stator leakage inductance of the virtual ac machine, respectively. Meanwhile, the grid supply voltage would be induced by a virtual air gap flux in the virtual ac machine. Several advantages can be obtained by applying the virtual flux control in controlling the rectifier. The advantage of this approach is that the developed control system is less sensitive to line voltage harmonics because of a low-pass filter

characteristic introduced by the virtual flux estimation procedure. The other benefit of using a virtual flux control is the absence of ac voltage sensors to detect the grid voltages, so that the whole system cost and size of the converter can be reduced.

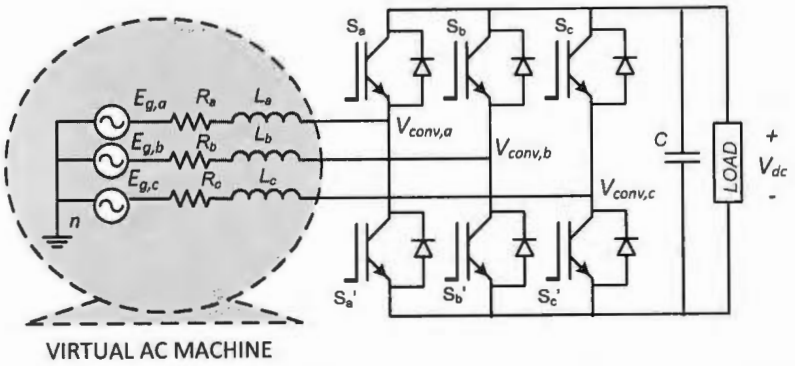


Figure 3-3: Three phase AC-DC converter with the AC side presented as a virtual AC machine

3.2 Method of the Grid Virtual Flux Estimation

The grid virtual flux vector in a three phase *abc*-reference frame $\bar{\Psi}_{g,abc}$ is defined as an integration of the grid voltage vector $\bar{E}_{g,abc}$, and can be written as:

$$\bar{\Psi}_{g,abc} = \int \bar{E}_{g,abc}\, dt \tag{3.1}$$

The grid three phase supply voltage can be calculated by using equation:

$$\begin{bmatrix} E_{g,an} \\ E_{g,bn} \\ E_{g,cn} \end{bmatrix} = R \begin{bmatrix} I_{g,a} \\ I_{g,b} \\ I_{g,c} \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} I_{g,a} \\ I_{g,b} \\ I_{g,c} \end{bmatrix} + \begin{bmatrix} V_{conv,an} \\ V_{conv,bn} \\ V_{conv,cn} \end{bmatrix} \tag{3.2}$$

Therefore, by applying the virtual flux definition of equation (3.1) to the voltage loop equation of (3.2), the grid flux can be estimated as shown in

$$\overline{\Psi}_{g,abc} = \int (\bar{V}_{conv,abc} + R\bar{I}_{g,abc})dt + L\bar{I}_{g,abc} \tag{3.3}$$

where $\bar{V}_{conv,abc}$ and $\bar{I}_{g,abc}$ present the converter pole voltage vector and the line current vector, respectively in the three phase *abc*-reference frame. The virtual flux vector $\overline{\Psi}_{g,abc}$ can be further described as:

$$\overline{\Psi}_{g,abc} = \begin{bmatrix} \Psi_{g,an} \\ \Psi_{g,bn} \\ \Psi_{g,cn} \end{bmatrix} = \int \bar{E}_{g,abc}\, dt = \begin{bmatrix} \int E_{g,an}\, dt \\ \int E_{g,bn}\, dt \\ \int E_{g,cn}\, dt \end{bmatrix} \tag{3.4}$$

In practice, the value of internal reactor resistance R can be neglected since its value is much smaller than the value of the line reactor impedance. Moreover, the power dissipated in the internal resistance is much lower than the active power associated with a load at the converter output dc bus. Hence, the virtual flux equation of (3.3) can be simplified as:

$$\overline{\Psi}_{g,abc} = \int \bar{V}_{conv,abc}\, dt + L\bar{I}_{g,abc} = \overline{\Psi}_{conv,abc} + L\bar{I}_{g,abc} \tag{3.5}$$

The proposed VFDPC works by utilizing a stationary $\alpha\beta$-reference frame. Therefore, it is necessary to develop the virtual flux estimator in the stationary reference frame. The grid virtual flux vector in the stationary $\alpha\beta$-reference frame $\overline{\Psi}_{g,\alpha\beta}$ is defined as the integration of the grid supply voltage vector $\bar{E}_{g,\alpha\beta}$ as shown in equations (3.6) and (3.7).

$$\overline{\Psi}_{g,\alpha\beta} = \int \bar{E}_{g,\alpha\beta}\, dt \tag{3.6}$$

$$\overline{\Psi}_{g,\alpha\beta} = \int \bar{V}_{conv,\alpha\beta}\, dt + L\bar{I}_{g,\alpha\beta} = \overline{\Psi}_{conv,\alpha\beta} + L\bar{I}_{g,\alpha\beta} \tag{3.7}$$

Subsequently, the grid virtual flux vector in equation (3.7) can be further expanded to acquire the grid virtual flux components in both real and complex of $\alpha\beta$-axes such as:

$$\Psi_{g,\alpha} = \int E_{g,\alpha} dt = \int V_{conv,\alpha} dt + LI_{g,\alpha} = \Psi_{conv,\alpha} + LI_{g,\alpha} \tag{3.8}$$

$$\Psi_{g,\beta} = \int E_{g,\beta} dt = \int V_{conv,\beta} dt + LI_{\beta,g} = \Psi_{conv,\beta} + LI_{g,\beta} \tag{3.9}$$

The converter pole voltage in the $\alpha\beta$-frame, denoted by $V_{conv,\alpha\beta}$, can be derived from the measured dc-link voltage V_{dc} and the converter switching states $S_{\alpha\beta}$ as shown in equations (3.10) and (3.11):

$$V_{conv,\alpha} = S_\alpha V_{dc} = \left(S_a - \frac{1}{3}(S_a + S_b + S_c)\right) V_{dc} = \frac{V_{dc}}{3}(2S_a - S_b - S_c) \tag{3.10}$$

$$V_{conv,\beta} = S_\beta V_{dc} = \frac{V_{dc}}{\sqrt{3}}(S_b - S_c) \tag{3.11}$$

The relationship between the grid supply voltage and the grid virtual flux quantities can be understood by representing those quantities in the dq-synchronous rotating reference frame as illustrated in Figure 3-4. Due to the integration characteristic of the virtual flux components, the grid virtual flux vector $\overline{\Psi}_{g,dq}$ is lagging the grid voltage vector $\bar{E}_{g,dq}$ by ninety degrees (90°). Since the virtual flux concept is based on the machine theory, the direct d-axis is aligned to the grid virtual flux vector $\overline{\Psi}_{g,dq}$, and the grid voltage vector $\bar{E}_{g,dq}$ is aligned to the orthogonal quadrature q-axis as shown in Figure 3-4. The magnitude of grid virtual

flux in d-axis $\Psi_{g,d}$ is equal to the magnitude of virtual flux vector $\overline{\Psi}_{g,dq}$. Besides, the magnitude of virtual flux in q-axis $\Psi_{g,q}$ is equal to zero for a balanced three phase supply voltage. On the other hand, the magnitude of the grid supply voltage in the q-axis $E_{g,q}$ is equal to the magnitude of the grid voltage vector $\bar{E}_{g,dq}$, meanwhile, the magnitude of the grid voltage in the d-axis $E_{g,d}$ is equal to zero.

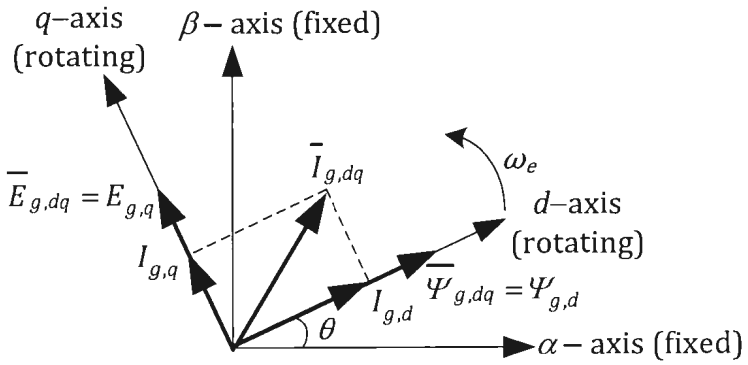


Figure 3-4: Phasor diagram showing the relationship between the grid supply voltage and virtual flux quantities

The ideal integration that is used to calculate the grid virtual flux as shown in equations (3.8) and (3.9) might saturate due the integration drift caused by either noise or dc offsets present in the sensed current or voltage [33-34, 51]. A simple solution for the drifting problem is to replace the pure integrator with first-order low-pass filter with appropriate cut-off frequency [51]. Therefore, the grid virtual flux estimation in a frequency domain transfer function can be written as:

$$\overline{\Psi}_{g,\alpha\beta} = \overline{\Psi}_{conv,\alpha\beta} + LI_{g,\alpha\beta} = \left(\frac{1}{s+\omega_c}\right)\bar{V}_{conv,\alpha\beta} + L\bar{I}_{g,\alpha\beta} \qquad (3.12)$$

where s is a Laplace transform variable, and ω_c is a cut-off frequency of the low-pass filter. A simple low-pass filter performs well as an integrator for the operating frequencies ω_e higher than the cut-off frequency ω_c ($\omega_e \gg \omega_c$), but at the same time, it will reduce the rectifier system performance since it produces errors in phase and magnitude of the virtual flux estimation components. These errors are undesirable since they can generate an incorrect selection of the voltage vectors from the switching look-up table and hence degrade the performance of Direct Power Control based on virtual flux. In order to minimize these errors, a phase and magnitude compensation method for the stator flux of induction machine as presented in [32] is analyzed and adopted in the virtual flux estimation procedure in this work. The estimation procedure provides a low-pass filter characteristic at all frequencies, except at the operating frequency (grid voltage frequency). Subsequently, the integration drift problem can be avoided while at the same time, good system performance is maintained.

When a pure integrator is used, the virtual converter pole flux vector in the $\alpha\beta$-reference frame $\overline{\Psi}_{conv,\alpha\beta}$ is calculated according to

$$\overline{\Psi}_{conv,\alpha\beta} = \int \bar{V}_{conv,\alpha\beta}\, dt \tag{3.13}$$

Under a sinusoidal steady-state condition, equation (3.13) can be resolved as

$$\overline{\Psi}_{conv,\alpha\beta} = \left(\frac{1}{s}\right)\bar{V}_{conv,\alpha\beta} = \frac{\bar{V}_{conv,\alpha\beta}}{j\omega_e} \tag{3.14}$$

To avoid the integration drift problem due to the dc offsets or the noise of electrical quantities measurement, a low-pass filter is normally used to replace the

pure integrator. If a first order low-pass filter with a cut-off frequency of ω_c is used to substitute the pure integrator, equation (3.14) becomes:

$$\overline{\Psi}'_{conv,\alpha\beta} = \frac{\overline{V}_{conv,\alpha\beta}}{j\omega_e + \omega_c} \tag{3.15}$$

where ω_e is the grid operating frequency, ω_c is the cut-off frequency of the low-pass filter in rad/s and $\overline{\Psi}'_{conv,\alpha\beta}$ is the estimated converter pole virtual flux vector, which is obviously not equal to $\overline{\Psi}_{conv,\alpha\beta}$ as written in equation (3.14). The relationship between the estimated $\overline{\Psi}'_{conv,\alpha\beta}$ and actual $\overline{\Psi}_{conv,\alpha\beta}$ converter pole flux vector, can be explained by substituting (3.15) into (3.14) which yields:

$$\overline{\Psi}_{conv,\alpha\beta} = \frac{\overline{\Psi}'_{conv,\alpha\beta}(j\omega_e + \omega_c)}{j\omega_e}$$

$$\overline{\Psi}_{conv,\alpha\beta} = \overline{\Psi}'_{conv,\alpha\beta} - j\frac{\omega_c}{\omega_e}\,\overline{\Psi}'_{conv,\alpha\beta} \tag{3.16}$$

The virtual flux components in (3.16) can be further expressed in the stationary coordinates for obtaining the magnitude of converter pole virtual flux at both real and complex axes as shown in equations (3.17) and (3.18):

$$\Psi_{conv,\alpha} = \Psi'_{conv,\alpha} + \Psi'_{conv,\beta}\frac{\omega_c}{\omega_e} \tag{3.17}$$

$$\Psi_{conv,\beta} = \Psi'_{conv,\beta} - \Psi'_{conv,\alpha}\frac{\omega_c}{\omega_e} \tag{3.18}$$

Both equations (3.17) and (3.18) show that the α and β components of the actual converter pole virtual flux $\Psi_{conv,\alpha\beta}$, are calculated based on the operating frequency ω_e, the low-pass filter cutoff frequency ω_c and the estimated converter pole virtual

flux vector $\Psi'_{conv,\alpha\beta}$. The complete grid virtual flux estimation procedure including the magnitude and phase error compensation is illustrated in Figure 3-5.

The virtual flux estimation will be implemented by using a digital signal processor (DSP) board. Therefore, a digital discretization technique plays an important role for

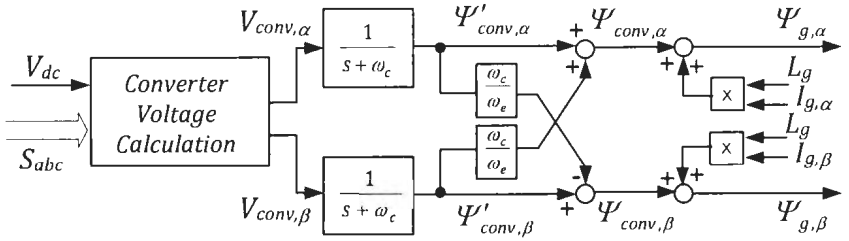


Figure 3-5: Detailed grid virtual flux estimation block diagram

estimating the virtual flux components with a higher degree of accuracy. The converter pole virtual flux is estimated by applying the discretization technique in equation (3.15). The following steps are presented in order to understand the implementation of virtual flux estimation with a digital signal processor.

Let the variable y be the converter pole virtual flux and variable x be the converter pole voltage. Then from the frequency domain transfer function of equation (3.15), one can write:

$$y = \frac{x}{s + \omega_c}$$
$$y(s + \omega_c) = x \tag{3.19}$$

Transforming equation (3.19) into a discrete time domain yields:

$$\frac{y_n - y_{n-1}}{T_s} + y_n\omega_c = x_n$$

$$y_n - y_{n-1} + y_n \omega_c T_s = x_n T_s$$
$$y_n + y_n \omega_c T_s = x_n T_s + y_{n-1}$$
$$y_n(1 + \omega_c T_s) = x_n T_s + y_{n-1}$$
$$y_n = \frac{x_n T_s + y_{n-1}}{(1 + \omega_c T_s)} \tag{3.20}$$

The subscripts of *n* and *n-1* in equation (3.20) represent the recent and the previous value of the particular components, respectively. Meanwhile, T_s is the sampling time and ω_c is the cut-off frequency of low-pass filter. In practical implementation, the variables y and x are separated into their real and imaginary components. Consequently, the estimated converter pole virtual flux in the stationary $\alpha\beta$-reference frame based on equation (3.20) are given by equations (3.21) and (3.22).

$$\Psi'_{conv,\alpha,(n)} = \frac{V_{conv,\alpha,(n)} T_s + \Psi'_{conv,\alpha,(n-1)}}{(1 + \omega_c T_s)} \tag{3.21}$$

$$\Psi'_{conv,\beta,(n)} = \frac{V_{conv,\beta,(n)} T_s + \Psi'_{conv,\beta,(n-1)}}{(1 + \omega_c T_s)} \tag{3.22}$$

Substituting equations (3.21) and (3.22) into equations (3.17) and (3.18), the final mathematical expression of grid virtual flux in the discrete time domain can be presented as:

$$\Psi_{conv,\alpha,(n)} = \frac{V_{conv,\alpha,(n)} T_s + \Psi'_{conv,\alpha,(n-1)}}{(1 + \omega_c T_s)} + \frac{V_{conv,\beta,(n)} T_s + \Psi'_{conv,\beta,(n-1)}}{(1 + \omega_c T_s)} \frac{\omega_c}{\omega_e} \tag{3.23}$$

$$\Psi_{conv,\beta,(n)} = \frac{V_{conv,\beta,(n)} T_s + \Psi'_{conv,\beta,(n-1)}}{(1 + \omega_c T_s)} - \frac{V_{conv,\alpha,(n)} T_s + \Psi'_{conv,\alpha,(n-1)}}{(1 + \omega_c T_s)} \frac{\omega_c}{\omega_e} \tag{3.24}$$

The grid virtual flux components are estimated by substituting the converter pole virtual flux as computed by equations (3.23) and (3.24) into the grid virtual flux

equations as shown in (3.8) and (3.9). The final grid virtual in term of real and imaginary components are given in equations (3.25) and (3.26), respectively.

$$\begin{aligned}\Psi_{g,\alpha} &= \Psi_{conv,\alpha} + LI_{g,\alpha} \\ &= \Psi'_{conv,\alpha} + \Psi'_{conv,\beta}\frac{\omega_c}{\omega_e} + LI_{g,\alpha} \\ &= \frac{V_{conv,\alpha,(n)}T_s + \Psi'_{conv,\alpha,(n-1)}}{(1+\omega_c T_s)} + \frac{V_{conv,\beta,(n)}T_s + \Psi'_{conv,\beta,(n-1)}}{(1+\omega_c T_s)}\frac{\omega_c}{\omega_e} + LI_{g,\alpha}\end{aligned} \quad (3.25)$$

$$\begin{aligned}\Psi_{g,\beta} &= \Psi_{conv,\beta} + LI_{g,\beta} \\ &= \Psi'_{conv,\beta} - \Psi'_{conv,\alpha}\frac{\omega_c}{\omega_e} + LI_{g,\beta} \\ &= \frac{V_{conv,\beta,(n)}T_s + \Psi'_{conv,\beta,(n-1)}}{(1+\omega_c T_s)} - \frac{V_{conv,\alpha,(n)}T_s + \Psi'_{conv,\alpha,(n-1)}}{(1+\omega_c T_s)}\frac{\omega_c}{\omega_e} + LI_{g,\beta}\end{aligned} \quad (3.26)$$

3.3 Derivation of the Instantaneous Active and Reactive Powers

The instantaneous active and reactive powers are defined by the product of the three phase voltages and currents [31, 52-53]. The instantaneous active power P is defined as the magnitude of the scalar product or the dot product between the three phase voltages and currents. On the other hand, the instantaneous reactive power Q is defined as the magnitude of the vector product or cross product between the three phase voltages and currents. The mathematical description of instantaneous active and reactive powers according to the measured input phase voltages and line currents are given in (3.27) and (3.28), respectively:

$$P = \bar{E}_{g,abc} \cdot \bar{I}_{g,abc} = E_{g,an}I_{g,a} + E_{g,bn}I_{g,b} + E_{g,cn}I_{g,c} \quad (3.27)$$

$$Q = \bar{E}_{g,abc} \times \bar{I}_{g,abc} = E'_{g,an}I_{g,a} + E'_{g,bn}I_{g,b} + E'_{g,cn}I_{g,c} \quad (3.28)$$

where the phase angle of $E'_{g,an}$, $E'_{g,bn}$, $E'_{g,cn}$ are 90° lags of $E_{g,an}$, $E_{g,bn}$ and $E_{g,cn}$, respectively. Subsequently, the instantaneous reactive power Q can be also described by equation (3.29):

$$Q = \frac{1}{\sqrt{3}}\{(E_{g,bn} - E_{g,cn})I_{g,a} + (E_{g,cn} - E_{g,an})I_{g,b} + (E_{g,an} - E_{g,b})I_{g,cn}\} \quad (3.29)$$

In order to utilize the virtual flux concept and consequently avoid any extra sensors to measure the grid input voltages, equations which describe the instantaneous active and reactive powers have to be derived. According to the space vector theorem, the input instantaneous active and reactive powers can be calculated based on the real and imaginary parts of the scalar product of the three

phase supply voltage vector and the conjugate input current vector as presented in equations (3.30) and (3.31):

$$P = Real\left\{\frac{3}{2}\left(\bar{E}_{g,\alpha\beta} \cdot \bar{I}^{*}_{g,\alpha\beta}\right)\right\} \tag{3.30}$$

$$Q = Imaginary\left\{\frac{3}{2}\left(\bar{E}_{g,\alpha\beta} \cdot \bar{I}^{*}_{g,\alpha\beta}\right)\right\} \tag{3.31}$$

The expression of the grid voltage vector in the power equations of (3.30) and (3.31), can be replaced by the appropriate grid virtual flux vector by manipulating the equation that defines the grid flux as described in equation (3.6) into the power derivation procedure. The grid virtual flux vector in the $\alpha\beta$-reference frame $\overline{\Psi}_{g,\alpha\beta}$, can be represented by the grid virtual flux magnitude $\left|\overline{\Psi}_{g,\alpha\beta}\right|$ and the angle component ωt, as shown in equation (3.32):

$$\overline{\Psi}_{g,\alpha\beta} = \left|\overline{\Psi}_{g,\alpha\beta}\right|e^{j\omega t} = \left|\overline{\Psi}_{g,\alpha\beta}\right|\left(cos(\omega t) + jsin(\omega t)\right) = \Psi_{g,\alpha} + j\Psi_{g,\beta} \tag{3.32}$$

Manipulating equation (3.6) and differentiating the grid flux vector given in equation (3.32), the following expression can be obtained:

$$\bar{E}_{g,\alpha\beta} = \frac{d}{dt}\overline{\Psi}_{g,\alpha\beta}$$

$$\frac{d}{dt}\overline{\Psi}_{g,\alpha\beta} = \left|\overline{\Psi}_{g,\alpha\beta}\right|\frac{d}{dt}\left(e^{j\omega t}\right) = j\omega\left|\overline{\Psi}_{g,\alpha\beta}\right|e^{j\omega t} = j\omega\left(\Psi_{g,\alpha} + j\Psi_{g,\beta}\right) \tag{3.33}$$

In order to derive the instantaneous active and reactive power based on virtual flux concept, a relationship between virtual flux vector components in the $\alpha\beta$-coordinates and the dq-coordinates as shown in (3.34) has to be used in the power derivation:

$$\overline{\Psi}_{g,\alpha\beta} = \left(\overline{\Psi}_{g,dq}\right)e^{j\omega t} \tag{3.34}$$

where

$$\overline{\Psi}_{g,\alpha\beta} = \Psi_{g,\alpha} + j\Psi_{g,\beta} \tag{3.35}$$

$$\overline{\Psi}_{g,dq} = \Psi_{g,d} + j\Psi_{g,q} \tag{3.36}$$

A differential expression of the grid flux vectors in equation (3.34) can be written as:

$$\frac{d}{dt}\overline{\Psi}_{g,\alpha\beta} = \frac{d}{dt}\left(\overline{\Psi}_{g,dq}e^{j\omega t}\right) \tag{3.37}$$

Solving the right side of equation (3.37) yields:

$$\frac{d}{dt}\overline{\Psi}_{g,\alpha\beta} = \frac{d\left(\overline{\Psi}_{g,dq}\right)}{dt}e^{j\omega t} + \overline{\Psi}_{g,dq}\frac{d\left(e^{j\omega t}\right)}{dt} \tag{3.38}$$

$$= \frac{d\left(\Psi_{g,d} + j\Psi_{g,q}\right)}{dt}e^{j\omega t} + j\omega\left(\Psi_{g,d} + j\Psi_{g,q}\right)e^{j\omega t} \tag{3.39}$$

For sinusoidal and balanced grid voltages, a differentiation of the grid flux vector in the dq-coordinates $\frac{d\left(\Psi_{g,d}+j\Psi_{g,q}\right)}{dt}$, would vanish because $\Psi_{g,d}$ and $\Psi_{g,q}$ are the grid virtual flux magnitude and constant in a rotating synchronous frame. Therefore, the differential of virtual flux dq components will give zero value and can be written as:

$$\frac{d\left(\Psi_{g,d}\right)}{dt} = j\frac{d\left(\Psi_{g,q}\right)}{dt} = 0 \tag{3.40}$$

Consequently, the differential of grid virtual flux components as shown in equation (3.39) can be simplified and shown in equation (3.41).

$$\frac{d}{dt}\overline{\Psi}_{g,\alpha\beta} = j\omega\overline{\Psi}_{g,dq}e^{j\omega t} = j\omega\left(\Psi_{g,d} + j\Psi_{g,q}\right)e^{j\omega t} \tag{3.41}$$

Equation (3.41) will be used extensively for deriving the instantaneous active and reactive powers base on a virtual flux concept as explained in the following subchapters.

3.3.1 Derivation of Instantaneous Active and Reactive Powers in the Synchronously Rotating *dq*-Reference Frame

With balanced three phase input voltages and input currents, the three phase input apparent power S_{in} is given by:

$$S_{in} = \frac{3}{2}\bar{E}_{g,\alpha\beta}\bar{I}^{*}_{g,\alpha\beta} \tag{3.42}$$

According to the flux definition, a grid voltage vector in the $\alpha\beta$-coordinates $\bar{E}_{g,\alpha\beta}$, is equal to the derivative of a grid virtual flux in the $\alpha\beta$-coordinates $\overline{\Psi}_{g,\alpha\beta}$, as shown by:

$$\bar{E}_{g,\alpha\beta} = \frac{d}{dt}\overline{\Psi}_{g,\alpha\beta} \tag{3.43}$$

Substituting (3.41) and (3.43) into the input apparent power of (3.42), equation (3.44) is obtained:

$$\begin{aligned}
S_{in} &= \frac{3}{2}\bar{E}_{g,\alpha\beta}\bar{I}^{*}_{g,\alpha\beta} \\
&= \frac{3}{2}\left\{\left(\frac{d}{dt}\overline{\Psi}_{g,\alpha\beta}\right)\bar{I}^{*}_{g,\alpha\beta}\right\} \\
&= \frac{3}{2}\left\{\left(\frac{d}{dt}\overline{\Psi}_{g,dq}e^{j\omega t}\right)\left(\bar{I}_{g,dq}e^{j\omega t}\right)^{*}\right\} \\
&= \frac{3}{2}\left\{\left(\frac{d\left(\overline{\Psi}_{g,dq}\right)}{dt}e^{j\omega t} + j\omega\overline{\Psi}_{g,dq}e^{j\omega t}\right)\left(\bar{I}_{g,dq}e^{j\omega t}\right)^{*}\right\}
\end{aligned}$$

$$= \frac{3}{2}\left\{\left(\frac{d\left(\Psi_{g,d}+j\Psi_{g,q}\right)}{dt}e^{j\omega t}+j\omega\left(\Psi_{g,d}+j\Psi_{g,q}\right)e^{j\omega t}\right)\left(\left(I_{g,d}+jI_{g,q}\right)e^{j\omega t}\right)^{*}\right\}$$

$$= \frac{3}{2}\left\{e^{j\omega t}\left(\frac{d\Psi_{g,d}}{dt}+j\frac{d\Psi_{g,q}}{dt}+j\omega\Psi_{g,d}-\omega\Psi_{g,q}\right)\left(\left(I_{g,d}-jI_{g,q}\right)e^{-j\omega t}\right)\right\}$$

$$= \frac{3}{2}\left\{e^{j\omega t}e^{-j\omega t}\left(\frac{d\Psi_{g,d}}{dt}I_{g,d}-j\frac{d\Psi_{g,d}}{dt}I_{g,q}-\omega\Psi_{g,q}I_{g,d}+j\omega\Psi_{g,q}I_{g,q}\right.\right. \quad (3.44)$$
$$\left.\left.+j\frac{d\Psi_{g,q}}{dt}I_{g,d}+\frac{d\Psi_{g,q}}{dt}I_{g,q}+j\omega\Psi_{g,d}I_{g,d}+\omega\Psi_{g,d}I_{g,q}\right)\right\}$$

Separating the real and imaginary components of equation (3.44) yields the apparent power equation of (3.45):

$$S_{in} = \frac{3}{2}\left(\frac{d\Psi_{g,d}}{dt}I_{g,d}+\frac{d\Psi_{g,q}}{dt}I_{g,q}-\omega\Psi_{g,q}I_{g,d}+\omega\Psi_{g,d}I_{g,q}-j\frac{d\Psi_{g,d}}{dt}I_{g,q}\right. \quad (3.45)$$
$$\left.+j\frac{d\Psi_{g,q}}{dt}I_{g,d}+j\omega\Psi_{g,q}I_{g,q}+j\omega\Psi_{g,d}I_{g,d}\right)$$

The differentiation of grid virtual flux components in equation (3.45) would vanish (equal to zero) since the components are constant in a synchronous rotating reference frame. Hence, the apparent power as shown in equation (3.45) can be simplified to:

$$S_{in} = \frac{3}{2}\left\{-\omega\Psi_{g,q}I_{g,d}+\omega\Psi_{g,d}I_{g,q}+j\left(\omega\Psi_{g,q}I_{g,q}+\omega\Psi_{g,d}I_{g,d}\right)\right\} \quad (3.46)$$

The input instantaneous active power P_{in} and reactive power Q_{in}, based on the estimated grid virtual flux can be computed by separating the equation (3.46) into the real and imaginary components as shown in equations (3.47) and (3.48), respectively:

$$P_{in} = \frac{3}{2}\omega\left(\Psi_{g,d} I_{g,q} - \Psi_{g,q} I_{g,d}\right) \tag{3.47}$$

$$Q_{in} = \frac{3}{2}\omega\left(\Psi_{g,d} I_{g,d} + \Psi_{g,q} I_{g,q}\right) \tag{3.48}$$

Note that, if the grid virtual flux vector $\overline{\Psi}_{g,dq}$ is aligned to the d-axis as shown in Figure 3-4, the orthogonal component of the virtual flux $\Psi_{g,q}$ is zero $\left(\Psi_{g,q} = 0\right)$. Consequently, the active and reactive powers as shown in equations (3.47) and (3.48) respectively, can be simplified to:

$$P_{in} = \frac{3}{2}\omega\left(\Psi_{g,d} I_{g,q}\right) \tag{3.49}$$

$$Q_{in} = \frac{3}{2}\omega\left(\Psi_{g,d} I_{g,d}\right) \tag{3.50}$$

Equations (3.49) and (3.50) show that if the d-axis is oriented to the grid virtual flux vector, the magnitude of the input active power P_{in} is directly proportional to the q component of the input line current $I_{g,q}$, meanwhile the magnitude of the input reactive power Q_{in} is proportional to the d component of the input line current $I_{g,d}$.

Although the derivation of instantaneous active and reactive powers using the synchronous reference frame provides sufficient information regarding the influence of the grid currents on the active and reactive powers, it requires extra computational effort to calculate the virtual flux angle and to perform the frame transformation procedure. Thus, to avoid a dq-transformation, the estimation of active and reactive powers based on the virtual flux concept in a stationary $\alpha\beta$-reference frame is essential.

3.3.2 Derivation of Instantaneous Active and Reactive Powers in the Stationary $\alpha\beta$-Reference Frame

With the balanced three phase input voltages and currents, the input complex power in a stationary reference frame can be written as:

$$S_{in} = \frac{3}{2}\bar{E}_{g,\alpha\beta}\bar{I}^{*}_{g,\alpha\beta} \tag{3.51}$$

The derivation of input instantaneous active and reactive powers in a stationary $\alpha\beta$-reference frame is performed by applying the virtual flux differentiating equation as shown in (3.33) to the complex power equation of (3.51). The derivation procedure is as follows:

$$\begin{aligned}
S_{in} &= \frac{3}{2}\bar{E}_{g,\alpha\beta}\bar{I}^{*}_{g,\alpha\beta} \\
&= \frac{3}{2}\left\{\left(\frac{d}{dt}\left(\overline{\Psi}_{g,\alpha\beta}\right)\right)\bar{I}^{*}_{g,\alpha\beta}\right\} = \frac{3}{2}\left\{\left(\left|\overline{\Psi}_{g,\alpha\beta}\right|\frac{d}{dt}\left(e^{j\omega t}\right)\right)\bar{I}^{*}_{g,\alpha\beta}\right\} \\
&= \frac{3}{2}\left\{\left(j\omega\left|\overline{\Psi}_{g,\alpha\beta}\right|e^{j\omega t}\right)\bar{I}^{*}_{g,\alpha\beta}\right\} = \frac{3}{2}\left\{j\omega\left(\Psi_{g,\alpha}+j\Psi_{g,\beta}\right)\left(I_{g,\alpha}-jI_{g,\beta}\right)\right\} \\
&= \frac{3}{2}\left\{j\omega\left(\Psi_{g,\alpha}I_{g,\alpha}+j\Psi_{g,\beta}I_{g,\alpha}-j\Psi_{g,\alpha}I_{g,\beta}+\Psi_{g,\beta}I_{g,\beta}\right)\right\} \\
&= \frac{3}{2}\left\{j\omega\left(\Psi_{g,\alpha}I_{g,\alpha}+\Psi_{g,\beta}I_{g,\beta}-j\left(\Psi_{g,\alpha}I_{g,\beta}-\Psi_{g,\beta}I_{g,\alpha}\right)\right)\right\} \\
&= \frac{3}{2}\omega\left\{\left(\Psi_{g,\alpha}I_{g,\beta}-\Psi_{g,\beta}I_{g,\alpha}\right)+j\left(\Psi_{g,\alpha}I_{g,\alpha}+\Psi_{g,\beta}I_{g,\beta}\right)\right\}
\end{aligned} \tag{3.52}$$

Hence, by separating the real and imaginary components of equation (3.52), the input instantaneous active power P_{in} and reactive power Q_{in} of the PWM ac-dc converter in a stationary reference frame can be written as:

$$P_{in} = \frac{3}{2}\omega\left(\Psi_{g,\alpha} I_{g,\beta} - \Psi_{g,\beta} I_{g,\alpha}\right) \tag{3.53}$$

$$Q_{in} = \frac{3}{2}\omega\left(\Psi_{g,\alpha} I_{g,\alpha} + \Psi_{g,\beta} I_{g,\beta}\right) \tag{3.54}$$

3.4 Hysteresis Controllers for the Proposed Virtual Flux Direct Power Control

Figure 3-2 shows that the reference active power P_{ref} delivered from the proportional integral (PI) of the dc-link voltage controller side, and the reference reactive power Q_{ref}, are compared with the estimated input instantaneous active power P and reactive power Q in order to obtain the power error signals that will be processed by two independent hysteresis controllers. The power error signals between the reference and estimated active and reactive powers which are denoted by Δ_P and Δ_Q respectively, can be written as:

$$\Delta_P = P_{ref} - P$$

$$\Delta_Q = Q_{ref} - Q \tag{3.55}$$

The two hysteresis controllers decide at which point an appropriate switching state is applied to the converter gate terminals. The basic principle operation of the two-level hysteresis controller is illustrated in Figure 3-6.

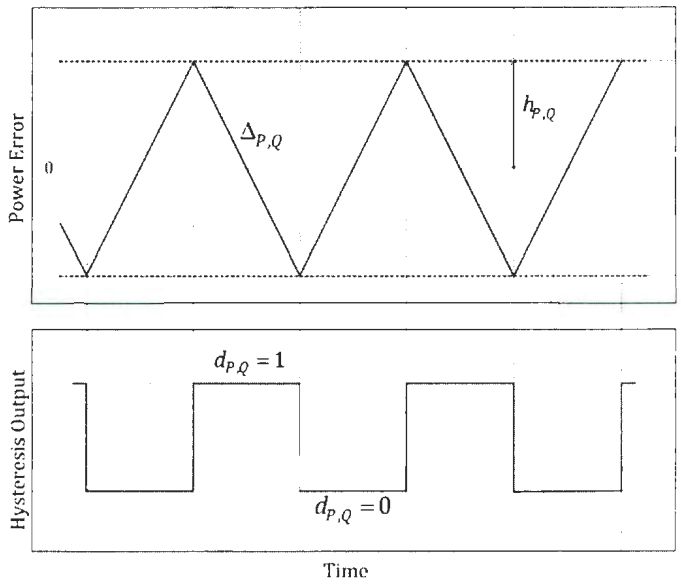


Figure 3-6: Behavior of a two-level hysteresis power controller

If the power error denoted by Δ_P or Δ_Q is increasing and touches the upper level of hysteresis band, the hysteresis controller produces output equal to 1 as shown in the lower diagram of Figure 3-6. The output of the hysteresis controllers designated by $d_{P,Q}$, remains constant at high state ('1') until the decreasing power error touches the lower level of the hysteresis band. The hysteresis controller output $d_{P,Q}$ will be used by the switching look-up table for selecting a suitable voltage vector which allows the converter to modify its instantaneous active and reactive power status to fulfill the load power demand. Once the power error touches the lower level, the hysteresis controller changes its output to the low state ('0') and remains constant at that level until the evaluation of the next power error conditions is performed.

The behavior of a hysteresis controller concerning its band level can be summarized as follows:

$$d_{P,Q} = 1 \begin{cases} \Delta_{P,Q} > h_{P,Q} \\ -h_{P,Q} \leq \Delta_{P,Q} \leq h_{P,Q} \text{ and } \dfrac{d\Delta_{P,Q}}{dt} < 0 \end{cases} \tag{3.56}$$

$$d_{P,Q} = 0 \begin{cases} \Delta_{P,Q} < -h_{P,Q} \\ -h_{P,Q} \leq \Delta_{P,Q} \leq h_{P,Q} \text{ and } \dfrac{d\Delta_{P,Q}}{dt} > 0 \end{cases} \tag{3.57}$$

where $h_{P,Q}$ is the hysteresis band for either the active or reactive power hysteresis controller. $d_{P,Q} = 1$ indicates that the controller must be able to drive the converter increasing the active or reactive power by selecting an appropriate voltage vector from the switching look-up table. On the other hand, $d_{P,Q} = 0$ implies that the controller must be able to reduce the level of active or reactive power by selecting a suitable voltage vector from the same switching look-up table.

3.5 Sector Location and Development of a New Switching Table for the Virtual Flux Direct Power Control

The accuracy of a grid voltage vector position calculation in a complex $\alpha\beta$-plane, has major influence on determining the selection of a suitable converter voltage space vector from a switching look-up table of the Direct Power Control. In the virtual flux direct power control (VFDPC) strategy, the switching table operates according to the position of the grid virtual flux vector which rotates in a complex $\alpha\beta$-plane at an angular velocity in radian per second. The grid virtual flux vector

angle θ, can be calculated by using an inverse trigonometric function based on the estimated virtual grid flux in $\alpha\beta$-coordinates as shown in the equation (3.58).

$$\theta = tan^{-1}\left(\frac{\Psi_{g,\beta}}{\Psi_{g,\alpha}}\right) \tag{3.58}$$

The $\alpha\beta$-plane is divided into 12 sectors. Each sector is 30° wide as shown in Figure 3-7. The sector numbers rotate in the anticlockwise direction and can be generally expressed by equation (3.59). The first sector is defined by the range between -90° and -60°, and the following sectors follow in the anticlockwise direction with the same 30° angle wide.

$$(n-4)30^{\circ} \leq \text{sector } n < (n-3)30^{\circ} \quad \text{where } n = 1,2,\ldots 12 \tag{3.59}$$

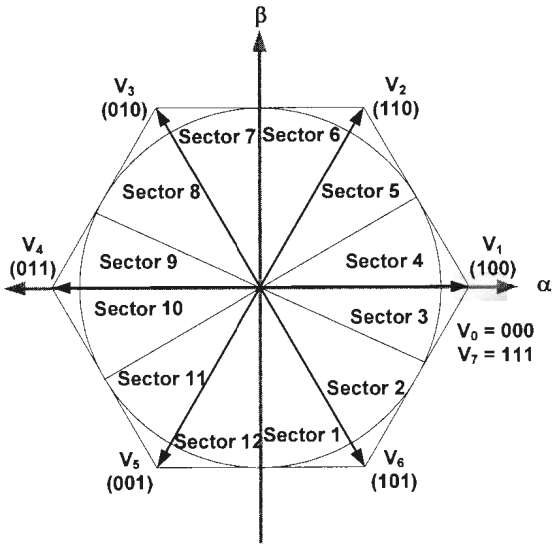


Figure 3-7: Sector location in $\alpha\beta$-plane based on grid flux orientation for Virtual Flux Direct Power Control (VFDPC)

The switching look-up table has a significant impact on the performance of VFDPC. It selects an appropriate converter voltage vector to force the input instantaneous active and reactive powers to flow in the desired direction and magnitude based on the position of the grid virtual flux vector (or grid voltage vector in DPC) and the errors of actual and estimated active and reactive powers.

A topology of the voltage source three phase ac-dc converter as shown in Figure 2-1 is able to produce eight voltage space vectors by performing eight different switch combinations. Each converter voltage space vector as shown in Figure 3-7 can be calculated based on the particular switching state and dc-link voltage as given by the following space vector equation:

$$\overline{V_n} = \boldsymbol{V_n} = \frac{2}{3} V_{dc} \left(S_a + S_b e^{j\frac{2\pi}{3}} + S_c e^{j\frac{4\pi}{3}} \right) \tag{3.60}$$

The converter voltage space vector $\boldsymbol{V_n}$ is numbered from zero to seven (n = 0,1,...7). S_a, S_b, S_c are the states of the upper switches of converter's leg a, b and c, respectively. As an example, $S_a = 1$ denotes that the upper switch of leg a is on, meanwhile $S_a = 0$ means that the upper switch is in the off state. The states of the lower switches must be assigned to be complementary to the upper ones to avoid a short circuit in the particular converter's leg.

The converter voltage vectors with n = 1,2, 3, 4, 5, and 6 are also called active vectors and have an equal amplitude given by $\frac{2}{3} V_{dc}$, and a sequential phase angle of $(n-1)60^{\circ}$. The remaining two voltage vectors denoted by n = 0, and 7 have an amplitude equal to zero. Hence they are also referred to as a zero vector and lies on

the center of the hexagon in Figure 3-7. The switching table has to select a correct voltage vector from the eight voltage vectors in order keep the error signals within the desired hysteresis band. The selected converter voltage vector will be applied continuously to the converter switches until the switching table receives a new command signal from the hysteresis controllers and the sector decision block. Table 3-1 shows the relationship between the converter space vectors and the switching sates. Equation (3.60) is used to define all the eight voltage space vectors in $\alpha\beta$-plane as shown by the space vector diagram in Figure 3-7.

Table 3-1: Relationship between the converter voltage space vector and switching states

Converter Voltage Space Vector (V_n)		**Switching States (S_a, S_b, S_c)**	**Voltage Space Vector Definitions**
Zero Vector	V_o	000	$V_o = 0$
	V_7	111	$V_7 = 0$
Active Vector	V_1	100	$V_1 = \frac{2}{3} V_{dc} e^{j0^\circ}$
	V_2	110	$V_2 = \frac{2}{3} V_{dc} e^{j60^\circ}$
	V_3	010	$V_3 = \frac{2}{3} V_{dc} e^{j120^\circ}$
	V_4	011	$V_4 = \frac{2}{3} V_{dc} e^{j180^\circ}$
	V_5	001	$V_5 = \frac{2}{3} V_{dc} e^{j240^\circ}$
	V_6	101	$V_6 = \frac{2}{3} V_{dc} e^{j300^\circ}$

The proposed switching look-up table is developed based on the instantaneous active and reactive power derivative method. The proposed switching table is able to choose the best converter voltage vector among the eight possible vectors in order to ensure smooth control of instantaneous active and reactive power during each of twelve sectors. The active and reactive power derivative technique is performed by differentiating the instantaneous active and reactive power equations that have been derived in subchapters 3.3.1 and 3.3.2. The instantaneous input active and reactive power of the front-end three phase ac-dc converter in a stationary $\alpha\beta$-reference frame are given by:

$$P = \frac{3}{2}\omega\left(\Psi_{g,\alpha} I_{g,\beta} - \Psi_{g,\beta} I_{g,\alpha}\right) \tag{3.61}$$

$$Q = \frac{3}{2}\omega\left(\Psi_{g,\alpha} I_{g,\alpha} + \Psi_{g,\beta} I_{g,\beta}\right) \tag{3.62}$$

Accordingly, the differentiation of active and reactive power can be represented as:

$$\frac{dP}{dt} = \frac{3}{2}\omega\left(\Psi_{g,\alpha}\frac{dI_{g,\beta}}{dt} + \frac{d\Psi_{g,\alpha}}{dt} I_{g,\beta} - \Psi_{g,\beta}\frac{dI_{g,\alpha}}{dt} - \frac{d\Psi_{g,\beta}}{dt} I_{g,\alpha}\right) \tag{3.63}$$

$$\frac{dQ}{dt} = \frac{3}{2}\omega\left(\Psi_{g,\alpha}\frac{dI_{g,\alpha}}{dt} + \frac{d\Psi_{g,\alpha}}{dt} I_{g,\alpha} + \Psi_{g,\beta}\frac{dI_{g,\beta}}{dt} + \frac{d\Psi_{g,\beta}}{dt} I_{g,\beta}\right) \tag{3.64}$$

Equations (3.63) and (3.64) show that the derivative of the active and reactive powers requires information on the variation of the grid line current and virtual flux components. If the grid supply voltage is assumed to be balanced and sinusoidal, the supply voltage in a stationary reference frame can be expressed as:

$$E_{g,\alpha} = E_g cos(\omega t) \tag{3.65}$$

$$E_{g,\beta} = E_g sin(\omega t) \tag{3.66}$$

Applying a definition of virtual flux into the grid voltages of (3.65) and (3.66), the grid virtual flux in a stationary reference frame can be written as:

$$\Psi_{g,\alpha} = \int E_{g,\alpha}\, dt = \int E_g cos(\omega t) dt = \frac{E_g sin(\omega t)}{\omega} = \frac{E_{g,\beta}}{\omega} \tag{3.67}$$

$$\Psi_{g,\beta} = \int E_{g,\beta}\, dt = \int E_g sin(\omega t) dt = \frac{-E_g cos(\omega t)}{\omega} = \frac{-E_{g,\alpha}}{\omega} \tag{3.68}$$

By linking the relationship between the grid voltage and the grid virtual flux as mentioned in (3.43) to the equations of (3.67) and (3.68), the derivative expression of grid virtual flux can be written as:

$$\frac{d\Psi_{g,\alpha}}{dt} = E_{g,\alpha} = -\omega \Psi_{g,\beta} \tag{3.69}$$

$$\frac{d\Psi_{g,\beta}}{dt} = E_{g,\beta} = \omega \Psi_{g,\alpha} \tag{3.70}$$

Based on the voltage loop equation derived from the single phase equivalent circuit of the front-end PWM ac-dc converter as shown in Figure 2-3, the instantaneous current variations can be expressed with their respective α, β components as:

$$\frac{dI_{g,\alpha}}{dt} = \frac{1}{L}\left(E_{g,\alpha} - V_{conv,\alpha} - I_{g,\alpha}R\right) \tag{3.71}$$

$$\frac{dI_{g,\beta}}{dt} = \frac{1}{L}\left(E_{g,\beta} - V_{conv,\beta} - I_{g,\beta}R\right) \tag{3.72}$$

Substituting equations (3.69), (3.70), (3.71) and (3.72) into the power derivative equations given by equations (3.63) and(3.64), the differentiation of active and reactive power can be expanded to:

$$\frac{dP}{dt} = \frac{3}{2}\omega\left(\Psi_{g,\alpha}\frac{1}{L}\left(E_{g,\beta} - V_{conv,\beta} - I_{g,\beta}R\right) - \omega\Psi_{g,\beta}I_{g,\beta} - \Psi_{g,\beta}\frac{1}{L}\left(E_{g,\alpha} - V_{conv,\alpha} - I_{g,\alpha}R\right) - \omega\Psi_{g,\alpha}I_{g,\alpha}\right) \tag{3.73}$$

$$\frac{dQ}{dt} = \frac{3}{2}\omega\left(\Psi_{g,\alpha}\frac{1}{L}\left(E_{g,\alpha} - V_{conv,\alpha} - I_{g,\alpha}R\right) - \omega\Psi_{g,\beta}I_{g,\alpha} + \Psi_{g,\beta}\frac{1}{L}\left(E_{g,\beta} - V_{conv,\beta} - I_{g,\beta}R\right) + \omega\Psi_{g,\alpha}I_{g,\beta}\right) \tag{3.74}$$

$$\frac{dP}{dt} = \frac{3}{2}\omega\left(\Psi_{g,\alpha}\frac{1}{L}\left(\omega\Psi_{g,\alpha} - V_{conv,\beta} - I_{g,\beta}R\right) - \omega\Psi_{g,\beta}I_{g,\beta} - \Psi_{g,\beta}\frac{1}{L}\left(-\omega\Psi_{g,\beta} - V_{conv,\alpha} - I_{g,\alpha}R\right) - \omega\Psi_{g,\alpha}I_{g,\alpha}\right) \tag{3.75}$$

$$\frac{dQ}{dt} = \frac{3}{2}\omega\left(\Psi_{g,\alpha}\frac{1}{L}\left(-\omega\Psi_{g,\beta} - V_{conv,\alpha} - I_{g,\alpha}R\right) - \omega\Psi_{g,\beta}I_{g,\alpha} + \Psi_{g,\beta}\frac{1}{L}\left(\omega\Psi_{g,\alpha} - V_{conv,\beta} - I_{g,\beta}R\right) + \omega\Psi_{g,\alpha}I_{g,\beta}\right) \tag{3.76}$$

If the choke resistance value is assumed to be negligible ($R \approx 0$), then the final equations of (3.75) and (3.76) can be simplified as:

$$\frac{dP}{dt} = \frac{3}{2}\omega\left(-\omega\Psi_{g,\alpha}I_{g,\alpha} - \omega\Psi_{g,\beta}I_{g,\beta} + \frac{1}{L}\left(\omega\left(\Psi_{g,\alpha}{}^2\right) + \omega\left(\Psi_{g,\beta}{}^2\right) - \Psi_{g,\alpha}V_{conv,\beta} + \Psi_{g,\beta}V_{conv,\alpha}\right)\right) \tag{3.77}$$

$$\frac{dQ}{dt} = \frac{3}{2}\omega\left(\omega\Psi_{g,\alpha}I_{g,\beta} - \omega\Psi_{g,\beta}I_{g,\alpha} + \Psi_{g,\alpha}\frac{1}{L}\left(-\omega\Psi_{g,\beta} - V_{conv,\alpha}\right) + \Psi_{g,\beta}\frac{1}{L}\left(\omega\Psi_{g,\alpha} - V_{conv,\beta}\right)\right) \tag{3.78}$$

The derivation of the final power differentiation equations as shown in (3.77) and (3.78), are influenced by the grid virtual flux, line currents, the line filter inductance

and the converter pole voltages. Each of the converter pole voltages is calculated based on the particular switching states and the dc-link voltage. The converter pole voltage vector is given by the following equation:

$$\bar{V}_{conv,\alpha\beta} = \bar{S}_{\alpha\beta} V_{dc} \tag{3.79}$$

The converter pole voltage vector and the switching state vector in a stationary reference frame denoted by $\bar{V}_{conv,\alpha\beta}$ and $\bar{S}_{\alpha\beta}$ respectively, can be separated into α and βcomponents as:

$$V_{conv,\alpha} = S_\alpha V_{dc};\ V_{conv,\beta} = S_\beta V_{dc} \tag{3.80}$$

$$S_\alpha = S_a - \frac{1}{3}(S_a + S_b + S_c)\ ;\ S_\beta = \frac{1}{\sqrt{3}}(S_b - S_c) \tag{3.81}$$

The differentiation of active and reactive power as given by equations (3.77) and (3.78) are plotted in order to study the effect of a particular converter voltage space vector $\boldsymbol{V_n}$ on the behavior of the instantaneous active and reactive power. Figure 3-8(a) and (b) show the behavior of the active and reactive power which is affected by the different converter voltage vectors $\boldsymbol{V_n}$.

The new switching table is developed based on the sign and magnitude of the change in active and reactive power for each sector. For example, for the angle in the range 0° to 30° as shown in Figure 3-8(a), the application of $\boldsymbol{V_3}$, $\boldsymbol{V_4}$, $\boldsymbol{V_5}$, $\boldsymbol{V_6}$, $\boldsymbol{V_0}$ or $\boldsymbol{V_7}$ voltage vectors will generate a positive time-derivative of the active power. As a result, if any of these vectors is applied, the active power tends to increase. On the other hand, the employment of $\boldsymbol{V_1}$ leads to a negative time-derivative which will decrease the active power. Voltage vector $\boldsymbol{V_2}$ has capability either to increase or

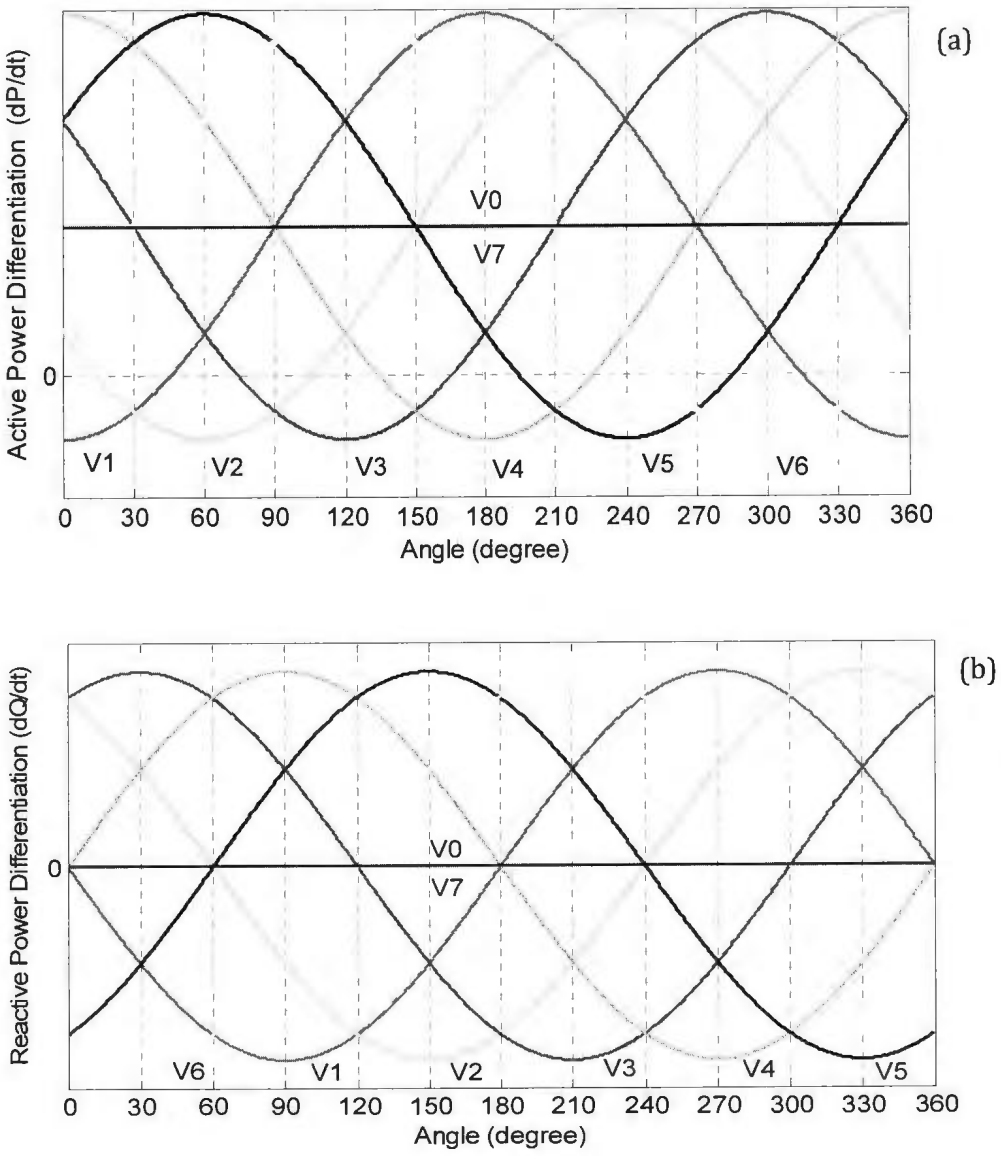


Figure 3-8: Active (a) and reactive (b) power differentiation characteristic under different converter voltage vectors V_n

to decrease the active power since vector V_2 generates both the positive and negative time-derivative of active power. The same procedure is applied for the analysis of different angles, including the reactive power characteristics.

The application of V_2, V_3, or V_4, voltage vectors will produce a positive time-derivative of reactive power as illustrated in Figure 3-8(b). Therefore, if any of these vectors is applied, the reactive power tends to increase. However, the use of V_1, V_5 or V_6 leads to a negative time-derivative which will reduce the reactive power. The employment of zero vectors denoted by V_0 and V_7 will produce zero time-derivative of reactive power. The zero vectors do not affect the reactive power significantly. However, the zero vectors can be utilized to decrease the switching frequency. The same method is applied for the analysis of different angles. Table 3-2 depicts the analysis results of the particular converter voltage on the behavior of active and reactive powers in all twelve sectors.

Table 3-2 shows that for the angle in the range of 0° to 30°, there are two possible space vectors to increase the active power and to decrease the reactive power which are denoted by V_5 and V_6. However, the levels in which they affect the active and reactive power are different. Voltage vector V_5 has a stronger effect on the active power than the voltage vector V_6 does. Thus, the use of voltage vector V_5 or V_6 might produce a large or small power variation that could result in increased or decreased the power ripple and current distortion, respectively. On the other hand, voltage vector V_6 has a larger influence on the reactive power than the voltage vector V_5 does. Therefore, different combinations of the space vectors can be used to achieve the same goal of controlling the active and reactive powers but each combination has distinct effects to the converter system such as current ripple,

switching frequency and dynamic performance. Consequently, different switching tables can be built to control the active and reactive powers.

Table 3-2: Analysis of the Particular Converter Voltage Vector on the Behavior of Active and Reactive power of the PWM AC-DC Converter

	Active power differentiation dP/dt			Reactive power differentiation dQ/dt		
Grid Supply Voltage Vector Angle	$\frac{dP}{dt} > 0$	$\frac{dP}{dt} < 0$	$\frac{dP}{dt} > 0$ and $\frac{dP}{dt} < 0$	$\frac{dQ}{dt} > 0$	$\frac{dQ}{dt} < 0$	$\frac{dQ}{dt} = 0$
$0^\circ \leq \theta < 30^\circ$	$V_3, V_4, V_5, V_6, V_0, V_7$	V_1	V_2	V_2, V_3, V_4	V_1, V_5, V_6	V_0, V_7
$30^\circ \leq \theta < 60^\circ$	$V_3, V_4, V_5, V_6, V_0, V_7$	V_2	V_1	V_2, V_3, V_4	V_1, V_5, V_6	V_0, V_7
$60^\circ \leq \theta < 90^\circ$	$V_1, V_4, V_5, V_6, V_0, V_7$	V_2	V_3	V_3, V_4, V_5	V_1, V_2, V_6	V_0, V_7
$90^\circ \leq \theta < 120^\circ$	$V_1, V_4, V_5, V_6, V_0, V_7$	V_3	V_2	V_3, V_4, V_5	V_1, V_2, V_6	V_0, V_7
$120^\circ \leq \theta < 150^\circ$	$V_1, V_2, V_5, V_6, V_0, V_7$	V_3	V_4	V_4, V_5, V_6	V_1, V_2, V_3	V_0, V_7
$150^\circ \leq \theta < 180^\circ$	$V_1, V_2, V_5, V_6, V_0, V_7$	V_4	V_3	V_4, V_5, V_6	V_1, V_2, V_3	V_0, V_7
$180^\circ \leq \theta < 210^\circ$	$V_1, V_2, V_3, V_6, V_0, V_7$	V_4	V_5	V_1, V_5, V_6	V_2, V_3, V_4	V_0, V_7
$210^\circ \leq \theta < 240^\circ$	$V_1, V_2, V_3, V_6, V_0, V_7$	V_5	V_4	V_1, V_5, V_6	V_2, V_3, V_4	V_0, V_7
$240^\circ \leq \theta < 270^\circ$	$V_1, V_2, V_3, V_4, V_0, V_7$	V_5	V_6	V_1, V_2, V_6	V_3, V_4, V_5	V_0, V_7
$270^\circ \leq \theta < 300^\circ$	$V_1, V_2, V_3, V_4, V_0, V_7$	V_6	V_5	V_1, V_2, V_6	V_3, V_4, V_5	V_0, V_7
$300^\circ \leq \theta < 330^\circ$	$V_2, V_3, V_4, V_5, V_0, V_7$	V_6	V_1	V_1, V_2, V_3	V_4, V_5, V_6	V_0, V_7
$330^\circ \leq \theta < 360^\circ$	$V_2, V_3, V_4, V_5, V_0, V_7$	V_1	V_6	V_1, V_2, V_3	V_4, V_5, V_6	V_0, V_7

The synchronization of the VFDPC with the grid virtual flux vector causes a 90° shift of the space vectors with respect to the line voltage vector. Therefore, a sector which represents an angle range between 0° to 30° in Figure 3-8 (a) and (b), is compatible to sector 1. The sector 1 is located in an angle between -90° and -60° in the $\alpha\beta$-plane as shown in Figure 3-7. Subsequently, a sector which represents an angle range between 30° to 60° in Figure 3-8 (a) and (b) is compatible to sector 2, which is located in an angle between -60° and -30° in the $\alpha\beta$-plane as shown in Figure 3-7. The same procedure is applied for the other remaining sectors. Table 3-3 shows a new switching look-up table for the proposed VFDPC. The new switching look-up table algorithm is developed by using the Matlab S-function feature and written in the C-language. The developed algorithm is used in both, the simulation study and the real-time digital signal processing implementation.

Table 3-3: A New switching look-up table for the PWM AC-DC Converter

Power error status		Sector position (θ_n) and converter voltage vector ($\boldsymbol{V_n}$)											
d_P	d_Q	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}	θ_{12}
0	0	$\boldsymbol{V_1}$	$\boldsymbol{V_1}$	$\boldsymbol{V_2}$	$\boldsymbol{V_2}$	$\boldsymbol{V_3}$	$\boldsymbol{V_3}$	$\boldsymbol{V_4}$	$\boldsymbol{V_4}$	$\boldsymbol{V_5}$	$\boldsymbol{V_5}$	$\boldsymbol{V_6}$	$\boldsymbol{V_6}$
0	1	$\boldsymbol{V_2}$	$\boldsymbol{V_2}$	$\boldsymbol{V_3}$	$\boldsymbol{V_3}$	$\boldsymbol{V_4}$	$\boldsymbol{V_4}$	$\boldsymbol{V_5}$	$\boldsymbol{V_5}$	$\boldsymbol{V_6}$	$\boldsymbol{V_6}$	$\boldsymbol{V_1}$	$\boldsymbol{V_1}$
1	0	$\boldsymbol{V_6}$	$\boldsymbol{V_6}$	$\boldsymbol{V_1}$	$\boldsymbol{V_1}$	$\boldsymbol{V_2}$	$\boldsymbol{V_2}$	$\boldsymbol{V_2}$	$\boldsymbol{V_3}$	$\boldsymbol{V_3}$	$\boldsymbol{V_4}$	$\boldsymbol{V_4}$	$\boldsymbol{V_5}$
1	1	$\boldsymbol{V_4}$	$\boldsymbol{V_4}$	$\boldsymbol{V_4}$	$\boldsymbol{V_4}$	$\boldsymbol{V_5}$	$\boldsymbol{V_6}$	$\boldsymbol{V_6}$	$\boldsymbol{V_6}$	$\boldsymbol{V_1}$	$\boldsymbol{V_1}$	$\boldsymbol{V_2}$	$\boldsymbol{V_2}$

3.6 Development of the Voltage Controller for the AC-DC Converter

The dc-link voltage control loop with a proportional integral (PI) compensator is used to regulate the dc output voltage according to a magnitude of the dc voltage reference. The proportional and integral gains of the PI controller are determined by using a symmetrical optimum (SO) method by considering the delay effects generated within the ac-dc converter system [19, 28]. The dc-link voltage control loop block diagram is shown in Figure 3-9.

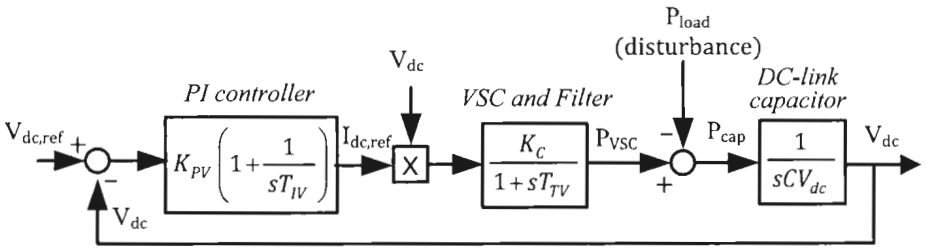


Figure 3-9: Voltage control loop with PI controller

The notations used in the voltage controller of Figure 3-9 are mentioned below:

K_{PV}	proportional gain of the PI regulator
T_{IV}	integrating time
K_C	converter gain
T_{TV}	total time delay in the voltage controller
C	dc-link capacitor
V_{dc}	dc-link voltage

The voltage control loop total time delay T_{TV} is defined by:

$$T_{TV} = T_s + T_{PWM} + T_f + T_d \tag{3.82}$$

where:

T_s sampling time period
T_{PWM} statistical time delay of pulse width modulation
T_f dc-link voltage low pass filter time constant
T_d converter dead time

The sampling time period T_s is taken into account for determining the PI parameters due to the fact that the control loop will be practically implemented in a discrete digital environment. Therefore, the processing delay time caused by the digital signal processor controller board, the gate driver circuits, the power converter and the statistical delay of pulse width modulation (PWM) signals generation T_{PWM}, are taken into consideration in calculating the PI parameters. In reference [19], the statistical delay of the PWM is approximated from zero to two sampling periods (T_{PWM} = 0 to $2T_s$). In the proposed VFDPC, the statistical delay of PWM is chosen to be equal to the sampling period $T_{PWM} = T_s$. During the real-time implementation, a digital low-pass filter with the filter time constant T_f is employed to reduce the ripple and noise of the measured dc-link output voltage. Therefore the filter time constant T_f is also included in the total time delay calculation T_{TV}. The low-pass filter time constant of $T_f = 0.003s$ has been found sufficient to obtain smooth and constant dc-link output voltage. The dead time T_d is negligible in the case of an ideal power converter and the converter gain K_c is assumed equal to one (K_c =1).

The simplified model of the voltage control loop is shown in Figure 3-10. The load power disturbance input signal P_{load} is used to evaluate the effectiveness of the voltage controller during the interruption of load power demand.

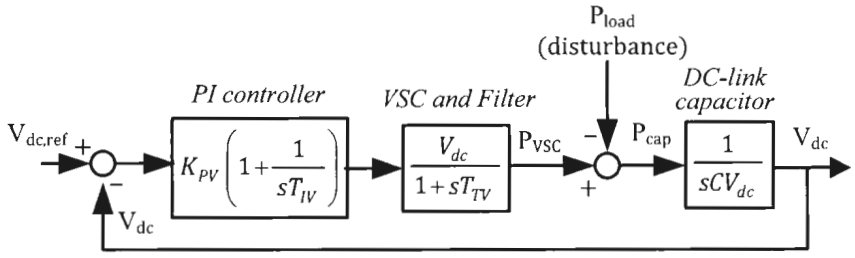


Figure 3-10: Simplified voltage control loop with PI controller

The open loop transfer function of the voltage controller $G_{OV}(s)$ of Figure 3-10 can be derived by assuming that the load power disturbance is constant. Therefore, the load power disturbance input signal can be eliminated from the voltage control loop during the derivation of voltage controller transfer function. The voltage open loop transfer function can be written as:

$$G_{OV}(s) = \frac{K_{PV}(sT_{IV}+1)V_{dc}}{sT_{IV}(sT_{TV}+1)sCV_{dc}} = \frac{K_{PV}(sT_{IV}+1)}{s^2T_{IV}C(sT_{TV}+1)} \tag{3.83}$$

Subsequently, the open loop transfer function equation $G_{OV}(s)$, is used to derive the voltage controller close loop transfer function $G_{CV}(s)$:

$$G_{CV}(s) = \frac{G_{OV}(s)}{1+G_{OV}(s)} = \frac{K_{PV}(sT_{IV}+1)}{s^3T_{IV}T_{TV}C + s^2T_{IV}C + sT_{IV}K_{PV} + K_{PV}} \tag{3.84}$$

According to the SO method, the proportional gain K_{PV} and the integral time constant T_{IV} of the dc-link voltage controller can be calculated by using equations (3.85) and (3.86), respectively.

$$K_{PV} = \frac{C}{2T_{TV}} = \frac{C}{2(T_s + T_{PWM} + T_f + T_d)} \tag{3.85}$$

$$T_{IV} = 4T_{TV} = 4(T_s + T_{PWM} + T_f + T_d) \tag{3.86}$$

Equations (3.85) and (3.86) will be used to calculate the voltage controller integral gain K_{IV} as shown in equation (3.87).

$$K_{IV} = \frac{K_{PV}}{T_{IV}} \tag{3.87}$$

The proportional gain K_{PV} and the integral gain K_{IV} of the PI controller will influence the frequency bandwidth and the phase margin of the voltage controller. In order to ensure that the PWM rectifier system operates in a stable condition, a cut-off frequency of the open loop voltage controller must be designed to be smaller than the converter switching frequency. Moreover, the phase margin and the gain margin of the open loop frequency response must be tuned to the appropriate level to maintain the stability of the system. According to the Nyquist stability criterion for frequency response, a closed loop control system will be stable if the phase margin of the open loop controller is less than 180°, meanwhile the gain margin is in the range of -5dB towards a higher negative value.

With the converter system parameters given in Table 3-4 and appropriate estimation of the total time delay T_{TV}, the calculation of PI parameters using equations (3.85) and (3.86) is performed. A bode diagram of the open loop voltage controller frequency response is shown in Figure 3-11. An analysis of the bode diagram reveals that the open loop voltage controller has a phase margin of 37.5° with 93.7rad per second (rad/s) or 14.91Hz cut-off frequency and produces negative infinity gain margin which indicate that the system is operating in a stable conditions.

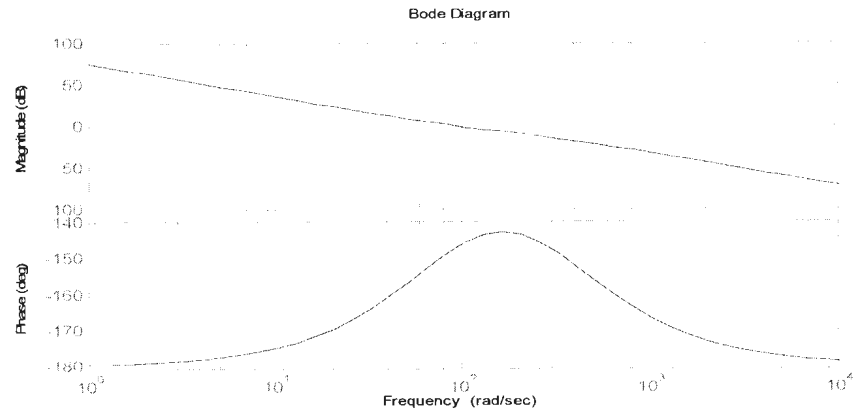


Figure 3-11: Bode diagram of the open loop voltage controller

The step response as shown in Figure 3-12demonstrates that the calculated PI controller parameters based on the symmetrical optimum (SO) method produces a stable transient response of the dc output voltage V_{dc} during a step change on the dc voltage reference $V_{dc,ref}$ at time t=1s. At time t=1.4s, a 10% disturbance in the load power P_{load} is injected into the voltage controller system. The PI controller is able to maintain the dc-link voltage at the reference value after suffering a small dip caused by the disturbance.

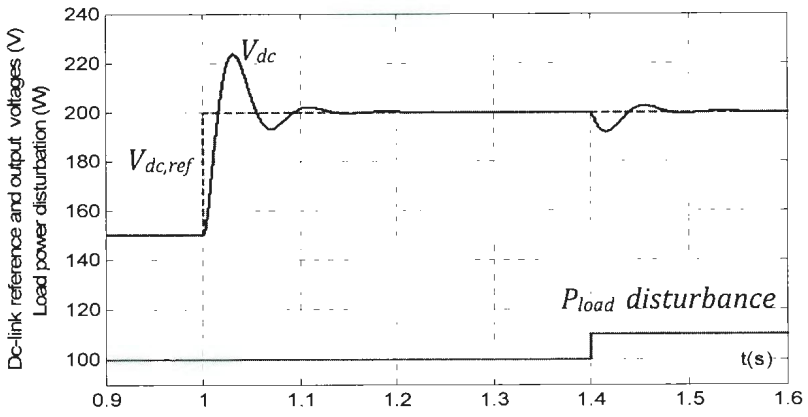


Figure 3-12: Dc-link voltage step response and load power disturbance rejection performances

3.7 Simulation Results and Performance Analysis of the Proposed Virtual Flux Direct Power Control under Balanced Three Phase Voltage Supply

The entire ac-dc converter system using the proposed virtual flux direct power control (VFDPC) is developed and simulated in the Matlab/Simulink discrete environment to study its performances under steady state and transient conditions. The main parameters used in the simulation are given in Table 3-4.

Table 3-4: Main parameters used in the simulation

Input phase voltage (peak) E_g	70.71V
Source voltage frequency f	60Hz
Dc-link voltage reference $V_{dc,ref}$	150V
Resistance of reactors R	0.2Ω
Inductance of reactors L	15mH
DC-link capacitor C	10.8mF
Load resistance R_{Load}	140Ω
Sampling time T_s	20μs
Sampling frequency $f_s = 1/T_s$	50Khz

Figure 3-13 (a) and (b) represent the balanced three phase grid side voltage and line current waveforms, respectively. The VFDPC utilizing the new switching table and the proposed virtual estimation method is able to produce almost sinusoidal line currents with unity power factor operation. An insight of the line current performance during steady state and unity power factor operation can be observed in the voltage and current waveforms shown in Figure 3-14 and the harmonic spectrum of the line current shown by Figure 3-15. The phase a supply voltage $E_{g,a}$,

is in phase with its associate line current $I_{g,a}$. The total harmonic distortion (THD) of the line current is 4.66% which is much lower than the current THD produced by the conventional diode bridge rectifier. The diode bridge rectifier generates 32.87% current THD as shown in the Figure 1-2.

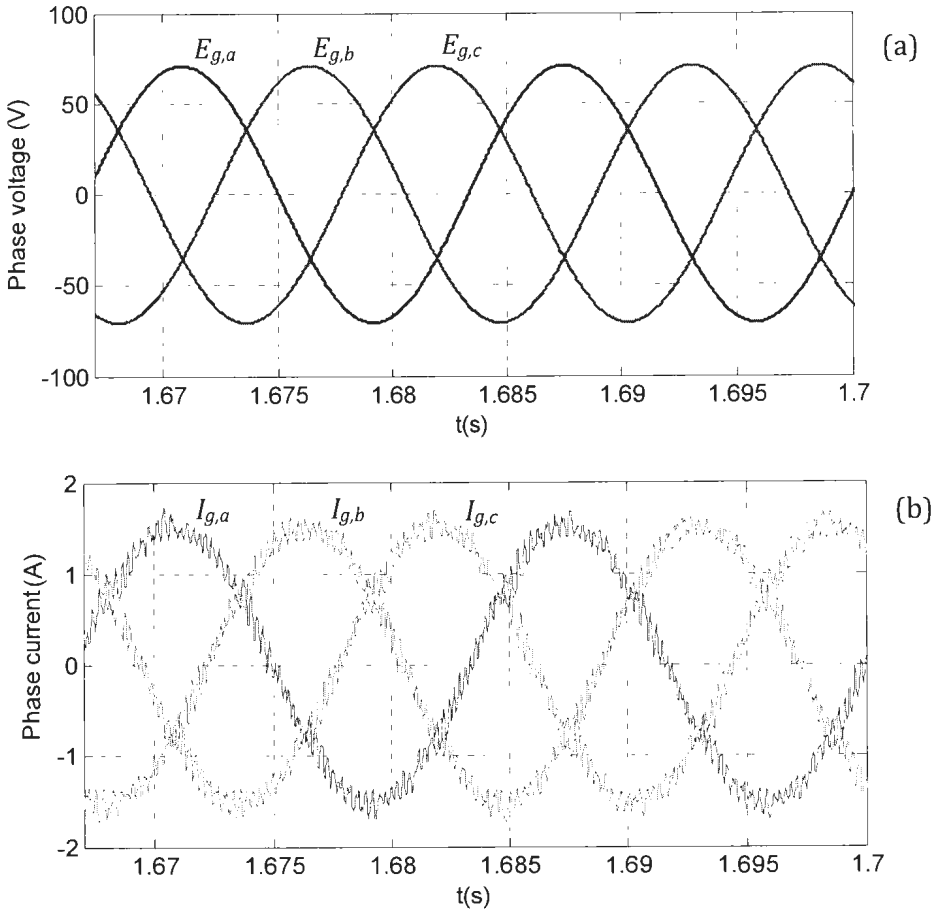


Figure 3-13: a) Three phase supply voltages b) Three phase input currents

The effectiveness of the virtual flux estimation and compensation method can be observed in Figure 3-16. The grid virtual flux components in stationary $\alpha\beta$-coordinates $\Psi_{g,\alpha\beta}$ are used to calculate the grid virtual flux vector angle. Accurate

angle information is required so that all the twelve sector locations for the switching table operation can be determined, and the input instantaneous power can be estimated correctly. The resulting α component of the grid virtual flux, denoted by $\Psi_{g,\alpha}$ in Figure 3-16, is lagging the grid phase a voltage $E_{g,a}$ by 90°. Meanwhile, the imaginary component given by $\Psi_{g,\beta}$ is lagging $\Psi_{g,\alpha}$ by 90°. The grid virtual flux vector angle is calculated and the resultant waveform is shown in Figure 3-17. The virtual flux vector angle then is used to produce the staircase waveform as shown in Figure 3-18 showing all the twelve sector locations as defined by equation (3.59). Although the integration part of the virtual flux calculation is performed by using a low pass-filter with a cut-off frequency of approximately 4.8Hz, the delay caused by the filter is successfully compensated.

The correct estimation of virtual flux components will ensure accurate calculation of the input instantaneous active power P and reactive power Q as shown in Figure 3-20. Subsequently, by setting the reactive power reference Q_{ref} to zero, the correct estimation of active and reactive powers will ensure the line currents are in phase with their respective grid phase voltages. In addition, the proposed VFDPC is able to produce the dc output voltage V_{dc} that is well regulated at a reference voltage $V_{dc,ref}$ of 150V as shown in Figure 3-20.

Figure 3-21 shows the phase a current $I_{g,a}$, and the switching signal S_a applied to the upper switch of the converter's leg a over one cycle fundamental period. It can be ob{erved that around the zero crossing of the phase a current, the frequency of the switching pulses raises. This variable switching frequency can be further

examined in the grid line current harmonic spectrum as presented previously in Figure 3-15. Even though the VFDPC produces low THD of line currents, it generates variable switching frequency with the current harmonics spread over a wide range of frequency.

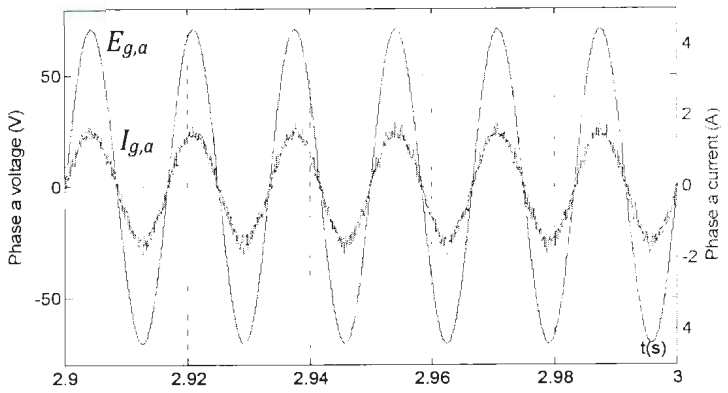


Figure 3-14: Phase *a* voltage and current at unity power factor operation

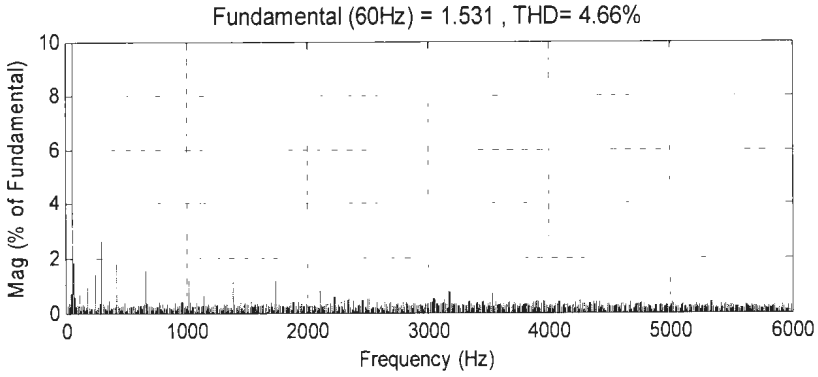


Figure 3-15: Harmonic spectrum of the input line current

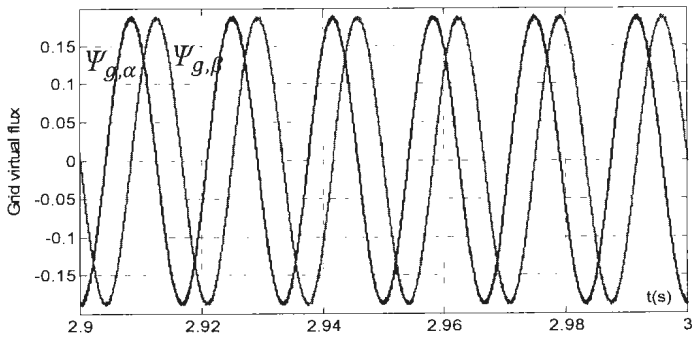


Figure 3-16: Grid virtual flux in a stationary $\alpha\beta$-reference frame

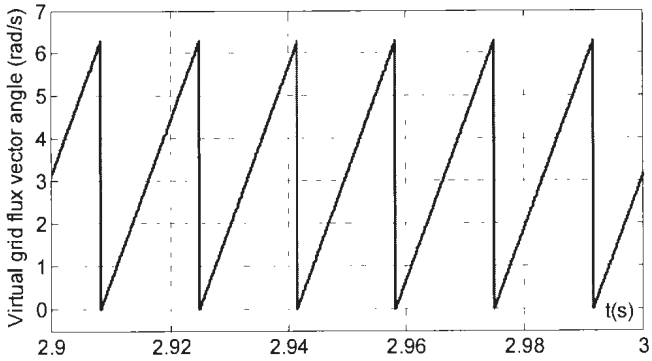


Figure 3-17: Grid virtual flux vector angle for the synchronization between controller and supply voltage

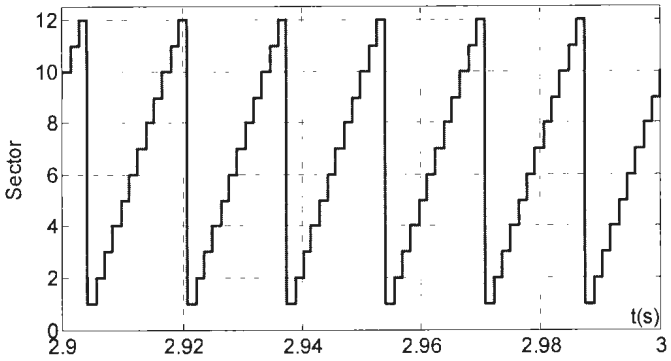


Figure 3-18: 12 sectors is generated from the grid virtual flux vector rotating in the $\alpha\beta$-plane

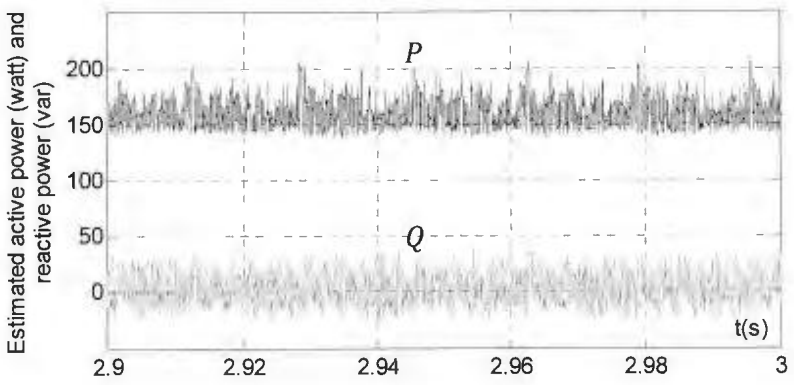


Figure 3-19: Estimated input instantaneous active power *P*, and reactive power *Q* during unity power factor operation

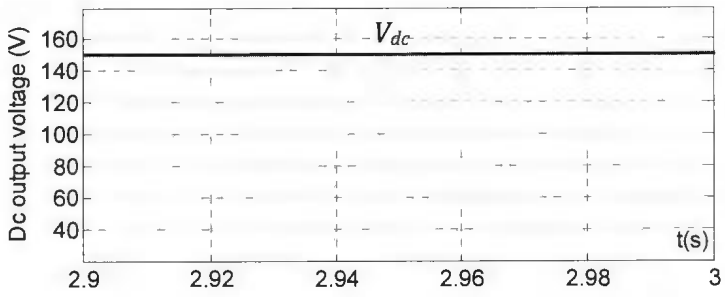
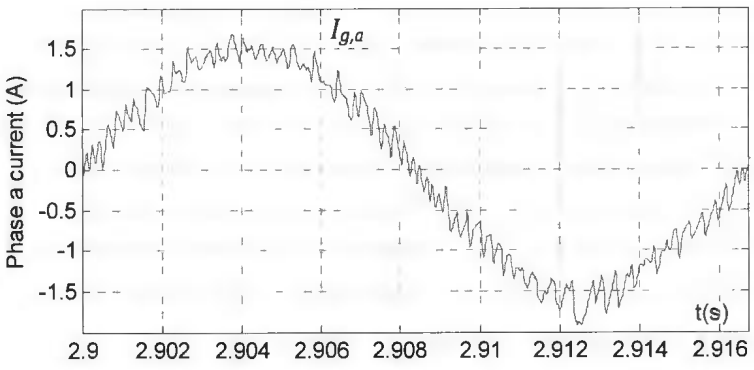
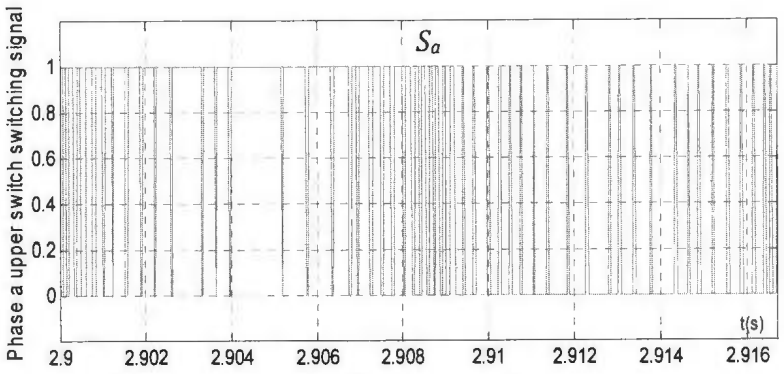


Figure 3-20: Generated dc-link output voltage



(a)



(b)

Figure 3-21: (a) Phase *a* current (b) Leg *a* upper switch signal

The input reactive power reference Q_{ref} is set to zero to operate the PWM rectifier in unity power factor mode. In some applications however, the front-end PWM rectifier is required to operate in a leading power factor mode to compensate the motoring loads of lagging power factor that are connected in a near-by utility grid. The proposed VFDPC is able to produce either a leading or lagging power factor operation by providing appropriate value to the reference reactive power Q_{ref}. The relationship between power factor pf, apparent power S, active power P and reactive power Q is shown in the following equation:

$$pf = \frac{P}{S} = \frac{P}{\sqrt{P^2 + Q^2}} \tag{3.88}$$

In this simulation study, the reference reactive power Q_{ref} is set to -50var and +50var in order to demonstrate a leading and lagging power factor operation, respectively. The resultant of both operation modes are shown in Figure 3-22 and Figure 3-23. The estimated reactive power Q tracks the reference value of Q_{ref}

successfully, while maintaining the magnitude of the estimated active power P for both power factor modes. The estimated reactive power Q is shifted down from 0 to -50 var, and the phase a current leads the phase a supply voltage during leading power factor operation mode as shown in the top and bottom of Figure 3-22. The estimated reactive power Q is shifted up from 0 to 50 var which will result the phase a current lags the phase a voltage as presented in the top and bottom of Figure 3-23.

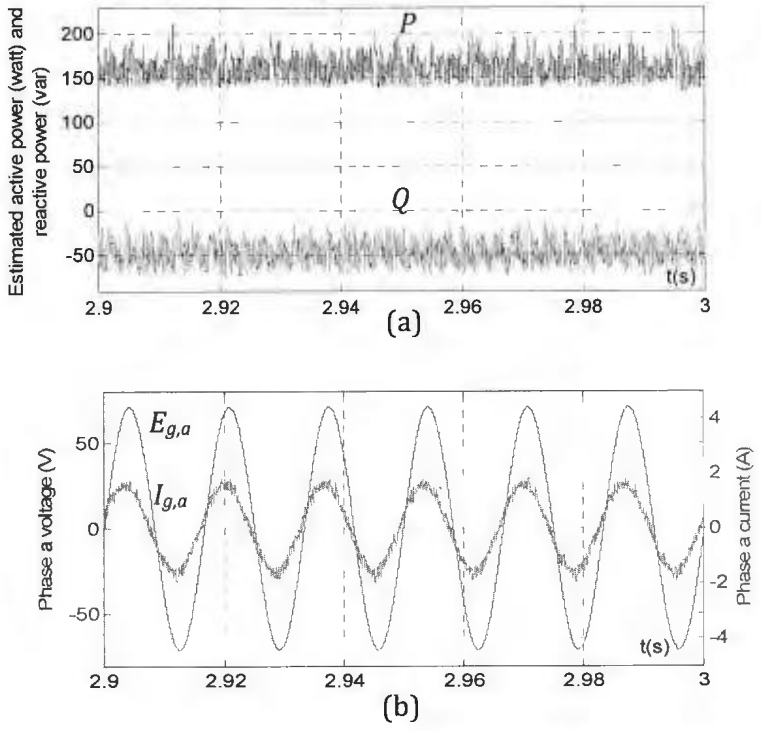


Figure 3-22: Generated waveforms during leading power factor operation. (a) Estimated active and reactive powers. (b) Phase a voltage and current

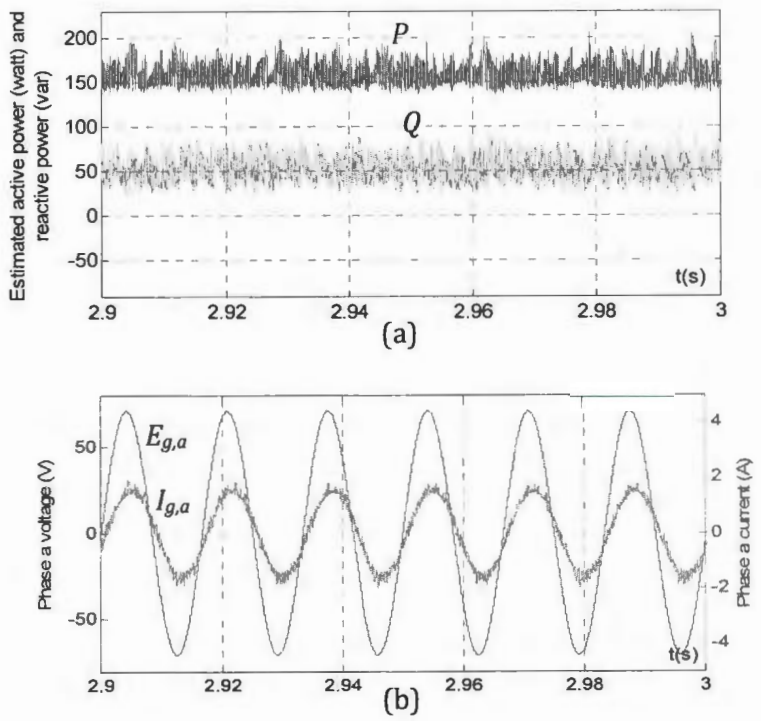
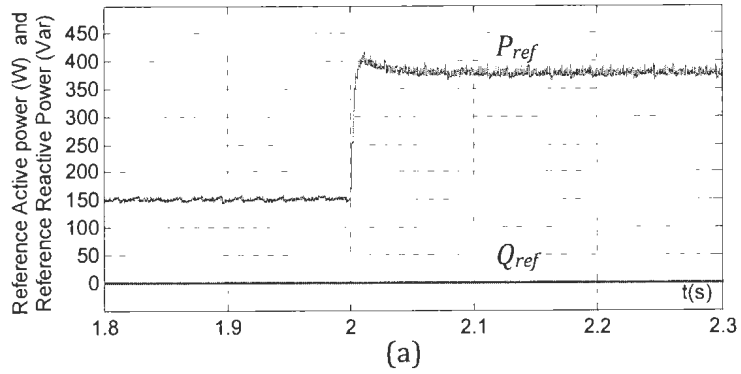


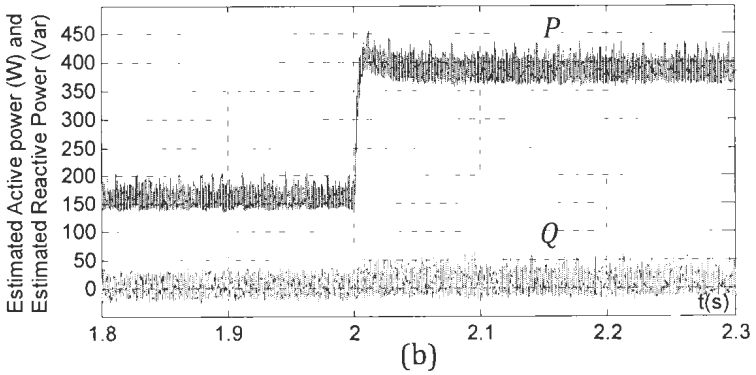
Figure 3-23: Generated waveforms during lagging power factor operation. (a) Estimated active and reactive powers. (b) Phase a voltage and current

Figure 3-24 (a)-(d) show transient responses for load variation under the unity power factor operation. The load variation is performed by connecting a 100 Ω resistor abruptly in parallel with the existing resistor across the dc-link capacitor to cause a sudden disturbance in the load power. The additional load is connected at a simulation time of 2 seconds. The magnitudes of the line current and the estimated input active power P, are changing simultaneously to accommodate increases of the load power demand P_{ref}. The response occurs very fast without any undesirable overshoot and oscillation. It can be observed that the estimated reactive power Q is almost insensitive to a change of the estimated active power P. The reference

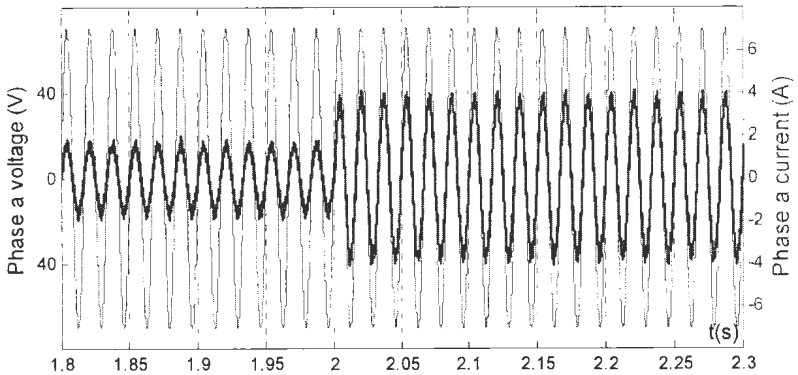
reactive power Q_{ref} and the estimated reactive power Q are kept constant at 0 var during a unity power factor operation mode. In addition, forced by the voltage PI regulator, the dc output voltage V_{dc} recovers to the original value of 150 V after experiencing a small dip as shown in Figure 3-24 (d).



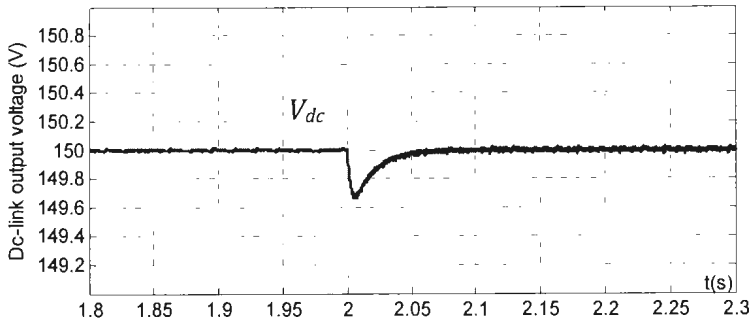
(a)



(b)



(c)



(d)

Figure 3-24: Transient responses for load variation from low to high power demand: (a) Active and reactive power references (b) Estimated active and reactive powers (c) Phase *a* current and voltage (d) Dc-link output voltage

A dynamic behavior of the front-end PWM ac-dc converter under step changes in output voltage reference is shown in Figure 3-25 (a)-(c). The voltage command $V_{dc,ref}$ changes from 150 V to 180 V at 2s and back to 150 V at 4s. With the calculated quantities of the dc-link voltage PI regulator, the dc output voltage V_{dc} quickly follow the $V_{dc,ref}$ with less overshoot as shown in Figure 3-25 (a). The line current $I_{g,a}$ increased and decreased to accommodate the increased and decreased of the converter dc output voltage. The estimated active power P also increased and decreased rapidly to new values during the step changes of output voltage while keeping the reactive power at 0 var.

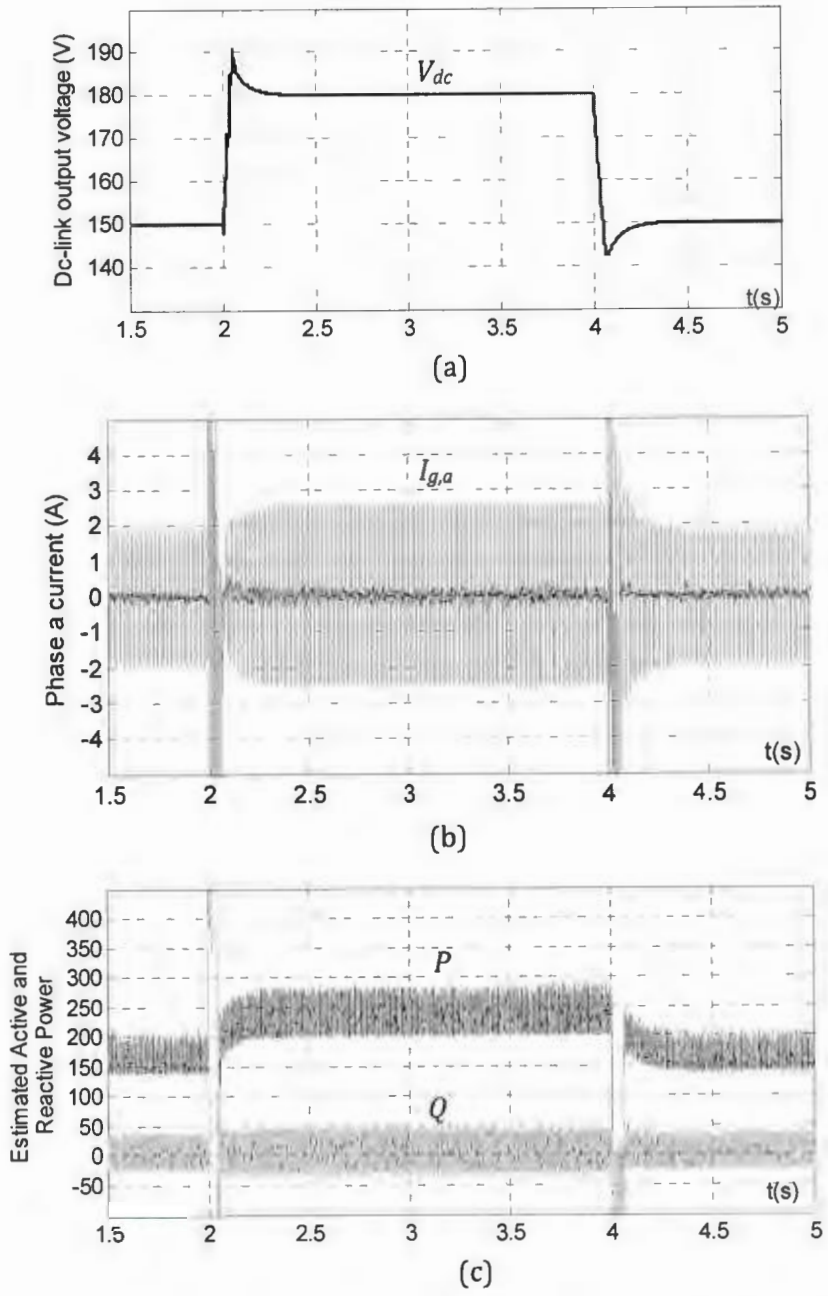


Figure 3-25: Transient response for dc output voltage changes: (a) Dc-link output voltage (b) Phase *a* current (c) Estimated active and reactive powers

3.7.1 Analysis of the VFDPC Utilizing Conventional Switching Look-Up Table

The simulation of VFDPC utilizing the conventional switching table introduced by Noguchi [22] is also performed to evaluate and compare the performance of the VFDPC utilizing both the new developed switching table and the conventional one under steady state and unity power factor operation. The conventional switching table is shown in Table 3-5:

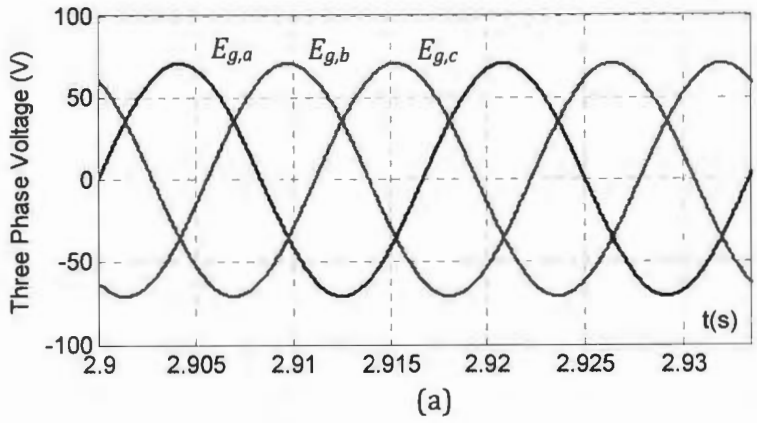
Table 3-5: Conventional switching look-up table for front-end PWM AC-DC Converter

Power error status		Sector position (θ_n) and converter voltage vector ($\boldsymbol{V_n}$)											
d_P	d_Q	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}	θ_{12}
0	0	$\boldsymbol{V_6}$	$\boldsymbol{V_1}$	$\boldsymbol{V_1}$	$\boldsymbol{V_2}$	$\boldsymbol{V_2}$	$\boldsymbol{V_3}$	$\boldsymbol{V_3}$	$\boldsymbol{V_4}$	$\boldsymbol{V_4}$	$\boldsymbol{V_5}$	$\boldsymbol{V_5}$	$\boldsymbol{V_6}$
0	1	$\boldsymbol{V_1}$	$\boldsymbol{V_2}$	$\boldsymbol{V_2}$	$\boldsymbol{V_3}$	$\boldsymbol{V_3}$	$\boldsymbol{V_4}$	$\boldsymbol{V_4}$	$\boldsymbol{V_5}$	$\boldsymbol{V_5}$	$\boldsymbol{V_6}$	$\boldsymbol{V_6}$	$\boldsymbol{V_1}$
1	0	$\boldsymbol{V_6}$	$\boldsymbol{V_7}$	$\boldsymbol{V_1}$	$\boldsymbol{V_0}$	$\boldsymbol{V_2}$	$\boldsymbol{V_7}$	$\boldsymbol{V_3}$	$\boldsymbol{V_0}$	$\boldsymbol{V_4}$	$\boldsymbol{V_7}$	$\boldsymbol{V_5}$	$\boldsymbol{V_0}$
1	1	$\boldsymbol{V_7}$	$\boldsymbol{V_7}$	$\boldsymbol{V_0}$	$\boldsymbol{V_0}$	$\boldsymbol{V_7}$	$\boldsymbol{V_7}$	$\boldsymbol{V_0}$	$\boldsymbol{V_0}$	$\boldsymbol{V_7}$	$\boldsymbol{V_7}$	$\boldsymbol{V_0}$	$\boldsymbol{V_0}$

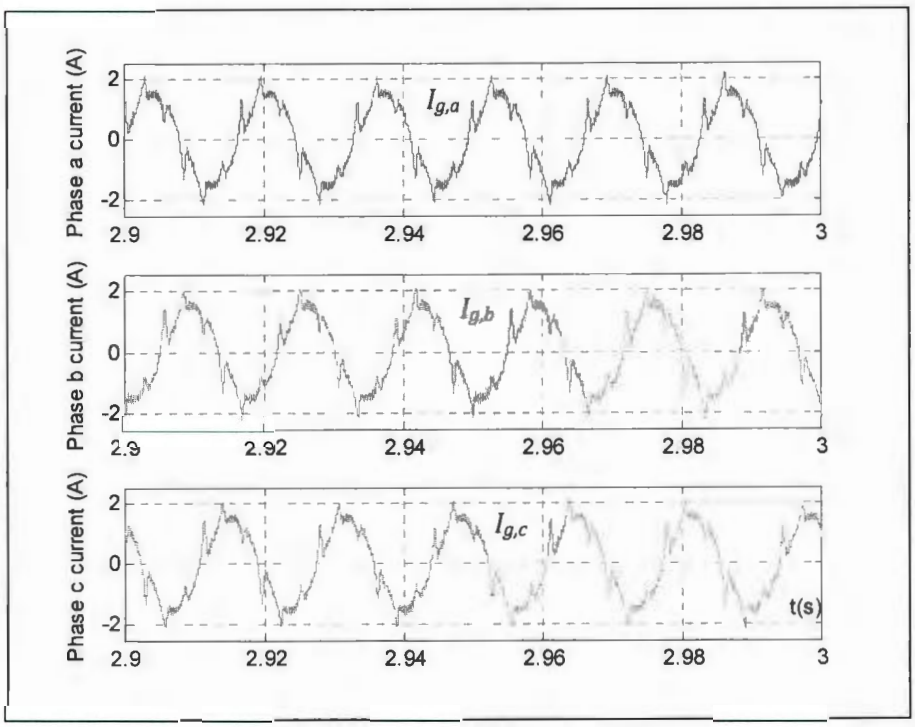
All parameters used in the simulation study are similar with the previous new switching table performance analysis as given by Table 3-4. Figure 3-26 (a) represents the balanced three phase supply voltage waveforms at the input side of the PWM rectifier. The resultant of three phase currents during steady state and unity power factor operation can be clearly observed in Figure 3-26 (b) and Figure 3-27. The input currents are distorted due to the poor estimation of the input active and reactive powers. VFDPC utilizing conventional switching table generates

current total harmonic distortion (THD) of 9.53% which is higher than the current THD obtained from the VFDPC utilizing the new developed switching look-up table. The AC-DC converter utilizing VFDPC with new switching table generates only 4.66% of current THD as stated in subchapter 3.7.

A poor estimation of the instantaneous power is mainly caused by the unsuitable selection of the converter voltage vector performed by the switching table. For example, the selection of converter voltage vector $\boldsymbol{V_6}$ in the sector 1 (θ_1) will not decrease the active power as demanded by the output signal of active power hysteresis controller ($d_P=0$). According to the Table 3-2, the use of $\boldsymbol{V_6}$ will increase the active power and at the same time, decrease the reactive power. In addition, the use of voltage vector $\boldsymbol{V_1}$ in the same sector position will not increase the reactive power as demanded by the output signal of reactive power hysteresis controller ($d_Q=1$). Based on the Table 3-2, the application of $\boldsymbol{V_1}$ will decrease the reactive power and at the same time also decrease the active power. Although the conventional switching table generates distorted line currents, the dc-link capacitor is still able to filter out the dc voltage output ripple in order to obtain purely dc voltage as shown in Figure 3-30.



(a)



(b)

Figure 3-26: a) Three phase input voltage b) Distorted three phase input currents due to inaccurate selection of the converter voltage vectors

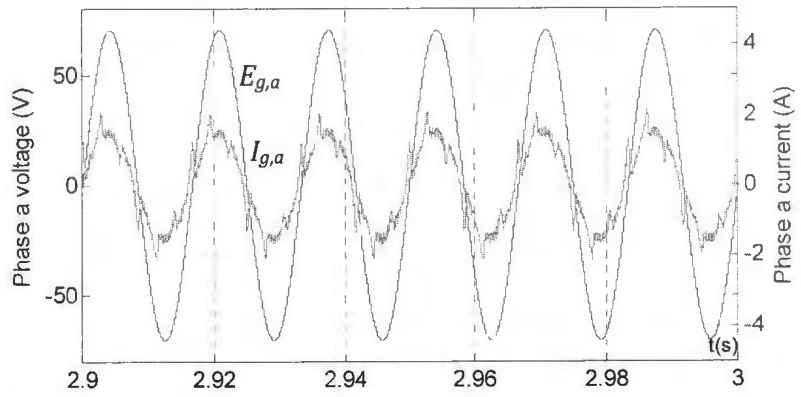


Figure 3-27: Phase *a* voltage and current during unity power factor operation produced by VFDPC with conventional switching table

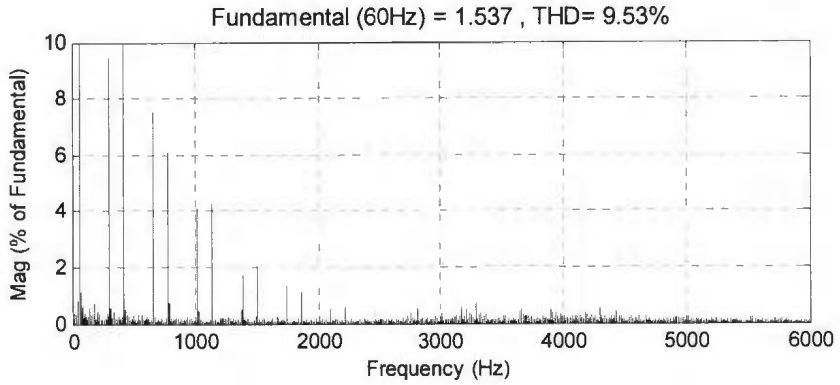


Figure 3-28: Frequency spectrum of the line current generated by VFDPC with conventional switching table

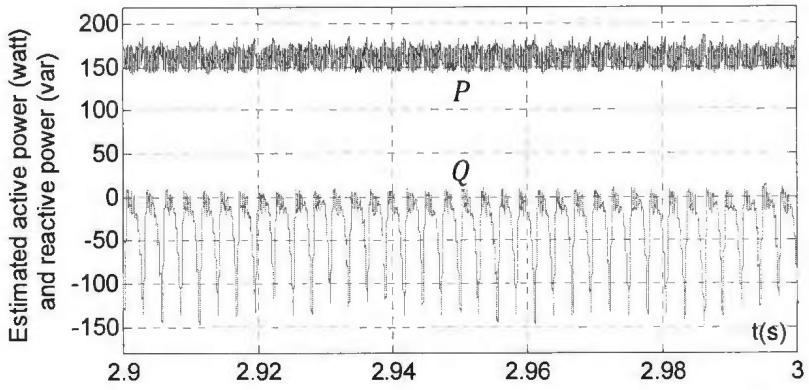


Figure 3-29: Estimated input instantaneous active power *P*, and reactive power *Q* during unity power factor operation.

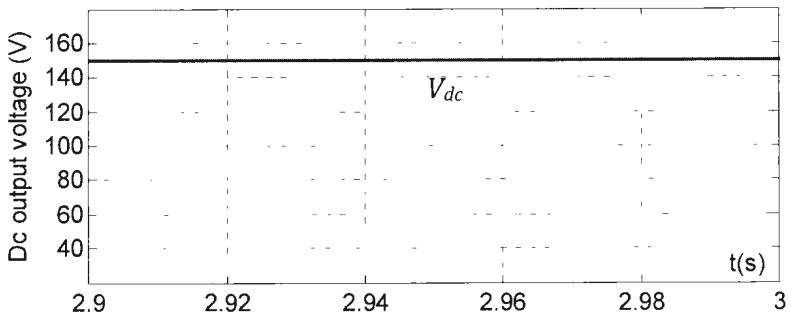


Figure 3-30: Dc-link output voltage obtained from VFDPC with conventional switching table

3.8 Simulation Results and Performance Analysis of the Proposed Virtual Flux Direct Power Control under Distorted Three Phase Voltage Supply

The proposed VFDPC utilizing the new switching table is also evaluated under distorted supply voltage. The voltage distortion is obtained by injecting 10% of the magnitude of the fundamental component into the fifth harmonic component of the positive sequence of the three phase voltage supply. The distorted three phase voltages with fifth harmonic injection can be defined as

$$E_{g,an} = |E|cos(\omega t) + |k * E|cos(5\omega t)$$

$$E_{g,bn} = |E|cos\left(\omega t - \frac{2\pi}{3}\right) + |k * E|cos\left(5\omega t + \frac{2\pi}{3}\right)$$

$$E_{g,cn} = |E|cos\left(\omega t + \frac{2\pi}{3}\right) + |k * E|cos\left(5\omega t - \frac{2\pi}{3}\right) \qquad (3.89)$$

where $|E|$ denotes the magnitude of phase voltage fundamental component, and k is equal to 0.1 for 10% of the fundamental component. Figure 3-31 shows the distorted three phase voltage simulation waveforms.

Due to the low-pass filter behavior performed by the integrator in the virtual flux estimator, the VFDPC with newly developed switching is able to maintain almost sinusoidal three phase currents with a unity power factor as shown in Figure 3-32 and Figure 3-33. The input current THD is 4.91% which is slightly higher than the one if the supply voltage is purely balanced and sinusoidal. As discussed in subchapter 3.7, the proposed VFDPC with new switching table produces current THD of 4.66% for balanced input voltage supply. Waveforms of the estimated active and reactive power and the dc output voltage are shown in Figure 3-35 and Figure 3-36, respectively.

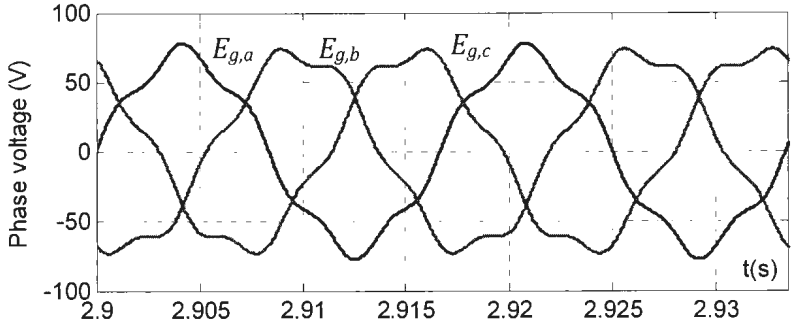


Figure 3-31: Distorted three phase voltage supply

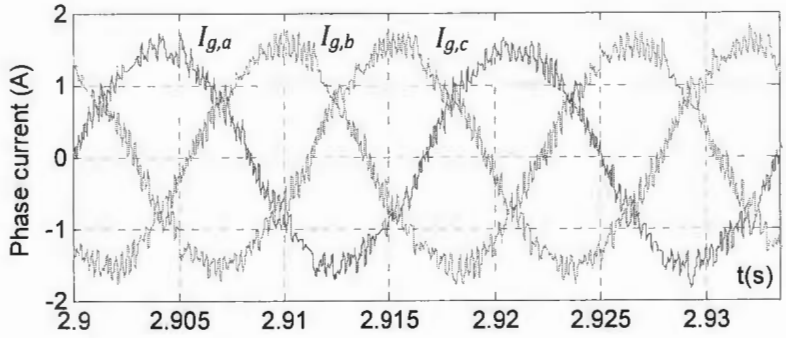


Figure 3-32: Three phase input currents are maintained under distorted three phase input voltage

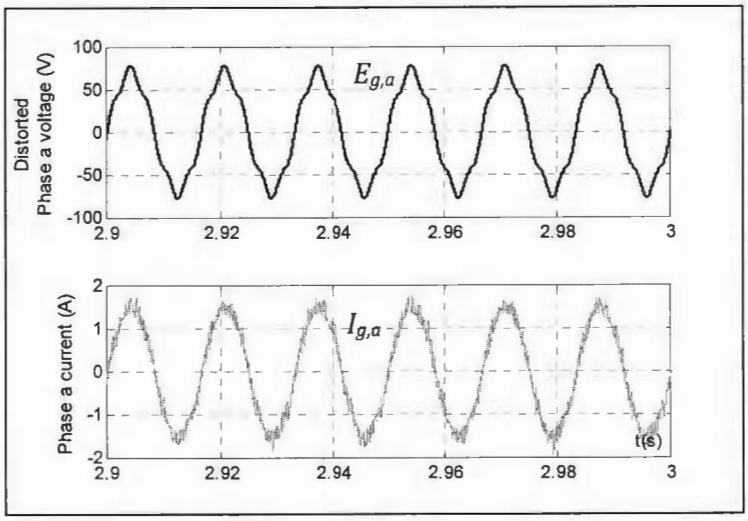


Figure 3-33: Phase *a* voltage and current are in phase at unity power factor

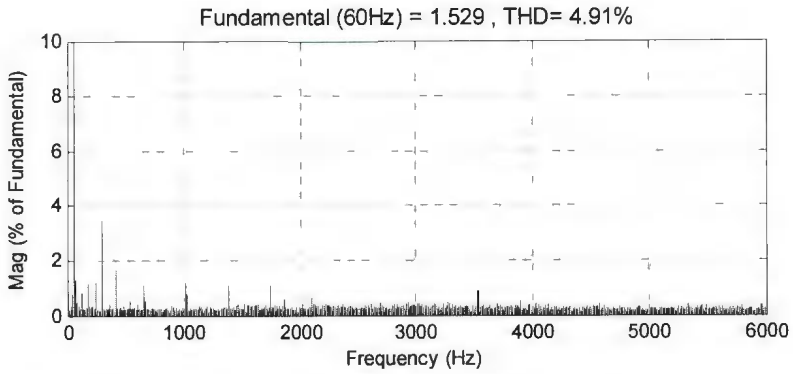


Figure 3-34: Harmonic spectrum of the line current under distorted voltage supply

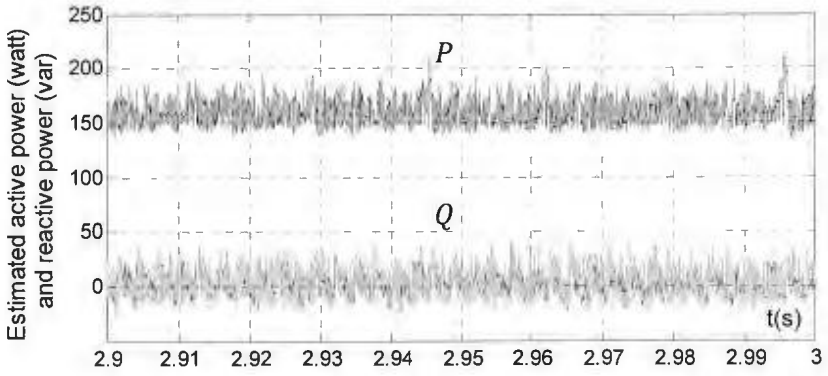


Figure 3-35: Estimated active power P, and reactive power Q under distorted voltage supply and unity power factor operation

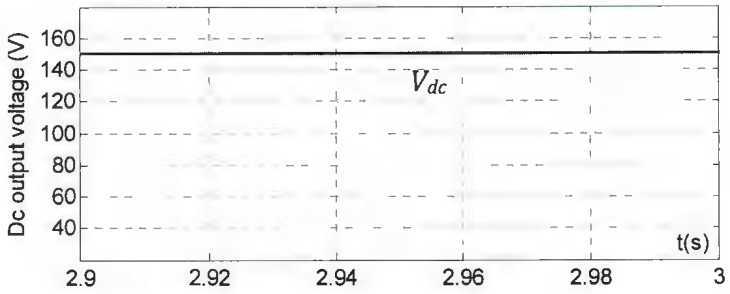


Figure 3-36: Generated dc-link output voltage

3.8.1 Analysis of the Conventional Direct Power Control under Distorted Three Phase Voltage Supply

The three phase ac to dc converter utilizing the conventional Direct Power Control (DPC) method working with a newly developed switching look-up table as shown in Figure 3-1 is also studied to evaluate the converter performance under a distorted three phase voltage supply. As mentioned in the previous analysis of the proposed VFDPC under distorted input voltage, the voltage distortion is obtained by injecting 10% of a magnitude of the fundamental component into the fifth harmonic component of the positive sequence of the three phase voltage supply. The three phase voltages and currents are measured to obtain the input instantaneous active and reactive power. The measured three phase grid voltage is also used to calculate the grid voltage vector and to determine the twelve sector locations of the switching look-up table.

The generated three phase current waveforms under distorted grid voltage can be clearly observed in Figure 3-37 and Figure 3-38. The input currents are obviously distorted and therefore, the currents at each phase are not identical in shape. Consequently, Figure 3-39 reveals that the conventional DPC with new switching table produces line current THD of 8.69% which is much higher than the current THD obtained from the proposed VFDPC. The proposed VFDPC utilizing new switching table generates 4.66% current THD which has been discussed in previous subchapter. The estimated active power and reactive power waveforms are shown in Figure 3-40. Even though the conventional DPC generates distorted line currents,

the dc voltage PI regulator at the output side of the converter is still able to track the dc voltage command to produce the dc output voltage of 150 V as shown in Figure 3-41.

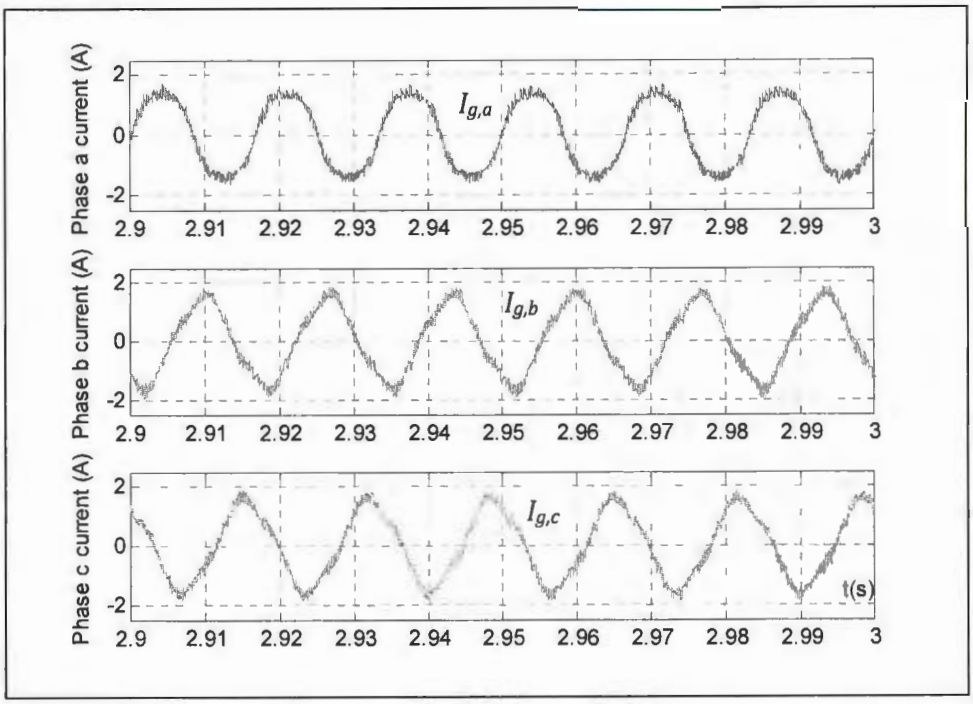


Figure 3-37: Distorted three phase input currents generated by the conventional DPC method

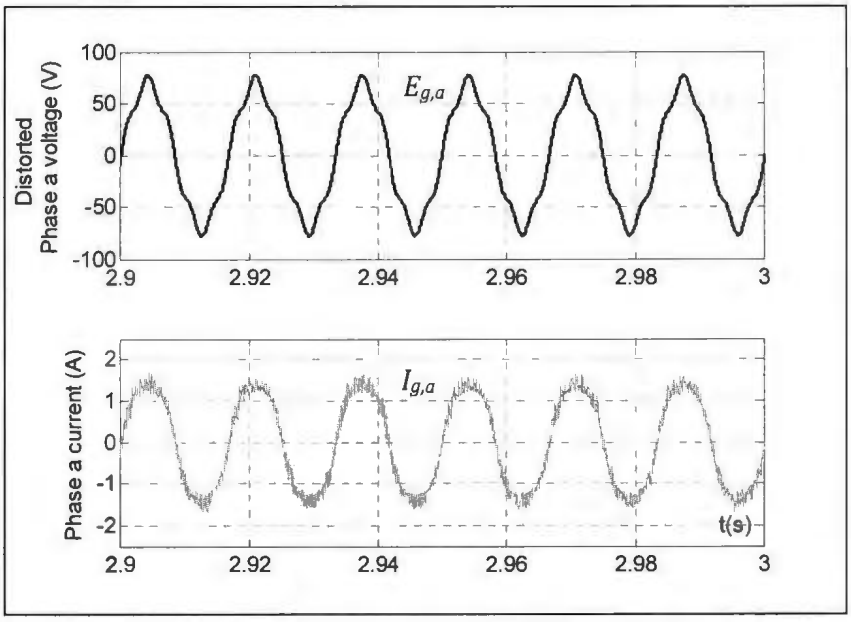


Figure 3-38: Phase *a* voltage and current at unity power factor

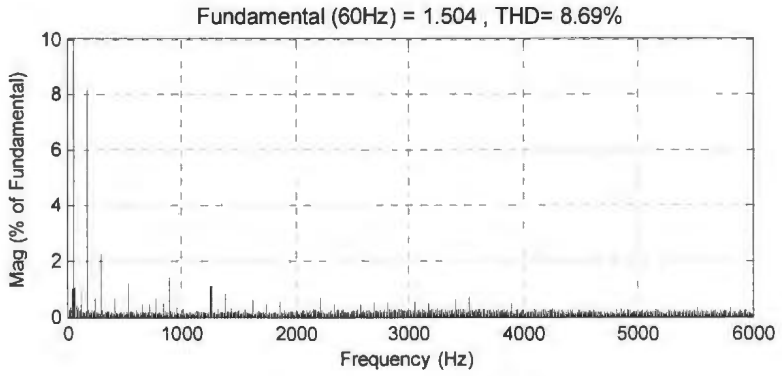


Figure 3-39: Harmonic spectrum of the phase *a* current

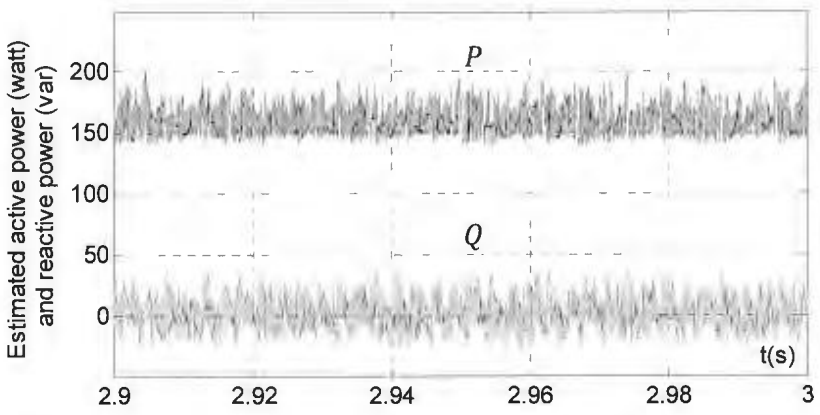


Figure 3-40: Estimated active power P, and reactive power Q under distorted voltage supply and unity power factor operation

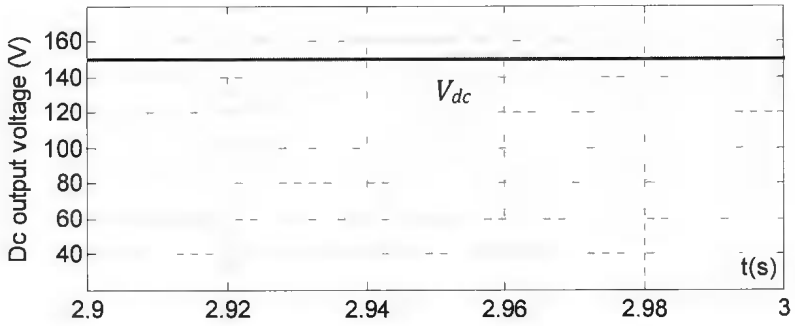


Figure 3-41: Generated dc-link output voltage

3.9 Simulation Results and Performance Analysis of the Proposed Virtual Flux Direct Power Control under Unbalanced Three Phase Voltage Supply

Unbalanced three phase voltage supply is very common in a weak ac system. The unbalanced phenomenon can be arising from single phase loads that are unevenly distributed in the grid system or the employment of a transformer with nonsymmetrical windings in the front-end of the rectifier system. Therefore it is essential to evaluate the feasibility and performance of the proposed VFDPC under an unbalanced voltage input condition. The unbalanced voltage supply condition in a simulation platform is achieved by decreasing the magnitude of the phase *a* voltage by 15% compared to the balanced case. The input voltage imbalance generates significant low frequency harmonic components in the input and output currents of the ac-dc converter. Under an unbalanced voltage condition, the ac input currents and the converter dc output current consist of even harmonic components in the order of 2, 4, 8, and so on. These harmonic components will increase the THD of the line input currents if no proper control action is taken to compensate for those harmonics.

Figure 3-42 shows the unbalanced three phase voltage with reduced magnitude on the phase *a* voltage. The proposed control scheme is able to maintain almost sinusoidal three phase currents with minimum distortion and unity power factor as shown in Figure 3-43 and Figure 3-44. As shown by the input current harmonic

spectrum in Figure 3-45, the line current THD is 4.78% which is slightly higher than the line current THD obtained during balanced input voltage.

The estimated reactive power Q is maintained at 0 var for a unity power factor operation as shown in Figure 3-46. The estimated active power P oscillates slightly due mainly to the second order harmonic component from the unbalanced input voltage condition. The second order harmonic also creates ripples to the dc output voltage as shown in Figure 3-30. The ripples have a frequency twice the fundamental frequency of 60 Hz. However this ripple can be further reduced by increasing the dc-link capacitance.

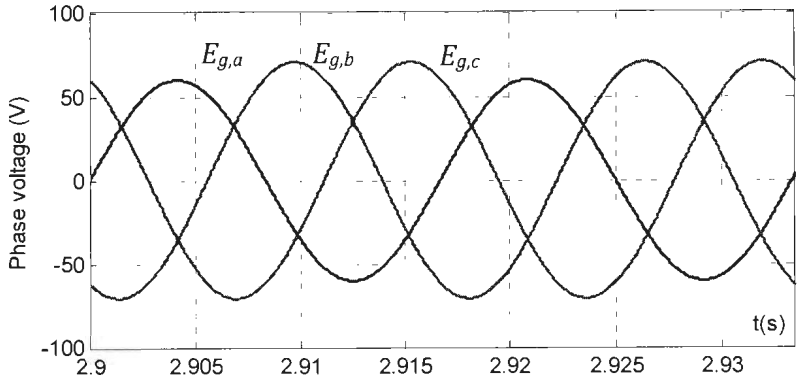


Figure 3-42: Unbalanced three phase supply voltages. The magnitude of phase *a* voltage decreases 15% from the balanced case

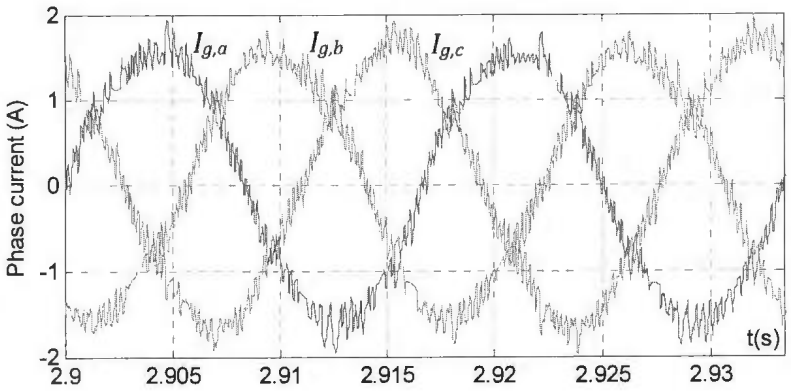


Figure 3-43: Three phase input currents

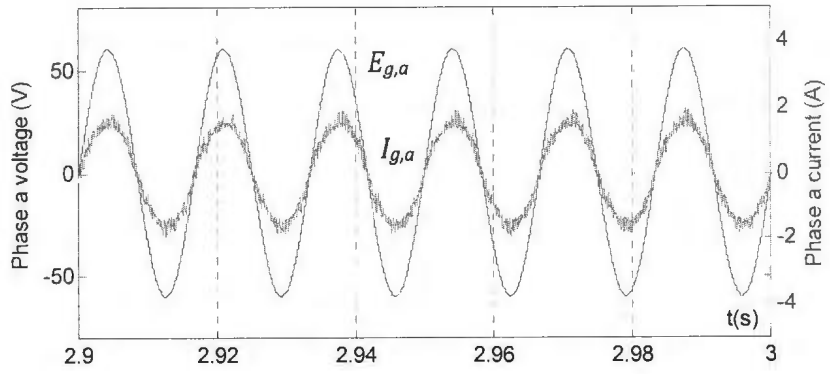


Figure 3-44: Phase *a* voltage and current at unity power factor operation

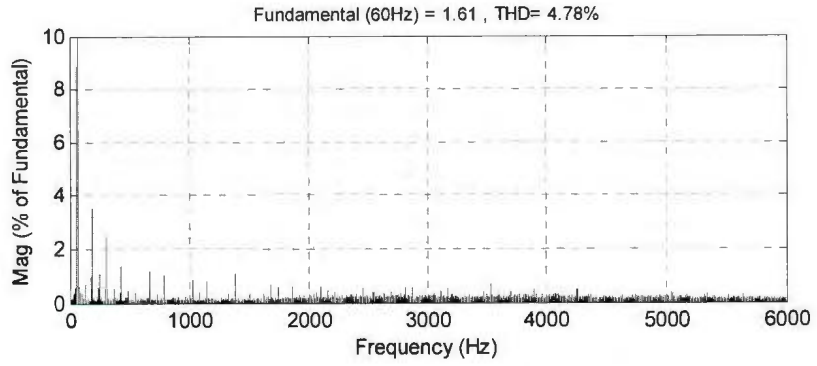


Figure 3-45: Harmonic spectrum of the line current

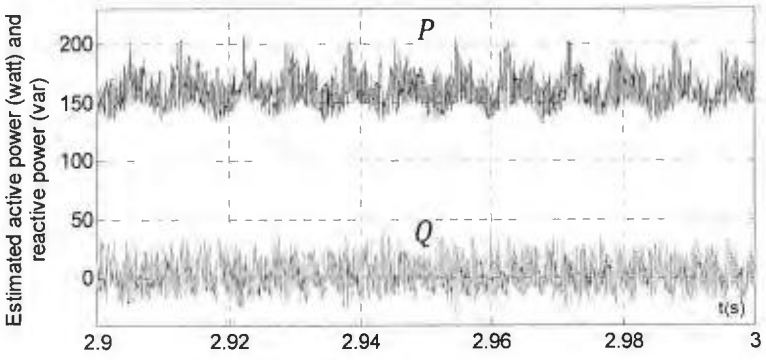


Figure 3-46: Estimated input instantaneous active power *P*, and reactive power *Q* during unity power factor operation

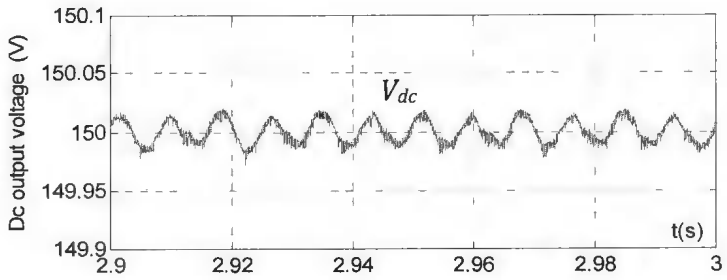


Figure 3-47: Generated dc-link output voltage for unbalanced input voltage

3.9.1 Analysis of the Conventional Direct Power Control under Unbalanced Three Phase Voltage Supply

The front-end ac-dc converter under input voltage imbalance, utilizing the conventional Direct Power Control (DPC) is also simulated to compare the performance of both the proposed and the conventional control methods. The waveforms of three phase currents produced by the conventional DPC under the unbalanced grid voltage supply condition and unity power factor operation are shown in Figure 3-48. It can be observed that the currents are distorted mainly by

the even low order harmonic components which are generated by the unbalanced three phase voltage supply. The generated current is in phase with its associate phase voltage during unity power factor mode as shown by the phase *a* voltage and current in Figure 3-49. Subsequently, Figure 3-50 shows that the line current THD is 6.80% which is slightly higher than the current THD obtained from the VFDPC under the same unbalanced input voltage condition. The estimated instantaneous power and the dc-link output voltage waveforms are shown in Figure 3-51 and Figure 3-52, respectively. The estimated reactive power Q is maintained at the reference value of 0 var for a unity power factor operation. The conventional DPC is able to produce the dc output voltage according to the command dc voltage of 150V. However, the dc-link output voltage contains a small amount of ripples due to the low order harmonics, mainly the second harmonic generated by the imbalanced input voltage.

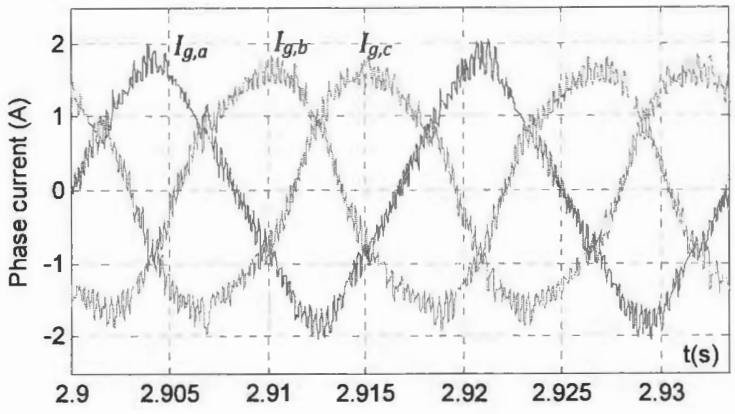


Figure 3-48: Distorted three phased input currents produced by the conventional DPC under unbalanced three phase input voltage

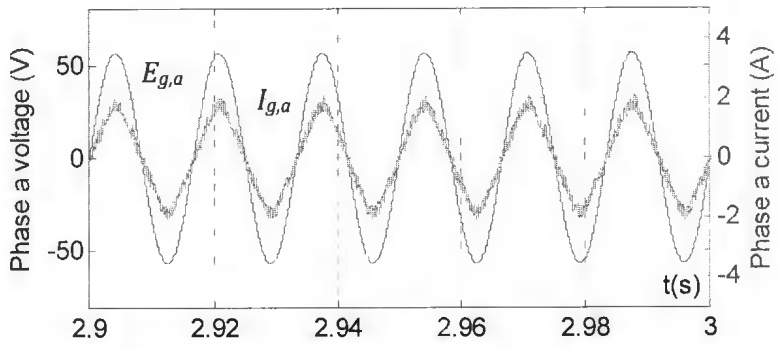


Figure 3-49: Phase *a* voltage and current at unity power factor

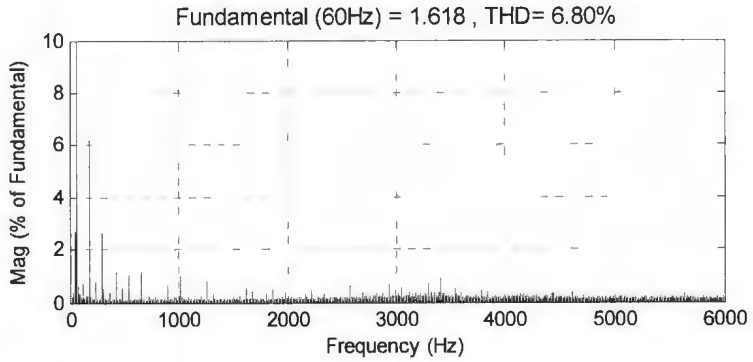


Figure 3-50: Harmonic spectrum of the line current

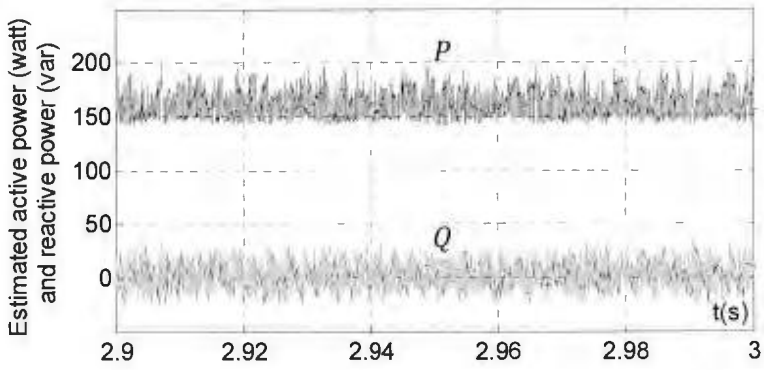


Figure 3-51: Estimated active power *P*, and reactive power *Q* under unbalanced voltage supply and unity power factor operation

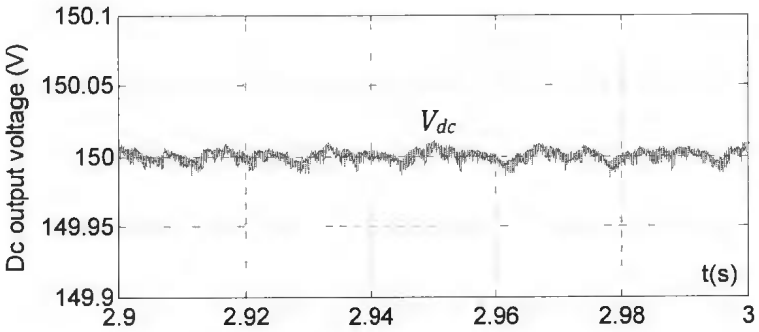


Figure 3-52: Generated dc-link output voltage

3.10 Implementation and Experimental Results of the Proposed Virtual Flux Direct Power Control

The development of the control algorithm is performed using Matlab/Simulink and the real-time implementation with the dSPACE DS1104 digital signal processing (DSP) board inserted in a desktop computer. The experimental prototype of the ac-dc converter system has been developed in the Memorial University of Newfoundland (MUN) Power Devices and System Research Laboratory to study and examine the proposed Virtual Flux Direct Power Control (VFDPC) scheme. The main hardware configuration for the experimental set-up is shown by the block diagram of Figure 3-53. The detailed description of the experimental set-up is presented in Chapter 5. The set-up consists of a three phase grid supply, three phase transformer, line inductors, ac-dc converter power circuit, gate drivers and isolation, dc-link capacitor, variable resistive load, voltage and current sensors, and DSP controller board.

The system parameters used in both the simulation and experiment are similar and given in Table 3-4. The sampling time T_s for real-time implementation has been increased to 66.667μs or 15kHz sampling frequency because the speed limitation of the DSP board.

A large capacitance of the dc-link capacitor at the output of the ac-dc converter acts like a short circuit across the three phase supply if no proper start up method is implemented during the initial operation of the front-end PWM rectifier system. High current will flow continuously through the capacitor until the capacitor builds

up sufficient voltage. This condition will result in a large starting current which can disturb the supply ac voltage, blow the line fuses or damage the switching devices such as IGBTs and bridge diodes. Therefore a systematic approach of starting up the ac-dc converter system unit is necessary.

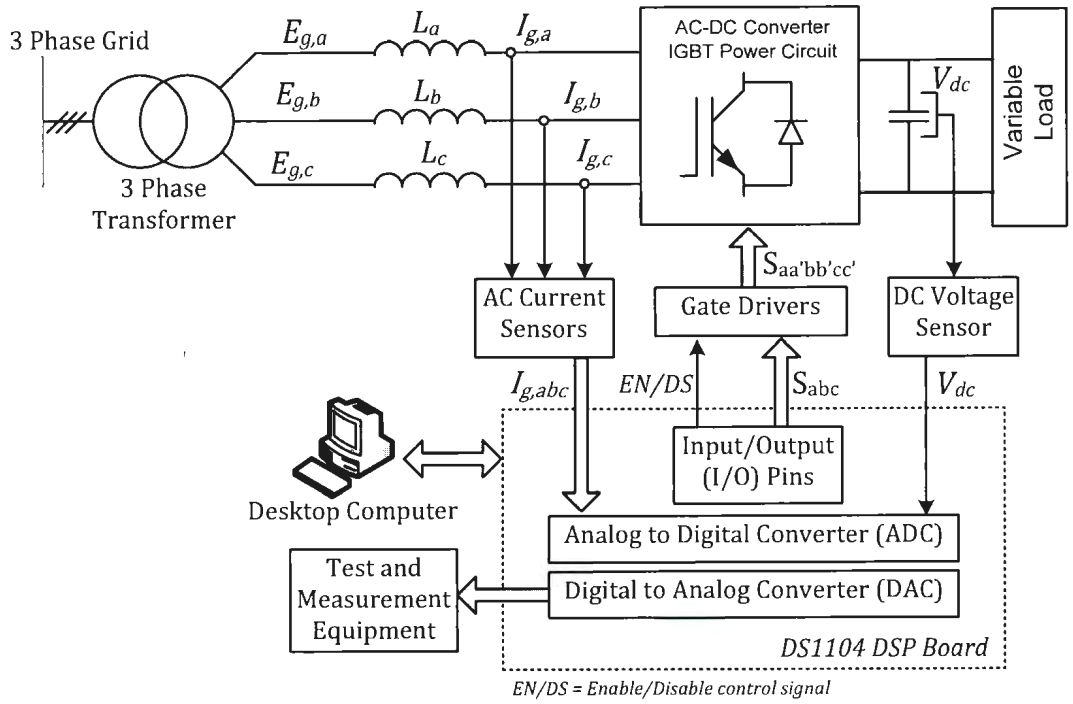


Figure 3-53: Configuration of the experimental set-up for Virtual Flux Direct Power Control (VFDPC)

In the proposed control method, the following way of charging up the unit is established. The capacitor is precharged to a certain dc voltage value V_{dc} through the anti-parallel diode of the IGBT switches. In the next step, the DSP is activated so that the initial grid virtual flux vector components and angle can be computed. At this

stage, the gating signals from the gate driver modules are disabled by a control signal received from the DSP board. The significant waveforms during the three phase diode bridge rectifier operating mode such as the dc output voltage V_{dc}, the grid flux angle θ, a real component of the grid virtual flux vector $\Psi_{g,\alpha}$ and the phase a current $I_{g,a}$, are shown in Figure 3-54.

The gating signals for the IGBTs are activated by enabling the gate drive modules through the control signal received from the DSP board. The control strategy will generate appropriate switching signals according to the switching look-up table so that the ac-dc converter system produces a dc output voltage according to the reference dc voltage value which is higher than the precharged voltage. The dc output voltage is slightly increased during the PWM rectifier mode until the system establishes the steady state operation as shown in Figure 3-54. The effectiveness of the virtual flux estimation and the angle calculation can be observed clearly in the same figure. The consistency of the grid virtual flux vector angle θ waveform during both, the diode rectifier and the PWM rectifier modes, and a sinusoidal shape with correct phase angle of the grid virtual flux vector components which are denoted by $\Psi_{g,\alpha}$ and $\Psi_{g,\beta}$, will ensure the generation of sinusoidal phase currents as shown in the same figure.

The efficacy of the virtual flux estimation and compensation procedures can be observed in Figure 3-55. The imaginary component of the grid virtual flux $\Psi_{g,\beta}$ is lagging the real component of the grid virtual flux $\Psi_{g,\alpha}$ by 90°. Both components are used by the phase locked loop to calculate the grid virtual flux vector angle. The

resultant of the grid virtual flux vector angle waveform θ, is also shown in Figure 3-55. The angle information is then used to generate the twelve sectors for the switching table.

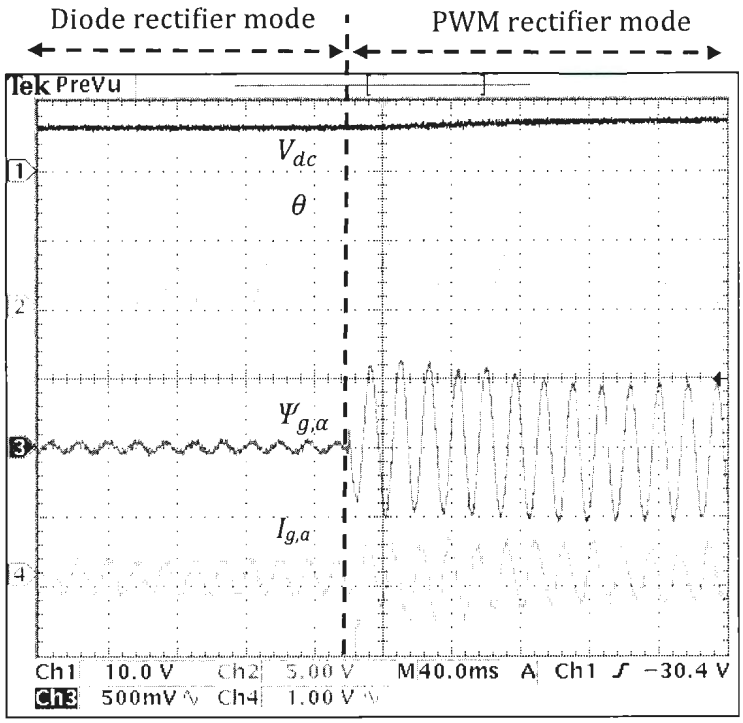


Figure 3-54: Waveforms of some main components during start up process. From top: Dc output voltage (250V/div), grid virtual flux angle (rad/s), real component of grid virtual flux (0.25wb/div), and phase *a* current (5A/div)

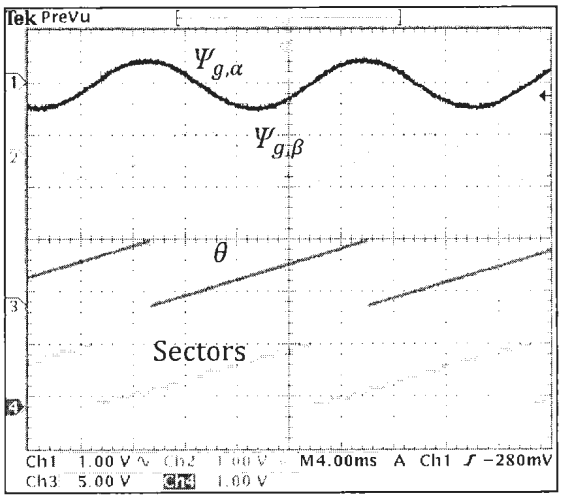


Figure 3-55: Waveforms obtained during the PWM rectifier mode. From top: Grid virtual flux in stationary reference frame, grid virtual flux vector angle, and 12 sectors

Figure 3-56 shows the three phase currents generated by the proposed VFDPC. The VFOC is able to produce almost sinusoidal currents with unity power factor operation. The phase voltages are in phase with their associate phase currents as shown in Figure 3-57.

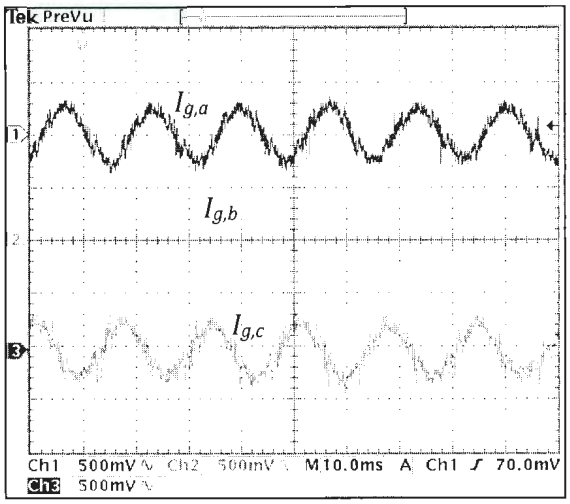


Figure 3-56: Three phase input currents (2.5A/div)

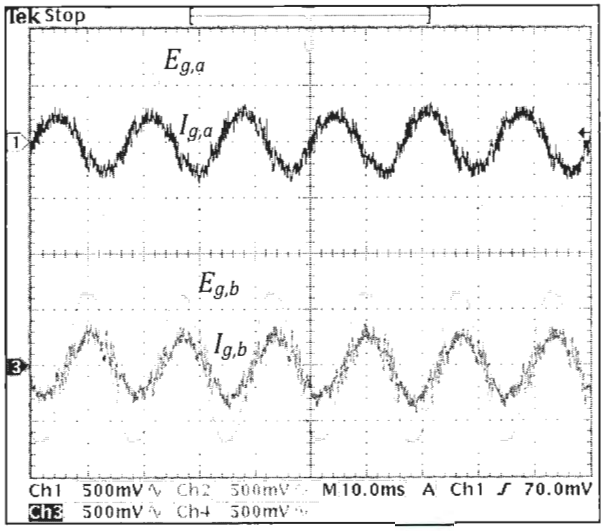


Figure 3-57: Phase voltages (75V/div) and currents (2.5A/div) at unity power factor. From top: Phase *a* voltage and current, Phase *b* voltage and current

The performance of the proposed VFDPC can be further analyzed from the input current harmonic spectrum shown in Figure 3-58. The current fundamental component is located at 60Hz as shown by the highest peak of the spectrum. The low amplitude of the rest harmonic components gives confirmation of the low total harmonic distortion in the line currents. The estimated input active power P and reactive power Q waveforms are presented in Figure 3-59. The reactive power reference Q_{ref} is set to zero to obtain unity power factor operation so that the phase voltages are in phase with their associate phase currents.

The front-end PWM ac-dc converter utilizing the proposed VFDPC is also able to produce either a leading or lagging power factor operation by providing proper value to the reference power Q_{ref}. The power factor can be calculated by using

equation (3.88). Base on that equation, the power factor *pf* is one if the reactive power is set to zero. The reference reactive power is set to about -160 var and +103

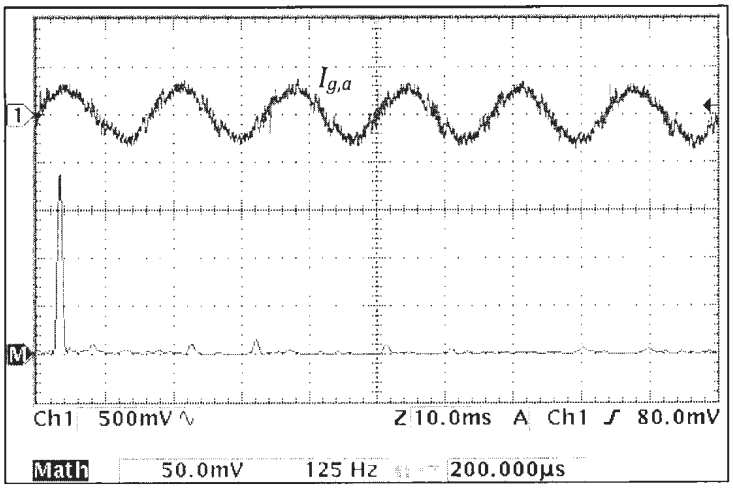


Figure 3-58: Harmonic spectrum of the input line current

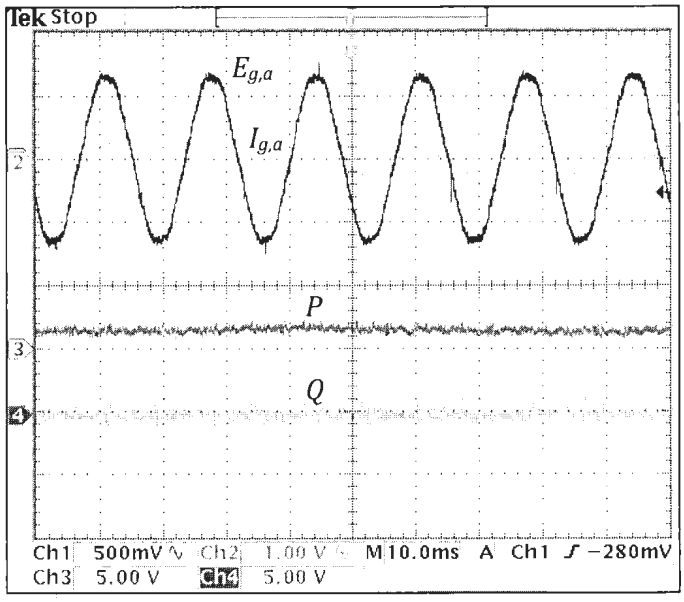


Figure 3-59: Generated waveforms during unity power factor. From top: Phase *a* voltage (75V/div) and current (5A/div), estimated input instantaneous active power *P* (625W/div), and reactive power *Q* (625Var/div)

var to demonstrate a leading and lagging power factor operation, respectively. Figure 3-60 and Figure 3-61 show the resultant waveforms from both power factor operation modes. The phase *a* current is leading the phase *a* voltage during leading power factor. On the other hand, the phase *a* current lags its associate phase voltage during lagging power factor mode. The estimated active power *P* does not change so much for both operation modes.

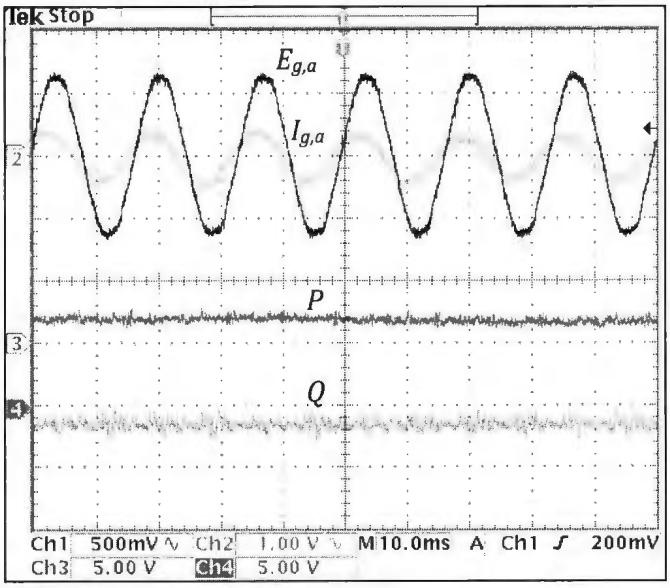


Figure 3-60: Generated waveforms during leading power factor. From top: Phase *a* voltage (75V/div) and current (5A/div), estimated input instantaneous active power *P* (625W/div), and reactive power *Q* (625Var/div)

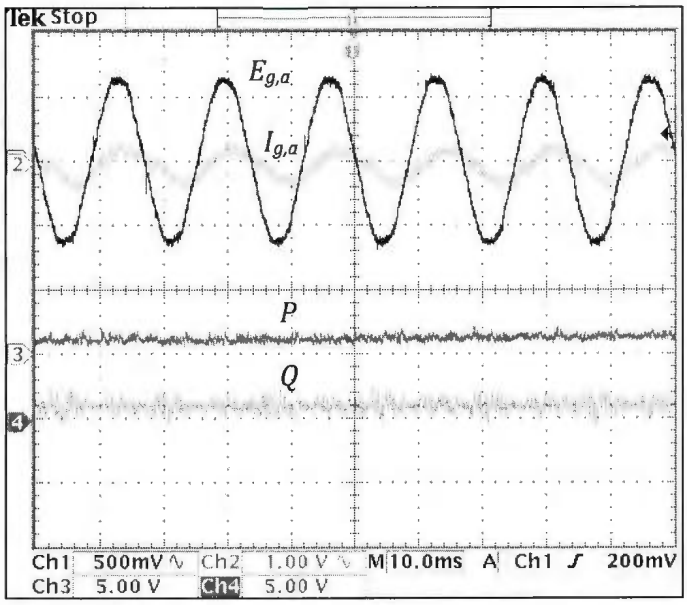


Figure 3-61: Generated waveforms during lagging power factor. From top: Phase *a* voltage (75V/div) and current (5A/div), estimated input instantaneous active power *P* (625W/div), and reactive power *Q* (625Var/div)

Experimental tests are also conducted to verify the dynamic performance of the proposed VFDPC. Figure 3-62 shows transient responses for rapid change of load power under unity power factor operation. The additional resistors are abruptly connected in parallel with the existing resistor at the output of the PWM rectifier to cause a sudden increase in the load power. As a result, the estimated input active power P and the phase currents increase simultaneously to fulfill the load power demand. The proposed control method is able to maintain the dc-link output voltage at the reference value of 150 V and the sinusoidal line currents with unity power factor. The estimated reactive power Q is kept at 0 var to maintain unity power factor operation of the PWM rectifier.

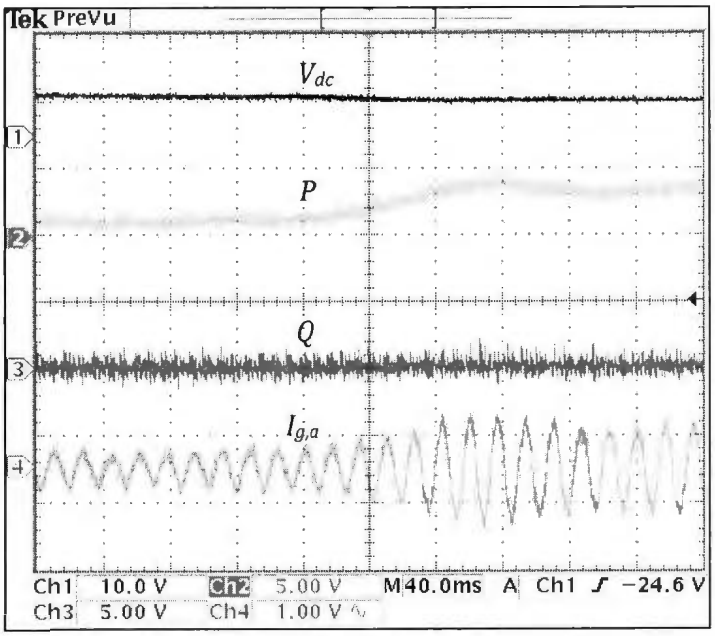


Figure 3-62: Transient response for load power increasing 143%. From top: Dc-link output voltage (250V/div), estimated input active power (625W/div), estimated input reactive power (625Var/div), and phase *a* current (5A/div)

Evaluation of the dynamic response under the change of load power from high to low power demand is performed by instantly disconnecting the additional resistors in parallel with the existing load resistor of 140 Ω. Figure 3-63 shows the transient responses during this condition. The input estimated active power P and the phase current are decreasing concurrently to meet the decreasing of the load demand. The dc output voltage level is kept almost constant at its reference value of 150 V while maintaining the sinusoidal line currents flowing through the ac-dc converter system.

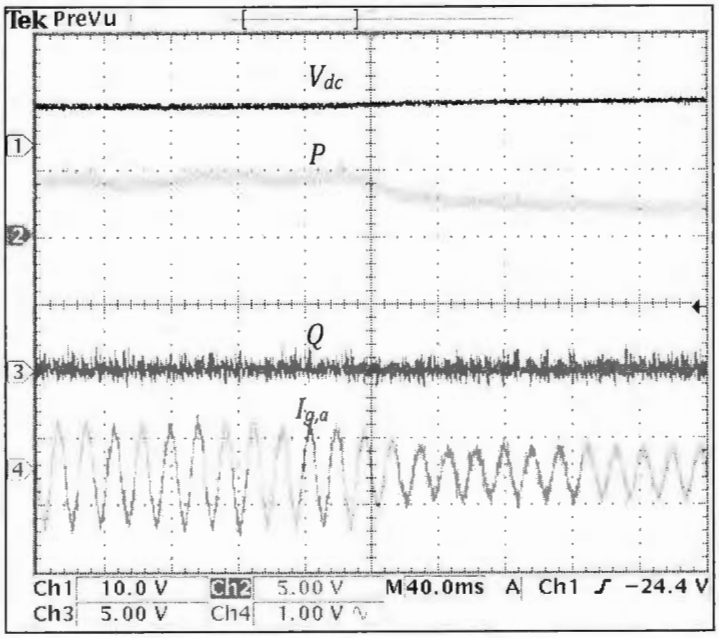


Figure 3-63: Transient response for load power decreasing 143%. From top: Dc-link output voltage (250V/div), estimated input active power (625W/div), estimated reactive power (625Var/div), and phase *a* current (5A/div)

A dynamic behavior of the front-end rectifier under a step change in output voltage reference is shown in Figure 3-64 and Figure 3-65. In Figure 3-64, the dc output voltage increases according to a change of the dc voltage reference from 150 V to 235 V. On the other hand, the dc output voltage decreases following the change of the dc voltage reference from 235 V back to 150 V as shown in Figure 3-65. The estimated active power P is also increased and decreased steadily to new values during the changes of output voltage while maintaining the estimated reactive power Q at 0 var. The proposed control method is able to generate almost sinusoidal phase currents with low THD and unity power factor before and after the changes of the dc output voltage reference.

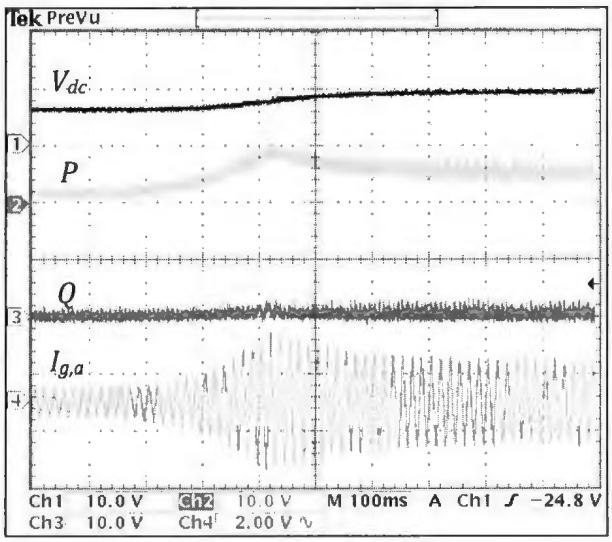


Figure 3-64: Dynamic response during a change in dc voltage reference from 150 to 235 V. From top: Dc-link output voltage (250V/div), estimated input active power (625W/div), estimated reactive power (625Var/div), and phase *a* current (10A/div)

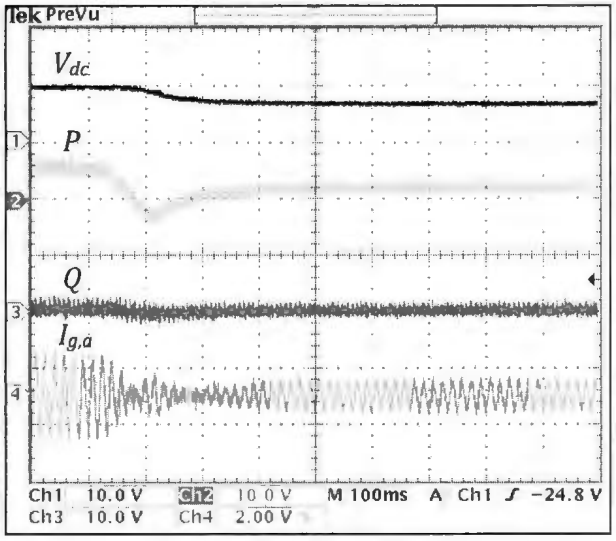


Figure 3-65: Dynamic responses during a change in dc voltage reference from 235 to 150 V. From top: Dc-link output voltage (250V/div), estimated input active power (625W/div), estimated reactive power (625Var/div), and phase *a* current (10A/div)

3.11 Experimental Results of the Virtual Flux Direct Power Control utilizing Conventional Switching Look-up Table

Experimental work is also conducted to evaluate and compare the performance of both the VFDPC utilizing the new developed switching table and the VFDPC working with the conventional switching look-up table as presented by the authors in [22] and [36]. The conventional switching table is given in Table 3-5. Figure 3-66 and Figure 3-67 represent the three phase currents during steady state and unity power factor operation mode. The input currents in all phases are distorted due to the unsuitable and non-optimal voltage vectors selected by the conventional switching table to operate the PWM rectifier. The selection of those voltage vectors will degrade the estimation of the input active and reactive powers. As a result, the waveforms of the estimated active and reactive power as shown in Figure 3-68 consist with significant ripple components. The current harmonic spectrum from the experiment as presented in Figure 3-69 gives confirmation of the previous simulation results that the conventional switching table generates higher THD of input current in comparison with the THD current produced by a newly developed switching table.

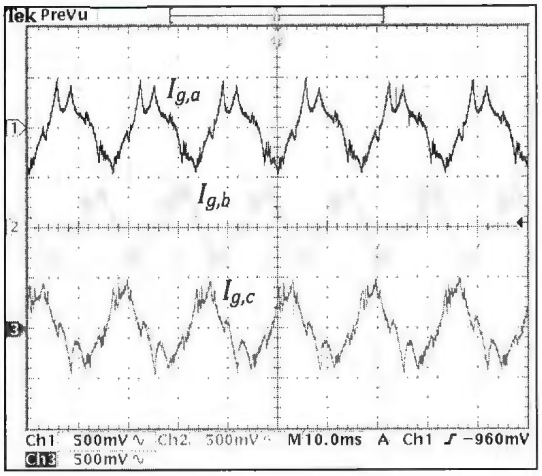


Figure 3-66: Three phase input currents produced by VFDPC with conventional switching table (2.5A/div)

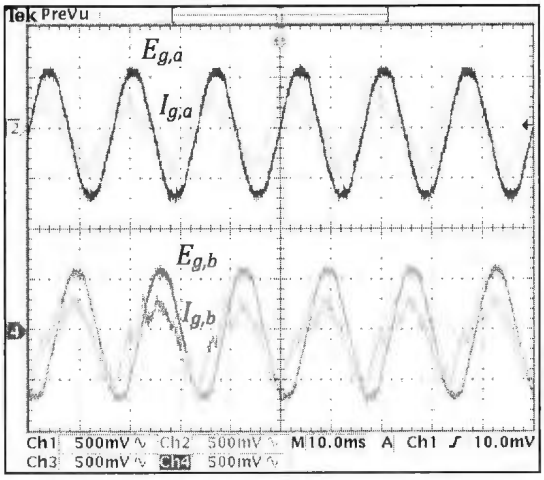


Figure 3-67: Phase voltages (75V/div) and currents (2.5A/div) at unity power factor. From top: Phase *a* voltage and current, Phase *b* voltage and current

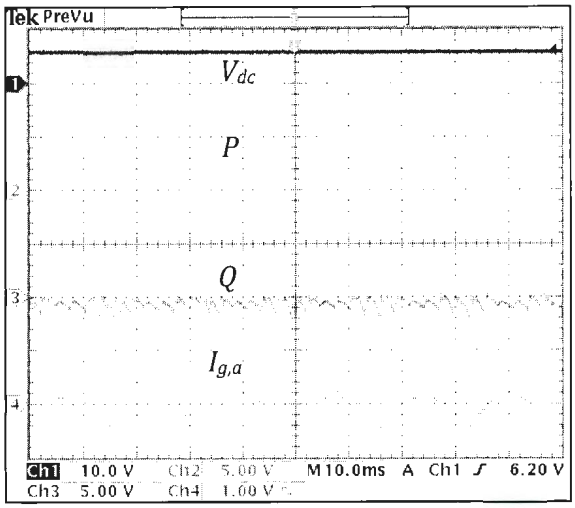


Figure 3-68: Generated waveforms during steady state and unity pf. Dc-link output voltage (250V/div), estimated input active power (625W/div), estimated input reactive power (625var/div), and phase *a* current (5A/div)

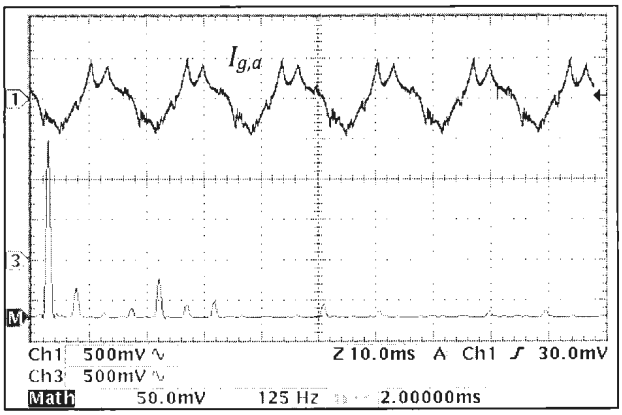


Figure 3-69: Harmonic spectrum of the input line current

3.12 Experimental Results of the Proposed Virtual Flux Direct Power Control under Unbalanced Three Phase Voltage Supply

Performance of the proposed VFDPC utilizing a newly developed switching look-up table is also experimentally studied during imbalanced three phase voltage supply condition. The magnitude of phase *a* voltage is decreased to 66% of the voltage magnitude during the balanced condition, while the remaining phase *b* and phase *c* are kept at their original values during the balanced voltage condition. Figure 3-70 shows the experimental unbalanced three phase voltage waveforms with reduce magnitude on the phase *a* voltage. The VFDPC scheme is able to produce almost sinusoidal three phase currents with unity power factor and low total harmonic distortion as shown in Figure 3-71 and Figure 3-72.

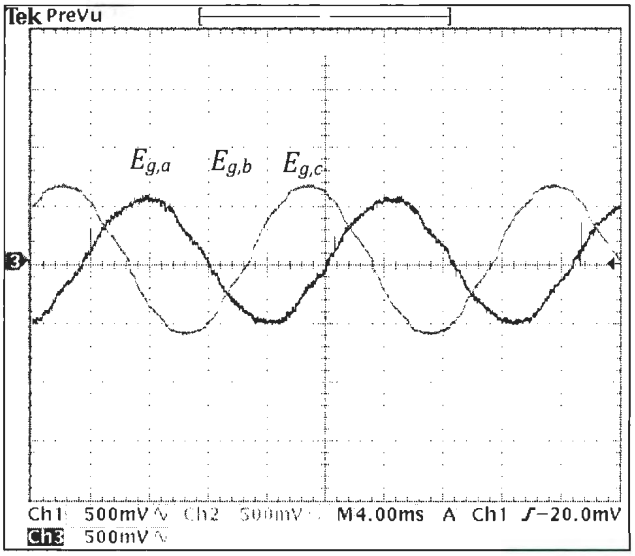


Figure 3-70: Unbalanced three phase input voltages (75V/div)

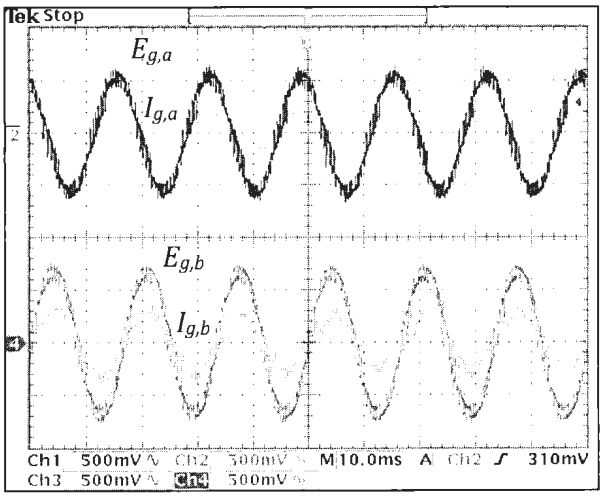


Figure 3-71: Phase voltages (75V/div) and currents (2.5A/div) at unity power factor. From top: Phase *a* voltage and current, Phase *b* voltage and current

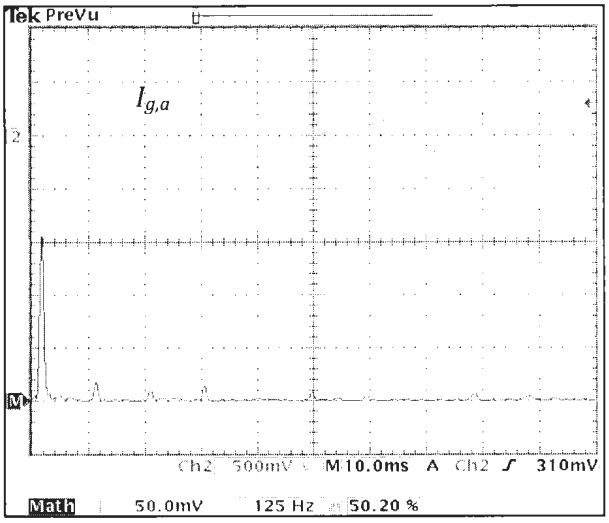


Figure 3-72: Harmonic spectrum of the input line current

Waveforms of the generated dc-link voltage V_{dc}, estimated active power P, estimated reactive power Q and grid phase a current $I_{g,a}$ during the steady state condition are shown in Figure 3-73. The estimated reactive power Q is maintained at

0 var for a unity power factor operation. The estimated active power P is oscillates slightly due mainly to the second order harmonic component generated from the unbalanced voltage supply condition. The dc-link capacitor effectively reduces the dc voltage output ripples caused by the second harmonic component.

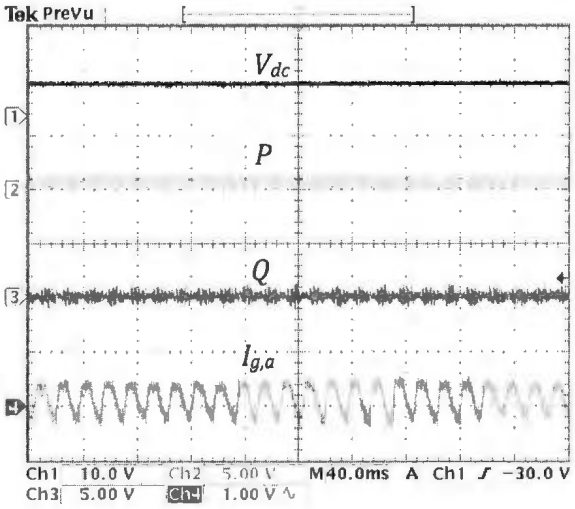


Figure 3-73: Steady state response. From top: Dc-link output voltage V_{dc} (250V/div), estimated input active power (625W/div) and estimated reactive power (625Var/div), and phase *a* current (5A/div)

Figure 3-74 shows the experimental waveforms obtained during rapid change of load power. The active power P and the phase a current $I_{g,a}$ increase simultaneously to fulfill increases of the load power demand. The reactive power Q is maintained at 0 var and the dc-link voltage is slightly reduced from its reference value.

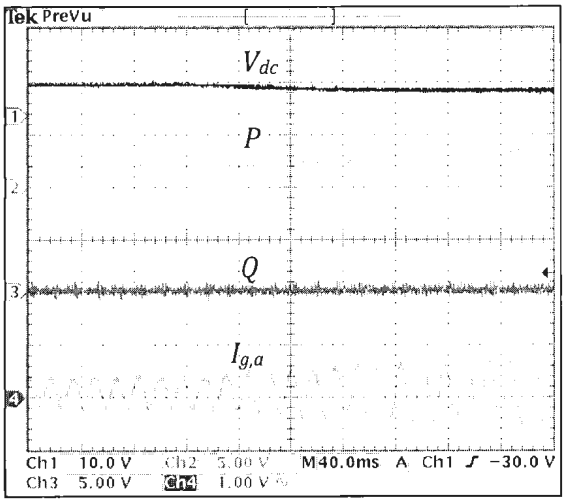


Figure 3-74: Transient response for load power increasing 143%. From top: Dc-link output voltage (250V/div), estimated input active power (625W/div), estimated input reactive power (625Var/div), and phase *a* current (5A/div)

3.13 Chapter Summary and Discussions

This chapter presents a new control scheme for the pulse width modulated three phase ac-dc voltage source converter without employing any voltage sensors to measure the three phase voltage supply. The Virtual Flux Direct Power Control (VFDPC) scheme utilizes only three current sensors for measuring the three phase currents, and a voltage sensor for measuring the dc-link output voltage. Therefore, the size and cost of the ac-dc converter system can be reduced. The proposed VFDPC has been successfully developed, simulated and implemented by estimating the grid virtual flux and the instantaneous active and reactive powers. Selection of the suitable converter voltage vector for switching purpose is performed by a newly designed switching look-up table. A comprehensive and systematic approach has been presented in developing the switching table. In addition, a compensation method to correct the magnitude and phase errors of the virtual flux estimation is introduced in this work. The proposed control scheme utilizes two hysteresis controllers in the power control loops and a discrete proportional integrator (PI) in the outer loop for regulating the dc-link output voltage.

The simulation results show that the proposed VFDPC is able to produce three phase input currents with low total harmonic distortion, unity power factor, changeable power factor operation mode, and adjustable dc-link output voltage. The real-time implementation of the ac-dc converter system incorporating the proposed virtual flux control technique is performed with the DS1104 digital signal processing board slotted in the desktop computer. There exists close agreement between the

simulated and experimental performance during both steady states and transient conditions. Moreover, the newly developed switching table generates lower harmonic distortion of line currents than the conventional switching table does.

Chapter 4

Development of the Grid Virtual Flux Oriented Control for the Three-Phase AC-DC Converter

4.1 Introduction

The basic idea of direct power control (DPC) is a direct control of active and reactive powers without any internal current control loop and pulse width modulator (PWM). The switching states are selected based on the error statuses which are denoted by d_P and d_Q, generated by two independent hysteresis controllers as shown in Figure 3-1 and Figure 3-2. The switching table has to be able to keep the error signals of desired and estimated active and reactive powers within the upper and lower hysteresis boundaries, by setting appropriate hysteresis bands and choosing the correct voltage vector for a particular grid voltage vector angle and load power demand. Although the hysteresis controller offers a fast dynamic response, it can be considered as a major factor responsible for the resulting variable switching frequency in the DPC method. Consequently, the current harmonic spectrum is spread into a wide frequency range and the maximum capabilities of the converter cannot be fully utilized.

In order to produce a fixed switching frequency while preserving the advantages of applying a virtual flux concept in the controller system, this chapter proposes a new approach for developing a controller which adopts the current

control technique used in voltage oriented control (VOC) and the power estimation method derived from the proposed virtual flux direct power control (VFDPC). The advantage of this approach is that the new developed control strategy which is known as virtual flux oriented control (VFOC) is less sensitive to line voltage variations because of a low-pass filter characteristic introduced by the virtual flux estimation procedure. The other benefit of VFOC is the absence of the voltage sensors to measure the grid three phase supply voltages, so that the whole system cost and size can be reduced.

4.2 Mathematical Model of the PWM Rectifier in a Synchronous Rotating *dq*-Reference Frame based on the Virtual Flux Concept

The proposed control scheme which is described as grid Virtual Flux Oriented Control (VFOC), is developed by combining the knowledge of the Voltage Oriented Control (VOC) scheme and the power estimation method derived in the direct power control based on grid virtual flux concept (VFDPC). The voltage equations of the PWM rectifier in the synchronous rotating *dq*-reference frame as shown in equations (4.1) and (4.2) cannot be implemented directly since no voltage sensors are employed to measure the three phase grid voltages. Consequently, the information of the three phase grid voltages is not available to obtain the grid voltages in a synchronous rotating reference frame as denoted by $E_{g,d}$ and $E_{g,q}$ in both equations.

$$E_{g,d} = RI_{g,d} + L\frac{dI_{g,d}}{dt} - \omega LI_{g,q} + V_{conv,d} \tag{4.1}$$

$$E_{g,q} = RI_{g,q} + L\frac{dI_{g,q}}{dt} + \omega LI_{g,d} + V_{conv,q} \tag{4.2}$$

Therefore, the estimation of the grid voltage equations in the *dq*-frame has to be made according to the virtual flux theory so that the proposed control scheme is able to utilize the decoupling and feed-forward components to enhance the performance of the PWM voltage source rectifier (VSR) during both balanced and unbalanced voltage supply conditions.

4.2.1 Derivation of the Proposed Mathematical Model for AC-DC Converter in a *dq*-Reference Frame

The voltage vector equation of ac-dc converter in a stationary $\alpha\beta$-reference frame is derived in a subchapter 2.3.2 and the final equation is given as:

$$\bar{E}_{g,\alpha\beta} = R\bar{I}_{g,\alpha\beta} + L\frac{d}{dt}\bar{I}_{g,\alpha\beta} + \bar{V}_{conv,\alpha\beta} \tag{4.3}$$

By manipulating the virtual flux definition as presented in equation (3.6), the three phase grid voltage vector $\bar{E}_{g,\alpha\beta}$ can be estimated by differentiating the grid flux vector $\overline{\Psi}_{g,\alpha\beta}$ as shown in (4.4).

$$\bar{E}_{g,\alpha\beta} = \frac{d}{dt}\overline{\Psi}_{g,\alpha\beta} \tag{4.4}$$

Equation (4.4) can be interpreted such that a time variation of the virtual flux vector results in the induced voltage vector.

The general relationship between $\alpha\beta$-reference frame and *dq*-reference frame vector components is given by

$$\bar{x}_{dq} = \bar{x}_{\alpha\beta} e^{-j\omega t} \tag{4.5}$$

where x represents the amplitude of any electrical quantity such as voltage, current or virtual flux. All components in stationary $\alpha\beta$-coordinates can be transformed into rotating dq-coordinates by using the transformation matrix given in (4.6). On the other hand, any components in rotating coordinates can be transformed into stationary coordinates by the transformation matrix equation shown in (4.7).

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{4.6}$$

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} x_d \\ x_q \end{bmatrix} \tag{4.7}$$

Hence, the relationship between the grid virtual flux vectors in the dq-frame and the $\alpha\beta$-frame can be derived as:

$$\bar{E}_{g,dq} = \bar{E}_{g,\alpha\beta} e^{-j\omega t}$$

$$\frac{d}{dt}\bar{\Psi}_{g,dq} = \frac{d}{dt}\bar{\Psi}_{g,\alpha\beta} e^{-j\omega t} \tag{4.8}$$

Rearrange equation (4.8), to obtain equation (4.9):

$$\frac{d}{dt}\bar{\Psi}_{g,\alpha\beta} = \frac{d}{dt}\bar{\Psi}_{g,dq} e^{j\omega t} \tag{4.9}$$

The grid current vector and the converter pole voltage vector in the stationary reference frame used in equation (4.3) can be transformed into the synchronous rotating reference frame by manipulating and rearranging equation (4.5). Subsequently, the voltage equation of ac-dc converter in the stationary reference frame as given in equation (4.3) can be represented and transformed into the synchronous reference frame as shown in equation (4.10).

$$\frac{d}{dt}\left(\bar{\Psi}_{g,dq}e^{j\omega t}\right) = R\bar{I}_{g,dq}e^{j\omega t} + L\frac{d}{dt}\left(\bar{I}_{g,dq}e^{j\omega t}\right) + \bar{V}_{conv,dq}e^{j\omega t} \tag{4.10}$$

It can be further resolved such as:

$$\begin{aligned}\frac{d\left(\bar{\Psi}_{g,dq}\right)}{dt}e^{j\omega t} + j\omega\bar{\Psi}_{g,dq}e^{j\omega t} \\ = R\bar{I}_{g,dq}e^{j\omega t} + L\frac{d\left(\bar{I}_{g,dq}\right)}{dt}e^{j\omega t} + j\omega L\bar{I}_{g,dq}e^{j\omega t} \\ + \bar{V}_{conv,dq}e^{j\omega t}\end{aligned} \tag{4.11}$$

$$\begin{aligned}\frac{d\left(\Psi_{g,d} + j\Psi_{g,q}\right)}{dt}e^{j\omega t} + j\omega\left(\Psi_{g,d} + j\Psi_{g,q}\right)e^{j\omega t} \\ = R\left(I_{g,d} + jI_{g,q}\right)e^{j\omega t} + L\frac{d\left(I_{g,d} + jI_{g,q}\right)}{dt}e^{j\omega t} \\ + j\omega L\left(I_{g,d} + jI_{g,q}\right)e^{j\omega t} + \left(V_{conv,d} + jV_{conv,q}\right)e^{j\omega t}\end{aligned} \tag{4.12}$$

As mentioned in subchapter 3.3, a derivative of the grid virtual flux vector in *dq*-coordinates $\frac{d\left(\Psi_{g,d}+j\Psi_{g,q}\right)}{dt}$, would vanish because $\Psi_{g,d}$ and $\Psi_{g,q}$ are the flux magnitude and are constant in the rotating synchronous frame. Therefore, splitting the real and imaginary parts of equation (4.12), will lead to the new voltage equations of the grid connected PWM VSR based on virtual flux in the *dq*-synchronous reference frame as shown in (4.13) and (4.14).

$$-\omega\Psi_{g,q} = RI_{g,d} + L\frac{dI_{g,d}}{dt} - \omega LI_{g,q} + V_{conv,d} \tag{4.13}$$

$$\omega\Psi_{g,d} = RI_{g,q} + L\frac{dI_{g,q}}{dt} + \omega LI_{g,d} + V_{conv,q} \tag{4.14}$$

The proposed VFOC method is synchronized with the grid virtual flux vector. Therefore the grid virtual flux angle θ is used by the transformation matrix given in equations (4.6) and (4.7). The angle θ can be calculated by using:

$$\theta = tan^{-1}\left(\frac{\Psi_{g,\beta}}{\Psi_{g,\alpha}}\right) \tag{4.15}$$

As the supply three phase voltages are not always purely sinusoidal and balanced, the grid virtual flux angle obtained by (4.15) may deteriorate. Therefore, a phase locked loop (PLL) is used to obtain the grid virtual flux vector angle. The PLL method used in this work is based on a synchronous reference frame of the grid virtual flux.

4.3 Estimation of the Current Vector References and Development of the Proposed Virtual Flux Oriented Control

The ideal integration that is used to calculate the grid virtual flux components as shown in equations (4.16) and (4.17) might saturate due to the integration drift caused by either noise or dc offsets present in the sensed current or voltage. Therefore, a low-pass filter normally replaces the pure integrator. However, a simple first-order low-pass filter will reduce the system performance because it produces errors in phase and magnitude of the virtual flux components. In order to minimize these errors, the phase and magnitude compensation method that has been previously presented in subchapter 3.2 is adopted in the virtual flux estimation procedure used in the proposed VFOC.

$$\Psi_{g,\alpha} = \int V_{conv,\alpha} dt + LI_{g,\alpha} \tag{4.16}$$

$$\Psi_{g,\beta} = \int V_{conv,\beta} dt + LI_{g,\beta} \tag{4.17}$$

The proposed VFOC exploits direct current vector control in the *dq*-coordinates by comparing the reference current and the measured current components in order to generate the correct voltage reference signals to the sinusoidal pulse width modulator (SPWM). Three current sensors are used to measure the actual three phase input currents. The three phase currents are transformed into the *dq*-coordinates by using the frame transformation matrix given by equations (2.17) and (4.6).

The reference current vector components $I_{g,d,ref}$ and $I_{g,q,ref}$, are calculated by manipulating the equations of instantaneous active and reactive power in the synchronous rotating reference frame which have been derived previously in subchapter 3.3.1. The estimated instantaneous active power P and reactive power Q in a synchronous reference frame are given by equations (4.18) and (4.19), respectively. Manipulating both power equations, the reference currents in *dq*-coordinates used by the proposed VFOC method can be written as shown in equations (4.20) and (4.21).

$$P = \frac{3}{2}\omega\left(\Psi_{g,d} I_{g,q} - \Psi_{g,q} I_{g,d}\right) \tag{4.18}$$

$$Q = \frac{3}{2}\omega\left(\Psi_{g,d} I_{g,d} + \Psi_{g,q} I_{g,q}\right) \tag{4.19}$$

$$I_{g,d,ref} = 2/3\left(\frac{-\Psi_{g,q}P_{ref} + \Psi_{g,d}Q_{ref}}{\omega\left(\Psi_{g,d}^2 + \Psi_{g,q}^2\right)}\right) \tag{4.20}$$

$$I_{g,q,ref} = 2/3\left(\frac{\Psi_{g,d}P_{ref} + \Psi_{g,q}Q_{ref}}{\omega\left(\Psi_{g,d}^2 + \Psi_{g,q}^2\right)}\right) \tag{4.21}$$

The reference active power P_{ref} is determined by using the information of the error signal produced by the voltage controller and the dc-link reference voltage $V_{dc,ref}$. The reactive power reference Q_{ref} in equations (4.20) and (4.21) is set to zero var to achieve unity power factor operation. In some applications however, the front-end ac-dc converter is required to operate in leading power factor mode to compensate for the motoring loads of lagging power factor that are connected in a near-by utility grid.

Figure 4-1 shows the control structure of the proposed VFOC. The objective of the control system is to maintain the dc-link output voltage V_{dc}, at the required level of dc-link reference voltage $V_{dc,ref}$, while maintaining almost sinusoidal currents drawn from the grid power system and in phase with their associate phase voltages to satisfy the unity power factor operation. The error signal between the command and the measured dc output voltage is processed by an outer proportional integral (PI) dc-link voltage controller. Accordingly, a dc current I_{dc} generated by the PI controller is multiplied with the dc-link reference voltage $V_{dc,ref}$ to acquire the required active power P_{ref}. The estimation of the current vector reference components $I_{g,d,ref}$ and $I_{g,q,ref}$ is performed by the Current References Estimator block which basically consists of equations (4.20) and (4.21).

The current reference components $I_{g,d,ref}$ and $I_{g,q,ref}$ are compared with their respective measured current components $I_{g,d}$ and $I_{g,q}$ to obtain the error signals which are fed to the two PI regulators that are located in the current control loop as shown in Figure 4-1. The PI regulators compensate any existing error by generating appropriate control voltages.

Equations (4.13) and (4.14) reveal that the voltage equations of the three phase ac-dc converter in each of the *dq*-coordinates are dependent on the other component in the other axis due to the cross-coupling terms $\omega L I_{g,q}$ and $\omega L I_{g,d}$. In order to implement independent controllers for the two coordinates, the influence of the *q*-axis component on the d-axis components, and the influence of the *d*-axis component on the *q*-axis components have to be removed. Therefore a decoupling network, consisting of blocks containing ωL information, is used in the proposed VFOC to minimize the coupling effects and hence improve the converter control performance. In addition, the estimated grid voltages $\omega \Psi_{g,q}$ and $\omega \Psi_{g,d}$ derived from the virtual flux concept, are utilized as the feed-forward components which can reduce the influence of any grid harmonic disturbance that will degrade the converter control system performance.

Finally, the converter pole voltage vector components $V_{conv,d}$ and $V_{conv,q}$ are generated by combining the voltages from the *dq* decoupling network and the feed-forward components as shown in Figure 4-1. The *dq* voltage components $V_{conv,d}$ and $V_{conv,q}$ are transformed back into the three phase *abc*-coordinates using the grid virtual flux vector angle θ information. The switching signals for the PWM rectifier

are generated by a sinusoidal pulse width modulator (SPWM). The SPWM works by comparing the converter pole voltages in *abc*-coordinates with a high frequency triangular carrier.

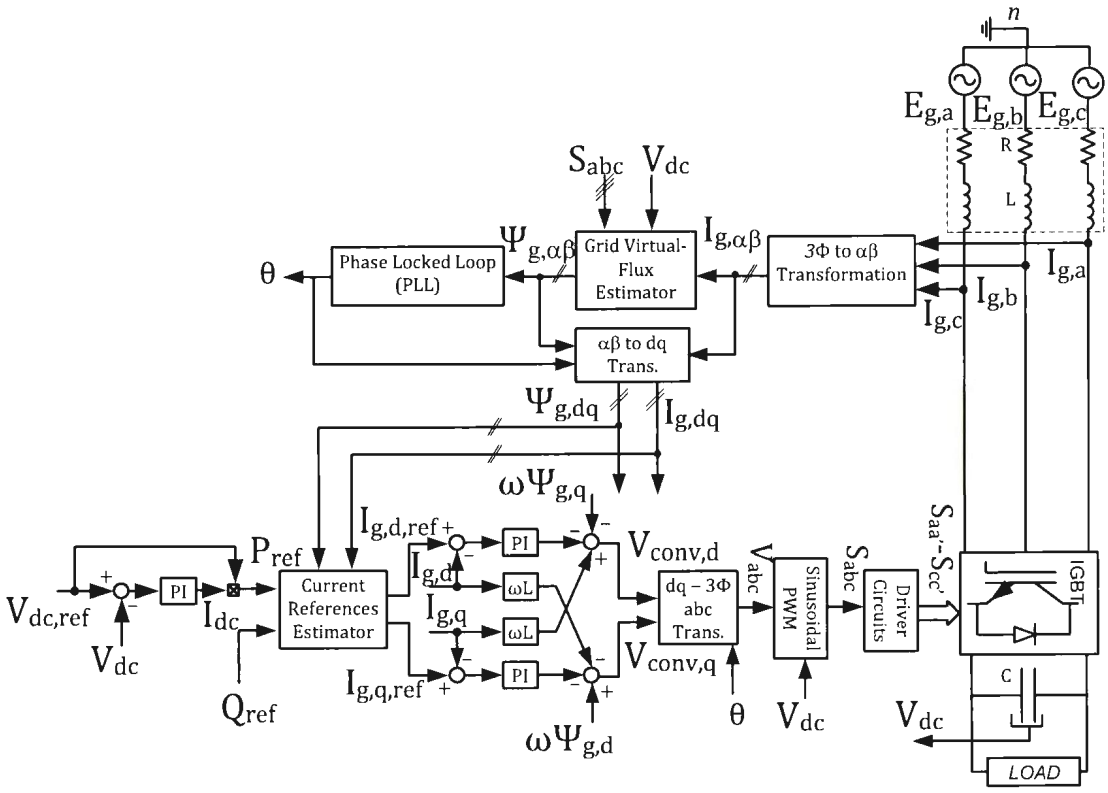


Figure 4-1: Control structure of the proposed VFOC scheme for PWM AC-DC Converter

4.4 Development of the Current Controller and Voltage Controller for the AC-DC Converter

The inner current control loop and the dc-link outer voltage control loop strongly affect the performance of the entire AC to DC converter system. References [13] and [28] present recently used voltage and current control techniques for the three-phase PWM voltage source converter (VSC). In general, there are two main groups of the voltage and current controllers; the voltage and current controllers operating in a stationary reference frame which are working with ac components, and the voltage and current controllers operating in a rotating reference frame which are working with dc components. However, the controllers working in a rotating reference frame have the advantage of being able to minimize a steady-state error.

In the proposed virtual flux oriented control (VFOC), the inner current controller and the outer voltage controller that operate in a rotating reference frame are employed. The parameters of three PI controllers, two of which are located in the current control loop and one in the voltage control loop, are tuned by using the symmetrical optimum (SO) method taking into consideration the time delay effects to the controller performance. The main contributions to the total time delay are the sampling time period T_s, statistical delay of pulse width modulation T_{PWM}, and switching dead time T_d [19, 28].

4.4.1 Development of the Current Controller

The current controller block diagram with a PI regulator is depicted in Figure 4-2. The current controller in Figure 4-2 is valid for both the direct d-axis and the quadrature q-axis of the line current vector. Therefore, the two PI controllers in d-axis and q-axis in the current control loops as shown in the proposed VFOC scheme block diagram of Figure 4-1, have identical PI parameters.

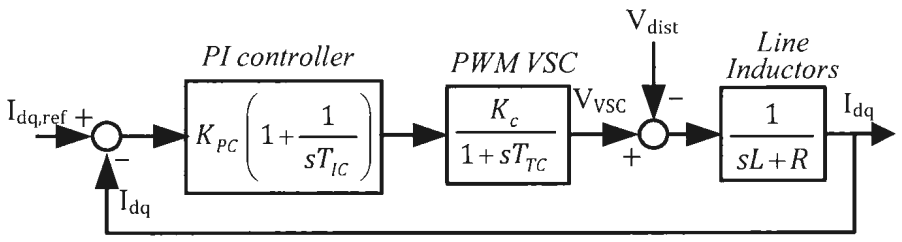


Figure 4-2: Current control loop with PI controller

The meanings of notations used in the current controller of Figure 4-2 are listed below:

K_{PC}	proportional gain of the PI regulator
T_{IC}	integrating time
K_C	converter gain
T_{TC}	total time delay in current controller
V_{VSC}	voltage of the PWM voltage source converter
V_{dist}	voltage disturbance
L	line inductance
R	inductor's internal resistance
I_{dq}	measured line current in a rotating reference frame
$I_{dq,ref}$	reference current in a rotating reference frame

The total time delay of the inner current control loop T_{TC} is defined by:

$$T_{TC} = T_s + T_{PWM} + T_d \tag{4.22}$$

where:

T_s sampling time period
T_{PWM} statistical time delay of pulse width modulation signals
T_d converter dead time

The converter gain K_C is assumed equal to one (K_C = 1). Meanwhile, the dead time T_d is negligible in the case of ideal converters. The transfer function of line inductors in Figure 4-2 can be modified for simplifying the current controller analysis. The modified transfer function of line inductors is used in the current control loop as shown in Figure 4-3:

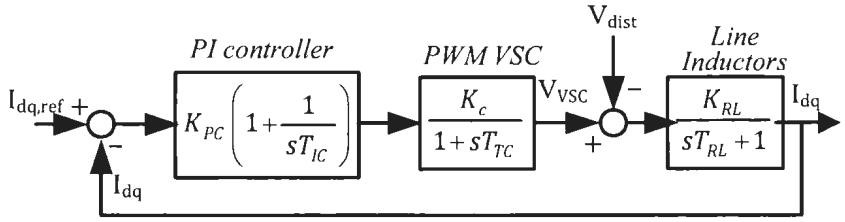


Figure 4-3: Current control loop with modified line inductors transfer function

T_{RL} is a time constant of the line inductors and can be written as:

$$T_{RL} = \frac{L}{R} \tag{4.23}$$

On the other hand, K_{RL} is a gain of the line inductors and equal to:

$$K_{RL} = \frac{1}{R} \tag{4.24}$$

By assuming the voltage disturbance V_{dist} is constant and the voltage source converter gain K_C=1, the current controller open loop transfer function $G_{OC}(s)$ can be derived as:

$$G_{OC}(s) = \frac{K_{PC}(sT_{IC} + 1)K_{RL}}{sT_{IC}(sT_{TC} + 1)(sT_{RL} + 1)} \tag{4.25}$$

Considering that the time constant of line inductors T_{RL} is the dominant time constant, the line inductors transfer function can be simplified as follows:

$$\frac{K_{RL}}{sT_{RL} + 1} \approx \frac{K_{RL}}{sT_{RL}} \tag{4.26}$$

Consequently, the current controller closed loop transfer function $G_{CC}(s)$ can be derived as:

$$\begin{aligned} G_{CC}(s) &= \frac{G_{OC}(s)}{1 + G_{OC}(s)} \\ &= \frac{K_{PC}K_{RL}(sT_{IC} + 1)}{s^3T_{IC}T_{TC}T_{RL} + s^2T_{IC}T_{RL}C + sT_{IC}K_{PC}K_{RL} + K_{PC}K_{RL}} \end{aligned} \tag{4.27}$$

According to the symmetrical optimum (SO) method, the proportional gain K_{PC} and the integral time constant T_{IC} of the current control loop can be computed as shown in equations (4.28) and (4.29), respectively.

$$K_{PC} = \frac{T_{RL}}{2T_{TC}K_CK_{RL}} = \frac{T_{RL}}{2T_{TC}K_{RL}} = \frac{T_{RL}}{2(T_s + T_{PWM} + T_d)K_{RL}} \tag{4.28}$$

$$T_{IC} = 4T_{TC} = 4(T_s + T_{PWM} + T_d) \tag{4.29}$$

Subsequently, the integral gain of the current controller K_{IC} can be computed by using:

$$K_{IC} = \frac{K_{PC}}{T_{IC}} \tag{4.30}$$

The proportional gain K_{PC} and the integral gain K_{IC} of the PI current controller must be tuned properly in order to satisfy the Nyquist stability criterias as mentioned in subchapter 3.6. In order to maintain the system stability, a cut-off frequency of the

fast open loop current controller has to be designed lower than the converter switching frequency. Meanwhile, the cut-off frequency for the slow open loop outer voltage controller is designed lower than the inner current controller cut-off frequency.

Current controller open loop analysis can be made by substituting equations (4.28) and (4.29) into the open loop transfer function $G_{OC}(s)$ given by equation (4.25). As a result, the complete open loop transfer function will have the form of:

$$G_{OC}(s) = \frac{K_{PC}(sT_{IC}+1)K_{RL}}{sT_{IC}(sT_{TC}+1)(sT_{RL}+1)} = \frac{T_{RL}K_{RL}(s4T_{TC}+1)}{2T_{TC}K_{RL}s4T_{TC}(sT_{TC}+1)(sT_{RL}+1)}$$

$$= \frac{T_{RL}(s4T_{TC}+1)}{2T_{TC}(s^2 4T_{TC}^2 + s4T_{TC})(sT_{RL}+1)} \approx \frac{T_{RL}(s4T_{TC}+1)}{(s^2 8T_{TC}^3 + s8T_{TC}^2)sT_{RL}}$$

$$= \frac{s4T_{TC}+1}{s^3 8T_{TC}^3 + s^2 8T_{TC}^2} \tag{4.31}$$

Consequently, the open loop transfer function of equation (4.31) is used to obtain the current controller closed loop transfer function $G_{CC}(s)$:

$$G_{CC}(s) = \frac{G_{OC}(s)}{1+G_{OC}(s)} = \frac{\frac{s4T_{TC}+1}{s^3 8T_{TC}^3 + s^2 8T_{TC}^2}}{1+\frac{s4T_{TC}+1}{s^3 8T_{TC}^3 + s^2 8T_{TC}^2}}$$

$$= \frac{s4T_{TC}+1}{s^3 8T_{TC}^3 + s^2 8T_{TC}^2 + s4T_{TC}+1} \tag{4.32}$$

AC to DC converter system parameters as given in Table 4-1 are used to determine the parameters of the PI controller of the current controller. The step and

frequency responses of the current controller are shown in Figure 4-4 and Figure 4-5, respectively. Figure 4-4 indicates that the calculated PI controller parameters based on the SO method generate a stable transient response of the line current during a step change on the current reference at time t=1s. At time t=1.04s, a step of voltage disturbance is applied to the current control loop. The PI regulator is able to retain the actual line current at the reference value after experiencing a small dip caused by the disturbance. A bode diagram of the open loop current controller frequency response is shown in Figure 4-5. The open loop current controller has a phase margin of 37.4° with 1170rad/s or 186Hz cut-off frequency, and infinity gain margin which indicate that the controller is working in stable conditions.

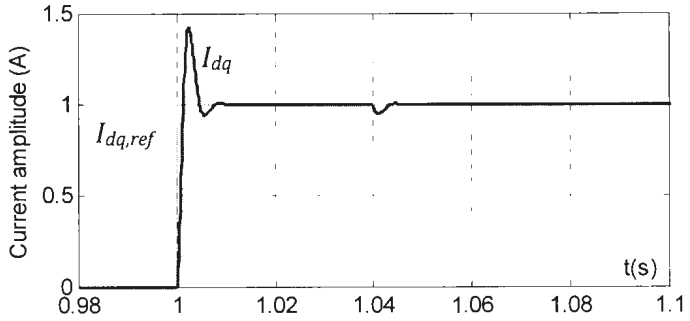


Figure 4-4: Line current step response and input voltage disturbance rejection performances

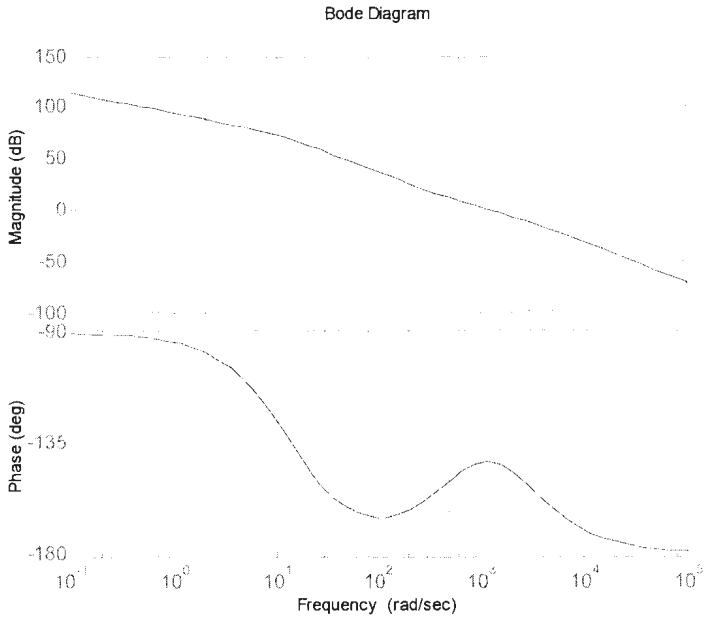


Figure 4-5: Bode diagram of the open loop current controller

As shown by the line current step response in Figure 4-4, tuning of the PI regulator based on the SO method generates about 40% current overshoot which is caused by the forcing element in the numerator of the closed loop current controller transfer function as given by equation (4.32). In order to reduce the current overshoot, a first order low-pass filter on the reference current can be used. The low-pass filter transfer function $G_{CLP}(s)$ is given by:

$$G_{CLP}(s) = \frac{1}{1 + sT_{CLP}} \tag{4.33}$$

The current reference low pass filter time constant T_{CLP} is set to $4T_{TC}$ for cancelling the numerator of equation (4.32). Therefore, the new current controller closed loop transfer function can be written as:

$$G_{CCnew}(s) = G_{CLP}(s)G_{CC}(s) = \frac{1}{s^3 T_{TC}^3 T_{TC} + s^2 T_{TC}^2 + s4T_{TC} + 1} \quad (4.34)$$

This new current controller closed loop transfer function can be approximated by first order transfer function as:

$$G_{CCnew}(s) = \frac{1}{s^3 8T_{TC}^3 + s^2 T_{TC}^2 + s4T_{TC} + 1} \approx \frac{1}{1 + s4T_{TC}} \quad (4.35)$$

The current control loop is modified to include the current reference low-pass prefilter as shown in Figure 4-6.

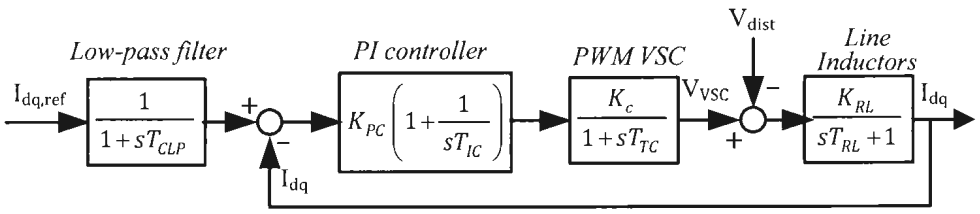


Figure 4-6: Current controller with a low-pass pre-filter connected to the line current reference signals

Comparison of the current controller performance with and without the reference current low-pass pre-filter is shown in Figure 4-7. The reduction of current overshoot during a step change in the reference current is clearly observed for the current controller with the pre-filter. However, the transient response for a step change in voltage disturbance is unchanged.

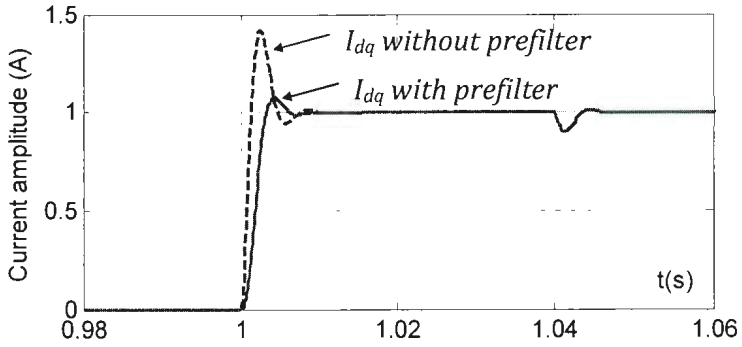


Figure 4-7: Performances on the line current step response and voltage disturbance rejection capability with and without a low-pass prefilter

4.4.2 Development of the Dc-link Voltage Controller

The dc-link voltage control loop with a PI compensator is used to regulate the dc output voltage of the ac-dc converter. The dc-link controller is developed by assuming that the inner current control loop can be modeled with the first order transfer function. Therefore, the closed loop of current controller $G_{CC}(s)$ is approximated by the first order transfer function with equivalent time delay of T_{TC} as shown in equation (4.36):

$$G_{CC}(s) = \frac{1}{1 + s4T_{TC}} \tag{4.36}$$

The total time delay in the closed loop current controller T_{TC} is defined by:

$$T_{TC} = T_s + T_{PWM} + T_d \tag{4.37}$$

where

T_s sampling time period
T_{PWM} statistical time delay of pulse width modulation
T_d converter dead time

Figure 4-8 shows the model of the dc-link voltage control loop with a PI regulator.

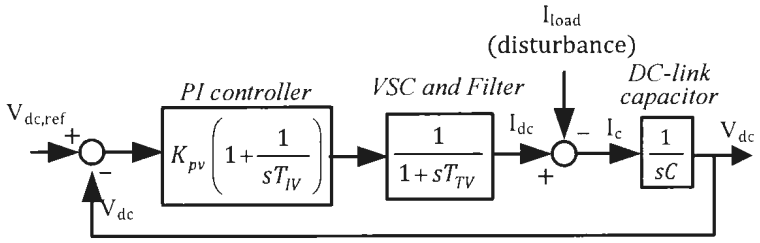


Figure 4-8: Voltage control loop with a PI controller

The voltage controller total time delay T_{TV} is defined as:

$$T_{TV} = 4T_{TC} + T_f \tag{4.38}$$

where:

T_{TC} total time delay in current controller
T_f dc-link voltage low-pass filter time constant

A digital low pass filter with the filter time constant T_f is utilized in real time implementation for reducing the ripple and noise of the measured dc-link output voltage. The time constant of $T_f = 0.003$s has been found satisfactory to achieve smooth and constant dc-link output voltage. The load current disturbance input signal I_{load} is added into the voltage control loop to evaluate the effectiveness of the PI regulator during the changes of load current demand.

The open loop transfer function of the voltage controller $G_{OV}(s)$ of Figure 4-8 can be derived by assuming that the load current disturbance is constant. Consequently, the load current disturbance input signal can be removed from the

voltage control loop during the derivation of voltage controller transfer function. The voltage open loop transfer function can be written as:

$$G_{OV}(s) = \frac{K_{PV}(sT_{IV} + 1)}{sT_{IV}(sT_{TV} + 1)sC} \tag{4.39}$$

Accordingly, the open loop transfer function is used to compute the voltage controller closed loop transfer function $G_{CV}(s)$:

$$G_{CV}(s) = \frac{G_{OV}(s)}{1 + G_{OV}(s)} = \frac{K_{PV}(sT_{IV} + 1)}{s^3T_{IV}T_{TV}C + s^2T_{IV}C + sT_{IV}K_{PV} + K_{PV}} \tag{4.40}$$

Based on the SO method, the converter system parameters given in **Error! Reference source not found.** and the proper estimation of the voltage controller total time delay T_{TV}, the dc-link voltage controller's proportional gain K_{PV} and integral time constant T_{IV} are computed by using equations (4.41) and (4.42), respectively.

$$K_{PV} = \frac{C}{2T_{TV}} = \frac{C}{2(4T_{TC} + T_f)} \tag{4.41}$$

$$T_{IV} = 4T_{TV} = 4(4T_{TC} + T_f) \tag{4.42}$$

The step and frequency responses on the voltage control loop are shown in Figure 4-9 and Figure 4-10, respectively. Figure 4-9 shows that with a proper tuning of a PI controller, the voltage controller is able to produce a stable transient response of the dc output voltage V_{dc} during a step change on the dc voltage reference $V_{dc,ref}$ at time t=1s. At time t=1.4s, a 10% disturbance in the load current I_{load} is injected into the voltage control loop. However, the dc-link output voltage is maintained at a reference value although suffering a small dip caused by a disturbance.

A bode diagram of the open loop voltage controller frequency response is shown in Figure 4-10. An analysis of the bode diagram reveals that the open loop voltage controller has a phase margin of 39.1° with 37.4rad/s or 6Hz cut-off frequency. The cut-off frequency value gives a confirmation that the bandwidth of the voltage control loop is lower than the bandwidth of the current control loop which is one of the important characteristics of the stable control system.

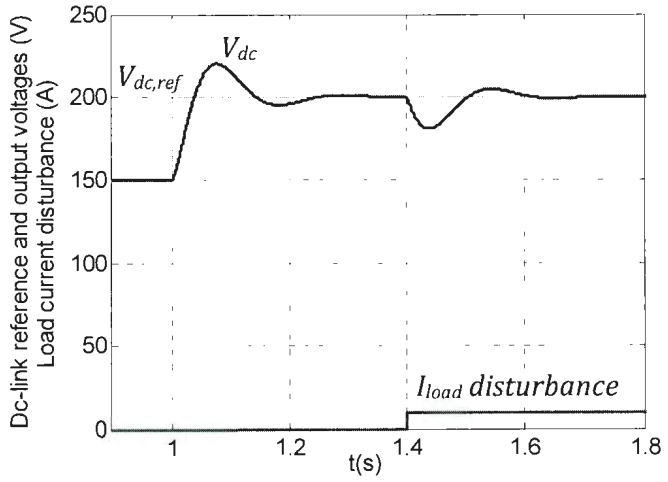


Figure 4-9: Dc-link voltage step response and load current disturbance rejection performances

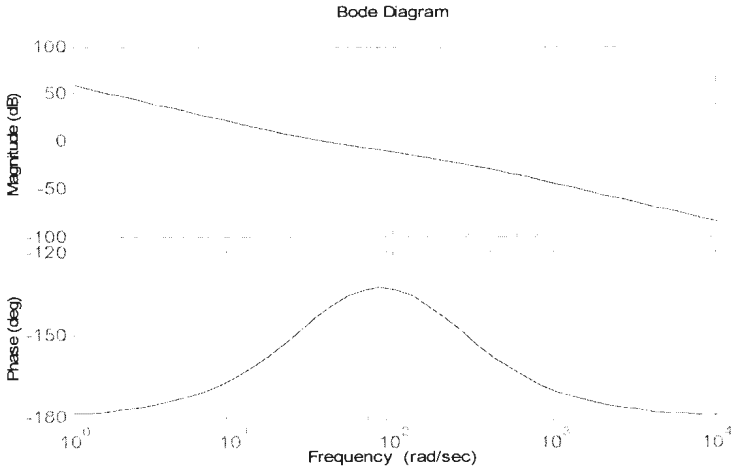


Figure 4-10: Bode diagram of the open loop voltage controller

4.4.3 Effects of the Decoupling and Feed-forward Components to the Current Controller Performance

The two dq voltage equations of the grid connected voltage source converter as shown in (4.13) and (4.14) are dependent on each other due the cross-coupling terms given by $\omega L I_{g,q}$ and $\omega L I_{g,d}$. The cross-coupling terms will reduce the controller performance by increasing the line current total harmonic distortion during step changes in the reference current magnitude. A decoupling network as shown in Figure 4-11 is introduced in the proposed VFOC in order to reduce the negative impacts of the coupling components and hence, improve the converter control performance. In addition, the feed-forward components given by $\omega \Psi_{g,q}$ and $\omega \Psi_{g,d}$ are added in the decoupling network to minimize the influence of grid harmonic disturbance to the current controller performance. Performances of the current controllers with and without the decoupling network and feed-forward components are compared through Matlab/Simulink simulation analysis.

Figure 4-12 shows the current responses due to step changes of the reference active current. The PI controllers in the current control loops are tuned based on the SO method which has been explained in previous sections. The reference d-axis current $I_{d,ref}$ is kept at 0A to imitate the condition of unity power factor mode. A step change of the q-axis current $I_{q,ref}$, which has direct influence on the active power, takes place at time t=1s. At this time period, $I_{q,ref}$ changes from 0A to 1A. Later, at time t=1.04s, $I_{q,ref}$ changes from 1A to -1A. The current controller with the

decoupling and feed-forward components produces smaller magnitude of oscillations in the *d*-

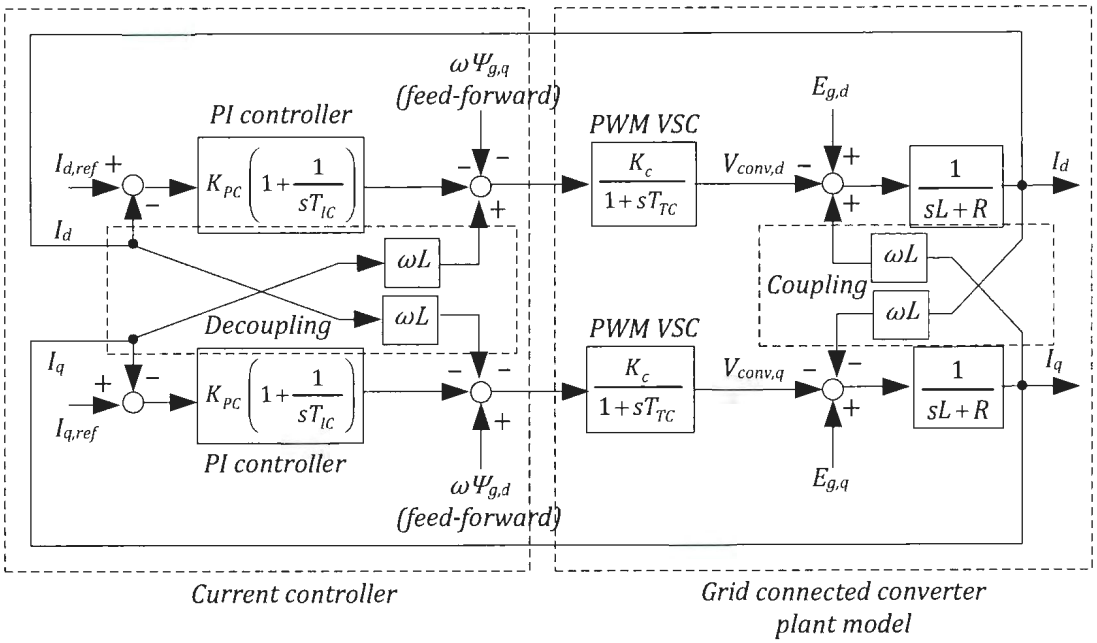


Figure 4-11: Current control structure of the grid connected voltage source converter

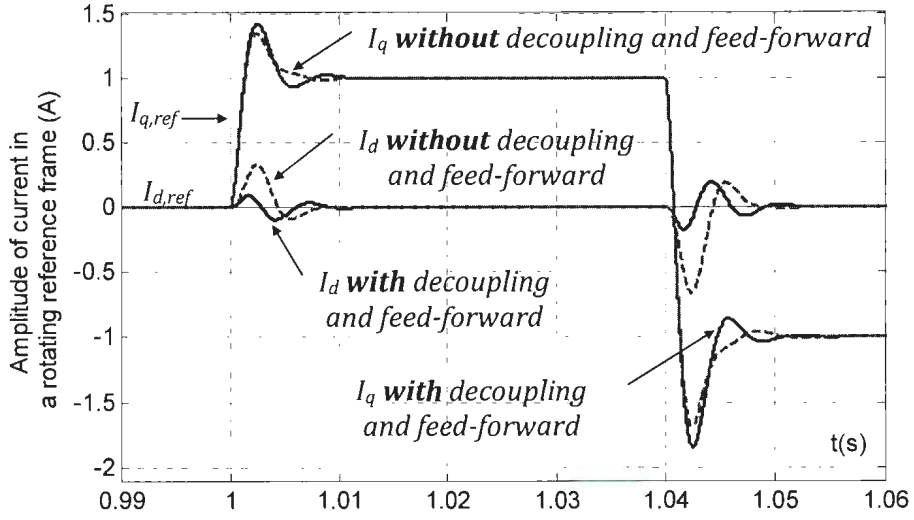


Figure 4-12: Current responses due to step changes in *q*-axis reference current

axis current I_d during step changes in the reference active current $I_{q,ref}$. Current I_d has a direct influence on the reactive power. However, the responses of the active current I_q to step changes in its reference, have almost similar responses for both controllers, with and without the decoupling and feed-forward components.

Performance of the proposed decoupling network of current controller with and without feed-back components being injected into the current controller is also evaluated by using Matlab/Simulink. Figure 4-13 shows the effects of the grid voltage disturbances to the *dq* line currents flowing from the three phase grid to the load via the voltage source converter. During initial condition of the simulation process, the *d*-axis current I_d, *q*-axis current I_q and *q*-axis grid voltage $E_{g,q}$ are set to 0A, 1A and 100V, respectively to imitate the condition of steady state and unity power factor operation mode. At time t=1s, a step change of 10% in the grid voltage $E_{g,q}$ is injected into the system and maintained until time t=1.04s. Subsequently, a step change decrease of 20% in the grid voltage $E_{g,q}$ takes place at time t=1.04s. The current controller incorporating the decoupling network and the feed-forward components generates smaller magnitudes of transients and oscillations in the *dq* line currents during the disturbances in the grid voltage supply. In contrast, the decoupling network without the feed-forward components produces significantly higher magnitude of transient and oscillation currents when the voltage supply is interrupted.

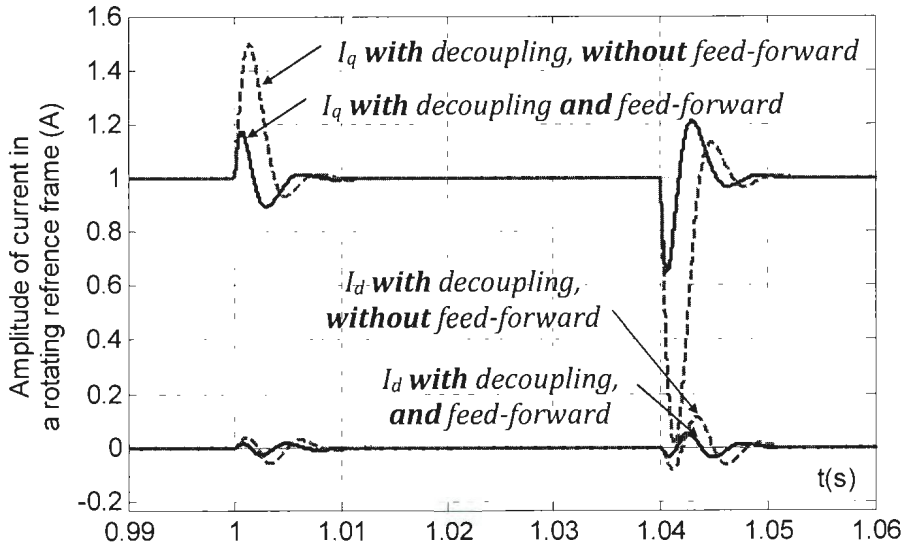


Figure 4-13: Current responses due to the disturbances in grid voltage supply

4.5 Simulation Results and Performance Analysis of the Proposed Virtual Flux Oriented Control under Balanced Three Phase Voltage Supply

The entire ac-dc converter system utilizing the proposed virtual flux oriented control (VFOC) is developed and simulated in the Matlab-Simulink discrete environment to study its steady state and dynamic performances. The main parameters used in the simulation are given in Table 4-1.

Table 4-1: Main Parameters Used in the Simulation

Input phase voltage (peak) E_g	70.71V
Source voltage frequency f	60Hz
Dc-link voltage reference $V_{dc,ref}$	150V
Resistance of reactors R	0.2Ω
Inductance of reactors L	15mH
DC-link capacitor C	10.8mF
Load resistance R_{Load}	140Ω
Sampling time T_s	20μs
Sampling frequency $f_s = 1/T_s$	50Khz
Switching frequency f_{sw}	2460Hz

The grid virtual flux components in the stationary $\alpha\beta$-reference frame and the rotating dq-reference frame are shown in Figure 4-14 and Figure 4-15, respectively. The virtual flux components in the dq-coordinates are used by the phase locked loop (PLL) to determine the grid virtual flux vector angle as shown in Figure 4-16. The correct estimation of the virtual flux components is required in order to make sure the controller is synchronized properly with the three phase supply voltage during both balanced and unbalanced voltage conditions. Furthermore, the accurate

information of the virtual flux vector components and angle, is required to ensure appropriate calculation of the reference currents in the *dq*-coordinates given by $I_{d,ref}$ and $I_{q,ref}$.

Figure 4-17 (a) and (b) represent the balanced three-phase grid side voltage and line current waveforms, respectively. The proposed VFOC method is able to produce balanced three phase sinusoidal line currents with unity power factor. A better insight of the line current performance during the steady state and unity power factor operation is given by Figure 4-18. The figure shows that the phase voltage is in phase with its associate phase current during unity pf mode. Moreover, the line current harmonic spectrum analysis as shown in Figure 4-19 reveals that the proposed VFOC produced 2.32% total harmonic distortion (THD) which fulfills the standard requirement and regulation, and the THD is lower than the current THD generated by the direct power control (DPC) method. The VFDPC with new switching table generates 4.66% current THD which is slightly higher than the 2.32% current THD generated by the proposed VFOC scheme. Note that the sinusoidal pulse width modulator produces side band harmonic components around the switching frequency and multiples of the switching frequency as shown in the line current harmonic spectrum in Figure 4-19. The proposed VFOC works by utilizing the synchronous rotating reference frame components. The line currents in the *dq*-frame I_d and I_q are shown in Figure 4-20. The measured d-axis current component is kept at 0A by the controller to achieve unity pf operation. The proportional and integral (PI) regulators used in the voltage and current control

loops are able to produce and regulate the dc output voltage V_{dc} according to the reference voltage $V_{dc,ref}$ of 150V as shown in Figure 4-21.

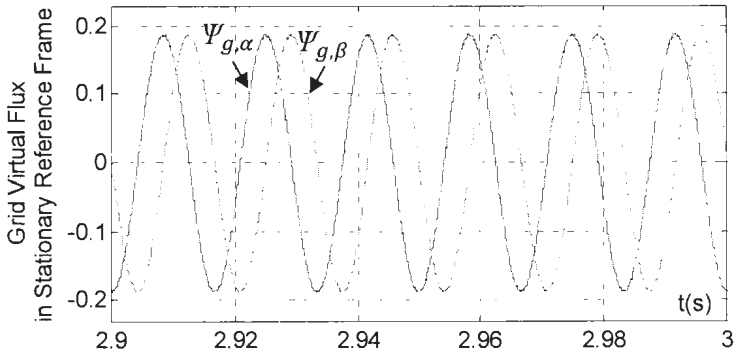


Figure 4-14: Virtual grid flux in stationary $\alpha\beta$-coordinates

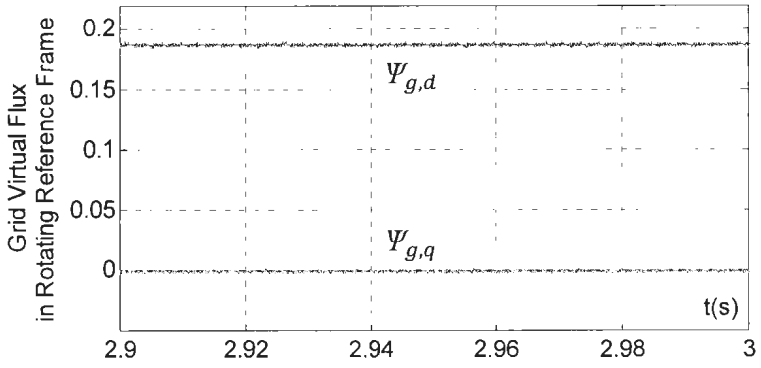


Figure 4-15: Virtual grid flux in rotating dq-coordinates

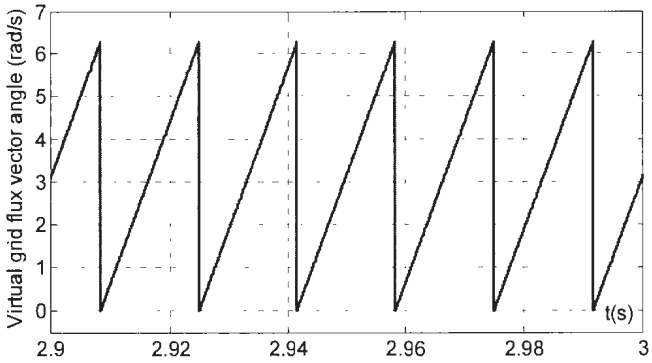


Figure 4-16: Grid virtual flux vector angle produced by phase locked loop

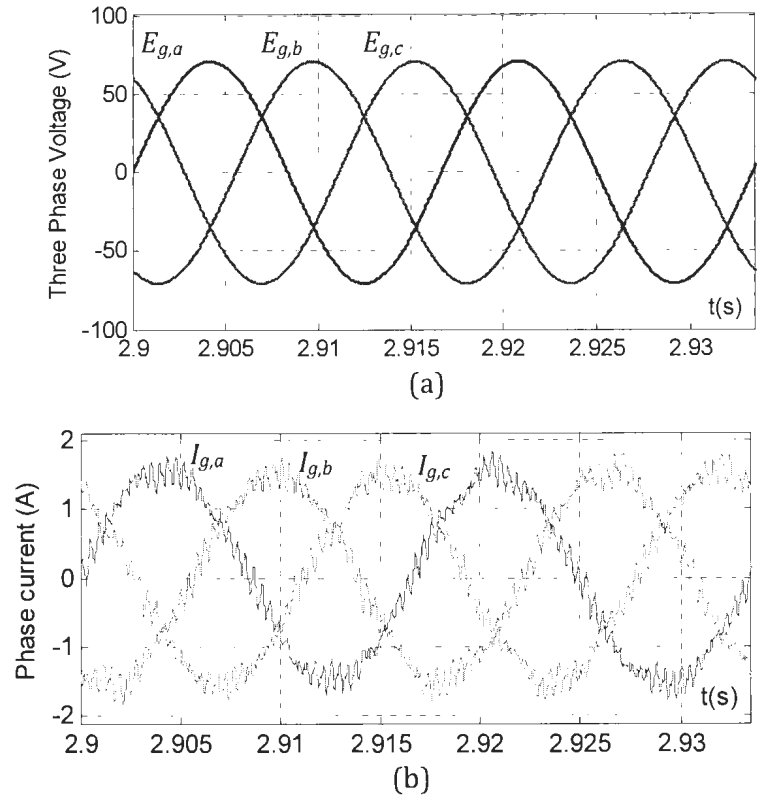


Figure 4-17: (a) Three phase input voltages (b) Three phase input currents

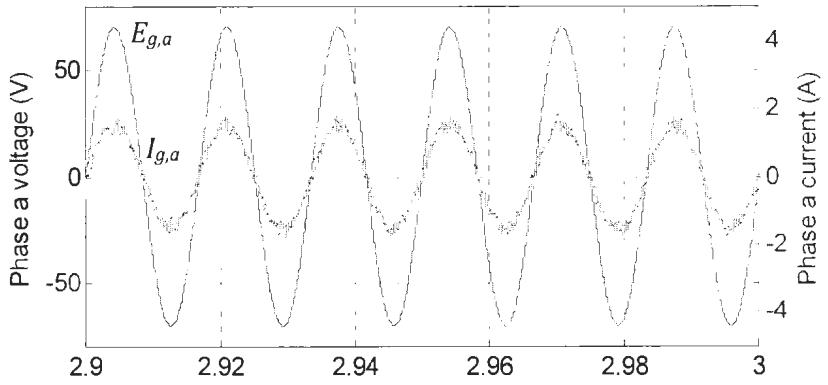


Figure 4-18: Phase *a* voltage and current at unity power factor

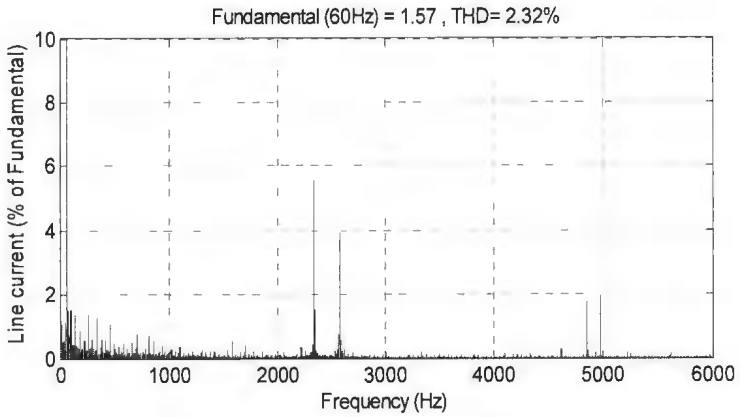


Figure 4-19: Frequency spectrum of the grid current

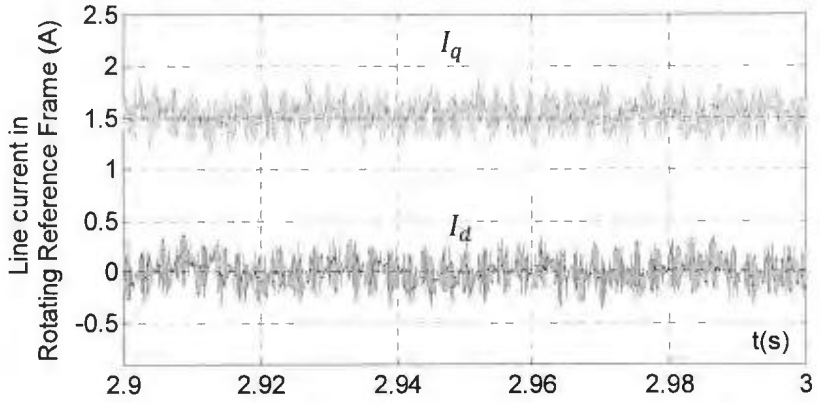


Figure 4-20: Supply currents in synchronously rotating *dq*-reference frame

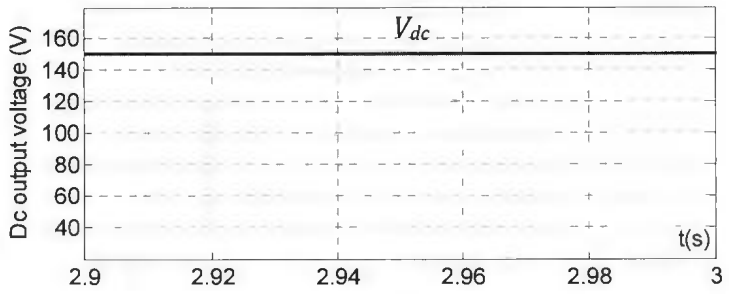
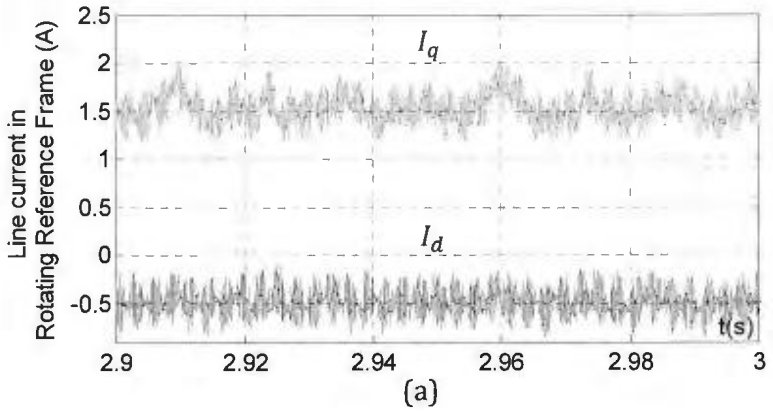


Figure 4-21: Generated dc-link output voltage

The proposed VFOC method is able to adjust the power factor of the converter system by providing a suitable value to the required reactive power Q_{ref} and therefore correct values of the reference currents as mentioned in equations (4.20) and (4.21) can be determined. In this simulation study, the reference reactive power Q_{ref} is set to -50var and +50var in order to demonstrate leading and lagging power factor operation modes as shown in Figure 4-22 and Figure 4-23, respectively. The actual line currents I_{dq} successfully track the reference currents $I_{dq,ref}$ in both power factor modes. The measured line current I_d is shifted down to a negative value which will cause the phase a current to lead the phase a supply voltage for leading power factor mode as shown in the top and bottom of Figure 4-22. On the other hand, a shift in the line current I_d from 0A to a positive value causes the phase a current to lag the phase a voltage during lagging power factor operation mode as shown in the top and bottom of Figure 4-23.



(a)

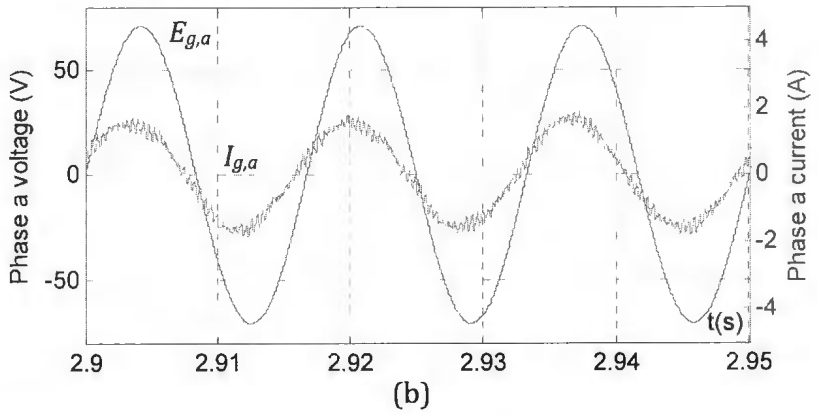


Figure 4-22: Generated waveforms during leading power factor operation mode. (a) Line currents in *dq*-frame (b) Phase *a* voltage and current

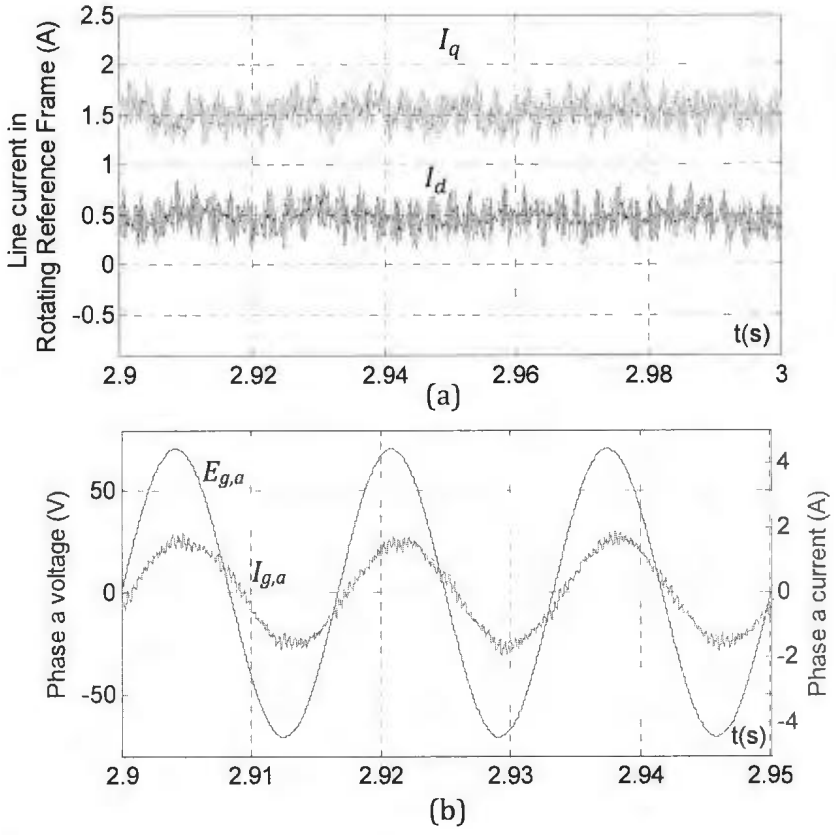
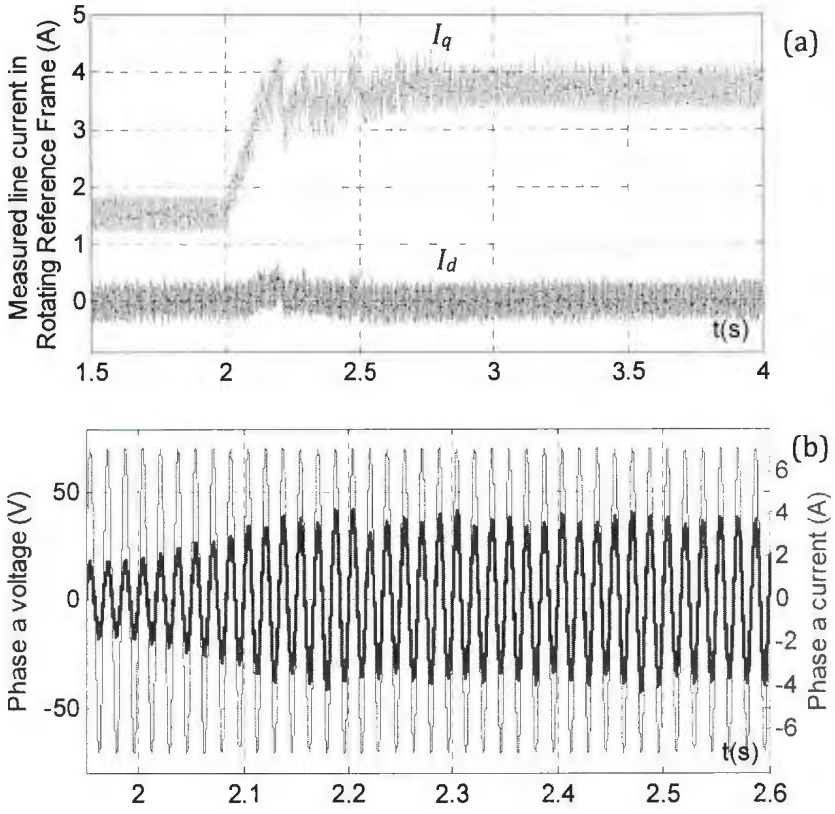


Figure 4-23: Generated waveforms during lagging power factor operation mode. (a) Line current in *dq*-coordinates (b) Phase *a* voltage and current

Figure 4-24 shows the rectifier dynamic behavior under load variation during unity power factor operation. The load variation is performed by connecting abruptly a 100Ω resistor in parallel with the existing resistor at the dc-link to cause a sudden disturbance in the load current. The resistor load is connected at a simulation time of 2 seconds. Forced by the voltage and current PI regulators, the line currents quickly increase to meet the demand for the additional load current without undesirable overshoot and oscillation. Moreover the dc-link voltage recovers to the original value of 150V after experiencing a small dip during the power transitioning process.



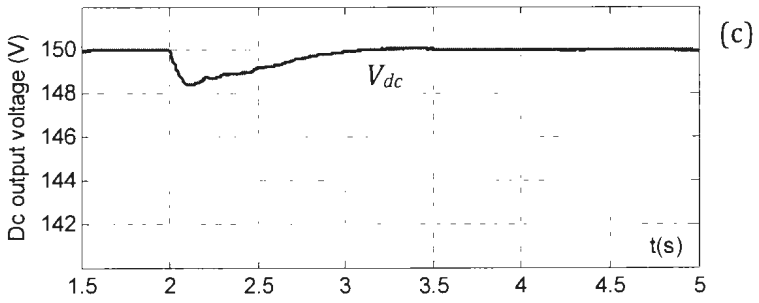
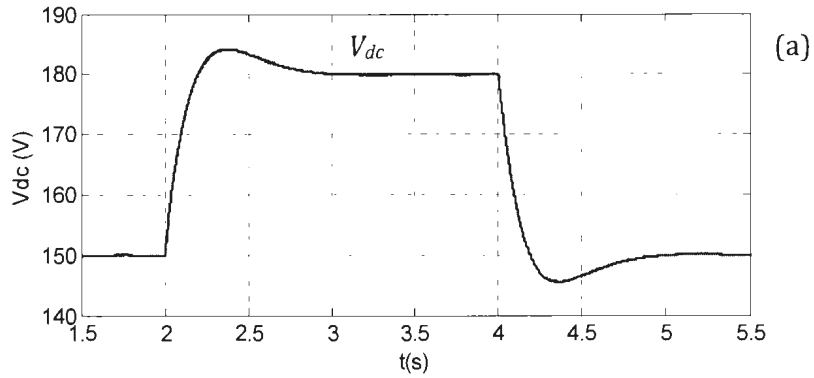


Figure 4-24: Transient responses for load variation from low to high power demand: (a) Line current in *dq*-coordinates (b) Phase *a* voltage and current (c) Dc-link output voltage

Transient responses of the ac-dc converter dc output voltage V_{dc} and line current I_{dq} under step changes in the output voltage reference $V_{dc,ref}$ are shown in Figure 4-25. The voltage command $V_{dc,ref}$ changes from 150V to 180V at 2s and back to 150V at 4s. With the estimated quantities for the feedback control, the control performance is satisfactory. The line current of the *q*-axis increased and decreased quickly to a new value during the step changes of output voltage while keeping the *d*-axis line current component at zero value to accommodate the increasing and decreasing of the converter output dc voltage.



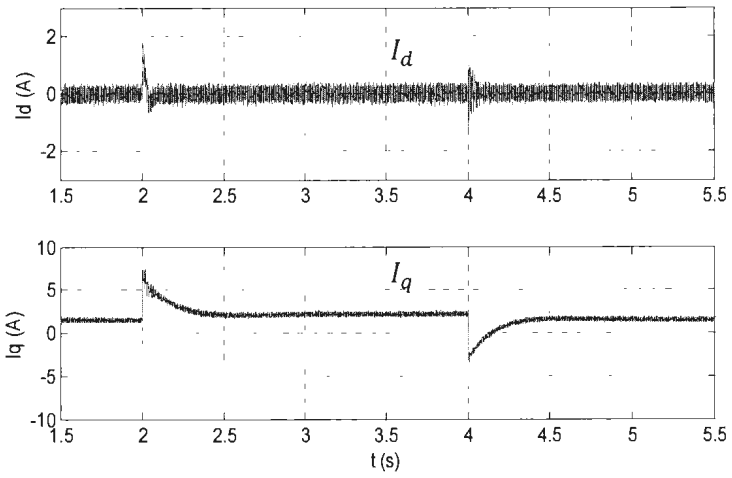


Figure 4-25: Transient response for dc output voltage changes: (a) Dc-link output voltage (b) Line current in *dq*-coordinates

4.6 Simulation Results and Performance Analysis of the Proposed Virtual Flux Oriented Control under Distorted Three Phase Voltage Supply

Simulation analysis is also conducted to evaluate the proposed Virtual Flux Oriented Control (VFOC) under distorted input supply voltage. The three phase voltage distortion is obtained by injecting 5% of the magnitude of the fundamental component into the fifth harmonic component of the positive sequence of the three phase voltage supply. A mathematical representation of the distorted three phase voltages with fifth harmonic injection is given by

$$E_{g,an} = |E|cos(\omega t) + |k * E|cos(5\omega t)$$

$$E_{g,bn} = |E|cos\left(\omega t - \frac{2\pi}{3}\right) + |k * E|cos\left(5\omega t + \frac{2\pi}{3}\right)$$

$$E_{g,cn} = |E|cos\left(\omega t + \frac{2\pi}{3}\right) + |k * E|cos\left(5\omega t - \frac{2\pi}{3}\right) \qquad (4.43)$$

where $|E|$ denotes the voltage magnitude of the phase voltage fundamental component, and k is equal to 0.05 for 5% of the fundamental component. Figure 4-26 shows the distorted three phase voltage waveforms. The low-pass filter action performed by the virtual flux estimation procedure has a significant impact to the quality of the three phase input currents as shown in Figure 4 27 and Figure 4-28. The proposed control method is still able to produce sinusoidal three phase currents and maintain the unity power factor operation. The input current THD is 4.02% which is slightly higher than the current THD for the balanced supply case. The proposed VFOC generates current THD of 2.32% during the balanced three phase input voltage condition. Waveforms of the input currents in a *dq*-reference frame, and the dc output voltage are shown in Figure 4-29 and Figure 4-30, respectively.

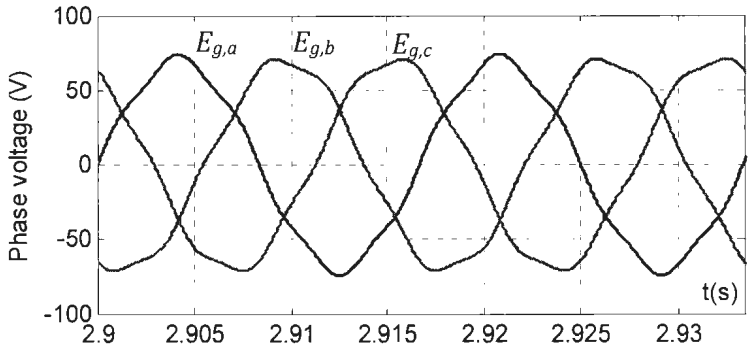


Figure 4-26: Distorted three phase voltage supply

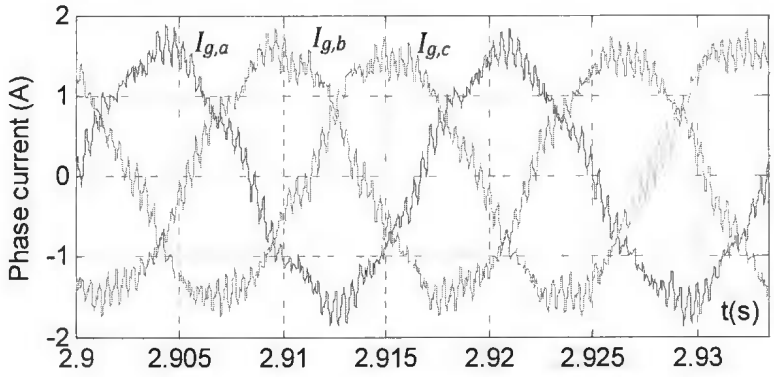


Figure 4-27: Three phase input currents

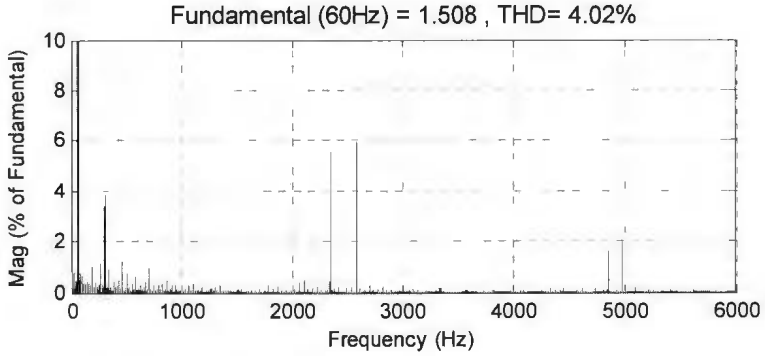


Figure 4-28: Harmonic spectrum of the line current

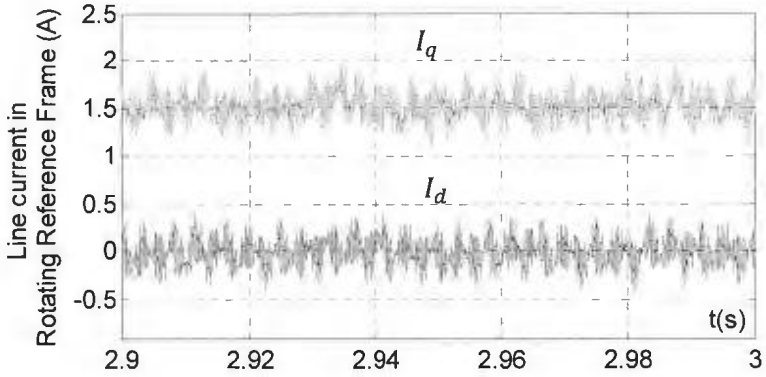


Figure 4-29: Line current in *dq*-coordinates

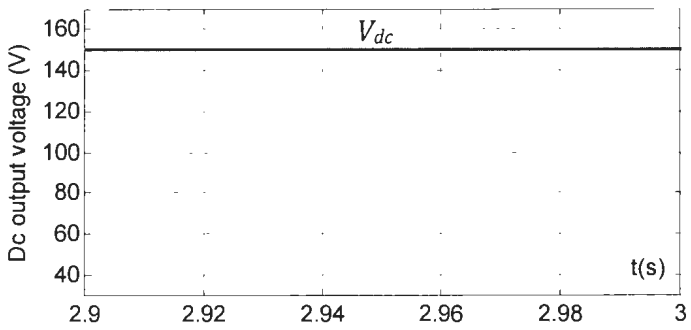


Figure 4-30: Generated dc-link output voltage

4.7 Simulation Results and Performance Analysis of the Proposed Virtual Flux Oriented Control under Unbalanced Three Phase Voltage Supply

Performance of the proposed Virtual Flux Oriented Control (VFOC) is also analyzed during unbalanced three phase voltage supply condition. The unbalanced voltage supply condition is obtained by decreasing the magnitude of phase *a* voltage to 85% of the voltage magnitude during the balanced condition. Figure 4-31 shows the unbalanced three phase voltage waveforms with reduced magnitude on the phase *a* voltage. The proposed VFOC is capable to maintain almost sinusoidal three phase currents with low total harmonic distortion and unity power factor as shown in Figure 4-32 and Figure 4-33. The magnitude of the phase *a* current is slightly reduced to accommodate the decrease of the magnitude of phase *a* voltage. The line current total harmonic distortion (THD) is 5.31% which is slightly higher than the input line current THD of 2.32% generated by the proposed VFOC during a balanced three phase voltage condition.

Due to the second harmonic component generated from the unbalanced three phase voltage supply, the measured currents in a rotating reference frame I_d and I_q, are slightly oscillating as shown in Figure 4-34. The measured d-axis current component is maintained at 0A for the unity power factor operation. Consequently, the second harmonic component generated by the unbalanced voltage supply will appear as the voltage ripples in the converter dc-link output voltage as shown in Figure 4-35. The voltage ripples have a frequency twice the fundamental frequency. The ripples can be further reduced by increasing the dc-link capacitance.

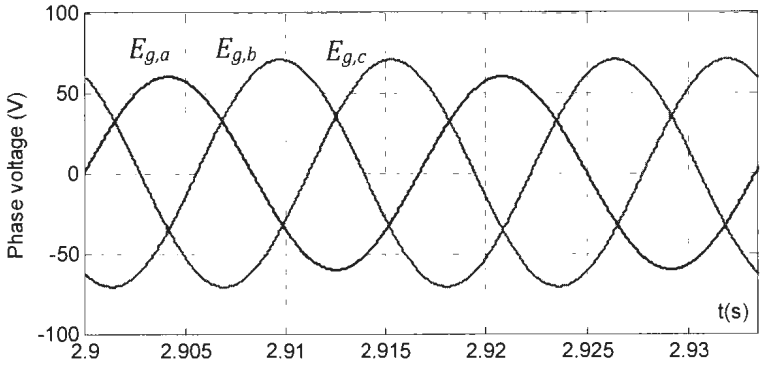


Figure 4-31: Unbalanced three phase input voltages

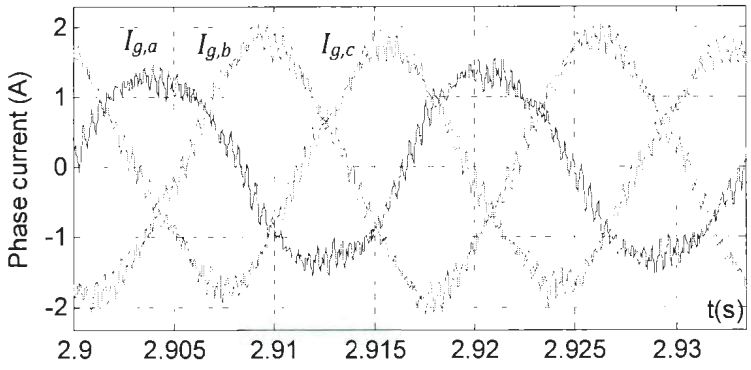


Figure 4-32: Three phase input currents

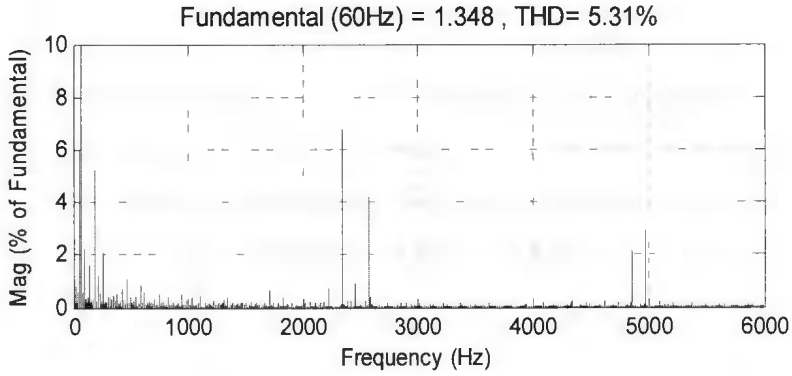


Figure 4-33: Harmonic spectrum of the line current

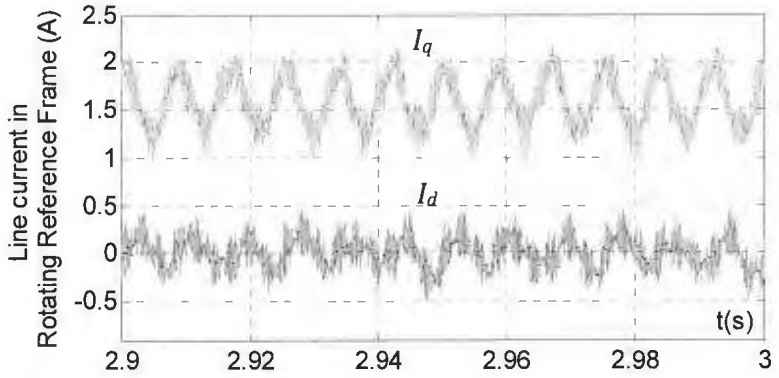


Figure 4-34: Line current in *dq*-coordinates

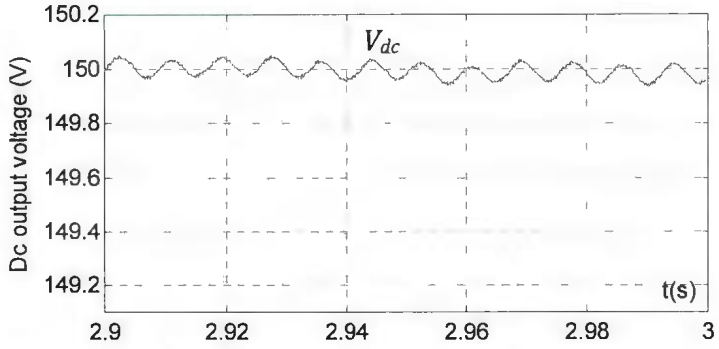


Figure 4-35: Generated dc-link output voltage

4.8 Implementation and Experimental Results of the Proposed Virtual Flux Oriented Control

The experimental implementation of the proposed Virtual Flux Oriented Control (VFOC) is performed by using the ac-dc converter system set-up, developed in the MUN Power Devices and System Research Laboratory. The development of the proposed control strategy is carried out using Matlab/Simulink and the real-time implementation with a dSPACE DS1104 digital signal processing board. The block diagrams in Figure 4-36 shows the configuration of main physical layout of the experimental set-up. The detailed explanation of the experimental set-up is given in Chapter 5. The main components of the experimental set-up consist of a three phase grid supply, three phase transformer, line inductors, ac-dc converter power circuit, gate drivers and isolation, dc-link capacitor, variable resistive load, voltage and current sensors, and DSP controller board.

The system main parameters are similar to the parameters used in the simulation, except that a few modifications are made in term of the sampling frequency and the switching frequency values, in order to accommodate the speed limitation of the digital signal processor board. The control algorithms are divided into two different sampling frequency loops according to the required sample time for each loop. The virtual flux estimation and the phase locked loop calculation are performed in a fast control loop with a sampling frequency of 16kHz, which corresponds to the sampling time of 62.5μs. On the other hand, the calculation of the *dq* current reference components, the outer dc-link voltage control loop and the

inner current control loop, are carried out by a slower rate of sampling frequency. The voltage control signals produced by the current control loop have to be synchronized with the switching frequency of the sinusoidal pulse width modulator to minimize the harmonic of the three phase input currents. Therefore, the sampling frequency of the slow control loops and the IGBTs' switching frequency have been chosen to 6kHZ which is equal to the sampling time of 166.67μs.

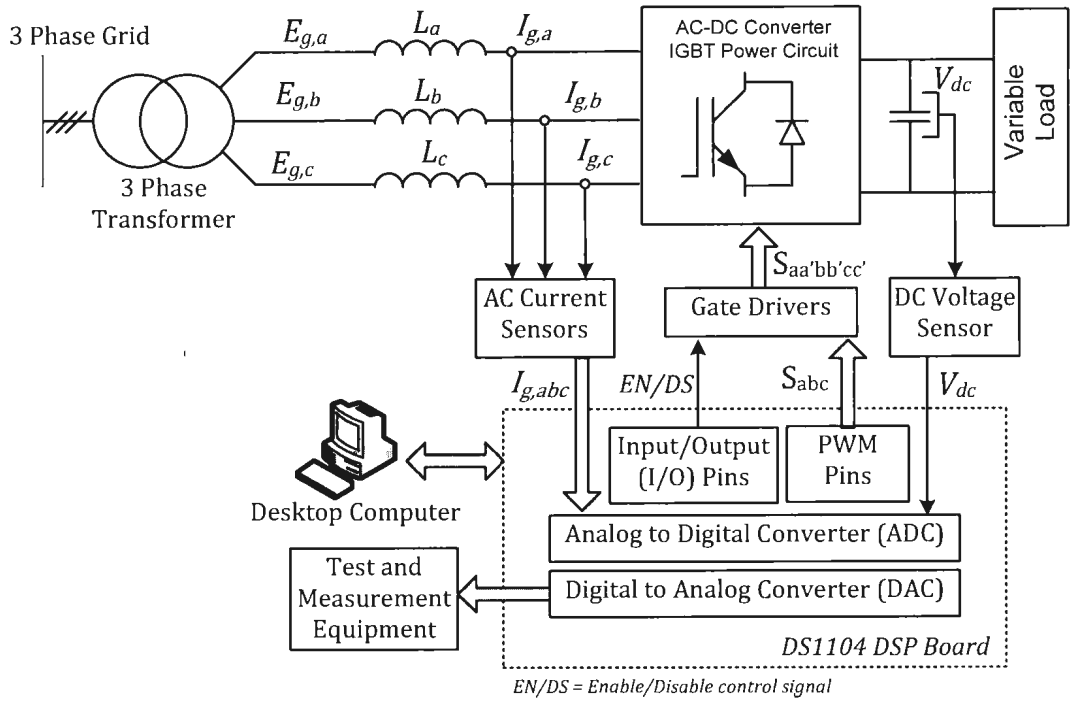


Figure 4-36: Configuration of the experimental set-up for Virtual Flux Oriented Control (VFOC)

A systematic and effective way for starting up the grid connected ac-dc converter is very important to prevent unnecessary large inrush current flowing

into the converter system. A detailed explanation for the start up implementation has been discussed in subchapter 3.10. Several waveforms that are monitored and obtained during the start up process are given in Figure 4-37. During the diode rectifier operation mode, the gate driver modules are disabled by the control signal from the DSP board. The dc-link capacitor is precharged to a certain dc voltage value V_{dc} given by equation (2.1) through the operation of anti-parallel diode across the IGBT switches. In the next stage, the DSP is activated to calculate the initial grid virtual flux vector components and angle for the synchronization purpose. The related waveforms during this process are shown clearly during the diode bridge rectifier mode in Figure 4-37.

The gating signals from the gate driver modules are fed to the IGBT switches once the modules are activated by a control signal received from the DSP board. The DSP board will generate appropriate switching signals base on the proposed control scheme algorithms. The magnitude of the actual dc-link output voltage is equal to the reference dc voltage, and higher than the precharged voltage. Figure 4-37 shows that the dc output voltage is slightly increased during the PWM rectifier mode until the system establishes the steady state operation. The consistency calculation of the grid virtual flux angle θ during both the diode bridge rectifier mode and the PWM rectifier mode, will ensure the converter system is starting up properly without unnecessary large starting input currents. Instead, sinusoidal phase currents with low total harmonic distortion are obtained during

the steady state operation as indicated by the phase *a* current waveform in the same figure.

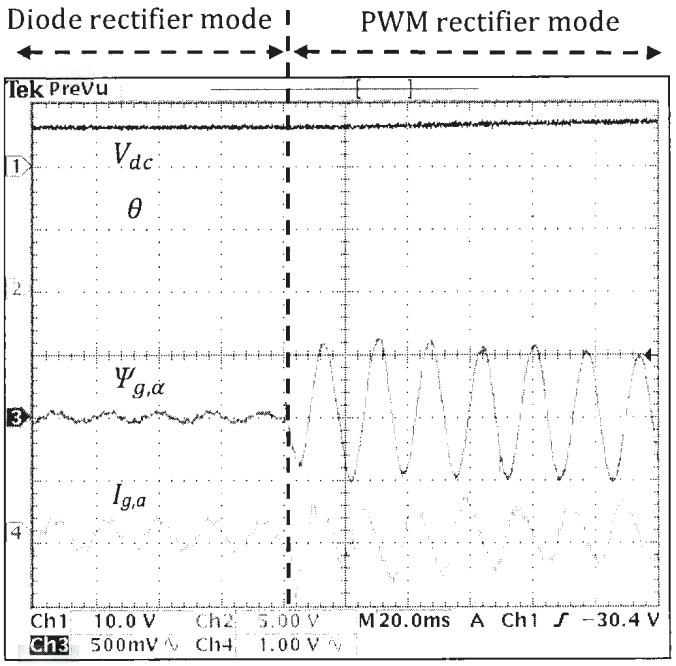


Figure 4-37: Waveforms of some main components during start up process. From top: Dc output voltage (250V/div), grid virtual flux angle (rad/s), real component of grid virtual flux (0.25wb/div), and phase *a* current (5A/div)

The effectiveness of the virtual flux estimation and compensation method can be observed in Figure 4-38. The imaginary component of the grid virtual flux in the stationary reference frame $\Psi_{g,\beta}$ is lagging the virtual flux real component $\Psi_{g,\alpha}$ by 90°. A digitally phase locked loop implementation is used to calculate the grid virtual flux vector angle θ. The angle information is used by the frame transformation matrixes as given in equations (4.6) and (4.7).

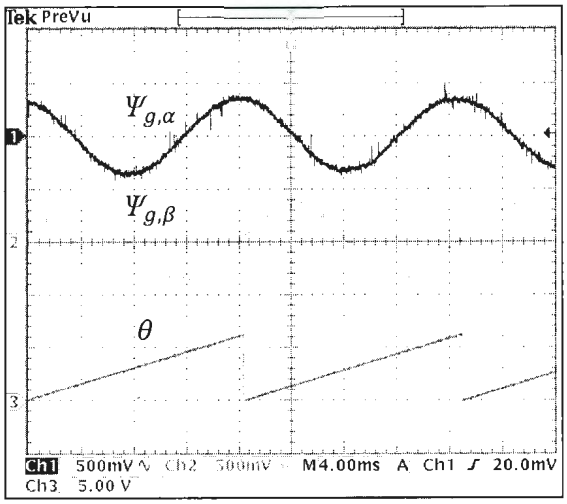


Figure 4-38: Waveforms acquired during the PWM rectifier mode. From top: Grid virtual flux in stationary reference frame, grid virtual flux vector angle

Figure 4-39 and Figure 4-40 show the input three phase currents produced by the VFOC method. The currents are almost sinusoidal and in phase with their associate phase voltages during the unity power factor operation mode. The current harmonic spectrum analysis as shown in Figure 4-41 indicates that the current fundamental component has the highest peak with a frequency of 60Hz. The low amplitude of the other harmonic components gives confirmation of the low total harmonic distortion in the line currents.

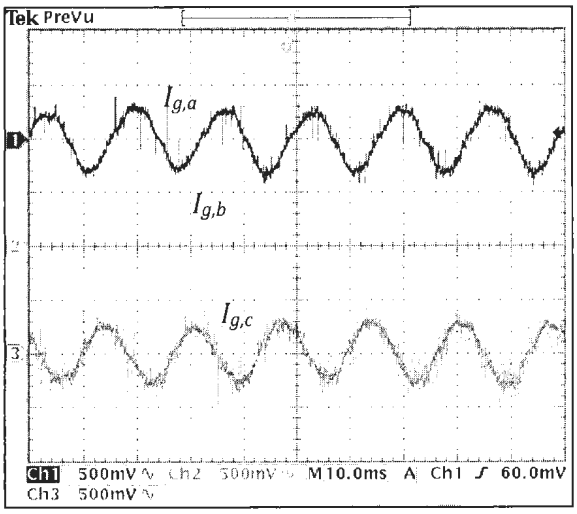


Figure 4-39: Three phase input currents (2.5A/div)

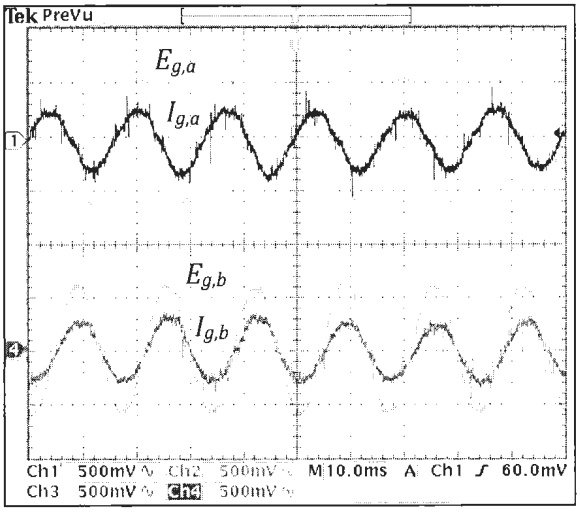


Figure 4-40: Phase voltages (75V/div) and currents (2.5A/div) at unity power factor. From top: Phase *a* voltage and current, Phase *b* voltage and current

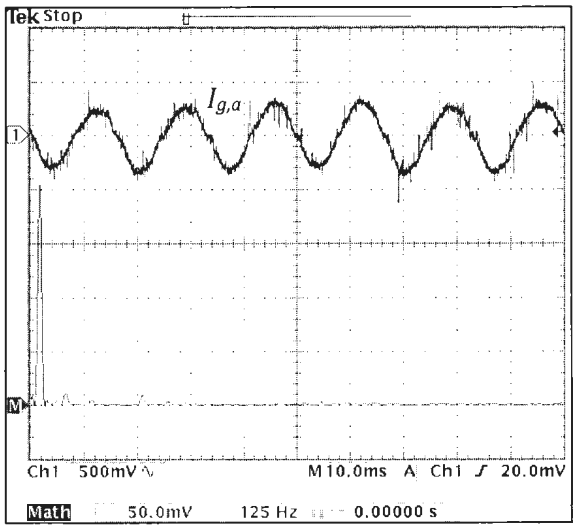
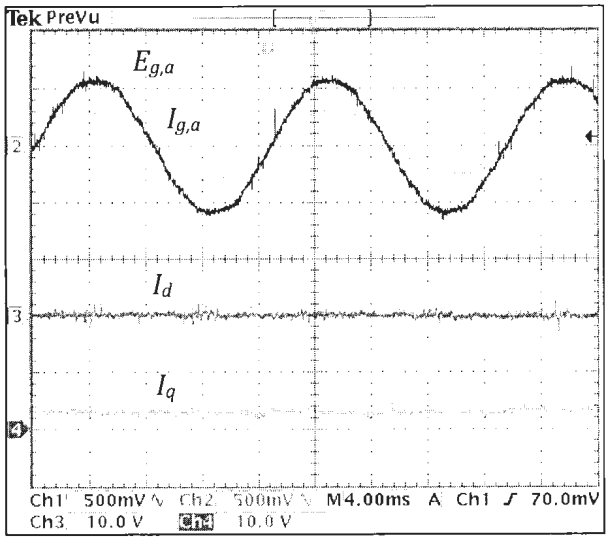


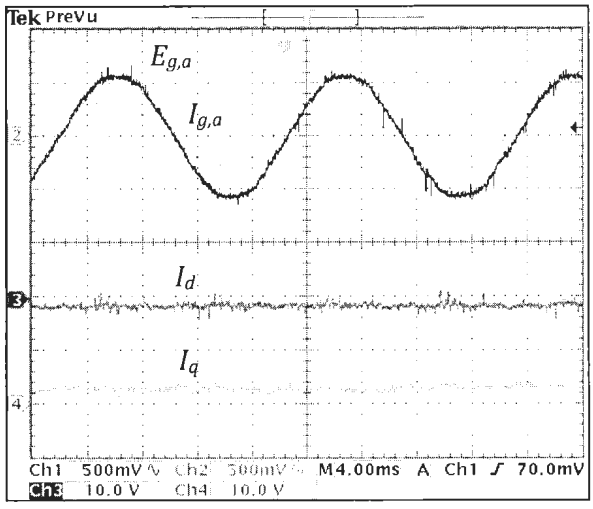
Figure 4-41: Harmonic spectrum of the input line current

The front-end ac-dc converter utilizing the proposed VFOC can be operated in three different power factor modes by providing proper value to the reactive power reference Q_{ref}. The reactive power reference is set to zero to obtain unity power factor operation which will result the phase a voltage is in phase with the phase a current as shown in Figure 4-42 (a). The measured d-axis current I_d is kept at 0A meanwhile q-axis current I_q has a positive value during the unity power factor mode. On the other hand, during the real-time implementation analysis, the Q_{ref} is set to approximately -74var and +74var in order to demonstrate a leading and lagging power operation modes as shown in Figure 4-42 (b) and (c), respectively. The measured line currents in a synchronous rotating reference frame I_{dq} successfully track the reference currents $I_{dq,ref}$ in both power factor modes. The real component of measured line current I_d is shifted down to a negative value which

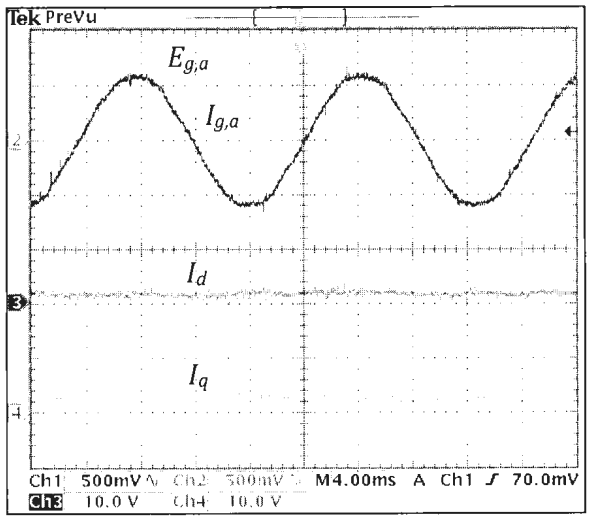
will cause the phase *a* current to lead the phase *a* voltage for leading power factor mode as shown in Figure 4-42 (b). Shifting, the line current I_d up to a positive value will cause the phase *a* current to lag the phase a voltage during lagging power operation mode as shown in Figure 4-42 (c). The magnitude of the complex component of measured line current I_q is kept constant and does not change significantly during all three power factor modes.



(a)



(b)



(c)

Figure 4-42: Generated waveforms during three different power factor operation modes. (a) Unity power factor (b) Leading power factor (c) Lagging power factor. From top: Phase a voltage (75V/div) and current (2.5A/div), d-axis current I_d and q-axis current I_q(5A/div)

Experimental tests are also conducted to verify the dynamic performance of the proposed VFOC. Figure 4-43 (a) and (b) show transient responses for sudden change of load power under unity power factor operation. The additional load resistors are abruptly connected and disconnected in parallel with the existing resistor at the output of the ac-dc converter to cause sudden increases and decreases in the load power demand. The magnitude of the measured q-axis current I_q and the phase a current $I_{g,a}$ are changing simultaneously to accommodate increases and decreases of the load power demand. The measured d-axis current I_d is kept at 0A to maintain unity power factor. The dc-link voltage V_{dc} level is kept almost constant at its reference value of 150V while maintaining the sinusoidal current line currents flowing through the ac-dc converter system.

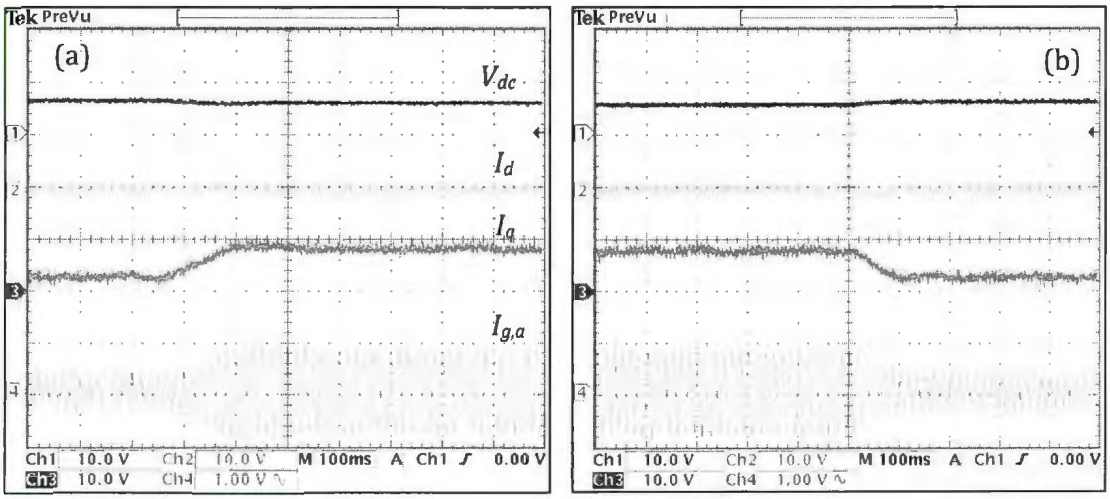


Figure 4-43: Dynamic response for load power changes. From top: Dc-link output voltage V_{dc} (250V/div), measured d-axis current I_d and q-axis current I_q, and phase a current (5A/div).
(a) Load power increasing 143% (b) Load power decreasing 143%

The converter's dynamic behaviors under step changes in dc output voltage reference $V_{dc,ref}$ are shown in Figure 4-44 (a) and (b). The voltage $V_{dc,ref}$ increases from 150V to 235V and decreases from 235V to 150V. With the proposed control method and the estimated parameters of the proportional integral regulators, the actual dc-link voltage V_{dc} increases and decreases according to the change of the dc voltage reference magnitude. Consequently, the measured three phase currents given by I_q and $I_{g,a}$ in Figure 4-44 are also increased and decreased steadily to new values while maintaining the d-axis I_d current at 0A.

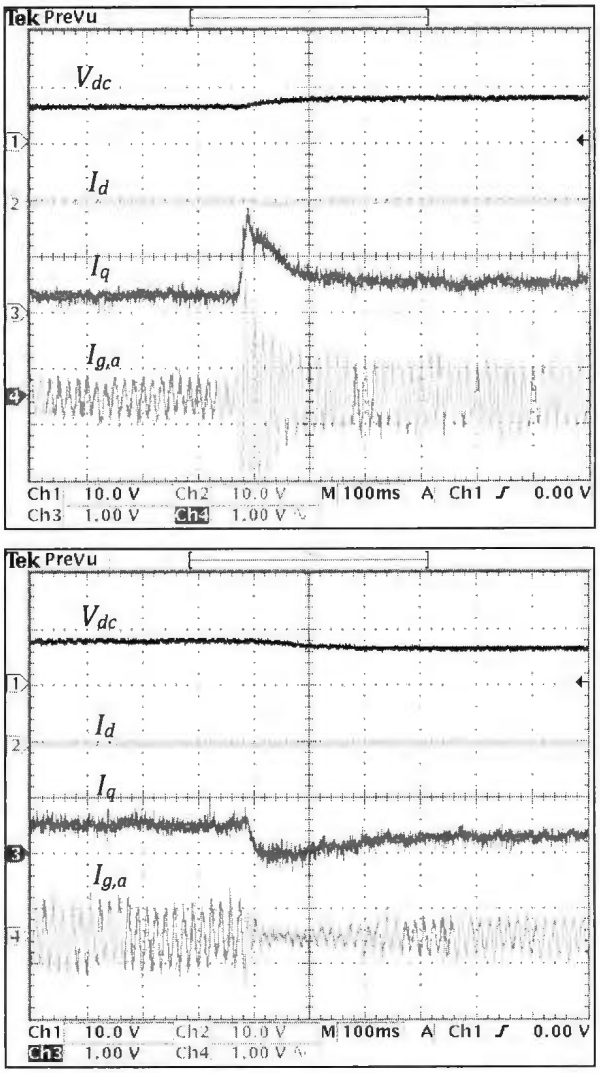


Figure 4-44: Dynamic response for changes in dc voltage reference $V_{dc,ref}$. rom top: Dc-link output voltage V_{dc} (250V/div), measured d-axis current I_d and q-axis current I_q, and phase *a* current (5A/div).
(a) $V_{dc,ref}$ increased from 150V to 235V (b) $V_{dc,ref}$ decreased from 235V to 150V

4.9 Experimental Results of the Proposed Virtual Flux Oriented Control under Unbalanced Three Phase Voltage Supply

Performance of the proposed VFOC is also experimentally studied during an unbalanced three phase voltage input condition. The unbalanced voltage supply is achieved by decreasing the magnitude of the phase *a* voltage to 66% of the voltage magnitude during the balanced condition. Figure 4-45 shows the experimental unbalanced three phase voltage waveforms with reduced magnitude on the phase *a* voltage. The proposed control method is able to maintain almost sinusoidal three phase currents with unity power factor and low total harmonic distortion as shown in Figure 4-46 and Figure 4-47. Due to the decrement of the phase *a* voltage magnitude, the magnitude of the phase *a* current is also slightly reduced compared with the currents on the other two phases. Figure 4-48 shows the experimental waveforms obtained during rapid change of load power. The magnitude of the measured q-axis current I_q and the phase a current $I_{g,a}$ are increasing simultaneously to fulfill increases of the load power demand. The measured *d*-axis current I_d is maintained at 0A and the dc-link voltage is kept at 150V according to its reference value.

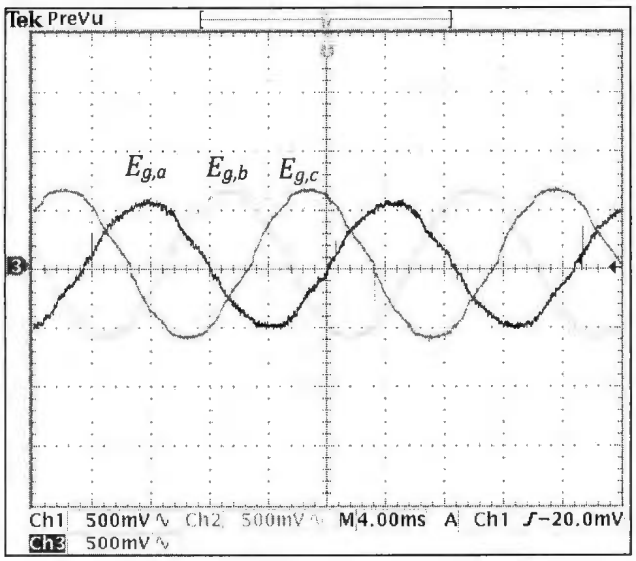


Figure 4-45: Unbalanced three phase input voltages (75V/div)

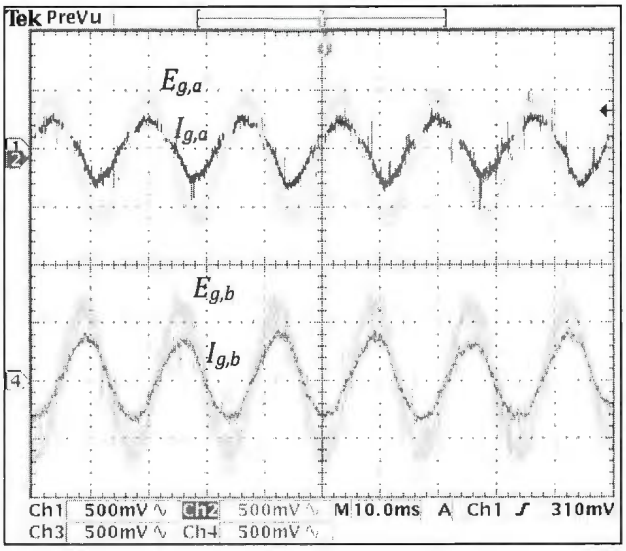


Figure 4-46: Phase voltages (75V/div) and currents (2.5A/div) at unity power factor. From top: Phase *a* voltage and current, Phase *b* voltage and current

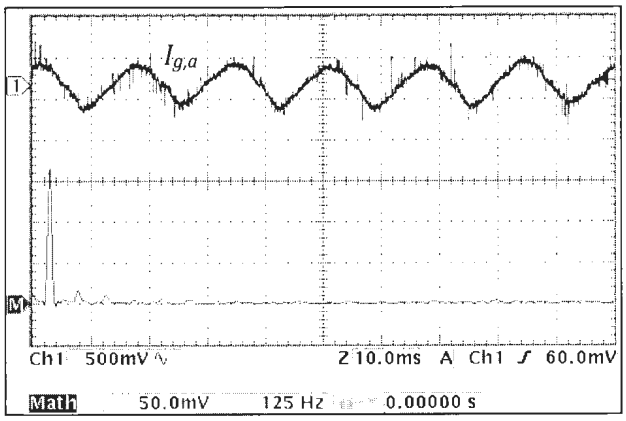


Figure 4-47: Harmonic spectrum of the input line current

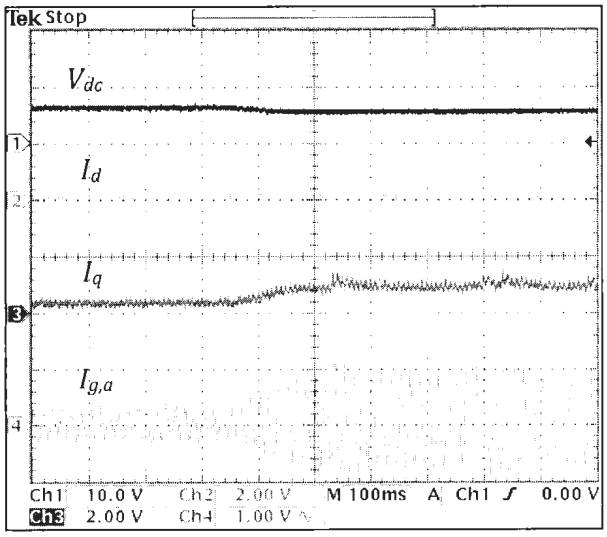


Figure 4-48: Dynamic response when the load power increased. From top: Dc-link output voltage V_{dc} (250V/div), measured d-axis current I_d and q-axis current I_q, and phase a current (5A/div)

4.10 Chapter Summary and Discussions

This chapter investigates a new approach to develop a control method for the front-end Pulse Width Modulator (PWM) ac-dc converter that is applicable for low and medium power voltage source inverter (VSI) system applications. The proposed Virtual Flux Oriented Control (VFOC) is developed by adapting and manipulating the Voltage Oriented Control (VOC) method and the instantaneous active and reactive power estimation techniques used in the Virtual Flux Direct Power Control (VFDPC). The use of three voltage sensors for measuring the magnitude and the angle of the grid three phase voltages, are avoided by applying a virtual flux concept in developing the control structure of the front-end ac-dc converter. The virtual flux control is used to extract the grid voltage information from the converter switching states, dc-link output voltage and three phase input currents. The voltage equations of the PWM ac-dc converter in a synchronous rotating reference frame incorporating the virtual flux components are newly derived. The proposed VFOC utilizes the decoupling control structure and feed-forward components to enhance the converter performance during balanced, unbalanced and distorted supply voltage. In addition, a digital phase locked loop (PLL) has been employed to estimate the grid virtual flux vector angle for the frame transformation purposes. A similar compensation method to correct the magnitude and phase errors of the estimated virtual flux components, used by a previously discussed Virtual Flux Direct Power Control (VFDPC), is implemented in the proposed VFOC. The VFOC scheme which

consists of the discrete proportional integral (PI) regulators in the outer voltage control loop and the inner current control loop, and operates with the sinusoidal pulse width modulator, has been successfully simulated in a Matlab/Simulink discrete environment. The experimental prototype of the ac-dc converter has been developed to implement and verify the proposed control method. The control algorithm is developed by using Matlab/Simulink and the real-time implementation with the dSPACE DS1104 digital signal processing board. The simulation and experimental results show that the proposed VFOC is able to produce fixed switching frequency with good performance both in steady-state and transient conditions.

Chapter 5

Experimental Set-up

5.1 Hardware Development

The experimental set-up is developed in the MUN Power Devices and System Research Lab in order to study and examine the operating characteristics of the proposed Virtual Flux Direct Power Control (VFDPC) and Virtual Flux Oriented Control (VFOC) schemes. Figure 5-1 shows the picture of the whole experimental set-up used in this work. The main components of the experimental set-up are labeled as follows:

(1) Three phase transformer

(2) Three phase variable tap transformer

(3) Circuit breaker

(4) Three phase line inductors

(5) Voltage and current sensors

(6) Three phase pulse width modulated ac-dc converter

(7) IGBT driver modules

(8) Dc power supply for the driver modules

(9) Dc-link capacitors

(10) Resistor bank

(11) Digital Signal Processor DS1104 connector panel

(12) Digital scopemeter

(13) Oscilloscope

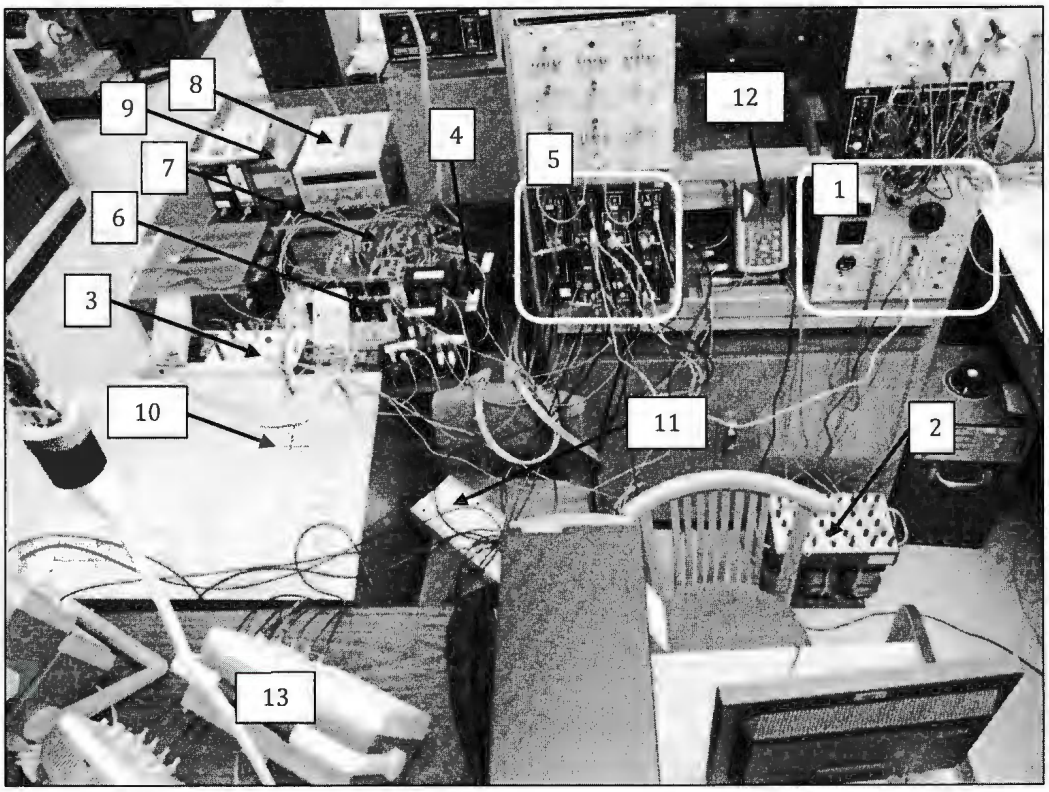


Figure 5-1: Physical layout of the main components in experimental set-up

A three phase pulse width modulated ac-dc converter is constructed using six power insulated gate bipolar transistors (IGBTs) type G4PSC71K and six ultrafast high voltage diodes type HFA08TB60 from International Rectifier. Each IGBT is rated at 600V, 60A and connected with an anti parallel ultrafast recovery high voltage diode. The rating of each diode is 600V, 8A. Figure 5-2 shows the picture of

the three phase ac-dc converter power circuit. The ac-dc converter is connected to the three phase transformer via three phase line inductors. Two inductors are connected in series to obtain a total inductance of 15mH at each phase. The inductors are rated at 20A, 50/60Hz and manufactured by Hammond. The photographs of the three phase transformer and the line inductors are shown in Figure 5-3 and Figure 5-4, respectively.

The dc-link electrolytic type capacitor at the output of the ac-dc converter is used to reduce the ripple and obtain a stable and constant dc voltage. The capacitor is connected in parallel with a load of resistor bank. The resistor bank is used to perform various experimental tests involving load power demand changes. Figure 5-5 and Figure 5-6 show the dc-link capacitor and the resistor bank used in the experiments.

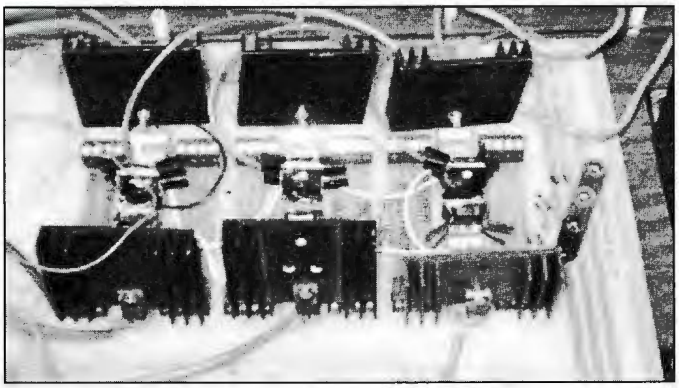


Figure 5-2: Three phase ac-dc converter power circuit

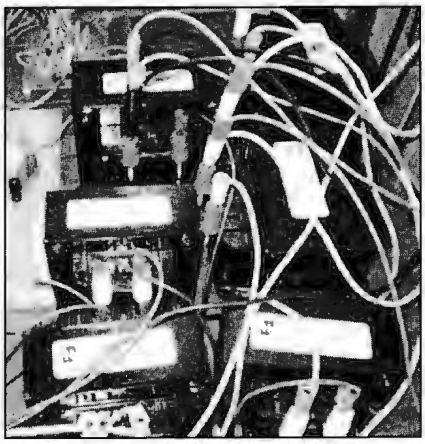


Figure 5-3: Three phase line inductors

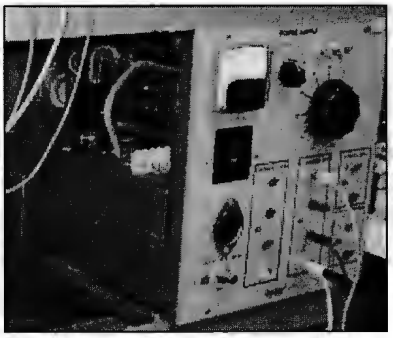


Figure 5-4: Three phase transformer

Figure 5-5: Dc-link capacitor

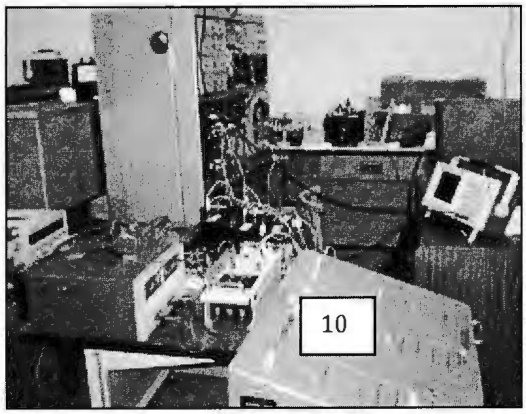


Figure 5-6: A resistor bank is shown by a label 10 in the experimental set-up picture

An IGBT is a voltage controlled device that needs an appropriate level of voltage to be supplied across its gate-emitter terminals in order to turn the device on and off. According to the technical data specifications, the IGBT requires voltage in the range of +15V to +20V to turn on, and 0V to -20V to turn off. However, the negative voltage magnitude is preferred for turning the power device off. The negative voltage will completely discharge the IGBT's internal input capacitance. Therefore, the gate drivers are developed as an interface between the DSP board signal output terminals and the power switches terminals. The gate drivers receive the switching signals from the DS-1104 terminals and amplify them to the correct level to drive the IGBT devices. Three modules of gate driver are developed with each module is used to drive the two IGBTs which are connected in series on the same leg of the ac-dc converter. Each module consists of three main parts, namely an isolated switch mode dc-dc converter, a dead time control and optocoupler circuits. The switch

mode dc-dc converter is constructed by using a push-pull topology due to its ability to step up the low input 12V dc voltage and provide isolated grounding points to the IGBTs. Figure 5-7 shows a structure layout of the isolated dc-dc converter which provides two ±15V dc output voltages with two isolated grounding systems. The two MOSFETs are driven by high frequency pulses produced by the PWM generator integrated chip (IC) type SG3524 manufactured by STMicroelectronics. The high frequency transformer is constructed such that there are two secondary centre tap windings for generating two isolated dc output voltage supplies. The transformer is wound around the EFD10 magnetic core. The switching signals from the transformer secondary windings are fed to the voltage regulators to obtain constant ±15V dc voltage.

Dead-time control is necessary to provide protection against a shoot-through fault in the converter leg. The dead time control block is adjusted manually by changing a resistance value of the variable resistor shown in Figure 5-8. The switching signals from the dead time control block are connected to the two optocoupler circuits as presented in Figure 5-9. Two gate drive optocoupler ICs type HCPL3150 manufactured by Hewlett Packard are utilized to provide isolation and protection of the DSP controller board from any incoming surge or high voltage signals from the power ac-dc converter. Figure 5-10 shows the picture of developed gate driver modules for the three phase PWM ac-dc converter.

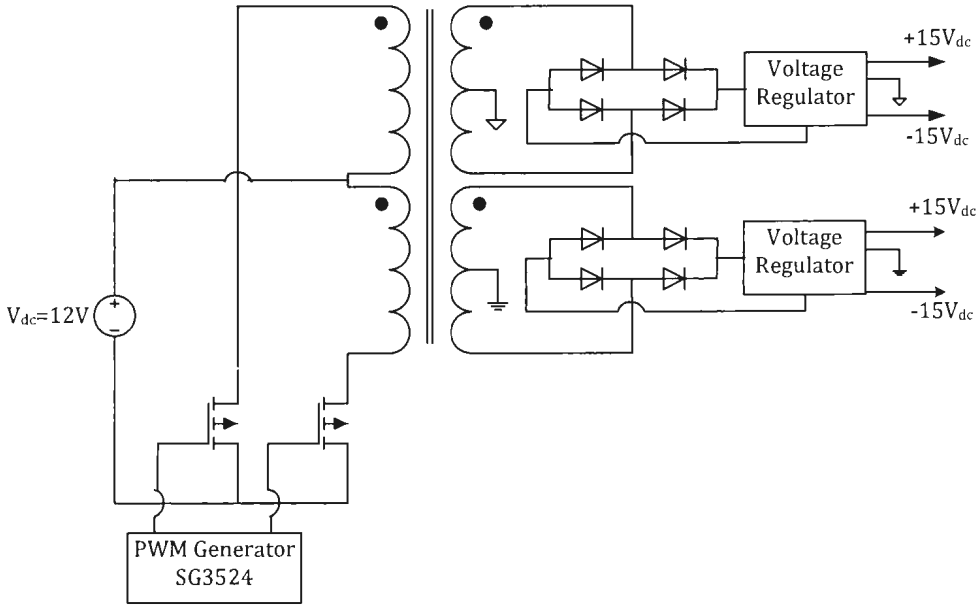


Figure 5-7: Isolated switch mode dc-dc converter topology

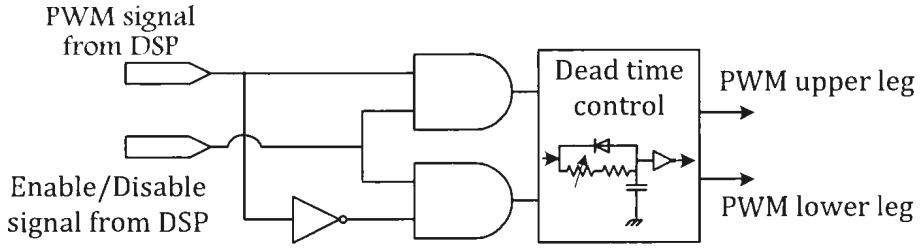


Figure 5-8: Dead time control block diagram

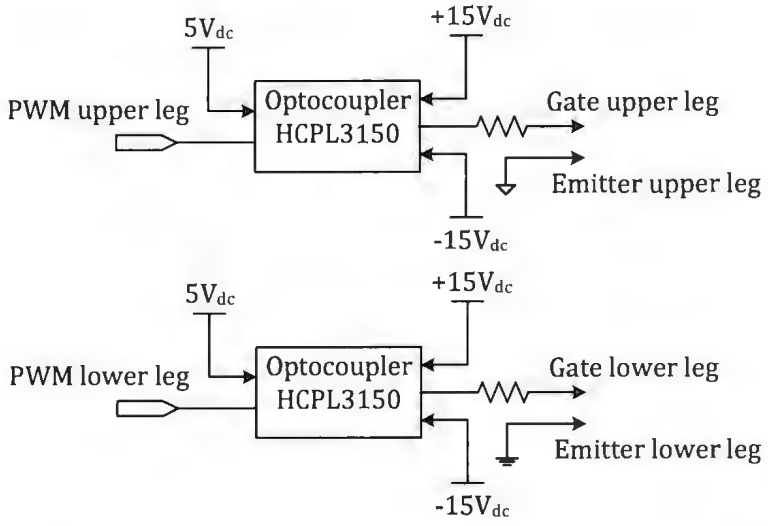


Figure 5-9: Gate drive optocoupler block diagram

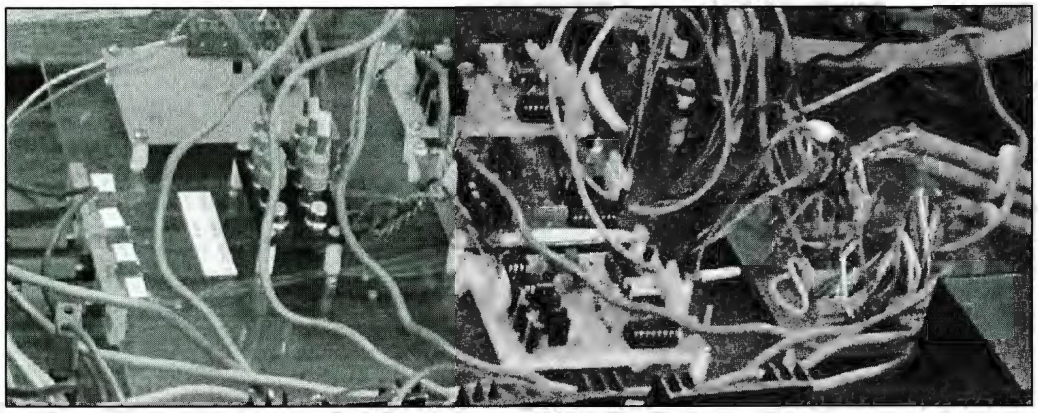


Figure 5-10: Gate driver modules for three phase ac-dc converter

5.2 DS1104 Digital Signal Processing Board

The controlled and PWM signals generation for the three phase ac-dc converter are practically implemented by utilizing the DS1104 controller board inserted in a desktop computer. The DS1104 DSP board consists of a MPC8240 floating point digital signal processor with a CPU speed of 250Mhz as the 64-bit master (main) processor, and a TMS320F240 fixed point digital signal processor with a CPU speed of 20Mhz as the 16-bit slave processor. The connector panel as shown in Figure 5-11 provides easy-to-use connections between the DS1104 and the devices to be connected to it. Some of the main features offered by the controller board are summarized as follows:

- Four muxed channels 16-bit analog to digital converter (ADC) and four channels 12-bit ADC. The ADC has ± 10V input voltage range. Therefore, all the measurement signals have to be rescaled before entering the DSP board via the DSP connector panel.
- Eight channels 16-bit digital to analog converter (DAC). The DAC has ± 10V output voltage range.
- 20-bit digital input/output (I/O) with Transistor-Transistor Logic (TTL) I/O levels. According to the standard technical specifications, TTL circuits operate with a 5V power supply. A TTL input signal is defined as "low" when the magnitude of the input signal voltage is between 0v and 0.8V, and "high" when the magnitude is between 2.2V and 5V. Meanwhile, the TTL "low"

output signal has a voltage level between 0V and 0.4V, and between 2.6V and 5V for a "high" output signal.

- The slave processor supports high speed Pulse Width Modulation (PWM) signals generation which includes one independent three phase PWM output and four independent single phase PWM output.
- ControlDesk software is provided by the dSPACE for managing and monitoring the Matlab/Simulink operation and the real-time implementation. The ControlDesk provides a platform for the user to change the control parameters and monitoring the important waveforms from the converter system in a real-time manner without interrupting the whole system operation. Figure 5-12 (a) and (b) show the screenshots of ControlDesk software used in the proposed control schemes.

Figure 5-11: Digital Signal Processor DS1104 connector panel

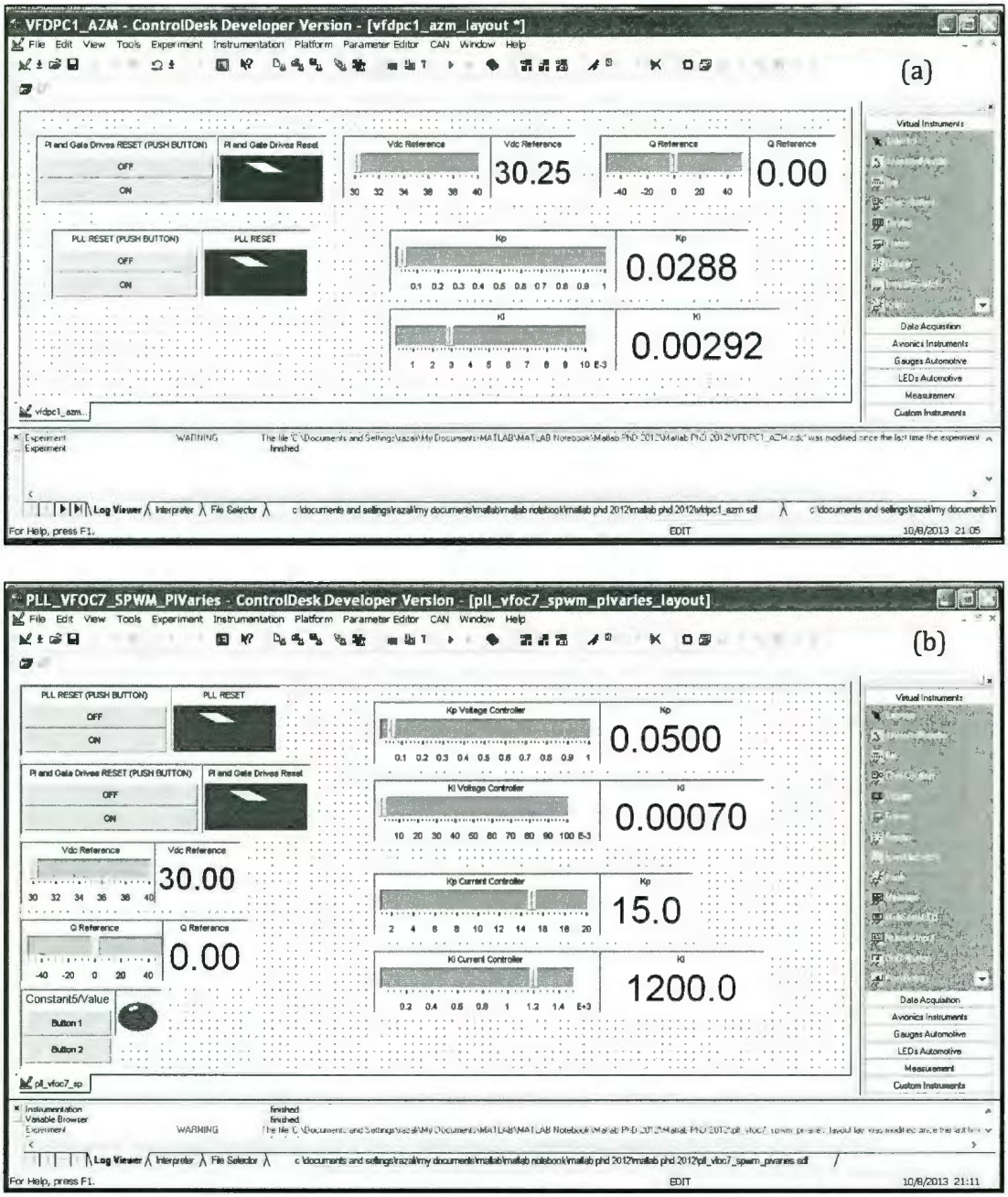


Figure 5-12: Screenshots from the ControlDesk software. (a) Screenshot of the proposed Virtual Flux Direct Power Control (b) Screenshot of the proposed Virtual Flux Oriented Control

Chapter 6

Conclusions and Suggestions for Future Work

The aim of this thesis is to obtain theoretical and practical knowledge about the operation, control and implementation of a grid connected front-end three phase ac-dc converter. Two control methods for the three phase ac-dc converter have been developed, analyzed and implemented. The first control method, the Virtual Flux Direct Power Control (VFDPC) utilizes a virtual flux concept in the control scheme. The virtual flux control technique is used to extract the grid voltage information from the converter switching states, dc output voltage, and line currents. Two improvements on the VFDPC have been proposed in this thesis. The first improvement is on the aspect of virtual flux estimation procedures and the second improvement is on the aspect of the proper switching state selection by the switching look-up table.

In subchapter 3.2, detailed explanations are given regarding a method to compensate for the virtual flux magnitude and phase errors produced by a conventional simple low-pass filter. Those errors are undesirable since they can generate an incorrect selection of the voltage vectors from the switching look-up table.

The fundamental idea of Direct Power Control (DPC) is a direct control of active and reactive powers without any internal current control loop and pulse width

modulator. The switching states for the power converter are selected via a switching table. The states are chosen based on the instantaneous error between the measured and the desired active and reactive powers. Therefore, the accuracy of the power calculations is required to achieve satisfactory performance. The correct result of power calculations is obtained by using the appropriate mathematical equations of active and reactive powers. Subchapters 3.3.1 and 3.3.2 present an intensive explanation of the steps required for deriving the active and reactive powers which incorporate the virtual flux theory in both the synchronous rotating reference frame and the stationary reference frame. The derivation procedures of the active and reactive powers presented in this thesis lead to the development of a new switching look-up table for VFDPC. A comprehensive and systematic approach has been presented in developing the switching table. The switching table is developed by differentiating the active and reactive power equations. In this way, the switching table is able to choose the best converter voltage vector in order to ensure smooth control of instantaneous active and reactive powers.

Fixed band hysteresis controllers used in the VFDPC have been recognized as a major contribution of variable switching frequency in the signals sent to the power switches of the ac-dc converter. In order to overcome the problem of variable switching frequency experienced by the VFDPC while preserving the advantages of applying a virtual flux concept in the control system, another control scheme for the three phase ac-dc converter has been proposed. The new control scheme namely, the Virtual Flux Oriented Control (VFOC) is introduced and developed from the

knowledge of Voltage Oriented Control (VOC) operation and the active and reactive powers derivation procedures. A mathematical model of the voltage source rectifier (ac-dc converter) incorporating the virtual flux components as shown by the equations (4.13) and (4.14) are newly derived. Both equations are used for developing the control structure of VFOC. Consequently, the proposed VFOC is able to include the decoupling and the feed-forward components to enhance the converter performance during both steady state and transient conditions. Some guidelines for tuning the proportional integral (PI) parameters of the current controller as well as the dc-link voltage controller are given in Chapter 4. The step and frequency response analysis have been used to verify and guide the selection of the PI parameters.

Simulations and experiments on the proposed VFDPC and VFOC schemes for the three phase ac-dc converter have been conducted to investigate and analyze the converter's steady state and dynamic performances under balanced, unbalanced and distorted voltage supply conditions. The results show that the VFDPC utilizing the new switching look-up table and the new VFOC scheme are able to produce almost sinusoidal three phase input currents with low total harmonic distortion, unity power factor, and adjustable power factor operation mode and dc-link output voltage.

While performing the study, the thesis makes the following contributions:

i) It performs a derivation technique to estimate the input instantaneous active and reactive power based on the grid virtual flux in both the stationary reference frame and the rotating synchronous reference frame.

ii) It proposes an improved grid virtual flux estimator, to correct the magnitude and phase errors of the grid virtual flux estimation.

iii) It introduces a comprehensive and systematic approach in developing a new switching table for virtual flux direct power control (VFDPC). The approach will provide detailed information regarding the effects of a particular converter voltage vector to the active and reactive power distributions.

iv) It proposes a new virtual flux oriented control (VFOC) method which operates without grid voltage sensors. The control scheme generates a fixed switching frequency and utilizes the decoupling and feed-forward components to enhance the converter control performance during balanced and non-ideal conditions of grid voltage supply.

v) A mathematical model of the three phase ac-dc converter in a rotating synchronous reference frame incorporating the virtual flux concept is newly derived. The model is used to develop the VFOC structure.

vi) It develops a simulation and an experimental set-up to verify the proposed improvement schemes on the VFDPC and the newly designed VFOC. The development of the control algorithms is performed using Matlab/Simulink and the real-time implementation with a dSPACE DS-1104 digital signal processor board.

Several recommendations for future work are listed as follows:

- Investigation on the application of the front-end PWM rectifier working with the proposed control schemes having an output load of voltage source inverter driving the electrical machine in general.
- Investigation on the application of the proposed control methods to grid connected inverter system where the dc voltage is supplied by the batteries, solar cells or fuel cells.
- The technique used in developing the new switching table, can be extended for developing a switching table for multi-level converter.
- The sinusoidal pulse width modulation (SPWM) is used by the proposed VFOC to produce a fixed switching frequency. However, other switching strategies such as a space vector modulation (SVM) and a third harmonic injection sinusoidal pulse width modulation (THISPWM) can be investigated for replacing the SPWM.
- Application of intelligent control techniques such as neuro-fuzzy, neural network, fuzzy logic and genetic algorithm incorporating a switching table in

the Virtual Flux Direct Power Control can be further investigated to enhance the converter performance both in steady and transient state conditions.

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Appendix I

*/New Switching Table for the Virtual Flux Direct Power Control Used in the Three Phase PWM AC-DC Converter */
/Written by Azziddin Mohamad Razali/

```
static void mdlInitializeSizes(SimStruct *S)
{
    ssSetNumContStates(S,0);   /* number of continuous states */
    ssSetNumDiscStates(S,0);   /*number of discrete states */
    ssSetNumInputs(S,3);       /* number of inputs */
    ssSetNumOutputs(S,3);      /* number of outputs */
    ssSetDirectFeedThrough(S,1);  /* direct feedthrough flag */
    ssSetNumSampleTimes(S,1); /* number of sample times */
    ssSetNumInputArgs(S, 0);
    ssSetNumRWork(S,0);        /* number of real work vector elements */
    ssSetNumIWork(S,0);    /* number of integer work vector elements*/
    ssSetNumPWork(S,0);    /* number of pointer work vector elements*/
    ssSetNumModes(S,0);    /* number of mode work vector elements */
    ssSetNumNonsampledZCs(S,0);/*number of nonsampled zero crossings*/
    ssSetOptions(S,0);         /* general options (SS_OPTION_xx) */
}

static void mdlInitializeSampleTimes(SimStruct *S)
{
    ssSetSampleTime(S, 0, INHERITED_SAMPLE_TIME);
    ssSetOffsetTime(S, 0, 0.0);

}

static void mdlInitializeConditions(real_T *x0, SimStruct *S)
{

}

static void mdlOutputs(real_T *y, const real_T *x, const real_T *u,
                       SimStruct *S, int_T tid)
{
/* Inputs: active power u[2], reactive power u[1]  and angle u[2]

For active power =1 (increase) */

  if(u[0] == 1 & u[2] == 1 & u[1] == 1){
    y[0] = 0; y[1] = 1; y[2] = 1;}
 else if(u[0] == 1 & u[2] == 1 & u[1] == 0){
    y[0] = 1; y[1] = 0; y[2] = 1;}
```

```
 else if(u[0] == 1 & u[2] == 2 & u[1] == 1){
    y[0] = 0; y[1] = 1; y[2] = 0;}
 else if(u[0] == 1 & u[2] == 2 & u[1] == 0){
    y[0] = 1; y[1] = 0; y[2] = 1;}
 else if(u[0] == 1 & u[2] == 3 & u[1] == 1){
    y[0] = 0; y[1] = 1; y[2] = 1;}
 .
 .
 .

}

static void mdlUpdate(real_T *x, const real_T *u, SimStruct *S, int_T
tid)
{
}

static void mdlDerivatives(real_T *dx, const real_T *x, const real_T *u,
SimStruct *S, int_T tid)
{
 }

static void mdlTerminate(SimStruct *S)
{

}

                        /* This file being compiled as a MEX-file */
                        /* MEX-file interface mechanism */

                        /* Code generation registration function */
```

Appendix II

List of technical papers which have been written and published related to this work:

1. A. M. Razali, M. A. Rahman, G. George and N. A. Rahim, "An Analysis of Direct Power Control for Three Phase AC-DC Converter," a revised paper has been submitted to the *Industry Applications, IEEE Transactions* on 2013.

2. A. M. Razali, M. A. Rahman and N. A. Rahim, "An Analysis of Current Control Method for Grid Connected Front-end Three Phase AC-DC Converter," International Energy Conversion Congress and Exhibition for Asia/Pasific (ECCE) 2013, Melbourne, Australia.

3. A. M. Razali, M. A. Rahman and G. George, "An Analysis of Direct Power Control for Three-Phase AC-DC Converter," in IEEE Industry Application Society Conference (IAS), October 2012, Las Vegas, USA.

4. A. M. Razali and M. A. Rahman, "Virtual Grid Flux Oriented Control Method for Front-end Three Phase Boost Type Voltage Source Rectifier," in Canadian Conference on Electrical and Computer Engineering (CCECE), 2012, Montreal, Canada.

5. A. Aktaibi, M. A. Rahman, A. M. Razali, "An Experimental Implementation of dq axis Wavelet Packet Transform Hybrid Technique for 3Ø Power Transformer Protection," in IEEE Industry Application Society conference (IAS), October 2012, Las Vegas, USA.

6. A. Aktaibi, A. M. Razali, M. A. Rahman, "Real-Time Testing of a d-q axis Wavelet Packet Transform Based Hybrid Digital Technique for Differential Protection of Salient Pole Synchronous Generator," in Newfoundland Electrical and Computer Engineering Conference (NECEC), 2012, Newfoundland, Canada.

7. A. M. Razali and M. A. Rahman, "Performance Analysis of Three-Phase PWM Rectifier Using Direct Power Control," in Electric Machines & Drives Conference (IEMDC), 2011 IEEE International, 2011, pp. 1603-1608.

8. A. M. Razali and M. A. Rahman, "Grid Voltage Sensorless Control Method for Front-end PWM Rectifier Connected to the Voltage Source Inverter," in

Newfoundland Electrical and Computer Engineering Conference (NECEC), 2011, Newfoundland, Canada.

9. A. M. Razali and M. A. Rahman, "Simulation Study of Three-Phase PWM Rectifier Based on Direct Power Control with Grid Voltage Sensorless Strategies," in Newfoundland Electrical and Computer Engineering Conference (NECEC), 2010, Newfoundland, Canada.

10. Aktaibi A., M. A. Rahman and A. M. Razali, "A Critical Review of Modulation Techniques," in Newfoundland Electrical and Computer Engineering Conference (NECEC), 2010, Newfoundland, Canada.