Circuit performance: The chips were measured on-wafer by using 50Ω coplanar test probes. The measured minimum input sensitivity V_{in} against input frequency f_{in} of the divider is plotted in Fig. 3. Above the minimum input voltage, reliable operation is guaranteed. More input power is required at lower frequencies because the circuit needs a minimum turn-on/off time for the input sinewave signal. That is, the input amplitude should be increased to maintain a required slew rate for a sinewave input signal at lower frequencies. The resonance frequency is ~48.5GHz. High sensitivity of < $0.7V_{p\text{-}p}$ amplitude was obtained in the frequency range 37–55GHz The measured input and output waveforms, and the output spectrum of the 1:2 dynamic dividers at the input frequency of 55GHz are shown in Fig. 4*a* and *b*, respectively. It should be noted that our test system has so far been defined up to 50GHz. The differential output voltage swing is $370mV_{p\text{-}p}$ at these maximum operating frequencies. The power dissipation is 300mW using two supply voltages of 4 and –2.5V.

Conclusion: The design and performance of a 'digital' dynamic frequency divider has been presented. The dynamic frequency divider operates reliably up to 55GHz that reaches V-band millimetre-wave frequencies and is close to the f_T of the used transistors. The high-speed performance of the frequency divider is suitable for application in measurement equipment, microwave, millimetre-wave, and satellite communication systems.

Acknowledgments: The authors thank G. Weimann for encouragement. The authors also thank the HEMT processing staff for fabrication of these circuits. The work was supported by the German Ministry for Education and Research BMBF.

© IEE 1998
27 July 1998
Electronics Letters Online No: 19981336

Z. Lao, A. Thiede, J. Hornung, M. Schlechtweg, H. Lienhart, W. Bronner, A. Hülsmann, T. Jakobus, J. Seibel, M. Sedler and G. Kaufel (*Fraunhofer-Institute of Applied Solid-state Physics, Tullastrasse 72, D-79108 Freiburg, Germany*)

Z. Lao: Now with Rockwell Semiconductor Systems, Newbury Park, CA 91320, USA

References

1 THIEDE, A., TASKER, P., HÜLSMANN, A., KÖHLER, K., BRONNER, W., SCHLECHTWEG, M., BERROTH, M., BRAUNSTEIN, J., and NOWOTNY, U.: '28-51GHz dynamic frequency divider based on 0.15μm T-Gate $Al_{0.2}Ga_{0.8}As/In_{0.25}Ga_{0.75}As$ MODFETs', *Electron. Lett.*, 1993, **29**, (10), pp. 933–934

2 KURISU, M., UEMURA, G., OHUCHI, M., OGAWA, C., TAKEMURA, H., MORIKAWA, T., and TASHIRO, T.: 'A Si bipolar 28GHz dynamic frequency divider'. ISSCC Tech. Dig., 1992, pp. 92–93

3 SARKISSIAN, J.-C., CAMIADE, M., SAVARY, P., SUAREZ, A., QUERE, R., and OBREGON, J.: 'A 60-GHz HEMT-MMIC analog frequency divider by two', *IEEE J. Solid-State Circuits*, 1995, **SSC-30**, (10), pp. 1062–1067

4 MILLER, R.L.: 'Fractional frequency generators utilizing regenerative modulation', *IRE Tech. Dig.*, July 1939, **27**, pp. 446–457

5 RAZAVI, B.: 'Challenges in the design of frequency synthesizers for wireless applications'. IEEE CICC Tech. Dig., 1997, pp. 395–402

6 JAKOBUS, T., BRONNER, W., HOFMANN, P., HÜLSMANN, A., KAUFEL, G., KÖHLER, K., LANDSBERG, B., RAYNOR, B., SCHNEIDER, J., GRÜN, N., WINDSCHEIF, J., BERROTH, M., and HORNUNG, J.: 'Stability of an AlGaAs/GaAs/AlGaAs E/D-HEMT process with double pulse doping'. Int. Symp. GaAs and Related Compounds, 1992, Inst. Phys. Conf. Ser. no. 129, Chap. 11, pp. 887–892

'Backgating' model including self-heating for low-frequency dispersive effects in III-V FETs

A. Santarelli, F. Filicori, G. Vannini and P. Rinaldi

A new approach is proposed which takes into account both traps and thermal phenomena for the modelling of deviations between static and dynamic drain current characteristics in III-V field effect transistors. The model is based on the well-known 'backgating' concept and can easily be identified on the basis of conventional static drain current characteristics and small-signal, low-frequency S parameters. Experimental results confirm the accuracy of the proposed model.

Introduction: Accurate nonlinear models of III-V field effect transistors FETs for microwave circuit design should also account for low-frequency dispersion of the electrical characteristics due to deep level traps and surface states. These phenomena cause considerable deviations between 'static' and 'dynamic' (e.g. pulsed) measurements of the DC characteristics, or, in terms of differential parameters, frequency dependent behaviour of the trans-admittance and output impedance even at low frequencies (e.g. < 100kHz).

The time constants associated with the dynamics of self-heating, which become relevant in an electron device especially under large-signal operation, although longer, are not always very different from those associated with traps or surface states (typically from fractions to hundreds of microseconds). Consequently, dispersion due to 'traps' (with this term hereafter we refer to both surface state densities and deep level traps) cannot always be dealt with separately from the dynamics of thermal effects due to self-heating.

The empirical modelling approach of dispersive phenomena presented in [1] provides very good predictive capabilities of bias-dependent dynamic drain current deviations due to traps and thermal effects in FETs. Moreover, its technology independence has been widely verified [1, 2]. However, owing to the need for non-conventional instrumentation for pulsed measurements, model identification could be cumbersome. In this Letter a simplified approach to modelling the dynamic drain current is presented, which allows for an identification procedure based on conventional DC and small-signal low-frequency (e.g. the lowest operation frequency of a microwave network analyser) S-parameter measurements. The model can easily be embedded both in conventional nonlinear equivalent circuits and look-up-table based black-box models.

Backgating model with self-heating: The proposed model is based on the assumption that the macroscopic dynamic effects on the drain current due to traps can be described in terms of a distributed electrical coupling (with very low cutoff frequency) between the gate/drain electrodes and the semi-insulator bulk (*'self-backgating'*) [3, 4]. This can be expressed by introducing in the drain current characteristic F^{DC} an equivalent gate voltage v_{gx}:

$$i_d(t) = F^{DC}\{v_{gx}(t), v_d(t)\} \qquad (1)$$

where

$$v_{gx}(t) = v_g(t) + \alpha_g(v_g(t) - V_{g0}) + \alpha_d(v_d(t) - V_{d_0}) \qquad (2)$$

V_{g_0}, V_{d_0} being the average values of the applied voltages $v_g(t)$, $V_d(t)$ and α_g, α_d suitable parameters to be determined. Note that under static conditions we have $v_{gx} \equiv v_g$, while under dynamic operation, at a frequency above the cutoff of dispersive effects, α_g and α_d account for deviations due to traps by 'feeding back' to the gate ('backgating') dynamic voltage deviations $v_g(t) - V_{g_0}$ and $v_d(t) - V_{d_0}$. This approach, although successfully used by some authors [4, 5], can accurately predict dynamic drain current deviations only when self-heating effects due to power dissipation are practically negligible. An improvement in the model accuracy can be achieved by introducing a suitable additional power-dependent term. To this end, it is convenient to introduce the dynamic channel temperature deviation

$$\Delta\theta(t) = \theta_s(t) - \theta_0 = R_\theta(p_s(t) - P_0) \qquad (3)$$

which virtually represents the difference between the temperature $\theta_s(t)$ under quasi-static operation and the actual channel

temperature θ_0 (which can be assumed constant for operation above the thermal cutoff) due to the average dissipated power P_0 under dynamic conditions. In eqn. 3 R_θ is the thermal resistance, and $p_s(t) \doteq F^{DC}\{v_g(t), v_d(t)\} \cdot v_d(t)$ is a virtually 'quasi-static' dissipated power, i.e. the power which would be dissipated if $v_g(t)$, $v_d(t)$ were 'slowly' time-varying voltages.

By assuming that the current dependence on the channel temperature θ can be approximated through a multiplying 'scaling' factor (i.e. temperature sensitivity is mainly due to carrier mobility variations) linearly dependent on $\Delta\theta$, we can write

$$i_d(t) = [1 + k_\theta R_\theta(p_s(t) - P_0)] \cdot F^{DC}\{v_{gx}(t), v_d(t)\} \quad (4)$$

where k_θ is a thermal sensitivity coefficient.

With respect to other models (see e.g. [6]), our approach can be applied starting from any existing model for the DC FET characteristics (based either on analytical expressions or look-up tables) and does not require pulsed measurements for its identification. In particular, the dynamic drain current is simply obtained from the DC expression by introducing the effects of the dynamic deviations of the voltages and dissipated power through only three additional parameters α_g, α_d and $K = k_\theta R_\theta$, which can be identified on the basis of conventional small-signal bias dependent measurements. To this end, eqn. 4 can be linearised, taking into account eqn. 2, with respect to $v_g(t)$ and $v_d(t)$ around a generic V_{g_0}, V_{d_0} quiescent bias condition, leading, respectively, to

$$g_m^{AC}\{V_{g_0}, V_{d_0}\} = [1 + K \cdot V_{d_0} \cdot I_{d_0} + \alpha_g] \cdot g_m^{DC}\{V_{g_0}, V_{d_0}\} \quad (5)$$

$$g_d^{AC}\{V_{g_0}, V_{d_0}\} = [1 + K \cdot V_{d_0} \cdot I_{d_0}] \cdot g_d^{DC}\{V_{g_0}, V_{d_0}\} + K \cdot I_{d_0}^2 + \alpha_d \cdot g_m^{DC}\{V_{g_0}, V_{d_0}\} \quad (6)$$

where $I_{d_0} = F^{DC}\{V_{g_0}, V_{d_0}\}$.

Eqns. 5 and 6 represent the low-frequency dynamic transconductance g_m^{AC} and output conductance g_d^{AC} as functions of the static drain current I_{d_0}, of its partial derivatives g_m^{DC}, g_d^{DC} and of the three model parameters α_g, α_d and K. The static transconductance g_m^{DC} and output conductance g_d^{DC} may be obtained, for instance, through numerical differentiation of the measured DC drain current or by analytical derivation of the mathematical expression used to model the static behaviour of the device. Moreover, g_m^{AC} and g_d^{AC} practically coincide with the real part of the corresponding small-signal, 'low-frequency' Y parameters measured at a suitable frequency above the cutoff due to dispersive effects but low enough to neglect high frequency charge storage phenomena. The Y parameters are easily obtainable from S-parameter measurements through known matrix transformation formulas. Thus, the three model parameters can easily be determined by minimising, over a suitable grid of bias conditions, the discrepancies between measured dynamic conductances and eqns. 5 and 6.

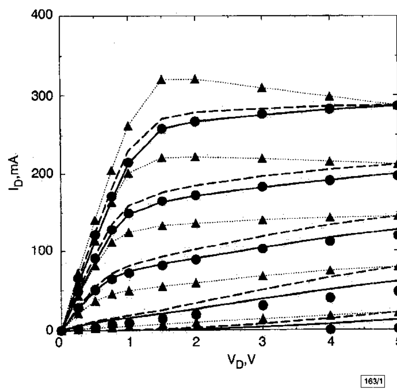

Fig. 1 *Static characteristics and comparison between measured and predicted pulsed drain currents for CFX32 GaAs MESFET*

Quiescent bias condition: $V_{g0} = 0$V, $V_{d0} = 5$V
Prediction of model including self-heating effects is clearly better than prediction obtained with two-parameter model
▲ static characteristics
● measured pulsed drain current
——— model including self-heating effects
– – – – two parameter model

Experimental results: The proposed model has been embedded in the HP-MDS programme for harmonic balance circuit analysis. In particular, the model equations have been implemented by using SDD (symbolically defined devices) components and two-dimensional look-up tables storing the measured values of the device DC characteristics $F^{DC}\{v_g, v_d\}$.

Experimental validation was carried out on a Philips CFX32 MESFET device which is characterised by relevant self-heating effects, as can be clearly seen from the negative slope at high V_{g_0}, V_{d_0} values of the DC characteristics shown in Fig. 1. In the same Figure the dynamic drain current characteristics predicted are compared with measurements obtained by applying short, simultaneous voltage pulses at the gate/drain electrodes starting from the quiescent condition $V_{g_0} = 0$V, $V_{d_0} = 5$V. Moreover, the accuracy improvement, obtained using the proposed model with respect to a two-parameter backgating model which does not account for self-heating, can be clearly seen.

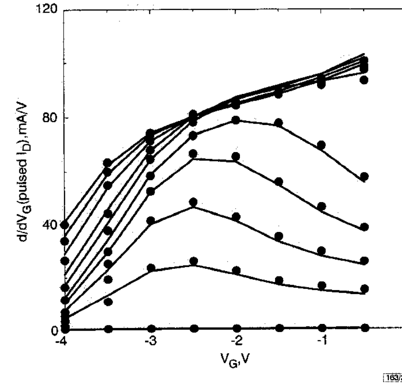

Fig. 2 *Numerical derivative with respect to V_g of measured and predicted pulsed drain current characteristics*

Quiescent bias condition: $V_{g0} = -2$V, $V_{d0} = 3$V
● measured
——— predicted

Good agreement was found, for different quiescent bias conditions, not only for the dynamic drain current (see Fig. 1) but also for its first order derivatives. As an example, Fig. 2 shows the derivatives with respect to V_g of the measured and predicted dynamic current characteristics for another quiescent bias condition ($V_{g_0} = -2$V, $V_{d_0} = 3$V). The agreement is quite good taking also into account the simplicity of the proposed model, which is based on only three 'global' parameters.

Acknowledgment: This work was partly supported by the Italian National Research Council under the MADESSII project.

© IEE 1998
11 August 1998
Electronics Letters Online No: 19981351

A. Santarelli and G. Vannini (*Research Center for Computer Science and Communication Systems, Italian National Research Council*)

F. Filicori (*Department of Electronics, Computer Science and Systems, University of Bologna, Viale Risorgimento 2, 40136 Bologna, Italy*)

P. Rinaldi (*Department of Electrical Engineering, University of Bologna, Viale Risorgimento 2, 40136 Bologna, Italy*)

G. Vannini: Also with Department of Electronics, Computer Science and Systems, University of Bologna, Viale Risorgimento 2, 40136 Bologna, Italy

References

1 FILICORI, F., VANNINI, G., SANTARELLI, A., MEDIAVILLA, A., TAZON, A., and NEWPORT, Y.: 'Empirical modeling of low-frequency dispersive effects due to traps and thermal phenomena in III-V FETs', *IEEE Trans.*, 1995, **MTT-43**, (12), pp. 2972–2981

2 SANTARELLI, A., VANNINI, G., BORGARINO, M., MENOZZI, R., BAYENS, Y., and VAN DER ZANDEN, K.: 'Modelling of low-frequency dispersive effects in GaAs and InP HEMTs'. Proc. GAAS'97, 1997, pp. 131–134

3 SCHEINBERG, N., BAYRUNS, R., and GOYAL, R.: 'A low frequency GaAs MESFET circuit model', *IEEE J. Solid-State Circuits*, 1988, **23**, (2), pp. 605–608

4 FIEGNA, C., FILICORI, F., VANNINI, G., and VENTURI, F.: 'Modeling the effects of traps on the IV-characteristics of GaAs MESFETs'. Proc. 1995 IEEE IEDM, 1995, pp. 773–776

5 JEON, K., KWON, Y., and HONG, S.: 'A frequency dispersion model of GaAs MESFET for large-signal applications', *IEEE MGWL*, 1997, **7**, (3), pp. 78–80

6 ROH, T., KIM, Y., SUH, Y., PARK, W., and KIM, B.: 'A simple and accurate MESFET channel-current model including bias-dependent dispersion and thermal phenomena', *IEEE Trans.*, 1997, **MTT-45**, (8), pp. 1252–1255

Impact of subchannel design on DC and RF performance of 0.1μm MODFETs with InAs-inserted channel

D. Xu, J. Osaka, T. Suemitsu, Y. Umeda, Y. Yamane and Y. Ishii

It isshown that a further performance improvement in MODFETs with InAs-inserted channel structures can be achieved by properly designing the subchannel layer that lies directly under the main channel of the InAs layer. The use of an $In_{0.30}Ga_{0.70}As$ layer grown with tensile strain on the InP substrate contributes to better accommodation of the 2D electron gas in the InAs layer. This translates to a > 10% increase in the maximum extrinsic transconductance and an 8% increase in the current gain cutoff frequency of a 0.1μm device.

Introduction: The performance of the modulation-doped field-effect transistor (MODFET) based on InP substrate has been significantly improved by using compressively strained In-rich InGaAs channel materials [1 – 4]. InAs is a desirable choice for channels because of its narrow bandgap of 0.35eV, which will form a deep quantum well and improve the confinement of the two dimensional electron gas (2DEG). In addition, the InAs layer has low alloy scattering and large Γ-L valley separation. The latter will translate to an advantage for high electric field transport, especially in short-gate-length MODFETs. Compared with the graded channel approach, intended for a larger total channel thickness for better 2DEG confinement [3, 5], the use of a thin layer of InAs in the channel is more favourable for better reproducibility of the epitaxy and subsequently fabricated devices.

However, bulk InAs has a lattice mismatch of ~3.5% with the InP substrate; therefore, it is very difficult to grow an InAs layer thick enough to form the whole channel on InP. Maeda *et al.* [6] introduced an In-rich subchannel, in addition to the InAs layer, to increase the average In content. However, this leads to degradation of 2DEG confinement in the InAs layer. We will show that this is actually a more important consideration in designing a subchannel layer. With the use of a Ga-rich subchannel, theoretical analysis clearly demonstrates a remarkable improvement in 2DEG confinement in the InAs layer. This results in improved in DC and RF performance.

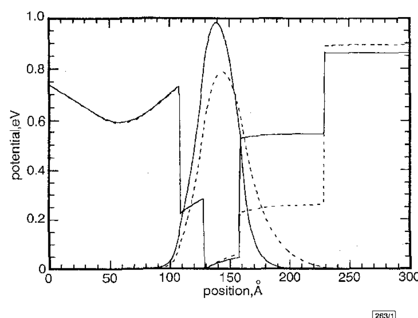

Fig. 1 *Minimum conduction-band energy diagram and squares of wave functions of electrons in first subbands of quantum wells of structures A and B*

– – – – structure A
——— structure B

Theoretical analysis and device fabrication: The MBE-grown MODFET structures consist of a 200nm i-InAlAs buffer, a 12nm i-InGaAs channel, a 2nm i-InAlAs spacer, a 5nm n^+-InAlAs supply layer, a 15nm i-InAlAs barrier and cap layers for non-alloyed ohmic contact. All the layers except the channel are lattice-matched to InP substrates, while the the Si doping density is $10^{19}/cm^3$ for all n^+ layers. Details of device fabrication can be found in [7]. Two channel designs were used. Structure A consists of a 7nm compressively strained $In_{0.70}Ga_{0.30}As$ subchannel with a 3nm InAs layer and a 2nm $In_{0.53}Ga_{0.47}As$ as the upper part of the channel [8]. In structure B, the 7nm compressively strained $In_{0.70}Ga_{0.30}As$ subchannel is replaced with a 7nm tensilely strained $In_{0.30}Ga_{0.70}As$ layer. We calculated the quantum states by self-consistently solving Schrödinger's and Poisson's equations. Fig. 1 shows the minimum conduction-band energy diagram and electron wave functions of structures A and B. Structure A has a first-subband energy of 0.19eV and Fermi level of 0.35eV; for structure B these values are slightly increased to 0.23 and 0.39eV, respectively. Use of $In_{0.30}Ga_{0.70}As$ leads to a remarkable shift of the 2DEG towards the InAs layer, resulting in a 17% population increase of first-subband electrons in the InAs layer.

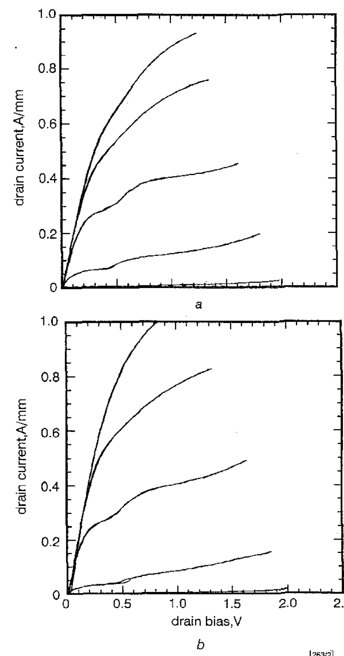

Fig. 2 *I-V characteristics of 0.1μm MODFETs based on structures A and B*

Gate bias for top curves = 0.6V; measurement step of gate bias = 0.2V
a Structure A
b Structure B

Device performance: Fig. 2 shows the excellent I-V characteristics of MODFETs, which exemplify their good pinchoff characteristics with an identical threshold voltage of –0.2V and a low knee voltage. Structure A shows a drain current I_{ds} of 0.9A/mm at gate bias V_{gs} of 0.6V and drain bias V_{ds} of 1V, and structure B exhibits an I_{ds} > 1A/mm under the same bias condition. The typical transfer characteristics for devices based on these two structures are shown in Fig. 3. At V_{ds} = 1, the maximum extrinsic transconductance of structure B is 1.7S/mm with an associated I_{ds} of 0.5A/mm. For structure A at the same bias, the peak transconductance is reduced to 1.5S/mm with a decreased I_{ds} of ~0.35A/mm. Therefore structure B exhibits a 10% improvement in transconductance compared with structure A. The device S-parameter characteristics were measured using a Cascade on-wafer probe station. Fig. 4 summarises the current gain $|h_{21}|^2$ and Mason unilateral power gain U_g against frequency at V_{ds} = 1 and with the V_{gs} for peak transconductance. The f_T and f_{max} obtained by extrapolating $|h_{21}|^2$ and U_g with –20dB/decade are 238 and 180GHz for structure B. This f_T value is 8% higher than that of structure A (f_T = 220GHz). As suggested by the calculation, the performance improvement should