Development of Multi-MHz Class-D Soft-Switching Inverters

by

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“Dedicated to my parents and my best friend, Fatemeh, for their unconditional love, patience, and support”

ABSTRACT

Wireless Power Transmission (WPT) systems are becoming rapidly mature and accessible to customers, and it is expected that they are going to take a large share of the electrical equipment market around the world in the near future. Many tech companies and university research labs have recently focused on design, development, and optimization of different blocks of these systems. WPT systems can be designed to transfer power either through electric fields or magnetic fields. Operating at the multi-MHz frequency will bring about the smaller size of the wireless link for both types of WPT systems.

The advent of Wide Bandgap (WBG) devices like Gallium Nitride (GaN) FETs and Silicon Carbide (SiC) MOSFETs has paved the road to design multi-MHz inverters and use them as the Radio Frequency (RF) power source in the transmitter of WPT systems. Designing an efficient inverter which can maintain its soft-switching performance while facing variable load or delivering variable output power is one of the major design challenges in this field. The second challenge in this area is related to the difficulties of Electromagnetic Compatibility (EMC) of the inverter, which is the direct result of operating at MHz switching frequency range. The Electromagnetic Interference (EMI) level can be reduced by designing a stronger filter or trying to remove the harmonics from the switching source.

In this thesis, to tackle the first challenge mentioned above regarding soft switching, the Dynamic Dead-Time Control (DDTC) approach is proposed and utilized to sustain the soft-switching of a multi-MHz Full-Bridge (FB) Class-D inverter over the full range of active load and output power. Simulation results are presented to show that dynamically controlling the Dead-Time (DT) during input DC voltage control and load variations,

reduces switch-node voltage overshoot, prevents large current spikes in the switching devices, and reduces associated high switching loss. Finally, experimental results obtained from the prototype of the system are provided to validate the effectiveness of the proposed approach.

Then, a soft-switching multi-MHz multi-level Class-D inverter is developed to address the second challenge of EMI issues associated with MHz switching frequency operation.The inverter is designed to eliminate the 3^{rd} and 5^{th} harmonics from its output voltage waveform. This will, in turn, make it possible to meet EMC and achieve the same level of harmonic attenuation on the output of the inverter with a smaller size and more efficient output EMI filter as opposed to utilizing a bulky, high-order, High-Quality (HQ) filter. The impact of DT on the modulation parameters of the multi-level inverter is investigated through mathematical analysis, and the results are utilized during the system simulations and practical implementation. A prototype is built to validate the theoretical and simulation analysis on a practical testbed. The harmonic analysis comparison carried out between the experimental results obtained from the multi-level inverter and FB Class-D inverter prototypes shows how the multi-level inverter is capable of suppressing unwanted 3^{rd} and 5^{th} harmonic to a much lower level which in turn leads to smaller size and more efficient output filter.

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List of Abbreviations

CSI	Common Source Inductance CSI
DT	Dead-Time
DDTC	Dynamic Dead-Time Control
eGaN	Enhancement-Mode GaN
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
GaN	Gallium Nitride
FB	Full-Bridge
HB	Half-Bridge
HQ	High-Quality
RF	Radio Frequency
SiC	Silicon Carbide
THD	Total Harmonic Distortion
WBG	Wide Bandgap
WPT	Wireless Power Transmission
ZVS	Zero Voltage Switching

CHAPTER 1

1 Introduction

1.1 Background

Power converters are one of the most important blocks of numerous electrical equipment. There has always been a high demand to increase the efficiency of power converters while reducing their size, which means raising their power density. A power inverter basically refers to any power electronic circuit that changes DC voltage to AC. Conventional power inverters have been mainly designed in tens or hundreds of KHz switching frequency and not much higher. Although higher switching frequency implies higher switching loss, the reduction in the size of power inductors as the direct result of higher switching frequency can increase the overall power density of the converter. The switching frequency of an inverter can be increased until the core of the inductor can tolerate the higher core loss

associated with the higher rate of the change in the magnetic flux. In other words, there is an optimal point for switching frequency of an inverter at which going beyond reduces adversely the power density. Considering the existing core material technology, the mainstream of the research and development in power converters, and commercially available products in the market, it can be said that the highest switching frequency of a power converter to achieve the highest power density cannot be higher than a few MHz. Inductor core technology should be mainly blamed for this problem, as it has not caught up yet with the rapid progress of switching devices. All existing materials which are used for building inductor cores experience very high core loss at frequencies higher than a few MHz.

Going back to the switching devices, silicon MOSFETs can operate at multi-MHz switching frequencies, but they undergo very high switching loss because of their relatively high input and output capacitance. The advent of Wide Bandgap (WBG) devices such as Gallium Nitride (GaN) FETs and Silicon Carbide (SiC) MOSFETs, however, has facilitated increasing the switching frequency to multi-MHz, while keeping the switching loss in the devices to an acceptable range. The main characteristics of these devices which have made them as powerful competitors to silicon MOSFETs at high-frequency applications are their much higher breakdown voltage, lower input and output capacitances, and lower drain-source on-resistance.

Considering the facts mentioned above about the current advancements and limitations of switching devices and inductor cores means that increasing the switching frequency of a power converter beyond a few MHz does not necessarily result in higher power density. As

a result, designing a power inverter at multi-MHz switching frequency can only be justified if there is an application that needs a switchmode multi-MHz power inverter. Non-efficient conventional active power amplifiers were traditionally the power source for applications that needed the power to be delivered in multi-MHz frequency. Nevertheless, there are now some applications in which the efficiency of the power source is extremely important. It can be said that Wireless Power Transmission (WPT) systems have changed the game in favor of multi-MHz switch-mode power inverters, as one of the most important features of a power transmission system is its overall high efficiency.

Conventional WPT systems can be divided into two main categories: capacitive and inductive coupled systems. Capacitive coupled systems use electric field to transfer power, as a result the mutual component between the transmitter and receiver electrodes is a capacitor. Inductive coupled systems, in contrast, use the magnetic field for power transmission; therefore, the mutual component between the electrodes is an inductor. Each system has its own strengths and weaknesses, meaning they should be selected based on the requirements and limitations of any particular application. In general, capacitive coupled WPT systems are lighter, more conformal from the physical shape point of view, and capable of operating at higher frequencies. The most important limitation of these systems, however, is the high sensitivity of the electrodes to the surrounding environment. Inductive coupled systems are generally heavier, less flexible in terms of the physical shape of the electrodes, and are operated at lower frequency due to the self-resonance of the inductive electrodes at high frequencies. The most important strengths of these systems, however, are their capability to operate in different environments and higher power levels.

1.2 Motivation

Designing a WPT system at multi-MHz as opposed to KHz switching frequency results in increasing power transfer distance, improving the misalignment range, and reducing the size of the resonators. A block diagram of a typical WPT system is presented in Figure 1-1.

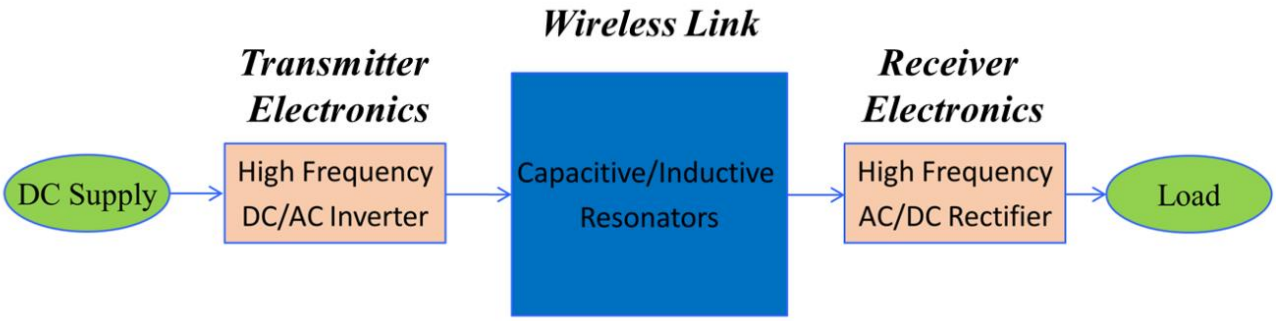

Figure 1-1: Typical wireless power system block diagram

Figure 1-1 shows that a typical wireless power system transfers power using either electric or magnetic fields through the wireless link or resonators. Using an efficient multi-MHz switch-mode inverter as the Radio Frequency (RF) power source in the transmitter electronics of a WPT system can considerably boost the overall efficiency of the entire system.

Different topics and areas can be explored while doing research in multi-MHz power inverters including but not limited to the converter topologies, soft-switching techniques, EMI and filtering, and switching devices.

Generally, Class-E and Class-D resonant inverters are the two types of topologies most referred to in the literature for multi-MHz switching frequency applications. The Class-E inverter with a ground-referenced switching device seems very practical to operate at multi-

MHz range because of its simple gate drive circuit and low Total Harmonic Distortion (THD). The classic Class-E inverter acts normally like an independent current source, making it desirable for certain types of applications. However, high drain voltage ringing and current stress and high dependency of the soft-switching performance on the switch-node capacitance, DC voltage fed to the inverter, and the load are the main disadvantages of this topology.

In contrast, the Class-D inverter has lower voltage and current stress (peak voltage across and maximum current through the device) and acts inherently like an independent voltage source, which makes it a suitable topology for certain types of applications. However, a complex gate drive circuit, a higher number of switching devices, sensitive soft-switching to the input DC voltage, and higher THD are the drawbacks of this topology.

Two main challenges in designing multi-MHz power inverters are maintaining soft-switching during output power control under different operating and loading conditions, on the one hand, and achieving an acceptable THD level on the output voltage on the other hand. An inverter design that overcomes these challenges can be used reliably as the power source in the transmitter electronics of a WPT system.

1.3 The focus of the Thesis

The two main challenges of designing a multi-MHz power inverter mentioned in Section 1.2 are addressed in this thesis by theoretical analysis, simulation, and experimentally developing two multi-MHZ power inverter topologies. The first inverter is a Zero Voltage Switching (ZVS) Full-Bridge (FB) Class-D inverter with controllable

output power. The input DC voltage fed to the inverter is the controllable parameter for output power regulation. Changing the input DC voltage while keeping the gate drive Dead-Time (DT) fixed forces the inverter to enter a partial ZVS operation. As a result, the first effort is to propose a control scheme called Dynamic Dead-Time Control (DDTC) that can maintain ZVS while regulating the output power.

Then, the challenge of the high THD level of the FB Class-D inverter is investigated by designing a multi-MHz Class-D based multi-level inverter. It is shown by mathematical analysis and simulation how a stepped waveform is capable of suppressing the level of the aggravating harmonics on the output voltage waveform. The experimental results obtained from the prototype built show the effectiveness of the approach.

1.4 Thesis Organization

The organization of this thesis is as follows:

Chapter 2 presents the literature review of WPT systems and different technologies being used for wireless power transfer. Different inverter topologies suitable for operating at multi-MHz frequency are discussed and pros and cons are mentioned. Different families of WBG devices are compared and a suitable switch is selected to be used in the simulation modeling and experimental implementation of the inverters.

Chapter 3 discusses the theory and formulations of the Class-D inverter with the ZVS tank, and simulation results are presented to describe the performance of the inverter.

Chapter 4 starts with an explanation of the different approaches for controlling the output power of a Class-D inverter. Then, the DDTC approach is proposed and experimentally

implemented on an inverter prototype built for this purpose. Experimental results are then presented to verify the assumptions, analysis, and simulation results provided earlier. Output voltage harmonic analysis concludes this chapter

Chapter 5 begins with the mathematical analysis of the stepped waveform with DT. Then, a Class-D multi-MHz multi-level inverter topology that can create the stepped waveform voltage on its output is discussed. After presenting simulation results of output power regulation with DDTC and output voltage harmonic analysis, hardware design for implementation of the system is proposed. The experimental results obtained are finally utilized to verify the capability of the proposed topology for soft switching and harmonic elimination.

Chapter 6 concludes the thesis, highlights the contribution of the research, and discusses future open research topics in this field.

CHAPTER 2

2 Review of the Literature

2.1 Wireless Power Transmission (WPT) Systems

Wireless Power Transmission or Transfer (WPT) systems are being developed at a much faster pace these days, making them mature enough to be integrated into electronic products in different industrial sectors such as telecommunication, automotive, medical, office interior, and aerospace. Several approaches have been proposed by researchers to transmit power wirelessly [1]; however, capacitive [2-8] and inductive resonant coupling [9-14] among all of the other approaches seem more attractive because they are less sensitive to displacement and misalignment of the transmitter and the receiver electrodes. These two techniques are compared in [15, 16], and the pros and cons of each method are highlighted. Inductive coupling is less sensitive to the environment and the medium that the power is

being transferred as it utilizes magnetic fields for power transfer. In contrast, capacitive coupling is very sensitive to the environment as the medium between the transmitter and receiver is the dielectric of the mutual capacitance between the transmitter and receiver. However, capacitive coupling can be implemented using much smaller resonators and at much higher operating frequency compared to the inductive coupling. F. Lu, et al. [17], studied an inductive and capacitive combined WPT system and experimentally verified the system to validate the idea of a hybrid arrangement. The hybrid systems provide more flexibility in terms of the environment that WPT systems can operate, yet the electronic design for both transmit and receive side are not that different than capacitive or inductive systems. The main drawback of resonant coupling systems is the requirement for relatively high operating frequency. Some works in this area have focused on the design and analysis of a WPT system at tens of KHz switching frequency and KW power range [18-24]. Considering existing technologies in inductor core materials, capacitor dielectric, and switching devices, this approach keeps the switching device and inductor core losses much lower and prevents challenges of operating near the self-resonant frequency of the passive components, which altogether brings about a cheaper solution. However, the bottleneck of KHz WPT systems is the relatively large size of the converters of the transmitter and receiver electronics and the wireless link. In recent years, the multi-MHz WPT applications have received a lot of attention, thanks to the progress in the switching device and drive circuit technologies [25, 26].

Increasing the switching frequency results in the higher cost of the design and components on one hand, but on the other hand, it lowers the overall size of the entire system. Operating

at multi-MHz switching frequency needs much more effort to deal with component parasitic elements and self-resonant frequency, as well as PCB design constraints at high frequencies. In [27-30], the effects of the component and PCB trace parasitics of a multi-MHz inverter are addressed, and optimized PCB layout and damping circuits are proposed to reduce the high-frequency ringing of the power loop.

In general, multi-MHz resonant coupled WPT systems can be divided into two categories in terms of resonators movements: stationary systems, and dynamically moving systems.

- Stationary wireless power systems can be divided into two groups:

I. The systems without power regulation on the transmission side and with or without impedance control on the receiver side. These types of systems present a broad range of resistive loads to the inverter from short circuit to the nominal resistive load, and from there to open circuit, depending on the power consumption on the receiver side.

II. The systems with power regulation on the transmission side and impedance control on the receiver side. These types of systems present a fixed resistive load to the inverter no matter the loading condition on the receiver side.

- Dynamically moving wireless power systems also can be divided into two main groups:

I. The systems with power regulation and dynamic matching networks on the transmission side, and impedance control on the receiver side. A proper design of the matching network can compensate impedance for an acceptable range of positions between the resonators and load variation on the receiver side. This will,

in turn, guarantee that the load presented to the inverter is almost always fixed and resistive.

II. The systems without matching network which can present a broad range of capacitive, resistive, and inductive loads to the inverter.

The work presented in this thesis can be used in both categories of stationary WPT systems and for the first category of dynamic WPT systems. There is currently no power inverter, to be used in the 2nd type of dynamically moving wireless link at the multi-MHz switching frequency, capable of handling active and reactive (capacitive and inductive) load at the nominal power and maintain soft switching. Using dynamic matching networks or other sorts of smart control is mandatory for this type of systems. Designing a matching network to compensate for the effects of wireless link displacement on the load presented to the transmitter is a very challenging subject that is investigated in the literature by some researchers [31-33]. Limited range of operation and high cost are among the major issues of the matching networks designed to operate in series with multi-MHz inverters in WPT systems.

2.2 Multi-MHz Power Inverters Applicable to WPT Systems

Conventional linear RF amplifiers like Class-A, Class-B, Class-AB, and Class-C are not suitable candidates for the power source on the transmitter side of a multi-MHz WPT system because of their low efficiency [34]. Instead, high-frequency switch-mode power converters can be appropriate replacements as their efficiency exceeds 90%. Class-E and Class-D inverters are the two most referenced topologies in the literature that can operate

at multi-MHz frequency. The higher efficiency of these power electronics modules is related to their soft-switching performance. In general, hard switching refers to switching a device while there is voltage across or current through the device. In contrast, either zero voltage or zero current during the state transition of the switch is enough to achieve soft-switching.

2.2.1 Class-E Power Inverter

Soft-switching Class-E inverters can be considered as the most efficient existing topology mainly because of their low number of switching devices [35, 36]. Generally, Class-E inverters provide less complexity in the design of the gate drive circuits by having only one switching device which is connected in such a way that the gate drive signal is referenced to the same ground of the entire circuit. The voltage ringing across the switching device, which is an almost half-sinusoidal waveform with low time derivatives on both turn-on and turn-off, also leads to low THD for this topology which is very important for Electro Magnetic Compatibility (EMC). However, high voltage and current stress on the switching device and large sensitivity of the soft-switching to the DC voltage and off-capacitance of the switching device are the main drawbacks of the Class-E inverters. This topology has been utilized several times in the design of multi-MHz WPT systems [37-40] as well as other applications [41]. A circuit diagram of a conventional Class-E inverter is presented in Figure 2-1.

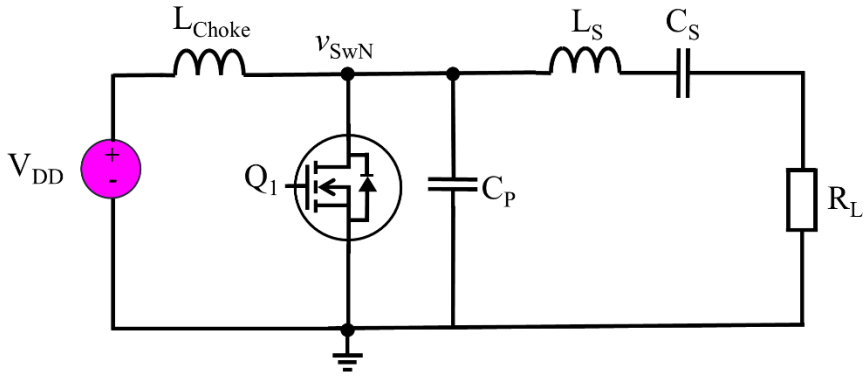

Figure 2-1: Circuit diagram of the classic Class-E inverter

Figure 2-1 shows a single-ended Class-E inverter that can practically operate at multi-MHz applications. The conventional Class-E inverter suffers from a high level of 2nd harmonic [42]. Proper tuning of the output filter along with choosing the right value for capacitance seen by switch node results in a full voltage ringing across the drain-source of the switch. This voltage ringing on the switch-node results in full soft-switching for the inverter. Waveforms of the gate signal and switch-node voltage of the inverter with full voltage ringing are shown in Figure 2-2.

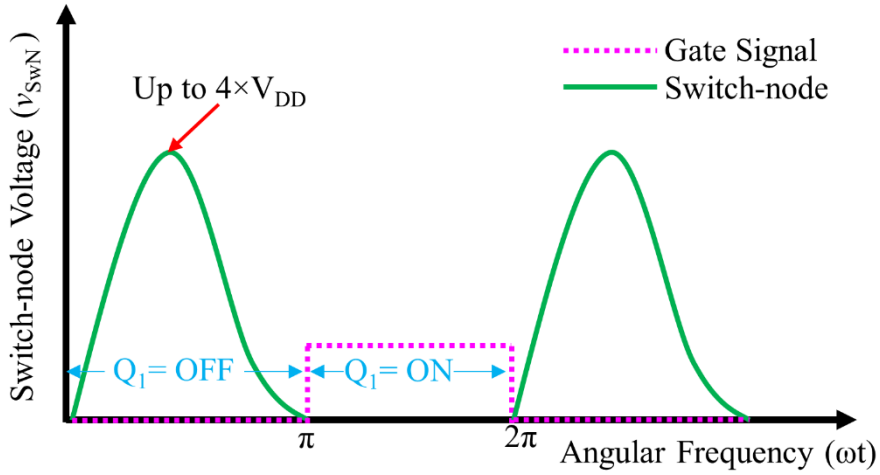

Figure 2-2: Class-E inverter gate-source and switch-node waveforms

Figure 2-2 shows one of the main drawbacks of the Class-E design which is its high drain-source voltage ringing reaching up to 4 times the input DC voltage. This means a high-voltage switch is required for a relatively low power inverter if Class-E topology is utilized. The conventional Class-E inverter acts like a current source, which means it can easily handle the nominal load and short circuit, but the open circuit can be detrimental [35]. New topologies are presented in [43-45] to convert a current source multi-MHz classic Class-E inverter to a voltage source or in other words making the inverter load independent. These new topologies can provide constant voltage to a resistive load, meaning that the inverter will not break down because of an open circuit. However, circulating current going through the added parallel inductor and the switch reduces the overall efficiency of the inverter.

Doubling the circuit presented in Figure 2-1 and adding a 180° phase shift between the gate signals applied to the switching devices results in a differential or push-pull Class-E topology. The first advantage of this extended topology is its higher power, but probably the more important one is providing a balanced output with eliminated 2^{nd} harmonic. Improving the efficiency of a push-pull Class-E inverter by adding a differential capacitor is explored in [46]. In [42, 47] new Class-E based inverter topologies are proposed to reduce the level of 2^{nd} harmonic on the switch node voltage, resulting in less voltage stress on the drain-source. Nevertheless, the soft-switching of these Class-E inverters are very sensitive to the off-capacitance seen by the drain of the switch and the current being injected to the switch-node, making tuning of the inverter very difficult. A detailed model of a Class-E inverter using the state-space technique is presented in [48] to achieve optimum switching operation.

2.2.2 Class-D Power Inverter

Hard-switching Class-D inverters suitable to operate in tens of KHz switching frequency are comprehensively discussed in [35]. A circuit diagram of a half-bridge Class-D inverter with output resonant filter and resistive load is shown in Figure 2-3.

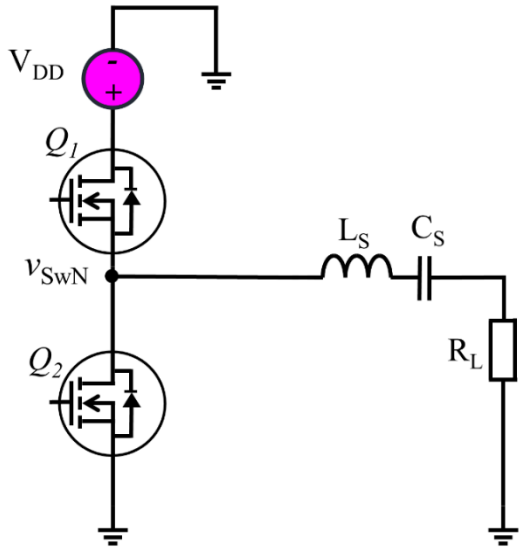

Figure 2-3: Circuit diagram of the Class-D half-bridge inverter

By applying non-overlapping gate signals with a 180° phase shift to Q_1 and Q_2, a square waveform is generated on the switch node. The gate signals and switch node voltage of this topology are presented in Figure 2-4.

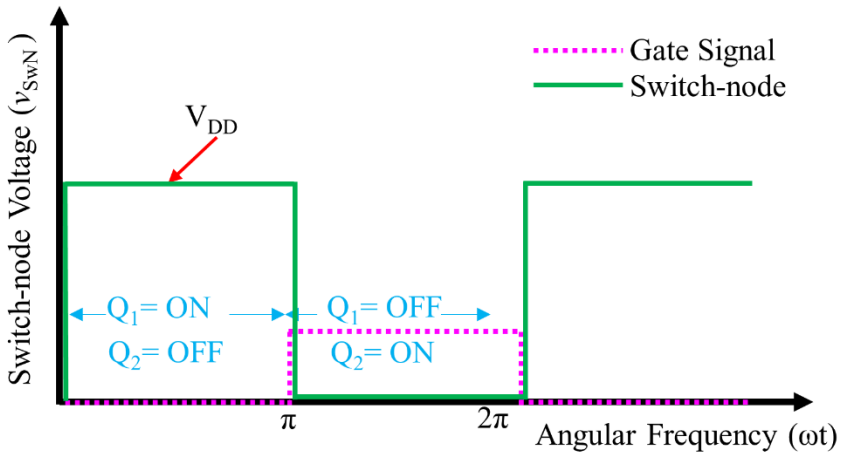

Figure 2-4: Class-D gate and switch-node waveforms

Using two half-bridge inverters in differential mode results in a full-bridge Class-D inverter which is presented in Figure 2-5.

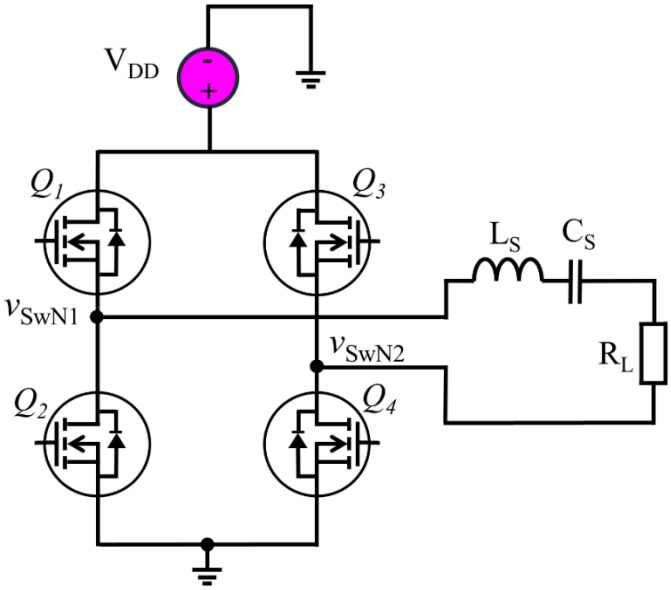

Figure 2-5: FB Class-D inverter

An analytical solution for Class-D inverter considering the switching transient time is presented in [49]. An improved Class-D inverter topology with an efficient snubber

network is proposed in [50] to address switching loss. In [51], the effect of non-idealities of a Class-D inverter operating at 500 KHz is explored. This topology operating at 200 KHz with an irregular driving pattern is the topic explored in [52]. The major constraint of these works is their relatively limited switching frequency which can not be increased to the MHz range.

The hard-switching Class-D inverter presented in Figure 2-3 cannot be used in MHz switching frequency and above due to the high switching loss. Soft-switching Class-D inverters operating up to 1 MHz switching frequency range are discussed in [53-56]. The Class-D soft-switching multi-MHz resonant inverter suitable to be used as RF source in the transmitter of WPT systems has recently been investigated in the literature [57-60]. An asymmetrical duty-cycle controlled soft-switching Class-D is analyzed in [61]. Steady-state analysis of this topology at any duty ratio and effect of the nonlinear parasitic capacitance of the switching device is also addressed in [62, 63].

The Class-D inverter, either half-bridge or full-bridge, operates at a much lower voltage and current stress on the switches compared to their Class-E counterparts. Robust soft-switching performance can also be achieved in Class-D easier than Class-E as it is less sensitive to the off-capacitance of the switching devices. Nevertheless, the Class-D topology needs a more complicated gate drive circuit, as the gate circuit of the top switch is referenced to the floating switch-node and not to the ground of the system. Improving the performance of the gate drive circuit of a Class-D topology in the MHz range is studied in [64-66]. Reverse recovery loss of the bootstrap diode used in the drive circuit of the top switch presents one of the major challenges in the design of Class-D inverters at multi-MHz

switching frequencies. A synchronous bootstrap technique to replace the diode with an eGaN FET with zero reverse recovery is presented in [67].

Class-D topology is extremely sensitive to the Common Source Inductance (CSI) of the power loop; therefore, the physical size of the loop on the PCB and parasitic inductance of the series switching devices have a significant impact on the performance of the inverter [68-74].

The THD of the output voltage of the Class-D topology is also higher than Class-E. This is basically related to the square waveform of the switch-node voltage which is rich in high-frequency harmonics due to the very fast rise and fall-time of the voltage. The output voltage of the Class-D inverter is naturally free of even harmonic, but the Class-E inverter suffers from the high amplitude of these harmonics. It is mentioned in Section 2.2.1 that 2^{nd} harmonic can be eliminated from the output voltage by using a differential Class-E topology. Figure 2-6 presents a harmonic level comparison between FB Class-D and Class-E push-pull inverters up to 200 MHz. The simulation is carried out with V_{DD} = 40 V and f_{sw} = 13.56 MHz.

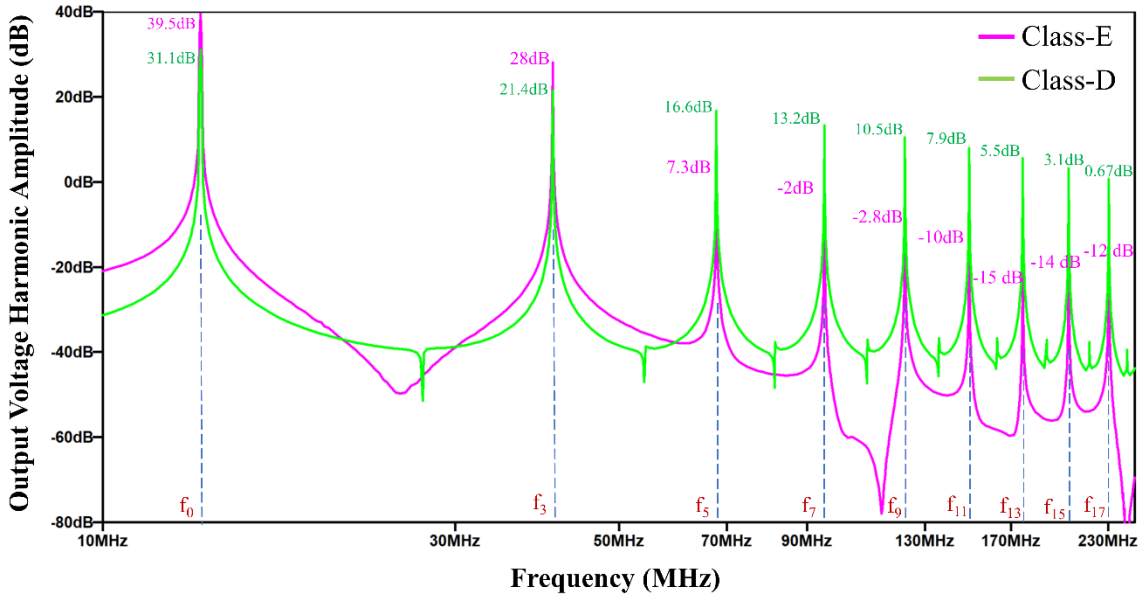

Figure 2-6: FB Class-D and Class-E push-pull output voltage harmonic analysis

Figure 2-6 shows that the differential Class-E inverter has lower harmonics level compared to the FB Class-D inverter. Using the basic definition of THD presented in Equation 2-1 [35], the THD of Class-D and Class-E inverters can be calculated as 42.1% and 26.5%, respectively.

$$THD = \sqrt{\frac{V_{R2rms}^2 + V_{R3rms}^2 + V_{R4rms}^2 + \cdots}{V_{R1rms}^2}} \qquad 2\text{-}1$$

The THD levels mentioned above imply that a lower Q output filter is needed for Class-E compared to Class-D topology to achieve the same suppression level on the high-frequency harmonics of the output voltage.

Soft-switching performance of both Class-D and Class-E inverters is sensitive to the amplitude and phase of the load attached to the output. WPT systems with or without

impedance matching network might present different loading conditions (active or reactive) to the power inverter because of relative movement of the resonators or change in the power consumption in the receiver side, as explained in Section 2.1. Load independent power inverters [43, 44, 47] can handle a broad range of resistive load, but they are vulnerable to reactive load. In [75-78], attempts are made to design an inverter that can compensate for a large range of resistive, capacitive and inductive loads. The main idea here is to use two parallel inverters that share a load through a capacitive and inductive link and control phase shift between the inverters and individual DC voltages applied to the inverters so that the impedance presented to the inverters remains resistive all the time. The main challenges for this approach are real-time load detection and closed-loop control stability.

Considering all the pros and cons of the two topologies explained in Section 2.2, the Class-D topology is selected in the first step because of its lower voltage and current stress on the switches and easier soft-switching tuning. Also, Class-D topology can be extended to a multi-level inverter to achieve a lower harmonic level on the output voltage waveform which finally results in improved EMC [79]. This development is investigated in the second step in this research.

2.3 Wide-Bandgap Devices Suitable for Multi-MHz Switching Frequency

Until recently, one of the biggest challenges in the design of multi-MHz inverters had been finding switching devices capable of operating efficiently in this range of frequency. Large input-output capacitances, slow rise and fall times, and package parasitic inductance associated with silicon MOSFETs limit their operating frequency to few MHz. WBG devices, however, have made it easier to design high-frequency high-power inverters,

thanks to their much higher breakdown voltage, lower input and output capacitances, and lower drain-source on-resistance [68-80]. Two main families of WBG devices, GaN FETs and SiC MOSFETs, are compared in [81].

The package design of Enhancement-Mode GaN (eGaN) FETs, including the size, shape, and terminal directions significantly reduces the parasitic inductance of the device [70]. The lower input and output capacitance of eGaN FETs result in lower current demand for turning on and off, hence faster rise and fall time. One of the most important targets in the design of an inverter is to achieve high efficiency. Conduction loss due to the on-resistance of a switching device can be considerably reduced by driving the device with higher gate-source voltage, as the on-resistance is inversely proportional to this voltage. The maximum gate-source voltage of eGaN FETs is 5 V whereas it is 15 V for MOSFETs, which means less complexity in the gate drive circuit of eGaN FETs.

SiC MOSFETs have higher on-resistance stability at a higher temperature and higher breakdown voltage compared to eGaN FETs. The thermal conductivity of SiC MOSFETs is better than eGaN FETs and MOSFETs, resulting in more effective heat transfer from the switching device to PCB and heatsink, and eventually higher power density of the converter. The maximum gate-source voltage of SiC MOSFETs is also 15 V, implying a more difficult drive circuit [68, 69]. The input and output capacitance and package parasitic inductance of SiC MOSFETs are also higher than eGaN FETs. Modeling and dynamic characterization of WBG devices is studied in [82-84].

By taking into account the characteristics of WBG devices explained in this section, eGaN FET is an ideal candidate to be used in the design of both inverter topologies throughout

this research mainly because it has the lowest package intrinsic inductance compared to the other switch families.

CHAPTER 3

3 Multi-MHz Full-Bridge Class-D Inverter with Soft-Switching

3.1 Introduction

This chapter starts with an explanation of the circuit and operation of a Full-Bridge (FB) Class-D inverter. A switch with appropriate electrical characteristics is then selected to enable operating the inverter at 13.56 MHz switching frequency. The circuit diagram, theoretical analysis, and different modes of operation of a soft-switching FB Class-D inverter are then discussed, and the effects of power regulation with input DC voltage and load variations on the soft-switching are examined through simulations.

3.2 FB Class-D Power Inverter

The FB Class-D power inverter, which consists of two half-bridge inverters operating in differential mode, along with the series resonant filter and the load is presented in Figure 3-1.

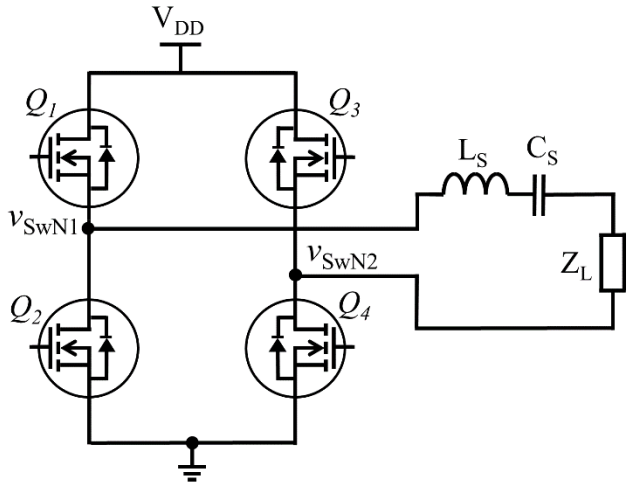

Figure 3-1: FB Class-D inverter with series resonant filter and load

Non-overlapping switching of Q_1-Q_4 and Q_2-Q_3 with 50% duty cycle less the dead-time (DT), provides almost a full square waveform between Switch-Node 1 (SwN_1) and Switch-Node 2 (SwN_2). The DT is a short period of time compared to the switching cycle in which both series switches (Q_1-Q_2 or Q_3-Q_4) are OFF to avoid half-bridge shoot-through. Neglecting the effect of DT on the differential output waveform and using Fourier series theory, the differential voltage (v_{Sw}) delivered to the output filter can be expressed as follows [35]:

$$v_{Sw} = v_{SwN1} - v_{SwN2} = \frac{4V_{DD}}{\pi} \sum_{n=1}^{\infty} \frac{1-(-1)^n}{2n} sin(n\omega t) \qquad \textbf{3-1}$$

3.3 Selecting the Switching Device

From the point of view of miniaturization and high power density, selecting a device with the appropriate voltage and current ratings which is capable of operating in a Class-D configuration and at multi-MHz switching frequency is a design challenge, and the following points should be considered in the selection of the device.

3.3.1 Source and Sink Current of Gate Drivers

The maximum source and sink current of commercially available bridge gate drivers in the market in the multi-MHz range are 1.2 A and 5 A, respectively (e.g. LM1205). These values determine the rise and fall times of the gate signal which are important in the performance of the inverter. Rise-time determines the maximum operating frequency of the inverter and fall-time governs the turn-off loss of the switch. Assuming 1 nsec to be the target for the rise-time and maximum 1.2 A constant current being sourced from the gate driver means the total charge that can be delivered to the gate cannot go higher than 1200 pC. From the gate voltage perspective, Silicon MOSFETs can operate with gate voltage ranging from 5 V to 15 V. However, they are better to be driven with the higher voltage to achieve higher channel enhancement and lower drain-source resistance ($R_{DS\text{-}ON}$). This situation is the same for SiC MOSFETs among WBG devices. However, assuming a fixed total charge required to be delivered from the driver to the switch for turning on, higher gate voltage would imply smaller gate capacitance that can be supported by the driver. As a result, eGaN FETs are better candidates for multi-MHz Class-D inverters because of their smaller input capacitance and lower maximum gate voltage (6V) associated with the lowest $R_{DS\text{-}ON}$. Table

3-1 provides an electrical characteristic comparison between samples of a Silicon MOSFET, a SiC MOSFET, and two eGaN FETs which can operate in multi-MHz switching frequency.

Table 3-1: Electrical characteristic comparison between different switching devices

	Vendor	**V_{DS} (V)**	**Drain Current (A)**	**R_{DS-ON} (mΩ)**	**Total Gate Charge (nC)**	**Input Capacitance (pF)**	**Output Capacitance (pF)**	**Dimension (mm × mm × mm)**
EPC8009 (eGaN FET)	EPC	65	4	130	0.37	45	19	2.05 × 0.85 × 0.68
GS66504B (eGaN FET)	GaN Systems	650	15	100	3.0	130	33	5.0 × 6.5 ×0.51
C3M0120090J (SiC MOSFET)	CREE	900	22	120	17.3	350	40	16.9 × 10.4 × 4.3
FDMC86116LZ (Si MOSFET)	Fairchild	100	7.5	103	4.0	232	45	3.3 × 3.3 × 0.8

Assuming a FB Class-D inverter with a maximum 45V input DC voltage and operating below 50W output power, the data provided in Table 3-1 shows that EPC8009 has the optimum electrical characteristics to be used in the inverter to operate at multi-MHz frequency.

3.3.2 Intrinsic Inductance of the Switch

The intrinsic inductance of the switch is mainly dictated by the physical size of the device. The intrinsic inductance of the switches and the power loop on the PCB determine the total Common Source Inductance (CSI), which in turn governs the maximum switch-node voltage overshoot. According to Table 3-1, eGaN FETs designed and developed by EPC have the smallest physical size and hence lowest package inductance, among all other counterparts. The package size and the shape and direction of terminals on EPC 8009 are designed to reduce the parasitic inductance of the component, considerably.

3.4 Soft-Switching in Class-D Inverters

High efficiency can only be achieved in a switching power inverter with a proper soft-switching technique. As the switching frequency increases, the soft-switching becomes even more important to attain high efficiency. One of the approaches referred to in the literature for ZVS in Class-D inverter with a series resonant filter utilizes a shunt capacitor along with inductive tuning of the resonant filter [56]. While this approach is very useful for applications in the KHz switching frequency range, it cannot be utilized at multi-MHz switching frequency as the duty cycle and, consequently, the associated dead time (DT) – the interval during which all the switches are OFF - is not long enough for the switching device off-capacitance and the shunt capacitor to be charged and discharged. Therefore, in the next section, a soft-switching circuit which is suitable to operate at multi-MHz switching frequency is investigated in detail.

3.4.1 Description and Operation of Parallel LC ZVS Circuit

M. d. Rooij [67] proposed a passive LC ZVS tank for a FB Class-D inverter operating in multi-MHz switching frequency. The LC circuit proposed provides a smooth drain-source voltage transition during switching cycles. The FB Class-D power inverter with the soft-switching circuit is shown in Figure 3-2.

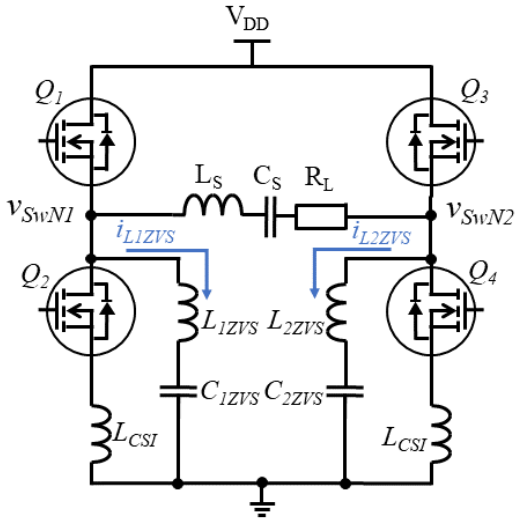

Figure 3-2: FB Class-D inverter with ZVS LC tank (L_{ZVS} and C_{ZVS})

The LC tank, shown in Figure 3-2, is designed so that its resonant frequency is much lower than the switching frequency of the inverter. This presents a purely inductive load to the switch-node at the actual switching frequency. As a result, the ZVS inductor charges and discharges linearly while the top or bottom switches are ON, respectively. At high switching frequencies, the inductor current during DT is approximately constant, providing enough current to achieve soft-switching, which eventually results in higher efficiency.

The ZVS capacitors, C_{1ZVS} and C_{2ZVS}, charge up to $V_{DD}/2$ which is the DC voltage offset on both switch-node voltage waveforms. All the switches are OFF during the DT interval,

and the off-capacitance voltages of the eGaN FETs swap almost linearly between 0 and V_{DD}, depending on the switch state before the commencement of the DT. Otherwise stated, if a switch is OFF before the DT, the output capacitance discharges during the DT and if a switch is ON before, the output capacitance charges. The sinking or sourcing current needed for the charging and discharging of the off-capacitances is provided by the ZVS inductor (L_{1ZVS}). Four operation modes of the left half-bridge inverter are presented in Figure 3-3 during one switching cycle.

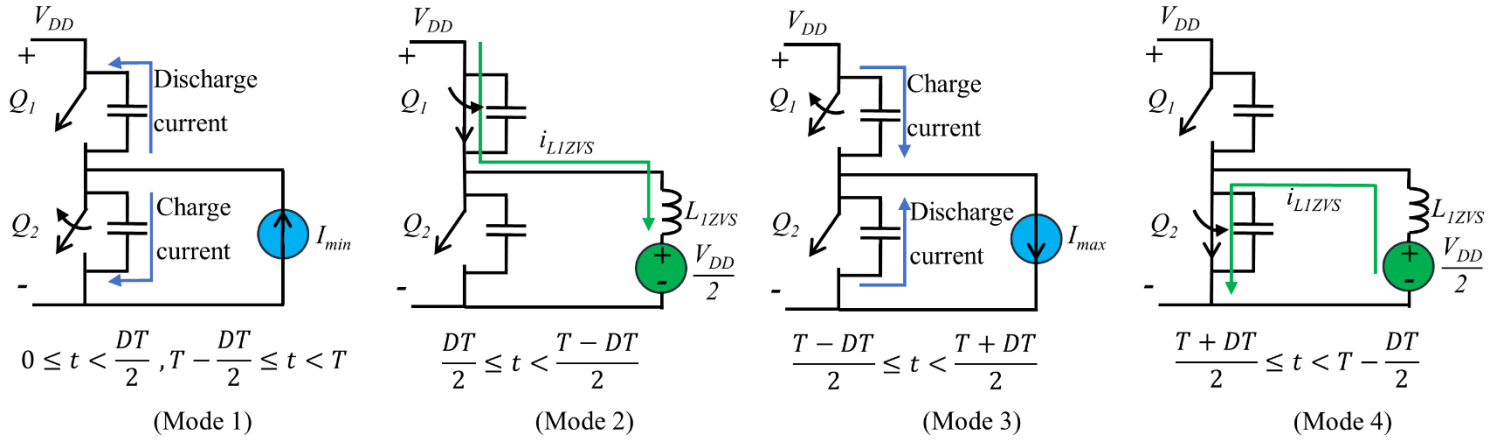

Figure 3-3: Operation modes of the half-bridge inverter with ZVS tank

Mode 1 and Mode 3 represent the DT interval, and Mode 2 and Mode 4 refer to the two intervals during which Q_1 is ON and Q_2 is OFF, and Q_2 is ON and Q_1 is OFF, respectively. The ZVS inductor L_{1ZVS} absorbs magnetic energy during the switching cycles in different directions and releases the energy during the DT interval.

3.4.2 Theoretical analysis of the ZVS inductor current

Equation 3-2 defines the current passing through both ZVS inductors during one switching cycle.

$$i_{LZVS}(t) = \begin{cases} I_{min} & 0 \le t < \frac{DT}{2}\ ,T - \frac{DT}{2} \le t < T \\ \frac{V_{DD}}{2 * L_{ZVS}}\left(t - \frac{DT}{2}\right) + I_{min} & \frac{DT}{2} \le t < \frac{T - DT}{2} \\ I_{max} & \frac{T - DT}{2} \le t < \frac{T + DT}{2} \\ -\frac{V_{DD}}{2 * L_{ZVS}}\left(t - \frac{T + DT}{2}\right) + I_{max} & \frac{T + DT}{2} \le t < T - \frac{DT}{2} \end{cases} \quad \text{3-2}$$

The minimum and maximum values of the ZVS inductor current can be expressed as

$$\begin{cases} I_{min} = -\frac{V_{DD}}{4 * L_{ZVS}}\left(\frac{T}{2} - DT\right) \\ I_{max} = +\frac{V_{DD}}{4 * L_{ZVS}}\left(\frac{T}{2} - DT\right) \end{cases} \quad \text{3-3}$$

Where T is the switching period and DT is the dead-time interval. The ZVS inductor current alternates linearly between the minimum and maximum values shown in Equation 3-3 when either of the switches on each half-bridge inverter is ON and can be assumed with high accuracy to remain nearly constant during the DT. In other words, the ringing of the inductor current with the off-capacitance voltages of both series switches during DT is ignored assuming a large enough inductor current and adequately short DT. Equation 3-3 implies that (a) the maximum and minimum current of the ZVS inductors depend directly on V_{DD} and inversely on L_{ZVS}, and (b) lower peak-to-peak inductor current swing can be achieved by higher DT.

The Class-D inverter topology is very sensitive to CSI of the power loop due to the resonance between the off-capacitance of the switches and CSI. This ringing can create a large voltage overshoot on the switch nodes during each voltage transition. CSI can be reduced considerably by selecting a switching device with smaller package size and parasitic inductance as previously discussed. The EPC8009 eGaN FET has very low input and output capacitances, making it suitable for switching at 13.56 MHz. Its smallest package size compared to its counterparts, results in extremely low parasitic inductance and it meets the acceptable voltage and current ratings for the power level needed for this design. The effect of CSI on the switching performance is addressed by adding L_{CSI} to the simulation circuit in the next section.

It is worth noting that the output capacitance of EPC8009 decreases almost linearly from 45 pF to 15 pF during which the drain-source voltage increases from 0V to 45V [70]. Thus, at higher voltages across the eGaN FETs, lower sinking or sourcing inductor current is required for charging and discharging the off-capacitance of the switches to maintain soft-switching. Assuming almost constant ZVS inductor current during DT and by considering Equations 3-2 and 3-3, the only parameter that can be used to control the inductor current during output power regulation while maintaining soft-switching is the DT.

3.5 Soft-Switching Analysis with Simulation

The input DC voltage of the inverter can be a control parameter for output RF power regulation. The effects of this parameter variation on the soft-switching of the inverter are analyzed and simulated in Section 3.5.1. In the next sub-section, inductive and capacitive

loads are presented to the inverter to evaluate the effects of reactive loads on the soft-switching performance of the Class-D inverter.

3.5.1 Soft-Switching and DC Voltage Variations

In this section, the inverter topology presented in Figure 3-2 is simulated in LTSpice, using EPC8009 SPICE model created by EPC. Table 3-2 presents the circuit parameters deployed in the simulation.

Table 3-2: Simulation parameters of the ZVS FB Class-D inverter in LTSpice

Parameter	Value	Description
f_{sw}	13.56 MHz	Switching frequency
f_0	13.56 MHz	Filter resonant frequency
L_S	1 µH	Series resonant inductor
C_S	137 pF	Series resonant capacitor
R_L	25 Ω	Output Load
V_{DD}	7.5 V - 45 V	DC Voltage
Q_L	3.4	Loaded quality factor
L_{1ZVS} & L_{2ZVS}	300 nH	ZVS inductors
C_{1ZVS} & C_{2ZVS}	1 µF	ZVS capacitors
L_{CSI}	0.2 nH	Common Source Inductance
DT	4-7 ns	Dead-Time range
T_{SMax}	1 ps	The maximum simulation time step

The v_{SwN1} waveform and the corresponding ZVS inductor current i_{L1ZVS} at V_{DD} =45V are shown in Figure 3-4 based on the four operation modes presented in Figure 3-3.

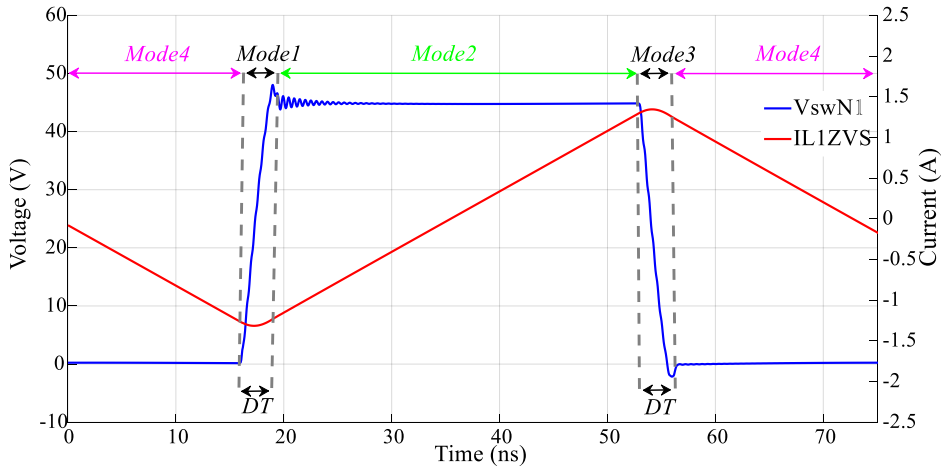

Figure 3-4: v_{SwN1} and i_{L1ZVS} waveforms

Due to the directly proportional dependency of the amplitude of the differential output voltage of the inverter on the input DC voltage, V_{DD} is the control parameter used here for output RF power regulation. A 0.2 nH inductor is added to each inverter channel to model CSI (L_{CSI}) which practically exists in the implementation of the inverter due to the parasitic inductance of the switching device package and PCB routing [85]. By taking into account the charge and discharge transitions of the off-capacitance presented in Figure 3-4 during DT period, an equation for DT can be calculated as follows:

$$DT = (2C_{off})\frac{V_{DD}}{I_{max}} \qquad 3\text{-}4$$

In Equation 3-4, C_{off} is the off-capacitance of the eGaN FET. Using Equation 3-4 and the nonlinear off-capacitance versus drain-source voltage characteristic of the eGaN FET [70], an optimal value is calculated for DT at each V_{DD} level to maintain ZVS while V_{DD} is varied. The range of DT utilized throughout the simulations is 4–7 ns. Variable DT is

carried out in the simulation while the input DC voltage is linearly regulated from 45V to 7.5V. The simulation results are shown in Figure 3-5 to Figure 3-9.

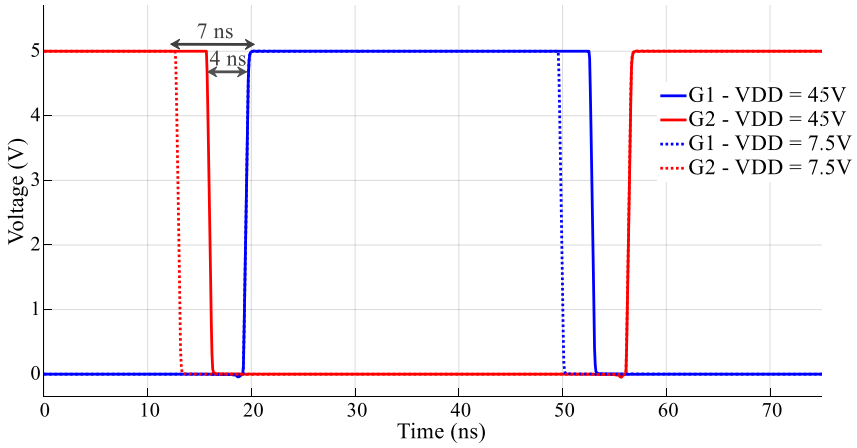

Figure 3-5: G_1 and G_2 gate signals at V_{DD} = 7.5V and 45V

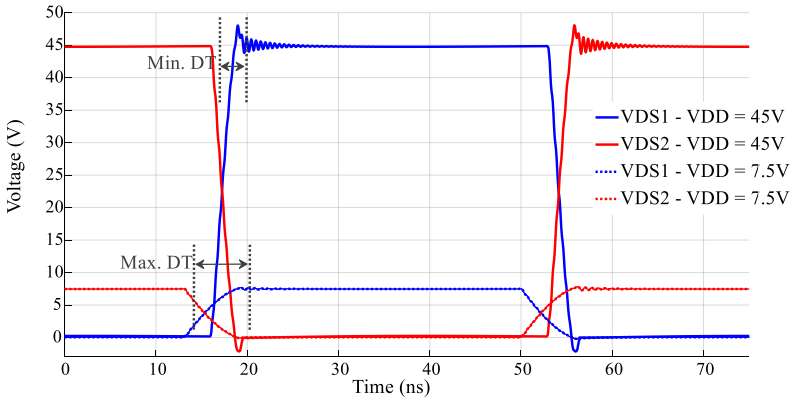

Figure 3-6: Q_1 and Q_2 drain-source voltage at V_{DD} = 7.5V and 45V

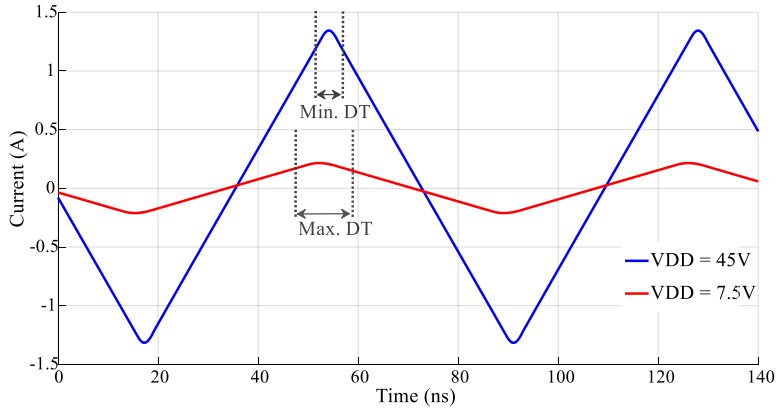

Figure 3-7: L_{1ZVS} current at V_{DD} = 7.5V and 45V

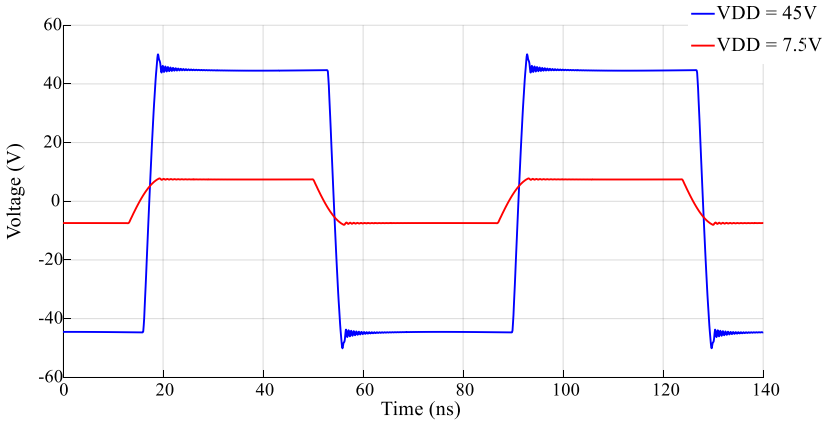

Figure 3-8: Switch-node differential voltage (v_{Sw}) at V_{DD} = 7.5V and 45V

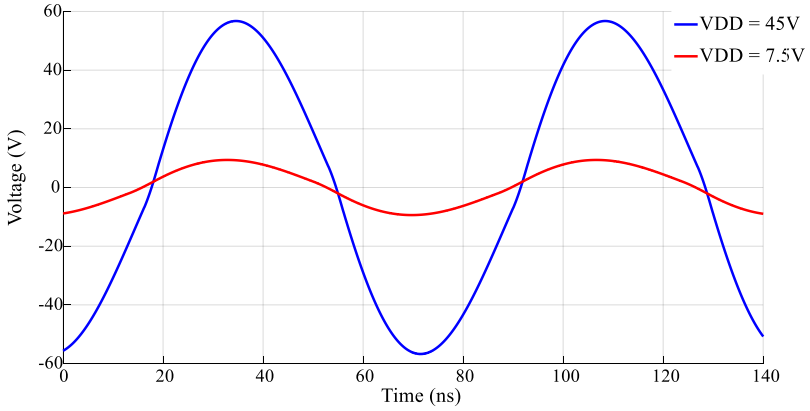

Figure 3-9: Load voltage at V_{DD} = 7.5V and 45V

Figure 3-5 presents the minimum and maximum DT required for the highest and the lowest level of V_{DD}, respectively. The Q_1 and Q_2 drain-source voltage at V_{DD} = 7.5V and 45V with maximum and minimum DT are shown in Figure 3-6. It can be seen in this figure that enough time is provided for the off-capacitances of eGaN FETs to charge and discharge linearly by controlling DT. The ZVS inductor current of the left half-bridge inverter at the minimum and maximum DC voltage and the maximum and minimum DT is presented in Figure 3-7. The differential switch-node and load voltages during input DC voltage regulation are also demonstrated in Figure 3-7 and Figure 3-8.

In this section, it is assumed that the inverter starts operating at V_{DD} = 45V; then, V_{DD} is reduced to 25V. The switch-node 1 voltage (v_{SwN1}) and Q_1 drain-source current at V_{DD} = 25V at fixed DT and DDTC are compared in Figure 3-10 and Figure 3-11.

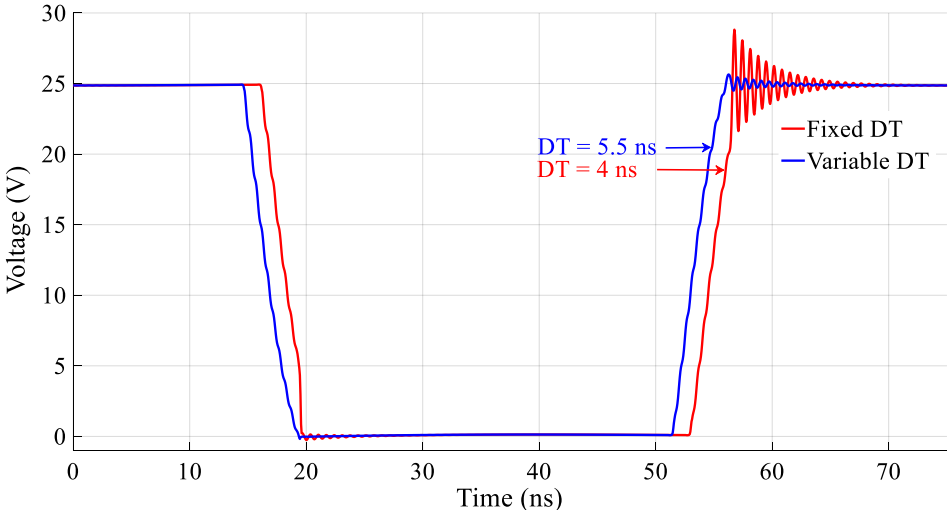

Figure 3-10: v_{SwN1} at V_{DD} = 25V with fixed DT and DDTC

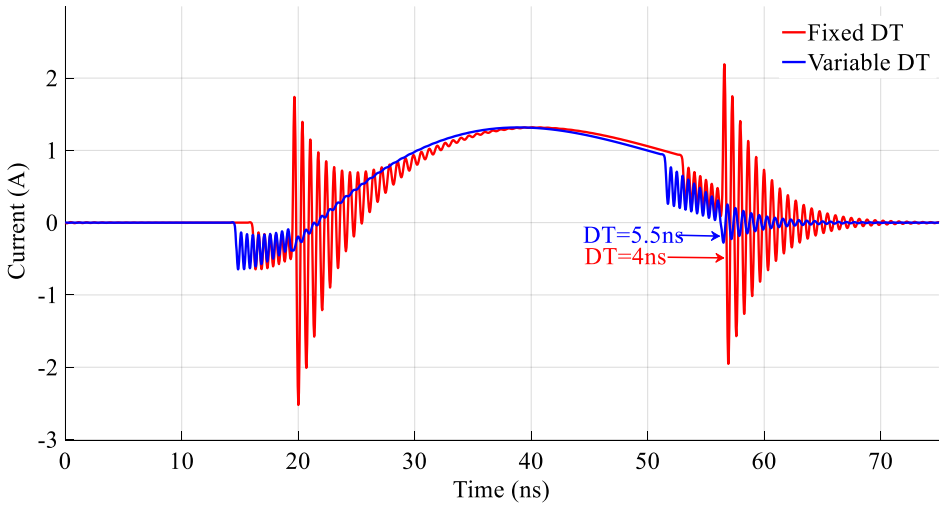

Figure 3-11: Q_1 drain-source current at V_{DD} = 25V with fixed and variable DT

Figure 3-10 indicates that fixed DT results in a large voltage overshoot on v_{SwN1} when the DC voltage is dropped from 45V to 25V. The large ringing in the voltage waveform is minimized when variable DT is used by increasing DT from 4 ns to 5.5 ns. Figure 3-11 indicates that early switching, due to the fixed DT, leads to large current spikes and consequently large instantaneous power loss on the switch, which are associated with the fast discharge of the off-capacitance of the switching device. Figure 3-12 demonstrates how DT is adjusted in the simulation to sustain soft-switching while V_{DD} is controlled.

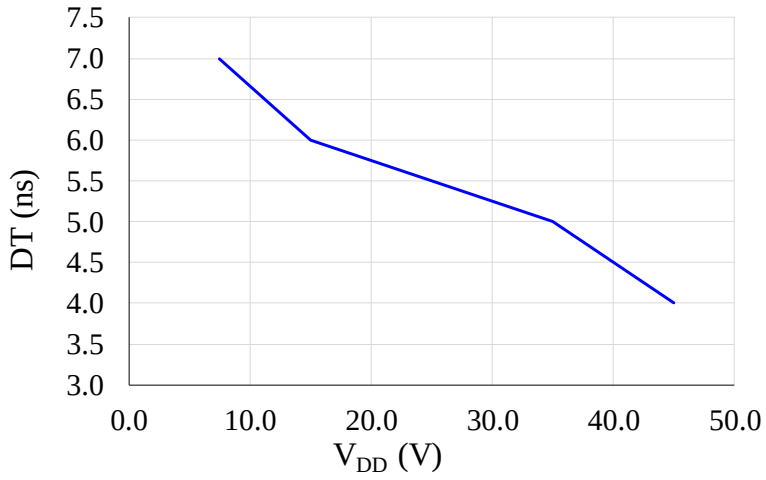

Figure 3-12: The range of DT for soft-switching vs. V_{DD}

Figure 3-13 and Figure 3-14 present the overshoot on v_{SwN1} and the ratio of the Q_1 drain-source peak current over the inverter RMS load current (i_{DS-Max}/i_{L-rms}) under fixed and variable DT at different V_{DD} levels. These comparisons can be used to evaluate the soft-switching performance of the inverter.

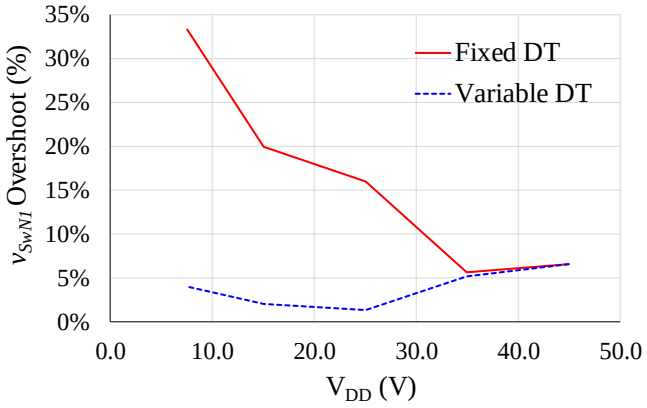

Figure 3-13: Switch-node 1 voltage (v_{SwN1}) overshoot at different V_{DD} levels

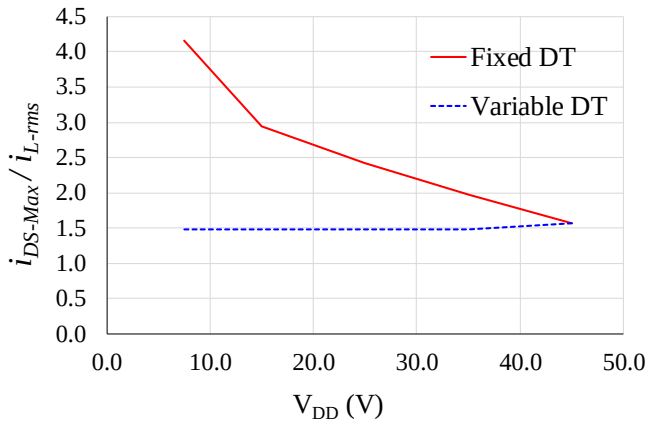

Figure 3-14: Q_1 drain-source peak current over the RMS load current (i_{DS-Max}/i_{L-rms})

Figure 3-13 and Figure 3-14 show that dynamically varying the DT can prevent large voltage overshoot on the switch-node while limiting the drain-source current spike during switching transitions. The large current spikes shown in Figure 3-14 results in lower efficiency and higher steady-state temperature, which can lead to permanent failure of the eGaN FETs unless larger heatsink is utilized for improved heat transfer.

3.5.2 Reactive load effect on Soft-Switching

The simulations presented in Section 3.5.1 were carried out under a fixed resistive load and variable DC voltage. In this section, the effect of capacitive or inductive load on the soft-switching is simulated. It is explained in Section 3.4 that the ZVS tank is designed with a resonant frequency much lower than the switching frequency (e.g. a couple of hundred KHz). As a result, the ZVS tank is presented as a purely inductive load to the switch node at the switching frequency, and the capacitor acts like a short circuit. As a result, any inductive load presented to the switch node results in a more lagging sinusoidal current

being drawn from or injected to the switch-node in every cycle. In other words, an inductive load can intensify the minimum or maximum ZVS inductor current seen by the switch-node (Equation 3-3). In contrast, a capacitive load draws a leading current from the switch node which reduces the maximum and minimum values of the ZVS inductor current. The effects of capacitive and inductive loads on the switch-node waveform at V_{DD} = 45 V are shown in Figure 3-15.

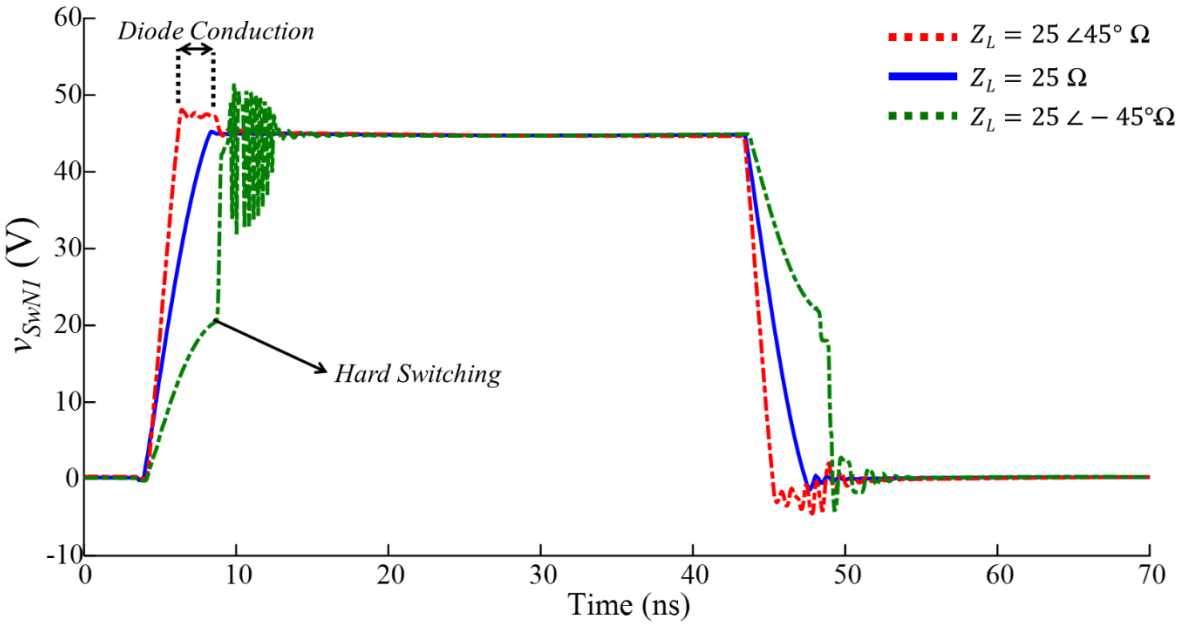

Figure 3-15: Switch-node 1 voltage (V_{SwN1}) under different loading conditions

In Figure 3-15, the blue, red, and green waveforms correspond to resistive, inductive, and capacitive loads, respectively. As it is expected for a tuned inverter with the ZVS tank, complete soft-switching occurs for the resistive load. The inductive load intensifies the lagging current drawn from the switch-node; as a result, the off-capacitances of the switches are charged and discharged rapidly, leading to anti-parallel diode conduction. The

leading capacitive load current cancels the lagging ZVS tank inductive current injected into the switch-node; thus, the inverter enters a hard-switching mode. The destructive effect of this type of load on the soft-switching of the Class-D inverter can be seen on the green waveform.

3.6 Summary

This chapter starts with a brief discussion of the basic operation of the FB Class-D inverter and formulations. Selecting a switching device for operating in a multi-MHz switching range is then discussed by comparing different available switch technologies from different vendors and from their electrical characteristic perspective. Theoretical analysis of a passive LC ZVS tank, modes of operation, and necessary formulation of a ZVS FB Class-D inverter are then presented. Simulation results and necessary formulations are presented to provide an insight into the effect of DT variation on the soft-switching. These results show how varying DT during input DC voltage variation can prevent large current spikes and associated high switching loss on the switches during output power regulation. The effects of capacitive or inductive load on the soft-switching of the inverter are finally examined through simulation. It is shown that the ZVS tank operates properly, resulting in complete soft-switching when the load is resistive; the off-capacitance charge and discharge quicker, leading to anti-parallel diode conduction when the load is inductive; and the ZVS tank become almost ineffective due to the leading current injected to the switch-node by the capacitive load, resulting in hard-switching.

CHAPTER 4

4 Full-Bridge Class-D Inverter with Dynamic Dead-Time Control

4.1 Introduction

In this chapter, different control methods for regulating the output RF power of a FB Class-D inverter are reviewed, firstly. Then, a hardware block diagram for the implementation of a soft-switching Class-D inverter with input DC voltage control is presented. The goal of this Chapter is to demonstrate that the soft-switching of a FB Class-D inverter can be sustained at 13.56 MHz switching frequency using Dynamic Dead-Time Control (DDTC) approach during output power regulation by input DC voltage variation. A prototype converter is developed and experimental results from the prototype converter are provided

in the last section to validate the effectiveness of the proposed approach and the improved performance from the point of view of the converter efficiency and temperature.

4.2 Different Methods for Output Power Control

Different approaches have been investigated in the literature to control the output power of a Class-D inverter [86-88]. As explained in Section 3.2, a Class-D inverter acts naturally like an ideal voltage source. As a result, the first and easiest way to control the output power is by changing the value of the load presented to the inverter. In other words, if the system can be designed in such a way that the load value varies from nominal load to open circuit, it is guaranteed naturally that the power can be regulated from maximum to zero by load modulation. However, this is not the practical scenario for many applications, and the inverter needs to be able to regulate the power no matter the load presented to the inverter. The second method for controlling the output voltage of a Class-D inverter is to change the switching frequency. As the output filter of this inverter is a High-Quality (HQ) resonant filter, by moving the switching frequency from the resonant frequency of the filter the output power will drop. Output power regulation using frequency modulation for an inverter operating at 13.56 MHz switching frequency, V_{DD} = 45V, series filter loaded quality factor of Q_L=3.4, and a differential load of R_L=25Ω is presented in Figure 4-1.

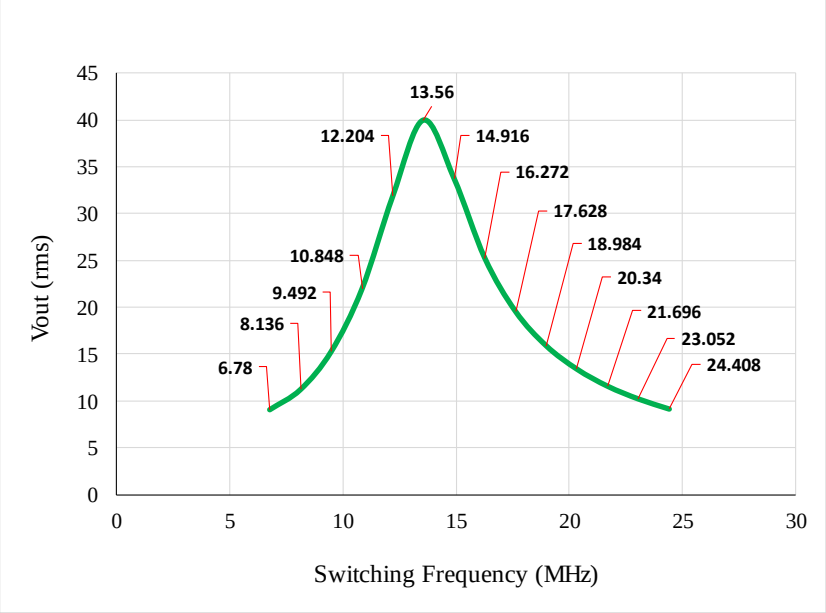

Figure 4-1: Class-D inverter output voltage regulation with switching frequency modulation, 13.56 MHz center frequency

Figure 4-1 shows that the output voltage amplitude can be regulated in a broad range by changing the switching frequency from 0.5 f_0 to 1.5 f_0, where f_0, the center frequency is 13.56 MHz. The main issue with this control method is EMI, as the range of frequency change is very wide which makes it extremely difficult to meet EMC. In general, it is more convenient to design the EMI filter for a system at a fixed operating frequency, as this will provide fixed criteria for the cut-off frequency of the input and output filters. In contrast, designing an EMI filter for a variable frequency system will impose more challenges as the filter needs to have enough attenuation over a much broader frequency range. Frequency control also changes the load at the switch node from resistive at the center frequency to capacitive (when the switching frequency is below the center frequency) or inductive (when the switching frequency is above the center frequency). As noted in Chapter 3, this has a detrimental effect on the ZVS operation of the inverter.

The third approach for output voltage control in Full-Bridge (FB) Class-D inverters is by changing the phase-shift between the switch-node voltages. The two Half-Bridge (HB) inverters with a series-balanced filter act like two sinusoidal voltage sources (v_1 and v_2). The circuit diagram of the FB Class-D inverter with controllable phase-shift is presented in Figure 4-2.

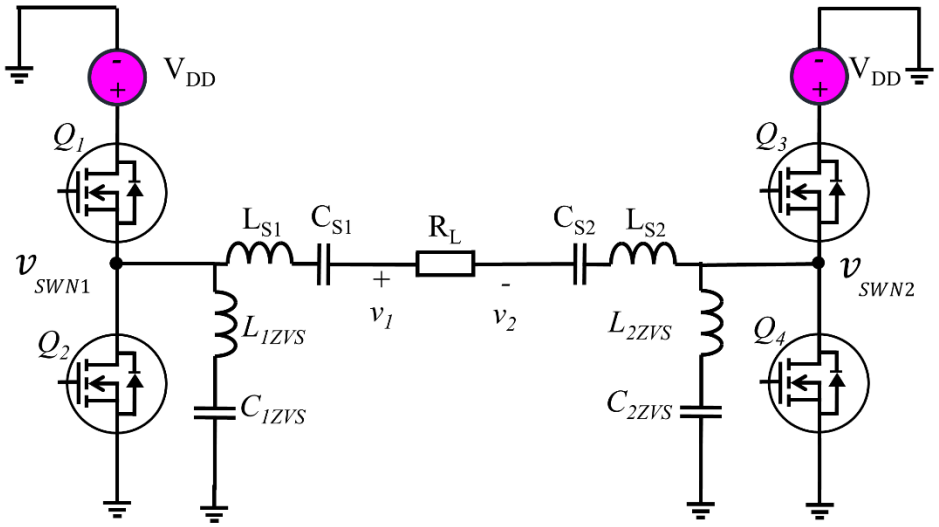

Figure 4-2: ZVS FB Class-D inverter with phase-shift control

Using trigonometric identities, the differential output voltage across the load can be written as follows:

$$v_{out} = v_1 - v_2 = \frac{2V_{DD}}{\pi}(\cos(\omega t) - \cos(\omega t + \varphi)) = \frac{4V_{DD}}{\pi}\sin(\omega t + \frac{\varphi}{2})\sin(\frac{\varphi}{2}) \qquad 4\text{-}1$$

For $\varphi = 0, \frac{\pi}{2}, and\ \pi$, the amplitude of the differential output voltage is $V_{out} = 0$, $\frac{2\sqrt{2}V_{DC}}{\pi}$, and $\frac{4V_{DC}}{\pi}$, respectively. Figure 4-3 shows the differential output voltage regulation with respect to the phase-shift of the inverter assuming V_{DD} = 45V.

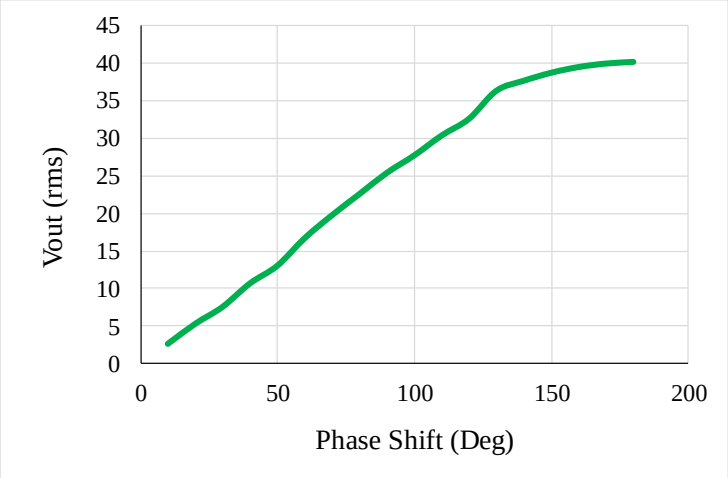

Figure 4-3: FB Class-D inverter output voltage control with phase-shift

Figure 4-3 shows that with a fixed DC input voltage (V_{DD}), the output voltage can be regulated from zero to maximum while the phase-shift is varied from 0° to 180°. The main drawback of this control method is that as the input DC voltage is kept constant in this control scheme for the entire range of the output power, the output capacitances of the switching devices charge and discharge to maximum input DC voltage no matter the level of the output power. The ZVS inductor rms current also remains constant according to Equation 3-3 when the input DC voltage is fixed. As a result, switching losses related to off-capacitance charge and discharge and the ZVS inductor current do not change during phase shift. In general, the losses in the inverter under phase-shift control remain constant, resulting in very low efficiency at light loads.

In this study, the output voltage is regulated using input DC voltage as the fixed frequency scheme results in easier EMI compliance, and the lower input DC voltage at lower output power results in less switching loss and consequently higher efficiency. The main important challenge of output power regulation using input DC voltage is the possible loss of soft-switching at lower voltages. This issue is addressed by employing Dynamic Dead-time Control (DDTC), which is presented in the next section.

4.3 Dynamic Dead-Time Control Hardware Implementation

In this section, hardware implementation of a fixed-frequency, power controllable FB Class-D inverter which can maintain soft-switching over a wide range of input DC voltage with minimum switching loss is presented. The output RF power is regulated by changing the input DC voltage applied to the inverter. As explained in Section 3.5.1, the inverter enters partial ZVS mode during output power regulation with input DC voltage variation if the DT remains fixed.

Dead-time (DT) control and related effects on the switching performance of power converters have been the subject of some research works in the literature [89-92]. However, the issue of DT control and related effects on the overall efficiency of multi-MHz inverters has not been addressed in the literature. In order to sustain ZVS during input DC voltage variations, the DDTC approach is proposed in this section for an inverter at 13.56 MHz. DDTC can be implemented on an inverter at 13.56 MHz switching frequency using a costly digital control platform such as DSP or FPGA. However, in this study, a low-cost and practical circuit using a microcontroller and an array of digital potentiometers are deployed.

The technique can be easily incorporated into a multi-MHz Class-D inverter design without the need to fully change the control platform or add unnecessary cost to the design. The proposed system is experimentally verified on a laboratory prototype built for this purpose. Figure 4-4 shows the block diagram of the entire system used to implement DDTC, including the Micro-Controller Unit (MCU), digital DT circuit, DC-DC buck-boost converter, DC/AC 13.56 MHz FB Class-D inverter, series resonant filter, and RF load.

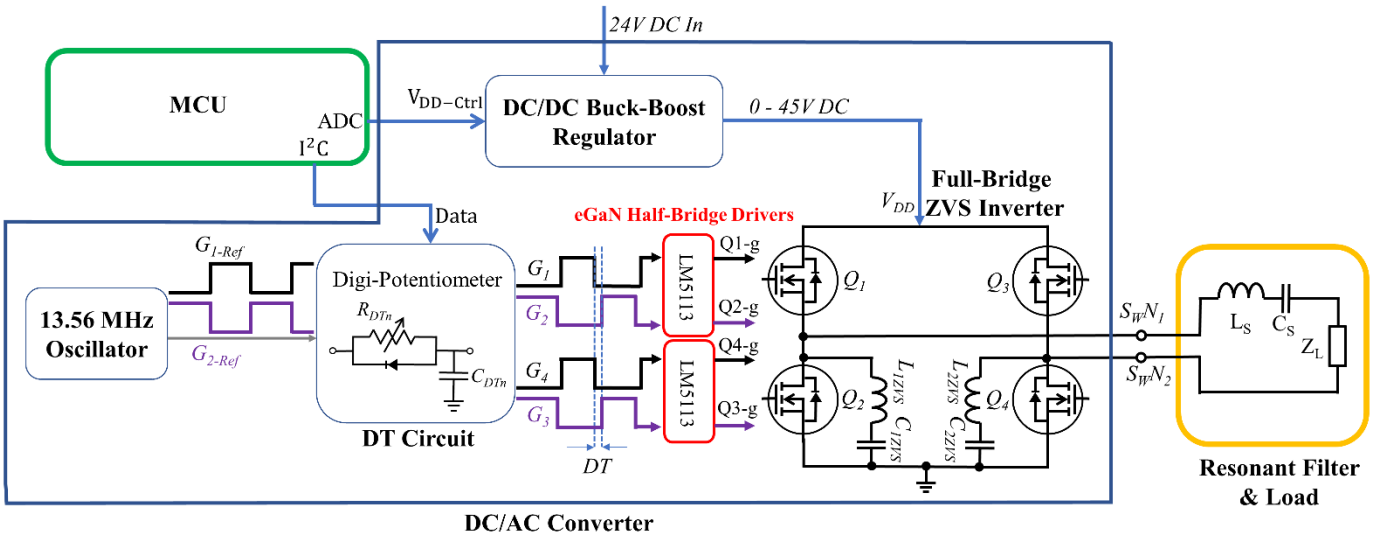

Figure 4-4: DDTC hardware block diagram

The basic idea is to simultaneously control V_{DD} and the DT between the gate signals being sent to the switches of the inverter. The MCU provides an analog signal to linearly control the output voltage of the DC-DC converter. It also sends digital commands to a 4-channel digital-potentiometer to adjust the DT of each switch gate signal. As shown in Figure 4-4, the circuit used for DT adjustment of each gate signal consists of a parallel reverse-connected Schottky diode and one of the channels of the digital-potentiometer (R_{DT}) connected in series with a capacitor (C_{DT}) which determines the discharge time constant of

the capacitor ($R_{DT}C_{DT}$). Diodes connected across each digitally controllable resistive channel of the potentiometer (R_{DTn}, n = 1-4) provide a fast discharging path for C_{DTn} while blocking the charging current. Accordingly, the C_{DTn} charging currents need to pass through R_{DTn}, resulting in a charging time constant which corresponds to DT. The DT circuit receives two non-overlapping 13.56 MHz clock signals ($G_{1\text{-}Ref}$, $G_{2\text{-}Ref}$) with 50% duty cycle and delivers four reference gate signals (G_1, G_2, G_3, and G_4) with controllable rise-time. These signals are then delivered to the eGaN FET drivers to be converted to the actual gate signals. The circuit has a negligible impact on the gate signals' fall-time because of the Schottky diodes that are utilized in parallel with R_{DTn}. Dynamically adjusting R_{DTn} through MCU results in variable C_{DTn} charging time constant and hence controllable DT_n. The MCU sends digital codes to the DT circuit to set the required DT_n which is required to maintain ZVS at a certain V_{DD}. As a first step, the value of DT_n is calculated using Equations 3-3 and 3-4. The value is then optimized in the real system to compensate for the practical tolerance that exists in L_{ZVS} and the off-capacitance of the eGaN FETs. In this research, the optimization is carried out by modifying the DT values obtained using Equations 3-3 and 3-4 to achieve the lowest overshoot on the switch-nodes. The modified values of DT are then stored in a DT lookup table for different V_{DD} levels. After programming the MCU with the modified lookup table, DT is set during the operation of the inverter for the desired V_{DD} level needed for delivering a certain power to the RF load. The circuit presented for DDTC implementation is low cost and can be easily integrated into a fixed DT system compared to migration to a DSP or FPGA based control system. Also, an oscillator with very high phase stability is used in this design, which makes dealing with the total jitter level of the design easier compared to a full high-speed digital controller.

4.4 Experimental Setup and Results

An experimental prototype of the DC/AC converter proposed in the block diagram shown in Figure 4-4 and the experimental results of representative waveforms, efficiency, and temperature of the converter are presented in this section.

4.4.1 Experimental Prototype

Figure 4-5 shows the PCB implementation of the DC/AC converter proposed in the block diagram shown in Figure 4-4. It is a 4-layer PCB with two ground planes on layers 2 and 4 and signals on layers 1 and 3 that are laid out manually using Altium Designer software. A 4-channel 1kΩ digital-potentiometer is utilized which represents R_{DTn} in the DT circuit. The PCB is optimally designed to keep the parasitic inductance of the inverter power loops at the lowest possible level which leads to a smaller voltage ringing on the switch node. The optimal layout is achieved by proper placement of switching components and high-frequency decoupling ceramic capacitors providing V_{DD} to the eGaN FETs of each half-bridge in very close proximity. The return current paths for the power loops of both half-bridges are also placed on the first internal layer to achieve the lowest CSI [27]. The optimal PCB layout helps, in that the effect of DDTC on the switch-node voltage overshoot can be measured more accurately.

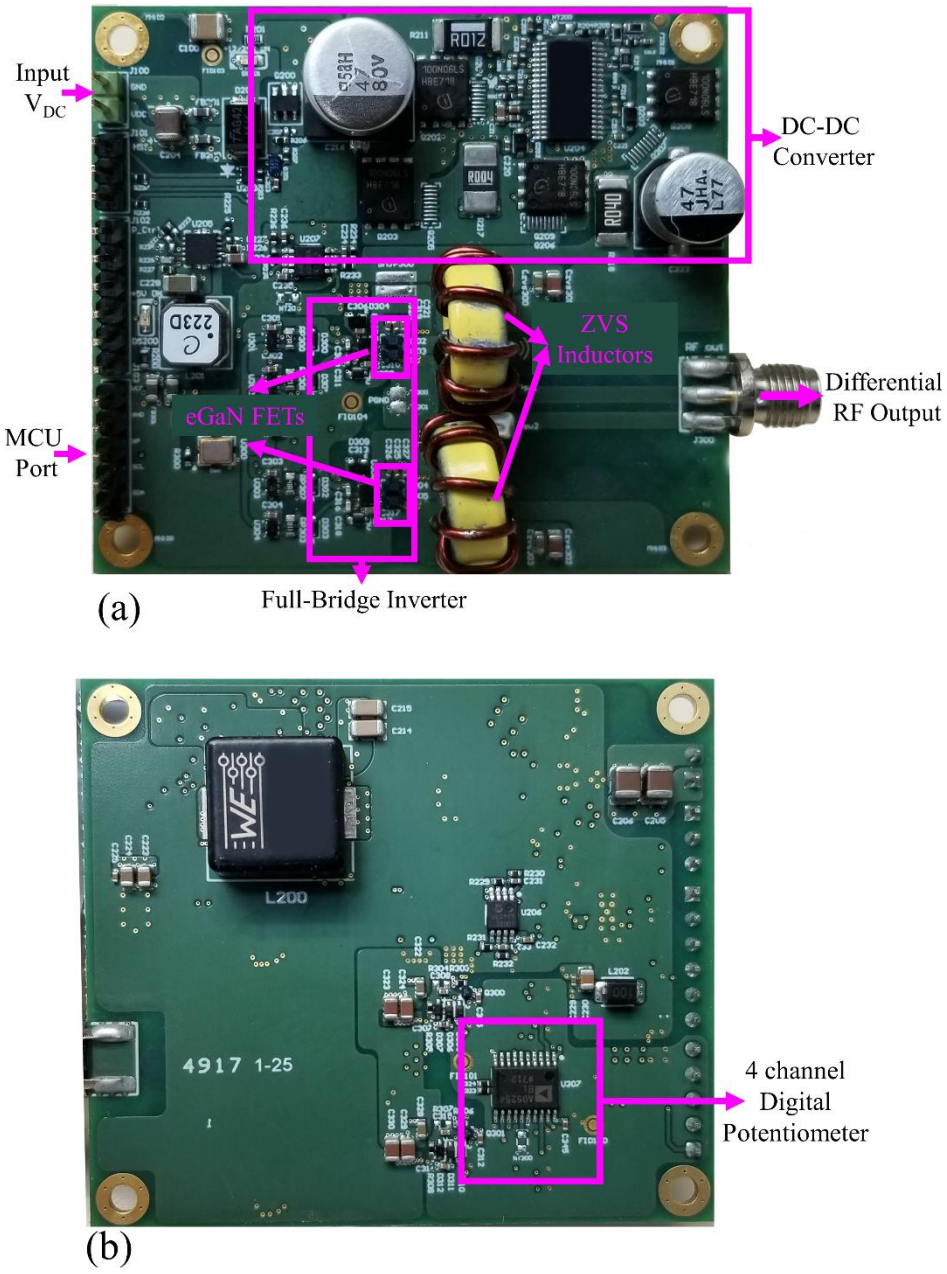

Figure 4-5: Experimental prototype of the DC/AC converter, 61 mm × 54 mm: (a) top layer, (b) bottom layer

Figure 4-6 shows the complete experimental set-up of the system shown in Figure 4-4. The computer is used as a master controller.

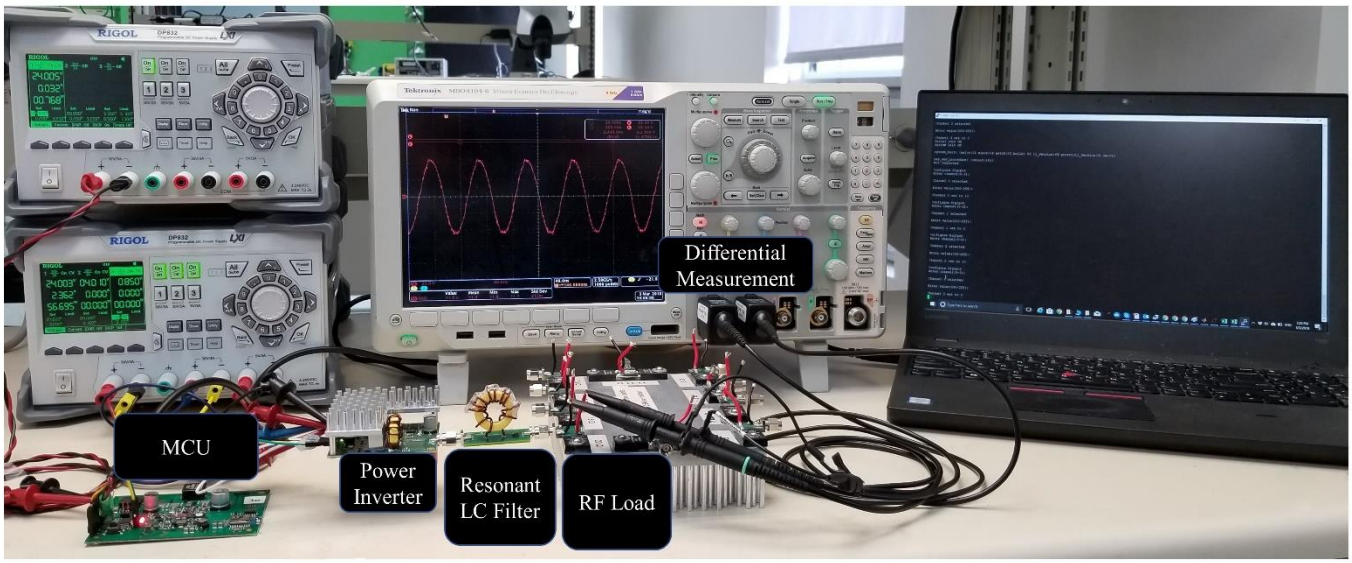

Figure 4-6: Experimental test setup including MCU, inverter, resonant filter, and RF load

The role of the master controller is to send high-level commands to the MCU board. These commands include turning on and off of the entire system and setting the level of the output RF power. The MCU, which is an Atmel AT32UC3C2512C-Z2U, controls the system locally as shown in the system block diagram of Figure 4-4. A 1GHz-5GS/s Tektronix oscilloscope series 4104-6 and single-ended 300V-1GHz passive probes with 3.9 pF input capacitance and very short ground leads (lowest probing inductance impact) are used for more accurate signal measurement at high-frequency. The same probes are also used in the differential mode to measure the differential voltage delivered to the RF load (see Figure 4-6). The parameters of the experimental setup are identical to the simulation parameters listed in Table 3-2, except for the DT range which is different due to the practical tolerance of the components and parasitics on the PCB.

The MCU firstly loads the digital-potentiometer with values calculated for R_{DTn} using Equation 4-2 which is derived by equating DT calculated from Equation 3-4 to the time

needed to charge C_{DTn} (= 22pF) up to the high voltage threshold of the gate driver (V_{TH} = 2.18 V), considering that the peak $G_{n\text{-}Ref}$ voltage is 5V.

$$R_{DTn} = \frac{DT}{0.57\ C_{DTn}} \qquad 4\text{-}2$$

The R_{DTn} is then optimized based on the switch-nodes overshoot and the overall inverter no-load power consumption. Switch-node voltage overshoot clearly shows if the off-capacitance of the switching devices are charging or discharging with the right pace within the DT, and the no-load power consumption of the inverter is mostly dominated by switching loss. As a result, making these two parameters minimum results in the best switching performance at different V_{DD} levels. Figure 4-7 shows the optimized values for R_{DT1} and R_{DT2} at different V_{DD} levels. The resistance values of the DT circuit of the second half-bridge inverter (R_{DT3} and R_{DT4}) follow a similar pattern because of the symmetry in the PCB layout resulting in almost similar layout parasitics.

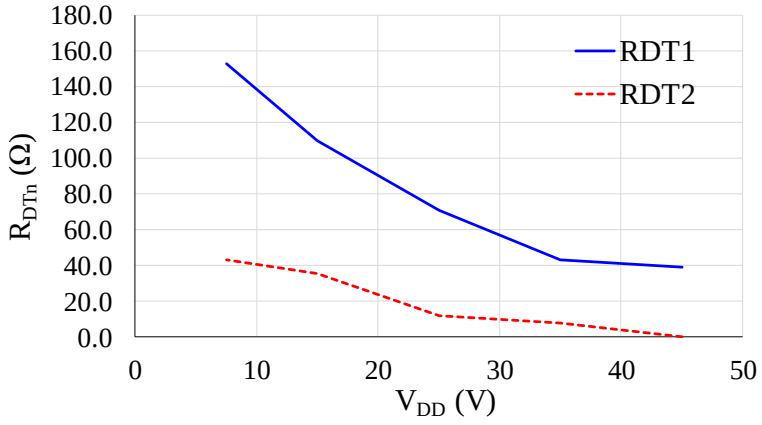

Figure 4-7: R_{DT1} and R_{DT2} optimized values vs. V_{DD}

4.4.2 Experimental Prototype Results

Figure 4-8 shows the real-time measurement of $G_{1\text{-Ref}}$, $G_{2\text{-Ref}}$, G_1, and G_2 signals during DDTC while V_{DD} is set at five different voltage levels. At each V_{DD} level setpoint, an optimized DT is obtained based on the lowest voltage overshoot on the switch-node and the lowest no-load power consumption. For each V_{DD} level, the waveforms of G_1, and G_2 gate signals are saved on the oscilloscope. The data obtained at different V_{DD} levels is eventually superimposed in MATLAB to provide a better overall picture of practical DT needed to achieve soft-switching. As the eGaN FETs are physically placed very close to the drivers and the decoupling capacitors to keep the gate and power loops very small (less than 0.2 mm space between the cases), there is no practical way to probe the actual gate signals to the eGaN FETs. Instead, the DT circuit output signals are probed, and the DT is calculated based on the input voltage threshold of the gate driver (V_{TH} = 2.18 V), as shown in Figure 4-8.

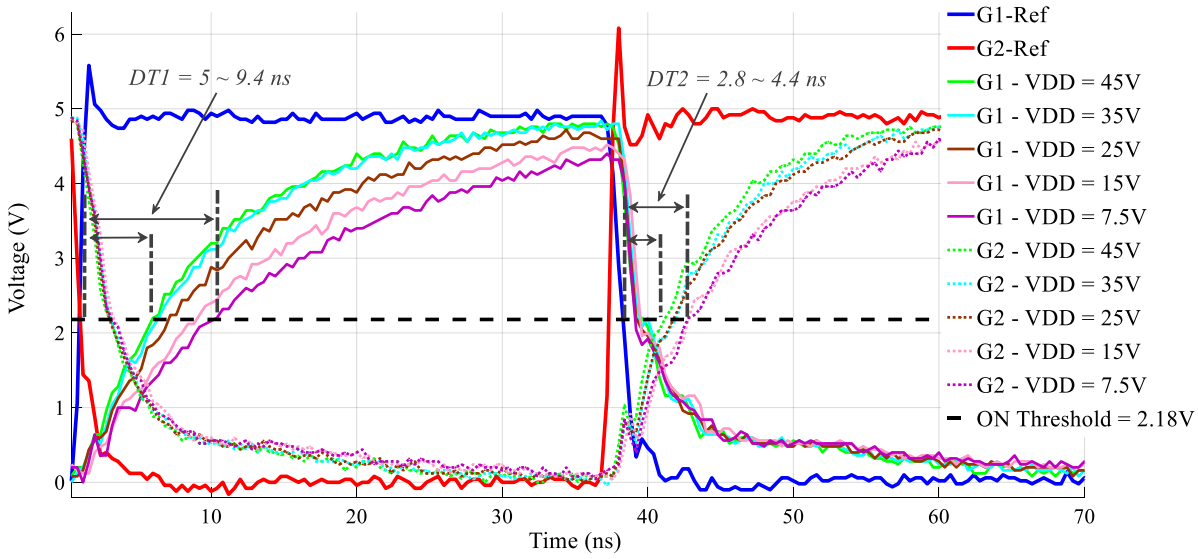

Figure 4-8: $G_{1\text{-Ref}}$, $G_{2\text{-Ref}}$, G_1, and G_2 references and gate signals at different V_{DD} levels

The R_{DTn} lookup table can be extended to a higher resolution at a higher number of steps for V_{DD} in case higher accuracy is required for a particular application. While regulating the RF output power, the digital-potentiometer is first loaded with R_{DTn} which is the optimal value for DT at a certain V_{DD} level. V_{DD} is then stepped up or down to provide the desired level of RF power to the load.

Switch-node 1 voltage (v_{SwN1}) waveforms at different voltage levels with fixed DT and DDTC are presented in Figure 4-9 and Figure 4-10.

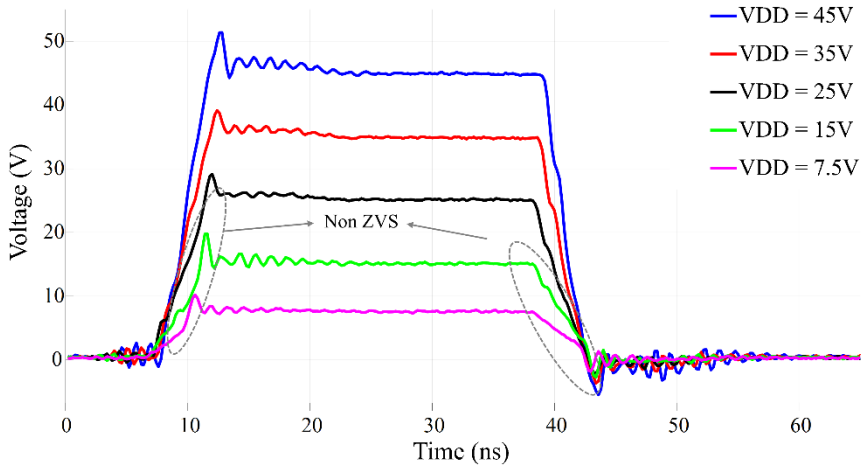

Figure 4-9: v_{SwN1} waveform at different V_{DD} levels with fixed DT

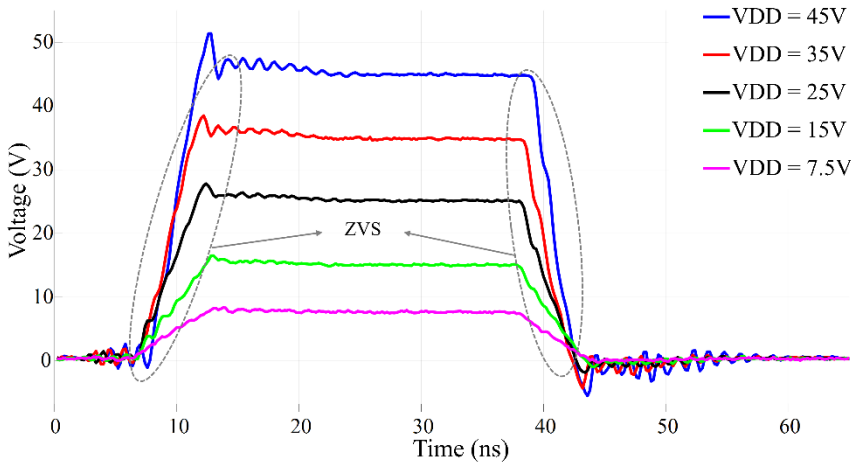

Figure 4-10: v_{SwN1} waveform at different V_{DD} levels with DDTC

The R_{DTn} values corresponding to V_{DD} = 45V are loaded and kept constant during V_{DD} regulation to obtain the experimental results for the fixed DT scenario. As a result, the soft-switching scheme of the inverter gradually phases out by decreasing the V_{DD} level (See Figure 4-9). It can be seen in Figure 4-10 that changing R_{DTn} dynamically and consequently DT_n helps the inverter to sustain soft-switching over the full range of V_{DD}. The test with fixed DT can also be performed by setting the DT for the lowest V_{DD} level instead of the highest. While this approach will guarantee enough time for soft-switching at all V_{DD} levels, the anti-parallel diode of the eGaN FET will conduct during the excessive DT interval, making the inverter extremely inefficient as the source-drain voltage of eGaN FET is very high (2.2 V in EPC8009). This issue is explained in Section 3.5.2 in detail. Adding external parallel Schottky diode with lower forward voltage to the eGaN FET to address this problem as suggested in [93] is also not practical because of the diode reverse recovery

and extra capacitance that will be introduced to the switch node. The v_{SwN1} overshoot percentage under the two test scenarios are compared in Figure 4-11.

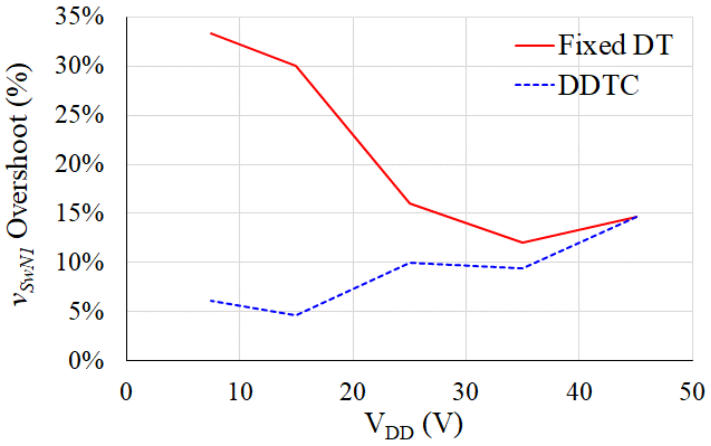

Figure 4-11: Switch-node 1 (v_{SwN1}) overshoot at different V_{DD} levels

Figure 4-11 shows that a lower switch-node voltage overshoot can be achieved when the DT is dynamically controlled during V_{DD} variations. The overshoot levels confirm the value that was used for L_{CSI} in Table 3-2.

Measuring the drain-source current of eGaN FET is practically impossible because of the extremely close proximity of the components on the PCB and high sensitivity of the power loop to parasitic inductance which can increase dramatically by a current probe. As a result, the simulation results provided in Figure 3-11 cannot be experimentally verified. Instead, in this section, the inverter is tested with both fixed DT and DDTC while changing the input DC voltage from 7.5V to 45V to examine its performance. The RF output power delivered to the 25 Ω load is regulated almost linearly from 1.68W to 59.36W, while the steady-state efficiency and temperature of the custom-designed heatsink attached to the eGaN FETs are measured. It is worth noting that EPC8009 is a top cooling device; so a proper heatsink

needs to be selected and attached to the top of the device. A very thin layer of thermal paste with very high thermal conductivity (5 W/mK) is also used to provide effective heat transfer between the body of the device and the heatsink. The results obtained from both tests are presented in Figure 4-12.

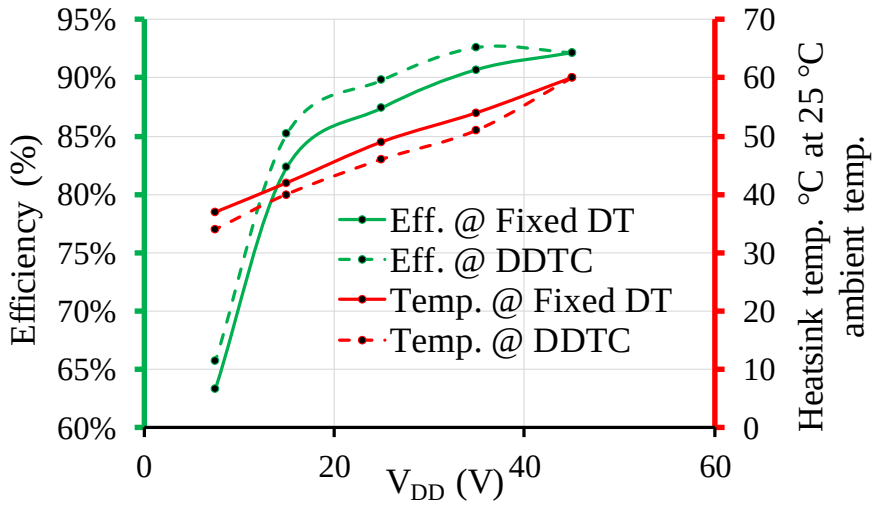

Figure 4-12: FB Class-D power inverter efficiency and heatsink temperature with fixed DT and DDTC at different DC voltage levels

Figure 4-12 shows how the inverter can sustain higher steady-state efficiency, determined as the ratio of the measured output power to input power. The lower operation temperature on the attached heatsink under DDTC compared to fixed *DT* while delivering regulated power to the RF load is alo shown in Fig. 4-12. The higher efficiency and lower overall PCB temperature shown in this figure is a direct result of complete ZVS under DDTC as opposed to partial ZVS with fixed DT. The efficiency of the inverter during load modulation is also shown in Figure 4-13.

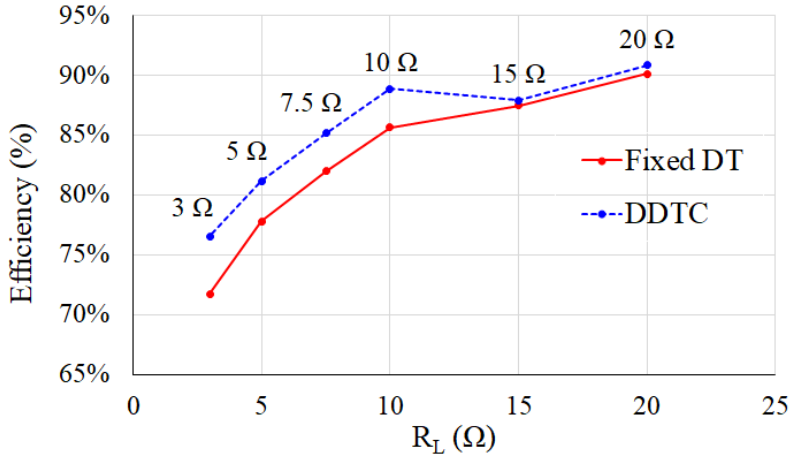

Figure 4-13: FB Class-D power inverter efficiency at fixed 40W output power delivered to various R_L

Figure 4-13 shows how the inverter can sustain higher efficiency under DDTC compared to fixed DT while delivering a fixed 40 W during load modulation.

4.5 Class-D Inverter Harmonic Analysis

One of the most important parameters in the performance evaluation of a power inverter is the harmonic content of the output voltage, measured as the total harmonic distortion. The harmonic analysis of the differential switch-node voltage of the FB Class-D inverter built and tested in this chapter with V_{DD} = 45V is demonstrated in Figure 4-14. The harmonic content of the output voltage of the inverter determines the cost and complexity of the output filter and the amount of effort needed to meet EMC regulations. The relatively high amplitude of the 3rd and 5th harmonics of the inverter differential switch-node voltage can only be attenuated with a high order or High Quality (HQ) resonant filter.

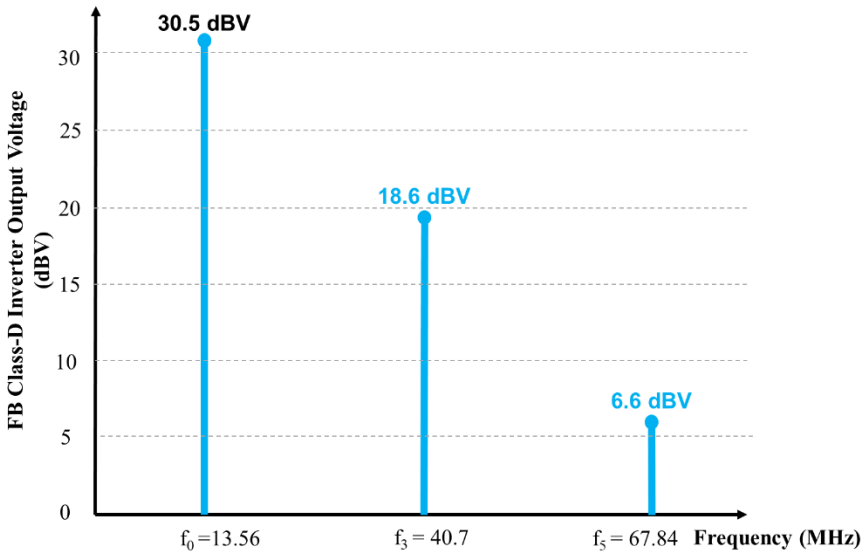

Figure 4-14: Class-D inverter output voltage harmonic analysis

Frequency tuning, large inductor size, and low efficiency are the main drawbacks of HQ resonant filters. As a result, an inverter which generates much lower unwanted harmonics on its output voltage and hence meets EMC requirements with a smaller size and more efficient output filter, is introduced in Chapter 5.

4.6 Summary

In this chapter, different approaches to control the output power of a FB Class-D inverter are firstly explained. By considering the challenges of maintaining soft-switching during output power regulation using input DC voltage (V_{DD}) control, the DDTC method is proposed and utilized to sustain soft-switching during output power regulation. A practical, low-cost circuit is then proposed for a more convenient integration of the control method to an inverter with fixed DT at 13.56 MHz. The DDTC scheme can be implemented in a

fixed DT inverter without the need to migrate to expensive high-speed controllers and related clock stability and jitter issues. An experimental testbed is then built which includes the prototype of the DC/AC converter, digital DT circuit, MCU, output resonant filter, and RF load to experimentally validate the effectiveness of the DDTC approach. The experimental results show that adjusting DT during V_{DD} control for output power regulation results in less voltage overshoot on the switch-nodes and consequently less switching loss. It is also shown that the inverter with DDTC can achieve higher steady-state efficiency and lower operating temperature compared to the system with fixed DT while delivering regulated power to 25 Ω RF load. The last section of this chapter presents the harmonic content of the Class-D FB inverter. The harmonic content shows that the inverter requires a filter with high attenuation level to suppress the 3^{rd} and 5^{th} harmonics to a level that can pass EMC regulations.

CHAPTER 5

5 Development of a Multi-MHz Multi-Level Class-D Inverter with Low Harmonics and Zero Voltage Switching

5.1 Introduction

Any power converter needs to be designed to meet EMC to be used as stand-alone or as a unit in a bigger electric system. Resonant coupled WPTSs are designed at multi-MHz frequency ranges to reduce the size of their transmitters and receivers. As a result, they need a low EMI power source on the transmit side capable of providing RF power at their operating frequencies. There are essentially two approaches for meeting EMC requirements in power inverters. The first approach is to design a power inverter which naturally generates higher frequency harmonics in the switching block and filtering them out in the next stage using an HQ EMI filter. The filter should have enough attenuation capability in the desired frequency

band to deliver clean power to the rest of the system. The main drawbacks of this approach are the large size and high loss of the filter inductor which results in a low overall efficiency of the filter block and consequently the power inverter.

The second approach is to avoid generating unwanted harmonics in the first place in the inverter and achieve the same EMC performance with less complex and less costly EMI filter design. The latter approach is explored in this Chapter using multi-level topology. This topology has been used for low switching frequency applications for a long time [94-97]. However, they were never investigated for multi-MHz application until recently [98, 99]. The topology investigated in this chapter is a Class-D multi-level inverter which produces stepped voltage waveform with very low 3^{rd} and 5^{th} harmonics, eventually allowing for much more flexibility in the design of the EMI filter. The topology also makes it possible for higher output power levels to be achieved as opposed to single-stage Class-D inverter.

The mathematical analysis of the stepped voltage waveform with low harmonics is presented in the next sections and derived equations are solved to calculate the modulation parameters required to suppress the level of the unwanted harmonics. The mathematical analysis is then used to simulate and experimentally implement a 3^{rd} and 5^{th} harmonic-free multi-MHz multi-level inverter. The feasibility of the approach, soft-switching performance, and harmonic elimination capability of the inverter during output power regulation are demonstrated through simulation results. More investigation is then carried out using experimental results obtained from a prototype PCB built.

5.2 Stepped Waveform with Zero 3rd and 5th Harmonics

Figure 5-1 demonstrates a stepped waveform without DT, which can theoretically generate zero 3rd and 5th harmonics with certain modulation index (m) and trigger angle (α) [100]. m and α as the main parameters of the stepped waveform are shown in Figure 5-1. For a general stepped waveform, m is a fraction of the top-level voltage (V_{DD}) and has a value in the range $0 < m < 1$. α defines the start point or trigger angle of the top-level voltage and can theoretically have values in the range $0° < \alpha < 90°$.

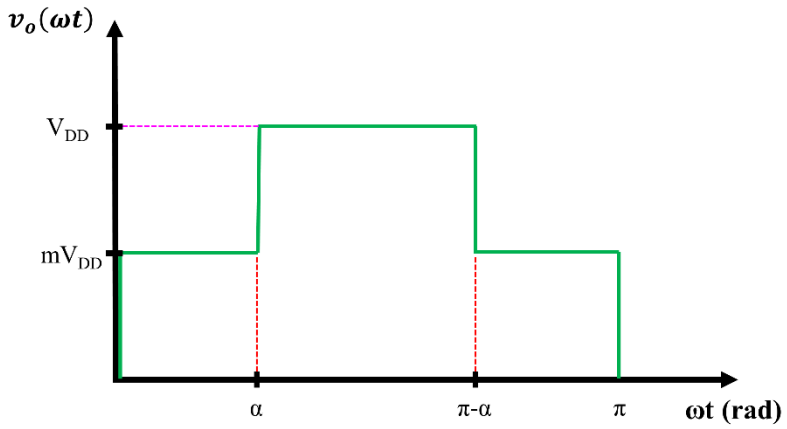

Figure 5-1: Half cycle demonstration of an ideal stepped waveform with the possibility of zero 3rd and 5th harmonics

Using Fourier expansion, the sine coefficients of the signal can be defined as follows:

$$v_{on} = \frac{2}{\pi}\int_0^{\pi} v_o(\omega t)\sin(n\omega t)\,d\omega t \qquad 5\text{-}1$$

$$= \frac{2V_{DD}}{n\pi}\left(m + (1-m)\cos(n\alpha) + (m-1)\cos\left(n(\pi-\alpha)\right) - m\cos(n\pi)\right)$$

As a result, the 1st harmonic amplitude of v_o can be written as follows:

$$v_{o1} = \frac{4V_{DD}}{\pi}(m + (1 - m)\cos(\alpha)) \qquad 5\text{-}2$$

The 3rd and 5th harmonics are zero if $v_{o3} = v_{o5} = 0$; which results in $m = 0.413$ and $\alpha = 45.05°$ [100].

As discussed in Chapter 3, for multi-MHz switching frequency operation, DT is comparable with the overall period of the signal; therefore, it can have an important impact on the level of the harmonics if not appropriately modeled. A detailed analysis of the effect of DT on the harmonic distortion of a Class-D inverter operating in KHz switching frequency is presented in [101]. Figure 5-2 shows a stepped waveform that incorporates the effect of DT to more accurately reflect the impact of this parameter on the level of the harmonics. Parameter D, shown in this figure, represents the DT in radians.

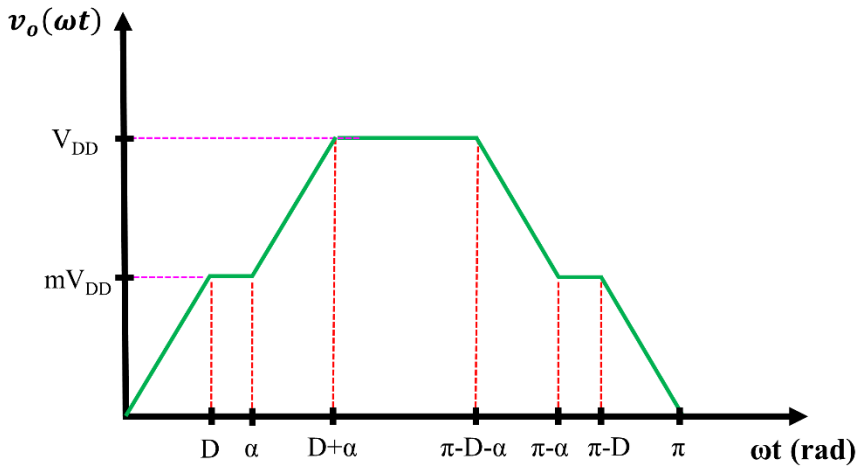

Figure 5-2: Half cycle of the stepped waveform with the possibility of zero 3rd and 5th harmonics

The waveform of Figure 5-2 is described by the following functions:

$$v_o(\omega t) = \begin{pmatrix} \frac{mV_{DD}}{D}\omega t & 0 \le \omega t < D \\ mV_{DD} & D \le \omega t < \alpha \\ \frac{(1-m)V_{DD}}{D}(\omega t - \alpha) + mV_{DD} & \alpha \le \omega t < \alpha + D \\ V_{dd} & \alpha + D \le \omega t < \pi - \alpha - D \\ \frac{(m-1)V_{DD}}{D}(\omega t - \pi + \alpha + D) + V_{DD} & \pi - \alpha - D \le \omega t < \pi - \alpha \\ mV_{DD} & \pi - \alpha \le \omega t < \pi - D \\ \frac{-mV_{DD}}{D}(\omega t - \pi + D) + mV_{DD} & \pi - D \le \omega t < \pi \end{pmatrix} \quad \text{5-3}$$

The cosine coefficients (a_n) are zero because the signal is odd and has a ¼-wave symmetry. Fourier analysis can then be applied over half a period of the signal to obtain the sine coefficients (b_n) as follows:

$$v_{on}(\omega t) = \frac{2}{\pi}\int_0^{\pi} v_o(\omega t)\sin(n\omega t)\,d\omega t$$

$$= \frac{2}{\pi}\Bigg[\underbrace{\int_0^{D}\frac{mV_{DD}}{D}\omega t\sin(n\omega t)\,d\omega t}_{I} + \underbrace{\int_D^{\alpha} mV_{DD}\sin(n\omega t)\,d\omega t}_{II}$$

$$+ \underbrace{\int_{\alpha}^{\alpha+D}\left(\frac{(1-m)V_{DD}}{D}(\omega t-\alpha)+mV_{DD}\right)\sin(n\omega t)\,d\omega t}_{III}$$

$$+ \underbrace{\int_{\alpha+D}^{\pi-\alpha-D} V_{DD}\sin(n\omega t)\,d\omega t}_{IV} \qquad 5\text{-}4$$

$$+ \underbrace{\int_{\pi-\alpha-D}^{\pi-\alpha}\left(\frac{(m-1)V_{DD}}{D}(\omega t-\pi+\alpha+D)+V_{DD}\right)\sin(n\omega t)\,d\omega t}_{V}$$

$$+ \underbrace{\int_{\pi-\alpha}^{\pi-D} mV_{DD}\sin(n\omega t)\,d\omega t}_{VI}$$

$$+ \underbrace{\int_{\pi-D}^{\pi}\left(\frac{-mV_{DD}}{D}(\omega t-\pi+D)+mV_{DD}\right)\sin(n\omega t)\,d\omega t}_{VII}\Bigg]$$

Integrals I to VII in Equation 5-6 are evaluated separately as follows:

$$\overset{I}{\rightarrow}\left[\frac{mV_{DD}}{D}\left(\frac{-D}{n}\cos(nD)+\frac{1}{n^2}\sin(nD)\right)\right]_{n=3} = \frac{-mV_{DD}}{3}\cos(3D)+\frac{mV_{DD}}{9D}\sin(3D) \qquad 5\text{-}5$$

$$\overset{II}{\rightarrow}\left[\frac{-mV_{DD}}{n}(\cos(n\alpha)-\cos(nD))\right]_{n=3} = \frac{mV_{DD}}{3}\cos(3D)-\frac{mV_{dd}}{3}\cos(3\alpha) \qquad 5\text{-}6$$

$$\xrightarrow{III}\left[\frac{(1-m)V_{DD}}{D}\left(\frac{-(\alpha+D)}{n}\cos\big(n(\alpha+D)\big)+\frac{1}{n^2}\sin\big(n(\alpha+D)\big)\right.\right.$$
$$\left.+\frac{\alpha}{n}\cos(n\alpha)-\frac{1}{n^2}\sin(n\alpha)\right)$$
$$\left.+\frac{1}{n}\left(\frac{(m-1)V_{DD}\alpha}{D}+mV_{dd}\right)\big(\cos(n\alpha)-\cos\big(n(\alpha+D)\big)\big)\right]_{n=3} \quad \text{5-7}$$
$$=\frac{-V_{DD}}{3}\cos\big(3(\alpha+D)\big)+\frac{(1-m)V_{DD}}{9D}\sin\big(3(\alpha+D)\big)$$
$$-\frac{(1-m)V_{DD}}{9D}\sin(3\alpha)+\frac{mV_{DD}}{3}\cos(3\alpha)$$

$$\xrightarrow{IV}\left[\frac{V_{DD}}{n}\big(\cos\big((\alpha+D)\big)-\cos\big(n(\pi-\alpha-D)\big)\big)\right]_{n=3}=\frac{2V_{DD}}{3}\cos\big(3(\alpha+D)\big) \quad \text{5-8}$$

$$\xrightarrow{V}\left[\frac{(m-1)V_{DD}}{D}\left(\frac{-(\pi-\alpha)}{n}\cos\big(n(\pi-\alpha)\big)+\frac{1}{n^2}\sin\big(n(\pi-\alpha)\big)\right.\right.$$
$$\left.+\frac{(\pi-\alpha-D)}{n}\cos\big(n(\pi-\alpha-D)\big)-\frac{1}{n^2}\sin\big(n(\pi-\alpha-D)\big)\right)$$
$$+\frac{(1-m)V_{DD}(-\pi+\alpha+D)-V_{DD}D}{nD}\big(\cos\big(n(\pi-\alpha)\big)$$
$$\left.-\cos\big(n(\pi-\alpha-D)\big)\big)\right]_{n=3} \quad \text{5-9}$$
$$=\frac{-V_{DD}}{3}\cos\big(3(\alpha+D)\big)+\frac{(1-m)V_{DD}}{9D}\sin\big(3(\alpha+D)\big)$$
$$-\frac{(1-m)V_{DD}}{9D}\sin(3\alpha)+\frac{mV_{DD}}{3}\cos(3\alpha)$$

$$\xrightarrow{VI}\left[\frac{mV_{DD}}{n}\big(\cos\big(n(\pi-\alpha)\big)-\cos\big(n(\pi-D)\big)\big)\right]_{n=3}=\frac{mV_{DD}}{3}\cos(3D)-\frac{mV_{DD}}{3}\cos(3\alpha) \quad \text{5-10}$$

$$\overset{VII}{\rightarrow}\left[\frac{-mV_{DD}}{D}\left(\frac{-\pi}{n}\cos(n\pi)+\frac{1}{n^2}\sin(n\pi)+\frac{\pi-D}{n}\cos\big(n(\pi-D)\big)-\frac{1}{n^2}\sin\big(n(\pi-D)\big)\right)\right.$$
$$\left.+\frac{mV_{DD}(-\pi+D)-V_{DD}D}{nD}\big(\cos(n\pi)-\cos\big(n(\pi-D)\big)\big)\right]_{n=3} \qquad 5\text{-}11$$
$$=\frac{-mV_{DD}}{3}\cos(3D)+\frac{mV_{DD}}{9D}\sin(3D)$$

Substituting Equation 5-5 to Equation 5-11 into Equation 5-4 and setting n = 1, 3 and 5, the sine coefficients of the 1st, 3rd, and 5th harmonics of the stepped waveform with DT are obtained as follows:

$$v_{o1}=\frac{2}{\pi}\left(\frac{2(1-m)V_{DD}}{D}\sin(\alpha+D)-\frac{2(1-m)V_{DD}}{D}\sin(\alpha)+\frac{2mV_{DD}}{D}\sin(D)\right) \qquad 5\text{-}12$$

$$v_{o3}=\frac{2}{\pi}\left(\frac{2(1-m)V_{DD}}{9D}\sin\big(3(\alpha+D)\big)-\frac{2(1-m)V_{DD}}{9D}\sin(3\alpha)+\frac{2mV_{DD}}{9D}\sin(3D)\right) \qquad 5\text{-}13$$

$$v_{o5}=\frac{2}{\pi}\left(\frac{2(1-m)V_{DD}}{25D}\sin\big(5(\alpha+D)\big)-\frac{2(1-m)V_{DD}}{25D}\sin(5\alpha)+\frac{2mV_{DD}}{25D}\sin(5D)\right) \qquad 5\text{-}14$$

By setting Equation 5-13 and Equation 5-14 to zero and numerically solving the resultant equations, a set of values for *m* and α at different DT values can be obtained and demonstrated on a 3D plot in Figure 5-3.

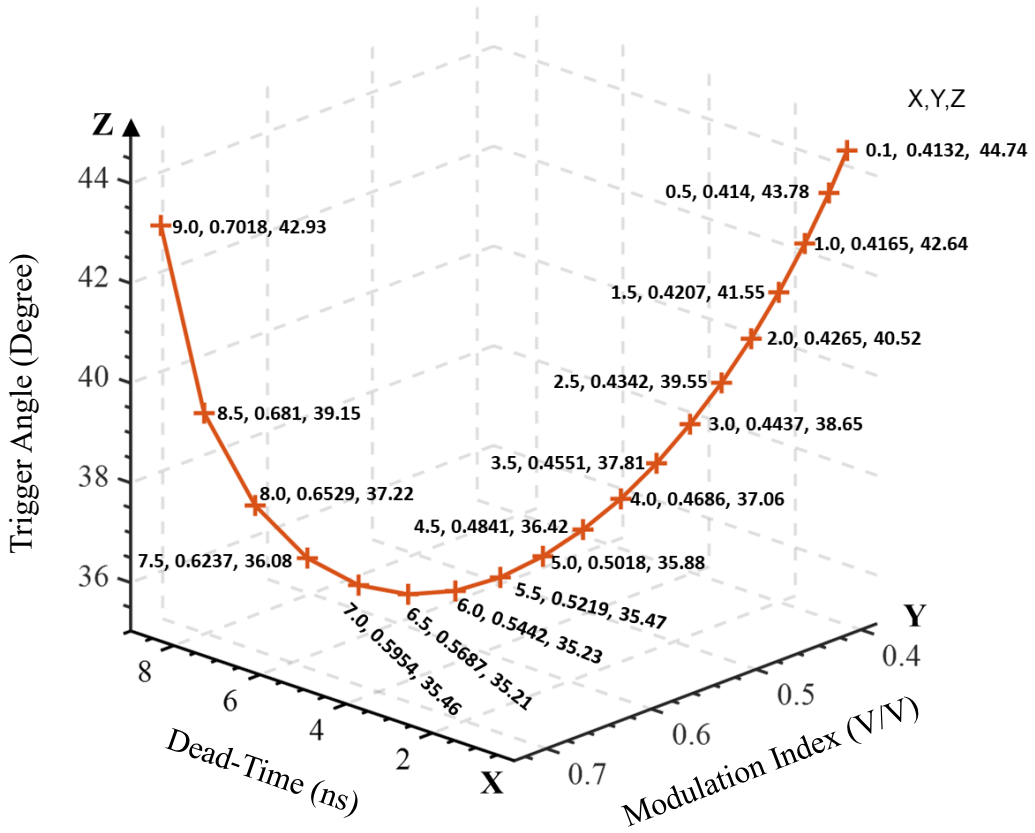

Figure 5-3: 3D plot of DT, *m*, and *α* variation

In Figure 5-3, α is in the range of 35° < α < 44°. Therefore, the top voltage level duty cycle of the stepped waveform can vary from 25% to 30%. Considering the period of the signal at 13.56 MHz (73 ns), the minimum time period for the top voltage signal including the DT is 17.6 ns at 25% duty cycle. Thus, DT values over 8.8 ns are not practical as it results in rising edge and falling edge overlap or no top voltage flat piece ($D + \alpha < \omega t < \pi - D - \alpha$). DT cannot be shorter than 4 ns either, due to the practical limitations on the rise time and fall time of digital controllers. Short DT also results in small ZVS inductors and high AC current going through the inductor, which may cause high core loss and saturation at 13.56 MHz switching frequency. As a result, considering the DT range presented in Figure 5-3 (0.1 ~ 9 ns), 6 ns is considered as a typical value for DT and is utilized in the next section for simulation purposes.

Considering the values presented in Figure 5-3, other modulation parameters of the stepped waveform utilized for simulations at DT = 6 ns in the next section are presented in Table 5-1.

Table 5-1: Zero 3rd and 5th harmonic stepped waveform parameters at DT = 6 ns

***DT* (ns)**	**Trigger Angle α (deg)**	**Modulation Index (*m*)**	**Duty Cycle ($\frac{180-2\alpha}{360} \times 100\%$)**
6	35.23	0.5442	30.4%

5.3 Multi-MHz Multi-Level Inverter Circuit Model

A multi-level inverter circuit model that is capable of creating an output voltage waveform similar to the stepped waveform shown in Figure 5-2 is presented in Figure 5-4.

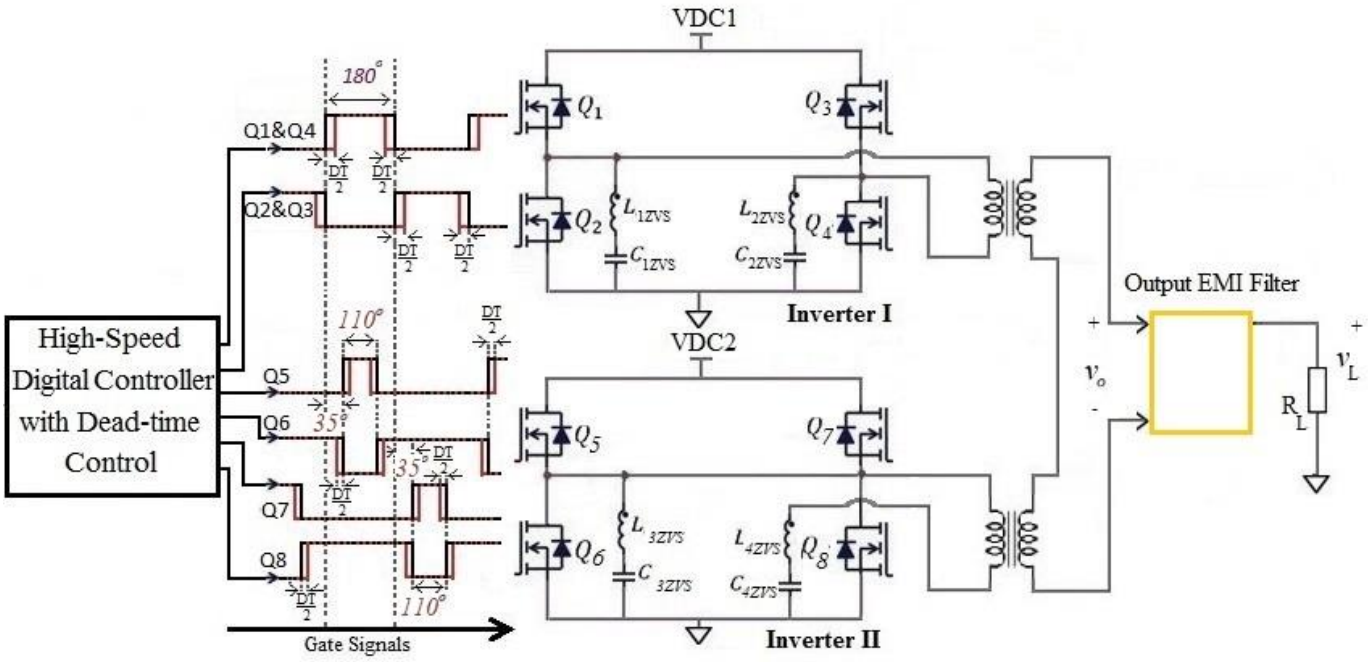

Figure 5-4: Multi-level ZVS inverter with DDTC, Inverter II gate signals at α = 35°

The topology consists of two ZVS FB Class-D inverters with different duty cycles. Inverter I has 50% duty cycle and Inverter II can operate with a variable duty cycle to generate the top

level of the stepped waveform. The topology also consists of a high-speed digital controller providing gate signals to the switching components; two high-frequency transformers used for adding up the output voltage of the inverters; and an output EMI filter to suppress unwanted harmonics.

The switching cycles and ZVS performance of both Class-D inverters shown in Figure 5-4 are identical to those of the single FB Class-D inverter explained in Section 3.4. Nevertheless, the switching performance of the inverter is simulated later in Section 5.4 of this chapter. As inverter II has a variable and less than 50% duty cycle, the upper switches (Q_5 and Q_7) conduct for less than 180º with 180º phase shift. The lower switches are OFF for the rest of the period to provide a path for the current of the ZVS inductors L_{3ZVS} and L_{4ZVS}.

V_{DC1} is the DC supply applied to inverter I and V_{DC2} is the DC supply applied to inverter II. The modulation index (m) shown in Figure 5-1 and Figure 5-2 is practically the ratio of the DC supply applied to inverter I (V_{DC1} = m V_{DD}) over the summation of the DC supplies applied to both inverters (V_{DC1}+V_{DC2} = V_{DD}). As a result, *m* can be rewritten as follows:

$$m = V_{DC1}/(V_{DC1} + V_{DC2}) \qquad 5\text{-}15$$

Using the value provided in Table 5-1 for *m* at DT = 6 ns to achieve zero 3rd and 5th harmonics, and assuming V_{DC1} = 15V, V_{DC2} can be calculated as 12.6V by utilizing Equation 5-15. These two values for V_{DC1} and V_{DC2} will be used for simulation purposes in the next section.

5.4 Multi-MHz Multi-Level Inverter Simulation Results

The simulations in this section are carried out in LTSpice and using EPC8009 switching device model. The system is first simulated at 13.56 MHz switching frequency and no-load to show the soft-switching performance of the inverter. Then, in Section 5.4.1, harmonic analysis is carried out on the output voltage of the inverter, and the results are compared with FB Class-D topology to show the effectiveness of the harmonic elimination approach. Then, output voltage regulation using DDTC is simulated in Section 5.4.2, and harmonic analysis and loading effect on the soft-switching are discussed. The circuit parameters used in the simulations are presented in Table 5-2.

Table 5-2: Multi-MHz multi-level inverter simulation parameters in LTSpice

Description	Parameter	Value
Switching frequency	f_{sw}	13.56 MHz
Output filter cut-off frequency	f_c	33 MHz
Inverter (I) ZVS inductors	L_{1ZVS}, L_{2ZVS}	800 nH
Inverter (II) ZVS inductor	L_{3ZVS}, L_{4ZVS}	500 nH
ZVS capacitors	$C_{1ZVS}, C_{2ZVS}, C_{3ZVS}, C_{4ZVS}$	1 µF (100V)
Dead-Time range	DT	4.5~8 ns
The maximum simulation time step	T_{sMax}	1 ps

The FB inverters operate at different V_{DC} levels and with different duty cycles but the same DT. This results in different values of ZVS inductors for Inverter I and Inverter II to achieve soft-switching. The ZVS inductor values are presented in Table 5-2.

The multi-level inverter no-load simulation is carried out, and the gate signals, drain-source voltages of the switches at one leg of each inverter, and output voltage of the multi-level inverter (v_o) at DT = 6 ns are presented in Figure 5-5 to Figure 5-7, respectively.

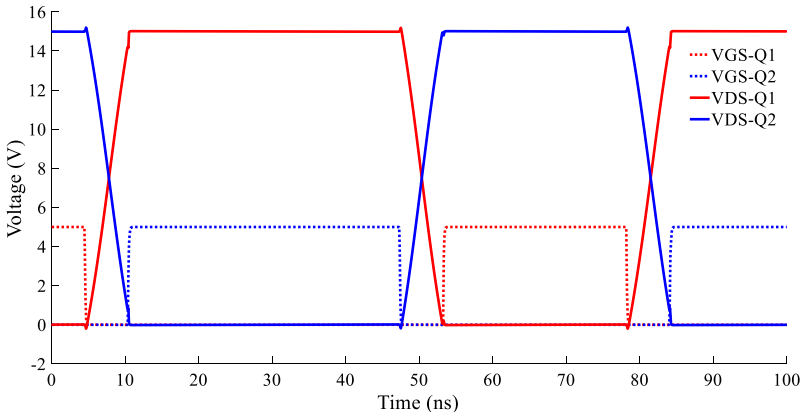

Figure 5-5: Gate and drain-source voltages of Q_1 and Q_2

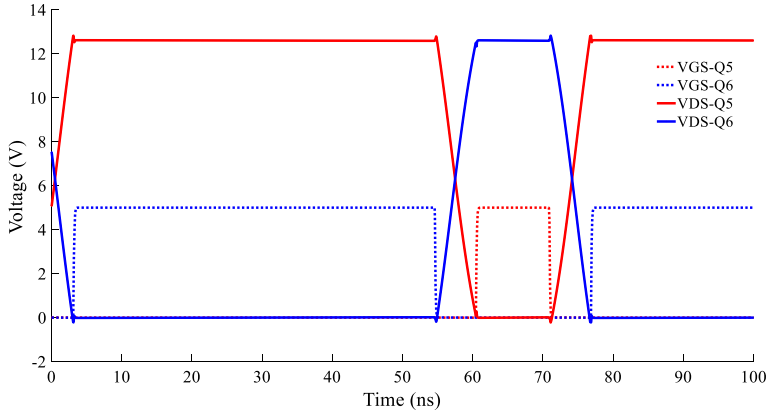

Figure 5-6: Gate and drain-source voltages of Q_5 and Q_6

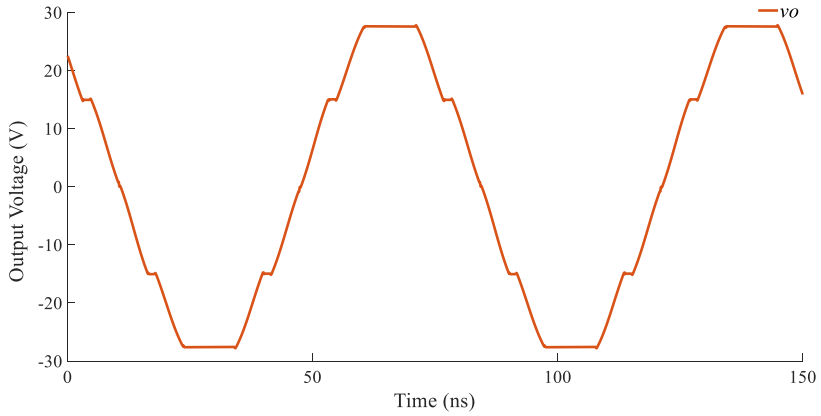

Figure 5-7: Output voltage of the multi-level inverter, DT = 6 ns, m = 0.5442, and α = 35.23°

Referring to the soft-switching analysis and the simulation results presented in Section 3.5 for FB Class-D topology (Figure 3-6 and Figure 3-10), it can be concluded that the absence of voltage ringing on the drain-source voltage of the eGaN® FETs during each transition shown in Figure 5-5 and Figure 5-6 implies that the off-capacitances of the switching devices in both inverters are fully discharged before turning on using ZVS inductor currents. This means soft-switching is achieved for both inverters in the multi-level topology. Figure 5-7 shows the stepped output voltage of the inverter with 6 ns rise and fall time at each transition.

5.4.1 Multi-MHz Multi-Level Inverter Harmonic Content

In this section, harmonic analysis is performed on the stepped waveform output voltage of the multi-level inverter presented in Figure 5-7. The analysis is carried out for 1st, 3rd, and 5th harmonics, and the results are then normalized over the 1st harmonic amplitude. A comparison is then demonstrated in Figure 5-8 between the normalized harmonic content of the output voltage of the multi-level inverter and the normalized data obtained in Section 4.5 for the FB

Class-D inverter. Figure 5-8 shows that the level of the 3rd and 5th harmonics are considerably lower on the output voltage of the multi-level inverter compared to the FB Class-D inverter. The lower amplitudes of the 3rd and 5th harmonics on the stepped output voltage of the multi-level inverter imply that a resonant filter with much lower Quality (Q) factor or even a low pass filter can be utilized to suppress unwanted harmonics, compared to the FB inverter that needs a more complex output filter. As a result, the analysis presented in this section confirms how it would be easier to design the output filter to meet EMC requirements using a multi-level inverter as opposed to FB Class-D topology discussed in Chapter 4.

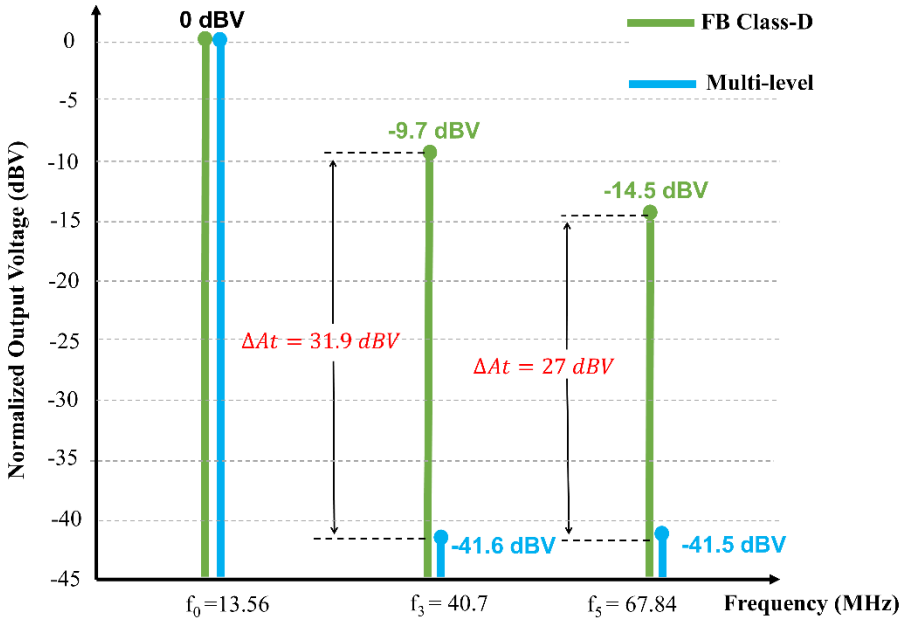

Figure 5-8: Comparing normalized harmonic analysis on the output voltage between multi-level and FB Class-D inverters

5.4.2 Multi-Level Inverter Output Power Control Using DDTC

In this section, the inverter is loaded with a 25Ω resistive load and the output power is regulated from 10% of the nominal output power (50W) to full load, in 5 steps. The optimum value for DT at different V_{DC} levels to achieve ZVS is determined based on the approach explained in Sections 3.5 and 4.4 which correlates the soft-switching of the inverter to the lowest ringing on the switch-node voltage and minimum no-load power consumption. Using this approach and changing V_{DC} from 0 to 45 V, DT values for ZVS are determined and the results are presented in Figure 5-9.

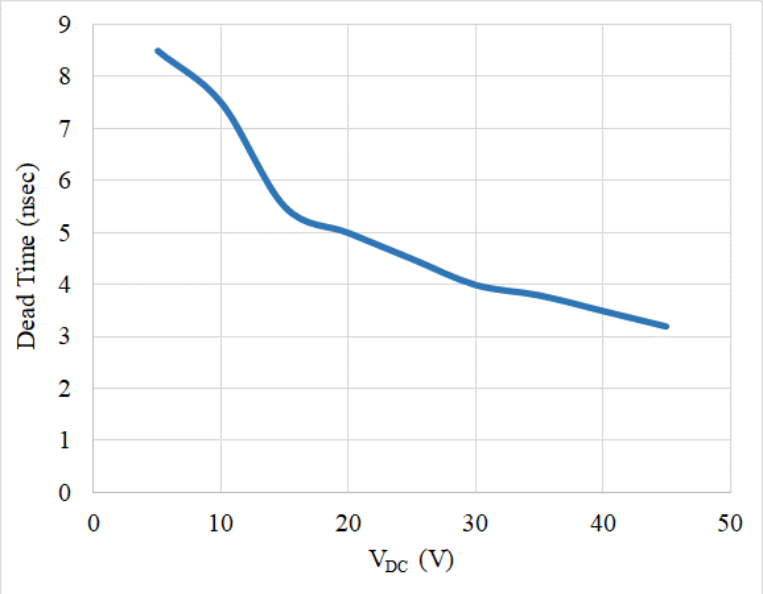

Figure 5-9: DT variation at different V_{DC} levels for soft-switching

The parameters of the multi-level inverter need to be calculated for DDTC to achieve proper soft-switching, the highest level of harmonic elimination, and accurate output voltage level during output power regulation. The first step is to initialize m and α with a proper start point value. Assuming that DT is going to change over the entire range, the best starting point would be the average of the values shown in Figure 5-3, resulting in $m_0 = 0.5$ and $\alpha_0 = 40°$. Then,

knowing the output power and the attached load, the load voltage v_L can be determined. Assuming that the multi-level inverter is eliminating the unwanted 3rd and 5th harmonic and the rest of the harmonics are also suppressed to a very low level, v_L can be considered equal to the 1st harmonic of the inverter output voltage v_{o1}. Using the formulation provided in Section 5.2 for ideal stepped waveform without the DT, the initial value of DC supply (V_{DD0}) can now be initialized using Equation 5-2 by substituting values calculated for v_{o1}, m_0, and α_0. Initial values for the two DC supplies, V_{DC10} and V_{DC20} can now be derived using Equation 5-15. DT value is specified at this stage using Figure 5-9 based on V_{DC10} and V_{DC2} levels. As V_{DC1} and V_{DC2} are not going to change considerably during the updates considering the entire range of m shown in Figure 5-3, DT is not updated after the initial assignment and is treated as a fixed parameter in determining the rest of the parameters. To achieve zero 3rd and 5th harmonics, m and α can now be updated by setting Equation 5-13 and Equation 5-14 to zero and solving the resultant two equations. DT, v_{o1} and the updated m and α are then inserted in Equation 5-12 to update V_{DD}. The final values for V_{DC1} and V_{DC2} are then determined using Equation 5-15 for the fine-tuning of the output voltage. The complete algorithm for multi-level inverter parameter selection is demonstrated in Figure 5-10. Using this algorithm, the multi-level inverter parameters for simulating output voltage regulation using DDTC are derived and the values are presented in Table 5-3 at different output power levels.

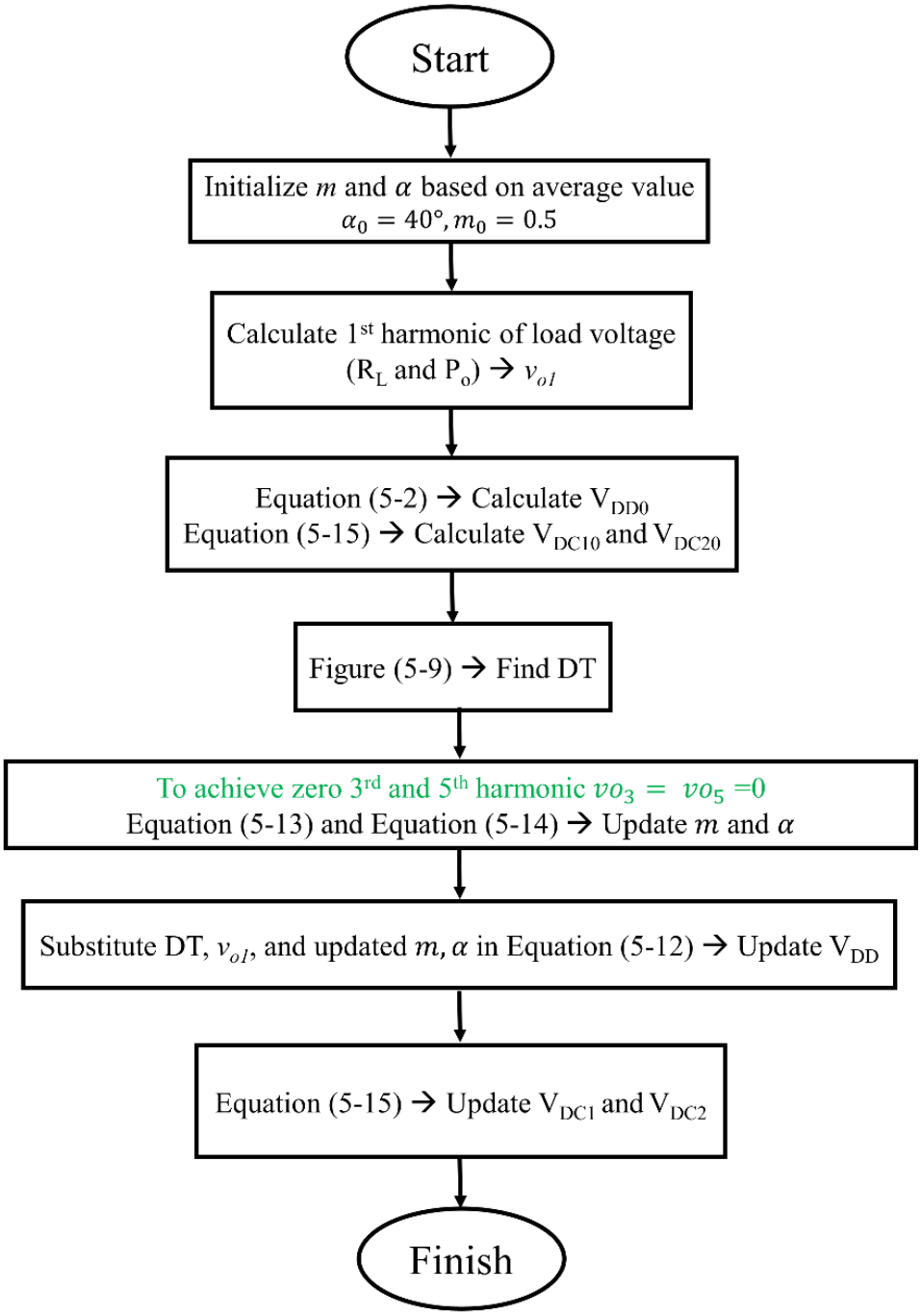

Figure 5-10: Multi-level inverter output voltage regulation algorithm using DDTC

Table 5-3: Simulation parameters of the multi-level inverter for output voltage regulation using DDTC, nominal output power ($P_{o\text{-}Nom}$) = 50W, R_L = 25Ω

Output power (W)	DT (ns)	*m* (V/V)	α (degree)	V_{DC1} (V)	V_{DC2} (V)
10% $P_{o\text{-}Nom}$	8.0	0.65	37.3	10.2	5.4
25% $P_{o\text{-}Nom}$	6.5	0.56	35.2	13.8	10.4
50% $P_{o\text{-}Nom}$	5.5	0.52	35.5	17.8	16.2
75% $P_{o\text{-}Nom}$	5.0	0.50	35.8	20.9	20.7
$P_{o\text{-}Nom}$	4.5	0.48	36.4	23.2	24.6

The multi-level inverter is simulated with parameters presented in Table 5-3 and the inverter output voltage (v_o) waveforms at different output power levels are presented in Figure 5-11. Harmonic analysis is then carried out on v_o at different output power levels to investigate the inverter's ability to eliminate unwanted harmonics. The results of the harmonic analysis carried out are presented in Figure 5-12. The results shown in this figure confirm that the algorithm presented in this section for calculating the inverter's parameter is valid, as the average level of 3rd and 5th harmonics at all different output power levels is at least 38.9 dBV lower than the level of the 1st harmonic. This frequency response will give much more flexibility in the design of the output EMI filter and help to reduce the size of the filter, considerably.

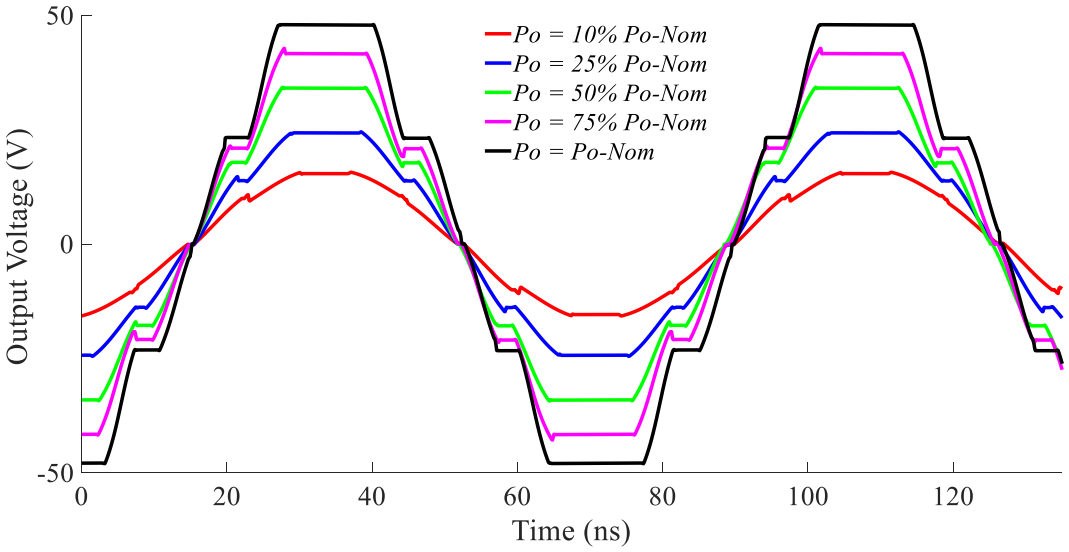

Figure 5-11: Multi-level inverter output voltage regulation with DDTC

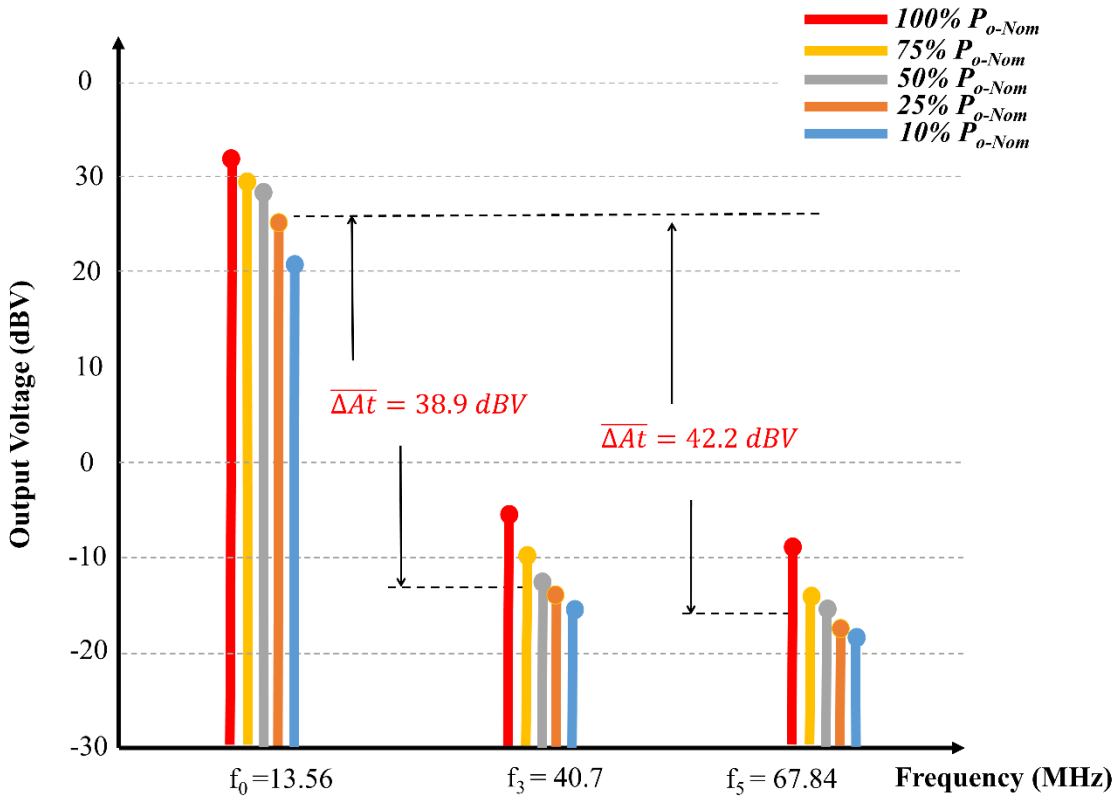

Figure 5-12: Multi-level inverter output voltage harmonic analysis during output power regulation

In this part, the loading effect on the soft-switching of the multi-level inverter is examined closely by demonstrating the drain-source current waveforms of two series switches from each inverter. These waveforms are shown in Figure 5-13. As the two Class-D inverters used in the multi-level topology have dedicated ZVS tanks, their operation from the soft-switching perspective is independent of each other. As a result, the same approach deployed in Section 3.5.1 to determine the soft-switching of the FB Class-D inverter from the current spike and the switch-node voltage ringing can be applied to the inverters in this section.

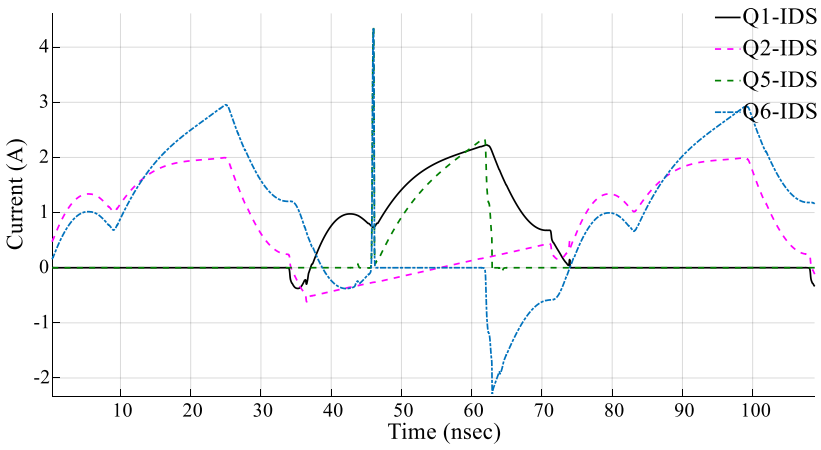

Figure 5-13: Drain-source currents of the switches at full load ($P_{o\text{-}Nom}$)

Figure 5-13 shows that the ZVS performance of Inverter I is not affected by the loading; as there is no spike on the Q_1 and Q_2 drain-source currents. However, to some extent, Inverter II loses the soft transition during turn on, as demonstrated by the current spike shown in Figure 5-13 at t = 45 ns. The current spikes of switch Q_5 and Q_6 in this figure indicate that Inverter II experiences some switching loss which is related to different load sharing percentages between the inverters. However, the current spikes and related time intervals are still well within the maximum tolerable electrical characteristics of EPC8009 ($I_{pulsedMax}$=7.5 A,

T_{pulse}=300 µsec). As the multi-level inverter consists of two Class-D inverters operating independently with dedicated ZVS tanks, the effect of capacitive and inductive load on the soft-switching follows the same pattern explained in Section 3.5.2. As a result, the simulation waveforms for these types of loads are not demonstrated in this section to avoid unnecessary duplication.

5.5 Practical Implementation

A system block diagram is proposed in Figure 5-14 for hardware implementation of a multi-MHz multi-level inverter.

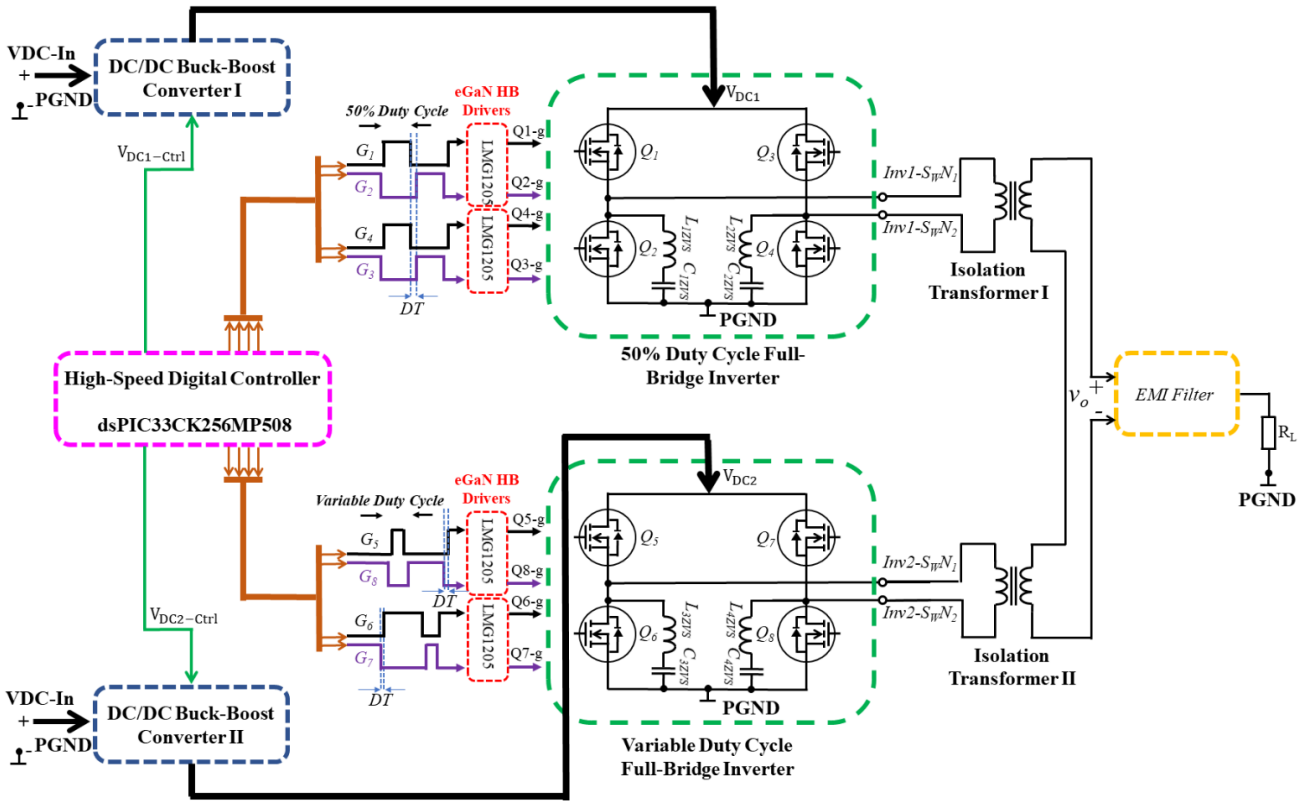

Figure 5-14: Multi-MHz multi-level inverter hardware block diagram

The system is composed of two DC-DC buck-boost converters to provide two separate sources of controlled DC voltages; two FB Class-D inverters to operate with different duty cycles; two isolation transformers to add up the differential switch-node signals; a dsPIC controller to control the DC-DC converters and provide phase-shift and duty cycle controllable gate signals to the inverters; output EMI filter to eliminate high-frequency harmonics; and RF load. The load is single-ended as the isolation transformer is utilized between the inverter and EMI filter.

5.5.1 PCB Layout of the Multi-MHz Multi-Level Inverter

A 6-layer PCB is built for the purpose of practical implementation of this system. Figure 5-15 shows the fully populated PCB with the different blocks highlighted.

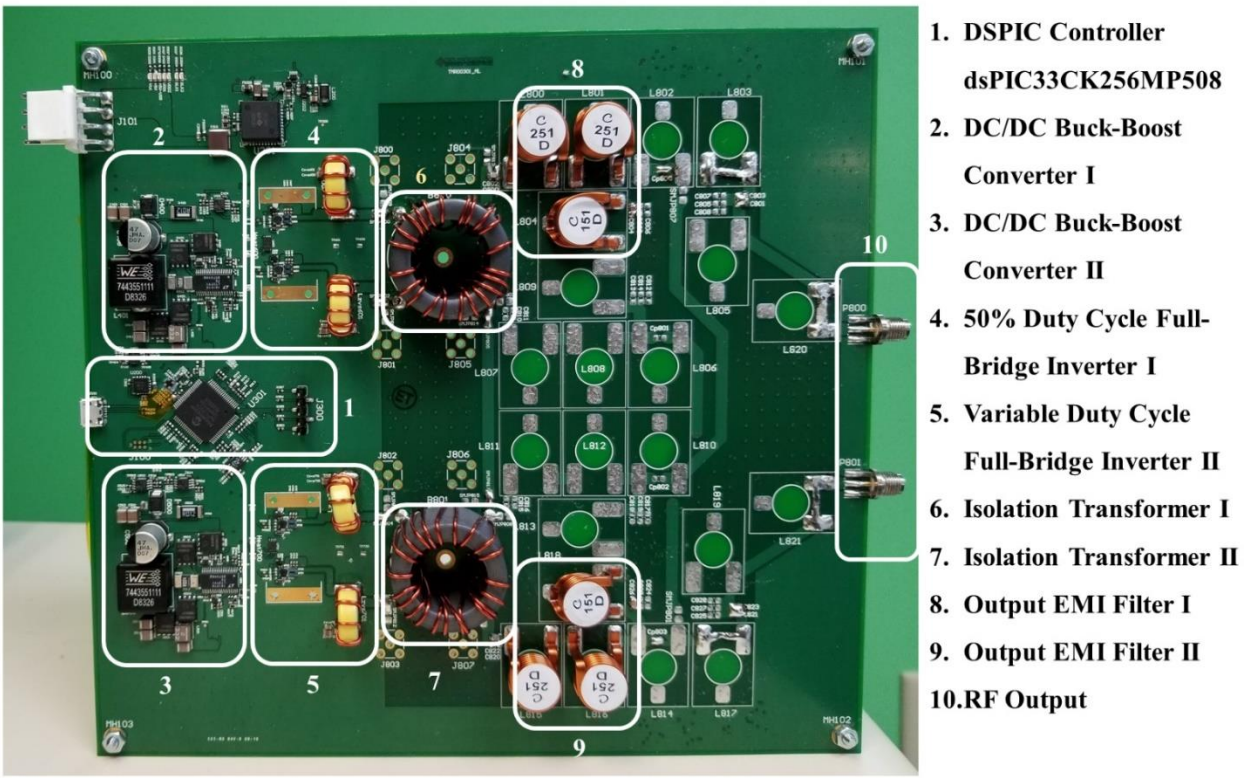

Figure 5-15: Multi-level prototype PCB implementation, 204 mm × 189 mm

The same design practice explained in Section 4.4 to achieve low CSI and a very small power loop is deployed here in the design of the PCB layout of both Class-D inverters. As the size of the PCB is relatively large at 13.56 MHz switching frequency, an attempt is made to match the transmission line impedance with the output load from the switch-nodes to the output connectors. Considering the two inverters as two single-ended power sources terminated to half of the output load ($R_L/2$), both transmission lines are designed to match to 12.5 Ω for the entire path by proper selection of trace width and the thickness of the dielectric between the top layer and first internal layer.

Except for the high-frequency isolated transformers, all the other blocks of the system presented in Figure 5-15 performed as expected according to the simulation and design specifications. The operational issues of the isolation transformers are explained in Section 5.6.

5.5.2 Experimental Results

In this section, the multi-level inverter is tested at no-load and without the output EMI filter. The reason is related to the operational issues of the isolation transformers which will be discussed in Section 5.6 in detail. The test setup used for the system verification is presented in Figure 5-16.

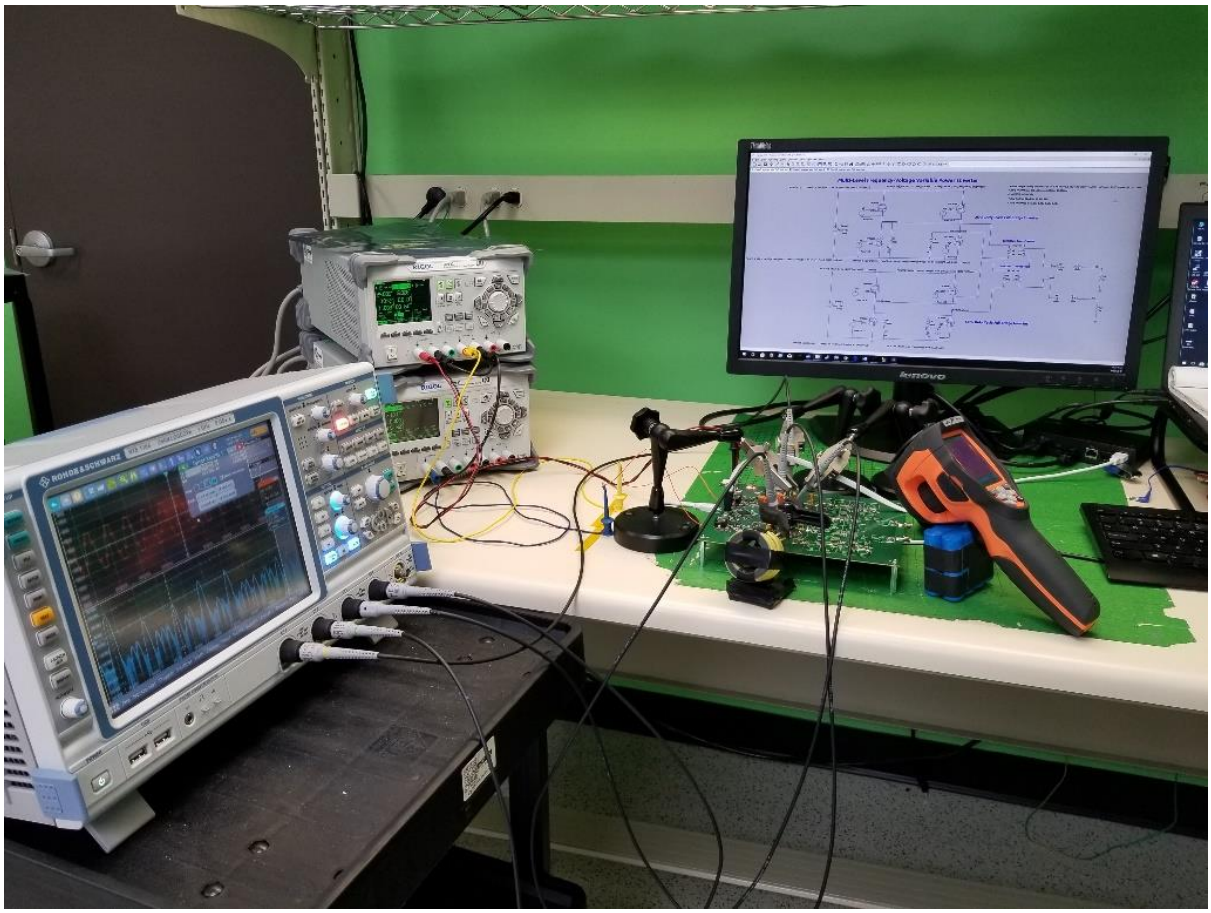

Figure 5-16: Multi-level inverter experimental setup

The voltage probes used for measuring the switch-nodes waveforms and transformer output voltage have 500 MHz bandwidth to provide more accurate measurements for harmonic analysis. The PC is used to send high-level commands to the dsPIC to control the DC voltage levels and gate signals' duty cycles and phase shifts. Figure 5-17 shows the switch-nodes of the multi-level inverter with values of m and α as provided in Table 5-1.

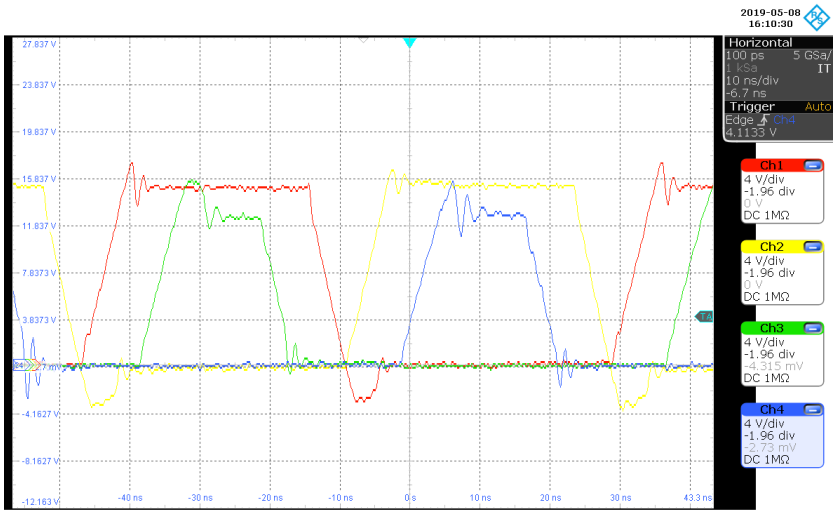

Figure 5-17: Multi-level inverter individual Switch-nodes, m = 0.54, α = 35.32°, V_{DC1} = 15V, and V_{DC2} = 12.6V

The stepped waveform of the output voltage of the transformer and related harmonic analysis are shown in Figure 5-18.

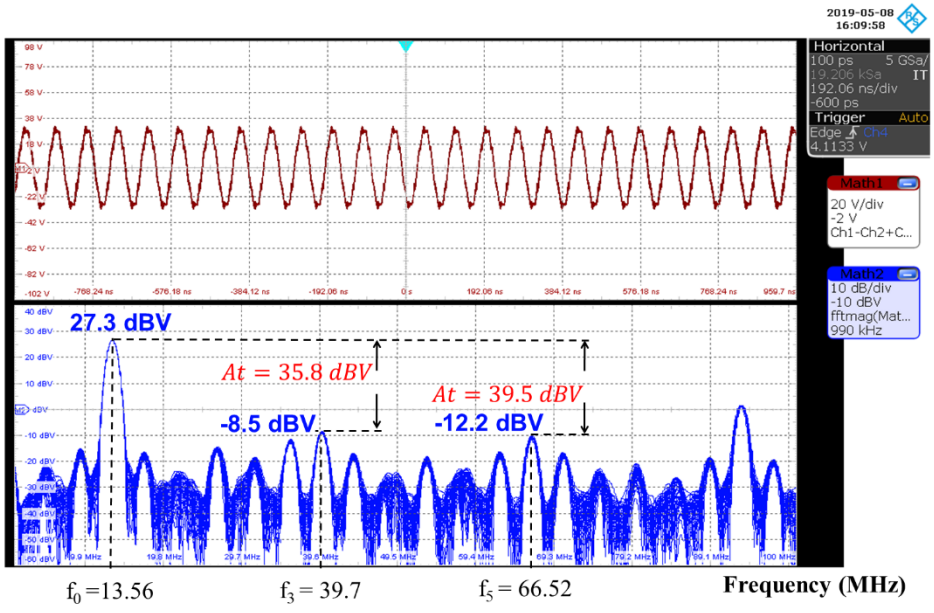

Figure 5-18: Multi-level inverter output voltage waveform and harmonic analysis

Figure 5-18 shows that the level of both 3rd and 5th harmonics are significantly reduced as expected, based on the theoretical analysis and simulation results presented in Section 5.2 and Section 5.4. The normalized harmonic content of the output voltage of the multi-level inverter shown in Figure 5-18 are compared with the normalized results obtained in Section 4.5 for FB Class-D inverter, and the results are shown in Figure 5-19.

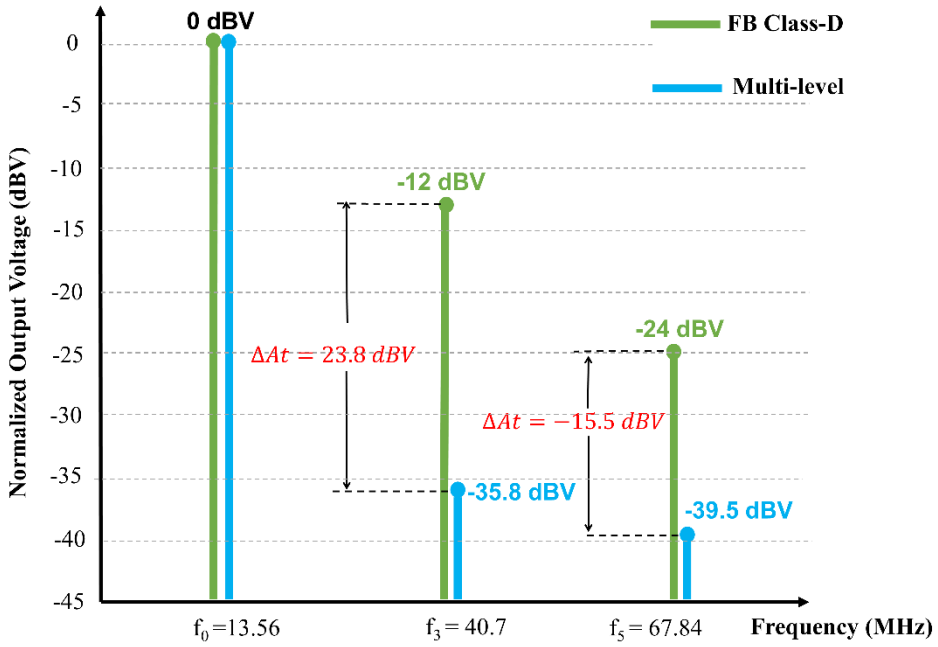

Figure 5-19: Normalized output voltage harmonic comparison between multi-level and FB Class-D inverter using experimental results

Figure 5-19 shows that the suppression capability of the multi-level inverter at 3rd and 5th harmonic of the output voltage is 23.8 dBV and 15.5 dBV higher than FB Class-D inverter.

5.6 Multi-MHz Isolation Transformer Design Issues

In this section, the issues related to the design of a multi-MHz isolation transformer are discussed. The core used in this design is the Material 67 from Fair-rite company. The relative permeability of this material is 40 and it is designed to have very low core loss at applications in tens of MHz. The core characteristics provided by the manufacturer show that the core loss will remain in an acceptable range while being used in multi-MHz applications as long as the magnetic flux stays below the saturation level. Figure 5-20 shows the Smith Chart of the impedance measurement of the transformer with a frequency sweep from 1 MHz to 500 MHz and a 50 Ω load.

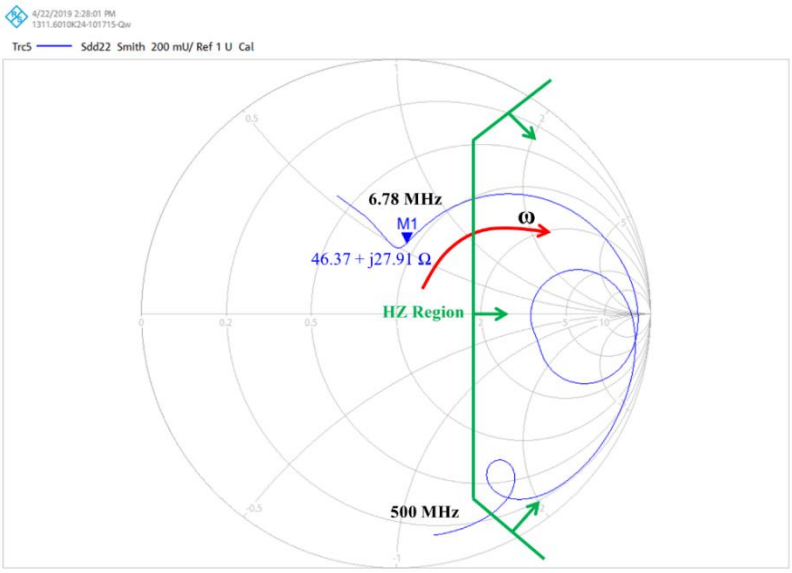

Figure 5-20: Transformer input impedance on Smith Chart, secondary winding loaded with 50Ω

The impedance Smith Chart provided in Figure 5-20 shows that the transformer has an acceptable inductive impedance level at 6.78 MHz which stays in the acceptable range up to 20 MHz. The impedance increases with increasing frequency, demonstrating an acceptable behavior as it acts more or less like a filter. The analysis carried out on the design of the

transformer before the final PCB implementation was with the transformer loaded with 50 Ω load. When the board was built and populated with all the blocks, including the isolation transformers, it was noticed that the transformer performance was not as expected according to the impedance analysis. The voltage waveform on the output of the transformer had a large amplitude oscillation at about 66 MHz undamped frequency. After more careful consideration, it was realized that the frequency analysis of the transformer with a fixed load does not represent the practical scenario when the transformer is connected to the fixed load through the output EMI filter. The EMI filter block attached to the secondary side of the transformer presents a 50 Ω load to the transformer at resonant frequency but it transforms the load to an almost open circuit at all higher frequencies. As a result, a new impedance analysis was carried out to observe the impedance characteristic of the transformer while it is open-circuited or loaded with very high impedance at frequencies higher than the resonant frequency. The Smith Chart of this analysis obtained from Rohde and Schwarz VNA is presented in Figure 5-21.

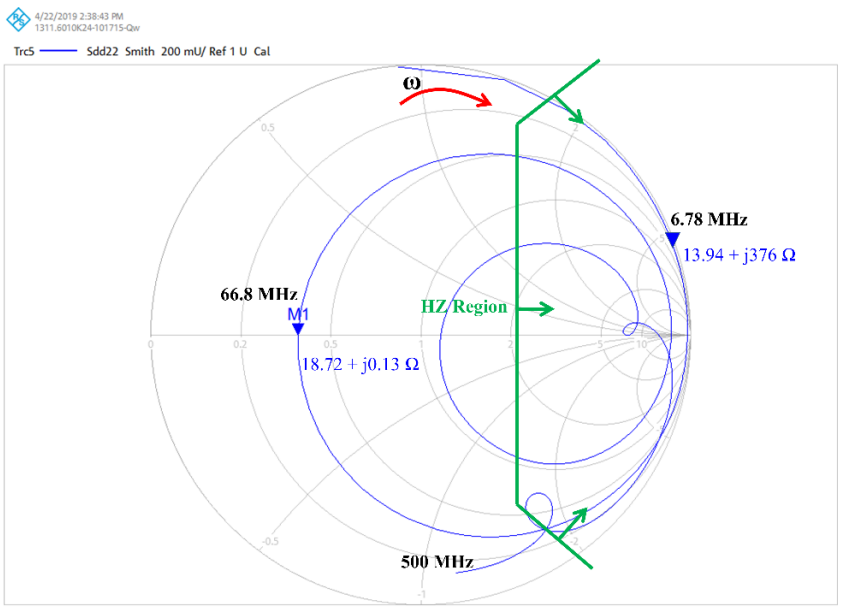

Figure 5-21: Transformer input impedance on Smith Chart, secondary winding open-circuited

Figure 5-21 shows that when the transformer is presented with a large impedance on its secondary side, it starts to self-resonate at 66.8 MHz which is the resonant frequency between the leakage inductance and inter-winding capacitance of the transformer winding. A more accurate model of the transformer was then developed to incorporate all the parasitic components. A simulation was then carried out using the detail transformer model attached to a Class-D inverter on the primary side and an output EMI filter and load on the secondary side. The circuit diagram of the detailed model developed in this section is presented in Figure 5-22. The parameters of the detailed model of the transformer can be determined using short circuit and open circuit tests, and oscillation analysis. These parameters are measured on the isolation transformer built for the multi-level inverter prototype shown in Figure 5-1, and the measurement results are presented in Table 5-4.

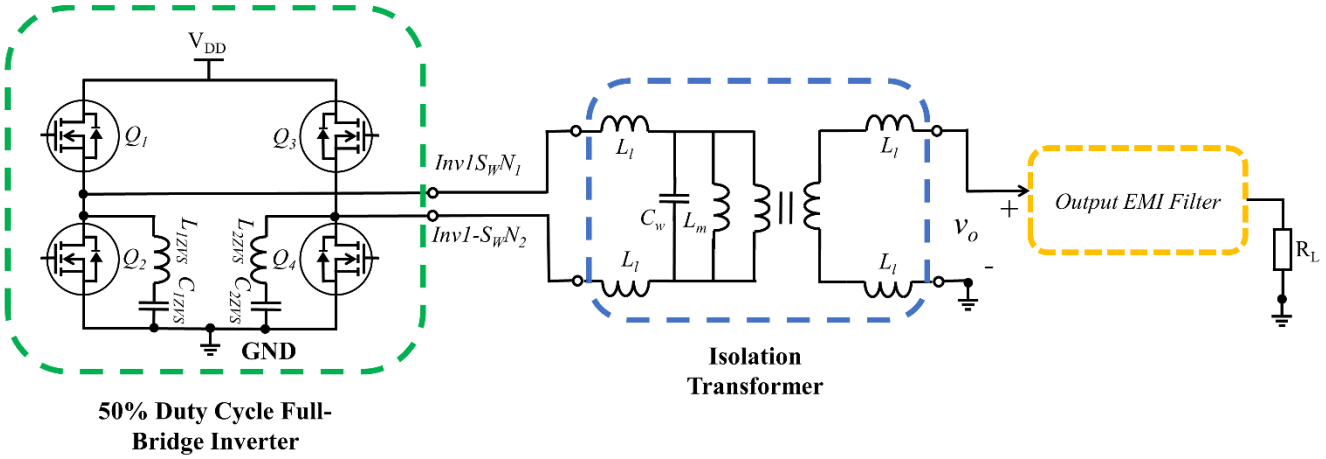

Figure 5-22: Isolation transformer detailed circuit modeling with parasitic components

Table 5-4: Isolation transformer electrical characteristic, material 67, toroid 7967001801, relative permeability (μ_r) = 40, diameter = 22.1 mm

Description	Parameter	Value	Comment
Leakage inductance	L_l	100 nH	Measured using the short-circuit test
Magnetizing inductance	L_m	8.5 µH	Measured using the open-circuit test
Inter-winding capacitance	C_w	28.3 pF	Measured using self-resonant frequency at 66.8 MHz (Figure 5-21)

The simulated waveforms of the output voltage (v_o) of the transformer with and without the effect of the EMI filter are presented in Figure 5-23.

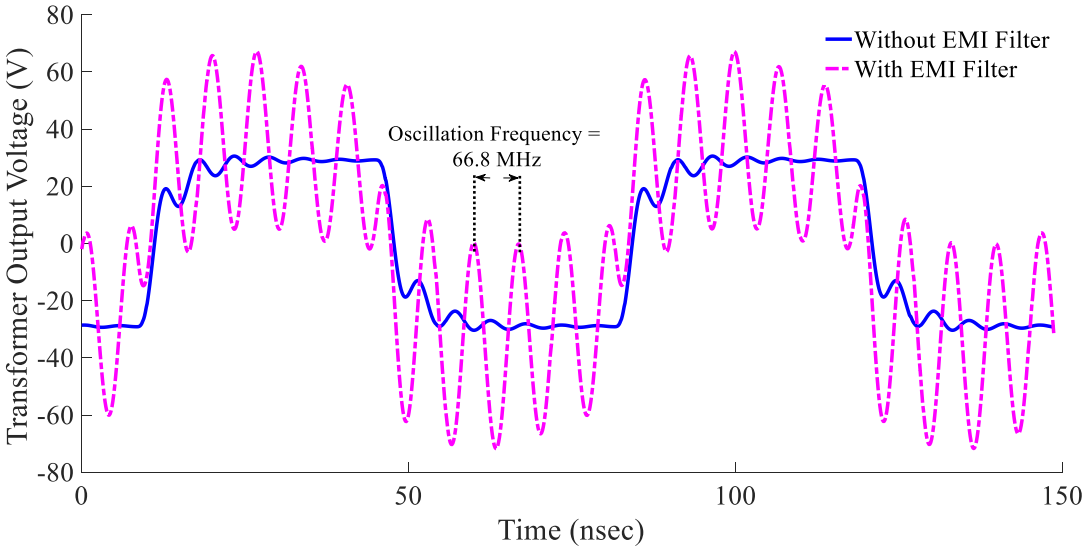

Figure 5-23: Simulating EMI filter impact on the isolation transformer output voltage (v_o) waveform using the transformer detailed model

The waveform presented in Figure 5-23 shows how the output EMI filter impedance transformation results in large oscillation on the output voltage of the transformer which is related to the frequency response of the transformer at no-load. The above analysis of the

issues related to the isolation transformer at muti-MHz operation requires detailed and further investigation. This was considered beyond the scope of the work and explains why the experimental results were performed for the no-load case.

5.7 Summary

In this chapter, after introducing the importance of harmonic suppression for achieving acceptable EMC performance, a mathematical analysis is presented for an ideal stepped waveform which can theoretically have zero levels at 3^{rd} and 5^{th} harmonics. Switching converters are not ideal and their output waveforms always suffer from these nonidealities. One of these nonideal conditions in switching converters is the effect of DT on the switch-node voltage. Therefore, this effect on a stepped waveform is addressed next, and new mathematical analysis and formulation are provided to achieve unwanted harmonic elimination. An analysis is also done in this section to demonstrate the relationship between the modulation parameters of the stepped waveform and DT. A circuit diagram for a multi-level inverter is then proposed to create the stepped waveform voltage on the output at 13.56 MHz. Simulation is then carried out in LTSpice using the multi-level inverter circuit model, and soft-switching, harmonic elimination capability, and output power regulation using DDTC are investigated through simulation results. A prototype of the multi-level inverter is then built, and the system is experimentally tested to validate the simulation results. The experimental switch-node waveforms obtained from the multi-level inverter prototype are demonstrated to show the soft-switching performance of the inverter. The multi-level inverter capability for harmonic elimination is finally compared with that of the FB Class-D inverter.

The last section of this chapter addresses the practical issues of designing an isolation transformer at multi-MHz frequency. A detailed model is developed using the experimental measurements to simulate and analyze the behavior of the transformer while an EMI filter is attached to the output.

CHAPTER 6

6 Conclusion and Future Works

6.1 Conclusions

The imminent need for transferring power wirelessly is bringing more resources to research in WPT systems and pushing the technology forward to make these systems cheaper, compact, reliable, safer, and more efficient. WPT systems are designed to operate at high frequency (hundreds of KHz, and multi-MHz) as this reduces the size of their transmitter and receiver electrodes and increases the physical range of their operation. As a result, the first challenge in developing these systems is to design efficient high-frequency DC/AC power inverters that can be used in the transmitter block. The high-efficiency power inverter makes it easier for the WPT system to meet the overall efficiency required for a power module.

Performance of the power inverter from the EMC perspective is the second challenge that determines if the inverter is suitable to be used in a WPT system. The EMI noise or the unwanted harmonics coming out of a power inverter finally find their way to radiate through the wireless link. A safe WPT system needs to pass EMC regulation, meaning that the harmonic contents of the output voltage of the power inverter need to be lower than a certain level.

In this research, after providing a short overview of different inverter topologies and switching devices suitable to operate at the multi-MHz switching frequency, the design and development of two different Class-D based multi-MHz inverters that can be utilized on the transmitter of a WPT system are addressed.

In the first step, a soft-switching FB Class-D inverter is simulated and the challenges of sustaining soft-switching during output power regulation are explained using behavioral analysis and simulation. Then, Dynamic Dead-Time Control (DDTC) approach is proposed to sustain soft-switching while controlling the output power. After presenting simulation results for the proposed approach, the experimental results obtained from a 13.56 MHz FB Class-D inverter prototype that is built for this purpose are presented to validate the theoretical assumption and simulation results. The experimental results prove that dynamically controlling the DT using the circuit proposed in this research can increase the overall efficiency of the inverter, reduce the temperature of the components and PCB, and reduce the voltage ringing on the switch-node waveforms. In the last part of this chapter, harmonic analysis is carried out to show that the high level of 3^{rd} and 5^{th} harmonic that exist on the output voltage of the FB Class-D inverter makes it inevitable to use a high-order or High-Quality (HQ) filter to meet EMC.

In the last chapter of this study, a multi-MHz multi-level inverter is developed that can eliminate the unwanted harmonics of the output voltage to a considerably lower level than the FB Class-D inverter. A mathematical analysis is carried out in the first step to show how a stepped waveform can have zero level on the 3^{rd} and 5^{th} harmonic of its fundamental frequency. As the DT in multi-MHz switching frequency covers an important portion of the switching cycle, a mathematical formulation that includes the effects of the DT on the modulation parameters of the stepped waveform is provided. Then, a set of modulation parameters is calculated for the stepped waveform at different DT values which can maintain zero levels of the unwanted 3^{rd} and 5^{th} harmonics. After introducing an inverter topology capable of making the stepped waveform on its output, the most practical DT value and related values of modulation parameters are used to simulate the inverter in LTSpice software. A full simulation is carried out to cover harmonic analysis and output power regulation of the multi-level inverter using DDTC, and the results are presented. A prototype PCB is then built and used for practical verification of the idea. Harmonic analysis is carried out on the experimental results obtained from the prototype in the next step. It is shown using the experimental results that the multi-level inverter can suppress the 3^{rd} and 5^{th} harmonics to much lower levels compared to FB Class-D inverter. This will, in turn, simplify the design of the output filter needed to meet EMC from a HQ resonant filter to a resonant filter with a much lower quality factor or even to a low pass filter. Finally, the design issues of the isolation transformer are addressed, and a detailed model for the multi-MHz isolation transformer is developed to explain the practical issues observed during the practical tests.

6.2 Contributions of the Thesis

This research provides an overview of different types of WPT systems, and the challenges that need to be overcome to design multi-MHz power inverters that are capable of operating efficiently and with the least amount of harmonic in these systems. Two inverter topologies that can be used for this purpose are addressed and their performance is compared. Also, different families of the switches which can be used in the design of the multi-MHz inverters are covered.

Behavioral analysis, mathematical formulation, and comprehensive simulation of a 13.56 MHz FB Class-D inverter is provided in this research paving the road for the development section. The first important contribution of this work is proposing and experimentally developing the DDTC approach for sustaining the soft-switching of a multi-MHz Class-D inverter during output power control. The simulation analysis and experimental results obtained from the inverter prototype are essentially presented for the first time in the field of multi-MHz power inverters

The second important contribution of this thesis is presented in Chapter 5. The detailed mathematical analysis of a stepped waveform including the effect of DT on the modulation parameters is fully addressed for the first time in the literature. The multi-MHz multi-level inverter PCB prototype is one-of-a-kind that is built during this research. The experimental results obtained from this prototype provide valuable insight into the practical feasibility of harmonic elimination in multi-MHz multi-level inverter designs.

6.3 Future Works

The next step that can be considered as a continuation of this work is to increase the power density of the existing multi-MHz FB Class-D and multi-level inverter by going to higher switching frequency bands, i.e., 27.12 and 40.68 MHz. Although increasing the frequency will increase the switching loss and make the hardware design much more challenging, the higher switching frequency reduces the amount of inductance needed in the filtering stage to achieve the same filter quality factor. The most important challenges in going to these higher switching frequencies, however, are designing a low loss gate driver and bootstrap circuits for the top switches of the Class-D topology, and appropriately dealing with high-frequency core loss of the inductors.

Another interesting future topic related to the multi-MHz multi-level inverter is to utilize isolated DC-DC converter and have the inverter blocks operating on isolated system grounds. This helps to avoid the challenges regarding the design of isolation multi-MHz transformer explained in Section 5.6 and, instead, designing isolation transformers at much lower switching frequencies (i.e. KHz) for the isolated DC-DC converters.

The next topic that can be considered in this field is the analysis and design of different EMI filter topologies that can be used exclusively on the output of multi-MHz inverters that are operating in the transmitter of WPT systems to achieve higher power density. Studying different filter topology, providing mathematical analysis, doing research on the component selection specifically the inductors, and proposing an optimized solution based on size and performance would have a great value in this field.

Another interesting topic in this filed is designing a multi-MHz inverter capable of handling a broad range of resistive, capacitive, and inductive loads. The system basically can consist of two internal inverters connected in parallel and controlled through their phase shift and individual input DC voltage. Soft-switching of the inverters, high-frequency instrumentation, load detection circuits, and the closed-loop control stability of the entire system are among the topics that can be investigated in this area, as well.

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8 Papers During the Ph.D. Program

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