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Chapter

Tunnel Field Effect Transistors Based on Two-Dimensional Material Van-der-Waals Heterostructures

Jiang Cao

Abstract

The successful isolation of graphene in 2004 has attracted great interest to search for potential applications of this unique material and other newborn members of the two-dimensional (2-D) family in electronics, optoelectronics, spintronics and other fields. Compared to graphene, the 2-D transition metal dichalcogenides (TMDs) have the advantage of being semiconductors, which would allow their use for logic devices. In the past decade, significant developments have been made in this area, where opportunities and challenges co-exist. Stacking different 2-D materials significantly increases the already considerable design space, especially when a type-II band alignment is obtained. This chapter will describe the recent progresses in the tunnel field-effect transistors based on 2-D TMD van-der-Waals heterostructure, which is one of the promising candidates for increasingly important low-power mobile computation applications. Due to their small size, such devices are intrinsically dominated by quantum effects. This requires the adoption of a fairly general theory of transport, such as the nonequilibrium Green's functions (NEGF) formalism, which is a method having been more-and-more used for the simulation of electron transport in nanostructures in recent years.

Keywords: two-dimensional material, van-der-Waals heterostructure, tunnel field-effect transistor, steep-slope switch, subthreshold swing

1. Introduction

The invention of the transistor in 1948 is arguably the major technological break-through of the twentieth century. The transistors are the building blocks of today's microprocessors and computers that are everywhere around us. Nowadays, billions of transistors are integrated into a microchip of only a square centimeter. Since the Nobel prize attributed to Shockley, Brattain and Bardeen in the 1956, and the invention of integrated circuits in the same decade, considerable efforts have been put to keep miniaturizing the metal oxide semiconductor field effect transistors (MOSFETs). A conventional MOSFET structure with descriptions of its working principle are shown in **Figure 1**. From one technology node to the next, MOSFETs are conceived to be smaller (following Moore's law), faster and less

power consuming. Thirty years of aggressive scaling have pushed the device dimensions close to the atomic range. The downscaling of MOSFETs has slowed down since the 65 nm node was reached. Issues related to the nanoscale dimensions of the devices started arising.

When the channel length is decreased below 1 μm, additional problems appear and are commonly called short-channel effects (SCEs). The SCEs for the MOSFETs are important when the channel length becomes comparable to the width of the depletion region. When the gate length is scaled down, the gate starts to lose the electrostatic control over the channel. On the other hand the source-drain bias (V_{DS}) gains a larger influence on the barrier. Such an effect is named drain-induced barrier lowering (DIBL). This loss of electrostatic integrity leads to a continue increase of the current and decrease of the off-state potential.

Moreover, the electron mobility is reduced due to collisions with the semiconductor/oxide interface. This surface scattering effect is enhanced by the increase of electric field in the confined regions, which pushes the electrons toward the surface of the device. The reduction of electron mobility is also caused by the necessity of using high doping levels in such scaled MOSFET. Finally, the average velocity of carriers is no longer linearly depend on the electric field in such small devices, which is called the velocity saturation.

The drawbacks of traditional bulk planar transistors have promoted the search for new architectures alternative to MOSFETs. The International Technology Roadmap for Semiconductors (ITRS) [1], which evaluates the technology requirements for the next-generation semiconductor device technology, predicts that additional new materials and transistor geometries will be needed to successfully address the formidable challenges of transistor scaling in the next 15 years. In **Table 1**, some main figures of merit extracted from the ITRS for the short- (2018) and long-term (2026) technologies, both for high-performance and low-power applications, are shown. Since the late 90s, it has been suggested to replace single-gate transistors by multi-gate structures in order to enhance the electrostatic control of the gate. Intel has already switched to the TriGate FET, also known as the FinFET, technology since the 22 nm node. Silicon-on-insulator has also been widely used to improve the performances of transistors, especially decreasing leakage currents [2].

To meet the requirements set by the ITRS for future nodes, scaling down the gate length is critical. The two-dimensional materials (2DMs) provide the ability to control the channel thickness at the atomic level, which will result in improved gate control over the channel and in reduced SCEs. In the next Section, I will discuss the properties of 2DMs and the 2DM van-der-Waals heterostructures (vdWHs) and their numerous possible applications in the electronic devices. Before that, let us
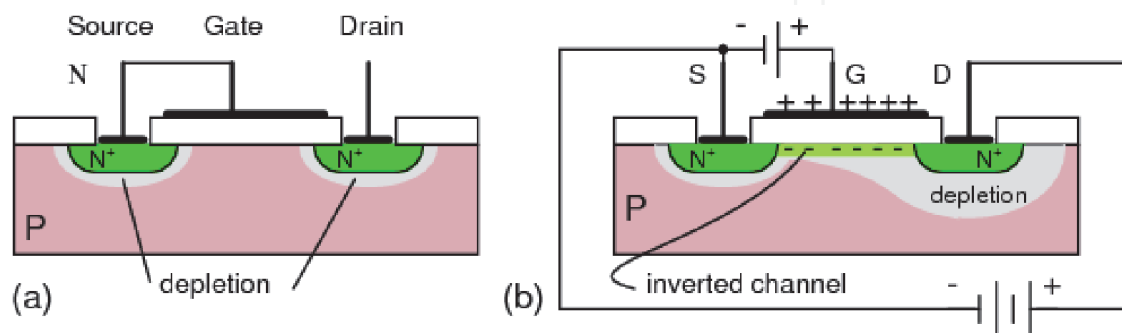

Figure 1.
Schematic cross-section of a N-channel MOSFET: (a) 0 V gate bias, (b) positive gate bias that charges the gate. The P-type substrate below the gate takes on a negative charge. An inversion region with an excess of electrons forms below the gate oxide. This region connects the source and drain N-type regions, forming a continuous N-region from source to drain.

	HP2018	LP2018	HP2026	LP2026
Channel length (nm)	10.2	11.7	4.9	5.6
V_{DD} (V)	0.78	0.78	0.66	0.66
I_{OFF} (nA/μm)	100	0.01	100	0.04
I_{ON} (μA/μm)	1610	556	1030	337
τ (ps)	0.488	1.564	0.432	1.514

Table 1.
Figures of merit extracted from ITRS [1] for the short- (2018) and long-term (2026) technologies, both for high-performance and low-power applications. V_{DD} is the supply voltage; I_{OFF} and I_{ON} are the drain currents per unit width in the off- and on-state; τ is the intrinsic delay time.

first look at the fundamental power consumption issues in the MOSFET and the FinFET technologies, then one of the promising technologies for solving this problem, namely the tunnel field effect transistors (TFETs).

2. Power consumption issues

Power consumption is a fundamental problem for nanoelectronic circuits. To give some examples, all the smartphones need to be recharged everyday; the data centers in the US used 91 billion kilowatt-hours of electricity in 2013. The power consumption in logic devices closely depends on the supply voltage (V_{DD}) through the following relation.

$$P = \underbrace{\alpha f_c C_L V_{DD}^2}_{\text{operating}} + \underbrace{I_{OFF} V_{DD}}_{\text{stand-by}}, \tag{1}$$

where α is called the activity factor, f_c denotes the clock frequency, C_L is the load capacitance (mostly gate and wire capacitance, but also drain and some source capacitances), and I_{OFF} is the off-state current. In the formula above, we can identify an operating and a stand-by power that both depend on V_{DD}. Lowering V_{DD} is thus necessary to decrease the consumption. However, a strong V_{DD} reduction significantly affects the performances of MOSFETs, as illustrated in **Figure 2(a)**. Indeed, the problem resides in the speed at which the transistor passes from the off- to the on-states as a function of the gate voltage. In the subthreshold regime of MOSFETs, the thermionic effect entails that at least 60 mV are necessary to increase the current by one order of magnitude at room temperature. In other words, the subthreshold swing (SS), i.e. the inverse of the derivative of the subthreshold slope

$$SS = \left(\frac{\partial \log_{10} I_{DS}}{\partial V_G} \right)^{-1}, \tag{2}$$

has a minimum value of

$$SS_{min} = \frac{k_B T}{e} \ln(10) = 60 \text{ mV/dec}, \tag{3}$$

where k_B is the Boltzmann constant, T is the temperature taken at 300 K and e is the absolute value of electron charge. If we keep the same on-current I_{ON} for the transistor while reducing V_{DD}, then I_{OFF} increases exponentially, see **Figure 2(a)**.
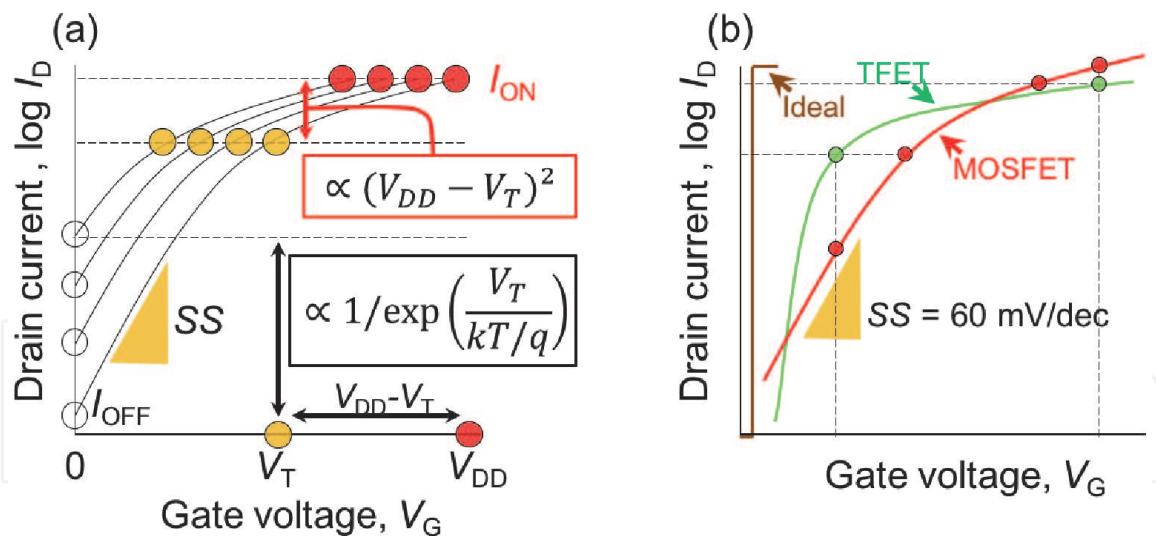
Figure 2.
(a) Transfer characteristics (drain current I_D vs. gate voltage V_G) of a MOSFET switch showing an exponential increase in I_{OFF} because of the thermionic limit of the subthreshold swing SS. Here the simultaneous scaling down of the supply voltage V_{DD} and the threshold voltage V_T, keeping the same I_{ON} by keeping the (V_{DD}-V_T) constant. (b) Qualitative comparison of the MOSFET switch (red) with a TFET (green) which has a steep off-on transition and a lower I_{OFF}. At low V_G, because of the subthermionic SS, the TFET offers a better performance and power reduction. At high V_G, the MOSFET switch becomes a better solution for higher performance thanks to the higher I_{ON}.

A possible way of reducing the voltage supply without performance loss is to increase the turn-on steepness, which means decreasing the average SS below the SS_{min}. Such devices, called steep-slope switches, are expected to effectively enable power scaling. Because of these MOSFET limitations, other device architectures are under active investigation, including the negative-capacitance FET (NC-FET) and the tunnel FETs (TFETs) [3].

3. Tunnel field-effect transistors

In contrast to MOSFETs, where charges are thermally injected over a potential barrier, the primary injection mechanism is band-to-band tunneling (BTBT), i.e. charge carriers transfer from one energy band into another. This tunneling mechanism was first identified by Zener in 1934 [4].

A typical TFET is composed of a p-i-n structure with a gated intrinsic region, see **Figure 3(a)**. Its working mechanism can be explained as follows. When a low voltage is applied to the gate, electrons tunneling from the valence band of the source to the conduction band of the drain is suppressed due to the gap in the intrinsic region, see **Figure 3(b)**. This is the off-state. When the potential applied to the gate brings the conduction band of the intrinsic limit at the same level as the source valence band, electrons can easily tunnel from source to drain, see **Figure 3(b)**. This is the on-state. In the ideal case, the transition from the off-state to the on-state is very fast, since the thermal tail of the injected electrons is cut by the top of the valence band in the source and the off-current is exponentially suppressed when the source Fermi level is within the gap of the intrinsic region. This would allow, in principle, very low SS, below SS_{min}, see **Figure 2(b)**.

Here, we briefly summarize the history of TFETs. The gated p-i-n structure was proposed in 1978 by Quinn et al. [5]. In 1992, Baba [6] fabricated TFETs called surface tunnel transistors in group III-V materials. In 1995, Reddick and Amaratunga [7] reported experiments on silicon surface tunnel transistors. In 2000, Hansch et al. [8] published experimental results on a reverse-biased vertical silicon
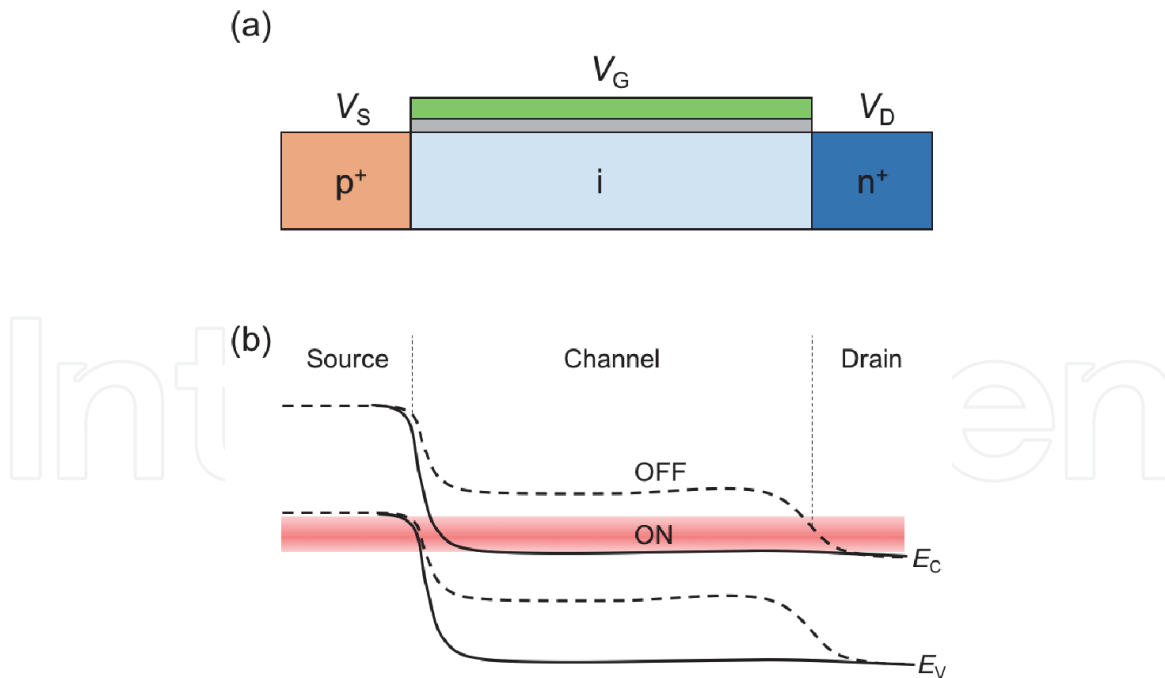
(a)

(b)

Figure 3.
(a) Schematic cross-section of n-type TFET with applied source (V_S), gate (V_G) and drain (V_D) voltages.
(b) Schematic energy band profile for the off-state (dashed lines) and the on-state (solid lines) in a n-type TFET.

TFET fabricated by molecular beam epitaxy. Aydin et al. [9] fabricated lateral TFETs on silicon-on-insulator in 2004. Recently, TFETs fabricated in various materials (carbon, silicon, SiGe and group III-V materials) have emerged experimentally as the most promising candidates for switches with ultralow standby power and sub-0.5 V supply voltage.

The goals for TFET optimization are to simultaneously achieve the highest possible I_{ON}, the lowest average SS over many orders of magnitude of drain current, and the lowest possible I_{OFF}. For TFETs, SS decreases with the gate voltage, therefore they are naturally optimized for low-voltage operation. To achieve a high tunneling current and a steep slope, the transmission probability of the tunneling barrier should pass from 0 to close to 1 for a small change in gate voltage around the threshold potential. This requires a strong modulation of the channel bands by the gate and a very thin channel barrier.

As mentioned above, there have already been many experimental attempts to build TFETs with bulk silicon and III-V group materials. Even though encouraging experimental results have been reported for the on-current and SS in Si- and III–V-based TFETs, these devices are very demanding in terms of gate control [10]. Moreover, their transfer characteristics can be seriously degraded by the presence of interface or bulk defects enabling inelastic trap-assisted tunneling in the OFF-state [11, 12].

The 2-D materials (2DMs) may overcome some of the above issues [13], and have great potential for TFETs, due to their scalability and absence of dangling bonds at interface. They can be stacked to form a new class of tunneling transistors based on an interlayer tunneling occurring in the direction normal to the plane of the 2DMs [14]. In the next Section, we will review the properties of various different 2DMs and their applications.

4. 2-D materials

For a long time, the 2-D materials were thought to be unstable [15]. In the first half of the last century, scientists predicted [16] that a 2DM would likely disintegrate at

finite temperature under the displacement of lattice atoms caused by thermal fluctuations. This theory was further supported by experiments observing that the melting temperature of thin film materials rapidly reduce with decreasing film thickness.

This belief remained unchanged until 2004, when Geim and Novoselov successfully isolated graphene by the mechanical exfoliation technique [17, 18]. Although there have been other independent reports of monolayer carbon materials isolation [19, 20], some even long before the reports from the Manchester group, the works in 2004 and 2005 unveiled the unusual electronic properties of graphene, thus generating an intensive research by physicists and chemists in the field of 2DMs and inspiring 2DMs-based nanoelectronics [21]. Since then, we have seen an exponential increase in the research activity in graphene and other 2DMs, such as the transition metal dichalcogenides (TMDs), hexagonal boron nitride (h-BN), black phosphorus, silicene and gemanene [22–25].

4.1 Electronic properties of graphene

In 1946, Wallace first calculated the band structure of graphene and showed uncommon semimetallic behavior in this, at that time imaginary, 2-D material [26]. Actually, Wallace's studies of graphene served him as a starting point to study graphite. Between 1957 and 1958, other works by McClure [27] and Slonczewski and Weiss [28] followed.

One of the most interesting aspects of the graphene is its low-energy band structure [21, 29], which is linear around the K and K' points of the Brillouin zone. In neutral graphene, the Fermi energy crosses exactly these points, which are also called Dirac points, because there electrons can be described by a 2-D Dirac Hamiltonian for massless fermions, except for the fact that in graphene the electrons move with a speed v_F, which is 300 times smaller than the speed of light, and that the spin degree of freedom in replaced by the so-called pseudospin degree of freedom corresponding to the two graphene sublattices. This determines the observation of very unconventional properties with respect to the usual 2-D electron gases (2DEGs) obtained in doped semiconductor heterostructures. For example, in the presence of a strong magnetic field, Landau levels form at both positive and negative energies (with respect to the Dirac points) at energies proportional to the square root of the magnetic field and of the level index. This gives rise to the anomalous integer quantum Hall effect [30, 31], which, compared to the case of 2DEGs, can be observed at relatively low magnetic field and high temperature, with interesting perspective applications in metrology [32]. The linear dispersion of the graphene energy bands also entails a very high electron mobility, up to 200,000 $cm^2/(Vs)$ at low temperature for suspended graphene [33].

Another interesting property of graphene is when laterally confined into nanoribbons, its electronic and transport properties are strongly affected by the geometry of the edges (armchair, zigzag or mixed) and the nature of their passivation. For example, under certain condition the ribbon can show a band gap, whose size is proportional to the inverse of the ribbon width. Such a gap might be important for applications in logic devices [34], which are however compromised by the huge mobility degradation due to the increase of the effective mass from one side, and the presence of edge roughness from the other.

4.2 Electronic properties of 2-D TMDs

Unlike traditional bulk semiconductors, such as Si and III-V group materials, 2-D TMDs have ultra thin thickness, no surface dangling bonds, and high flexibility,

which make them promising candidates [35] to solve the new challenges the semi-conductor industry is facing today, including short-channel effects, power dissipation, integration and flexible applications. Recently, one of the large research interests in the field of 2DMs is the understanding of the fundamental electronics properties.

MoS_2 is a typical and well-studied TMD material [36, 37]. Its layers consist of hexagons with the Mo and S atoms located at alternating corners. The most striking feature of bulk MoS_2 is that, compared to zero-bandgap graphene and insulating *h*-BN, it is a semiconductor with an indirect band gap of 1.29 eV [38]. Several studies have confirmed a transition from an indirect band gap to a direct band gap for MoS_2 as the thickness of bulk MoS_2 is decreased to that of a monolayer. Such a similar transition is also demonstrated for other TMD materials. Kuc et al. [39] performed an extended study of the influence of quantum confinement on the electronic structures of monolayer and few-layer MS_2 (M = W, Nb, Re) using first-principles calculations. They found that WS_2, which is similar to MoS_2, exhibits an indirect (bulk, E_g =1.3 eV) to direct (monolayer, E_g =2.1 eV) band gap transition. The band alignment of various monolayer semiconducting TMDs and monolayer SnS_2 has been obtained from first-principle calculations [40].

Electrical characterizations of single-layer MoS_2 have shown n-type conductivity with a room temperature mobility in the range of 0.5–3 cm^2/(V·s) [18, 41]. Using a halfnium oxide gate dielectric, Radisavljevic et al. [42] demonstrated a room-temperature mobility of single-layer MoS_2 is at least 200 cm^2/(V·s), similar to that of graphene nanoribbons, but still much lower than that of either pristine graphene or Si transistors. Because of the low mobility, MoS_2 transistors are probably more suited for low-power applications compared to Si transistors, rather than for high-performance applications.

4.3 2DM-based MOSFET

Apart from the main technological challenges in geometric scaling, a bigger intrinsic challenge is represented by the material properties: carrier mobility in silicon strongly decreases with body thickness reduction or increased doping, thus undermining possible improvements in the device switching speed. In this context, the 2DMs with their extreme thinness can serve as a convenient alternative. Considering digital electronic applications, graphene-based FETs cannot conform to the ITRS requirements because of its zero band gap, which leads to at most a few tens I_{ON}/I_{OFF} ratio, and large I_{OFF}. Many attempts have been made in order to open an energy gap in graphene, for example by applying a strong electric field over bilayer graphene [43], by quantum confinement in graphene nanoribbons with well-controlled width [44–46], by doping graphene with adatoms like boron atoms [46, 47].

The advantage of 2-D TMDs over graphene is the existence of an energy gap, which is crucial for low I_{OFF} and high I_{ON}/I_{OFF} ratio. Comparing to bulk materials, semiconducting 2-D TMDs have unique features that make them attractive as a channel material for FETs: their atomic thinness, the lack of dangling bonds, and a mobility comparable to Si [48]. One of the earliest uses of TMDs in FETs was reported in 2004, where WSe_2 crystals showed mobility comparable to the best single-crystal Si FETs (up to 500 cm^2/(Vs) for p-type conductivity at room temperature), and a 10^4 I_{ON}/I_{OFF} ratio at a temperature of 60 K [49]. This result was soon followed by devices based on thin films of MoS_2 with a back-gated configuration, resulting in mobility values in the range 0.1–10 cm^2/(Vs) [18, 50].

The first implementation of a top-gated transistor based on monolayer MoS_2 was reported by Kis et al. [51]. This device showed excellent I_{ON}/I_{OFF} ratio (10^8), n-type conduction, room-temperature mobility of >200 cm^2/(Vs) and SS of 74 mV/dec [51]. The top-gated geometry allowed a reduction in the voltage necessary to switch

the device and the integration of multiple devices on the same substrate. The high-*k* dielectric used in this device, HfO_2, also gave the additional benefit of improving the mobility of monolayer MoS_2. Top-gating with a high-*k* dielectric was also used in a p-type FET with an active channel made of a monolayer flake of WSe_2, which showed room-temperature hole mobility of 250 $cm^2/(Vs)$, close to 60 mV/dec SS and 10^6 I_{ON}/I_{OFF} ratio [52].

Although 2-D TMDs may not compete with conventional III–V transistors on the mobility values, for devices with very short channel length the transport becomes nearly ballistic, thus mitigating this issue. The ultimate thin body of 2-D TMDs provides high degree of electrostatic control that is important for device scaling and for reducing the SCEs. Furthermore, the relatively large effective mass for electrons and holes in TMDs represents an advantage, since a larger effective mass implies a larger density of states and therefore a larger ballistic I_{ON}. Taking into account the above facts, 2-D TMDs are promising candidates for future digital electronics. Recently, a demonstration of extremely scaled transistor based on a MoS_2 channel and 1-nanometer carbon nanotube gate was successfully implemented by Desai et al. [53]. This device exhibited SS of 65 mV/dec (near ideal value for MOSFET), and I_{ON}/I_{OFF} ratio of 10^6.

5. TFETs based on 2-D material vdWHs

One promising alternative energy-efficient switch to a MOSFET is TFET. To date, significant progress has been made in TFETs built on bulk Si, Ge, and III-V compound materials. TFETs built on bulk Si usually suffer from poor on-state current because of its large and indirect bandgap. To enhance tunneling, heterostructures have been adopted using III-V compound materials. The on state current of the TFET built on InAs/InGaAsSb/GaSb heterostructure nanowire has reached several µA/µm [54]. Despite tremendous advancements in the field, achieving simultaneously high on state current density and sub-thermionic SS over multiple current decades remains an open challenge for the TFETs. Various studies have demonstrated that the band edge roughness of the semiconductor in combination with the trap states at the surface and interfaces are limiting SS of the TFETs [55]. In addition, doping is known to further reduce band edge sharpness given the random distribution of the dopant atoms in the lattice. To overcome these fundamental limitations, 2-D layered materials show promise toward obtaining steep band edge tunneling devices, since they intrinsically have atomic level flatness.

5.1 Vertical vdWH TFET

A promising research direction is the stacking of different 2-D layered materials and/or 3-D bulk materials for fabricating vertical heterostructures with novel operation principles [56, 57]. A TFET was demonstrated to work by Britnell et al. [58] using two independently controlled graphene layers separated by thin hexagonal boron nitride ($h - BN$) layers acting as tunneling barrier. Recently, a vertical TFET based on bilayer MoS_2 as the channel and degenerately doped p-type Ge as the source, was fabricated by Sarkar et al. [59] and showed rather low SS of 31 mV/dec over 4 decades, and quite high on-current in TFETs, with V_{DD} as low as 0.1 V. The van der Waals gap between the 2-D MoS_2 and Ge acts as an extremely thin tunneling barrier, which enhances the tunneling and the on-current.

Early preparations of vdWH required the layer-by-layer exfoliation and restacking. However, restacking might bring adsorbates between layers,

detrimental for creating vdWHs with atomically sharp interfaces, demonstrated by Haigh et al. [60]. The intercalation of selected 2D materials with alkali metal ions offered an alternative way to vdWH construction. To boost on state current, the materials with high carrier mobilities such as graphene and Ge are suitable for the injection layers, while the semiconductors and insulators such as hBN and MoS_2 tend to be chosen as barrier layers. The carriers mainly transport between the two 2-D layers via interlayer tunneling. Yu et al. have demonstrated vdWH FET using a graphene/MoS_2 junction. However, the working mechanism of this device was proven to be the thermionic emission acrossing a Schottky barrier [61]. Similar tunneling phenomenon had also been observed in a WSe_2-based vertical graphene-TMD vdWH transistor by Shim et al. [62]. An extraordinarily large I_{ON}/I_{OFF} ratio of 5×10^7 was achieved at 180 K. The negative differential resistance (NDR) device made of BP/ReS_2 vdWH was reported to show rather high peak-to-valley current ratio values of 4.2 and 6.9 at room and low temperatures, showing advantages for future multi-valued logic devices [63]. Vertical vdWH TFET can be constructed using different 2-D semiconductor layers forming type-II (staggered) heterostructure band alignment. Under gate voltages, the band alignment passes from type-II to type-III (broken gap), such transition ignites the interlayer tunneling. Yan et al. reported a practical vertical n-type vdWH TFET built with $SnSe_2$/WSe_2 vdWH, showing a minimum SS of 37 mV/dec and a I_{ON}/I_{OFF} ratio exceeding 1×10^6 [64].

Similar with TFETs, there are recently some other different types of vdWH transistors that also operate with the assistance of tunneling. Here, we introduce two of them namely Dirac-source and cold source FETs. Quite recently, Peng's group proposed a novel Dirac-source FET which can operate below the thermionic limit for several decades at room temperature [65]. In the source material, electrons follow the thermal Boltzmann statistics, leaving an exponential tail inside the conduction/valence band. This tail is exactly the origin of the thermionic limit of SS = 60 mV/dec at room temperature. Here, the idea of the Dirac-source is to make this tail decay faster than the exponential function, by exploiting the particular energy dependence of DOS of graphene. The DOS decreases rapidly with energy approaching the Dirac point. For a n-type FET, if we set the Fermi level in graphene below the Dirac point, we can press down the thermal tail and decrease SS to below 60 mV/dec at room temperature. Extending on this concept, the cold source FETs have been proposed and investigated by Logoteta et al. [66], employing MoS_2-nanoribbon as the source material, which exploits a narrow-energy conduction band to intrinsically filter out the thermionic tail of the electron energy distribution. It should be noted that in principle, the Dirac-source and cold source FETs do not purely work on the tunneling mechanism to achieve sub-thermionic SS. Rather, the switching is obtained by modulating the height of a potential barrier under the gate electrode, exactly as in MOSFETs. The authors of these works expect that the operation of these devices to be significantly less sensitive to the performance-degrading factors plaguing the TFETs, such as the traps, band tails and roughness.

6. Quantum transport modeling

To solve the emerging problems and to investigate improved strategies both need advanced predictive simulation and modeling as theoretical guidance. The accuracy of the theory model will influence the exploring directions to a great extent. To properly describe and model the tunneling current flow in TFETs,

we need to develop a simulation approach able to take into account quantum phenomena as well as non-ideality effects due to phonon assisted tunneling. With appropriate simplifications to overcome the computational difficulties, the Non-Equilibrium Green's Function (NEGF) formalism provides a suitable framework to simultaneously treat the quantum transport of coherent carriers and the impact of diffusive phenomena such as electron-phonon interaction. The concept and the first applications of the NEGF were given by Schwinger [67], Kadanoff and Baym [68], Fujita [69], and Keldysh [70] at the beginning of the 1960s. The main advantages of NEGF are that it is full quantum, adaptable to different Hamiltonian types (effective mass, $k \cdot p$, tight-binding), and able to deal with many-body interactions through the introduction of self-energy operators [71–74].

Let us start by considering the Hamiltonian operator $\hat{H} = \hat{H}_0 + \hat{V}$. To evaluate the time evolution of the Green's function $G(\mathbf{r}, t; \mathbf{r}', t')$ in the Heisenberg picture, the time derivative of $G(\mathbf{r}, t; \mathbf{r}', t')$ can be obtained

$$\left(i\hbar \frac{\mathrm{d}}{\mathrm{d}t} - H_0(\mathbf{r}) \right) G(\mathbf{r}, t; \mathbf{r}', t') = \delta(t - t')\delta(\mathbf{r} - \mathbf{r}')$$

$$-i \int \mathrm{d}\mathbf{r}_1 \int_C \mathrm{d}t_1 V(\mathbf{r} - \mathbf{r}_1)\delta(t_1 - t)G^{(2)}(\mathbf{r}_1, t_1, \mathbf{r}, t; \mathbf{r}_1, t_1, \mathbf{r}', t'), \tag{4}$$

where $G^{(2)}$ is the *two-particle* Green's function. By further differentiating $G^{(2)}$, we get an equation of motion containing the three-particle Green's function, whose equation of motion depends on the four-particle Green's function, and so on.

Instead of solving the infinite hierarchy of the Green's functions, the irreducible self-energy is introduced, which is represented with the symbol Σ, and which is a functional of the single-particle Green's function G. We can replace the right-hand side expression $-iV(\mathbf{r} - \mathbf{r}_1)\delta(t_1 - t)G^{(2)}(\mathbf{r}_1, t, \mathbf{r}, t; \mathbf{r}_1, t, \mathbf{r}', t')$ by $\Sigma(\mathbf{r}, t, \mathbf{r}_1, t_1)G(\mathbf{r}_1, t_1; \mathbf{r}', t')$ into (4) to get

$$\left(i\hbar \frac{\mathrm{d}}{\mathrm{d}t} - H_0(\mathbf{r}) \right) G(\mathbf{r}, t; \mathbf{r}', t') = \delta(t - t')\delta(\mathbf{r} - \mathbf{r}')$$

$$- \int \mathrm{d}\mathbf{r}_1 \int_C \mathrm{d}t_1 \Sigma(\mathbf{r}, t, \mathbf{r}_1, t_1)G(\mathbf{r}_1, t_1; \mathbf{r}', t'). \tag{5}$$

The Green's function G is defined by the contour ordering along the contour $C = C_+ + C_-$ close to the real axis in the complex time plan. Since it is not obvious to keep track of the time-branch in the evaluation of the integral, four new Green's functions are defined: G_c the chronologically time-ordered Green's function, G_a the anti-chronologically time-ordered Green's function, $G^<$ the lesser Green's function and $G^>$ the greater Green's function. These four functions are not independent since $G_c + G_a = G^> + G^<$. The greater and lesser Green's functions are directly related to the hole density and electron density in the system. We also define the advanced and retarded Green's functions $G^A = G_c - G^>$, $G^R = G_c - G^<$, with $G^R - G^A = G^> - G^<$. We can define the same quantities for the Σ self-energy leading to the lesser $\Sigma^<$, the greater $\Sigma^>$, the advanced Σ^A and the retarded Σ^R self-energies. We also have the relation $\Sigma^R - \Sigma^A = \Sigma^> - \Sigma^<$.

Under steady-state condition, the Green's functions depend on time difference $\tau = t - t'$. We can Fourier transform the time difference coordinate τ to energy $G^{R,A,<,>}(\mathbf{r}, \mathbf{r}'; E) \equiv \int \frac{\mathrm{d}\tau}{\hbar} e^{iE\tau/\hbar} G^{R,A,<,>}(\mathbf{r}, \mathbf{r}'; \tau)$, as well as for the self-energies $\Sigma^{R,A,<,>}(\mathbf{r}, \mathbf{r}'; E) \equiv \int \frac{\mathrm{d}\tau}{\hbar} e^{iE\tau/\hbar} \Sigma^{R,A,<,>}(\mathbf{r}, \mathbf{r}'; \tau)$. Using Langreth's rules [75], the equations of motion for the Green's functions with respect to time t become

$$
\begin{cases}
(E - H_0(\mathbf{r}))G^R(\mathbf{r}, \mathbf{r}'; E) = \delta(\mathbf{r} - \mathbf{r}') - \displaystyle\int d\mathbf{r}_1 \Sigma^R(\mathbf{r}, \mathbf{r}_1; E) G^R(\mathbf{r}_1, \mathbf{r}'; E), \\[2mm]
(E - H_0(\mathbf{r}))G^A(\mathbf{r}, \mathbf{r}'; E) = \delta(\mathbf{r} - \mathbf{r}') - \displaystyle\int d\mathbf{r}_1 \Sigma^A(\mathbf{r}, \mathbf{r}_1; E) G^A(\mathbf{r}_1, \mathbf{r}'; E), \\[2mm]
(E - H_0(\mathbf{r}))G^<(\mathbf{r}, \mathbf{r}'; E) = \displaystyle\int d\mathbf{r}_1 \Sigma^R(\mathbf{r}, \mathbf{r}_1; E) G^<(\mathbf{r}_1, \mathbf{r}'; E) + \Sigma^<(\mathbf{r}, \mathbf{r}_1; E) G^A(\mathbf{r}_1, \mathbf{r}'; E), \\[2mm]
(E - H_0(\mathbf{r}))G^>(\mathbf{r}, \mathbf{r}'; E) = \displaystyle\int d\mathbf{r}_1 \Sigma^A(\mathbf{r}, \mathbf{r}_1; E) G^>(\mathbf{r}_1, \mathbf{r}'; E) + \Sigma^>(\mathbf{r}, \mathbf{r}_1; E) G^R(\mathbf{r}_1, \mathbf{r}'; E).
\end{cases}
\tag{6}
$$

The electron and hole concentration are respectively given by

$$
\begin{cases}
n(\mathbf{r}, t) = \langle \hat{\psi}^\dagger(\mathbf{r}, t)\hat{\psi}(\mathbf{r}, t) \rangle = -i\hbar G^<(\mathbf{r}, t; \mathbf{r}, t), \\[2mm]
p(\mathbf{r}, t) = \langle \hat{\psi}(\mathbf{r}, t)\hat{\psi}^\dagger(\mathbf{r}, t) \rangle = +i\hbar G^>(\mathbf{r}, t; \mathbf{r}, t).
\end{cases}
\tag{7}
$$

Under the steady-state condition, the relations can be expressed in the energy domain

$$
\begin{cases}
n(\mathbf{r}) = -i \displaystyle\int \frac{dE}{2\pi} G^<(\mathbf{r}, \mathbf{r}; E), \\[2mm]
p(\mathbf{r}) = +i \displaystyle\int \frac{dE}{2\pi} G^>(\mathbf{r}, \mathbf{r}; E).
\end{cases}
\tag{8}
$$

The total space charge density is therefore given by $\rho(\mathbf{r}) = e[p(\mathbf{r}) - n(\mathbf{r}) + N_D(\mathbf{r}) - N_A(\mathbf{r})]$, where e is the absolute value of the electron charge, N_D and N_A are the donors and acceptors concentrations.

The current density vector is given by

$$
\vec{J} = \frac{e\hbar}{2m_0} \lim_{\mathbf{r}' \to \mathbf{r}} (\nabla_{\mathbf{r}'} - \nabla_{\mathbf{r}}) G^<(\mathbf{r}, t; \mathbf{r}', t).
\tag{9}
$$

In practice, to evaluate $\vec{J}$ the lesser Green's function is expanded in a local basis, and the ∇-operator and m_0 are replaced by appropriate matrix elements $h_{m,n}$.

Noticing that at steady-state the time derivative of the charge density is zero. This implies that the $\nabla_{\mathbf{r}} \cdot \vec{J} = 0$ and the stationary current should be conserved in the device. In the presence of elastic scattering alone, the current density is conserved for electron at any given energy. With the inelastic scattering, the total current (integrated over energy) should be conserved.

The G^R and G^A Green's functions define the spectral function as

$$
A(\mathbf{r}, \mathbf{r}'; E) = i\left[G^R(\mathbf{r}, \mathbf{r}'; E) - G^A(\mathbf{r}, \mathbf{r}'; E)\right].
\tag{10}
$$

The spectral function provides information about the nature of the allowed electronic states, regardless of whether they are occupied or not, and can be considered as a generalized density of states. The diagonal elements of the spectral function give the local density of states (LDOS), $D(\mathbf{r}, E) = \frac{1}{2\pi} A(\mathbf{r}, \mathbf{r}; E)$. Therefore the trace of the spectral function gives the density of states $N(E) = \text{Tr}[A(E)] = \int d\mathbf{r} A(\mathbf{r}, \mathbf{r}; E)$.

On the other hand, the charge density can be included into the Poisson equation to renew the electrostatic potential, as $\nabla_{\mathbf{r}} \cdot [\varepsilon(\mathbf{r})\nabla_{\mathbf{r}}\varphi(\mathbf{r})] + \rho(\mathbf{r}) = 0$, with the charge density ρ, and the dielectric constant ε. Since the potential depends on the charge

density, which is given by the $G^<$ Green's function, the exact Green's function G both determines and is determined by the potential ϕ. The coupling between Green's function and the Poisson's equation needs to be solved self-consistently.

The Hamiltonian in a tight binding (TB) form can be obtained from the Wannier bases naturally. This procedure is called the maximally localized Wannier functions (MLWFs) method [76]. Or it can be obtained by the effective-mass approximation (EMA) and the k·p methods. These methods have been successfully utilized to predict the quantum transport behaviors of the devices based on many traditional and 2-D materials [77–87]. It should be noted that in the first principles calculations periodic boundary condition is necessary. As mentioned above, the TFET performance can be improved significantly by vdWHs that are not suitable for the first principles calculations.

7. Conclusions

We have given a literature survey on recently developed TFETs based on 2-D materials and their vdWHs. Compared with conventional MOSFETs, TFETs mainly work through the BTBT mechanism, resulting in large I_{ON}/I_{OFF} ratios within small supply voltages. To boost the on- and off-state behaviors simultaneously, heterojunctions should be adopted in the TFET design. Then, various novel TFETs based on the vdWHs are studied from structures to working mechanisms. We have also presented the quantum transport simulation method based on the NEGF formalism. However, no 2-D materials vdWH TFET in the experiments exhibits a satisfactorily overall performance. There is still a long way to realize 2-D TFET application. However, we hold an optimistic attitude toward vdWH TFET.

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Conflict of interest

The authors declare no conflict of interest.

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