Chapter

AMOLED Displays with In-Pixel Photodetector

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Abstract

The focus of this chapter is to consider additional functionalities beyond the regular display function of an active matrix organic light-emitting diode (AMOLED) display. We will discuss how to improve the resolution of the array with OLED lithography pushing to AR/VR standards. Also, the chapter will give an insight into pixel design and layout with a strong focus on high resolution, enabling open areas in pixels for additional functionalities. An example of such additional functionalities would be to include a photodetector in pixel, requiring the need to include in-panel TFT readout at the peripherals of the full-display sensor array for applications such as finger and palmprint sensing.

Keywords: AR, VR, OLED, readout, TFT, high resolution, extra functionalities, fingerprint, additional, functionalities, lithography, in-panel, high resolution, photodetector

1. Introduction

Active matrix OLED (AMOLED) displays are today's mainstream consumer displays available in various form factors, such as smart watches, mobile displays, and large area television. They are highly appealing because of their wide viewing angles, nice color saturation and great potential for curved, flexible and/or rollable format. There are several options for (flexible) backplane technologies based on thin-film transistors (TFTs), namely, metal-oxide TFTs (such as indium gallium zinc oxide or IGZO), low-temperature polycrystalline silicon (LTPS) TFTs, or a combination of IGZO and LTPS, more precisely LTPO or low-temperature polycrystalline silicon and metal oxide. All these technologies have their pros and cons. Among others, IGZO semiconductors are n-type only which is sufficient for a backplane driving an OLED but is less adequate for peripheral circuits. Another key important asset of IGZO is the ultralow source-drain leakage current due to the large bandgap of the semiconductor, enabling long retention times of data storing, i.e., pixels are not leaking. In contrary, LTPS has both n- and p-type devices and thus the capability of CMOS circuits. LTPS transistors can drive larger currents due to the intrinsically higher mobility, enabling complex in-pixel compensation schemes and peripheral circuits. However, with LTPS transistors the leakage will be larger. This is a key reason why LTPO has been developed: this technology combines

the ultralow leakage current of IGZO and a p-type LTPS transistor resulting in a hybrid complementary technology. An OLED is an organic LED emitting light directly proportional to its forward current. Therefore it requires a current source as driver in the pixel. In many cases, this is achieved by placing a TFT in series with the OLED and driving it in saturation.

In this chapter, we will investigate the potential to embed additional functionalities in the display. Therefore, several strategies will be discussed focusing on improving the resolution of the current displays, by technology optimization introducing photolithography patterning of the OLED and by design evaluating external compensation vs. internal compensation. The extra space in the pixel, due to the combination of photolithography and simple pixel circuit, provides opportunities to include extra functions at the same original area. The focus in this book chapter is to add a photosensitive detector for fingerprint and palmprint readout.

2. Display resolution roadmap for various applications

Resolution (number of pixels) and pixel pitch (size and spacing of pixels) are two main parameters defining the architecture of the display arrays. The first, expressed typically in megapixels, is standardized by the content type, resulting in different generations of TVs: VGA, full HD, 4K, and, most recently, 8K. The latter, expressed typically in pixels per inch (ppi) or pixels per degree (ppd), is used as a benchmark for smartphones, with high-end models featuring densities in the range of 600 ppi. This is a value that gives a good enough image quality for hand-held devices, with the viewing distance of approximately 30 cm (1 foot). At the same time, future near-to-eye augmented reality/virtual reality (AR/VR) displays impose ultrahigh definition, as the pixel density needs to be beyond the pattern resolving capabilities of the human retina (30 cycles per degree) [1, 2]. The resolution should be maximized to provide the highest possible output within the eye box in any given point of the 180° field of view (FOV), also to enable foveated rendering.

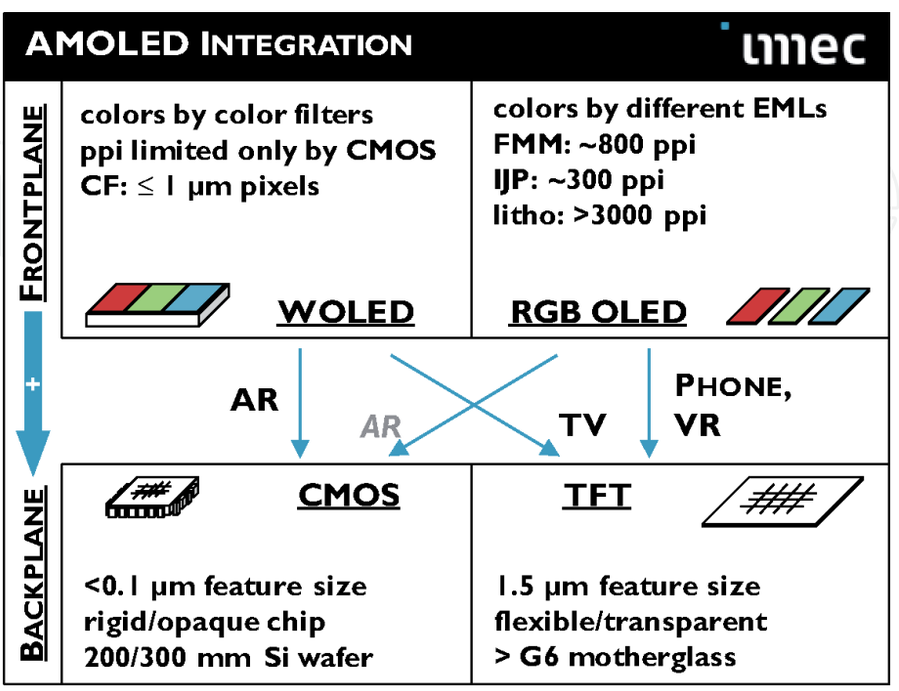

Figure 1.
Color-by-white vs. RGB OLED frontplane can be fabricated on top of CMOS or TFT backplane. Each combination is suitable for different applications.

An aperture ratio close to unity will eliminate the screen door effect and ensure natural experience. Transparency is necessary to avoid sense of isolation from the real-world view and to diversify from the virtual reality (VR) headsets (**Figure 1**). To realize all of the above, we need both the microdisplay-like pixel pitch down-scaling [3] and the flat-panel-display-like (FPD) backplane size up-scaling [4, 5]. Switching to advanced nodes in flat panel backplane manufacturing can result in ultrahigh-definition, direct-view AR displays fabricated in a cost-effective way.

3. Lithographic patterning of OLEDs to increase resolution

In order to realize an ultrahigh resolution display, all elements of the system (backplane, frontplane, and driving) need to provide appropriate pixel density. On the frontplane side, several options for the light source can be chosen (**Figure 2**). OLED technology currently dominates the smartphone display industry not only with performance but also with the cost structure. In this case, the colors are defined by depositing separate device stacks for each color, which is typically referred to as side-by-side, red-green-blue (RGB) array. In OLED TVs, one common white OLED stack is combined with a color filter array (CFA). The limitation of the side-by-side RGB array is the pixel density, limited by the fine metal masking (FMM) technology, which uses deposition through a metal mesh. The white OLED array can achieve very small pixel pitch, which is only limited by the backplane and CFA resolution but imposes brightness loss due to CF transmission. Patterning multicolor OLEDs by photolithography can address the needs of ultralow pixel pitch for the future AR displays by realizing side-by-side OLED stacks with extreme density.

Patterning OLEDs by photolithography is an emerging, disruptive fabrication technique. The main challenge is the extreme chemical sensitivity of OLED materials with solvent, moisture, air, and temperature exposure responsible for performance degradation. The choice of appropriate photolithography chemistry is crucial, with fluorinated [6] or non-fluorinated systems [7] as the dominant options. **Figure 3** shows the concept of using a negative-type photoresist to define patterns on top of OLED in a subtractive approach. First, the OLED stack is deposited as a plain layer over the entire substrate, on top of a pixel definition layer (PDL). This defines the active area of the light emitter. Second, photoresist is deposited on top of the entire substrate. Then, it is exposed through a lithography mask and developed to obtain the required pattern. Afterwards, the OLED layers that are not covered by the photoresist are etched away (typically with dry etching, such as reactive ion etch). In the end, the photoresist is stripped to achieve patterned OLED islands.

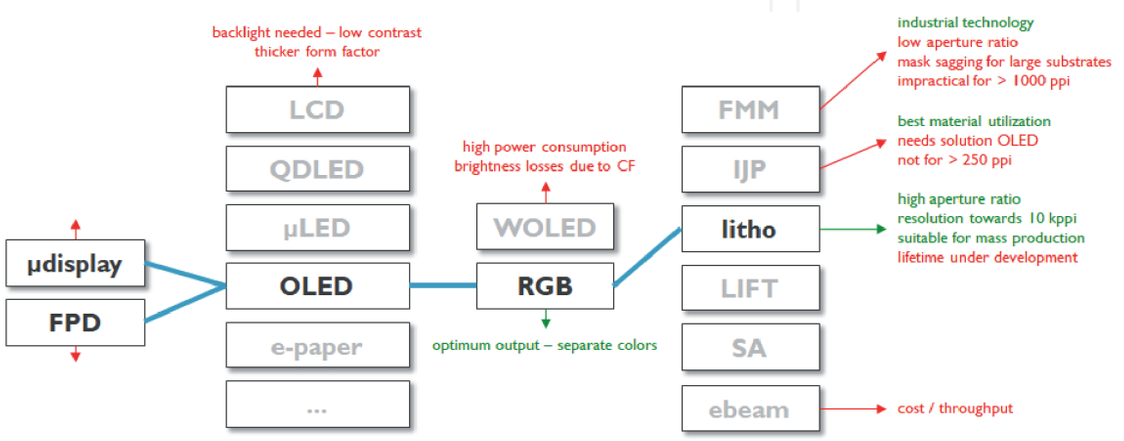

Figure 2.
Various display configuration options.

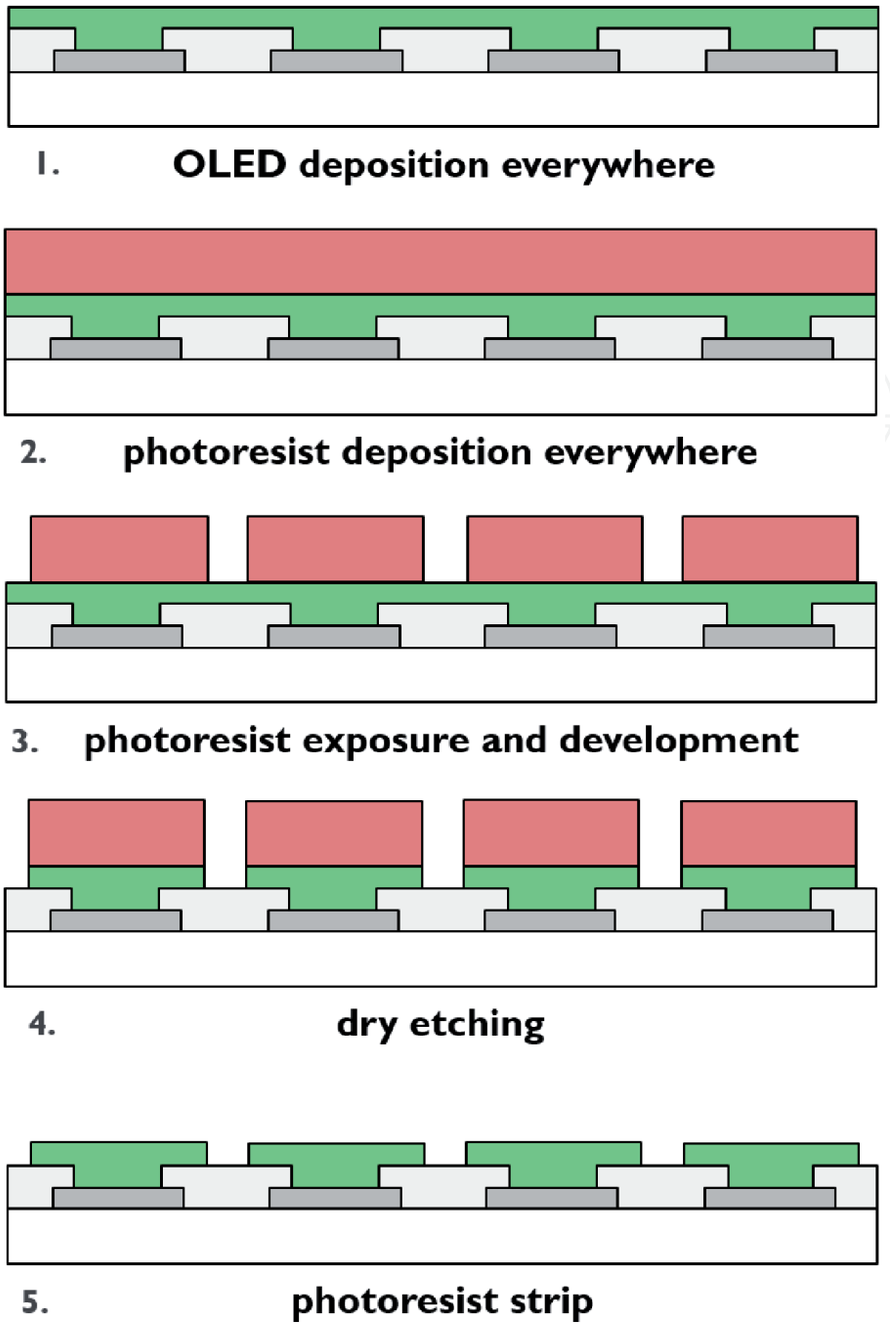

Figure 3.
Process flow for photolithography patterning of OLED stacks.

Photolithography allows pattern transfer beyond 1 μm resolution, enabling high-density lines and spaces. Transfer of small islands means that, with appropriate alignment (e.g., with an i-line stepper), a pixel density of a few thousand pixels per inch (ppi) can be realized. Transfer of openings means that pixel spacing can be minimized, resulting in a high aspect ratio. This is applicable for both TFT-based flat panel displays and CMOS-based microdisplays. Tests on patterning the OLED emission layer have shown that it is possible to achieve 1 μm pitch lines and spaces (**Figure 4**). Furthermore, the photoluminescence signal of the EML is maintained proving compatibility of this process with OLED material. 1 μm presented here is not a fundamental limit of the approach but rather a limit of the lithography mask design used in the experiment.

The achievable pixel density of the frontplane is limited not only by the photoresist used but also by the critical dimension (CD) and alignment/overlay accuracy of the litho tools used. In the i-line steppers typical for flat panel

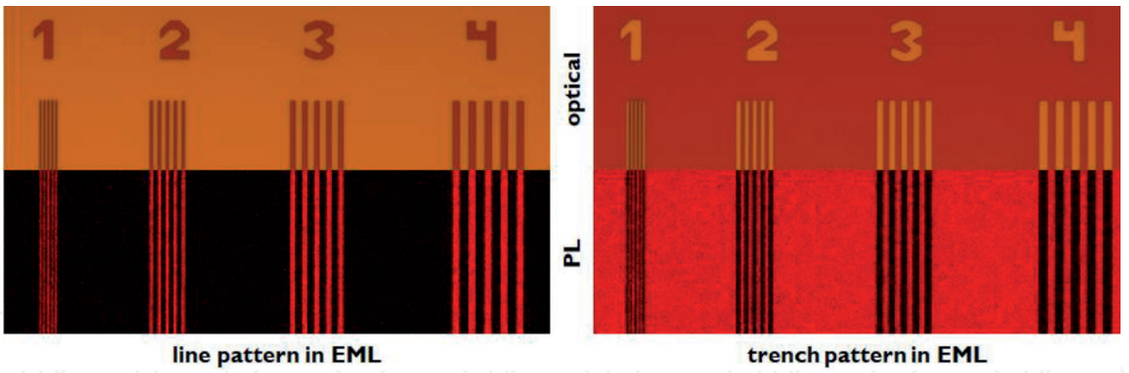

Figure 4.
OLED patterns of 1, 2, 3 and 4 μm: optical and corresponding photoluminescence pictures of red EML patterned as lines (left) and spaces (right).

manufacturing, the achievable CD is 1.5 μm with an overlay between 0.25 and 0.5 μm. In contrast, CMOS fabs used for microdisplay manufacturing feature more advanced semiconductor nodes, with 248 nm KrF or 193 nm ArF light sources. Assuming a minimum PDL opening (defining the active area) of 500 nm, a 1.5 μm node imposes a density limit of 3500 ppi (for RGB) with an aperture ratio below 5%. Going to KrF steppers, the achievable density increases to 10,000 ppi while keeping the aperture ratio above 35%. This demonstrates the need of a tooling upgrade for future AR displays, both for the frontplane and the backplane. Denser and more efficient packing of pixels requires scaling down of the technology node, especially in FPD manufacturing.

OLED patterning by photolithography means that the deposition of the stack is interrupted (vacuum break) and the photoresist interacts with the organic materials. In the most simple case, the photolithography process is performed in a clean room in ambient atmosphere. The devices are loaded back into the glove box after the etch step for each color and after the photoresist strip when all colors are finished. This raises a serious challenge for the device lifetime. If the process is not optimized for compatibility with the stack, the current-voltage-luminance (IVL) curve shifts to the right (increased turn-on voltage) and to the bottom (reduced luminance). As a consequence, the brightness of the patterned OLED drops very fast and disappears even after a few minutes (**Figure 5**). Optimization of the photoresist system, of the OLED stack [8] and of the fabrication process, is needed to achieve OLED performance enabling implementation into devices. At imec, we demonstrated phosphorescent green OLED with T90 lifetime of >150 h at the starting brightness of 1000 nit. Efficiency remained above 85 cd/A before and after patterning. Current performance is considered an important step on the path to industrial technology readiness level, estimated to be T97 of at least 1000 h (for the green stack) [8].

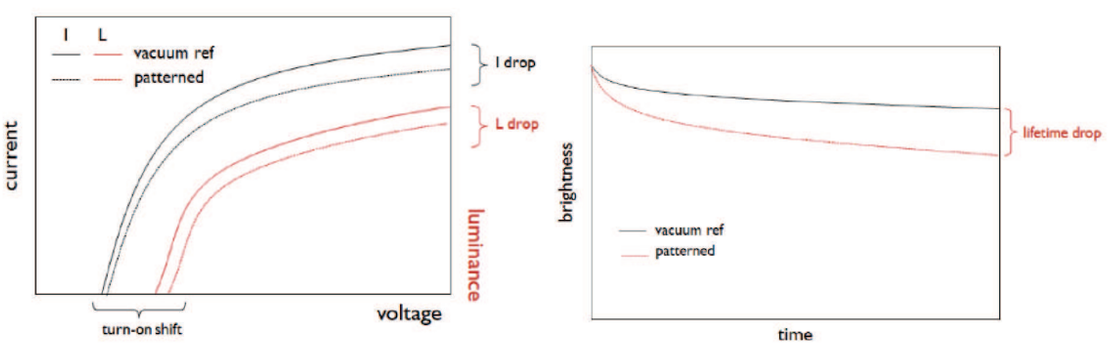

Figure 5.
IVL and lifetime curves for reference OLED and the possible effects of degradation by patterning.

Figure 6 shows an example comparison of unpatterned and patterned OLED lifetime curve at initial brightness of 1000 nit. The performance improvement can bring the two curves closer together.

OLED photolithography was used to fabricate passive displays with a 1400 × 1400 pixel array (almost 2 megapixels). 6 μm metal lines and 10 μm line pitch with SiN pixel definition layer (PDL) were used on glass substrate. Green and red OLED stacks were deposited by thermal evaporation in ultrahigh vacuum. After deposition of the first color (until above emission layer), photoresist was spin-coated, baked, exposed, and developed. Then, the OLED stack not covered by the photoresist was removed by dry etching. After that, the sample went back to the ultrahigh vacuum chamber for second color deposition, and the patterning process was repeated, this time finishing with stripping the photoresist. A semitransparent top contact stack was subsequently deposited, and the display was encapsulated with cavity glass. Both colors can be driven separately, and the PDL design allows for emission of a fixed image specified for each color (**Figure** 7). Subpixel pitch of 10 μm resulted in smooth edges and excellent feature representation. The device was tested for tens of hours with both colors on. No drop of brightness nor appearance of defects could be observed [9].

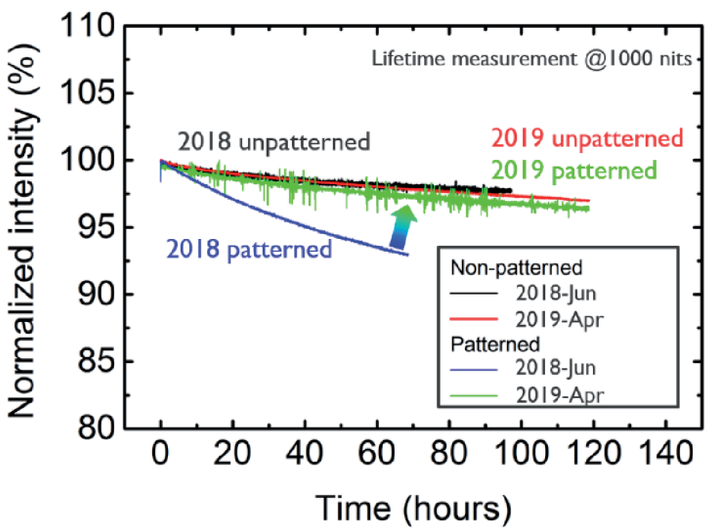

Figure 6.
Lifetime curves of a phosphorescent green OLED at 1000 nit starting brightness for unpatterned and patterned stack.

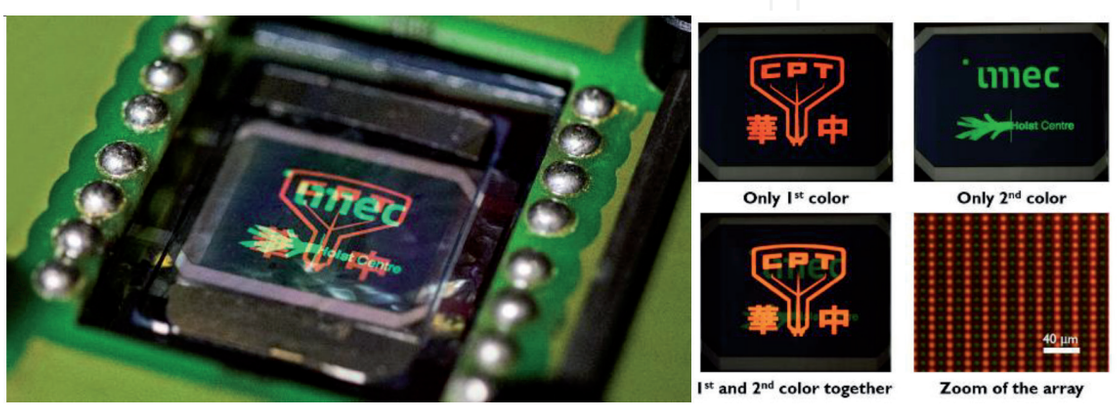

Figure 7.
Passive 1250 ppi patterned OLED display with 1400 × 1400 pixels, 10 μm subpixel pitch, and independent color driving: general view (left) and detailed view for different color drivings (right).

This fabrication process is compatible with both CMOS backplanes and flexible TFT backplanes. The frontplane can thus be implemented in an active matrix display. Of course, photolithography can be used several times to realize more colors for a full-color display.

4. Increased resolution by pixel driving techniques

To increase the display resolution, not only the technology (backplane and frontplane) but also the pixel driving techniques should be optimized. The OLED light output is dependent on the drain current of the driving TFTs of the AMOLED displays. Due to inherent variations in AMOLED displays, some compensation methods to the drain current of the TFTs are required to achieve uniform brightness. This can be implemented through either in-pixel compensation [10] or external compensation [11, 12]. Since in-pixel compensation schemes typically require more transistors inside the pixel, external compensation methods are preferred for high-resolution applications. **Figure 8** shows pixel circuits and a possible layout for in-pixel compensation, using an 8T1C [10] pixel, and external compensation using a 3T2C [11] and, respectively, a 2T1C [12] pixel. For all these layouts, the same design rules were used. It is clear from this figure that a display with external compensation, especially the 2T1C pixel circuit, can achieve a much higher pixel density.

The achievable pixel density depends on both the pixel circuit and the design rules imposed by the technology, such as the critical dimension (CD) of the lithography tool. **Figure 9** compares the achievable resolutions for different CDs for the 8T1C, the 3T2C, and the 2T1C pixel circuit. Although the CD of 1.5 μm, as currently achievable with typical i-line steppers, only yields a maximum pixel density of 565 ppi for the 8T1C pixel circuit, the same CD already yields a significant improvement for the pixel circuits using external compensation, namely, 847 ppi for the 3T2C pixel

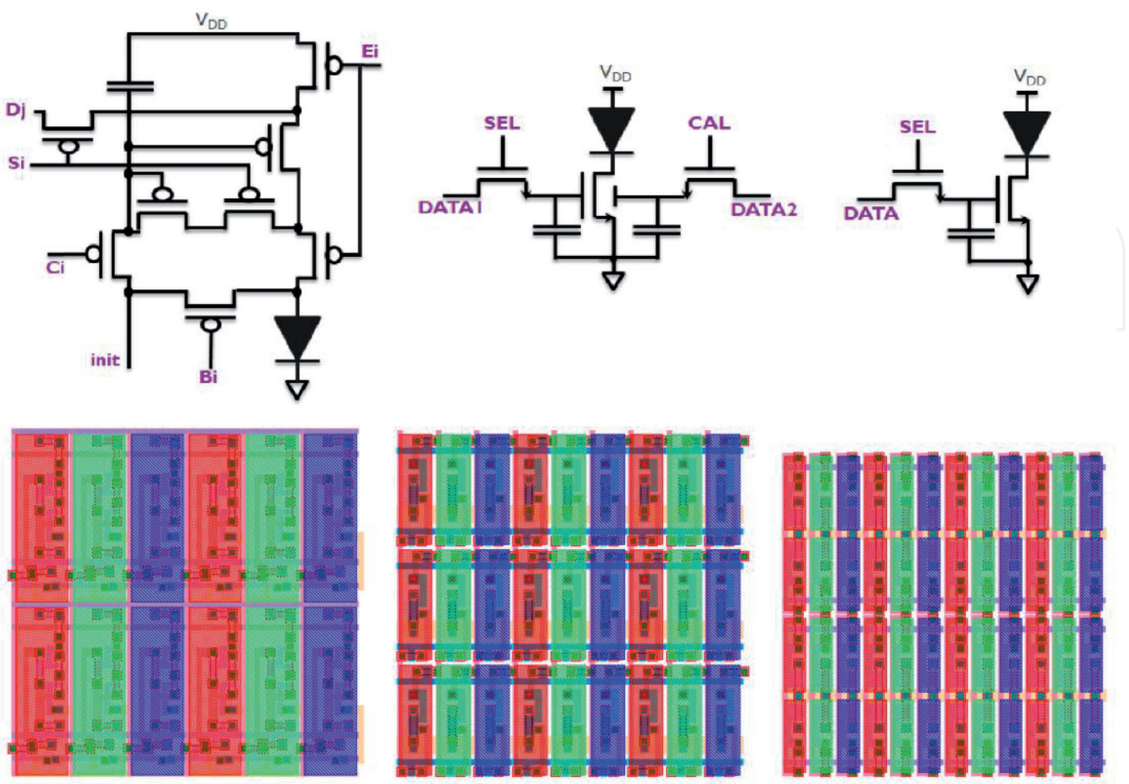

Figure 8.
Pixel circuits and corresponding layouts for (left) 8T1C, (middle) 3T2C, and (right) 2T1C pixels.

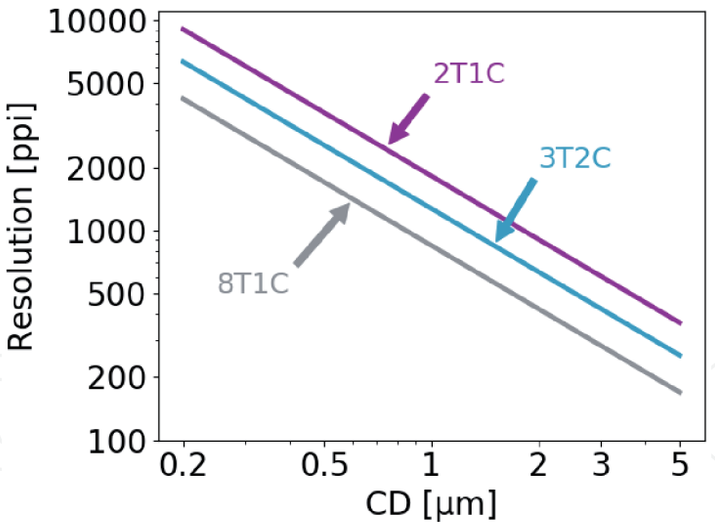

Figure 9.
Pixel resolution vs. critical dimension (CD) for various pixel schemes.

circuit and 1210 ppi for the 2T1C pixel circuit, respectively. Furthermore, improvements in technology allowing smaller CD will even further increase the achievable pixel density, up to 9070 ppi for the 2T1C pixel circuit, when using a CD of 0.2 µm.

The compensation principle for the 3T2C pixel circuit relies on the fact that applying a voltage on the backgate of a transistor will shift the threshold voltage (V_T) of that transistor. By applying the correct compensation voltage to the backgate of the drive transistor of each pixel, all V_T variations can be eliminated, resulting in a more uniform display. This compensation method uses three different modes of operation for the display. The first mode of operation is the calibration mode. In this mode, the correct compensation voltage is determined for each pixel by applying a certain reference voltage to the frontgate and measuring the current through the pixel while varying the backgate. When the measured current matches a predetermined reference current, the voltage on the backgate is the correct compensation voltage, which will be stored both on the capacitor connected to the backgate and in external memory. Once the correct backgate voltage is set for every pixel, the display can be switched to normal operation. In this mode, the display is driven with the normal video data, which is written to the frontgate of each pixel. Since the CAL signal is low in this mode, the charge on the capacitor will remain, and hence the backgate voltage will be the compensated voltage. However, due to leakage, this charge will slowly change over time. Therefore, a third mode of operation is added, namely, the calibration refresh. In this mode, the SEL signal is kept low, but the CAL signal is running through the display, while the compensation data is applied to the data lines. This way the compensation voltage is restored on the backgate, to ensure the V_T uniformity remains over time. This compensation method shows a significant improvement in current variation, as demonstrated in **Figure 10**.

The current through the drive TFT (I_{DS}), and thus through the OLED, when operating in saturation regime can be calculated for a certain data voltage (V_{GS}) by using Eq. (1):

$$I_{DS} = \frac{\mu * C_{ox}}{2} * \frac{W}{L}(V_{GS} - V_T)^2 = \beta * (V_{GS} - V_T)^2 \quad (1)$$

Compensating only for V_T can eliminate variations in current for one gray level; however, if the β-factor is different for each pixel, the current will still vary for different gray values, even after V_T compensation. This is shown in **Figure 11** for the 3T2C pixel. As a consequence, we propose a new compensation method

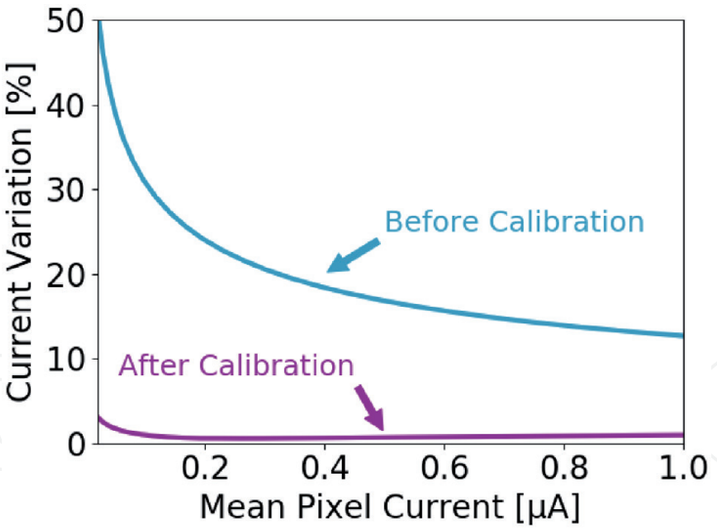

Figure 10.
Current variation of a 3T2C display before and after compensation.

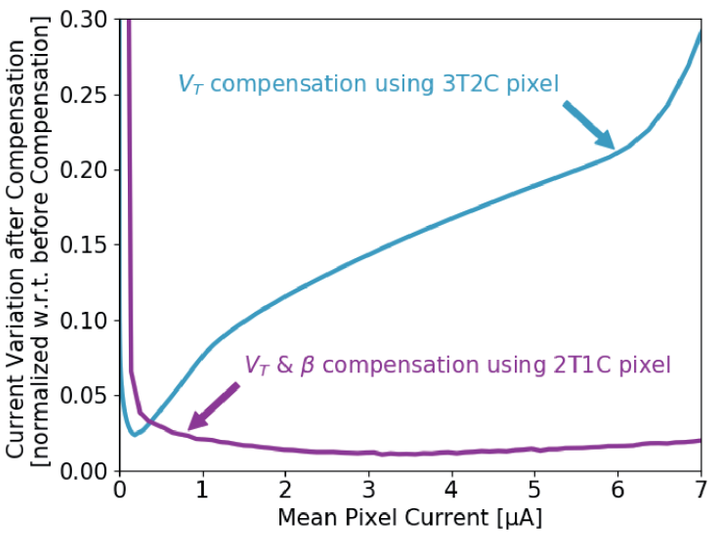

Figure 11.
Current variation of a 3T2C and 2T1C display before and after compensation.

to compensate for both β and V_T variations. Similarly as the previous described compensation method, we will first characterize the current through each pixel for multiple data voltages, whereafter the measurements are fitted to Eq. (1).

For each pixel, the extracted β and V_T values are stored. Based on these values, the V_{GS} voltages can be calculated for each pixel by the driver IC for each desired gray level by using Eq. (2):

$$V_{GS} = \sqrt{\frac{I_{DS}}{\beta}} - V_T \tag{2}$$

This calculation is relative simple and straightforward, as it only requires a multiplication, a subtraction, and a square root calculation, which enables to display real-time video content by using this methodology. **Figure 11** shows the current variation improvements directly obtained from our AMOLED displays, by utilizing the V_T-only compensation method and comparing it to the V_T and β compensation method. As mentioned above, the simple V_T compensation method provides good variation results for a small range, whereas the combined parameter method improves the variation across all desired gray levels.

5. Adding a fourth pixel for finger/palmprint sensing

Fingerprint sensor arrays (Figure 5.1) [13] are becoming a mainstream security mechanism for mobile devices and are today available as autonomous silicon-based component. The integration of the fingerprint sensor array together with AMOLED displays [14–16] would benefit the footprint of the mobile device and the functionality, enabling detection of multiple fingers at once or even a palmprint.

5.1 Side by side/under/over display pixel

Fingerprint sensors combined with AMOLED displays can be realized in three different configurations for the sensor pixels: (1) in the same plane of the display pixels and (2) under and (3) over the display pixels (**Figure 12**). With sensors in the same plane, the display module gains optical sensing capability by incorporating photodetector pixels between OLED pixels. Sensors, under or above the display, require a separate fingerprint module. A fingerprint module under the display would need a semitransparent display and light scattering management. A fingerprint module over the display requires a transparent imager to avoid changes in display emission. In the previous section, we have demonstrated that a higher resolution backplane can be achieved at the same critical dimension by introducing external compensation methods. This combined with the photolitho-based patterning method of OPD and OLED will the crucial enablers for such a configuration as analyzed in Paragraph 3.

5.2 Passive/active sensor pixel

The pixel circuit architecture of the sensor array can be either passive or active [17]. The passive pixel is depicted in **Figure 13** and is comprised by the photoelement, a capacitor, and a select TFT. The main difference of the active pixel is that it requires an extra TFT acting as a local amplifier. For high-resolution applications, the active pixel is not recommended, since its footprint is larger than the footprint of passive pixels.

5.3 Integrated readout circuit

The integration of peripheral readout circuitry in panel side-by-side with the display peripherals is beneficial for resolution, connectivity, and potential lower system cost of the device. In this paragraph TFT-based integrated readout is demonstrated by using our IGZO n-type only TFTs.

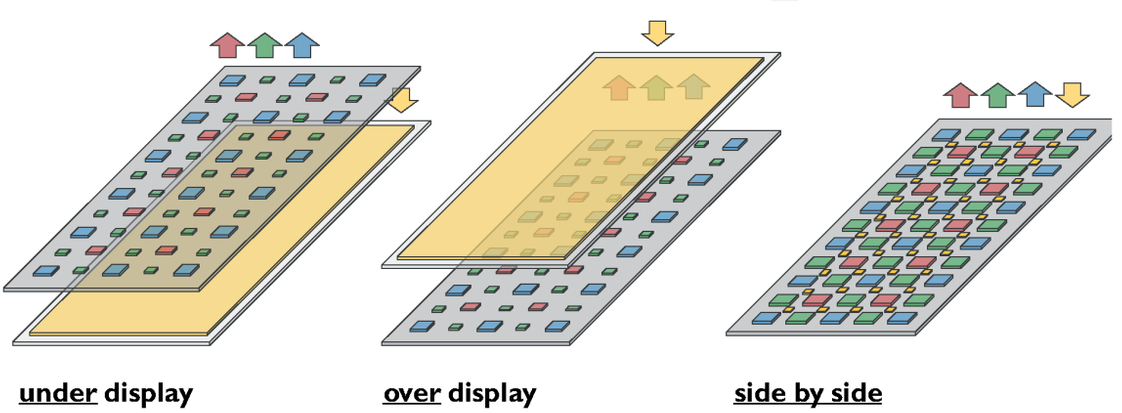

Figure 12.
Fingerprint integration configurations in AMOLED displays.

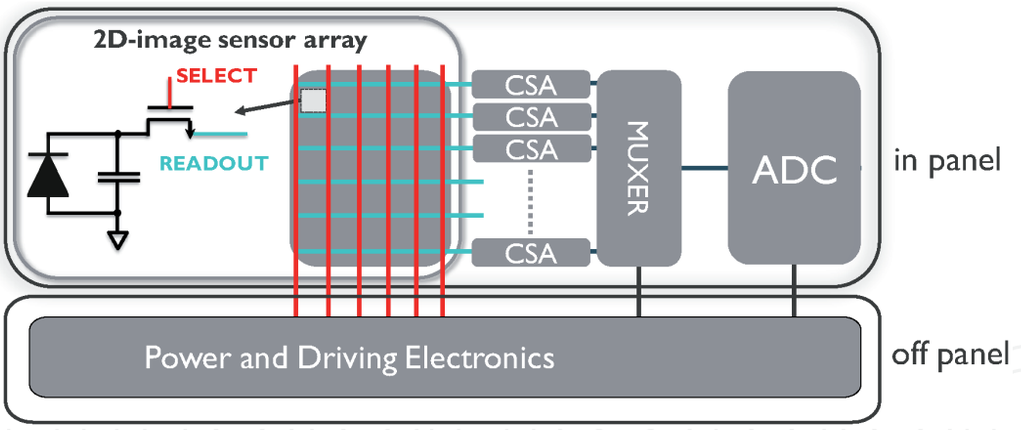

Figure 13.
Block diagram of the proposed in-panel fingerprint sensor array with integrated CSA for each line, multiplexer (MUX), and ADC. Power and driving electronics remain off-panel.

The necessary blocks to implement an in-panel readout system are a charge sense amplifier (CSA), a multiplexer (MUX), and an analog to digital converter (ADC). The CSA is reading out the charge stored in each pixel of the array. The MUX is multiplexing the CSA outputs directly to the ADC, decreasing the number of the required ADC converters. The ADC is converting the analog voltage received from the CSA to a digital code. Various TFT-based analog blocks have been demonstrated in the literature [18–24]. Metal-oxide TFT technologies are preferable due to uniformity over large areas, very low leakage currents, and lower cost over area. In the following section, fast and small footprint ADCs and charge sense amplifiers (CSA) are discussed to meet the specifications of an in-panel fingerprint array.

In **Figure 13**, the high-level block diagram of the in-panel readout system is shown. The five main blocks are detailed: a two-dimensional (2-D) image sensor array, the CSAs connect on each row of the array, a multiplexer connects four or more rows (MUX), and ADC connects to every MUX and off-panel power and driving electronics. Each column of the 2D image sensor array is readout from the corresponding row by a CSA. The pixels are readout subsequently enabled by the "SELECT" signals from the columns and converted to digital code through the MUX and an ADC. The MUX enables a larger footprint for the ADC, up to 4 to 8 times larger compared to a single line (50 μm). Hence, the ADC and MUX needs to be 4 to 8 times faster than the CSA. A 1–2 fps readout of 1M pixel imager (1000 × 1000 pixels) sets a readout speed of 1–2 kS/s per line for each CSA. This translates to 4–8 kS/s for the ADC if a 4:1 MUX is used or 8–16 kS/s for a 8:1 MUX. The slower ADC configuration sets the specification limitation to the width of the ADC to 200 μm, whereby the faster allows a width of 400 μm.

5.4 Dual-gate metal-oxide technology

Figure 14 (a) depicts the cross section of the dual-gate self-aligned metal-oxide (MO) technology on a 15-μm-thick polyimide film [25, 26]. The metal-oxide (IGZO or ITZO) TFTs are fabricated with two metal gates (M0, M1) and source-drain metal contacts (M2). An additional metal layer (M3), not shown in the cross section, is beneficial for footprint but also for performance and noise. The CSA experimental results shown in the following sections are designed with an extra metal layer, also used as anode layer.

Figure 14(b) shows the distribution of the extracted on-current (I_{ON}) from the measured transfer characteristics of 480/20 (μm/μm) IGZO (red) and ITZO (orange) dual-gate TFTs. The IGZO TFTs exhibits a median I_{ON} of 54.4 μA, whereas

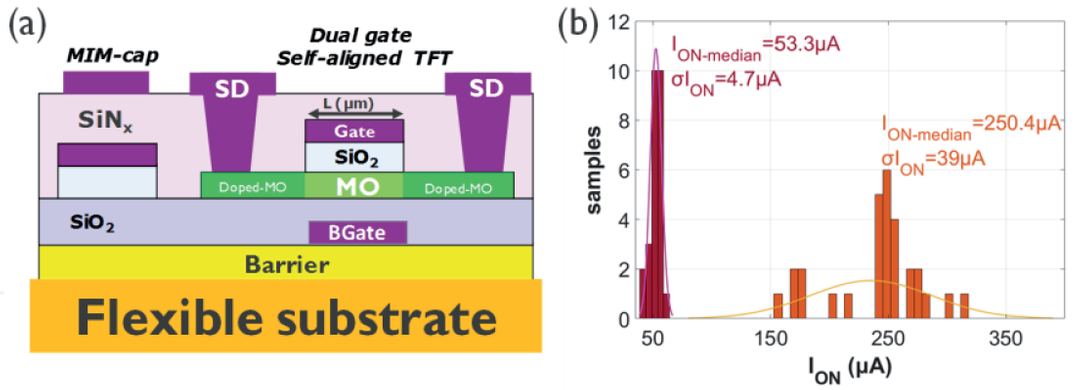

Figure 14.
(a) Cross section of dual-gate self-aligned metal-oxide technology on flexible polyimide substrate and (b) extracted on-current (I_{ON}) from experimental data of 480/20 (μm/μm) dual-gate self-aligned ITZO (red) and IGZO (orange) TFTs.

the ITZO dual-gate TFT exhibits a median of 250.4 μA. Although the I_{ON} of the ITZO TFT is 5 times larger, the normalized spread of I_{ON} to the median over the wafer is double (15.4% for ITZO and 8.8% for IGZO). Threshold voltage is also extracted from the same measurements, yielding 1.16 V (and σV_t = 242 mV) for ITZO and 1.77 V (and σV_t = 94 mV) for IGZO TFTs. The 480/20 TFT is the largest footprint TFT used in the implemented designs. In **Figure 15**, microphotos of the (a) ADC and (b) the L = 3 μm CSA are shown.

5.5 Charge sense amplifier

The schematic of the CSA is shown in the **Figure 16(a)**. The schematic of the operational amplifier (OPAMP) used in the CSA is shown in **Figure 16(b)**. The OPAMP comprises a differential pair and a load that is driven by a two-stage buffer, initiated by a start-up circuit. The driver consists of two diode-connected load inverters as input and output stages. The output stage is driven by a start-up circuit to initialize the operation and provide ~1 loop gain positive feedback bias to the n-type load of the differential amplifier such that gate voltage follows source voltage. A buffer is also included at the output nodes A and B to increase the speed of the amplifier.

The experimental results of open-loop experiments of the OPAMP are shown in **Figure 17** for dual-gate self-aligned IGZO TFTs of minimum channel length of L = 5 μm. The maximum gain for the 5 μm design is 43.2 dB with a phase margin of 52°. Both parameters are critical for stable closed-loop operation of an OPAMP. The

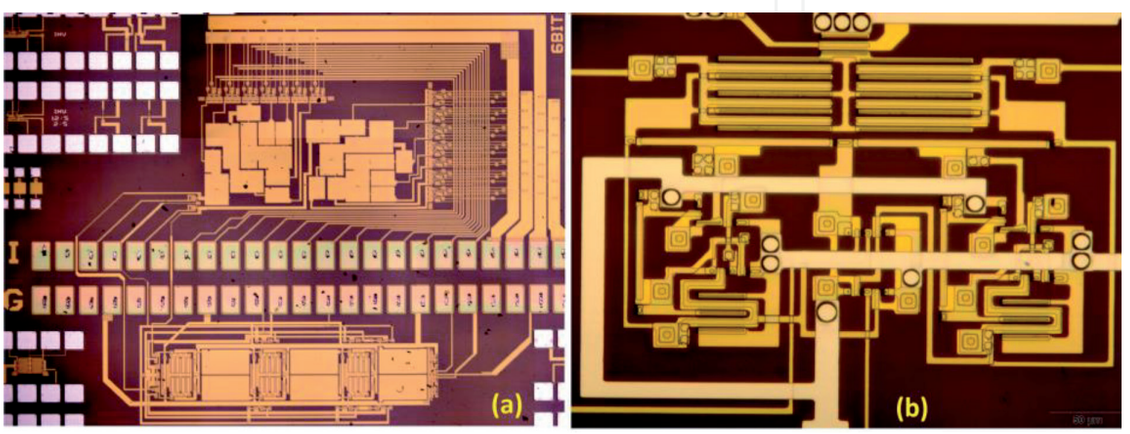

Figure 15.
Microphotos of the (a) ADC and (b) L = 3 μm CSA on flexible substrate.

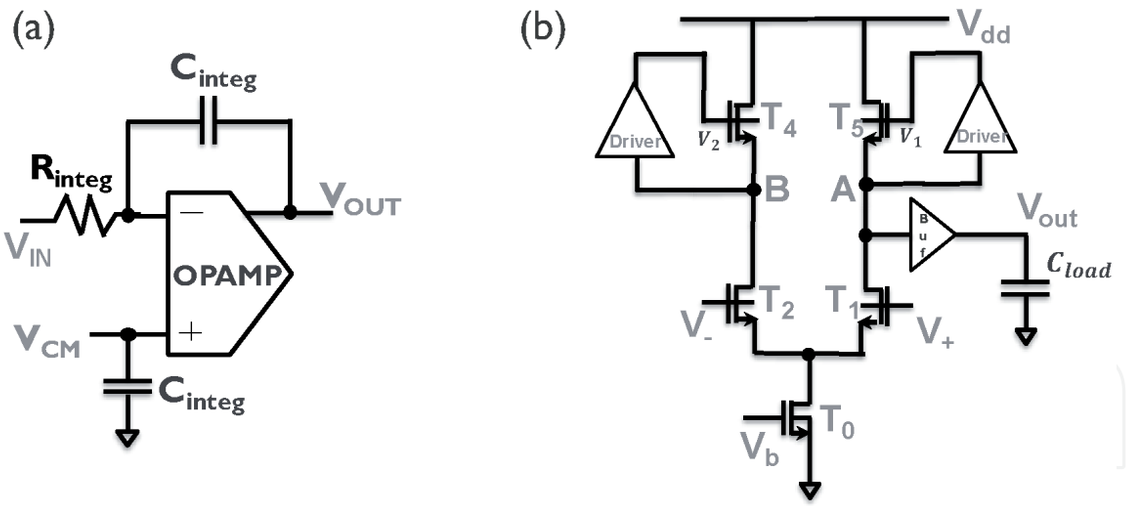

Figure 16.
Schematic of (a) charge sense amplifier (CSA) and (b) the OPAMP schematic using dual-gate self-aligned TFTs used in the CSA in (a).

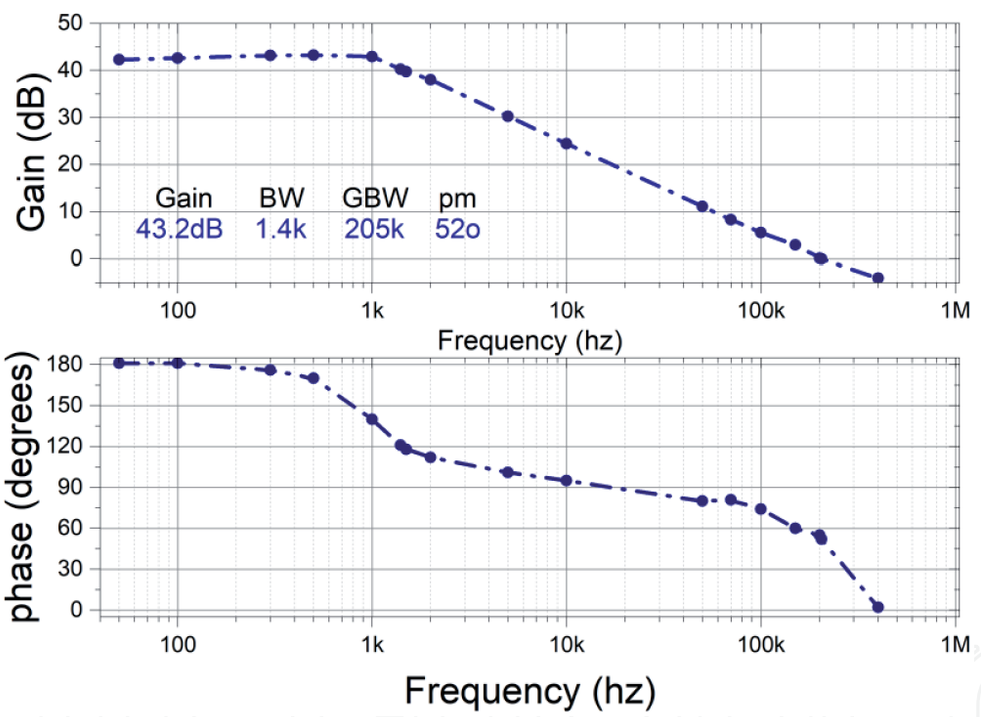

Figure 17.
Experimental bode plots of the OPAMP using dual-gate self-aligned IGZO technology for L = 5 μm.

obtained bandwidth (BW) is 1.4 kHz, and gain-bandwidth reaches 205 kHz. These specs are compared to other publications in the state-of-the-art **Table 1** using TFTs. The footprint of the CSA is 0.28 mm^2 with the capacitors. The footprint of the CSA can be decreased to 0.07 mm^2 if 3 μm design is implemented. These footprints will result in a bezel width of 5.5 mm (L = 5 μm) and 1.3 mm (L = 3 μm) [27] for a 50 μm pixel size.

5.6 Analog to digital converter

The successive approximation C-2C architecture is selected as ADC architecture, due to the low power dissipation and the 0.1% uniformity of metal-insulator-metal capacitors across large-area thin-film wafers. The schematic of the ADC is shown in **Figure 18**. The comparator is the most critical building block of the ADC for speed

Circuit	This work	2018 [11]	2012 [8]	2013 [10]	2014 [9]
Supply (V)	**15**	15	10.5	5	50
Gain (dB)	**43**	32	~21	18.7	19.2
GBW (kHz)	**205**	140	2	472	100*
pm (°)	**52**	53	50*	neg	46
Area (mm^2)	**0.28**	0.3	*Discrete*	2.08	—
Substrate	**PI**	PI		PI	Glass
L (μm)	**5**	5	10	6	10

*Estimated.

Table 1.
In-Ga-Zn-O-TFT differential amplifier comparison.

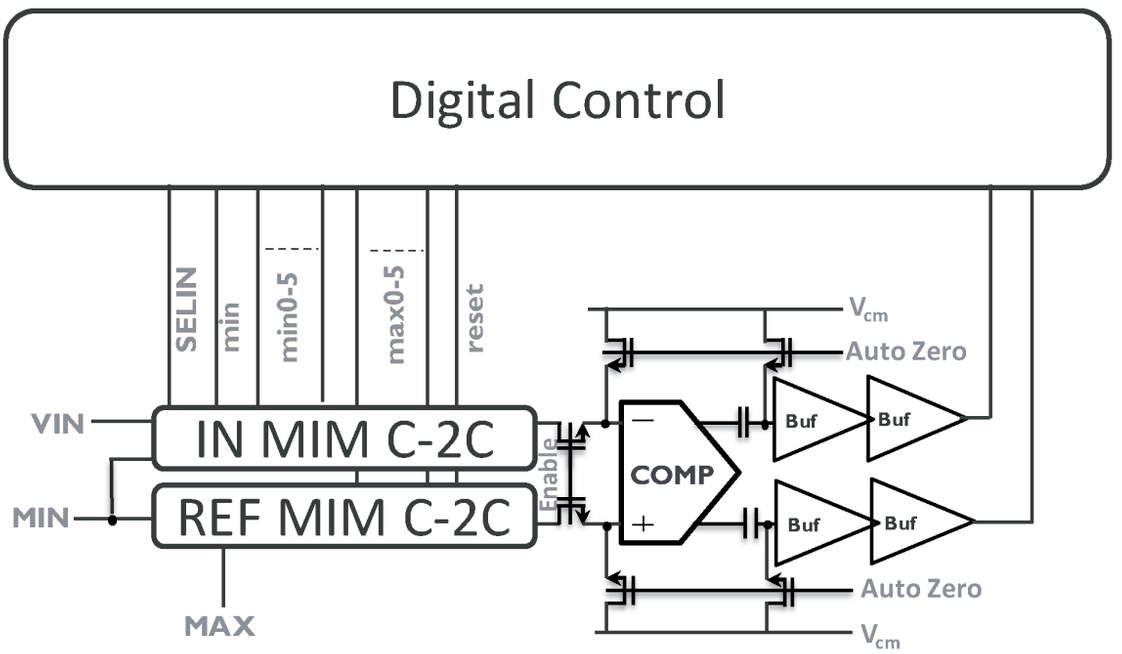

Figure 18.
The implemented SADG TFT ADC block diagram driven with offset compensation.

and accuracy. To improve the accuracy of the comparator, open-loop offset cancelation [28] is used. The response of a L = 5 μm dual-gate self-aligned TFT-based comparator at 10 kHz for two inputs ΔV_{in} = 0 and 10 mV is shown in **Figure 19**. The offset of the comparator is minimized to less than 10 mV using open-loop cancelation, even though the V_t variation of the TFTs is one order larger.

The experimental results of the reconstructed samples from a sinusoidal analog wave applied at the input of the IGZO ADC are shown in **Figure 20(a)**. The IGZO ADC achieves 6-bit resolution at a sampling speed of 133 S/s at 15 V power supply using a L = 20 μm comparator. The clock speed of the IGZO ADC is at 2 kHz matching the bandwidth of the comparator, and 15 clocks are required to complete the conversion. Two options are available to increase the sampling speed of the ADC as set by the specification for 1–2 fps fingerprint readout: channel length downscaling and/or change of TFT technology or change of ADC architecture to flash but then for 6-bit the area might increase dramatically due to the multiple resistors needed and 64 comparators.

The minimum length of the TFTs of the measured ADC is L = 20 μm. The length of the TFT of the comparator of the ADC defines the speed of the circuit.

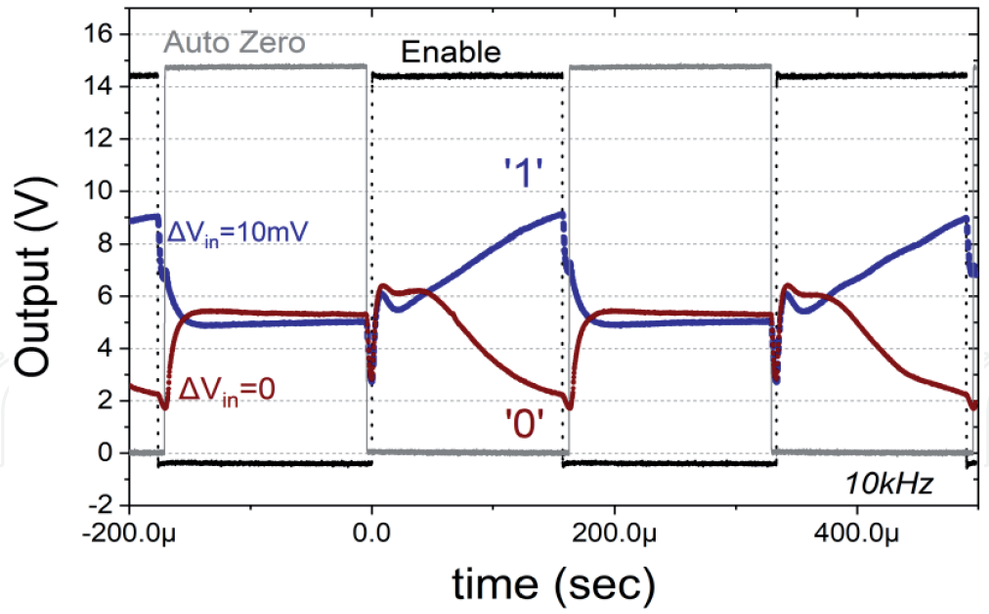

Figure 19.
Measured comparator output with auto-zero offset cancelation for designs using TFTs of minimum L = 5 μm at 10 kHz.

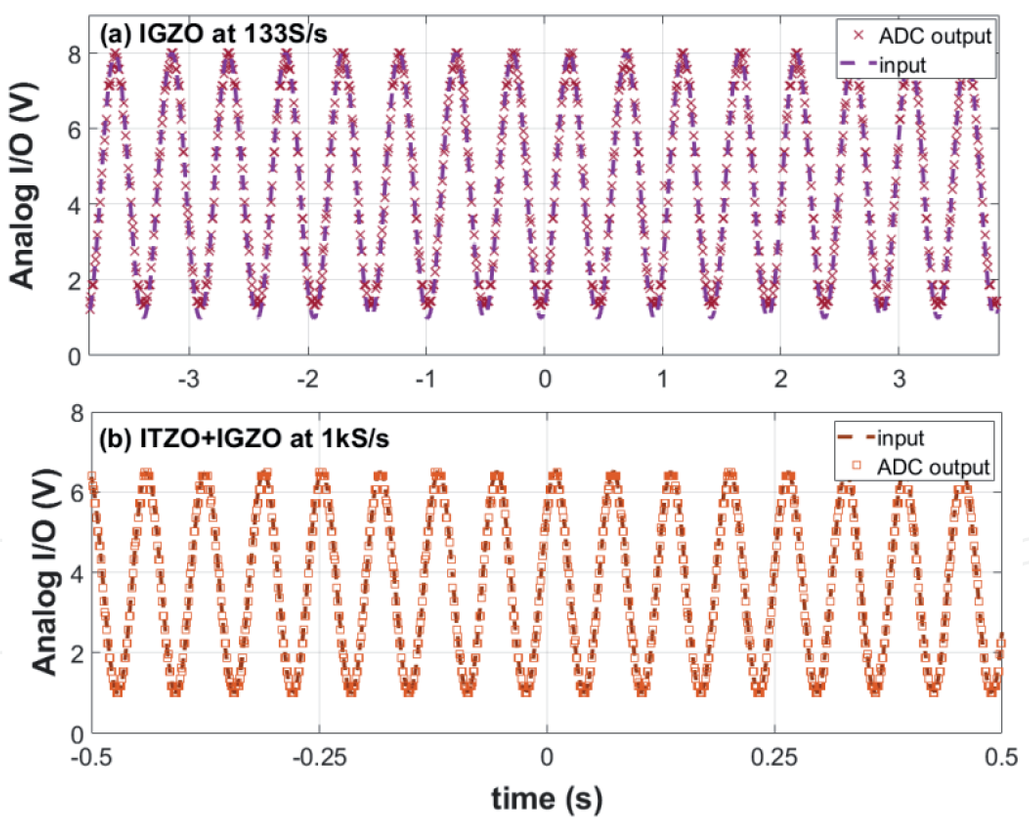

Figure 20.
(a) The applied analog input of 2.061 Hz sinewave signal to the ADC and the reconstructed output points from the digital output of the ADC at a clock frequency of 2 kHz for IGZO and (b) the applied analog input of 15.625 Hz sinewave to the 15 kHz clocked ITZO ADC and the reconstructed output.

In **Figure 19** the response of the L = 5 μm comparator is shown validating 10 kHz operation, 5 times faster compared to the 20 μm comparator used in the ADC. This indicates that 5 μm comparator can increase the sampling speed by 5 times.

Another option to enable a larger increase of the ADC speed is to introduce ITZO TFT for the ADC. ITZO TFT exhibits 5 times larger I_{ON} which leads to faster

responses [**Figure 20(b)**]. The ITZO ADC achieves a similar bit resolution of the applied sinusoidal wave at 1 kS/s sampling speed and at 10 V supply voltage. Combining both ITZO and downscaling of the length of the TFTs of the comparator will lead to sampling speeds above 4 kS/s as required for the in-panel readout system of 1 fps. The power dissipation of the ITZO ADC is at 550 μW at 10 V power supply and at 110 μW at 15 V power supply for the IGZO implementation.

In conclusion, TFT-based in-panel analog circuits for 1 fps readout of a fingerprint or palmprints array is presented in this paragraph. The circuit blocks can be integrated side-by-side to the flat panel display with integrated sensor array. Two analog blocks are discussed, being an analog to digital converter and charge sense amplifier. ADCs and CSA downscaling to 5 μm including a 500% I_{ON} boost of the ITZO TFTs enable the 4 kS/s operation specifications for the in-panel readout circuits. The use of complementary technologies such as LTPS or LTPO would result an increased performance for important parameters such as the gain-bandwidth and the resolution and speed of the ADC. This will enable a better optimized system for this application.

6. Conclusions

In this book chapter, we have discussed a roadmap to include additional functionalities on displays by adding a fourth pixel to the display. The purpose of the fourth pixel in this work was a photodetector pixel to realize an in-panel fingerprint or palmprinting function. Several options have been discussed to enable this roadmap. At first, we have elaborated several techniques to realize higher-resolution frontplane (OLED) and TFT backplanes. For the frontplanes, photolitho patterning of the OLED was introduced as a disruptive technology impacting significantly the frontplane resolution. External compensation techniques for the backplane when driving OLEDs are proposed in this book chapter, resulting in a uniform and higher-resolution display by using only 2T1C schemes. As photodetector pixel, we proposed a passive 1 T pixel, with included peripheral circuits to enable a lower system cost.

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