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Chapter

Development and Characterization of High-Quality HfO_2/InGaAs MOS Interface

Sukeun Eom, Min-woo Kong and Kwang-seok Seo

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Abstract

The scope of this chapter is to introduce a highly efficient HfO_2 atomic layer deposition (ALD) process with superior interface defect characteristics that can be applied on high-mobility III-V substrates. For a long time, the major academic research of III-V metal-oxide-semiconductor (MOS) studies was mainly oriented on searching for the suitable high-k dielectric, and among the reported high-k/III-V MOS studies, Al_2O_3 and AlN have demonstrated the most promising results. However, usually, the dielectrics with higher dielectric constant suffered from more defective interface quality including the HfO_2, which should be overcome to meet the intensive operation voltage scaling requirements. In order to protect the interface of the HfO_2/III-V MOS, the exposed III-V surface has to be carefully treated before, while, and after the whole high-k deposition process. For this purpose, the effect of isopropyl alcohol precursor and in situ cyclic nitrogen plasma treatment on the HfO_2 ALD process at III-V substrates was thoroughly investigated. Remarkable interface state density levels with strong inversion behavior were achieved, which have not been observed at the previous HfO_2/InGaAs studies. Also, detailed analysis of the interface characteristics was investigated to broaden the understanding of the improvement phenomenon.

Keywords: high-k oxides, hafnium oxide (HfO_2), atomic layer deposition (ALD), III-V channel, indium gallium arsenide (InGaAs), metal-oxide-semiconductor (MOS)

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1. Introduction

Over the past decades, the semiconductor foundry business has gone through a dynamic transformation. Recently, the foundries are leading the process development race at 10 nm [1, 2] and even to 7 nm [3, 4] and will continue to do so. However, the traditional physical scaling of advanced MOSFETs in conjunction with Dennard's scaling rules has become extremely challenging as to increase the drive currents for faster switching speeds at lower supply voltages is largely at the expense of large leakage current in extremely scaled device [5]. As a result, even with the huge R&D investments, the semiconductor firms gradually lagged the advertised on-chip feature sizes demonstrated in the scaling roadmap, and finally the end of Moore's law has been declared with the end of the 2016 International Technology Roadmap of Semiconductors (ITRS) [5, 6]. Also, the emergence of internet of things (IoT) and big data applications has driven a necessity of abundant

computing and memory resources that requires always-on and high-performance ultralow-power devices to generate data instantly. Several device architectures and novel materials based on both analytical and experimental academic research were proposed in the metal-oxide-semiconductor field-effect transistor (MOSFET) technology. Among the viable technologies, the compound semiconductor especially the III-V materials have stood out to be a promising channel candidate for the future highly scaled CMOS application.

The light effective mass of III-V materials compared to the Si even in the highly strained case leads to a higher electron mobility and a higher injection velocity, which should translate into a great turn-on performance even at a lower operation voltage (V_{DD}) level down to 0.5 V. Moreover, there is already a mature industry that uses III-V high electron mobility transistors (HEMTs) for high-frequency applications [7, 8], and it provides excellent techniques such as InGaAs and InAs quantum well (QW) FETs [9, 10]. However, most of these III-V compound semiconductors have smaller bandgaps, which have great impact on the band-to-band tunneling leakage currents. In addition, according to Yan's model [11], the higher permittivity of these materials may worsen the short channel effects (SCE). In spite of the demerits that may limit the scalability, the benefits are much more attractive which makes the III-V channel technology a powerful beyond CMOS solution. However, the use of III-V compound semiconductors has been reluctant to the industry because of its high-cost manufacturing process and CMOS-incompatible process. Naturally, it brought out a strong motivation of research of III-V hetero-integration on a Si platform. The main obstacle of III-V on Si integration research is that as huge lattice constant mismatch exists between those two materials, growing epitaxial films directly on Si without defect is difficult [12]. Accordingly, different approaches have been developed, and among them, direct wafer bonding [13, 14] and aspect ratio trapping (ART) [15, 16] technologies have projected the most promising results.

Consequently, the remaining issue toward the practical realization of III-V materials is its defective interface quality which has been the major drawback compared to Si [17–21]. The poor native oxide quality compared with SiO2 is challenging even more with III-V materials. The III-V compound semiconductors are typically composed of binary, ternary, or even quaternary material by covalent bonding, and more complex elements mean a much richer population of possible oxides for the III-V materials [22]. These native oxides are not thermodynamically stable and very leaky that rise serious issues of creation of significant surface states on the oxide-semiconductor interface and huge trap-assisted gate leakage current [17, 19]. At the early stage of research, GaAs MOSFET suffered from high density of interface states (over 3 orders compared to Si) hindering inversion mode operation.

In order to overcome the defective interface problem, many research groups conducted extensive research effort with a search for a perfect gate dielectric that suits the III-V substrate [23, 24]. The study of atomic layer deposition (ALD) high-k dielectric led to a successful integration of high-k gate dielectrics on III-V substrate, and recent research is mainly focused on the development and interface characterization of ALD high-k and III–V compound semiconductor. To evaluate the objective III-V metal-oxide-semiconductor (MOS) characteristics, it is important to understand the trapping mechanism and know what kind of measurement is required. For Si, the primary defects are the well-known P_b centers, which are dangling bonds at the immediate interface with the dielectric [25]. However, for the III-V material, the anti-sites and interstitials are the critical defect centers [17], and the small DOS of the III-V materials is also a weak point [26]. These differences lead to different trapping mechanism, and unlike Si MOS, the III-V MOS gate stack often exhibits a particular C-V phenomenon typically known as the frequency dispersion effect [27].

The features of the frequency dispersion effect are threefold. First, large inversion-like hump occurs even at high measurement frequency, which could not be an actual inversion characteristic theoretically. Secondly, the C-V curve horizontally shifts to the negative direction as the measurement frequency decreases. Finally, the accumulation capacitance increases as the measurement frequency decreases.

The large interfacial trap densities (D_{it}) that reside within high-k dielectric and III-V substrate are mostly responsible for the explained features [28]. The high D_{it} especially the near mid-gap states act as generation recombination centers that attribute to the inversion hump phenomenon in the weak inversion regime. In addition, the large donor-like D_{it} near the conductance band (for n-type substrate) induces a substantial surface charge that needs to be compensated by larger gate biases resulting in a horizontal shift in the C-V curve. Detailed discussions are well explained through both theoretical and experimental research [27, 28]. The accumulation capacitance increase, however, is quite difficult to be explained only by the interface traps. There have been numerous publications on this particular accumulation dispersion behavior, and discussion led to an explanation of a carrier transport model from the crystalline semiconductor into the border traps, which are defects within the bulk of the dielectric [29]. The capture and emission process occur at border traps with the interaction of conduction band electrons resulting in discrepancy of accumulation capacitance, and the thermal barrier in capture process is responsible for the strong temperature dependency.

Among the reported high-quality insulator/InGaAs interface studies, the direct deposition of hafnium oxide (HfO_2) on InGaAs substrate has generally led to poor electrical characteristics, and there are only few studies aimed at improving the intrinsic HfO_2/InGaAs interface quality [30, 31]. These studies also target only in pretreatments, which is vulnerable during oxide deposition. Meanwhile, O_3 and H_2O are the most common oxidants employed in HfO_2 ALD. However, one of the disadvantages of H_2O-based ALD is high-concentration hydroxyl groups in the films, which degrades the dielectric interface during the post deposition annealing process [32]. In addition, sufficiently long purge time is needed because H_2O tends to physisorb on the surface strongly, especially at low temperature. To solve this problem, O_3 is used as one of the most promising alternative oxidants in ALD process, due to its strong oxidization and high volatility. However, O_3 is known to oxidize the III-V surface during the initial deposition cycles which will neglect the prior surface treatments that easily cause the formation of inferior native oxides [33]. The excess interfacial oxidation of the InGaAs surface initiated by the use of ozone is widely reported in the previous studies. H_2O oxidant also is not totally free from surface oxidation [34]. Therefore, the research on alternative oxidation sources is necessary for the HfO_2/InGaAs MOS studies to make the effort made in the pretreatment studies work.

2. Development of IPA-based ALD HfO_2 on n-type InGaAs substrates

Looking into the oxidant candidates, isopropyl alcohol (IPA) is known to be irresponsive to the semiconductor surface during the initial ALD cycles [35], and as most pretreatment studies are aimed at removing the native oxides of the III-V surface, the IPA oxidant will be able to efficiently suppress the surface oxidation after the pretreatment process.

In order to study the effect of using IPA oxidant, O_3 was used as the reference to compare. The basic cycle of the HfO_2 deposition is consisted of a TEMAH precursor pulse and an oxidant (O_3 or IPA) exposure with N_2 purging process between the precursor injection and oxidant process. The temperature of the IPA precursor was

maintained at 4°C. The vapor pressure of IPA at 4°C is around 10 mmHg, which is four times smaller than that at the room temperature [36]. It is important to control the excessive vapor pressure because it leads to a longer purge time, which disables an efficient ALD cycle.

The ALD characteristics of HfO_2 using O_3 and IPA oxidants are shown in **Figure 1**. Oxidant pulse times were 1 and 3 s for O_3 and IPA, respectively, which

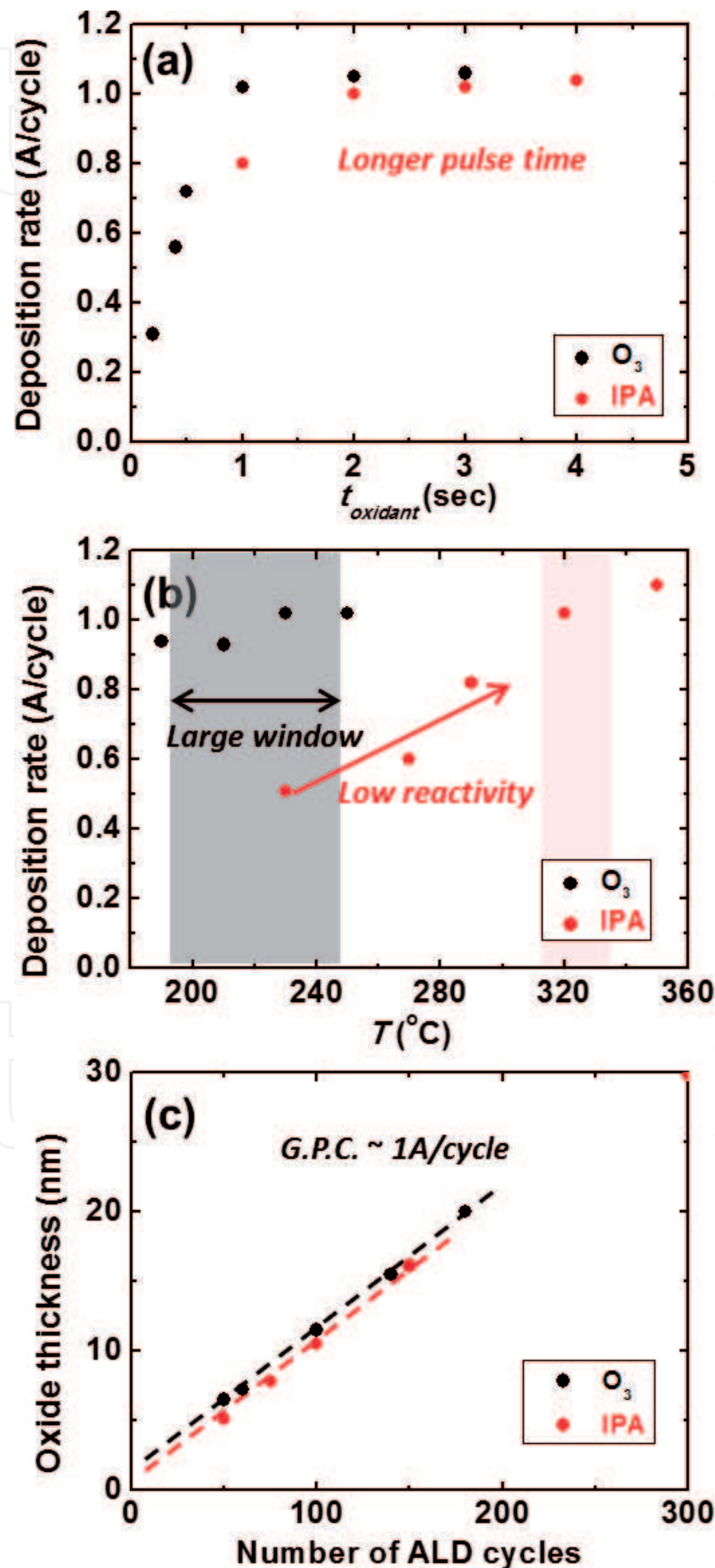

Figure 1.
Comparison of the O3- and IPA-based HfO2 ALD characteristics: (a) deposition rate vs. oxidant time, (b) deposition rate vs. deposition temperature, and (c) growth per cycle rate.

were chosen to meet the saturation requirement of ALD. Both oxidants had similar saturated deposition rate of 0.1 nm/cycle. Noticeable difference was observed in the temperature windows of oxidant type. While stable deposition rate of O_3 oxidant was maintained in a large temperature range, saturated deposition rate of IPA oxidant was only observed in a small temperature range around 320°C. In low temperatures, low deposition rate is due to insufficient reaction which is originated from low reactivity of IPA. Also, in high temperatures above 320°C, thermal decomposition of Hf precursor occurs, and it hinders the self-limiting characteristics of ALD. Therefore, the deposition temperatures of HfO_2 ALD were chosen to be 230 and 320°C for O_3 and IPA, respectively. Moreover, the film thickness per ALD cycles is presented. It is observed that the linear deposition rate per cycle is obtained for both oxidants and a thicker interface layer thickness appears to be existed for the O_3 oxidant due to is strong reactivity (**Figure 2**).

Based on the ALD characteristics, the HfO_2/Si MOS capacitors are fabricated on the Si substrate. All samples underwent standard Si cleaning steps that consisted of SPM- and HF-based cleaning and 400°C 10 min annealing after the dielectric deposition. The C-V and forward gate leakage characteristics are measured and discussed. First of all, the C-V hysteresis difference is notable. As anticipated, the C-V hysteresis significantly decreases by employing the IPA oxidant. Powerful

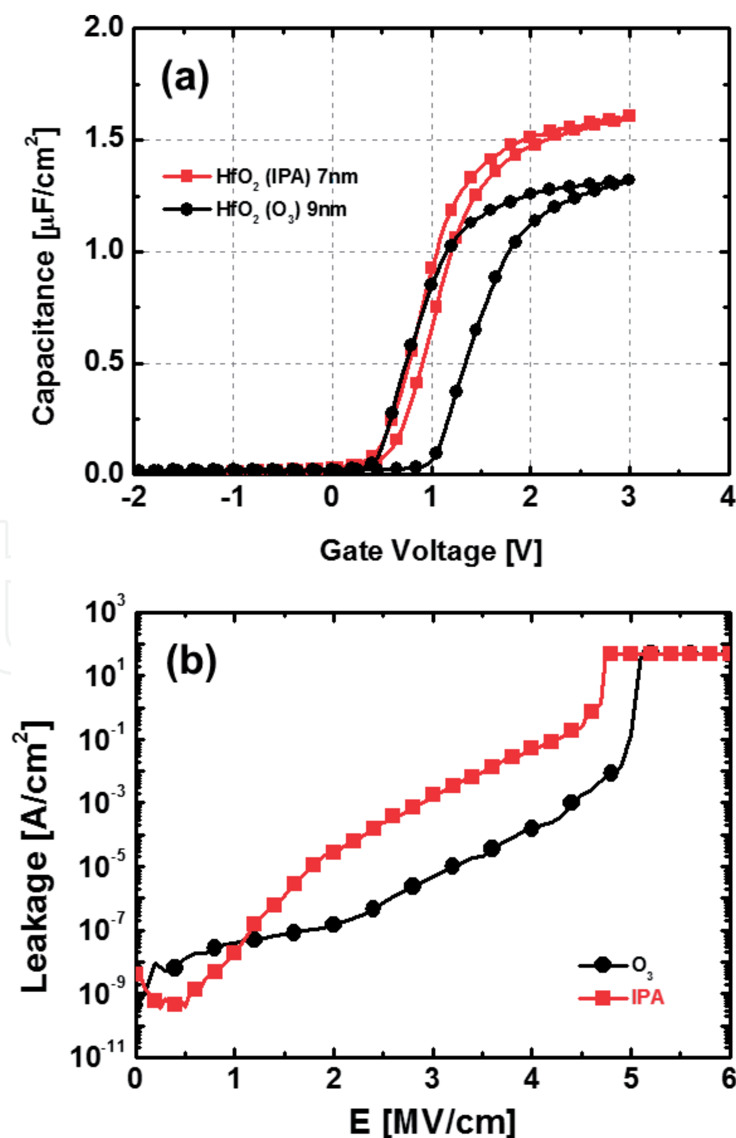

Figure 2.
Comparison of O_3- and IPA-based HfO_2/Si MOS capacitors: (a) C-V and (b) leakage-E plot.

oxidation ability of ozone may induce undesired interfacial oxide at the Si interface forming defective hafnium silicate leading to a large hysteresis, while IPA-based HfO_2 appears to be negligible on this effect [37]. The dielectric constants of IPA-based and O_3-based HfO_2 extracted by the thickness series method are 19.4 and 17.6, respectively [38]. While the C-V results report promising potential of IPA oxidant in ALD HfO_2, the leakage properties suggest a different aspect. Leaky forward gate leakage especially in the medium gate voltage range of the IPA-based HfO_2 is presented compared to the O_3-based HfO_2. It is well known that at this gate bias range, the dominant leakage mechanism is by the Poole-Frenkel tunneling, which is a conduction method of electron tunneling from a metal electrode to traps in a nearby insulator layer, followed by detrapping of the electrons from the traps by virtue of a lowered potential well due to an applied electric field [39]. It usually implies the bulk quality of dielectric; in short, the larger the leakage in this E-field is, the more inferior the gate insulator is. It is speculated that by using the IPA oxidant, the bulk quality may be inferior than using the O_3 oxidant in ALD HfO_2. This might affect the further scaling down potential and the border trap density in ALD HfO_2 application on InGaAs substrate [40].

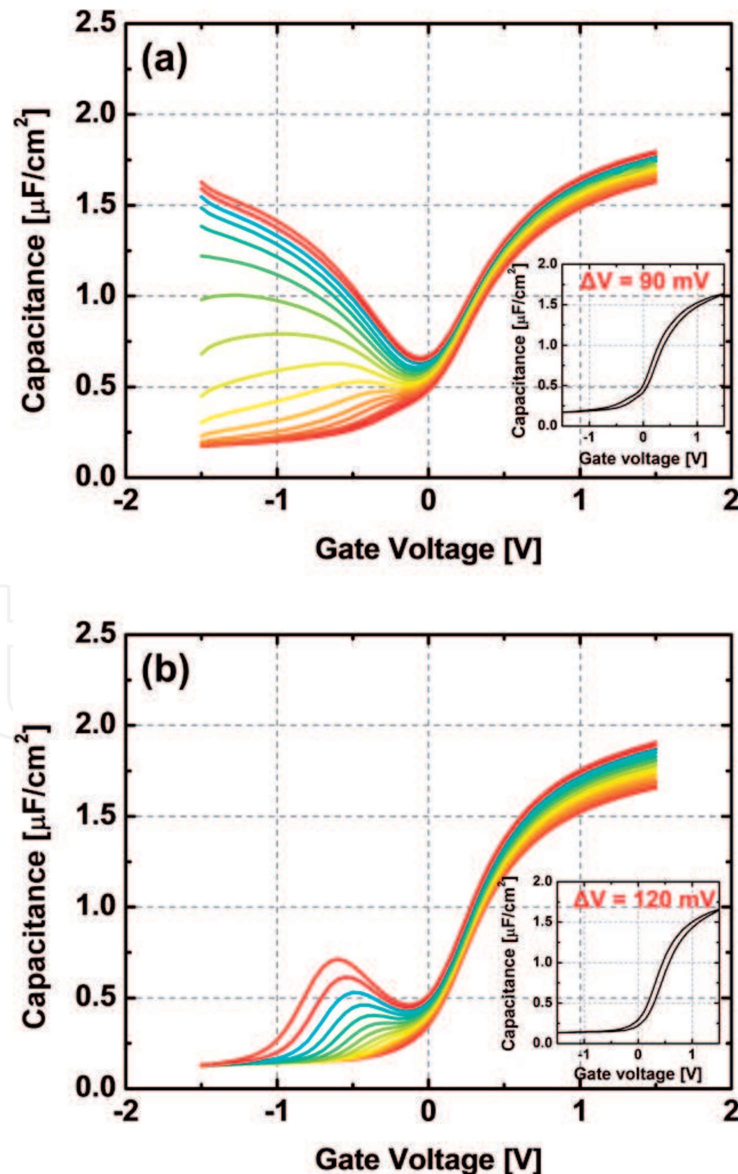

Figure 3.
Multifrequency C-V responses of (a) O_3- and (b) IPA-based HfO_2/In0.53Ga0.47As MOS capacitors; insets are the hysteresis at 1 MHz.

By using the developed O_3- and IPA-based HfO_2 dielectrics, HfO_2/InGaAs MOS capacitors were successfully demonstrated [41]. The multifrequency (1 kHz–1 MHz) C-V characteristics of HfO_2/n-$In_{0.53}Ga_{0.47}As$ MOS capacitors using the O_3 and IPA oxidants are presented in **Figure 3**. The C-V curves of the O_3-based HfO_2 ALD showed a large inversion hump in the negative bias range, which is attributed to the large density of interface defect states near the mid-gap trap level. In contrast, those of the IPA-based HfO_2 ALD showed a notable suppression of the inversion hump behavior. In addition, by employing the IPA oxidant, the effective oxide thickness (EOT) has decreased. We hypothesize that the reduced inversion hump and decrease of the EOT originate from the suppression of unintentional interfacial oxides by the use of the IPA oxidant. Detailed material characteristics analysis was conducted and proved the hypothesis to be convincing [41]. To our knowledge, it is the first successful demonstration of HfO_2 deposition using IPA at InGaAs substrate.

Despite the advantages of using the IPA oxidant, frequency dispersion at the accumulation region slightly increased from 3.3 to 4.7% per decade. In **Figure 4**, these values were used to estimate the border trap densities (N_{bt}) by using a distributed bulk-oxide trap model, and increased N_{bt} of 1.1×10^{20} cm^{-3} eV^{-1} was extracted compared to 6.7×10^{19} cm^{-3} eV^{-1}. Also, larger C-V hysteresis and severely degraded

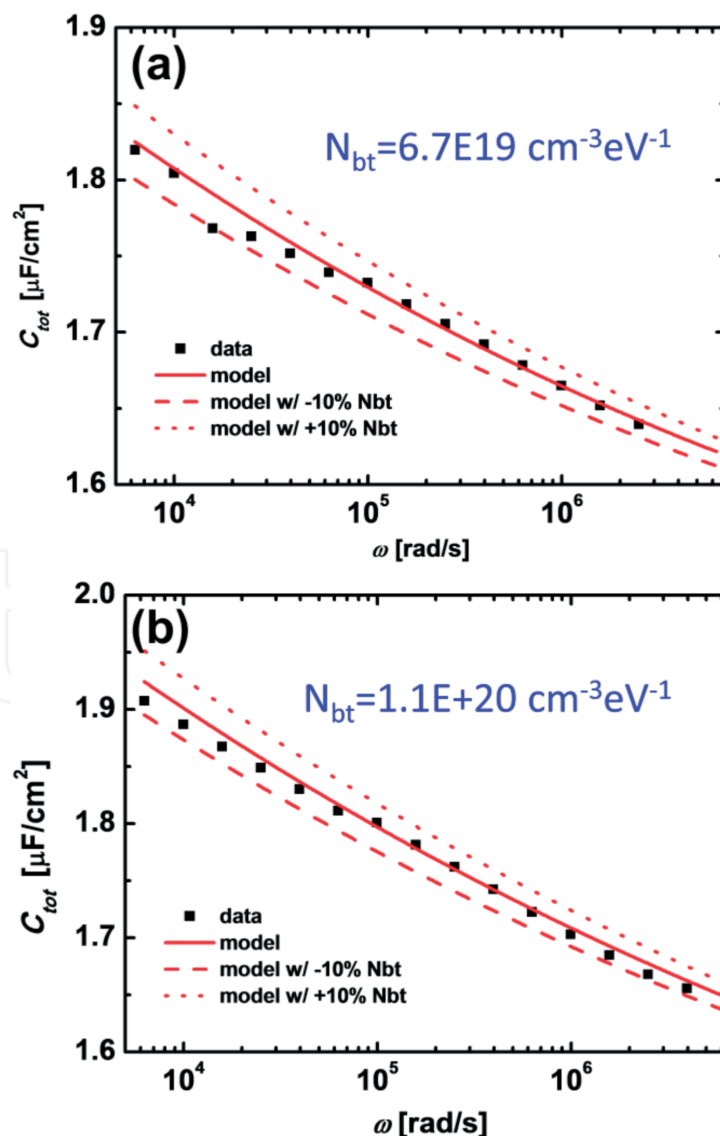

Figure 4.
Border trap estimation of HfO_2/InGaAs MOS capacitors by using the distributed oxide bulk trap model (a) O_3-HfO_2 and (b) IPA-HfO_2.

leakage currents at positive bias are noticed. Based on these results, an inferior quality of the HfO_2 film for using IPA oxidant was predicted which should be resolved for reliable use of the IPA oxidant.

In order to improve the weak IPA-based HfO_2 bulk quality, the study of origin in HfO_2 defect is necessary. One of the main concerns in the replacement of SiO_2 to HfO_2 is that compared to SiO_2, HfO_2 generally suffers from high defect densities leading to several issues such as large carrier trapping, mobility degradation due to coulombic scattering in the channel surface, and threshold voltage shifts in gate stress conditions [42]. To be specific, the threshold voltage shift issue was not a new phenomenon that suddenly happened with use of HfO_2. In immature SiO_2 MOSFETs, it is widely known that the extrinsic contaminations in SiO_2 with alkali ions induce this similar phenomenon [43]. However, with HfO_2, it appeared to be caused by the high defect concentrations, which originated from a more fundamental problem, not an extrinsic defect. Consequently, many researches were devoted to HfO_2 physical model simulation in order to identify the type of defects and their energy levels, and by these physical studies, researchers hoped to learn how the deposition and processing conditions can be optimized to minimize these defect origins [42, 44, 45].

Based on computational calculations, it is identified that oxygen vacancies in HfO_2 are both the principal trap and main cause of the discussed issues, and its formation energy and energy levels were also calculated [44]. Hence, in order to reduce the defect densities, experiments regarding deposition and post processing conditions were aimed to remove or passivate these defects, with an oxygen-rich ambient. However, in many cases, it only worked to some extent and led to new issues of excessive oxidation leaving oxygen interstitials and oxygen diffusion to the interface [46].

Additionally, due to the low density of states of III-V semiconductors, III-V substrates are heavily influenced to border traps that could severely worsen the device performance resulting in poor reliability properties. Therefore, not only the interface but also the bulk characteristics of HfO_2 should be considered in III-V MOS studies, and improvement in both qualities is definitely important.

One of the most effective methods to improve the inherent properties of HfO_2 is the incorporation of nitrogen to passivate oxygen vacancies, and it has been extensively utilized in many recent studies [47–51]. Significant improvement in the electrical characteristics of various high-k gate dielectrics by nitrogen incorporation has been demonstrated, and it is found that interfacial layer growth is effectively suppressed [49] and there is lower boron penetration with nitrogen incorporation [51]. Also, lower leakage current density in HfO_xN_y is widely reported due to suppression of oxygen vacancy traps [50]. It has been reported that nitrogen incorporation in HfO_2 can be achieved by several methods mostly by nitrogen ambient plasma-based nitridation [47, 50] or ammonia (NH_3) ambient high-temperature annealing treatment [52, 53]. For Si-based MOS studies, the later approach is known to be very powerful for achieving good uniformity of nitrogen incorporation and excellent interface quality due to the absence of plasma damage. However, in order to successfully apply nitrogen incorporation technology on III-V substrate, the low thermal budget of III-V compound semiconductor always has to be considered, and high-temperature annealing treatment should be ruled out for nitrogen incorporation study in III-V MOS. In the other hand, although plasma-based nitridation technology offers low thermal budget capacity, most studies generally suffers from several issues such as nonuniform nitrogen distribution throughout dielectric, plasma-induced damage due to high-power plasma for dielectric penetration, and high energy potential nitrogen species substituting well-combined Hf-O bonds. Post deposition plasma treatments have recently been suggested for InGaAs MOS

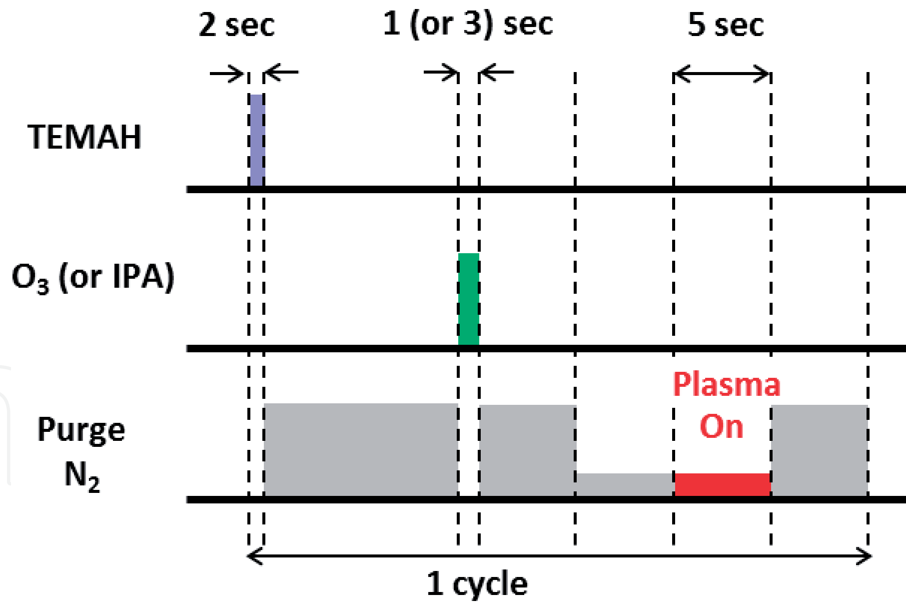

Figure 5.
ALD cycle sequence of the developed HfO$_x$N$_y$ processes on InGaAs substrates.

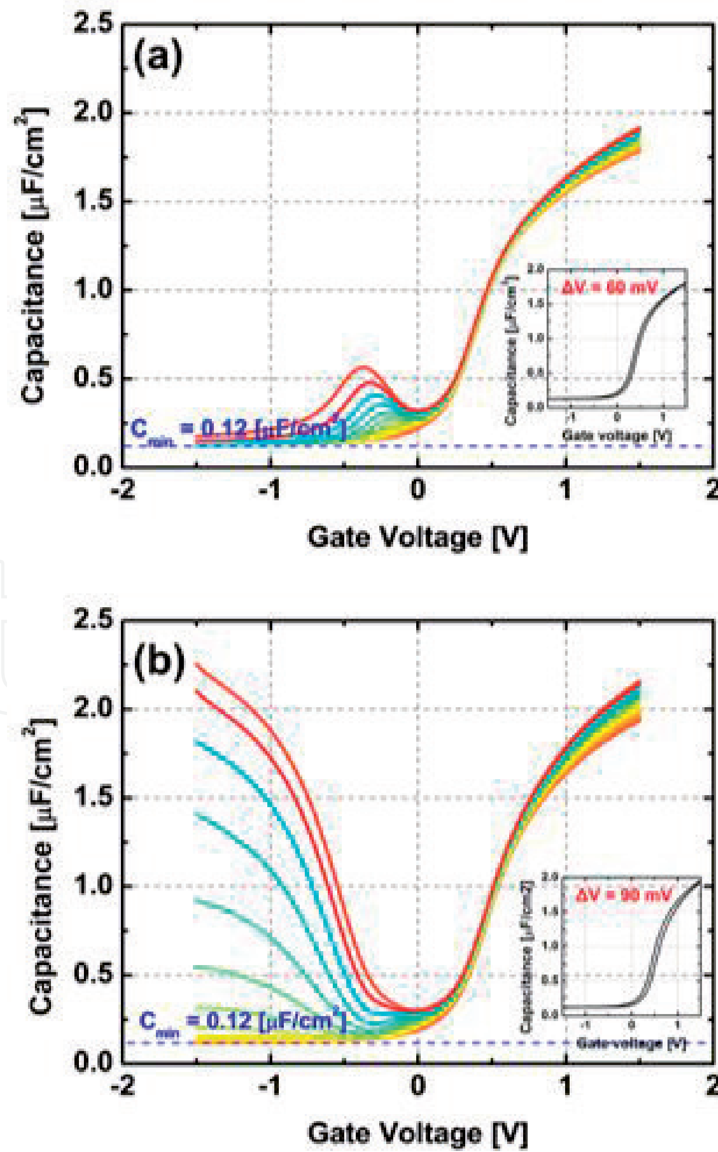

Figure 6.
Multifrequency C-V responses of (a) O$_3$- and (b) IPA-based HfON/In$_{0.53}$Ga$_{0.47}$As MOS capacitors; insets are the hysteresis at 1 MHz.

devices [54]; however, no effort was made to improve the nitridation technology regarding the discussed issues.

As a result, in order to improve the film quality of HfO_2, a cyclic nitrogen low-power plasma step was added within the ALD cycles to passivate oxygen vacancies uniformly without causing damage or surface degradation. Through this technology with a combination of IPA oxidant, achievement of improvement in both interface and bulk quality of high-k/InGaAs MOS properties is expected. The detailed information of the ALD sequence is depicted in **Figure 5**. Every cycle consisted of sequential precursor pulse steps and a gas stabilization step followed by 5 s of 50 W N_2 plasma step with purge steps between pulse steps. It is discovered that there is a trade-off relationship of plasma condition. The plasma power should be enough for effective passivation although it may degrade the substrate by radiation damage. Through the developed ALD sequence, with adequate plasma condition, the HfO_2 layer is improved without having influence in the substrate.

By using the proposed nitridation technology, HfO_xN_y/InGaAs MOS capacitors are fabricated showing promising results as shown in **Figure 6** [41]. A significant suppression of the frequency dispersion was observed upon nitrogen incorporation in every gate bias range. The inversion humps and flat band voltage shift were effectively reduced for all samples, which imply that the defective interface states

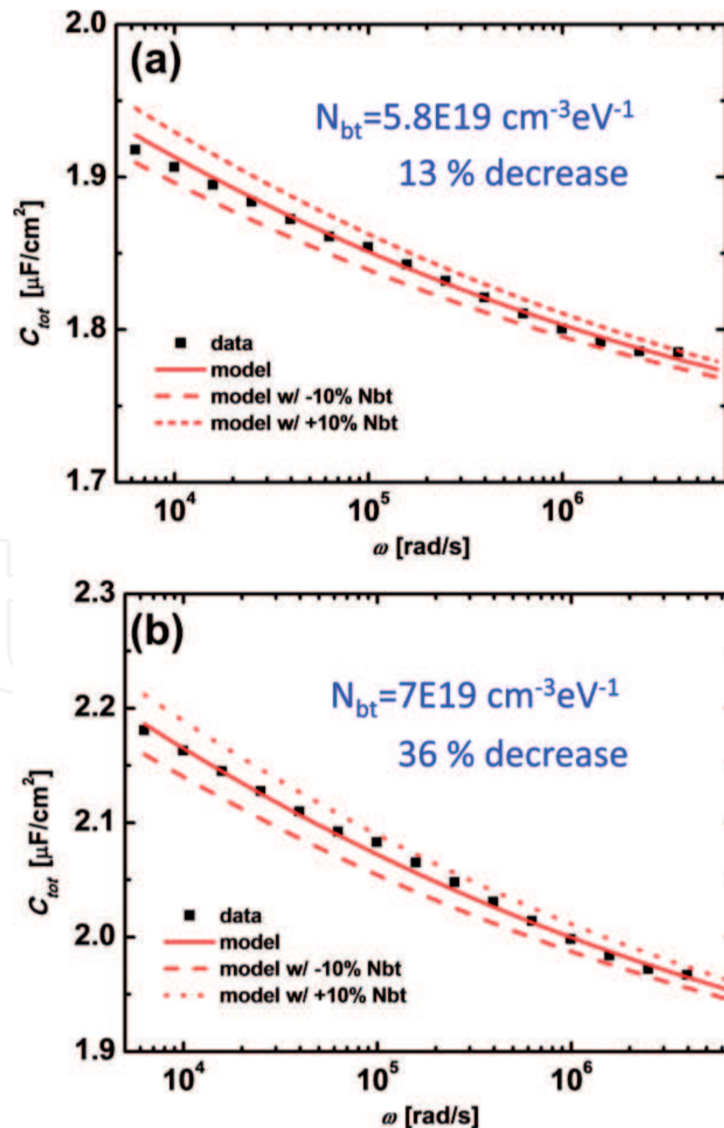

Figure 7.
Border trap estimation of HfON/InGaAs MOS capacitors by using the distributed oxide bulk trap model (a) O_3-HfON and (b) IPA-HfON.

near the mid-gap level can be treated with nitrogen incorporation. It is hypothesized that oxygen diffusion through the oxygen vacancies of HfO_2, which results in the formation of As-Ga anti-sites, was greatly reduced, as oxygen vacancies were effectively passivated with nitrogen [17]. Therefore, nitrogen may block further oxygen diffusion, thereby preventing surface oxidation, which could occur not only during but also after dielectric deposition. Furthermore, the frequency dispersion in the accumulation region greatly reduced to 2.1 and 3.2% per decade for O_3- and IPA-based ALD, respectively. These values are comparable to suppressed dispersion values in low-EOT gate stacks, which imply excellent reliability quality of dielectric stacks on III-V substrate [55]. As the proposed nitridation technology is aimed to treat inferior bulk qualities of HfO_2, it showed greater impact on IPA-based HfO_2. The inversion behavior was observed for the IPA-based ALD HfO_2 which has not been reported from the former HfO_2/InGaAs MOS studies, and it will be further discussed (**Figure 7**).

3. Characterization of IPA-based ALD HfO_2 on n- and p-type InGaAs substrates

Based on the n-type MOS results, the D_{it} was extracted using the conductance method as shown in **Figure 8**. The combination of IPA oxidant and PA-ALD HfO_xN_y with standard interface treatments resulted in a reduced D_{it} level of $4.5 \times 1011\ eV^{-1}\ cm^{-2}$ at $E_c - E_t = 0.3$ eV. Based on the D_{it} distribution, it is evident that the inversion behavior observed in the C-V curves is due to the significant mid-gap D_{it} decrease, which is consistent with the previously reported studies. As the mid-gap D_{it} is known to correlate to the As-Ga anti-site defect and the ozone-based HfO_xN_y lacked inversion characteristics with high mid-gap D_{it}, these defects might be the reason why the inversion behavior is difficult to be achieved in most studies. Also, these defects might be formed in the initial ALD steps through the oxidant exposure. Also, in **Figure 9**, we have benchmarked our results, comparing them

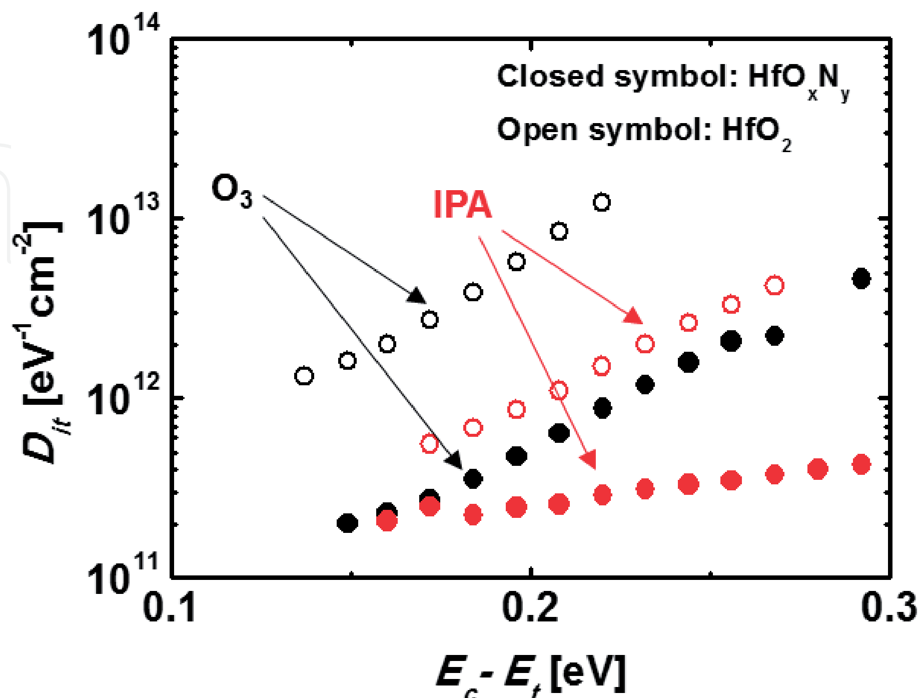

Figure 8.
The D_{it} distribution of the fabricated III-V MOS capacitors showing great reduction in the mid-gap D_{it} with the IPA-based HfO_xN_y.

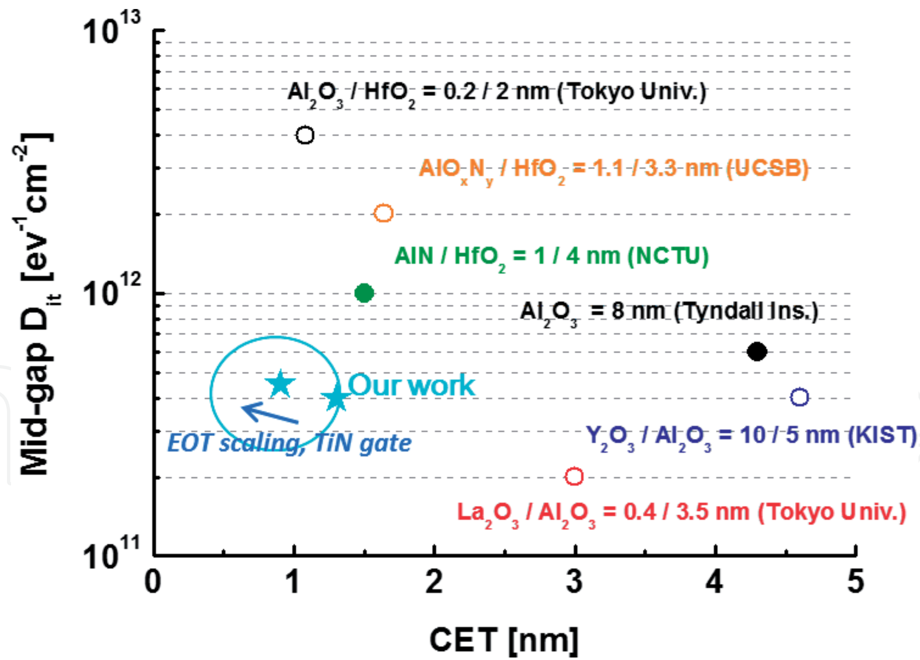

Figure 9.
Benchmarking the mid-gap D_{it} values of the proposed high-k ALD compared to the best results in the field of III-V MOS. The filled circles represent C-V curves with inversion behavior.

to the best results ever reported in the field of III-V MOS device studies [56–61]. Extraordinary mid-gap D_{it} values are achieved with low CET values with the proposed technology. Especially, while other studies mostly suffer from insufficient dielectric constant of the IL, our work employs HfO_2 as an IL, which has merit in terms of the EOT scaling.

In addition, with conductance method in the measurement frequency range of 1 kHz–1 MHz, the n-type MOS capacitor results can only provide information of D_{it} distribution near the conduction band. In order to estimate the total D_{it} distribution throughout the bandgap in InGaAs, p-type InGaAs MOS was fabricated and analyzed. The p-type InGaAs MOS capacitors are fabricated in the same process flow of n-type MOS capacitors.

The multifrequency C-V measurements of IPA-based PA-ALD HfO_xN_y/n-$In_{0.53}Ga_{0.47}As$ MOS capacitors compared to the HfO_2 (O_3) sample is presented in **Figure 10**. Compared to the reference, the optimized HfON process exhibits significant frequency dispersion suppression with steeper C-V slope. This result is comparable to the previously reported high-quality p-type InGaAs MOS results. It is assumed that the interface improvement mechanism is similar to the previous n-type MOS analysis.

Based on the results, the D_{it} distribution within the InGaAs bandgap is extracted with the conductance method shown in **Figure 11**. The D_{it} level at the exact mid-gap energy level ($E_g/2$ = 0.375 eV) is around 8×10^{11} eV^{-1} cm^{-2}. This value is still low for reported III-V MOS interface, and it is suggested that based on the D_{it} distribution, the accumulation mode n-channel III-V devices are favorable than the inversion mode p-substrate III-V devices because the overall D_{it} levels are much lower at the conduction band area.

Moreover, temperature-dependent conductance method was performed in order to analyze the mid-gap D_{it} level thoroughly. High-temperature (350, 400 and 450 K) multifrequency C-V analysis was conducted on HfON/InGaAs MOS capacitors. The C-V results of each measurement temperature are shown in **Figure 12**.

As the measurement temperature increases, the inversion response gets stronger at higher frequencies compared to the room temperature-measured results. Also,

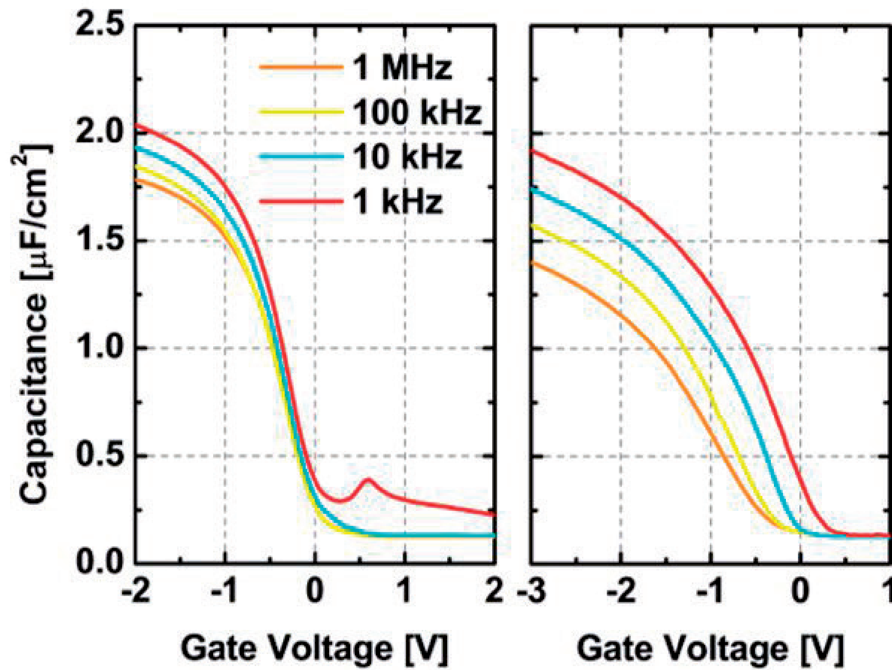

Figure 10.
C-V characteristics of IPA-based PA-ALD HfO_xN_y (left) and O_3-based HfO_2 (right) on p-type $In_{0.53}Ga_{0.47}As$ substrates.

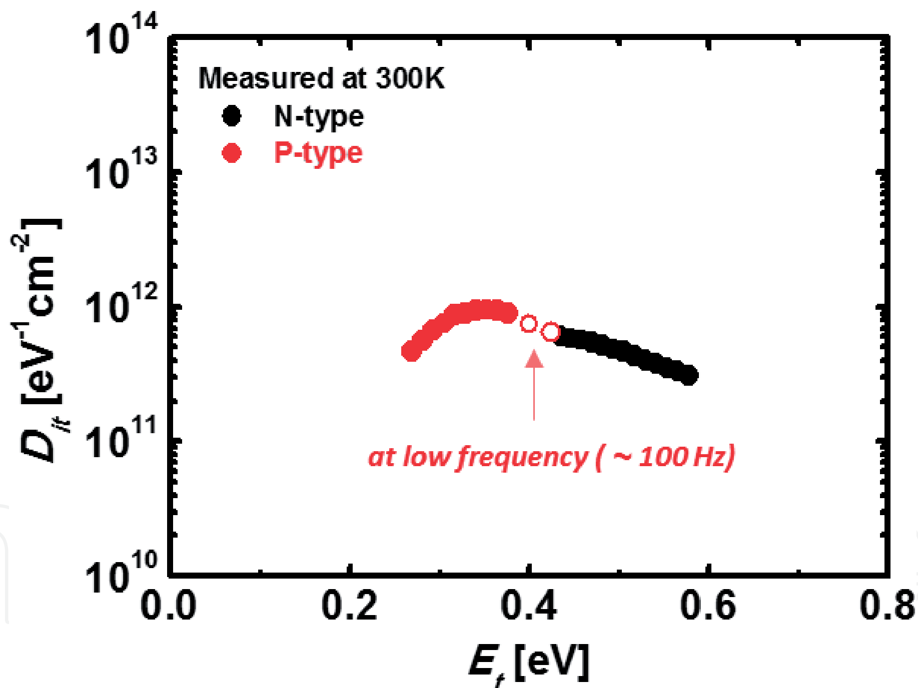

Figure 11.
The total D_{it} distribution within the $In_{0.53}Ga_{0.47}As$ bandgap, which is extracted from the n- and p-type MOS capacitors.

while the dispersion at the accumulation region seems to be similar, there was a significant impact on the inversion hump phenomenon which is the interface trap characteristic. The measurement noise at higher temperature and lower frequencies was also noted. When the measurement temperature reaches around 450 K, the strong inversion response occurs even at 1 MHz, and it interferes with the interface trap-related conductance peak making the deconvolution process impossible.

The D_{it} distribution was estimated from the temperature-dependent conductance technique as shown in **Figure 13**. As the measurement temperature increases, the

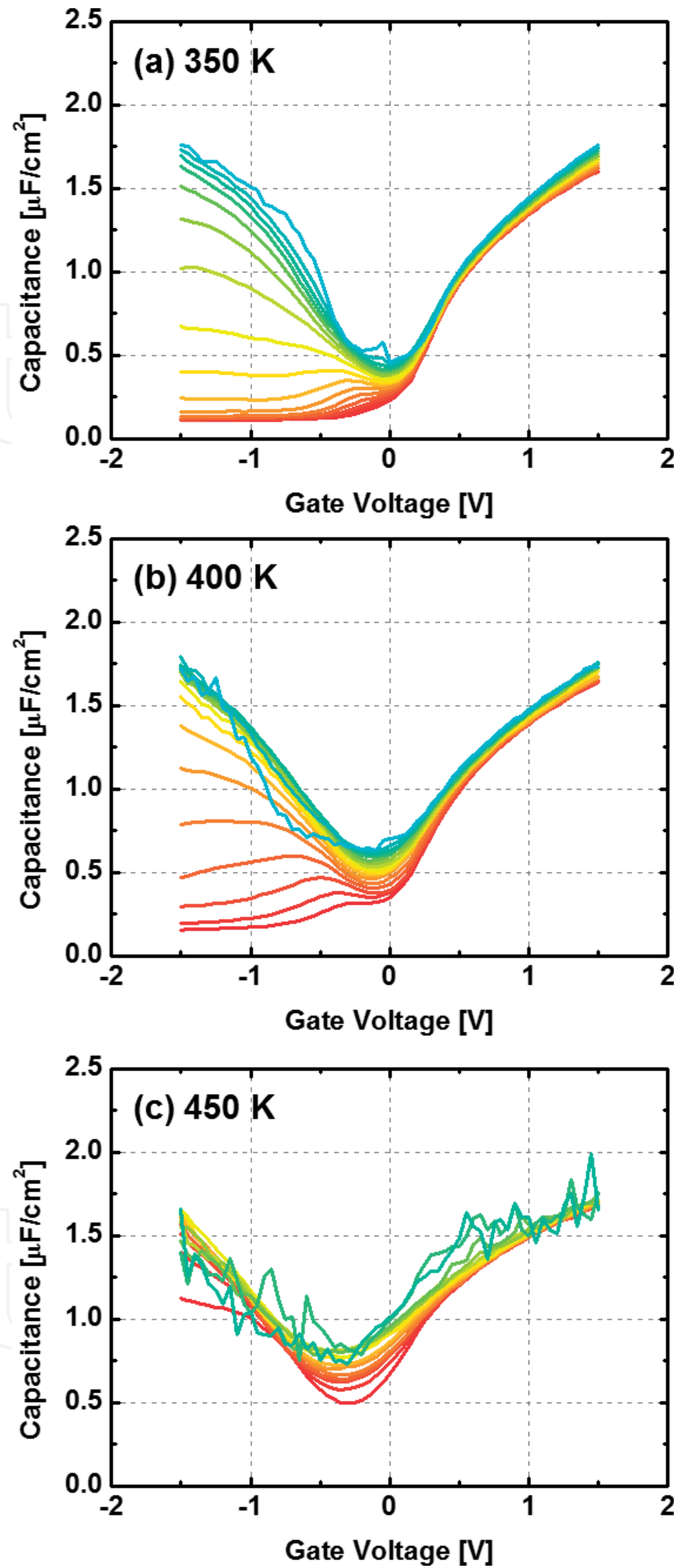

Figure 12.
C-V characteristics of IPA-based PA-ALD HfO_xN_y on n-type InGaAs substrate measured at (a) 350 K, (b) 400 K, and (c) 450 K.

deeper energy range could be measured. Similar D_{it} profile was observed showing a peak energy level around the exact mid-gap level (~0.375 eV). The peak D_{it} value is slightly higher than the previously estimated value which would be the effect of

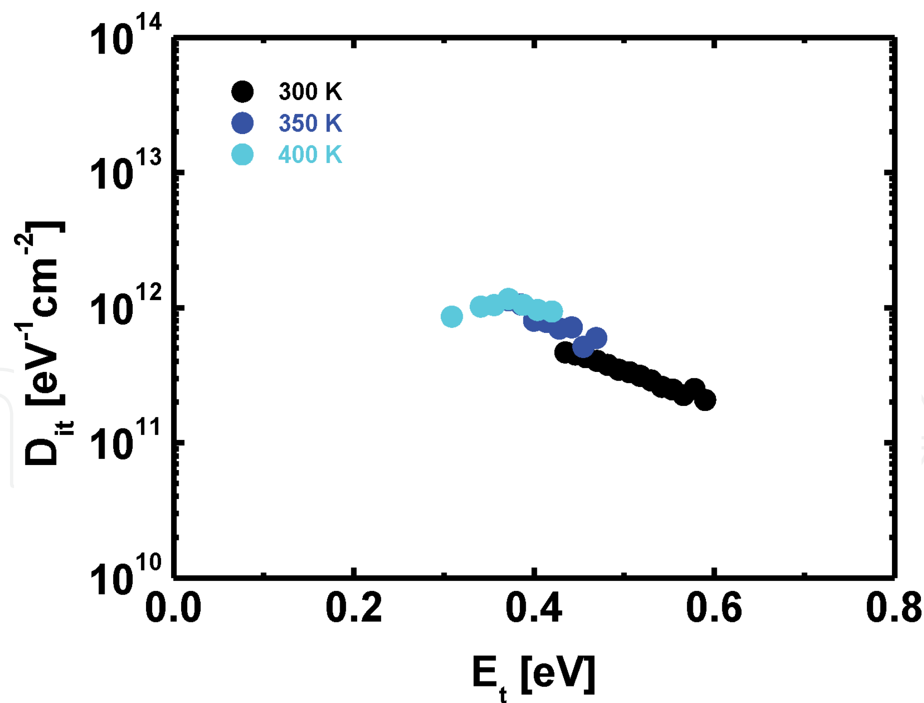

Figure 13.
The total D_{it} distribution within the $In_{0.53}Ga_{0.47}As$ bandgap, which is extracted from the temperature-dependent conductance method.

enhanced thermal broadening of trap response in higher temperatures. The differences between the D_{it} profile estimation can be summarized as follows: While using p-MOS capacitors, a larger energy level range is observable with no thermal broadening of the trap response due to the fixed measurement temperature. On the other hand, using a temperature-dependent method has a thermal broadening issue but only requires one sample for characterization.

It was noted that the inversion behavior of IPA-based HfO_xN_y ALD is attributed to the mid-gap D_{it} level decrease. However, in order to verify true inversion characteristics, more analyses must be investigated. In **Figure 14**, the conductance profile of sample O_3-based HfO_2 and IPA-based HfO_xN_y InGaAs MOS capacitors are depicted.

Both C-V profiles have shown inversion-like behavior in the negative bias region. However, clear difference is observed between the conductance profiles. While huge and Gaussian conductance profiles in the negative bias regions are observed for O_3-based HfO_2, smaller Gaussian conductance peaks are observed in depletion region, and distinct from these peaks, saturated conductance profiles are observed for IPA-based HfO_xN_y. Therefore, it is concluded that the inversion-like behavior in O_3-based HfO_2 is attributed from the huge and broad conductance peaks that reflect high mid-gap D_{it} levels, while inversion behavior in IPA-based HfO_xN_y might be attributed from real true minority carrier inversion.

In **Figure 15**, to verify true inversion characteristics of IPA-based HfO_xN_y, the minority carrier response was investigated based on the extraction of the transition frequency, w_m, which is known to be a characteristic of a strong inverted surface for III-V MOS capacitors [62]. It is known that at the transition frequency, the $-wdC/dw$ and G_m/w share the same peak magnitude in the strong inversion gate bias. Notably, $-wdC/dw$ and G_m/w share the same peak magnitude at the same transition frequency of 4 kHz which suggests that IPA-based HfO_xN_y exhibits true inversion behavior. The true inversion behavior of hafnium oxide-based dielectrics on InGaAs substrate has not been reported yet which implies significant potential.

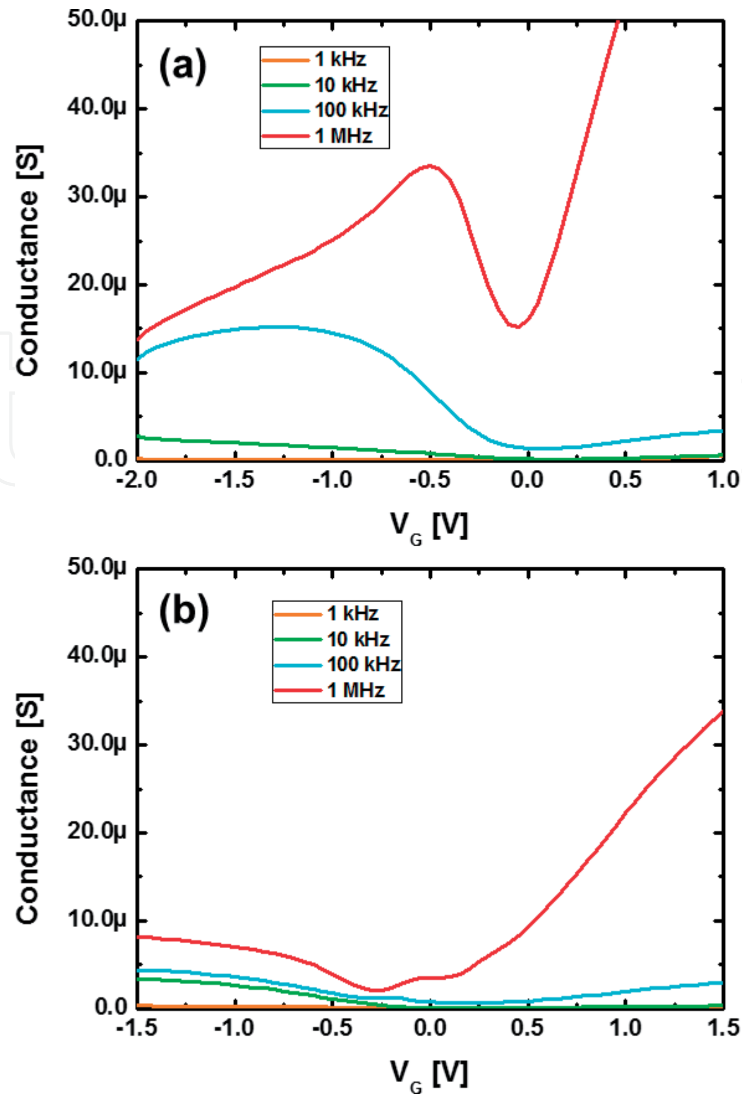

Figure 14.
The conductance profiles for (a) O_3-HfO_2 and (b) IPA-HfON ALD.

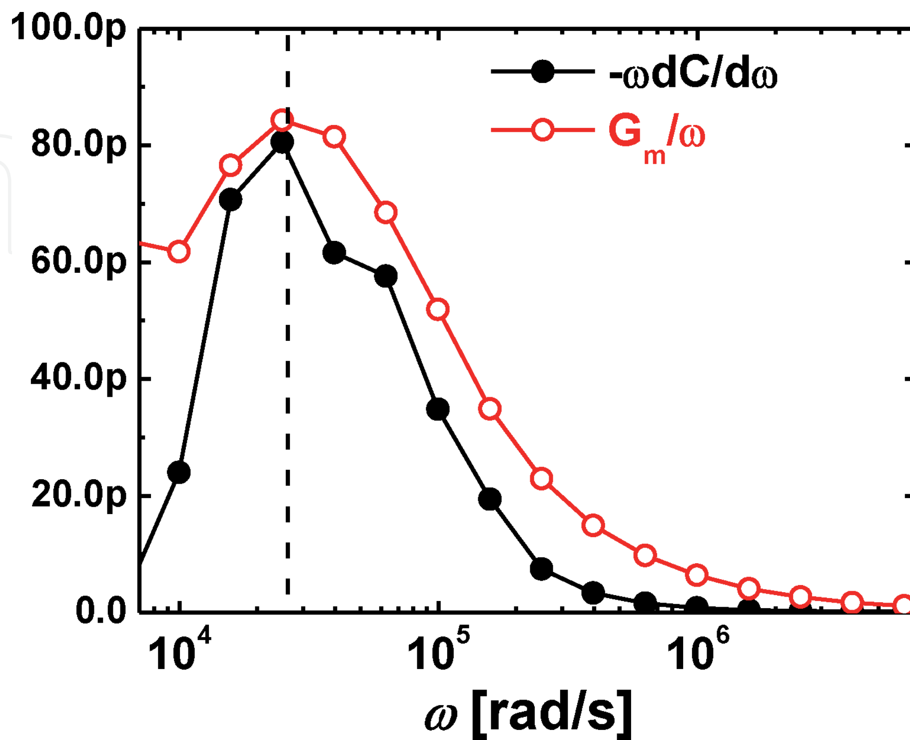

Figure 15.
–wdC/dw and G_m/w profiles for IPA-HfON/InGaAs MOS.

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4. Conclusions

In order to achieve both low EOT and low D_{it}, a highly advanced gate stack, prepared by using an IPA oxidant in the PA-ALD of HfO_xN_y on $In_{0.53}Ga_{0.47}As$ substrates, was proposed and showed the most outstanding results. A cyclic nitrogen low-power plasma step was added within the ALD cycles to passivate the oxygen vacancies uniformly without causing damage or surface degradation in comparison to the post deposition nitridation technology. Remarkable mid-gap D_{it} levels with strong inversion characteristics were achieved which has not been reported in the previous HfO_2/InGaAs interface studies. The improved interface characteristics can be attributed to both low surface oxidation ability of IPA and suppression of oxygen diffusion by effective nitrogen passivation to oxygen vacancies in HfO_2. The proposed ALD HfO_xN_y was fully characterized by investigating different dopant types and measurement temperatures. The results show comprehensive understanding on the interface defect density distribution. It is suggested that not only surface treatments but also the development of an advanced HfO_2 ALD process has a great impact on the quality of the III-V MOS interface and the IPA-based HfON interfacial layer might have great potential in future technology node.

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