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PAOD: a predictive approach for optimization of design in FinFET/SRAM

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ABSTRACT

The evolutions in the modern memory units are comeup with FinFET/SRAM which can be utilized over high scaled computing units and in other devices. Some of the recent systems were surveyed through which it is known that existing systems lags with improving the performance and optimization of FinFET/SRAM design. Thus, the paper introduces an optimized model based on Search Optimization mechanism that uses Predictive Approach to optimize the design structure of FinFET/SRAM (PAOD). Using this can achieve significant fault tolerance under dynamic cumpting devices and applications. The model uses mathematical methodology which helps to attain less computational time and significant output even at more simulation iteration. This POAD is cost effective as it provides better convergence of FinFET/SRAM design than recursive design.

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1. INTRODUCTION

The use of miniature circuits in veriety of electronic and electrical device is rapily growing and hence concern towards memory utilization of SRAM [1]. The SRAM provides simple operation, accessibility and high speed process but its size and cost are the concerning issues [2], [3]. The cost of SRAM usage is greater than DRAM as it occupies more space than DRAM. Hence, the transistor design of FinFET is more studied for SRAM [4]. However, FinFET/SRAM also exhibits area, stability, output, access time, power consumption, etc issues [5], [6]. Other modeling like double gated, back gated design, designs with dynamic feedback were discussed in recent past for FinFET/SRAM design [7], [8]. It is observed that most of the design methodologies were hardware-based approach as well as prototyping but there exist some open-end problems and are not solved i) predictive design model of FinFET/SRAM is introduced to offer better performance with accuracy, ii) existing studies have narrowed scale of implementation error which doesn't seem to offer fault tolerance to the SRAM design, iii) least works were carried out to jointly study the impact of design on output, energy, and memory units response. Thus, a better design optimization is not found from the literature which motivates the research community to have futuristic design optimization of FinFET/SRAM. This manuscript presents a predictive Approach for Optimization of Design in FinFET/SRAM. The manuscript is categorized as: Section 2 presents existing research work and problem identification in Section 3. Proposed methodology is given in Section 4 and elaborated discussion of algorithm implementation in Section 5. The accomplished outcomes were analyzed with comparative analysisis represented in Section 6 followed by conclusion in Section 7.

1.1. Background

The existing system on SRAM is presented in (Girish and Shashikumar [9]) is presented and identified certain set of problems of cost optimization that was addressed in most recent implementation (Girish and Shashikumar [10]). This section discusses approaches towards enhancing performance of FinFET/SRAM. The work of Bhattacharya and Jha [11] addressed the problem of stabilization of its reading operation using monolithic integration approach. Study toward identification of errors in SRAM by Fang and Oates [12]. Chen *et al.* [13] have introduced a technique for facilitating an effective writing operation for reducing the supply voltage. Yang *et al.* [14] addressed the problem associated with near-threshold based operation improving the reading performance. Karl *et al.* [15] has developed a prototype design of SRAM emphasizing on collapsing voltage for minimizing energy consumption during write operation. Zhang *et al.* [16] have performed optimization using dopant over their prototype of SRAM targeting as scaling the voltage factor. Kulkarni *et al.* [17] have adopted an amplification technique for enhance sensing performance in FinFET. Hu *et al.* [18] have presented SRAM design with better improvement over noise for improved performance of reading and writing operation. Bhattacharya and Jha [19] have presented a synthesis-based approach for accelerating the process of extracting the capacitance factor for a given layout arrays of SRAM. The technique also introduces an exclusive partitioning process for better efficiency. Song *et al.* [20] have presented a scheme for addressing the power issue in 128 mb of SRAM focusing on multiple density factors. Mishra and Mahapatra [21] have carried out a simulation-based approach for investigating the stability problems associate with SRAM. This work is reported to offer fault tolerance operation however their approach was limited to only normal operating conditions of circuits. Asenov *et al.* [22] have presented a unique approach of design optimization considering variability factor in the simulation study. The work carried out by Joshi *et al.* [23] has investigated variability of devices with respect to the SRAM using statistical approach. Mounica and Ganesh [24] have illustrated about new NVSRAM circuit that generates superior "instant-on operation" related to previous methods used in SRAM's. Riyadi *et al.* [25] have demonstrated the influence of gate material and process on subthreshold performance of junctionless FET, by comparing four sets of gate properties and process methods. All the above existing approaches do not address the design optimization problem of FinFET/SRAM and hence offers a broader scope of carrying out a research work.

1.2. The problem

After reviewing the existing approaches towards FinFET/SRAM design, good amount of research using hardware platform were found but none of these works have given optimal throughput and improved performance. Hence, existing approaches couldn't offer fault tolerance as they were no much standard computational model with an extensive analysis to prove it. Moreover, the memory units and their respective communication with other connected memory units have not been investigated in past ith respect to memory and power that is significant degraded in the upcoming design of chip multiprocessor. Therefore, the problems statement is "*design a system which can balance multiple aspects like power consumption, increased output, and faster processing*."

2. PROPOSED METHODOLOGY

The proposed system a predictive Approach for Optimization of Design in FinFET/SRAM to enhance the throughput performance. The following Figure 1 gives proposed system architecture.

The proposed system introduces three different functionalities of FinFET/SRAM which when combined with internal memory should offer maximum throughput without any dependencies of increasing resources. A novel mechanism of search-based optimization scheme is applied that considers various operations of SRAM, formulates an objective function, whose process is controlled by a novel cut-off function in order to achieve convergence. The next section briefs about algorithm implementation.

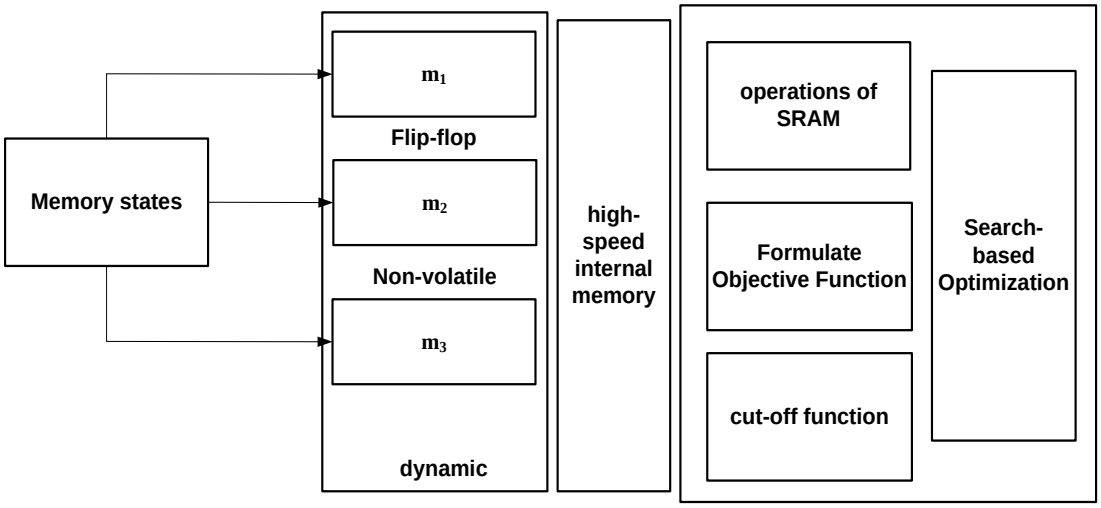

Figure 1. Implemented system scheme

3. ALGORITHM DESIGN

For a memory unit to be fault tolerant, it is necessary to ensure that it can cater up all the situation of resource utilization and querying process. It is also necessary to ensure how each memory units communicates with each other in order to accomplish the processing task. Therefore, the formulation of the proposed system is carried out for multiple states of memory corresponding to FinFET/SRAM. The proposed algorithm introduces a novel search-optimization-based predictive approach where the input to the algorithm are m1, m2, m3 (different memory), α (operations of SRAM), γ (high speed memory (internal)), σ (memory units), τ (cut-off function), pdef (defined parameter) and final outcome is accomplishment of converging point. The incorporated steps of the algorithm are:

Algorithm for design optimization of FinFET SRAM

Input: m_1, m_2, m_3, α, γ, σ, τ, p_{def}
Output:converging point
Start
1. *init* → m_1, m_2, m_3
2. Set $f_{obj}(x) \rightarrow \sum_{i=1}^{5} \alpha$
3. form Matrix β=[m_{prime}, M_{onchip}]
4. arrange $\beta=\gamma(m_1, m_2, m_3)$ in σ
5. compute τ=abs{H}
6. While τ is not achieved do
7. Forp=0 to μ
8. randSelect(p_{def}) from μ
9. $r_{adap} \rightarrow g(\tau)$
10. End
11. Assess all outcomes and shortlist best
12. End
13. Convergence achieved
End

The algorithm focuses on coupling of SRAM memory states by considering high speed internal memory for speeding up the computation process. The variables m1, m2, and m3 correspond to higher capability of memory (Line-1). The algorithm also formulates an objective function to ensure design optimization. The proposed algorithm formulates an objective function "fobj(x)" which has dependency of 5 parameters of operations of SRAM i.e. α1, α2, α3, α4, and α5 corresponds to i) reading operation in local memory along with its cost, ii) writing operation in local memory with its cost, iii) reading operation of remote memory along with its cost, iv)writing operation of remote memory along with its cost, and v) cost of making the data go mobile from one to another memory segment (Line-2). The matrix β is created which maintains two forms of memory i.e. prime memory (Mprime) and on chip memory (Monchip). The next step

defines a function γ (high speed memory) where the memory elements are going to be structured for direct accessibility when queried for allocation (Line-4). This step impacts on positive energy saving and balanced allocation of necessary resources. The algorithm than initiates begin its search optimization for obtaining better convergence point of design. For this, we apply a novel formulation of a cut-off function τ that we choose to compute instead of initializing like in majority of studies in existing system. The computation of the cut-off function is carried out by computing a matrix H which depends on cumulative state of memory and cost function (Line-5). The complete evaluation is also dependent on cardinality of data items as well as cost of data as well. Line-6 to Line-12 corresponds to proposed search optimization scheme with an intention to obtain better convergence point of design of SRAM. The initial step in this search-based optimization is to perform random selection of population, where population is a set of all best possible outcomes of resource allocation policies of FinFET/ SRAM. The proposed system will apply a greedy approach in order to perform random selection of populationμ (Line-8). The next step is to apply a function g on cut-off function (Line-9), which corresponds to replicate behaviour with adaptive approach radap. This process is enhancement on the prior population extraction where it offers formulating more elite outcome from a set of one of more elite population. The computation of the function g(τ) mainly depends on maximum value τmax, best value τbest, and average value of cut-off function τavg and is empirically represented as,

$$g(\tau) = c.\frac{\tau^{p}}{\tau^{q}} \tag{1}$$

Where the notation τp and τq corresponds to (τmax- τbest) and (τmax- τavg) respectively. The variable c represents system matrix whose values depends on final application to be designed and hence could be configured likewise. The prime idea of this search optimization is to assess the presence of sufficient resource for allocation of particular memory units in FinFET/SRAM. It also has the capability to assess its adjacent cores of memory units and easily localize certain units. Such approaches are not seen in any existing approach for design enhancement of SRAM. The final step of search optimization includes resisting of the accomplishing the convergence point. We define convergence point as an instance of an outcome where minimal resource is used to obtained better yield of SRAM that is more capable of making it fault tolerant. Therefore, the final step of proposed algorithm is to performing sorting and to check for the best values of the outcome. The process is continued until and unless all the populations μ are checked (Line-11 and Line-13). An interesting fact to see for is the process of swapping the memory unit with each other in order to cater up the dynamic job requirements. This process results in building more capability to the FinFET / SRAM for exhibiting better convergence performance with less inclusion of memory parameters. Hence, this proposed optimization technique will also ensure better energy conservation scheme as well as it also has the capability to minimize and control of leakage power. At the same time, the proposed algorithm encourages progressive steps and not iterative steps, for which reason computational burden is kept within a specific limit. The next section outlines the results being obtained.

4. RESULTS DISCUSSION

The MATLAB is used for simulation over 6-bit machine of windows platform. A hypothetical task is generated to assess the memory factor with respect to throughput and response time. The test platform uses core i3 process of 2GHz frequency. The baseline memory states m1, m2, and m3 are configured with multiple energies of 0.2nJ-20nJ, 0.5ns-20ns and 2mW-100mW for access operation, delay and leakage power respectively. The system outcomes using Search Optimization (SO) is compared with Particle Swarm Optimization (PSO).

Figure 2 highlights that proposed system of SO offers better throughput performance in contrast to PSO based approach. The prime reason for this trend is – PSO based design optimization scheme offers iterative process to obtain the elite outcome of convergence. This causes increase in latency owing to excessive read-write operation resulting in maximum resource allocation. Hence, PSO based schemes offers fault tolerance for only lesser iteration. In the meanwhile, proposed SO-based scheme offers a progressive exploration process where the all the cumulative outcomes are already defined and process of optimization narrows down the search process using a cut-off function and hence makes the process much progressive and less iterative. Normally, such optimization process is not witness in existing FinFET/SRAM design in any of the existing system and hence our proposed system can be said to offer better balance between the energy being depleted dring read-write operation.

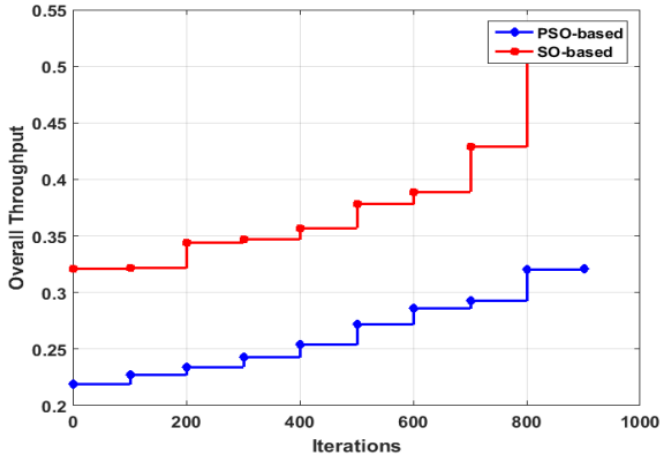

Figure 2. Comparative result of throughput

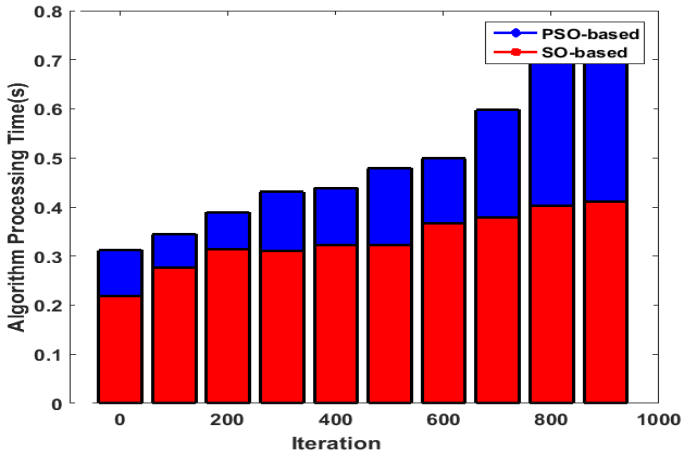

Figure 3. Comparative result of response time

A closer look into the proposed technique shows that it offers significant reduction of the write operation up to 35% and minimizes energy consumption to 20% approximately. Owing to adoption of randomized process of initiating a search, proposed algorithm performs faster operation which contributes to faster algorithm execution time. The second reason for faster response time is that proposed algorithm performs parallel search process of obtaining elite outcome of convergence point. This cut downs the computational time to 50% and is quite useful for handling massive and dynamic task. At the same time, greedy mechanism further simplifies the process of initiating and managing the search depending on the best value of the cut-off function that consistently updates it. The computational complexity in Figure 3 of the proposed system is therefore very less and it has nearly uniform trend, which makes the performance quite predictive for the proposed system.The outcome of graphical trend therefore exhibits that proposed system offers better throughput performance measured with respect to probability that could suit well to any form of applications using FinFET/SRAM with less energy consumption, more yield, and faster computational time. It is best suitable for upcoming designs of registers with high speed operation, sophisticated smart phones with advanced mobile networks, buffer management in n-based routers, etc.

5. CONCLUSION

The proposed system introduces three different roles of SRAM in the form of memory units aiming to to minimize the energy depletion and other issues concerning with the latency. The proposed technique gives a an optimized model based on Search Optimization mechanism that uses Predictive Approach to optimize the design structure of FinFET/SRAM (PAOD). The implementation of system is a computational

model that suits well with any computational environment. The study outcome shows that proposed system offers better response and higher throughput.

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