

DC performance analysis of a 20nm gate length n-type Silicon GAA junctionless (Si JL-GAA) transistor

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ABSTRACT

With integrated circuit scales in the 22-nm regime, conventional planar MOSFETs have approached the limit of their potential performance. To overcome short channel effects 'SCEs' that appears for deeply scaled MOSFETs beyond 10nm technology node many new device structures and channel materials have been proposed. Among these devices such as Gate-all-around FET. Recently, junctionless GAA MOSFETs JL-GAA MOSFETs have attracted much attention since the junctionless MOSFET has been presented. In this paper, DC characteristics of an n-type JL-GAA MOSFET are presented using a 3-D quantum transport model. This new generation device is conceived with the same doping concentration level in its channel source/drain allowing to reduce fabrication complexity. The performance of our 3D JL-GAA structure with a 20nm gate length and a rectangular cross section have been obtained using SILVACO TCAD tools allowing also to study short channel effects. Our device reveals a favorable on/off current ratio and better SCE characteristics compared to an inversion-mode GAA transistor. Our device reveals a threshold voltage of 0.55 V, a sub-threshold slope of 63mV / decade which approaches the ideal value, an Ion/Ioff ratio of 10e + 10 value and a drain induced barrier lowering (DIBL) value of 98mV/V.

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1. INTRODUCTION

Today, a large part of the world economy is owned by the electronics industry. In 1958, integrated circuit concept was introduced by J. Kilby. A few years later, in 1965 [1] Gordon MOORE enunciated his law explaining that the number of transistors on a chip will double every 18 months. With MOSFETs miniaturization the integration density increased allowing to reduce significantly manufacturing costs. Hence, reduction of conventional MOSFETs dimensions has reached its limits because of the appearance of unpleasant effects called "short-channel effect" [2-8] that became very pronounced. In order to reduce these issues a new MOSFET architectures have been developed. These new multiple gate devices also called MUGFET have been extensively studied. This multiple gate devices that replace the conventional MOSFET are : Double-gate, Triple-gate, Pi-gate, Omega-gate, Surrounding gate (square and cylindrical gate-all-around), and finally junctionless FET [9-11] also referred to as junctionless gated resistor that has simpler and less number of fabrication steps than the conventional MOSFETs.

Junctionless transistors are variable resistors that are controlled by the device gate electrode. The silicon channel is a heavily doped nanowire that can be fully depleted to turn the device off. The device

electrical characteristics are the same to normal MOSFETs ones, but the physics is dissimilar. The very first Junctionless transistor has been proposed by Lilienfeld in 1925, but was remained as an idea and was regrettably never fabricated. In 2010, the first JLT was effectively fabricated by J.P. Colinge. In 2011, Choi et al. have conceived a 50 nm gate length gate GAA JLT architecture fabricated on silicon. Later, an N-channel JLT GAA with heavily doped poly-silicon nanowire channel has been reported by Su et al. Zhao et al studied in 2011 a P-type JLT device on Germanium-on-insulator. Dr. A Kranti, J P Colinge and their research group have detailed the design guidelines of such a structure, see Figure 1 [12].

The junctionless transistor is a very promising Metal-Oxide-semiconductor field effect transistor architecture based on a single type (N+N+N+ or P+P+P+) doping of source, drain and channel [13-15]. Junctionless FET represents an innovative class of field effects devices having no abrupt doping junctions. As cited before, the basic structure of a junctionless transistor consists of a uniformly highly doped channel that is controlled by the device gate electrode. This no-junction device is basically a resistor in which the mobile carrier density can be modulated by the device gate. Unlike its conventional MOSFET counterpart, the JLT offers diverse advantages such as : a simpler manufacturing process, a reduced propagation delay, a low electric field at ON state [16], volume conduction (in bulk), improved mobility and insensitive to gate / channel interface effects [15], dynamic power dissipation, and faster switching. It has been shown that the ideal MOSFETs threshold slope obtained is equal to 60 mV / decade actually; manufactured devices can not achieve this value due for exemple to the influence of interface traps. However, the conduction mechanism in the junctionless transistor is based on volume conduction leading its threshold slope to approach the ideal threshold slope value [9].

Different works have been presented studying JLT devices such as bulk planar JLTFET [16], single gate silicon-on-insulator (SOI) JLFET [15], multi-gate nanowire junctionless transistors[17], gate-all-around nanowire junctionless transistors [18], as well as junctionless tunnel FET [19]. Our study allows us to design a 3D GAA junctionless transistor with rectangular cross section using ATLAS SILVACO software. 3-D bohm quantum potential (BQP) transport device simulation has been used to evaluate the conceived device performance allowing considering quantum effects. In this work, SCEs of our conceived JLT GAA are also investigated.

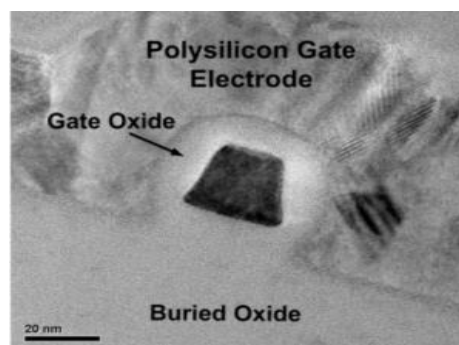


Figure 1. TEM cross section of a JLT nanowire transistor [12]

2. DEVICE DESCRIPTION

MUGFET transistors are further characterized based on the doping of their source, drain and channel regions. The performance variations of JL-GAA FETs strongly depends on doping concentration where the ultrathin active silicon film doping must be as much as necessary high in order to achieve an appropriate source/drain series resistance as realizing efficient volume depletion. Usually, there are three main conduction mechanisms in multigate FETs from the doping prospective. That are inversion, accumulation and partial depletion mode, where the source, drain and channel regions are doped as N+P N+, N+N N+ and N+N+N+ respectively. The inversion and accumulation mode transistors [14], [20]–[22] are the standard MOSFETs based on the formation of PN or Schottky junctions where the drain is initially reverse biased to restrict any current flow in the channel region unless a sufficient gate voltage is being applied to create an inversion layer to provide a way for the carriers to flow between the source and drain regions. Hence these transistors are normally off and after the inversion layer being created, the current flows and the transistor turned on.

Figure 2 shows the energy band diagram for an n-channel junctionless transistor, here we assume a P+ polysilicon gate electrode. Flat-band condition is achieved while a positive gate bias equal to

the workfunction difference between the nanowire and the gate material is applied to the gate of the device as shown in Figure 2 (a). When a zero gate bias is applied, the channel region is fully depleted as shown in Figure 2 (b).

The JL-GAA device is studied using 3-D Silvaco TCAD simulation. SILVACO can analyze and predict the behavior of new devices, without the elevated cost required to manufacture the real components [23]. In order to highlight the ameliorations in performance made by the JL GAA devices compared to GAA ones, these two structures are studied. Figure 3 shows the 3-D n-channel Junctionless Gate-All-Around structure with a rectangular cross-section conceived and studied in this work. The gate length L_g , is fixed at 20 nm according to ITRS specifications for the technology node used. As shown in Figure 3 (b) a refined meshing has been used in our device channel region and a less refined meshing is used in the other regions, to optimize the time of device characteristics simulation. The studied JLT GAA and GAA cross-sections are shown in Figure 4. Figure 4, allows to spotlight the difference between the GAA and GAA JLT where for junctionless transistor channel, source and drain are uniformly highly doped. All parameters details for our simulated JLT GAA are given in Table 1.

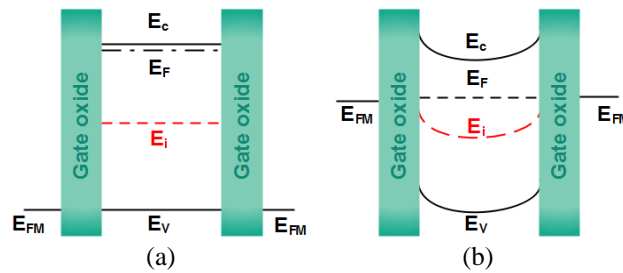


Figure 2. Energy-band diagram for an n-channel Junctionless transistor in (a) flat-band condition (the device is turned on), (b) in off state (the channel region is fully depleted)

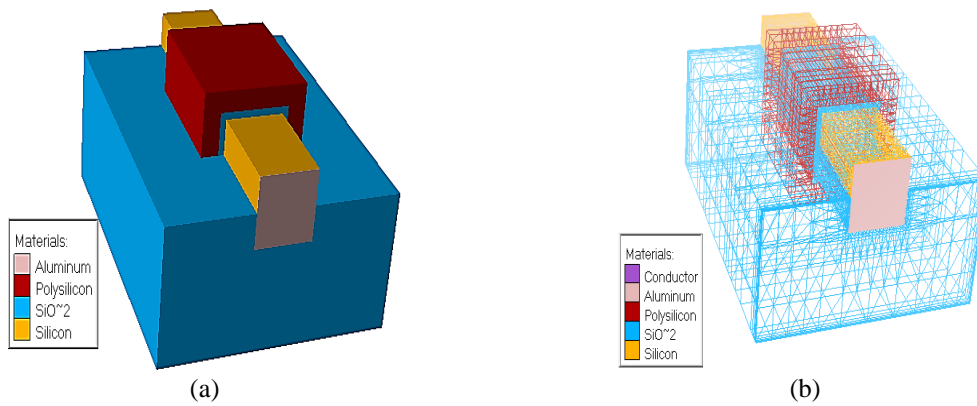


Figure 3. (a) Device structure of n-type GAA and GAA-JLT, (b) meshing structure of n-type GAA and GAA-JLT

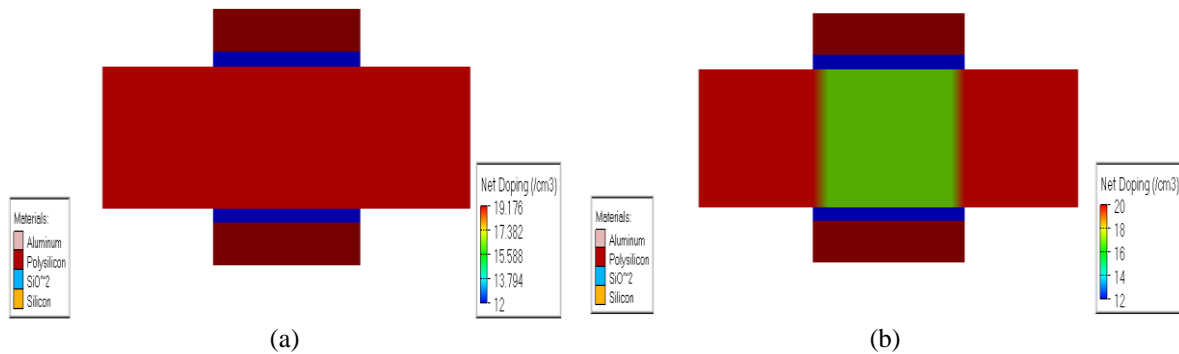


Figure 4. Cross-section of GAA MOSFET with doping concentration (a) JL GAA, (b) GAA

Table 1. Device Parameters of JL GAA

Device Parameters	JL GAA (N+N+N+)
Gate length	20nm
Channel width	10 nm
Channel height	10 nm
Gate oxide thickness	1 nm
N-Channel concentration level	1.5e+19
Buried oxide layer thickness	20 nm

3. RESULTS AND DISCUSSION

In this section, DC performance parameters of the studied Junctionless GAA are presented, allowing to enumerate our device characteristics such as its on-state current, its threshold voltage, the DIBL, Sub-threshold slope (SS) and I_{on}/I_{off} ratio. Our results have been obtained using ATLAS SILVACO software where quantum effects have been considered to describe accurately the electrical behaviours of all nanoscale devices and to assess their performance limits.

The on-state current drive of the junctionless transistor is given by [14] :

$$I_{DSat} \approx q\mu N_D \frac{T_{ch} W_{ch}}{L} V_D \quad (1)$$

$$V_{DSat} = V_G - V_{Fb} - \left(\frac{qN_D T_{ch}}{2\epsilon_{ch}} + \frac{qN_D T_{ch}}{C_{ox}} \right) \quad (2)$$

N_D is the doping density, T_{ch} and W_{ch} are the channel thickness and width respectively, V_D is the drain voltage, L is the gate length, ϵ_{ch} is the relative permittivity of the channel material and C_{ox} is the gate oxide capacitance. $I_{DS}-V_{DS}$ characteristics of the studied n-channel JL-GAA under different supply voltage V_{GS} levels are reported in Figure 5. $I_{DS}-V_{GS}$ characteristic is reported in Figure 6.

The junctionless gate all around transistors are practically fully depleted by regulating the work function of gate material at OFF-state. This device needs reasonably high doping for relatively a high drive current at ON-state. We can see that our device shows an excellent electrostatic control with relatively high ON-state current and low OFF-state one leading to a high I_{ON}/I_{OFF} ratio.

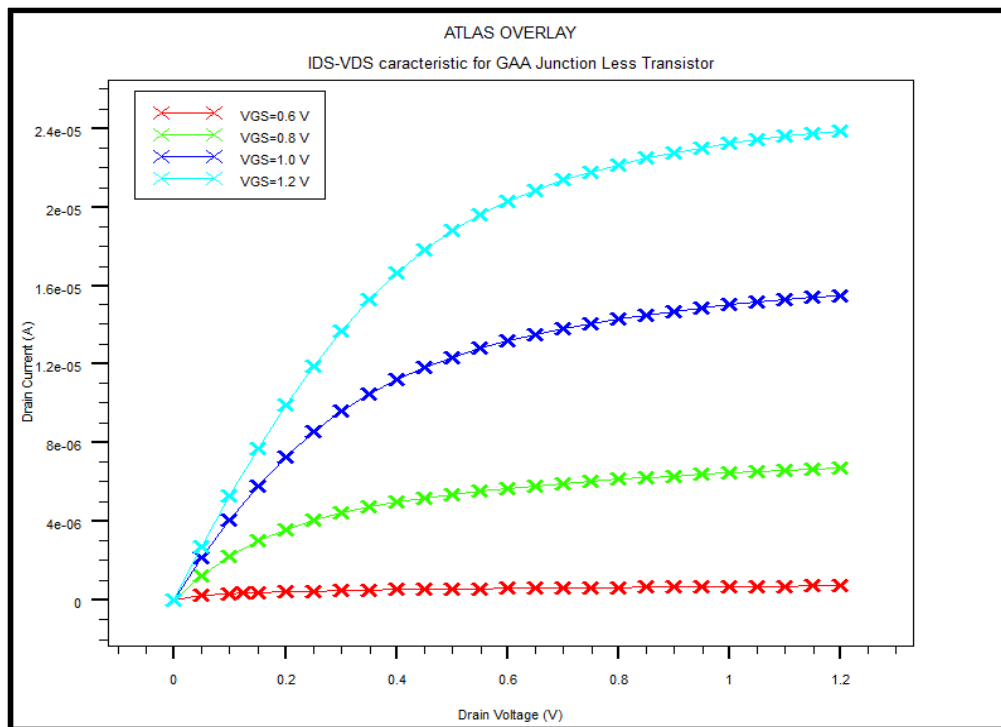


Figure 5. Output characteristics of GAA Junctionless transistor

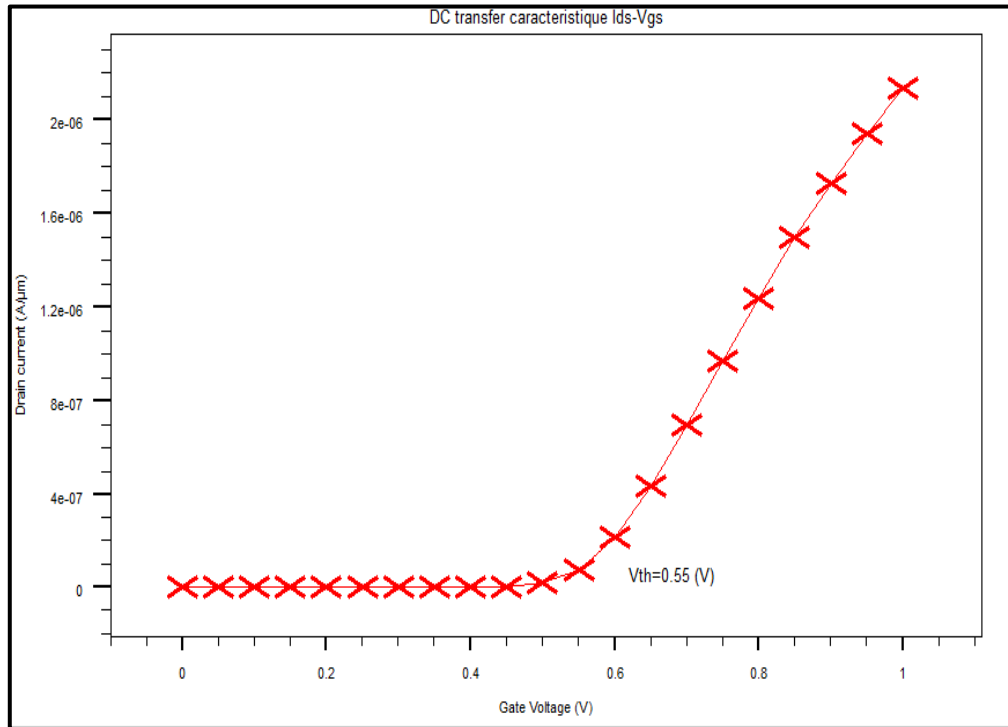


Figure 6. Transfer characteristics of GAA Junctionless transistor

3.1. Threshold voltage (V_{th})

The threshold voltage is the gate voltage at which the magnitude of diffusion current equals drifts current and transistor turns on. The expression of V_{th} is given by [24]:

$$V_{th} = \phi_{MS} - qN_D \left[\frac{WH}{C_{ox}} + \frac{1}{\epsilon_{ch}} \left(\frac{WH}{2H+W} \right)^2 \right] + \frac{\pi^2 \hbar^2}{2qm^*} \left[\frac{1}{H^2} + \frac{1}{W^2} \right] \quad (3)$$

where ϕ_{MS} is the metal-semiconductor work function, N_D is the carrier doping concentration, W and H are the channel width and height respectively, ϵ_{ch} is the relative permittivity of the channel material, C_{ox} is the gate oxide capacitance, m^* is the effective mass and h is the Planck's constant. The GAA JL transistor for our simulation turned on at $V_{th}=0.55$ V as shown in Figure 5. Our results allow to observe that we have obtain an appropriate V_{th} due to the P++ doping polysilicon gate used.

3.2. Drain-induced-barrier-lowering (DIBL)

The DIBL is one of many short channels effects. It is attributed to the electrostatic influence of the drain on the barrier height of injection barrier. By increasing the drain voltage V_{DS} , there is expansion of the space charge area at the drain. This space charge area can reduce the height of the injection barrier. The DIBL is given by [25] :

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{DS}} \quad (4)$$

The DIBL for the MOSFET devices is generally higher than 100mV/V for the gate length less than 50 nm [25]. For our device the DIBL = 98.3 mV/V as shown in Figure 7 for gate length 20 nm. This relatively low value is due to the absence of junction in JL GAA Transistor [26].

3.3. Sub-threshold slope (SS)

The SS is another parameter of short channel effects to estimate the sub-threshold characteristics "SS" of nanoscale short channel MOSFET devices [27]. SS determines the efficiency of a transistor to switch from its off-state to its on-state. It is defined as [14]:

$$SS = \frac{\delta V_{GS}}{\delta(\log I_{DS})} \tag{5}$$

As shows in Figure 8 the SS of our GAA JL transistor is low (< 80mV/dec) and is equal to 63mV/dec at room temperature.

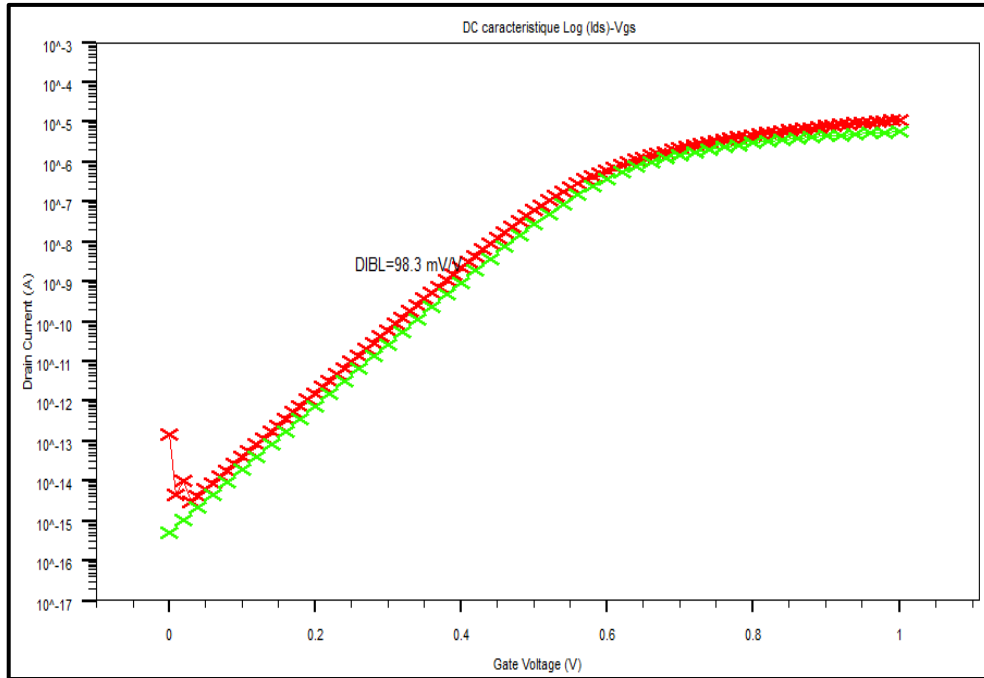


Figure 7. Transfer characteristics log(I_{DS}) vs V_{GS} of GAA Junction Less transistor at different value of V_{DS}

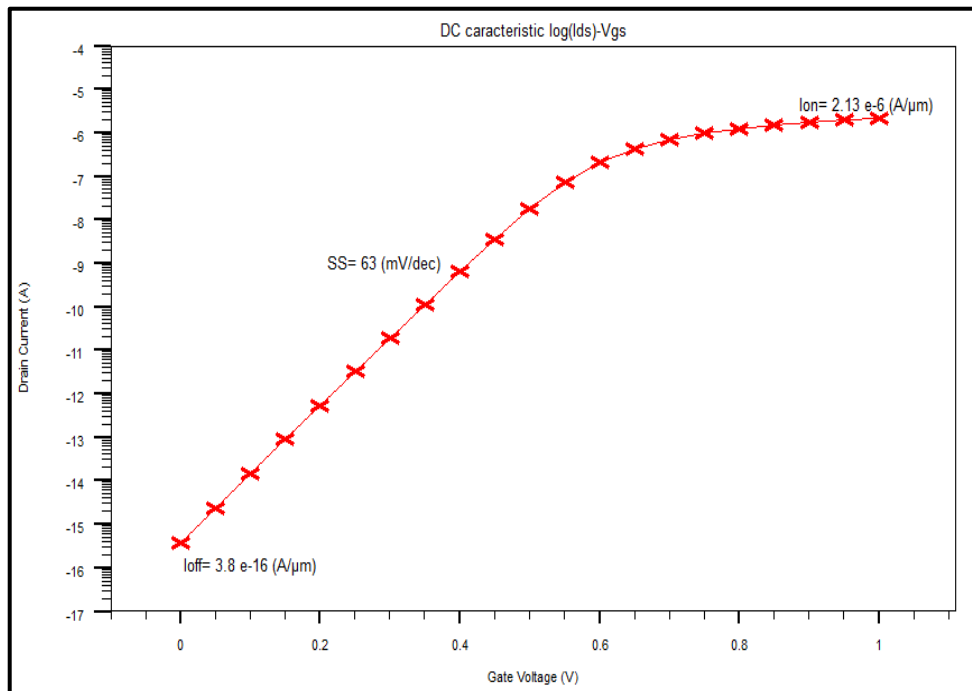


Figure 8. Transfer characteristics log(I_{DS}) vs V_{GS} of GAA Junction Less transistor

3.4. I_{on} , I_{off} and I_{on}/I_{off} ratio

The on-state current (I_{on}) is defined as the value of the drain current (I_D) at high value of V_{GS} with a constant V_{DS} voltage. The off-state current (I_{off}) is defined as the value of the drain current (I_D) at low value of V_{GS} and constant V_{DS} [28]. For JLT devices and in the on-state, there is a large body current. This body current is due to the doping concentration in the channel that is relatively high, to which surface accumulation current can be added. In an other hand, in the off-state the device channel is turned off by depletion of carriers and this is in fact due to the difference in workfunction between the material of the device gate and the semiconductor. Indeed, in JLT devices, the doping has to be high enough for obtaining a suitable current drive and the cross section of JLT devices has to be sufficiently small to be able to turn the device off. More gate control leads to more I_{on}/I_{off} ratio which represents high performance (high I_{on}) and low leakage current (low I_{off}) for the CMOS transistor, Typically it is around $10^6 \sim 10^{10}$. Any decrease in I_{on}/I_{off} ratio can cause slow output transitions or low output swings. For our device the $I_{on}/I_{off} \approx 10^6 \sim 10^{10}$. All the results obtained for our simulation are given in Table 2.

Table 2. Variation of the device electrical parameters

	JLGAA
DIBL (mV/V)	98,3
I_{on} (A)	2.13E-6
I_{off} (A)	3.8E-16
I_{on}/I_{off}	0.55E+10
SS (mV/dec)	63
V_{th} (V)	0.55

3.5. Comparative study of Si-JLT GAA and Ge-JLT GAA

In order to study the impact of channel material on the device characteristics Silicon and Germanium n-channel JL-GAA are presented. The output characteristics of these devices under different supply voltage V_{GS} levels are reported in Figure 9. The transfer characteristic is shown in Figure 10.

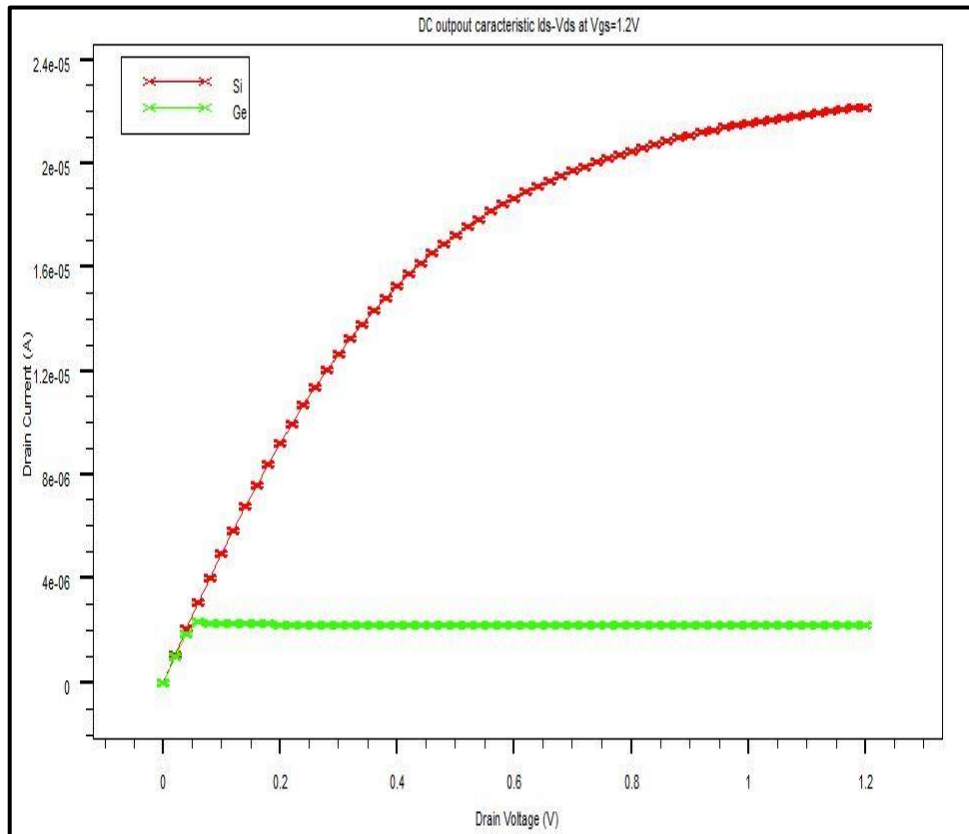


Figure 9. Output characteristics of Si and Ge GAA Junctionless transistor

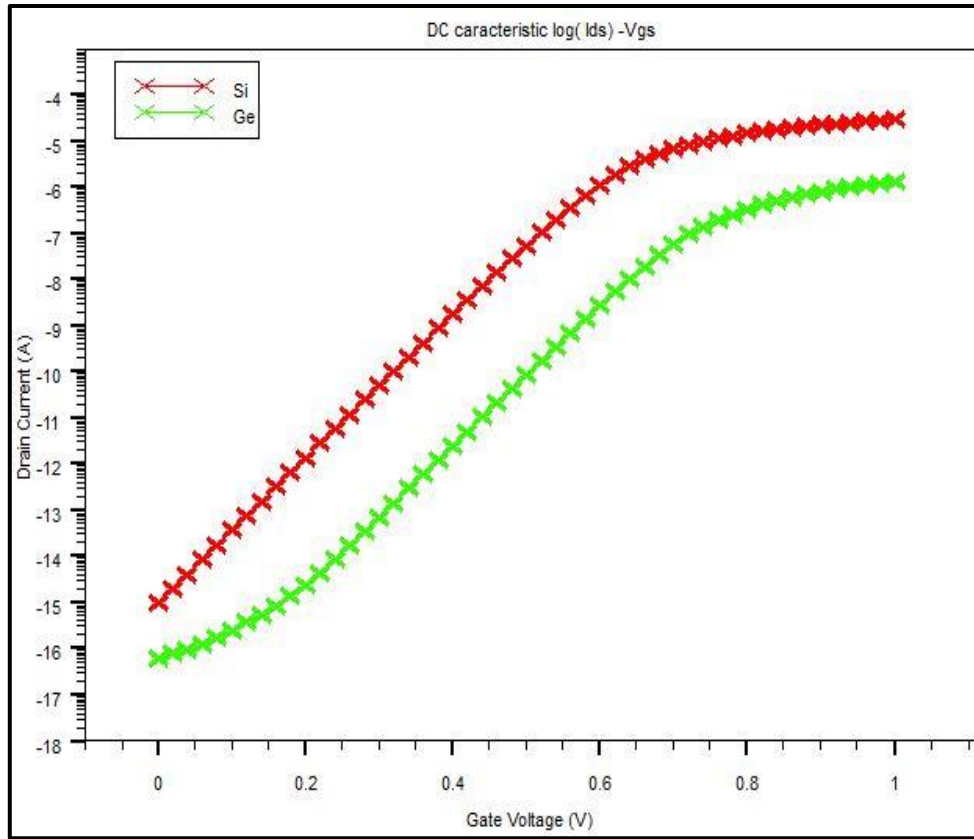


Figure 10. Transfer characteristics of Si and Ge GAA Junctionless transistor

The I_{on} current of a silicon n-channel JLT-GAA is about twice upper than I_{on} current of a germanium-channel JLT-GAA. DC performances of our two devices are given in Table 3. Our results allow us to confirm that silicon JLT-GAA have better DC performance compared to Germanium JLT-GAA. The leakage current of a germanium JLT-GAA is lesser than a leakage current of a silicon device. This result is due to the difference between the band gap energy of germanium and band gap energy of silicon ($E_{gGe} < E_{gSi}$). The I_{off} current is given by [29]:

$$I_{off} = I_0 e^{((V_{GS}-V_{th})/\eta U_T)} \tag{6}$$

η is a coefficient that expresses the sensitivity of the transistor control by the gate and I_0 is a current value at $V_{GS}=V_{th}$. The metal-semiconductor work function $\phi_{MS}(\phi_{MS} = \phi_M - (\chi_s + (E_g/2q) + \phi_F))$ depends on the band gap energy E_g . When E_g increases ϕ_{MS} decreases, threshold voltage V_{th} decreases and I_{off} increases. In Table 4 we summarize all our simulation results that we compare to some results found in literature. Our results are compared to some results found in literature. We can see that the results we obtained are in agreement with other results obtained for different JLT GAA devices, which indicates the good approach of our simulations.

Table 3. DC results obtained for Si and Ge GAA JLT

	Si-JLGAA	Ge-JLGAA
DIBL (mV/V)	98,3	11.2
I_{on} (A)	2.13E-6	1.31E-6
I_{off} (A)	3.8E-16	6.33E-17
I_{on}/I_{off}	0.55E+10	2.07E+10
SS (mV/dec)	63	64
V_{th} (V)	0.55	0.72

Table 4. Different results obtained for JLT GAA found in literature.

Structure	Simulation results obtained for our 20nm gate length JLT GAA		[14]	[26]	[30]	[31]	
	Si-JL-GAA	Ge-JL-GAA	JL-Multigate	JL-NW	JL-NW	Si-JL-DG	Ge-JL-DG
Lg (nm)	20	20	1000	50	20	20	20
W(nm)	10	10	30	-	10	10	10
DIBL (mV/V)	98,3	11.2	-	7	78	47	22
I _{on} (A)	2.13E-6	1.31E-6	-	-	1000uA/um	-	-
I _{off} (A)	3.8E-16	6.33E-17	1E-15	-	-	-	-
I _{on} /I _{off}	0.55E+10	2.07E+10	>>1E+6	-	5E+6	-	-
SS (mV/dec)	63	64	64	60	92	69.2	64.7
V _{th} (V)	0.55	0.72	-	-	-	-	-

4. CONCLUSION

In this paper, the DC device performance analysis of a 20nm gate length n-type JunctionLess transistor GAA with a rectangular cross section has been evaluated. This Junctionless transistor is a variable resistor controlled by a gate electrode. For this work, a 3-D Bohm Quantum Potential (BQP) transport device simulation has been used to evaluate the DC device performance. The studied device reveals a low sub-threshold slope SS=63 mV/decade, and a good current density 25mA/mm. The Junctionless device structure studied shows improved ON to OFF current ratio of about 10e+10 that can be observed from our results compared to GAA MOSFET because of reduced SCEs. In addition, our device shows lower SS and DIBL to those of the GAA device at gate length Lg of 20 nm. At the end of this study, we can observe that the DC behaviour exhibited by the proposed GAA JL device is very promising. Indeed, the junctionless improves the control of the gate on the channel allowing using this device in different applications.

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